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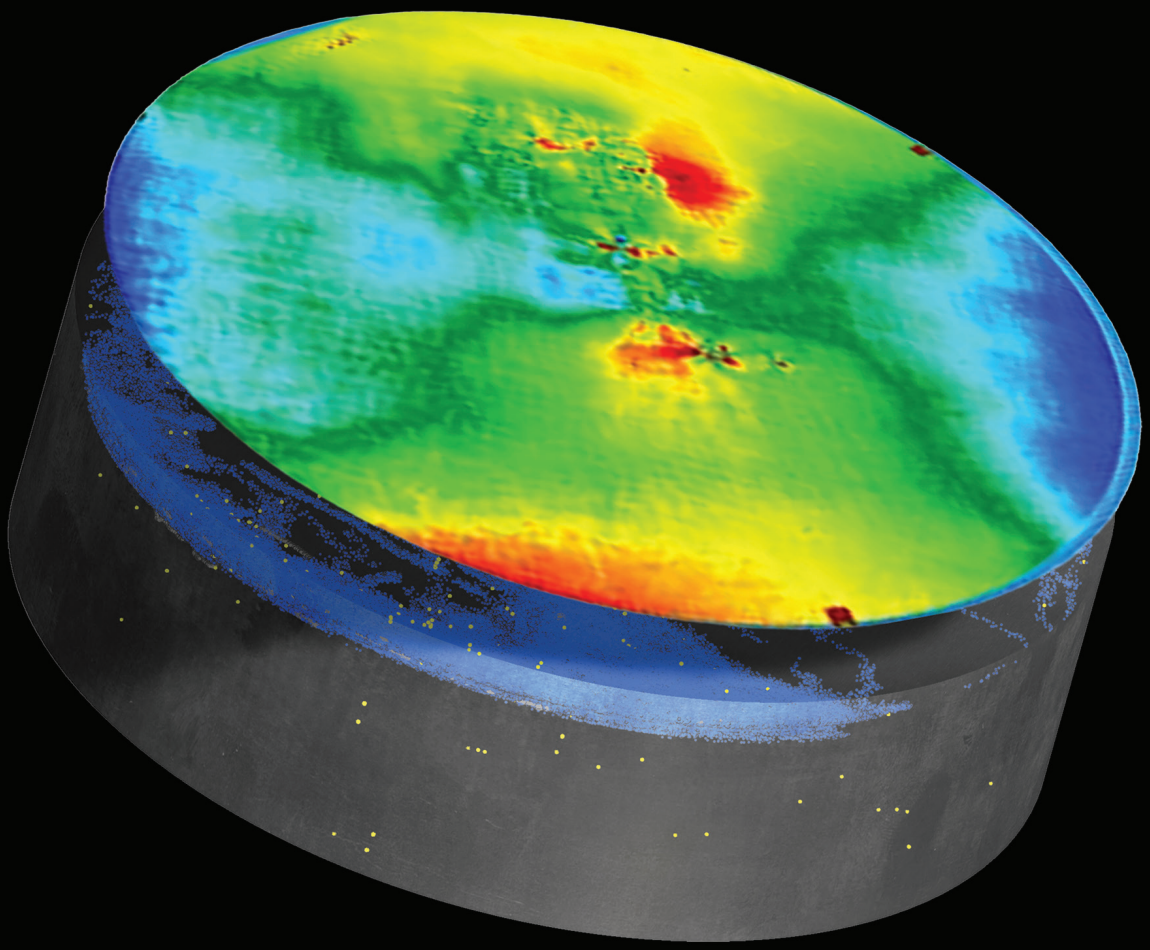

TAKING THE GUESSWORK OUT OF SiC PRODUCTION

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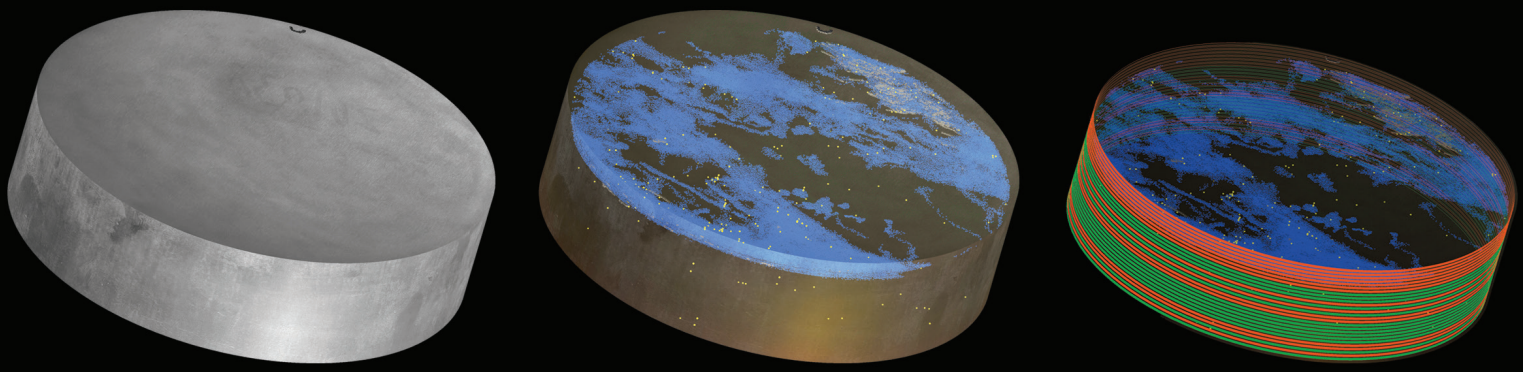

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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

Deep UV LEDs are shedding their feeble credentials

WHEN one thinks of deep-UV LEDs, it's easy to focus on the negatives – and there are plenty of them.

After all, these short-wavelength emitters are often impaired by a lattice mismatch that spawns light-quenching defects, and a low doping efficiency for holes that hampers carrier injection. And then there's the low extraction efficiency, particular troublesome at the very shortest wavelengths, due to a switch in the dominant direction for polarisation to transverse magnetic; and the need for novel forms of epitaxy to get the best out of these devices, even though this still produces a performance that falls well short of those for blue LEDs.

But while there is still a significant gap between the performance of UVC LEDs and their visible cousins, it's not quite the chasm it once was. Take the best 265 nm devices from ams Osram, slated to enter commercial production around this time next year (see p. 14). Their output power is 200 mW, realised at a wall-plug efficiency of just over 10 percent, and the lifetime is 20,000 hours, well beyond what's required in some applications.

During the pandemic, UVC LEDs attracted a great deal of attention as sources for killing Covid-19. Since then, interest has waned in using these emitters for disinfecting air and surfaces, and water treatment is once again seen as the biggest application by many – and certainly by those at ams Osram.

For all potential markets for the deep-UV LED, competition comes in the form of the mercury lamp. It's bulky, fragile, has a lifetime less than that of the best UV LEDs, and it takes several minutes to reach full power – but, and it's a big but, this incumbent is capable of producing a substantial output.

Due to the limitations of the mercury lamp, LEDs emitting at 265 nm – that's the sweet spot for germicidal effectiveness – are ideal for point-of-use applications. These sources can be fitted to taps, water dispensers, and the point-of-entry to one's home.

Where deep-UV LEDs face far stiffer competition is large-scale water treatment, associated with industrial and municipal applications, where the source is on all the time. Here the power of the solid-state source emitter is an issue, and gains are required to win market share.

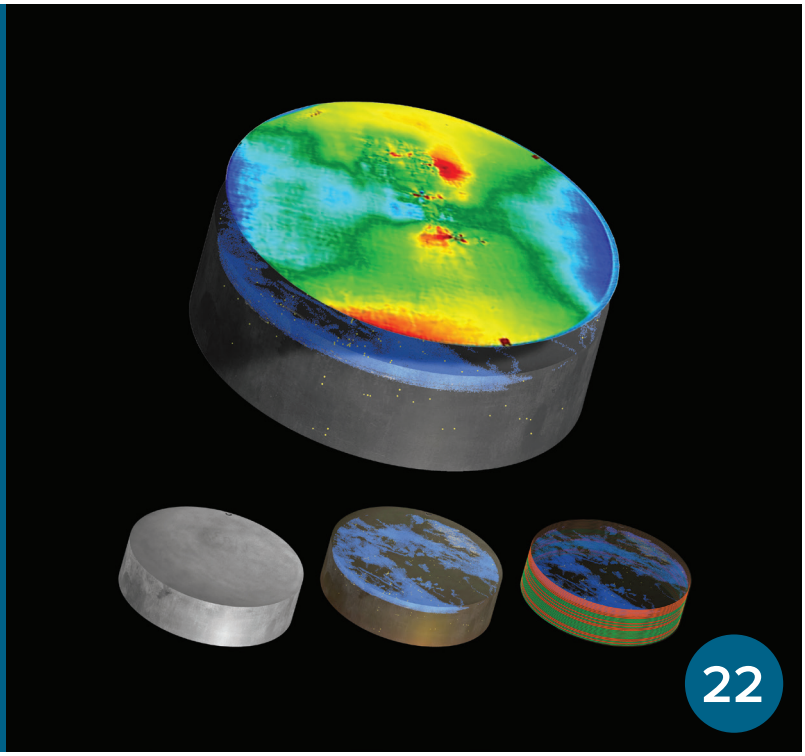
Based on the progress of all classes of LEDs, those emitting in the UVC are going to continue to increase in power, while offering a reduction in the cost-per-lumen. And while this market will only be worth a fraction of that of the general lighting market, it's yet another example of compound semiconductor devices aiding humanity's advances.

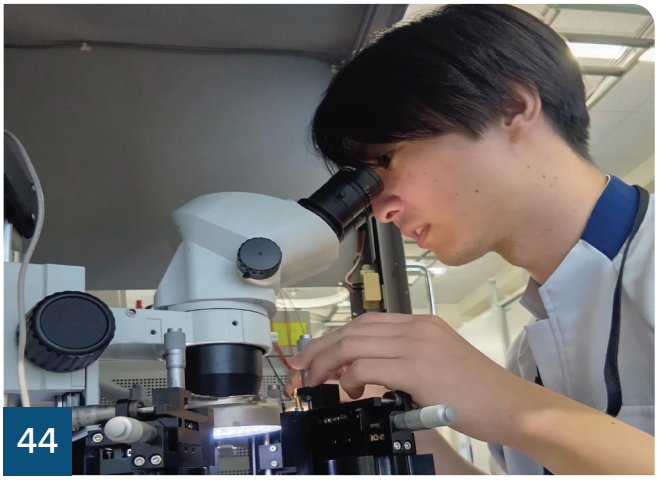
COMPOUND SEMICONDUCTOR

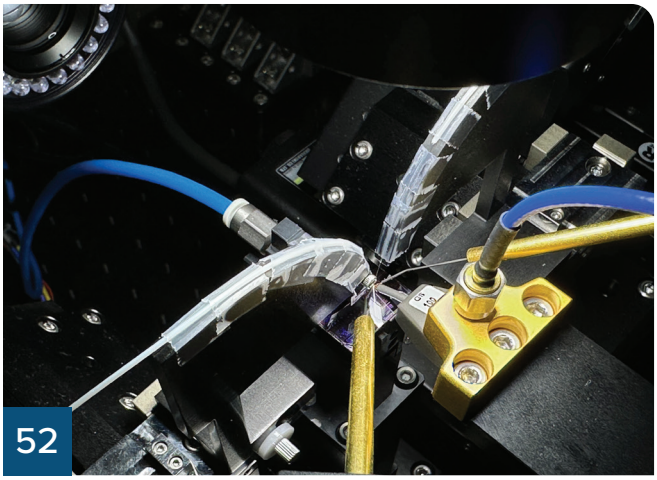
COVER STORY

Taking the guesswork out of SiC production

Thanks to advances in metrology, it's now possible to scrutinise a SiC puck before it's wafered and identify material defects that govern yield and profitability







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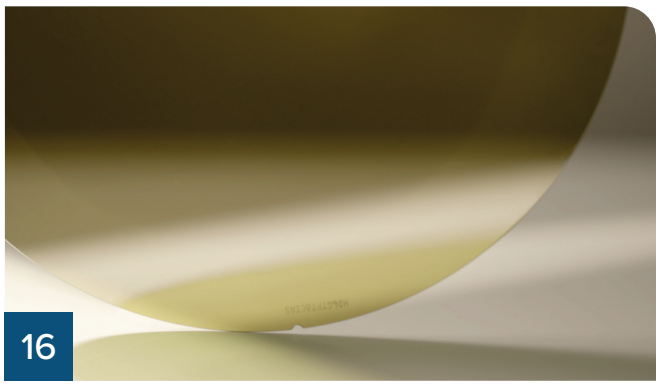

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Imec launches 300 mm GaN programme

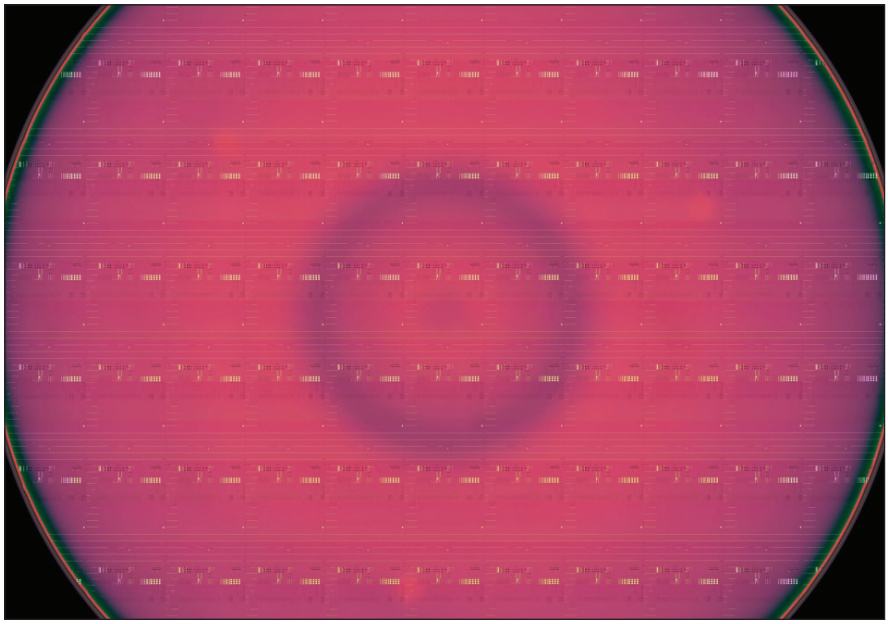
Aixtron, GlobalFoundries, KLA Corporation, Synopsys, and Veeco join imec's GaN power electronics program track on 300mm as first partners

IMEC, the Belgian research and innovation hub, has announced Aixtron, GlobalFoundries, KLA Corporation, Synopsys, and Veeco as first partners in its 300 mm GaN open innovation programme track for low- and high-voltage power electronics applications.

This programme track, part of imec's industrial affiliation programme on GaN power electronics, has been set up to develop 300 mm GaN epi growth, and low- and high-voltage GaN HEMT process flows.

As well as reducing GaN device manufacturing costs, the use of 300 mm substrates will also allow the development of more advanced power electronics devices, such as efficient low-voltage point-of-load converters for CPUs and GPUs.

Stefaan Decoutere, fellow and programme director of the GaN power electronics program at Imec: "The benefits of transitioning to 300 mm wafers go beyond upscaling production and reducing manufacturing costs. Our CMOS-compatible GaN technology now has access to 300 mm state-of-the-art equipment that will allow us to develop more advanced GaN-based power devices. Examples are aggressively scaled low-voltage *p*-GaN gate HEMTs for use in point-of-load converters, supporting energy-efficient power distribution for CPUs and GPUs."



As part of the 300 mm GaN programme, a baseline lateral *p*-GaN HEMT technology platform will first be established for low-voltage applications (100 V and beyond), using 300 mm silicon (111) as a substrate. For this, process module work centred around *p*-GaN etch and Ohmic contact formation is ongoing.

Later, high-voltage applications are targeted. For 65 V and above, developments will utilise 300 mm semi-spec and CMOS-compatible QST engineered substrates (a material with poly-crystalline AlN core). During the developments, control over the bow of the 300 mm wafers, and their mechanical strength are prime concerns.

The launch of the 300 mm GaN programme follows successful 300 mm wafer handling tests and mask set development. Imec expects to have full 300 mm capabilities installed in its 300 mm cleanroom by the end of 2025.

"The success of the 300 mm GaN development also hinges on the ability to establish a robust ecosystem and jointly drive innovation from 300 mm GaN growth and process integration to packaging solutions," adds Stefaan Decoutere. "We are therefore pleased to announce Aixtron, GlobalFoundries, KLA Corporation, Synopsys, and Veeco as first partners in our open R&D programme track on 300 mm GaN and hope to welcome more partners soon. Developing advanced GaN power electronics requires close coupling between design, epitaxy, process integration, and applications – a coupling that has proved to be critical for our pioneering work on 200 mm GaN."

"The success of the 300 mm GaN development also hinges on the ability to establish a robust ecosystem and jointly drive innovation from 300 mm GaN growth and process integration to packaging solutions."

Vertical Semiconductor raises $11 million

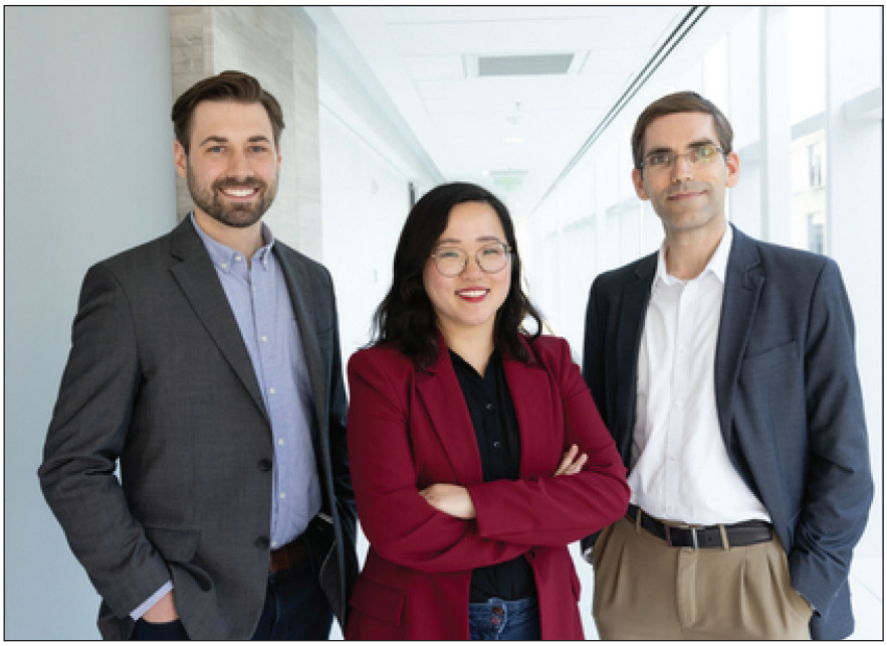
MIT GaN spin-out bets on the next wave of power growth for AI chips and data centres

VERTICAL SEMICONDUCTOR, a spin-out from the Massachusetts Institute of Technology (MIT), has announced $11 million in seed funding to help accelerate development of vertical GaN transistors to deliver the next wave of power to AI chips in data centres.

The company's GaN transistors are designed to ease data centre power bottlenecks by pushing energy conversion closer to the chip. This is said to improve efficiency by up to 30 percent and enable a 50 percent smaller power footprint in AI data centre racks.

"The pace of AI is not only limited by algorithms. The most significant bottleneck in AI hardware is how fast we can deliver power to the silicon," said Cynthia Liao, CEO and co-founder of Vertical. "We're not just improving efficiency, we're enabling the next wave of innovation by rewriting how electricity is delivered in data centres at scale."

Vertical's technology is built on a decade of research at MIT's Palacios Group – a GaN research lab. The company has demonstrated the technology on 8-inch wafers using standard silicon CMOS semiconductor manufacturing methods, enabling integration with existing process technology and making it ready for real-world deployment for devices from 100 V to 1.2 kV.



➤ Pictured above: founders of Vertical Semiconductor: Josh Perozek, Cynthia Liao, and Tomás Palacios

"The Vertical team has cracked a challenge that's stymied the industry for years: how to deliver high voltage and high efficiency power electronics with a scalable, manufacturable solution," said Matt Hershenson, Venture Partner at Playground Global, which led the funding round. "They're not just advancing the science – they're changing the economics of compute."

Additional investors include JIMCO Technology Ventures, Milemark Capital, and Shin-Etsu Chemical.

Rohm and Infineon to collaborate on SiC packages

Companies to second source selected packages for SiC power chips with plans to expand to GaN in the future

Rohm and Infineon have signed an agreement to collaborate on packages for SiC power semiconductors used in applications such as on-board chargers, photovoltaics, energy storage systems, and AI data centres.

The partners aim to enable each other as second sources of selected packages for SiC power devices, a move which will increase design and procurement flexibility for their customers. In the future, customers will be able to source devices with compatible housings from both Rohm and Infineon.

As part of the agreement, Rohm will adopt Infineon's innovative top-side cooling platform for SiC, including TOLT, D-DPAK, Q-DPAK, Q-DPAK dual, and H-DPAK packages. Infineon's top-side cooling platform offers several benefits, including a standardised height of 2.3 mm for all packages.

At the same time, Infineon will take on Rohm's DOT-247 package with SiC half-bridge configuration to develop a compatible package. That will expand Infineon's recently announced Double TO-247 IGBT portfolio to include SiC half-bridge solutions.

Rohm's DOT-247 delivers higher power density and reduces assembly effort compared with standard discrete

packages. Featuring a unique structure that integrates two TO-247 packages, it enables a reduction in thermal resistance by approximately 15 percent and inductance by 50 percent compared with the TO-247. The advantages bring 2.3 times higher power density than the TO-247.

Rohm and Infineon plan to expand their collaboration in the future to include other packages with both silicon and wide-bandgap power technologies, such as SiC and GaN.

"We are excited about working with Rohm to further accelerate the establishment of SiC power devices," said Peter Wawer (above left), division president green industrial power at Infineon. "Our collaboration will provide customers with a wider range of options and greater flexibility in their design and procurement processes, enabling them to develop more energy-efficient applications that will further drive decarbonisation."

"Rohm is committed to providing customers with the best possible solutions. Our collaboration with Infineon constitutes a significant step towards the realisation of this goal, since it broadens the portfolio of solutions," said Kazuhide Ino (above right), member of the board, managing executive officer, in charge of power devices business at Rohm.

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CGD partners with GlobalFoundries

CAMBRIDGE GaN Devices (CGD) has announced that it is working with GlobalFoundries (GF) to strengthens CGD's fabless strategy, expanding the supply chain for the company's single-chip ICeGaN power devices.

Simon Stacey (pictured above), COO of CGD, said: "Applying the CGD design flow to the excellent GF process design kit (PDK) is essential to enabling CGD to develop and manufacture our next generation GaN power devices at a much faster time to market. We are delighted to be partnering with GF, as their renowned foundry services and commitment to GaN are a perfect fit for our ICeGaN power devices."

ICeGaN combines a GaN switch, interface and protection circuitry on the same GaN chip, in contrast to most other solutions that use multi-chip or co-packaged solutions.

CGD's pioneering single-chip technology runs with standard silicon MOSFET drivers and is built using a standard silicon CMOS wafer fab process. This means that there is no need for a specialist process in the wafer fab. Using GF's 8-inch process also ensures the manufacturing costs of CGD products remain inherently competitive, according to the company.

Ams Osram and Nichia sign broad IP agreement

Comprehensive cross-license agreement covers thousands of patent-protected innovations in LED and laser technologies

AMS OSRAM and Nichia have expanded their long-standing IP collaboration with a comprehensive cross-license agreement covering thousands of patent-protected innovations in LED and laser technologies.

The agreement, signed by Aldo Kamper, CEO of Ams Osram, and Hiroyoshi Ogawa, president of Nichia, grants both companies mutual access to each other's patents for nitride LED and laser components. And, for the first time, also covers sophisticated LED packages and LED modules, such as matrix headlamps. The move aims to strengthen the IP protection both companies offer to their customers.

Ams Osram and Nichia have invested heavily in R&D over decades. They say that with the new patent cross-license agreement, customers will gain enhanced IP safety when using products based on their patented technologies. Both companies have a long history of cross-license agreements, which started in 2002 and continued through today, with an update in 2010. The new agreement covers R&D results from the last 15 years.

"In an industry driven by innovation, intellectual property is the foundation of trust and long-term value. Unfortunately, we continue to see LED and laser products entering the market that do not meet essential IP standards. Together with Nichia, we encourage customers to scrutinise claims of IP compliance and to choose partners holding a unique IP position like Ams Osram and Nichia", said Kamper.

"As the two global leaders in the LED and laser industry, Nichia and Ams Osram have renewed the most comprehensive and robust cross-licensing agreement in the sector. Customers who select products from Nichia or Ams Osram benefit from extensive patent protection, ensuring confidence in their business activities. Standing together, we will continue to safeguard the market's integrity by encouraging respect for intellectual property throughout our industry", said Ogawa.

Northrop Grumman opens access to US chip facilities

New business model aims to expand secure production of defence microelectronics on US soil

NORTHROP GRUMMAN has announced that its Microelectronics Centre is now open for external aerospace and defence companies to access the company's three US government-accredited semiconductor manufacturing facilities.

According to the company, this decision expands the secure production of defence microelectronics on US soil. The open-access business model allows commercial businesses, aerospace and defence companies, the US Government, academia, federally funded research and development centres and others, to design, manufacture, package and test microelectronics domestically for commercial and defence applications.

It will also give access to end-to-end US-based advanced packaging facilities with reliable semiconductor design, post-processing, assembly and test for current and future generation technologies.

Northrop Grumman-produced semiconductor products and components will also be available for purchase via an online storefront. Vern Boyle, vice president of the Northrop Grumman Microelectronics centre: "By opening our defence-grade manufacturing facilities to partners, Northrop Grumman is expanding and strengthening the resilience of America's semiconductor industry and supply chain. We are providing partners with unprecedented access to design and develop domestic chips as well as the ability to directly purchase from us, enhancing collaboration across the broader defence industrial base."

Northrop Grumman's Microelectronics centre is comprised of three manufacturing facilities – two US government-accredited semiconductor foundries in California and Maryland and an advanced packaging facility in Florida.

Foundry services include silicon mixed-signal, analogue, or digital ASIC's; GaAs or GaN compound semiconductor MMIC's; or power transistors in silicon or SiC.

The packaging facility is capable of 100 mm to 300 mm wafer bumping, probing, and dicing, which allows multiple smaller, specialised chips to be combined into a single, more powerful electronics package. Unlike traditional methods that place multiple chips side-by-side into a system, advanced packaging integrates multiple specialised chips together with high-density connections into a 3D chip stack.

Europe's tech giants unite to secure photonics future

Bosch, Volkswagen, Nokia, Zeiss, Trumpf and other industry leaders urge the EU to create €2 billion photonics programme

IN a joint statement, some of Europe's biggest industrial names, including Bosch, Volkswagen, Mercedes-Benz, Nokia Bell Labs, Zeiss, Trumpf, Ams Osram and EssilorLuxottica have urged the EU to create a €2 billion photonics programme in the next EU Framework Programme (FP10).

The call from companies across Europe's defence, automotive, healthcare, manufacturing, and telecoms sectors, aims to unlock €6-8 billion in private co-investment and secure Europe's tech sovereignty. They argue that without a bold and dedicated strategy, Europe risks falling further behind China and the US in the global race for photonics – the light-based technologies that underpin 20 percent of the EU economy.

The joint statement calls on the EU to establish a €2 billion stand-alone photonics programme under FP10; to launch Photonics Grand Challenge proposals in fields such as AI, space, quantum, and defence; and to strengthen resilient European supply chains for critical photonics components and materials.

"Photonics is the invisible force behind everything from AI and quantum computing to secure communications, energy, healthcare, defence, and mobility," said Lutz Aschke, president of Photonics21. "But Europe is at risk of losing its critical, competitive edge unless FP10 delivers a stand-alone €2 billion photonics programme, capable of unlocking €6-8 billion in industrial co-investment."

The signatories stress that photonics is one of the few digital technologies where Europe has long been a leader, but warn that China's share of the global photonics market has surged from 10 percent in 2005 to 32 percent in 2022, while Europe's has slipped to 15 percent.

"Photonics is a strategic technology for Europe's prosperity, autonomy, and security. This joint statement shows that Europe's industrial leaders stand united," said Aschke.

Novosense, UAES and Innoscience join forces on GaN

Chinese trio sign agreement to reshape GaN power electronics for new energy vehicles

CHINESE FIRMS Novosense Microelectronics, UAS, and Innoscience have signed a strategic co-operation agreement to jointly advance GaN power electronics for new energy vehicles (NEVs).

The three parties will collaborate on next-generation intelligent integrated GaN products with Novosense bringing experience in analogue and mixed-signal IC design; UAES (a joint venture of Zhong-Lian Automotive Electronics and Robert Bosch) contributing knowledge in system integration and automotive applications; and Innoscience bringing expertise in GaN device technology.

Building on the combined expertise, the partners aim to tackle critical challenges such as efficiency, reliability and cost. They say the resulting new devices will deliver more reliable GaN driving and protection features, enabling higher power density and paving the way for commercial adoption across the automotive industry.

Xiaolu Guo, deputy general manager of UAES, said: "UAES has been at the forefront of automotive electronics for decades, consistently responding to industry needs through innovation. GaN technology is a vital enabler for vehicle electrification. Partnering with Novosense and Innoscience allows us to integrate capabilities from device to system level, driving

GaN industrialisation and delivering efficient, reliable and cost-effective solutions for our customers."

Shengyang Wang, founder, chairman and CEO of Novosense, commented: "Upgrading the NEV industry requires deep collaboration across the value chain. By combining UAES's system integration expertise with Innoscience's GaN leadership and Novosense's IC design capabilities, we are creating a powerful synergy. This strategic partnership sets a benchmark for industry collaboration, ensuring both technological breakthroughs and market value creation."

Jingang Wu, CEO of Innoscience, added: "The potential of GaN in automotive power electronics is only beginning to be realised. True impact will come from aligning device innovation with system requirements. We look forward to working closely with Novosense and UAES to extend the boundaries of GaN applications in automotive electrification and to translate technological advantages into tangible industry benefits."

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Axcelis and Veeco to merge

AXCELIS TECHNOLOGIES and Veeco Instruments have agreed to combine in an all-stock merger. The resulting company is expected to have an enterprise value of around $4.4 billion.

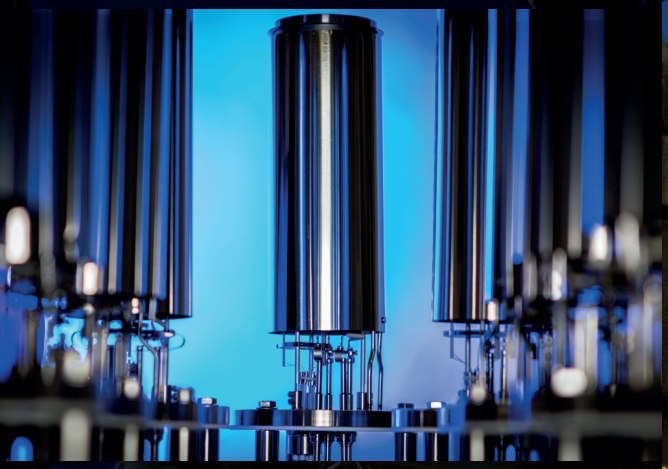
The combination will create the fourth largest US wafer fabrication equipment supplier by revenue, and will offer a product portfolio spanning ion implantation, laser annealing, ion-beam deposition, advanced packaging solutions and MOCVD.

"This combination marks a transformational milestone for both Axcelis and Veeco, establishing a new leader in semiconductor capital equipment with complementary technologies, a diversified portfolio and an expanded addressable market opportunity," said Russell Low, president and CEO of Axcelis.

He added: "We have long admired Veeco's history of innovation and its track record of delivering breakthrough products. I had the privilege of previously working at Veeco and I hold deep appreciation for its incredible talent, culture and innovation. Together, we will be well-positioned to serve large and growing end markets poised to benefit from significant secular tailwinds, creating exciting opportunities for employees and accelerating next-generation innovation for our customers."

"This merger capitalises on the core competencies of both Veeco and Axcelis to address our customers' critical needs," said Bill Miller, CEO of Veeco. "With increased R&D scale, the combination of these two exceptional businesses will accelerate our ability to solve material challenges, enable advanced chip manufacturing and build an even stronger company that can deliver superior value for all stakeholders."

RIBER's MBE 6000



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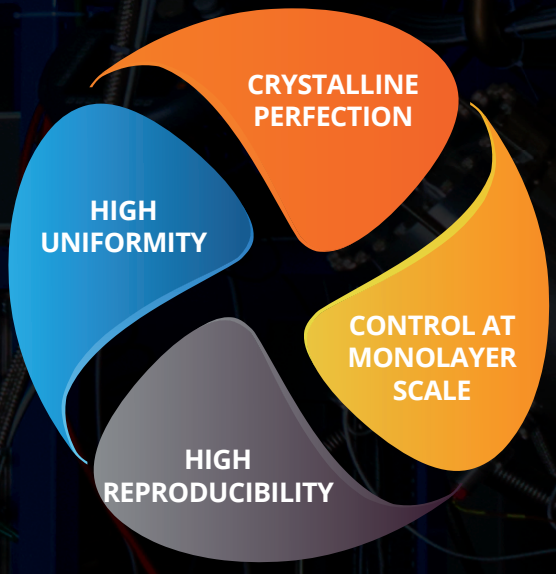

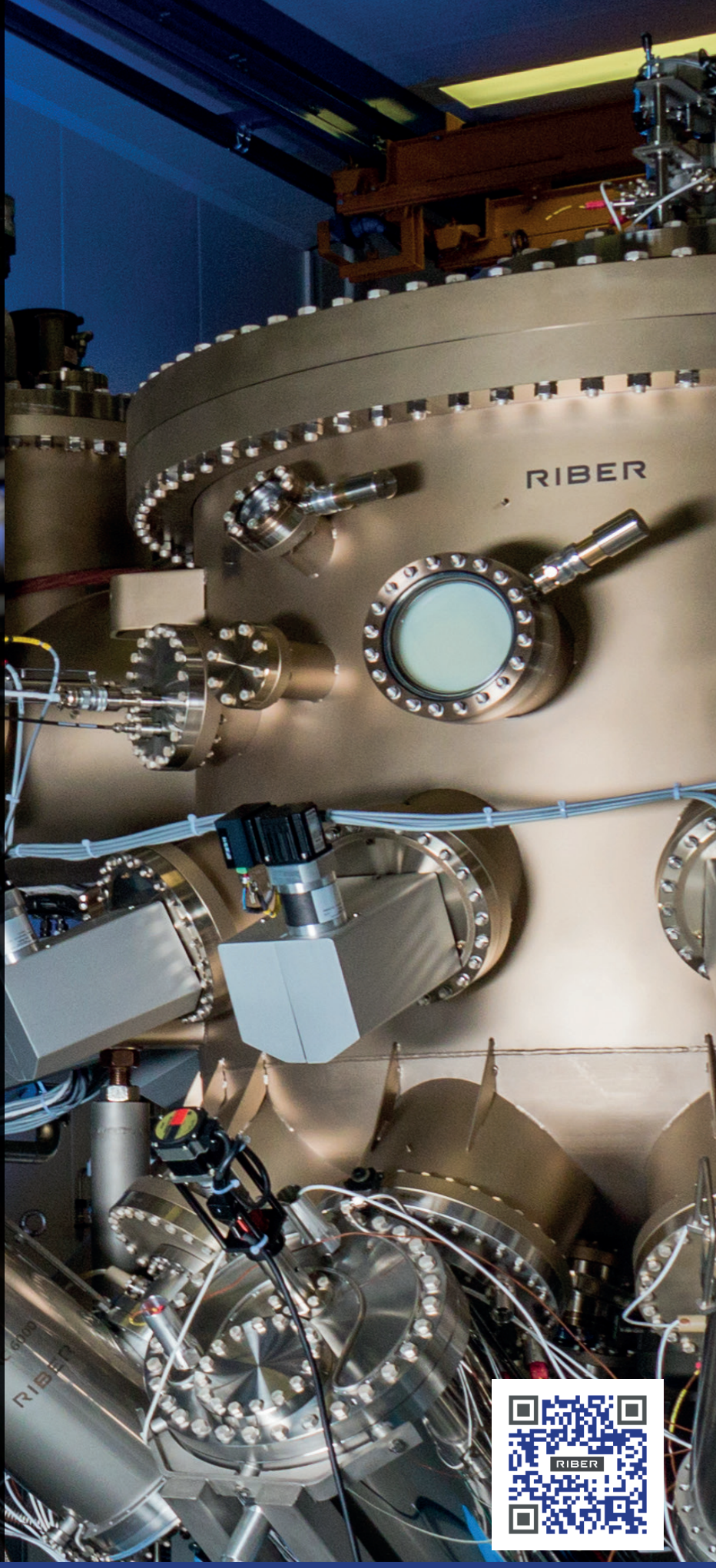

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UVC LEDs up their game

More powerful, efficient and longer lasting UVC LEDs are making a compelling case for water purification

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

IN YEARS GONE BY, the performance figures for nitride-based LEDs operating in the deep-UV fell far short of those emitting in the blue. But differences in the key characteristics of these two emitters are narrowing all the time, and the metrics for UVC LEDs now feature a number of impressive specifications.

Take the recent announcement from ams Osram, for its latest generation of UVC LEDs, slated to enter volume production in just over a year. Its best 265 nm-emitters now deliver an optical output of 200 mW at a wall-plug efficiency of just over 10 percent, while offering a lifetime of more than 20,000 hours.

When commenting on these figures, ams Osram's Senior Key Expert for Applications, Alexander Wilm, refrains from singling out any one number. Instead, he claims that it's the combination of the three that's particularly impressive.

➤ UVC LEDs have attracted much interest over many years for the disinfection of air and surfaces.

Wilm points out that there are UVC LEDs on the market that are more powerful, and also those with a higher wall-plug efficiency. "But having this efficiency at this output power and at more than 20,000 hours lifetime, that is something that is not that easy to do. That's why we think we are really unique."

The latest device from ams Osram has almost double the efficiency of its most powerful commercially available 265 nm LED, which delivers 115 mW at a wall-plug efficiency of 5.3 percent. And if the European opto-electronics powerhouse wanted to grab the headlines with an even higher wall-plug efficiency number than the 10.2 percent it is quoting for its latest devices, it could boast a value of almost 15 percent, realised by dialling down the drive current of its flagship LED to 20 mA.

"But then you only have 15 milliwatts, which is very little, so it will not help you in applications," warns Wilm, who is focusing on meaningful figures, and ultimately the practical deployment of ams Osram's products.

Recent improvements to the performance of the company's UVC LEDs have come through refinements to epitaxy, alongside improvements in chip and package design.

Brighter, more efficient devices can be attributed to an increase in the conversion of electrons to photons, and to better light extraction from the chip.

"The biggest improvement we made is the new package," says Wilm. He explains that improving the interaction of the package and the chip has led to an increase in outcoupling of UV emission.

While there is much interest within the UV LED industry in AlN substrates that offer excellent thermal conductivity and lattice-matching with epilayers,

engineers at ams Osram are using sapphire substrates for their devices.

"Sapphire is a standard material for LED production. It's available, widely used, and the base for our other LEDs," remarks Wilm. "Right now, we believe that sapphire is the future for us."

Covid's legacy?

During the height of the Covid-19 pandemic, UVC LEDs were widely viewed as an attractive option for killing this coronavirus. But since then, interest has dwindled in using this class of LED for that application.

However, Wilm does not see this as a major impediment for the future of the UVC LED, as by far its biggest application is water treatment, a multi-billion-dollar sector that's growing fast.

For water treatment, UVC LEDs compete with mercury lamps, the incumbent solution. Lamps emit significant powers, but have a number of weaknesses: they are bulky; fragile; they take several minutes to warm up; have a lifetime that's shorter than a UV LED (typically lasting 8,000 to 14,000 hours); and their disposal is far from trivial, due to the damaging effects of mercury on human health.

Another weakness of the mercury lamp is that its emission peak, fixed at 253.7 nm, is not ideal for water treatment.

"The peak of the germicidal effectiveness is at 265 nanometres," says Wilm, who adds: "We steered our LEDs exactly to this sweet spot."

There are a number of opportunities for UVC LEDs within the water treatment sector.

One is point-of-use, with solid-state emitters fitted to a water tap. And there is also what's referred to as point-of-entry, with water bombarded by UVC as it enters a home.

In both these cases, the UV source only needs to be on when water is flowing. As well as ruling out the mercury lamp for this application, due to its very slow warm-up time, this operating condition allows the driving conditions for the device to be adjusted, to get more out of the LED – and use fewer of them. As this solid-state emitter is off far more than its on, it doesn't need a lifetime as long as 20,000 hours, so this can be traded for a higher output power, produced by cranking up the current.

➤ Point-of-use water treatment is an application where UVC LEDs are an ideal light source.

Where the mercury lamp dominates is large-scale water treatment, associated with industrial and municipal applications. In these cases, the UVC source is on all the time, and high powers are the key yardstick.

"200 [milliwatts] is a good starting point," says Wilm, who points out that even more powerful devices will follow. "If you compare it to five years back, the power that you got was around below 50."

Among the customers already buying UVC LEDs from ams Osram is Hergy International, a Taiwanese producer of water sterilisation equipment. 265 nm LEDs manufactured by ams Osram are deployed in Hergy's Perazim series of drinking water sterilisers, which include a model that processes 2 litres of water per minute while consuming just 3 W, and a variant that handles flows of up to 6 litres per minute.

When 200 mW UVC LEDs enter volume production towards the end of 2026 they may lead to an even more impressive range of products from Hergy – and they may be joined by more competitive rivals, given that ams Osram's more powerful 265 nm emitters will be available to all.

By then, ams Osram – as well as its peers – may have even reported more impressive results. After all, UVC LEDs are getting ever more powerful, efficient, and long lasting, and these trends show no sign of abating.

For water treatment, UVC LEDs compete with mercury lamps, the incumbent solution. Lamps emit significant powers, but have a number of weaknesses: they are bulky; fragile; they take several minutes to warm up; have a lifetime that's shorter than a UV LED and their disposal is far from trivial, due to the damaging effects of mercury on human health

Wolfspeed: Making material gains

The pioneer of SiC starts to offer 200 mm substrates and epiwafers to all

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

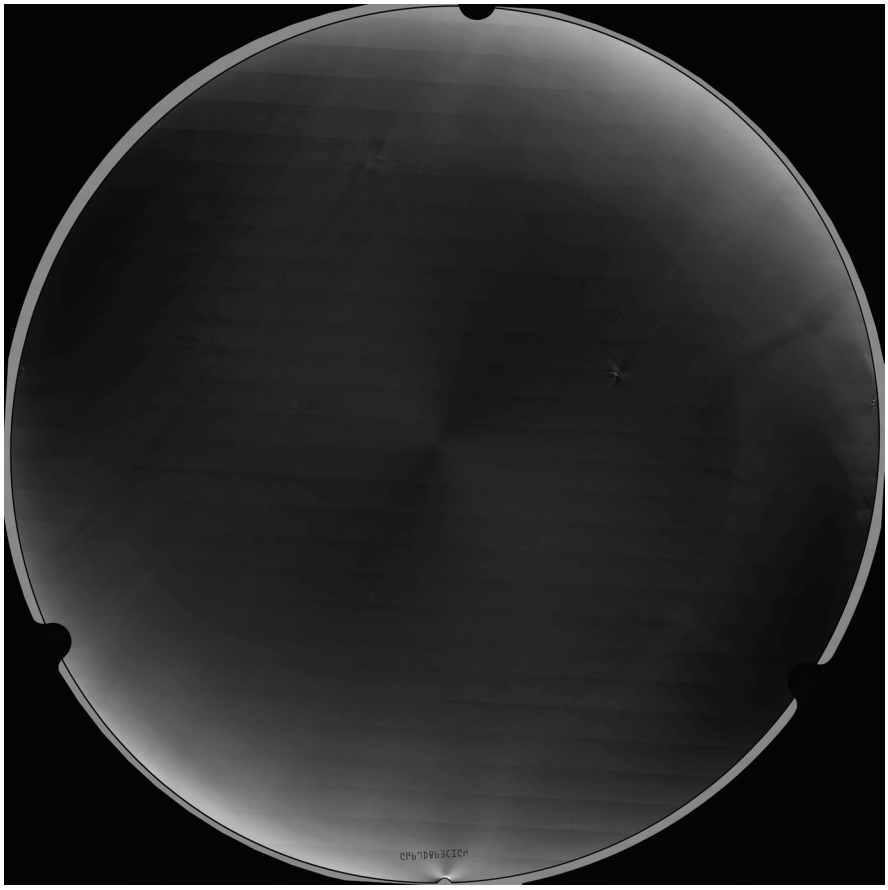
FOR THE last year or so, Wolfspeed has been in the news for the wrong reasons. Recent coverage of this SiC specialist has focused on its crippling debt, a filing for Chapter 11 Bankruptcy protection, and a global market softness that holds back its exploitation of a vastly expanded production capacity.

These ferocious headwinds have caused the company to lay off many staff, and are behind a share price that's fallen through the floor.

However, over the last few weeks Wolfspeed has started to change the narrative. Helping to drive this are a filing of positive press releases: one details a financial restructuring process that has enabled the company to emerge from Chapter 11 protection and substantially reduce its debt – a good move, but one that's been very, very hard on existing shareholders; and another outlines the opening up of its 200 mm substrate and epiwafer expertise to all.

In the halcyon days of the SiC industry, when global substrate supply struggled to keep pace with demand, Wolfspeed signed a handful of substantial wafer supply agreements totalling around $2 billion. These deals enabled the likes of Infineon, STMicrolectronics, onsemi and Rohm to secure 150 mm SiC substrates from the world's leading supplier.

Last year Wolfspeed started to expand this side of its business by offering its 200 mm substrates to selected high-volume customers, while fine-tuning material specifications. And now it's gone one step further, opening up this product to all.



➤ The uniformity in the cross-polarised image underscores the quality of Wofspeed's 200 mm substrates.

According to Cengiz Balkas, Wolfspeed's Chief Business Officer, this latest step reflects the company's readiness to supply the industry with the quality and volumes of 200 mm SiC that will be needed.

"We've gone through these wafer transitions many times in our history," says Balkas, who explains that migrations from one diameter of substrate to a larger variant always begin with internal use of the larger size. "Once we go through that initial heavy lifting of getting everything settled in, we come to market and start ramping our commercial customers."

For the company's 200 mm format, substrates are manufactured at its historic facility in Durham, North Carolina, with production of SiC MOSFETs and Schottky barrier

diodes undertaken at the device factory in Mohawk Valley, New York.

As Wolfspeed is the largest consumer of 200 mm substrates, used to make its 600 V, 1200 V and 1700 V SiC MOSFETs and Schottky barrier diodes, it's of no surprise that the majority of this material is deployed for internal chip production. "But we definitely have enough volume to start ramping our customers," says Balkas.

Quantity and quality

Any chipmaker that uses Wolfpseed's 200 mm substrates will not trade a larger size for inferior quality. "They're definitely better than our 150 mm wafers millimetres," says Balkas, explaining that they have lower densities of micropipes, screw dislocations and basal place dislocations, as well as a lower residual stress and better surface parameters.

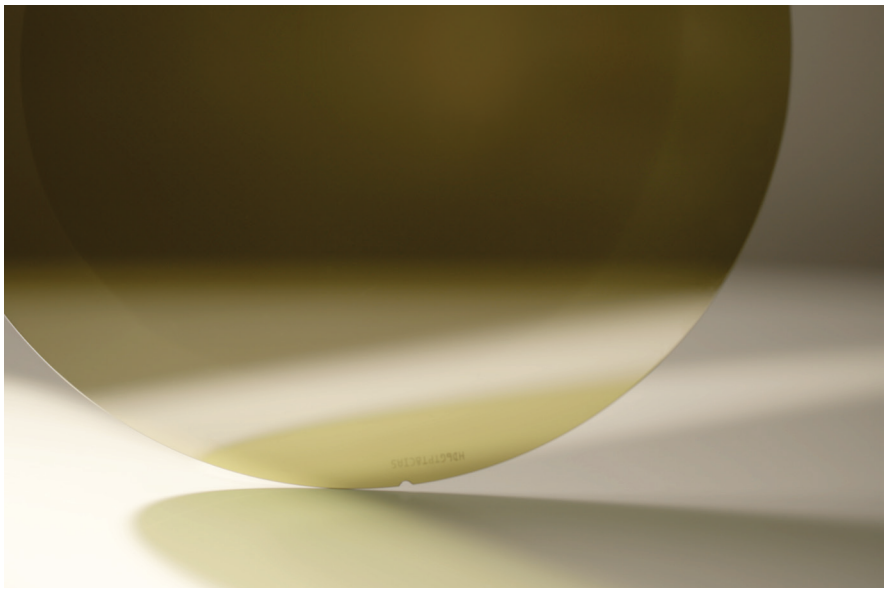
Improvements in material quality will continue at Wolfspeed, and while efforts are focused on the 200 mm format, insights into how to produce better boules will be applied to the manufacture of 150 mm products.

For all forms of SiC substrate, Wolfspeed will be following the well-known pathway for the semiconductor industry, making substrates better and cheaper over time. According to Balkas, the cost-per-unit area of the company's substrates is on a "pretty significant reduction curve".

Prices that customers pay for this format are confidential, and will depend on volume. It's possible that those switching from 150 mm to the larger format will initially pay more per-unit-area when ordering small quantities to get going, but as volumes increase for both the customer and Wolfspeed, the larger format will be the more economical one.

Spurred on by the growth of the SiC market, more companies are producing substrates, with Wolfspeed facing particularly fierce competition from China. According to the market research firm Yole, Wolfspeed is still the clear leader in this sector, but its market share is in decline.

In any market, rivals always look for factors that allow them to stand out from the crowd. Viewed in these terms,



Balkas believes that Wolfspeed's vertically integrated approach gives it a crucial edge.

"We make automotive-qualified power devices in our New York factory," says Balkas, who points out that this allows Wolfspeed to have a credible case when customers consider placing orders for 200 mm substrates.

A number of producers of SiC substrates are looking to raise their profile by showcasing 300 mm substrates. While this is an impressive feat, it is far from clear how long it will be until high-volume production of SiC power devices even begins on 300 mm lines.

"For us, next steps are to get through the 200-millimetre transition and ramp the industry on 200-millimetre. It looks pretty early to me to discuss 300-millimetre," argues Balkas.

Outsourcing epitaxy

Within the wide bandgap power electronics industry, many of the producers of GaN HEMTs are fabless, while the SiC sector is dominated by those with their own production lines.

Given this, one may not expect much demand for SiC epitaxy. But there is, and always has been, according to Balkas.

"What we see, especially in the early stages of a diameter change, is that our customers really have a need for epi services. If I look at the 150 mm-millimetre long-term agreement, we had a significant amount of 150 volume – that was a combination of availability of epi, quality of the epi, and the pricing that we can offer."

For epitaxy on 200 mm SiC, Wolfspeed offers thickness and doping uniformities of ± 8 percent and ± 12 percent, respectively, as baseline specifications – figures derived by considering all points within an area that's defined by edge exclusions of 3 mm for usable area, and 4 mm for doping uniformity. Useable area is more than 85 percent, for a 5 mm by 5 mm grid.

Those impressed with these figures and interested in securing these epitaxial services should have no concerns whatsoever related to Wolfspeed keeping their IP completely confidential.

"We're extremely proud of our history and reputation in the market," says Balkas, who reveals that the company has multiple protection rules to prevent any customer information relating to their epiwafer design from reaching those within the company that work on Wolfspeed's own devices. "Our track record is spotless."

By combining epitaxial services on 200 mm SiC with substrate access to all, Wolfspeed is in a great position to lead this industry's production of power devices on the larger format. It's a significant milestone that will be welcomed by producers of SiC MOSFETs and Schottky barrier diodes. But only time will tell how much this will do to help to revive the fortunes of Wolfspeed, and fill its vastly expanded capacity.

GaN: Tracking fast-charging with 'Lichi Law'

All forms of GaN fast charger are delivering an increase in output power of around 50 percent every 12 months

BY XINKE LIU FROM SHENZHEN UNIVERSITY

THE SILICON INDUSTRY is well-known for its laws. The most famous of these, attributed to Intel co-founder Gordon Moore, states that the number of components on an IC doubles every year. And also known to many is the law formulated by Robert Denard: as transistors are reduced in size, there's no change in power density, as voltage and current scale with the length of the channel. Note, however, that since the mid-noughties, it appears that Dennard scaling has broken down.

There are also laws within the compound semiconductor industry. Maybe you have heard of Haitz's law, which states that every decade the LED's cost-per-lumen falls by a factor of ten, and that for a given wavelength, the light generated by a packaged device increases by a factor of 20. And more recently, thanks to the efforts of a Chinese collaboration that I am involved with, there's 'Lichi law', describing the performance changes associated with GaN charging, named after the lychee trees that are near my laboratory at Shenzhen University.

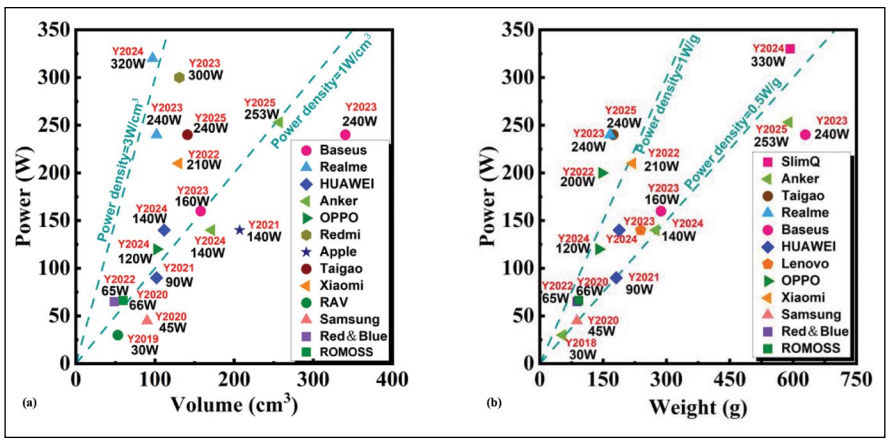
Over the last few years sales of GaN power devices have rocketed, following their adoption into consumer fast-charging products. Our collaboration has been delving into performance-related aspects of this, by conducting in-depth market research, and back in 2023 we identified the development laws at that time, leading us to propose Lichi law – it states that, on average, for every 12-month interval, the output power of commercial GaN fast chargers increases by about 50 percent. Two years on, we have found that consumer GaN fast charging is still following Lichi Law, and the industrial market is now enjoying similar dynamics.

To illustrate this rapid rise in output power, consider that back in 2018 the Anker GaN fast charger launched to market delivered just 30 W. While impressive at the time, a number of brands are now launching products with an output power of more than 300 W, and a power density exceeding 3.3 W cm^{-3}.

Our work includes a survey for 3C certification data of GaN fast-charging products, which has enabled us to produce a visual comparison of the power parameter distribution of products listed in different years (see Figure 1).

Based on this data, one can see that fast-charging products before 2021 are predominantly concentrated below 1 W cm^{-3}, with power density generally in the range 0.7-0.9 W cm^{-3}, reflecting the state of maturity of early GaN technology. By 2023, most fast-charging products surpassed 1 W cm^{-3}, with some even exceeding 2 W cm^{-3}, which may be the industry's first experimental high-density products. Fast-charging products are clustered in the 1-3 W cm^{-3} band from 2024 to 2025. So far, the maximum power density is 3.3 W cm^{-3}, but a few products are appearing at around just 1.8 W cm^{-3}, reflecting the technology stratification of the market – some vendors are pursuing the ultimate density, while others are focused on cost and stability.

Looking at the distribution of the mass of these chargers (see Figure 1 (b)), it is clear progress has been made. In 2018, when Anker introduced the first 30 W GaN fast charger, it had a mass of 54 g and a power density of only 0.53 W g^{-1}. In 2022 OPPO broke new ground, with its 200 W GaN fast charger with a mass of 147 g and a power density of 1.36 W g^{-1} – this was the first fast charger to break through 200 W and have a power density of over 1 W g^{-1}.



➤ Figure 1. (a) GaN fast-charging output power-product volume diagram. (b) GaN fast-charging output power-product quality diagram.

Since then, Realme and Taigao have raised the bar, launching 240 W GaN fast chargers with power densities of 1.44 W g^{-1} and 1.37 W g^{-1} in 2024 and 2025, respectively.

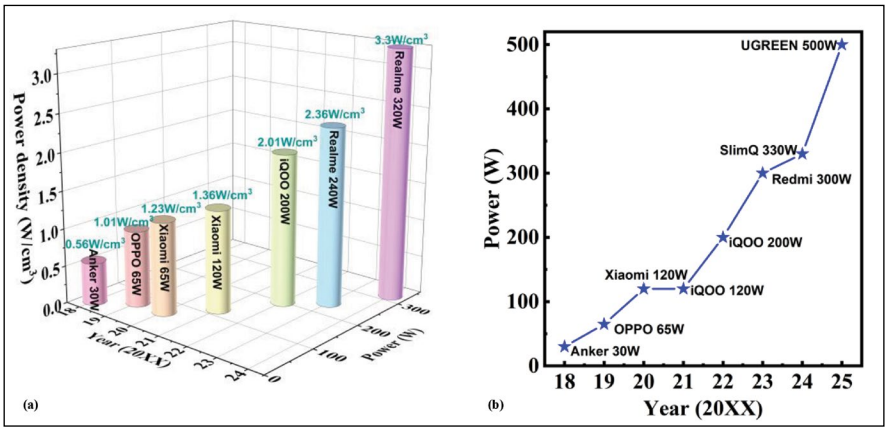
We have also collected data on the maximum power and power density of GaN fast-charging products over time, and plotted power density growth (see Figure 2 (a)) and power growth (see Figure 2 (b)). These graphs show that power and power density rise over time with a rate of increase that's highly consistent with the previously proposed 'Lichi Law' – that is, for every 12 months, the output power of commercial GaN fast-charging power units increases by about 50 percent.

Another observation is that GaN technology is accelerating its penetration from consumer-grade fast charging to industrial-grade power supplies, a trend that began in 2020. This finding has come out of conducting a comprehensive study, spanning 2018 to 2025, of consumer-grade fast charging and industrial-grade GaN power products (see Figure 3).

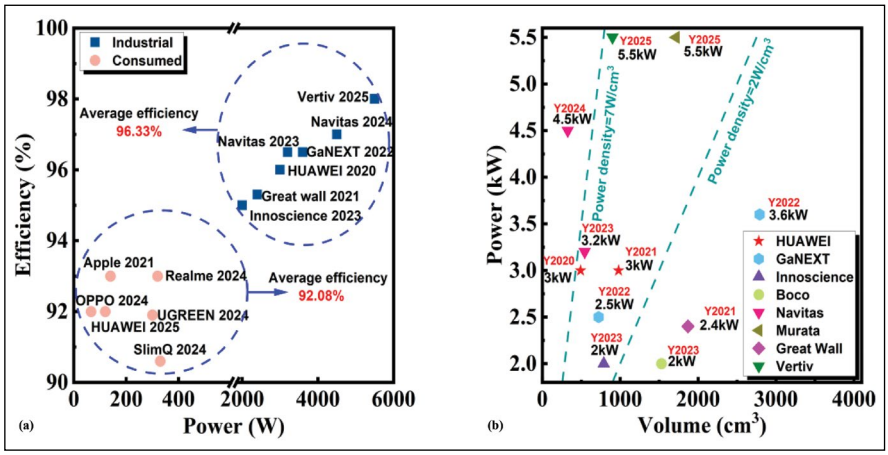
Compared to consumer-grade GaN fast-charging products, industrial-grade GaN power supplies are on average 4 percent higher, in terms of efficiency, and more than threefold higher, in terms of power output.

We have also determined that GaN has been more widely and deeply applied in the industrial sector, and its high-power, high-efficiency characteristics can be given full play in industrial scenarios, where it can fulfil demand for high-performance power supplies for industrial equipment.

Our extensive investigation of market dynamics has also identified a clear trend in increasing output powers. Between 2020 and 2021, we found that GaN technology was mainly verified in the initial stage of low and medium power scenarios. An example of this is Huawei's launch of 3000 W products with the potential for power density improvement. Come 2022, GaNEXT launched 3600 W GaN server power supplies with a 20 percent increase in power over their predecessors, but still with lower volumes and efficiencies, due to packaging technology. At that time, the average power density of these industrial power supplies



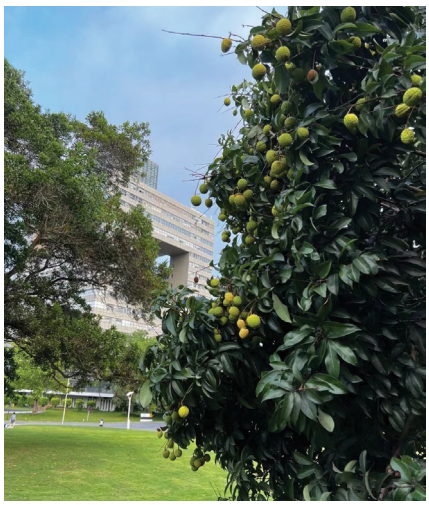
➤ Figure 2. Consumer GaN fast charging in recent years, evaluated in terms of (a) power density and (b) power.



➤ Figure 3. (a) Efficiency-power diagrams for industrial and consumer GaN power supplies. (b) Power-volume diagram for industrial GaN power supplies.

did not exceed 5 W cm^{-3}, with sales predominantly oriented to lightweight scenarios, such as edge computing.

The last few years have seen significant progress. Since 2023, Navitas has made breakthroughs in GaN server power supplies, with power densities



ranging from 5.88 W cm^{-3} for 3200 W products in 2023 to 13.79 W cm^{-3} for 4500 W modules in 2024, representing a 134 percent increase in volumetric efficiency in two years. At this point GaN technology began to be scaled for data centre applications, with an 8500 W prototype unveiled in 2024 with a 136 percent power increase from 2022, marking a breakthrough for GaN in medium-to-high power boundaries.

When deployed in industrial GaN power supplies, the power output density of GaN is generally within the range 3-6 W cm^{-3}. Underscoring the outstanding advantages of GaN in industrial applications, that power output density is two-to-three times higher than that in consumer GaN fast charging.

Our comprehensive study of the evolution of GaN in power charging includes a review of peak power data of industrial GaN server power supplies, and parameters of consumer-

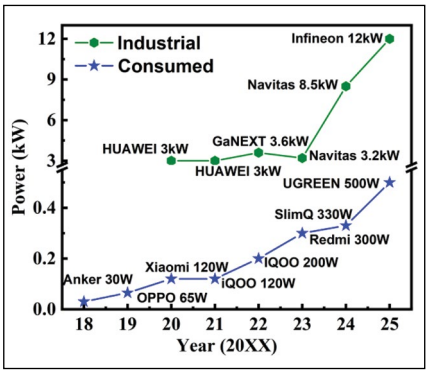


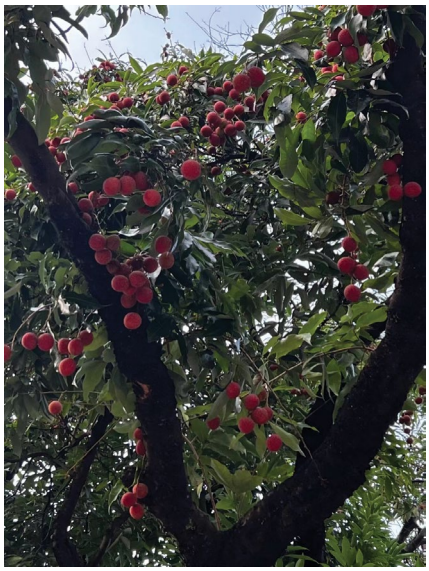
Figure 4. GaN consumer-grade fast charging and industrial-grade power supply development.

grade products. This has enabled the construction of a power-year coordinate system, and a comparative chart of power evolution technology development between industrial and consumer fields (see Figure 4).

By undertaking a thorough analysis of this chart, we have observed the trajectory of GaN technology. Our data shows that the performance improvement for GaN power devices is highly consistent with 'Lichi law'. Specifically, the output power of industrial-grade GaN power supplies increases by about 50 percent every 12 months.

We can conclude that through our study of consumer-grade GaN fast charging and industrial-grade GaN server power supplies, the output power of GaN fast charging tends to increase by about 50 percent every 12 months.

Contributors to Lichi's Law include: Zhixiang Zhong, Yutong Wu, Bing Jiang and Hezhou Liu from Shenzhen University; Jingbo Li from Zhejiang University; Jinping Ao from Jiangnan University; Lixuan Chen from Unilumin Group Co., Ltd; Yuxi Wan and Daohua Zhang from Shenzhen Pinghu Laboratory; Zhanwu Yang from Red & Blue Microelectronics (Shanghai) Co; and Shengsen Chen from Cotell Intelligent Technology (Shenzhen) Co. Ltd.



Every March, the fragrance of lychee flowers flows through the Li-Garden at Shenzhen University. For the next few months, as the lychee heads towards a full blossom, it's attractive to sit beside these trees and ponder. During such times, the initial ideas were formed on the possibility of a law related to progress in GaN power chargers.

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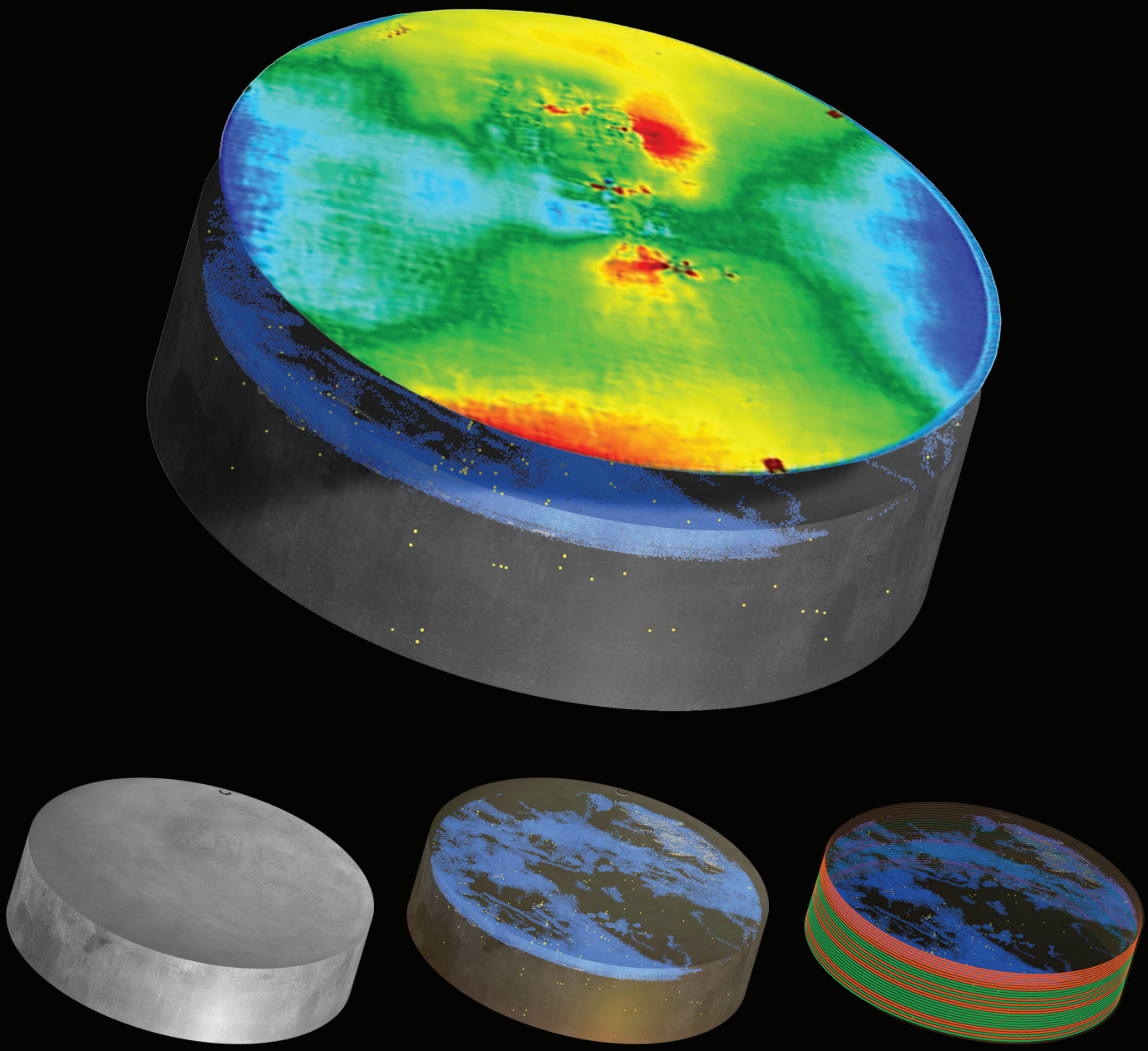


Taking the guesswork out of SiC production

Thanks to advances in metrology, it's now possible to scrutinise a SiC puck before it's wafered and identify material defects that govern yield and profitability

BY IVAN ORLOV, CAROLINE CHÈZE AND FRÉDÉRIC FALISE FROM SCIENTIFIC VISUAL, AND MARKUS STÖHR AND MICHAEL SCHÖLER FROM PVA TEPLA

WITHIN the semiconductor industry, SiC is a transformative material. This wide bandgap compound drives innovation in power electronics, electric vehicles, renewable energy and advanced communications, thanks to its remarkable properties that include a high electron saturation velocity and breakdown field, exceptional thermal conductivity and mechanical robustness. These strengths enable diodes and transistors to operate at higher voltages, higher frequencies and more extreme temperatures than ever before.

We have been closely following the evolution of SiC and have witnessed staggering progress that's been made over the last three decades to position this material as the backbone of efficient power electronics. We're not alone in knowing there's far more to come, with many forecasting SiC will remain central to the industry for the foreseeable future.

While today SiC is seen almost exclusively as a material for high-performance power devices, its potential extends to several other promising applications, including AR glasses, interposer layers in advanced packaging, data centers, and AI chips.

All these applications are leading to an increase in demand for high-quality substrates at accessible prices. There is plenty of headroom when it comes to improving the quality and, especially, the yield of SiC material. These improvements, however, are hindered by crystalline defects that impact device performance and reliability.

To name just a few examples, there are micropipes that threaten to trigger leakage currents and breakdown, basal plane dislocations and stacking faults that cause bipolar degradation, and polytype regions that may lead to premature failure.

To mitigate these risks, it is imperative to identify and reject 'killer' defects. However, today's practice is to undertake comprehensive defect inspection at the wafer stage (see Figure 1) – and we would argue that's too late, given that by then significant time and cost have already been invested in slicing and polishing.

It's easy for downstream device makers and final users to overlook the significance of this problem, because defective material is filtered out earlier in the chain. Yet, the associated cost is built into every SiC device.

To fully understand the importance of this issue, note that substrates can represent up to 40 percent of the final device cost, and SiC material yields can be as low as 50 percent. Thus, continuing to only detect 'killer' defects at the wafer stage is a substantial cost barrier to mass adoption of SiC.

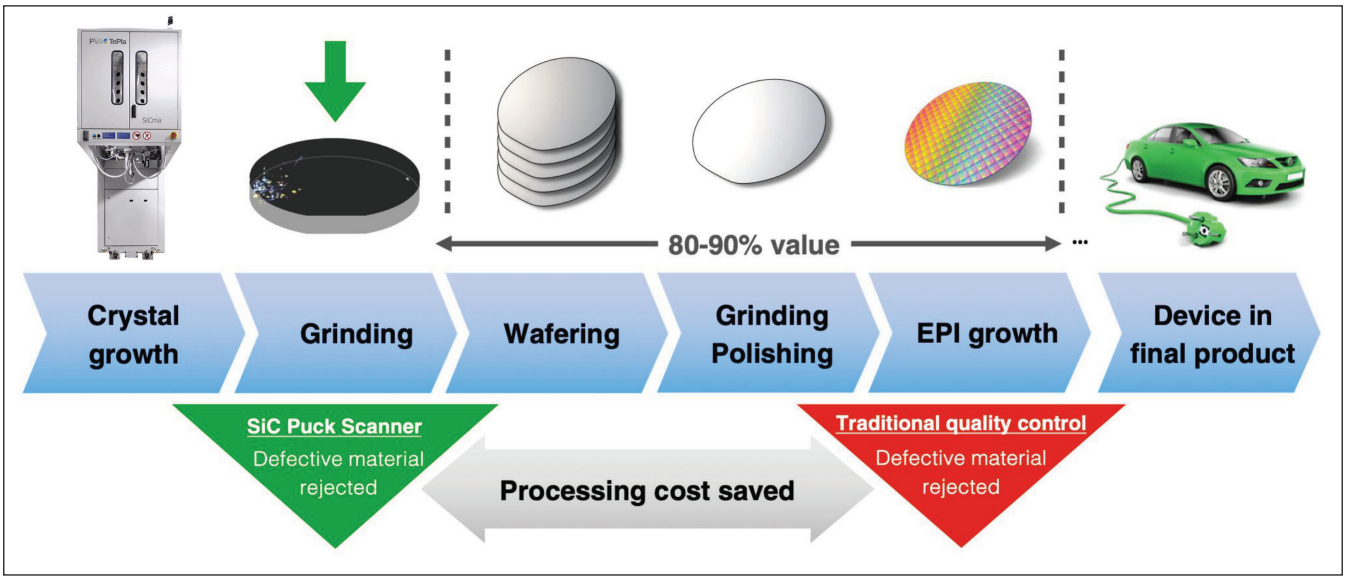
As SiC utilisation accelerates, our industry faces a pressing question: How can manufacturers ensure a high substrate quality while increasing wafer diameter? In response, PVA TePla and Scientific Visual now offer pioneering metrology solutions that redefine quality control for SiC.

The SiC Puck Scanner

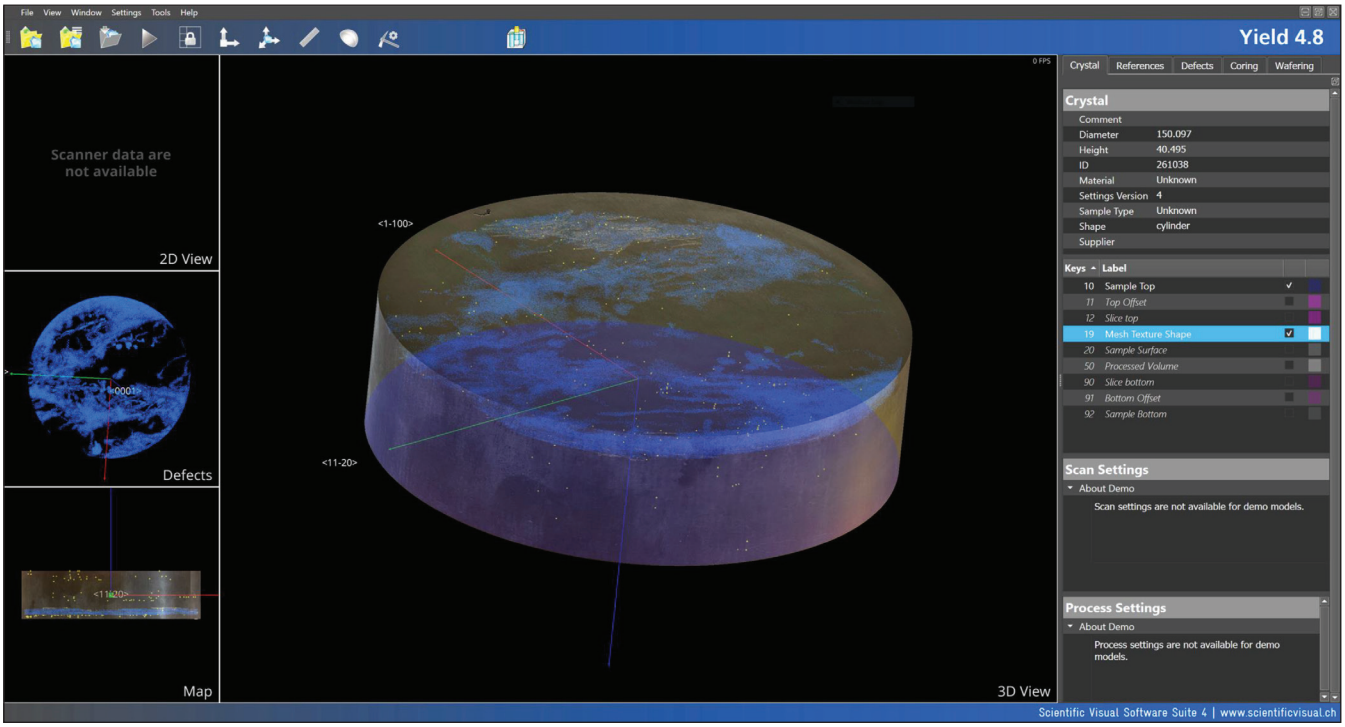
This September we unveiled the new SiC Puck Scanner at the International Conference on SiC and Related Materials, in Busan, South Korea. It is the first system to deliver non-destructive three-dimensional defect mapping directly within the puck volume (see Figure 2). It's a game changer, leveraging advanced tomography to visualise critical defects before any wafering or costly processing begins.

With this tool, sub-standard pucks can be set aside prior to the costly wafering stage, allowing manufacturers to dedicate their slicing capacity solely to high-grade material. For the first time, producers can apply reproducible, quantitative defect metrics rather than relying on subjective visual checks.

A further advantage is that the scanner enables SiC substrate makers to move beyond 'one-size-fits-all' decisions and instead adopt more tailored wafering strategies.



➤ Figure 1. Traditionally, the first comprehensive control of SiC defects in the production chain takes place at wafer level (red triangle), when substantial resources have already been devoted to processing. The new SiC Puck scanner shifts the quality control to an earlier stage (green triangle).



➤ Figure 2. 3D defect map – output of the SiC Puck Scanner. Shown here is the puck that's been used for the end-to-end study. Scans reveal lattice defects with micron-scale resolution, including polytypes, micropipes, voids, inclusions, dislocation clusters, and others. Colours correspond to defect morphology.

For instance, by drawing on precise defect coordinates, manufacturers can optimise wafering strategies by specifying the optimal cut levels. In case of wire-saw slicing, the goal is to position more defects within the kerf, thus excluding them from future wafers. This is achieved through Smart Wafering, a computer-aided patent-protected routine embedded in the YieldPro software that computes the most efficient puck position (offset) in a wafering system. As an example, we measured a 7 percent or greater increase in quality wafers compared to the 'blind' wafering in low- and mid-defective pucks.

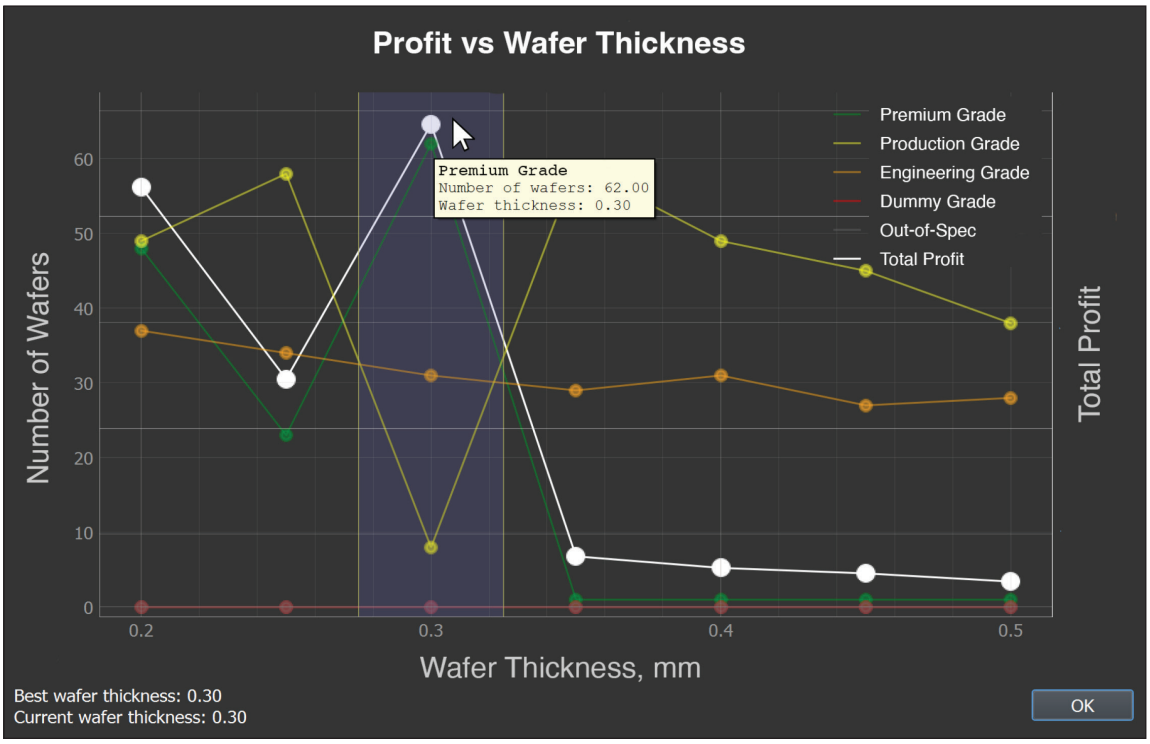
In laser wafering, this technique allows one to identify suitable slicing regions and skip overly defective areas that could distort the cleaving track. Maximising yield is achieved by reducing processing, and delivering more high-quality material – all without expanding growing capacity. Additionally, each puck can be assigned to applications most aligned with its defect profile.

Volumetric defect mapping allows manufacturers to make data-driven decisions at the earliest possible point in the production chain. In practice, we have found that up to 50-60 percent of the wafering cost can be preserved by rejecting defective material early, rather than scrapping wafers after processing. Furthermore, digital maps provides transparent quality data that can be shared with colleagues and customers.

The benefits of puck scanning extend well beyond immediate cost savings. Scanning also serves as a tool for rapid improvement of bulk SiC growth. Each crystal defect is a message about a growth issue. Interpreting these messages promptly is key.

A traditional quality feedback loop involves puck wafering, wafer-level inspection, and a subsequent feeding of quality measurements back to the crystal growth team – a process that often takes months, with the message arriving too late to take corrective measures. The original wafer sequence in the puck is frequently lost, hindering efforts to trace the stack of defect formation in the puck. The puck scanning keeps the information and shortens the feedback loop to just a few hours. Now growth teams can inspect the furnace output almost instantly (grinding is still needed), and adjust parameters prior to starting the next growth cycle. For the first time, producers can quantitatively measure

The benefits of puck scanning extend well beyond immediate cost savings. It also serves as a tool for rapid improvement of bulk SiC growth. Each crystal defect is a message about a growth issue. Interpreting these messages promptly is key.



➤ Figure 3. Profitability plot of a puck processing. It shows profit as a function of wafer thickness, taking into account defect distribution, as well as wafering and polishing costs. Coloured curves represent the number of wafers obtained in each grade, while the white curve indicates the total monetary profit. In this example, the maximum number of premium-grade wafers is achieved at a thickness of 0.3 mm.

the effectiveness of recipe changes or furnace modifications on defect reduction.
After all, what gets measured gets managed.

As well as driving yield improvements in traditional production, we are working to open new possibilities. Let's now talk about the financial implications.

Down the production chain, the value of epi-ready wafers is graded by well-established metrics, that include defectiveness. Knowing the defect constellation while still at the puck stage makes it possible to predict these metrics in advance. This feature, currently in beta testing, is embedded within the YieldPro software coming with the new scanner. It lets users define custom wafer grades – such as Prime, Production, or Engineering – based on specific defect limits or existing industry standards. Using 3D puck scans, future wafers are auto-classified accordingly after the puck scanning. These grading protocols can be shared with downstream partners or customers.

This capability in turn allows manufacturers to evaluate puck processing profitability, factoring in defect levels, as well as wafering and polishing costs.

For example, the YieldPro software can build a profitability curve as a function of wafer thickness to assess how different wafer thicknesses influence financial gain (see Figure 3).

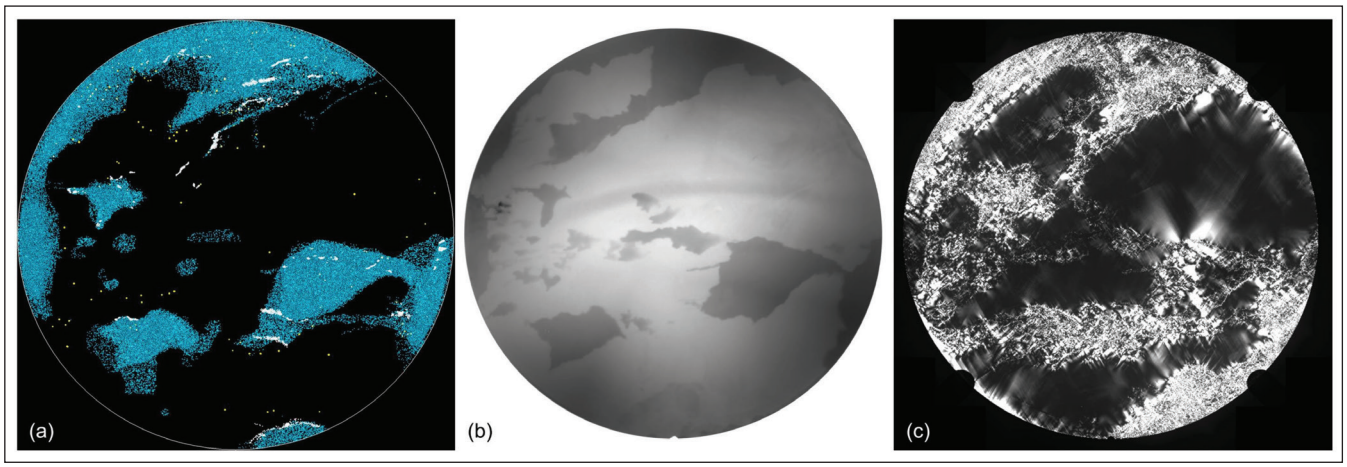
As trade of pucks between growers and wafer manufacturers increases, objectively determining their yields is becoming increasingly important. Thanks to an assessment of quality at the puck level – before wafering begins – manufacturers of SiC substrates can align their production with specific orders, customer requirements, and market conditions.

Given the significant benefits of the SiC Puck Scanner, it's not surprising that we are seeing swift interest in it. The upstream chain is now adopting automated quality control, following the trend established downstream.

Case Study: From puck to wafer – digital traceability in action

The SiC Puck Scanner can detect a wide range of defects: polytypes, micropipes, voids, inclusions, dislocation clusters, microcracks, and more. While the device is not a substitute for post-wafering inspection, as it's possible that some minor defects

> "The success of SiC in power electronics and e-mobility depends on detecting defects at the earliest stages. From a cost perspective, preventing defective material from propagating into processing is essential. It is reassuring that PVA and Scientific Visual are addressing this challenge with a dedicated metrology tool."
>
> *Jochen Friedrich, Head of Materials Department, Fraunhofer IISB*



➤ Figure 4. Example of correlation between SiC puck inspection and wafer inspection (a) 1mm-thick layer taken from the SiC Puck 3D twin at 1.62 mm depth, (b) the corresponding wafer under UV light, (c) the same wafer analysed by dislocation and stress mapping.

may go undetected, it provides an essential first line of defence. During the scanner's development, we continuously evaluated the accuracy of its performance by studying the correlation between puck inspection results and wafer-level defects through end-to-end case studies. While most of the tested material remains under NDAs, we received permission to disclose one case involving one of the thickest pucks we inspected.

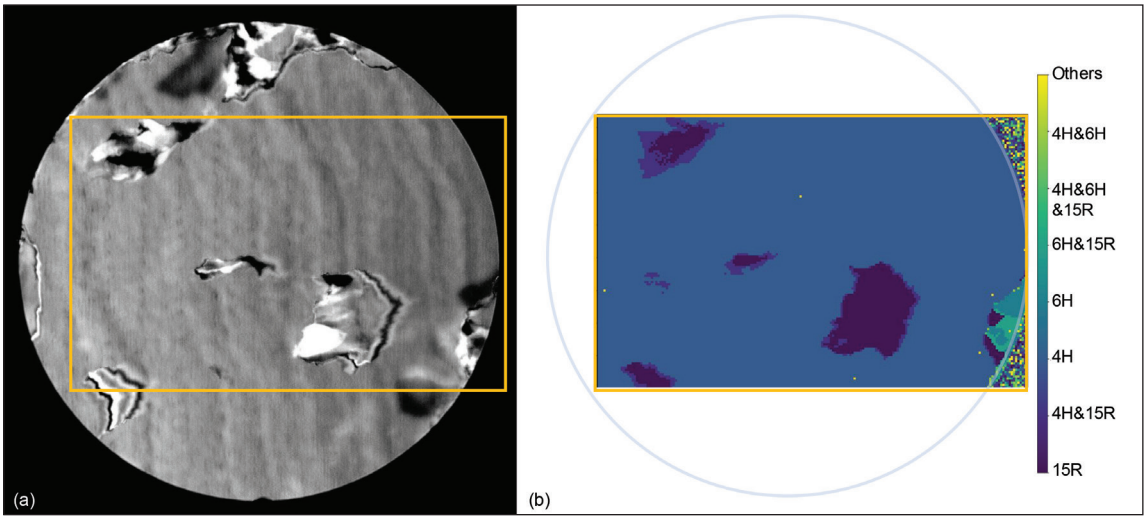
A 150 mm-diameter, 40.7 mm-thick SiC puck was scanned in SiC Puck Scanner to generate a full volumetric defect map. It was then sliced into 1 mm-thick wafers and analysed with traditional wafer inspection methods: Raman spectroscopy, UV illumination and near-infrared photoluminescence imaging. By tracing initial wafer orientations and positions within the puck, we were able to reconstruct detected defects layer by layer for the above techniques, and correlate them with the initial puck scan.

Results demonstrated a strong correlation between the defects detected in the puck and those observed in extracted wafers (see Figures 4 and 5). As expected, the characterisation revealed polytype regions, dislocation walls, and inclusions present in the sample – but not individual dislocations.

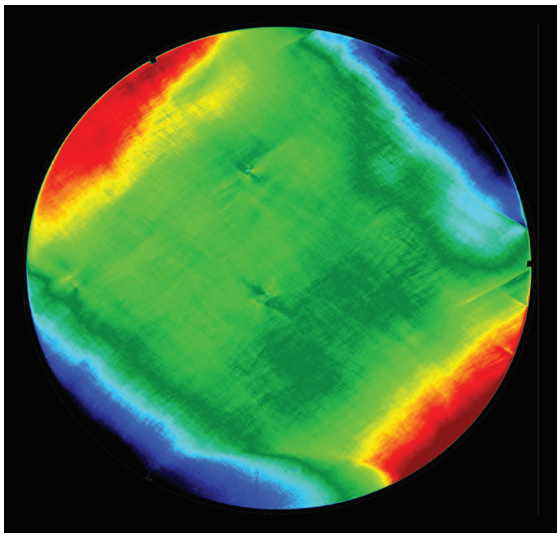
Finally, the produced wafers were inspected for stress using SIRD SiC 200 – Scanning InfraRed Depolarization stress-measurement technique (see below). This allows one to bring the volumetric defect results and post-wafering stress measurement into one 3D model (on the cover page), and study the correlation between internal defects and stress level in the material, which paves the way for multi-method metrology.

SiC-Wafer-Stress Metrology: The SIRD SiC 200 system

Stress measurements at the wafer level can be performed using new PVA TePla's SIRD SiC 200 Scanning Infrared Depolarisation tool. This tool provides fully automated, quantitative stress mapping across a broad range of dopings and materials (see Figure 6). Because the entire measurement and evaluation process is recipe-based and features



➤ Figure 5. Example of correlation between SiC puck inspection and wafer inspection: (a) Raw image of 65 µm-thick layer at 1.62 mm depth revealed by the SiC Puck scanner, (b) Raman heat-map of part of the resulting wafer with thickness 1 mm.



➤ Figure 6. Shear stress map measured by the SIRD SiC 200 system. The map shows the shear stress distribution inside the 150 mm SiC wafer, with large, extended stress fields at the outer edge and smaller defect-induced stress fields.

automated wafer handling, no operator intervention is required. This ensures reliability and repeatability at scale and supports 24/7 fab production. Achieving this level of automation is challenging; however, our team at PVA TePla draws on more than 25 years of experience in 300 mm silicon metrology.

Quantifying stress within a wafer is critical because stress correlates with defect growth and results in geometric deformations, such as bow and warpage. These deformations significantly reduce yield and impair device performance and reliability. By providing rapid, non-destructive, operator-independent stress analysis, the SIRD SiC 200 system enables customers to identify hidden risks before they escalate into costly problems. The SIRD SiC 200, having the ability to detect stresses at as low as 100 Pa, is therefore essential.

High sensitivity in stress measurements is crucial because process control requires detecting minuscule changes in the stress field for effective and reliable monitoring of each step. Additionally, this sensitivity enables the detection of defects inside the wafer, from micropipes to threading dislocations. This is possible because each defect causes a characteristic surrounding stress field. Measuring stress also offers valuable insight into process monitoring, from crystal growth to epitaxial-layer deposition. Each of these processes leaves a distinct stress fingerprint embedded within the wafer. This information becomes increasingly important as wafer sizes increase and process control windows narrow.

The SIRD SiC 200 system can be deployed in fabs to monitor the SiC substrate production process in its entirety – from measuring substrate-level stresses during crystal growth to detecting defects during epitaxy monitoring. After configuring a dedicated recipe for each process step, the system automatically measures and analyses wafers to calculate key indicators such as stress distribution and defect count. No operator access is necessary, because everything operates via SECS/GEM and overhead transport systems, in compliance with SEMI GEM300 standards.

Advanced metrology is set to revolutionise the SiC crystal industry as profoundly as it transformed the automotive and electronics manufacturing sectors earlier. Paradoxically, while the later stages of semiconductor production have embraced automated metrology, digital twins, and data-driven quality feedback loops, the early stages – crystal growth, inspection, and wafering – still largely depend on intuition and manual judgment.

We are glad to witness a gradual shift in this landscape. At Scientific Visual and PVA TePla, we are helping shape that future, delivering innovations that provide measurable, real-world value. Early-stage defect detection, yield optimisation, and objective quality grading are no longer optional – they are essential for any company striving to compete in the SiC space.

With our solutions, manufacturers are empowered to reduce waste, boost throughput, and secure a clear competitive advantage. But adopting advanced metrology is about more than improving quality – it means forging a supply chain that is resilient, transparent, and ready for the future. Getting rid of unnecessary processing translates into a lesser environmental footprint of SiC substrate production. As the industry evolves, those who invest in early-stage inspection and digital traceability will stand best poised to lead not only in innovation but also in sustainability.

SiC's future depends on intelligence and precision from the very start of the production chain. We are proud to be at the forefront of this development.

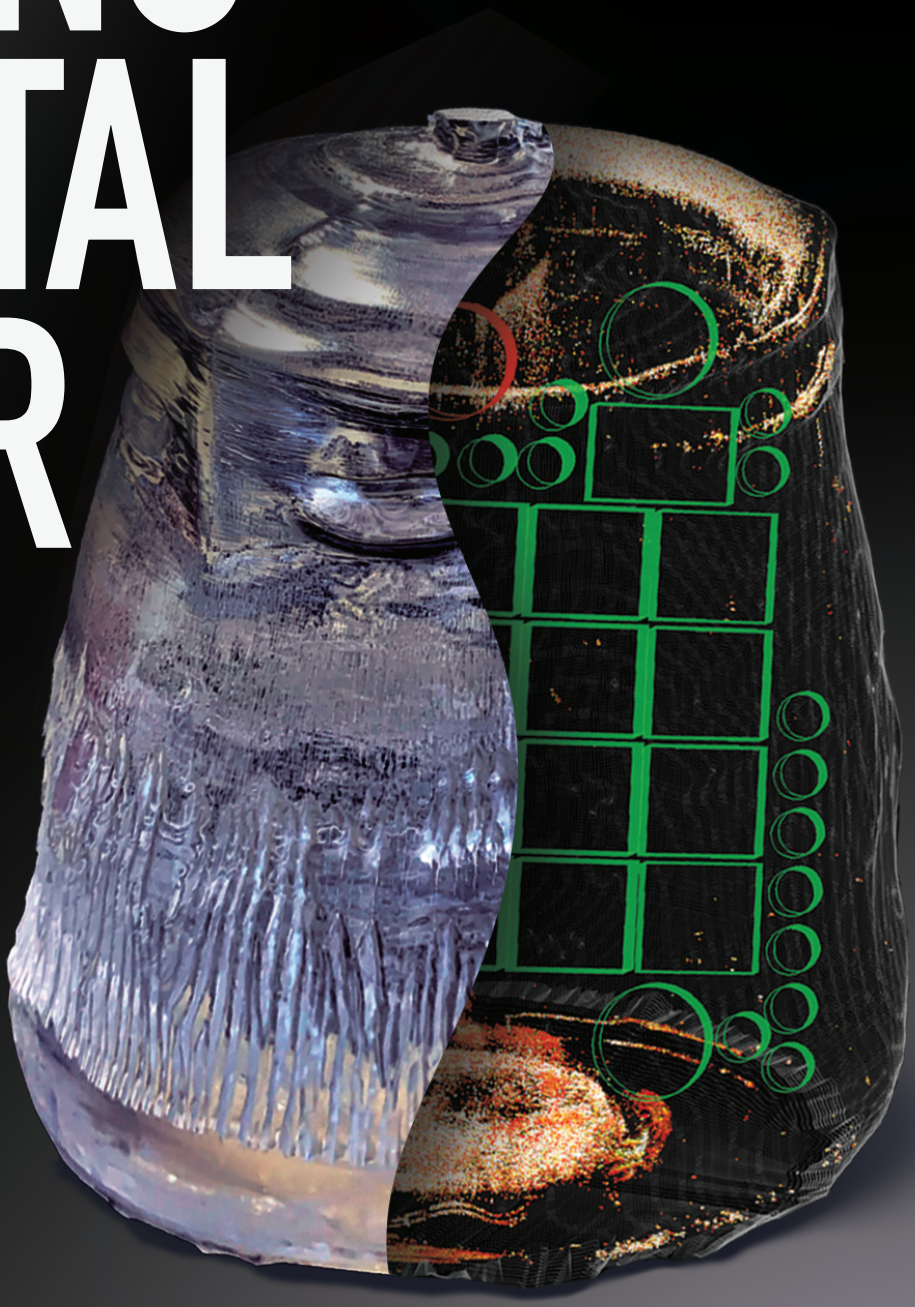
We gratefully acknowledge the professional collaboration and timely support from Lapmaster Wolters (Switzerland, Germany) for puck wafering, Ntek Latent Technologies Inc. (Taiwan) for wafer surface preparation, VisionTec (Singapore) for wafer optical and photoluminescence characterisation, and the PVA TePla Tech-Hub team (Germany) for Raman measurements.

Ready to elevate your SiC production? Contact us for a demonstration or visit us at SEMICON Europa, Booth C1531.

FURTHER READING

- FAQ on SiC Puck Scanner
- SIRD Wafer Stress Measurement
- PVA TePla Metrology Portfolio

GETTING CRYSTAL CLEAR

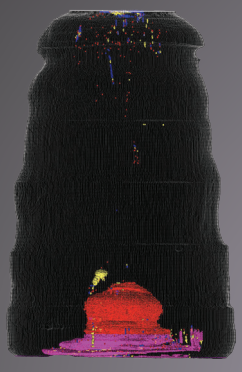


Automated quality control of industrial crystals

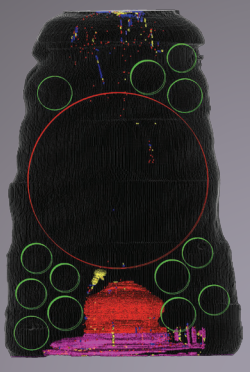
At Scientific Visual, we transform crystal data into actionable insights. From watch covers to 300-kg raw boules, our Swiss-engineered scanners reveal microscopic defects within the crystal volume before machining begins. This enables fabs to recover more usable material, avoid costly downstream losses, and improve crystal growth faster through early-stage defect identification.

Explore data-driven crystal processing.
Visit scientificvisual.ch today.

Unprocessed crystal



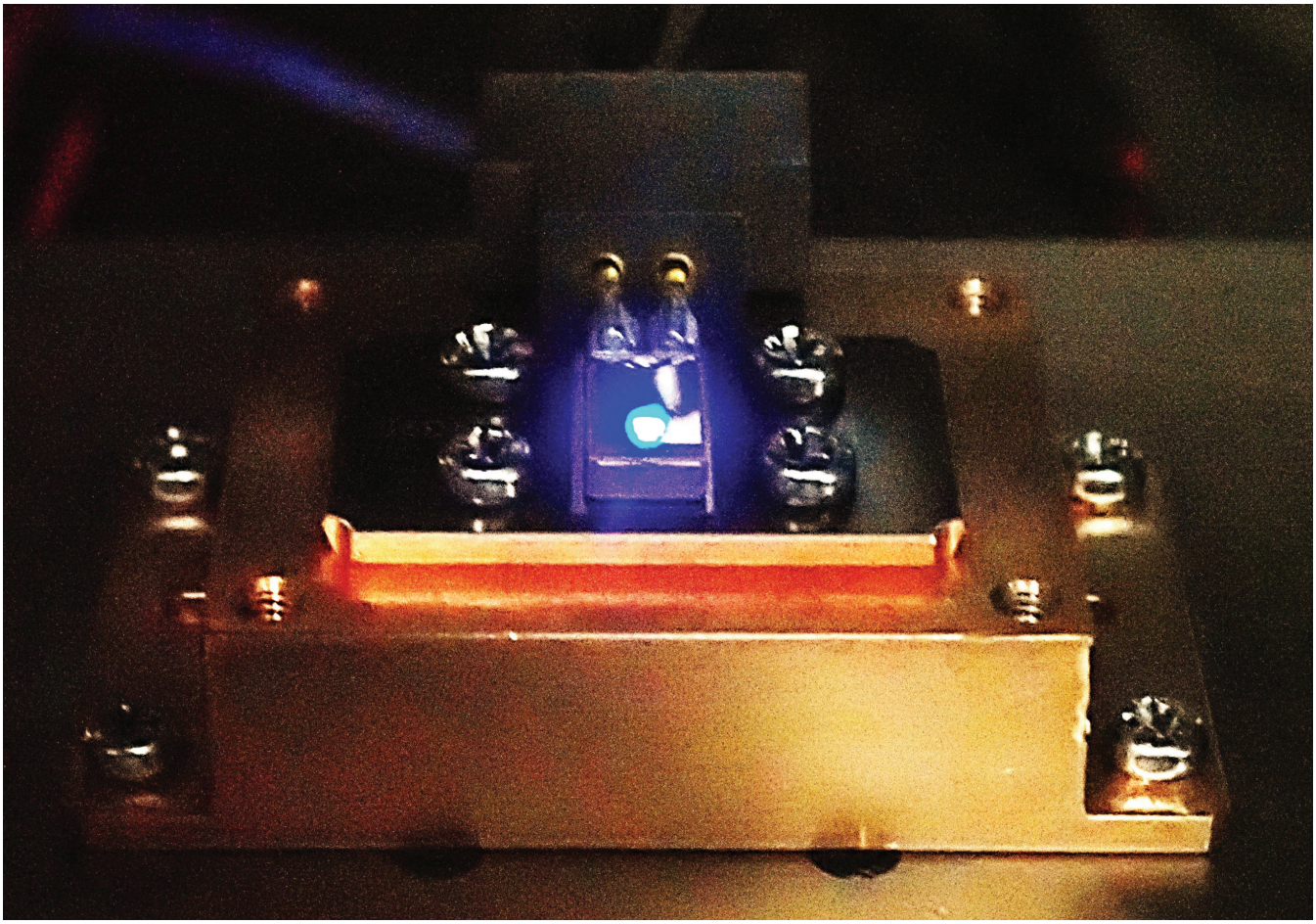
3D scan with defect map



Coring plan and graded end items

Scientific Visual

Sapphire CaF2 SiC LBO LT LN Laser crystals



Breakthroughs in blue and green laser diodes

More powerful and efficient GaN-based lasers are aiding displays and simplifying copper processing

BY RYOTARO KONISHI, YOJI NAGAO, TSUYOSHI HIRAO, KATSUHIRO KISHIMOTO, TERUYUKI MORITO, TOMONORI MORIZUMI, YOSHITAKA NAKATSU, TOMOYA YANAMOTO AND SHIN-ICHI NAGAHAMA FROM NICHIA CORPORATION

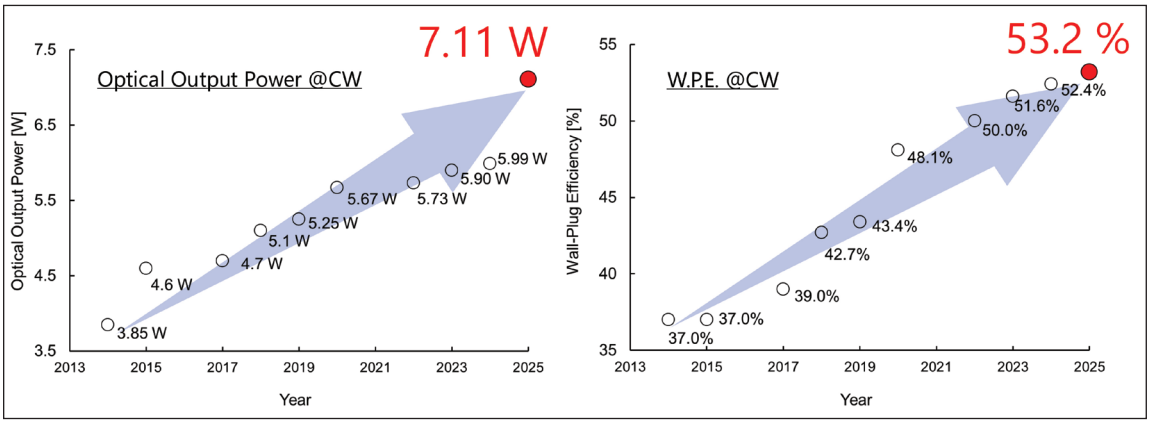
RECENT IMPROVEMENTS to GaN-based laser diodes (LDs) are positioning these sources as pivotal technologies in various applications. Opportunities have emerged in displays and laser processing, thanks to increases in the efficiency of this class of laser, along with a narrowing of its spectral width and the advent of exceptional reliability.

Within the display industry, the high efficiency and output power of GaN-based blue and green LDs are contributing to improved colour reproduction and brightness in digital cinema projectors, laser TVs, and large laser projectors. In addition, these emitters are supporting the development of high-performance RGB laser-light sources, enabling a wider colour gamut and enhanced visual experiences.

Meanwhile, in the industrial domain, high-output-power blue LDs are significantly enhancing laser processing capabilities, particularly for challenging materials like copper. These powerful sources are enabling high-precision and efficient metal welding, cutting, and processing, opening new fields in manufacturing and processing technology. They include opportunities in sectors such as the automotive industry.

Technological advances in blue lasers

As is often the case with compound semiconductor technologies, improvements to the performance of GaN LDs have taken place over many years. Nichia, as the pioneer and leading producer of GaN LDs, has driven these advancements.



➤ Figure 1. Nichia's history of the 455 nm blue LDs.

The development of blue LDs, pioneered by our company, began in earnest in the early 2000s, with the first successful demonstration in 2001. Back then, lasers delivered a modest optical output of just 5 mW. Thanks to rapid advancements, the first watt-class LDs were introduced in 2007. By 2022, we realised another impressive milestone in the history of the GaN LD, the first device surpassing a wall-plug efficiency of 50 percent.

Increases in the wall-plug efficiency and optical output of these blue LD chips have not come in the form of a handful of big jumps, but steady improvements over many years. This progress is attributed to both technological innovation and optimisation of the manufacturing processes (see Figure 1).

Our 455 nm blue LDs have a mere 2 nm spectral width, concentrating almost all their optical energy within this narrow range, which is approximately one-tenth of the spectral width of conventional LEDs. This capability to convert half of the electrical input power into laser light within a range of just 2 nm highlights the efficiency of our technology. However, this efficiency still lags behind the best GaAs-based LDs, indicating room for further improvement.

The manufacture of our LDs begins by loading a 2-inch c-plane freestanding GaN substrate into an MOCVD reactor and depositing an epitaxial stack consisting of *n*-type layers, and the active region, and finally *p*-type layers. Subsequent etching of the *p*-side of this epiwafer creates a ridge structure, to which we add *n*-type and *p*-type electrodes (see Figure 2). Production of the laser is completed with the addition of mirrors, created by cleaving the wafer and coating the bare facets with dielectric mirrors.

To minimise optical absorption losses, we meticulously design the optical confinement structure of our epitaxial stack. This careful consideration is crucial for ensuring that our LDs have a high efficiency and performance. In the final step of the laser manufacturing process, we employ a junction-down method to mount our chips into TO-Can packages. This approach trims thermal resistance and enables optimal heat dissipation.

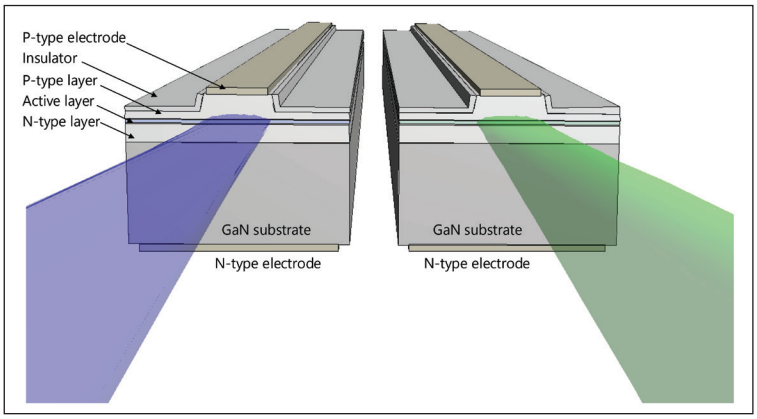
Earlier this year, we announced a 455 nm blue laser with an optical output of 7.11 W and a wall-plug efficiency of 53.2 percent, under a drive current of 3.5 A (see Figure 3). These record-breaking figures have been realised through improvements in chip design that include reducing internal absorption losses, enhancing carrier injection efficiency, trimming operating voltage by reducing resistance, and decreasing thermal resistance by expanding the cavity length.

One of the standout characteristics of our blue lasers is their exceptional reliability. Based on a lifetime test lasting 5,000 hours at a rated current of 3.5 A, we estimate a lifetime that exceeds 30,000 hours (see Figure 4). Thanks to this reliability, our blue LDs are expected to last significantly longer than conventional lamp light sources, which typically require replacement after a few thousand hours.

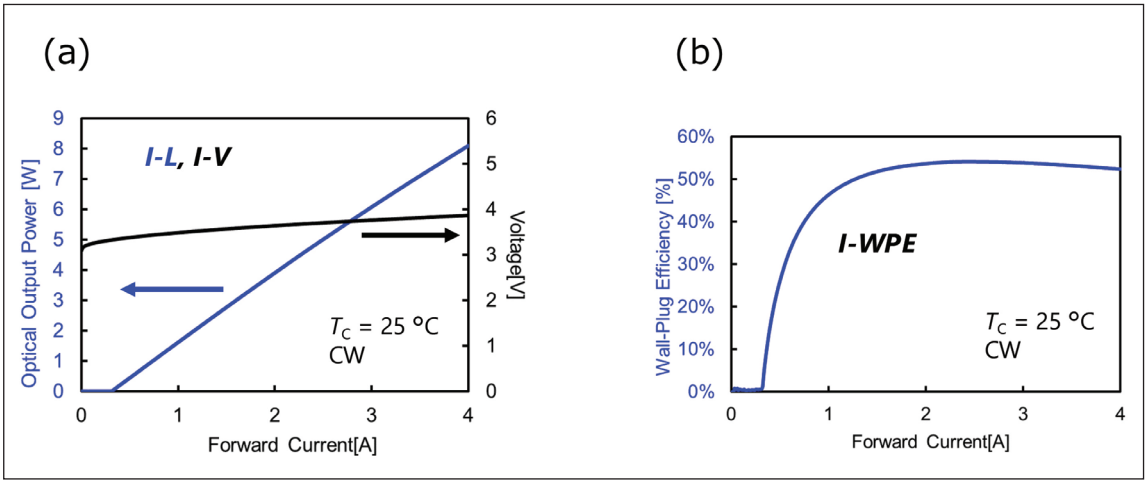
To accommodate various output requirements, multiple blue LDs can be packaged together. This approach creates light sources with optical outputs ranging from 20 W to 100 W. Recently, there has been a global shift from lamps to solid-state light sources, and this trend is expected to continue. At the heart of this transformation are LDs, which are anticipated to become mainstream across all markets.

Gains for green lasers

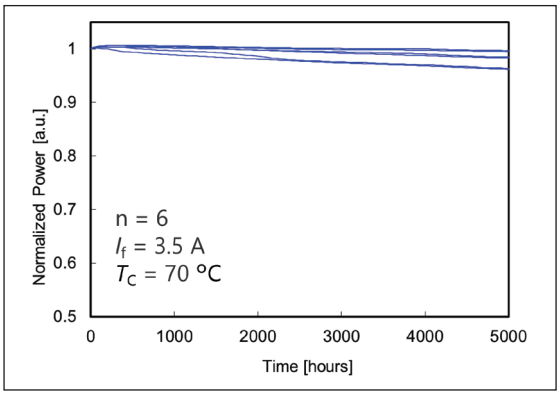
Another recent triumph is the increase in the wall-plug efficiency of our 525 nm green LDs to just beyond 25 percent. Note that these lasers can fully



➤ Figure 2. Nichia's multimode laser diodes.



➤ Figure 3. (a) Current-light (I-L) and current-voltage (I-V) characteristics of blue LD under CW operation at 25 °C. (b) Current-WPE (I-WPE) characteristics of blue LD under CW operation at 25 °C.



➤ Figure 4. Lifetime test results of blue LDs under an automatic current control of 3.5 A CW operation at a case temperature of 70 °C. Operating current is normalised by its initial value.

cover the standards of digital cinema in the green region.

Key to our success is tackling the challenges related to piezoelectric polarisation, which reduces the overlap between electrons and holes and thus lowers the radiative efficiency. Our solution involves thinning the active layer. Although piezoelectric polarisation still occurs, a sufficiently thin active layer helps to mitigate the reduction in light emission.

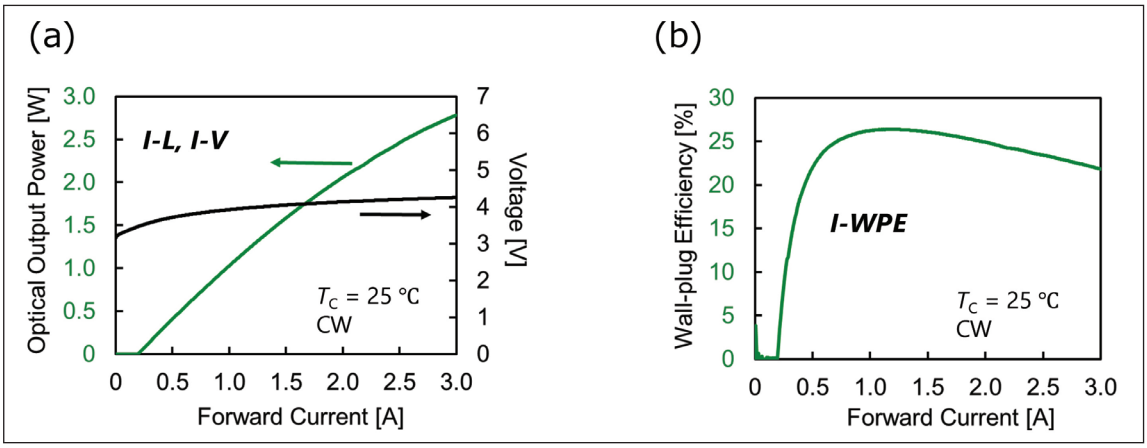
We have observed and recorded the advantages of thinning the quantum wells within our green LDs. Our 525 nm device that benefits from a low threshold current produces an optical output of 1.97 W at a 25.2 percent wall-plug efficiency when driven at 1.9 A (see Figure 5). Additionally, we have begun in-house production of GaAs-based red LDs alongside the blue and green LDs reported here, enabling us to respond flexibly to customer demands and accelerate the development of RGB products.

Processing with blue lasers

In addition to contributing to display brightness, blue LDs are playing a crucial role in laser processing. Since 2017, we have been developing lasers for copper processing, successfully commercialising ultra-high-power lasers that far exceed those used for displays.

As the mobility industry transitions from gasoline vehicles to electric vehicles (EVs), demand for copper processing is increasing. Copper plays a critical role in EV performance, due to its high conductivity, and this material is widely used in motors, batteries, and other key electrical components.

Traditionally, the processing of metals with lasers has involved the use of sources in the infra-red. But



➤ Figure 5. (a) Current-light (I-L) and current-voltage (I-V) characteristics of green LD under CW operation at 25 °C. (b) Current-WPE (I-WPE) characteristics of green LD under CW operation at 25 °C.

that's not a great spectral domain for copper, which is a challenging material to process, due to its high thermal conductivity. Switching the wavelength from the infra-red to the blue is highly beneficial, with the energy-absorption efficiency in the blue more than ten times higher than that in the infra-red. Due to this, blue lasers enable more efficient energy transfer, making them very attractive candidates for processing copper, particularly in welding and cutting applications, where they are adept at meeting precision and speed requirements.

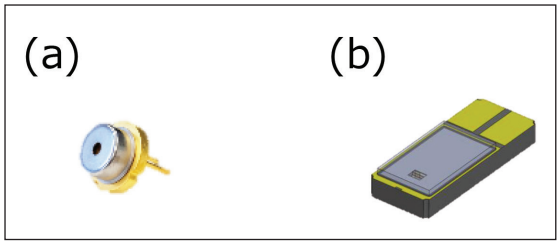
Thanks to these advantages, we expect our sources to lead to high-efficiency laser processing, stabilisation of the molten pool, and a reduction of spatter in copper welding. Realising a higher output power from blue LDs is essential for this purpose. Our developments have led to optical outputs exceeding 25 W for blue LDs used in processing applications, compared with about 7 W for display use.

To increase the optical output from a single chip, we have made significant changes to its structure. While display LDs have a cavity length of 1500 μm and a chip width of 150 μm, for processing we are promoting a far larger chip: it has a length and width of 4000 μm and 400 μm, respectively. These changes aim to reduce thermal resistance and accommodate higher currents.

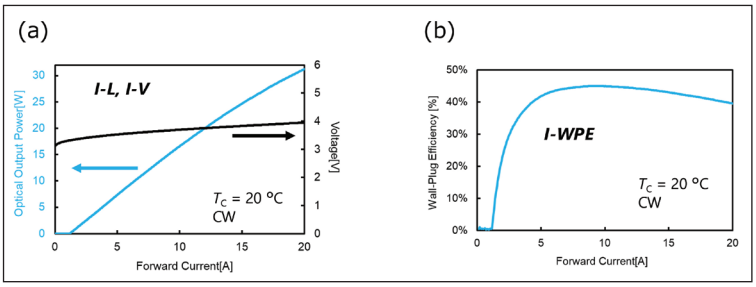
Another change we have made is to switch from a conventional Φ9 package to a surface-mount device package, further reducing thermal resistance (see Figure 6). This refinement improves the thermal management capabilities of the LDs, enabling higher-current applications. While the rated current for display use is 3.5 A, for processing LDs are operating at 16.5 A, and delivering an optical output of 26.8 W at a wall-plug efficiency of 41.6 percent (see Figure 7).

We have demonstrated the reliability of our high-output blue LDs through rigorous testing. Undertaking lifetime tests at a rated current of 16.5 A, we have found that power degradation is less than 1 percent after 2,500 hours (see Figure 8). This result indicates that it's possible to enjoy stable copper processing during prolonged operation, making our laser diodes a reliable choice for industrial applications.

In conjunction with our advances in high-output blue LDs, we are developing blue direct diode laser modules for copper processing. These modules, incorporating multiple high-output blue LDs, produce optical outputs exceeding 800 W from a fibre with a core diameter of 110 μm. This 800 W model is currently in preparation for mass production, and is expected to significantly enhance laser processing capabilities across various industrial applications.



➤ Figure 6. (a) ϕ9 package. (b) Surface-mount device package.

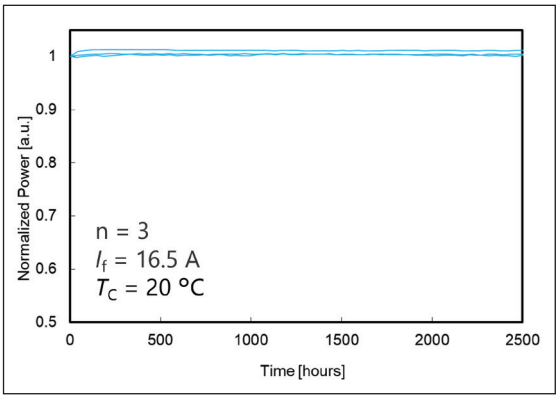


➤ Figure 7. (a) Current-light (I-L) and current-voltage (I-V) characteristics of blue LD for processing under CW operation at 20 °C. (b) Current-WPE (I-WPE) characteristics of blue LD for processing under CW operation at 20 °C.

Looking ahead

Improvements in efficiency will be a valuable asset, not only for projector applications but also for various markets that include the industrial sector. The shift from traditional light sources to laser light sources is already underway, and is expected to accelerate further.

Looking ahead, our commitment to ongoing improvement and innovation in the field of laser technology remains steadfast. We anticipate that LDs will spur advances in various industries, and pave the way for new applications that leverage their unique characteristics.



➤ Figure 8. Lifetime test results of blue LDs for processing under an automatic current control of 16.5 A CW operation at a case temperature of 20 °C. Operating current is normalised by its initial value.

FURTHER READING

- R. Konishi *et.al.*, "High-power GaN-based edge-emitting laser diodes", Proc. SPIE **13366** 133660C (2025)
- K. Kishimoto *et.al.*, "Development of highly efficient blue and green edge-emitting laser diodes", Proc. SPIE **12886** 1288609 (2024)

High-bandwidth energy-efficient networks

Arrays of VCSELs promise to provide incredibly efficient LiFi communication at terabit data rates

BY DENISE POWELL FROM THE COMPOUND SEMICONDUCTOR CENTRE, HOSSEIN SAFI FROM THE UNIVERSITY OF CAMBRIDGE, AND MOHAMED MISSOUS FROM INTEGRATED COMPOUND SEMICONDUCTORS

IN A WORLD that's strongly focused on boosting energy generation to fulfil future demand, many overlook the benefits that come from trimming energy consumption. But those of us that are working within our community tend to know better, viewing device and material optimisation as levers with the potential to increase power conversion efficiency at the system level, and ultimately reduce the overall energy requirements from the grid.

It's unlikely that you'll be surprised by forecasts for a substantial increase in the energy consumption of data centres over the coming years. According to the International Energy Agency, in 2024 the global energy usage of data centres totalled around 415 TWh, equating to 1.5 percent of global consumption – and by 2030, demand is expected to have more than doubled to 945 TWh, primarily driven by AI-enabled data centres, for which energy demand is expected to quadruple. Ericsson has published related, additional insight in a whitepaper. That document includes a prediction that energy usage of digital services will continue to increase by 10 percent every year until 2030, by which time it will have climbed to reach approximately 1,100 TWh. To put these figures into perspective, in 2023 Scotland's energy consumption totalled 64.5 TWh.

Growth of energy consumption at this rate is clearly unsustainable. It has led McKinsey to predict that there is going to be a data centre energy supply deficit of more than 15 GW in the US alone, due to demand for AI-ready capacity. And this view is not an outlier, with many online sources claiming that

demand will outstrip supply, leading to electricity constraints in some areas. This is a problem that stretches far beyond Net Zero ideology; we simply do not have the energy-generation capability demanded by future architectures.

Unfortunately, energy is not the only problem facing the communications sector. Another issue is that the radio-frequency wireless networks are becoming increasingly congested, due to 4K video streaming, as well as a growing number of connected IoT devices – those in use are expected to reach 40 billion by 2030. In locations where there are a high number of connected devices in proximity, such as in a smart-city or smart-factory environments, the background noise level is higher, so stronger signals are needed from each device.

The congested RF network is very much a last mile problem. Today it's not necessarily a significant challenge to deliver high-speed connectivity to a building, but it is becoming increasingly difficult to ensure a high-speed connection to every device on a specific network. And failing to do so is not an option, as AI-enabled Industry 4.0 solutions demand high-speed, uninterrupted connectivity of machines and devices.

If the AI revolution is to become a reality, there can be no delay in rolling out resilient indoor networks that combine low power consumption with high transmission speeds. Thankfully, compound semiconductor-based solutions can meet these requirements, addressing the ever-growing problems of increasing energy usage and the need for high bandwidth.

Move over RF

The ideal solution has to tick quite a few boxes. It must be based on an architecture that: has a low energy consumption; delivers high bandwidth for ultra-capacity connectivity; is resilient, secure and scalable; and offers lower costs, for both ownership and operation.

Judged against this list, optical wireless communication (OWC) is a compelling candidate. Compared with RF solutions, this technology, using light to transfer data, offers a far broader spectrum for greater flexibility, immunity to interference, cost-efficiency and ease of deployment.

There's both a strength and a weakness of OWC, associated with its line-of-sight communication. This characteristic makes it ultra-secure, with transmission confined, particularly in premises where access is restricted – but this can lead to problems in open spaces, as links can be disrupted or affected by environmental variations.

Note that when security is at a premium in indoor applications, OWC can easily be combined with additional security measures, such as quantum key distribution.

Within the OWC market, the fastest growing segment is Light Fidelity, often shortened to LiFi. Responsible for coining this term is the the University of Cambridge academic Harald Haas, who first demonstrated LiFi in a TED Talk in 2011, where he employed conventional LEDs for data transmission. In 2012 Haas co-founded pureLiFi, taking a Chief Scientific Officer role at this start-up, the first organisation to commercialise LiFi technology. The year after pureLiFi founded, it launched the Li-1st system, following an Innovate UK part-funded project with Cisco.

Latest generation of LiFi systems modulate infrared light in order to transmit data. This form of communication delivers far higher data rates than currently deployed WiFi systems, which have a practical data rate in the region of 1 Gbit s^{-1}. Note that for indoor networks, one should avoid paying too much attention to published WiFi speeds, as they have little relevance, unless the router is used by one device at any one time. Anyone who has tested their home WiFi speed in frustration, using apps such as Speedtest, will unfortunately be familiar with the downsides of a shared bandwidth in a busy household.

Complimenting WiFi with LiFi could have extraordinary implications for future interactions with others, machines, devices and infrastructure.

Resilience through versatility

Whilst LEDs may appear to be an optimum choice for LiFi, allowing ordinary lighting infrastructure to double up as a transceiver (with some infrastructure modifications), the performance of these emitters is suboptimal, in terms of achievable bandwidth. In this regard lasers are far more attractive, with laser-based LiFi offering transmission speeds a hundred times faster.

Not all laser sources are well-suited to LiFi, or even OWC. Key criteria are a low-energy consumption, high bandwidth, ease of manufacture, reliability and scalability – and when judged against that list, there really is no match for the VCSEL.

Strengths of the VCSEL for deployment in the majority of OWC networks include high modulation speeds, good power-conversion efficiencies, ease of fabrication, and a significantly lower cost-of-manufacturing per die.

With edge-emitting and distributed-feedback lasers, output power scales linearly with die length and demands the support provided by more bulky subsystems that have a higher power consumption. These issues are avoided with VCSELs, thanks to vertical light emission out of the plane of the substrate. It is relatively easy to combine many VCSELs in arrays, enabling a hike in output power without a significant increase in die size.

Another attribute of the VCSEL is its Gaussian beam profile. This enables far-more-efficient links than those realised with LEDs, as a less powerful source provides the same transmitted power across the optical link.

Also featuring on the long list of impressive characteristics of the VCSEL is its tremendous flexibility, in terms of device architectures. Design engineers can consider single-mode devices through to stacked-junctions; the epitaxy and device options available are vast; and there's also array scalability.

Certainly within REASON

Following the development of niche single-mode VCSELs for quantum clocks and magnetometers, UK partners Integrated Compound Semiconductors (ICS) in Manchester and the Compound Semiconductor Centre (CSC) in Cardiff joined forces with the LiFi team at Cambridge University, headed up by Haas under a future telecoms project.

Working together, we embarked on a two-year project called REASON:

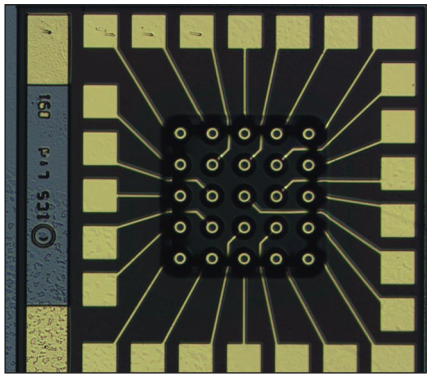
Realising Enabling Architectures and Solutions for Open Networks. Part-funded by the Department of Science Innovation and Technology – and benefitting from a total budget just shy of £12 million, as well as the involvement of UK-wide academic, RTO and industry heavy-weights – we have been focused on reshaping the future of open network architectures, with efforts directed towards openness and greater interoperability.

To put the scale of our activity into perspective, VCSEL development, coupled with novel modulation techniques, have been included as one of three strands under one of six work packages. Our focus in the work package was to develop custom device solutions for multiple-access networks, including advanced radio, optical-wireless and fibre technologies. The other two strands included GaN RF power amplifiers and InP optical amplifiers.

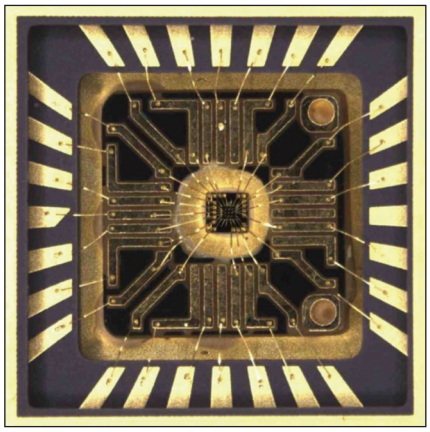
An attractive option for transmitting vast amounts data is spatial multiplexing. For this form of transmission, which is key to increasing aggregate data throughput, there's a preference for individually addressable monolithic VCSEL array architectures. But this source brings challenges, in terms of both epitaxy and device fabrication. To ensure closely matched emitters, it is crucial to ensure uniform epitaxy and fabrication processes.

Through project REASON, we have developed small-scale, 5 x 5, addressable VCSEL arrays (see Figures 1 and 2). We began at 940 nm, before progressing to 980 nm and 1060 nm.

Building on quantum programmes, ICS designed epitaxial structures for three wavelength platforms and new



➤ Figure 1. Addressable 5 x 5 VCSEL array.



➤ Figure 2. VCSEL array mounted on a prototype package for characterisation.

device layouts, and also undertook array fabrication. CSC contributed high-uniformity epitaxy processes, crucial to formation of quantum devices and beneficial to array matching. The team at University of Cambridge set the specifications for the arrays, applied modulation techniques, and integrated beam-shaping to characterise VCSEL array performance in a custom OWC link.

Our best-performing devices were those emitting at 940 nm. These VCSELs met the per-element output power target of 5-10 mW at a drive current of 12-16 mA, with a threshold of 1.2 mW and a 10 GHz 3dB bandwidth. Notably, these devices were produced using established processes to demonstrate the feasibility of basic monolithic arrays for OWC. Their fabrication did not require significant optimisation of the epitaxy processes or device platform development. The variants at 1060 nm suffered from optical losses, due to a lack of full optimisation of the epitaxial process at this wavelength.

Using bespoke modulation and multiplexing techniques, the team at Cambridge University demonstrated record free-space aggregate data rates of over 300 Gbit s^{-1} for monolithic VCSEL arrays, at close to half the energy consumption of commercial WiFi systems. The results provide a promising platform for our collaboration to continue to develop and push the capability closer to 1200 nm for greater peak-powers.

The widely accepted eye-safe threshold for lasers is around 1400 nm. For wavelengths further into the infra-red, radiation is absorbed by the cornea without being focused on the retina.

According to theoretical research, the permissible peak-power for laser sources varies not only with wavelength, but also with beam waist, which can be controlled by adjusting the aperture width of the VCSEL. The maximum transmit power of the laser source increases linearly until around 1150 nm. Beyond that, the maximum transmit power increases exponentially until 1200 nm, before returning to a linear relationship.

The permissible peak-power curve, which depends on both wavelength and beam waist, equips system and device designers with significant flexibility in optimising system performance and cost, based on the application. For indoor applications, VCSEL arrays for LiFi ideally emit at wavelengths beyond 1200 nm. However, device and drive parameters can be tailored to ensure that the lasers are eye-safe at lower wavelengths.

Thanks to the versatility of VCSEL architectures, researchers can explore quite a few different opportunities. For example, one of the discrete single-mode 850 nm VCSELs developed during the QFoundry project to scale-up manufacturability of quantum photonic components has been characterised by the team at Bangor University in a 2.5 m OWC link. This effort involved a comparison with an off-the-shelf multimode VCSEL. The QFoundry VCSEL, fabricated by ICS using CSC epi, outperformed the off-the-shelf variant, boasting a lower relative intensity noise and twice the date rate – 38 Gbit s^{-1}, compared with 19 Gbit s^{-1} for the multimode device – at an eye-safe transmitted optical power of around -1.47 dBm.

Based on our results, we are viewing VCSEL-based architectures as a possible pathway towards Tbit s^{-1} communications networks. There is a case to be made for VCSEL-based LiFi to support sustainable infrastructure for 6G and rapidly growing AI-enabled datacentres for a post-fibre paradigm, whilst addressing the increasing problem of congested RF networks. Over the coming years, there will be an increase in demand for low-latency networks. They are fundamental to extended-reality immersive

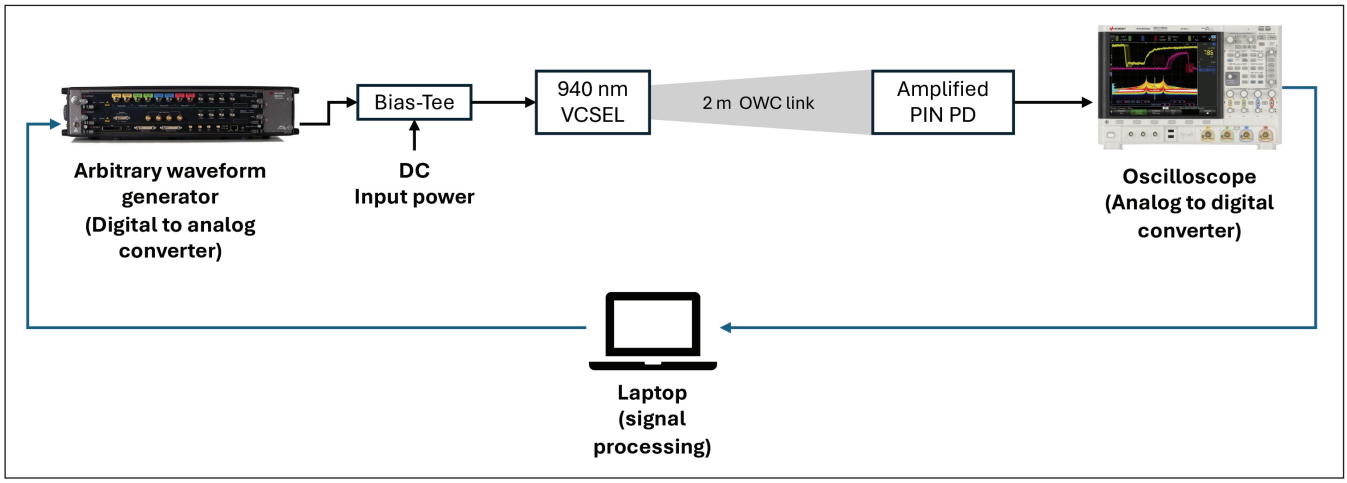


Figure 3. Schematic of the free-space link architecture developed at the University of Cambridge for data transmission

technologies that include augmented, virtual and mixed reality experiences, as well as holographic communication. VCSEL-based LiFi systems offering ultra-high bandwidths provide a pathway towards wide-scale adoption of multi-user setups, without impacting the user experience.

We expect the deployment and wider adoption of VCSEL-based LiFi communication networks to follow typical new technology adoption product lifecycles. There is still work to do at all levels of the supply chain, from epitaxy development through to device platform, package and system optimisation. Packaging technologies are going to have a big role to play in minimising parasitic capacitance, and VCSEL-based LiFi will require new customised package development.

Prototype devices are already offering a step-change in bandwidth versus power consumption. Thanks to this, when first-generation systems are available, they are likely to be adopted in applications at a higher margin, where bandwidth is absolutely critical. A subsequent generation of products will set to increase the bandwidth at the device level, as well as optimising modulation techniques.

Ultimately, whilst standards have embraced LiFi, there is still work to do in establishing appropriate business models, and interaction across infrastructure and network providers is needed to ensure that LiFi becomes a mainstream technology in commercial and residential environments.

CS can have the comms cake and eat it

Today, there is much debate over the value of Net Zero and AI. But the compound semiconductor community should welcome these revolutions with open arms.

What's beyond doubt is that future networks will need to embrace a fusion of transmitter technologies, and the majority of them will involve compound semiconductors, including architectures based on GaAs, GaN and InP. And as these networks roll out, there's a compelling case for reducing optical fibre usage and migrating to lower-power systems through efficient OWC networks. A shift in this direction has the potential to improve both the CapEx and the OpEx of the datacentres of tomorrow.

Low-cost VCSEL array-based OWC architectures, offering lower power consumption for the same output power, can also aid satellite networks that provide communication links. Deployment of these links is rising fast, and eye-safety is not a concern out in space, enabling greater flexibility in system and device design.

Recently, there has been a significant shift in the global political landscape, with more countries looking to have greater domestic capability surrounding the manufacture of key technologies. This upheaval brings an urgency for sovereign components in UK telecoms infrastructure that can offer resilience and enhanced security characteristics. Meeting this goal is not trivial, as historically there not been a high level of interaction across the communications supply chains. Our groundbreaking REASON project is helping to address this weakness by establishing collaboration across materials and device development, through to systems developers and network providers.

Our work forms part of our industry's efforts in ensuring that compound semiconductors will capture every piece of the communications pie. Whether it's long-distance or short-range links, or connected or wireless networks, III-V devices, including VCSELs for LiFi, are a key technology.

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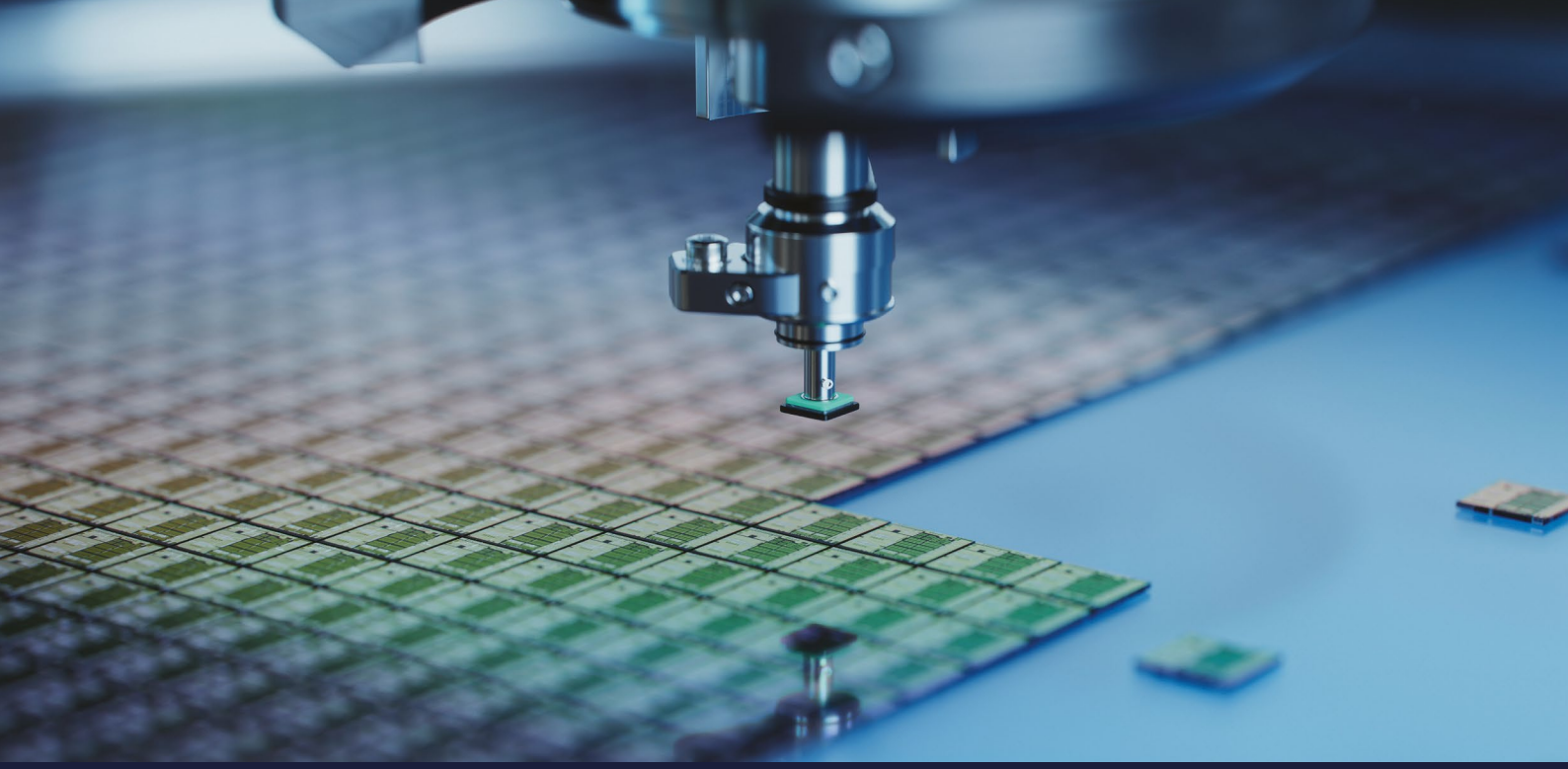

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When every microsecond counts

Infineon's CoolSiC JFET is a new class of switching device that enables power distribution systems to be immune from delays

BY ROBERT ROESNER AND BARIS YILDIRIM FROM INFINEON TECHNOLOGIES

ONCE an electrical circuit is overloaded, you would expect a circuit breaker to respond immediately and reliably. But in today's fast-moving, electrified systems, such as electric trucks, AI data centres and modern industrial manufacturing plants, 'immediately' is no longer fast enough. In these scenarios every microsecond counts, and standard protective devices, such as fuses, relays, and moulded case circuit breakers, are failing to keep up within the rapidly growing world of AC and DC power systems. Those components were designed for a different era, when millisecond response times were fast enough. But they lack the speed, precision, and intelligence demanded by today's systems, shortfalls that have serious consequences.

Take a modern electric truck, for example: if a fault occurs during high-speed charging or rapid acceleration, and the device isn't disconnected quickly, critical components can overheat, threatening to damage power electronics and even cause a fire. Similarly, in an AI data centre, if a short circuit occurs on a power bus and isn't quickly isolated, an entire rack can be crippled, resulting in data loss, downtime and expensive hardware damage.

Both these examples illustrate how vulnerable modern systems are to electrical faults, especially now that vehicles, factories, and data infrastructures are increasingly electrified, compact, and complex. This changing landscape places new demands on power distribution systems: higher voltages, faster protection, and significantly tighter safety margins.

Alternatives with flaws

Solid-state protection devices based on the MOSFET are already commercially available. They address many shortcomings of mechanical switches – including contact wear, slow reaction times, and imprecise thresholds – but they have their limits, especially in high-voltage or high-current applications.

While SiC MOSFETs outperform their silicon-based cousins by offering better overall switching performance, plus a higher efficiency and improved thermal characteristics, even this class of transistor cannot fully close the gap when it comes to robustness under fault conditions or sustained operation in linear mode. One significant downside of the SiC MOSFET is its relatively high on-resistance ($R_{DS(ON)}$), leading to the need for larger devices that drive up both cost and complexity. To manage the resulting thermal load or enable higher current levels, designers have to resort to parallelizing multiple devices, an approach that demands deep product and system expertise.

Furthermore, SiC MOSFETs have limitations in avalanche robustness and linear-mode stability, constraining the fault-handling capabilities of these devices under extreme conditions, like pre-charging or un-clamped inductive switching. These limitations force engineers to compromise, rather

than deploying an optimal solution – trading speed for safety, or efficiency for design simplicity. But in modern systems where fault isolation has to happen as fast and reliably as possible, these trade-offs aren't just inconvenient, they're potential points of failure.

For next-generation applications, such as solid-state circuit breakers, battery disconnect switches, and hot-swap electronic fuses in AI data centres, system designers need something more: a technology that combines an ultra-low $R_{DS(ON)}$ with thermal stability in linear mode and robust avalanche behaviour to ensure fast, safe and reliable performance under harsh conditions.

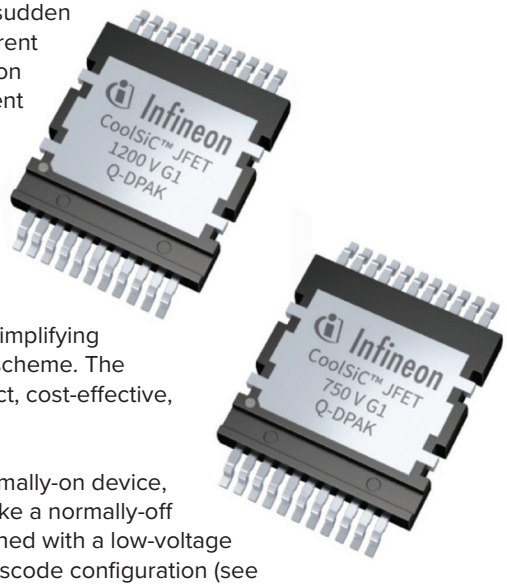
Built to protect

To overcome the limitations of mechanical protection devices and extend the capabilities of solid-state switches, our company, Infineon Technologies, has developed a new type of discrete switching device: the CoolSiC JFET (see Figure 1). Based on a JFET cell design, our device takes a different approach to high-voltage switching in power distribution. It is designed specifically for modern applications, where milliseconds are too long and conventional MOSFETs are falling short. Rather than building on conventional MOSFET architectures, this device is engineered for efficiency, ruggedness, and simplifying system design in demanding environments.

The CoolSiC JFET is based on a purely vertical trench structure (see Figure 2) that minimises conduction losses and maintains a stable electrical performance, even under changing load conditions. This form of transistor addresses significant weaknesses associated with MOSFET-based solutions, which often require larger cooling elements or derating to stay within safe limits. In contrast, the CoolSiC JFET retains its efficiency across a wide load range, including continuous line operation, a condition that occurs in electric vehicle battery disconnects and server power distribution.

One reason for the consistent efficiency stems from how the SiC JFET conducts current. Unlike the SiC MOSFET, which relies on a thin surface-level *n*-channel, current flows through the entire volume of the semiconductor. Due to bulk conduction, JFETs are normally on, resulting in reduced channel resistance (see Figure 3). While the drift region – which blocks voltage – limits both device types similarly, JFETs benefit from lower resistance in the channel itself. Thanks to this, SiC JFETs have a lower overall $R_{DS(ON)}$ for the same chip size, enabling systems to run cooler. This translates into better efficiency in high-voltage designs.

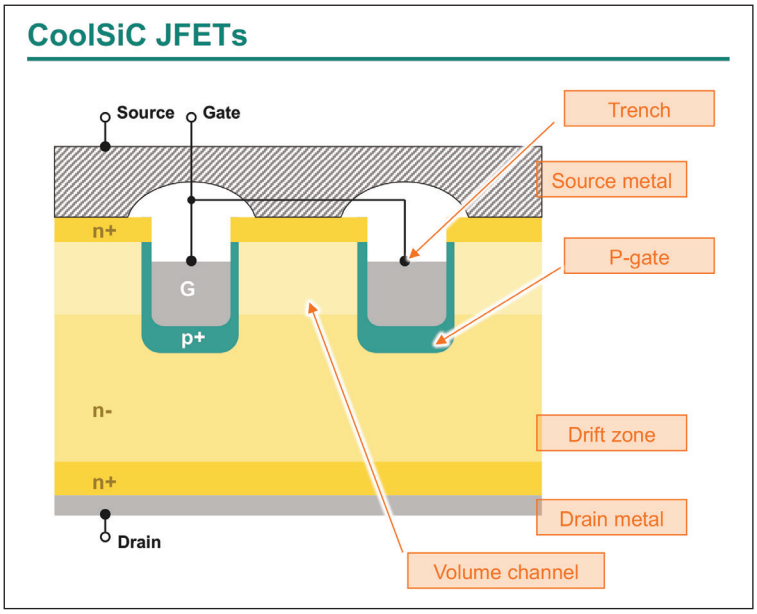
Another attribute of the SiC JFET is its avalanche ruggedness. In fault scenarios such as short circuits and overloads, this device responds quickly and consistently, handling sudden voltage spikes and current surges. This fast reaction helps prevent equipment failure, and mitigates risk at the system level. In addition, the JFET can absorb high energy internally, eliminating the need for elaborate external clamping circuits and simplifying the overall protection scheme. The upshot: a more compact, cost-effective, robust design.



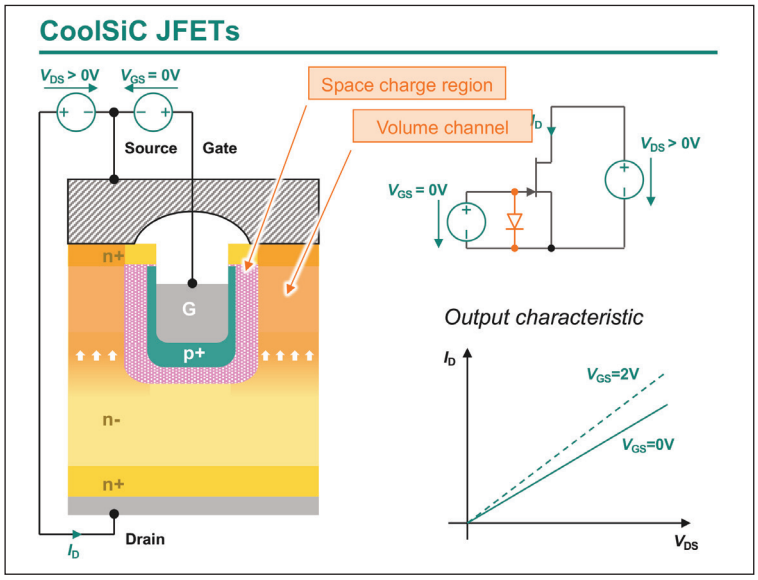
➤ Figure 1. The discrete CoolSiC JFET family has been developed with solid-state power distribution applications in mind.

Though naturally a normally-on device, the JFET can behave like a normally-off switch when it's combined with a low-voltage silicon MOSFET in a cascode configuration (see Figure 4). In this configuration, the pairing provides the benefits of JFET conduction and ruggedness, alongside the control characteristics of MOSFETs. Merits of the MOSFET-JFET combination include reliable and predictable switching behaviour, as well as essential features for applications like solid-state breakers or industrial protection switches. And another strength enjoyed by designers is the flexibility to implement the JFET-MOSFET into existing control architectures with minimal changes.

Note that other arrangements also yield impressive results. For example, a pair of JFETs is an attractive option in systems requiring bidirectional current flow, such as battery disconnect switches or AC protection devices. In this case, two JFETs in a source-to-source configuration offer directionality, while increasing design flexibility and facilitating integration into complex architectures.



➤ Figure 2. Volume conduction and vertical current flow enable low resistance and efficient high-voltage switching.



➤ Figure 3. In normally-on JFETs, current flows through the volume (or bulk) channel with minimal resistance.

Equally important is the device's packaging. Housing die in a Q-DPAK surface-mount package with top-side cooling allows for efficient heat extraction away from the chip (see Figure 5). It's an arrangement that simplifies heat management and helps realise a higher power density, particularly valued in applications where space and cooling capabilities are limited. Helping to excel in these regards is our .XT interconnect technology – it provides additional support associated with transient thermal performance, and helps to handle demanding load cycling, ensuring long-term reliability, even in harsh environments.

It would be wrong to view CoolSiC JFETs as simply drop-in replacements for MOSFET-based devices. They also offer design-level benefits for building more compact, more reliable protection with fewer external components and reduced system complexity. Whether in battery disconnect switches for electric vehicles, electronic fuses in AI servers, or fast-acting solid-state circuit breakers in industrial environments, the ability to respond quickly and reliably can make all the difference.

What engineers need to know

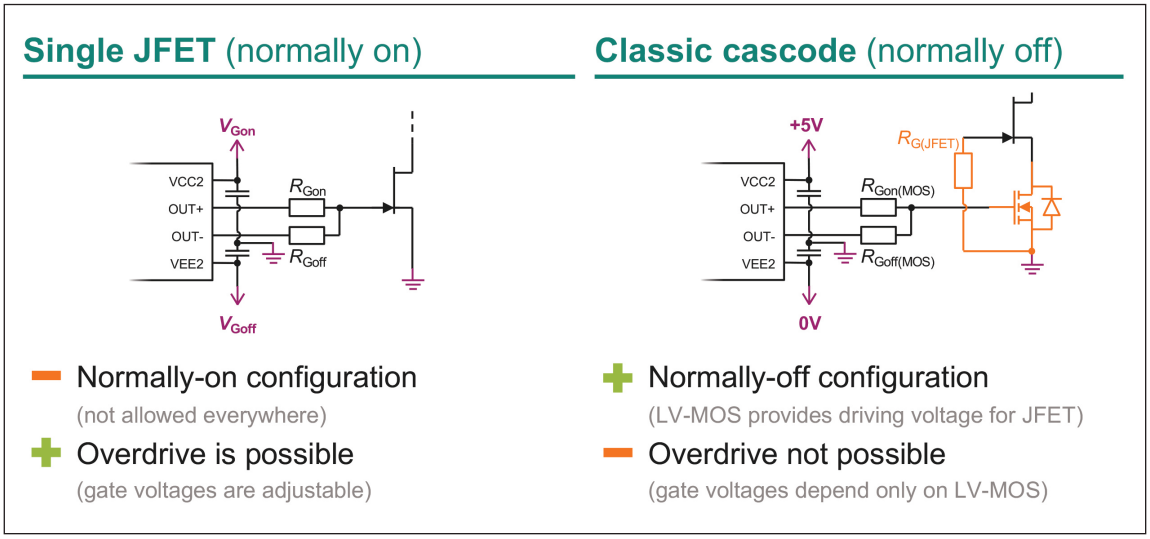
While CoolSiC JFETs offer many benefits for modern power distribution design, they don't behave exactly like conventional MOSFETs. In order to get the most out of them, engineers need to take a few key design aspects into account early in the process.

As these devices are often used in safety-critical systems, like electric vehicles or industrial power supplies, it is crucial to understand how they behave under fault conditions. For example, if the gate signal fails or a short circuit occurs, the system must remain safe. It is important to consider known safety standards at an early stage, including those from the International Electrotechnical Commission and Underwriters Laboratories.

However, one of the most significant points is the control of the device. When a JFET is used in a cascode configuration, it's crucial to carefully control the gate signals. Doing so prevents unwanted switching operations, especially during rapid voltage changes or when switching on. Other important goals for a designer are a good layout and a reliable clamping circuit to ensure safe and consistent operation of the switch.

It's also essential to avoid overlooking thermal design and mechanical details. Long-term reliability may be influenced by factors such as the PCB layout, the connection to cooling elements, and the way in which the device tolerates vibrations or temperature changes over time.

Thanks to top-side cooling, JFETs can dissipate heat more effectively than conventional packages, thereby simplifying thermal management – but only if the component is properly connected to a heat sink or copper area on the board. Design engineers need to note that early consideration of heat flow helps avoid issues later on. And these engineers should also be aware that testing and validation under real-world conditions is an absolute must in systems where safety is a top priority.



➤ Figure 4. In the cascode configuration, a MOSFET is added so that the JFET behaves like a normally-off device.

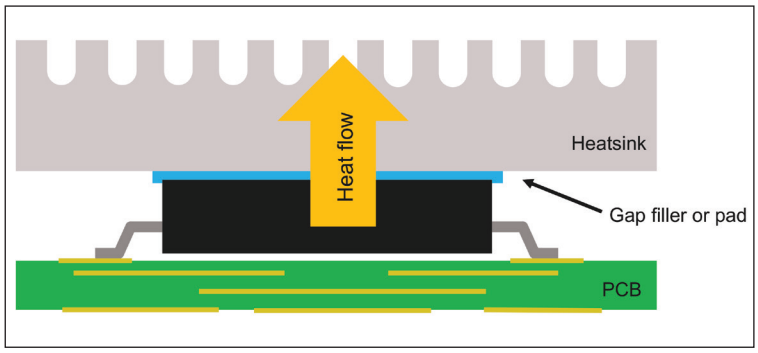
In short, the CoolSiC JFET offers a powerful combination of system simplicity, efficiency, and reliability, especially in designs where space is at a premium and response times critical. However, thoughtful integration is essential for unlocking new levels of performance in next-generation power systems. This advice applies to electric vehicles and AI data centres, and also to microgrids and renewable energy systems.

Keeping pace with tomorrow's systems

Some of the key trends in power supply systems are that they are becoming faster, more compact and increasingly software-defined. As a result, mechanical protection methods struggle to keep up. That's a disaster in today's highly electrified world, where every microsecond counts and reliability, speed, and safety are more important than ever. These needs are behind the launch of the CoolSiC JFET – a high-voltage switch that offer engineers new tools to meet modern system demands, while responding to faults instantly and reliably.

Whether protecting AI servers, disconnecting EV batteries, or enabling semiconductor-based power switches in industrial systems, JFETs help to build safer, smarter, and more easily scalable power supply architectures. By reducing system complexity and improving thermal performance, they also allow for more compact designs without sacrificing robustness.

Plans are now in place to expand the portfolio with additional package and module options, covering a broader range of applications and current ratings. For engineers developing next-generation electrified systems, this expanding family of devices offers an opportunity to rethink protection methods at the speed demanded by modern systems, and to make power distribution ready for what's next.



➤ Figure 5. The top-side cooled package simplifies cooling management.

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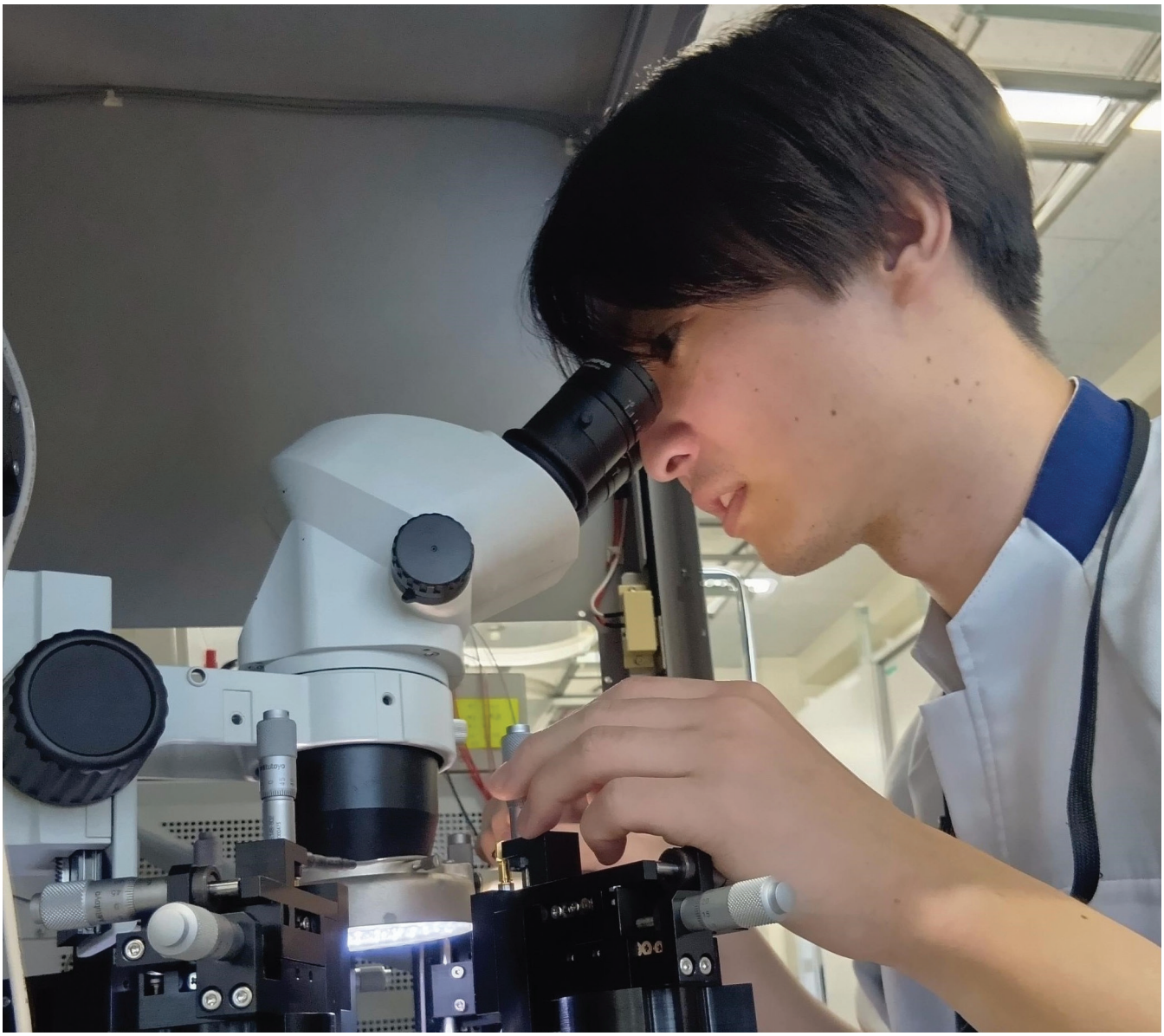


Cranking up the switching speed with a *p*-GaN shield

Adding a *p*-GaN shield to a vertical GaN-on-GaN transistor trims capacitance and enhances high-power, high-speed switching

BY NAOKI TORII, DAISUKE SHIBATA, MASAHIRO OGAWA, MASAO KAWAGUCHI, HIROYUKI HANDA, NAOHIRO TSURUMI, SATOSHI TAMURA AND YOSHIO OKAYAMA FROM PANASONIC

SALES OF power electronics are tipped to soar throughout this decade and beyond. Driving this trend is the increase in production of electric vehicles and the growth of data centres, which have more demanding power requirements due to the uptake of AI.

For every application using power electronics, an increase in their efficiency is beneficial. Gains may include an increase in driving range, a reduction in electricity bills, less heating, and a lower carbon footprint.

Due to these benefits that result from a superior efficiency, there is an increasing uptake of devices based on wide bandgap semiconductors. So far, those based on SiC have generated the most

revenue, with MOSFETs grabbing headlines for winning deployment in electrical vehicles.

However, despite enjoying much success, SiC devices have some significant deficiencies. They included the interface between SiC and SiO_2, which is far from perfect.

Avoiding these issues is the lateral GaN transistor, which is already netting significant sales by dominating the market for the fast-charging of mobile devices. One of the benefits of this class of device, which can be grown on large-area, low-cost silicon substrates, is that high levels of mobility are realised without doping. Instead, internal polarisation is exploited to produce a two-dimensional electron gas (2DEG).

This lateral device is a significant milestone for the GaN transistor, providing the first 'killer' application – premium fast-charging units for the likes of smartphones, tablets and laptops. But going beyond this is far from easy with these lateral devices, because it is very challenging to reach high values for output current and breakdown voltage and thus output power. With this device geometry, critical design considerations for high power are the area of the electrodes, and the spacing between the source and drain on the surface of the device.

Offering a very promising way forward is a new architecture, involving a shift from a lateral to a vertical geometry. With these more compact devices, which a number of teams have been developing from around the world over the last few years, source and drain electrodes are placed on opposite sides of the substrate, enabling design engineers to scale the power of the transistor while not significantly increasing its footprint.

Our company, Panasonic, is one of the trailblazers of the vertical GaN transistor. We have developed a variant that's a high-power vertical GaN JFET, which we refer to as a VJFET. It's produced using the re-growth of *p*-GaN/AlGaN/GaN channels.

For GaN devices to realise their full potential at the system level, where they promise to aid miniaturisation and trim loss, it is essential that they are capable of high-speed switching. Governing this key metric is the reverse-transfer capacitance – also known the capacitance between the gate and the drain – that impacts the mirror period required to charge the capacitance between the gate and drain.

Conventional VJFETs are held back by a high reverse-transfer capacitance, associated with opposing placement of gate and drain electrodes. But we have recently addressed this issue with a ground-breaking refinement to the device: the addition of a *p*-GaN shield on a normally-off GaN VJFET that's grown on a native substrate (see Figure 1 for details of its structure).

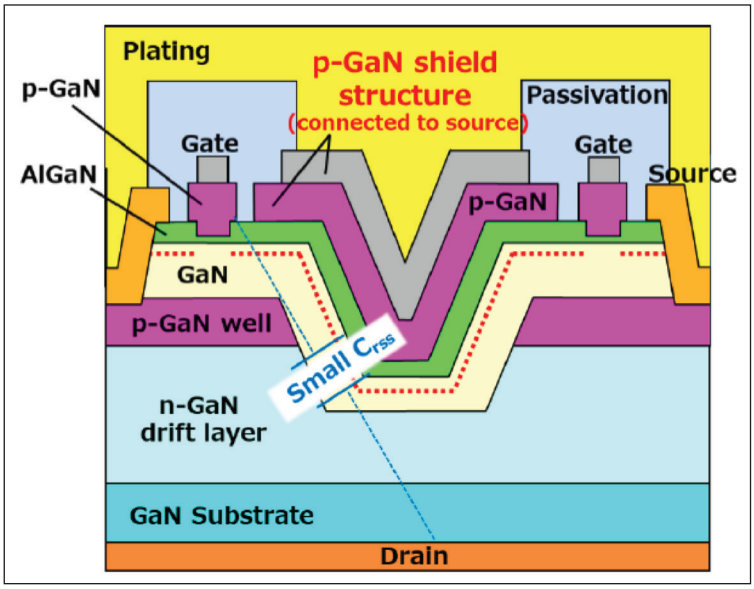
Simulation insights

To evaluate and understand the benefits and implications of this device, we have simulated its performance. This is benchmarked against the conventional VJFET that combines normally-off operation with a low on-resistance, and features a re-grown *p*-GaN gate/AlGaN/GaN structure formed on a V-groove.

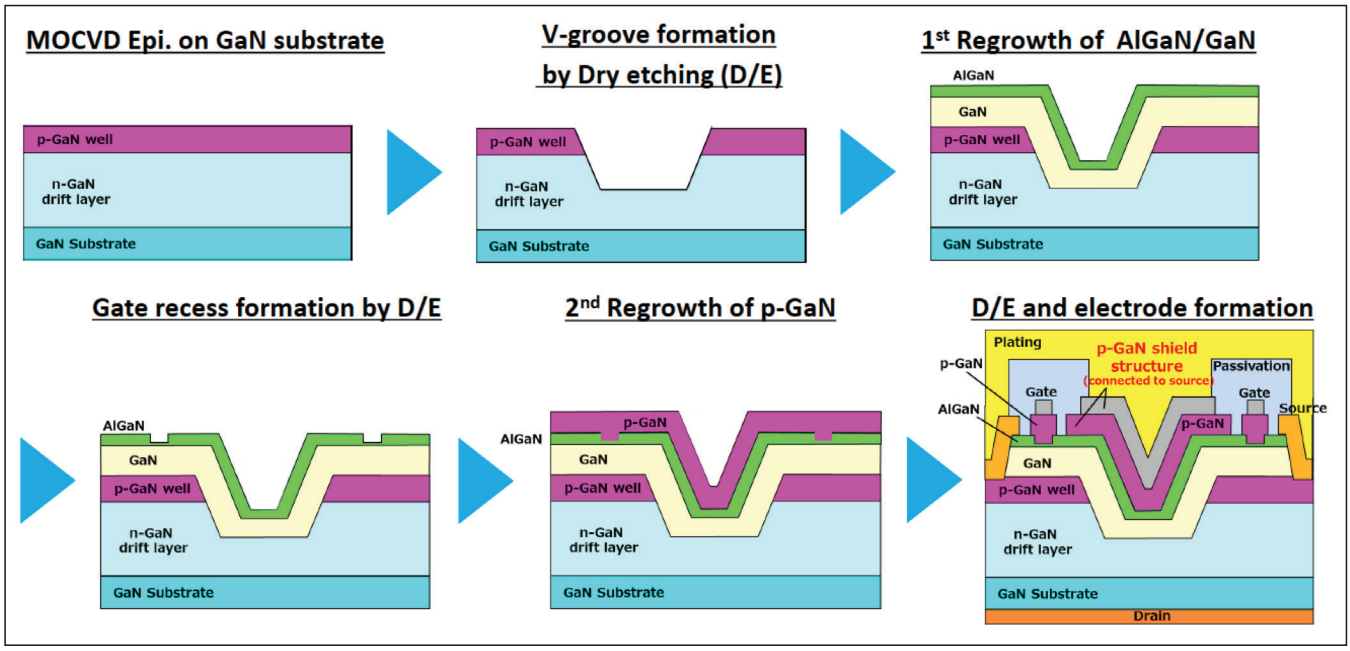
Our novel VJFET has a strategically introduced *p*-GaN shield over the V-groove that is at the same potential as the source. For this device, the gate is formed on the plane separately from the *p*-GaN shield structure. This design has a far lower reverse-transfer capacitance than its conventional counterpart, thanks to effective shielding between the gate and drain by the *p*-GaN well and the *p*-GaN shield structure.

Simulations of both forms of VJFET show that our refinement to this transistor delivers a substantial reduction in the reverse-transfer capacitance over a wide range of drain-source voltages. Over a range of voltages up to 500 V, our device has a reverse-transfer capacitance that's well below a picofarad, while its conventional counterpart has a value of many tens of picofarads. These simulations also show that shortening the length between the edge of the *p*-well and the *p*-GaN gate enables an additional reduction in the reverse-transfer capacitance.

Our simulations have also revealed that with our VJFET with a *p*-GaN shield, the thickness of the AlGaN barrier has a strong influence over normally-off operation and a low on-state resistance. By modelling this device, we have determined the profile of the conduction band and the density of the 2DEG, for a gate-source voltage of 0 V. This work shows that in the gate region complete depletion is realised with a 20 nm-thick $Al_{0.2}Ga_{0.8}N$ barrier layer. Meanwhile, in the slanted region, an $Al_{0.2}Ga_{0.8}N$ barrier that's 80 nm-thick enables the



➤ Figure 1. Panasonic's vertical JFET features a *p*-GaN shield structure that enables superior switching, thanks to a reduced reverse-transfer capacitance.

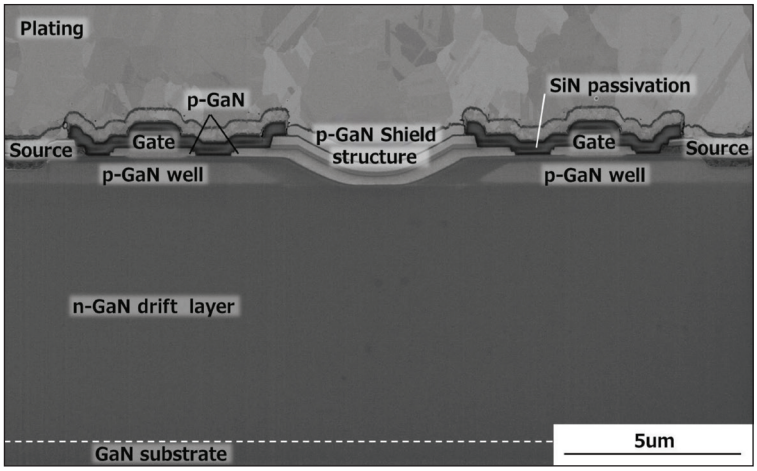


➤ Figure 2. Panasonic's process for the fabrication of its vertical JFET with a *p*-GaN shield structure.

formation of a high-density 2DEG and a low channel resistance.

Further findings from our simulations reveal that as well as slashing the reverse-transfer capacitance, our V-shaped *p*-GaN shield structure in the V-groove suppresses the off-state leakage current by relaxing the electric field at the *p*-GaN well's edge, where there is damage caused by the dry etching process. This work has also determined that increasing the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield reduces the electric field strength at the edge of the *p*-GaN well, thanks to a relaxing of the electric field by the *p*-GaN shield structure. There is a price to pay for this benefit, however: as the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield extends, there is an increase in the electric field strength at the bottom of the *p*-GaN shield.

Based on these findings, we have concluded that experimental investigations are needed to optimise the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield while realising a low off-state leakage current.



➤ Figure 3. A scanning electron microscopy image of a *p*-GaN shield vertical JFET.

Device fabrication...

Fabricating our novel VJFETs began by loading bulk GaN substrates into an MOCVD reactor and depositing a 7 μm-thick silicon-doped GaN drift layer with a carrier concentration of 1.3 x 10^{16} cm^{-3}, followed by a magnesium-doped *p*-GaN well with a carrier concentration of more than 1.0 x 10^{19} cm^{-3}. With this heterostructure, the blocking voltage should exceed 900 V.

The next steps in the fabrication process involved etching V-shaped grooves in the epiwafer with an inductively coupled plasma, and re-growth of $Al_{0.2}Ga_{0.8}N$ and GaN. We varied the thickness of the $Al_{0.2}Ga_{0.8}N$ barrier layer from 50 nm to 80 nm, and employed a thickness for this ternary of 20 nm under the gate, realised by partial removal with inductively coupled plasma etching.

To complete the fabrication of our VJFETs, we added a *p*-GaN epilayer, and selectively etched this to form the gate and *p*-shield structure. We then applied a selective etch to the $Al_{0.2}Ga_{0.8}N$/GaN/*p*-GaN well to form the source electrode. The final device features a Ti/Al source electrode, a Pd/Au gate electrode, a *p*-GaN shield electrode, and a Ti/Al/Ti/Pt/Au electrode on the backside of the GaN substrate (see Figure 2 for an overview of the fabrication process, and Figure 3 for a scanning electron microscopy image of our device).

... and characterisation

Electrical measurements of our transistors, which have an active area of 0.002 mm^2, reveal a threshold voltage of 1.5 V. The on-state resistance decreases with the thickness of the barrier layer, and for an 80 nm thickness, the product of

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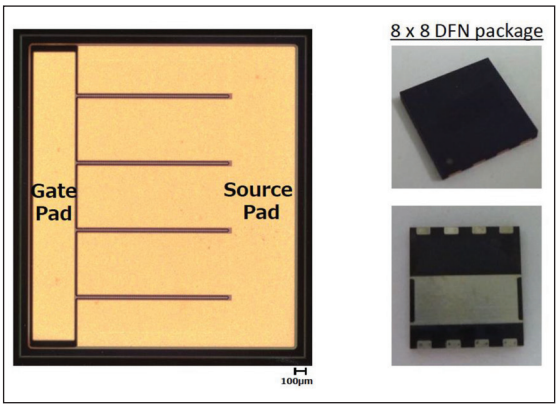

Figure 4. Designed for high-current operation, this *p*-GaN shield vertical JFET has a chip size of 2.9 mm by 2.6 mm.

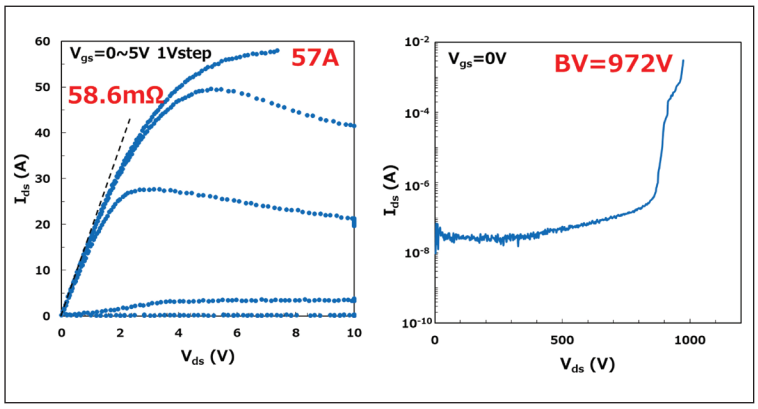

Figure 5. On-state (left) and off-state (right) DC output characteristics of the *p*-GaN shield vertical JFET.

on-resistance and area is 1.23 mΩ cm^2. Plots of off-state leakage current at a range of drain-source voltages show that the leakage is far less when the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield is 200 nm, rather than 0 nm or 400 nm. For the 200 nm distance, the drain-source voltage has little impact on leakage current, which is around tens of microamps per square centimetre.

We have also evaluated a 2.9 mm by 2.6 mm *p*-shield VJFET designed for high-current operation (see Figure 4). This device has a maximum drain current of 57 A, an on-state resistance of 58.6 mΩ, and a breakdown voltage of 972 V (see Figure 5). Encouragingly, at a drain-source voltage of 500 V, the reverse transfer capacitance is just 2.92 pF – that's less than one-eighth of the value for its conventional counterpart (see Figure 6). In addition, the input capacitance is lower, thanks to the reduced gate area.

A key figure-of-merit for our *p*-shield VFJET is the product of its on-resistance and its reverse-transfer capacitance. This figure is just 171 mΩ pF, less than that for commercially available SiC MOSFETs (see Figure 7).

Using an inductive load, we have investigated the switching performance of our *p*-shield VJFETs at 400 V and 20 A. Values for turn-on are 14.3 V ns^{-1} and 76.7 V ns^{-1} for our conventional and *p*-shield VJFETs, respectively. The turn-on loss is reduced by 75 percent compared with that for a conventional device.

Based on a wide portfolio of results, we can conclude that our novel VJFETs are promising candidates for serving in applications requiring high powers and high speeds.

This work was partly supported by 'Project for Acceleration of Social Implementation and Dissemination of Components and Materials for Realizing Innovative CO_2 Emission Reduction' of the Ministry of Environment of Japan.

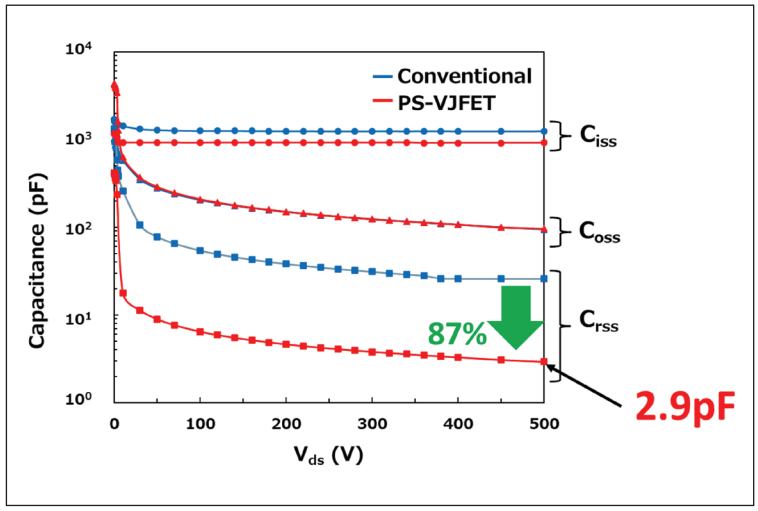

Figure 6. The *p*-GaN shield enables a substantial reduction in reverse-transfer capacitance.

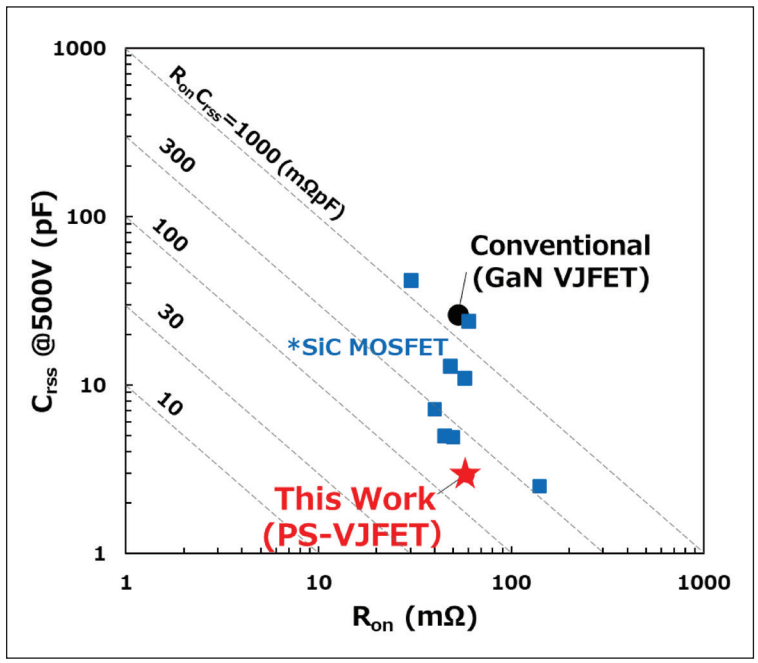

Figure 7. Benchmarking the Panasonic *p*-GaN shield vertical JFET against its conventional counterpart and 650 V SiC MOSFETs, using figures provided by data sheets.

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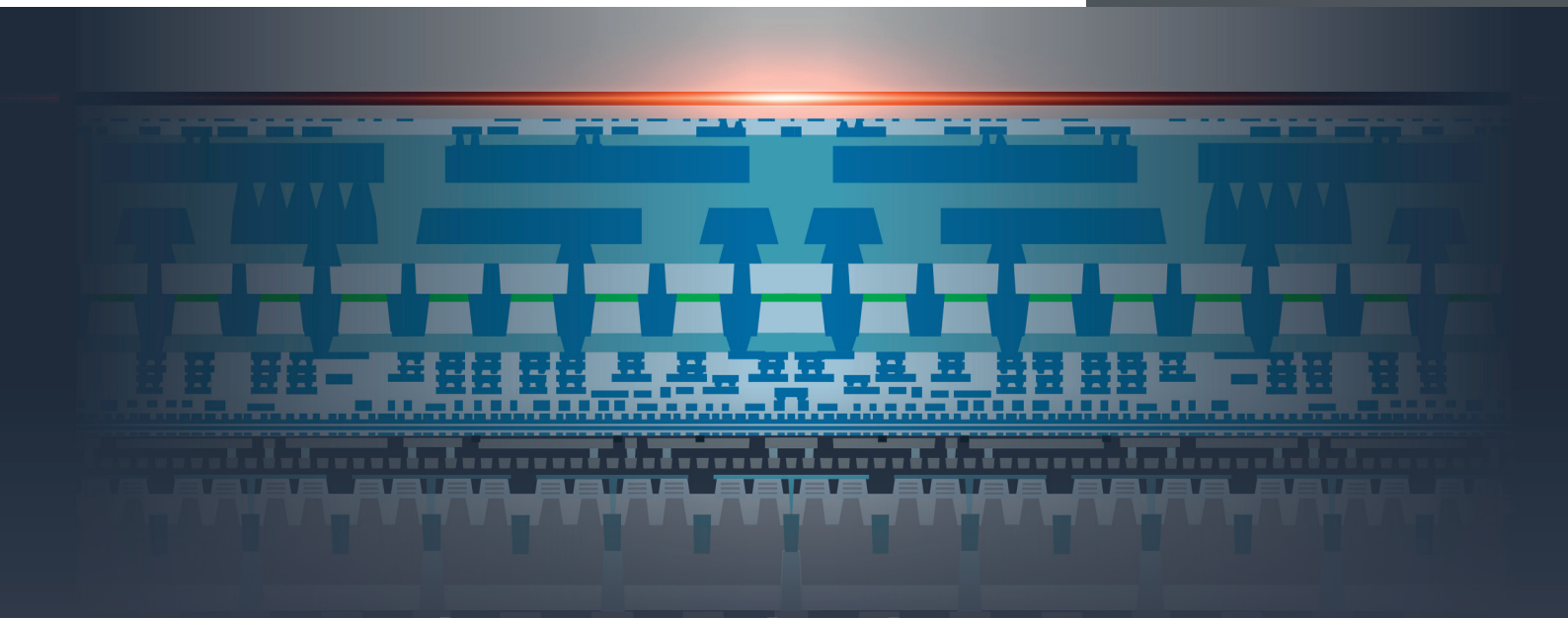

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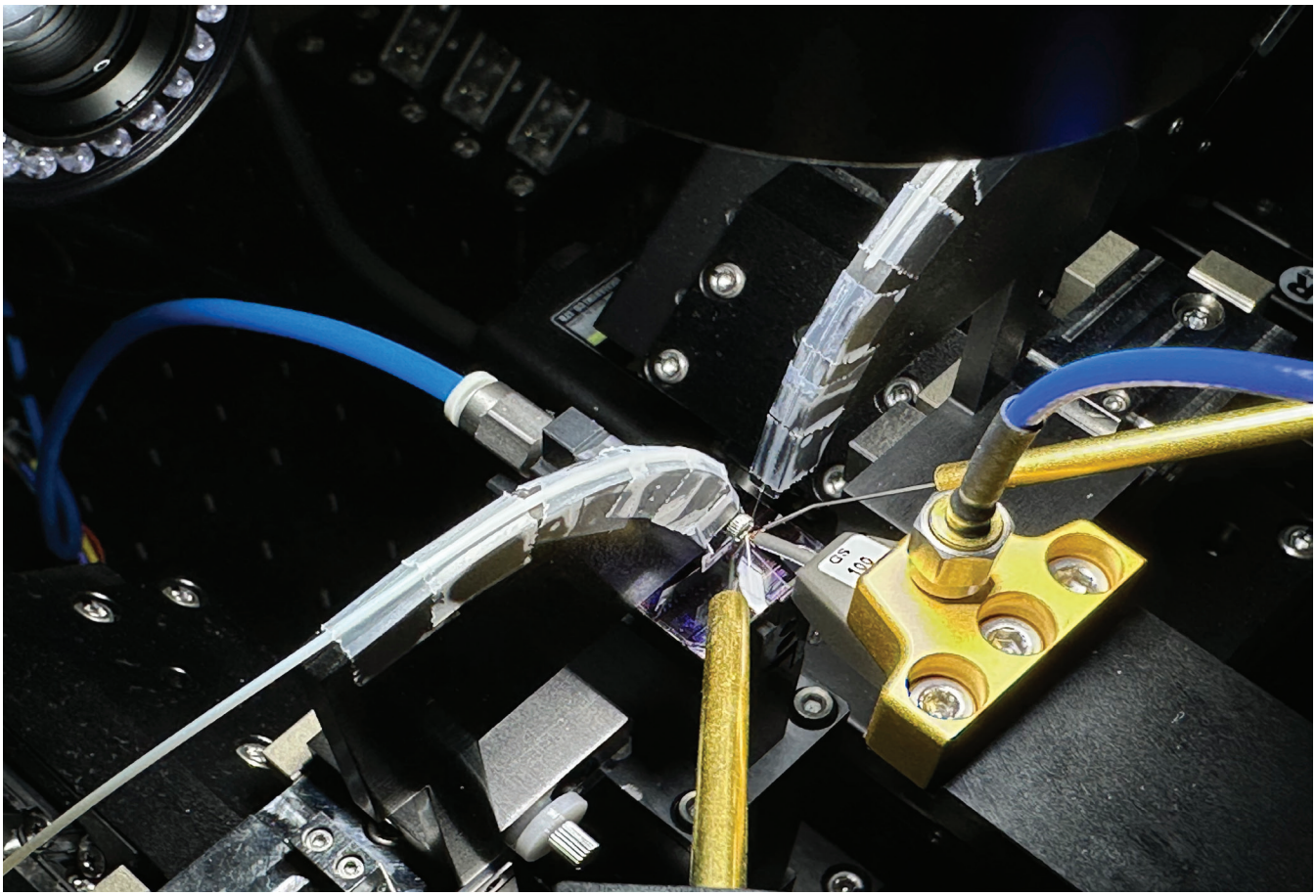


Trapped light boosts detection efficiency

InGaAs avalanche photodiodes equipped with photon-trapping structures realise record-breaking efficiency, aiding sensing in tomorrow's applications

BY RUI SHAO, JISHEN ZHANG AND XIAO GONG FROM THE NATIONAL UNIVERSITY OF SINGAPORE

There are a number of exciting applications involving the use of photonics in the short-wave infrared, which is a spectral domain spanning 900 nm to 2.5 μm. This region is employed for advanced driver assistance systems, biomedical imaging and high-speed optical interconnects.

Regarding the latter, demand is on the rise, spurred on by surging interest in artificial intelligence. In this revolutionary form of computing, there are compelling arguments for transmitting and receiving data via infra-red light through optical fibres, rather than routing electrical signal through copper wires.

However, to ensure that this shift in transceiver technology is successful, optical receivers must combine a high bandwidth with a superior signal-to-noise ratio and a high detection efficiency – and ideally, accomplish all of this using monolithic electronic-photonic integration.

Against this backdrop InGaAs-based avalanche photodiodes (APDs) are gaining a great deal of attention, thanks to their exceptional sensitivity, compact footprint, and broad absorption spectrum. With this class of detector, there has been significant progress in responsivity and bandwidth, for devices on both InP and silicon substrates.

For those that produce APDs, if there's a need to increase responsivity, the well-trodden path is a thickening of the InGaAs absorption layer. However, there's a penalty to pay for this – an increase in carrier transit time that applies the brakes to the detector's speed. And that's not the only downside, as a thicker absorber also exacerbates dark current, degrading the signal-to-noise ratio.

A variety of reflector-based techniques have been explored to address these challenges. But there's also a more efficient alternative, involving the

integration of a photon-trapping structure within the APD. With this approach, there's enhanced light absorption, realised without the need for complex reflector designs or additional epitaxial growth. Instead, engineers draw on the synergy between thinner active layers and photon-trapping microstructures to boost bandwidth and photon efficiency simultaneously.

Inspiration for photon trapping is found in nature. There are natural light-trapping mechanisms in biological structures, such as butterfly wings and moth eyes, that maximise absorption through micro- and nano-scale arrangements, effectively guiding incident light into the lateral plane rather than reflecting it away. Device designers adopting these strategies can realise highly efficient light absorption in a thin InGaAs layer, and significantly enhance detection efficiency without sacrificing bandwidth.

Despite the tremendous promise that photon-trapping has in helping to produce high-performance InGaAs APDs, research in this area is limited. But we are addressing this at the National University of Singapore by pioneering the development of InGaAs/InAlAs APDs that incorporate photon-trapping structures. We have successfully integrated these detectors onto a silicon-on-insulator substrate.

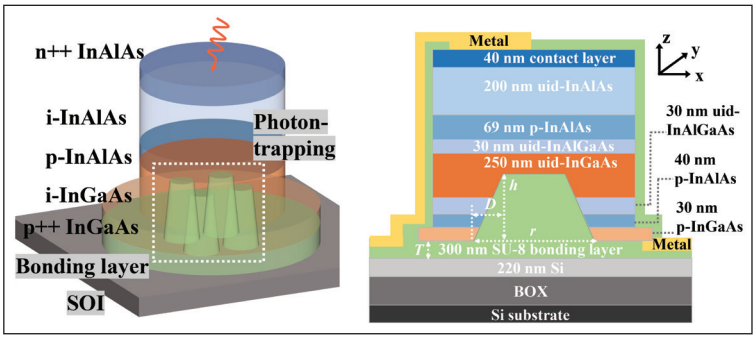
Strengths of our APDs include a responsivity of 0.75 A W^{-1} at unity gain, realised with an InGaAs absorption layer around just 250 nm-thick. Additionally, we have achieved a remarkable enhancement in external quantum efficiency compared with conventional InGaAs APDs, for a spectral range spanning 1550 nm to 1630 nm.

Comprehensive simulations guided our device design and fabrication process. Using this approach, we have produced APDs with a dark current of just 51.3 nA at 90 percent of the device's breakdown voltage, and a maximum multiplication gain exceeding 100. The high-performance of our devices is also highlighted by detectivities of 9.34×10^{10} Jones at 4 V and 3.43×10^{12} Jones at 24.1 V, along with a broad operational voltage range, spanning 4 V to 24.1 V.

Light-trapping mechanisms

For normal incident light, which primarily propagates vertically, absorption scales with InGaAs layer thickness. However, there's more to consider when evaluating our devices. Note that conventional vertical resonance modes yield narrow spectral responses and negligible lateral light confinement – and with our photon-trapping structure, incident photons are instead coupled into lateral propagation modes, trapping light within the plane via the surrounding InAlAs layer and the SU-8 cladding.

At the core of our innovative design are two-dimensional photonic crystals, formed from etching



➤ Figure 1. Three-dimensional illustration of the InGaAs APD with photon-trapping structures and the unit cell of the device with detailed layer structures.

nanostructures into the device surface. With these novel APDs, incoming light is diffracted and reflected at the two-dimensional photonic crystals, to create coupling into lateral propagation modes that confine photons within the InGaAs absorber (see Figure 1 for the unit cell structure and key design parameters of our device, which incorporates a separate-absorption-grading-charge-multiplication region that features a multiplication layer and an InGaAs absorption layer, approximately 200 nm and 250 nm thick, respectively).

To quantify the impact of our two-dimensional photonic crystals, we conducted electrical and optical simulations. They reveal that introducing these photonic structures generates localised electric field peaks at the edges, while simultaneously reducing the electric field in the upper multiplication and absorption regions. Based on these findings, we are aware that there is a need for careful design of geometrical parameters, to avoid premature breakdown and a field-related tunnelling current.

Additional optical simulations by our team explored the impact of variations in the period, radius, etch depth, and lateral etching distance of our two-dimensional photonic crystals, as well as the SU-8 bonding-layer thickness. This effort enabled us to carefully select the geometry for our APDs, by considering both the results of our simulations and practical constraints. The designs that followed provide diffraction-enabled light confinement, and lead to the formation of multiple resonance peaks within the InGaAs absorption layer, further amplifying absorption efficiency.

Guided by our simulations, we fabricated devices using an optimised process. We began by loading an InP substrate into an MBE chamber and depositing a stack of III-V epilayers. To form two-dimensional photonic crystals, we patterned our epiwafers using electron-beam lithography, prior to inductively coupled plasma reactive ion etching to create structures with a desired depth and slanted sidewalls. After that, we formed a tungsten electrode by sputtering and lithography.

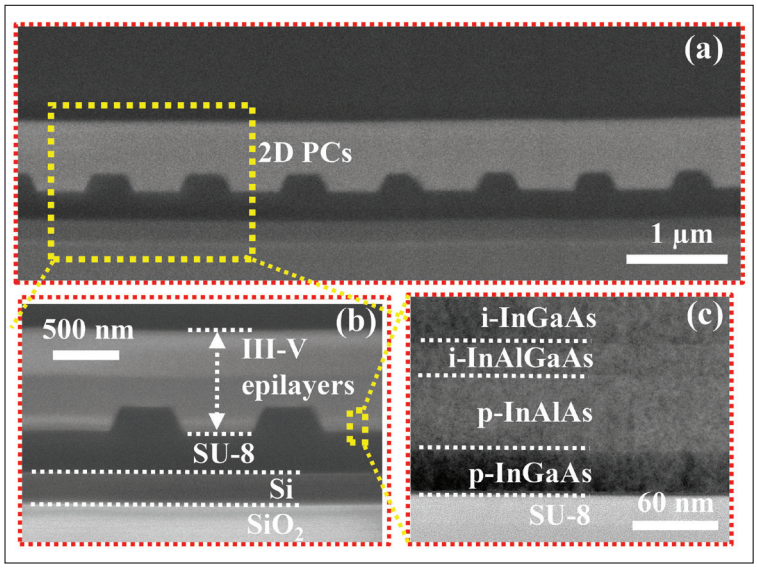


Figure 2. Cross-sectional scanning electron microscopy images of the photon-trapping APD on the silicon-on-insulator substrate. (a) Cross-sectional view of the active mesa region with the photonic crystal array. (b) The zoom-in view of the photonic crystal with III-V epilayers. (c) The zoom-in view of the interface at the SU-8 bonding layer and III-V epilayers.

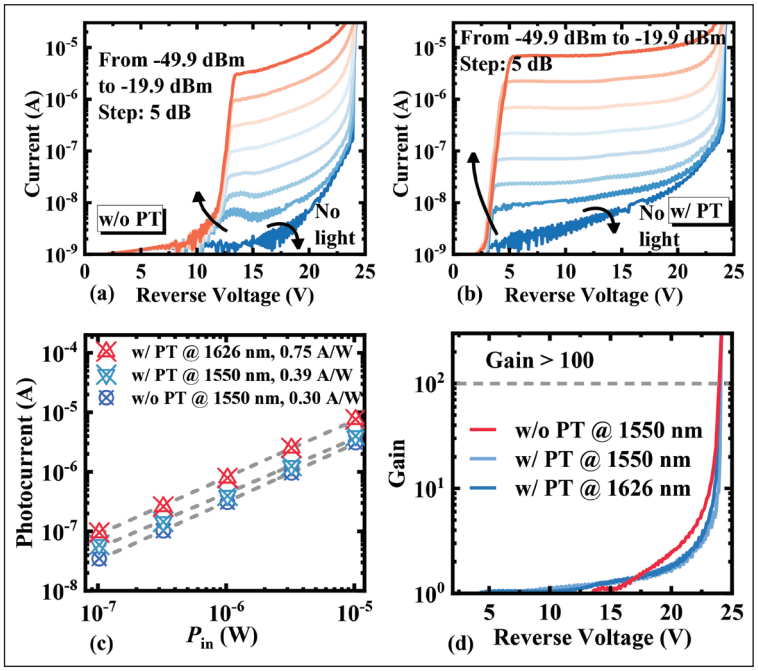


Figure 3. Current-voltage (I-V) characteristics of the APDs (a) without photon-trapping structures at 1550 nm, and (b), with photonic-trapping structures at 1626 nm, by varying the intensity of illuminated light. (c) The plot of photocurrent versus light intensity at unit gain. (d) Multiplication gain of the APDs with and without photon-trapping structures at different voltages.

The next steps began by spin-coating an SU-8 adhesion layer on the SOI substrate. We then bonded III-V die in a flip-chip manner, applying a pressure of 80 N cm^{-2} at 150°C for 30 minutes. To ensure light trapping in the InGaAs absorber, we carefully optimised the thickness of the SU-8 bonding layer to be consistent with optical simulations.

From an industrial perspective, there is a preference for oxygen plasma-assisted oxide bonding. By adopting this approach that's been extensively studied and widely adopted for III-V-to-silicon wafer-to-wafer bonding, we have been able to efficiently fill our etched two-dimensional photonic crystals on the InP substrate with an oxide cladding, prior to chemical mechanical polishing.

Heterogeneous integration followed, by bonding a III-V wafer to silicon wafer. Note that this procedure for filling two-dimensional photonic crystals is fully compatible with existing III-V-to-silicon wafer-to-wafer bonding technology.

Fabrication of our devices is completed by: removing the InP handle substrate with concentrated HCl, a step that involved partial etching of the InGaAs etch-stop layer to reduce undesired absorption during measurements; deposition of a contact metal; mesa etching, using $H_3PO_4/H_2O_2/H_2O$ solution to minimise surface defects; and passivating the device, using a SU-8 cladding layer.

We have inspected our APD with a scanning electron microscope, which is helpful when characterising the photonic crystal array (see Figure 2 (a)). This form of microscopy clearly reveals truncated-cone-shaped two-dimensional photonic crystals with smooth slanted sidewalls. Zooming in, smooth and flat interfaces are visible between the III-V active layers and the SU8 adhesion layer on the SOI substrate (see Figure 2 (b)). Clear layer structures for the III-V stack (see Figure 2 (c)) confirm that MBE growth realises well-controlled layer thickness and elemental compositions.

Device evaluation

Electro-optical characterisation began by plotting current-voltage curves for our control APD and the photon-trapping APD, with a mesa radius of 15 μm, both with and without light illumination (see Figure 3 (a) and (b)). For measurements under illumination, we employed a lensed fibre to direct light with an intensity ranging from -49.9 dBm to -19.9 dBm on the active region.

This investigation uncovered a significantly reduced punch-through voltage for the photon-trapping APD, attributed to local electric-field peaks at the edges of the two-dimensional photonic crystal in the InGaAs absorber. This partially high electric field drives photogenerated carriers in the InGaAs layer into the InAlAs multiplication layer.

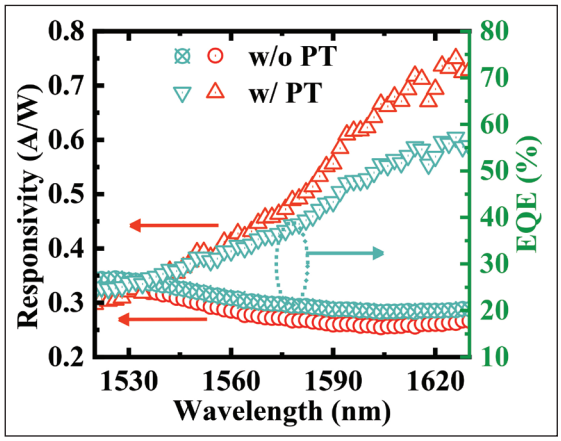
Measurements conducted at 90 percent of the breakdown voltage recorded dark currents for the control APD and the photon-trapping APD of 16.9 nA and 51.3 nA, respectively. While the dark current of the photon-trapping variant is higher, it is still acceptable, thanks to proper engineering of the two-dimensional photonic crystal shapes that ensures effective minimisation of the field-related tunnelling dark current. Also helping to improve performance are the slanted sidewalls that efficiently smooth the electric-field and prevent premature breakdown.

Via variations in input power, we have measured and extracted optical response current characteristics (see Figure 3 (c) for the extracted steady-state photoresponsivity of the control APD and the photon-trapping APD at a unit gain). Both devices realise a multiplication gain of more than 100 (see Figure 3 (d)). The photon-trapping APD realises responsivities of 0.75 A W^{-1} at 1626 nm and 0.39 A W^{-1} at 1550 nm, resulting in external quantum efficiencies of 57.2 percent and 31.2 percent, respectively. Compared with the control, the photon-trapping APD offers enhancements by factors of 2.38 and 1.3 at 1626 nm and 1550 nm, respectively.

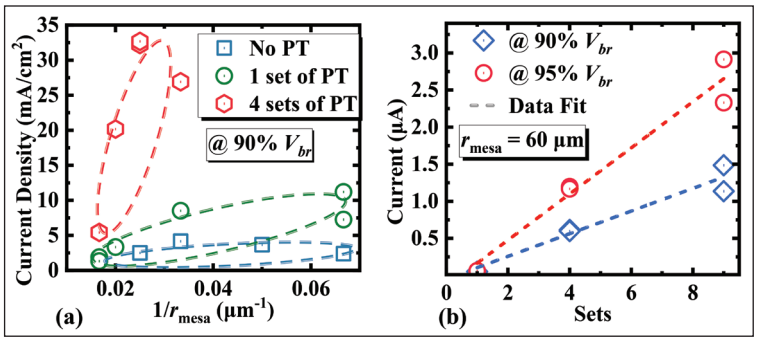
We have looked in more detail at the absorption spectra of both types of APD, considering unit gain. This involved extracting wavelength-dependent responsivity, by varying the light intensity and wavelength of a narrow-linewidth tuneable laser. For the photon-trapping APD, we recorded a broadband enhancement of light absorption from 1536 nm to 1630 nm, and a maximum peak of 0.75 A W^{-1} at 1626 nm (see Figure 4). These results showcase the effectiveness of the photon-trapping mechanism, which offers tunability of the absorption peak through changes in the periods and radii of the two-dimensional photonic crystals.

As well as enhancing optical performance, photon-trapping significantly impacts the electrical field inside the device. To understand the leakage mechanism in our photon-trapping APDs, we extracted dark current density, plotting values for different mesa radii under voltages equal to 90 percent and 95 percent of the breakdown voltage (see Figure 5 (a) and (b)). This investigation uncovered a strong dependence of the dark current on the two-dimensional photonic crystal's area, and indicated that the perimeter leakage current is the dominant leakage source at high reverse biases.

To understand the leakage generation mechanism, we recorded the temperature-dependence of the reverse dark current between 240 K to 320 K (see Figure 6 for Arrhenius plots of the dark current for both devices). This study found that at small reverse biases, the dark current of both forms of APD increases slightly with increases in temperature. We account for this by considering more severe thermal generation. At a bias of 10 V, both forms of APD have comparable activation energies, while a slightly smaller activation energy is obtained in the photon-trapping APD at a larger reverse bias of 20 V. These observations suggests that the tunnelling-related generation of the dark current is more prevalent in photon-trapping APDs at larger reverse biases.



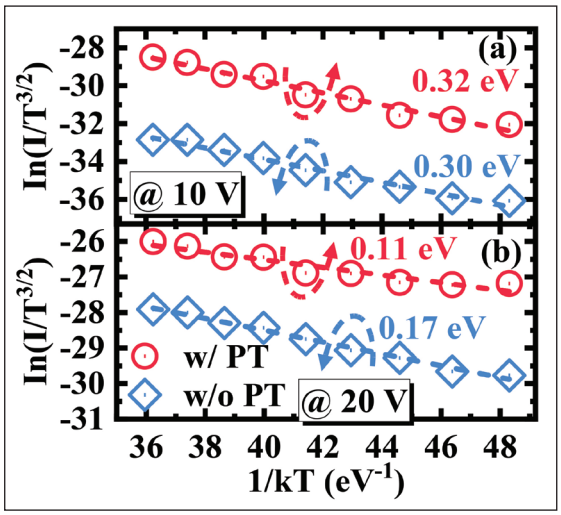
➤ Figure 4. Extracted responsivity and external quantum efficiency (EQE) versus wavelength.



➤ Figure 5. (a) Reverse dark current density versus the reciprocal of mesa radius at 90 percent breakdown voltage. (b) Dark current versus the number of photonic crystals at 90 percent and 95 percent breakdown voltage.

One of the downsides of dry etching the III-V epilayers in the active region is that it creates a long-term degradation issue. There's an increase in dark current, predominantly generated in the upper side of the absorbing layer that's close to the InAlAs multiplication layer. Another impediment to a low

Strengths of our success include: a 2.38 times enhancement in external quantum efficiency; the heterogenous integration of high-performance InGaAs/InAlAs APDs on the silicon photonics platform, using a large-scale manufacturable integration approach; and a comprehensive analysis and characterisation in the optical and electrical domains, providing an in-depth understanding of photon-trapping structures.



➤ Figure 6. Arrhenius plot of the control and photonic-trapping APD at (a) 10 V, and (b) 20 V, with extracted activation energies.

dark current, as well as the reliability of the photon-trapping APD, is ion implantation into the charging layer. For our devices, the etch depth for the photon-trapping APDs is only around 220 nm, so 130 nm away from the top surface of the InGaAs absorber. By tuning the period and radius of the photonic crystal, we will be able to further reduce the etch depth and enhance long-term reliability.

Additional weaknesses associated with dry etching III-Vs include surface roughness and damage, which leads to surface traps and defects at the sidewalls. We have adopted a few approaches to reduce surface damage. Our efforts include using low-ion-energy dry etching, followed by a few seconds of wet etching, to reduce surface damage caused by ion bombardment. Filling the III-V voids with SU-8 helps to passivate dangling bonds.

We have benchmarked our photon-trapping APDs against surface-illuminated germanium-on-silicon APDs, InGaAs-based APDs on various substrates, and AlInAsSb APDs with photon-trapping structures (see Table 1). This comparison, using key figures-of-merit, demonstrates that our devices exhibit outstanding performance in terms of responsivity, multiplication gain, and dark current, even with thin InGaAs/InAlAs layers on the SOI substrate. This underscores the great potential for improving optical performance with photon-trapping structures, and especially heterogeneous integration with silicon photonics.

Our work is a significant milestone in developing III-V APDs for future optoelectronic integrated circuits. Strengths of our success include: a 2.38 times enhancement in external quantum efficiency; the heterogenous integration of high-performance InGaAs/InAlAs APDs on the silicon photonics platform, using a large-scale manufacturable integration approach; and a comprehensive analysis and characterisation in the optical and electrical domains, providing an in-depth understanding of photon-trapping structures. This work lays the foundation for photon-trapping APDs to serve in driver assistance systems, biomedical applications and next-generation computing.

	Our work	[9]	[6]	[10]	[11]	[4]	[5]	[7]
Material	InGaAs /InAlAs	Ge/Si	Ge/Si	Ge/Si	GeSn /Ge/Si	InGaAs /InAlAs	InGaAs /InAlAs	AlInAsSb
Substrate	SOI	SOI	Si	SOI	Si	InP	Si	GaSb
Structure	PTAPD 250 nm absorber	APD 1.03 µm absorber	PTAPD 700 nm absorber	APD	MQW APD	APD 2.2 µm absorber	APD 1.1 µm absorber	PTAPD 200 nm absorber
Res.	0.75 A/W @ 1626 nm	0.3 A/W @ 1550 nm	0.32 A/W @ 1550 nm	0.55 A/W @ 1310 nm	0.33 A/W @ 2003 nm	1.05 A/W @ 1550 nm	0.54 A/W @ 1550 nm	0.35 A/W @ 2000 nm
EQE	57.2%	24.0%	25.6%	52.1%	20.4%	84%	43.2%	21.7%
Gain	>100	40	21	10	15	> 100	21	>100
Operation Window	4 - 24.1 V	11 - 29 V	2 - 16 V	2.5 - 18 V	0.3 - 10 V	47 - 64 V	15 - 22 V	15 - 20 V
Detectivity (Jones)	9.34×10^{10}, 3.43×10^{12}	$^{*}5.26\times10^{9}$	$^{*}5.85\times10^{8}$	$^{*}6.02\times10^{9}$	$^{*}5.20\times10^{8}$	6.78×10^{12}	$^{*}7.74\times10^{9}$	$^{*}2.32\times10^{11}$
I_{dark}	51.3 nA @ 90% V_{br}	~2 µA @ 95% V_{br}	1 mA @ 97% V_{br}	900 nA @ 90% V_{br}	124 µA @ 90% V_{br}	7.8 nA @ 95% V_{br}	261 nA @ 95% V_{br}	230 nA @ 95% V_{br}

➤ Table 1. Benchmark of the APDs for SWIR detection, including InGaAs, InP, germanium, and GaSb material systems.

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ANGEL EVENTS

Aluminium treatment boosts the efficiency of green miniLEDs

Record-breaking efficiencies result a flow of trimethylaluminium after quantum-well growth

RESEARCHERS from China have increased the optical efficiency of green LEDs by employing aluminium treatment during the growth of quantum wells.

The devices produced by the collaboration – a partnership between Yancheng Teachers University, the Institute of Semiconductors, Xiamen University, and Yangzhou Zhongke Semiconductor Lighting – have a peak external quantum efficiency (EQE) of 65 percent and a wall-plug efficiency of 60 percent.

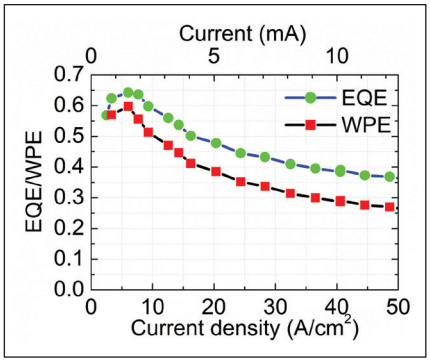
According to team spokesman Hongjian Li from Xiamen University, these efficiencies enable the team's miniLEDs to be attractive candidates for deployment in displays.

Green LEDs are not as efficient as their blue cousins, due to: piezoelectric fields, which pull apart electrons and holes and hamper light emission; and the need for a higher indium content in the wells, which leads to a higher density of light-quenching defects.

Due to these drawbacks, visible LEDs suffer from a 'green gap'. It is a significant issue that the global research community has tried to address with a number of novel approaches, including the use of non-polar and semi-polar structures, nanowires, quantum dots, staggered and graded quantum wells, and shallow quantum-well designs.

Significant successes to date by other Chinese collaborations are a peak EQE of 53.3 percent at 527 nm, as well as a peak EQE of 55.6 percent at 525 nm for a GaN-on-silicon LED.

Li and co-workers have exceeded these EQE values with a device that's grown on a patterned sapphire substrate and features aluminium-treatment, applied between the growth of the InGaN quantum wells and GaN barriers.



➤ Droop, attributed to Auger recombination, leads to a decline in the efficiency of green LEDs produced with an aluminium treatment.

After loading the sapphire substrate into the MOCVD reactor, the team deposited a 30 nm-thick nucleation layer at a low temperature, followed by a stack of epilayers.

After growing each InGaN quantum well at 760°C, the team introduced trimethylaluminium into the chamber for 10s with a flow rate of 8 μmol min^{-1} while maintaining ammonia flow and stopping the flow of indium and gallium sources. Growth of GaN barriers followed, after the temperature had been ramped to 940°C.

Processing epiwafers into flip-chip miniLEDs with a mesa area of 0.025 mm^2 involved: inductively coupled plasma etching to expose the *n*-type contact layer; electron-beam deposition and patterning of ITO and Cr/Al/Cr/Pt/Au layers on the *p*-GaN and *n*-GaN surfaces, respectively; addition of a distributed Bragg reflector, formed from alternating layers of Ta_2O_5 and SiO_2; and the formation of Cr/Al/Ni/Al/Ti/Pt/Au contact pads.

X-ray spectroscopy of the epistructure revealed an AlGaN layer around just 0.5 nm-thick on top of the InGaN quantum wells. According to this metrology technique, the gallium mole fraction in this AlGaN layer is a very high, with an aluminium content around just 10 percent, due to atom over-reactions in the MOCVD chamber.

The team also studied its material with high-resolution transmission electron microscopy, finding just three 'V' pits in a 3 μm-width area. This observation is claimed to indicate a very low defect density in the active region.

Evidence of superior radiative recombination arising from the aluminium-treatment comes from time-resolved photoluminescence. Exciton lifetime in the LED structure without this treatment is 75 ns, compared with 17 ns for the improved active region. Meanwhile, atomic force microscopy on the surface of the quantum wells has determined that aluminium treatment decreases the size of the pits and reduces surface roughness from 4.8 nm to 1.7 nm, enabling step-flow growth.

Another benefit of the aluminium treatment is that it reduces the blue shift in peak wavelength with current density.

For the device with aluminium treatment, the peak EQE and wall-plug efficiency occur at a current density of around 5 A cm^{-2}, and fall to 47.8 percent and 38.5 percent, respectively, when driven at 20 A cm^{-2}.

"We believe that Auger recombination is the main cause for the efficiency droop in InGaN green LEDs," says Li, who explains that the collaboration's next goal is to produce devices operating at longer wavelengths, such as those emitting in the red.

REFERENCE
➤ Y. Zhao *et al.* Appl. Phys. Express **18** 082001 (2025)

Two-step anneal aids SiC interfaces

Annealing twice under a mix of hydrogen and argon produces reliable SiC MOSFETs with high mobilities

ENGINEERS from the University of Osaka are claiming to have improved the performance and reliability of the SiC-SiO_2 interface with a two-step annealing process.

Their approach, involving annealing steps in a mixture of argon and hydrogen gas that deliver a hike in channel mobility and improve reliability against bias stress, promises to improve the performance of SiC MOSFETs.

Despite soaring sales, this class of transistor suffers from a high density of interface states that capture free electrons in the channel, leading to an increase in on-resistance, especially for devices with blocking voltages between 600 V and 1200 V.

For many decades, developers and producers of SiC MOSFETs have devoted much effort to trying to improve the quality of the SiC-SiO_2 interface, with gains resulting from the incorporation of impurity atoms, such as nitrogen, phosphorous, boron and sodium.

Since the late 1990s, the standard approach for improving the SiC-SiO_2 interface is a post-oxidation anneal in nitric oxide. This anneal reduces the density of interface states and increases field-effect mobility, but there is a degradation in reliability – seen, for example, in an instability in the threshold voltage – probably associated with the introduction of nitrogen atoms beside the interface. One significant issue that arises is a degradation in reliability against a negative gate-voltage stress that limits the gate voltage that can be applied to the SiC MOSFET.

Recently, developers of SiC MOSFETs have found that it's possible to improve the performance and reliability of their devices by minimising the oxidation of SiC during the formation of the gate oxide. This approach supresses carbon-related defects, but as the process relies on interface nitridation, reliability remains a concern.

The novel approach by the researchers from the University of Osaka breaks new ground by improving the reliability and performance of SiC metal-oxide-semiconductor (MOS) devices without resorting to interface nitridation.

Drawing on an approach widely used in silicon MOS technology, their groundbreaking process is based on dilute hydrogen annealing, and involves annealing before and after gate oxide deposition. The purpose of this two-step anneal is to reduce defects near the surface of SiC, and at the SiC-SiO_2 interface. Oxidation of SiC is minimised as much as possible.

The success of this approach has been demonstrated through the fabrication of SiC MOS capacitors and MOSFETs. To produce these devices, the team began by growing an *n*-type epilayer with a donor density of about 5 x 10^{15} cm^{-3} to 2 x 10^{16} cm^{-3} for the MOS capacitors, and an *n*-type epilayer with an acceptor density of about 5 x 10^{15} cm^{-3} for the MOSFETs.

Source/drain and body contact regions for the MOSFET were defined by ion implantation through a SiO_2 capping layer, subsequently removed and replaced with a carbon cap. Argon annealing activated the dopants, prior to removal of the cap by low-temperature oxidation, wet-cleaning of the sample surface and the addition of the gate oxide.

Formation of the gate oxide began by annealing at 1300°C under a mixture of hydrogen and argon gases, a step designed to remove defects near the SiC surface.

Cleaning of the sample surface in a HF acid solution followed, before plasma-enhanced CVD added a SiO_2 film. After that the team annealed this structure under CO_2 at 1300°C for 30 minutes, before annealing for another 30 minutes at 1200°C under a mixture of hydrogen and argon gases.

To evaluate this process, the engineers also produced a portfolio of control samples. One did not have the first annealing step, another had the second anneal in just argon, and samples were also formed by dry oxidation, and oxidation followed by a NO anneal under optimal conditions.

For both capacitors and MOSFETs, oxide thicknesses were 40-50 nm, and electrodes were made of aluminium.

Electrical measurements on the capacitors determined that the team's two-step process is as effective as NO annealing at reducing the density of interface states.

Note that samples with just a first anneal, or annealing just under argon, have a markedly higher density of interface states.

Secondary ion mass spectrometry revealed that NO annealing led to a concentration of more than 10^{21} cm^{-3} at the interface of this MOS capacitor, compared with around 10^{19} cm^{-3} when using the two-step anneal.

Peak field-effect mobility for the SiC MOSFET produced with the team's optimised process is 17.2 cm^{-2} V^{-1} s^{-1}, compared with just 2-3 cm^{-2} V^{-1} s^{-1} for the variant produced by dry oxidation. The engineers attribute this improvement to an increase in free electrons, thanks to a reduction in the density of interface states.

Measurements of the flatband voltage drift are supressed by the two-step anneal in the mixture of hydrogen and argon gas. According to the team, this provides evidence of improved reliability.

REFERENCE

➤ T. Kobayashi *et al*. Appl. Phys. Express **18** 081002 (2025)

GaN: Reducing the on-resistance of GaN *p-n* diodes

Vertical GaN power devices could benefit from better *p*-type contacts, realised by magnesium implantation and ultra-high-pressure annealing

ENGINEERS from North Carolina State University, Adroit Materials and Poland's Institute of High-Pressure Physics have reduced the specific on-resistance of vertical *p-n* GaN diodes formed by magnesium implantation by nine orders of magnitude.

Spokesman for the team, Spyridon Pavlidis, says that this improvement, realised by incorporating magnesium deposition and annealing into the contact stack, has allowed their devices to have a performance on par with those of epitaxial GaN diodes.

The collaboration's diodes combine excellent rectification ratios with very high current densities and a record-low differential specific on-resistance.

This breakthrough will aid the development of vertical GaN devices that require contacts to magnesium-implanted *p*-type GaN.

"Ion implantation is a critical part of the semiconductor device processing 'tool box', since it enables selective area doping," says Pavlidis. "This is necessary for manufacturing high-performance transistors and diodes, such as MOSFETs, junction barrier Schottky diodes, and beyond. By controlling where dopants are introduced in the device, we can dictate where current flows and manage electric fields."

The team's work helps to address many of the obstacles associated with the realisation of GaN devices that employ magnesium implantation for *p*-type doping. These challenges include realising: sufficient doping activation and defect mitigation via post-implantation annealing; control of the final dopant profile, due to unwanted diffusion during annealing; prevention of GaN surface decomposition and preservation of electrical properties after annealing; and the formation of high-quality contacts on the implanted structure.

Higher activation energies are produced with ultra-high-pressure annealing, which can also prevent surface decomposition but fails to provide a low-resistance *p*-type contact.

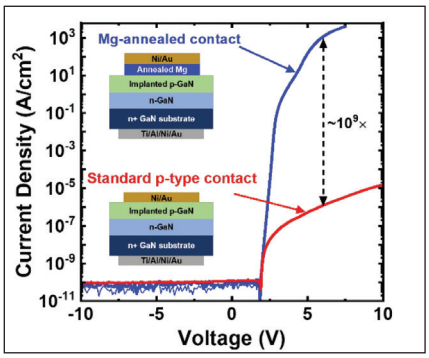
To address this issue, Pavlidis and co-workers have investigated the impact of physical vapour deposition and annealing of pure magnesium on implanted *p*-type GaN.

It's an approach that's previously been shown to form a low-resistance contact to low-doped *p*-type GaN, with success attributed to a number of mechanisms. They include: the mutual diffusion of magnesium and gallium, to help create a very heavily doped *p*-type layer; a reduced barrier height at the metal-semiconductor interface; and the formation of magnesium-intercalated nitride superlattices, introducing ionised acceptors via polarisation.

For the team's investigation, they produced two vertical diodes – a control, and a magnesium-annealed variant. Device fabrication began by loading *n*-type GaN substrates into an MOCVD chamber and depositing a 5 µm-thick GaN drift layer with a silicon dopant concentration of around 4 x 10^{16} cm^{-3}. Magnesium implantation followed, using ion energies of 25 keV and 75 keV and doses of 4.4 x 10^{13} cm^{-3} and 2 x 10^{14} cm^{-3}, with a tilt angle of 7° to form an initial box of around 100 nm. Samples were than annealed at 1300 °C for 100 minutes undrer 400 MPa in nitrogen gas.

Electron-beam evaporation of nickel and gold added an anode contact to the control, while the magnesium-annealed samples were formed through thermal evaporation of around 60 nm of pure magnesium onto the magnesium-implanted layer using photolithography. Both contacts were subsequently annealed.

Plots of current-voltage characteristics revealed that the control exhibits



➤ Magnesium-annealing (right) improves the performance of *p-n* diodes, which benefit from the removal of a *p*-type Schottky contact in series with the *p-n* junction.

expected traits, with an exponential increase in current at an anode bias below 2 V, and a reverse-biased *p*-type Schottky current-limited regime at higher bias. In sharp contrast, diodes with a magnesium-annealed contact exhibit a repeatable 10^9 improvement in on-current and on-resistance at forward voltages beyond 5 V.

The team attributes these improvements to increased hole conduction through the magnesium-annealed *p*-type contact. Under a forward bias, the extracted on-resistance is 0.65 mΩ at an on-current density of around 1 kA cm^{-2}. This is claimed to be the lowest on-resistance for magnesium-implanted *p-n* diodes, and comparable to vertical GaN-on-GaN epitaxial *p-n* diodes. The rectification ratio is more than 10^{12}.

Capacitance-voltage measurements identified a *p*-type Schottky contact in series with the *p-n* junction in the control device. With the magnesium-annealed contact this unwanted feature disappears, allowing carriers to be injected into the *p-n* junction via the anode contact.

Pavlidis and co-workers are now working on improving the contact process and reducing the turn-on voltge for the diodes. "Beyond *p-n* diodes, we are now applying the combination of implantation and contact technology to more advanced vertical GaN devices."

REFERENCE
➤ M. A. Hasan *et al.* Appl. Phys. Express **18** 091002 (2025)

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