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# FUNCTIONAL OXIDES FOR 300 MM SILICON

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# VIEWPOINT

BY RICHARD STEVENSON, EDITOR



## Picking the best platform

WHAT'S THE BEST foundation for the production of nitride epistructures? Well, there's no easy answer, as the best solution depends on the device in question.

For arguably the most important optoelectronic device, the LED, one of the leading platforms is sapphire. Although this foundation fails to ensure perfect lattice matching, it's affordable, scalable, and its surface may be textured to boost light extraction.

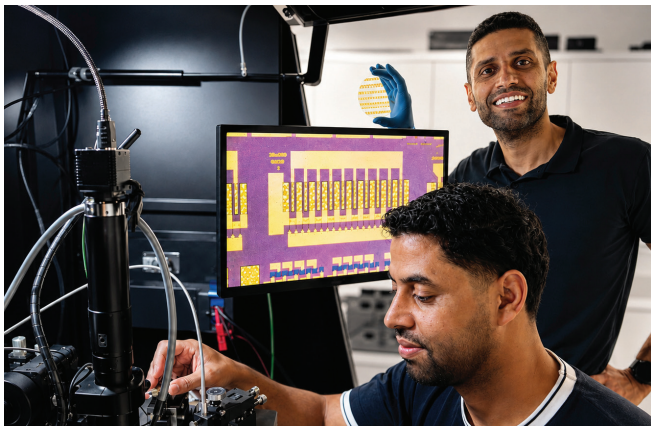
Offering an alternative for the high-volume manufacture of LEDs is silicon. This substrate enables device production in depreciated silicon fabs, as well as ease of integration with a silicon backplane, which drives the devices – an elegant solution for small displays based on microLEDs.

Silicon is also a contender for RF devices, where it competes alongside SiC. The latter offers a superior thermal conductivity, and is employed in applications where reliability is a high priority.

The other significant market for III-N devices is power electronics. Here, silicon substrates are widespread, and they are adopted for similar reasons to those for making LEDs on this platform. But there is a case for using sapphire, a platform many dismiss, due to its poor thermal conductivity. Pioneers of this approach include Transphorm, which released a 1200 V HEMT in 2023; and Power Integrations, releasing a 2.2 kV variant earlier this year.

Also advancing this technology is Farid Medjdoub's team at the Institute of Electronics, Microelectronics and Nanotechnology, in partnership with Prima Innotech (see p. 24). Their view is that while the relatively poor thermal conductivity of sapphire is a drawback, it's not a show stopper, and designers must also consider a number of other factors, such as blocking voltage, leakage, on-resistance, dynamic behaviour and manufacturability.

Options for realising higher blocking voltages include extending the source-to-drain distance, thickening the buffer layers, and introducing field plates. But the French team decided to avoid them all, and see what's possible when avoiding all electrostatic hardware.



Impressive results are realised with HEMTs having a carbon-doped buffer just 0.5 µm-thick. Successes include a blocking voltage of 5.5 kV, for devices with a source-to-drain distance of 40 µm; and, based on benchmarking, a competitive combination of specific on-resistance and breakdown voltage, according to comparisons with GaN power devices grown on silicon and SiC.

Arguably more impressive is a high-current device that avoids severe current collapse. Featuring 20 gate fingers and a total gate periphery of 10 mm, it delivers almost 3A under pulsed operation.

Medjdoub and co-workers have considered the benefits that might come from separating the sapphire substrate from its device, which is transferred to a more thermally conductive host; as well as direct growth of their optimised stack onto an engineered substrate.

A key point to take from the team's work is that one does not have to seek a material that excels on many fronts. More success might come from heterogeneous integration, which allows different materials to tick different boxes.

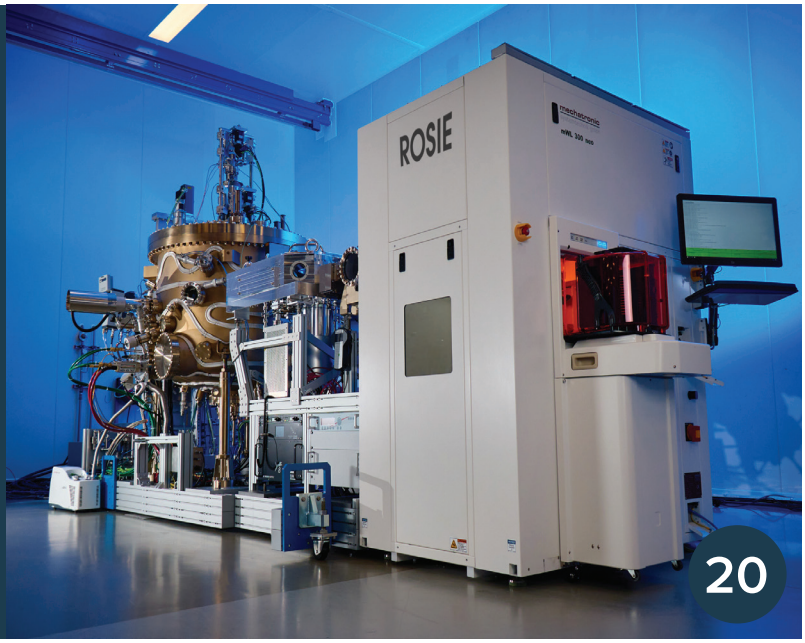
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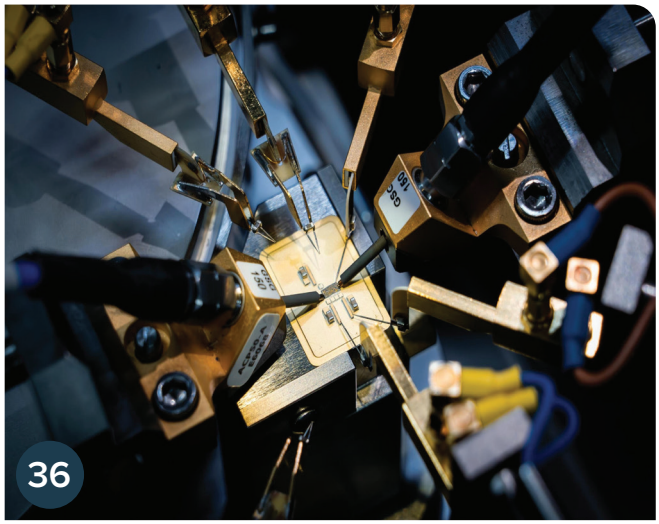
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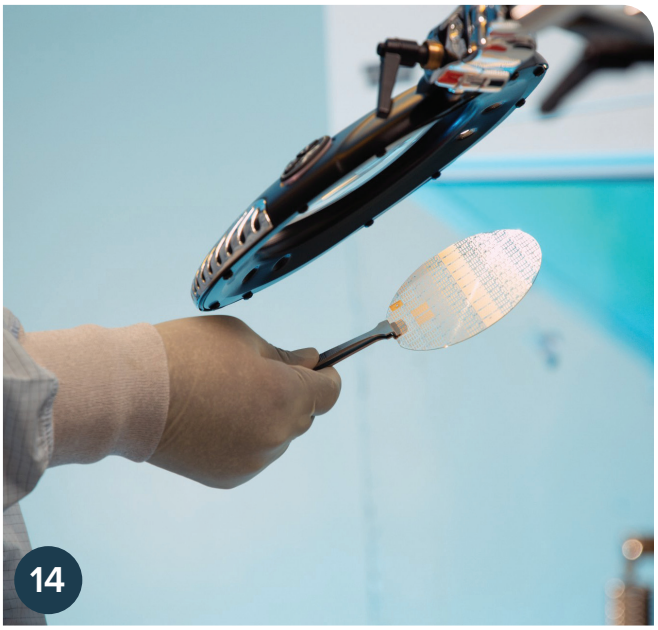
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# Major suppliers bet on VCSEL near-packaged optics

## VCSEL demand to reach 650 million units by 2031, says TrendForce

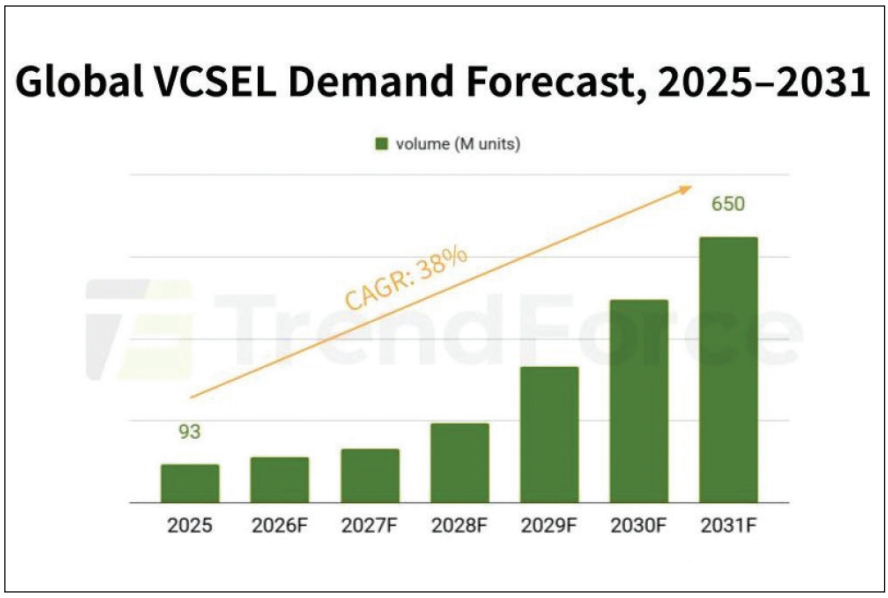
TRENDFORCE'S latest report *2027 Infrared Sensing and Optical Communication Market Trend*, shows growing interest in VCSEL-based near-packaged optics (NPO) for data transmission in data centre networks.

Major companies like Lumentum, Furukawa Electric, Coherent, Broadcom, Ams Osram, and HiSilicon are investing heavily in R&D, because of the technology's benefits of low power usage, easier maintenance, and a mature supply chain.

Several VCSEL NPO solutions are expected to launch between 2027 and 2028. Coupled with rising demand for short-reach optical transceivers, this trend is projected to boost VCSEL sales to 650 million units by 2031, growing at a CAGR of 38 percent from 2025 to 2031.

In scale-up network architectures for AI data centres, active electrical cables primarily rely on multiple re-timers to mitigate data loss and signal attenuation. However, as transmission speeds advance into the 1.6 Tb $s^{-1}$ era, high-frequency electrical signal attenuation over copper cables increases significantly. This is expected to accelerate the transition toward optical interconnect technologies for short-reach transmission, including architectures such as VCSEL NPO and microLED co-packaged optics (CPO).

Looking at supplier strategies, Lumentum, Furukawa Electric, Coherent, Broadcom, Ams Osram, and HiSilicon are developing VCSEL NPO solutions to capture future opportunities in scale-up networks. Coherent, Broadcom, Ams Osram, and HiSilicon are adopting mature 850 nm VCSELs paired with photodiodes to achieve aggregate bandwidth of up to 3.2 Tb $s^{-1}$, though chromatic dispersion will limit further improvements in transmission distance and bandwidth.




Lumentum and Furukawa Electric have adopted higher-cost 1,060 nm VCSEL solutions, while Coherent is also planning to adopt this approach. They offer extremely high fibre-coupling efficiency, low dispersion, low relative intensity noise, and strong performance at elevated operating temperatures, making them better suited to future increases in transmission speeds.

TrendForce notes that microLED CPO and VCSEL NPO require arrays of emitters and receivers to be integrated with ASICs/GPUs to achieve ultra-low power consumption and extremely high transmission density. Although microLED CPO offers long-term potential to approach the theoretical limit of energy consumption per bit, the technology continues to face challenges involving mass transfer, optical fibre compatibility, and coupling efficiency. Its supply chain also remains under development.

Compared with microLED CPO, VCSEL NPO offers more mature commercial conditions in terms of power consumption per bit, maintenance flexibility, and supply-chain readiness. Both 850 nm and 1,060 nm solutions can address the high-density transmission requirements of AI data centres. By offering a balance between performance and practical feasibility, VCSEL NPO has emerged as a highly competitive option for scale-up optical interconnect architectures at this stage.

Future VCSEL NPO development will focus on further improving overall performance. On the optical side, suppliers will seek to optimise the combination of VCSEL wavelengths and optical fibre technologies. At the chip level, development will focus on increasing the data rate of individual VCSELs from 100G to the 200G standard, as well as developing smaller VCSELs, known as micro VCSELs with individual device sizes of 100-200 µm. Higher-density, multi-channel arrays can then be used to further increase transmission bandwidth.

Overall, says TrendForce, continued improvements in performance, technology maturity, and supply-chain readiness are strengthening the competitive advantages of VCSEL NPO and accelerating the development of barriers to entry around the technology.

# Atomera and IQE to jointly develop RF GaN-on-silicon

Companies will co-optimise MST-enabled GaN-on-silicon wafers, which IQE will manufacture

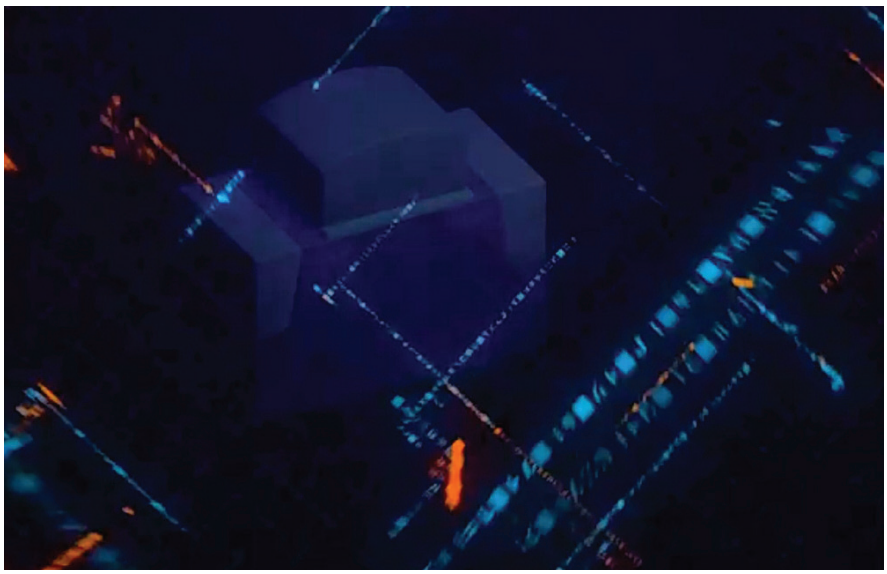
ATOMERA, a semiconductor transistor materials and technology licensing company, has entered into a Joint Development Agreement (JDA) with compound semiconductor wafer specialist IQE, to bring high-performance, cost-effective RF GaN to market.

The collaboration builds on Atomera's recently announced application of Mears Silicon Technology (MST) to silicon substrates for RF GaN and IQE's compound semiconductor epitaxy expertise. Under the agreement, the companies will collaborate to demonstrate GaN epitaxy on Atomera's MST-enabled silicon wafers.

With an initial focus on RF GaN-on-silicon applications, the work aims to demonstrate best-in-class linearity and loss for high-volume RF markets.

"IQE has built its business on delivering compound semiconductor epitaxy that meets the industry's highest performance bar, and this collaboration with Atomera is a natural extension of that work," said Rodney Pelzel, chief strategy and technology officer at IQE. "We are pleased to partner with Atomera on MST for GaN-on-silicon. The technology has the potential to provide a cost-effective substrate that is able to achieve the performance required by the market."

Atomera and IQE anticipate a multi-cycle development process, with engineering teams from both companies working together to optimise the multi-layer structure to identify the highest-performing RF material. The JDA also leaves room for the companies to expand their work, both to further refine RF GaN and to pursue other GaN use cases, including power electronics.



The project will centre on the production and testing of MST-enabled GaN-on-silicon wafers, with the goal of rapidly developing the best achievable MST-enabled GaN-on-silicon material and making samples available for foundry, IDM and fabless customer engagement.

"GaN has become critical to RF and power applications, but bringing high-performance GaN to volume production at a cost that works for mainstream markets remains a real challenge. This collaboration with IQE lets us apply MST's performance advantages to that space with a partner who brings deep compound semiconductor expertise. IQE is more than a development partner for MST. They are a catalyst to accelerate MST GaN-on-silicon time to market and could become an influential manufacturer of MST-enabled wafers," said Scott Bibaud, president and CEO of Atomera.

> MST is a quantum-engineered epitaxial silicon material that enhances transistors to deliver significantly better performance in semiconductor devices while shrinking die sizes and reducing cost

MST is a quantum-engineered epitaxial silicon material that enhances transistors to deliver significantly better performance in semiconductor devices while shrinking die sizes and reducing cost. When applied to GaN epitaxy, it enables improved RF GaN performance on silicon substrates.

Atomera's patented material technology is designed to enable more efficient, better-controlled current flow, supporting improvements in device performance and power efficiency across a wide range of applications.

# $73 million CHIPS funding for Vertical Semiconductor

MIT spin-out wins funding to accelerate R&D for next-generation GaN tech for US AI data centres

VERTICAL SEMICONDUCTOR has announced it has signed a letter of intent with the US Department of Commerce's CHIPS Research and Development Office (CRDO) to receive up to $73 million in federal incentives under the CHIPS and Science Act.

The proposed incentives are expected to accelerate research and development of next-generation vertical GaN power transistors, and unlock domestic production of this technology for artificial intelligence (AI) and high-performance computing applications.

Spun out of MIT, Vertical Semiconductor is developing vertical GaN FinFET technology that drives efficiency and power density in power systems for AI data centres and critical energy infrastructure. The company is scaling up a technology originally invented with the support of the US Department of Energy's Advanced Research Projects Agency – Energy (ARPA-E).



"Power is the most significant bottleneck in the build-out of AI infrastructure," said Cynthia Liao, CEO and co-founder of Vertical Semiconductor. "The CHIPS R&D award will accelerate Vertical Semiconductor's R&D and commercialisation initiatives for vertical GaN, which will expand American compute capacity within existing power constraints."

Led by Vertical Semiconductor in collaboration with commercial partners, this vertical GaN R&D and commercialisation initiative aims to culminate in a first-of-its-kind 2.5 MW AI rack designed to reduce energy losses by 30 percent, shrink physical footprint by 50 percent, and convert previously wasted electricity into deployable compute capacity.

The project would deploy these transistors across the full AI data centre power chain, driving compounding performance benefits from the grid to the compute.

# Intel unveils photonics roadmap

INTEL laid out its silicon photonics technology blueprint at the OCP 2026 conference, positioning the technology as the core architecture for next-generation high-performance computing and AI data centres.

Nic Dubé, Intel's VP of data centre systems and solutions, described silicon photonics as a "golden hammer" and claimed Intel is the only foundry in the industry capable of volume production on 300 mm InP wafers.

Intel said its integrated laser design uses a highly reliable light source requiring no additional maintenance, while also supporting industry standards for external light sources; preserving design flexibility across different system architectures and providing the industry with a US foundry supply source for multi-wavelength light sources.

Intel uses near-packaged optics and co-packaged optics to push optical components as close as possible to compute chips and network switch chips, shortening the transmission path for high-speed electrical signals and easing the signal attenuation and power burden of copper wiring in high-speed, long-distance scenarios.

Intel's stated energy target is to reduce the transmission energy of optical interconnect systems to under 5 picojoules per transmitted bit.

For data-centre operators, if optical interconnects can push energy per transmitted bit below 5pJ bit$^{-1}$, it would directly affect the power allocation and thermal design of large-scale AI clusters, which in turn would influence rack density and total cost of ownership.

However, before industry standards are settled and repair models are validated, most operators are expected to first verify reliability through small-scale deployments before gradually scaling up adoption.

# Infineon and NVIDIA collaborate on GaN-based power conversion

Companies to focus on high-voltage intermediate bus converter for 800 $V_{DC}$ AI data centres

Infineon is advancing its collaboration with NVIDIA on 800 Volt direct current ($V_{DC}$) power architectures for AI data centres.

This builds on the companies' joint work first announced in May 2025 and detailed further in October 2025, which centred on serviceable, hot-swappable 800 $V_{DC}$ server racks.

Timed with NVIDIA's GTC Berlin developer conference, the announcement centres on the high-voltage intermediate bus converter (IBC), one of the most critical and demanding conversion stages in the power delivery chain of AI data centres.



"AI is fundamentally reshaping the demands we place on power infrastructure, and semiconductors are at the heart of solving that challenge," said Jochen Hanebeck, CEO, Infineon Technologies AG.

"Our collaboration with NVIDIA on 800 Volt power architectures shows what is possible when deep semiconductor expertise meets the pace of innovation required by AI."

Driven by the extreme power draw of AI workloads, data centres have adopted intermediate-bus architectures in which an IBC steps down the main bus voltage feeding accelerator cards into a lower-voltage rail, allowing downstream stages to efficiently generate the tight core and point-of-load rails that AI processors require.

This multi-stage approach reduces distribution losses, all while meeting strict constraints on board area, thermal limits and uptime. As AI infrastructure scales, 800 $V_{DC}$ is being introduced alongside existing AC and lower-voltage DC architectures as an additional distribution option for higher-density compute.

Compared to silicon, GaN allows power devices to switch significantly faster with lower losses, which enables higher switching frequencies of up to 1 MHz at the IBC stage. This in turn allows the size of magnetic components and passives to shrink considerably, directly translating into higher power density and lower board heights, a critical advantage as rack space becomes an increasingly scarce resource in AI data centres.

At the same time, GaN's low conduction and switching losses support best-in-class conversion efficiency, helping to limit heat generation, even as power levels per rack continue to climb toward the megawatt range. Infineon says that these characteristics make GaN the preferred semiconductor technology today capable of meeting the combined demands of power density, efficiency, and fast transient response at the IBC stage.

Infineon and NVIDIA collaborate along the entire data centre power chain. In addition to IBCs, this also includes power path protection solutions, as announced in October 2025, targeting safety and service aspects, such as the hot-swap controller functionality, and enabling future server boards to operate in 800 $V_{DC}$ power architectures.

GaN's low conduction and switching losses support best-in-class conversion efficiency, helping to limit heat generation, even as power levels per rack continue to climb toward the megawatt range

# Power GaN patenting in Q2 2026

KnowMade's latest patent monitor reveals a concentration of inventions around enhancement-mode transistors

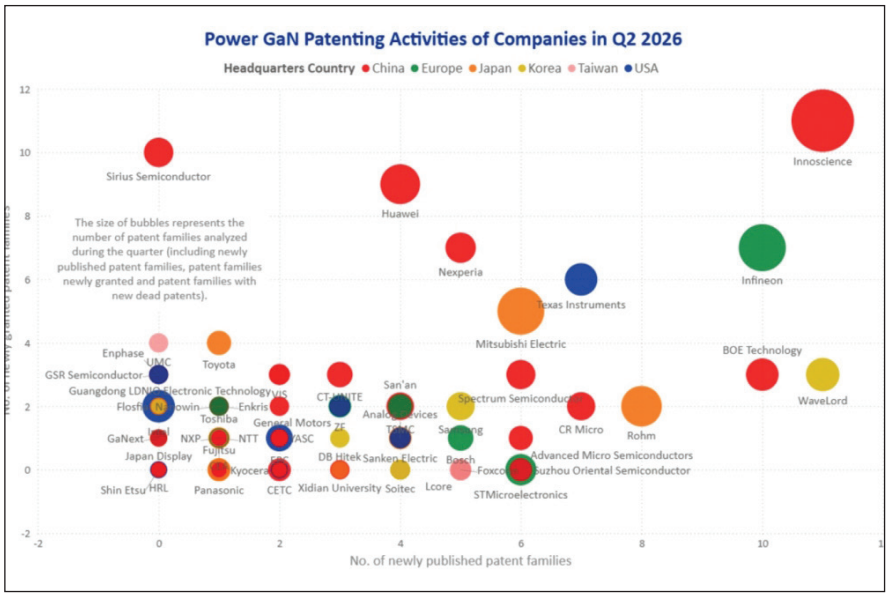
KNOWMADE'S Q2 2026 Lateral Power GaN Patent Monitor reveals a quarter led by industrial patent assignees, while several Chinese universities maintained a strong presence in GaN power device innovation.

Around 500 patent families were published in the power GaN patent landscape during Q2 2026, and approximately 300 patent families received a grant for the first time. At the individual patent level, around 800 new patents were granted. Meanwhile, close to 120 patent families had patents that expired or were abandoned by their assignees.

Assignees focused their patent protection efforts primarily on China and the United States. Europe and South Korea also showed positive filing dynamics during the quarter, in contrast with Japan and Taiwan.

Across the supply chain, newly published inventions concentrated on power GaN devices, particularly enhancement-mode transistors, and on circuits and applications incorporating these devices. Thermal management remained a recurring technical theme, spanning wafers, devices, packaging, modules and circuits.

In power GaN devices, Innoscience stood out for its newly published and newly granted inventions. Measured by the number of individual patents newly granted during the quarter, however,




Innoscience, Texas Instruments and Samsung reached similar levels. Among academic assignees, UESTC and Xidian University showed strong device IP activity; UESTC has also recently accelerated its filings related to circuits and applications.

Upstream, WaveLord led wafer and epiwafer activity by both newly published and newly granted patent families. Its number of newly granted individual patents also placed it ahead of Soitec, Taiwan-Asia Semiconductor and Siltronic in this segment.

In packaging and modules, Nexperia and Mitsubishi Electric shared the lead in newly published and newly granted patent families. Further downstream, automotive companies were prominent among the most active assignees for circuits and applications, including General Motors, Volkswagen, Marelli and Bosch, alongside Infineon.

The landscape also gained around 100 new entrants, approximately 70 percent of them being Chinese companies. Roughly 75 percent of newcomers entered through circuits and applications, the most downstream part of the power GaN supply chain. This includes all identified newcomers from the United States – four companies and one state-backed organisation – and Europe – two universities and three companies.

Across the supply chain, newly published inventions concentrated on power GaN devices, particularly enhancement-mode transistors, and on circuits and applications incorporating these devices. Thermal management remained a recurring technical theme, spanning wafers, devices, packaging, modules and circuits.

# Infineon signs 200 mm SiC wafer agreement with Wolfspeed

Multi-year agreement with Wolfspeed supports Infineon's conversion from 150 mm to 200 mm SiC manufacturing

INFINEON and Wolfspeed have signed a new multi-year supply agreement for 200 mm SiC wafers, changing Infineon's existing Wolfspeed supply relationship from 150 mm to 200 mm substrate technology.

"SiC is at the heart of the energy transition, and securing a high-quality, resilient supply of 200 mm substrates is essential to delivering on our customers' long-term commitments," said Alexander Gorski, COO at Infineon.

"This agreement further broadens our strong supply base for our 200 mm high-volume manufacturing, building on a 20-year supply relationship between our two companies."

"It strengthens supply chain security for our customers and provides additional flexibility and scalability to support Infineon's future growth."

AI data centres are beginning to emerge as a significant demand driver for SiC power semiconductors. Power conversion efficiency across the data centre power chain is a direct operating cost consideration for hyperscalers managing infrastructure at scale.

The switching efficiency and thermal performance of SiC make it a technically suitable option for specific power conversion stages where silicon reaches its practical limits.

Together with growing SiC adoption across electric vehicle drivetrains, solar inverters and industrial motor drives, these trends support a strong long-term outlook for high-quality 200 mm SiC substrates.

The transition to 200 mm SiC wafers delivers large manufacturing economics compared to 150 mm production. Larger



wafer diameter increases usable die area per wafer, reduces per-unit substrate cost, and improves overall manufacturing efficiency.

Infineon operates a multi-source SiC substrate strategy to maintain supply chain flexibility, including its 200 mm SiC fab in Kulim, Malaysia, which is designed to be the world's largest and most competitive SiC manufacturing facility.



# XMax to acquire GaN firm Hexa Creation

Transaction gives XMax footing in high-voltage GaN power technology for data centre infrastructure

XMax, a distributor of contemporary furniture and AI software, has entered into a share purchase agreement to acquire all the shares of Hexa Creation, a US-based early-stage power semiconductor company focused on 1200 V vertical GaN technology.

XMax wants to extend its AI strategy into power infrastructure for AI computing and other high-voltage applications. The company believes the acquisition supports its broader strategy of diversification and long-term value creation.

Hexa Creation's technology roadmap centres on a native 1200 V vertical GaN trench MOSFET designed for high-voltage and high-power applications beyond the 650 V-and-below range where much of today's commercial GaN market is concentrated. Hexa holds an exclusive license to certain patents and related IP owned by one of the largest public universities in the United States supporting its high-voltage vertical GaN technology platform.

As next-generation AI data centres move toward higher-voltage power architectures, including emerging 800 $V_{DC}$ systems, XMax believes demand may increase for high-efficiency, 1200 V-class power semiconductor devices. Hexa Creation is targeting these emerging AI power-infrastructure applications, as well as electric vehicles, energy storage, ultra-fast charging and other high-voltage markets.

"This acquisition marks XMax's entry into high-voltage power semiconductors, a field closely tied to the growing power demands of AI infrastructure. The acquisition of Hexa Creation diversifies our business opportunities and complements XMax's growing AI business as XMax builds out AI software, platform-based



and GPU services through our wholly owned subsidiaries XMax AI Inc. and Elonx AI Holdings PTE. Ltd.," said Andy Lu, CEO of XMax.

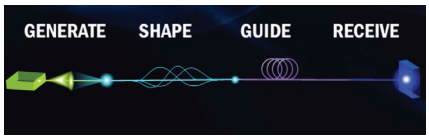
"We believe the acquisition by XMax would give our 1200 V vertical GaN work a path toward commercialisation. We believe vertical GaN can bring higher efficiency and power density to high-voltage applications, and XMax's support allows us to focus on advancing that technology." said Yuji Zhao, CEO and founder of Hexa Creation.

# Coherent launches PhotonLink platform for next gen data centres

PHOTONICS firm Coherent has announced PhotonLink, an integrated optics platform that brings together Coherent's portfolio of photonics technologies, assembly and test capabilities to deliver complete optical solutions for next-generation AI data centres.

The platform supports co-packaged optics (CPO), near-packaged optics (NPO) and emerging chip-to-chip connectivity.

"The next leap in AI requires more than faster chips – it requires a new way to connect them," said Jim Anderson, CEO at Coherent. "Customers need complete optical solutions, not just individual components. Coherent is uniquely positioned to bring together the critical technologies, integrate and test the finished assemblies, and




manufacture them at scale. PhotonLink puts that capability to work for the next generation of AI infrastructure."

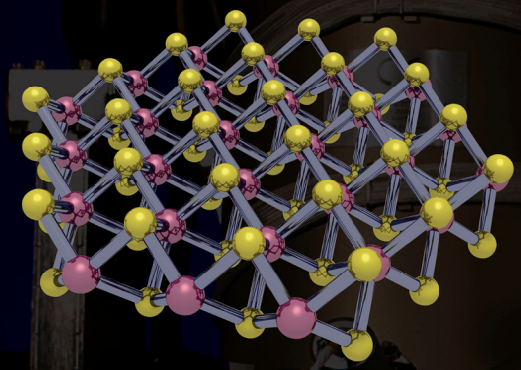
The PhotonLink platform spans four functions of the optical path: Generate, Shape, Guide and Receive. The portfolio includes InP lasers, VCSEL arrays, silicon photonics, isolators, specialty fibres, micro-optics and detectors. Coherent integrates these technologies into external laser sources, precision fibre assemblies and optical modules tailored to customer architectures.

Coherent has more than ten CPO customer engagements and more than ten NPO engagements, with anchor customers and long-term agreements secured for both architectures. The company also has more than five engagements in emerging chip-to-chip connectivity. Revenue from the PhotonLink platform is expected to begin ramping in Q4 of CY2026.

PhotonLink builds on Coherent's data centre manufacturing base, which has shipped more than 300 million InP lasers and more than one billion InP and GaAs photodetectors. Coherent is expanding its 6 inch InP and specialty fibre manufacturing capacity to support the PhotonLink ramp.

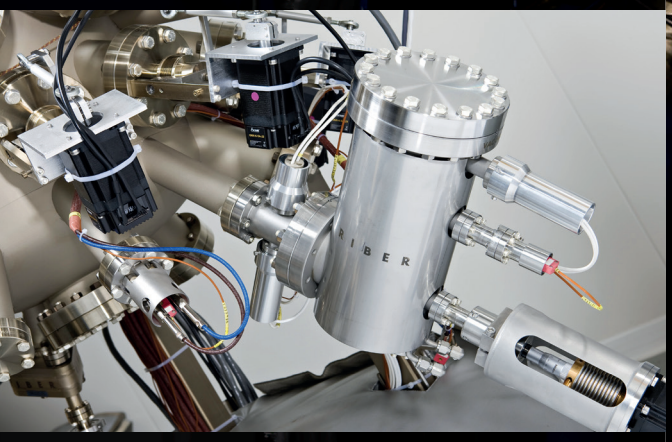
Coherent hosted a PhotonLink launch event on September 21 at the Gran Hotel Miramar in Málaga during the European Conference on Optical Communication (ECOC) 2026.

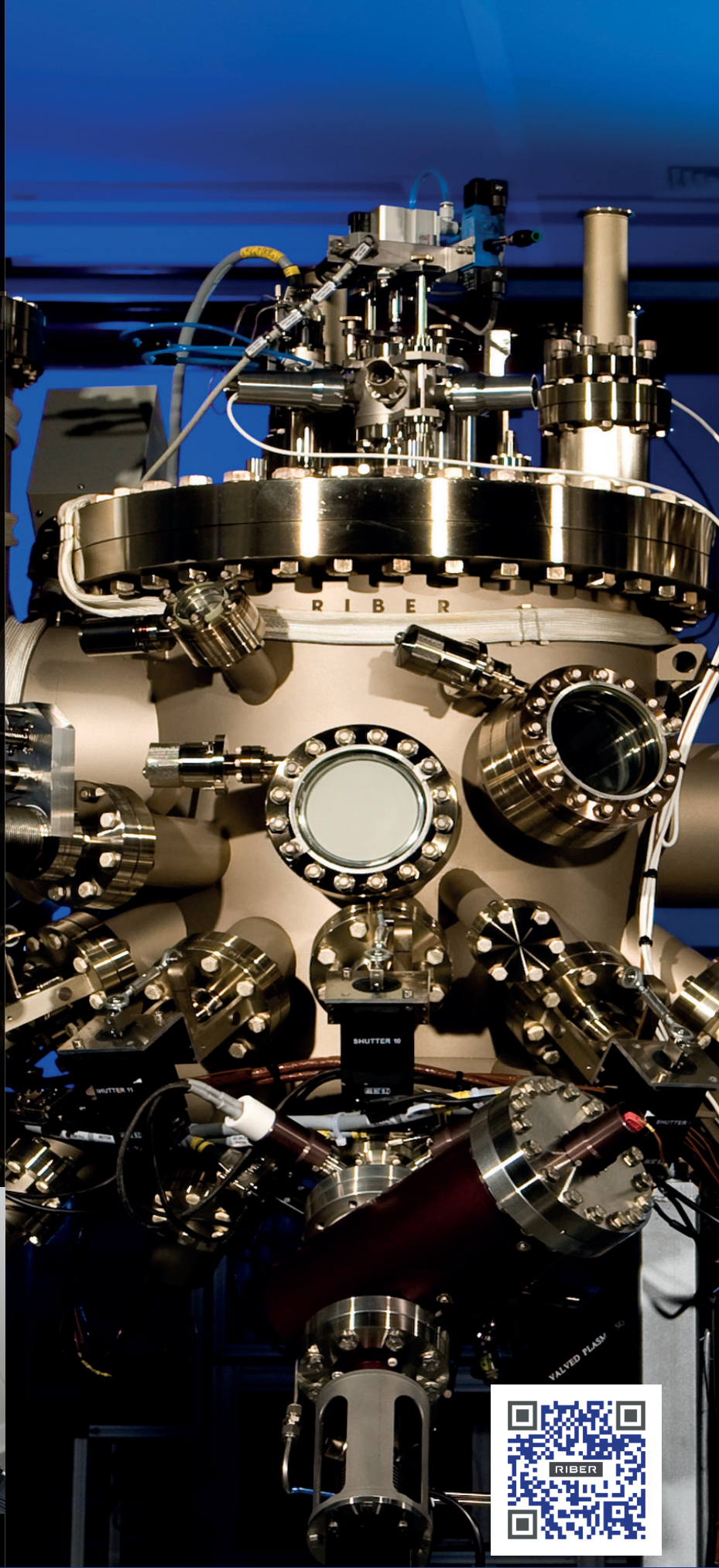
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# Diamond delivers a hike in power density

Northrop Grumman's GaN HEMTs deliver a five-fold increase in RF power density, thanks to the exceptional thermal conductivity of polycrystalline diamond

**BY RICHARD STEVENSON, EDITOR, CS MAGAZINE**

OUR INDUSTRY does not rest on its laurels. Following the emergence of any ground-breaking device, it's not long before efforts are directed at finding ways to deliver a hike in its performance.

For the RF GaN HEMT, DARPA is driving improvements in key metrics through a programme entitled THREADS: Technologies for Heat Removal in Electronics at the Device Scale. Within this programme, diamond is viewed as the ultimate material for optimising heat extraction, due to its incredibly high thermal conductivity – it's five times that of copper.

Thanks to diamond's exceptional thermal conductivity, devices drawing on this attribute run cooler, opening the door to operation at far higher power densities. That's valued in many applications, including advanced radar, satellite communication, several forms of secure communication, electronic jamming and very high-performance sensing. Armed with more powerful devices, designers can construct systems that deliver an increase in performance; or maintain performance while using fewer devices, leading to a trimming of size and cost.

A key player in the THREADS programme is Northrop Grumman, which is working with engineers at Stanford University.

Efforts at Northrop Grumman began in December 2023, supported by



$6.4 million from DARPA, which financed the fulfilling of the key objectives of the first phase of the project. They include propelling the power density for GaN-on-SiC HEMTs operating below 10 GHz from a previous benchmark of around 5-7 W $mm^{-1}$ to around five times this figure. That's an ambitious goal to set – but DARPA is well-known for instigating programmes with very challenging objectives.

"We were able to achieve 26 watts per millimetre," remarks Ben Heying, Director of Microelectronics at Northrop Grumman's Space Park Foundry, who explains that this success stemmed from trimming thermal resistance. The team dropped the thermal resistance by '0.37X' – exceeding the '0.40X' target reduction.

Heying is keen to emphasise another important success realised in phase I, which is reliability.

"When you're powering a device at these high powers, they typically don't last too long, because the temperature gets very, very high. But we were able to achieve 1,000 hours, so very good stability."

This matters to Northrop Grumman, which has little interest in 'hero' results.

"We want to get something that we can actually put into our systems," explains Heying, pointing out that this implies strict reliability requirements.

Not included in the objectives of the THREADS programme is a requirement for the maximum operating temperature of the HEMT. But that does not mean the team at Northrop Grumman doesn't record this.

Heying says that throughout the programme he and his team have been developing thermal models that account for different materials, and measuring thermoreflectance – the temperature changes inferred from how a material reflects light to gauge the temperature of the device.

## Cooler diamond

Key to Northrop Grumman's success is the deposition of diamond at a low temperature, a step undertaken at Stanford University. Deposition occurs after forming the HEMT and its accompanying circuitry, and thinning the SiC substrate to around 100 µm.

While the growth of diamond is carried out in a commercial reactor, the process is not trivial. Heying describes the details as 'very proprietary'.

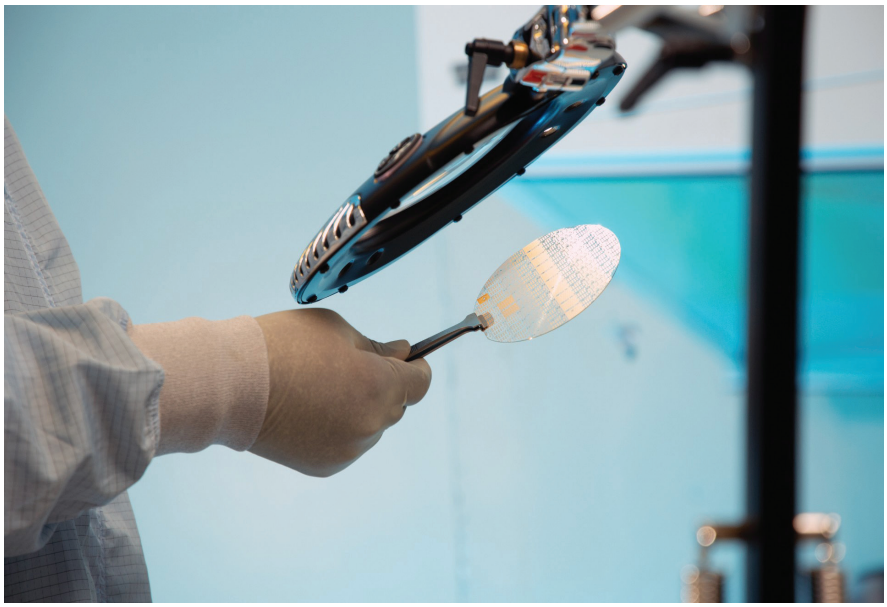
Using a low growth temperature avoids damage to the HEMT, but risks the deposition of graphite, which has an inferior thermal conductivity. Engineers at Stanford take care to avoid this, growing high-quality grains with a diameter of the order of 50 µm.

To optimise HEMT performance, engineers form a channel in the SiC along the width of the gate, which is the hot spot for this transistor. Into this trench goes diamond, to ensure that the device benefits from a very low thermal resistance. The transistor is designed so that following extraction of heat from the hottest region, lateral spreading takes place, to enhance thermal management.

## Phase II

Recently, DARPA awarded Northrop Grumman an additional $7 million to participate in phase II of the THREADS programme, running until the end of 2027. Efforts are directed at delivering an additional three-fold increase in power density.

Heying is not divulging details surrounding how the team will tackle this next goal, but does reveal that efforts will be directed at optimising the handling of the electrical fields within the HEMT, and how the materials come together.



Working in partnership with Stanford University, engineers at Northrop Grumman have developed more powerful RF HEMTs, which feature exceptional heat extraction close to the gate, thanks to the addition of polycrystalline diamond.

"The pure materials that we're working with have a fairly good thermal conductivity, but we're putting multiple layers together, and every time you do that you end up with an interface. So, you have to engineer those as well."

## From R&D to production

It will not be long before Northrop Grumman's success in the THREADS programme benefits its customers.

"Over the next couple years, probably a year and a half, we're going to be taking a variant of that Phase I device and turning that into something that we can put into production."

What's not clear is whether the new commercial products will feature diamond-based cooling. Note, though, that Northrop Grumman has this capability in-house, and could transfer technology from Stanford.

So, many pure-play commercial customers, as well as those working in the defence sector, could soon benefit from the breakthroughs at Northrop Grumman.

This US-based company has partners all around the world, and so as long as they are granted an export license, they will be beneficiaries from more powerful HEMTs with superior cooling, possibly thanks to the addition of diamond.

Key to Northrop Grumman's success is the deposition of diamond at a low temperature, a step undertaken at Stanford University. Deposition occurs after forming the HEMT and its accompanying circuitry, and thinning the SiC substrate to around 100 µm. While the growth of diamond is carried out in a commercial reactor, the process is not trivial. Heying describes the details as 'very proprietary'.

# Polar: Another convert for GaN-on-silicon

Licensing technology from imec expands Polar Semiconductor's GaN portfolio with the addition of E-mode devices operating at various voltages

**BY RICHARD STEVENSON, EDITOR, CS MAGAZINE**

FOR MANY YEARS, our industry has banged the drum for GaN-on-silicon power electronics. We've been championing this technology by highlighting the low on-resistance that boosts efficiency, and the capability to switch at very high frequencies, opening the door to smaller and lighter power supplies.

Recently, the compelling case for GaN has been winning converts in the silicon industry. They include Polar Semiconductor, a US-owned foundry that's based in Bloomington, Minnesota, which is near Minneapolis. Expanding beyond its strong pedigree in silicon power devices, Polar started by licensing D-mode GaN HEMT technology from the Japanese chipmaker Renesas; and now it is adding the E-mode variant to its line-up, by engaging the expertise of IC-Link, imec's design and manufacturing division.

Polar has a rich history within the semiconductor industry. Founded in 1962 under the moniker Control Data, it initially focused on the manufacture of ICs for the hard-disc-drive industry. Construction of a 2-inch fab followed in the late 1960s, enabling the facility to operate as a captive foundry. Over the intervening years two additional fabs have been built on the site, wafer size has increased – including the introduction of a 200 mm line in the early 2000s – and ownership has changed hands. Sanken Electric acquired the company in 2005, prior to shared ownership, with Sanken accounting for 70 percent and Allegro the other 30 percent.

Among the many changes over the years, arguably the biggest is the recent transformation. This includes a take-over by private equity firms, and the drawing of funding from the US CHIPS Act that is designed to help drive Polar's expansion into GaN power devices, and ultimately strengthen domestic production of GaN HEMTs.

Supported by a total investment in the facility of up to $525 million, Polar has changed its role to a merchant foundry, and updated its 100,000 ft$^2$ facility. The injection of cash is aiding efforts to double production capacity from 20,000 wafers per month.

Helping to grow this capacity, according to Polar Vice President of Marketing, Ken Obuszewski, is the purchasing of about 150 new tools. "We have added automation and overhead transport," says Obuszewski, who explains that visitors are impressed by the modernisation of the 200 mm fab.

Alongside new tools has been a rise in head count, increasing by about 20 percent to more than 600 staff.



➤ The modernisation of Polar's 200 mm fab includes the introduction of overhead transport.

## Turning to GaN

Over many decades, Polar has solidified its position as an expert in power semiconductors. This includes discretes, such as MOSFETs and IGBTs, and a technology referred to as BCD, which is short for bipolar-CMOS-DMOS.

"We do BCD up to 900 volts, and even up to 1,200 volts; IGBTs at 1,200 volts," says Obuszewski, who claims that GaN fits very well into this power legacy.

Driving Polar's interest in wide bandgap technology is the opportunity to gain an edge over its silicon-centric rivals.

"Silicon discretes is a very mature technology, so it's harder to differentiate yourself. You're more likely to be competing on pure price," says Obuszewski, who argues that by diversifying into GaN, Polar has the opportunity to develop unique expertise.

The company has decided not to broaden its capabilities through the addition of SiC, viewed as a more mature technology that's suffering from an over-investment in capacity.

What's not in Polar's DNA is developing its own technology from scratch, and bringing this to market.

"We've taken the smart approach to work with people who have expertise in GaN, and to leverage their learnings and apply it to our foundry."

Polar enjoys frequent engagement with Renesas and Imec. At times, engineers are on site, helping to solve more challenging problems.

"But it's not to the point where we need somebody co-located, constantly," says Obuszewski. "We've been growing our own GaN team as well. We're now up to four integration engineers."

At present, Polar does not produce GaN-on-silicon epiwafers in house. Instead, it sources from a third party. Due to this, there's a need for incoming inspection, partly due to concerns related to bow. In this regard, Renesas offers salient advice.

In addition, the Japanese chipmaker has helped to offer solutions to address the threat of contamination. This has been a concern, given that Polar is not dedicating a line to just GaN.

According to Obuszewski, what's been the most challenging task to date is the development of the ohmic contact and its etching, to optimise for on-resistance.

## GaN foundries

Against a backdrop of growing sales for GaN-on-silicon technologies, the decision by TSMC to exit this business will have raised a few eyebrows.

For those offering these services, or intending to do so, the move by TSMC gives them more opportunity, since a strong ecosystem of GaN foundries is yet to be established.

Today there are not that many GaN foundries, according to Obuszewski. Off the top of his head, he lists Vanguard and Power Chip in Taiwan, the German chipmaker Global Foundries, and X-fab, which is based in the US.

"The world is bifurcating. Any large semiconductor company needs a China supply chain and a Western supply chain. We fit very well with the Western supply chain."

## From D-mode to E-mode

Thanks to the licensing agreement with Renesas, Polar has established a 650 V D-mode technology. The deal with imec is now broadening that portfolio considerably – as well as adding E-mode, there's an expansion of the voltage range. Initially at 600 V and 100 V, there's the potential to go further in both directions.

"The current 100-volt can scale down to 40 volts," says Obuszewski, adding that this is then expected to reach to 24 V.

"Low voltages are very interesting, especially around the data centre architectures."

At the other end of the spectrum, there's an opportunity to use imec's technology for 1200 V devices.

Another advance Obuszewski anticipates is the introduction of monolithic integration. This move, involving the introduction of logic components, would eliminate the requirement for a separate drive chip.

As well as those goals, Polar plans to move from outsourcing GaN-on-silicon epiwafers to in-house production.

Understandably, a ramp in GaN revenue is also on the roadmap.

"We have clear line of sight to 10 percent, by the end of the decade," says Obuszewski. "But we have the opportunity to take that to 20 percent, based on the demand we're seeing."



# Better transistors won't solve your RF system issues

To ensure that world-class millimetre-wave transistors deliver their full potential, it's essential to optimise packaging, thermal design and integration

**BY TUDOR WILLIAMS FROM FILTRONIC**

THERE'S a tendency to assume that leaps in RF performance come from far better transistors. After all, that's held true for much of the past few decades. Yet, just like the stock market, past performance is no guarantee of future success.

For those of us that have developed microwave and millimetre-wave systems, it's common knowledge that system performance is not just determined by the device – beyond a certain point, what surrounds it is just as important. When frequencies rise, thermal management starts playing a critical role, along with packaging, manufacturing tolerances, and the interfaces between components.

In the millimetre-wave domain, small imperfections exert a measurable impact on efficiency, output power and overall system behaviour. As a result, the effectiveness of an RF system is not simply governed by the performance of the semiconductor device in isolation. What really matters is how successfully that technology is integrated into a robust, manufacturable solution.

## The frequency challenge

Success on this front is increasingly important, due to an inevitable shift towards higher frequencies in several significant applications. They include: communications networks, needing more capacity; satellites, demanding more throughput; and defence systems, expected to process and move greater volumes of data than ever before. As the spectrum available at millimetre-wave frequencies provides a way to meet those demands, development activity is continuing to move up, towards frequencies found in the Q, V, E and W-band.



An engineer at work at Filtronic's high-frequency engineering laboratory

Anyone who has spent time developing hardware at these frequencies knows that design challenges change quite dramatically when moving up the spectrum. At lower frequencies, strong device designs often mask weaknesses elsewhere in the system. But at millimetre-wave frequencies, that helpful margin largely disappears. In this domain once negligible losses increase in significance, packaging features start influencing electrical performance, and even small mechanical variations exert a measurable effect on the behaviour of the finished assembly.

Due to these issues, engineers must shift their focus from the device itself towards the performance of the subsystem as a whole. So, the challenge is not limited to just developing a high-performing transistor. While that's an essential starting point, the bigger test is ensuring that great performance survives the journey through MMIC design, packaging, interconnects, waveguide structures and every other part of the RF chain. At millimetre-wave frequencies, that's often where a system succeeds or falls short, and where many of the most interesting engineering challenges now exist.

## Packaging matters

Traditionally, packaging is viewed as a relatively trivial task, undertaken after the real RF design work is done. However, while that may have been true at lower frequencies, it is certainly not the case at millimetre-wave. Here, packaging is now very much part of RF design, and separating the two is increasingly difficult.

Those of us that have worked on high-frequency subsystems are painfully aware of this. We can recount times when a design looks excellent in simulation, and performs exactly as expected at the device level, before hopes are dashed when losses and discontinuities elsewhere in the signal path erode performance. There are many potential culprits. Bond wires, transitions, interconnects and package interfaces influence the result, with impacts increasingly pronounced as frequencies and power levels rise.

The real measure of success isn't what happens in the laboratory. It's whether that performance is reproduced consistently in a high-yield, long-lifetime manufacturable product, day after day, and unit after unit. Those goals demand as much attention to packaging, assembly and process control as to the device itself.

Increasingly, the best results are coming from close collaboration between RF designers, process engineers, packaging specialists and subsystem engineers, working in unison towards a shared system objective.

## The thermal reality

If there's one area where engineering ambition still has to answer to physics, it's thermal management. While compound semiconductor devices are continuing to deliver impressive gains in power density, and allowing engineers to squeeze more performance into ever-smaller footprints, there is no escaping the thermal consequences.

Higher power densities generate more heat, and extracting this in an efficient manner holds the key to achieving the performance that the device promises on paper. It's not uncommon that the largest constraint to output power, efficiency and even long-term reliability is the ability of the subsystem to dissipate heat effectively.



➤ High-volume, high-value manufacturing at Filtronic.

Due to this, it is inappropriate to consider thermal management as a separate engineering discipline. Instead, one must evaluate the direct influence of thermal behaviour on RF performance – it affects everything from gain and efficiency to stability and reliability. As a result, thermal modelling is increasingly intertwined with RF design, particularly at millimetre-wave frequencies, where performance margins may be tight and overall efficiency is typically lower. Invariably, the best solutions build thermal considerations into the architecture from the outset, rather than address this after completing RF design.

## Integration: the real differentiator

Today, success is increasingly defined by how well technologies are brought together, rather than the performance of any single component. Customers place their emphasis on whether the complete subsystem fulfils their requirements – it could be a satellite gateway, a defence platform or a communications network.

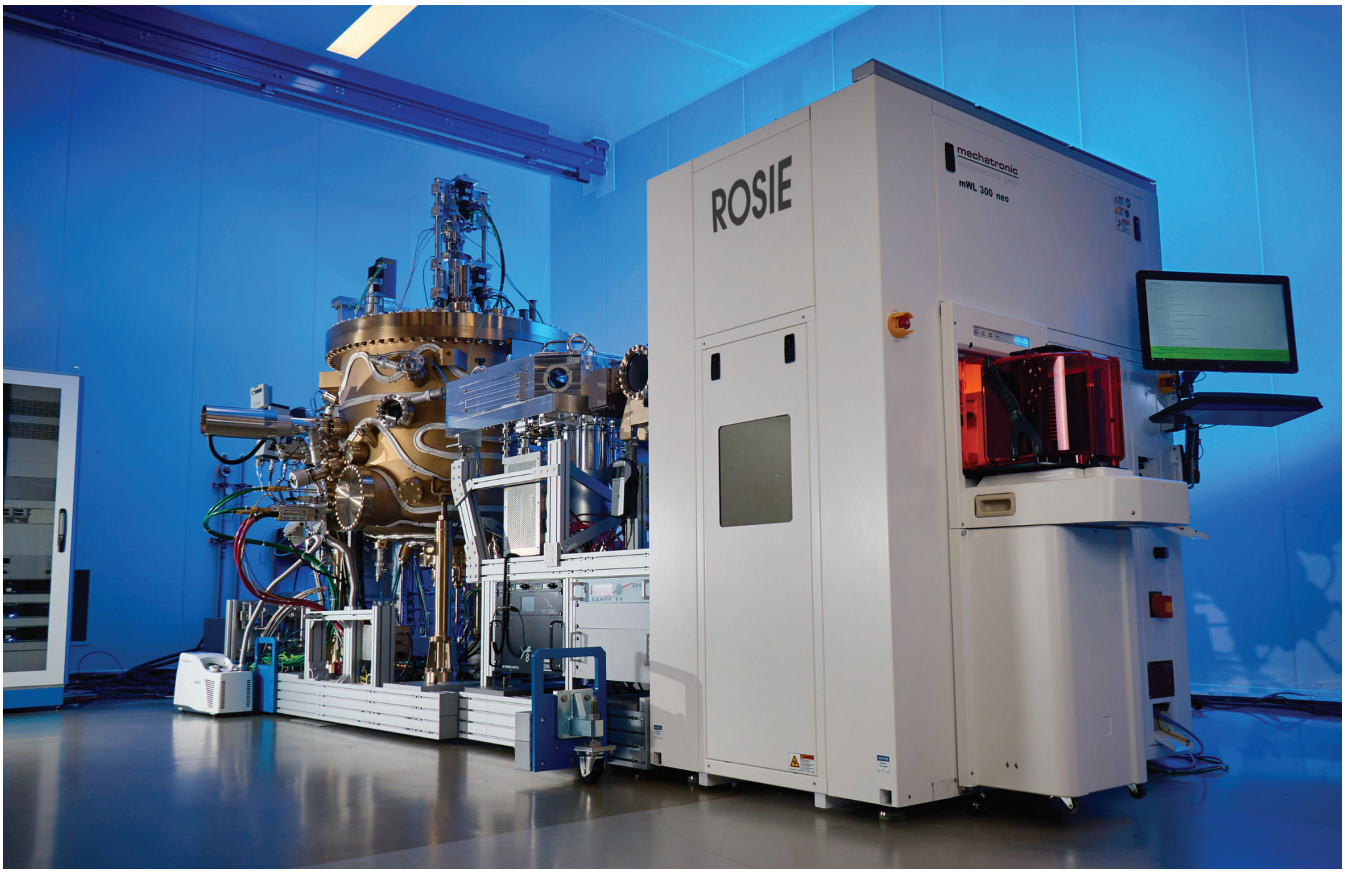
To excel in this regard, power amplifiers, filters, frequency-conversion stages, waveguide structures, antennas and control electronics must all work together, within a carefully engineered architecture. With system complexity on the rise, alongside operating frequency, the ability to integrate these technologies effectively is an increasingly important differentiator.

The good news is that over many years, there has been a much-needed shift towards system-level thinking. Engineers are now well aware that improving one aspect of performance tends to introduce a challenge elsewhere, whether that's thermal management, manufacturability, reliability, or size and weight constraints. The challenge is rarely about maximising a single parameter; it's about achieving the right balance across the subsystem.

## Beyond the transistor

As engineers take an increasingly holistic approach, compound semiconductor technology will still remain at the heart of high-frequency communications, with continued device innovation playing a key role in industrial progress. However, many key engineering challenges now sit beyond the semiconductor design itself.

To ensure that a device delivers its full potential, engineers must consider packaging, thermal management, manufacturability and subsystem architecture. These factors are increasingly important as the millimetre-wave era flourishes. Here, organisations that thrive are those taking a system-level view and recognising that competitive advantage is not simply a matter of building better devices, but integrating them into reliable, repeatable, high-performing RF subsystems.




# Functional oxides for 300 mm silicon

Silicon photonics and quantum computing will benefit from Riber's recent MBE platform, which supports the growth of oxides on 300 mm silicon

**BY CLAUDINE PAYEN FROM RIBER**

WE ARE living in an era experiencing a rapid growth in data traffic, driven by cloud computing, artificial intelligence and high-performance computing. Due to these trends, optical interconnects in data centres must improve, to satisfy demand for higher data rates, lower power consumption and greater integration density.

Key to addressing all these goals is a critical building block in the transmission chain, the electro-optic modulator – it converts electrical signals from electronic circuits into optical signals, which are subsequently transmitted down fibre at very high data rates. Much effort is directed at improving the performance of these modulators, which ideally combine a very high bandwidth with minimal power consumption, low drive voltage, low optical losses and high integration density, while remaining compatible with large-scale manufacturing processes.

One of the most attractive platforms for addressing this challenging list of requirements is silicon photonics. However, this material system has a fundamental limitation for electro-optic modulation: it fails to offer a significant intrinsic linear Pockels electro-optic effect. Due to this shortcoming, there is much interest in integrating materials that address this weakness head-on to overcome some of the limitations of conventional silicon modulators.

Among the various electro-optic materials under investigation, one with a particularly strong potential is barium titanate, which has the chemical composition $BaTiO_3$, and is often referred to as BTO. It is classed as a ferroelectric oxide, has a perovskite crystal structure, and exhibits high electro-optic coefficients.

When evaluating the promise of any material for electro-optic modulation, two key considerations are the voltage and the interaction length required to achieve a given phase shift. The desire for a low voltage, or a short interaction length, is captured by a metric known as the $V\pi L$ product. When BTO modulators are integrated on a silicon photonics

platform, the value for VπL can be as low as 0.2 V cm, realised alongside modulation at 25 Gbit $s^{-1}$.

Unfortunately, high Pockels coefficients do not guarantee a high-performance for an integrated modulator – a number of scientific and technological challenges must also be addressed before BTO can be deployed on a large scale.

One hurdle concerns material quality; and in particular, the crystalline quality of thin films, and the control of their ferroelectric domains. The electro-optic response of BTO depends strongly on crystallographic orientation, strain state and the ferroelectric domain configuration. Due to this, it is critical to control these parameters across the wafer, as this is needed to realise high, uniform and reproducible performance.

A second challenge relates to the integration of BTO with silicon photonics platforms. Currently under investigation are a variety of strategies, including epitaxial growth. Can any of these approaches combine high crystalline quality with integration schemes compatible with silicon photonics manufacturing?

## Opportunities in quantum tech

The excellent electro-optic properties of BTO ensure that this material is a promising one for quantum technologies, and in particular, quantum computing architectures operating at cryogenic temperatures. A key building block in this sphere is the superconducting-qubit processor, which manipulates quantum information in the microwave domain. Since optical photons are far better suited to the transmission of information over long distances, there's a need to develop interfaces between these two domains. Success is critical to advancing interconnected superconducting quantum processors that will ultimately enable distributed quantum computing.

With quantum architectures, electro-optic properties could make valuable contributions at several levels. That includes electro-optic modulators operating at low temperatures, as this enables the generation, routing and modulation of optical signals directly within a cryogenic environment. This technology is particularly attractive for the development of cryogenic photonic circuits, which could interface low-temperature systems with instrumentation operating at room temperature.

Note that BTO is especially promising in this context, as it retains its strong electro-optic response at cryogenic temperatures.

## From material control to device performance

Datacom and quantum applications share a common challenge: controlling the properties of BTO, to ensure a reliable, reproducible device performance. In this context, MBE is a particularly attractive approach. This class of epitaxy enables growth of thin films while ensuring very precise control of thickness, composition and interfaces. Thanks to the independent control of elemental fluxes, ultra-high-vacuum growth conditions and the use of *in situ* characterisation techniques such as RHEED, with MBE it's possible to monitor and optimise the earliest stages of growth.

This level of control is critical when integrating BTO on silicon. During the growth of perovskite oxides directly on silicon, there's the threat of an amorphous $SiO_2$ layer forming at the interface, and preventing epitaxial growth. To avoid this, engineers can insert a strontium titanate ($SrTiO_3$ or STO) buffer layer between silicon and BTO.

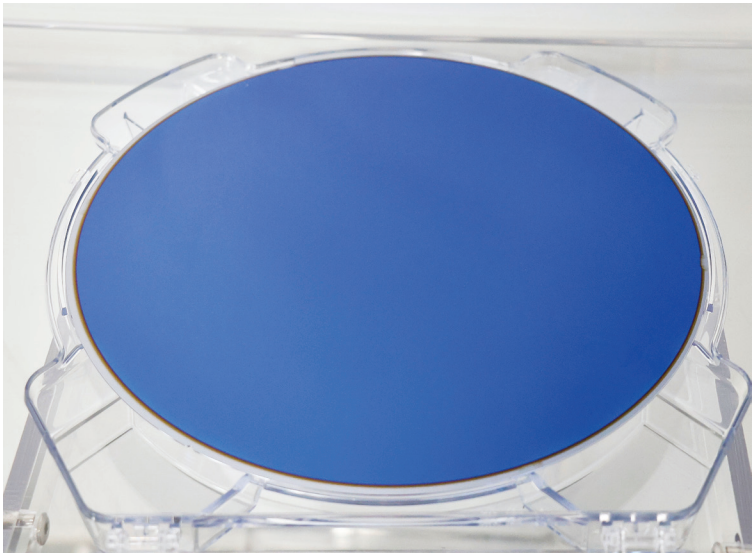
A team at Oak Ridge National Laboratory pioneered this approach. Many years ago, they demonstrated that precise control of the first monolayer enables epitaxial integration of perovskite oxides on silicon. Following engineering of the interface between silicon and STO, the latter provides a crystalline perovskite surface suitable for epitaxial growth of BTO.

Don't dismiss this STO buffer as just an intermediate layer: the oxide provides a key interface between silicon and the electro-optic material. Its crystalline quality, stoichiometry, and the structure of the interface between STO and silicon influence the orientation, defect density and strain state of BTO grown on top. Since these parameters are directly linked to the ferroelectric and electro-optic properties of BTO, it is a key technological challenge to control STO nucleation and growth.

With MBE, engineers enjoy precise control of the entire growth process, from silicon surface preparation through to the epitaxy of the STO buffer and BTO layer. These growers benefit from accurate control of the interfaces, stoichiometry, crystal structure and strain of the BTO/STO/silicon heterostructure.




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## ROSIE: a 300 mm silicon platform

Building on our patented reactor that's designed for oxide epitaxy, our company, Riber, has developed a platform for integrating functional oxides on silicon wafers. Our goal has been to combine the precise control of MBE with the requirements of the semiconductor and silicon photonics industries.

Our efforts led to the launch of ROSIE, which is short for Riber Oxide Silicon Epitaxy. It's a platform designed for the growth of functional oxides on 300 mm silicon wafers.

One feature of ROSIE is its architecture: front-opening unified pod to front-opening unified pod. This enables 300 mm wafer handling in an environment that's suited to silicon manufacturing requirements.

With the introduction of ROSIE, the objective is no longer simply demonstrating the outstanding properties of BTO on laboratory-scale samples. Now the aim is to develop and qualify processes directly relevant to industrial semiconductor infrastructure.

## Connecting materials and devices

To qualify ROSIE within a structured scientific environment and establish a direct link between material growth and device performance, we are playing our part in a three-year collaboration that also involves the Novo Nordisk Foundation Quantum Computing Program (NQCP)/Niels Bohr Institute (NBI) in Denmark. Our initiative is called POEM, which is short for Photonic Oxide Engineered Materials.

As part of this effort, we have installed ROSIE at the Niels Bohr Institute. This allows our expertise in MBE equipment and growth processes to be combined directly with NQCP/ NBI expertise in advanced materials, nanofabrication and quantum devices. Working together, we are aiming to shorten the learning cycles between material growth and functional device evaluation.

We have two process engineers working on the ROSIE platform, developing, optimising and stabilising the growth processes. These engineers are trying to control the silicon interface, optimise the STO buffer, and develop BTO growth processes. Their overriding objective is to establish reproducible processes on 300 mm silicon substrates. In parallel, Peter Krogstrup's team at NBI are using materials produced with ROSIE to fabricate and characterise devices, primarily targeting quantum applications.

As a next step we intend to establish a development loop that is particularly valuable for functional materials. Working in unison, we correlate device-level performance with the structural and functional properties of the layers, and draw on this to refine the growth conditions. By adopting this approach for BTO, we expect to gain a deeper understanding of the relationships between the STO/silicon interface, crystalline quality, strain, ferroelectric domains and electro-optic response.

## Serving the wider community

Our ROSIE project is not limited to the POEM programme. In parallel, we are engaging with the broader scientific and industrial community, by allowing them to get their hands on BTO/STO samples on 300 mm silicon, produced using the ROSIE platform. This allows them to evaluate these heterostructures without having to draw on their own dedicated MBE growth infrastructure. It is possible that these materials will be integrated into users' own fabrication processes, to develop and evaluate devices.

We expect that this opportunity will be particularly welcomed by communities working in silicon photonics, electro-optic modulators, cryogenic photonics and quantum technologies. By opening this materials platform to a wider range of users, we are exposing ROSIE-grown materials to a broader diversity of device architectures and applications.

What's clear is that our strategy behind ROSIE extends beyond the development of an MBE system. We are aiming to establish an ecosystem for integrating functional oxides on 300 mm silicon, by connecting growth equipment to process development, material engineering and device fabrication.

Ultimately, our ambition is to drive the evolution of MBE-grown BTO/STO/silicon heterostructures from research materials to a reproducible technology platform on 300 mm silicon. ROSIE promises to create a bridge between the outstanding electro-optic properties of BTO and their implementation in future integrated devices.

## FURTHER READING

➤ https://nqcp.ku.dk/about-nqcp/



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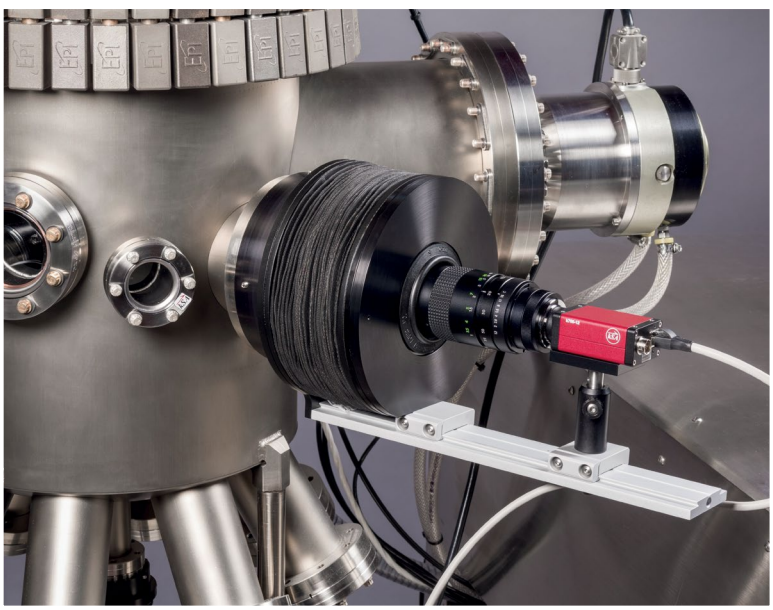
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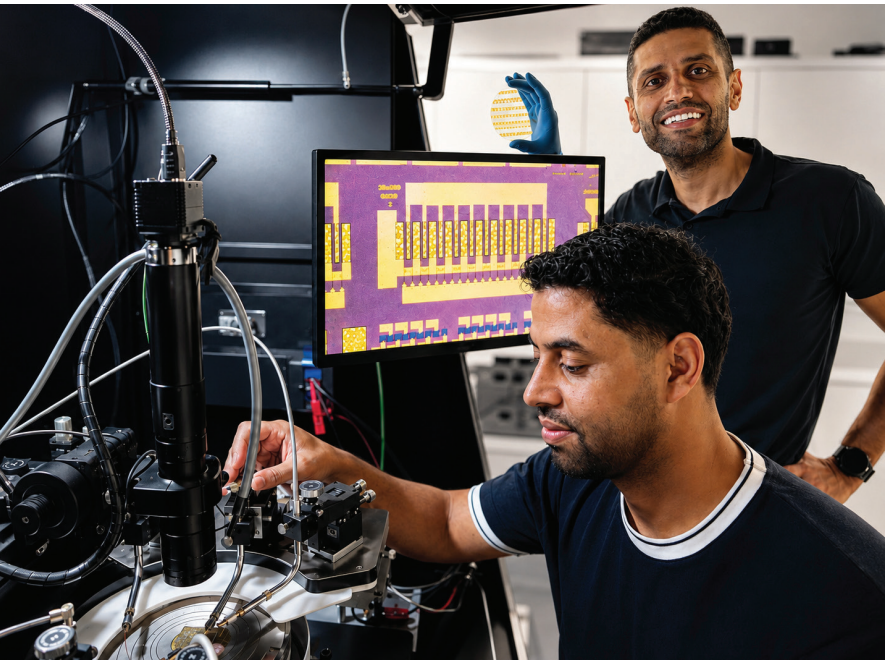
# Rethinking GaN on sapphire

A thin GaN-on-sapphire platform with carbon-buffer engineering and an AlGaN back-barrier delivers multi-kilovolt blocking, a low on-resistance and ampere-level currents

**BY ADRIEN BIDAUD, ABDELKHALEK SEFSSAFI, LYES BEN HAMMOU, ETIENNE OKADA, KATIR ZIOUCHE AND FARID MEDJDOUB FROM CNRS-IEMN AND AJIT PARANJPE FROM PRIMA INNOTECH**

WIDE and ultra-wide bandgap semiconductors are transforming the prospects for efficient power conversion. Within this portfolio, GaN has a number of key strengths. Its high critical electric field and excellent electron transport enable these devices to switch far faster than those based on conventional silicon technology, while handling higher voltages. But there is a concern with this class of power device: what substrate provides the best foundation?

The most common candidate is silicon, which attracts enormous interest, as it is inexpensive and available in large diameters. And another leading contender is SiC, offering outstanding thermal properties, but at a higher material cost.



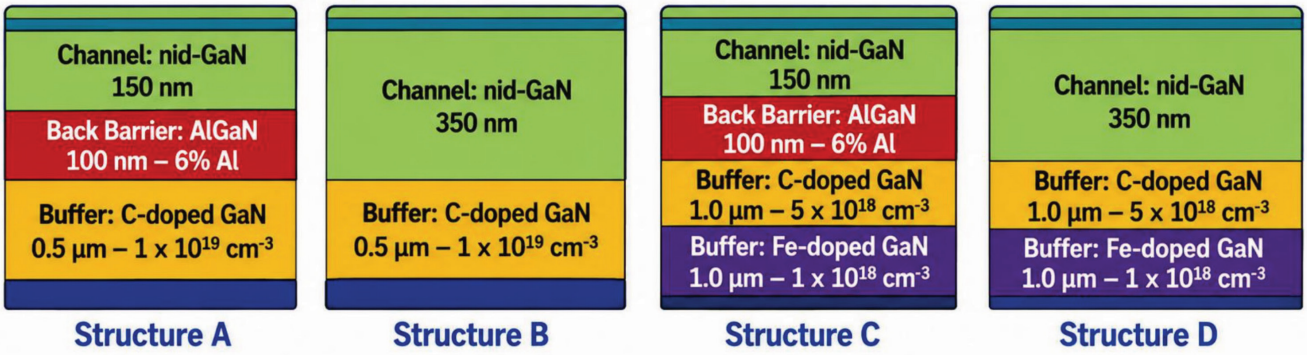
Often overlooked is yet another mass-produced substrate, sapphire. It tends to be viewed as a platform belonging to the optoelectronics world. That's understandable: sapphire is a mature, economical substrate for GaN epitaxy, but its relatively low thermal conductivity suggests it is not well-suited to high-power switching.

However, recent work by our team – a partnership between engineers at the Institute of Electronics, Microelectronics and Nanotechnology in Lille, France, and Prima Innotech – suggests that this judgement is too simplistic. Rather than asking whether sapphire is the perfect substrate in every respect, we have asked a different question: how good can the high-voltage performance from a thin GaN-on-sapphire stack be when the buffer, channel confinement and electric field are deliberately engineered together?

The answer is both surprising and encouraging. We have discovered that field-plate-free lateral HEMTs on thin GaN-on-sapphire structures can deliver blocking voltages as high as 5.5 kV, while preserving a competitive specific on-resistance and scaling to high currents. While these results don't remove sapphire's thermal limitation, they show that this must not be confused with an inability to support excellent electrical performance.

## Revisiting sapphire

There are a number of good reasons to take another look at sapphire. Following decades of LED manufacturing, GaN-on-sapphire has a




➤ Figure 1. Epitaxial stack engineering investigates the effects of channel thickness, AlGaN back barrier, and buffer design.

mature epitaxial ecosystem based on a relatively inexpensive substrate. Thanks to this infrastructure, high-quality GaN layers can be grown on a platform already established for large-scale compound semiconductor manufacturing.

The usual objection is heat. As sapphire's thermal conductivity is only about 40 W $m^{-1}$ $K^{-1}$ – so far below that of SiC – there's the threat that a GaN device that dissipates substantial power will experience a higher channel temperature. As this is a genuine concern for high-current power transistors, any realistic GaN-on-sapphire roadmap must address this issue, rather than ignore it.

But the thermal conductivity is not the only property determining the usefulness of a power platform. Device designers also consider blocking voltage, leakage, on-resistance, dynamic behaviour, manufacturability, and ultimately the possibility of integrating the active layers with another heat-spreading material. Due to this, our approach is to consider two separate questions, often bundled together: can sapphire support a very strong GaN power device electrically, and if so, how should one manage its thermal weakness?

## Thin by design

Conventional routes to realising higher blocking voltages in lateral GaN transistors often rely on lengthening gate-to-drain distances, adding thicker buffers and introducing field plates. These three levers can be effective, but each carries a penalty. Extending the access region increases resistance; thicker buffers require more epitaxial material, potentially increasing growth time and mechanical stress; and field plates help to redistribute the electric field, but at the price of additional capacitance and process complexity.

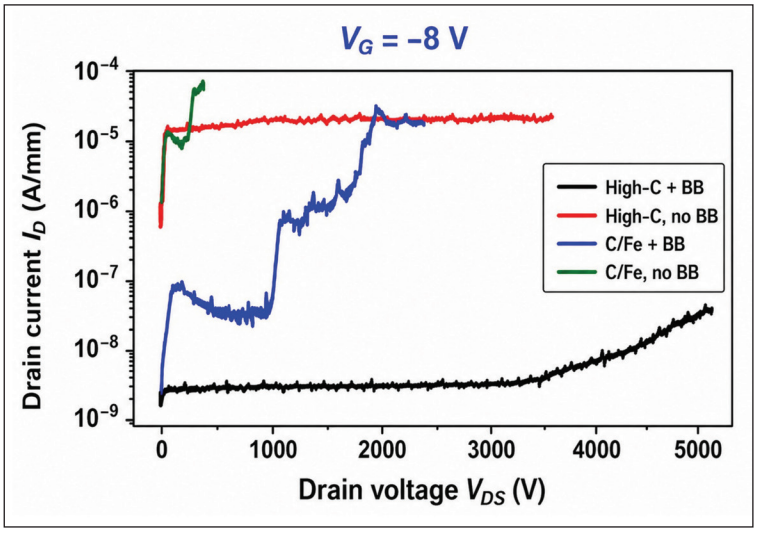
Due to these drawbacks, we wanted to discover how far we could go without extra electrostatic hardware. So, we avoided field plates when investigating whether variations in the gate-to-drain distance are a good way to realise voltage scaling. With this simple geometry, incorporating a gate length of 2 µm, the emphasis is on the epitaxial stack.

Our optimised structure contains a 20 nm-thick AlGaN barrier, a 150 nm-thick unintentionally doped GaN channel, a 100 nm-thick $Al_{0.06}Ga_{0.94}N$ back-barrier and a carbon-doped GaN buffer that's just 0.5 µm-thick. The carbon concentration in this high-resistivity buffer is around $1 \times 10^{19}$ $cm^{-3}$.

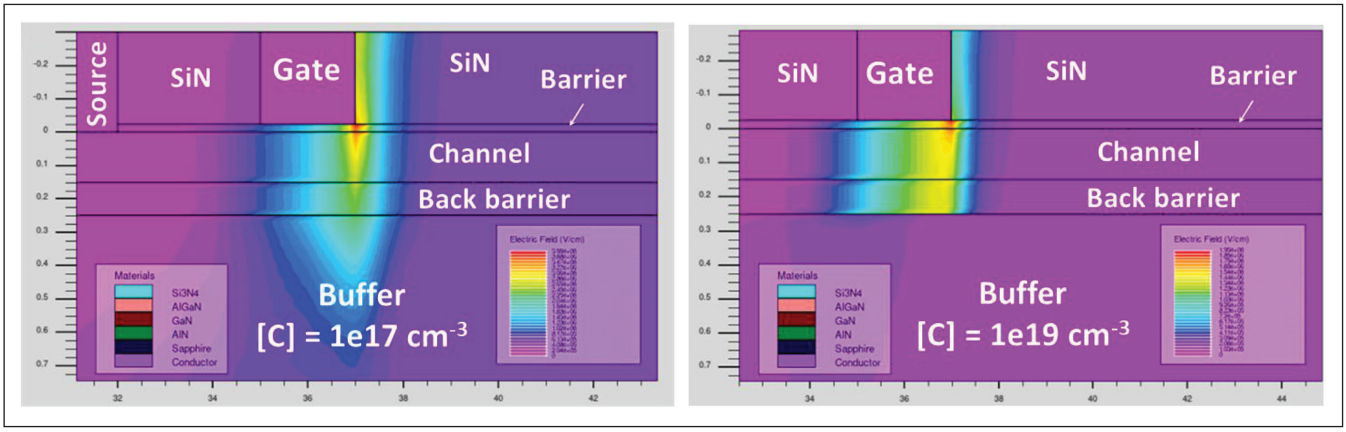
Crucially, a stack that's suitable for blocking high voltages does not destroy the transport properties of the channel. According to Hall measurements, our heterostructure has a sheet carrier density of about $8.6 \times 10^{12}$ $cm^{-2}$, an electron mobility close to 1800 $cm^2$ $V^{-1}$ $s^{-1}$, and a corresponding sheet resistance of roughly 400 ohms per square. These values, indicative of a high-quality two-dimensional electron gas, show we have a low-resistance foundation for efforts directed at blocking several kilovolts.

## Shaping the field

In our devices, the two key epilayers below the channel perform different tasks. The carbon-compensated GaN buffer plays a significant role in suppressing the off-state leakage and delaying vertical punch-through, while the AlGaN back-barrier raises the conduction band below the channel, improving electron confinement and reducing spillover into the buffer.




➤ Figure 2. Off-state blocking, showing how buffer insulation and back-barrier confinement shape leakage behaviour.




➤ Figure 3. Electric-field engineering in the buffer. Technology computer-aided design maps at a drain bias of 1 kV show that increasing the carbon concentration from $1 \times 10^{17}$ cm$^{-3}$ to $1 \times 10^{19}$ cm$^{-3}$ substantially reduces the peak electric field beneath the gate.

Our investigations, involving experimental work and simulations based on technology computer-aided design, highlight the contributions of various layers.

We have shown that an increase in the carbon concentration has the strongest impact on blocking capability. Simulations show that raising the carbon concentration in our 0.5 µm-thick buffer from $1 \times 10^{17}$ cm$^{-3}$ to $1 \times 10^{19}$ cm$^{-3}$ strongly redistributes the electric field beneath the gate. When blocking 1 kV, the calculated peak field in the GaN region falls from around 3.2 MV cm$^{-1}$ to about 1.8 MV cm$^{-1}$.

While the back-barrier has a more modest direct impact on breakdown voltage, it has a pronounced influence on confinement and leakage behaviour. That's crucial, because simply increasing compensation in the buffer is not enough: the channel must remain well controlled when the drain voltage rises. The best devices combine strong buffer insulation with good vertical confinement.

Our multi-faceted approach is the central message of our work. What we show is that a high blocking voltage does not have to come from a brute-force increase in epitaxial thickness or ever more elaborate field plates – it may also stem from shaping where the electric field and the carriers are allowed to go.

## Five kilovolts

The payoff of our approach is easy to see when we increase the gate-to-drain spacing. When extending this to 40 µm, our optimised field-plate-free transistor blocks 5.5 kV. This corresponds to an average lateral electric field of about 1.4 MV cm$^{-1}$ over the gate-drain region.

As expected, increasing the gap between the gate and drain leads to a higher on-resistance, because electrons have farther to travel through the access region. However, the specific on-resistance remains competitive, at around 15 mΩ cm$^2$ at the longest spacing. This value, combined with the measured breakdown voltage, yields a Baliga figure of merit above 2 GW cm$^{-2}$ – that's a useful measure of how effectively a power device combines high-voltage blocking with low conduction loss.

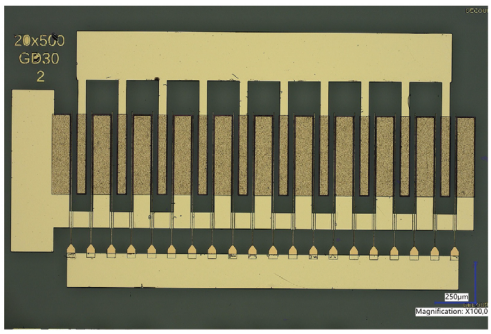
Note that this combination is more important than simply having a high breakdown voltage. Devices that block impressive voltages, but pay for this with excessive resistance, are of limited practical interest. When benchmarking our devices against other reported GaN-on-sapphire devices, as well as GaN devices on silicon and SiC and selected vertical structures, we find that they have a very competitive combination of specific on-resistance and breakdown voltage.

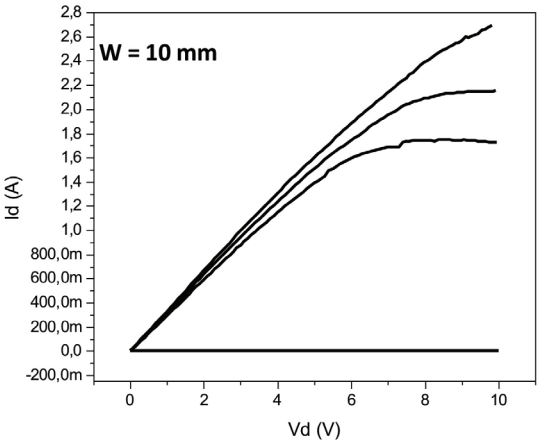
We must emphasise that our voltages are obtained without a field plate. That's not to say that field plates are undesirable; they remain powerful design tools. But demonstrating a blocking voltage of 5.5 kV without them shows that it is possible to transfer much of the electric-field management to epitaxial design. This equips future device engineers with the freedom to decide whether additional field shaping is worth the accompanying parasitic capacitance and extra fabrication steps.

## Scaling current

If a high-voltage unit cell is to be useful, it must be scaled to meaningful current delivery. Due to this, we fabricated multi-finger transistors using the same basic architecture. They include a representative device with 20 gate fingers, each 500 µm wide, that has a total gate periphery of 10 mm and a gate-drain spacing of 30 µm. Measured output characteristics show that, as expected, current increases with the number of fingers. Our 20-finger device delivers close to 3 A under pulsed operation, with scaling remaining close to that expected from smaller structures within the measured range.

Scaling is an important demonstration for sapphire. This platform has often been associated with small devices and moderate power levels, partly due to its




➤ Figure 4. Multi-finger design and output current-voltage characteristics demonstrating current scaling to ampere-level operation.

thermal reputation. While the realisation of ampere-level currents does not by itself solve thermal management, it verifies that it's possible to transfer the high-voltage epitaxial concept from small test structures to substantially wider transistors without suffering an electrical scaling penalty within the measured operating range.

## Dynamic questions

Static performance is only part of the story for GaN. If charge trapping takes place, this can raise the dynamic on-resistance after an off-state voltage stress, making a device that looks excellent on a conventional current-voltage curve a disappointment during switching.

Our first set of drain-current-transient measurements is encouraging, but must be interpreted carefully. After a 1 s trapping condition at a drain voltage of 20 V, the fall in measured current is only a few percent, and recovery is relatively rapid. So, we do not observe severe current collapse under our preliminary low-stress conditions.

What we are not claiming from these results is that we have dynamic stability under multi-kilovolt stress. High-voltage trapping remains a principal issue we must investigate and optimise. For us, that distinction is important: while a static 5.5 kV result is established, dynamic behaviour at comparable electric fields is still a next step.

## Beyond sapphire

The remaining challenge brings us back to the objection hounding sapphire from the outset: heat. If an active GaN stack delivers excellent electrical performance, does sapphire have to remain underneath it for the entire life of the device?

Not necessarily. One route we are exploring is to use sapphire for what it does well – supporting mature, cost-effective GaN epitaxy – before separating this substrate from the thin active stack, which would be bonded to a more thermally conductive host, such as bulk AlN or a SiC-based carrier. In that architecture the growth substrate and the foundation for the final device don't have to be the same material.

We are also considering a second, longer-term route, offering a more favourable thermal path: the direct growth of our optimised thin HEMT stack on an engineered substrate. This approach avoids a transfer step, but places more stringent demands on epitaxial compatibility and material quality.

Both our solutions offer new ways to think about the substrate problem. Rather than searching for one material that simultaneously provides low cost, mature epitaxy, excellent electrical isolation and exceptional thermal conductivity, we are backing heterogeneous integration, which allows those functions to be separated.

Ultimately, this message may be the most important implication of our GaN-on-sapphire results. We are not advocating that sapphire should underpin every GaN power substrate, and our present devices do not remove the need for high-voltage dynamic and thermal validation. But they do show that sapphire can support a remarkably strong electrical platform, so long as the epitaxial stack is designed around its properties, rather than despite them.

Based on our encouraging results – a blocking voltage of 5.5 kV, a Baliga figure of merit exceeding 2 GW cm$^{-2}$, current scaling close to 3 A, and a simple field-plate-free architecture – the case for revisiting GaN-on-sapphire is stronger than ever.

What's needed next is to preserve those advantages while engineering away the remaining thermal and dynamic constraints. If there's success on this front, there is a strong case to be made that the mature substrate that helped establish the GaN LED industry should find a second major role, serving in the high-voltage power electronics industry.

## FURTHER READING

➤ A. Bidaud *et al.* "Record $R_{ON}$-BV Trade-Off and Scalable Heterogeneous Integration in Field-Plate-Free GaN-on-Sapphire HEMTs" CS MANTECH (2026)

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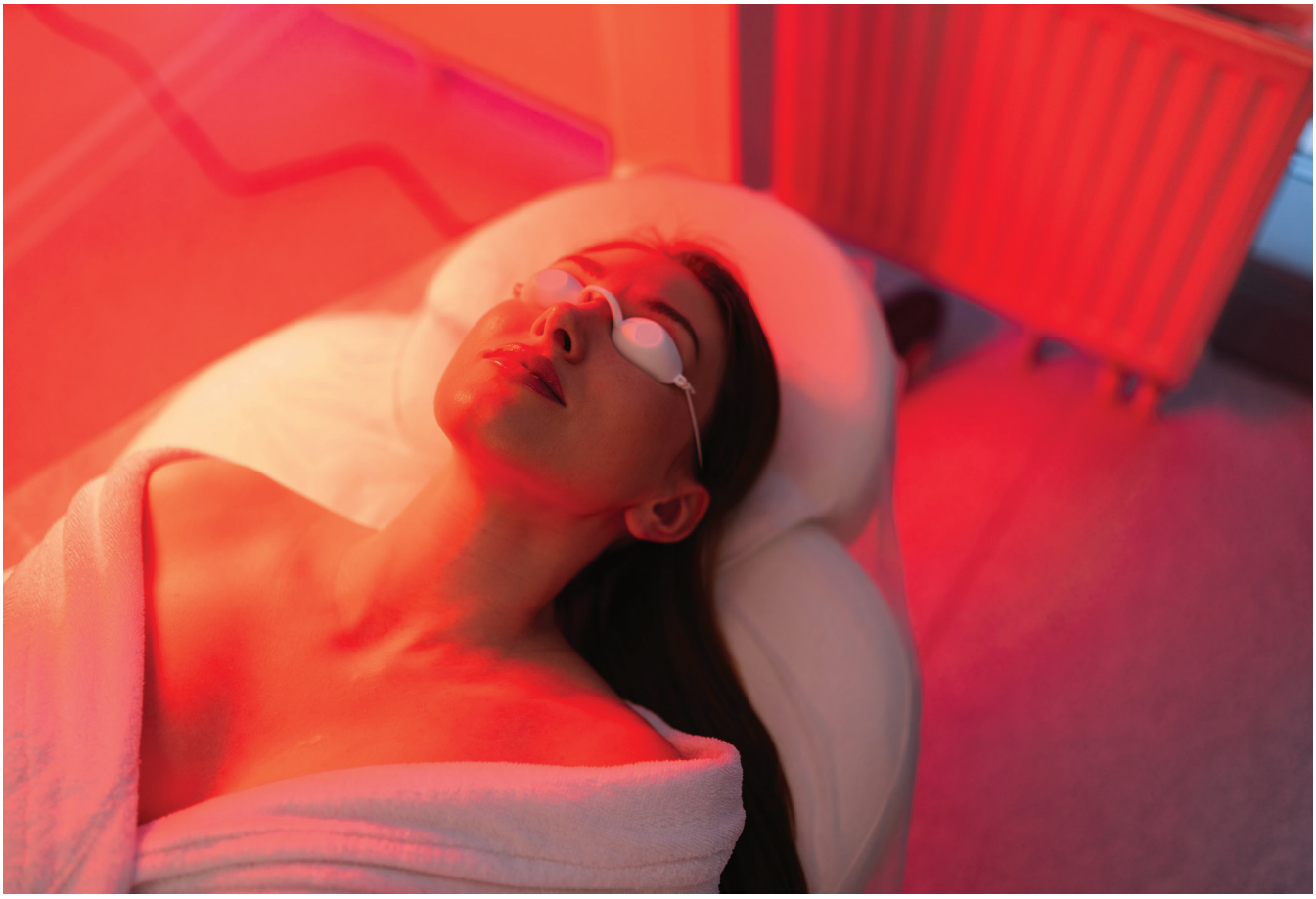
# Flexible microLEDs without compromise

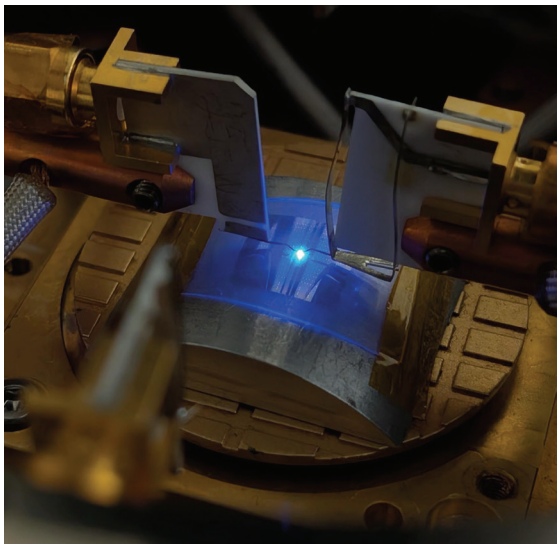
Photonic die transfer preserves the performance of InGaN microLEDs while enabling flexible devices to deliver brighter and more efficient light output

**BY PRANAV GAVIRNENI AND WILLIAM WONG FROM THE UNIVERSITY OF WATERLOO AND HARRY CHOU AND VIKRAM TURKANI FROM PULSEFORGE**

MEDICAL PROFESSIONALS use numerous treatments to help their patients, including quite a few that involve light. There's photodynamic therapy, using light to activate medicines that kill abnormal, pre-cancerous, or cancerous cells; UV phototherapy, which helps clear up stubborn skin conditions, such as psoriasis, eczema, and vitiligo; and red-light therapy, a treatment for improving blood flow, reducing joint pain, and easing inflammation.

When light plays a role in a patient's treatment, it's ideally applied directly to a specific area. And promising to do just that with exceptional efficacy are flexible biomedical systems, which can deliver a new level of control over how light interacts with the human body. Such systems could be based on conformal devices, which wrap onto soft tissue to deliver highly localised optical stimulation, enabling functions not possible with rigid platforms. However, realising this capability requires more than just mechanical flexibility – it demands light sources that remain efficient, stable, and precisely controlled while operating on deformable surfaces.





➤ Figure 1. A microLED emitting blue light during operation, illustrating the high brightness and small size that enable dense arrays with fine spatial control.

Meeting these performance demands are microLEDs. They have a high brightness, fast response, and micron-scale dimensions, making them well suited to dense arrays, where they deliver light with high spatial resolution (see Figure 1). It's a combination of attributes that's essential for applications where optical output must be confined and controlled within a small form factor, such as wearable and implantable systems.

Unfortunately, when microLEDs are considered for these applications, they are held back by a constraint that is difficult to overcome. This affliction plagues the most common form of microLED, which is made from InGaN and related materials, and relies on growth and processing conditions that demand rigid crystalline substrates, such as sapphire. While such substrates provide the materials quality that's required for efficient emission, they fix the device in a form that cannot bend or conform. Note, though, that it's not possible to turn to flexible polymeric substrates that offer mechanical compliance, because they are incompatible with the fabrication processes needed to produce high-quality emitters. So, the crux of the matter is a fundamental mismatch: the platform delivering performance fails to enable functionality.

To overcome this limitation requires a radical re-think, regarding how microLED systems are assembled. It's an issue we've been exploring at the University of Waterloo and PulseForge, with success coming from a pioneering process that separates device fabrication and system integration.

Our process begins with the optimisation of the microLED on its native substrate. These emitters are then transferred to a flexible platform using a two-step process that preserves electrical and optical performance (see Figure 2). Crucially, this approach exposes the device's backside, enabling control over light extraction beyond the constraints of the growth wafer.

## A rigid foundation

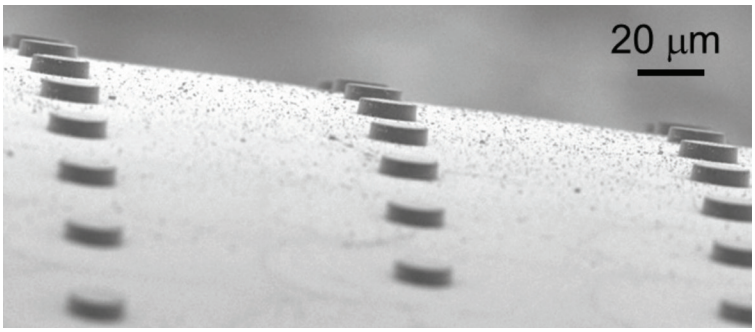
When combining different materials systems in a single device, the challenge is not just a matter of bringing disparate entities together; integration forces a tradeoff.

One option is to keep materials separate, and connect them only through wire bonds, or by mounting side-by-side on a circuit board. The merit of this approach is that it preserves material quality, as each device is fabricated on its ideal substrate. But there is a downside – a limitation on how tightly the systems can interact.

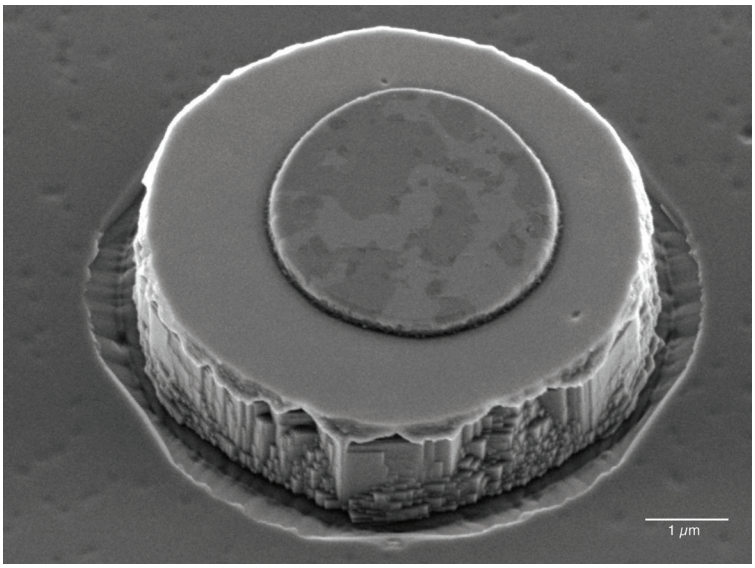
At the other extreme is the integration of materials directly at the device level. However, while this enables functions and scaling outside the realm of what's possible with conventional interconnects, this level of integration comes with strict constraints: the materials must be chemically, thermally, and mechanically compatible. Break these non-negotiables and defects emerge, performance degrades, and the advantages of integration vanish.

The trade-off is particularly severe for III-nitride microLEDs. Production of high-performance InGaN devices demands growth and processing under conditions that require rigid, crystalline substrates, such as sapphire. These substrates are great at providing the thermal stability and structural quality needed for efficient light emission. That's not the case with flexible materials, which cannot support the temperatures or processes needed to build high-quality devices, but have the form required for conformal systems. So, the rub is that the platform that delivers performance is not the platform that enables flexibility.

Our approach, which separates these roles, is conceptually simple. However, it's difficult to execute, because unlike packaged chips, microLEDs at the same stage are exposed and fragile. This issue arises because shrinking device dimensions to the micron scale leads to an increase in sensitivity to mechanical stress, thermal exposure, and process variation (see Figure 3). Note that techniques that are effective for larger devices, such as conventional




➤ Figure 2. Scanning electron microscope image of microLED arrays on a flexible substrate after 2-part transfer process.




➤ Figure 3. Scanning electron microscope image of a 6 μm microLED before transfer.

pick-and-place assembly, do not readily scale to dense arrays of micronscale emitters.

So, the obstacles we have faced are not limited to figuring out how to simply move devices from one surface to another. While doing so, it's imperative that we retain the performance that's realised on the native wafer, while integrating devices onto a new platform that enables additional functionality. Our two-step process, fulfilling those objectives, is summarised in Figure 4.

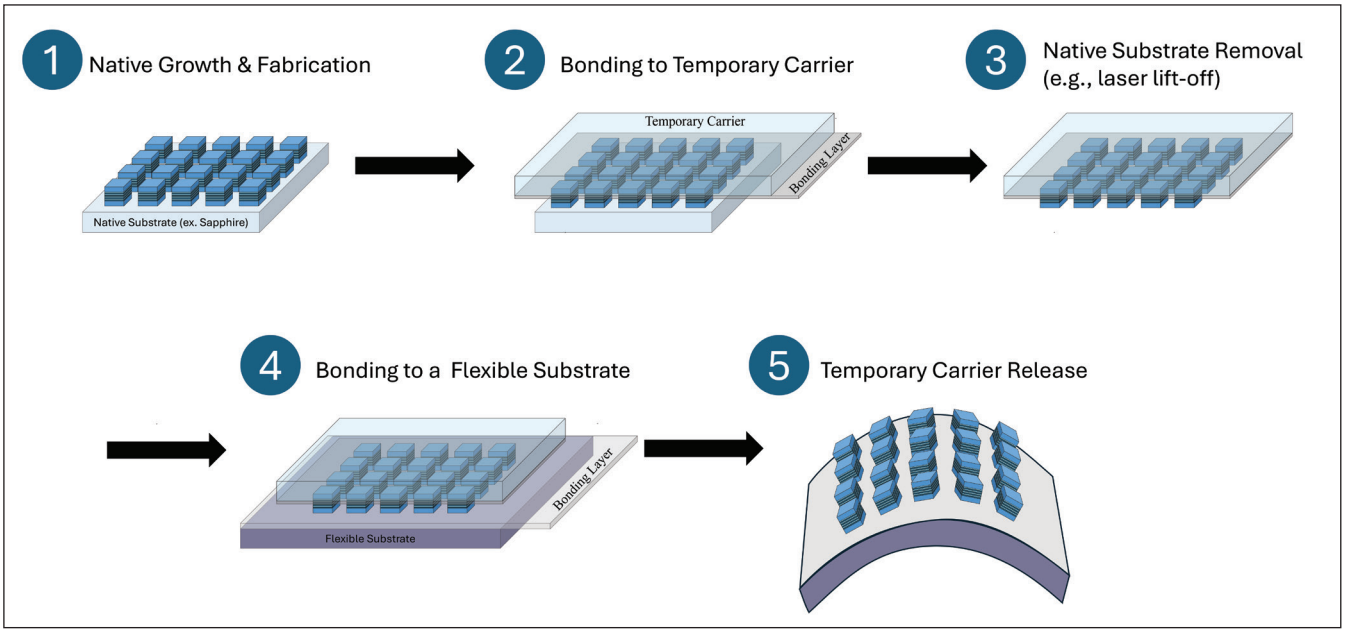
## Photonic die transfer

A key part of our process involves separating where the device is made from where it is used. This step, introduced only at the final stage – it's after the devices have been fully defined – ensures retention of established fabrication processes.

The release of microLEDs from their native substrate is undertaken with laser lift-off. This is a well-established technique in III-nitride processing, used to remove sapphire while preserving device integrity. During this step, we transfer devices onto a temporary carrier, which enables subsequent handling and processing.

Where the biggest challenge lies is in the detaching of devices from their growth wafer, and their subsequent transfer to a flexible substrate, a move that must be made without degrading performance. For micron-scale emitters arranged in dense arrays, this is far from straightforward. Flexible polymeric substrates are unable to withstand large mechanical forces, prolonged heating, or aggressive chemical processing. This rules out common microLED transfer techniques, such as laser, thermal, mechanical, and elastomer-based methods, as they involve stress, non-uniform separation, or excessive thermal exposure. These effects hamper performance by increasing leakage current, degrading contacts and reducing emission uniformity. Ultimately, there's a lowering of the yield of functional devices.

We overcome these limitations with a form of photonic die transfer. Based on PulseForge technology, our approach allows the transfer of devices from the carrier onto the flexible substrate. Rather than relying on mechanical separation or bulk heating, we direct short broadband light pulses through a transparent carrier to an engineered bond interface (this is illustrated in Figure 5). Optical




➤ Figure 4. MicroLEDs are first grown and fabricated on a rigid native substrate, such as sapphire, to support high-temperature III-nitride processing. Completed devices are then bonded to a temporary carrier, to allow the removal of the native growth substrate. After backside access and optional optical engineering, the microLEDs are bonded to a thin flexible polymeric substrate. A final photonic die transfer step separates the temporary carrier, leaving intact high-performance microLEDs on a mechanically flexible platform.

energy is converted into highly localised heat through an embedded absorbing layer, leading to separation precisely at the interface. Thanks to confinement of energy at the bond layer, we minimise mechanical shock and limit thermal exposure to the microLEDs.

Our localised, interface-driven release distinguishes our photonic die transfer technology from conventional transfer methods. We avoid mechanical and peel-based techniques, which apply stress across the entire device and increase the risk of fracture in micron-scale emitters; and we also steer clear of thermal release methods, which heat the entire stack – this is potentially damaging to temperature-sensitive materials, limiting compatibility with polymeric substrates, and increasing overall processing time. Instead, thanks to the technology developed at PulseForge, we selectively deliver energy only where separation is required, enabling rapid, non-contact transfer while preserving device integrity. Our process can be scaled across large areas, by stepping the light source (see Figure 6). This supports parallel transfer of dense microLED arrays, as we don't have to handle devices one at a time.

An additional advantage with our approach is the opportunity to reuse the temporary carrier. As the separation occurs at the bond interface, and leaves the carrier largely unaffected, this can be recovered and re-used in subsequent cycles with minimal rework. Benefits are a trimming of materials consumption, a significant reduction to process cost, and an addressing of the sustainability challenge in advanced semiconductor manufacturing.

With conventional transfer approaches, these benefits are realised rarely. Often sacrificial layers or carrier substrates are discarded after a single use, contributing to materials waste and an increased processing overhead.

## Design after growth

Our photonic die transfer process does more than move microLEDs onto a flexible substrate. It also removes a key limitation that is built into devices on their native wafer: a significant fraction of the generated light never escapes.



➤ Figure 5. PulseForge assisted photonic die transfer uses short broadband light pulses to expose the carrier light-absorbing layer, driving rapid heating and carrier release without direct mechanical stress to the microLEDs. The process supports large-area operation and allows the temporary carrier to be recovered for reuse.

On sapphire, photons emitted in the active region are partly guided into the substrate, where they are lost, either through trapping or absorption. These optical losses are set by the growth geometry and cannot be addressed after fabrication. Removing sapphire eliminates this constraint and exposes the GaN backside, as shown in Figure 2, to create a new optical boundary that can be engineered before final integration.

This matters because microLED efficiency is not determined solely by photon generation. It also depends on how effectively photons exit the device. When the backside is accessible, the optical environment can be modified during the transfer sequence, rather than being fixed by the growth wafer.

The immediate benefit is a reduced substrate-guided loss, allowing more light to escape for the same electrical input. Ultimately, there's an increase in effective brightness.

Further gains could be realised by introducing a reflective layer or textured surface on the exposed device backside prior to bonding to the flexible substrate. This layer would redirect photons otherwise propagating away from the emission surface, returning them toward the viewer. In this way, light previously




➤ Figure 6. The PulseForge transfer system enables large-area processing by stepping the light source across the substrate, supporting the parallel transfer of dense microLED arrays. The process supports large-area operation and allows the temporary carrier to be recovered for reuse.

An additional advantage with our approach is the opportunity to reuse the temporary carrier. As the separation occurs at the bond interface, and leaves the carrier largely unaffected, this can be recovered and re-used in subsequent cycles with minimal rework.

lost into the substrate would be partially recovered, increasing the usable output without altering the diode structure itself.

This shift changes the role of transfer. On the native wafer, optical losses are largely fixed once growth is complete. But after substrate removal, they become adjustable. So, the same step that enables mechanical flexibility also creates an opportunity to improve light extraction, provided the device and its optical surroundings are considered together.

To determine whether this added flexibility comes at the expense of device integrity, we have compared performance before and after integration. We initially characterised microLEDs on sapphire, to establish baseline electrical and optical behaviour, prior to transfer and release onto the flexible platform using photonic die transfer. Any degradation would appear as increased leakage current, a shift in emission spectra, or a reduced efficiency. But we find that devices retain their electrical and spectral characteristics while benefiting from the modified optical environment, confirming that transfer preserves device quality while enhancing light extraction.

## Preserved quality

By separating fabrication from integration, we have introduced a potential pitfall: Could the transfer process degrade the device?

MicroLEDs are sensitive to defects, contact damage, and thermal and mechanical stress – and all have an immediate impact on the electrical response. If there's an increase in leakage current, this indicates defect formation in the junction, while changes in forward bias behaviour point to contact degradation or increased series resistance. There might also be a small uptick in turn-on voltage, raising power consumption and reducing operating efficiency.

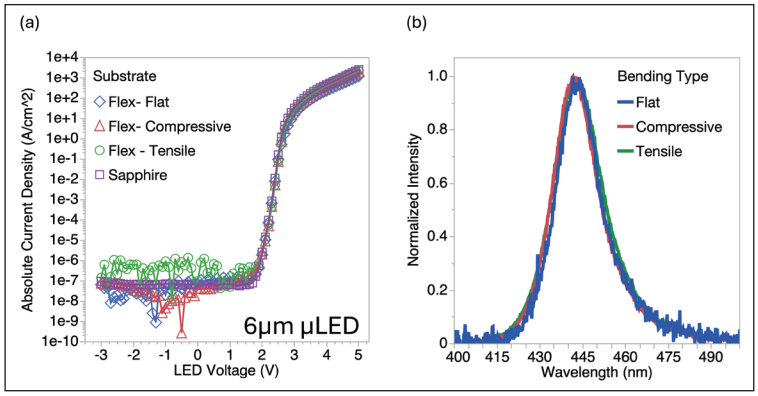
Due to these concerns, we measure our device performance before and after transfer. By scrutinising current-voltage characteristics, emission spectra, and efficiency, we obtain a direct comparison of device integrity through the process (see Figure 7).

With our approach, the electrical response does not change. Our microLEDs-on-sapphire exhibit a low leakage current and stable forward operation, consistent with high-quality junctions. Transfer to a flexible substrate preserves these characteristics, even for devices as small as 6 µm in diameter. Due to an absence of increased leakage, alongside no alterations to forward behaviour, we can deduce that our photonic die transfer steps do not introduce measurable electrical damage.

What's equally encouraging is that our optical response shows the same stability. Emission spectra remain unchanged after transfer, with no measurable shift in peak wavelength (see Figure 7 (b)). So we can conclude that the active region is unaffected by transfer, with recombination processes governing light generation remaining intact.

Another matter must be investigated with the introduction of mechanical flexibility: Does performance remain stable under deformation? We have found that under tensile and compressive bending, the emission profile shows negligible change. This stability is essential. Even small spectral shifts would limit the usefulness of microLEDs in biomedical systems (and also in displays and optical communication), due to the need for a consistent colour and wavelength during operation.

Based on our thorough examination, we conclude that our transfer process introduces no measurable electrical or optical penalty. Our microLEDs retain their behaviour on the native wafer after substrate removal, integration, and mechanical deformation. By preserving performance, if there is any change to brightness or efficiency, we attribute this to a change in the optical environment, rather than damage to the device.




➤ Figure 7. (a) Current voltage characteristics for 6 µm microLEDs show comparable behaviour on sapphire and after transfer to flexible substrates, including under flat, tensile, and compressive bending conditions. (b) Normalised electroluminescence spectra remain stable under bending, with only minor wavelength shifts and no measurable spectral broadening.

## Unlocked efficiency

A really important question to address is whether the performance of our microLEDs improves after they are removed from the growth substrate. Measurements reveal that efficiency increases. For 6 µm microLEDs, peak wall-plug efficiency rises from around 9 percent on sapphire to approximately 12 percent on the flexible substrate (see Figure 8). We have also studied devices with other dimensions, finding that peak efficiency improves by up to 1.5 times. This boost in efficiency is beneficial, as it reduces the power required to realise the same brightness.

It should be emphasised that this gain in efficiency is not driven by the diode. The electrical characteristics are unchanged, with emission spectra showing no measurable wavelength shift. Carrier injection and radiative recombination are also unaffected. What's behind the improvement is how the light is extracted.

The removal of sapphire eliminates a major loss pathway, allowing fewer photons to be trapped. In conjunction, exposing the GaN backside changes optical boundary conditions set by the growth wafer. For our microLEDs, this change alone increases the fraction of usable light. In future, we could investigate more advanced designs that build on this, using backside texturing or reflective layers to extract more photons that would otherwise be lost.

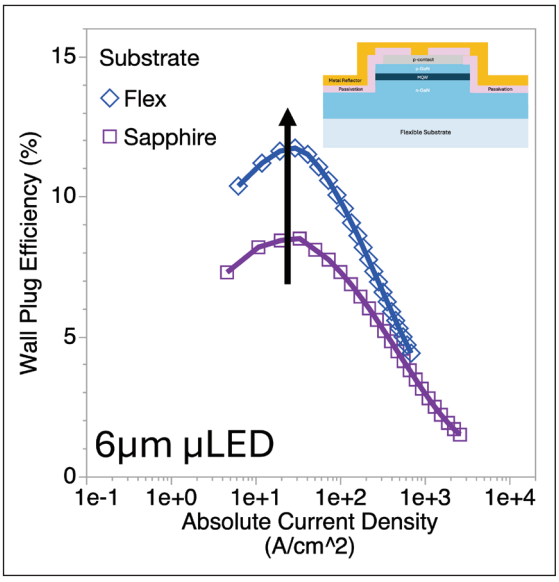
Separation is key. While growth defines how efficiently photons are generated, transfer determines how effectively they are delivered.

The gains in efficiency that come from separation are more pronounced as device dimensions shrink. For microLEDs below 10 µm, efficiency tends to decline, due to an increase in surface recombination. But if that's avoided, and efficiency is maintained while scaling, this enables higher pixel densities, finer spatial control, and lower power operation. They are significant benefits, as these characteristics are essential for wearable and implantable biomedical systems, where optical sources must deliver precise output on soft, moving surfaces without excessive heat.

## Beyond bending

Once the microLEDs are free from rigid substrates, they can be combined with platforms that match the mechanical and functional demands of the application. This includes new opportunities to control light extraction. As well as flexibility, there's the opportunity to use light more effectively. That's a particularly valuable combination in systems demanding precise optical delivery within a limited form factor, such as wearable and implantable biomedical platforms that must operate reliably on soft, moving surfaces.

While our success has focused on microLEDs, our approach is applicable to other forms of compound semiconductor devices that face the same constraint – that is, the substrate that enables optimal growth is not the one that best supports system-level operation. Transfer-based integration provides a way to resolve this mismatch, allowing devices to be fabricated under ideal conditions, before placing them where they deliver the greatest impact.



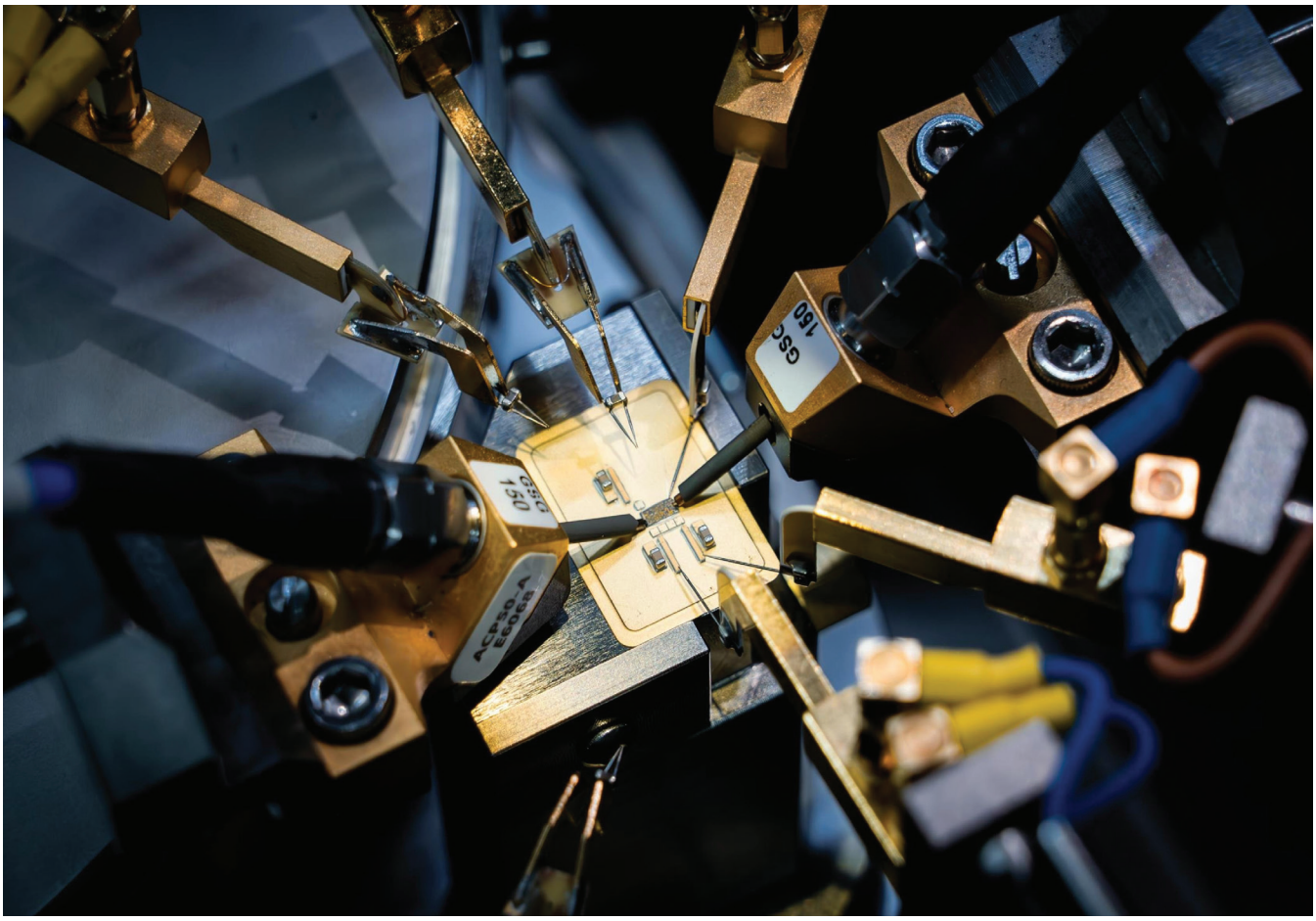

➤ Figure 8. Wall-plug efficiency as a function of absolute current density shows higher peak efficiency after transfer to the flexible substrate, consistent with increased light extraction.

This changes the role of transfer. It is no longer just a final packaging step, but part of device design. It's now possible to engineer electrical performance, optical behaviour, and mechanical function separately, prior to integration.

For biomedical systems, this enables a new class of compact, high-resolution optical platforms, where dense arrays of microLEDs deliver precise, stable light on conformal substrates with reduced power consumption. By building devices on wafers optimised for performance, prior to their assembly into systems that maintain that performance while operating directly on the body, our technology is bringing continuous, high-fidelity optical interaction into practical wearable and implantable systems.

## FURTHER READING


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# Unifying GaN RF and logic

A gold-free GaN-on-silicon platform that combines high-power RF devices with robust digital logic strengthens the foundations of tomorrow's mixed-signal circuits

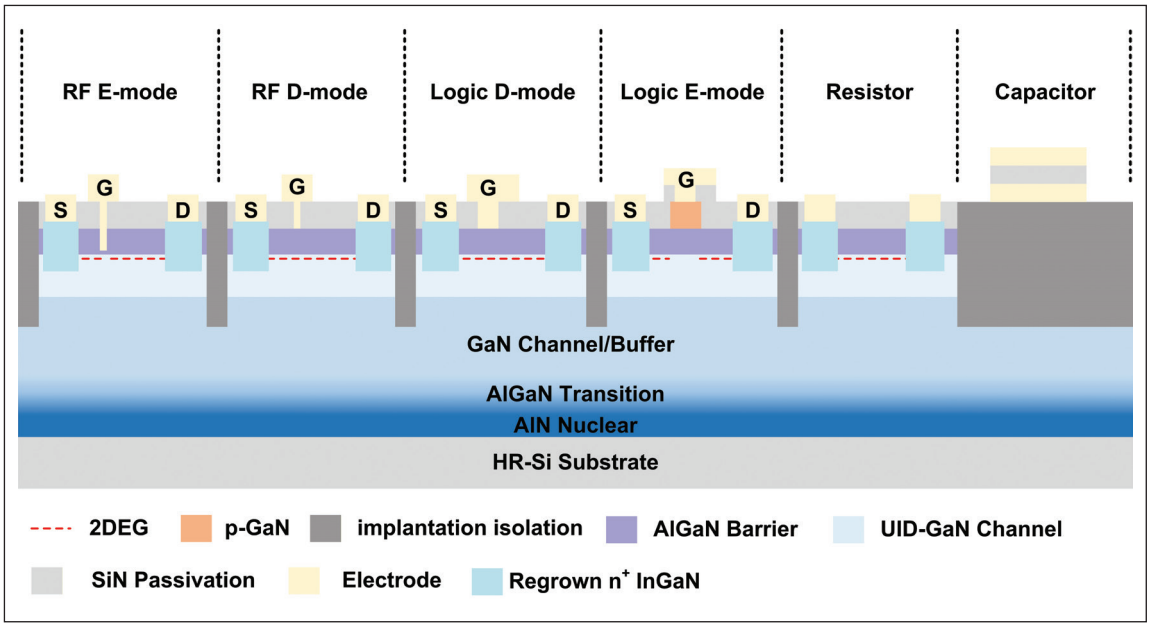
**BY BIN HOU, JIALE DU, HAO LU, LING YANG, XIAOHUA MA AND YUE HAO FROM XIDIAN UNIVERSITY**

TODAY'S wireless infrastructure is asked to do much more than simply amplify and transmit signals. In the latest communication systems – particularly those serving 5G networks, satellite links and adaptive RF front-ends – the core semiconductor platform has to support high-frequency and high-power operation, while providing precise control and reliable digital decision-making. This set of requirements has spurred the development of very large-scale integrated circuits in RF front-end modules, and placed more stringent demands on mixed-signal integrated circuits, which combine RF analogue functions with digital logic on a single chip.

GaN is well suited to tackling this demanding task, thanks to the high density of its two-dimensional electron-gas (2DEG), its high critical electric field and its high saturation velocity. These strengths, which can be realised in large-scale, low-cost, CMOS-compatible wafers, give GaN-on-silicon devices great potential to provide high microwave power, alongside high logic performance. The combination of high-performance enhancement-mode (E-mode) and depletion-mode (D-mode) GaN equips the monolithic GaN-on-silicon platform with an attractive route to realising compact, versatile, robust mixed-signal systems.

Unfortunately, it is far from straightforward to fulfil this promise. One issue impeding success is that conventional GaN RF technologies tend to rely on gold-containing metallisation, which creates compatibility concerns for large-scale integration with silicon-based process flows. And another problem is that many GaN-on-silicon platforms struggle to deliver a high RF power density, stable enhancement-mode operation and strong digital logic performance. Both weaknesses must be tackled if GaN is to move beyond discrete RF power devices and become a broader platform for integrated mixed-signal electronics.

Taking on this challenge is our team from Xidian University. We are developing a GaN-based monolithic integrated platform on 6-inch high-




➤ Figure 1. A GaN-based monolithic integrated platform for RF and digital logic applications on 6-inch high-resistivity silicon substrates with a gold-free metal structure.

resistivity silicon. Our approach employs a gold-free metal process, and integrates E-mode and D-mode GaN devices for both RF and logic applications.

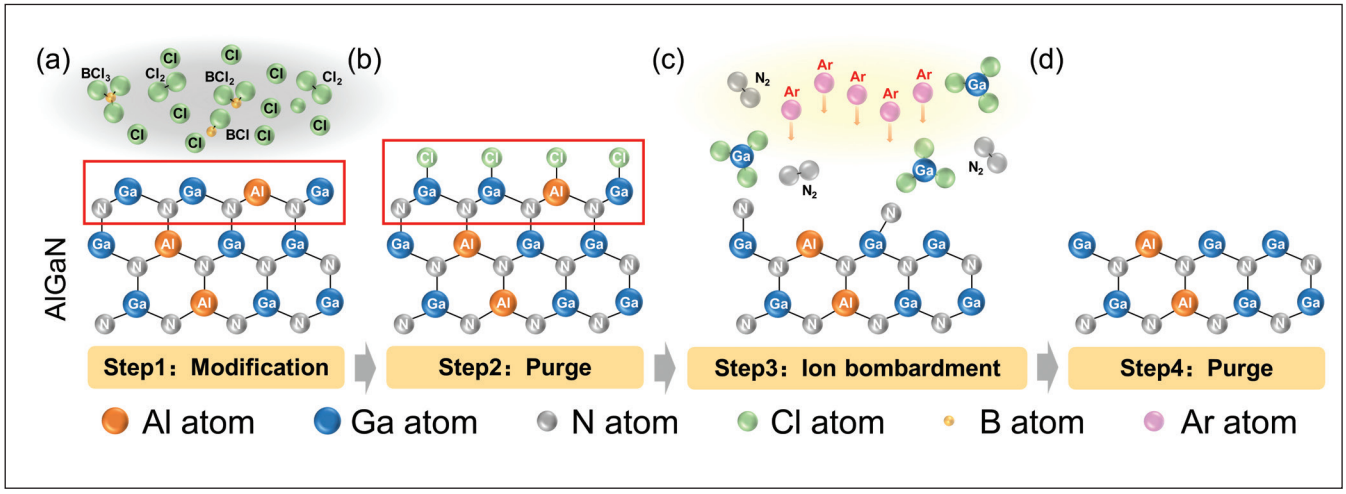
## Shared foundations

Underpinning our technology is a III-N epitaxial structure, formed on a 6-inch high-resistivity silicon substrate. Its growth begins with an AlN nucleation layer, followed by a step-graded AlGaN transition layer, a GaN buffer, an unintentionally doped GaN channel, an AlGaN barrier and a *p*-GaN cap. We include a step-graded transition layer, as this helps to address the lattice mismatch between GaN and silicon. Its inclusion supports the growth of a high-quality buffer and channel.

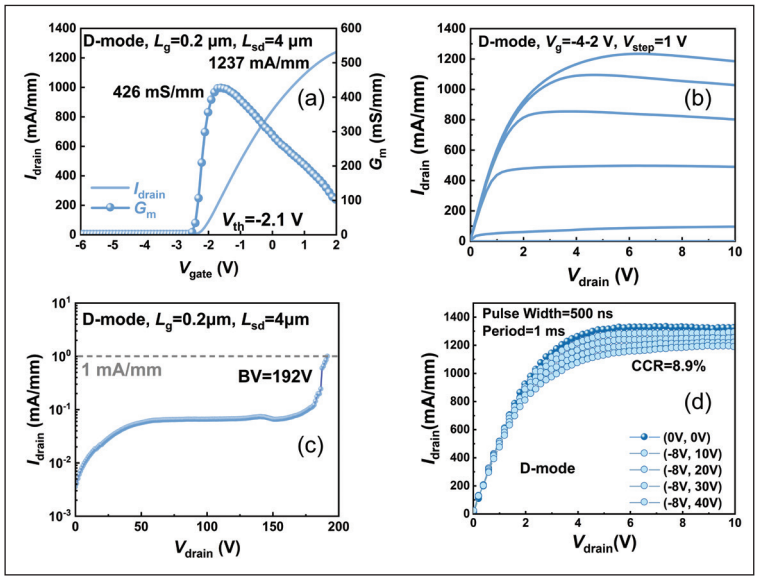
Our high-quality epitaxial platform enables the co-fabrication of RF and logic modules on a single wafer. In the RF section, we fabricate D-mode and E-mode devices with a gate length of 0.2 µm, a gate width of 100 µm, and a source-to-drain spacing of 4 µm. In the logic section, we deploy E/D-mode devices with longer gate dimensions – gate length is 1 µm – and widths tailored for logic operation. Here, the source-to-drain spacing is 6 µm. Resistors and capacitors are integrated in the logic part, enabling functional circuits rather than isolated transistors (see Figure 1).

A key requirement for our platform is that it employs a gold-free process – this is crucial for compatibility with CMOS manufacturing flows. However, replacing conventional metallisation must not come at the expense of RF performance, so we have countered the threat of significant thermal and parasitic loss, introduced during a high-temperature alloy annealing process.

We avoid this pitfall by introducing a Ti/Al/Pt/Ti ohmic stack, together with an $n^+$ InGaN regrowth after ohmic recess etching. With this approach, we ensure a direct contact to the two-dimensional



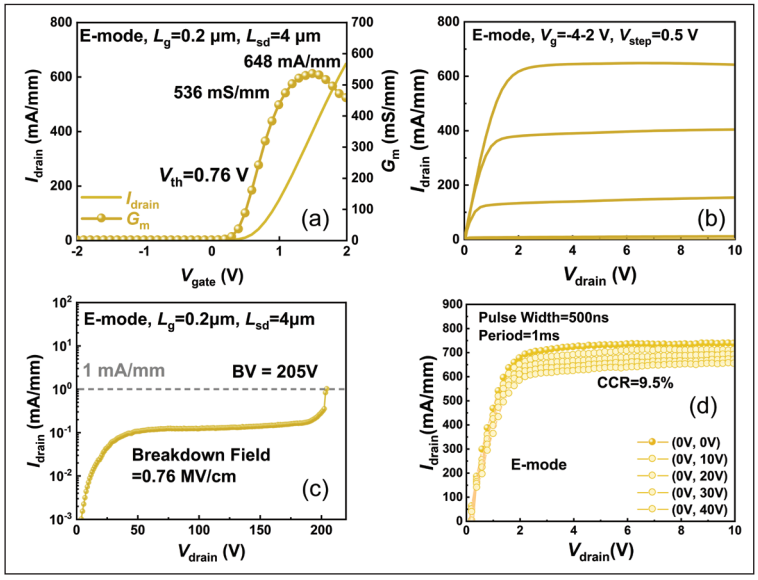

➤ Figure 2. Mechanism schematics of the atomic layer etching process for RF/logic applications. (a) $BCl_3/Cl_2$ chemical modifications upon the surface of an atomic (Al)GaN layer, (b) purge process for the removal of residual $BCl_3/Cl_2$ radical, (c) argon ion bombardment, (d) purge process for the removal of the atomic chlorinated layer.




➤ Figure 3. DC characteristics of the D-mode GaN devices for RF applications with a gate length, $L_g$, of 0.2 μm, and a source-to-drain distance, $L_{sd}$, of 4 μm. (a) transfer curves, (b) output characteristics, (c) off-state breakdown properties and (d) double pulsed current-voltage (I-V) test.

electron gas, leading to an ultra-low ohmic contact resistance of 0.058 Ω mm. Note that there is also strong wafer-level uniformity across the 6-inch substrate.

A crucial benefit of the very low contact resistance is that it reduces access resistance, unlocking a high current drive for RF applications. This low resistance aids integrated circuits, contributing to lower loss and more stable operation. Just as importantly, an impressive performance is achieved without gold, allowing our platform to retain its compatibility




➤ Figure 4. DC characteristics of the E-mode GaN devices for RF applications with a gate length, $L_g$, of 0.2 μm, and a source-to-drain distance, $L_{sd}$, of 4 μm. (a) transfer curves, (b) output characteristics, (c) off-state breakdown properties and (d) double pulsed I-V test.

advantage while supporting demanding RF operation.

## E-mode RF GaN devices

The fabrication of E-mode GaN RF devices demands careful gate engineering. To shift the threshold voltage into the positive domain – the essence of E-mode operation – the AlGaN barrier beneath the gate must be recessed with extremely high precision, while producing a smooth surface. If the recess is too shallow, the device might fail to provide reliable E-mode operation; and if it is too deep or too damaging, carrier transport will be impaired, with RF performance suffering.

To walk this tightrope, we turn to atomic layer etching for the gate recess. This form of etching, involving sequential surface modification and ion-assisted removal to provide precise control of the etching depth, limits plasma-induced damage (see Figure 2). For our E-mode RF devices, we use atomic layer etching to define a precisely controlled 4 nm-thick AlGaN barrier beneath the gate. Microscopy confirms the integrity of our recessed region and the smoothness of the remaining AlGaN surface.

Measurements on our 0.2 μm D-mode RF devices reveal a threshold voltage of -2.1 V, a drain current of 1237 mA $mm^{-1}$, and a transconductance of 426 mS $mm^{-1}$. For their E-mode cousins, there's a positive threshold voltage of 0.76 V, a drain current of 648 mA $mm^{-1}$ and an even higher transconductance – it's 536 mS $mm^{-1}$. Based on these numbers, we conclude that introducing the E-mode gate recess does not sacrifice the high carrier transport needed for RF operation.

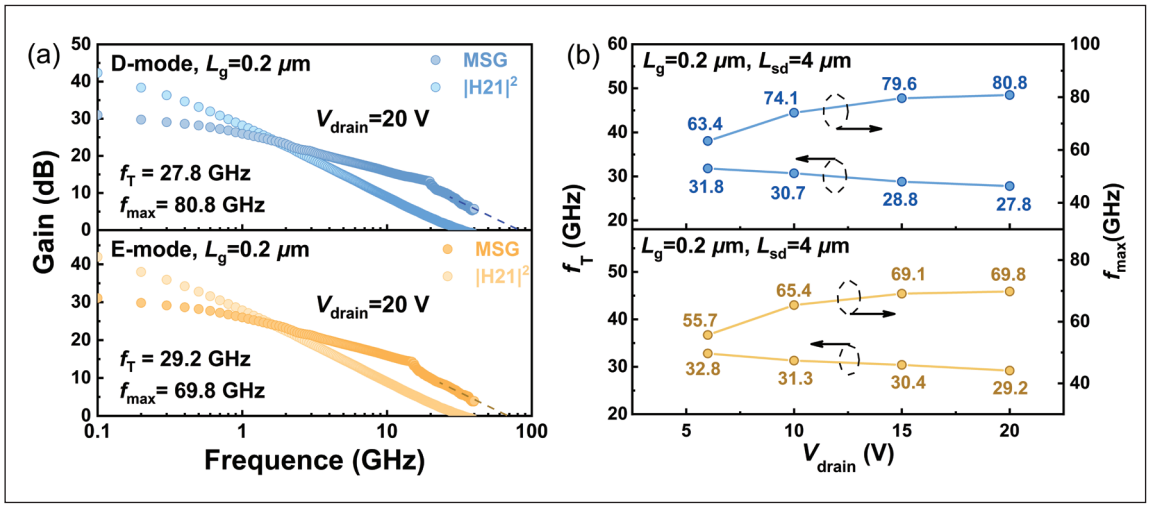
Our devices also exhibit a decent high-voltage capability. D-mode and E-mode RF devices deliver breakdown voltages of 192 V and 205 V, respectively. These are very respectable values, considering a source-to-drain spacing of 4 μm. This breakdown performance is much valued, providing the headroom needed for high-voltage RF power operation.

Another encouraging set of results come from pulsed measurements, which determine current-collapse ratios of 8.9 percent and 9.5 percent for D-mode and E-mode devices, respectively. These values indicate that trapping-related degradation is well relieved (see Figure 3 and Figure 4).

## High-power RF characteristics

We have confirmed the RF potential of our platform with small-signal and large-signal measurements. Operating at a drain voltage of 20 V, our E-mode device has a cut off-frequency, $f_T$, of 27.8 GHz, and a maximum oscillation frequency, $f_{max}$, of 80.8 GHz. For our D-mode device, $f_T$ is 29.2 GHz and $f_{max}$ 69.8 GHz (see Figure 5).

Large-signal load-pull measurements at 3.6 GHz reveal the most significant advance. Operating with




➤ Figure 5. (a) Small signal performances of both E/D-mode RF devices with a gate length, $L_g$, of 0.2 μm and a source-to-drain distance, $L_{sd}$, of 4 μm. (b) Cut off-frequency, $f_T$, and a maximum oscillation frequency, $f_{max}$, as a function of drain voltage for both E/D-mode RF devices.

a drain voltage of 45 V, our D-mode device delivers a saturated output power density of 11.0 W mm$^{-1}$ and an associated power-added efficiency (PAE) of 51.21 percent. Under the same operating voltage, our E-mode device produces a saturated output power density of 5.74 W mm$^{-1}$ at a PAE of 44.92 percent (see Figure 6).

We conclude from these figures that our gold-free GaN-on-silicon devices support microwave-frequency operation while retaining the integration advantages of the silicon substrate.

One of the drawbacks of E-mode RF GaN devices is that they often face a difficult balance between delivering a high threshold voltage, a high current drive and a high RF power. Our results show that we ease this compromise through the combination of atomic layer etching, combined with high-quality epitaxy and the deployment of low-resistance gold-free ohmic contacts. Our E-mode device maintains a positive-threshold operation while delivering an RF power performance suitable for high-power applications.

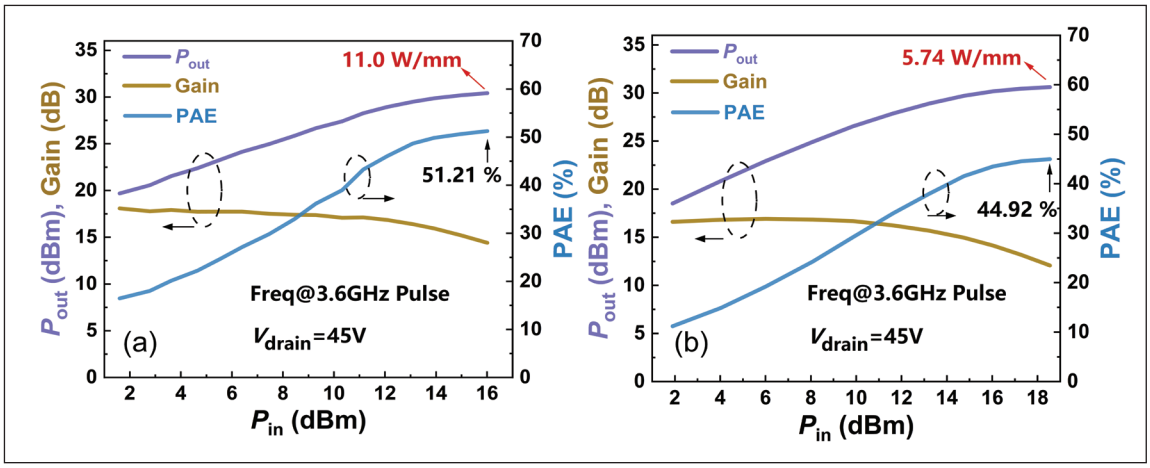
Its counterpart, our D-mode device, delivers 11.0 W mm$^{-1}$ at 3.6 GHz, highlighting its ability to play a key role in a shared platform supporting demanding RF amplification. We infer from the linear increase in output power with drain voltage of up to 45 V that there's a stable safe-operating region, which is vital for practical RF power modules. Taken together, our D-mode and E-mode results show that our monolithic platform can accommodate both high-power RF amplification and normally-off device operation.

## Logic-RF integration

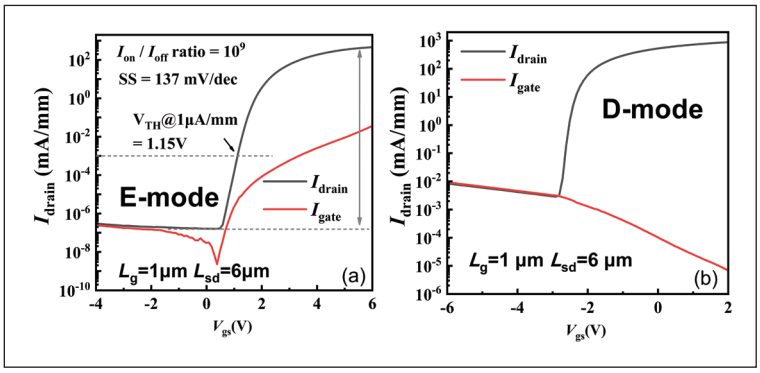
For future mixed-signal GaN systems, a high RF output power alone is insufficient. Also needed is digital logic, used to provide control, protection, switching, signal conditioning and adaptive operation. For this reason, our platform incorporates *p*-GaN E/D-mode logic devices and circuits.

Our E-mode devices for logic applications have a threshold voltage of 1.15 V and an off-state current of just 2.7 × 10$^{-7}$ mA mm$^{-1}$. These attributes ensure robust operation of digital logic, which demands well-defined switching thresholds and a low static leakage. Through interconnection of D-mode and E-mode GaN HEMTs, we have realised integrated GaN inverters on the same monolithic platform (see Figure 7).

When operating under a supply voltage of 5 V, our inverters exhibit excellent voltage transfer behaviour. High and low noise margins are 2.43 V and 2.19 V,




➤ Figure 6. Load-pull characteristics of 0.2 μm RF devices at 3.6 GHz of (a) D-mode and (b) E-mode GaN HEMT at a drain voltage ($V_{drain}$) of 45 V.




➤ Figure 7. DC characteristics of (a) E-mode and (b) D-mode GaN devices for logic applications with gate length of 1 μm and a source-to-drain distance of 6 μm, respectively.

respectively, indicating that the operating window is balanced and robust. Output swing relative to supply voltage is close to the theoretical maximum, indicating strong signal integrity and efficient use of the available voltage range (see Figure 8).

Building on this success, we have gone on to demonstrate more complex logic functionality. This has included the construction of inverter, NAND and NOR circuits, implemented on the monolithic platform and tested under continuous switching operation. These circuits, operating at driving frequencies from 100 kHz to 1 MHz, show that our platform supports a diverse and useful set of digital building blocks. Thanks to this logic capability, we are revolutionising the role of GaN-on-silicon technology, moving it from simply a power-transistor platform to one that's an integrated RF and digital-control platform (see Figure 9).

## Mixed-signal promise

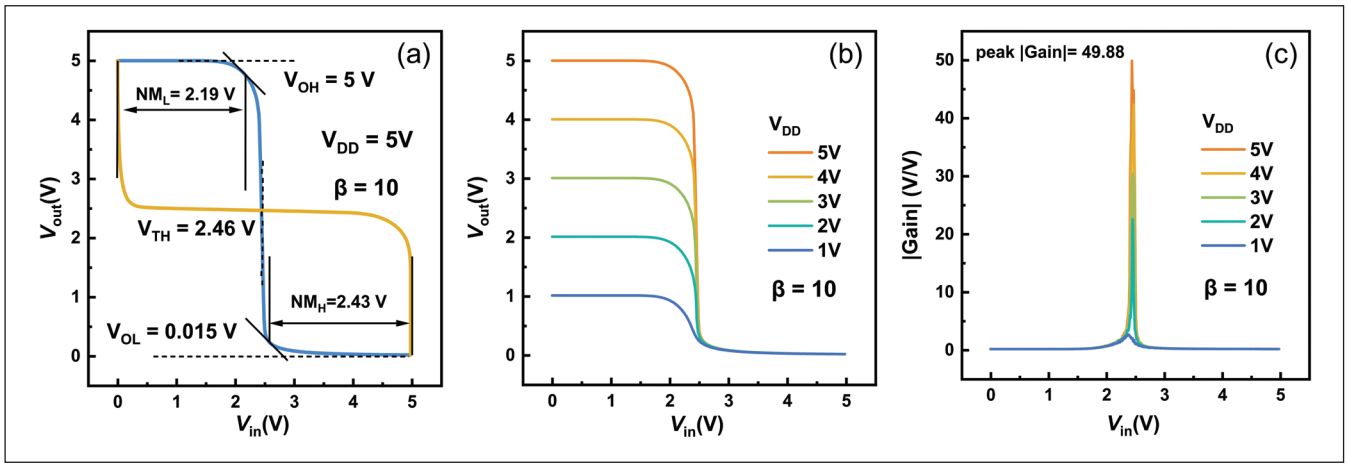
Combining RF and digital logic functions on the same GaN-on-silicon wafer opens a compelling path for future mixed-signal circuits. That's valuable, as in practical systems, RF power devices rarely operate in isolation. Instead, they require biasing, switching, monitoring and protection circuitry. If these functions are implemented using separate chips or incompatible process technologies, system complexity increases and parasitics limit performance.

A monolithic GaN platform offers a more elegant approach. It allows RF amplification, logic control and passive elements to be integrated more closely, trimming interconnect length and enabling more compact circuit architectures. Our foundation, high-resistivity silicon, supports this move to more sophisticated RF operation; and the 6-inch wafer format provides a pathway to scalable manufacturing.

Our platform has a number of valued assets: an ultra-low ohmic contact resistance, a high RF current drive, a high breakdown voltage, a low current collapse, a high output power density and robust logic noise margins. Working in unison, these attributes directly address the long-standing gap between high-performance GaN RF devices and integrated GaN digital logic.

Crucially, our results also point towards more adaptive RF systems. In next-generation wireless and satellite communication hardware, power amplifiers may need to respond dynamically to changing signal environments, modulation formats and operating conditions. By integrating digital logic alongside RF power devices, our technology promises to support smarter bias control, protection functions and reconfigurable operation. These capabilities are only going to increase in importance, given two big trends within communication systems are higher powers and greater intelligence.

Our next step is to extend our platform, moving on from demonstrating devices and logic gates to the targeting of more complex mixed-signal circuits. Success hinges on further optimisation of layout, thermal management, circuit architecture and reliability under RF operating conditions. Fortunately, the essential building blocks for such endeavours are in place, as we are able to realise E-mode




➤ Figure 8. (a) The voltage transfer curves and calculated noise margin of the GaN inverter working at a $V_{DD}$ of 5 V. The width of the gate, $W_g$, for E/D mode devices are 80 μm/8 μm. (b) The $V_{in}$–$V_{out}$ transfer characteristics with different $V_{DD}$ values and (c) the voltage gain.

and D-mode RF devices, *p*-GaN logic transistors, inverters, NAND and NOR gates, resistors and capacitors on the same gold-free GaN-on-silicon platform.

By unifying high-power RF performance with digital logic capability, our gold-free monolithic GaN platform provides a promising foundation for next-generation mixed-signal electronics. It strengthens the case for GaN-on-silicon as a scalable, versatile, integration-friendly technology for future RF front-ends, communication systems and intelligent power-amplifier modules.

## FURTHER READING


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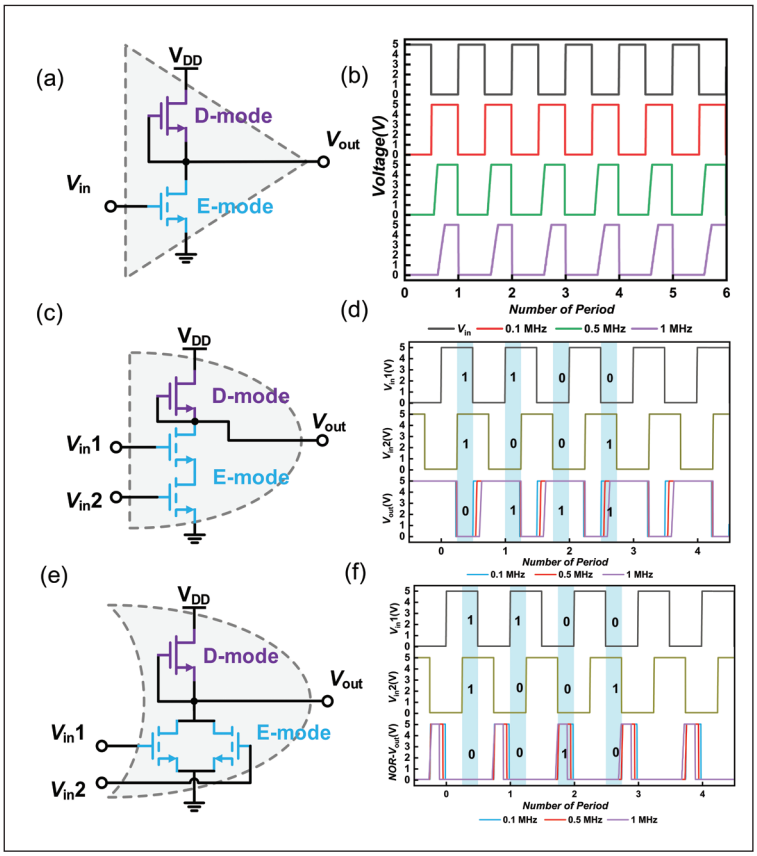




Figure 9. Logic circuits and results in the monolithic integrated platform. (a), (c), (e) Schematics of circuit diagrams for inverter, NAND and NOR circuits. (b), (d), (f) Waveforms under continuous switching operation for inverter, NAND and NOR circuits with driving frequencies varied from 100 kHz to 1 MHz.



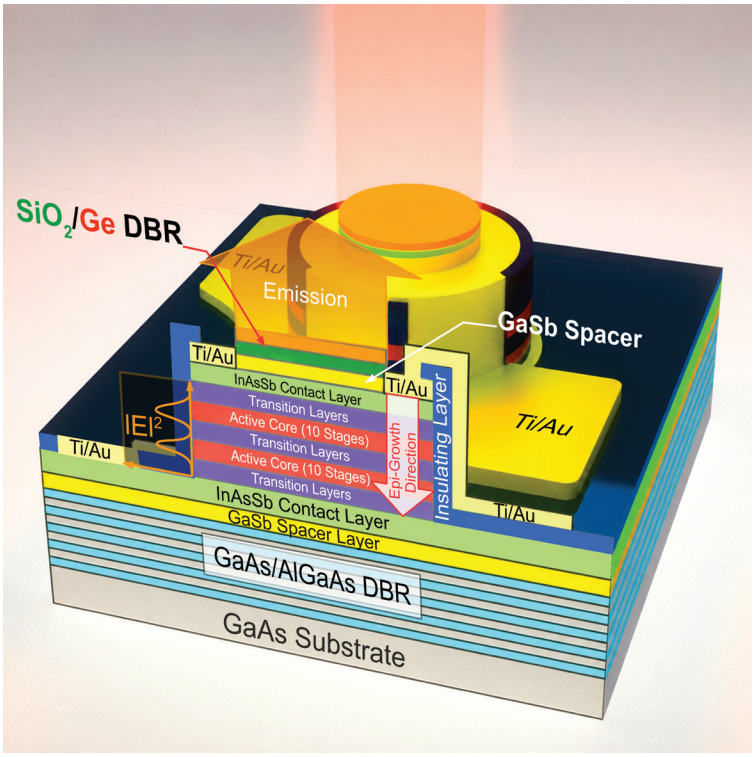

# Record-breaking mid-wave infrared LEDs

Adding a resonant cavity to mid-wave infrared LEDs featuring an interband cascade structure results in record spectral intensities, valued for chemical sensing and infrared scene projection

**BY JEREMY MASSENGALE, CHUL SOO KIM, CHADWICK CANEDY, IGOR VURGAFTMAN AND JERRY MEYER FROM THE U.S. NAVAL RESEARCH LABORATORY, ALONG WITH MIJIN KIM FROM AMENTUM AND COLIN IVERSEN AND VIJAYSEKHAR JAYARAMAN FROM PRAEVIUM RESEARCH**

EMERGING as a strong contender for a compact, efficient source emitting in the mid-wave infrared, which is the spectral domain spanning 3-5 µm, is the interband cascade laser (ICL). Now it is the laser of choice in many battery-driven chemical sensing applications operating on a low power budget.

Behind this success is a marriage between the interband optical transitions of a conventional diode laser and the cascaded stage architecture of a quantum cascade laser. Now an established source, the ICL realised the key milestone of room-temperature continuous-wave (CW) operation in 2008, and since then this laser concept has spawned a host of related technologies exploiting derivative staged designs. They include the IC infrared photodetector, the IC thermophotovoltaic device, and the ICLED.




For some chemical-sensing applications, including pipeline leak detection and industrial process control, ICLEDs are an attractive alternative to ICLs, as their manufacture is more straightforward and less expensive. Additional strengths include vertical emission, so no waveguide structure is needed, and the opportunity to qualify growth/fabrication in bulk before individual devices are diced, cleaved, and mounted with facet coatings.

Another application for ICLEDs is infrared scene projection, to support laboratory testing of imaging infrared focal-plane arrays. Creating an IR scene requires the generation of a high-fidelity synthetic image, which may include features with widely varying temperatures, such as missile plumes, engine heating, vehicles, and personnel. It's critical to use realistic, scenario-specific conditions, including atmospheric attenuation.

## Adding a resonant cavity

To build on the significant strengths of the ICLED, our team – a collaboration between the Naval Research Laboratory, Amentum, and Praevium Research – is improving this device through the introduction of a resonant cavity.

One may ask why this addition is needed, given that conventional ICLEDs are already emitting powers of up to several milliwatts, which is sufficient for many spectroscopic chemical-sensing applications. But the spectral bandwidth is quite broad – it is typically of the order of 1-2 µm, which is far wider than the linewidth of molecular fingerprint absorption features. With the introduction of a resonant cavity, the emission from the ICLED is narrowed by well over an order of magnitude, and when the wavelength is tuned to match a given chemical absorption feature, the upshot is a higher absorption contrast.

When narrow-linewidth RCLEDs are employed for infrared scene projection, they can simultaneously produce signals at multiple wavelengths, with minimal crosstalk between sub-bands. However, to simulate a high apparent temperature, it's essential to maximise emittance, defined as the output-power per emission area, and also the radiance, which is the emittance per unit solid angle. For applications at very specific wavelengths the spectral intensity, which is the emittance per unit wavelength, is key. For devices with high emittance, introduction of a resonant cavity can greatly enhance the spectral intensity.

Efforts to maximise emittance are impaired by internal losses. When electrons and holes are injected into a mid-wave IR LED they are more likely to recombine non-radiatively via the so-called Meitner-Auger process, than produce light. As the Meitner-Auger decay rate increases exponentially with wavelength, this reduces the output beyond 4 µm – and it explains why the highest reported mid-wave IR emittances occur in the 3-4 µm range. That makes it more challenging to succeed in maximising the emittance and spectral intensity of RCICLEDs operating at longer mid-wave IR wavelengths.

## Design, growth and fabrication

To optimise the performance of our RCICLEDs, we have performed a carefully-choreographed dance between design/simulation, MBE growth, cleanroom fabrication, and optical characterisation – when viewed in conjunction, they form a feedback loop. Key to our success is drawing on several decades of development at NRL, where researchers have fine-tuned expertise related to all aspects of interband cascade emitter production. In order to implement the most favourable distributed Bragg reflector (DBR) mirrors for this latest project, NRL joined forces with Praevium Research, a pioneer in the exploitation of heterogeneously-bonded DBRs, to form high-performance resonant-cavity optoelectronic devices.

The foundation for the recent success is NRL's ICLEDs, emitting near 4.5 µm. Those devices employ type-II quantum wells in 20 active cascade stages, split into two groups of 10. This division allows both groups to centre on peaks of the optical field in the resonant cavity (see Figure 1), providing a modest improvement in the output. Growth of this optimised epitaxial design takes place at NRL, using MBE and a GaSb substrate.

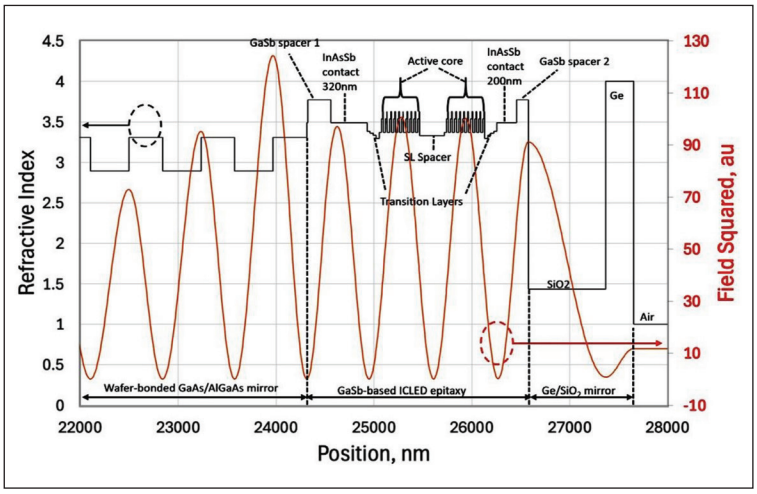



Figure 1. Profiles of the refractive index (orange) and simulated optical mode intensity (black) along the vertical axis within the RCICLED cavity.

Following initial testing at NRL, wafer materials are sent to Praevium. Here, the epitaxial side has been wafer-bonded to a 33-period GaAs/$Al_{0.92}Ga_{0.08}As$ DBR that has a reflectivity of more than 99 percent and forms the bottom mirror of the RCICLEDs. The GaSb substrate is then removed with a chromic acid-based etch, before standard ICLED fabrication techniques are applied, including patterning LED

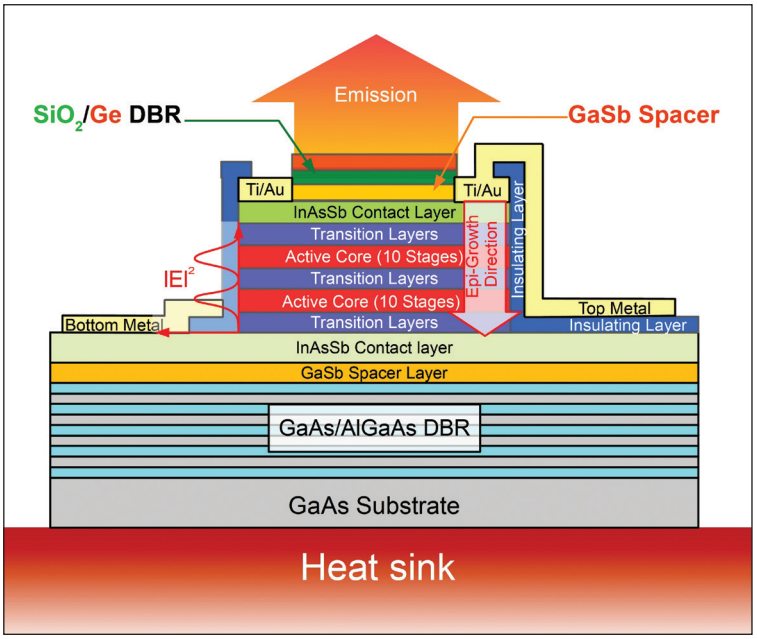



Figure 2. Side-view schematic of the epi-down-mounted RCICLED with 20 active stages split into two groups of 10. The two DBR mirrors defining the cavity are 33 periods of GaAs/$Al_{0.92}Ga_{0.08}As$ on the bottom and a single-period of $SiO_2$/germanium on the top (Device A only).

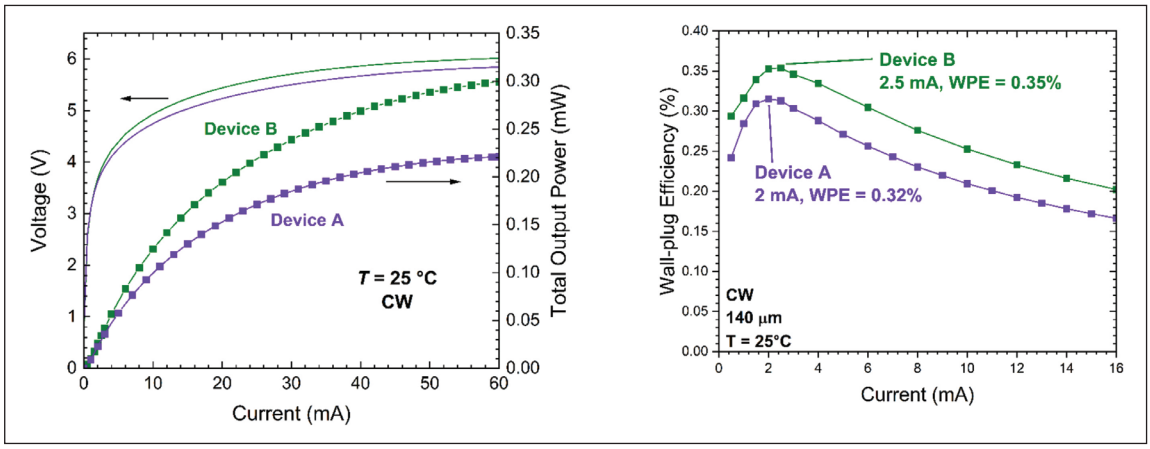



Figure 3. Continuous-wave light-current-voltage characteristics (left) and wall-plug efficiency (right) of Devices A (violet) and B (green) at room temperature.

mesas, to form circular apertures with a diameter of 140 µm, and the deposition of annular top and bottom contacts.

We have produced two forms of emitter in the current study. Device A has a top mirror with a single-period $SiO_2$/germanium DBR that has a reflectivity of more than 85 percent (see Figure 2), and Device B has top mirror formed simply by the semiconductor/air interface, which has a reflectivity of around 30 percent. It is expected that the higher reflectivity top mirror of Device A will result in a narrower linewidth in the resulting emission relative to Device B.

Both classes of RCICLED have been characterised in CW mode at 25°C. Measurements of output power and emission spectrum involved collecting light with an f/1 optic, which corresponds to a collection angle of 26°. For cavities with a high quality factor (Q factor), which is typical in RCLEDs, the measured linewidth is actually highly dependent on the collection angle – set by the collection optic used in the measurement!

Spectra of devices A and B reveal resonance linewidths for these LEDs of 40 nm and 107 nm, respectively – that's dramatically narrower than the more typical value of around 1 µm for conventional ICLEDs processed without a cavity. Peak resonances for devices A and B are 4.47 µm and 4.46 µm, respectively, close to the design value of 4.5 µm. These results are encouraging. To the best of our knowledge, they are the first reports of room-temperature CW operation of resonant cavity LEDs emitting beyond 4 µm. What's more, device A has the narrowest linewidth to date for any LED with a peak wavelength beyond 3.4 µm, thanks to its high-reflectivity top mirror. This linewidth, which is limited by collection angle rather than the quality factor of the cavity, is a valuable asset for chemical sensing and multi-spectral IR scene projection applications.

Plots acquired at 25°C for the CW output power as a function of current and voltage reveal maximum output powers of 0.22 mW and 0.30 mW for device A and B, respectively (see Figure 3). These values, realised for a drive current of 60 mA (near rollover), indicate an emittance of 1.94 W $cm^{-2}$ for device B, based on emission area. That's the highest ever value reported for a mid-wave IR LED operating beyond 3.4 µm, whether driven in CW mode or with a high pulsed duty cycle (we ignore results for a device with out-coupling, enhanced by an immersion lens on its emission surface).

Values for wall-plug efficiency at 25°C for both devices peak at 0.32-0.35 percent, recorded at low drive current. At higher currents efficiency gradually declines. Although these values may seem low, they are characteristic of mid-wave IR LEDs. While low efficiencies stem partly from non-radiative decay, they take a bigger hit from total internal reflection, which prevents most generated radiation from exiting the device.

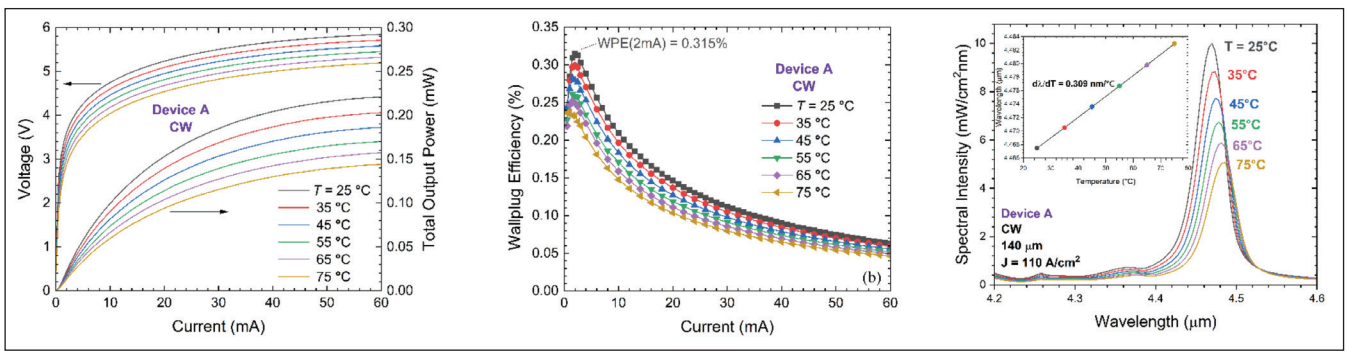



Figure 4. Temperature-dependent continuous-wave light-current-voltage characteristics (left), wall-plug efficiency (middle), and spectral intensity (right) of Device A over the range 25-75 °C.

Our RCICLEDs, emitting a high spectral intensity in a bandwidth that's as narrow as 40 nm, will be compelling candidates for chemical sensing, multi-spectral IR scene projection, and a number of other applications. Prior to commercialisation, challenges must be addressed, related to controlling the efficiency and directionality of the light escaping the semiconductor.

A significant strength of our devices is their excellent temperature stability between 25°C and 75°C, according to plots of output power as a function of current and voltage for device A (see Figure 4). At the highest measured temperature, wall-plug efficiency still peaks at nearly 0.24 percent. Spectral data indicate an almost negligible widening of the resonance linewidth with temperature (from 40 nm to 42 nm), along with a very gradual red-shift in the centre wavelength, which increases at a rate 0.31 nm $°C^{-1}$.

A key figure of merit for spectroscopic applications and multi-sub-band infrared scene projection is spectral intensity, which is defined as the emittance per unit wavelength. The most appropriate approach to determine this quantity involves some calculus of the emission spectrum (obtained by determining the spectrum's derivative as a function of wavelength, when the integration over δλ segments is normalised to the total output power). However, there are many reports in the scientific literature where spectral intensities are crudely approximated, simply by taking the ratio of total emittance to the full-width-at-half-maximum linewidth – this is only accurate for a top-hat emission profile.

For our devices, emission includes significant tails (see Figure 4). We 'removed' them when remeasuring spectra, using a narrow-bandpass filter

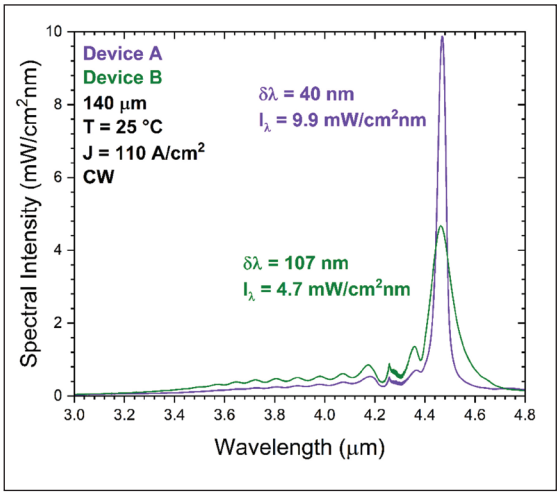



Figure 5. Continuous-wave spectral intensities of Devices A (violet) and B (green) under moderate current injection at room temperature. The legend indicates values at the resonance peaks.

that excludes wavelengths far from the peak. This determined that around just 70 percent of the total output emitted by both RCICLEDs fell within the cavity resonances.

It should be noted that when the width is limited by collection angle, as is the case for these devices, only linewidths measured with the same collection angle can be compared meaningfully. For example, the difference in apparent linewidths measured with an f/1 and an f/2 collection optic can exceed a factor of 3!

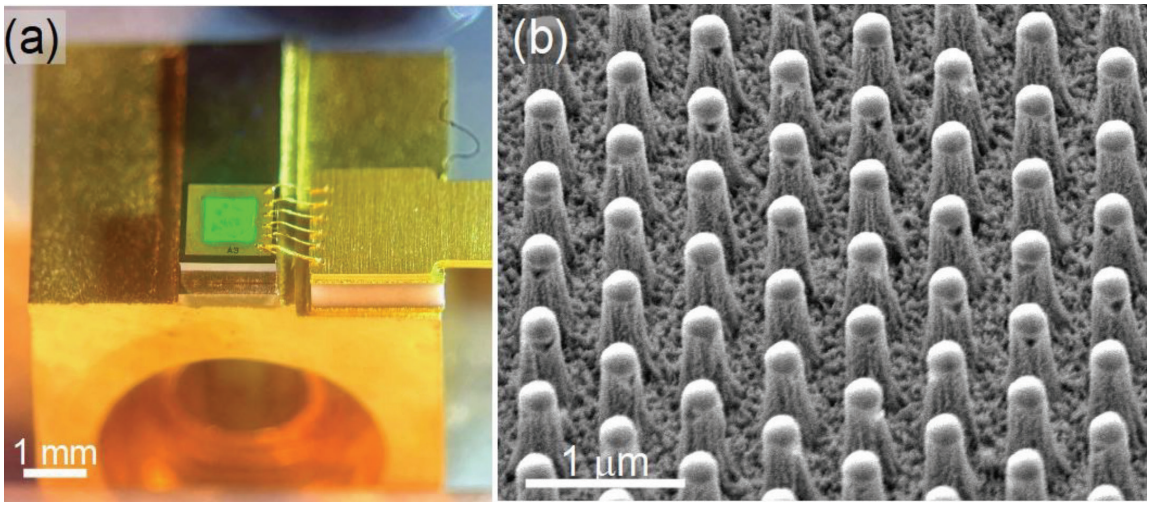



Figure 6. (a) Optical micrograph of the moth-eye (ME) ICLED mounted epi-down on a C-mount. The greenish-blue emission from the device is attributed to diffraction by the ME surface pattern. (b) Tilted-view SEM image showing the ME nanopillar array. Scale bars: 1 mm and 1 μm for (a) and (b), respectively.

We have determined the dependences on wavelength of properly-calibrated spectral intensities for both devices (see Figure 5). For device A, the peak value is 10 mW $cm^{-2}$ $nm^{-1}$. This is more than four times the previous best for a mid-wave IR RCLED.

## Enhancing output

For mid-wave IR LEDs with a flat, high-index output surface, such as that of a GaSb substrate, most radiation is trapped by total internal reflection, due to a critical angle of around just 15°. This limits the maximum out-coupling efficiency to about 4 percent, even when ignoring the reflection of some of the radiation falling within this cone (some portion of which may still be emitted following one or more bounces between the top and bottom surfaces). Adding a single-layer anti-reflection coating increases the maximum out-coupling, but only a little, with this figure rising to about 5.3 percent.

These values highlight the considerable headroom for a higher wall-plug efficiency, which may be realised by enhancing the low outcoupling efficiency. The most straightforward way to accomplish this is to replace the flat output surface with an immersion lens or micro-lens. However, that's less practical when emitters need to be deployed in tightly-packed arrays with small pitch.

Simple alternatives are to roughen the output surface on the wavelength scale, or introduce a specially-designed 'motheye' pattern. We have pursued the latter, realising a modest output enhancement (see Figure 6 for a scanning electron microscopy image of a preliminary motheye structure). Efforts are ongoing to exploit methods that deliver high efficiencies in visible LEDs.

## Towards the future

Our RCICLEDs, emitting a high spectral intensity in a bandwidth that's as narrow as 40 nm, will be compelling candidates for chemical sensing, multi-spectral IR scene projection, and a number of other applications. Prior to commercialisation, challenges must be addressed, related to controlling the efficiency and directionality of the light escaping the semiconductor. Future designs, incorporating engineered output surfaces, such as motheye, microlens, and integrated metalens structures, will need to increase radiance while preserving the vertical-emission geometry that makes ICLEDs attractive for arrays and scalable manufacturing. In parallel, we will continue to pursue optimisation of the active-stage, cavity, and DBR designs, as this promises further improvements to the emissivity, linewidth, and spectral intensity of these sources.

*Praevium Research acknowledges support by SBIR contract number N6833524C0298 funded by Navair, and NRL acknowledges support by a CRADA with Praevium Research.*

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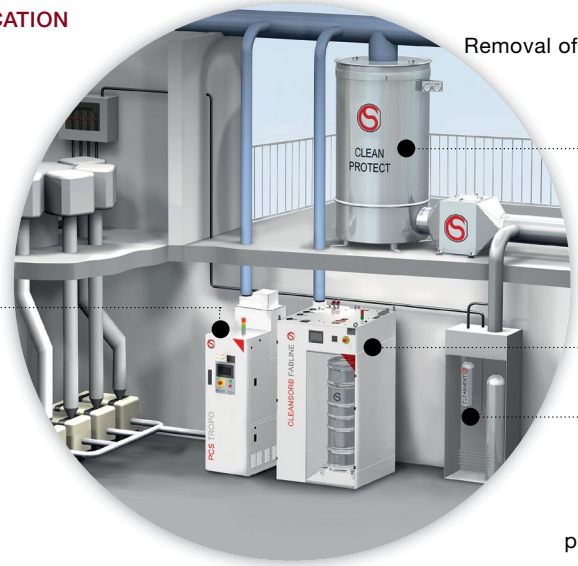
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# Banishing breakdown in GaN HEMTs

A punch-through gate design equips the E-mode GaN HEMT with an inherent non-destructive breakdown capability

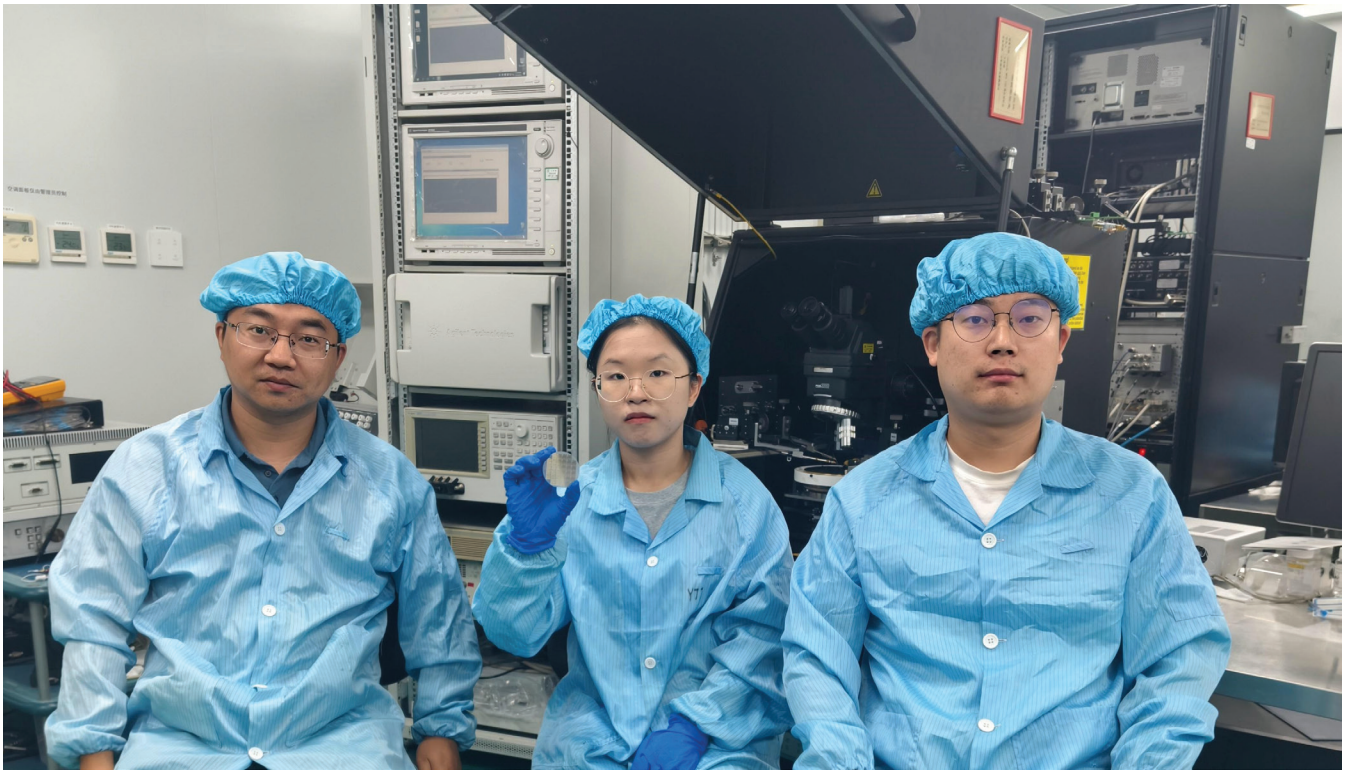
BY JINGJING YU, JUNJIE YANG, BO SHEN AND JIN WEI FROM PEKING UNIVERSITY

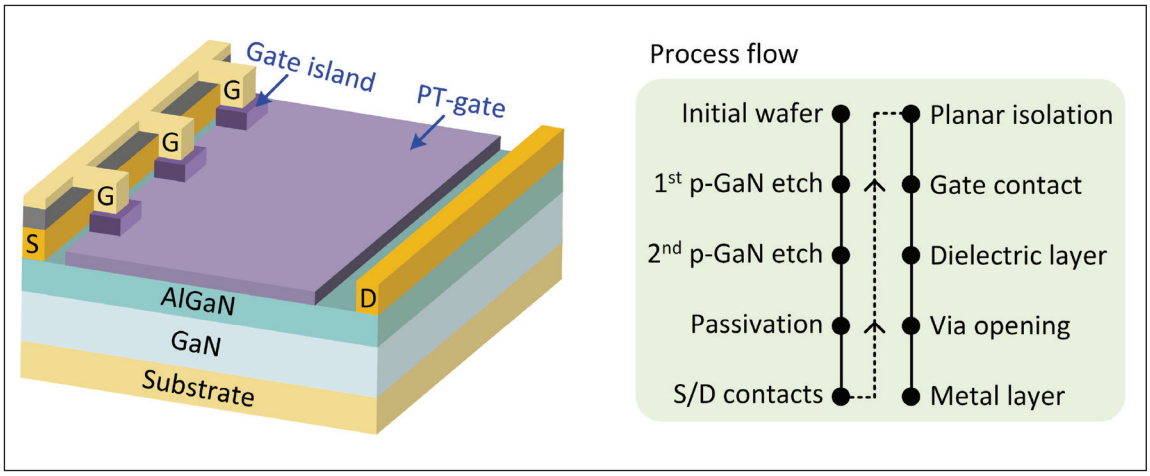
WITHIN THE PORTFOLIO of power devices, the GaN HEMT is renowned for its high power and high frequency, resulting from a fast switching-speed and low conduction loss. Today, HEMTs with a *p*-GaN gate are combining enhancement-mode operation with a low on-resistance and a high breakdown voltage, a set of attributes that are attractive for consumer applications, such as fast chargers and class-D audio amplifiers. However, the broader adoption of the GaN HEMT in demanding industrial applications is impeded by its limited robustness against transient overvoltage spikes, common in high-frequency power switching applications.

This weakness is not found in vertical silicon and SiC power devices – they typically exhibit non-destructive breakdown behaviour under transient voltage overshoots, due to an intrinsic avalanche capability. In contrast, lateral GaN power HEMTs tend to suffer from destructive breakdown, possibly due to the absence of a *p-n* junction that effectively removes impact-ionisation-generated carriers. Due to this weakness, engineers significantly overdesign the blocking capability of state-of-the-art GaN power HEMTs.

One option for addressing the limited transient overvoltage reliability in GaN transistors is to add snubber circuits that suppress the voltage oscillation. However, this solution complicates design and increases system volume.

An alternative is to parallel a GaN power HEMT with a device with a lower breakdown voltage, such as a monolithically integrated silicon or SiC *p-n* junction diode. But such pairings are problematic, entailing






➤ Figure 1. The structure and process flow of the proposed *p*-GaN gate punch-through HEMT (PT-HEMT).

intensive research into stress compensation during the growth of GaN epitaxial layers on specially designed substrates. What's more, there's the need for additional fabrication steps to form diodes within the substrate and electrically connect diodes with corresponding HEMTs. This adds to complexity and overall cost.

Due to the drawbacks of the two approaches just outlined, a better approach is needed for delivering repetitive non-destructive breakdown behaviour. Rather than pairing the GaN HEMT with other devices or circuits, efforts should be directed at refining this transistor.

## Punch-through gate design

Offering one solution is our team from Peking University. We are pioneers of a novel punch-through concept, based on a standard E-mode *p*-GaN gate HEMT platform (see Figure 1).

Our device, fabricated on a standard *p*-GaN gate HEMT epiwafer, delivers E-mode operation. Its uniqueness comes from its combination of: an array of *p*-GaN islands along the width of the device, providing a control gate; and a thinned *p*-GaN layer, acting as a punch-through gate (PT-gate), that covers most of the access region. We position the PT-gate edge at 3 µm from the drain terminal.

When the PT-gate is fully depleted under a high drain bias, this leads to a punch-through of the underlying 2DEG channel at a large yet safe off-state drain bias. This results in a non-destructive breakdown. Modulating the length and thickness of the PT-gate layer enables adjustments to the breakdown voltage, to accommodate various voltage ratings.

We fabricated our devices on a 2-inch GaN-on-sapphire wafer featuring a buffer layer, a 200 nm-thick GaN layer, a 15 nm-thick $Al_{0.2}Ga_{0.8}N$ barrier layer, and a 90 nm-thick *p*-GaN layer. Partial etching of the *p*-GaN layer forms gate islands, before a second etch defines the PT-gate. On this processed wafer we deposit a 50 nm-thick $SiO_2$ layer by plasma-enhanced CVD at 300°C. Etching of this $SiO_2$ layer and then depositing a Ti/Al/Ni/Au stack introduces source and drain ohmic contacts, annealed at 810°C. Fluorine ion implantation provides planar isolation, prior to the deposition of a Ni/Au stack on gate islands, annealed to form an ohmic contact to *p*-GaN. Another $SiO_2$ layer is then deposited by plasma-enhanced CVD, before contact windows are formed by a dry etch. Finally, a Ti/Au stack is added, to provide metal interconnections and probing pads.

Crucially, this fabrication process is compatible with standard *p*-GaN gate HEMT technology. Fabrication of the PT-gate structure is easy to realise with an additional *p*-GaN etching process.

## Underlying mechanism

When our device is in its off-state, a high drain bias generates a depletion region within the PT-gate, which is the thinned *p*-GaN layer. This depletion region expands progressively from the drain side toward the source side, and once the PT-gate is fully depleted, it loses electrostatic control over the underlying 2DEG channel. At this point the 2DEG channel is punched through, resulting in a non-destructive breakdown.

The good news is that while conventional HEMTs suffer from severe dynamic degradation in on-resistance, due to charge trapping, our PT-HEMTs maintain exceptional stability. We attribute this superiority to the dual role of the PT-gate: first, surface trapping is effectively screened by mobile holes within the PT-gate; and second, buffer trapping is significantly suppressed by hole injection from the PT-gate into the underlying layers.

To provide experimental evidence of this mechanism, we have investigated the relationship between the PT-gate depletion voltage and the punch-through breakdown voltage. This involved fabricating a dedicated *p*-channel JFET to analyse the depletion dynamics of the thinned *p*-GaN layer. In this configuration, the thinned *p*-GaN layer serves as the conduction channel, while an ohmic contact to the 2DEG acts as the gate. When we increase the gate-to-source voltage to the threshold voltage, the depletion region expands beyond the length of the *p*-GaN layer to pinch off the *p*-channel current path. Measurements show that the threshold voltage increases with the length of *p*-GaN layer and the thickness of the thinned *p*-GaN.

We fabricated specific test devices to characterise the punch-through breakdown voltage with different designs, in terms of the length of the *p*-GaN layer and the thickness of the thinned *p*-GaN. All devices feature a PT-gate covering the 2DEG channel and a control gate outside the active region. During characterisation at a gate-to-source voltage of 0 V, we observed a sharp rise in current after the drain-to-source voltage reached the punch-through breakdown voltage, signalling the onset of the punch-through effect.

A summary of the relationships between the length of *p*-GaN layer, and both the PT-gate depletion voltage and the punch-through breakdown voltage, is provided in Figure 2 (b) and (c). Definitive evidence that the full depletion of the PT-gate is the cause of non-destructive breakdown behaviour in PT-HEMTs is provided by the well-matched values for the PT-gate depletion voltage and the punch-through breakdown voltage.

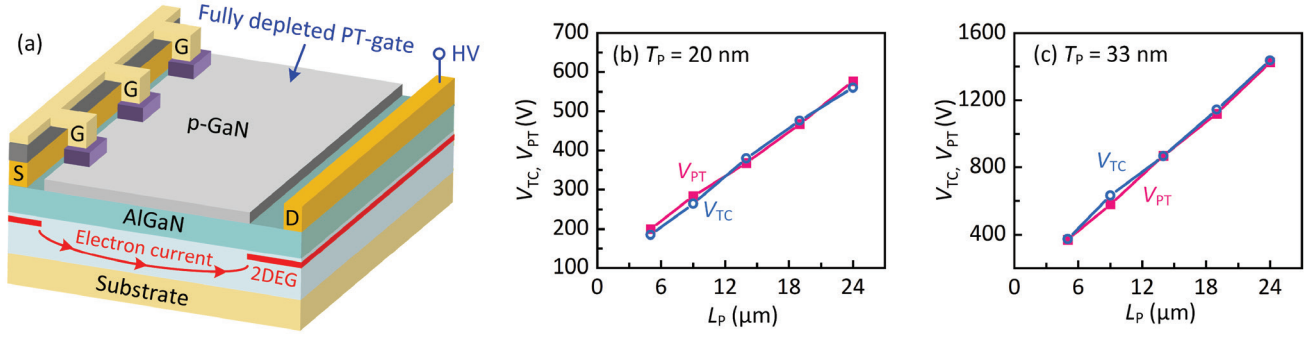
## Non-destructive breakdown

To underscore the importance of our new design, we have compared the off-state characteristics of our PT-HEMT with a conventional *p*-GaN gate HEMT (see Figure 3 (a)). Both these devices have a gate-to-drain spacing of 12 µm, and the PT-HEMT has a *p*-GaN thickness of 33 nm. For the conventional HEMT, catastrophic, destructive breakdown occurs at 1176 V – that's defined as the voltage where drain current rises sharply. Following this breakdown, the device behaves as a low-resistance resistor, indicating that the breakdown is destructive. In contrast, our PT-HEMT exhibits a stable, non-destructive breakdown behaviour at a clamping voltage of 874 V, offering a built-in safety margin for power systems.

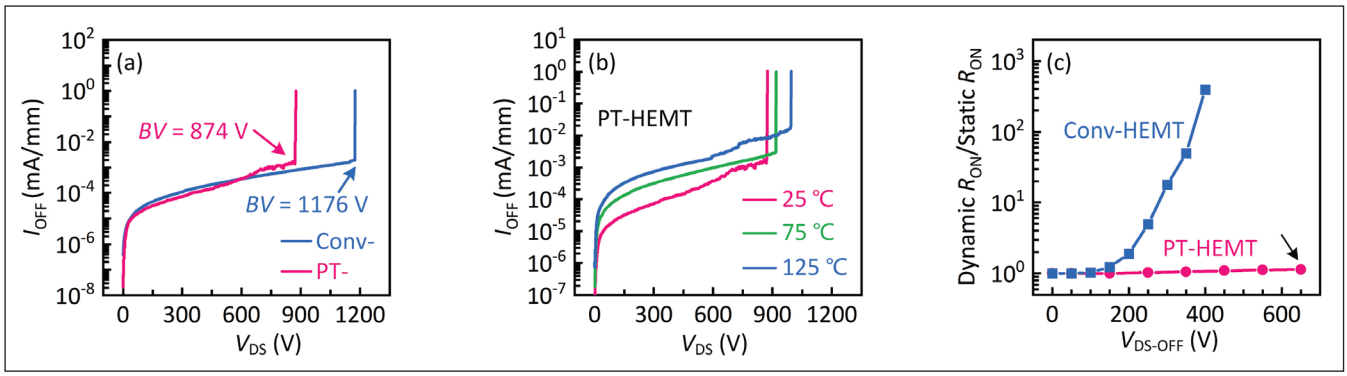
We have investigated the temperature dependence of the punch-through mechanism. Our measurements reveal that the breakdown voltage of our PT-HEMT climbs from 874 V at 25°C to 992 V at 125°C (see Figure 3 (b)). Note that this positive temperature coefficient – potentially linked to temperature-dependent trapping and de-trapping processes – is highly desirable for power applications. The primary benefit of a positive temperature coefficient is the promotion of a more uniform current distribution across the device area during breakdown events. In turn, this prevents localised overheating and enhances overall robustness.

For GaN power HEMTs, another critical bottleneck that restricts the application of these devices to higher voltage ratings is a degradation in the dynamic on-resistance. Due to this concern, we have investigated if this is an issue in our devices (see Figure 3 (c)).

The good news is that while conventional HEMTs suffer from severe dynamic degradation in on-resistance, due to charge trapping, our PT-HEMTs maintain exceptional stability. We attribute this superiority to the dual role of the PT-gate: first, surface trapping is effectively screened by mobile holes within the PT-gate; and second, buffer trapping is significantly suppressed by hole injection from the PT-gate into the underlying layers. Consequently, the PT-HEMT achieves a remarkably low ratio between the dynamic and static on-resistance: it is less than 1.2, even after high-voltage stress.




➤ Figure 2. (a) Schematic illustration of the punch-through breakdown mechanism in the PT-HEMT. Summary of the PT-gate depletion voltage (VTC) and punch-through breakdown voltage (VPT) as a function of LP with (b) TP = 20 nm and (c) TP = 33 nm.




➤ Figure 3. (a) Off-state performance of the conventional HEMT and PT-HEMT with an $L_{GD}$ of 12 µm. The breakdown in conventional HEMTs is destructive, while in PT-HEMTs it is non-destructive. (b) Temperature-dependent off-state performance of PT-HEMTs. (c) Dynamic $R_{ON}$ characteristics of the conventional HEMT and PT-HEMT.

Thanks to the incorporation of a punch-through path, our design effectively overcomes the inherent absence of avalanche breakdown in the GaN HEMT. By equipping our devices with a non-destructive breakdown capability, alongside a low dynamic on-resistance degradation, we have positioned them as very compelling candidates for hardening power systems in harsh operating conditions.

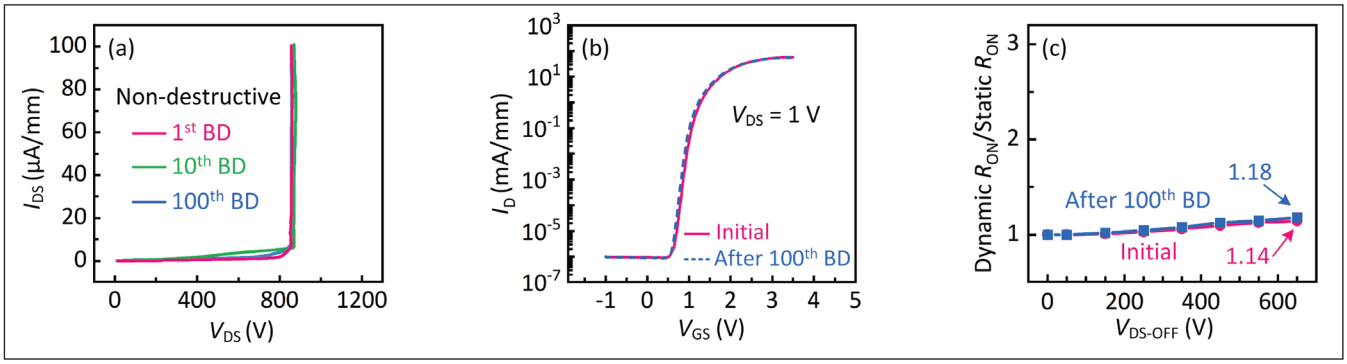
To demonstrate the non-destructive breakdown behaviour of our PT-HEMT more intuitively, we have undertaken rigorous repetitive breakdown characterisation, which includes current-driven breakdown measurements (see Figure 4 (a)). During the test, we limited the maximum current to 100 µA mm$^{-1}$ to prevent overheating of our devices. We set the gate-to-source voltage to 0 V, and employed a current source to force a drain current through our device. Encouragingly, our PT-HEMT successfully sustained over 100 non-destructive breakdown cycles, while clamping the drain-source voltage at a punch-through voltage of approximately 870 V.

We have recorded the static and dynamic performance of our PT-HEMT before and after 100 cycles of punch-through breakdown (see Figures 4 (b) and (c)). This device exhibits a stable threshold voltage and subthreshold swing. Crucially, even after repetitive high-voltage stress, our PT-HEMT maintains a ratio for dynamic-to-static on-resistance of just 1.18, at a drain stress voltage of 650 V. This result shows that our PT-HEMTs have an inherent capability to handle transient overvoltage spikes in high-power switching applications.

There is good reason to believe that our PT-HEMT will support the growth of applications that GaN power electronics can serve. One of its key metrics is its flexibility, with modifications to the length and thickness of the PT-gate layer enabling the device to cater for different voltage requirements. As our novel transistors are inherently suitable for handling transient overvoltage spikes in high-power switching applications, they promise to deliver a step-change in transient-overvoltage robustness in high-voltage GaN technology.

## FURTHER READING

➤ J. Yu *et al.* "E-Mode p-GaN Gate Punch-Through HEMT with Robust Non-Destructive Drain Breakdown" in IEDM Tech. Dig., Sec. 26-4 (2025)




➤ Figure 4. (a) Current-driven breakdown characteristics of a PT-HEMT with an $L_{GD}$ of 12 µm, demonstrating 100 cycles of non-destructive breakdown with stable breakdown voltages around 870 V. (b) Transfer curves and (c) dynamic $R_{ON}$/static $R_{ON}$ ratio of a PT-HEMT before and after 100 cycles of non-destructive breakdown.

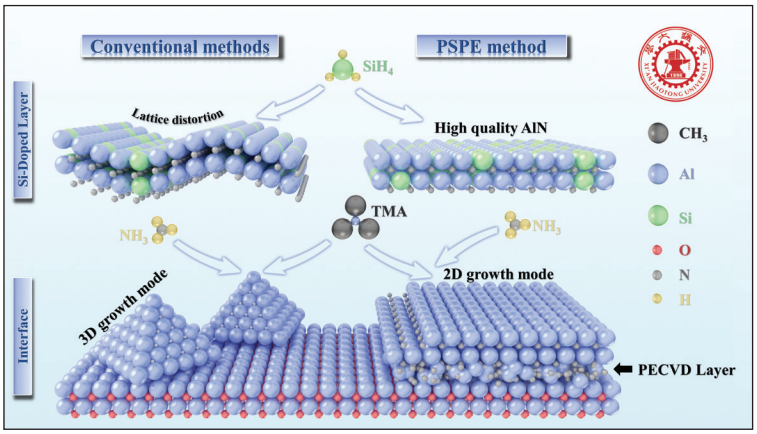
# Novel growth enhances AlN-on-sapphire epiwafers

## High-quality AlN-on-sapphire results from combining plasma-enhanced CVD with pulsed MOCVD

ENGINEERS from Xi'an Jiaotong University, China, have improved the quality of 150 mm AlN-on-sapphire epiwafers by bringing together two well-known epitaxial technologies.

The team uses plasma-enhanced CVD to provide an initial AlN seed, prior to pulsed MOCVD growth of an AlN epitaxial layer.

This combination, referred to as plasma-seed pulsed epitaxy (PSPE), ensures the control of nucleation, growth modes, and defect evolution. Improvements over just pulsed epitaxy include a reduction in surface roughness by 30 percent, a decrease in stress by more than 50 percent, and a slashing of screw and edge dislocations by an order of magnitude.




➤ By controlling nucleation, growth modes and defect evolution, plasma-seed pulsed epitaxy (PSPE) improves the quality of AlN grown on sapphire.

Using plasma-enhanced CVD for the growth of the initial AlN seed enables modification of nucleation and early growth behaviour. This provides a good foundation for growth of an AlN layer using a pulsed precursor sequence.

"In our pulsed process, trimethylaluminium and ammonia are introduced sequentially – for 4 seconds and 2 seconds per cycle, respectively. This pulsed growth constitutes the 'pulsed epitaxy' component of the PSPE method," explains team spokesman Li Geng.

To demonstrate the benefits of PSPE, Geng and co-workers characterised two samples. The first has a 20 nm-thick AlN layer grown by plasma-enhanced CVD, followed by three layers of AlN, all grown by pulsed epitaxy MOCVD – a 1000 nm-thick undoped layer of AlN, and then two 300 nm-thick layers of AlN with different levels of silicon doping. The second sample, produced to provide a benchmark, just has layers grown by pulsed epitaxy MOCVD.

Using X-ray rocking curves, the team determined screw and edge-type dislocation densities in the control sample of $6.0 \times 10^8$ cm$^{-2}$ and $4.4 \times 10^{10}$ cm$^{-2}$, respectively. In comparison, the sample produced using PSPE has equivalent densities of $9.2 \times 10^7$ cm$^{-2}$ and $1.8 \times 10^9$ cm$^{-2}$, respectively.

Cross-sectional transmission electron microscopy shows that the absence of the 20 nm-thick AlN layer grown by plasma-enhanced CVD leads to the generation of a high density of screw dislocations at the AlN-sapphire interface. As epilayer growth continues, most dislocations form dislocation loops, prior to annihilation; and edge dislocations, also originating at the heterointerface, extend vertically to the surface. In contrast, for the sample produced by PSPE, the few edge dislocations that are present are annihilated, and almost no screw dislocations are generated at the interface.

Additional characterisation of the control sample revealed a relatively high intrinsic compressive stress in the AlN that arises from lattice mismatch, and can be partially compensated by low levels of silicon doping. With the sample produced by PSPE, as there is a substantial relaxation of intrinsic stress before silicon doping, the tensile stress introduced by low levels of silicon doping can lead to a deterioration in surface morphology. For both samples, at higher silicon concentrations, there's excessive stress accumulation, causing an increase in surface roughness.

Note that Geng does not view the higher roughness of the PSPE sample at low doping levels – it's 1.68 nm, compared with 1.17 nm for the control – as a fundamental limitation of the team's hybrid growth approach. He argues that while the slight surface-quality degradation associated with silicon-induced stress under certain doping conditions needs to be considered when optimising the silicon concentration, the overall effect of PSPE is positive: "It provides a smoother surface, together with substantially improved crystal quality and reduced residual stress."

Efforts are now being directed at optimising the PSPE method, which includes considering the impact of adding silicon and carbon impurities. "Our ongoing optimisation has already resulted in a noticeable improvement in the epitaxial quality compared with the results reported in this paper," says Geng. "This gives us confidence that the PSPE method still has considerable room for further improvement."

REFERENCE
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# Ammonia plasma treatment enhances ß-$Ga_2O_3$ Schottky barrier diodes

## Superior electrical characteristics stem from interfacial chemical modifications produced by ammonia plasma treatment

RESEARCHERS from Xidian University have turned to ammonia plasma treatment to improve the electrical characteristics of ß-$Ga_2O_3$ Schottky barrier diodes. With this treatment, the team's devices benefit from a lower turn-on voltage and a suppressed reverse-leakage current.

"The effectiveness of ammonia plasma treatment originates from our understanding of $Ga_2O_3$ surface defects," says team spokesman Yobo Wang, who points out that low-valence gallium on the $Ga_2O_3$ surface compromises device performance by causing interface defects and lattice discontinuity. Thanks to the reducing nature of an ammonia plasma, these surface defects are repaired with this treatment, which elevates the valence state of gallium from low-valence to $Ga^{3+}$.

Over a number of years, this team and others have investigated many approaches to improving the interface in ß-$Ga_2O_3$ devices, and ultimately advancing electrical performance. It's been shown that oxygen annealing passivates oxygen vacancies, reducing line-shaped defects on the ß-$Ga_2O_3$ surface, but leads to an increase in specific on-resistance; and it's been demonstrated that surface etching can remove donor-like impurities and significantly enhance the breakdown voltage, but it's challenging to ensure repeatability. Investigations have also revealed that post-annealing improves interface quality, but often at the expense of the specific on-resistance; and $N_2O$ plasma treatment reduces the turn-on voltage but has a limited impact on interface traps.

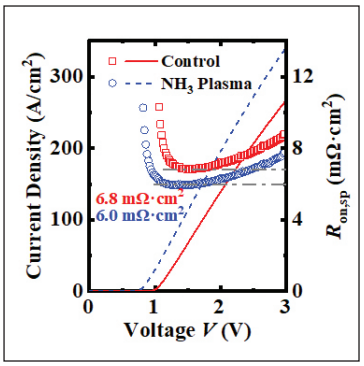
Judged against this backdrop, efforts by Wang and co-workers have much appeal – they improve the interface quality of ß-$Ga_2O_3$ Schottky barrier diodes, trim their turn-on voltage, boost breakdown and suppress the reverse-leakage current.

Proof of success comes from comparing a control and plasma-treated device, both produced by first growing an 11 µm-thick silicon-doped ß-$Ga_2O_3$ layer on a highly tin-doped ß-$Ga_2O_3$ substrate. Fabrication of both of these diodes began by chemical cleaning, sputtering Ti/Au on the backside of the substrate, and annealing at 475°C for 60 s under nitrogen gas to form the cathode ohmic contact.

For subsequent plasma treatment, the partially processed devices were loaded into a plasma-enhanced atomic layer deposition chamber. Treatment for a duration of 20 minutes at 300°C involved an RF power of 2500 W, and ammonia and argon flows of 100 sccm and 60 sccm, respectively.

To complete device fabrication, circular Schottky Ni/Au anodes were added to samples removed from the chamber, as well as controls avoiding this plasma-treatment step.

Capacitance-voltage plots of both types of diode revealed that ammonia plasma treatment reduces the built-in voltage from 1.21 V to 0.98 V. Drawing on X-ray photoelectron spectroscopy measurements, the team attribute this fall in built-in voltage to combination of nitrogen incorporation into the ß-$Ga_2O_3$ surface, a reduction in the gallium sub-oxide and adsorbed oxygen.




➤ Ammonia treatment boosts the current density, trims the operating voltage, and reduces the specific on-resistance.

Treated devices have a specific on-resistance of 6.0 mΩ cm², compared with 6.8 mΩ cm² for the control. Wang and co-workers are unable to determine contributions to these values from the epitaxial layers, substrates, current spreading, and the Schottky and ohmic contacts.

Under a forward voltage of 3 V, the treated device has a higher current density – it's 341 A $cm^{-2}$, compared with 267 A $cm^{-2}$ for the control. According to the team, improved conduction performance comes from a reduced specific on-resistance and a lower on-voltage.

Drawing on capacitance and conduction plots over a frequency range from 1 kHz to 1 MHz, the team determined that ammonia plasma treatment led to a 30 percent reduction in interface states, attributed to the reduced gallium-suboxide and the adsorbed oxygen.

Ammonia plasma treatment also produced an increase in breakdown voltage from 822 V to 974 V.

The next goals for the team include refining the process conditions of the ammonia plasma treatment process, and combining this with $Ga_2O_3$ diode termination technologies and *p-n* junction diode design schemes. Success should lead to higher performance devices.

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➤ H. Hu *et al*. Appl. Phys. Lett. **129** 123501 (2026)

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