COMPOUND SEMICONDUCTOR

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INSIDE

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A NEW LEASE OF LIFE FOR CPV

Grid-friendly renewable energy flows from a system that combines III-V cells with thermal energy storage

SLASHING THE COST OF EPITAXY

A radical form of HVPE speeds growth, ensures high-quality interfaces, and allows inclusion of aluminium-based alloys

THE GLORIOUS GATE OXIDE

Experiments reveal that there is no need to worry about the lifetime of the SiC gate oxide under negative stress

Global mega trends require best performance III-V materials

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VIEWPOINT

By Dr Richard Stevenson, Editor

Will history repeat itself?

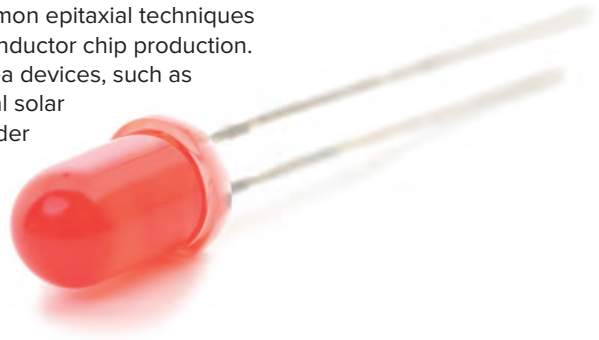
IN TECHNOLOGY-DRIVEN INDUSTRIES, such as ours, movement tends to be in just one direction. Take, for example, the RF devices that we produce to support mobile communication. As infrastructure advances from one generation to another to realise higher data rates, we have shipped RF devices that amplify at higher frequencies, and over a broader bandwidth. Or consider the GaN-based LED. Through increases in its output power and efficiency over several decades, it has expanded the tasks it fulfils. Initially deployed to primarily light keypads, it is now also backlighting displays and illuminating homes, offices and public places.

But progress isn't always linear, as we highlight in this issue.

Not that long ago, consumer electronics overtook data comms as the biggest market for the VCSEL, driven by Apple's pioneering use of this emitter for facial recognition. Where Apple led others followed – but they aren't any more, instead favouring software-based approaches (see p. 16). Despite this, sales of VCSELs for consumer electronics are still on the rise – but this growth is being outpaced by the data comms sector, which is returning to pole position.

Another arena where previous domination might make a comeback is epitaxial growth. Back in the 1970s our industry employed HVPE for the production of a range of devices, including commodity red-emitting LEDs.

Due to several significant weaknesses associated with this growth technology – such as poorly controlled growth windows; a limited palate of materials; and the inability to provide sharp interfaces, including those required for *p-n* junctions – MOCVD and MBE have taken over as the most common epitaxial techniques for compound semiconductor chip production. However, for large-area devices, such as flexible multi-junctional solar cells not operating under concentration, the throughput of the incumbent growth technologies is not high enough for cost-effective production.



To speed up epitaxial growth, a team from the National Renewable Energy Laboratory is revisiting HVPE (see p. 26). By modifying the design of the reactor, they are addressing weaknesses while maintaining strengths, including a very fast growth rate, which can be described in terms of millimetres per hour.

A very impressive element of innovation is the use of several growth chambers, with the wafer shuffled back and forth, enabling realisation of sharp interfaces. Additional gains come from supplying uncracked hydride sources to the surface, aiding control over the growth rate; and introducing the growth of aluminium-containing alloys via a new precursor and a lower growth temperature.

Growth of a range of structures – including solar cells, distributed Bragg reflectors and HBTs – has demonstrated that this new form of HVPE, named Dynamic HVPE, is highly versatile and very capable. And while it has the greatest appeal for manufacturing large-area devices, such as solar cells, it has the potential to deliver cost reductions for many forms of chip production. So maybe the incumbent of yesteryear will kick on to become the dominant force of tomorrow.

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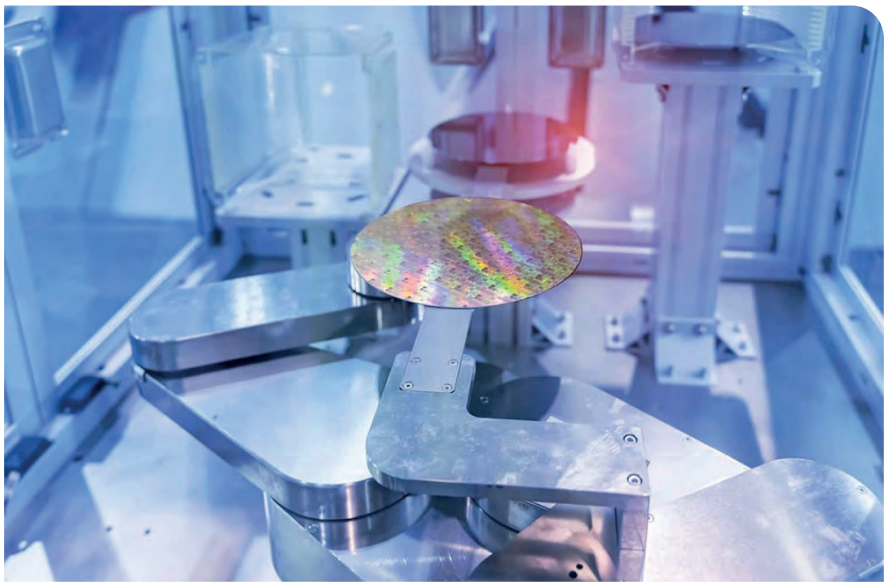
GlobalFoundries gets $30 million to expand GaN production

US federal funding will advance innovation and production of next-generation GaN power chips

GLOBALFOUNDRIES has been awarded $30 million in US federal funding to advance the development and production of next-generation GaN-on-silicon semiconductors at GF's facility in Essex Junction, Vermont.

The funding will enable GF to purchase tools and extend development and implementation of 200 mm GaN wafer manufacturing for making chips for high-power applications including electric vehicles, industrial motors and energy applications.

GF's facility in Essex Junction, Vermont, near Burlington, was among the first major semiconductor manufacturing sites in the United States. Today nearly 2,000 GF employees work at the site, with a manufacturing capacity of more than 600,000 wafers per year. The Fab is a Trusted Foundry and manufactures secure chips in partnership with the US Department of Defense, for use in some of the nation's most sensitive aerospace and defence systems.



This Other Transaction Agreement was entered into by the Defense Microelectronics Activity via the Trusted Access Program Office (TAPO) of the US Department of Defense. TAPO's primary mission is to procure advanced semiconductors for the Departments most critical and sensitive weapons systems platforms. TAPO has been supporting dual use (both civilian and military applications) GaN-on-silicon development efforts since 2019 as GaN provides a stable semiconductor suitable in high-power, high-frequency devices the DoD needs to maintain technology advantage for the United States. This current development phase plans to leverage previous TAPO successes and continue maturing this dual use technology.

"GlobalFoundries has been a critical partner to the Trusted Access Program Office, enabling semiconductor assurance (Trust) to advanced semiconductor technologies for the Department's most advanced weapon systems platforms.

This engagement is just one step the DoD is taking to ensure the US has continued access to advanced microelectronics technologies such as GaN," said DMEA director Nicholas Martin.

First foldable microLED TV

C SEED presented the world's first foldable 144 inch microLED TV at CEDIA Expo 2022. The C SEED HLR TV is hidden inside a compartment box, and activated with the push of a button on a remote control. It takes 60 seconds to rise to its height of 2.5 m and then the five /seven massive MicroLED panels unfold automatically within the next 45 seconds. After use, the HLR TV submerges back into its box.

The HLR TV features outdoor microLED technology with 1.6 pixel resolution and IP65 rating, providing 4,000 nits brightness, a far wider colour gamut and a higher contrast than conventional LED screens. The HLR TV processes image data up to 100,000 times per second, enabling the screen to display 64 billion colours.

Porotech produces the world's first 'all-in-one' full-colour microLED display

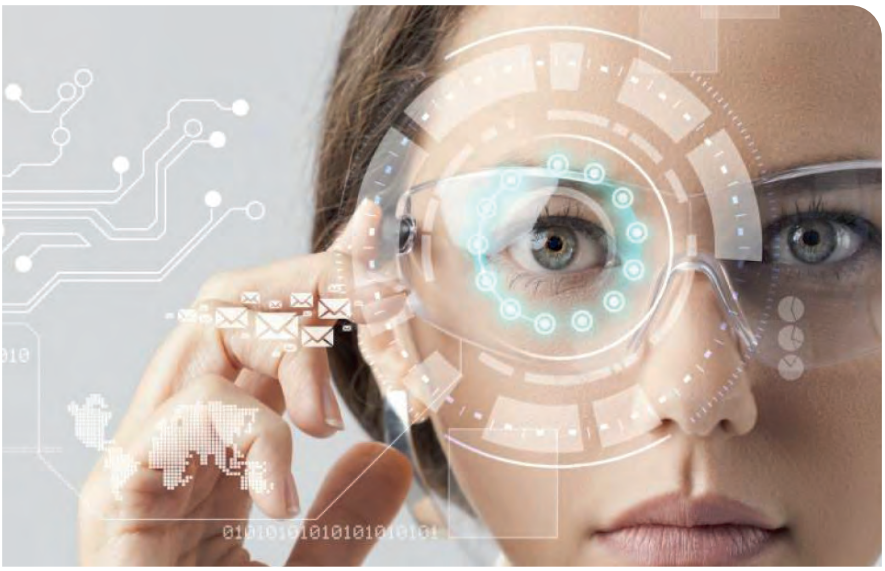
Porotech's DynamicPixelTuning tech enables a single pixel to emit across the entire colour spectrum, including white light

POROTECH, a UK start-up focused on microLED and GaN semiconductor technology, is claiming the world's first public demonstration of an 'all-in-one' full-colour display of microLED pixels.

Porotech is pioneering displays that use a single microLED diode for all colours, moving away from the constraints of the RGB (red-green-blue) sub-pixel model that underpins all current commercial display technologies.

Porotech's innovation lies in its DynamicPixelTuning (DPT) technology. PoroGaN, the GaN-based material that underpins DPT, allows a modulated current to be leveraged to emit visible light covering the entire colour spectrum on a single microLED chip. Among the colours it can emit, a DPT microLED is able to achieve a world first by emitting pure white from a single pixel.

The company thinks DPT is game-changing for the display industry at large. By removing the need for RGB sub-pixels, DPT allows a microLED-driven display to increase overall pixel density fourfold. As a result, DPT can produce substantial gains in resolution, brightness and efficiency for every type of display. This breakthrough is of particular interest for small form factor displays that demand high resolution, such as AR and VR displays, as well as wearable tech.



Porotech will be making the first public debut of DPT at CES 2023 in Las Vegas, where it will be showcasing a 0.26 inch DPT microdisplay with a sub-5 μm full colour pixel, followed by various other industry events in Q1 2023.

Porotech's CEO and co-founder Tongtong Zhu says: "The world's first full colour and all-in-one microLED display is a monumental achievement by Porotech. Mass-produced microLEDs will be pivotal for the future of displays, particularly the emerging AR and VR spaces. Our technology has solved a fundamental technical and engineering problem facing microLED display quality, manufacturability, and – most importantly – system integration."

"This doesn't just herald widespread adoption of consumer-grade MR, VR, and AR. In fact, DPT also offers radical improvements in TV, signage, and smart wearables in both consumer and professional contexts. By allowing pixels to move beyond RGB and quadrupling the resolution of any given display, DPT is set to unlock new uses for displays in every segment of society."

First III-V commercial foundry for Spain

A NEW state-of-the-art foundry for III-V-based photonics is planned to be operational in Spain late 2023.

SPARC (III-V Semiconductor Foundry and Advanced Photonics Research Centre) will be Spain's first commercial III-V foundry. Based in Vigo, it will have a 1,600 m^2 cleanroom for wafer production, and a research centre that will assist customers in bringing fully-certified photonic products to the market. SPARC aims to capitalise on the potential of III-V semiconductors (GaAs, InP, GaN,..) to accommodate the increasing number of markets and applications that rely heavily on light, photonics and high-speed electronics.

SPARC intends to address a large customer base across a wide range of different markets, including optical communications, displays, lighting, aerospace, automotive, biomedical, sensing, and quantum technologies, as well as high-speed- and/or high-power electronic applications.

STMicroelectronics to make SiC substrates in Sicily

First-of-a-kind SiC epitaxial substrate manufacturing facility in Europe

STMICROELECTRONICS will build an integrated SiC substrate manufacturing facility in Italy to support the increasing demand from ST's customers for SiC devices across automotive and industrial applications as they transition to electrification and seek higher efficiency. Production is expected to start in 2023, enabling a balanced supply of SiC substrates between internal and merchant supply.

The SiC substrate manufacturing facility, built at ST's Catania site in Sicily alongside the existing SiC device manufacturing facility, will be a first of a kind in Europe for the production in volume of 150 mm SiC epitaxial substrates, integrating all steps in the production flow. ST is committed to develop 200 mm wafers in the next future.

This project is a key step in advancing ST's vertical integration strategy for its SiC business. The investment of €730 million over five years will be supported financially by the State of Italy in the framework of the National Recovery and Resilience Plan and it will create around 700 direct additional jobs at full build-out.

ST's high-volume STPower SiC products are currently manufactured in its fabs in Catania and Ang Mo Kio (Singapore). Assembly and test are done at back-end sites in Shenzhen (China) and Bouskoura (Morocco). The investment in this SiC substrate manufacturing facility builds on this expertise and is a significant milestone on ST's path towards reaching 40 percent internal substrate sourcing by 2024.

"ST is transforming its global manufacturing operations, with additional capacity in 300 mm manufacturing and a strong focus on wide bandgap semiconductors to support its $20+billion revenue ambition. We are expanding our operations in Catania, the centre of our power semiconductor expertise and where we already have integrated research, development and manufacturing of SiC with strong collaboration with Italian research entities, universities and suppliers," said Jean-Marc Chery, president and CEO of STMicroelectronics.

"This new facility will be key to our vertical integration in SiC, reinforcing our SiC substrate supply as we further ramp up volumes to support our automotive and industrial customers in their shift to electrification and higher efficiency".

Next stop for InP: consumer applications?

THE InP market, dominated by datacom and telecom applications, is expected grow from $2.5 billion in 2021 to around $5.6 billion in 2027 driven by: high-data-rate modules, above 400G; by big cloud services; and national telecom operators requiring increased fibre-optic network capacity.

But, according to Yole Intelligence, consumer applications will be the next showcase for the InP industry, with a 37 percent CAGR between 2021 and 2027. "There has been a lot of speculation on the penetration of InP in consumer applications. The year 2022 marks the beginning of this adoption. For smartphones, OLED displays are transparent at wavelengths ranging from around 13xx to 15xxnm, " said Ali Jaffal, technology and market analyst at Yole Intelligence.

OEMs are interested in removing the camera notch on mobile phone screens and integrating these 3D-sensing modules underneath the OLED displays. In this context, they are considering moving to InP edge-emitting lasers to replace the current GaAs VCSELs. However, such a move is not straightforward from cost and supply perspectives.

Yole Intelligence noted the first penetration of InP into wearable earbuds in 2021. Apple was the first OEM to deploy InP SWIR proximity sensors in its AirPods 3 family to help differentiate between skin and other surfaces. This has been extended to the iPhone 14 Pro family.

The leading smartphone player has also changed the aesthetics of its premium range of smartphones, the iPhone 14 Pro family, reducing the size of the notch at the top of the screen to a pill shape. To achieve this new front camera arrangement, some other sensors, such as the proximity sensor, had to be placed under the display.

The impact of an innovative company like Apple adding such a differentiator to its product significantly affects companies in its supply chain, and vice versa.

Traditional GaAs suppliers for Apple's proximity sensors could switch from GaAs to InP platforms since both materials could share similar front-end processing tools. Yole Intelligence certainly expects to see new players entering the InP business as the consumer market represents high-volume potential.

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Oxford Instruments and ITRI develop novel GaN architecture

Energy efficient GaN MISHEMT technology allows critical transistor components to operate at higher voltages

OXFORD INSTRUMENTS alongside its research partner Industrial Technology Research Institute (ITRI) has developed a new GaN HEMT device architecture, defined by a recessed and insulated gate junction into the AlGaN layer. The new device is called a GaN MISHEMT.

The technology developments allow critical transistor components to operate at higher voltages to increase performance and reliability, while also achieving a safer and more energy efficient (normally off 'E-mode') operation compared to existing devices.

Oxford Instruments Plasma Technology and ITRI started their collaborative research programme for 'next-gen' compound semiconductors in 2021. This latest breakthrough comes from that partnership. In the meantime, Oxford Instruments unveiled an exclusive supply deal with Laytec, whose endpoint technology is used to control the GaN MISHEMT recess gate depth. Recess depth accuracy and repeatability is critical to tune device performance characteristics.

Klaas Wisniewski, Oxford Instruments' Strategic Business Development director, commented: "We have excellent strategic partners and customers like Enkris, ITRI, LayTec and Rohm, and our GaN solutions are positioned strongly to serve, grow and gain from big opportunity markets. Our leading atomic layer etch and atomic layer deposition technology is raising material engineering performance to achieve new levels of surface quality and defect reduction, to meet the growing demand for higher performing devices."

Klaas also added: "With our technology partner ITRI, high-volume GaN manufacturing customers and our focussed investment into high value and proprietary process solutions, we expect the GaN device market to be a key driver for our business and technology roadmap."

"ITRI has well-established expertise and history in providing GaN HEMT manufacturing solutions that enable the global supply chain for GaN power electronics and RF applications. However, to solve the technology challenges associated with fabrication of next generation devices, we needed more accurate and controlled technology solutions such as atomic layer etch for GaN HEMT high volume manufacturing," commented Robert Lo, deputy general director, EOSL, ITRI.

Through our long standing partnership with Oxford Instruments, we have successfully qualified and integrated their atomic layer etch solution for a recessed gate MISHEMT into our GaN HEMT pilot production line

Klaas Wisniewski presented a talk entitled *Enhancing GaN HEMT Performance for Power Electronics Applications with Atomic Scale Processing Production Solutions* in September at Semicon Taiwan.

World's first inverted gallium oxide DI-MOS transistor

Novel Crystal Technology confirms major progress in the development of gallium oxide power transistors

JAPAN-BASED Novel Crystal Technology (NCT) is reporting the basic operation of a high-breakdown voltage (1 kV) Ga_2O_3 inverted double implanted MOS transistor (DI-MOSFET) with a sufficiently high threshold voltage of 6.6 V. This is believed to be a world's first for β-Ga_2O_3. The details on this development were announced at the 83rd *Japan Society of Applied Physics Autumn Meeting Symposium* on September 21, 2022.

NCT has been aiming to commercialise the β-Ga_2O_3 transistor since 2019.

Until now, normally-off β-Ga_2O_3 transistors have used a fin structure that does not require a *p*-type layer because the *p*-type conductive layer technology has not yet been established. However, the fin must have a fine structure of 0.4 µm or less with good dimensional control. It has been difficult to fabricate large devices such as this with a chip size of several millimeters square with good yield.

In response to this problem, NCT has been developing an inverted MOS channel structure that can be manufactured with high yield even using conventional stepper exposure equipment and dry etching equipment.

Instead of relying on developing the technically challenging β-Ga_2O_3 *p*-type conductive layer, the current development uses a high-resistance β-Ga_2O_3 layer doped with nitrogen as an acceptor impurity and a well layer made through an activation heat treatment. In a mobility evaluation, the fabricated long-channel lateral transistor exhibited a high threshold voltage of 6.2 V, which could not be achieved with a fin structure, and a higher MOS channel mobility (52 $cm^2 V^{-1} s^{-1}$) than that of a device made from SiC.

NCT will analyse the characteristics of the nitrogen-doped β-Ga_2O_3 high-resistance layer in the prototype inverted MOS transistor as part of the project commissioned by the Acquisition, Technology & Logistics Agency. In addition, it will conduct trial production on a 4-inch mass production foundry line, improve the device characteristics, and ensure reliability. It will also proceed with the development of a full β-Ga_2O_3 power module combined with a Ga_2O_3 Schottky barrier diode that is now being commercialised.

ITRI and Ganvix extend GaN VCSEL venture

ITRI has announced a continued partnership with Ganvix, a company developing GaN VCSELs. The two parties completed the development of the first blue GaN lasers and signed a phase II agreement to extend their joint venture.

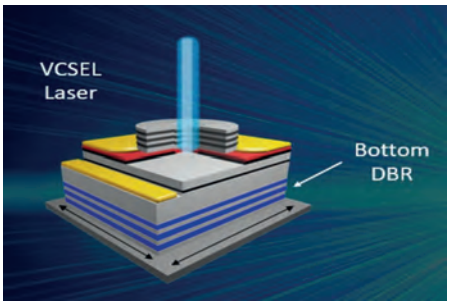
GaN VCSELs operating in the blue wavelength range has been demonstrated successfully, based on the close collaboration between Ganvix's design and ITRI manufacturability. The next phase of development under the agreement will include expanding the wavelength range from blue to green; qualification testing; and packaging of discrete lasers and laser arrays.

Ganvix uses nano-porous technology to deliver compact, lightweight blue/green/UV VCSEL lasers that produce superior wavelength control, smaller spot size, and array architectures, allowing substantial innovation across a wide range of applications.

ITRI will continue to apply its substantial capability and infrastructure for the manufacture of electro-optic devices to accelerate Ganvix's time to market. The resulting products will address the nascent opportunity for high-performance and low-cost GaN VCSELs in the billion-dollar global markets.

GaAs VCSELs that operate in the infrared spectrum are one of the fastest-growing technologies in electro-optics today. However, GaAs cannot emit light in the ultraviolet or visible. For these applications, GaN is required, but there has been no commercially viable solution to form the laser cavity mirrors required until now. Ganvix has solved this problem, using nano-porous technology to engineer the optical properties of GaN.

"For future metaverse application, the three-primary-colour VCSELs will play a key role," commented Shih-Chieh Chang, general director of ITRI's Electronic and Optoelectronic System Research Laboratories. "We are very happy to continue to deepen the cooperation with Ganvix and launch commercialised products, which can also drive Taiwan's industries to enter the metaverse market," he said.



"We are excited to announce the successful demonstration of blue VCSEL lasers," said John Fijol, CEO of Ganvix. "This marks a critical achievement, enabling commercialisation of these new laser devices. We look forward to the next phase of our relationship working with ITRI to bring these devices to market."

Toray and A*STAR collaborate on SiC heat dissipation

Joint research to develop practical applications for high heat-dissipating adhesive sheets for SiC power semiconductors

TORAY INDUSTRIES and A*STAR's Institute of Microelectronics (IME) in Singapore have begun joint research to develop practical applications for high heat-dissipating adhesive sheets for SiC power semiconductors.

Prospective applications include automobiles, smart grids and data centres. In particular, from the viewpoint of further energy conservation, SiC power semiconductors are being applied more extensively for automotive applications.

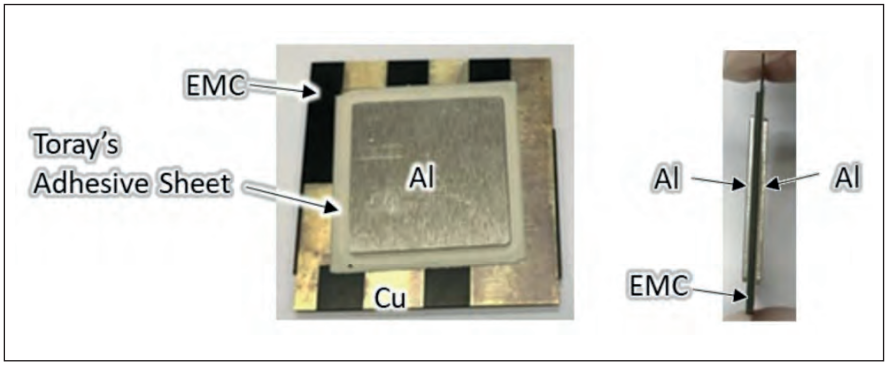
Development efforts will combine Toray's material and fabrication technologies with IME's design, prototyping and evaluation technologies. This will improve the simplicity and reliability of processes to apply high-heat-dissipating adhesive sheets and enhance semiconductor quality, dependability, and safety.

Toray and IME aim to provide comprehensive solutions to SiC device manufacturers and contribute to the uptake of high-efficiency SiC power semiconductors.

Toray will promote this joint research with support from the new Toray Singapore Research Centre (TSRC, a department of Toray International Singapore Pte Ltd), which opened in Singapore in June of this year.

Toray offers electro-coating materials such as Semicofine non-photosensitive polyimide and Photoneece photosensitive polyimide that employ proprietary molecular design technology as well as FALDA adhesive film. Semiconductor, electronic component, and display manufacturers rely heavily on these products because of their high reliability.

Since 2016, Toray has participated in several international consortiums on IME's advanced semiconductor packaging, deepening collaboration and achieving results through joint research.



Toray and IME previously collaborated to develop a robust SiC power semiconductor module that incorporates high-heat dissipation adhesive sheets from the FALDA lineup. General heat-dissipating adhesive materials using grease and solder have a large contact thermal resistance with the cooler, resulting in failure due to inadequate cooling of the semiconductors.

Toray and IME resolved these problems by applying Toray's material to create the first prototype of a new SiC power semiconductor module using a heat-dissipating adhesive sheet with a very low contact thermal resistance, which is lower than conventional products. Durability tests at high temperatures confirmed that the module lasted for a significantly large number of power cycles.

In this joint research, Toray and IME will continue to prototype and evaluate devices to improve the simplicity and reliability of processes to employ high-heat-dissipating adhesive sheets in the drive for commercialisation.

Yuichiro Iguchi, corporate VP of Toray's Research Division, commented: "We have long respected IME's prowess in SiC power semiconductor design and evaluation technology. We're delighted to collaborate with Singapore's government agencies on such public-private R&D projects. We look forward to accelerating efforts to overcome the challenges of applying advanced heat dissipation technology to enhance energy efficiency and help drive to sustainable economic growth."

Terence Gan, executive director of A*STAR's Institute of Microelectronics, said: "We are pleased to team up with Toray to spur greater innovation in SiC power semiconductors. Our mutual capabilities come together in a complementary fashion to enable the co-development of novel heat-dissipating solutions. Toray's R&D presence in Singapore will also help build a stronger R&D ecosystem in this part of the world."

UV LED manufacturing breakthrough

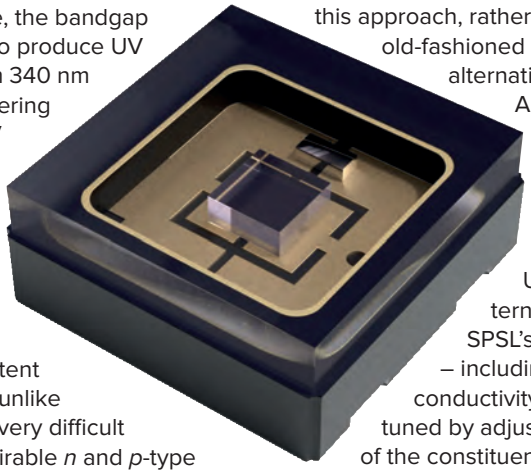
Silanna says its short period superlattice approach allows easy wavelength tuning, higher power at short wavelengths, and exceptional lifetime performance

SILANNA UV says that a breakthrough in UVC LED technology offers advantages for applications as diverse as disinfection, water quality monitoring, gas sensing, liquid chromatography, and chemical and biological analysis.

The Australian company say its new manufacturing approach promises to make deep ultraviolet and far ultraviolet LEDs easier to make, more efficient at shorter wavelengths, and more reliable.

Silanna UV's patented short period superlattice (SPSL) approach is claimed to overcome many of the difficulties that plague competing AlGaN UVC LED technologies. In essence, Silanna UV has effectively created a new material, a nanostructure, which is much easier to control and has properties that are far superior to traditional AlGaN. The benefits for UVC LED quality are revolutionary, according to the company.

For years, UVC LED manufacturers have relied on traditional AlGaN formulas. In theory, by adjusting the ratio of aluminium to gallium in the alloy lattice, the bandgap can be tuned to produce UV emissions from 340 nm to 210 nm, covering most of the UV spectrum.

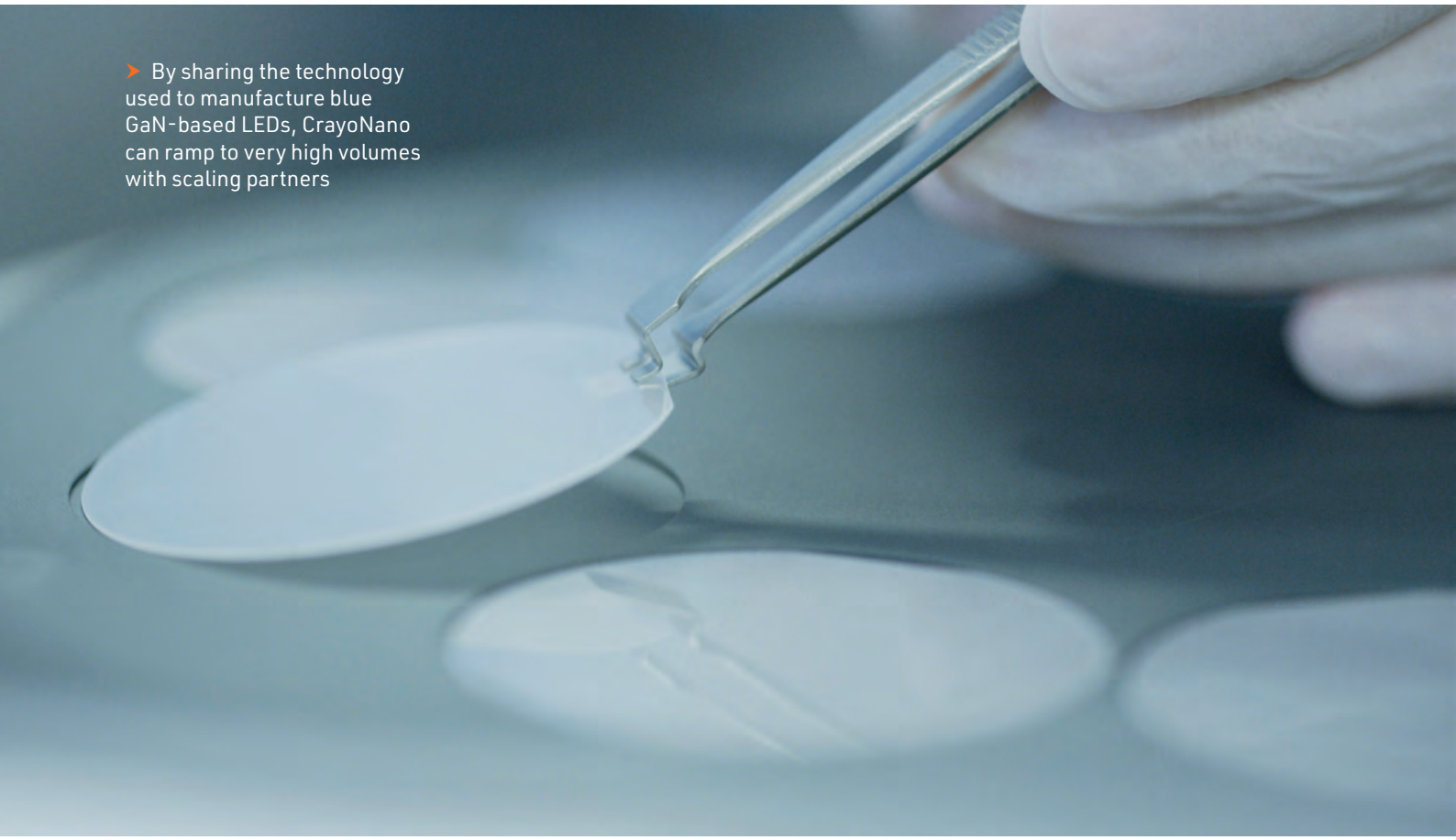


But in reality, emission below 260 nm requires high aluminium-content AlGaN, which, unlike GaN, makes it very difficult to achieve desirable *n* and *p*-type doping, particularly at the shortest wavelengths, leading to poor electrical performance. High-aluminium content AlGaN also suffers from light extraction issues due to the polarization of emitted light, causing significant loss of light output, particularly in the far UV range below 240 nm.

To overcome these problems in UV LEDs, Silanna UV uses new technology. Instead of the common AlGaN method, Silanna UV uses a SPSL. In this approach, rather than using an old-fashioned ternary alloy, alternating layers of AlN and GaN (as many as several hundred layers) are meticulously built up to create a so-called SPSL. Unlike a traditional ternary alloy, this SPSL's key properties – including bandgap and conductivity – can be finely tuned by adjusting the thickness of the constituent layers.

"This means that the issues caused by High-aluminium content AlGaN are mitigated – in particular, that older method's poor electrical characteristics and short wavelength light-loss."

Silanna says its SPSL technology gives major advantages over UVC LED competitors, including the maintenance of high power at shorter wavelengths, superior electrical properties, and outstanding lifetime performance.



By sharing the technology used to manufacture blue GaN-based LEDs, CrayoNano can ramp to very high volumes with scaling partners

Deep-UV LEDs: Start-up seeks success with a fab-lite focus

A Norwegian start-up looks to prosper in the deep-UV LED market with reliable, packaged emitters

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

THE RAZOR-THIN margins facing makers of visible GaN-based LEDs has ensured that this market is anything but a happy hunting ground for start-ups. But fledgling firms with interest in this area do have the tantalising prospect of significant, lucrative success, if they can produce variants that provide emission in the deep UV.

That's the market being pursued by fab-lite firm CrayoNano, which has already raised €30 million and has the opportunity access on another €5 million, if necessary. Based in Trondheim, Norway, this spin-out of the Norwegian Technology University has established product design and processing facilities at its head-quarters and in Taiwan, and developed a production process for making high-performance UVC LEDs that can be undertaken in any high-volume fab that makes GaN-based LEDs.

The company's first product line, the CrayoLED, draws on fundamental research and IP conducted into graphene and GaN-based nanowires. While details of this technology are currently under wraps – more will be said in 2023, via an exclusive feature in *Compound Semiconductor*, so watch this space – CrayoNano is willing to discuss the performance of its deep-UV LEDs, its fab-lite strategy, and the market opportunities for its packaged emitter.

According to Michael Peil, CrayoNano's Chief Revenue Officer, although the company's debut product, which has been developed in cooperation with key customers, doesn't break any records, it is

a strong allrounder with an impressive performance on many fronts.

The company's debut product, the H-Series (CLH-N3S) LED, emits at 275 nm. Targeting water purification, but also suitable for air and water purification, it has an output power of 80 mW. That's towards the upper end of the range for commercial high-power UV LEDs on the market – they span around 40 mW to 100 mW.

"Some products have a higher output power but much less lifetime," points out Peil, who adds that to ensure customer confidence in the lifetime numbers that CrayoNano quotes, it uses a third party with an accredited measurement lab to provide this crucial piece of information. There are promising signs from the initial data that the lifetime, based on the time it takes for the output to fall from its initial value by 30 percent, is typically more than 10,000 hours. That's sufficiently long to enable success in the marketplace.

CrayoNano has carefully considered the processing and production that it employs for its packaged UVC chip. "You need to have a high-transparency, endurable packaging technology," argues Peil. "You can go cheap, but that doesn't serve the purpose of having a long-life requirement."

The packaged CrayoLED H-Series UVC LED features a high-thermal-conductivity ceramic to minimise the junction temperature, and optical materials that combine minimal degradation with the ability to direct the emitted light at its intended destination.

Peil claims that many of the suppliers of UVC LEDs struggle to scale to the high volumes required to unleash a multi-billion-dollar market for this class of device. "[Deep-UV LEDs] need to be produced in hundreds of millions, if not billions of pieces."

The company's fab-lite strategy can deliver these volumes. The CrayoNano fab in Taiwan is capable of ramping production to tens of millions of chips – and once that capacity can no longer meet orders, additional production will be provided by several scaling partners, such as SemiLEDs, thanks to the compatibility of the company's approach with blue-chip MOCVD technology.

"That gives us the possibility to keep cap-ex requirement low, and to diversify the technology," comments Peil, who reveals that CrayoNano's long-term ambitions in the semiconductor industry are not limited to LEDs.

Covid's legacy

A capability to kill the Covid-19 virus fuelled tremendous interest in the deep-UV LED during the height of the pandemic, and spurred rocketing sales.

"Covid was a trigger, not only indicating the need for new technology, but also the requirements for standardisation, to make this a good solution for health applications," remarks Peil.

While we may be transitioning to a world where we live with Covid, new pandemics could emerge, where deep-UV LEDs could have a role to play, including those associated with livestock.

Peil sees the water purification market as an opportunity for fast growth in UVC LED sales. While mercury lamps have a higher efficiency than UVC LEDs – it's typically 15 percent, rather than up to 5 percent – their bulkiness hampers incorporation in systems for purifying tap water at its point of use. With UVC LEDs delivering high energy densities, emission can be efficiently directed to where it's needed to provide disinfection, leading to a higher efficiency at the system level.

Local purification of tap water with a deep-UV LED is very attractive, argues Peil. "If we can avoid chlorine utilisation, the taste is better. For example, you will see application in soft drinks mixers at home."

There's also the opportunity for grey water re-use. This is already being implemented in Japan, a nation with much resource awareness.

Another resource, currently at the forefront of the minds of many, is energy. Traditionally, thermal processes are used for disinfection, but the high electricity bills now being faced in many countries could drive a switch to deep-UV LEDs.

This is but another example of the many market opportunities for CrayoNano, which will grow shipments of deep-UV LEDs with a fab-lite model that has no constraints over capacity.

➤ CrayoNano's first product, the CrayoLED H-Series (CLH-N3S), produces typically 80 mW of optical power at 275 nm, making it an attractive candidate for water purification.

VCSELs: Datacoms will regain the lead

Driven by increasing uptake of streaming services and video calls, sales of the VCSEL to the datacom market are set to soon eclipse those to the consumer electronics sector

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

WITHIN OUR INDUSTRY, the norm is for sales of a particular device to progress from one application to another. Take, for example, the LED. Its first killer application came from backlighting the screens and the keypads of mobile phones, before a subsequent substantial hike in revenue came from backlighting larger screens – notebooks, laptops and TVs – and sales swelled again when this emitter replaced incandescent and fluorescent lightbulbs.

The VCSEL, however, is on a very different trajectory. According to Yole Intelligence, part of Yole Group, datacoms will soon return to being the largest application for the revenue of this device, following the current period when lion's share of sales is coming from the consumer electronics sector, thanks to deployment of this class of laser in the smartphone. The French market analyst is forecasting sales of VCSELs to the datacom market to grow at a compound annual growth rate (CAGR) of 22 percent over the next five years, to hit $2.1 billion by 2027. In comparison, revenue from the consumer electronic sector will increase at a CAGR of 16 percent, to reach $1.7 billion.

➤ Video-calling is contributing to rising sales of VCSELs to the datacoms market.

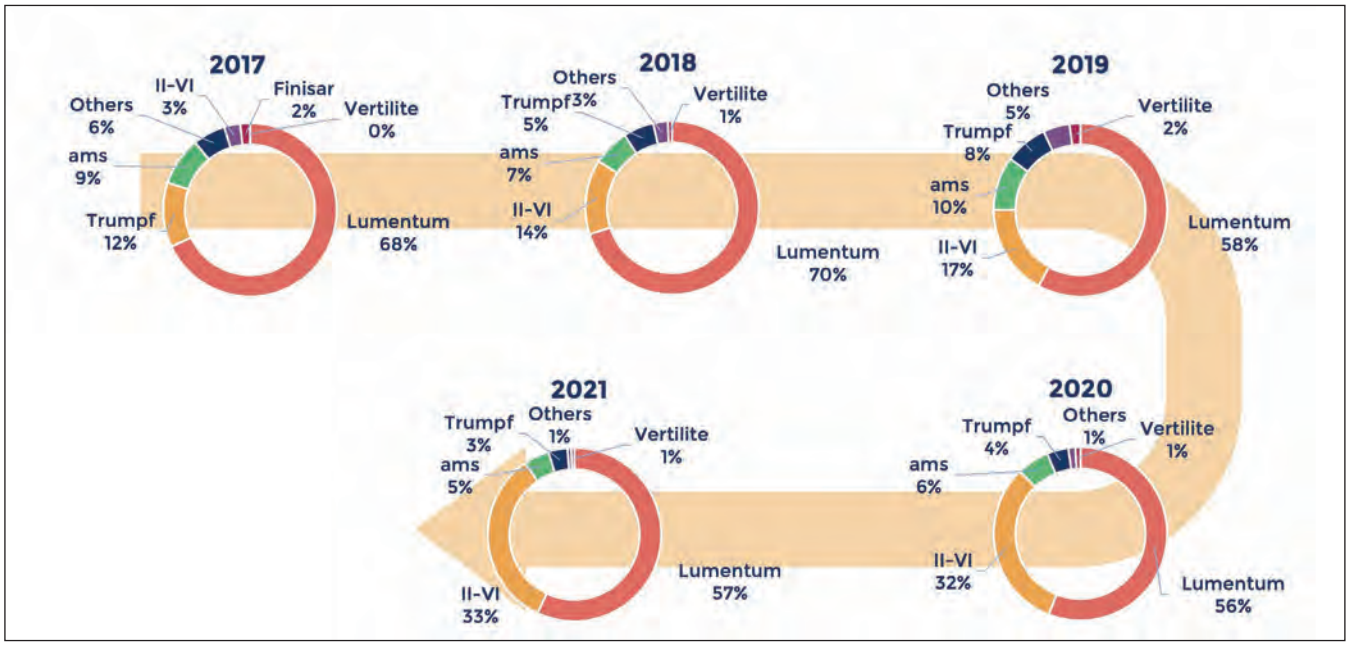
Deployment of the VCSEL in the smartphone can be traced back to the launch of the iPhone X in Fall 2018. That ground-breaking model incorporated a VCSEL for the dot projector, and another for the flood illuminator.

"Then we saw Android players, like Huawei, Xiaomi, and so on, introduce 3D recognition into the smartphone," explains Pierrick Boulay's, Senior Technology & Market Analyst in Yole Intelligence's Photonics and Sensing Division.

According to Boulay, a key difference between Apple and its competitors is the way that it employs the VCSEL. Apple uses a structured light approach, while its rivals have employed time-of-flight technologies to avoid any potential IP issues.

These makers of Android phones are now tending to ditch the VCSEL, as they launch new models that tap into 5G networks. The latest communication standard is impacting the smartphone's limited budget, with components for processing and providing 5G signals causing a significant rise in the bill of materials associated with the RF front-end. Something has to give, and VCSELs are being discarded, replaced with software that offers a similar user experience.

Apple's smartphones now incorporate a small VCSEL for the proximity sensor, and a pair of them for the face ID – one provides the flood illuminator and another the dot projector. With the tech giant's



smartphone shipments steady, and an inevitable decline in chip prices with time, VCSEL sales for this particular application are expected to remain stable.

But sales to the consumer electronics sector will still increase, thanks to the deployment of the VCSEL in other products. "I've been told recently that the latest Apple watch is embedding a VCSEL inside," remarks Boulay, who says that this class of laser may also be used in laptops, to provide identification.

Initially, Lumentum provided Apple with all the VCSELs for its smartphones. But to reduce supply chain risk with a second source, Apple encouraged Finisar to become a VCSEL supplier, promising orders totalling $390 million. The US manufacturer grabbed this opportunity, and over the intervening years its VCSEL production business has been acquired by II-VI and subsequently incorporated into Coherent, which now has a similar share of the market to Lumentum (see Figure).

While Lumentum and Coherent dominates sales of the VCSEL to the consumer electronics sector, they don't have the same grip in the datacoms market, which Boulay describes as "really fragmented". Other companies competing for sales include Trumpf, Sony and Broadcom, as well as Seoul Semiconductor, which initially established itself as a provider of LEDs, before expanding its optoelectronic products portfolio.

Boulay says that the rapid increases in sales of VCSELs to the datacom market is being driven by heavy data-consuming applications, such as Amazon. "There are also video games, on-line shopping, and social networks with more video content: Instagram, WhatsApp and so on."

A few years ago, it seemed that the next killer application for the VCSEL would be lidar for autonomous vehicles. But now that's looking less likely, warns Boulay.

"The Uber accident a few years ago really put a stop to the development of the taxi. The integration of lidar in ADAS vehicles is today limited to high-end vehicles, and that means low volumes."

For the autonomous vehicle market, makers of VCSELs are having to compete with those providing fibre lasers and edge-emitting lasers. It is the latter that is out in front, with a market share of around 70-75 percent.

However, this might be eroded by the development of VCSELs with multiple junctions between the mirrors to boost output. High powers, allied to a small size, has led some companies in China to develop lidar systems incorporating VCSELs alongside detectors with a high degree of sensitivity, such as single-photon avalanche photodiodes and silicon photomultipliers.

Another potential battleground for makers of VCSELs and edge-emitters is tomorrow's OLED-based smartphones. These models are to feature superior aesthetics, realised with either a smaller notch or no notch at all. If they incorporate a laser, it will need to operate at around 1400 nm, to ensure its emission is transparent to the organic material. Two leading candidates for this source are an InP edge-emitting laser and a dilute-nitride VCSEL.

Sales of the latter are unlikely to make much of a contribution to the total VCSEL revenue over the next five years, which is forecast to climb to $3.9 billion. That's a very healthy figure that's good news for the manufacturers of this device, along with the producers of substrates, material sources and growth tools that support their efforts.

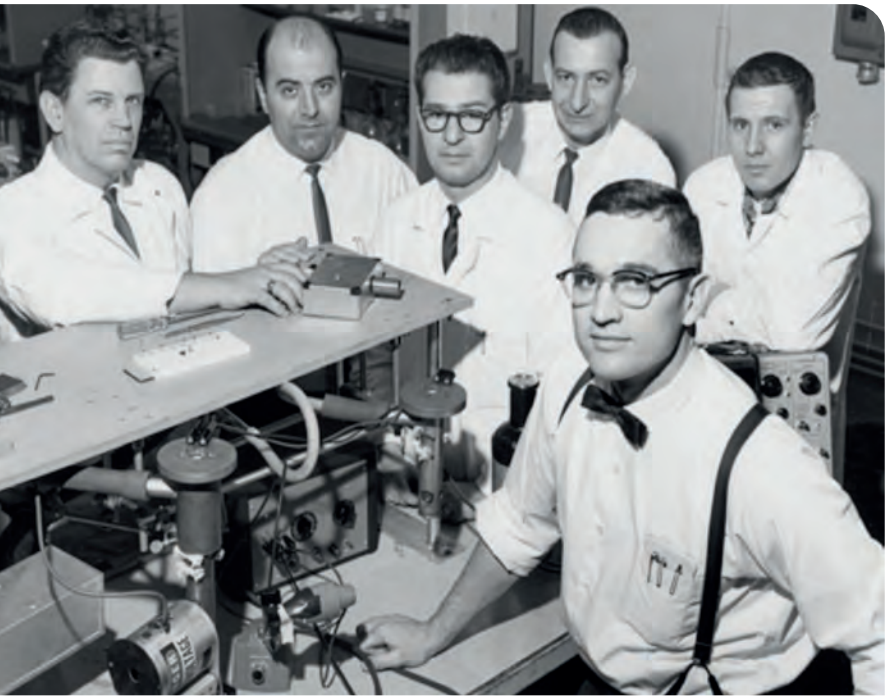
➤ Yole Intelligence has tracked the changes in the market share held by makers of VCSELs in the mobile and consumer sector.

The legacy of Professor Nick Holonyak, Jr.

We take a look back at the life of a trailblazer, whose inventions included the visible LED and many forms of semiconductor laser

BY MIKE KRAMES FROM ARKESSO AND RUSSELL DUPUIS FROM GEORGIA INSTITUTE OF TECHNOLOGY

'PIONEER' AND 'VISIONARY' are often overused today, but both of these terms are accurately applied to Professor Nick Holonyak, Jr. This ground-breaking academic – fondly called just 'Nick' by his friends, colleagues and sixty PhD graduate students at the University of Illinois at Urbana-Champaign (UIUC) – was not only a very innovative and hard-working scientist and engineer, but also a role model for his students for his perseverance, his ability to create new and exciting results from a modest laboratory not stocked with a lot of advanced equipment, and his making sure that the graduate students got adequate credit for their work. Holonyak's pioneering work in semiconductor materials and devices underpins much of the internet, lighting, telecom, visual displays, as well as the face-recognition systems, e.g., 'Face ID', and high-efficiency power device technologies being developed today.



➤ Nick Holonyak and his research team in the GE Syracuse Lab with the apparatus for testing visible red laser diodes in about 1962. Courtesy: GE.

His many innovations include the first ternary compound semiconductor epitaxial layers, the first III-V heterojunctions, the first ternary LED and laser diode, and the first III-V quaternary and quaternary laser diodes. In addition, he is to thank for creating the first processes for producing: a stable III-V semiconductor native oxide, impurity-induced layer disordering, quantum-well laser diodes, the transistor laser and various silicon-based technologies.

Holonyak was the first graduate student of two-time Physics Nobel Prize winner John Bardeen. Holonyak began his doctoral studies at UIUC under Bardeen in 1951, after completing his BSEE degree at that university in 1950. He graduated with his PhD in 1954 and joined Bell Telephone Labs in Murray Hill NJ, where he worked on developing the first silicon diffused-junction devices. Declining to seek a draft deferment, he was drafted into the US Army in 1955 and served in the US Army Signal Corps until to 1957. On leaving, he joined General Electric Company (Syracuse NY), where he worked on power and signal *p-n-p-n* devices (including the invention of the shorted-emitter; the symmetrical silicon-controlled rectifier; and thyristor switches, such as triodes for alternating currents).

While at GE, between 1960-1963 Holonyak developed the first visible-spectrum LED and laser diode, a red-emitting *p-n* junction fabricated from the first III-V semiconductor ternary device, based on GaAsP. In 1963, he predicted that ultimately the world would have white LEDs – a surprising and remarkable statement at that time.

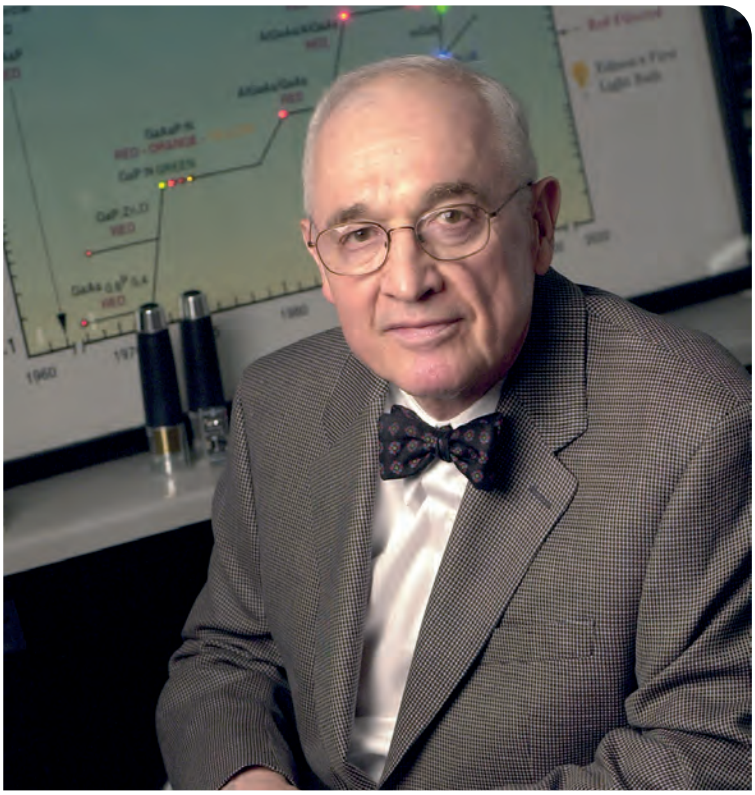
Holonyak joined UIUC as a Full Professor in the Electrical and Computer Engineering department in 1963 at the invitation of John Bardeen. In 1970, Holonyak and his students developed the first quaternary III-V alloy in order to improve laser diode performance. His group also developed the first quantum-well laser diode in 1977, and demonstrated room-temperature operation of these devices in 1978. Other significant contributions

from his team have included advances in III-V laser diodes and III-V materials, such as impurity-induced disordering (1981), native oxide formation (1990), and a collaboration on the development of the transistor laser (2004).

This trailblazer was an active teacher and researcher for 50 years until his formal retirement in 2013, when he became Professor Emeritus. He continued to make technical contributions after his retirement, expanding his publications to over 600 technical journal articles. He also holds over 60 patents. Over many decades, recognition for his contributions has come from numerous award (see "Acknowledging Holonyak's tremendous contributions").

Holonyak's background was a humble one. He was born in southern Illinois, the son of a coal miner, an immigrant from the Carpathian Mountains in Ukraine. As a boy he had a keen interest in all things electrical and mechanical, fueled by insatiable curiosity. He worked on the railroad for a time during high-school summer 'vacations', which inspired him to find a career that would utilize his mind rather than his back.

Holonyak had an incredible way of educating and mentoring his graduate students, a method developed in the twentieth century that seems out of place today in the age of the internet, yet was so powerful and effective. Holonyak was in the department every day, six days a week – or sometimes even seven. He would be either in the lab, his office, the library, or the gym (Nick was quite physically active). He would have impromptu coffee 'sessions', one each morning and afternoon. In these, students who were available would gather around him, and he would quickly launch into a story, or series of stories. They were often detailed tales of past work and/or people (such as John Bardeen). This was not abstract storytelling, but insight that would inevitably address one or more of the issues one of the current students was having with a project in the lab. Holonyak would have picked up the problem just by walking around, and paying attention, not addressing it directly, but instead through storytelling that was not only a highly engaging way to address issues but a form that educated everyone present simultaneously. And he did this twice a day, every day: more than two thousand sessions per student. One graduate recently remarked after hearing of Holonyak's passing: "Those coffee times gave me more insight to how to be an engineer than all the 6 years I was at U of I."



Nick Holonyak in 2002 with a diagram showing the development of visible LEDs since 1962. Courtesy: UIUC.

Many of Holonyak's PhD students have gone into academia or leadership roles in technology industries, so his legacy continues to expand through their many generations. There is no doubt his contributions will continue to create value and further improve the lives of many people on this planet. He is missed greatly.

ACKNOWLEDGING HOLONYAK'S TREMENDOUS CONTRIBUTIONS

Holonyak's many awards include the:

- IEEE Jack A. Morton Award (1981)
- Electrochemical Society Solid State Science and Technology Award (1983)
- Sigma Xi Monie A. Ferst Award (1988)
- IEEE Edison Medal (1989)
- Charles Hard Townes Award of the Optical Society of America (1992)
- American Electronics Association 50th Anniversary Award (1993, "Inventing America's Future")
- National Academy of Sciences Award for the Industrial Application of Science (1993)
- American Society for Engineering Education Centennial Medallion (1993)
- Vladimir Karapetoff Eminent Members' Award of Eta Kappa Nu (1994)
- TMS John Bardeen Award (1995, The Minerals, Metals, and Materials Society)
- 2000 IEEE Third Millennium Medal, Frederic Ives Medal of the Optical Society of America (2001)
- U.S. National Medal of Technology (2002)
- U.S. National Medal of Science (2003)
- IEEE Medal of Honor (2003)
- NAE Chares Stark Draper Prize (2015)
- Benjamin Franklin Medal of the Franklin Institute (2017)
- Queen Elizabeth II Prize in Engineering (shared with four other colleagues, 2021)

Hitting the road running

The world's first dedicated, open, pure-play 150 mm SiC wafer foundry offering a fast route to market has already established a rapidly filling order book

BY DAVID CLARK AND RAE HYNDMAN FROM Clas-SiC

AS DEMAND for SiC devices and materials continues to grow, there is much need for SiC wafer foundry services. Helping to address this is our team at Clas-SiC Wafer Fab, the UK's only production volume SiC wafer foundry. Our activities span 'process design kit (PDK)' orders – including MOSFETs, junction barrier Schottky (JBS) diodes and merged *p-i-n* Schottky (MPS) diodes – to recent collaborative projects with major automotive industry players. Within those activities, we are continuing to enhance our capabilities, to ensure our market leadership in technology, quality, and speed. All of this is being realised with impeccable timing – just as the market for SiC power devices is taking off.

The origins of our company can be traced back to the vision of our founder, CEO and former Chairman of the Board of II-VI, Carl Johnson. In 2017 he led the incorporation of our company, which has been

founded to provide a ready-made capability for rapid prototyping of new SiC devices in a low-to-medium-volume wafer fab. By succeeding in this endeavour, we are enabling new market entrants to make a speedy journey from custom device design to device fabrication, aided by our established and experienced team offering proven technology.

Since our founding we have made great progress, beginning with the construction, from scratch, of a SiC-dedicated wafer fab in Lochgelly, a town located on the outskirts of Edinburgh. The nucleus of our management and engineering team has come from a nearby wafer fab that closed in 2017. Over 30 years that 100 mm fab manufactured millions of silicon devices for high-reliability automotive, rail, fire safety, and medical applications – and from 2004 it processed SiC wafers. With full qualification to ISO9001 and ISO TS16949 standards, that 100 mm fab has equipped us with a unique, experienced pedigree – qualities rarely found in a start-up.

Due to this envious heritage, our company is more re-start than start-up, but from the ground up, in a new facility with new tooling.

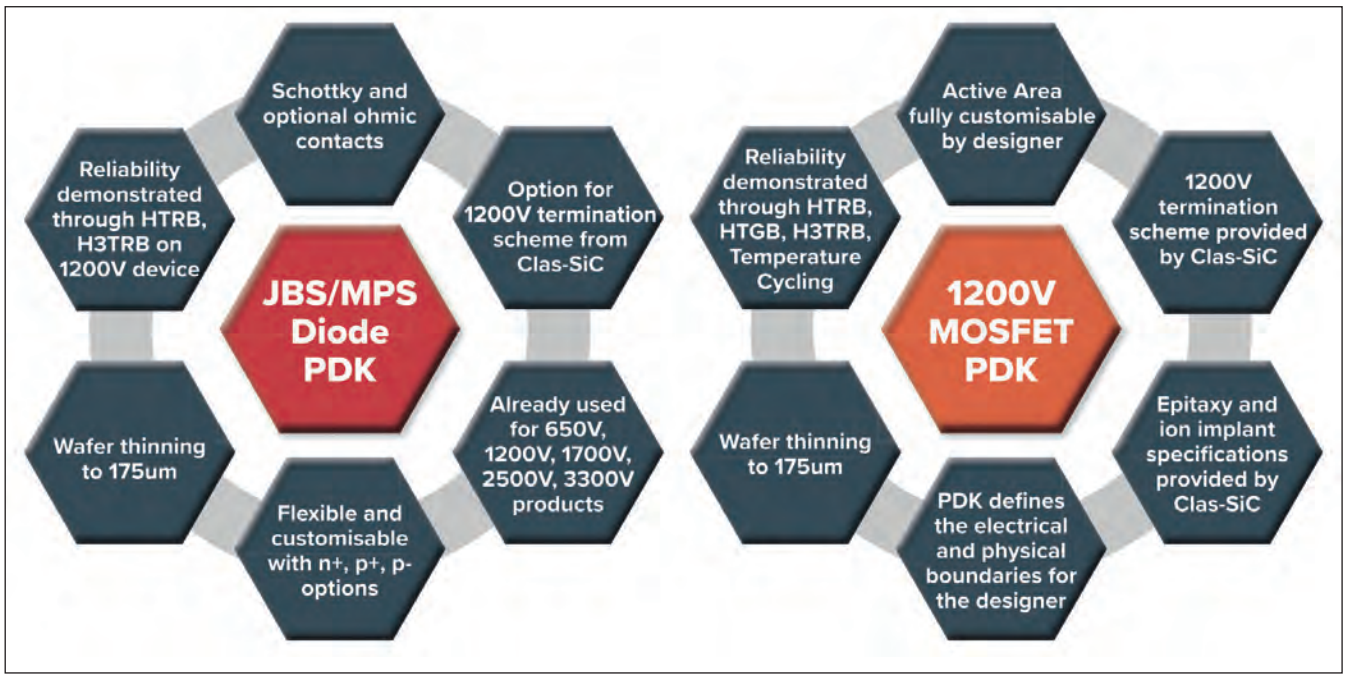
Even so, we still had to build a new wafer fab from scratch. That's a major undertaking, which began by identifying and procuring suitable industrial units. Significant new-build expansion followed, providing additional cleanroom space and facilities that enabled us to almost double our original floor space. We have populated this with brand-new facilities, meeting all modern safety standards. These facilities support the tool set and meet the ISO class 5 cleanroom requirements for SiC device fabrication. Started in 2017, we completed this project in 2019.

A full tool set

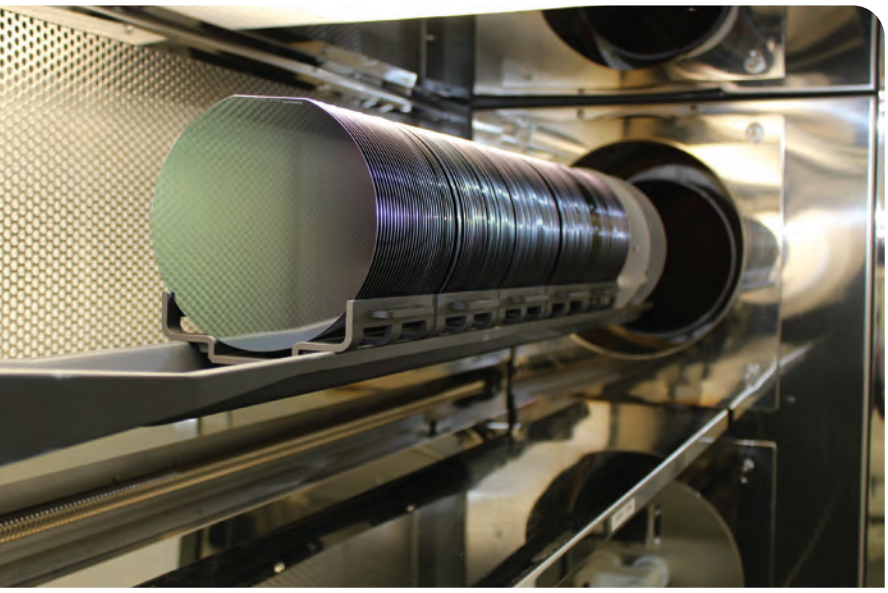
During our build we made rapid progress relating to the detailed specifications for, and procurement of, our wafer fabrication tool set. We decided to adopt a large number of tools from the silicon industry, employing well-known 'workhorse' equipment from previous silicon technology nodes. Many of these tools are supported by local vendors, from what was once fondly known as 'Silicon Glen'. We have upgraded these tools so that they can handle transparent SiC substrates, rather than the highly-reflective silicon substrates they were designed to process. We have also made significant investment in additional SiC-specific tooling, including a state-of-the-art high-temperature SiC ion implanter, and a high-temperature implant annealing furnace. This has given us the capability to fabricate SiC power devices from incoming epiwafers, using processes that include wafer-thinning, backside-metallisation and laser-annealing.

We also made investment in wafer-level testing such that we can carry out blocking tests up to 10 kV and conduction-mode tests up to 500 A. Our state-of-the-art testers and automatic probers facilitate rapid testing. We also have reliability testing ovens for high-temperature reverse-bias and high-temperature gate-bias (HTGB) tests that validate our processing platforms.

Following our tool procurement, we entered a comprehensive engineering phase involving tool acceptance, qualification and formal certification. We demonstrated planar SiC Schottky diode capability in 2020, followed by the more difficult demonstration of the planar MOSFET capability early in 2022.



➤ Figure 1. Clas-SiC offers Process Design Kits to customers, enabling them to successfully produce custom devices on diode and MOSFET platforms.



Our philosophy has been to employ a reference 15 A, 1200 V MPS diode and a reference 80 mΩ, 1200 V MOSFET as the two vehicles to demonstrate the functionality and reliability of our process platforms. Both reference device types have successfully completed a full suite of rigorous, JEDEC-like reliability testing (see Table 1 for details). Drawing on this proven technology, we have assembled and published PDKs. Our customers are using them to produce custom devices on our diode and MOSFET platforms (see Figure 1 for a summary).

Speeding to market with PDKs

Designers using our 1200 V MOSFET PDK are able to employ their full innovation to customise the active area of their devices. We provide a 1200 V termination scheme, along with all the processing details. To assist the designer, our PDK includes a Design Rule Manual and Design Rule Check deck.

The PDK is incredibly flexible. It has even allowed one designer to successfully embed multiple sensors within their MOSFETs.

A common customer strategy is to design a multi-project wafer (MPW) mask set. This allows simultaneous fabrication and assessment of many design variations, such as planar, orthogonal and hexagonal architectures.

Thanks to our comprehensive offering, all processing takes place on a common platform, with standard processes and modules. This results in minimal non-recurring engineering and rapid fabrication of prototype MOSFETs. These devices can be produced within twelve weeks, providing customers the advantageous position of a faster route to market.

Our JBS/MPS diode PDK is even more flexible. Offering 1200 V termination, our diode PDK has also been used to design devices across the 650 V – 3300 V range with fully-customised, high-voltage termination schemes. Like the MOSFET, manufacture

Viewpoint: Clas-SiC founder Carl Johnson

I have been involved in compound semiconductors all my working life. Back in 1971, it was clear to see that the II-VI compound semiconductor materials CdTe, ZnSe and ZnS – along with the elemental semiconductor material diamond and the compound semiconductor material SiC – would be the workhorse optical and electro-optical materials in the infrared region of the electromagnetic spectrum. Based on this view, I co-founded II-VI Incorporated to explore, manufacture and supply the highest quality versions of these selected materials.

In 1998, we awakened to the fact that SiC would become an important electronic material, so II-VI launched an effort to become an important supplier of high-quality 6H and 4H-SiC substrates. II-VI initially supplied 2-inch diameter substrates in 2000, before progressively increasing the size. In 2016 II-VI demonstrated the first 200 mm substrates.

The story of my founding of Clas-SiC dates back to March 2017, when I heard that a company in Glenrothes, Scotland, planned to shutter its silicon/SiC wafer fab. I was on the next flight to Edinburgh. I knew it would be synergistic to hire the highly skilled, experienced team of former employees to establish a rapid prototyping and low-to-medium rate production wafer fab to serve the plethora of fabless SiC power device innovators that were soon to be our customers.

At the outset, Clas-SiC adopted a time-tested set of seven values that I helped to establish at II-VI.

These values, which have guided decision making and culture at Clas-SiC since its inception, are:

- Customers first
- Honesty and integrity
- Open communication
- Teamwork
- Continuous improvement and learning
- Manage by the facts
- A safe, clean, and ordered workplace

We value all our employees. We strive to maintain an environment that offers every one of them an opportunity to grow as fast as they choose, relative to their skill sets and shouldering of responsibility.

Virtually all employees have had the opportunity to become shareholders at Clas-SiC via stock option awards upon the achievement of company-wide goals, or the occasional offer to purchase shares from other shareholders. We believe that employee ownership in a start-up like Clas-SiC is a 'once-in-a-lifetime' opportunity, whose value and benefits should not be underestimated by either the employees or their company.

Why SiC is such a big deal

For high-power energy-conversion applications, silicon power devices have been doing a great job until now. However, energy efficiency is becoming ever more important, due to recent restrictions in energy availability. This means everyone must use energy as efficiently as possible. Wide bandgap semiconductors such as SiC facilitate this goal.

This material is an excellent choice for applications requiring at least 650 V – and an incredibly strong candidate for those requiring 1 kV or more. Although today's SiC MOSFETs and diodes are more expensive than the silicon parts they are displacing, by enabling higher switching frequencies, they allow for a significant reduction in the size and weight of the associated system magnetics. These advantages result in an appreciable cut in the overall system cost and volume, as well as increased efficiency. For most applications, especially those involving transport, trimming size and weight alone saves energy.

As a bonus, SiC offers improvements in power conversion and energy efficiency. What's more, due to its wide band gap, SiC can run at higher temperatures than the silicon parts it replaces, reducing cooling requirements, yet another welcome reduction in size and weight for transport applications.

takes place on a common processing platform, using standard processes and modules.

This results in minimal non-recurring engineering and a direct, reliable route for diode prototype fabrication within just eight weeks.

We have also demonstrated 1700 V and 3300 V MOSFET technologies. Alpha-level PDKs are now available, and full 1700 V and 3300 V MOSFET PDK releases will follow once reliability testing is complete.

It should be noted that standard processes and modules underpinning our PDKs can and have been used with other process technologies. This facilitates rapid fabrication of highly-customised devices, with minimal non-recurring engineering.

By employing PDKs, we can preserve our position as a pure-play foundry, with a clear division of Intellectual Property (IP). Process IP remains with Clas-SiC, while design IP strictly belongs to our customers.

Tool and materials suppliers are interested in our reference devices, using them to investigate new concepts. One example of this is our collaboration with Oxford Instruments, which used our reference to validate a contactless SiC plasma polish approach that could supersede chemical-mechanical polishing. This partner appreciates our support, with company Technical Marketing Manager, Grant Baldwin, describing the project as a 'fantastic collaboration'.

Advanced technology projects

As well as employing Clas-SiC's fundamental technologies across a range of customer programmes, the company is also participating in UK Driving the Electric Revolution (DER) and Advanced Propulsion Centre (APC) funded collaborations. They include:

CELERITAS

- CELERITAS – an APC collaboration where Clas-SiC's 1200 V MOSFET technology is applied to an ultra-fast battery charging application

ESCAPE

- ESCAPE (End to End Supply Chain Development for Automotive Power Electronics) – an APC collaboration where leading edge SiC trench MOSFETs are being developed in Clas-SiC's wafer fab

- ASSiST (Advanced SiC Solid State Transformer) – a DER collaboration where Clas-SiC's 3300 V MOSFET technology is applied to a solid-state transformer application

More information on these projects can be found at:
www.der-ic.org.uk/post/der-ic-success-in-ukri-supply-chains-for-net-zero-competition
www.apcuk.co.uk/funded-projects/sprint-celeritas/
www.apcuk.co.uk/funded-projects/mclaren-escape/

Test	Diode	MOSFET
1200V HTRB at 175C	80 devices for 1000 hours	80 devices for 1000 hours
+25V/-10V HTGB at 175C	N/A	80 devices for 1000 hours
H3TRB at 80C 80% humidity	80 devices for 1000 hours	80 devices for 1000 hours
Temperature Cycling -55C/+150C	N/A	40 devices for 1000 cycles

➤ Table 1. Tests on a reference 15 A, 1200 V MPS diode and a reference 80 mΩ, 1200 V MOSFET demonstrate the functionality and reliability of Clas-SiC's process platforms.

Investing in human resources

Clas-SiC has invested heavily in human resources. While it's been a challenge to recruit in today's tight labour market, excellent progress has been accomplished by:

- Attitude/aptitude-based hiring of operator staff
- Employing modern apprentices to future-proof the equipment engineering talent pool. This has been very popular with operator staff, providing them a pathway for career progression
- Recruiting graduate apprentices, who attend university on a day-release programme while gaining practical experience, all going towards fitting them out for a career in process engineering
- Sponsoring the most capable electronics undergraduates via the UKESF scheme, providing them with internships and the potential for employment once they graduate
- Facilitating a total of $230,000 of STEM funding for local high schools to encourage young people towards a science/engineering career

Future plans

Due to the high level of interest in our SiC PDKs, we are enjoying a steep increase in customer demand.

Buoyed by this we recently doubled headcount to more than 50, and we have plans under way to double again. Running in parallel, our ISO9001 certification is actively under way, with ISO TS16949 qualification planned for 2023. Additionally, we are undertaking an equity-investment round, instigated to fund demand-driven expansion of our capacity by a factor of 2.5 and enhance operational resilience, all on the existing facility footprint.

We have a great deal to look forward to, including exciting volume projections from current and prospective customers.

To fulfil our obligations when these projections come to fruition, we are actively engaging with potential SiC wafer fab partners that are capable of handling high-volume, capacity-hungry customer products. When those products outgrow our capacity, we will hand over to our partners that will be ready to provide high-rate-production capabilities.

From our outset, we have never had any intention of treading water. Our next goals include: qualifying 1700 V and 3300 V MOSFET platforms; continual, incremental refinements to our existing 1200 V MOSFET PDK; continuing to work with our design partner to develop a second-generation 1200 V MOSFET PDK that will enable a significant reduction in MOSFET specific on-resistance while enhancing short-circuit withstand times; and the development of a planar JFET platform, to be launched later this year.

We closely follow technology trends. Observing them has led us to decide that high-voltage devices and trench-MOSFET technology are the next areas for our development programme. This will enable us to offer PDKs for highly customised applications that leverage these advanced technologies. Our customers' needs dictate our roadmap, and will continue to do so.

Solutions for Compound **semiconductor passivation**

ZnSe
SiN
Oxide

RIBER's **CPS passivation tools**

UHV environment for solving the oxidation issues

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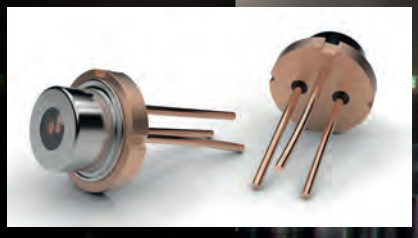

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Bringing down the cost of III-V epitaxy

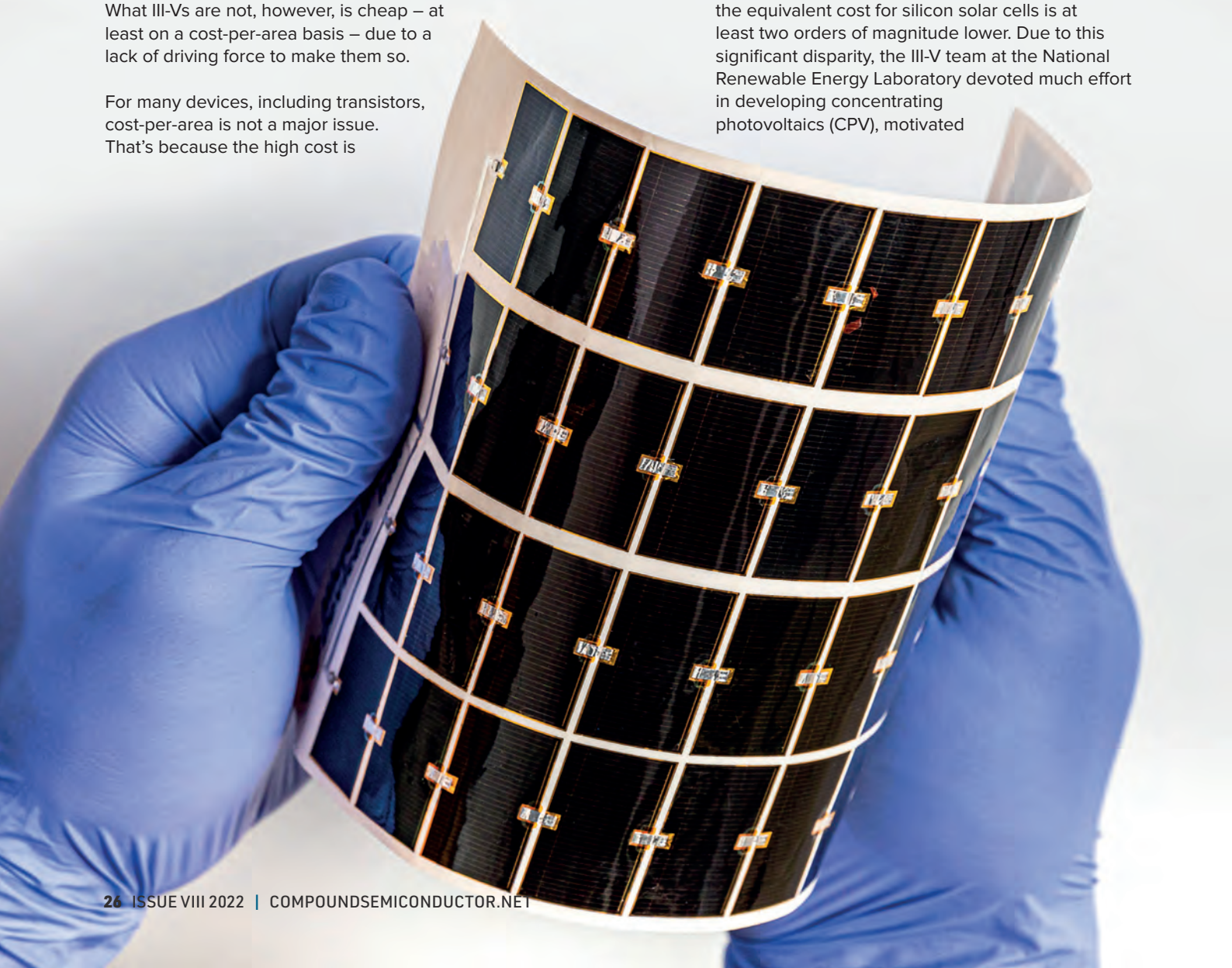
A radical form of HVPE that speeds growth, ensures high-quality interfaces, and allows the inclusion of aluminium-containing alloys will revolutionise production of III-V devices

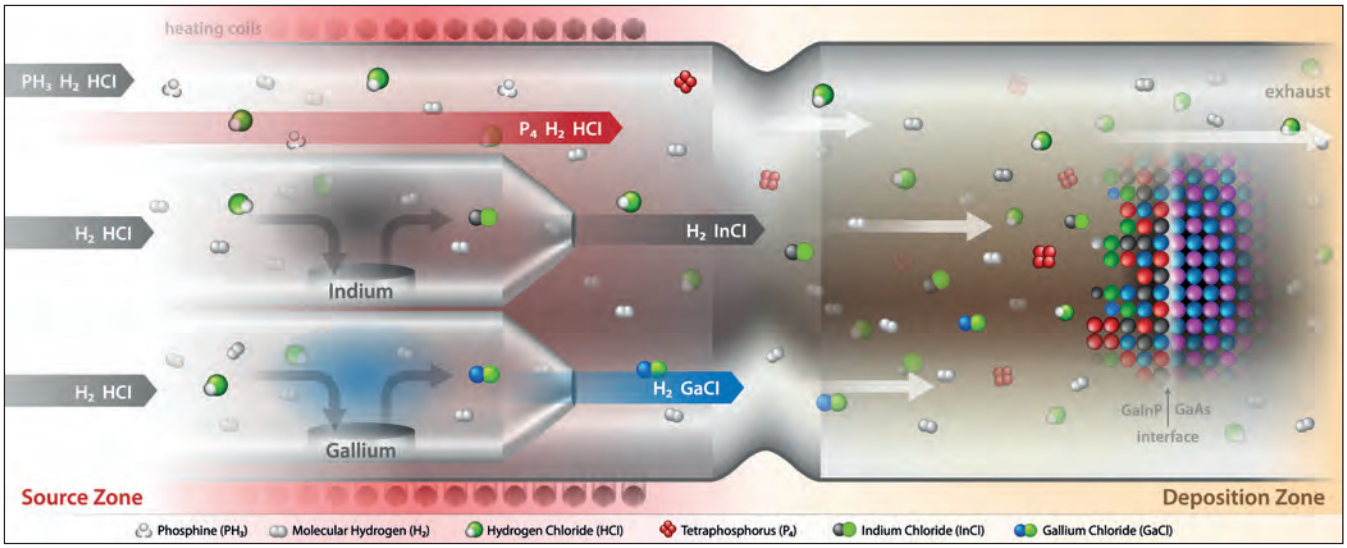
BY AARON PTAK, JOHN SIMON AND KEVIN SCHULTE FROM NREL

III-V semiconductors are the gold standard for many devices. They sit at the heart of lasers and LEDs, high-speed and high-power electronics, and space photovoltaics (PVs). Consider, for example, the latter: PVs made from III-Vs have demonstrated the highest energy-conversion efficiency and specific power for any material system, and can be very lightweight, thin and flexible, as well as incredibly stable – that's everything anyone would want from a solar cell. What III-Vs are not, however, is cheap – at least on a cost-per-area basis – due to a lack of driving force to make them so.

For many devices, including transistors, cost-per-area is not a major issue. That's because the high cost is amortized through the production of thousands and thousands of devices from every wafer. However, some applications don't have this luxury, including PV – both solar and thermal – and microLEDs deployed to populate substantial display areas.

Again, using solar cells as an example, it costs between $30,000 and $50,000 to cover a square meter with high-efficiency III-V PV, while the equivalent cost for silicon solar cells is at least two orders of magnitude lower. Due to this significant disparity, the III-V team at the National Renewable Energy Laboratory devoted much effort in developing concentrating photovoltaics (CPV), motivated





➤Figure 1. Conventional HVPE growth process.

by the hope that the high cost of solar cells would be offset by relatively cheap aluminium, glass, and steel. Unfortunately, due largely to plummeting prices of silicon PV over the last decade, the CPV market never materialized.

Our new challenge is to make III-V devices competitive in one-Sun, non-concentrated applications where the benefits of thin, light, flexible, stable, high-efficiency III-V PV can truly shine. These attributes will allow III-Vs to be deployed in applications where today's more prevalent solar technologies cannot, such as powering unmanned aerial vehicles, or being moulded into car bodies and integrated into architecture in ways that are more aesthetically pleasing. But there is a problem of scale. As each 6-inch III-V wafer produces just 4-5 W of power, the area required to produce megawatts, let alone the gigawatts needed to power an increasingly electrified world, is astonishing.

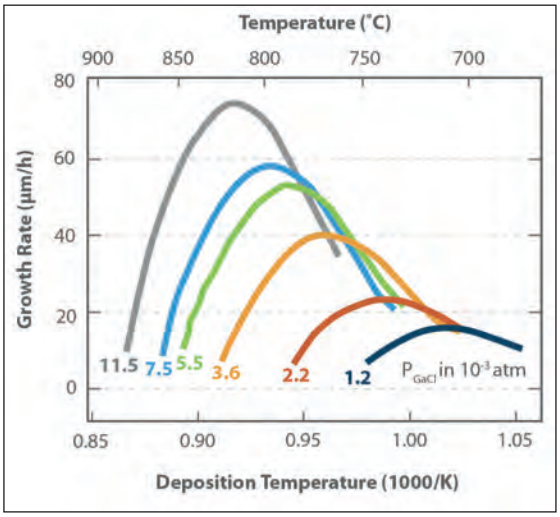
If these III-V devices are to move from niche markets, such as space PV, to widespread terrestrial applications without the aid of concentration, their cost will have to tumble. Success on this front would be welcome throughout the compound semiconductor community. Even for producers of devices where the size of the chip is a secondary matter, due to demand for III-Vs rising across the board, a substantial fall in cost would be good news.

Cost drivers

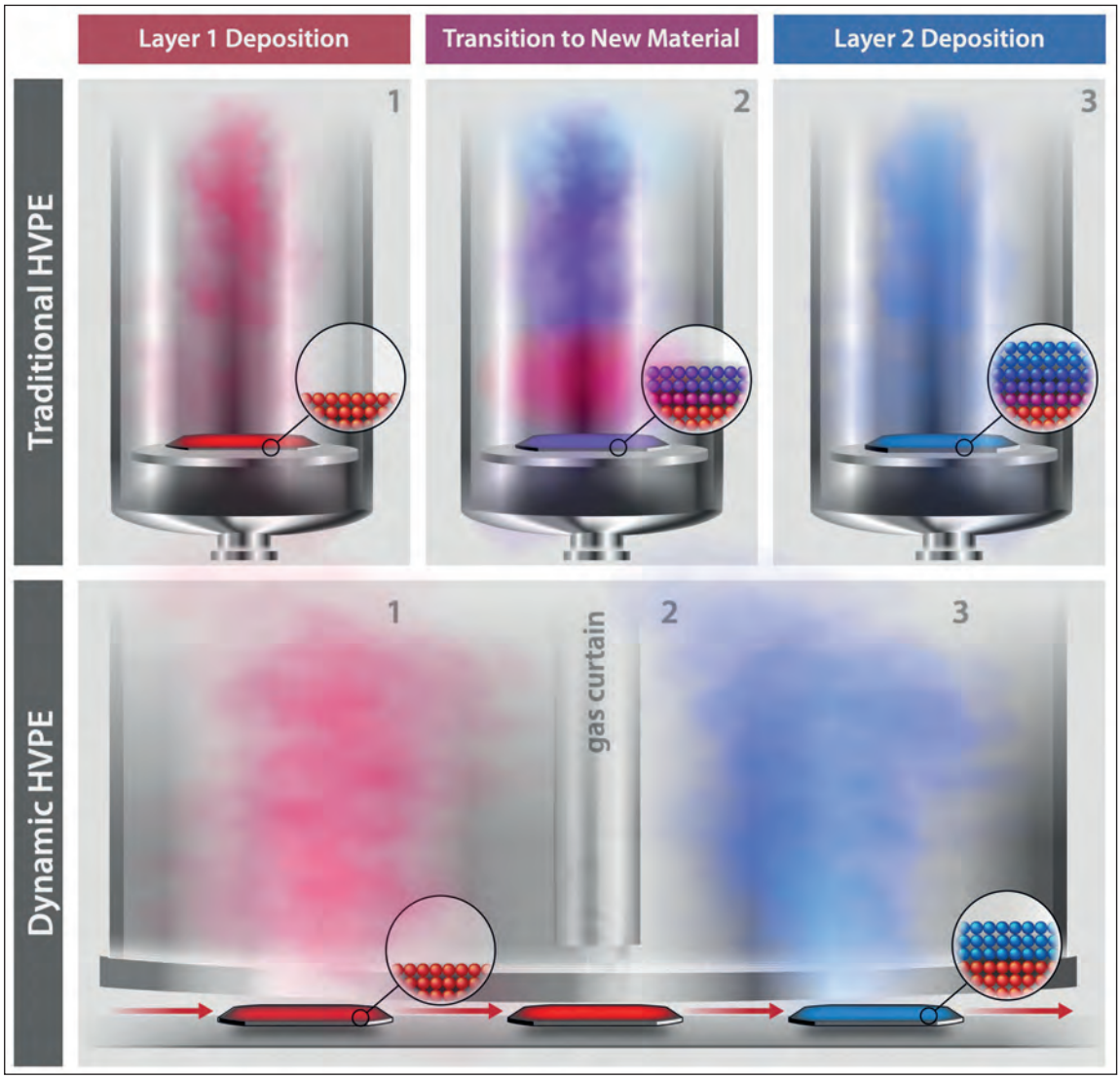
Three main factors contribute to the cost of producing III-V devices: the price of the substrate, the expense associated with the epitaxial process, and device processing. Substrate production costs have fallen in recent years, driven by increased demand for VCSELs and other optoelectronics, while post-processing has benefitted from higher levels of automation. The cost of epitaxy, however, has remained stubbornly high, which is why we have been focusing on an approach to slash the cost of epitaxial growth. Today's MBE and MOCVD tools are batch systems, which limit throughput and hamper scaling to very large production volumes. Growth involves either relatively expensive precursors, used inefficiently, or costly high-vacuum equipment. What's needed, especially for area-intensive device applications, is a low-cost, high-throughput and easily scalable deposition method that produces materials and devices with the same quality as the incumbent approaches.

We see HVPE as an exciting possible solution. Developed between the 1960s and the 1980s, this growth technique is well known for using high growth rates to produce high-quality III-Vs with excellent purity from inexpensive source materials (see Figure 1).

In its heyday, engineers produced a number of devices by HVPE, including commodity GaAsP visible LEDs, grown on compositionally graded buffer layers on GaAs substrates. HVPE was well-



➤Figure 2. Growth rate of GaAs grown by HVPE using different metal chloride partial pressures. The growth rate is limited by kinetics at low temperature and the effects of decomposition at higher temperature.



➤Figure 3. Schematic representation of heterostructure growth using traditional- and Dynamic HVPE.

suited to producing this type of device. High growth rates could accommodate relatively thick graded layers that minimize the dislocation density, but were to blame for an incapability to produce high-quality *p-n* junctions – this weakness stemmed from the challenges in realising abrupt changes in the growth chemistry within the HVPE reactor. To sidestep these challenges, *p-n* junctions were created by diffusion. This workaround offers an insight into why HVPE has not been applied to complex device structures.

Limitations of traditional HVPE

Refinements to MBE and MOCVD growth technologies throughout the 1980s enabled these techniques to outperform HVPE, which gradually fell out of favour. The two alternatives that now dominate III-V epi-growth have three major advantages over traditional HVPE: wide, easily controlled process windows; the ability to create structurally- and chemically- abrupt interfaces between device layers; and a wider palette of materials, including aluminium-containing alloys like AlGaAs and AlGaInP that were notoriously difficult to grow by HVPE.

Here we discuss the challenges of traditional HVPE in more detail, before outlining our solutions that are making HVPE relevant in today's epitaxy landscape.

With traditional HVPE, the growth rate is governed by the reduction of As-Ga-Cl species on the surface by active hydrogen. The energy barrier to crack molecular hydrogen limits growth rates at lower growth temperatures, while decomposition is an important factor at higher temperatures. These trends are behind an 'inverted U-shaped' growth rate dependence on temperature (see Figure 2). In comparison, growth rates for MBE and MOCVD are temperature insensitive over a large temperature range. In short, while HVPE boasts higher growth rates, it fails to provide a wide, temperature-independent process window that simplifies the growth of a targeted layer thickness or alloy composition.

The HVPE process involves *in situ* generation of metal chlorides – realised through the reaction of metallic gallium and indium with anhydrous HCl – that provide group III precursor species. This reaction typically takes place in a hot quartz

ampoule within the reactor. When growing a layered stack of different materials, there's a need to stop the reaction, purge out the products and change to a new chemistry – but this takes up valuable time. Speeding this up is not easy, as there is significant chemical inertia in the process, and attempts to do so can lead to graded interfaces (see Figure 3). The high growth rates inherent in HVPE exacerbate the extent of the graded material. Due to this challenge, the traditional HVPE process is incapable of growing the abrupt heterointerfaces required for today's modern, complex device structures.

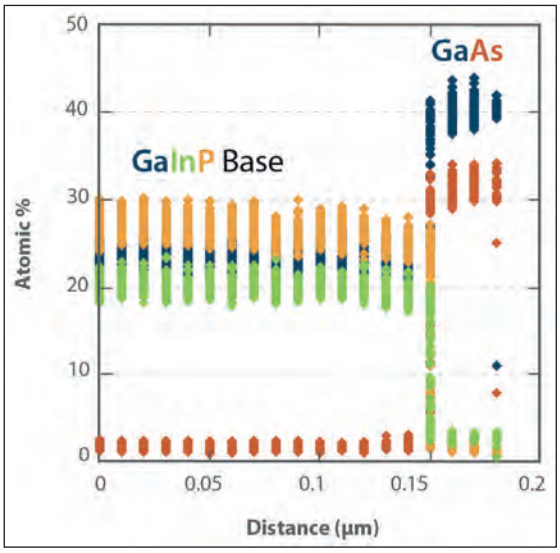
Two of the critical materials for realizing many high-efficiency device structures, from lasers and LEDs to transistors and solar cells, are AlGaAs and AlGaInP. Roles undertaken by these high-bandgap materials include providing the cladding layers for other materials, and acting as an active layer in devices operating in the visible domain. In HVPE, the analogous aluminium-containing precursor to the standard Ga and In precursors, GaCl and InCl, is AlCl. However, this molecule is extremely reactive. It etches quartz, the most common HVPE reactor material, and is likely to pyrolyze and deposit on reactor walls before it even reaches the substrate unless the reactor runs at 1000°C or more. These temperatures are incompatible with the incorporation of relatively volatile indium-containing molecules, and so preclude the formation of AlInP and its related alloys. Even when AlCl reaches the substrate, it has such a fast reaction with the group V source that it outcompetes all other precursors, leading to the formation of AlAs instead of controllable ternary and quaternary alloys.

HVPE reimagined – Dynamic HVPE

Driven by the need to drastically reduce the cost of IIIV PV for all applications, we have spent the last decade revisiting, refining, and reinvigorating HVPE to exploit its beneficial properties while minimizing the negatives. Our key innovation is to keep the process gases constant and move the wafer, rather than keeping the wafer stationary while changing the reactant gases, as is the case in traditional epitaxy (see Figure 3). This single change completely sidesteps traditional HVPE's chemical inertia, which is behind the graded interfaces.

We have named our approach Dynamic HVPE, to differentiate this process from traditional HVPE. With the conventional form of HVPE, changing process gases to transfer from the deposition of one material to another leads to significant growth time under a mixed atmosphere containing both gases. That's undesirable, tending to result in substantial growth of graded-composition material, due to growth rates that are often in excess of 1 μm/min.

To address this issue, Dynamic HVPE employs two adjacent growth chambers, each prepared with steady-state gas flows and growth conditions, and a wafer that moves between them in less than two seconds, leading to chemically- and structurally-abrupt



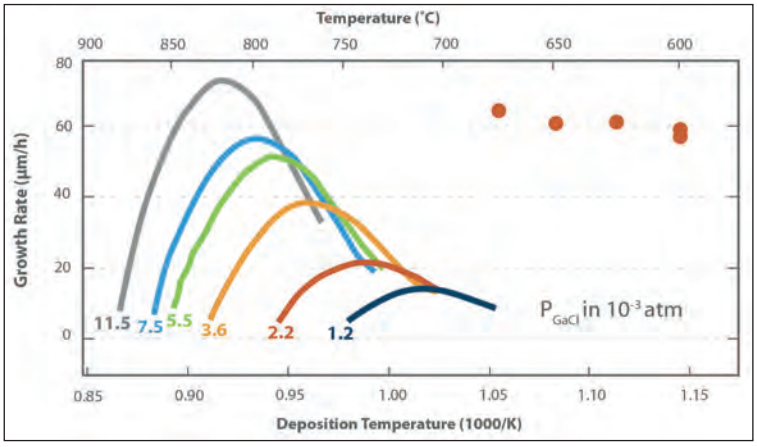
➤Figure 4. Energy dispersive X-ray spectroscopy measurements showing a chemically-abrupt GaInP/GaAs heterointerface deposited by Dynamic HVPE.

heterointerfaces. According to energy dispersive X-ray spectroscopy measurements taken in a transmission electron microscope, undertaken on a GaAs/GaInP heterointerface, Dynamic HVPE ensures atomic-scale interface abruptness (see Figure 4).

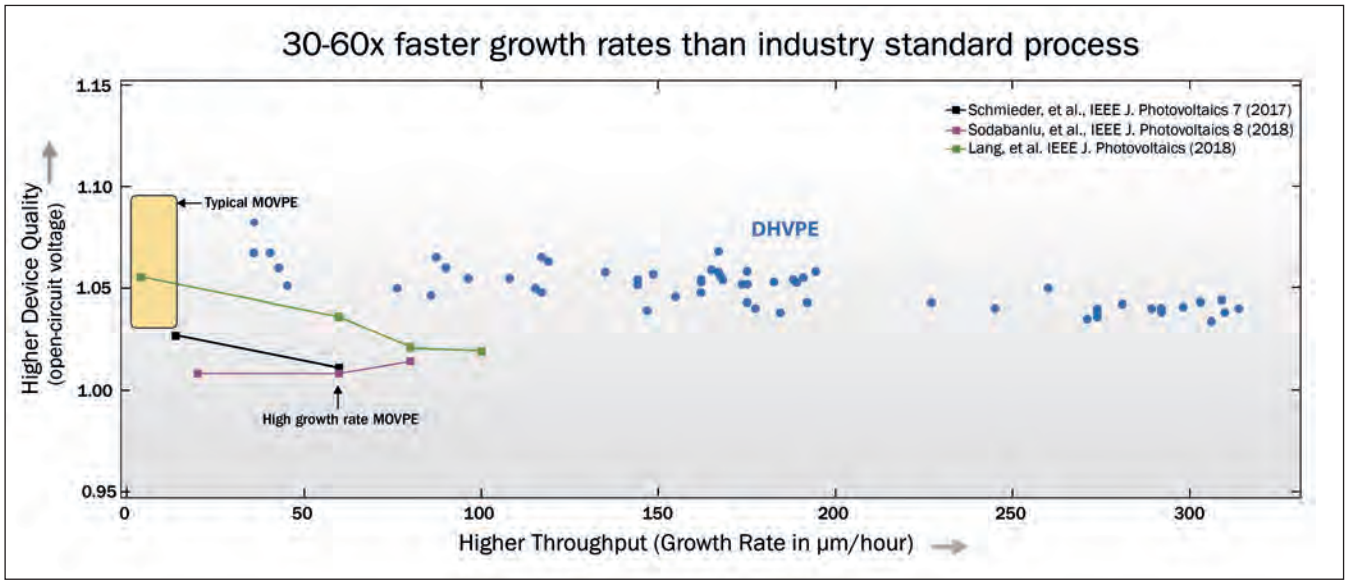
Such a high degree of interfacial control holds the key to significant improvement in device performance compared with devices grown by traditional HVPE using growth pauses. For double heterostructures, a common feature in many optoelectronic devices, our superior form of HVPE provides a five-fold decrease in the interface recombination velocity, according to time-resolved photoluminescence. This indicates that Dynamic HVPE is suitable for the production of arbitrarily complex device structures that rely on low-defect interfaces for high-performance operation.

Precisely controlling rapid growth

Building on this success, we moved next to tackle the challenge of process controllability. Due to the temperature dependence of the growth process,



➤Figure 5. Comparison of the GaAs growth rate temperature dependence for traditional (curves) and hydride-enhanced HVPE (red points). Hydride-enhanced HVPE maintains high growth rates at much lower deposition temperatures.

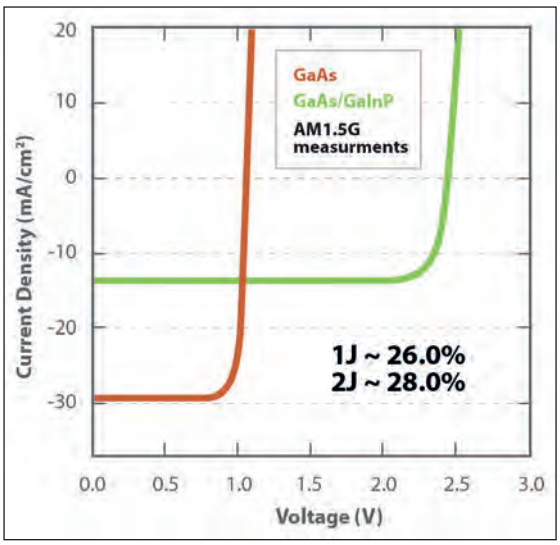


➤Figure 6. Performance of GaAs solar cells grown at a high rate using the hydride-enhanced mechanism.

caused by the large activation energy of the chlorine reduction step, minor changes in temperature can produce drastic variations in growth rates and alloy compositions. In traditional HVPE, the hydrogen atoms that are responsible for reducing chlorine on the surface and opening new surface sites for arsenic adsorption typically come from the hydrogen ambient used for growth. As molecular hydrogen pyrolysis kinetics are quite slow at typical growth temperatures – that is, there is limited cracking – the chlorine reduction process is very inefficient.

Cracked hydride gases, such as arsine, offer another potential source of active hydrogen species. However, arsine cracks almost immediately under typical hot-wall HVPE growth conditions, so relatively little active hydrogen would reach the growing surface.

Our solution to combatting the chlorine reduction rate-limiting step is to provide more active hydrogen where it's needed – at the surface. We accomplish this by introducing uncracked hydride gases to the surface, where they quickly break apart. This populates the surface with a large amount of active hydrogen, which scavenges chlorine from gallium and open sites to arsenic adsorption. This fundamental change transforms HVPE from a kinetically-limited growth process that needs high temperatures to realise high growth rates, to a mass-transport-limited process that is insensitive to growth temperature. Armed with this attractive *modus operandi*, HVPE is aligned with incumbent growth techniques.



➤ Figure 7. Single- and dual-junction III-V solar cells incorporating AlInP window layers.

With Dynamic HVPE, growth rates are tremendously fast – so much so that we can measure them in millimetres per hour, rather than the microns per hour. For GaAs, we have demonstrated rates in excess of 0.5 mm/h (see Figure 5). Critically, these extreme growth rates still lead to excellent device performance, a point illustrated in measurements of the open-circuit voltage of a solar cell (see Figure 6). We observe very little change in performance for growth rates from just less than 50 µm/h to 300 µm/h – and the change that is apparent is fully accounted for by decreasing doping levels with higher growth rates at constant doping flow.

Solving the aluminum issue

Growing aluminium-containing materials is challenging. Our solution is to switch the precursor from the highly-reactive AlCl to the more stable $AlCl_3$. To produce $AlCl_3$ from Al and HCl, while avoiding having significant formation of AlCl at the same time, we employ lower temperatures than those normally present in a HVPE system. For the growth of aluminium-containing alloys we use temperatures near 400 °C, realised by either introducing a colder region inside the reactor or adding an external $AlCl_3$ generator – each solution brings its own benefits and challenges.

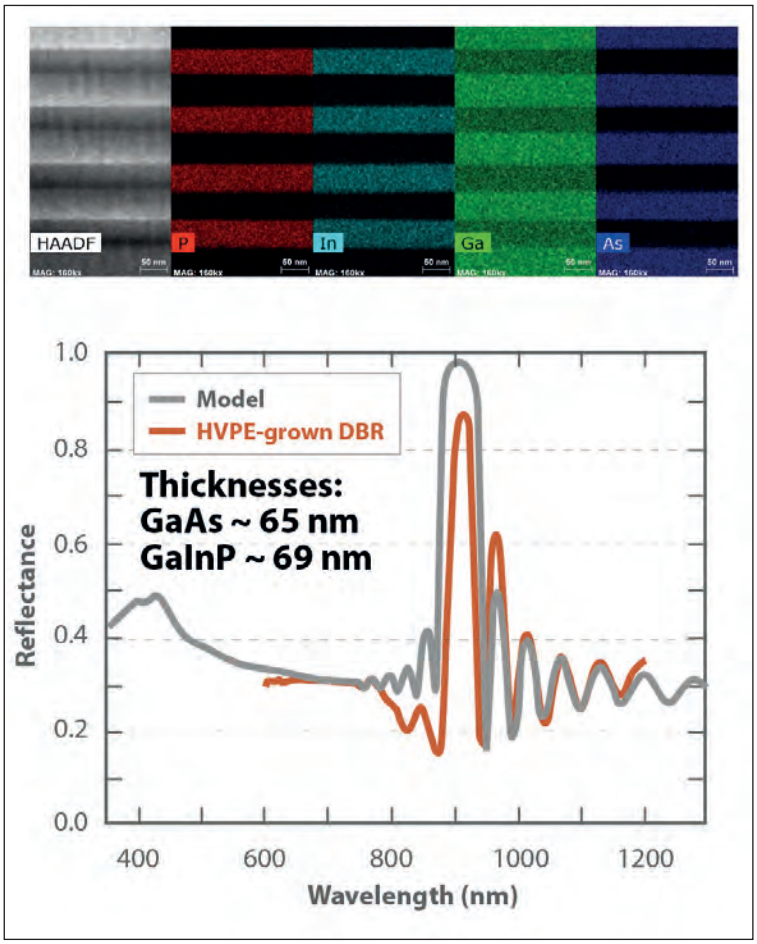
Using $AlCl_3$ enables the controllable formation of AlGaAs alloys across the entire composition range, as well as the growth of Al(Ga)InP, which

was long deemed impossible by HVPE. The epilayers produced by this approach still contain oxygen and silicon impurities, presumably from either wall reactions with the small amount of monochloride formed along with the trichloride, or from monochloride formed on the substrate surface. However, this work is in its infancy, and there is ample room for optimization.

Despite these challenges, we have been able to incorporate aluminium-containing materials into devices, including single- and dual-junction solar cells that incorporate AlInP window layers (see Figure 8). The efficiency of these cells is increasing, closing the gap with MOCVD-grown devices.

By solving the three limitations of HVPE – the lack of sharp interfaces, variations in growth conditions with temperature, and the challenge of growing aluminium-containing alloys – we have broken down the barriers to matching the performance of devices grown by today's mainstream technologies. Now there's the opportunity to combine the quality associated with MBE and MOCVD with lower costs and a far higher throughput.

To showcase the capability of Dynamic HVPE for the growth of a wide variety of devices we have fabricated three types of non-solar structure: a distributed Bragg reflector with 20 pairs of GaInP/GaAs that provides high reflectance at a wavelength of around 900 nm, confirming thickness control and flat, parallel interfaces (see Figure 8); a one-off growth of a HBT (not shown) that displays current modulation and gain, indicating initial proof-of-concept for transistor growth by Dynamic HVPE; and a compositionally-graded GaInP buffer layer, grown on a GaAs substrate to a lattice mismatch of 3.8 percent (not shown), that has the same dislocation density as MOCVD-grown structures. This buffer takes less than 10 minutes to grow. These results with all three structures underscore the promise of Dynamic HVPE, a technique that combines very fast growth rates with inexpensive precursors and a tremendous potential for achieving enormous scale for a vast range of devices, including VCSELs, LEDs, thermophotovoltaics and emitters/receivers for power beaming.



➤ Figure 8. Transmission electron microscopy and energy dispersive electron diffraction measurements of a portion of a GaInP/GaAs DBR structure grown using Dynamic HVPE (top), and the measured reflectance of the DBR (bottom).

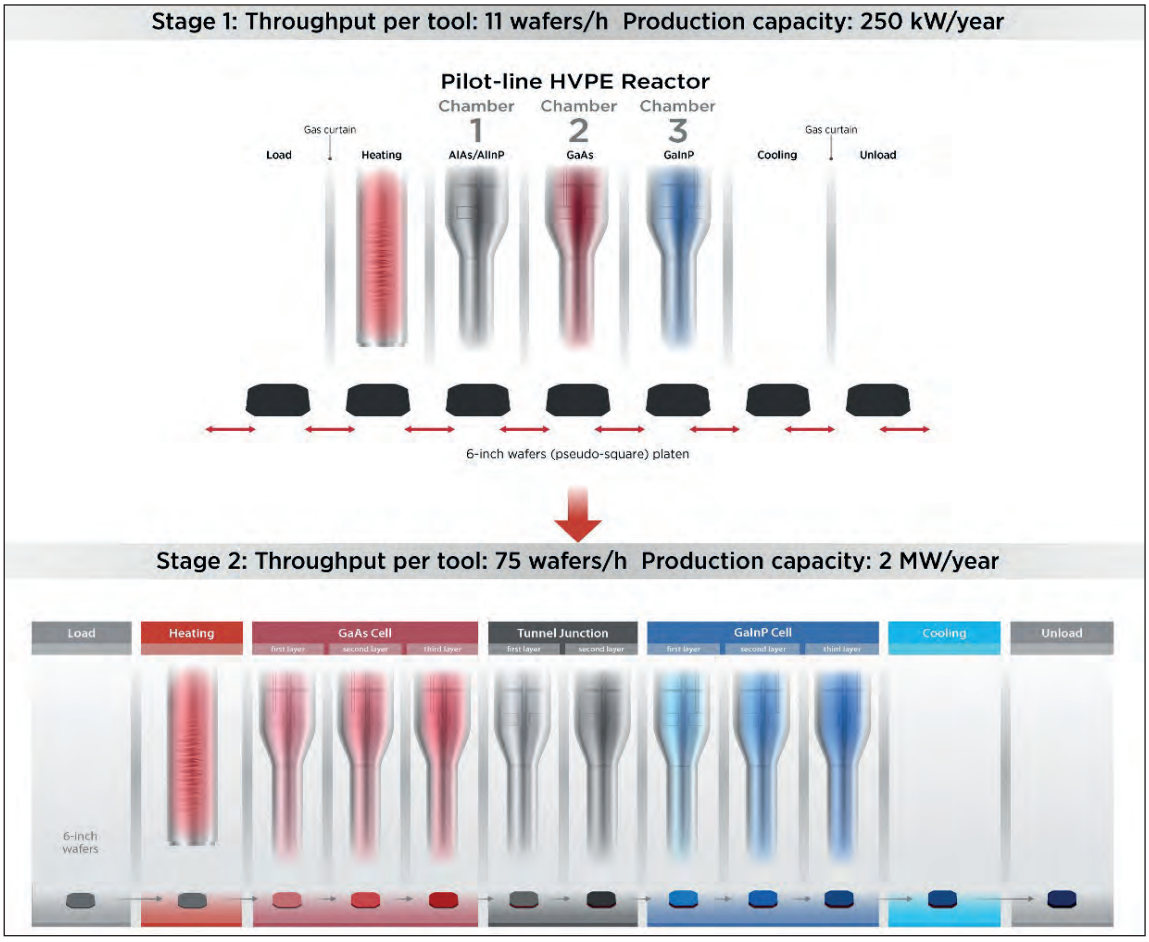
The path ahead

Scale is the most potent cost-reduction tool available for semiconductor growth, crucially for large-area devices. Increasing throughput delivers cost savings throughout production. Even devices with a relatively small footprint benefit from trimming cost and the ability to easily expand production when needed. By turning to Dynamic HVPE, chipmakers can employ an approach that opens the door to much greater scale for the production of III-V devices.

The dynamic wafer transfer process, which we have validated in our research reactor, is inherently scalable, so it lends itself perfectly to a fully in-line production system. In Figure 9 we offer an illustration of an in-line Dynamic HVPE system capable of producing multi-junction III-V solar cells. Note that the number and capability of the different chambers could be adjusted for any arbitrary device structure with any number or type of layers. We estimate that a system such as this could produce 500,000 wafers per year – that's approximately 70 times that of today's batch systems. This leap in throughput will slash costs, in addition to meeting future production demands.

As a first step toward this high-throughput production future, we are soon to take delivery of a pilot-scale Dynamic HVPE system featuring three growth chambers, to simulate a pseudo in-line growth reactor. This system will shuffle 6-inch wafers back and forth to build up a full device structure, rather than wafers moving continuously in one direction. Even the production volume of this pilot system should reach 80,000 wafers per year, equating to 300 kW of one-Sun, non-concentrated PV.

We are planning to commission our new system this Fall, before optimising its performance for device quality and throughput of high-efficiency



➤ Figure 9. Schematic representations of the pilot-production Dynamic HVPE reactor scheduled for delivery to NREL in Fall 2022 (top), and a concept of the fully-inline production reactor capable of producing 500,000 wafers per year.

multi-junction III-V PVs. Success on these fronts will represent a major step towards drastically lowering the cost of III-V solar cells and providing a pathway to lower cost and larger scale for all III-V devices.

- *Visit NREL.gov to learn more about lower-cost III-Vs and licensing opportunities.*

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Integrated energy storage unlocks CPV's full potential

Packed with III-V cells, a small solar module that's almost two thousand times more powerful than a typical silicon PV panel holds the key to grid-friendly renewable energy

BY JOHN LASICH AND KIRA RUNDEL FROM RAYGEN

A SHEEP PADDOCK in the Australian outback is the surprising location for the world's largest next-generation storage project, backed by global energy majors.

Driving this renewable deployment is RayGen, our company that's located in Melbourne, Australia. We are in the final stages of constructing and commissioning a ground-breaking system that combines electricity generation from 4 MW of solar with a 3 MW / 50 MWh storage facility. Located near the rural community of Carwarp – roughly six hours' drive inland from Melbourne – this unassuming site hosts the world's largest next-generation storage project. It is here that we are showcasing a world-leading technology that offers a superior alternative to lithium-ion batteries and pumped hydro.

Rising out of the sheep paddock at this revolutionary site are four solar towers, shining in the summer sky. At the top of each is a dense array of III-V GaAs solar modules, which convert a concentrated solar beam into electricity and heat. Close to the towers sit two large pits; covered, insulated, and filled with water. Between them, they store enough thermal energy to provide 50 MWh of dispatchable electricity – equivalent to a 'big battery'.

➤ Figure 1. Srinivasa Balamurugan, module manufacturing expert, holds a solar module, fabricated at RayGen's automated module manufacturing facility in Melbourne, Australia. The small 10 cm x 10 cm module produces 2.5 kW of electricity and 5.0 kW of heat under 750x concentration.

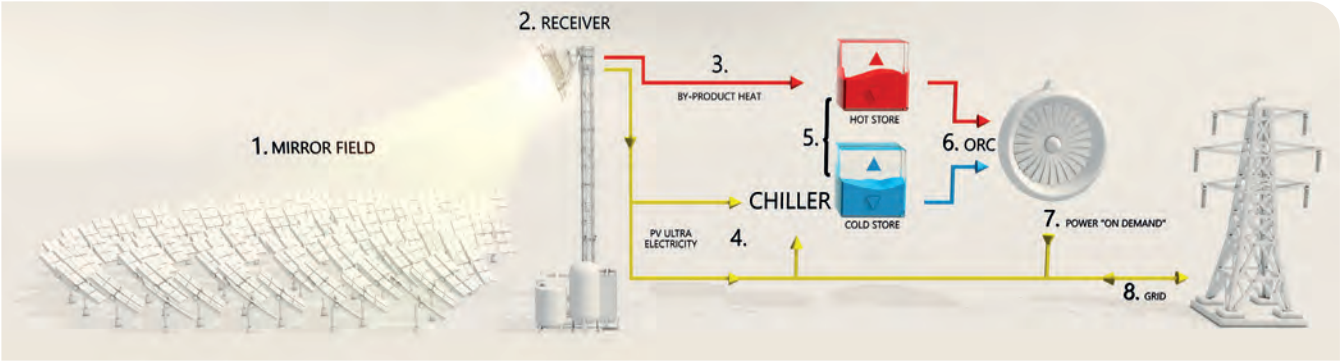
Spurred on by the world's largest energy companies, we have a growing pipeline of projects approaching gigawatt scale. All these potential deployments offer growing demand and an exciting market opportunity for the compound semiconductor industry.

A band-aid solution

Tending to employ mono- and multi-crystalline silicon photovoltaic (PV) solar panels, today's solar farms are causing some headaches for global grids.

Due to the tremendously successful cost reduction of silicon PV, its deployment is now so extensive that it has led to market saturation during solar hours. Midday prices have been driven to zero and below, while overwhelmed grids are curtailing solar output. Then, as soon as the sun sets – or even disappears behind a cloud – alternative generation has to kick-in immediately, in order to satisfy demand.

Gas generators or lithium-ion batteries that can quickly respond to changes in grid loads have become the default solution to fixing grid instability issues caused by fluctuations in renewable energy output. However, while power from silicon PV and wind is inexpensive, the cost of open-cycle gas generation and electro-chemical battery storage is certainly not. In fact, the cost associated with solar-PV-plus-batteries is so high that their use alone would likely prevent the mass deployment that is needed for decarbonisation. Or, to put it bluntly, gas generators and lithium-ion batteries remain a band-aid solution suitable for short-term support.



➤ Figure 2. (1) A field of mirrors concentrates sunlight onto raised RayGen solar modules. (These modules are high-efficiency and actively cooled). (2) RayGen's solar modules convert sunlight to power with approximately 90 percent efficiency – 30 percent to electricity and 60 percent to heat. (3) Captured hot water (by-product from the cooling system of the modules) is stored in a nearby water reservoir. (4) Generated electricity chills water in a second reservoir or is sold to the grid. (5) The insulated reservoirs maintain a temperature difference of 90 °C. (6) The stored difference in temperature is used to drive a heat-to-power engine. (7) This turbine provides the grid with reliable, on-demand power and an option for baseload power.

In reality, what's needed to decarbonise the world's electricity grid is large-scale deployment of renewable energy alongside low cost, bulk storage.

RayGen's solar-and-storage

Our proprietary technology (see Figure 2) is designed to do just that by addressing the growing need for renewable generation paired with bulk storage. The world-first approach to solar that we are taking – described in jargon as 'tower-mounted concentrated photovoltaic co-generation' – is the key enabler for our trailblazing approach to storage, which we describe as water-based electro-thermal energy storage or 'Solar-Hydro'.

Beneath each solar tower in a RayGen solar system are nearly three hundred wireless, automated, dual-axis heliostats that track the sun's movements across the sky. These mirrors concentrate sunlight by a factor of almost one thousand onto the receiver that's positioned at the top of the tower.

The receiver incorporates more than four hundred RayGen modules. The surface of each is just 10 cm by 10 cm in size, less than an inch thick, and populated by one hundred highly efficient III-V triple-junction GaAs-based solar cells. Operating with an efficiency approaching 38 per cent, these cells directly convert the concentrated beam into electricity.

A sophisticated cooling system keeps the cells within their operational limits – and generates 90 °C heat as a by-product. This cooling system includes an electrically insulating, thermally conducting industrial ceramic and a water-cooled heat sink.

Each module produces 2.5 kW of electricity and 5 kW of heat – equivalent to a rooftop of a typical home fitted with silicon PV and solar-hot-water panels. As there are 441 modules in a receiver – just over 4 m^2 of active area – this produces 1 MW of electricity and 2 MW of thermal energy.

The RayGen solar system has been in operation since 2014. Over the intervening years there have been multiple iterations to the module, the receiver, the heliostat and the control system.

We use a suite of our proprietary IP to integrate some established technologies to create a new product. Tapping the natural synergies between the components delivers a new level of performance. We are the only company that has successfully demonstrated tower-mounted concentrated photovoltaic (CPV) co-generation, which physically separates the concentrator optics (mirrors) from the solar converter (modules), using proprietary software to ensure alignment. We are able to leverage expertise and investment in heliostats from the solar thermal industry, and employ the highest efficiency cells produced for satellites. Like silicon PV – and unlike previous versions of CPV – our system is modular and easy to manufacture, with mass-volume heliostats produced via an established and separate supply chain to our own high-performance PV module production.

Another strength of our technology is that it provides a higher capacity factor for solar generation than most silicon PV projects. Our system is limited to using direct normal irradiance – a measure of cloudless sunshine – but overcomes this restriction with a few innovations. We employ dual-axis tracking to capture more of the sunlight in the morning and afternoon, along with low-cost 'booster' heliostats to add extra concentration outside peak sun periods.

The approach that we are pioneering produces electricity with a similar land area and generation profile to silicon PV, but at a competitive or lower cost, and with the added benefit of by-product heat. The heat is crucial to energy storage, allowing our system to shift its electricity production from the middle of the day, when prices are low, to the evening and winter months, when prices are high.

➤ Figure 3. Construction of the 4 MW electricity plus 3 MW/ 50 MWh storage project near Mildura, Australia, is nearing completion. Each solar field utilises nearly 300 mirrors to concentrate light onto a central receiver. (The cold and hot water pits can be seen behind the fields of mirrors.)

RayGen's 'water battery'

The surplus energy that's generated by our system is stored in a 'water battery' and subsequently recovered via a heat engine.

We store our by-product solar hot water at 90°C in what is known as a stratified hot-water pit thermal-energy storage system. Such systems were developed for Northern Europe, where they are used to store thermal heat from the summer sun as hot water, which provides hydronic domestic heating during the winter. To maintain the high temperature while limiting water loss, these pits are insulated, lined and sealed. This is very effective, with thermal losses of the stored energy typically less than 10 percent over six months.

Within our system, we also employ a second pit of water, cooled to 0°C via an off-the-shelf electric chiller. The chiller is a standard ammonia heat pump, traditionally used in food and beverage refrigeration. The electricity to run the chiller can be drawn from the generation (PV) part of our system, or imported directly from the electricity grid when wholesale prices are low.

Electricity is then generated 'on demand' from the temperature difference in the pits with an Organic Rankine Cycle turbine, of the kind widely used in the geothermal industry. The turbine uses a small amount of ammonia as the working fluid, which boils at less than 90 °C. Heat from the hot water pit boils the ammonia, with the resulting pressurised vapour powering a turbine, before the cold water condenses the ammonia back to a liquid in the closed-loop system.

The modest temperature difference of 90 °C between the two pits limits the heat-to-power efficiency. Simple calculations based on thermodynamics give a maximum theoretical cycle efficiency, based on the Carnot Cycle, of 25 percent, while the practical efficiency is in the 12-to-15 percent range.

On the charging side of the storage cycle, the system has a coefficient of performance of 6 or more. This gives the system an impressive round-trip electrical efficiency of between 70 and 80 percent. That means that for every 1 MWh of electricity used to power the industrial chiller when market prices are low, around 0.7 - 0.8 MWh is produced by the turbine when prices are high.

Additional advantages of the modest temperatures are that the storage medium is low cost and thermal losses are low. In many ways our storage system is analogous to pumped hydro. Round-trip efficiencies are equivalent, and the volume of water required for one hour of storage is roughly the same. One way to think about the two bodies of water separated in temperature by 90 °C is that they are equivalent to a pumped hydro system separated in height by 1 km – but without the physical constraint of finding a geographic location suitable for pumped hydro.

Ultimate grid flexibility

RayGen storage can be charged by the electricity generated by the multi-junction cells or by the grid. The latter option can de-congest the grid, acting as a load during times of renewable saturation. If additional storage duration is needed, it's simply a matter of digging larger pits and filling them with water.

Further, with our technology, it is easy to co-locate storage within a solar renewable-energy zone. By co-locating long duration storage with solar, we increase the utilisation of grid transmission out of the renewable energy zone, leading to a lowering of the cost of delivered power for customers. The turbine generator set provides natural, synchronous inertia and can participate in voltage regulation and contingency markets.

Another feature of our technology is that it can be independently sized. Working with AGL Energy, we have developed a sophisticated techno-economic linear optimisation model for optimising the configuration and operation of our system for different applications and market conditions. While our approach to renewables is novel, we have selected equipment of existing technologies, using the best bits for our system. We have drawn on pits from Danish district heating, ORC turbines from geothermal plants, and chillers from food and beverage refrigeration; and our solar system incorporates: the modularity and easy manufacturability of silicon PV; the mirror collectors of concentrated solar power; and the high-efficiency cells from satellites and CPV.

➤ Figure 4. Four RayGen solar towers during commissioning. RayGen's storage construction is nearing completion and will be operating commercially in early 2023.

Real-world results

Last year we closed a US$40 million Series C funding round to demonstrate the technical feasibility of our proprietary Solar Power Plant. Strategic investments came from global energy majors Chevron, Equinor and Schlumberger; Australia's largest utility, AGL; listed renewable developer Photon Energy; and the Australian Renewable Energy Agency (ARENA). This financing supported the construction of our grid-connected flagship power plant at Carwarp (see Figures 3 and 4). Following the breaking of ground in the third quarter of 2021, this project is now nearing completion, with commercial operation expected by early 2023.

The Carwarp project is likely to be the first of many by us that will spring up in Australia and, ultimately, the world. Following the successful delivery of this flagship deployment, we will be completing much larger projects that are already in development. Scaling system capacity is relatively easy, with larger projects simply requiring more solar fields and larger, off-the-shelf turbines. This will involve scaling the 3 MW turbine used in the Carwarp project to the typical 25 MW turbine used for geothermal applications. Future projects will likely be deployed in 'blocks' of 50 MW of solar plus 25 MW of storage, with storage capacity scaled to fit a project's specific requirements.

Targeting high-volume deployment, we are focused on developing utility-scale projects with our strategic investors. One example is our partnership with Photon Energy, which has secured land in the Eyre Peninsula, South Australia, for a project that combines 300 MW of solar with 150 MW of storage, backed by 3.6 GWh of storage capacity. This project, on track to receive development approval in 2023, will be larger than any battery project in construction or operation.

The challenge ahead

Over the coming years the deployment of renewable energy is sure to grow, which will increase the need for long-duration storage. This expansion has exciting implications for epiwafer capacity within the compound semiconductor industry.

To remain competitive, we will need to keep pace with cost reductions in the incumbent technology, silicon PV. This will be supported by a move to higher-volume, lower-cost III-V cells, which will hinge on modifications to the existing epitaxial approaches for higher-volume throughput per reactor, such as the Dynamic HVPE technology pioneered by NREL (see p. xx for this issue), alongside automated cell processing.

With ample headroom for further enhancement in III-V multi-junction cell performance and cost, the future looks bright for both ourselves, and for the compound semiconductor industry.

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Epitaxial transfer enhances electronic-photonic circuits

A scalable process that unites silicon with the III-Vs allows well-established electronic applications to be served alongside those requiring specialized photonics

BY LEAH ESPENHAHN, JOHN CARLSON, PATRICK SU AND JOHN DALLESASSE
FROM THE UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

FOR MANY DECADES we have been dreaming of a new era for integrated circuits, where complex electronic functions are combined with dense photonic emitters on a single die – all accomplished at manufacturing scale. Up until now, the application of this vision has been hindered by the limited potential for broad deployment of such circuits. There has been no market pull for this technology, as well as insufficient motivation to drive development of viable integration processes, which are scalable and eliminate precision alignment at the individual emitter level.

Now, however, that need is finally arriving. The deployment of VCSEL arrays for facial recognition, general 3D imaging, and lidar has prompted the question: 'How dense can we integrate these functions?' There is also a related question, arising from the massive power requirements of data centres: 'What is the lowest energy we can use to transmit all this information?' For those that ponder both those questions for long enough, they'll ultimately be mulling over this: 'How do I combine dense electronic and photonic functions on a single die in a wafer-scale process?'

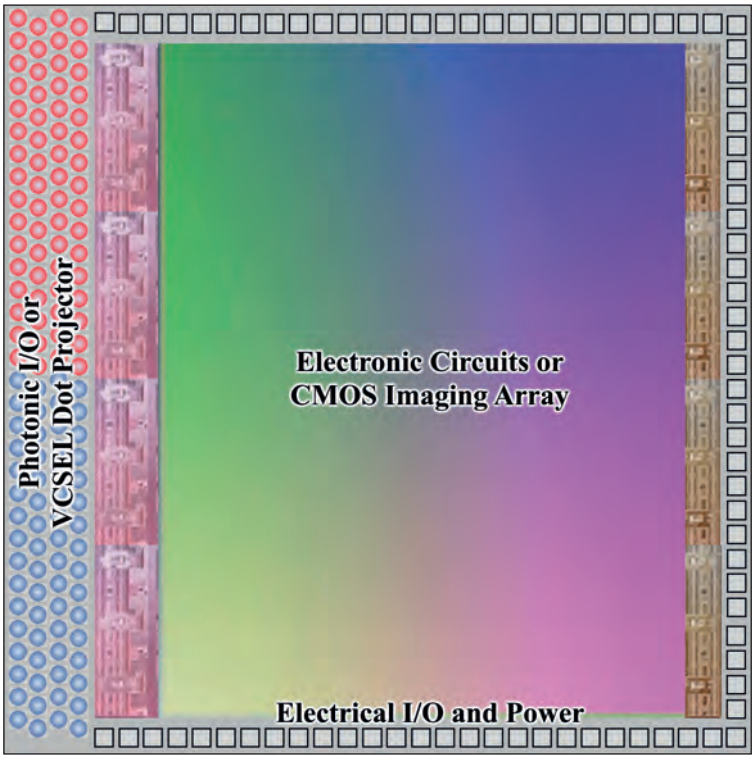
Many groups have wrestled with the later question. This has spawned many different approaches to integrate III-V material with silicon – and all have significant drawbacks. Take, for example, flip-chip bonding, a process that takes fully-formed VCSELs, or other photonic components, and attaches them to silicon die with solder or stud bumps. The placement accuracy of these flip-chipped devices is often limited by the capability of the pick-and-place tool, and the connection formed by the solder bumps tends to provide a poor thermal pathway restricting device performance. Another downside of this process is that it is slow, with any improvement in placement accuracy coming at the expense of throughput.

To alleviate these drawbacks, our team from the University of Illinois at Urbana-Champaign has developed an epitaxial transfer integration method that has many merits compared with alternative technologies. Its primary merits are: the opportunity to select different III-V epitaxial stacks for distinct photonic functions; the use of a wafer-scale photolithographic process to align photonic devices to electrical components; and an improved thermal pathway, enhancing heat extraction from the III-V photonic devices.

Our epitaxial transfer technique allows us to define selective III-V materials in specified regions on the silicon host, rather than integrating full wafers or fabricated die. With this approach we fabricate photonic devices with a wafer-scale process following the formation of these islands – this eliminates the need for individual high-precision die placements. Such a methodology has a level of functionality that allows emitter and detector epi to be integrated to provide optical input/output, and facilitates integration of a VCSEL dot projector with a CMOS imaging array, to provide a greater density of function in mobile handsets (see Figure 1 for an illustration of the functionality).

Strengths of our approach include more efficient use of III-V material and a higher density of function, leading to circuits that are smaller, lighter, cheaper and consume less power. What's more, unlike other integration methods, our technology allows designers to integrate different III-Vs across the wafer with unparalleled density, enabling them to take advantage of the broad range of functions made possible with distinct III-V semiconductors for different components and devices. And on top of that, our integration technique offers the improved alignment of photonic devices and the opportunity to increase their density.

Our two-step approach begins by using a carrier wafer to provide coarse alignment of the photonic device epitaxial material, a task that is well within the accuracy of pick-and-place machines and the alignment accuracy of low-precision bonding tools. The second step, which aligns the photonic devices relative to the features in the silicon wafer hosting the electronic devices, is performed after integration, using wafer-scale photolithographic process steps. This strategy enables us to make more compact and diverse devices than would be possible with standard integration techniques, which are limited in accuracy.



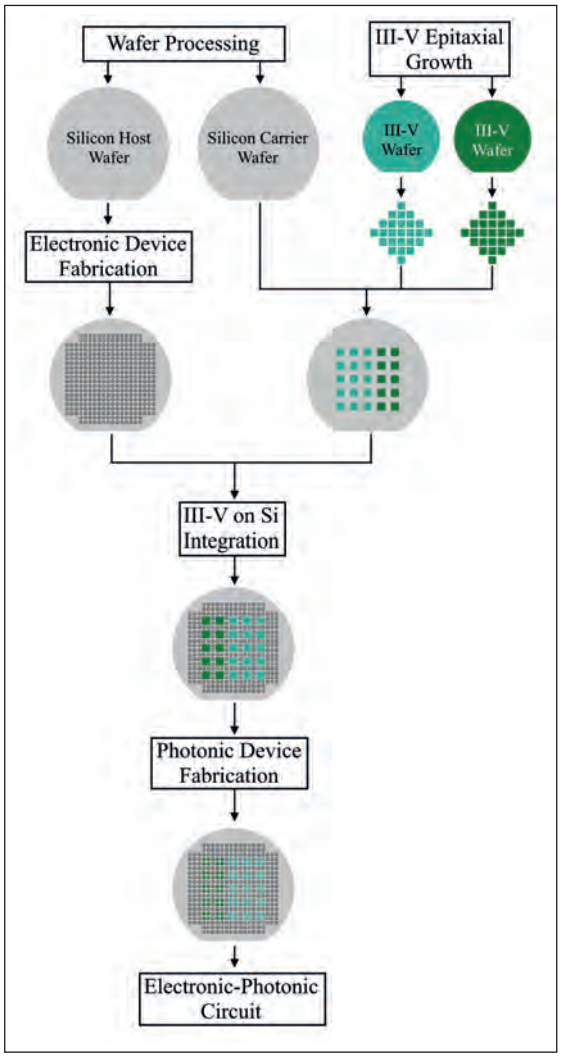
➤ Figure 1. Depiction of an integrated CMOS die enabled by epitaxial transfer, including an integrated array of III-V photonic devices with silicon electronic circuitry.

There are also gains that result from the removal of the III-V substrate during integration. Its extraction enables epitaxial material to take advantage of some of silicon's material properties after bonding. The benefits are particularly impactful with the most used III-V substrate material, GaAs, which has a relatively poor thermal conductivity compared with silicon. As we shall see in due course, when GaAs-based photonic devices are integrated with silicon and the substrate then removed, they deliver an improved thermal performance relative to devices fabricated on a native GaAs substrate.

The process flow for creating our silicon-photonic circuits utilizes two silicon wafers; a host and carrier (an overview is provided in Figure 2). Fabrication begins by applying a standard front-end-of-line process to a silicon host, and using a second carrier wafer to prepare the III-V material for integration. Any number and variety of III-V chiplets are temporarily bonded to this carrier. A permanent bond is subsequently formed to the silicon wafer with electronic devices, following III-V substrate removal, photolithography and dry etching. The final step is the fabrication of photonic devices and arrays on the integrated III-V materials.

Epitaxial transfer integration

Our integration process can be divided into three main stages: III-V substrate removal, III-V island formation, and epitaxial transfer (see Figure 3 for an illustration of these three steps).



➤ Figure 2. An overview of the silicon/III-V integration approach pursued at the University of Illinois at Urbana-Champaign.

During III-V substrate removal we temporarily bond pieces of III-V material to a silicon carrier. The bonding of these small pieces of III-V, which may be referred to as chiplets, is epitaxial side down. This process begins by depositing, onto the carrier wafer, a thin dielectric that serves two purposes: this layer improves adhesion to the temporary bonding polymer; and it reduces thermal stresses during the bonding processes, leading to superior process uniformity. Following the addition of the dielectric, a temporary bonding polymer is spun on top of this layer using a standard photoresist spinner. After that, chiplets are placed on the polymer, positioned in approximately mirrored locations to where the III-V epitaxy is desired on the final, silicon CMOS host. Note that in a manufacturing setting this process would be undertaken with a pick-and-place machine. The bonding polymer is then cured in a nitrogen-purged vacuum environment, with pressure applied to the top of these chiplets to minimise air pockets and contaminants that would degrade the bonding process. Following bonding of the chiplets to the silicon carrier, the III-V substrate is removed to leave just the III-V epitaxial layers bonded to the carrier. Lapping removes the substrate, creating material polished to a mirror finish. In our lab, we lap witha manual process that typically leaves 5 μm - 15 μm of III-V substrate. But this could be reduced significantly with industry-level lapping tools.

After substrate removal, chiplets are defined into III-V islands with a photolithographic process. This eliminates unneeded III-V material and provides precise definition of the islands locations. Determining the size of these islands is the accuracy of the wafer-to-wafer bond alignment tool, as well as the intended size for the photonic devices. Using standard methods we metallize the islands, in preparation for their eutectic bonding to pads on the silicon host wafer.

Following carrier wafer processing, our metallized III-V islands on the carrier wafer are brought into contact with metal pads on the silicon host wafer,

before the stack is placed in a conventional wafer bonding tool. A eutectic alloy is formed between the metals, allowing a permanent bond to form at low, CMOS-compatible temperatures. Once the eutectic bond is fully formed, the carrier wafer and remaining temporary bonding polymer are removed, to leave only the transferred epitaxial material on the silicon host substrate. The III-V material is planarized using a planarization polymer, in this case BCB-3022, before it is processed into photonic devices.

VCSEL Integration

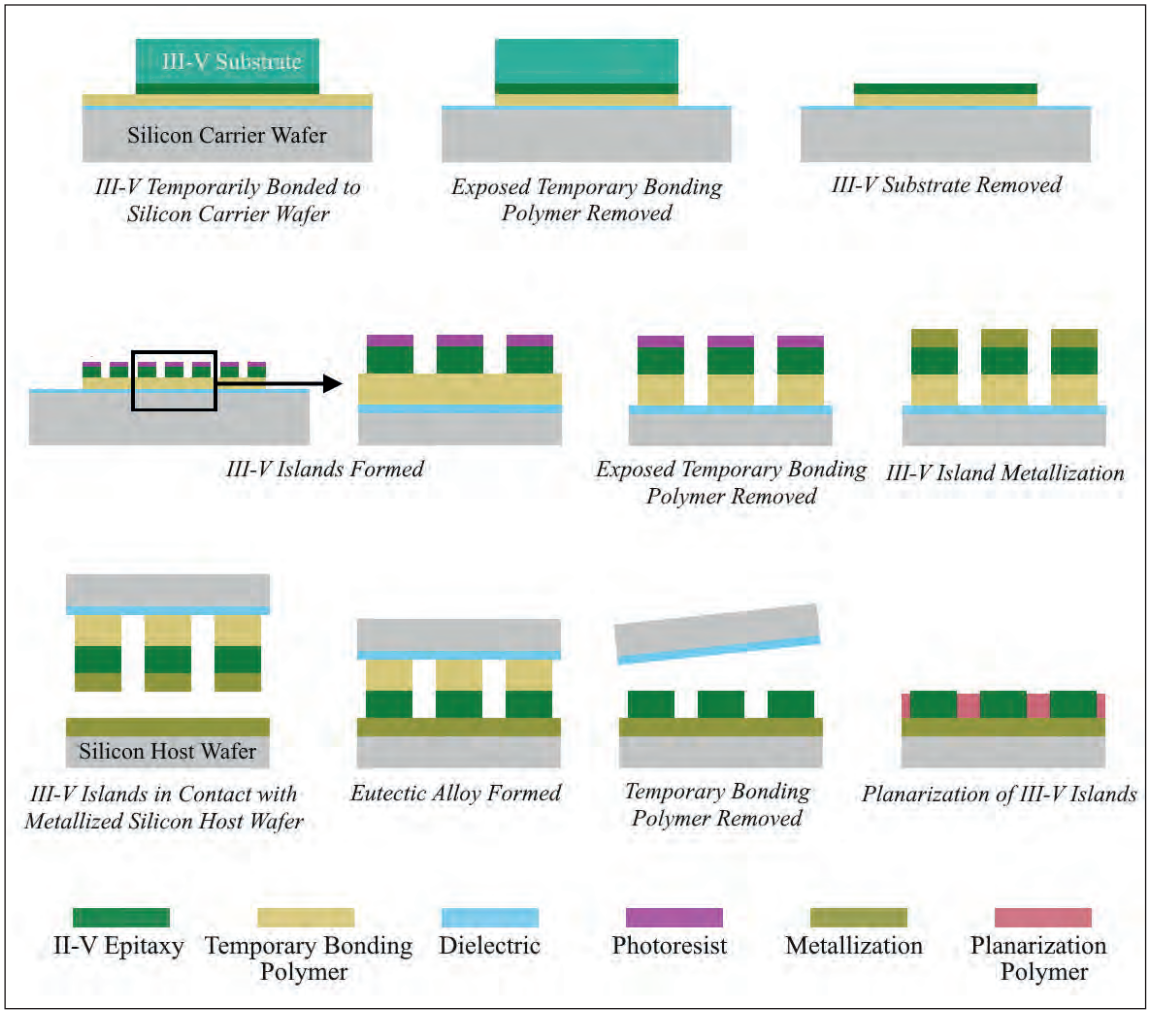
From facial recognition in smartphones to autonomous vehicle object detection and data communication, VCSELs serve ubiquitously in modern consumer and enterprise applications. Yet despite all this success they have their weaknesses. One major concern is a device performance that plummets under high-temperature, compounded by a poor thermal conductivity of the GaAs substrate. Another issue is an emission wavelength that shifts with temperature, creating challenges for some elements that may be in the optical path, such as diffractive optics, gratings, and filters.

To combat these concerns, we are pioneering integration of VCSELs via epitaxial transfer from GaAs to silicon. This new foundation alleviates heating effects in VCSELs, resulting in improved efficiencies and wavelength stability, even at elevated temperatures.

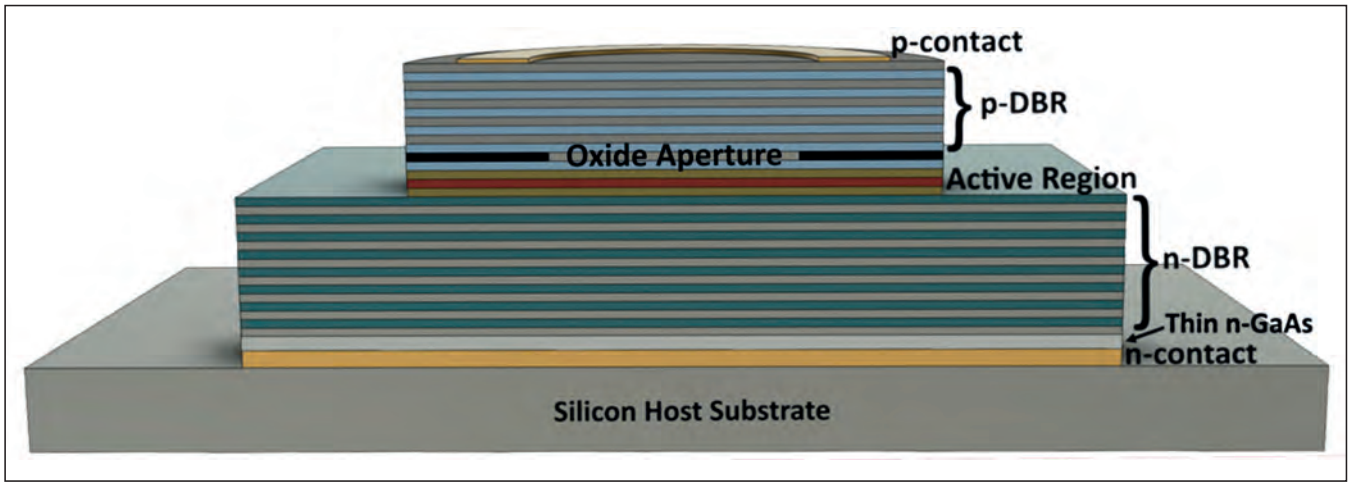
We have demonstrated the benefits of this approach by forming a permanent bond for the VCSEL epitaxial islands with a Pd/Ge stack, which is a standard gold-free *n*-contact for GaAs-based devices. We metallize the silicon host with a Ti/Al stack, chosen because titanium improves adhesion and aluminium forms a eutectic alloy with germanium on the epitaxial islands. The Ti/Al stack provides an *n*-side contact for the VCSELs, where a probe area for testing is available via exposed metal between these devices (see Figure 5 (a)).

The VCSELs we fabricate on integrated epitaxial material have a standard device structure, a 10 μm-diameter oxide aperture, and a standard Ti/Pt/Au stack for the *p*-contact (see Figure 4). Gold, commonly used as a protective metal cap layer, fulfils that role in these VCSELs. However, it could be replaced by a different metal to maintain CMOS compatibility for fully integrated devices.

To evaluate the thermal performance of our



➤ Figure 3. III-V epitaxy integration on silicon process flow (not to-scale).

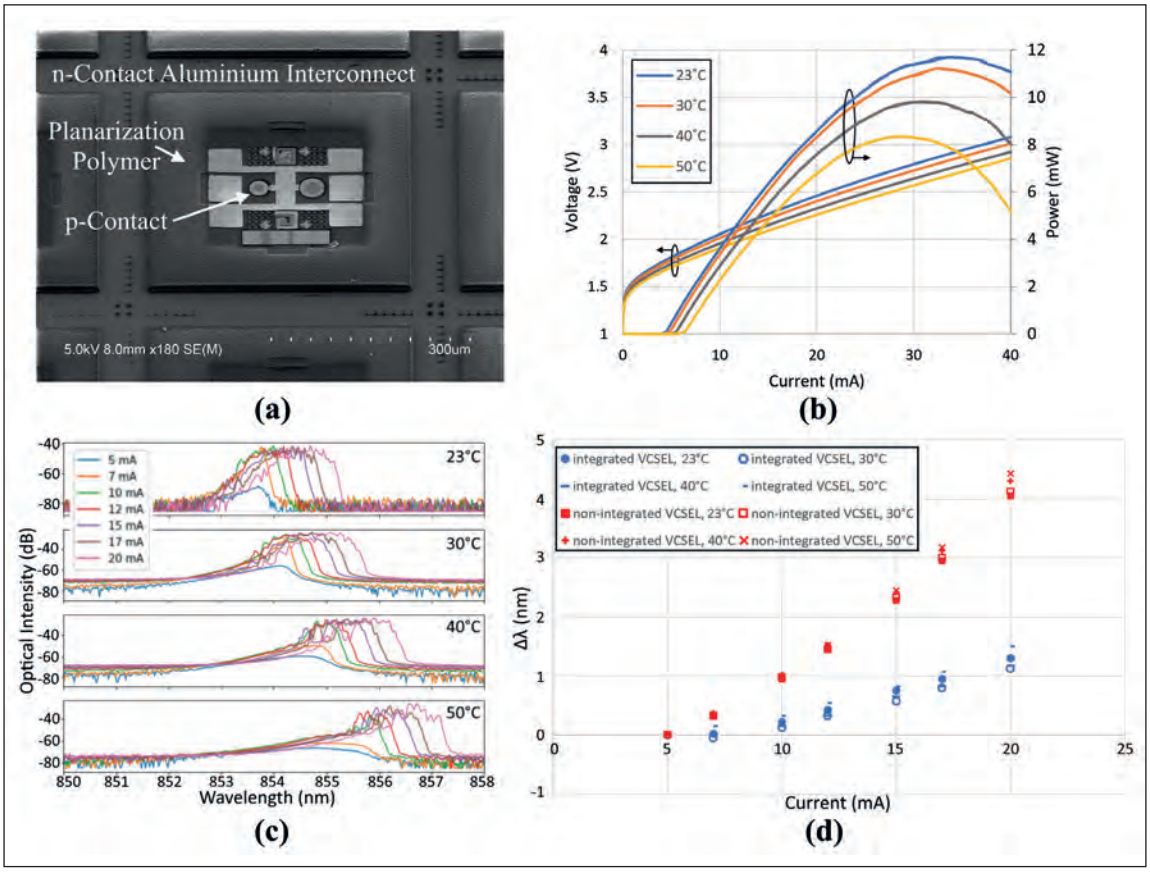


➤Figure 4. The integrated VCSEL pioneered by the team from the University of Illinois at Urbana-Champaign benefits from removal of the GaAs substrate.

integrated devices, we tested them from room temperature (23 ˚C) to 50 ˚C, using a thermoelectric cooler operating under reverse bias to adjust the temperature of the devices. Tracking the temperature was a temperature probe, while wafer probes provided current injection and measured the voltage outputs. To measure the VCSEL's optical output, above this device we placed a ball-lensed optical fibre probe, connected to a Newport 818-UV photodetector with an OD-3 attenuator.

Our measurements showed that our VCSELs are capable of CW operation at room temperature, with a threshold current of approximately 4 mA and a rollover at 33 mA.

Our value for the threshold current is common for non-optimized VCSELs of the given oxide aperture size, but the thermal rollover occurs at a much higher current than usual, indicating an improved thermal environment for the device.



➤ Figure 5. Integrated VCSEL results. (a) Scanning electron microscopy of VCSELs. Left: 10 μm oxide aperture VCSEL, right: unused, 20 μm oxide aperture VCSEL. (b) Light-current-voltage (L-I-V) measurements of VCSEL from room temperature (23 ˚C) to 50 ˚C. (c) Optical spectra of a VCSEL from room temperature (23 ˚C) to 50 ˚C, for drive currents from 5 mA to 20 mA. (d) Comparison of normalized leading peak wavelength shift between an integrated VCSEL and a non-integrated VCSEL of similar oxide aperture size.

At the elevated temperature of 50 ˚C, the threshold current increased to approximately 6 mA and the rollover decreased to 29 mA. These shifts from room-temperature values are consistent with the whole device heating to the set temperature. Differential resistance for our VCSEL is 37 Ω at room temperature and 33 Ω at 50 ˚C. These values are relatively low, thanks to removal of the thick GaAs substrate from the current path.

Another benefit that stems from the improved thermal environment of our VCSELs is the quashing of the temperature-induced wavelength shift with current injection. Measurements of VCSEL emission spectra – recorded by positioning an optical fibre, connected to an optical spectrum analyser, above the centre of the device – revealed that compared with a non-integrated device of similar aperture size, our variant produces a three-fold decrease in red-shift with current (see Figure 5 (c) and (d)). In comparison to flip-chip bonded VCSELs with a similar aperture size, our VCSEL bonded via epitaxial transfer has around a seven-fold decrease in red-shift, according to reports in the literature. These results highlight the significantly enhanced wavelength stability of integrated VCSELs produced by the epitaxial transfer integration technique compared with their state-of-the-art standalone siblings.

Our work highlights the primary strengths of our process: it's wafer scale, and its capability to form photonic devices on silicon with precise referencing to features on the silicon host. We are encouraged that our results do not just show parity of performance for our VCSEL, but improved performance. This highlights the potential of this process for large-scale electronic-photonic integration. The possibilities, including highly compact systems for 3D imaging and data transmission, are endless.

This feature draws upon work supported by the National Science Foundation under Grant No. (1640196). The authors are additionally thankful for support provided by the II-VI Foundation. Figure 5 (a), (c), and (d) are variations upon figures first presented in Espenhahn, 2022 cited below in "Further Reading".

FURTHER READING

- J. Dallesasse *et al*. "Heterogeneous Integration for Silicon Photonic Systems: Challenges and Approaches." 2021 5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM). IEEE, 2021.
- L. Espenhahn *et al*. "Heterogeneously integrated VCSELs on silicon." Vertical-Cavity Surface-Emitting Lasers XXVI. 12020 SPIE (2022)
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The glorious gate oxide

Should one worry about the lifetime of the gate oxide of SiC power MOSFETs under negative gate stress? Absolutely not, now that experiments show that they last as long as they do under a positive gate stress

BY SATYAKI GANGULY, BRETT HULL, DANIEL LICHTENWALNER AND JOHN PALMOUR FROM WOLFSPEED

➤ Top: The world's first 200 mm SiC wafer fabrication facility, located in Mohawk Valley, NY.

ONE OF THE GREATEST strengths of the 4H form of SiC is an electric breakdown field that is around ten times that of silicon. This means that for a given voltage rating, SiC power devices can feature a thinner drift region and higher doping than their silicon counterparts. In turn, this allows SiC power devices to have a far lower on-resistance (see Figure 1) and a simple unipolar MOSFET structure – there's no need for complex architectures, involving super-junctions or bipolar conduction. On top of this, SiC power devices have low leakage currents at relatively high temperatures, and a high thermal conductivity that supports higher current densities, enabled by the low on-resistance.

Drawing on all these attributes, SiC MOSFETs have demonstrated clear-cut advantages over other material systems, in terms of power density, efficiency, switching speed and thermal management. So significant are these gains that if every data centre on Earth used SiC instead of the incumbent, silicon, Manhattan could be powered for an entire year by the energy savings provided by this wide bandgap material.

The success story of SiC power devices dates back to just after the turn of the millennium. One of the key milestones came in 2002, when our company, Wolfspeed, released its first commercial 600 V junction-barrier Schottky diode. In 2011 we followed this up with the launch of the industry's first SiC MOSFET, rated at 1200 V; and within a further three years we had introduced the world's first 1700 V SiC half-bridge module.

More recently we have been grabbing the headlines for our efforts at increasing production capacity. This April we opened the world's first 200 mm SiC wafer fabrication facility, heralding the electrifying present and future of SiC power devices.

We are not alone in producing SiC power devices, which are finding deployment in automotive, renewable energy, power supply, and industrial applications. Setting us apart from our peers is the broadest commercial portfolio, which currently includes SiC MOSFETs and Schottky diodes in both discrete package and bare die form, as well as power modules. Our SiC MOSFETs scale from 650 V to 1700 V, with on-resistances ranging from 10-1000 mΩ; and our family of Schottky diodes span 600 V to 1700 V, with a best-in-class forward-voltage drop that trims conduction losses and boosts overall system efficiency. We continue to diversify, recently introducing 650 V Schottky diodes in a compact QFN 8 mm by 8 mm package, and 650 V MOSFETs in a TO lead-less package that have a footprint 60 percent smaller than the through-hole packages on the market today. Another breakthrough has been the introduction of our E-Series family of

power devices: they are automotive qualified, humidity robust, and optimized for on-board automotive charger, DC/DC converter and drivetrain applications, as well as PV inverters. This launch has further bolstered our reputation for SiC devices in the automotive market space.

Evaluating reliability

SiC power devices offer a level of reliability that is already excellent and on an upward trajectory, thanks to continual advancements in SiC substrate quality, epitaxial growth capabilities and device processing. However, harsh operating conditions, combined with ever demanding and evolving market requirements, are driving gate oxide reliability requirements for SiC power devices ever higher.

There are two key aspects to gate oxide reliability: threshold voltage stability and gate oxide lifetime. Nobel-prize-winning physicist Herbert Kroemer once famously remarked that the 'Interface is the device', and rightly so. Owing to differences between SiC and silicon MOS interfaces, SiC gate oxide reliability has always been carefully scrutinized, and judged against the gate oxide reliability of silicon devices.

The threshold voltage stability for the SiC MOSFET is, in general, similar to that for its silicon sibling. However, there are fundamental differences between the two material systems. They include smaller conduction band and valence band offsets between the 4H polytype of SiC and SiO_2, compared with silicon and SiO_2; the higher interface trap density for the 4H-SiC MOS device; and a difference in the interface chemistry – a nitrided gate oxide is employed for SiC, and hydrogen passivation for the SiO_2/silicon interface. Due to all these differences, it is likely that threshold voltage shift mechanisms could differ between SiC and silicon MOS devices.

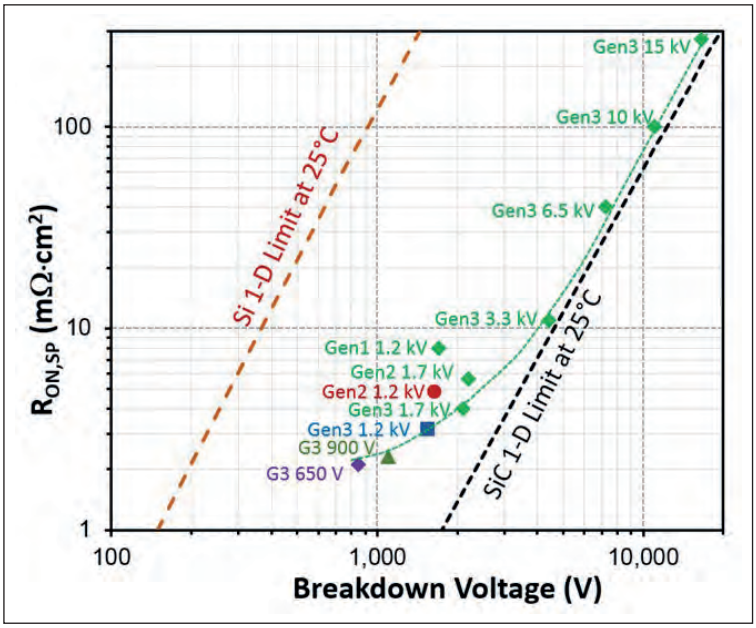
Within the wide bandgap community, much effort has been devoted to uncovering the mechanisms behind the observed shifts in the threshold voltage of SiC MOSFETs, using bias-temperature instability tests. These investigations have considered both positive and negative gate biases, and demonstrated threshold stability, alongside long-term reliability for practical applications.

The second part of gate oxide reliability, which is gate oxide lifetime, has also been carefully studied for SiC MOS devices. Our company has reported an attractive median time-to-fail gate oxide lifetime of 10,000 years at 175 °C and at a gate oxide electric field of about 4 MV/cm for *n*-channel SiC power MOSFETs through both constant and ramped positive gate bias time-dependent dielectric breakdown studies.

For silicon MOSFETs, the time-dependent dielectric breakdown is arguably one of the most well characterized and cited failure mechanisms of all time. While several models exist, for SiC the majority of researchers use the linear thermochemical electric field model to explain the time-dependent dielectric breakdown. This tends to provide the most conservative estimation. Of the two more common alternatives, the model that considers the inverse of the electric field gives extremely optimistic intrinsic lifetime extrapolations, so its validity is questionable; and the model based on a power-law governed by voltage is unsuitable, because it's been developed for ultra-thin gate oxides. Due to these issues, it's hardly surprising that the linear electric field model is widely used for SiC. This model assumes that a positive gate voltage results in the tunnelling of carriers, which create defects in the oxide film. When these defects reach a critical point, they initiate dielectric breakdown at that local weak point.

Evaluating negative bias

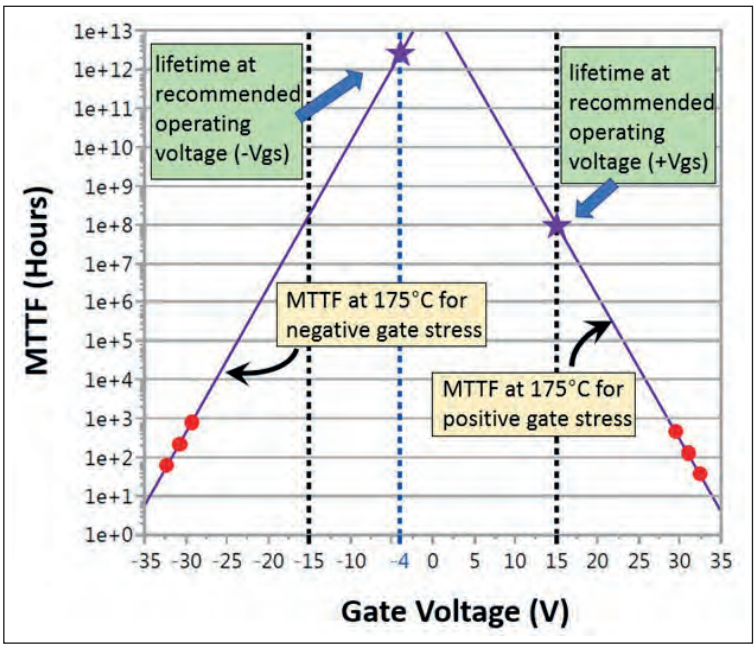
The curious reader may have noticed that while the SiC community's discussions on the threshold voltage stability encompass both positive and negative gate biases, when it comes to gate oxide lifetime, the focuses is on the positive gate bias stress for *n*-channel SiC MOSFETs. That limitation occurs because, until our recent efforts, there has been little to no work published on the gate oxide lifetime under negative gate bias for SiC MOSFETs. This is surely a significant omission, given that to turn these enhancement mode *n*-channel devices off, the channel is shut down by taking the gate bias well below the gate threshold voltage, and at



➤ Figure 1. Unipolar one-dimensional specific semiconductor drift on-resistance ($R_{ON,SP}$ in mΩ-cm²) versus breakdown voltage. Dashed orange and black lines show the theoretical limits at room temperature (RT) for silicon and SiC respectively. The RT data points represent various generations and voltage ratings of Wolfspeed SiC MOSFETs, and the green dashed line is a guide to the eye for that data. Adapted from J. W. Palmour et al., Proceedings of the 26th International Symposium on Power Semiconductor Devices & IC's, June 15-19, 2014.

least down to 0 V. From a blocking perspective, devices have no trouble realising this at 0 V gate bias. However, during turn-off, device performance improves by applying a gate bias well below 0 V. Turning MOSFETs off with a negative gate bias trims the turn-off energy loss by increasing the gate current during the turn-off transients – in turn, this forces the gate capacitance to discharge quicker than if turned off using a 0 V bias. Another point to consider is that in systems that employ multiple devices in either a parallel or a bridge configuration, devices tend to be turned off with a negative gate bias. This approach is employed because it provides further protection against parasitic turn-on, which can occur with unbalanced transients across multiple chips in a system. The importance of negative gate bias, and subsequently the necessity of gate oxide lifetime study of SiC power devices under such bias condition, certainly calls for careful investigation thus far overlooked.

To improve the understanding of the gate oxide reliability of SiC MOSFETs under a negative gate bias, we have performed constant voltage time-dependent dielectric breakdown testing on our Gen3 1200 V discrete MOSFETs at 175 °C, with applied negative gate biases much higher than the maximum recommended operating gate voltage of -4 V. Keeping source and drain at ground potential, we evaluated around 30 devices at these three gate stress voltages: -29.5 V, -31 V and -32.5 V. We monitored the gate leakage current of each device individually, which enabled us to collect the individual failure times of the stressed devices during these accelerated tests. For a true comparison, we also performed a positive gate bias time-dependent dielectric breakdown study with gate stress voltages of +29.5 V, +31 V and +32.5 V on Gen3 1200 V devices, using an identical sample size to that of the negative bias case.



➤ Figure 2. Wolfspeed Gen3 MOSFET time-dependent dielectric breakdown (TDDB) median-time-to-failure (MTTF) versus gate stress voltage at 175 °C. Red data points represent the extracted MTTF values at the gate stress voltages tested, while solid lines are the fit and extrapolation as described in the text. Stars represent fiducial points to illustrate the predicted MTTF lifetime at the recommended operating gate voltage stress condition (both positive and negative). Adapted from S. Ganguly *et al.*, IEEE International Reliability Physics Symposium (IRPS), pp. 8B.1-1-8B.1-6, 2022.

We found that the failure times for each of the stress conditions followed a well-behaved Weibull distribution. The extracted value for a characteristic that's referred to as Weibull β – it's known as the shape parameter, and it represents failure rate behaviour – is well above 2, indicating an intrinsic wear-out failure mechanism under both positive and negative gate stress. As we found similar failure time distributions and values for Weibull β, we were able to conclude that it is likely that there are similar failure mechanisms under both positive and negative gate biases.

Drawing on the Weibull failure time distribution, the linear electric field acceleration model and the maximum likelihood estimation, we extracted values for the median time to fail and extrapolated the lifetime. We found that the lifetime for the gate oxide is nearly identical for positive and negative bias, with a median time to fail of around 10,000 years (this is for conditions of 175 °C and a gate stress at -15/+15 V, which corresponds to a gate oxide electric field of about 4 MV/cm). We wish to point out that as the recommended negative gate-source voltage of -4 V for a MOSFET to turn-off the channel is generally much lower than the recommended positive gate-source value of +15 V during on-state, the oxide lifetime during the off-state should be much longer than it is during on-state operation (see Figure 2).

At this point, while you may be impressed by the stellar SiC MOSFET gate oxide lifetime under negative gate bias, you might be wondering what is the physical explanation behind this observation. Let us try to explain in a little detail. As we have already mentioned, tunnelling is to blame for the time-dependent dielectric breakdown of the gate, with breakdown occurring once defect accumulation reaches a critical point. It follows that if the levels of current flow under positive and negative gate bias are similar, so will be the extent of damage occurring in the gate oxide, and thus the resulting gate oxide lifetime. This view is credible, given that electrons under positive gate bias see an energy barrier of around 2.8 eV, and holes under negative gate bias see an energy barrier of 2.9 eV. Further support for this view comes from our TCAD simulations and electrical measurements. They show that the similar barrier heights lead to a similar level of Fowler-Nordheim tunnelling current flow under both positive and negative gate biases, thus accounting for the similarity in gate oxide lifetime in the two cases.

We have also established a correlation between the failure locations in a MOSFET unit cell and the failure signatures during time-dependent dielectric breakdown stress. The gate leakage profiles from the time-dependent dielectric breakdown stress under a negative bias show two distinct failure signatures – a soft fail, 'A', and a hard fail, 'B' – under all three stress voltages (-29.5 V, -31 V, and -32.5 V). We found that the post-failure leakage in type 'A' devices is orders of magnitude lower than it is in type 'B' failed devices.

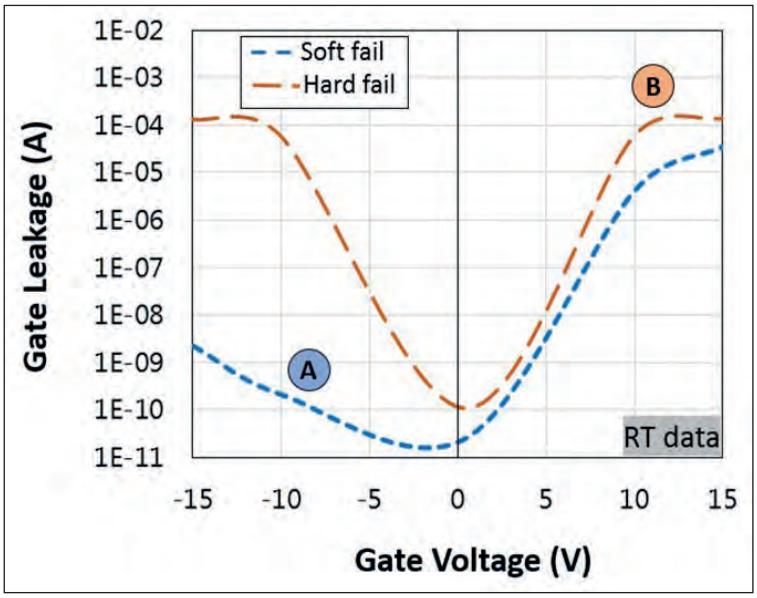
As part of this study, we have measured the room-temperature gate leakage current at a range of gate voltages (see Figure 3), for failing devices with differing *in-situ* leakage signatures. When applying a positive gate voltage sweep, we found that the 'A'-type and 'B'-type devices had very similar, high current levels of more than 10 μA at gate-source voltage of 15 V. But when we swept with a range of negative gate voltages, results differed markedly. The 'soft' fail devices, which we've labelled type 'A', exhibited a current that's lower by orders of magnitude than the type-'B' devices, which encountered hard failure. This observation is consistent with *in-situ* data recorded at a higher bias and temperature during the time-dependent dielectric breakdown stress.

Our next step involved trying to determine whether the different electrical failure signatures – that is, the type 'A' and the type 'B' devices – have any degree of correlation with the failure locations in a MOSFET unit cell. To see whether this is the case, we undertook physical failure analysis, involving thermal imaging followed by focused ion-beam cross-section and scanning-electron microscopy imaging. These forms of microscopy were performed on multiple failed devices that have the two different failure types.

Inspecting these devices revealed that the subset with a soft fail ('A'-type) signature had a gate oxide rupture in the JFET gap of the MOSFET (see Figure 4(a)). On the other hand, those with the hard fail ('B'-type) signature had a gate oxide rupture in the n^+/*p*-well area of the MOSFET (see Figure 4 (b)). This is not just a mere coincidence: it is repeatable across many devices, and it can be explained by considering the energy band diagram of the poly-SiO_2-SiC interface.

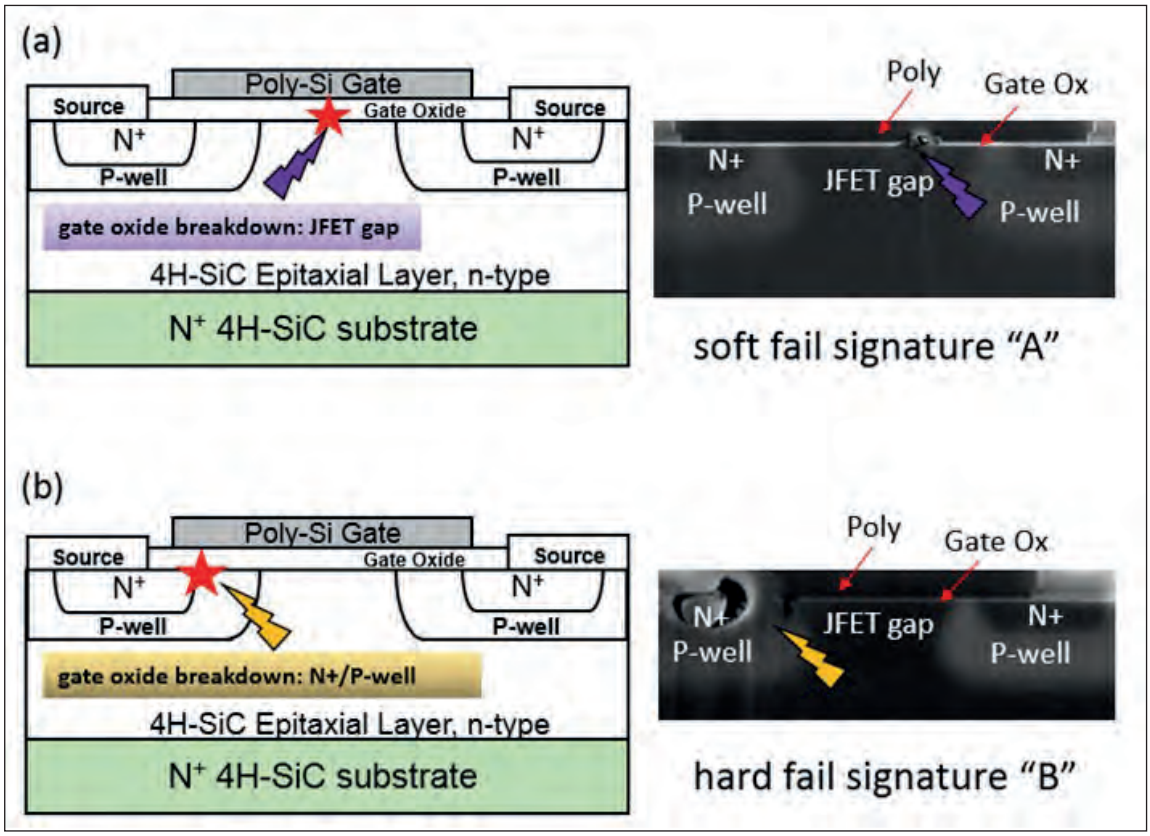
Enthusiastic readers can find a detailed account of our explanation in a paper published earlier this year (for details, see 'Further Reading'). Here, we offer a simpler alternative. It is our view that during the time-dependent dielectric breakdown stress, if there are gate oxide ruptures in the SiO_2, the likelihood is that this will convert the poly-SiO_2-SiC interface to essentially a Schottky junction. For the poly-SiO_2-SiC that sits over the *p*-well, the majority-carrier holes will accumulate there under a large negative gate bias. Meanwhile, for the poly-SiO_2-SiC over the n^+ source, the abundance of the majority-carrier electrons will remain, even under a negative gate bias. It's a different state of affairs, though, when the rupture takes place in the low-doped *n*-type SiC JFET gap region. In this case, electrons will deplete under a similar bias condition. This is consistent with our electrical measurements – and offers an explanation of why there is a much higher current under large negative gate bias when the gate oxide breakdown occurs in the n^+ or *p*-well region, than when the rupture occurs in the depleted *n*-type SiC JFET gap.

For the ruptured areas under positive bias, current flow will always be high under positive bias,



➤ Figure 3. Post time-dependent dielectric breakdown negative gate stress failure, at room-temperature. Typical gate leakage versus gate voltage current sweep data for devices with two distinct failure signatures ('A': soft fail, 'B': hard fail). During positive sweep ($V_{GS} > 0$) leakage levels are similar in 'A' and 'B', whereas during negative sweep ($V_{GS} < 0$) the leakage level of 'B' is orders of magnitude higher than 'A'. Adapted from S. Ganguly et al., IEEE International Reliability Physics Symposium (IRPS), pp. 8B.1-1-8B.1-6, 2022.

Our work shows that the gate oxide lifetime extracted from our devices under normal operating and accelerated negative gate bias conditions is a very close match to that extracted from positive gate stresses



➤ Figure 4. Schematic cross section as well as focused ion beam, cross-sectioned scanning electron microscopy images, showing gate oxide rupture after negative gate bias time-dependent dielectric breakdown (TDDB): (a) in the JFET gap for the type 'A' soft-fail electrical signature, (b) the n^+/p-well for the type 'B' hard-fail electrical signature. Adapted from S. Ganguly et al., IEEE International Reliability Physics Symposium (IRPS), pp. 8B.1-1-8B.1-6, 2022.

because electron accumulation can take place at the n^+ source and at the *n*-type SiC JFET gap region. In the case of failures above the *p*-well, even though majority carrier holes will be depleted at the *p*-well and poly(/SiO_2) interface under a positive bias, there is still a high current due to inversion electrons in the *p*-well. So, regardless of whether the gate oxide rupture take place in the *n*-type JFET, the *p*-well or n^+ area, the resultant gate current level will remain high under positive gate bias.

Our work shows that the gate oxide lifetime extracted from our devices under normal operating and accelerated negative gate bias conditions is a very close match to that extracted from positive gate stresses. This work should help alleviate any concerns regarding the gate oxide lifetime and failure mode under hole transport, rather than conventional electron transport. While our investigation considers a planar MOSFET design, it is possible that similar observations hold for other cell designs, such as those employing a trench. However, experimental verification is required before any claims can be made. Another key finding from our investigations is that the different electrical failure signatures that exist under negative gate time-dependent dielectric breakdown stress correlate with failure locations in a MOSFET unit cell. This observation promises to aid the early phase of any new process development, as it will allow the failure location to be identified from gate leakage data, without the need for physical failure analysis. We hope this insight, as well as others provided by our study, will help the SiC world to power up even more!

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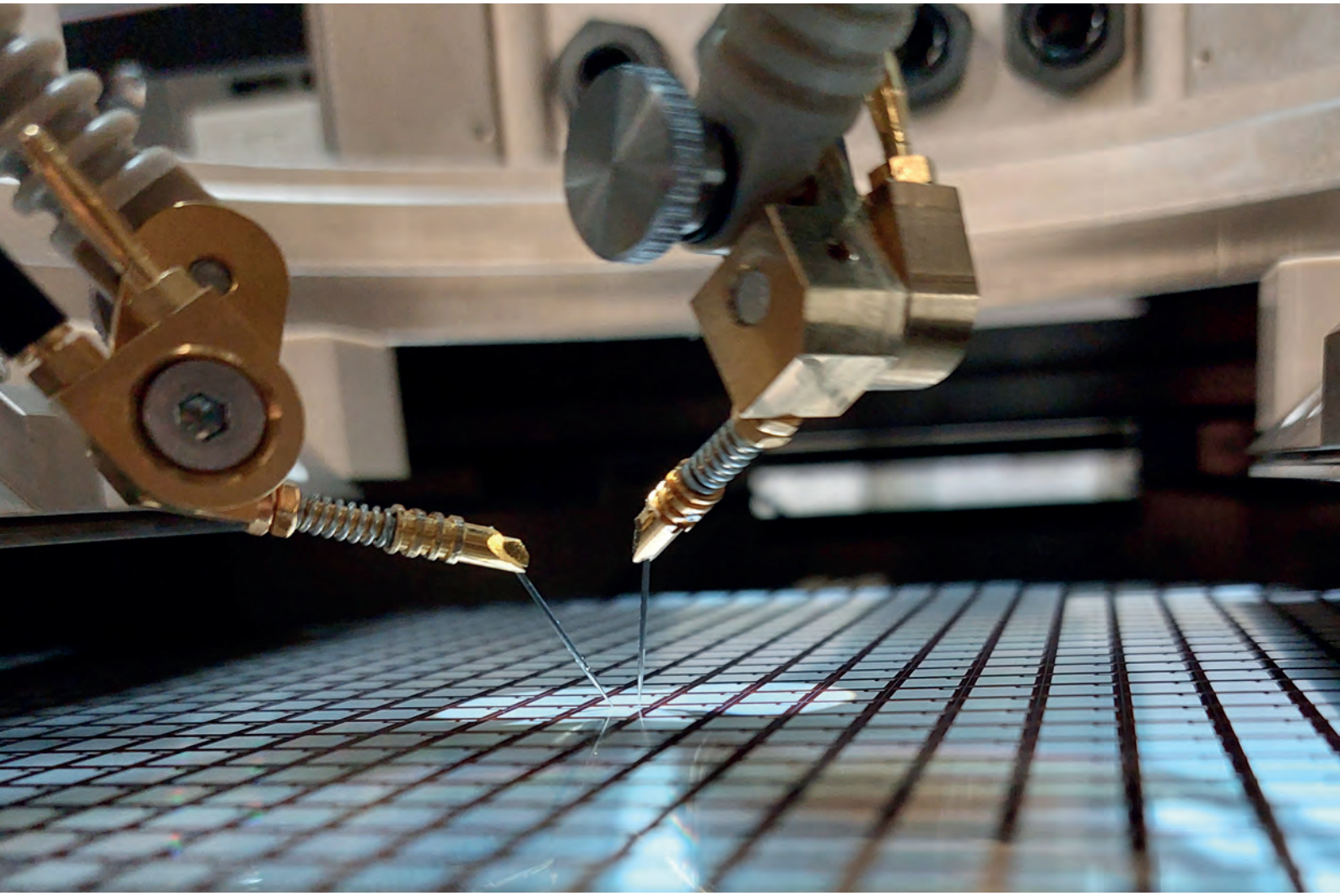


Cubic SiC: Tomorrow's champion for power electronics?

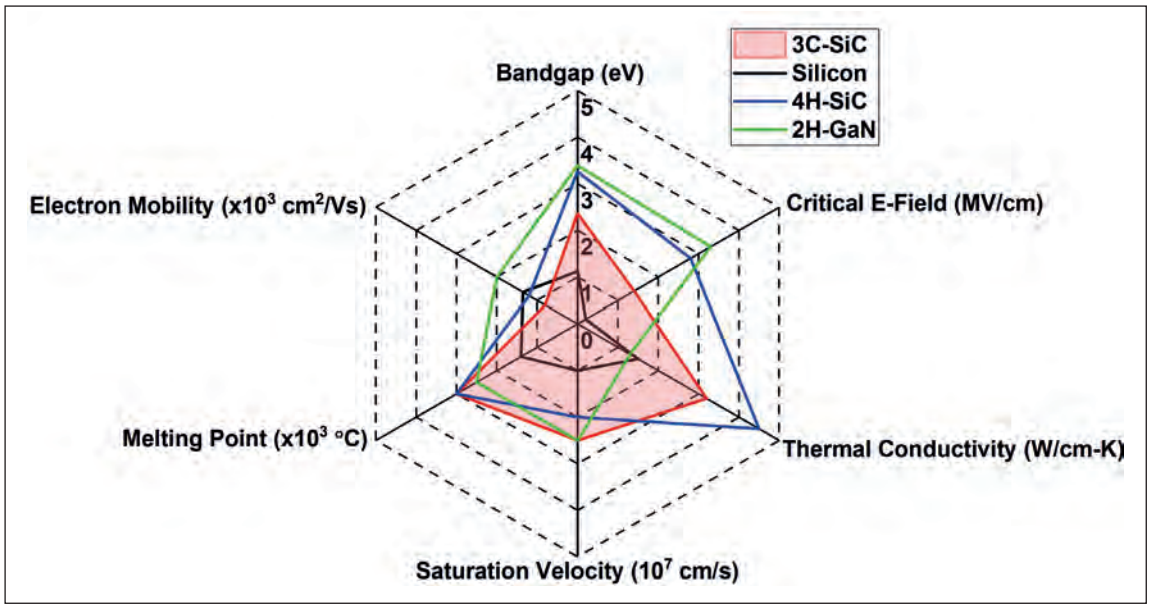
Offering the same crystal structure as silicon, alongside a wider bandgap and the potential for high reliability, what's to stop cubic SiC from playing a major role in tomorrow's power electronics industry?

BY MIKE JENNINGS FROM SWANSEA UNIVERSITY

THE UPTAKE of the Tesla is welcome on many fronts. Its lack of a combustion engine helps to trim carbon emissions; it is relatively quiet, thanks to battery power; and, much closer to home for those within the compound semiconductor industry, its early adoption of SiC power electronics is driving sales of these devices.

Where Tesla leads, other makers of electric vehicles are sure to follow. They too will employ SiC devices in their power trains, swelling sales of these wide-bandgap devices. Demand is tipped to be so strong that four of the leading makers of these chips – Wolfspeed, Infineon, STMicroelectronics and onsemi – are forecasting annual sales from this class of device to top $1 billion by the middle of this decade. Given the phenomenal success that SiC power devices are set to enjoy, one would presume that they are free from flaws. But that's not actually the case. There are, in fact, significant concerns relating to reliability, centred around the gate oxide.

The predominant role that SiC power devices have in electric vehicles is to convert the output from the battery, which is typically 800 V DC, to an AC form that drives a motor – producing up to 200



➤ Figure 1: Electrical and material properties radar chart of cubic SiC versus silicon and other commercial wide bandgap materials. This chart presents major semiconductor material parameters for power electronics applications.

kW or so of power. The voltage requirement is not particularly testing, as its well within the range of most conventional 4H-SiC devices, which span 650 V to 1.7 kV.

There are concerns surrounding the gate oxide because, like its silicon counterparts, the 4H-SiC transistor is based on a vertical MOSFET design. With this architecture failure of the gate oxide at elevated temperatures is a primary weakness. This is not that surprising, as the gate oxide used in this form of MOSFET is much thinner than its silicon equivalent, in order to maintain an acceptably low threshold voltage. Unfortunately, two unwanted consequences result from this thinner oxide: increased importance of the oxide-semiconductor interface, and an electric field inherent within the oxide that is typically two-and-a-half times that at the SiC surface.

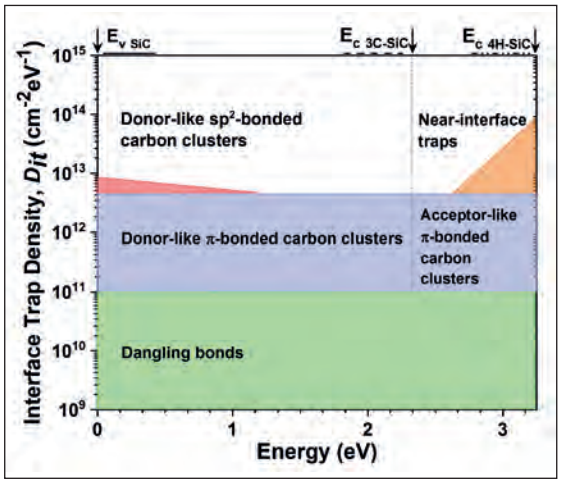
Both these issues are particularly troublesome in trench MOSFET architectures, because they are exacerbated by the trench corner. To counter this, those designing the latest trench MOSFET devices derate their blocking voltage capability to protect the fragile gate oxide.

Another option for addressing concerns related to reliability is to mirror the approach that's taken with GaN devices. Taking this tact has led some designers to advocate cascode co-packaged devices, such as the pairing of a 4H-SiC JFET with a silicon MOSFET. But this combination constrains performance, particularly at high temperatures.

Cubic SiC: a bastion for longevity

Enter cubic SiC, also known as 3C-SiC – an exciting material that promises to be 'Mr Reliable'! There's still much work to do with this polytype, as wafers and epitaxial layers are at a very early stage and hence, defective. However, massive strides in bulk material and the growth of 3C-SiC on silicon have been recently accomplished – they are detailed in the previous edition of this magazine by Francesco La Via from the Institute of Microelectronics and Microsystems at Catania, Italy.

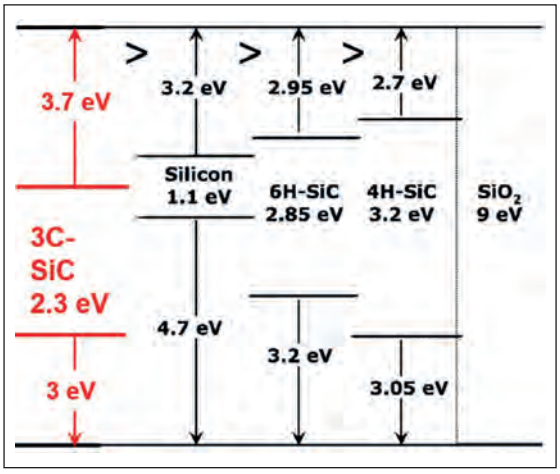
You may be wondering why so much excitement surrounds 3C-SiC. After all, compared with GaN and 4H-SiC it has a lower bandgap, a smaller critical electric field, a modest electron mobility and a low thermal conductivity (see Figure 1). Surely, this shows that 3C-SiC is inferior to those two wide bandgap titans, GaN and 4H-SiC.



➤ Figure 2: Interface trap density plot comparing cubic (3C-) SiC to commercial (4H-) SiC. 3C-SiC shows a favourable (or much reduced) trap density due to the absence of near-interface traps prevalent within the 4H- system. This is a plot is modified from R. Esteve, "Fabrication and Characterization of 3C- and 4H-SiC MOSFETs," Doctoral thesis, KTH Royal Institute of Technology, Stockholm, 2011.

While all of these pointers are valid, they overlook two crucial factors that are not covered within tables listing the properties of semiconducting materials: processing, including the quality of the interface, which may involve a metal or insulator; and reliability in the field. These are considerations that clearly matter. After all, what good is a wide bandgap material if it cannot be used to make a device, or one that only lasts for a single switching cycle.

Of course, these concerns don't apply to commercial 4H-SiC and GaN – but processing of these materials, particularly GaN, is radically different and more challenging than it is for traditional silicon. In comparison, 3C-SiC, with its cubic nature and a humble energy bandgap of 2.36 eV, is closer to silicon than the other members of the wide bandgap family. These traits offer many benefits when it comes to processing 3C-SiC into devices.



➤ Figure 3: Semiconductor-SiO_2 band offsets of other wide bandgap materials compared to cubic (3C) SiC, taken from F. Li *et al*. Materials **14** (2021)

Let's first consider the MOS interface. Power electronics applications engineers tend to want a high impedance gate, such as a MOS gate. That's proved elusive to the developers of 4H-SiC devices, who have been grappling with a poor MOS interface for the best part of 30 years – even today, it is still its Achilles heel. In the early days of the 4H-SiC MOSFET, inversion mobility was so poor – typically just 5 $cm^2\ V^{-1}\ s^{-1}$ – that the channel resistance constituted more than 90 percent of total device resistance. This is unacceptably high and untenable, in terms of utilisation within a power electronics converter. While poor mobility in 4H-SiC is now managed, as alluded to earlier, there are still problems associated with the move to trench architectures, centred around high-temperature reliability issues.

There are three main types of trap adversely affecting the MOS interface: near-interface traps; acceptor-like carbon clusters; and dangling bonds, which occur at the interface (see Figure 2 for an illustration of trap types, and a comparison of the 4H-SiC and 3C-SiC MOS interface). With 4H-SiC, the conduction band edge is swamped by all types of trapping mechanisms, including near-interface traps, which are the most dominant. In stark contrast, 3C-SiC is not affected by these near-interface traps. Of course, it is still hampered by acceptor-like carbon clusters, which have a far greater impact than dangling bonds. One key consequence of these three forms of trap is that alternative approaches to hydrogen annealing are typically required to passivate the SiC MOS interface.

What is the important takeaway from all these considerations? It's that far less effort should be required to realise higher channel mobilities, and thus lower on-state resistances, when it comes to 3C-SiC MOSFETs. In fact, efforts at developing 3C-SiC MOSFETs are already bearing fruit, with mobilities of more than 100 $cm^2\ V^{-1}\ s^{-1}$ demonstrated. It is worth noting that in addition to these results for 3C-SiC-on-silicon, there is work with bulk 3C-SiC that indicates improved performance and commercial viability for *p-n* diodes. Potential merits of bulk 3C-SiC, as opposed to the heteroepitaxy of 3C-SiC on silicon, include ease of processing technology with respect to ion implantation and metallisation. There is also the promise of scaling the voltage through adjustments to layer thickness, an attractive attribute from a commercial standpoint. This feature is especially welcome at voltages beyond 650 V, where there is competition from silicon MOSFETs, superjunction devices, insulated gate bipolar transistors, 4H-SiC MOSFETs and GaN HEMT topologies.

At Swansea University, our team is working to prove these new materials for automotive applications. The automotive and aerospace industries are notorious for insisting upon the highest reliability standards whilst keeping the cost to a minimum. That means testing gate oxides to high temperatures and

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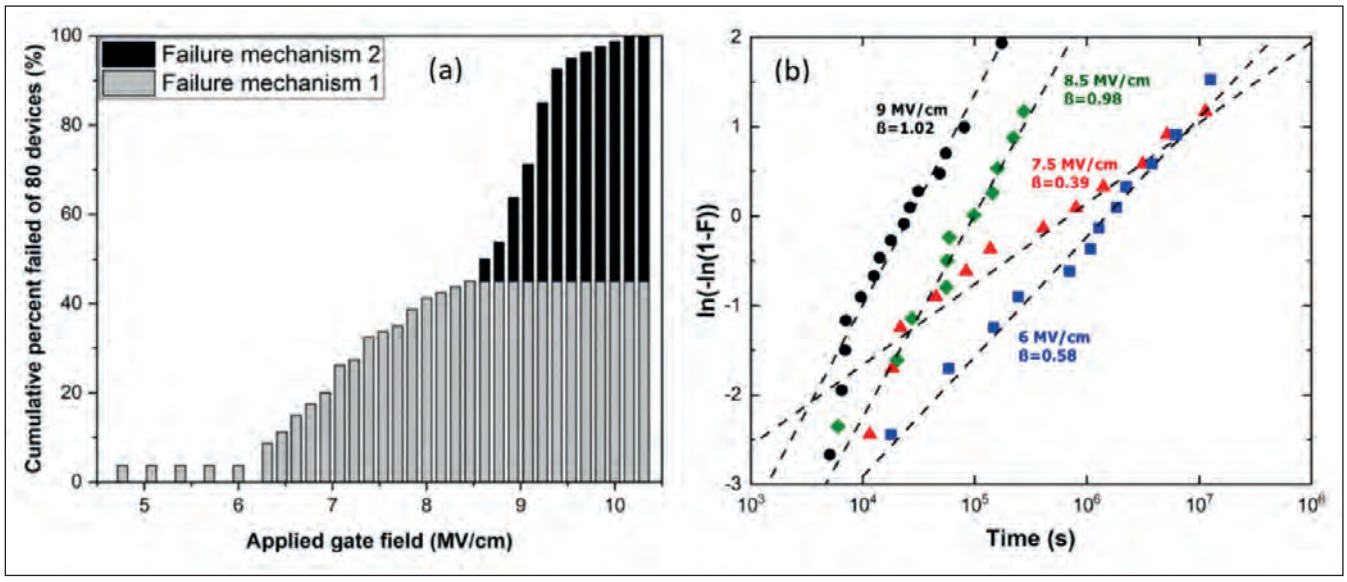

➤ Figure 4: Distribution of failures of 3C-SiC MOS capacitors for varying electric fields (a) and corresponding Weibull distributions (b), taken from F. Li *et al*. Materials **14** (2021). The time dependent dielectric breakdown analysis is conducted at electric field values of 6 - 9 MV cm^{-1}. The failure percentage increases steadily up to an electric field strength of 8.5 MV cm^{-1}, above which, the failure number rapidly increases to 100 percent.

performing accelerated lifetime analysis at the chip-level. Physical considerations suggest that 3C-SiC could offer excellent reliability. Its band offset to the SiO_2 gate oxide is 3.7 eV, a value much larger than that for silicon and 4H-SiC (see Figure 3). This is a major asset, as for a given critical electric field for the dielectric, the tunnelling current through this oxide is exponentially dependant on the band offset, which is sometimes referred to as the barrier height. One consequence of this advantage is that the electric field within a 3C-SiC MOS system can be two-to-three times higher than that for 4H-SiC, for the same leakage current into the gate driver circuitry. Due to this, de-rating requirements for a 3C-SiC trench power MOSFET can be far less stringent than those for a 4H-SiC sibling.

The 3C-SiC MOS interface also promises a high level of gate oxide reliability and a long lifetime. Measurements by Swansea University in collaboration with Warwick University on a structure with an interface formed with a gate oxidation process based on N_2O show a stabilised leakage current and a critical electric field strength at around 8 MV/cm, which is the highest value observed for a 3C-SiC MOS structure. Even preliminary 3C-SiC MOS capacitors, formed on epitaxial material with an inherent high defect density, offer a breakdown field strength of 8 MV/cm, approaching values for 4H-SiC of typically 9 - 11 MV/cm.

Our team has recently carried out a time-dependent dielectric breakdown analysis of 3C-SiC MOS capacitors (see Figure 4). We attribute their low failures to crystal deficiencies in the 3C-SiC substrate that have an impact on the localised material properties. For high field failures – that's a field strength of more than 8.5 MV/cm – failures result from an increased leakage current, or impact ionisation, due to high critical electric fields.

The primary conclusion from this work is that even at high electric fields, exceeding 8.5 MV/cm, acceleration slopes remain low for 3C-SiC. These slopes are an order of magnitude lower than 4H-SiC, suggesting extrinsic defects are still the dominant failure mechanism overall.

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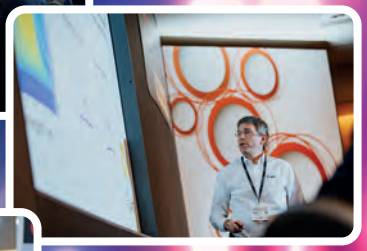
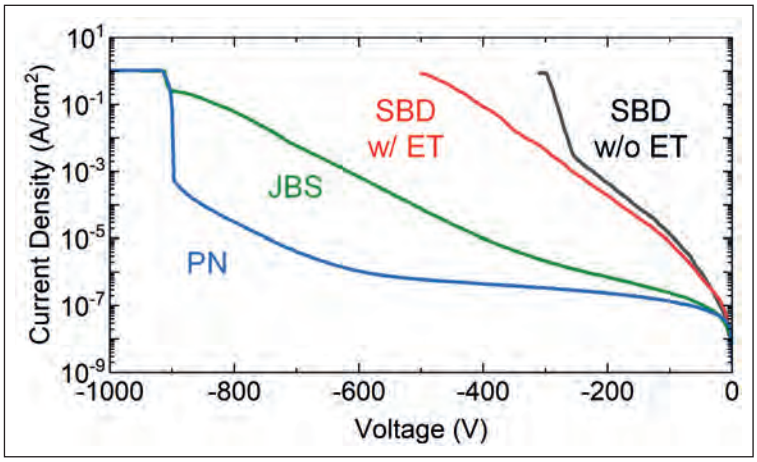


Realising implantation in GaN

Activating magnesium implantation with ultra-high-pressure annealing yields vertical GaN junction barrier Schottky diodes with exceptional performance

UNTIL VERY RECENTLY, there has been a glaring omission from the toolbox of engineers that work with GaN: the absence of an ion implantation process. But that has now been remedied, thanks to a process involving ultra-high-pressure annealing of magnesium dopants, developed by a team from the US and Poland.

According to Dolar Khachariya from Adroit Materials – speaking on behalf of the ground-breaking team that also includes those from North Carolina State University and the Institute of High-Pressure Physics, Poland – the ion-implantation and activation techniques that they have developed for GaN are successful and reliable.



➤ Reverse-bias measurements of the *p*-*n* diode, the junction barrier Schottky (JBS) diode, and the Schottky barrier diode (SBD) with and without edge termination (ET).

"This technique has allowed us to obtain kilovolt-class-blocking GaN junction barrier Schottky diodes on native GaN substrates," explained Khachariya, adding that realising even higher blocking voltages is relatively simple, as it just involves increasing the thickness of the GaN epilayer while maintaining the implantation and activation techniques.

Khachariya claims that if GaN-based junction barrier Schottky (JBS) diodes were manufactured by the team's approach, they would exceed the performance of existing SiC- and silicon-based devices and be significantly more cost-effective.

Although ammonothermal GaN, the ultimate form of bulk GaN, provided the foundation for the work of the researchers, Khachariya said that the same results should be possible with HVPE-grown GaN substrates.

To increase the current capabilities of the diode, larger-diameter devices are required. This is not an issue for GaN substrates grown by the ammonothermal method, because they have dislocation densities in the low 10^4 cm^{-2}. But Khachariya warned that for HVPE-grown GaN, there is the possibility that large-area devices might not work as intended, due to dislocation densities that are at least two orders of magnitude higher.

Fabrication of the team's diodes began by loading an ammonothermal n^+ GaN substrate into a vertical, cold-wall, RF-heated MOCVD reactor and depositing a 5 μm-thick *n*-type GaN drift layer with a net carrier concentration of around 1.3 x 10^{16} cm^{-3}. To realise a shallow box profile for implanted magnesium at a concentration of around 2 x 10^{19} cm^{-3}, the researchers employed a two-step implantation process, involving a tilt angle of 7°, ion energies of 75 keV and 25 keV, and corresponding doses of 2 x 10^{14} cm^{-2} and 4.4 x 10^{13} cm^{-2}, respectively. Subsequent heating of the sample to 1300 °C for 30 minutes at 400 MPa, under a nitrogen gas to prevent decomposition, activated magnesium ions in the sample.

JBS diodes with a 0.1 mm by 0.1 mm device area were formed by adding Ni/Au *p*-type ohmic contacts, followed by Ni/Au Schottky contacts, to the front of the device, and a Ti/Al/Ni/Au stack to the back side of the substrate. For comparison, the team also produced Schottky diodes with and without edge termination.

Electrical measurements of JBS diodes and Schottky diodes with edge termination revealed turn-on voltages of 0.75 V and 0.7 V, respectively, and an ideality factor of 1.03, indicating near-ideal Schottky behaviour. On-resistance for the JBS diode is just 0.6 mΩ cm^2, a value that is claimed to be among the lowest for all GaN-based JBS devices. Reverse-bias measurements showed that the leakage current in the JBS diode is far lower than that for both forms of Schottky diode (see Figure). The breakdown voltage of the JBS diode is a record-breaking 915 V, according to the team.

According to Khachariya, the next targets are the development of larger diodes that are capable of handling 1 A to 100 A, and devices with a higher breakdown voltage capability of around 5 kV, realised by increasing the drift epilayer thickness and further reducing *n*-type doping.

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3C-SiC enhances the GaN HEMT

GaN-on-silicon HEMTs with a 3C-SiC interlayer combine a relatively low transmission loss with a very high breakdown voltage

FOR THE PRODUCTION of GaN HEMTs for power and RF applications, the silicon substrate has its pros and cons. It majors on a large, low-cost and widely available platform, but it is impaired by significant thermal and lattice mismatches with the epilayers – this gives rise to a high density of dislocations and cracking, imperfections that compromise the device's performance, its reliability and its lifetime.

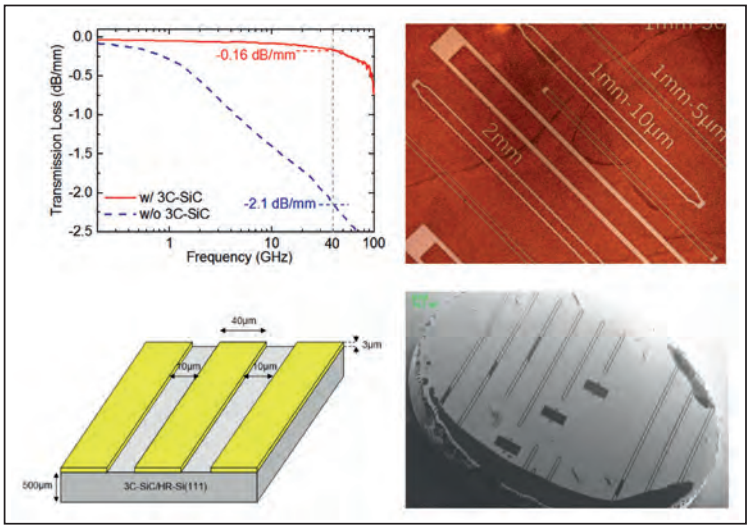
However, it appears that it's now possible to enjoy the benefits of silicon, without having to suffer the weaknesses, by inserting a 3C SiC interlayer. Efforts by an international collaboration – led by researchers at the University of Sherbrooke, Canada, and supported by those at the Center for the Development of Advanced Technologies, Algiers; Liverpool John Moores University, UK; and the French institutions LIMMS/CNRS-IIS and IEMN/CNRS – have led to the fabrication of GaN HEMTs with a relatively low transmission loss of 0.16 dB/mm at 40 GHz, and a soft breakdown voltage of around 1530 V at 1 μA/mm, which is said to be three times larger than that of conventional devices.

The foundation for this work is an engineered substrate produced by Air Water Corporation that combines 500 μm-thick, high-resistivity (111) silicon with a 3C-SiC transition layer. Air Water Corporation has been working on 3C-SiC since the 1970s, and in 1992 it filed it first patent on GaN on 3C-SiC.

"It seems that this company has great experience in co-doping 3C-SiC, and has achieved high-quality crystal structures and high electrical resistivity," remarked Brahim Benbackhti, who spoke to *Compound Semiconductor* on behalf of the collaboration, and is affiliated to both the University and Sherbrooke and the Center for the Development of Advanced Technologies.

Benbackhti and co-workers have investigated the growth of GaN-based structures on 3C-SiC-on-silicon, and also on just silicon, to provide a control – and they have fabricated and tested a range of devices produced from both these epiwafers.

Buffers for the devices were either a 3 μm-thick layer of AlGaN, employed for the control, or a 1.3 μm-thick layer of AlGaN deposited on a 1.7 μm-thick layer of vanadium-doped 3C-SiC. On both buffers the team added a 1.8 μm-thick $Al_{0.18}Ga_{0.82}N$ back barrier, a 150 nm-thick undoped GaN channel, and a 4 nm-thick $Al_{0.45}Ga_{0.55}N$ back barrier. *In-situ* growth of a 20 nm-thick SiN cap layer passivated the surface and prevented strain relaxation.



MOS HEMTs were fabricated with a source-to-gate spacing of 2 μm, a gate length of 1.5 μm, and a gate-to-drain distance of 15 μm. Measurements using coplanar waveguides, with dimensions optimised for 50 Ω impedance, revealed that inserting the 3C-SiC interlayer slashed transmission loss at 40 GHz from 2.1 dB/mm to just 0.16 dB/mm. This result is said to be superior to those obtained on substrates made from either GaN, high-resistivity silicon or diamond.

The researchers have also investigated the breakdown voltages of their transistors. The device with the conventional design exhibited an increase in leakage current beyond 300 V, with leakage hitting 1 μA/mm at 395 V. In comparison, the variant with the 3C-SiC interlayer required a drain-source voltage in excess of 1.5 kV to hit this value.

Benbackhti told *Compound Semiconductor* that reliability is the biggest obstacle to large-scale commercialisation of GaN-based devices with the 3C-SiC interlayers. "Therefore, the behaviour of the device and its lifetime, under different electrical and thermal stresses, needs to be investigated."

To date, GaN HEMTs with a 3C-SiC interlayer have been shown to be good candidates for power switching. "For RF power electronics, it is crucial to examine the thermal resistance introduced by the 3C-SiC interlayer, which could act as a thermal barrier and limit the device performance in RF," commented Benbackhti.

➤ Measurement on coplanar waveguide structures reveal a low transmission loss in GaN-on-silicon structures with a 3C-SiC interlayer.

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➤ A. E-H. Khediri *et al.* Appl. Phys Lett. **121** 122103 (2022)

UV irradiation exposes flaws at the interfaces of SiC and SiO_2

When nitridation is used to produce SiC MOSFETs, it creates traps that are activated by UV radiation and could thrwart device reliability

TO TRIM INTERFACE TRAPS in SiC MOSFETs and increase the channel mobility in this class of transistor, many makers of this device are employing an interface nitridation step involving nitric oxide.

However, this process has its downsides: it is thought to generate very fast states, and recent research by a team from Japan suggests that it also introduces additional traps, which are not active until irradiation by UV light. These traps have been shown to cause hysteresis and frequency dispersion in capacitance-voltage characteristics, and to threaten to impair the long-term reliability of metal-oxide-semiconductor (MOS) devices.

The team from Osaka University and the National Institute of Advanced Industrial Science and Technology gained these insights from fabricating and investigating a range of MOS capacitors on 4H SiC. Several samples were formed by taking 4H-SiC ($11\bar{2}0$) epilayers with a donor density of 1.5×10^{15} cm^{-3}, forming a gate oxide by heating at 1200 °C for 28 minutes, and then annealing under argon at 1200 °C for 30 minutes. These steps created a gate oxide with a thickness of around 55 nm. Variants were produced by NO nitridation of the material for either 10, 30, 60 or 120 minutes.

In addition to these samples, the researchers also produced: a reference on 4H-SiC (0001) with a donor density of $0.8\text{-}1.0 \times 10^{16}$ cm^{-3}; and a non-nitrided sample, formed by oxidation at 1600 °C in a 0.3 percent oxygen atmosphere.

To study the impact of UV light, the team placed their samples under vacuum, before subjecting them to an excimer source emitting at 172 nm. Irradiation lasted for 10 minutes, the longest time that the UV source could operate stably. Following irradiation, aluminium gate electrodes were added by vacuum evaporation to form MOS capacitors.

Plots of capacitance as a function of voltage at 1 MHz revealed just a small shift in the flatband voltage in nitrided samples, indicating that nitridation is effective in reducing interface defects. However, after exposure to excitation at 172 nm, nitrided capacitors exhibited a large hysteresis and a stretching out of the capacitance-voltage characteristics. In comparison, for the non-nitrided sample, there is minimal degradation with exposure to the excimer UV source.

As the energy of the 172 nm source is below the bandgap of SiO_2, UV light will pass through the SiO_2 film before reacting with the interface. So it follows that the nitridation process induces hidden traps that are near/at the interface and activated by UV light.

The researchers have also determined the density of interface traps in their samples, using forward capacitance-voltage characteristics.

Prior to UV exposure, the density of interface traps is lower in the nitrided samples, showing that this process improves interface quality. But after exposure to UV radiation, the nitrided samples suffer from a large increase in the density of interface traps near the conduction band edge, a finding consistent with high-frequency capacitance-voltage measurements.

Another part of the team's work has been the investigation of trap states near the valence band edge, realised by illuminating samples with emission between 250 nm and 450 nm during capacitance-voltage measurements. This particular study found that sample exposure to the excimer laser led to a hysteresis and stretch-out of the capacitance-voltage characteristics in the negative voltage region, indicative of trap states near the valence-band edge. In contrast, the non-nitrided sample showed little degradation from excimer excitation.

Electron injection stress tests have also been undertaken, involving the application of an oxide field of 6 MV cm^{-1} for up to 2000 s. The team found that after exposure to the excimer source, the flatband voltage increased in all nitrided samples, but not in the non-nitrided sample. This finding provides evidence that nitridation induces hidden near-interface oxide traps.

To sum up, the investigations by the team have shown that in nitrided structures, the excimer UV light activates electron and hole traps, as well as near-interface oxide traps. This has led the researchers to conclude that caution must be taken when implementing nitrided SiC MOS devices in harsh radiation environments.

REFERENCE

➤ H. Fujimoto *et al.* Appl. Phys. Express **15** 104004 (2022)

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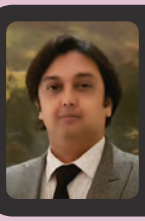

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