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CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

VOLUME 30 ISSUE IX 2024
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INSIDE

Promoting the PCSEL

There is no question that the PCSEL has a wonderful set of attributes. But can it find its killer application?

Solar cells: The hunt for 50 percent

Lattice-matched solar cells with five or six junctions look to surpass the conversion efficiency of 50 percent

Producing vertical GaN power devices

Tuning wafer bow by laser patterning enables the growth of thick epitaxial layers for vertical high-voltage devices

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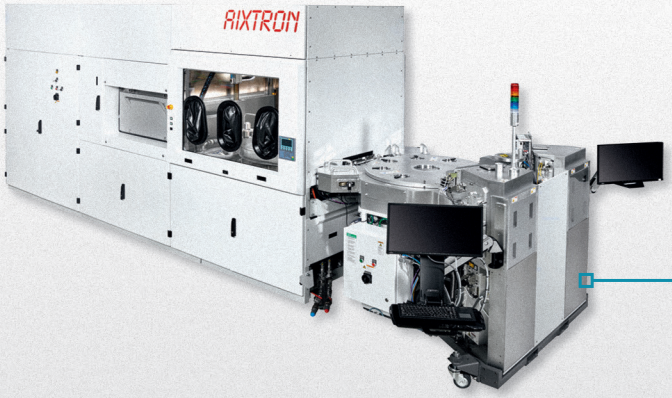
THE NEW G10 SERIES

Your Productivity Solution for All Advanced Epitaxy Materials



G10-SiC

- 9x150 mm (6") or 6x200 mm (8")
- New hardware & process surpassing Single Wafer Reactor uniformities
- +50 % productivity per fab area with large batch technology & small footprint

End Markets/Products:
EV inverters & charging infrastructure

G10-GaN

- 8x150 mm (6") or 5x200 mm (8")
- 1st fully automated compact GaN MOCVD cluster designed 100 % for Si Power fabs
- Novel hardware solution for unmatched barrier uniformities and device yields

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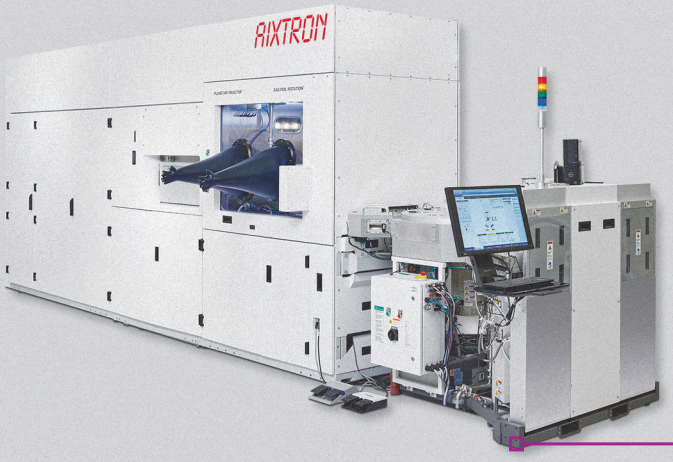

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End Markets/Products:
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VIEWPOINT

By Richard Stevenson, Editor

Milestones in time and space

There are a number of ways we can measure the growth of our industry. We can consider the annual revenue of all the devices we produce, or their total number, which is phenomenal. Or we could consider how dependent the world is on what we produce, or the number of people that our industry employs.

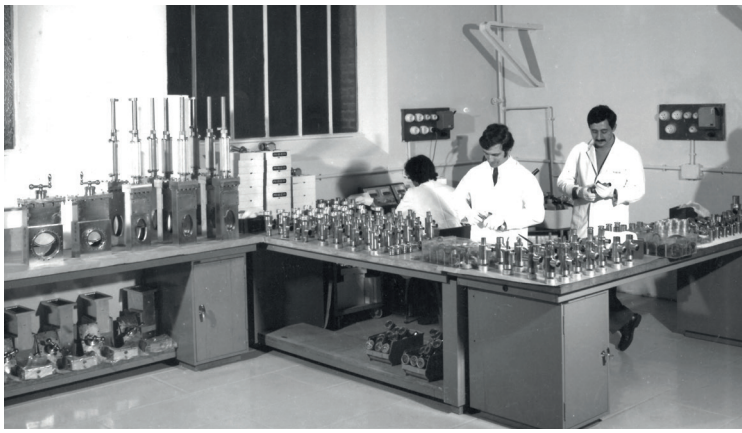
There are also simpler ways, involving less calculation and rigour, that offer a way to tell compelling stories about our industry's expansion. And while they are a little anecdotal, that doesn't stop them from making the point that the compound semiconductor industry is going from strength to strength.

In this issue you can read about how our industry continues to advance in time and space. There's a piece detailing the history of Riber, now celebrating its 60th anniversary, and another about Agnit Semiconductor, the nascent pioneer of GaN chipmaking in India.

Back in 1964, when four French engineers started Riber, the compound semiconductor industry did not exist. So, it's hardly a surprise that in the very early days, this firm focused on stainless steel fabrication and welding for vacuum applications, before diversifying, initially with Joule-effect evaporators and vacuum chambers. From there, the portfolio expanded to analytical instruments, such as Auger spectroscopes.

The defining moment came ten years after founding, when Klaus Ploog, a legend in MBE, called on Riber to build him a system for the epitaxial growth of films of GaAs. This first system paved the way for many more, first for research communities in academia and industry – still significant markets for Riber – and over the last few decades, for chip manufacturers.

While I'm sure Riber is well-known to you, you may not have heard to Agnit. It's a spin-out of the Indian Institute of Science, which provides an incubator for producing GaN epiwafers and power and RF devices.



Agnit has just raised $3.5 million, which will help increase the yield of its die, improve their reliability and enable the company to win qualification in a number of markets.

Within the GaN power market, IP is crucial. Agnit is strong on this front, drawing on technology developed by and licensed from the Indian Institute of Science. It also has more than 20 patents, which could prove useful, should the company ever need to defend itself or take action against infringement of its own IP.

In fact, patent filing is another way to track the growth of our industry, reflecting the vast sums that can be made from employing great technology in many devices. They include GaN power and RF chips, as well as various structures made by MBE, where Riber has played a key role for many decades.

Happy anniversary, Riber.

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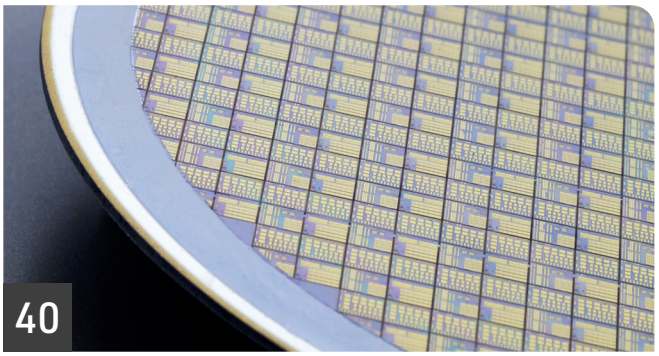

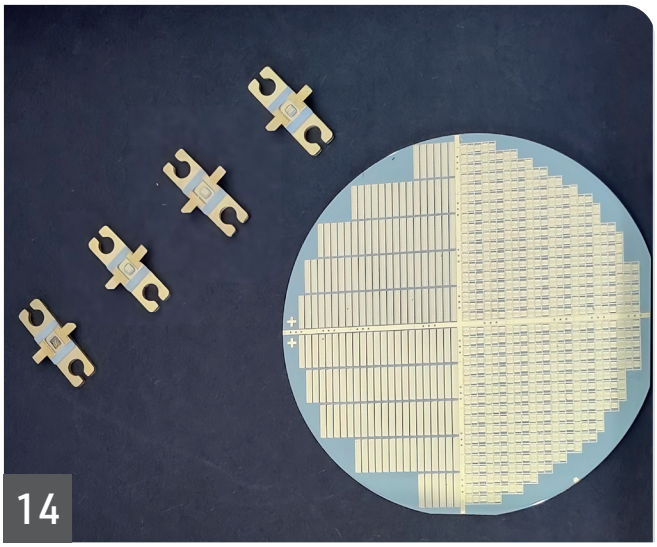

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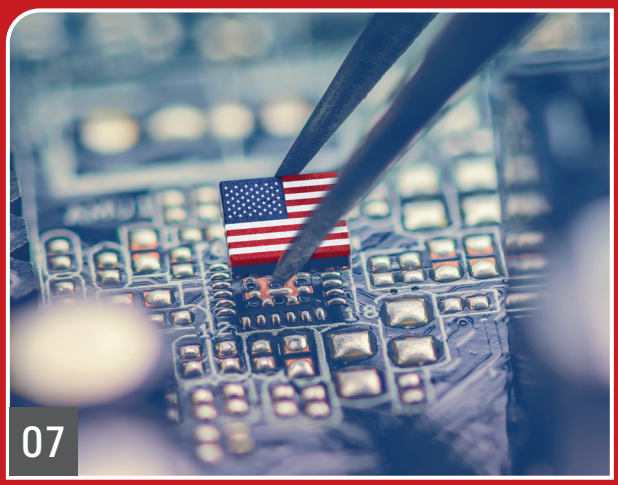

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SICC shows first 300mm SiC wafer

Chinese SiC wafer company exhibits first 300 mm *n*-type SiC substrate at Electronica 2024

AT ELECTRONICA 2024, Chinese SiC wafer company SICC will exhibit what is thought be the first 300 mm *n*-type SiC substrate.

SICC already makes 150 mm and 200 mm *n*-type conductive SiC, and high-purity semi-insulating substrates.

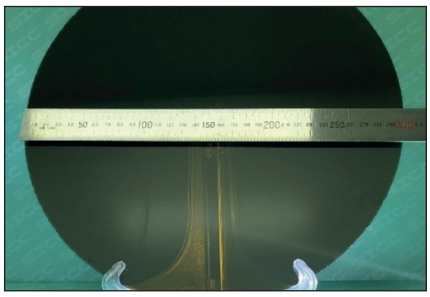
The company has also developed large-size *p*-type SiC substrates.

But the 300 mm *n*-type substrate, it says, is an industry breakthrough that highlights SICC's ability to push the boundaries of semiconductor technology.

For example, in its 200 mm conductive 4H-SiC single crystal substrates, SICC says it has achieved near-zero threading screw dislocation and extremely low basal plane dislocation densities, which significantly enhances yields.

For its high-purity semi-insulating SiC substrates, SICC claims zero micro pipe density. (Micro pipes are SiC crystal defects that can cause electronic devices to short circuit and fail).

The company puts its success down to the ability to precisely control the



crystal growth process, ensuring consistent wafer quality .

The company, which has headquarters in Jinan, is currently further expanding its 200 mm SiC wafer manufacturing capacity at its Shanghai plant.

All change at Wolfspeed as CEO steps down

WOLFSPEED has announced that Gregg Lowe, who has led the company's transition to a pure-play SiC company, will depart this month from his roles as president and CEO and as a member of the board.

In the meantime, Thomas Werner, chairman of the board, has been appointed as executive chairman while the board works to identify Wolfspeed's next CEO.

"On behalf of the full board, I would like to thank Gregg for his service and dedication to Wolfspeed," Werner said. "Since joining the company as CEO in 2017, Gregg has spearheaded our transition into a leading, pure-play SiC company well-positioned to capture the long-term opportunities ahead."

"The board has always been focused on driving long-term value, and at this inflection point in Wolfspeed's journey, the board agreed that this is the right time for a leadership transition."

Werner added: "As we look ahead, we are firmly committed to our key strategic initiatives, which includes executing against the milestones outlined in our recent CHIPS PMT agreement, completing our restructuring initiatives to lower our break-even point and accelerate our path towards profitability, and delivering sales growth on a consistent basis. Wolfspeed is materially undervalued relative to its strategic value and I will focus on driving the company's priorities and working with the finance committee of the board to explore options to unlock value."

Lowe said, "I am honoured to have had the opportunity to lead Wolfspeed and work alongside such talented and dedicated colleagues. Over the past seven years, we have transformed Wolfspeed into the only pure-play and vertically integrated SiC operator in the country to capitalise on the structural and long-term demand for next-generation semiconductor technology."

"While there is work still to be done, I have every confidence that Wolfspeed will execute on its strategic priorities and extend its SiC leadership in the years to come."

Werner will oversee the continued execution of Wolfspeed's strategy in close alignment with Wolfspeed's senior leadership team, the board and the board's operations and finance committees. Following Werner's appointment as executive chairman, board member Stacy Smith was appointed as lead independent director.

Werner has been a member of the board since March 2006, and chairman since October 2023. He has served as the executive chairman of SunPower Corporation, a publicly traded solar cells and solar panel company, since February 2024, and as principal executive officer of SunPower from February 2024 until August 2024.

Werner was Sunpower's chairman from June 2010 to November 2021 and its CEO from June 2003 to April 2021. Prior to SunPower, he was CEO of Silicon Light Machines Corporation, an optical solutions subsidiary of Cypress Semiconductor, from July 2001 to June 2003.

Earlier, Werner was VP and general manager of the Business Connectivity Group of 3Com Corporation, a network solutions company.

Samsung to exit LED business

Korean giant to focus on areas with better growth prospects, including power semis and Micro LED technology, says TrendForce

ACCORDING TO market research firm TrendForce, Samsung Electronics has begun restructuring its business, with the semiconductor division deciding to withdraw from the mainstream LED business, due to the group's performance falling short of expectations.

The division will instead focus on core areas with better growth prospects, including power semiconductors and microLED technology

Samsung Electronics' preliminary unaudited financial results released on 8 October for the third quarter of 2024, showed that the company's profit and revenue for the quarter fell below market expectations. Sales were 79 trillion KRW (around $57 billion), a 17.2 percent year-on-year increase but lower than the market estimate of 81.57 trillion KRW ($59 billion). Operating profit was 9.1 trillion KRW ($6.6 billon), a 274.5 percent year-on-year increase but down 12.8 percent from the previous quarter, and also below analysts' estimate of 11.5 trillion KRW ($8.3 billion).

At the beginning of 2023, Samsung established a special task force for power semiconductors, and by the end of the year, it further reorganised its operations, transforming the LED division into the Power Semiconductor Division.

In July 2023, Samsung announced that it would launch 8-inch GaN power

semiconductor foundry services by 2025, targeting applications in consumer electronics, data centres, and automotive markets. As part of this plan, Samsung introduced German company Aixtron's MOCVD system into its Giheung 8-inch wafer foundry, during the second quarter of this year.

Macom gets CHIPS Act funding for GaN-on-SiC project

US SEMICONDUCTOR company Macom Technology has been selected to lead a development project to establish advanced GaN-on-SiC process technologies for RF and microwave applications.

Funded by the CHIPS and Science Act through the United States Department of Defense (DoD), the project will focus on developing semiconductor manufacturing processes for GaN-based materials and MMICs operating efficiently at high voltages and at millimetre-wave frequencies.

Macom is a member of the Commercial Leap-Ahead for Wide Bandgap Semiconductors Microelectronics Commons Hub and will work with North Carolina State University, Adroit Materials and the Naval Research Laboratory on this project.

The year 1 value of this award is $3.4 million. This award expands

upon a series of GaN technology development activities with the DoD, including a 2021 Cooperative Research and Development Agreement with the United State Air Force Research Laboratory, where Macom successfully transferred AFRL's 0.14 μm GaN-on-SiC MMIC process to its Massachusetts-based US Trusted Foundry.

This was followed in 2023 by a $4 million AFRL contract to develop GaN technologies for millimetre-wave applications and a Defense Advanced Research Projects Agency award valued at up to $10.1 million aimed at improved heat dissipation for high power applications.

Earlier this year, Macom was awarded a separate CHIPS-funded GaN technology development contract worth up to $11.4 million.

"Our strategy is to increase domestic production of state-of-the-art RF and microwave power technologies to support our military's radar and sensing applications and to enable next generation telecommunications networks," said Stephen Daly, Macom president and CEO.

"We believe the technologies and products developed under these contracts will help keep the United States and Macom on the leading edge."

GaN and SiC 'first' for data centre PSU

Navitas announces 98 percent efficient 8.5 kW AI data centre PSU

NAVITAS SEMICONDUCTOR has announced what it claims is the world's first 8.5 kW power supply unit (PSU), powered by GaN and SiC technologies to achieve 98 percent efficiency, for next-generation AI and hyperscale data centres.

The AI-optimised 54 V output PSU complies with Open Compute Project and Open Rack v3 specifications and uses high-power GaNSafe and Gen-3 Fast SiC MOSFETs configured in 3-phase interleaved PFC and LLC topologies.

The company says that the PSU's shift to a 3-phase topology for both the PFC and LLC (compared with 2-phase topologies used by competing PSUs) enables the industry's lowest ripple current and EMI. Furthermore, the PSU reduces the number of GaN and SiC devices by 25 percent compared with the nearest competing system, which reduces the overall cost.

The PSU has an input voltage range of 180 to 264 V_{AC}, a standby output voltage of 12 V, and an operating temperature range of -5°C to 45°C. Its hold-up time at 8.5 kW is 10 ms, with 20 ms possible through an extender.

The 3-Phase LLC topology is enabled by high-power GaNSafe, which integrates control, drive, sensing, and critical protection features. GaNSafe has short-circuit protection (350 ns maximum latency), 2 kV ESD protection on all pins, elimination of negative gate drive, and programmable slew rate control. All these features are controlled with 4-pins, allowing the package to be treated like a discrete GaN FET, requiring no VCC pin.

The 3-Phase interleaved CCM TP-PFC is powered by Gen-3 Fast SiC MOSFETs with 'trench-assisted planar' technology.

"This complete wide bandgap solution of GaN and SiC enables the continuation of Navitas' AI power roadmap, which enables this 8.5 kW and plans to drive to 12 kW and higher in the near-term", said Gene Sheridan, CEO and co-founder of Navitas. "As many as 95 percent of the world's data centres cannot support the power demands of servers running NVIDIA's latest Blackwell GPUs, highlighting a readiness gap in the ecosystem. This PSU design directly addresses these challenges for AI and hyperscale data centres."

Navitas displated the PSU for the first time at Electronica 2024 (November 12th– 15th).

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GlobalFoundries confirms $1.5B CHIPS Act funding

Funding supports GF's Vermont GaN facility modernisation and New York expansion plans

GLOBALFOUNDRIES and the US Department of Commerce have announced an award of up to $1.5 billion in direct funding to GF through the CHIPS and Science Act.

The award follows the previously signed preliminary memorandum of terms announced in February 2024 and will enable GF to expand its chip manufacturing and technology development in the US, across a range of end-markets including automotive, smart mobile devices, IoT, data centres, and aerospace and defence.

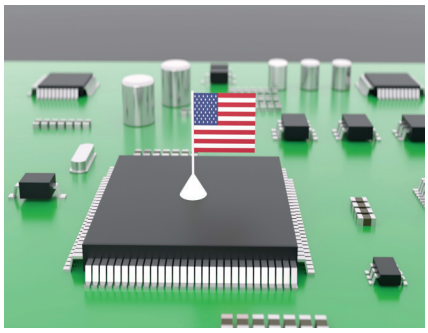
One of the key project's GF's CHIPS award will support is modernisation of GF's existing fab in Essex Junction, Vermont, to expand production capacity and create one of the world's leading facilities capable of high-volume manufacturing of next-generation GaN semiconductors for use in electric vehicles, data centres, IoT, smartphones and other critical applications.

Money will also go towards expansion of GF's existing Malta, New York, fab by adding technologies already in production at GF's Singapore and Germany facilities, to enable a secure and reliable supply of domestically manufactured essential chips for the US auto industry.

Funding may also go towards the construction of a new state-of-art fab on GF's Malta, New York, campus to meet expected demand for US-made essential chips across a broad range of markets and applications including automotive, AI in the data centre and at the edge, as well as aerospace and defence.

"The idea of strengthening US semiconductor manufacturing has been five-plus years in the making. With bipartisan support, that idea evolved into the CHIPS and Science Act," said Thomas Caulfield, president and CEO of GF. "GF's essential chips are at the core of US economic, supply chain and national security. We greatly appreciate the support and funding from both the US Government and the states of New York and Vermont, which we will use to ensure our customers have the American-made chips they need to succeed and win."

In aggregate, these projects represent more than $13 billion of investment



over the next 10-plus years across GF's two US sites. This investment includes the $1.5 billion CHIPS and Science Act award, more than $550 million in support from the New York State Green CHIPS Program, as well as funding and support from Vermont, GF ecosystem partners and key strategic customers, and other incentives.

Combined, these investments are expected to create close to 1,000 direct manufacturing jobs and more than 9,000 construction jobs over the life of these projects.

GF's fabs in New York and Vermont are both Trusted Foundry accredited and manufacture secure chips in partnership with the US government.

X-FAB and SMART Photonics partner on micro-printing

Companies to use X-Celeprint's micro-transfer printing to build next-generation transceivers with silicon photonics and InP integration

SPECIALIST FOUNDRY X-FAB and InP photonics foundry SMART Photonics have announced a collaboration to integrate X-FAB's silicon photonics platform with SMART Photonics' InP chiplets.

They aim to use use micro-transfer printing (MTP), licensed from X-Celeprint, for heterogeneous integration, enabling new capabilities for datacom and telecom applications.

InP technology supports modulator bandwidths exceeding 120 GHz, making it a good solution for next-generation multi-terabit telecom and datacom standards – pushing transceiver speeds far into the terabit realm. In contrast, silicon photonics technologies hit a performance ceiling at around 70 GHz.

The collaboration aims to deliver scalable, high-volume solutions that combine the best of both technologies.

By co-optimising silicon photonics, InP, and MTP technologies to fulfill customer requirements, the collaboration will enable new

functionalities and improved system performance while reducing integration costs through relaxed photonics packaging requirements.

The MTP technology enables a broad degree of freedom for the system and product designers, by providing flexible integration of various material system chiplets into the product design.

Johan Feenstra, CEO of SMART Photonics, explains: "As the demand for integrated photonics rapidly increases, thanks to the growth of AI and data transfer, our joint solutions will enable much faster data rates while reducing overall power consumption, and therefore the environmental footprint."

Rudi De Winter, CEO of X-FAB, adds: "Through heterogeneous integration, we are combining the best of the InP and silicon photonics worlds."

"This will allow our customers to develop innovative solutions addressing the societal challenges of our times such as decarbonization. It is also a great opportunity to build a strong European value chain."

This collaboration builds upon the PhotonixFAB EU funding project, which aims to provide a path to scalable high-volume manufacturing for SOI and SiN silicon photonics, MTP-ready InP chiplets and micro-transfer printing of chiplets.

X-FAB and SMART Photonics recently signed a Memorandum of Understanding to formalise their collaboration.

The aim is to support lead customers with industrial prototyping by 2026, with risk production readiness by 2027.

Early customer engagements can be supported within the ongoing PhotonixFAB project framework.

India's DRDO announces GaN and SiC milestones

INDIA'S Defence Research and Development Organisation (DRDO) has announced a significant milestone in semiconductor technology by developing indigenous methods for producing 4-inch SiC wafers and fabricating GaN HEMTs up to 150 W.

A statement from the Indian Ministry of Defence said that these advancements, achieved by the DRDO's Solid State Physics Laboratory (SSPL), also include MMICs with power capabilities up to 40 W, suitable for applications extending to X-band frequencies.

The establishment of indigenous GaN-on-SiC-based MMIC production has been successfully implemented at GAETEC (Gallium Arsenide Enabling Technology Centre) in Hyderabad.

These technologies are considered essential for modern combat systems, radar technologies, electronic warfare,

aerospace, satellite communications, and green energy initiatives.

IQE announces departure of CEO

Americo Lemos leaves the company, with Jutta Meier taking up the position of interim CEO

IQE PLC, a supplier of compound semiconductor wafer products, has announced that Americo Lemos, CEO, has left the company.

Mark Cubitt, who recently joined the IQE board as chair-elect, will become the executive chair of IQE. He is currently non-executive chair at AIM-Listed Beeks Group and Concurrent Technologies.

Jutta Meier will take up the position of IQE's interim CEO in addition to her CFO role. Meier joined IQE in January 2024 from Intel Corporation.

Phil Smith, who has been chair of IQE since 2019, will step down from his role but remain on the IQE board as a non-executive diirector.

IQE says it will begin the search for a permanent CEO immediately.

Phil Smith, chairman of IQE, said: "Whilst IQE continues to navigate the semiconductor market recovery, we are confident that the company's renowned technical expertise is well aligned to long-term growth market vectors."

He continued: "In Mark and Jutta we have two excellent individuals with the necessary sector and leadership skills to capture that growth in partnership with our customers, employees and broader stakeholders. Their immediate priorities will include a focus on executing on the near-term pipeline as well as cash generation across the group and on unlocking embedded value by pursuing the IPO of our Taiwan business. They will examine other efforts to optimise our asset base and ensure that resources are centred around IQE's strategic areas of expertise."

Following the departure of Lemos, IQE revealed that revenue for the full year 2024 is expected to be broadly flat year-on-year, resulting in around £115 million. In line with the rest of the industry, the company says it is continuing to see a slower than anticipated recovery in key sectors driven by weak consumer demand in end markets. The group expects this to result in an adjusted EBITDA of at least £5 million.

In light of the results, IQE has announced a strategic review.

Smartkem and AUO collaborate on rollable microLED displays

Collaboration marks first microLED display product in development using Smartkem's technology

SMARTKEM, a UK developer of organic thin-film transistors (OTFTs), has partnered with AUO, the largest display manufacturer in Taiwan, to jointly develop the world's first advanced rollable, transparent microLED display.

Smartkem's chairman and CEO Ian Jenk says its technology has the potential to take today's microLED TVs from high-end market prices of $100,000 down to mass market prices.

"Because our transistors are processed at such a low temperature compared to other technologies, we are able to pour them directly on top of the microLEDs, completely eliminating the problematic mass transfer and laser welding processes required with other technologies," explained Jenks.

He adds: "The key feature that enables the development of this microLED display is our unique low-temperature process that allows the use of low-cost, flexible plastic rather than glass. We believe that, if successful, this collaboration will be a significant milestone for Smartkem in its road to commercialisation, and for microLED display product development using our technology."

Wei-Lung Liau, CTO of AUO, commented, "AUO has dedicated years to developing the ultimate microLED display technology, forging alliances with ecosystem partners to enable mass production. In this collaboration, AUO has developed groundbreaking technologies that boost the high transparency and free-form in applications of microLED. With proprietary materials from Smartkem and the OTFT production process from ITRI, we are collaboratively developing the world's first rollable microLED display for potential commercialisation with cost advantage. We believe this will create new opportunities for the display industry and continue to expand value chain partner cooperation and influence."

Display analyst and DSCC (Display Supply Chain Consultants) CEO, Ross Young, commented, "This is an exciting project that, if successful, will demonstrate the cost effectiveness of Smartkem's technology in the most demanding of microLED applications, and could generate substantial market interest."

The project between Smartkem and AUO will commence on January 1, 2025. The collaboration has been awarded a grant from the 2024 Taiwan-UK Research & Development Collaboration, supported by The Taiwanese Ministry of Economic Affairs and Innovate UK, part of UK Research and Innovation.

The 2024 UK-Taiwan Collaborative R&D Initiative has invested more than £10 million this year to promote bilateral industrial technology research and development cooperation.

The nine award-winning projects will promote the joint development of advanced technologies in fields such as electrical information communication, biomedicine, and electromechanical by Taiwan-UK enterprises.

> "The key feature that enables the development of this microLED display is our unique low temperature process that allows the use of low-cost, flexible plastic rather than glass. We believe that, if successful, this collaboration will be a significant milestone for Smartkem in its road to commercialisation, and for microLED display product development using our technology"

‘All-GO-HEMT’ to develop β-gallium oxide heterostructures

€2 million German-funded project aims to increase in efficiency in power electronics

A €2 MILLION German-funded project called All-GO-HEMT aims to increase efficiency in power electronics and make a significant contribution to sustainable energy generation.

Led by Andreas Fiedler of the Leibniz-Institut für Kristallzüchtung (IKZ), the project aims to develop modulation-doped β-$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 heterostructures that exhibit high electron mobility.

Compared to established materials such as silicon, GaN and SiC, Ga_2O_3 offers potential for increasing efficiency that has not yet been fully exploited.

“We believe that the development of more efficient materials can make a significant contribution to the energy transition and enable the industry to successfully master the challenges of the future,” explains Fiedler.

Even though power electronics based on Ga_2O_3 promise to be more efficient, the material is inferior to established materials in terms of charge carrier mobility. “Gallium oxide behaves to the established materials in the same way as ten metres of dirt road to one kilometre of freeway. Due to the shorter distance, your car consumes less, and despite the lower speed, you reach your destination faster - all thanks to a more compact design,” explains Fiedler.

The central aim of the project is to overcome the material limitation of Ga_2O_3 in terms of charge carrier mobility with the help of the innovative design of an aluminium-alloyed heterostructure and thus eliminate this disadvantage.

Fiedler emphasises: “We are convinced that the efficiency of power electronics can be significantly increased through a combination of a more compact design and higher charge carrier mobility in our newly developed materials.”

Another goal of All-GO-HEMT is to create a reliable material basis of Ga_2O_3 and the newly developed alloy with aluminum of the highest crystalline quality for research and industry. This basis is necessary because the development of high-performance devices with compact design and optimised manufacturing processes is currently limited by the insufficient availability of high-quality material.

Compared to established materials such as silicon, GaN and SiC, Ga_2O_3 offers potential for increasing efficiency that has not yet been fully exploited

The project partner Ferdinand-Braun Institut (FBH) will use this material basis to develop new prototypes for power electronic devices. These prototypes will then be tested by ZF Friedrichshafen AG, the industrial mentor, for their suitability for industrial application. In addition, the entire value chain, from crystal growth to the finished device, will be analysed by the industrial mentors Aixtron SE and Siltronic AG in order to quantify and evaluate the economic and ecological benefits of this technology at an early stage.

Putting India on the global GaN stage

University spin-out Agnit has just secured funding to grow its GaN portfolio, a combination of epiwafers and power and RF devices

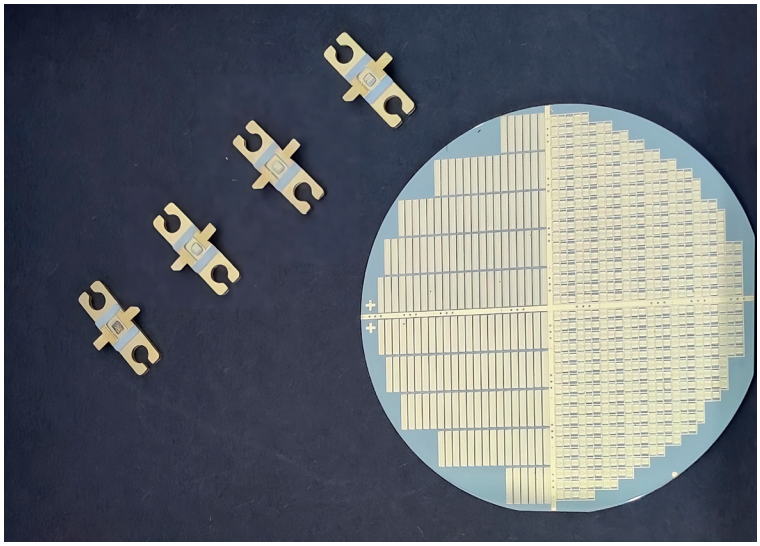
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THERE ARE a number of ways to measure the growth of an industry.

For GaN electronics, which serves both the power and RF sectors, evidence of its rapid rise is seen in its double-digit rises in revenue, which will swell this market to several billion dollars by the end of this decade. But that's not the only way to track success. The growth of GaN is also seen in the geographical expansion of its chipmakers. As well as big the names in the US, Europe, Japan and China – such as Navitas, EPC, Transphorm, Infineon, Toshiba and Innoscience – smaller players are cropping up all over the world, including in unfamiliar locations, such as India.

Breaking new ground on this sub-continent is Agnit, a spin-out of the Indian Institute of Science that has just raised another US $3.5 million to advance its GaN portfolio, a mix of epiwafers and power and RF devices.

Company co-founder and CEO, Hareesh Chandrasekar cannot lay claim to Agnit being the sole trailblazer for compound semiconductor manufacturing in India, because it's just possible that there is another maker of such devices hiding from view. But he is adamant that Agnit is the first to use indigenous technology, rather than getting it from somewhere else.



Introducing semiconductor manufacturing in India could be crucial to the growth of this nation's economy, says Chandrasekar. "If India is going to be a 5, 7, $10 trillion economy in the next decade or so, there's no way this is happening without us having a presence in the electronics manufacturing ecosystem."

While there are a number of options for gaining a foothold in the semiconductor industry, some are more attractive than others, with cutting-edge CMOS having a formidable financial barrier to entry.

"We felt that gallium nitride was a nice sweet spot," says Chandrasekar, who argues that while this technology is not as complex as state-of-the-art CMOS, and doesn't demand fabs with price tags of several billion dollars, it's up and coming, and there is a local pull for products.

An academic heritage

Founded in late 2019, but initially impeded by the global pandemic that stalled the start of this company's operations until January 2021, Agnit receives tremendous support from the Indian Institute of Science, in terms of both facilities and expertise.

This institute is a great incubator for Agnit, having constructed a pilot production line for GaN that has a peak capacity of about ten 6-inch wafers per day. Supporting this is a very good characterisation suite.

Another asset of this institute is its extensive development of GaN technology, creating a strong IP base that draws on many, many years of research.

Imparting expertise from the Institute to Agnit is seamless, as four of the seven founders, all still involved, are academics with complementary capabilities related to the fabrication, operation and reliability of GaN devices. The other three co-founders, now the core management team, have PhDs in the field of GaN, but bring a different skillset, partly thanks to time spent working in the semiconductor industry. Strengthening this team are a growing number of employees, now totalling 16.

In terms of the commercialisation of its GaN device portfolio, Agnit has initially focused on the RF, before more recently expanding into the power domain.

Agnit's RF devices are marketed to the telecom and the strategic sector. Products from rival suppliers are already being deployed in base stations, encouraging the Bangalore start-up to pursue more niche applications associated with 5G networks. "It could be things like private networks," says Chandrasekar.

For the power market, which Chandrasekar describes as "pretty hot now", there are many players with unique business models. To carve out a space in this sector, he and his colleagues are trying to address a particular set of problems associated with the unique, local market. Prototyping is underway.

To support its device development, Agnit is packaging its die in-house. But this will change when it moves into production, with this final manufacturing step outsourced, using the strong local ecosystem.

"We are also exploring global partnerships to see how we can actually leverage the global packaging capacity for the GaN chips that we make," says Chandrasekar.

The third string to Agnit's bow is its supply of GaN epiwafers to chipmakers.

"We had already supplied to academia," says Chandrasekar, adding that the new additional capacity is enabling Agnit to expand its horizons and build foundry relationships for the global supply of GaN-based power and RF epiwafers.

One of the issues hampering the GaN industry for many years is that epi is a "black box," according to Chandrasekar. "When you buy a batch of wafers, you never know if they're the right ones to begin with for your process or not. That has always been a big stumbling block."

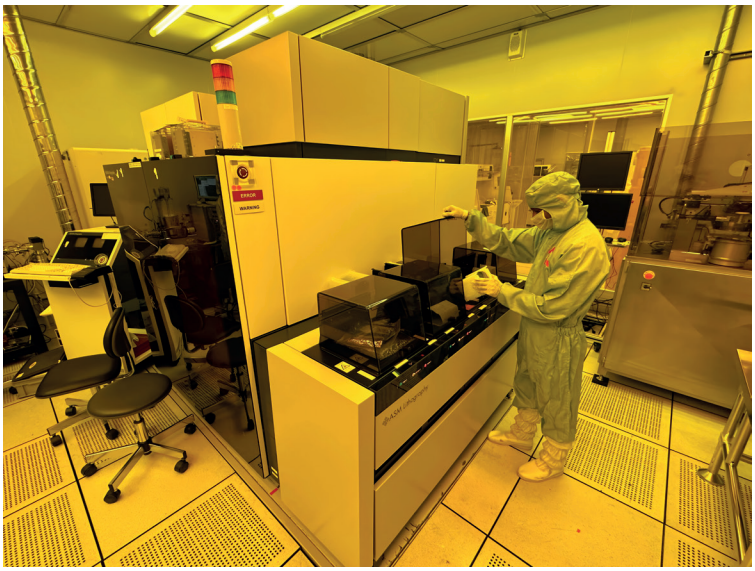
Agnit is addressing this concern by offering the capability to adjust the epitaxial process based on internal device feedback. This helps customers target particular performance specifications.

Patents and IP

Agnit has a strong IP portfolio, supported by technology developed from the Indian Institute of Science, which it licences exclusively. The start-up has more than 20 patents, of which 15 or so are global patents.

Like the leaders of many foundries, those calling the shots at Agnit have thought very carefully about what IP requires patenting, and what is best left undisclosed. Such decisions are guided by whether patents have the potential to expose and demonstrate infringement. "If you can't do that, then it makes very little sense to patent your IP," argues Chandrasekar.

Highlighting the need for defendable IP are the patent battles being fought between Innoscience and EPC and Infineon. While such skirmishes may alarm some chipmakers within the GaN industry, they are not a major concern to those leading Agnit. "Everything that we commercialise has our own patents as a backing, or our trade secrets and know-how as a backing," says Chandrasekar. "We are quite careful about that."



➤ Agnit produces GaN power and RF devices at the incubator at the Indian Institute of Science.

Investing in its future

The US$3.5 million raised this Autumn came from a seed round led by 3one4 Capital and Zephyr Peacock.

This investment will help to increase production yields for 4-inch GaN-on-SiC epiwafers for RF devices, and for 6-inch GaN-on-silicon wafers for the power sector.

In addition, the funding will be used improve device reliability, an issue that Agnit takes very seriously. "This will help our devices be qualified for various reliability standards that we are targeting based on the markets that we choose to go after," remarks Chandrasekar.

As well as advancing yield and reliability, the seed funding will support prototype development – in particular, power devices for the domestic market, as well as RF devices for the telecom sector.

Two big goals for the next 12 months are to get RF products in the market, in both the telecom and strategic sectors, and to grow the epiwafer supply business, supporting these customers with device data.

"In 24 months, we'll also have the first alpha samples available on the power devices that we're working on, which will be sampled to customers for integration into their systems," adds Chandrasekar.

The CEO expects the majority of its sales over the next few years to come from domestic markets, but 30 percent will be overseas. If such success follows, that will surely help to grow the role of India on the global GaN stage.

MicroLEDs: Eliminating etching

Pyramidal microLEDs on patterned SiC deliver a great performance, even when their dimensions approach the nanoscale

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

IDEALLY, when producing compound semiconductor devices, every process adds functionality without introducing compromise. For example, the addition of an anti-reflection coating should increase the efficiency of a multi-junction solar cell without limiting its lifetime; and when mirrors are added to a laser, they should boost reflectivity without introducing light-quenching defects.

On the whole, processing epiwafers into devices follows this formula, with a succession of positive steps creating a high-performance chip. But there is an exception: the microLED. When crafting such a smaller emitter, its dimensions are typically defined by etching, a step that creates imperfections, including dangling bonds that drag down efficiency. It's possible to restore this device's performance through passivation, using techniques such as plasma-enhanced CVD and atomic layer deposition. But wouldn't it be better to never damage these miniature marvels, rather than having to repair them?

Pursuing this attractive approach with vigour is the Swedish start-up Polar Light Technologies. This spin out of Per Olof Holtz's group at Linköping University has been gathering pace this year as it looks to increase the spectral coverage of its devices, engage with other companies, and win further funding to support its shift from development to production.

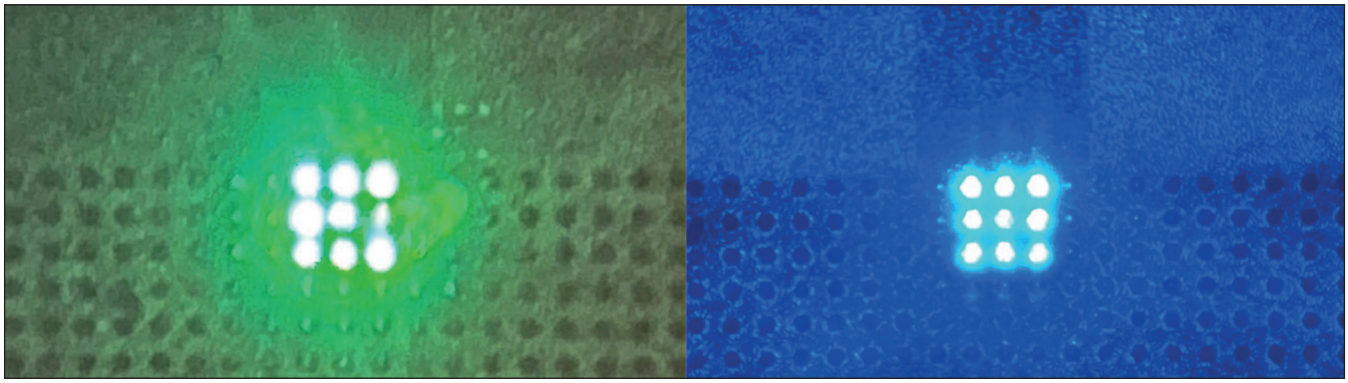
The core technology of Polar Light Technologies is its pyramidal LEDs, formed by growth of GaN-based structures on patterned SiC substrates by MOCVD.

According to the company's Chief Product Officer and co-founder, Ivan Martinovic, the initial target market for these novel emitters is the light source for augmented-reality headsets. Martinovic views his company's technology as a competitive candidate for making monochrome panels in products made by the likes of Jade Bird Display, with full-colour images formed with an optical system that combines the output of red, green and blue sources.

Looking further ahead, Martinovic expects microLEDs, including those he is helping to pioneer, to penetrate the automotive industry, due to their high level of robustness. MicroLEDs may also take market share from OLEDs in the smartwatch sector, where they promise to enable a battery life of several days.

For the first of these target markets, augmented-reality headsets, displays should have a pixel size approaching two microns, says Martinovic. "The subpixel should be even smaller, and with the spacing, it's a sub-micron game at that point."

As well as increasing the fidelity for the user of the headset, microLEDs that are small enough to meet this requirement deliver cost benefits.



➤ Polar Light Technologies has produced blue and green pyramidal microLEDs, and is working on red-emitting varaints.

"Whether it's for micro-displays, where you monolithically integrate onto silicon, or mass transfer for large-area displays, you want to have really, really small LEDs," argues Martinovic. "You can't have five- or ten-micron microLEDs, even for big panel displays. You will use too much epi for your display."

Note that it's not possible to produce conventional microLEDs as small as this that deliver high performance. "You're in the area where damage caused by the etching is getting so out-of-hand that it's almost not controllable anymore," says Martinovic.

While the pyramidal microLEDs excel at such small dimensions, they do incur a substrate cost penalty compared with more conventional LEDs, due to the use of SiC. However, this expense is overshadowed by etching-related issues, argues Martinovic, who points out that the size of SiC substrates is increasing while their price is staying the same. "So, in that case, you can say that the price is coming down."

The pyramidal shape of Polar Light Technologies' microLEDs delivers a number of benefits, including an increase in the light extraction efficiency and an emission profile that leads to better utilisation of light.

So far, demonstrations of the company's technology have focused on devices emitting in the blue and green, but evidence of capability in the red is in the pipeline.

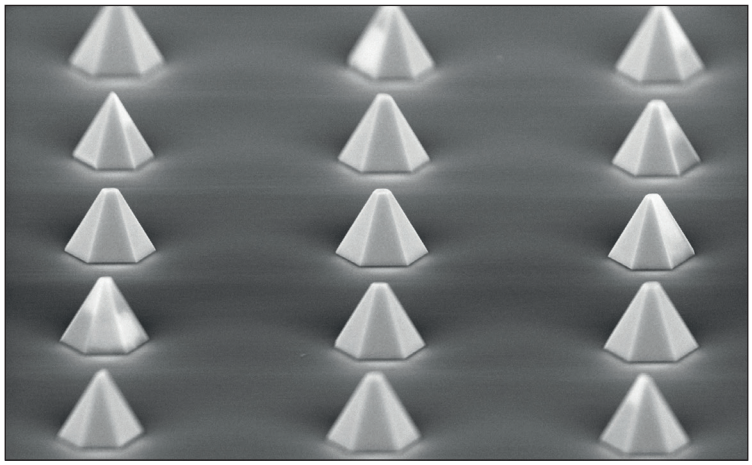
Propelling the emission of GaN-based LEDs to the red is not easy. Success requires increasing the indium content in the quantum wells, but that leads to significant strain that spawns non-radiative defects. Switching to wider wells can alleviate this strain, but at the expense of a fall in the recombination efficiency, due to a reduction in the overlap of electrons and holes, which are pulled towards opposite edges of the wells by internal electric fields.

These problems diminish with pyramidal LEDs. Due to their geometry, they are semi-polar and thus enjoy a reduction in the strength of the internal electric fields that hamper radiative recombination.

Polar Light Technologies has been honing its pyramidal microLEDs over many years. The company formed in 2014, with much initial effort devoted to research and filing patents.

Funding for the start-up, which comes from a number of local venture capital firms, only began in 2021.

"We've gathered a really nice network of Swedish and Nordic VCs. We've chosen to focus on them. We want to keep it here," says Martinovic, who is now working on a "medium-sized" round that is slated to close at the end of this year.



➤The triangular shape aids light extraction and is behind the semi-polar active region that helps increase radiative recombination.

"At the end of next year, we're gearing up to bring in a more serious level of funding - let's say the A round for Polar Light."

So far, the company has carried out all the process steps in house, including the fabrication of the silicon chips that are used to drive the microLEDs.

"We're using a cold bonding approach to hybridise, to put together gallium nitride LEDs with silicon CMOS," says Martinovic. He explains that a bonding approach involving heating is not permitted, because slight differences in thermal expansion coefficients would lead to a misalignment that exceeds the pitch of the display.

This in-house *modus operandi* is unlikely to continue, as Martinovic and his colleagues are looking to start working with partners. "We're much more active right now and much more open to collaborations than we've ever been. That's part of that direction of going towards product. We're not going to do this ourselves."

It's a good move, as more collaboration will be key to driving the success of microLEDs in a number of displays, where bright, miniature emitters that are free from etching look to shine.

"Whether it's for micro-displays, where you monolithically integrate onto silicon, or mass transfer for large-area displays, you want to have really, really small LEDs. You can't have five- or ten-micron microLEDs, even for big panel displays. You will use too much epi for your display"

ALD: Speeding the pathway from development to production

Oxford Instruments' suite of ALD tools ensures a reliable process transfer from development to production

BY GRANT BALDWIN AND AILEEN O'MAHONY FROM OXFORD INSTRUMENTS PLASMA TECHNOLOGY

IN ANY MANUFACTURING ENVIRONMENT, engineers face a critical challenge when moving a process on from prototype or development to volume production. Reproducing results obtained in a compound semiconductor device development lab at scale is not straightforward, due to the fundamental design of development systems tending to differ from that of production systems.

During the device development process, developers want as many options and capabilities as possible, as this widens their process window, while allowing them the opportunity to pull many levers when trying to nudge the process toward a desired result. But having the opportunity to play with superfluous parameters and process knobs is a double-edged sword, threatening to introduce risk in production environments, where more options mean more components to monitor, control and maintain. What's really needed is to find a way that allows process engineers to benefit from system flexibility in development, without having to compromise production transferability.

At Oxford Instruments Plasma Technology, located on the outskirts of Bristol, UK, we offer a solution to this problem for those using atomic layer deposition (ALD). We have a complementary pair of systems within our ALD product range that combine, in a very innovative way, development flexibility with high-volume

➤ Oxford Instruments Plasma Technology's PlasmaPro ASP and Atomfab suite of atomic layer deposition systems

manufacturing repeatability and throughput. Read on to discover how we fulfil these disparate goals.

Development with PlasmaPro ASP

Our PlasmaPro ASP, launched in the last 18 months, is designed to give process engineers all the flexibility and capability to develop the industry's most advanced high-quality ALD layers for research and development, with incredibly high rates and low damage.

Initially, we launched our PlasmaPro ASP into the quantum market. Here it offers a deposition rate that is 2-3 times higher than comparable ALD systems, and provides a process solution for superconducting nitrides, such as NbN and TiN. For those using rival tools, depositing superconducting thin films can take up to 12-15 hours, slowing down implementation in certain quantum applications.

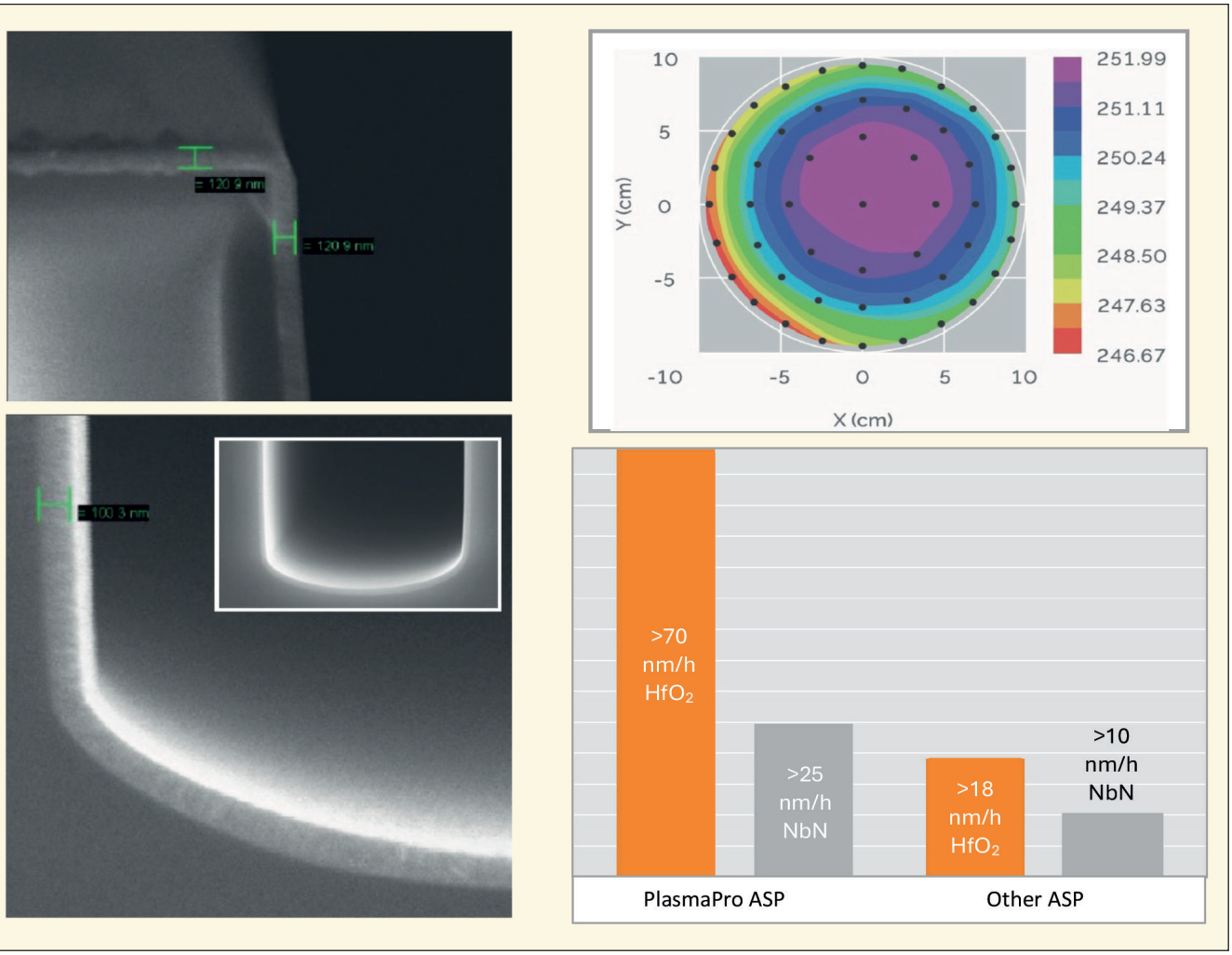
When targeting deposition of these superconductors, we identified an ideal set of processes to launch our PlasmaPro ASP. Our new ALD system offers deposition rates of more than 25 nm hr^{-1} for NbN, and in excess of 35 nm hr^{-1} for TiN. Our PlasmaPro ASP provides the capability to tune film properties, such as stress and crystallinity, enabling engineers to dial in the desired properties of their deposited material.

After launching the PlasmaPro ASP with a suite of the most challenging thin films required for any application, we developed additional ALD films. By adding to this repertoire, we are able to give our customers a truly unique platform for ALD development.

Production with the Atomfab

Although high deposition rates provided by the PlasmaPro ASP enable a crucial breakthrough for quantum applications, such rates are not usually a critical requirement for ALD process development systems. So why did we design the PlasmaPro to deliver such high rates?

The answer is found in the innovative way that our development and production ALD systems – Atomfab – work together. This duo share the same genetics, including the same patented plasma source design and user interface, referred to as PTIQ. Thanks to this holistic product range concept, our PlasmaPro ASP benefits from a high deposition rate with process flexibility, as well as ease of process transferability from development to our Atomfab production-proven ALD system. By design, this transfer is incredibly straightforward and negates the need for process requalification at the production level.



➤ 130 nm conformal superconducting NbN deposited in 8:1 aspect ratio trench using PlasmaPro ASP. Trench etched using PlasmaPro 100 Estrelas in cryogenic mode.

Quantum
High deposition rate, conformal superconducting nitrides enabling accelerated quantum adoption

Development
>10 ALD processes currently available

Accelerated Pathway

Plasma Source Design

Clusterable

Serviceability

Wafer Stage Options

Bias & High Temperature

Roadmap for Future Production Qualification

Precursor Pot Option

X 6

X 4

Uptime Specs & Service Options

Research Spec

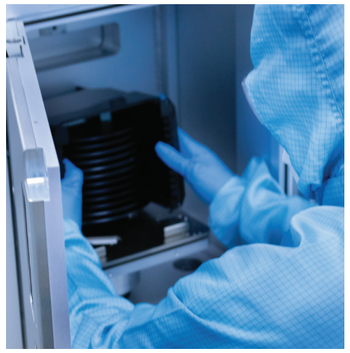
Production Spec

Process Options

Flexible

Dedicated

Production
>7,000 wafers per month at 200 mm



AR / VR
Low temperature processing with excellent conformality for mechanical protection

Silicon Carbide
Enabling enhanced SiC MOSFET performance with high quality oxides and trench conformality

Gallium Nitride
Production-qualified GaN HEMT passivation with low CoO, validated at global install base

Optoelectronics
High quality moisture barrier for lasers. Passivation of VCSEL & LED devices.

We have demonstrated that processes developed on PlasmaPro ASP are easy to transfer and replicate on the Atomfab. This feature is tremendously beneficial to engineers who begin by developing a process to deposit an ALD film, before having to quickly ramp up production.

Since 2020 our Atomfab has been production-qualified throughout the world for ALD passivation of GaN HEMTs. When optimised to run a single plasma ALD process on up to 200 mm wafers, this tool provides a monthly throughput of more than 7,000 wafers for oxide passivation, and over 9,000 wafers for a nitride interface layer on GaN HEMTs for each ALD chamber on a cassette handler.

While throughput is crucially important for device fabrication, quality is also vital. Due to this, we are as innovative in our process development as we are in our product development. Our efforts in GaN HEMT device fabrication highlight this broad outlook. Here we have established a market-leading position in both ALD and atomic layer etch, as well as demonstrating a range of processes to control and optimise material interfaces to improve device performance.

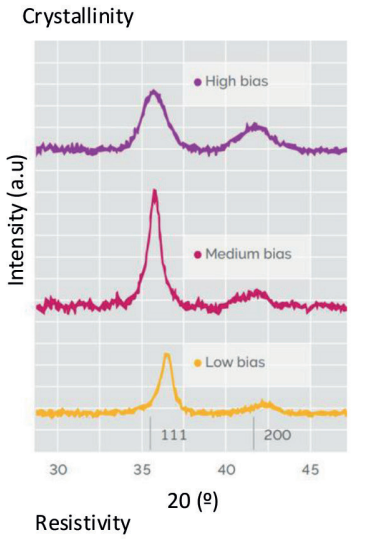
One technique that we have developed, yielding excellent results by optimising the material interface, involves a pre-ALD plasma surface treatment, prior to oxide or nitride interfacial layer deposition. The processes work together to reduce the interface trap density and improve the GaN HEMT performance at a significantly reduced cost of ownership – it is more than four times lower in cost than the incumbent ALD solution. All this is accomplished whilst meeting our customers' expectations in terms of system uptime, mean time to repair, mean time to clean, mean time between cleans, and mean time between assists.

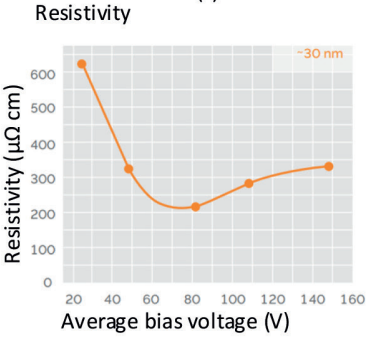
Accelerated development

Having the capability, to carry out ALD at high rates on a development system, opens up a world of new opportunities for applying ALD where previously not possible. As well as speeding up development, thicker ALD layers that were previously not thought possible can be developed, and ALD can be considered for new applications with a wider process application window. Once developed on the PlasmaPro ASP, processes can be seamlessly transferred to the Atomfab and ramped to production to enable ALD in high-volume device manufacturing. It is such an advantage to have a suite of products designed to achieve continuity between development and production phases, and arguably this kind of innovation is unique in its category, and with it being available in our technology portfolio, will now be accessible to all ALD users worldwide.

➤ Process flexibility data for PlasmaPro ASP and production quality data for Atomfab below for ALD

Data showing precise tunability using electrode bias control on PlasmaPro ASP



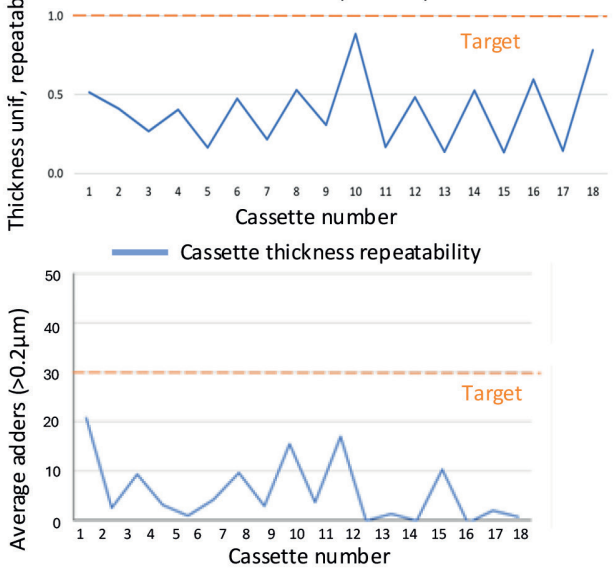


Plasma ALD Material	PlasmaPro ASP released
NbN	✓
TiN	✓
Al_2O_3	✓
SiO_2	✓
Al_2O_3 thermal	✓
TiO_2	✓
AlN	✓
HfO_2	✓
Ga_2O_3	✓*
GaN	✓*

*Data courtesy of TU/e

Atomfab: Cassette to cassette ALD AL_2O_3 thickness repeatability

Total Al_2O_3 deposition 26 µm, 450 wafers, 18 cassettes.
Average thickness uniformity per cassette ±0.9%.
Cassette to cassette thickness repeatability ±0.4%.



Atomfab specification 200 mm	Al_2O_3	AlN	SiN
Within wafer thickness uniformity	<±1.0%	<±2.0%	<±3.0%
Wafer-to-wafer repeatability	<±1.0%	<±1.0%	<±1.0%
Refractive index @ 632.8 nm	>1.63	>1.90	>1.93
Production stage	qualified	validation	validation

➤ Riber's component assembly room in the early 1970s.

Riber celebrates 60 years of success

With a pedigree in vacuum technology stretching back 60 years, Riber has an enviable track record in MBE innovation that shows no signs of abating

BY CLAUDINE PAYEN FROM RIBER

ENGINEERING COMPANIES operating at the cutting edge of technology are renowned for their precision. Such firms are built on calculation, with every alteration accounted for. There's little room, if any, for uncertainty.

So it's almost unthinkable that given all this attention to detail, one such outfit is shrouded in a mystery since its conception. But that's the case for Riber, our company that's a pioneer of MBE, and now celebrating its 60th anniversary.

What, you may ask, is the nature of this mystery? Well, it is the reason behind the name of the company, founded by four engineers in 1964. There is no apparent connection between any of them and the name of our company.

Looking back on those formative years, what is known is the initial focus, a combination of stainless-steel fabrication and tungsten-inert-gas welding for high-vacuum applications, an emerging technology of the time. Alongside this, we distributed American-made micro-welders and ion pumps.

Like many small and successful start-ups, we quickly expanded our portfolio. Three years in, we started to make Joule-effect evaporators, vacuum chambers and a series of accessories. It's a direction of travel that continued into the 1970s, when our design office would draw plans for increasingly complex chambers. Such work drove our first technological shift, as we moved into the production of analytical instruments, such as Auger spectroscopes and low-energy electron diffraction systems.

During this time of transition, our clientele expanded from research laboratories to include industrial companies. We also developed new accessories, such as valves, ultra-high vacuum (UHV) linear and rotary feedthroughs, and many other components.

Pioneering MBE

A major milestone came in 1974, when we created a unique system at the request of the now legendary pioneer of MBE, Klaus Ploog, who had just started leading a group at the Max Planck Institute for Solid-State Research in Stuttgart, Germany. Using the UHV chamber we provided, Ploog and his co-workers were able to deposit arsenic and gallium via evaporation. Their efforts led to the development of the first Knudsen cells, comprising a graphite

crucible 2 cm^3 to 3 cm^3 in size, accompanied by a thermocouple and a heating element spiralled around machined alumina. Samples produced in this chamber were just 10 mm in size.

Our driving force behind these fledgling MBE tools is Pierre Bouchaïb, the product manager during our formative years. While the nature of the growth in this chamber was yet to be christened MBE, this work marked the beginning of increasing interest in this technology from laboratories like IBM, Bell Labs, NEC, Rohm and Sony. All would go on to play a key role in the development of this class of epitaxy.

From these early days onwards, MBE has advanced in both its capability and the performance of the growth tools. Critical to this progress are the partnerships that we have formed with our users. We have a deep commitment to collaboration, which is part of our core values. As Bouchaïb used to say: "Our only limit is the imagination of our clients."

As interest in MBE expanded throughout the 1970s and beyond, with research groups keen to explore the mechanisms behind the growth of material, we shipped more and more systems. Often designed for research, they could accommodate substrates up to 2 inches in diameter, but would often be used to produce epilayers on smaller platforms.

During the 1980s, we reached a manufacturing milestone, passing the production of 100 systems sold in 1984, and we also received a strong endorsement from a master of MBE, Al Cho. Often referred to as the father of this particularly growth technology for his trailblazing work at Bell Labs, Cho visited our headquarters on the outskirts of Paris during the 1980s, and paid tribute to the key features of our MBE tool. He argued that the best MBE machines should exclusively feature a liquid-nitrogen cooling unit, cells and a manipulator, as anything else was a source of contamination. Our systems are built around these core principles.

From research to industrialisation

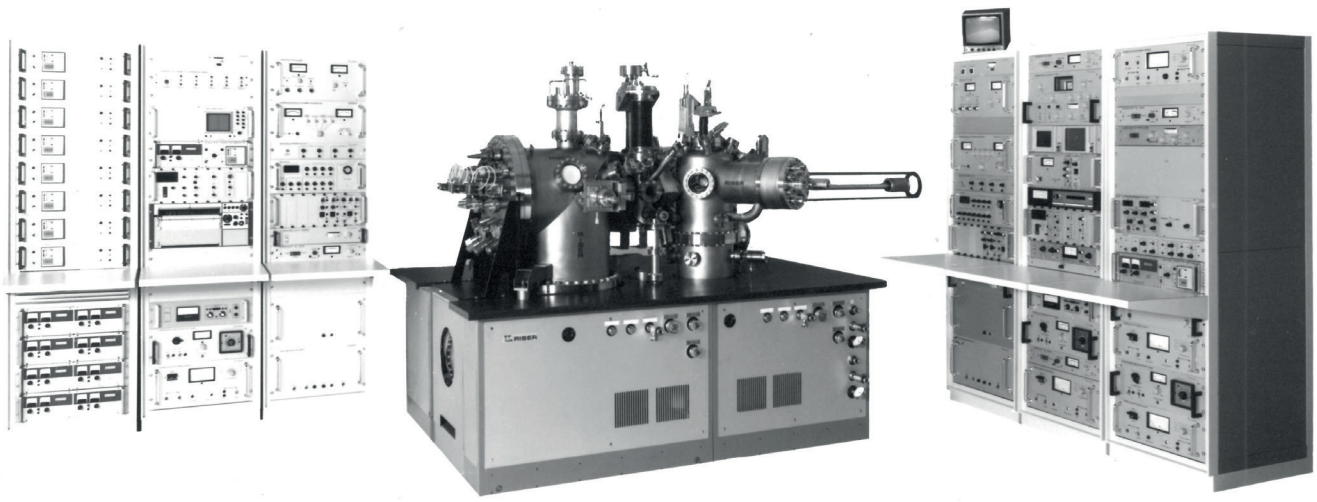
Inspired by scientific discoveries, many new commercial applications related to compound semiconductor devices have emerged since the 1990s. To support this, we have expanded our portfolio, introducing more industrial machines. This includes the MBE 49, our first fully automated industrial prototype, unveiled in 1990. Developed for the company Bandgap in the US, this reactor broke new ground by enabling several substrates to be grown simultaneously.

We have also advanced our effusion cell technologies. A great deal of progress has been made with valve cells for cracking group V elements, enabling a significant increase in the arsenic incorporation on substrates; and we have also improved cells for group III elements, which now offer capacities of several hundred cubic centimetres.

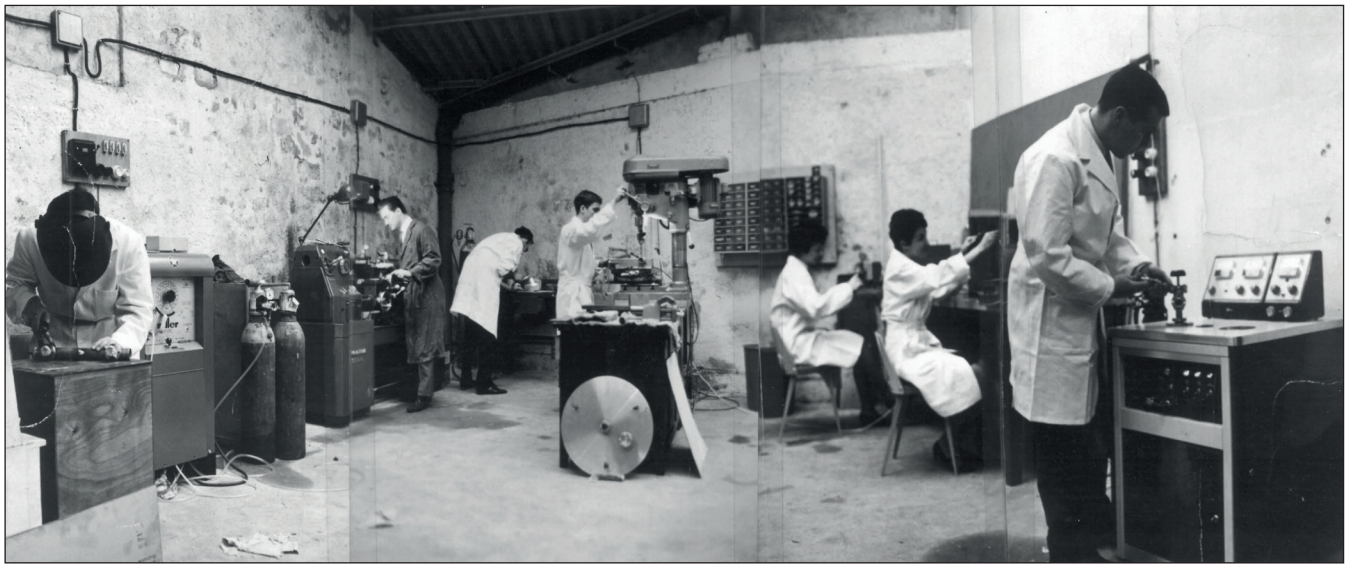
A key juncture in our history came in 1994, when we decided to focus exclusively on producing MBE systems. At this point in time we divested our instrumentation division, now known as the company Cameca. Back in the early 1990s, our portfolio included secondary ion mass spectrometers, instruments for Auger spectroscopy, and low-energy electron diffraction systems.

Our focus on MBE has helped us in our efforts to develop new tools. In 1997 we launched the MBE 6000, which offers double the capacity of the MBE 49. This hit the market at a time when production systems in an industrial setting were gaining substantial traction, with around 50 already operating worldwide.

Throughout our history, we have continued to innovate, never resting on our laurels. This willingness to keep pursuing excellence and questioning what might be best has led us to some fundamental changes. Through a project called ANISET, named after a spirit that's well known and



➤ Riber's first MBE system. Photo from 1980.



➤ The starting assembly room. Photo from 1964.

appreciated in the south of France and has the taste of aniseed, we worked with Jean Massies and his team at CRHEA in the late 1990s to transition MBE reactors from a horizontal to a vertical design. Since then, this new geometry has become the standard for MBE growth.

Today we offer an extensive range of MBE reactors for research and production. Our focus is on improving the reproducibility, stability and uniformity of our machines, goals that we are helping to fulfil through sustained work on manipulators and cells. Through our acquisition of Addon in 2008, we have expanded our product range to include RF cells, as well as cells designed specifically for corrosive materials, such as antimony, magnesium and tellerium. Another advance is our introduction of a 'cluster' version of our machines, providing full flexibility and automation. This move has been motivated by the emergence of centres of excellence, and the pooling of machines by multiple working groups.

➤ Today's cleanroom at Riber, featuring an MBE 6000 system.

Silicon photonics and quantum materials

Last year, we launched the highest capacity machine on the market: the MBE 8000. This highlights how we have come full circle, from the most advanced research machine to the most demanding production system.

Today, as well as selling state-of-the-art MBE tools, we also offer the hardware to support exceptional epitaxy. We provide our clients with real-time, *in-situ* control, featuring feedback loops on all growth parameters, thanks to a range of optical instruments called EZ-Tools that are compatible with our entire product range.

The capability of our instrumentation never stands still, thanks to ambitious development at Epicentre, a joint laboratory between ourselves and LAAS-CNRS.

We are also playing a key role in emerging technologies, such as silicon photonics. We are developing a platform called ROSIE - Riber oxide silicon epitaxy – that will enable the growth of barium titanate on 300 mm silicon substrates. It's a project that's addressing the challenge of the adoption of this technology in high-volume silicon fabs.

Alongside this, we are finalising the validation of a quantum platform that combines standard epitaxy with 120 K epitaxy to produce superconducting materials. Over the coming months we shall start to offer this opportunity to the MBE community.

Like the compound semiconductor industry, we have come through some challenging periods. But drawing on 60 years of success, we continue to be a key player, ready to tackle the challenges that will lie ahead for the next 60 years.

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GaN: Going Beyond Fast Charging
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Maintaining Momentum for the microLED
Apple's decisions to terminate its venture with Osram has sent shockwaves through the microLED industry. But this emitter still has tremendous potential that will be set free with the introduction of novel technologies.

Optimising Opportunities for SiC success
As sales of electric vehicles stutter, SiC revenues could face some bumps in the road ahead. So, what's the best approach to optimising returns in these uncertain times?

Expanding the Emission Envelope
What strategies will extract an even better performance from the various classes of lasers and LEDs? And what applications could benefit from these superior sources?

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Higher bandgaps promise to propel the performance of power devices to a new level. But which materials have the greatest potential? And what's must be done to unlock this promise?

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ANGEL EVENTS

Promoting the PCSEL

There's no question that the PCSEL has a wonderful set of attributes. But can it find its killer application?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

IT'S OFTEN SAID that the speed of technological advance is gathering pace, and now occurs at breakneck speed. And for many consumers this is their experience. But we may question this view, drawing on our understanding of what it takes to make real progress with a ground-breaking idea.

Whether we work in the power electronics sector, or in optoelectronics, we appreciate that it takes countless hours to simply get a new device to work well. And before that novel chip even gets close to being a successful consumer product, there is an inordinate amount of work to do, which includes ramping this device in volume at an acceptable yield and securing lucrative customers contracts.

The many challenges faced when climbing this mountain to successful commercialisation explain why it often takes decades to go from promising results to high-volume production. It's a pathway that all devices must follow, including that of the PCSEL – the photonic-cavity surface-emitting laser – that is now celebrating its 25th anniversary. This class of laser, which employs a photonic crystal to provide optical feedback, has a wonderful set of attributes, including: the emission of an incredibly narrow, single-mode beam, that ensures exceptional brightness; and the opportunity to span a vast range of wavelengths. However, the PCSEL is by no means a mature device, and there's still a long way to go before it will ever be considered a commercial success.

To discuss the PCSEL's progress to date and map out its possible future, those that are developing this technology, along with those that are simply curious about its prospects, gathered on 7-8 November at Aston University.

Based on the number of delegates attending this inaugural face-to-face meeting, interest in the PCSEL is rocketing. The organising committee, led by Richard Hogg from Aston University and Adam McKenzie from the University of Glasgow, hoped to attract 40 or so to this two-day workshop, based partly on attendance at a couple of recent on-line meetings. So, they were delighted and enthused with an attendance of around 120, which drew on those working in academia and industry. While those from academia dominated the agenda, presentations were given by Vector Photonics and Huawei, and those attending included

➤ Above: Aston University, which is located in the heart of the UK's second biggest city, Birmingham, hosted *The International Workshop on PCSELs 2024*.

representatives from nLight, Trumpf, Lumentum, Mitsubishi Electric and ASML – the latter is keen to uncover a more efficient source in the extreme UV for production of state-of-the-art silicon ICs.

PCSEL progress

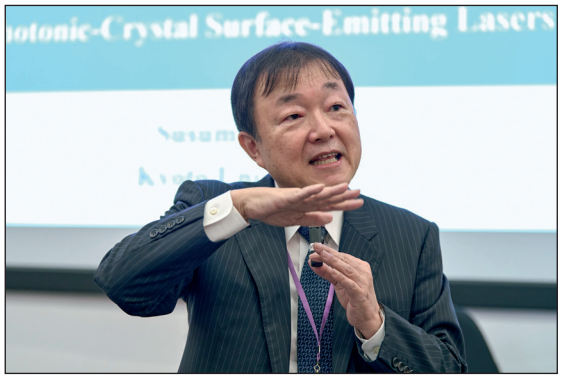
There's no doubt that securing a presentation from the pioneer of the PCSEL, Susumu Noda from Kyoto University, helped to drive up attendance at the International Workshop on PCSELs 2024. During his keynote address, he spoke about improvements in the performance of this device and its many potential applications.

Many will view lidar as just a technology for self-driving cars. Noda, though, has identified many more opportunities, all where the PCSEL can provide the light source. He believes that lidar has a role to play in the smart mobility of robots, farm machines and construction machines, and this laser-based technology can also be used for weather sensing.

The Kyoto academic argued that in addition, PCSELs can be deployed for laser-based processing. Such applications include smart manufacturing of electronics, solar cells and automobiles. And there are also opportunities for this form of surface-emitter in the entertainment industry, in laser-based displays, and in medical applications, where this source can perform the function of a scalpel.

Looking in more detail at these applications, Noda added that the weaknesses of conventional lasers include a low beam quality, a large divergence angle, and low functionality, which includes a lack of beam scanning. Such issues may be addressed with additional optics, but the upshot is a bottleneck to applying semiconductor lasers.

Another downside of the current lasers used in some industries is their size. CO_2 lasers can be 1.5 m in length, and fibre lasers have dimensions of



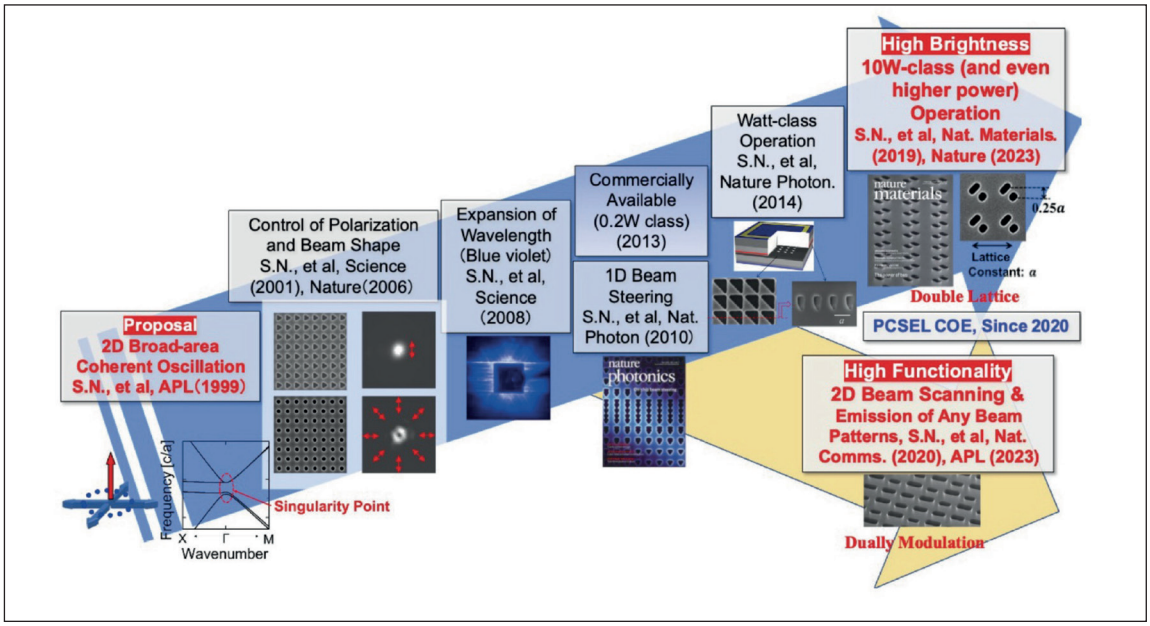
➤ Kyoto University's Susumu Noda, pioneer of the PCSEL, is behind many of its advances.

50 cm. While the PCSEL may be larger than some compound semiconductor chips, it's still orders of magnitude smaller than those lasers.

Since proposing the PCSEL in 1999, Noda and his team have taken significant strides in improving its performance. Major milestones include: the commercial availability of a 0.2 W class PCSEL in 2013; embedding air holes in 2014; and the realisation of 10 W class devices in 2019, aided by the introduction of a double lattice. More recent highlights include a PCSEL with an active area of 500 µm that delivers a low-divergence 20 W beam at room temperature, the realisation of single-mode emission from -40°C to 100°C, and a maximum brightness of at least 1.5 GW cm^{-2} sr^{-1}.

With PCSELs, power scaling stems from increasing the size of the emitting circular region. Diameters of 10 mm or more could lead to powers of 1 kW or more.

Noda and his colleagues have produced a single-mode PCSEL with a 3 mm active area that has a threshold current as high as 25 A, a divergence of 0.5°, and a brightness of 1 GW cm^{-2} sr^{-1}. To demonstrate the capability of this laser, driven at typically 100 A, Noda shared a video that shows how this source easily cuts through stainless steel.



➤ Milestones by Susumu Noda's group from Kyoto University.

A few years ago, Noda and his colleagues established a Centre for Excellence for PCSELs at Kyoto University. This 100 m^2 facility, featuring a fabrication line for the PCSEL, has space for companies to play their part and explore commercial opportunities for this device. More than 140 firms are involved in this work at this centre

If an even more powerful source is required, one option is to unite the output of several PCSELs by forming an array of them. Noda and his colleagues have considered this, as well as increasing the active region, with impressive results realised with the latter approach – they are soon to be shared.

Most of the work from Kyoto University has involved GaAs-based PCSELs emitting in the infrared. However, the team have also worked with other material systems. In 2022, they reported Watt-class GaN PCSELs with a divergence angle of 0.2°; and they have also explored the InP/InGaAsP material system that provides emission at the key telecom wavelengths of 1.3 μm and 1.55 μm, producing a source with an output power of more than 300 mW.

A few years ago, Noda and his colleagues established a Centre for Excellence for PCSELs at Kyoto University. This 100 m^2 facility, featuring a fabrication line for the PCSEL, has space for companies to play their part and explore commercial opportunities for this device. More than 140 firms are involved in this work at this centre. Efforts to promote the PCSEL could also get another helping hand from a Kyoto University, with the launch of a spin-off PCSEL maker slated for late next year.

➤ A key player behind the International Workshop on PCSELs 2024, the inaugural face-to-face meeting for the ever-growing PSCEL community, is Richard Hogg from Aston University.

The Scottish start-up

Another key player driving the commercialisation of the PCSEL is the University of Glasgow spin-off Vector Photonics. Speaking on its behalf at the two-day workshop, company CTO Richard Taylor emphasised that PCSELs are "material agnostic". Thanks to this attribute they can span an incredibly wide wavelength range, realised with devices made from InP, GaAs and GaN material systems, and incorporating both interband and intraband transitions.

Taylor briefly described the process that Vector Photonics employs to produce its VCSELs, with steps that include electron-beam lithography and epitaxial layer overgrowth. While many PCSEL developers have air holes in their devices, Vector Photonics has the capability to fill holes created in a photonic crystal lattice with compound semiconductor material, such as *p*-doped GaAs, prior to planarization of the surface.

Like Noda, Taylor discussed a number of potential applications for the PCSEL. He shared data showing that InP-based devices emitting at around 1.3 μm can target specific emission wavelengths through adjustments in the spacing of the photonic crystal lattice. These devices are candidates for the source for dense wavelength-division multiplexing. According to Taylor, there are also opportunities for PCSELs in free-space communication, in material processing, in lidar, and in displays, where they enable low speckle.

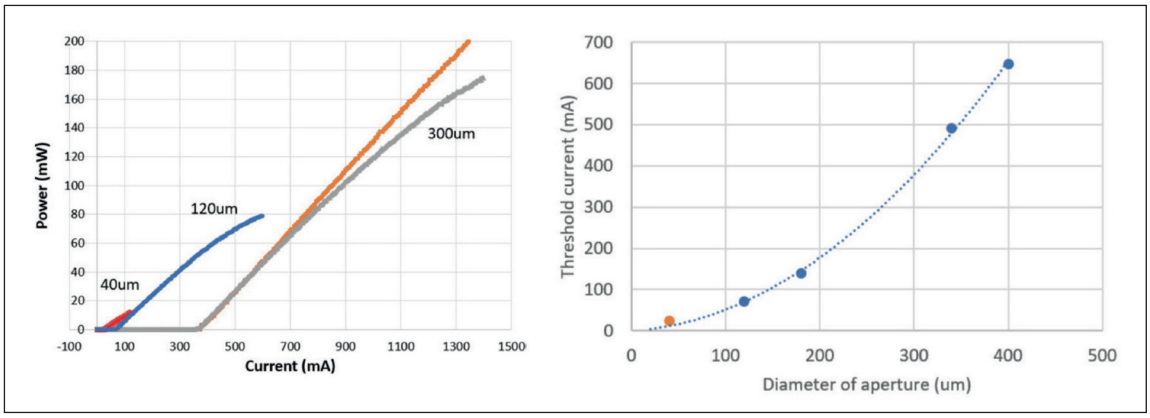
Huawei's first steps?

In terms of industrial development of the PCSEL, the UK is very active – as well as Vector Photonics, much work has been undertaken at Huawei's Ipswich Research Centre (IRC). Two perspectives from this facility were provided at the workshop: details of progress in developing InP PCSELs were outlined by senior device engineer Karl Boylan; while Graham Berry, the CTO of the research centre, offered a view on the prospects of this device in a number of markets.

Huawei's IRC, formed in 2012, is well suited to developing III-V optoelectronics. Within this facility, employing 180 staff, are MOCVD tools, plus those for processing wafers into chips and packaging them.

Engineers at the IRC have been investigating InP-based PCSELs, viewed as a disruptive technology, as alternatives to distributed feedback and edge-emitting lasers at 1.3 μm and 1.5 μm.

Boylan revealed that for this work, the team developed PCSELs based on the InGaAlAs material system. He argued that the merits of this particular alloy include a higher differential gain than InGaAsP, and thanks to a high conduction band offset, operation over a wide temperature range.



➤ Figure 1. Results by Huawei demonstrate power scaling of the PCSEL, realised by increasing the aperture of this class of laser.

To support development efforts, the team from the IRC has been working with Ana Vukovic's group at Nottingham University. Vukovic and co-workers have helped with design and simulation, investigating how the depth profile influences performance. Based on this work, 'safe zones' have been identified for single-mode performance that are less critical to small changes in PCSEL parameters.

Devices produced by the IRC include a PCSEL emitting at 1.3 μm that delivers a CW output power of 330 mW at 2 A, and has a power conversion efficiency of 15 percent. Under pulsed operation at 5 A, output power is almost 1 W. "All in all, quite good results for us," remarked Boylan.

Additional measurements revealed a side-mode suppression ratio of more than 50 dB, and linearly polarised emission in the far field with a degree of polarisation of more than 95 percent. Boylan and his co-workers have also demonstrated scaling of output power with aperture size (see Figure 1).

Efforts have also been directed at developing 1.55 μm PCSELs. Those at the IRC have produced lasers with a double-lattice design that feature encapsulated air holes beneath the InGaAlAs active region. For these PCSELs, the side-mode suppression ratio is more than 40 dB. Measurements also determined pulsed output powers of 171 mW at 25°C and 40 mW at 85°C, and a power conversion efficiency of 7.8 percent.

A reality check

The downside of any group of enthusiastic device developers is that their optimism threatens to lead to an inflated view of prospects. Due to this, the delegates will have benefitted from hearing the level-headed view of Berry.

Let's be clear Berry is a fan of the PCSEL, and would be delighted to see this class of laser displacing the incumbents. But to do so, the PCSEL will need to navigate what's described as the 'Darwinian Sea' and emerge with a compelling set of credentials for deployment.

For the PCSEL, fabrication within different material systems leads to differing levels of maturity. So, there's a need to consider the potential of this device on a case-by-case basis. Berry has identified opportunities for deployment in communications systems, automotive lidar, sensing, laser processing and displays. And he has gone on to consider, in detail, the potential for the InP PCSEL to enjoy commercial success as the pump laser for Raman amplifiers, the CW light source for silicon photonics, and the laser for gas detection.

To win deployment as the pump laser for Raman fibre amplifiers, the PSCEL will have to compete with the grating-stabilised Fabry-Pérot laser, which produces an output power of around 600 mW that is coupled into a fibre. Users of these amplifiers would prefer higher power sources, possibly producing two-to-three times as much power. It's a goal that might be fulfilled with distributed feedback lasers, with engineers at Huawei's Yuanfeng Mao Optical Research Department in Wuhan having produced devices with a 4 μm-long cavity that emit more than 850 mW per facet. In comparison, PCSELs produced at the IRC deliver up to just over 1 W when driven in pulsed mode, with a performance that could be improved by optimising the *p*-side reflector. Based on this analysis, to succeed in this application, Berry believes the target is a cooled 2 W InP PCSEL.

For silicon photonics, lasers are deployed in two different ways. One approach is to use an uncooled single-laser source and split the output into 4 or 8 lanes; and the alternative is a number of lower-power, cooled sources with close channel spacings. Buried heterostructures lasers with distributed feedback are the incumbents for providing a single source. According to Berry, devices produced by Casala Technologies and operating at 75°C can deliver up to 200 mW at 800 mA. He pointed out that PCSELs only deliver this power at up to 45°C, and there is also a need to reduce their aperture size, a move that demands improved thermal management.

For applications such as AI, high-performance computing and high-density optics, leaps in performance, efficiency, cost and bandwidth will be enabled by an increase in the number of wavelengths deployed. Berry cited Sivers' demonstration of wavelength-division multiplexing,

using 32 distributed feedback lasers operating in a 16 nm window with a 0.5 nm spacing. If PCSELs could be flip-chipped onto a silicon platform, this could lead to a substantial reduction in the size of the laser array. Distributed feedback lasers produce 20 mW at 45°C when driven at 100 mA, a level of performance that is certainly possible with a PCSEL, according to Berry.

Gas sensing, the third application Berry has considered in detail, can be served by InP-based VCSELs, such as those made by Vertilas. These are relatively difficult to produce, requiring dielectric mirrors and tunnel junctions. Distributed feedback lasers with short cavities are also competing for the gas sensing market, and if PCSELs are to succeed, they will need to address current-spreading issues.

A killer application?

Discussions on the commercial opportunities for the PCSEL also took place during an Industry Round Table session. No consensus on a killer application emerged, but a number of areas for improvement were identified. Both VCSELs and edge-emitters have significantly superior power-conversion efficiencies to the PCSEL, and improvements in this regard would make this device more compelling and aid its thermal management.

There are also concerns related to reliability and yield, topics that tend to attract more activity from industrial developers than those in academia. Some work by Vector Photonics has produced encouraging results. Noda also commented on reliability, saying it's rare to see failures, probably due to the low photonic density in these devices.

Those in industry would be delighted for those in academia to direct their efforts at issues that will help drive the commercialisation of the PCSEL, such as studies related to thermal management and reliability. But based on many of the presentations at The International Workshop on PCSELs 2024, many university researchers are more likely to be interested in either: stretching the emission of this device deeper into the UV or further into the infra-red, considering how topological features can control certain aspects of the PCSEL; or investigating the nature of the polarisation that's emitted.

In its first 25 years, the PCSEL has certainly come a long way. It's now capable of delivering many watts using incredibly narrow beams, leading to tremendous figures for brightness. Such strengths are pulling researchers from academia and industry into an ever-growing community, which continues to progress the PCSEL. It now feels that this device nearing significant commercial success, but critical to this is if – and it's a big if – there are targeted improvements, helping the makers of this device excel when they pursue the right applications.

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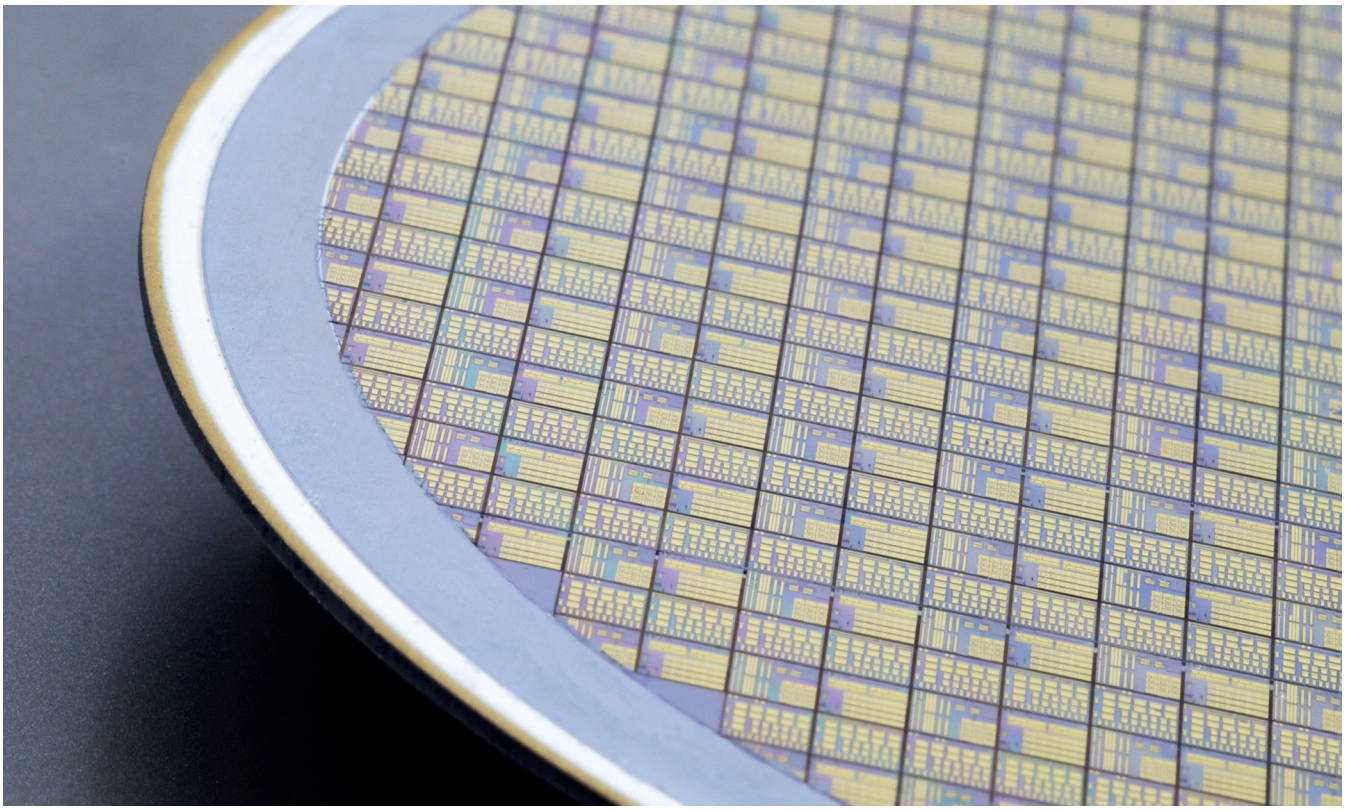


Vertical power devices with thick GaN layers on sapphire

Tuning of wafer bow by stealth laser patterning enables the growth of thick epitaxial layers of GaN on sapphire for vertical high-voltage devices

BY ELDAD BAHAT TREIDEL, ENRICO BRUSATERRA, FRANK BRUNNER, ALEXANDER KÜLBERG AND OLIVER HILT FROM FERDINAND-BRAUN-INSTITUT (FBH)

DOMINATING THE HEADLINES of our industry are the vast sums spent on building new SiC fabs and expanding the capacity in existing facilities. In general, such efforts are directed at increasing production of 1.2 kV MOSFETs, a key component in electric vehicles that is helping to maximise their range.

It is beyond question that the SiC MOSFET outperforms its silicon equivalent. But it could be outclassed by vertical GaN-based power switching devices, which promise a superior bang-per-buck.

Leveraging the potential of this class of GaN-based power devices will not be easy – it requires addressing of a number of key challenges. These include: growing a *p-n* diode on a very thick drift layer that has a well-controlled low doping concentration and supports a high blocking voltage; realising a low forward resistance; and ensuring avalanche capability and short-circuit robustness. Finally, the device heterostructure must be compatible with standard process lines.

It is not clear what the most suitable foundation for this device is. While GaN substrates are attractive from a material quality standpoint, their size is limited to between 50 mm and 100 mm, they come at a high price of around \$150 cm^{-2}, and have a relatively high resistivity, exceeding 1 mΩ cm and going up to 50 mΩ cm. Due to these limitations, foreign substrates are usually employed for such devices, with silicon and sapphire being the leading candidates. For both options, the backside drain contact can be established after either local silicon substrate removal, or the removal of the sapphire substrate by laser lift-off.

Regardless of the choice of foreign substrate, heteroepitaxy impairs material quality, with GaN

suffering from an increased dislocation density. Compounding this concern, a blocking capability larger than 1.2 kV demands GaN epitaxial layers with more than 10 μm thickness, magnifying issues associated with lattice mismatch and differences in the thermal expansion coefficients. These issues include increases in threading dislocation density, leakage current, mechanical strain, fragility and wafer bow.

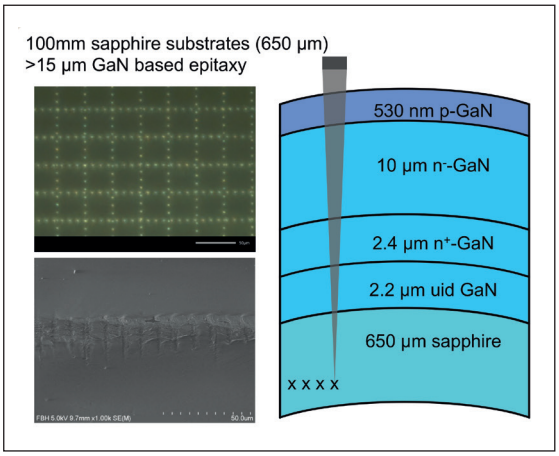
A laser focus

The team at the Ferdinand-Braun-Institut (FBH) is addressing all these issues with a novel approach that employs laser patterning. At the 2024 CS Mantech conference, a technology was unveiled allowing to grow GaN drift layers that are more than 10 μm thick on 100 mm sapphire substrates. Without further measures the resulting high wafer bow would make these wafers un-processable on commercial equipment designed for flat silicon wafers. Progress on this front allowed the demonstration of fully functional quasi-vertical electronic devices, in the form of *p-n* diodes, offering a reverse blocking capability of 1.2 kV.

Key for this success was previous work at FBH on using a focused laser beam to reduce the bow of GaN-on-sapphire-based UV LED wafers. To this end, localised damage inside the sapphire substrate, close to its backside surface was created by a tightly focused laser beam. This damage compensates the internal stress that stems from the large lattice mismatch between the epitaxially grown GaN layers and the sapphire substrate.

With this approach it was possible to reduce bow of sapphire wafers with a diameter of 50 mm and an overall thickness of less than 450 μm. However, upscaling of this technology requires extension to larger wafers with even thicker epitaxial GaN layers. Characterisation of 100 mm GaN-on-sapphire wafers with a total GaN layer thickness above 15 μm shows encouraging results.

At FBH we have an industrial process line that tolerates a wafer bow of less than 125 μm,

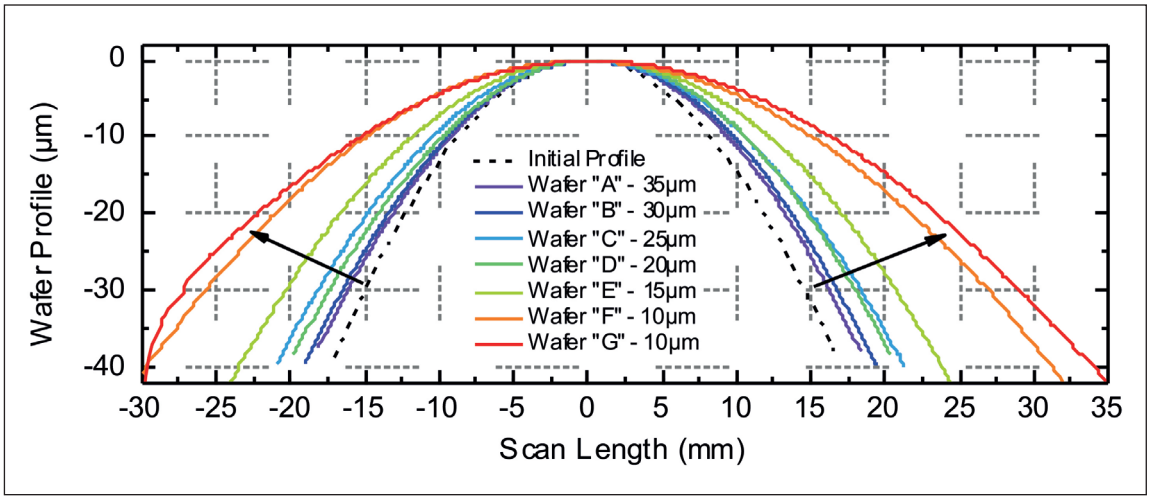


➤ Figure 1. Laser grid pattern top view with 30 μm pitch (top left) and cross-section of the laser damage along one scribe line, resulting in 10 μm of laser spacial period (bottom left). Illustration of the laser scribing process (right).

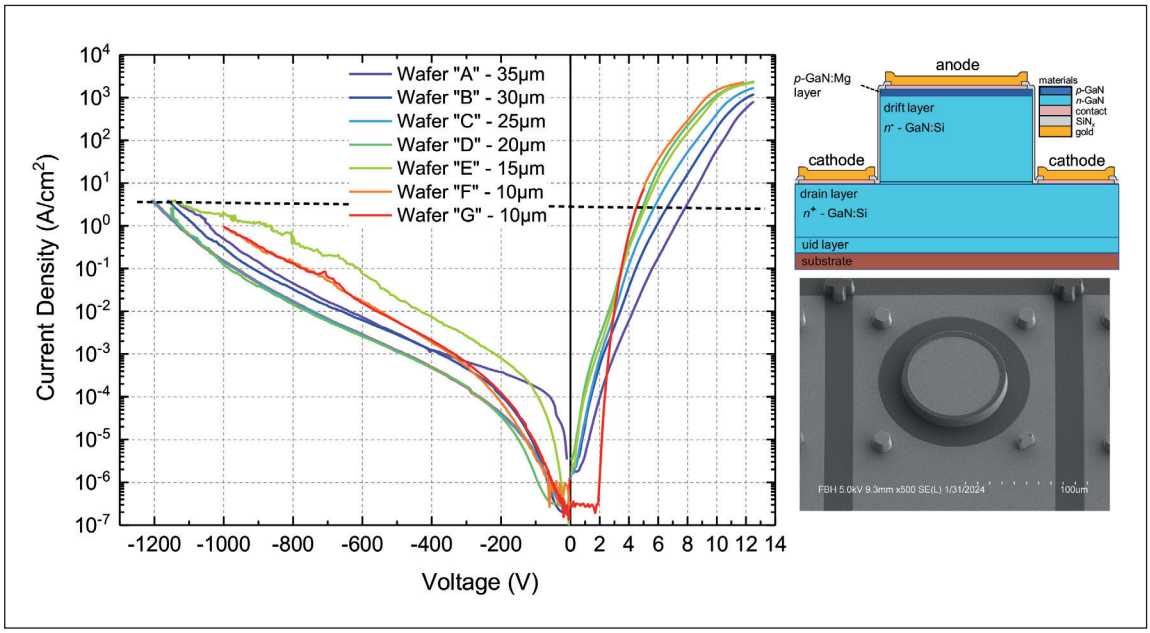
corresponding to a radius of curvature of more than 10 m. However, even with such an accommodating line, wafers with a high bow, but still within process limitations, can still present conformity issues, such as those associated with automated robotic handling, vacuum handling, and uneven temperature exposure.

Our investigations of the impact of laser scribing of GaN-on-sapphire wafers include bow measurements as well as electrical characterization of processed quasi-vertical *p-n* diodes.

The fabrication of our devices began by loading 650 μm-thick sapphire substrates with a diameter of 100 mm into an MOCVD reactor and depositing a 2.2 μm-thick unintentionally doped GaN transition layer, followed by a 2.4 μm highly conductive *n*-type GaN bottom layer, and a 10 μm n^--GaN drift layer with donor density of 1.4×10^{16} cm^{-3}. The doping concentration of the drift layer was assessed with on-wafer electrochemical capacitance-voltage measurements and post-processing capacitance-voltage measurements. After growth of the drift layer, we added a 530 nm-thick top *p*-type layer to form a *p-n* junction and an anode terminal. This structure has a total GaN epitaxial layers thickness of more than 15 μm, and produces an initial wafer bow of around 300 μm, corresponding to a wafer



➤ Figure 2. Optical interferometric bow profile for a range of wafers with different scribing pitches.

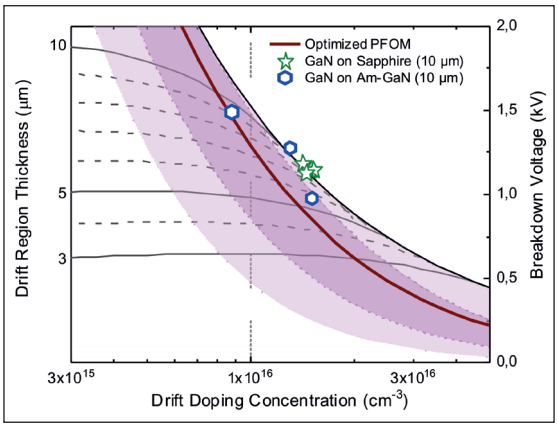


➤ Figure 3. Wafer-level median reverse and forward characteristics for quasi vertical *p-n* diodes produced on wafers with a different scribing pitch (left). An illustration of the cross-section of a quasi-vertical *p-n* diode (top right) and a scanning electron microscopy image of such diode (bottom right).

radius of curvature of about 3.8 m if no measures for bow reduction are applied.

Using a fixed focus depth and scribing pitches ranging from 10 µm to 35 µm, these wafers were patterned by focused laser irradiation from the top side through the epitaxial layer stack. The resulting damage is located around 200 µm above the bottom surface of the sapphire substrate. We employed a 532 nm laser with a repetition rate of 40 kHz, using a feed speed of 400 mm s^{-1} and a continuous laser power of 160 mW, with the focus of the laser inside the sapphire.

The scribing pattern lines are running perpendicular to the flats with the prescribed pitch. Scribing began in the *x* direction (perpendicular (or parallel) to the main flat), and then in the *y* direction, with total processing time roughly 4 hours per wafer.



➤ Figure 4. A comparison of the performance of GaN-on-sapphire quasi-vertical *p-n* diodes with the ideal breakdown voltage values.

Perfect pitch?

Optical interferometric bow profile measurements at different scribe densities revealed that wafer bow progressively is reduced with decreasing pitch. A smaller scribing pitch produces a monotonic increase in the radius of curvature, and bow reaches values as low as around 40 µm, realised with scribing pitch of 10 µm. Note that the change to the radius of curvature resulting from laser scribing is inversely proportional to the scribing pitch.

To evaluate the impact of this bow reduction on processability and device performance, we processed quasi-vertical *p-n* diodes on our line.

We compared devices from wafers with different bow values after laser patterning with different scribe pitch. The reverse-bias off-state current and blocking strength is only marginally impacted by the scribe pitch. In sharp contrast, the onset voltage of our *p-n* diodes is strongly dependent on the laser scribing pitch. This most probably is related to the strain in the layers that is not accommodated by wafer bow.

Our work shows that the laser scribing of sapphire substrates with thick GaN epitaxial drift layers is a potential route for high-volume manufacturing of 1.2 kV vertical GaN devices on low-cost foreign substrates if the carrier concentration in the drift layer can reproducibly be adjusted to about 1×10^{16} cm^{-3}.

This work has received funding from the ECSEL Joint Undertaking (JU), under grant agreement No 101007229. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Germany, France, Belgium, Austria, Sweden, Spain, Italy.

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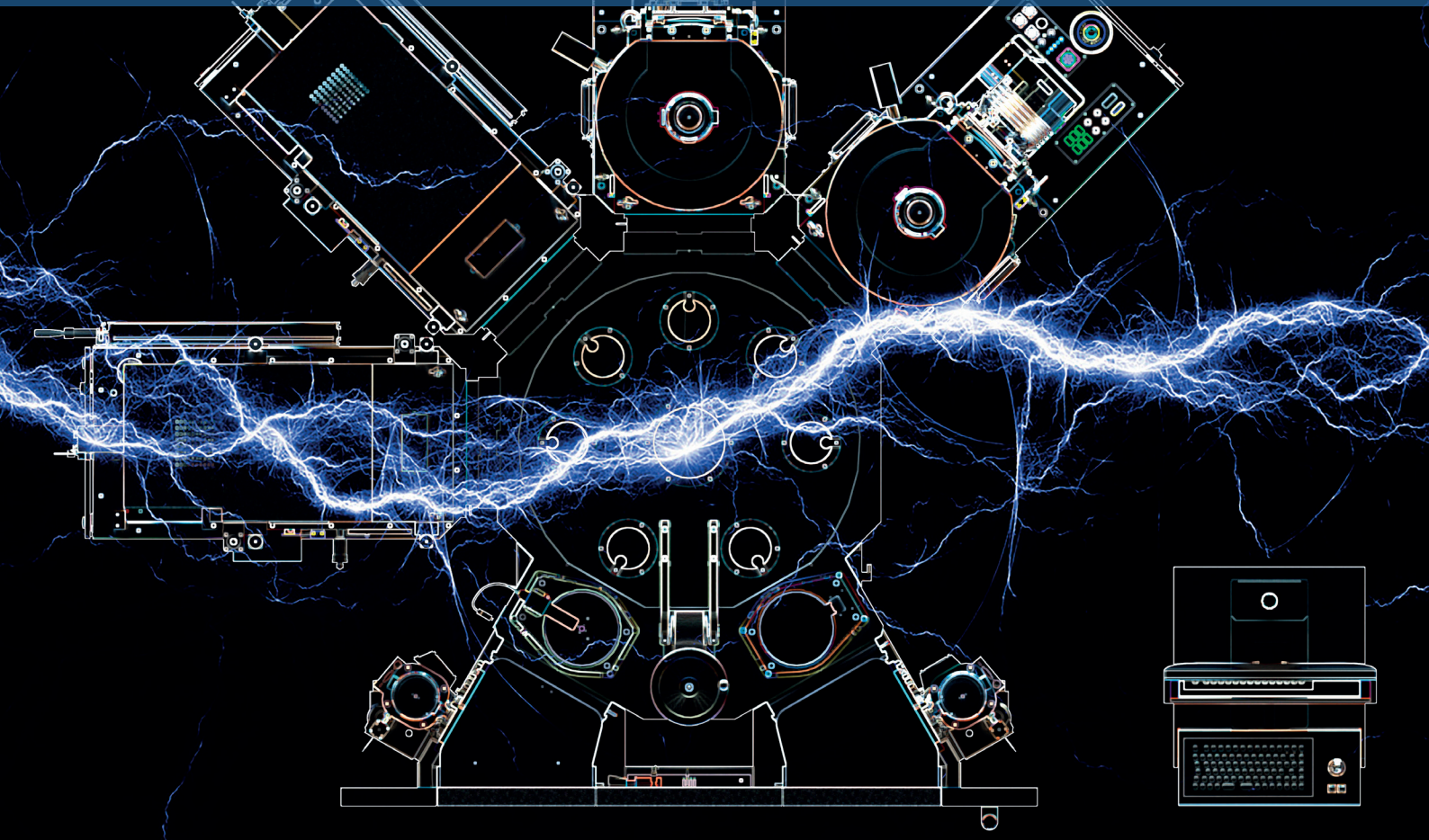

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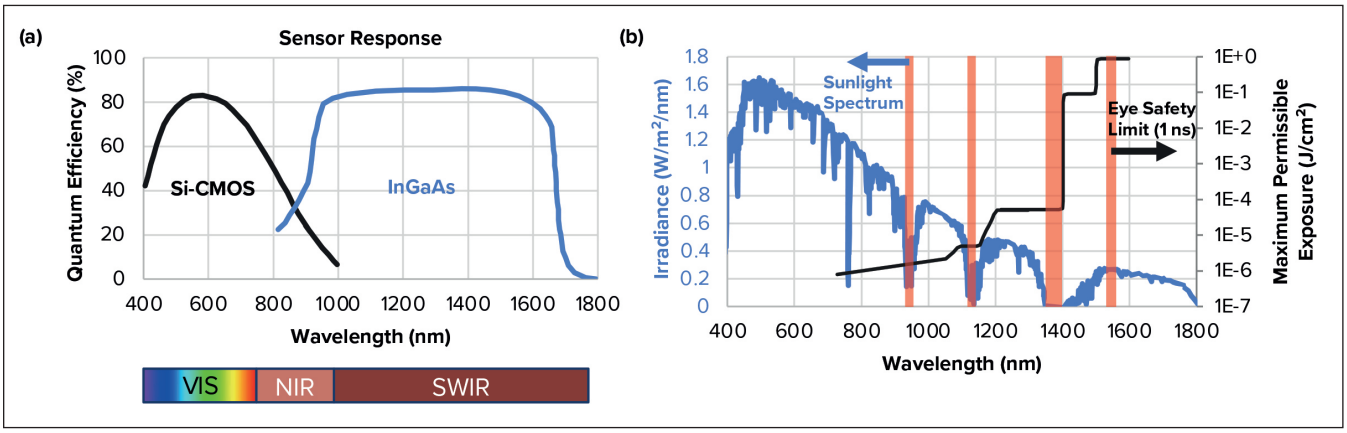
Realising high-performance sensors with heterogeneous integration

Manufacturing InGaAs photodetectors directly on CMOS silicon revolutionises shortwave infrared sensors for consumer markets

BY BEI SHI AND JONATHAN KLAMKIN FROM AELUMA

IN QUITE A NUMBER of applications there is much demand for scalable, low-cost, high-performance sensors. Such sensors are wanted for autonomous systems, robotics, defence and aerospace technologies, artificial intelligence (AI), mobile phones, smart watches, and augmented reality/virtual reality (AR/VR).

Within the sensor portfolio, those based on silicon CMOS dominate detection in the visible as well as in the near-infrared at wavelengths up to around 940 nm. However, silicon sensors fail to cover the vast majority of the short-wave infrared (SWIR) domain, which spans 900 nm to 1700 nm. That's a significant impediment, because sensors operating within this spectral band enjoy a number of valuable benefits, including: lower solar interference, enabling better outdoor operation; access to highly mature components, including lasers, for illumination-detection scenarios such as light



➤ Figure 1. (a) Sensor response comparison for silicon and InGaAs detectors. (b) Solar irradiance and maximum permissible exposure of eyes to the lidar emitter power from visible to SWIR. Red vertical bars indicate typical lidar operation wavelength bands.

detection and ranging (lidar), which is used in 3D imaging and autonomous systems; performance in the dark, enabling night vision; the possibility to detect in inclement weather conditions, such as fog and rain; and 'eye-safe' wavelengths, which allow for a much higher illumination power in the presence of people – this enables higher-resolution, longer-range imaging for facial identification, lidar, and other 3D imaging applications.

Silicon versus InGaAs

When operating at 940 nm, a wavelength commonly used in mobile devices, silicon detectors benefit from a low solar interference. However, they are held back by a very low detection efficiency. Here a more attractive alternative is InGaAs, which as well as offering a much higher efficiency at 940 nm, is capable of operating in eye-safe wavelength bands. One of the great strengths of InGaAs sensors is that they can cover a much broader spectrum than their silicon counterparts, spanning from the visible to as far as 2600 nm – it's an extensive response that allows them to be used for enhanced night vision and thermal imaging. Within the spectral response of InGaAs detectors sit bands for consumer lidar and 3D imaging at 905 nm to 940 nm, 1130 nm, 1350 nm to 1400 nm, and 1550 nm.

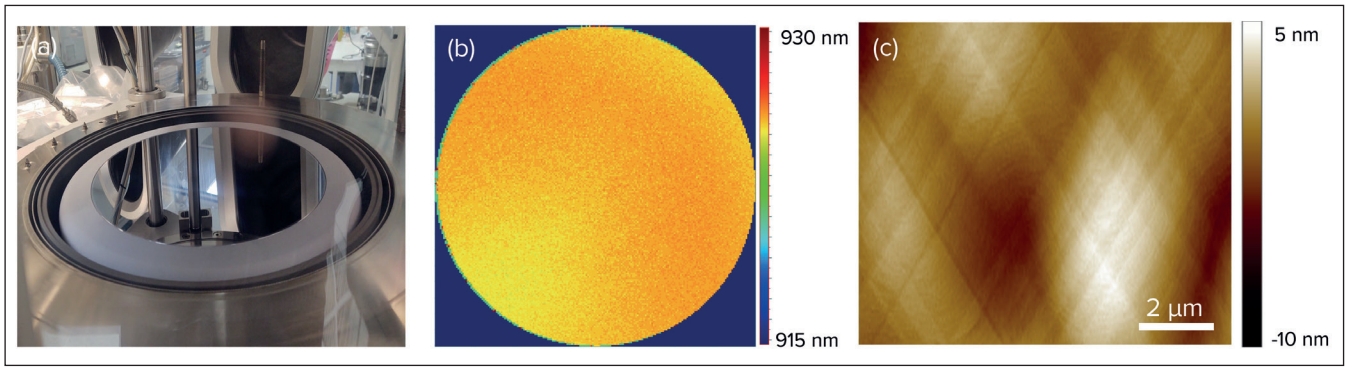
Note that while the first of these, the 905 nm to 940 nm band, is also supported by mature silicon detectors, such as silicon single-photon avalanche detectors (SPADs), it is not eye safe, which limits the maximum detectable object distance. That makes detectors based on the family of InGaAs materials compelling candidates, because they deliver high efficiency detection at longer, eye-safe wavelengths. It should be noted that although InGaAs detectors are not as well-known as those based on silicon, they are proven in many formats, including *p-i-n* photodiodes, linear-mode avalanche photodiodes (APDs), and Geiger-mode APDs that are otherwise known as SPADs. (A comparison of the sensor response of silicon detectors and InGaAs SWIR detectors is shown in Figure 1, and a comparison of photodetector technologies for the near infrared and SWIR sensing applications is provided in Figure 2).

Performance, scale, cost and applicability

Although the quantum efficiency – defined as

	Incumbent technologies		Technologies for scaling and cost reduction		
Technology:	Si SPAD	InGaAs-on-InP	Ge-on-Si	Colloidal QD	**InGaAs-on-Si**
Substrate size:	8 to 12 in.	2 to 4 in.	8 to 12 in.	8 to 12 in.	8 to 12 in.
Eye Safe:	No	Yes	Somewhat	Somewhat	**Yes**
Performance:	Good	Best	Fair	Fair	**Best**
Multiplication (APD, SPAD):	Yes	Yes	Possible	No	**Yes**
Wafer-scale integration:	Yes	No	Yes	Yes	**Yes**
Status:	Mature Scalable	Mature Not Scalable	Maturing Scalable	Maturing Scalable	**Maturing Scalable**

➤ Figure 2. Technology comparison regarding sensor manufacturing scalability, cost and performance. Aeluma is focused on large-wafer InGaAs-on-silicon photodetector manufacturing.



➤ Figure 3. (a) Photograph of 12-inch InP-on-silicon wafer in a deposition chamber. (b) Full-wafer photoluminescence peak wavelength map illustrating excellent uniformity across the wafer. (c) Atomic force microscopy map characterising surface smoothness of an InP film deposited on a silicon substrate.

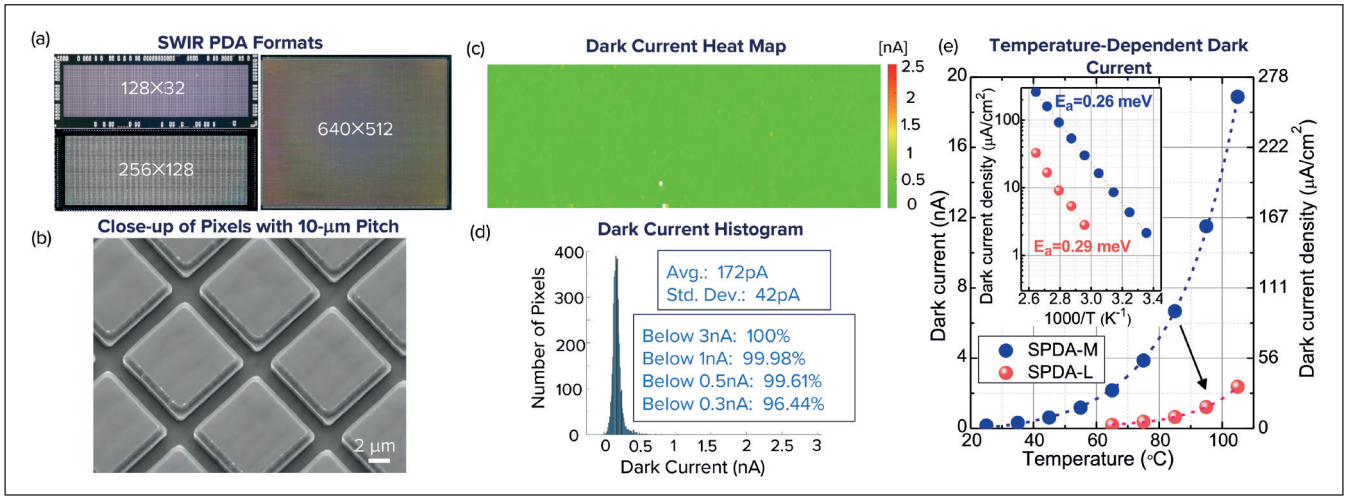
the fraction of incident light that contributes to a photocurrent signal – is low for silicon detectors in the commonly used 905 nm to 940 nm region, that's not stopped this technology from being widely adopted for consumer applications, including mobile devices and automotive lidar. Behind this adoption are cost considerations. Traditional InGaAs detectors are manufactured on InP substrates, which are typically confined to 2- to 4-inches in diameter, and are expensive and fragile. The latter weakness is significant, because it poses handling challenges during manufacturing processes.

Yet despite this fragility, InP is widely used for manufacturing semiconductor lasers operating at SWIR wavelengths for telecommunication applications. Part of the reason for this appeal is that these InP lasers are far smaller than photodetector arrays used for 3D imaging and lidar. This substantial increase in size is an important consideration, because InP technology does not scale to larger substrate sizes, due to its high cost and fragility. But from a performance perspective, InGaAs-on-InP is by far the better candidate for SWIR imaging and lidar applications.

Driven by the demand for high-performance sensors in consumer applications, alternative technologies are generating much attention for SWIR detectors. Contenders piquing much interest include those based on the germanium-on-silicon and colloidal quantum dot systems. Under development, both technologies provide a path for scaling, but they are somewhat unproven, especially for the common 1550 nm SWIR wavelength. What's more, both candidates only provide a limited performance. For wavelengths beyond around 1500 nm, they are impeded by a low quantum efficiency – and those based on germanium also suffer from a high dark current.

InGaAs-on-silicon direct heteroepitaxy

For many years, the direct heteroepitaxy of high-performance compound semiconductors on large-diameter mismatched substrates has been pursued



➤ Figure 4. (a) Photographs of photodetector arrays with various array formats, including 128×32, 256×128, and 640×512. Pixel pitches that range from 10 µm to 90 µm. (b) Close-up scanning electron microscopy image of fabricated pixels with a pitch of 10 µm. (c) Exemplary dark current heat map of the 128×32 photodetector arrays. (d) Extrapolated histogram for yield analysis. (e) Dark current of a single detector pixel as a dependence of the stage temperature, to derive the dark current doubling temperature. Inset shows the extrapolation of the activation energy for two photodetector array structures. The operating bias is -5 V for all data provided in this figure.

for scaling. It's an approach often deployed during the production of GaN devices, due to a lack of affordable native substrates, with chip production beginning with growth of GaN on SiC and increasingly silicon. The use of direct heteroepitaxy, as opposed to other heterogeneous integration techniques such as wafer or chiplet bonding, is a 'leapfrog approach'. These substantial advances are particularly profound for InGaAs detector arrays, which would require expensive, smaller InP substrates to support bonding approaches.

The use of direct heteroepitaxy, as opposed to other heterogeneous integration techniques such as wafer or chiplet bonding, is a 'leapfrog approach'. These substantial advances are particularly profound for InGaAs detector arrays, which would require expensive, smaller InP substrates to support bonding approaches.

At Aeluma, Inc. of Goleta, CA, we are pursuing this revolutionary pathway, using the heterogeneous integration of InGaAs and silicon to unite best-in-class SWIR material with mass-market microelectronics manufacturing. It is a marriage that provides the most viable path to scale for consumer markets while maintaining high-performance sensing.

We believe that we are the first entity to pursue large-volume scaling of components based on arsenide, phosphide and antimonide materials, especially for 3D optical sensing applications. To support this effort, we have established a state-of-the-art 12-inch MOCVD capability that can produce 12-inch epiwafers that have a smooth surface and that demonstrate intense photoluminescence (see Figure 3). Characterising these epiwafers reveals that they are able to support scalable manufacturing processes.

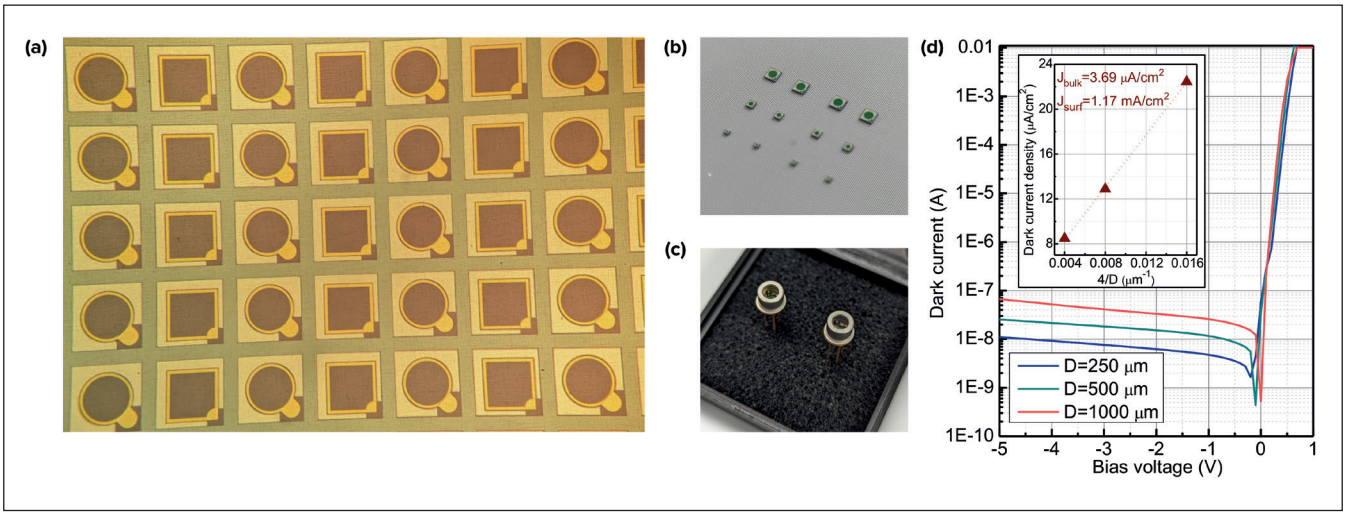
Scalable InGaAs photodetectors

One of the primary products that we have brought to market is the SWIR photodetector array, manufactured on our large-diameter substrate platform. It's a technology that's applicable to 3D imaging, lidar, mobile devices, medical imaging, industrial automation, autonomous systems, and AR/VR (see Figure 4 (a) for images of SWIR photodetector arrays manufactured with our platform).

We have produced a variety of array sizes, including common formats, such as 640 by 512 pixels, a standard for video graphics array cameras. Our pixel size and pitch vary, from only a few microns, up to tens of microns.

Within our portfolio we have the SPDA-M series SWIR arrays. According to a dark current 'heat map' and histogram, an array from this series excels in uniformity and yield (see Figures 4 (c) and 4 (d)). For an operating bias of -5 V, the average pixel dark current is 172 pA, corresponding to a dark current density of approximately 2.4 μA cm^{-2}. This array features 128 by 32 pixels and the pixels have an active area of 85 μm by 85 μm.

Arrays in both our SPDA-M and SPDA-L series deliver a high performance when having to operate at high temperatures. Under these conditions they still have a low dark current (see Figure 4 (e)), with values of just 18 nA for 85 μm by 85 μm active-area



➤ Figure 5. Large-area SWIR photodetector sensors for consumer markets. Images of (a) fabricated photodetectors, (b) bare die, and (c) packaged sensors. (d) Bias-dependent dark current data and inset illustrating dependence of dark current density on device geometry to analyse dark current performance.

pixels from the -M series operating at 105°C, and 2.4 nA for the -L series with identical pixel size at the same high temperature. We have calculated the activation energy, using a formula that involves the dark current, the temperature, and the Boltzmann constant. This calculation determined that the activation energy for the -L series is slightly higher than that for the -M series, indicating that we have the opportunity to improve photodetector material performance even further at higher operating temperatures.

In addition to our SWIR photodetector array, we have developed large-area photodetector sensors for consumer markets. These sensors range in size from 250 μm to 1000 μm, and may be delivered as either bare dies or in standard transistor outline (TO) packages (see Figure 5 for images of these sensors, and a summary of one series of large-area photodetector sensors aimed primarily at operation in the 1300 nm to 1400 nm wavelength band).

One of the strengths of these photodetectors is their dark current density, which can be as low as 8.47 μA cm^{-2} at room temperature. To investigate the various contributions to dark current performance, we have measured the dark current density for differing photodetector geometries with varying diameters (see the inset of Figure 5 (d)).

We have considered the total dark current density to be a combination of that associated with bulk, and that from surface recombination. Based on this analysis, we have determined that the surface leakage generated during device fabrication is the leading contributor to the dark current of our large-area InGaAs photodetectors. This has led us to conclude that while the performance of our large-area photodetectors is sufficient for many applications, we may be able to introduce improvements as we transition to mature, large-volume manufacturing processes.

Integration with CMOS

For camera integration, we unite our photodetector arrays with read-out integrated circuits (ROICs) to form focal plane arrays. Traditionally, die-to-die flip-chip bonding, often using indium solder bumps, integrates SWIR photodetector arrays with ROICs. That's notably different from the approach that's used with CMOS image sensors, which leverage wafer-scale integration, thanks to wafer size and process compatibility. With our large-diameter wafer platform, we are uniquely positioned to enable wafer-scale integration of InGaAs SWIR photodetector arrays.

There are a number of approaches we have available for wafer-scale integration. We can turn to direct placement die-to-wafer bonding, as well as a direct bond interconnect wafer-to-wafer integration. Both allow us to leverage copper pillar and planar copper-to-copper interconnects, options that outperform indium bumps in terms of energy consumption, bandwidth, and pixel size. Our expectation is that wafer-scale integration will ultimately increase performance while enabling scaling and cost reduction.

The key point to take away is that our InGaAs SWIR photodetector sensors, produced using large-diameter wafers, enable scaling and cost reduction without sacrificing performance. This will help us to address the demand for high-performance SWIR sensors in many markets, including mobile phones, AR/VR, autonomous driving, smart watches, defence and aerospace, industrial automation and machine vision.

But that's just the start. Our large-scale compound semiconductor platform can also be a game-changer in AI, quantum computing and 5G/6G wireless. How? By enabling quantum-dot lasers for communication and sensing; nonlinear materials integration for quantum communication and frequency conversion; and high sensitivity detection for energy applications.

In short, as well as promising to enhance existing system performance, our technology has the potential to generate new markets not previously envisioned, due to scaling and performance limitations that we now seek to overcome.

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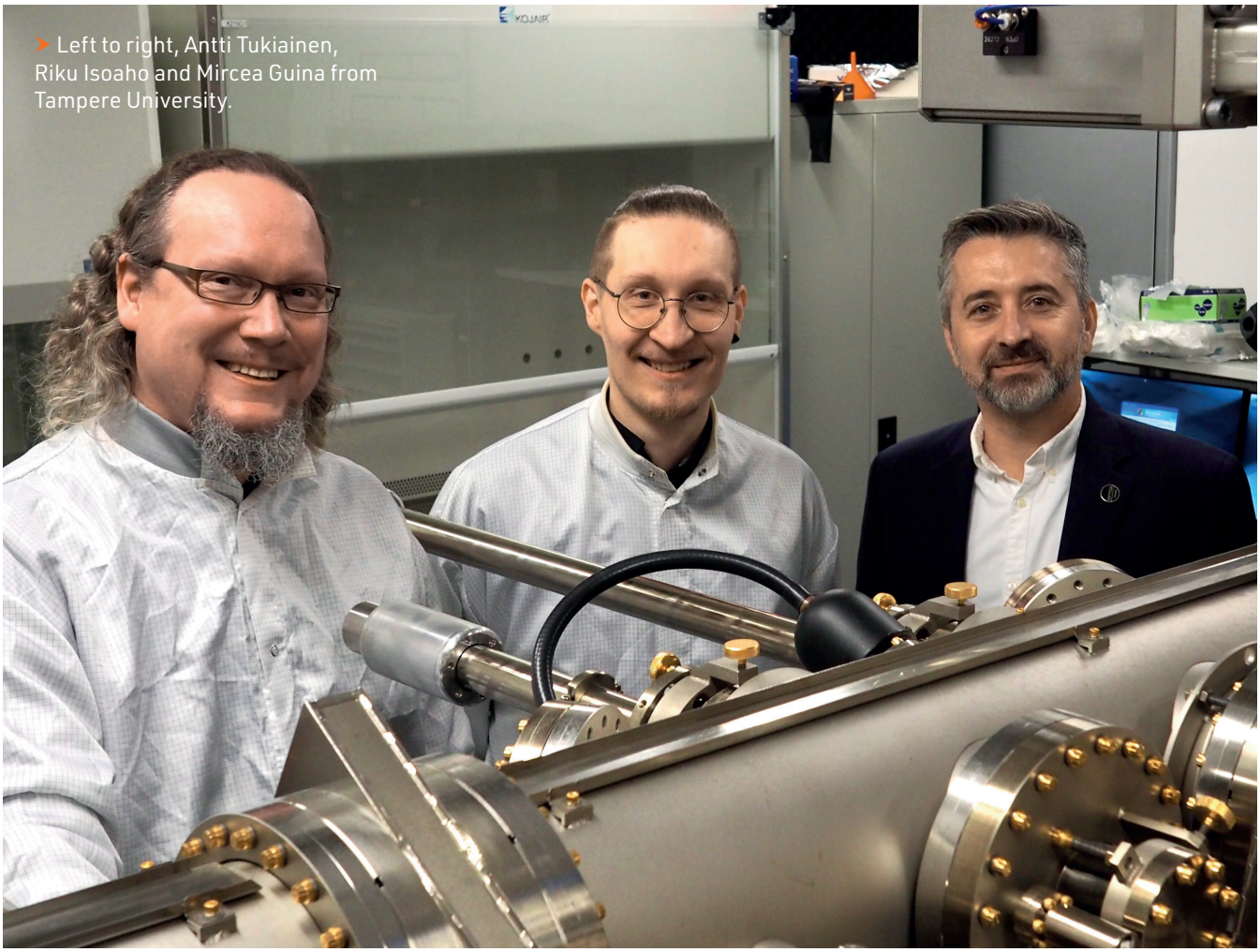


Left to right, Antti Tukiainen, Riku Isoaho and Mircea Guina from Tampere University.

Multi-junction solar cells: **The hunt for 50 percent**

Lattice-matched solar cells with five or six junctions look to surpass the landmark conversion efficiency of 50 percent

BY MIRCEA GUINA, RIKU ISOAHO, ARTO AHO AND ANTTI TUKIAINEN FROM TAMPERE UNIVERSITY

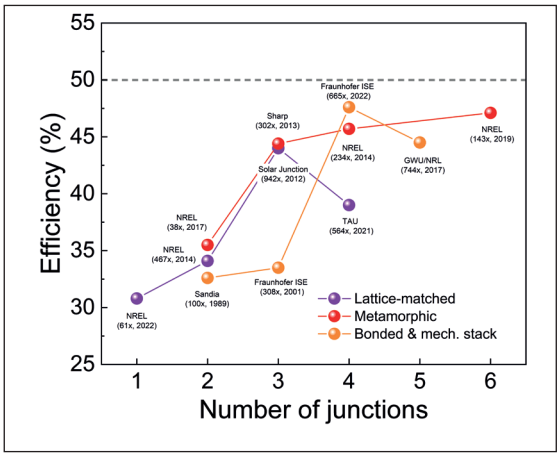
WHEN IT COMES TO photovoltaic conversion efficiencies, III–V multi-junction solar cells are the gold standard. For the past three decades this class of compound semiconductor devices has been breaking record efficiencies and pushing the limits of photovoltaic technologies.

There are opportunities for these multi-junction cells on earth and up in space. Their combination of high efficiencies, high power-to-weight ratios and excellent durability has ensured that these devices are the key technology for power generation in space. Meanwhile, in terrestrial applications, these cells can be deployed in concentrated photovoltaic systems, where focusing sunlight onto the solar cells by lenses or mirrors leads to even higher efficiencies.

Operation under very high levels of concentration, typically many hundreds of suns, is behind record results for efficiency. The current world record stands at 47.6 percent, realised by researchers at Fraunhofer ISE in 2022 with a wafer-bonded

four-junction photovoltaic cell operating at a concentration of 665 suns. That's tantalisingly close to the 50 percent efficiency milestone, which yet remains elusive, despite extensive efforts.

During the last decade or so, realising record efficiencies with multi-junction devices has involved at least four junctions. Now the focus is shifting to five or more junctions, a move that's considered essential for realising practical candidates that will eclipse the 50 percent target (see Figure 1).



➤ Figure 1. Conversion efficiencies for practical devices.

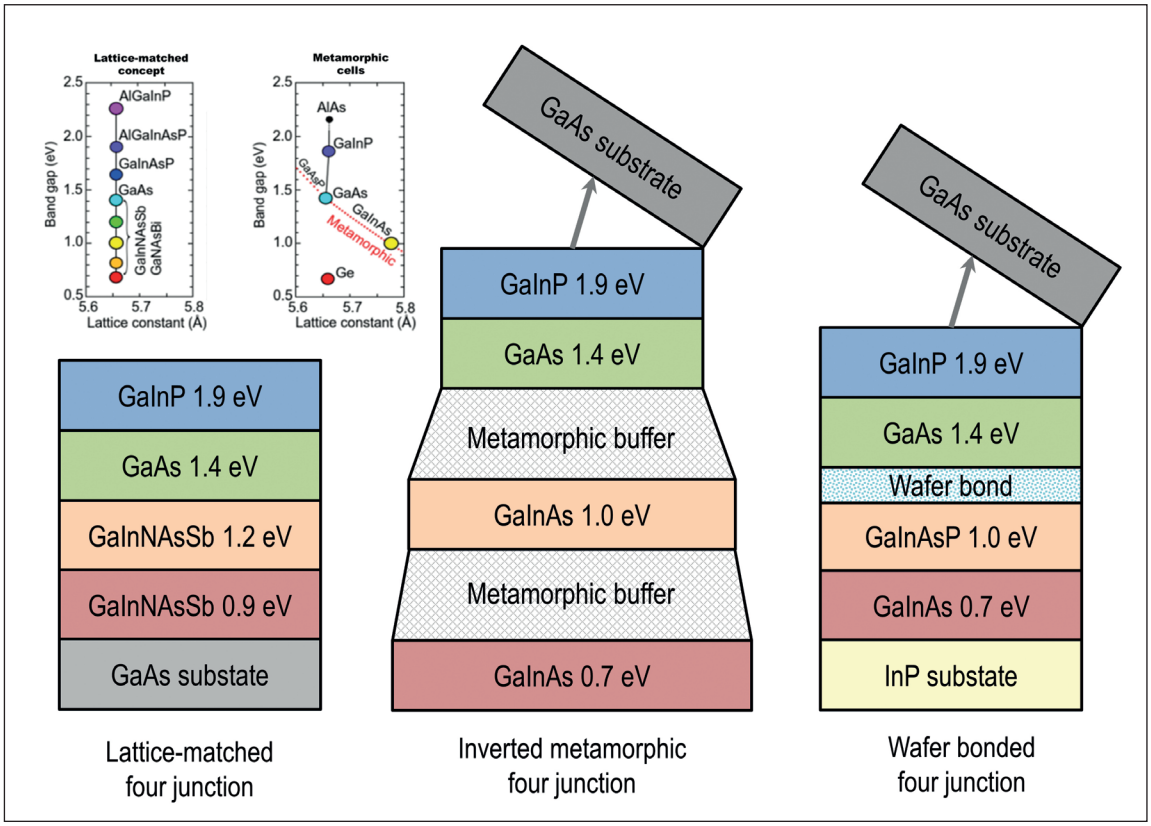
Unlocking higher efficiencies

Multi-junction solar cells excel in efficiency by dividing the incident solar spectrum between multiple subcells, each absorbing photons at different wavelength ranges. It is the distribution of the incident sunlight spectrum that ensures that radiation is utilised more efficiently, and in turn boosts the overall efficiency of the device.

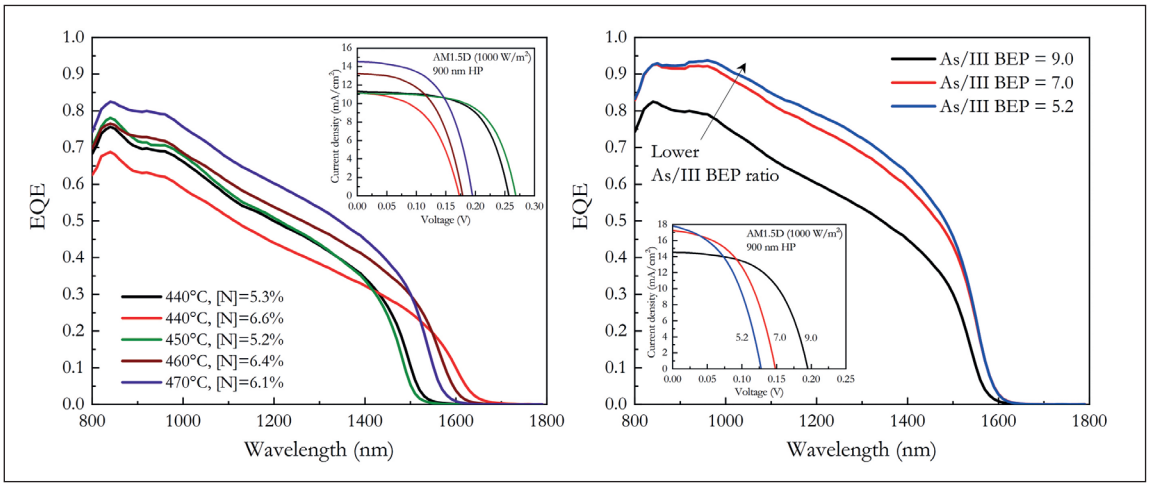
In principle, the greater the number of subcells, the higher the maximum efficiency. For a purely hypothetical multi-junction solar cell that's equipped with an infinite number of junctions, the maximum efficiency is 68.7 percent. That figure is calculated for illumination under one sun, with the theoretical maximum of this hypothetical device rising to 86.8 percent under concentration. For a two-junction solar cell the theoretical efficiency under concentration is as high as 50 percent, but it's likely five or more junctions are needed to reach this value with a practical device.

There are a variety of approaches and materials that can be utilised for realising multi-junction solar cells (see Figure 2). The most widely adopted are stacked architectures based on III–V compounds. III–Vs are a prime choice because of their wide range of tunability, in terms of bandgap energies and lattice constants, assets that enable the monolithic stacking of multiple subcells from different III–V materials.

An elegant approach for monolithic integration is the lattice-matched architecture. Initially developed to outperform single-junction GaAs solar cells, this type of III-V tandem solar cell is formed by stacking a lattice-matched subcell, typically made from AlGaAs or GaInP, on top of a GaAs subcell. It's possible to enjoy higher efficiency by increasing the number of active junctions, a move that's led to the development of lattice-matched triple-junction cells that are grown on germanium substrates.



➤ Figure 2. Different approaches for the fabrication of multi-junction solar cells.



➤ Figure 3. Improvement of external quantum efficiencies for narrow gap GaInNAsSb subcells with optimisation of growth temperature and arsenic overpressure. Insets: Current-voltage curves measured for the GaInNAsSb solar cells under 900 nm high-pass filtered AM1.5D (1000 W m^{-2}) illumination.

Note that germanium has a dual role – as well as providing a foundation for the growth of III–V cells, it is utilised as an active bottom subcell. Adopting this approach, Spectrolab raised the bar for efficiency to 41.6 percent under concentration in 2009. This triple-junction design is currently the staple of the space industry, providing over 30 percent conversion efficiencies in space applications, where concentration of sunlight is impractical.

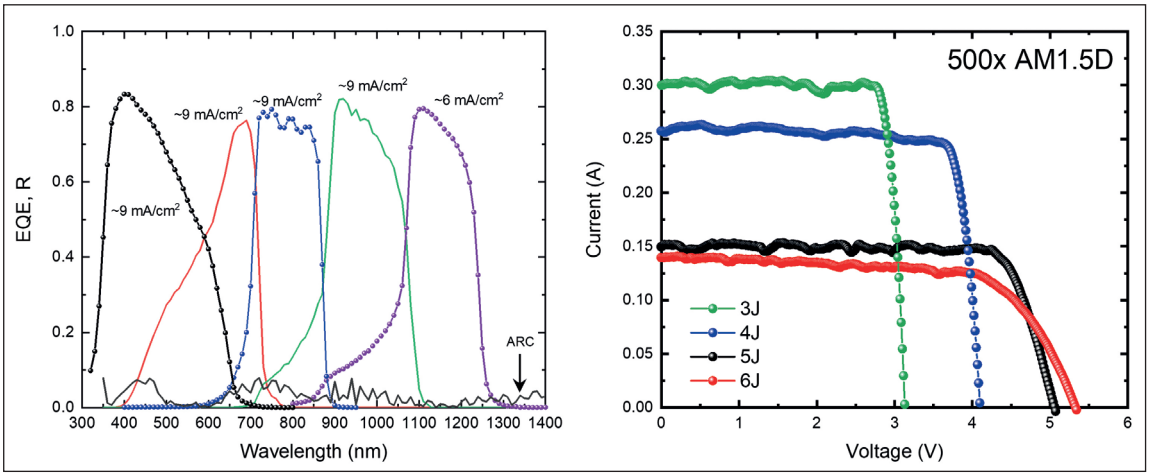
Unfortunately, the triple-junction architecture with lattice-matched designs is not an ideal platform for increasing efficiency through the addition of extra junctions. It's downside stems from the rather limited availability of traditional III–Vs with suitable bandgaps that can be lattice-matched to GaAs or germanium substrates.

Addressing this weakness requires the development of novel lattice-matched subcell materials. In this regard, one highly promising material system is the dilute nitrides, which can be lattice-matched to GaAs and germanium while offering a bandgap as low as 0.7 eV. Another alternative is to fabricate lattice-matched multi-junction devices on an InP platform; however, the scarcity of suitable high-bandgap materials and the relatively high cost of InP have hindered progress with this approach.

To overcome the limitations associated with lattice-matched materials, some pioneers of III–V multi-junction solar cells have turned to metamorphic designs. This approach relaxes the strict lattice-matching requirements between subcells, opening the door to a far broader selection of materials and optimised bandgap energies, key to improving performance.

However, there are prices to pay for switching to lattice-mismatched materials. There is the threat of compromised crystalline quality and an increase in device thickness. That's not to say that metamorphic multi-junction architectures cannot triumph – they have achieved notable success, with record efficiencies. Notably, in 2019, the National Renewable Energy Laboratory broke the efficiency record for all photovoltaics, with an inverted metamorphic six-junction solar cell delivering an efficiency under concentration of 47.1 percent.

Since then, the record has changed hands and now resides with Fraunhofer ISE. In May 2022 they



➤ Figure 4. Left: External quantum efficiencies for subcells in a prototype GaInP/GaAs/AlGaAs/GaInNAsSb/GaInNAsSb five-junction cell. Right: Current-voltage curves measured for lattice-matched devices under 500 suns concentration.

reported a four-junction solar cell formed with wafer-bonding technology that delivers an efficiency of 47.6 percent. To claim the record, these researchers grew subcells on multiple substrates, before fusing them together to create a two-terminal multi-junction solar cell.

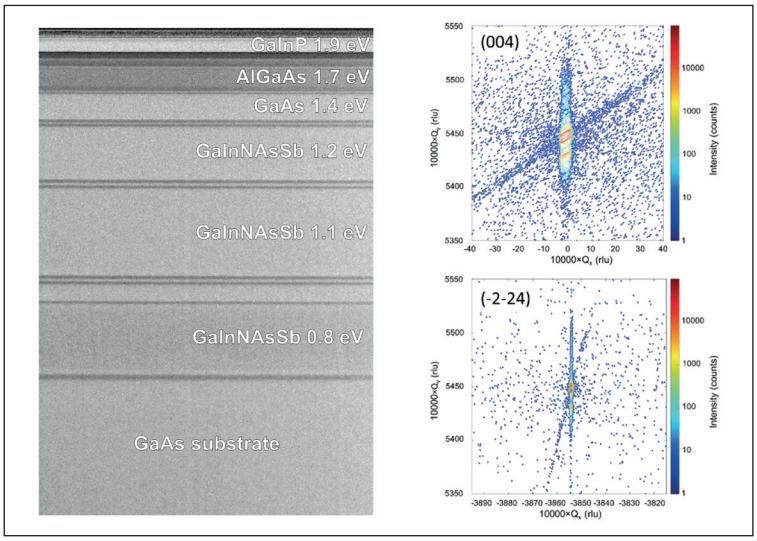
It is also possible to mechanically stack subcells without electrical interconnections in a four-terminal configuration. However, while both this approach and wafer-bonding enable high efficiencies, they are more complex and costly than monolithic integration.

With the 50 percent efficiency target now tantalisingly close, the future of advanced multi-junction solar cells with five or more junctions is highly promising. But what technology will get us over the line? While the inverted metamorphic and wafer-bonded approaches have undoubtedly set high standards for ultra-high conversion efficiencies, it is the lattice-matched approach, bolstered by recent material advancements, that is emerging as a very compelling candidate in the race to reaching the milestone of 50 percent efficiency.

Advantages of lattice matching

The lattice-matched multi-junction architecture offers several advantages over competing technologies, most notably in practicality and cost-effectiveness. Lattice-matching minimises semiconductor material, thanks in part to the absence of thick metamorphic buffer layers. What's more, there's no need for a complex substrate removal process, an essential step in the production of inverted metamorphic cells. It's also worth noting that lattice-matched designs can use identical or similar tunnel junctions between all subcells, further streamlining the design. And last but by no means least, when compared with wafer-bonded and mechanically stacked multi-junction cells, the monolithic lattice-matched approach is simpler and more cost-efficient, as it avoids handling multiple substrates.

In addition to all these strengths, the lattice-matched architecture enhances functionality, particularly for space solar cells. Although lattice-matched designs have been primarily developed on GaAs substrates, it is rather easy to transfer them to germanium substrates, allowing this technology to be applied to germanium-based multi-junction systems standardly used for space applications. In addition, these cells are well-suited for thin-film processing, thanks to reduced internal strain. This functionality enables the fabrication of flexible, lightweight photovoltaic systems with superior power-to-weight ratios, traits highly appreciated by the space industry.



➤ Figure 5. Cross-sectional scanning electron microscope image (left) and reciprocal space maps (right) for a prototype lattice-matched six-junction solar cell produce at Tampere University.

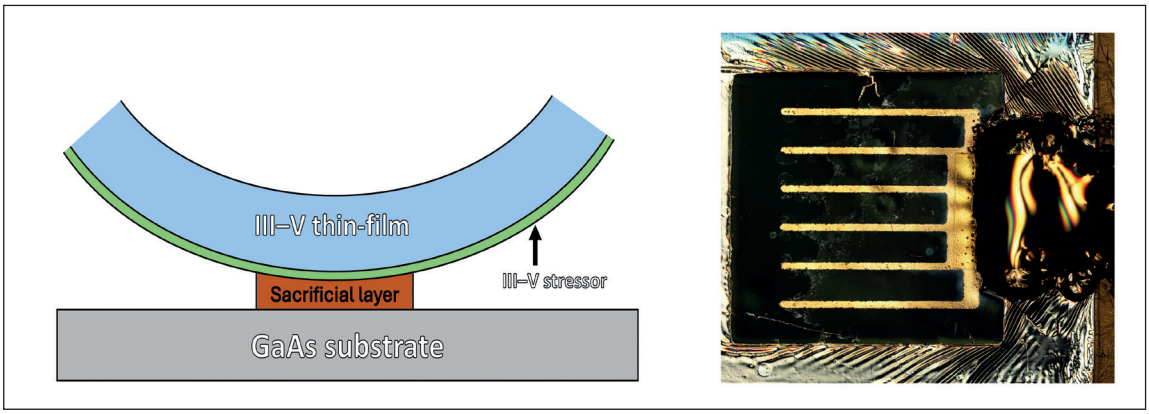
The draw of dilute nitrides

For lattice-matched multi-junction cells on GaAs or germanium substrates, there's a very limited choice of suitable binary or ternary III–Vs with direct bandgaps. Options are limited to just GaInP, AlGaAs, and Ga(In)As. In essence, this constrains lattice-matched architectures only to the established GaInP/GaInAs/germanium triple-junction designs.

Fortunately, the palette has expanded through developments in novel III–Vs, particularly dilute nitrides. This is a game-changer, giving rise to the opportunity to introduce more diverse multi-junction designs with more junctions.

For those not familiar with dilute nitrides, they are III–V compounds with small amounts of nitrogen incorporated into their lattice, a relatively small modification that significantly alters their material properties. What makes dilute nitrides, such as GaInNAs(Sb) alloys, attractive for solar cells applications is that as they can be grown lattice-matched on GaAs or germanium substrates with bandgaps ranging from 1.4 eV down to 0.7 eV. This wide range of bandgaps, realised while maintaining

The lattice-matched multi-junction architecture offers several advantages over competing technologies, most notably in practicality and cost-effectiveness. Lattice-matching minimises semiconductor material, thanks in part to the absence of thick metamorphic buffer layers



➤ Figure 6. Illustration of the epitaxial lift-off (ELO) process for a structure with an internal stressor layer (left), and a picture of an experimental self-peeling GaAs solar cell with inkjet printed polymer used for making the contacts (right, credit: Prabudeva Ramu).

lattice matching, enables the design of lattice-matched multi-junction cells with better subcell combinations.

The introduction of dilute nitrides to the solar community began with their consideration as a replacement for the germanium junction in triple-junction solar cells. In this role, they can reach the ideal bandgap of 1 eV for the bottom cell.

The downside of dilute nitrides is that they are notoriously challenging to synthesize with sufficient quality for solar cell applications. However, much progress has come from growing this material by MBE, rather than MOCVD. Using this form of epitaxy, epitaxy, the first 1 eV GaInNAs(Sb) subcells have been successfully integrated into multi-junction devices. Highlights of such progress include the former record efficiency of 44 percent with a triple-junction cell incorporating a GaInNAs bottom junction, realised by Solar Junction in 2012.

Our team at the Optoelectronics Research Centre (ORC) at Tampere University has also enjoyed success with dilute nitrides. Back in 2015, we fabricated a GaInP/GaAs/GaInNAsSb triple-junction cell by MBE that produced an efficiency of 37 percent under concentration. This has laid the foundation to our exploration of a pathway to the 50 percent milestone.

To expand the possibilities of lattice-matched designs, we started by developing four-junction cells incorporating two GaInNAsSb subcells. For this design we divide the 1 eV dilute nitride subcell from the triple-junction design into a 1.2 eV GaInNAsSb subcell and a bottom GaInNAsSb junction with a reduced bandgap of around 0.9 eV, realised by increasing the nitrogen content from 3 percent to about 4 percent. This led us to report a lattice-matched AlGaAs/GaAs/GaInNAsSb/GaInNAsSb four-junction cell with a 37 percent efficiency under moderate concentration in 2018. Three years later we announced an improved version with a GaInP top junction and enhanced current-matching that produced 39 percent efficiency under concentration. These successes highlight the potential of lattice-matched multi-junction solar cells with dilute nitride materials for reaching ultra-high efficiencies.

While dilute nitrides with bandgaps of around 1 eV have been successfully utilised in multi-junction solar cells, they fail to cover a significant portion of the infrared spectrum, holding back expansion beyond the four-junction design. To overcome this limitation, we have been focusing on developing lattice-matched narrow bandgap GaInNAsSb alloys for next-generation multi-junction cells with five or more junctions. Our goal has been the development of GaInNAsSb alloys with 0.7–0.8 eV bandgaps that bridge the gap between 1 eV dilute nitrides and germanium.

It's far from easy to reach a bandgap of 0.7 eV with dilute nitrides. Nitrogen concentrations have to be pushed to practical limits, creating significant challenges for material quality and epitaxy. But we have made much progress on this front, demonstrating, in 2019, proof-of-concept MBE-grown GaInNAsSb junctions with a bandgap of 0.73 eV and a nitrogen concentration of around 8 percent. These cells maintain crystalline integrity, but high nitrogen levels degrade their optical and electrical properties.

Recently, we have realised more promising results with 0.8 eV GaInNAsSb junctions containing about 6 percent nitrogen (see Figure 3). This slight reduction in nitrogen composition, combined with further optimisation of MBE growth, significantly improves photocurrent from this bottom cell by reducing background doping levels. These optimised 0.8 eV GaInNAsSb junctions are already suitable for integration in multi-junction devices, potentially enabling efficiencies that would break the 50 percent barrier.

Drawing on this success, our next logical step has been the pursuit of lattice-matched multi-junction cell designs incorporating either five or six junctions and leveraging these novel materials. We have already developed prototypes for both cells (see Figures 4 and 5).

Our five-junction variant builds on our the four-junction design, incorporating an additional AlGaAs subcell between the GaInP and GaAs top cells. Early results reveal promising open-circuit voltages exceeding 5 V under concentration, nearly 1 V higher than those of the four-junction cell. However,

the bottom dilute nitride junction limits the current, resulting in a conversion efficiency of approximately 30 percent. Realising the targeted current density of around 9 mA cm^{-2} with further optimisation of this five-junction cell, increasing efficiency to around 45 percent under concentration is not unrealistic.

For our six-junction prototype, we incorporate three dilute nitride subcells, employing the newly developed 0.8 eV GaInNAsSb subcell as the bottom junction. To enhance current-matching between the subcells, we adjust the bandgaps of the two other GaInNAsSb subcells to higher energies than those adopted in the five-junction design, while maintaining the same bandgap configuration for the top three junctions. Although device integration is still in its early stages, experimental results are promising, with open-circuit voltages around 5.5 V under concentration. However, similar to the five-junction prototype, the current-matching target is yet to be realised, limiting the experimental efficiency to approximately 30 percent.

Fulfilling their full potential

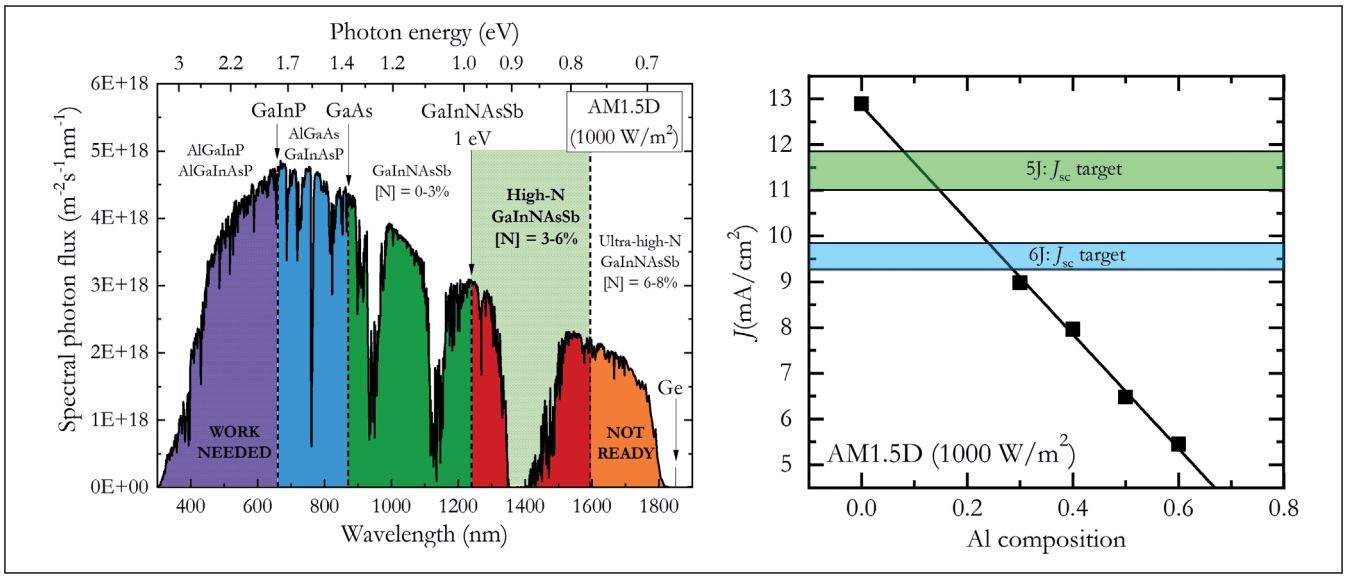
Although our prototype five- and six-junction cells demonstrate the potential of the lattice-matched approach for next-generation multi-junction devices, there is still significant room for optimisation. Most notably, in order to realise the targeted current values, we need to carefully tune subcell bandgaps and thicknesses to optimise current generation. This is far from trivial, because increasing the number of junctions makes current matching increasingly challenging and precise.

Turning to advanced processing techniques helps to further enhance the performance of multi-junction devices. Within this toolkit is the anti-reflective coating, added to minimise reflectance across the entire spectral range of the solar cell. This must be applied with great care, as the design of the coating impacts current balancing between the subcells. Success necessitates meticulous tailoring for optimal device performance. In practice, this tends to involve the application of optimised multilayer coatings with increasing complexity. Our prototype five- and six-junction cells already employ six-layer dielectric anti-reflective coatings. We also have the option of using nanostructured coatings, which provide low reflectance over a wide spectral bandwidth.

To expand the application of multi-junction cells to high-value specialised areas where flexibility is a benefit or even a requirement, these devices can be processed as thin-film structures using epitaxial lift-off (ELO). It is a technique already deployed for the fabrication of thin GaAs-based solar cells with fewer junctions, motivated by the need to increase the power-to-weight ratio in space power systems and unmanned aerial vehicles. Another benefit of ELO is that it enables substrate re-use, thereby providing major benefits in terms of the sustainability of critical materials.

Start-up tf2 devices, a spin-off of Radboud University Nijmegen, has demonstrated the application of ELO to a four-junction photovoltaic cell. However, converting this research result to wide-scale production is yet to take place, much due to the complexity of the process. One issue that has to be tackled is that typical multi-junction solar cells incorporate a high degree of strain, making the lift-off process structure dependent and potentially resulting in structural damage once the thin-film active device is removed from the substrate.

Benefiting from the lattice-matching of our structures, we are advocating a new method that ensures higher controllability of film curvature, realised through controlling the strain within the



➤ Figure 7. Left: Materials and material systems suitable for lattice-matched multi-junction solar cells on GaAs and germanium. Right: Current densities of experimental AlGaInP solar cells grown at Tampere compared to the current density targets of five and six junction cells.

structure. A key element in our process is the use of an InGaAs/GaAs stressor layer, grown beneath the solar cell, that helps control the extent of the strain required to roll-out the thin film (see Figure 6). An external polymer stressor layer can be added to enhance control over lift-off.

We have already demonstrated our ELO technique for a single-junction GaAs cell, and we are now working on extending the process for multi-junction structures. They have an increased thickness, and precise strain management is required across different subcells to ensure a controlled self-rollup. Another of our goals is to develop methods for fabricating electrical contacts for thin-film solar cells utilising inkjet-printed polymers. An alternative to wire bonding, our printing-based approach promises to improve the handling of thin-film structures and boost cell performance, while potentially trimming manufacturing costs.

The thin-film configuration also offers another advantage: it enables the fabrication of back reflectors, enhancing the current generation and radiation resistance of space solar cells. Our lattice-matched six-junction design would greatly benefit from a back reflector, as it's addition could enhance current generation in the novel narrow-gap GaInNAsSb bottom junction. We have extensively developed back reflectors for III–V solar cells, with both planar and textured structures applied to dilute nitride and quantum-dot solar cells.

To produce lattice-matched multi-junction designs with a higher number of junctions that incorporate better bandgap configurations, there is a need for III–V subcells with bandgap energies exceeding 2 eV. Two suitable candidates are AlGaInP and AlGaInAsP. However, it is a challenge to fabricate high-performance subcells with these compounds, due to issues related to impurities, doping, and carrier mobilities. The well-established path to realising higher bandgap energies is to introduce higher aluminium compositions, but that exacerbates these issues.

Taking on these challenges, a team from NREL has successfully utilised a 2.1 eV AlGaInP layer in its metamorphic six-junction cell. However, the addition of this higher bandgap layer increases series resistance. Our preliminary AlGaInP junctions show similar limitations, but we estimate that AlGaInP junctions with aluminium concentrations of between 10 percent and 26 percent could potentially realise current-matching in lattice-matched five- or six-junction designs, provided that further research addresses the challenges with high series resistances, improving their performance under high concentrations (see Figure 7).

Such success would be another step on the way to breaking the 50 percent barrier. It's a goal that's tough, but far from impossible.

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ANGEL EVENTS

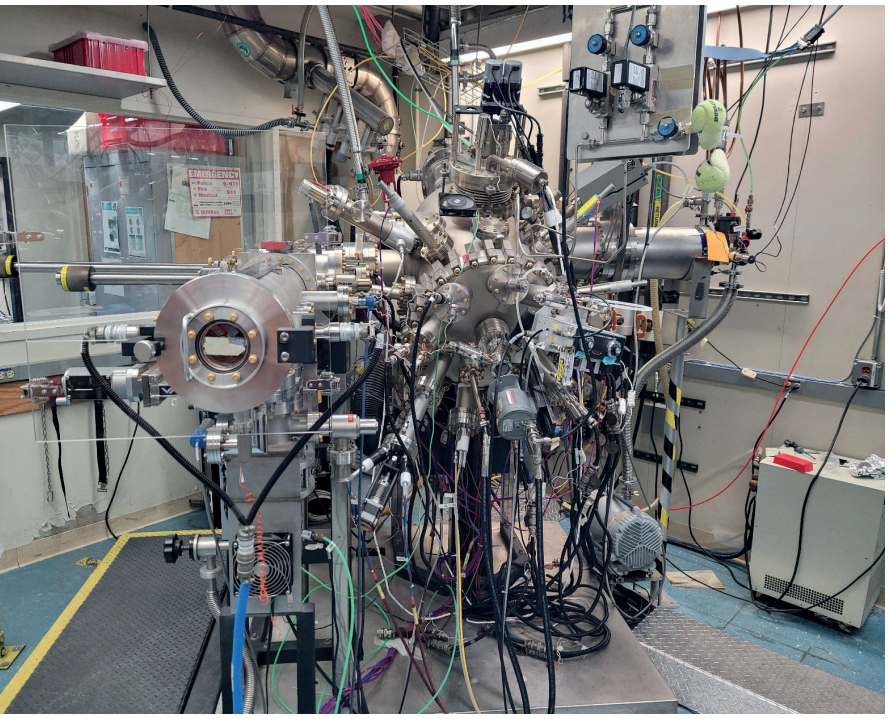
Advancing GaN power devices with **ammonia MBE**

Operating in the kilovolt regime, GaN vertical *p*-*n* high-power diodes produced by ammonia MBE combine a fast growth rate with an ultra-clean thick drift layer and a smooth surface morphology

BY ESMAT FARZANA,* JIANFENG WANG, KAI SHEK QWAH, ASHLEY WISSEL-GARCIA, KELSEY JORGENSEN, TAKEKI ITOH, ZACHARY BIEGLER, MORTEZA MONAVARIAN AND JAMES SPECK FROM THE UNIVERSITY OF CALIFORNIA, SANTA BARBARA

THE LAST FEW YEARS have seen a surge in demand for efficient power devices. It's a ramp that's been spurred on by the rise of a number of next-generation technologies, including fast chargers, data centres, smart grids, high-speed telecommunication, and electric transportation.

For these high-power switching applications, today's silicon-based technology is not up to the task, with concerns surrounding its poor efficiency, excessive voltage levels, bulky system volume, extensive heating, and power loss. This has driven interest in alternatives based on newer materials systems, such as wide bandgap semiconductors, which are attracting much attention thanks to their capability to enhance power-handling while shrinking system size. Amongst these promising candidates GaN has much appeal, thanks to its excellent combination of a high material breakdown field of around 3.3 MV cm^{-1}, a high mobility, good thermal conductivity, and the availability of both *p*-type and *n*-type material.



➤ The Nitride 930 MBE growth system used for ammonia MBE growth at UCSB.

With such attractive properties, it's of little surprise that GaN has already been adopted in a wide variety of commercial electronics, including RF transistors, power amplifiers, and LEDs. However, for the case of power electronics, commercial GaN devices tend to be limited to 650 V, typically employing lateral topologies.

Switching to a vertical device geometry enables an increase in the operating range beyond 650 V, thanks to a superior electric field confinement and enhanced current capability, supported by a large-area backside contact. However, to enter the multi-kilovolt range, these vertical power devices need to have thick GaN drift layers with very low and well-controlled doping alongside minimal compensation.

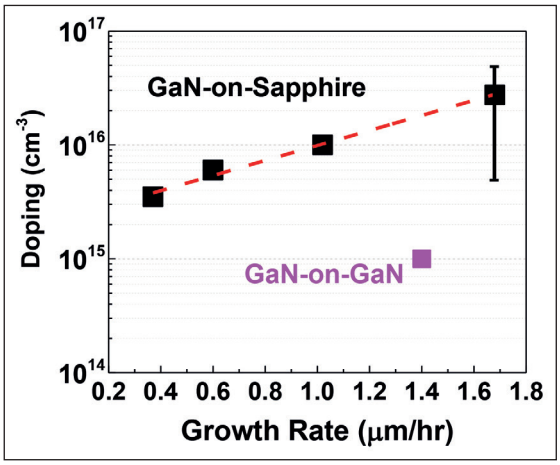
Historically, it has been difficult to address these challenges, due to a lack of freestanding high-quality native substrates. This limitation explains why much of the development of conventional GaN devices has taken place on foreign substrates, such as sapphire and silicon. One downside of these heteroepitaxial growth platforms is that they lead to a high dislocation-density in the epilayers – it is about 10^8 cm^{-2}. Such a high dislocation density may still be tolerable in lateral RF transistors, because dislocations remain perpendicular to the lateral channel. However, that's not the case in vertical devices, where the threading dislocation core directly appears along the vertical channel. For these devices, dislocations severely degrade device performance, creating a high leakage, reducing breakdown voltage, and impairing current transport.

In recent years this state-of-affairs has shifted, due to rapid advances in freestanding GaN substrates, which have significantly lower dislocation densities, ranging from 10^4 cm^{-2} to 10^6 cm^{-2}. These far lower dislocation densities are opening new doors and starting to redefine the landscape of GaN power devices. Within the GaN community, efforts are now being directed at the development of efficient strategies for growing thick epitaxial layers with low impurities that will ensure the desired high-voltage rating with vertical device structures. However, growing thick epilayers is challenging. It demands fast growth rates, comparable or more than 1 µm hr^{-1}, to ensure timely growth, a requirement that leads to increases in impurity concentration and surface roughness.

A significant research effort over many years has involved improving the quality of thick GaN epilayers on native substrates. However, these reports tend to focus on MOCVD-growth of GaN. It's an epitaxial technology that offers a fast growth rate, but due to the use of a chemical-vapour-based synthesis process involving precursors, such as trimethylgallium, it often introduces a high concentration of carbon and hydrogen impurities in the GaN epilayer. These impurities are a menace, dragging down doping efficiency in GaN, due to a combination of donor compensation effects by carbon, and magnesium acceptor passivation effects by hydrogen. Due to these issues, it is far from easy to realise controllable doping over a wide range in *n*-type and *p*-type GaN with conventional MOCVD.

Ammonia MBE for thick GaN

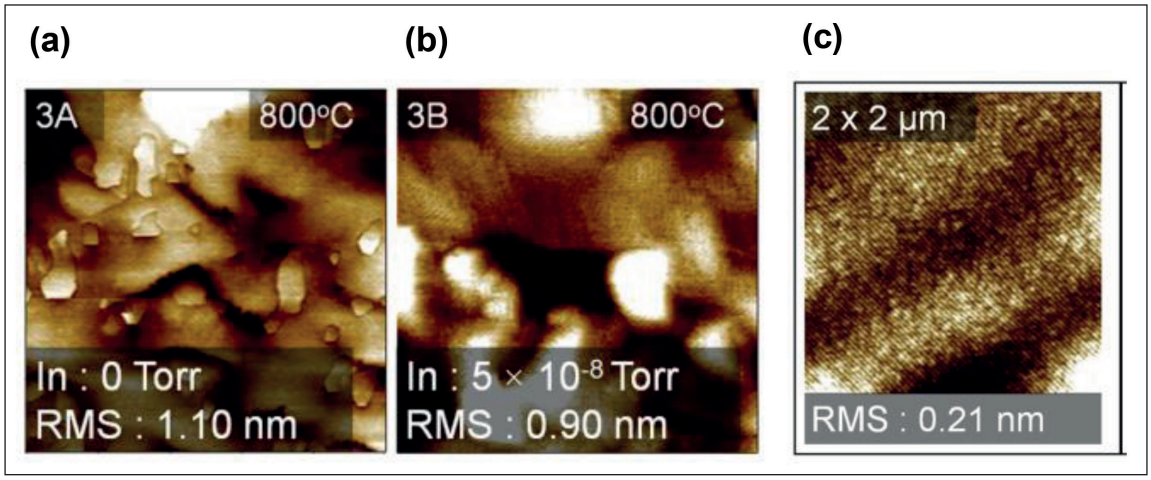
To overcome these challenges, our team that is based at the University of California, Santa Barabara (note that some of us have recently moved on, taking up academic positions elsewhere) have developed an alternative approach to growing thick GaN epilayers that employs ammonia MBE.



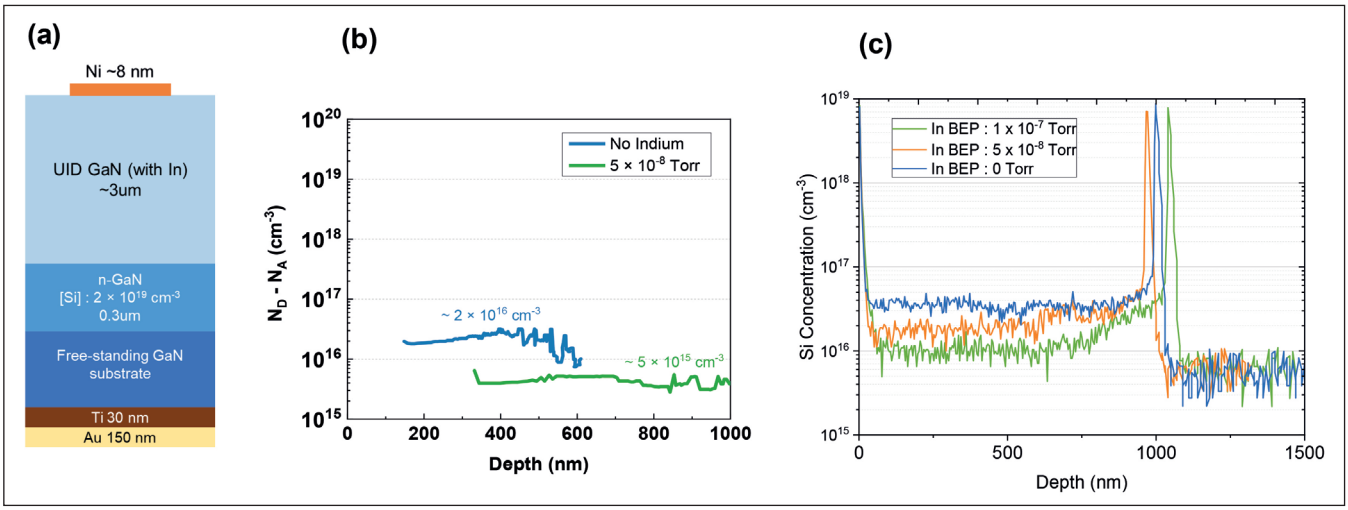
➤ Figure 1. Unintentional background doping in ammonia MBE GaN epilayers as a function of growth rate. The GaN-on-GaN epilayers provided the lowest doping compared with the GaN-on-sapphire ones. For more details, see APL Materials **9** 081118 (2021).

Compared with MOCVD, all forms of MBE offer four key advantages: a clean growth environment in an ultra-high vacuum, which allows the formation of high-purity GaN layers with a background doping as low as 10^{15} cm^{-3}, as well as minimal compensating impurities, such as carbon and hydrogen; a controlled doping profile over a wide range of concentrations, spanning the mid 10^{15} cm^{-3} to 10^{20} cm^{-3}, thanks to minimal compensating impurities; fully activated as-grown *p*-GaN, due to an absence of hydrogen passivation effects; and the opportunity to form an abrupt p^+-*n* junction, due to absence of the magnesium memory effect, a well-known challenge in MOCVD GaN growth.

Within the family of MBE, ammonia MBE offers additional advantages over its plasma-enhanced MBE counterpart. The latter utilises gallium-rich



➤ Figure 2. Atomic force microscopy scans of 2 µm by 2 µm area for unintentionally doped ammonia MBE GaN epilayers (a) on GaN-on-sapphire template using an indium flux beam-equivalent pressures of 0 Torr (b) on GaN-on-sapphire template using an indium flux 5 × 10^{-8} Torr (c) on a Mitsubishi Chemical Corporation free-standing GaN substrate using indium flux beam-equivalent pressures of 5 × 10^{-8} Torr. Homoepitaxial GaN growth on a free-standing GaN substrate shows the smoothest surface morphology with very low root-mean-square roughness of 0.21 nm. For more details, see APL Materials **10** 081107 (2022).



➤ Figure 3. (a) An ammonia MBE GaN-on-GaN vertical Schottky diode with epilayers grown with an indium surfactant using an indium flux beam-equivalent pressure of 5×10^{-8} Torr. (b) Lower background unintentional doping achieved by using indium as surfactant. (c) Lower background doping was consistent with silicon secondary ion mass spectrometry impurity profiles in the GaN epilayer with an increased indium flux beam-equivalent pressure. For more details, see APL Materials **10** 081107 (2022).

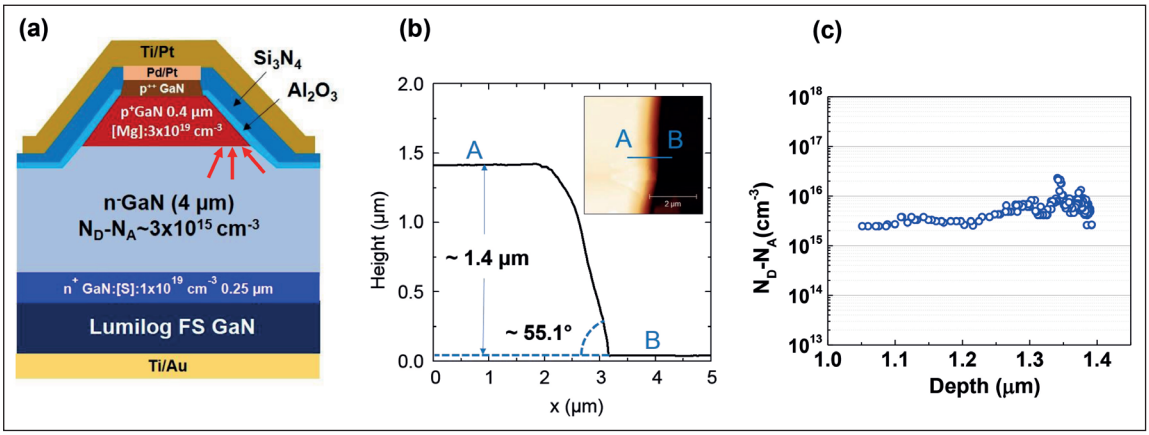
growth conditions, while ammonia MBE allows the growth of GaN deep within the nitrogen-rich region. Due to this, ammonia MBE eliminates gallium droplets, a problem that plagues plasma-enhanced MBE and causes a poor surface morphology.

In recent years, part of our focus has been directed at advancing ammonia MBE growth for the development of high-voltage vertical GaN power switches. Through our pursuit of a synergistic effort that extends from ammonia MBE growth optimisation to device development, we have been able to demonstrate kilovolt-range vertical GaN-on-GaN *p-n* diodes.

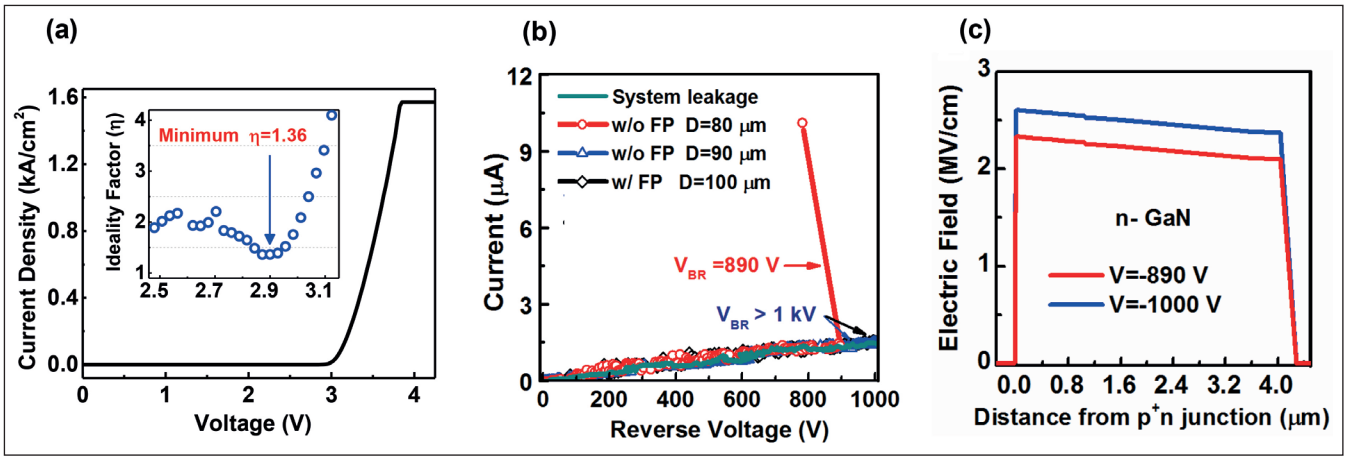
Optimising growth

These efforts began by optimising the growth conditions for ammonia MBE to enable a thick drift layer with a low level of unintentional doping, realised with a reasonably high growth rate. To uncover conditions for this, we carried out a systematic study with a Veeco 930 reactor using sapphire and free-standing GaN substrates and growth rates from 0.37 μm hr^{-1} to 1.68 μm hr^{-1}. After growing our epiwafers, we processed them into diodes to extract a net background doping, using 1 MHz capacitance-voltage measurements.

From this study, we determined a monotonic increase in background doping in the unintentional doped GaN from 3.5×10^{15} cm^{-3} to 6×10^{15} cm^{-3} and then 1×10^{16} cm^{-3}, for increases in growth rate from 0.37 μm hr^{-1} to 0.6 μm hr^{-1} and then 1 μm hr^{-1}. Switching to a free-standing GaN substrate slashed the background doping, with a value of around 10^{15} cm^{-3} recorded for a growth rate 1.4 μm hr^{-1} (see



➤ Figure 4. (a) Schematic of the fabricated ammonia MBE GaN vertical GaN-on-GaN p^+-*n* diode. (b) Atomic force microscopy image of the sidewall field plate analysis. The profile along cutline AB shows a step height of 1.4 μm and a sidewall angle of about 55°. (c) 1 MHz capacitance-voltage extracted an unintentional doping of 3×10^{15} cm^{-3} in the drift layer of the ammonia MBE GaN *p-n* diode. For more details, see IEEE Electron. Device Lett **41** 1806 (2020).



➤ Figure 5. (a) Forward current density-voltage characteristics of the ammonia MBE GaN vertical GaN-on-GaN *p-n* diode showing excellent transport behaviour with a minimum ideality factor 1.36 (inset). (b) Reverse breakdown characteristics for the ammonia MBE GaN *p-n* diodes showing that the best diodes did not show breakdown up to -1000 V (equipment limit). The leakage current of the diodes is obscured by the system leakage (c) Simulated electric field profile using TCAD that shows a punch-through electric field profile where the peak field appears at the abrupt junction interface at 0 μm with 2.6 MV cm^{-1} at 1000 V. For more details, see IEEE Electron. Device Lett **41** 1806 (2020).

Figure 1). We attribute this marked improvement to a reduced incorporation of dislocation defects, which other groups have attributed to behaving as gettering centres of donor-like oxygen impurities. Our unintentional doping level of around 10^{15} cm^{-3} is one of the lowest values reported in GaN epilayers, and about an order of magnitude lower than that for GaN grown by MOCVD.

Optimisation of the growth conditions has included improving surface smoothness. This is challenging at fast growth rates, which increase the likelihood of forming morphological and native defects, and incorporating unintentional impurities, including shallow dopants and compensating acceptors. For the growth of III-nitrides, surfactants are often used to reduce the surface roughness, with their introduction assisting adatom mobility and thus reducing native defect formation and improving morphology. It's also possible that surfactants reduce unintentional impurity incorporation.

To realise a smooth surface morphology, while adopting a fast growth rate of around 1 μm hr^{-1}, we have turned to indium as a surfactant for thick GaN epilayer growth. It's reported that the introduction of indium reduces the diffusion barrier for gallium and nitrogen adatoms to just 0.12 eV and 0.5 eV – without it, these values are 0.7 eV and 1.3 eV, respectively.

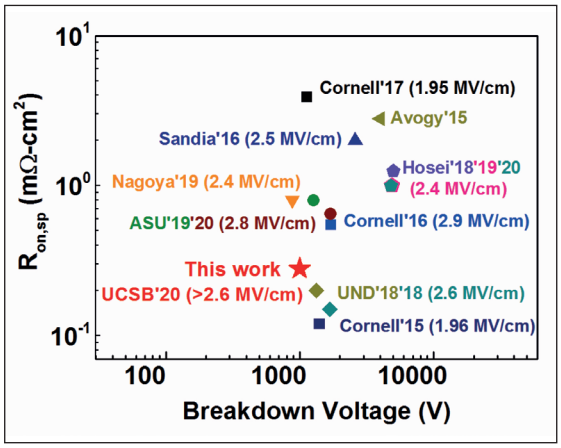
Using indium surfactants with a beam-equivalent pressure of 5×10^{-8} Torr, we have trimmed the root-mean-square surface roughness from 1.1 nm to 0.9 nm with the introduction of indium surfactants, when growing a GaN epilayer on sapphire (see Figure 2). For the same conditions, moving to a free-standing GaN substrate reduces the root-mean-square surface roughness to 0.21 nm. Another benefit of the native substrate is that it reduces the dislocation density, with that produced by Mitsubishi Chemical Corporation providing a reduction by two orders of magnitude, from around 10^8 cm^{-2} to around 10^6 cm^{-2}.

Introducing indium surfactants also improves the background doping concentration, driving it down from 2×10^{16} cm^{-3} to 5×10^{15} cm^{-3}. In addition, there is a lower silicon incorporation when using an indium surfactant, according to secondary ion mass spectrometry (SIMS) (see Figure 3). We think that the probable reason for this is indium bonding at step edges, which prevents silicon impurities from occupying dangling bonds or vacancies in the GaN surface.

Making vertical power devices

Drawing on establishing the conditions for high-quality GaN epilayer growth, we have gone on to use this expertise to produce vertical power devices. This work has taken several directions: the fabrication of vertical p^+-*n* GaN diodes with a kilovolt-range breakdown performance that use a punch-through field profile to fully utilise the low doped drift layer; the use of efficient edge termination to mitigate the high field at the p^+-*n* junction interface; deployment of high-quality contact layers to support a low contact resistance; and the use of optimal fabrication techniques to mitigate process-induced damage.

Working towards these directives, we employed ammonia MBE to grow a p^+-*n* GaN diode on a Lumilog free-standing GaN substrate. This device incorporated an unintentionally doped GaN layer grown at 0.6 μm hr^{-1}, as well as a 400 nm-thick p^+ GaN layer grown at 0.32 μm hr^{-1} and featuring a magnesium doping concentration of 3×10^{19} cm^{-3} to complete the p^+-*n* junction (see Figure 4 (a)). To minimise impurity incorporation from the substrate,



➤ Figure 6. Benchmark plot of the specific on-resistance versus breakdown voltage for the UCSB work and reported vertical homoepitaxy GaN *p-n* diodes from literature. The peak electric field is shown in parenthesis. For more details, see IEEE Electron. Device Lett **41** 1806 (2020)

we grew a buffer under our device that's about 250 nm thick, and silicon-doped at a concentration of 1×10^{19} cm^{-3}. Our epistructure also contained a 10 nm-thick, p^{++} GaN cap layer, with magnesium doping at a concentration of 3×10^{20} cm^{-3}. We produced our full epilayer structure, consisting of p^{++} cap/p^{+} layer/*n*-drift layer/n^{+} buffer, using uninterrupted ammonia MBE growth under a gallium-limited condition.

From this epiwafer we fabricated circular p^{+}-*n* GaN diodes with an 80 μm to 100 μm diameter, a Pd/Pt anode and a backside ohmic Ti/Au cathode. We realised edge termination with a side-wall angle (55°) field-plate (see Figure 4 (b)). By using an angled field plate, rather than a steep vertical field plate (90°), we gradually smoothed the crowded electric field at the p^{+}-*n* junction interface. We obtained this sidewall angle, with an etch depth of around 1.4 μm, using an optimised dry etch with an inductively coupled plasma, followed by a wet etch with potassium hydroxide. The wet etch for 25 minutes also helped minimise dry etch-induced damage. To provide additional passivation of the etched sidewall, we turned to atomic layer deposition, adding a 26 nm-thick layer of Al_2O_3 at 300°C. This oxide layer protected the device layers during subsequent deposition of a Si_3N_4 layer around 205 nm-thick, added by plasma-enhanced CVD. This layer served as the field-plate dielectric.

Electrical measurements on our diodes revealed outstanding characteristics. The extracted doping from 1 MHz capacitance-voltage profiles is 3×10^{15} cm^{-3} (see Figure 4 (c)), in line with the SIMS-detected background silicon concentration, while compensating carbon was below the SIMS detection limit of 10^{16} cm^{-3}, underscoring the purity of the ammonia MBE of GaN.

The high quality of the epilayer ensured excellent forward-transport properties. Under forward bias, our diodes exhibit a minimum ideality factor of just 1.36 – that's among the lowest reported for vertical *p-n* GaN diodes – and a specific on-resistance of only 0.28 mΩ cm^{-2} (see Figure 5 (a)).

Operating under reverse bias, the breakdown voltage exceeds our measurement limit of 1 kV, while diodes without edge termination had a breakdown voltage of 890 V (see Figure 5 (b)). According to Silvaco TCAD simulations, there is a punch-through electric field profile at a reverse bias of 1000 V with a peak electric field of more than 2.6 MV cm^{-1} located at the p^{+}-*n* junction interface (see Figure 5 (c)). It's worth noting that this kilovolt-range performance is realised with a significantly thinner drift layer of around 4 μm – that's less than half the thickness of that required for vertical homoepitaxial GaN *p-n* diodes grown by MOCVD (see Figure 6).

Future directions

By combining efficient field management and low-damage processing techniques, to the best of our knowledge we have broken new ground by demonstrating the first GaN vertical *p-n* high-power diodes grown by ammonia MBE that can operate in the kilovolt range. Key to our success is our combination of the growth of an ultra-clean thick drift layer, a fast growth rate, and a smooth surface morphology.

Building on our success, which has showcased ammonia MBE as a premier growth technique for future GaN high-power devices, we have started to investigate aluminium-rich AlGaN and AlN films on AlN template substrates. These efforts have involved single-composition AlGaN layers as well as graded-composition AlGaN all the way down to GaN. This work is laying the foundation for exploring AlGaN/GaN transistors, AlGaN power diodes, and superjunction devices. All will certainly benefit from the excellent material quality achieved by ammonia MBE.

* The current affiliation for Esmat Farzana is the Department of Electrical and Computer Engineering, Iowa State University

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Double heterostructure HEMTs for handsets

GaN-on-silicon HEMTs with an AlN barrier and an AlGaN back barrier deliver a ground-breaking output power at a battery-compatible voltage

A COLLABORATION of engineers based in Singapore claims to have broken new ground by investigating the potential of a double heterostructure design for low-voltage GaN-on-silicon HEMTs.

These researchers argue that this class of transistor is a compelling candidate for power amplification in the 5G Frequency Range 2 band – this is defined as more than 24 GHz, and features a number of bands more than three times as wide as those found below 6 GHz. As a rule of thumb, the maximum data rate from any band is proportional to its width, making the double-heterostructure HEMT an attractive option for high-speed uplinks and downlinks.

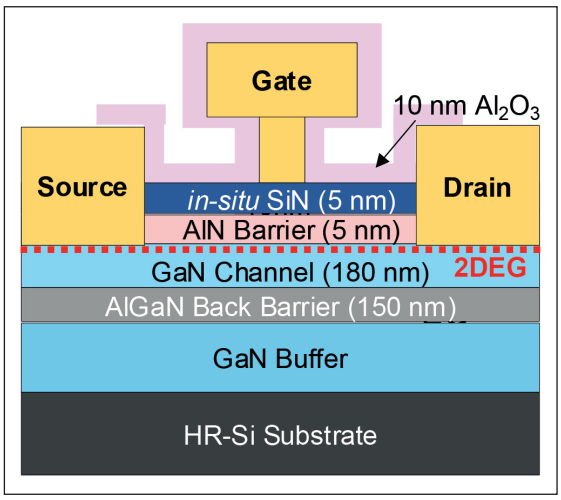
Up until now, efforts at investigating GaN devices operating at low voltages, an essential requirement for deployment in handsets, have been limited single heterostructures. Meanwhile, the development of double-heterostructure devices, which offer excellent carrier confinement and enable a high mobility and a high saturation velocity, has only occurred at higher voltages.

Strengths of the double-heterostructure devices, made by engineers at Nanyang Technical University, A*STAR, the Singapore-MIT Alliance for Research and Technology, and the National University of Singapore, include a record-breaking saturated output power for low-voltage GaN-on-silicon HEMTs operating in the 5G Frequency Range 2 band.

Fabrication of this team's HEMTs began by loading a high-resistivity silicon substrate into an MOCVD chamber and depositing a 1 μm-thick GaN buffer, followed by a 150 nm-thick AlGaN back barrier, a 180 nm-thick GaN channel, a 5 nm-thick top barrier, and a 5 nm-thick SiN_x layer. According to Schrödinger-Poisson calculations by the engineers, this double heterostructure ensures a significantly better carrier confinement than a single heterostructure.

Processing of the epiwafer into devices involved the addition of Ti/Al/Ni/Au ohmic contacts, device isolation by mesa etching, the addition of Ni/Au T-shaped gates, and passivation realised by atomic layer deposition of a 10 nm-thick layer of Al_2O_3.

Measurements on these transistors, which have a gate length of 120 nm, gate-source and gate-drain spacings of 690 nm, and a source-to-drain spacing of 1.5 μm, revealed a maximum drain current of 1.9 A mm^{-1}, an on-resistance of 1.5 Ω mm, and a maximum transconductance of 0.66 S mm^{-1}. The cut-off frequency of the HEMT is 145 GHz, and the maximum oscillation frequency 195 GHz.



➤ GaN-on-silicon HEMTs with a double heterostructure produce 1.3 W mm^{-1} at 30 GHz, when operating at 5 V.

Large-signal performance, evaluated at 30 GHz and 5 V and involving the use of on-wafer load-pull measurements, determined a saturated output power of 1.3 W mm^{-1} (16.12 dBm), with an associated power-added efficiency of 32 percent and a gain of 3.7 dB.

Leader of the team, Geok Ing Ng, told *Compound Semiconductor* that the dimensions of their HEMTs are in the right ball-park for use in handsets."We believe a gate length of 100 nm to 120 nm would satisfy practical millimetre-wave handset applications. This is considering the transistor's short-channel effects, fabrication complexity and yield, among other factors."

However, he says that there are no obstacles to lateral scaling of these transistor, to improve performance at higher frequencies, such as the W-band. "We used the term 'aggressive scaling' to generically refer to lateral scaling. Notably the source-drain spacing – currently 1.5 μm – could be reduced."

One of the team's next goals is to conduct a comprehensive study of low-voltage millimetre-wave GaN-on-silicon HEMTs, considering epitaxy and device design. "Through aggressive lateral scaling of the transistor, we hope to explore the performance limits of GaN-on-silicon HEMTs at higher frequencies, such as the W-band."

Another aim is to go beyond simply focusing on the output power of the HEMT and start looking at other specifications, such as linearity, an important metric for the RF front-end.

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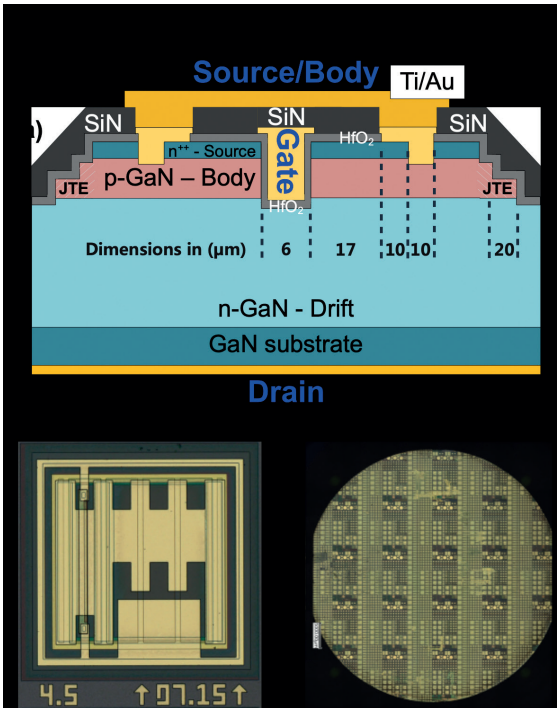
Turbocharging the GaN MOSFET with a HfO_2 gate

Introducing a HfO_2 gate dielectric by atomic layer deposition trims leakage current, boosts breakdown voltage, and cranks up the output power density

RESEARCHERS from Sandia National Laboratories, Albuquerque, have delivered a dramatic improvement in the performance of vertical GaN MOSFETs through the introduction of a HfO_2 gate dielectric.

This team's 1.2 kV MOSFET delivers an output current density of 330 mA mm^{-1} – that's more than ten times that of the highest values reported for 1.2 kV-class GaN and SiC MOSFETs – alongside a leakage current that's just 0.5 nA at 2 MV cm^{-1}, and a breakdown strength of 5.2 MV cm^{-1}.

Team spokesman, Andrew Binder, told *Compound Semiconductor* that for many years it has been assumed that high-κ dielectrics, such as HfO_2, are not suited to wide bandgap semiconductors, due to the low band offset and an associated leakage current.



➤ GaN trench MOSFETs deliver a ten-fold hike in output current density with the introduction of a HfO_2 gate dielectric.

"This work demonstrates that given the right conditions it is possible to get low leakage and good film properties, despite the low band offset," claims Binder, adding: "This also poses an interesting question, if it can be done on GaN, could it be done on SiC?"

Binder and his co-workers believe that the biggest contributor behind the hike in current density is the higher permittivity of the dielectric, which ensures a decrease in channel resistance. "Compared to SiC MOSFETs with an SiO_2 insulator, our HfO_2-gated MOSFET has a factor of five increase in permittivity."

When the impact of a higher permittivity is considered alongside additional factors, such as a higher channel mobility and a channel length that's shorter than SiC D-MOSFETs, one can start to explain the ten-fold hike in current density. This could be a game-changer in the power electronics industry, where there is much demand for 650-1200 V SiC MOSFETs from makers of electric vehicles.

In this voltage class, channel resistance is a significant limitation to device performance, so the substantial reduction realised by the Sandia team could enable a significant competitive advantage for chipmakers that incorporate their technology.

"Another consideration is that a significant reduction in on-resistance means that for the same current rating each die becomes smaller, which means the cost-per-die decreases, as there are now more die per wafer," adds Binder.

He and his co-workers produced their devices by loading an *n*-type free-standing GaN substrate from Mitsubishi Chemical Corporation into an MOCVD reactor and depositing a 12 μm-thick drift layer, followed by a 0.5 μm-thick *p*-body and a 0.25 μm-thick source layer. Etching followed to define the trench, body and junction termination extension. Prior to addition of the gate dielectric, the team prepared the surface with ozone treatment and a piranha clean, and activated dopants via annealing.

The team turned to a Savannah S100 reactor operating at 150 °C to deposit a 100 nm-thick layer of HfO_2, using 960 atomic layer deposition cycles, before adding source, gate and drain contacts.

Electrical measurements on vertical GaN MOSFETs revealed a current density of 330 mA mm^{-1} at a drain bias of 5 V, and a positive threshold bias of 3.5 V. Specific on-resistance is 8 mΩ cm^2, but could fall to just 1.1 mΩ cm^2 by scaling the cell pitch from 70 μm to 10 μm.

Binder and co-worker are keen to explore the possibility of replicating their success with HfO_2 on a SiC transistor. "Vertical gallium nitride is still a relatively immature platform for device development," says Binder, who points to a very mature, established commercialisation path for SiC MOSFETs. "If we can demonstrate HfO_2 on SiC successfully, then we have a quicker path to market than we do with vertical GaN."

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Transforming the current density of AlN Schottky barrier diodes

Introducing a graded layer in AlN Schottky barrier diodes increases their maximum current density by three orders of magnitude

ENGINEERS from North Carolina State University and Adroit Materials have raised the bar for the current density of AlN Schottky barrier diodes by three orders of magnitude.

The team's diodes, capable of operating at a current density of more than 5 kA cm^{-2}, feature a highly doped $Al_{0.75}Ga_{0.25}N$ contact layer and a lightly doped AlN drift layer. It's a combination that can create an electron barrier at this interface – but is avoided by adding a compositionally graded layer, key to enabling a far higher forward current.

By delivering a dramatic increase in the current density of AlN Schottky barrier diodes, the team is helping these devices to fulfil their tremendous promise. This class of diode has the potential to serve in high-voltage, direct-current power transmission and locomotive drive systems, where it could offer a breakdown voltage of more than 10 kV. Note that thanks to a breakdown field that's greater than 16 MV cm^{-1} and a high electron mobility, AlN has a Baliga figure of merit more than 30 times that of GaN or SiC, enabling AlN devices with blocking voltages in the 10 kV range to have drift layers just a few microns thick.

Crucial to the fabrication of a high-performance device is an ohmic contact, realised with a quasi-vertical structure featuring a heavily-doped AlGaN layer as the contact layer.

To assess the impact of the AlN/AlGaN interface on the maximum forward current, the engineers carried out simulations using Silvaco TCAD software.

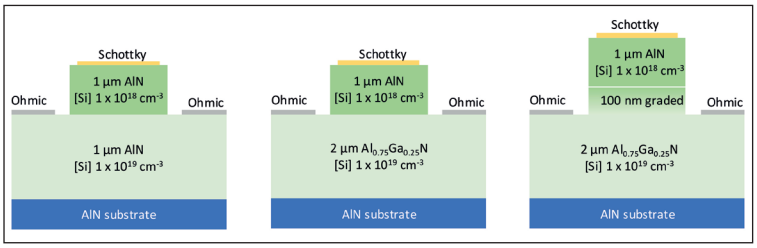
This modelling revealed that when there is an abrupt heterojunction, a sharp discontinuity is present in the band structure that introduces a barrier for electrons flowing from AlGaN to GaN. When operating under forward bias, this electron barrier is reverse biased and acts as a nonlinear series impedance. Inserting the compositionally graded layer eliminates the electron barrier.

Proof of the benefit of introducing the compositionally graded layer is provided by measurements on devices with and without this feature. Three different devices were fabricated: a control with a homoepitaxial AlN contact layer, another with an abrupt heterojunction, and a third with a graded layer heterojunction (see Figure).

All three variants were produced by loading Hexatech single-crystal AlN substrates with an average dislocation density of 10^3 cm^{-2} into an MOCVD chamber. After depositing an AlN-based stack on the substrate, the team processed the resulting epiwafers by photolithography and reactive-ion etching to form circular mesas, with electron-beam evaporation adding ohmic contacts.

Electrical measurements on these devices, which had radii ranging from 25 μm to 300 μm, revealed current scaling with the Schottky contact area for radii up to 50 μm. For radii larger than this, current density decreases with increasing device area.

Plots of room-temperature current-voltage characteristics determined an ideality factor of no more than 1.2, and an on-off ratio in excess of 10^{11}. This led the team to conclude that they had produced high-quality Ohmic contacts.



The team also found that the device with the graded-layer hetero-junction produced a current that's a factor of 10^3 higher than that with the abrupt junction, and 10^4 higher than the control.

AlN-based Schottky diodes with the abrupt and graded hetero-junctions were also investigated with impedance spectroscopy. Plots uncovered a bias-dependent feature in the diode with the abrupt junction that's attributed to the electron barrier. As this bias-dependent feature is not seen in the graded hetero-junction diode, the team concluded that this measurement offers further evidence for the hike in maximum current density stemming from either the reduction or removal of the electron barrier.

Despite the lack of edge termination to aid field management, the breakdown voltage of the diode is as high as 680 V, corresponding to a maximum electric field of 12.3 MV cm^{-1}.

➤ Introducing a graded-layer hetero-junction increases the forward current density of the diode by three or more orders of magnitude.

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