COMPOUND SEMICONDUCTOR

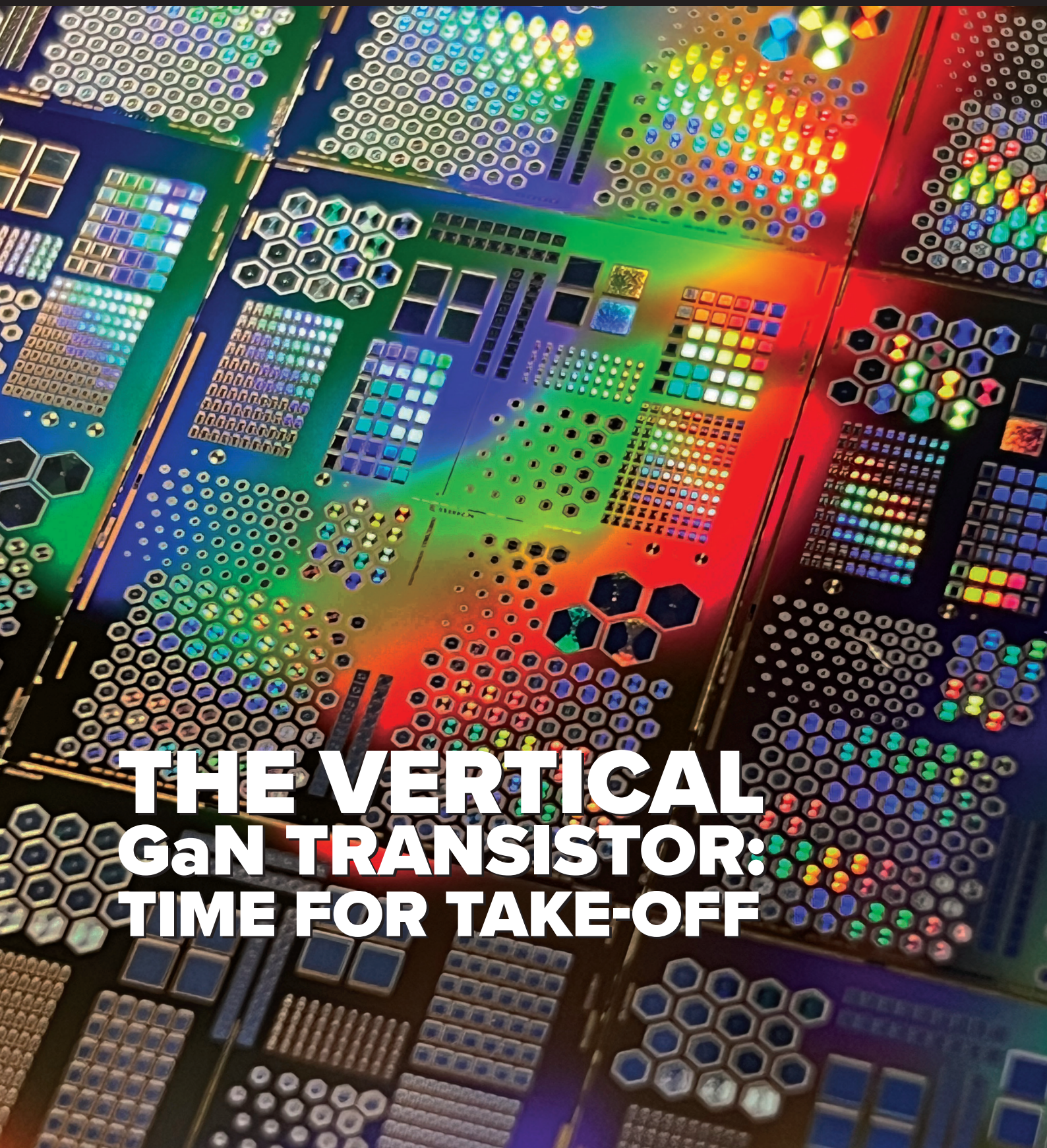
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

30 YEARS ANNIVERSARY

VOLUME 31 ISSUE IX 2025

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

COMPOUNDSEMICONDUCTOR.NET



THE VERTICAL GaN TRANSISTOR: TIME FOR TAKE-OFF

AIXTRON

THE G10 SERIES

G10-SiC

SiC power epi production platform with 150/200 mm wafer size flexibility

Your **Productivity Solution**
for All Advanced Epitaxy Materials

AIXTRON SE - Dornkaulstr. 2 • 52134 Herzogenrath • Germany - Phone: +49 2407 9030 0 - www.aixtron.com

VIEWPOINT

BY RICHARD STEVENSON
EDITOR

GaN: Going in which direction?

IN OUR INDUSTRY, we use a number of figures-of-merit to judge devices. We can benchmark LEDs by their lumens-per-Watt and their lumens-per-dollar, and assess the performance of power devices by Baliga's figure-of-merit: it's calculated by squaring the breakdown voltage and dividing that figure by the specific on-resistance.

As well as these rather precise figures, there's another one that's far more vague – it's the bang-per-buck.

Revolutionary devices often excel in the 'bang'. Think, for example, of the vertical GaN transistor. Compared to its conventional cousin that's netting substantial sales via the fast charging of mobile devices, it offers a higher breakdown voltage for a given chip area, along with superior reliability and simplified thermal management.

But what about the 'per buck'. Well, that's been a major sticking point. Traditionally, vertical GaN transistors have been produced on GaN substrates, a foundation that has many weaknesses. Drawbacks include a high price, limited availability, and relatively small diameters that hamper scaling, an issue that's probably to blame for the death of start-ups that have tried to commercialise this device.

Overcoming this limitation is the MIT spin-out Vertical Semiconductor. This fabless firm is pioneering the use of engineered substrates with a diameter of 200 mm for the production of vertical GaN transistors (see 'p. 14' for more details). By switching to this foundation, Vertical is able to manufacture its power devices in 200 mm foundries that are primarily used to produce silicon devices with CMOS technology.

While the approach is novel, the markets Vertical is targeting are anything but. Yes, you've guessed it – it's EVs and data centres, with the later spurred on by the growth of AI.

Given the tremendous excitement in both those booming markets by many producers of GaN power devices, it would be easy to assume that sales to these sectors are already substantial, and will rocket over the next few years.

But the reality is somewhat different, at least according to well-respected market analyst, Yole Group. Figures from their latest report on GaN power devices show that the consumer market generated sales worth $250 million in 2024, and is forecast to be worth $2 billion in 2030. In comparison, while the rate of growth in the EV and telecom & infrastructure sectors will grow even faster, by 2030 revenues will still be far behind, with estimated values of $0.5 billion and $0.4 billion, respectively.

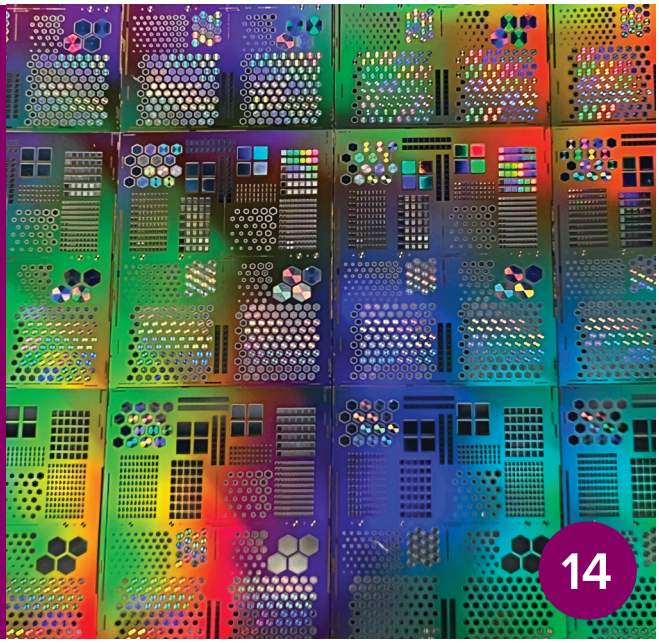
Sales, though, are only part of the equation. Margins matter, and they are often squeezed in long-standing applications. So, the focus of EVs and data centres is understandable, given the potential to combine multi-billion-dollar revenues with significant profits in the 2030s.

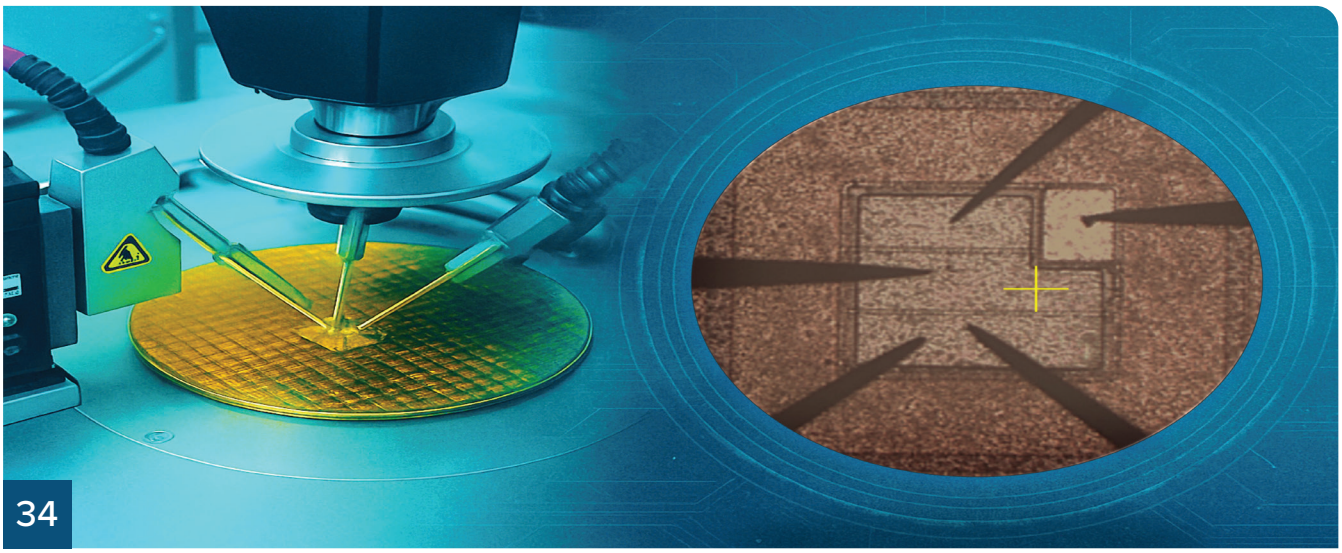
COMPOUND SEMICONDUCTOR

COVER STORY

The vertical GaN transistor: Time for take-off

Using 200 mm foundries, MIT start-up Vertical Semiconductor will produce finFETs on engineered substrates



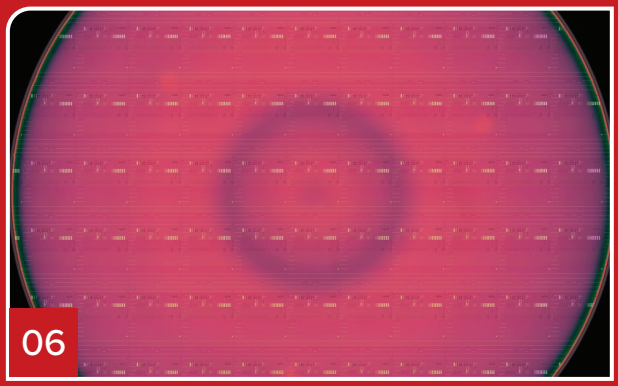


40

NEWS ANALYSIS

RESEARCH REVIEW

NEWS


06

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
News Editor Christine Evans-Pughe christine.evans-pughe@angelbc.com
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Event & Media Sales Executive Ranjodh Shergill ranjodh.shergill@angelbc.com +44 (0)2476 718970
Circulation Scott Adams scott.adams@angelbc.com
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205

Sales and Product Manager James Cheriton james.cheriton@angelbc.com +44 (0)2476 718970
Chief Executive Officer Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970
Chief Technical Officer Scott Adams scott.adams@angelbc.com +44 (0)2476 718970
Directors Jackie Cannon, Sharon Cowley

Published by Angel Business Communications Ltd, 6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. **T:** +44 (0)2476 718970
E: info@angelbc.com
W: angelbc.com

Imec achieves record GaN breakdown voltage

Achieves voltage resistance exceeding 650 V on Shin-Etsu Chemical's 300 mm QST substrate

BELGIAN research hub Imec has achieved a record GaN breakdown voltage exceeding 650 V using Shin-Etsu Chemical's 300 mm-diameter QST substrate, which has been adopted for Imec's 300 mm GaN power device development programme, launched in October 2025.

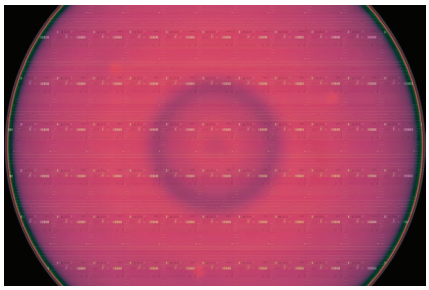
The initial results showed that Imec has successfully fabricated a 5 μm-thick high-voltage GaN HEMT, using Aixtron's Hyperion MOCVD equipment, with a breakdown voltage of over 800 V.

The results show that the QST substrate, which has a thermal expansion coefficient matched to GaN, can stably deliver excellent GaN crystal growth performance, even at large diameters.

Shin-Etsu Chemical, licensed by US company Qromis, manufactures 150 mm and 200 mm QST substrates, as well as GaN-on-QST epitaxial substrates of various diameters. In September 2024, it started providing 300 mm QST samples in a joint initiative with Qromis. Shin-Etsu Chemical and Qromis have also established a close partnership to provide 300 mm QST substrates for Imec 's 300 mm CMOS fab in Leuven, Belgium.

Because Imec's existing silicon wafer production line can be used for GaN, increasing the substrate diameter is expected to reduce production costs. However, GaN growth on silicon wafers suffers from increasingly poor production yields at larger diameters, due to issues such as wafer warpage, preventing practical mass production.

The 300 mm QST substrate solves this issue by enabling the epitaxial growth of thick-film 300 mm GaN for high-voltage applications without warping or cracks – previously unattainable on silicon substrates – thus significantly reducing device costs.



To date, Shin-Etsu Chemical has been enhancing facilities for 150 mm and 200 mm QST substrates and is currently working toward the mass production of 300 mm QST substrates.

The QST substrates are currently being evaluated by many Japanese and international customers for applications such as power devices, high-frequency devices, and LEDs. They are currently in the development phase for practical applications to address the recently increasing interest in AI data centre power supplies.

SiCSem breaks ground on India's first SiC fab

CHENNAI-BASED SiCSem has broken ground on India's first end-to-end SiC semiconductor production facility. The plant at Info Valley-II in Bhubaneswar represents the largest single investment (around $220 million) in the state of Odisha's emerging semiconductor ecosystem.

SicSem is partnering with British firm Clas-SiC Wafer Fab to set up the facility, which will eventually produce 60,000 SiC wafers annually and package 96 million units.

The aim is for the fab to help India become self-sufficient in power semiconductor devices for electric vehicles, fast chargers, green energy, photovoltaic inverters, motor controls, and beyond 5G communication.

The plant will create 5,000 direct and indirect employment opportunities and is expected to become operational by 2027-28.

The project received approval from the India Semiconductor Mission in August 2025.

Qorvo and Skyworks to merge

Joint company will form a $22 billion US-based RF, analogue and mixed-signal company

QORVO, known for its RF expertise and GaAs/GaN processes, and Skyworks, a maker of analogue and mixed-signal semiconductors, have agreed to combine the two companies in a cash-and-stock transaction that values the joint US-based enterprise at approximately $22 billion.

"This combination marks an important milestone for our industry and for Skyworks," said Phil Brace, CEO and president of Skyworks. "Combining Skyworks' and Qorvo's complementary portfolios and world-class engineering teams will strengthen our ability to meet growing customer demand across mobile and diversified broad markets. With enhanced scale, a more diversified customer base and operational synergies, we can bring even greater innovation to our customers and sustainable value to our shareholders."

"Qorvo and Skyworks share a culture of innovation and a commitment to solving our customers' most complex challenges," said Bob Bruggeworth, CEO and president of Qorvo. "Together with Skyworks, we can accelerate innovation and deliver broader and more comprehensive solutions across numerous growth areas. We are excited to leverage the combined strengths of our teams and product and technology portfolios to build on our capabilities in mobile and significantly expand our presence in defence and aerospace, edge IoT, AI data centre, automotive and other industries powered by secular growth trends."

With combined *pro forma* revenue of approximately $7.7 billion and Adjusted EBITDA of $2.1 billion, the view is that the combined company will be better positioned to compete against larger players – supported by a stronger, more balanced revenue base that enables more predictable performance, a more efficient cost structure and resilient cash generation through cycles.

The combined company also has over 12,000 issued and pending patents, which should enable faster development of system-level solutions and new design-win opportunities, according to the press announcement.

Under the terms of the agreement, Qorvo shareholders will receive $32.50 in cash and 0.960 of a Skyworks common share for each Qorvo share held at the close of the transaction, which implies a combined enterprise value of approximately $22 billion.

The boards of directors of both companies have unanimously approved the transaction, which is expected to close in early calendar year 2027, subject to the receipt of required regulatory approvals, approval of Skyworks shareholders and Qorvo shareholders and other closing conditions.

Infineon's chief marketing officer joins Wolfspeed

Matthias Buchner to broaden customer base for next-generation 200 mm SiC platform

SiC specialist Wolfspeed has appointed Matthias Buchner as SVP of global sales and chief marketing officer, effective December 1, 2025. Buchner will report directly to CEO Robert Feurle.

Buchner joins Wolfspeed from Infineon Technologies AG, where he most recently served as SVP of marketing for the Power & Sensor Systems division, responsible for strategic communication, partnership management, distribution marketing, digital marketing and marketing operations for a business worth at least $3 billion.

Over his more than 20-year career, he has held senior leadership positions at Infineon, Micron Technology, and other technology companies, with deep experience in both silicon and SiC power solutions, business development, and global customer engagement.

Buchner will lead Wolfspeed's sales and marketing organisations with a focus on leveraging the company's next-generation SiC devices, produced on its 200 mm manufacturing platform. The appointment supports Wolfspeed's strategy to broaden its customer base across diverse, high-growth markets including automotive, renewable energy, industrial power systems, and AI-driven data infrastructure.

"Attracting a world-class sales and marketing executive like Matthias at this critical juncture underscores Wolfspeed's commitment to capturing the immense opportunities ahead," said Robert Feurle, Wolfspeed's president and CEO.

He added: "His global leadership experience across silicon and SiC technologies – spanning automotive, industrial, and other competitive markets – will be instrumental as we strengthen our customer relationships

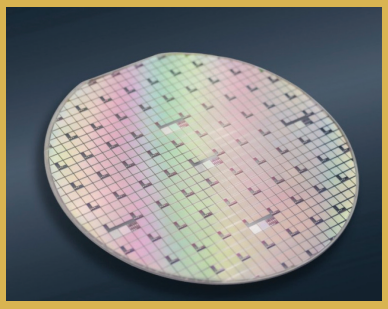
and expand into rapidly growing segments such as AI data centers, renewable energy, grid infrastructure, and aerospace and defence. With Matthias joining our team, Wolfspeed is exceptionally well positioned to translate our vertically integrated SiC platform into sustainable, profitable growth."

Buchner said: "I am very excited to join Wolfspeed at this important moment for the company and the industry, Wolfspeed's deep domain expertise in producing SiC devices sets the industry standard for performance and quality in today's competitive landscape. Building strong, trusting relationships with our customers will be a key focus for me immediately out of the gate, as we work together to accelerate the global transition from silicon-based to silicon-carbide-based technologies."

Wolfspeed recently came out of Chapter 11 with a strategic refinancing initiative to strengthen its balance sheet and position it for sustained, profitable growth. In conjunction with this effort, Wolfspeed has rationalised its production footprint. This includes the planned closure of its 150 mm device fab on the Durham campus by the end of calendar 2025, as well as the decision to discontinue development of a proposed fab in Saarland, Germany.

Onsemi reveals vertical GaN-on-GaN semiconductors

ONSEMI has introduced vertical GaN-on-GaN power semiconductors, which it says set a new benchmark for power density, efficiency and ruggedness for AI data centres, electric vehicles, and other energy intensive applications.



Dinesh Ramanathan, SVP of corporate strategy, Onsemi said: "Vertical GaN is a game-changer for the industry and cements Onsemi's leadership in energy efficiency and innovation."

By conducting current vertically, the new vertical GaN power semiconductors can handle high voltages of 1,200V and above in a monolithic die, switching high currents at high frequency with superior efficiency to deliver smaller and lighter systems.

The technology, developed by Onsemi's Syracuse, New York, R&D team, can cut losses in high end power systems by almost 50 percent, according to the company. By operating at higher frequencies, it can also reduce the size, including passives like capacitors and inductors by a similar amount. Compared to commercially available lateral GaN, vertical GaN devices are approximately three times smaller.

The company is sampling both 700 V and 1,200 V devices to early access customers.

Macom to manufacture HRL's GaN-on-SiC process

Macom to transfer advanced T3L high frequency semiconductor process into volume production

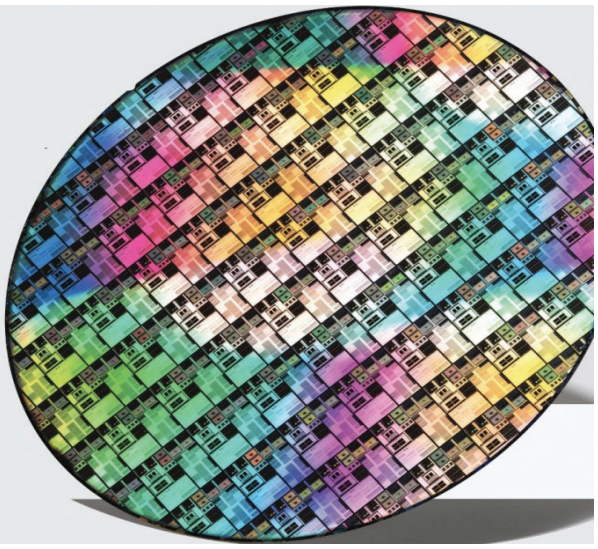
MACOM TECHNOLOGY has entered into an agreement with HRL Laboratories to license and manufacture HRL's proprietary 40 nm T3L GaN-on-SiC process technology. HRL and Macom will work collaboratively on a rapid process transfer of this proprietary semiconductor process from HRL's facility to one of Macom's US Trusted Foundries.

HRL, jointly owned by Boeing and General Motors, is regarded as a pioneer in the R&D of innovative RF and microwave GaN-on-SiC process technologies. T3L uses a proprietary epitaxial structure and an advanced gate design, which contribute to its high performance and enhanced reliability at millimetre-wave frequencies.

T3L was matured by HRL under the Office of the Undersecretary of Defense's (OUSD) State-of-the-Art Radio Frequency Gallium Nitride (STARRY NITE) and DARPA's Dynamic Range Electronics and Materials (DREaM) programmes, along with additional HRL funding that includes owner contributions.

"We're pleased to partner with HRL and look forward to establishing a close working relationship. T3L is one of the most advanced high-frequency semiconductor processes in the industry, which we anticipate will enhance our existing portfolio and accelerate execution of our roadmap," said Stephen Daly, President and Chief Executive Officer, Macom. "We were not part of the STARRY NITE or DREaM programmes; however, Macom and our customers will soon be the beneficiaries of the results, as we industrialise this technology."

> "We were not part of the STARRY NITE or DREaM programmes; however, Macom and our customers will soon be the beneficiaries of the results, as we industrialise this technology"



"This new relationship with Macom demonstrates HRL's expertise at developing and proving technology concepts and then transitioning them into production," said Rob Vasquez, president and CEO, HRL.

"Our GaN-on-SiC process technologies were established over many years of diligent work, and we're excited to now partner with Macom to advance the work into high volume production."

NcodiN secures €16 million to tackle AI bottlenecks with miniature laser

Transforming the future of AI hardware with optical interposers featuring integrated nanolasers

NCODIN, the deep-tech startup pioneering optical interposer technology with integrated nanolasers, has secured €16 million in oversubscribed Seed financing round.

The funding will propel NcodiN from R&D to industrial scale, enabling product development, key engineering hires to support the industrialisation of its technology in a CMOS pilot line on 300 mm wafers, and the build-out of its supply chain and customer partnerships.

The equity round was led by MIG Capital, with participation from Maverick Silicon, PhotonVentures, and Verve Ventures, alongside continued support from existing backers Elaia, Earlybird, and OVNI.

Transforming the Future of AI Hardware, NcodiN is developing NConnect, a new generation of photonic interposers designed to overcome the 'copper wall' – the performance and energy limits of electrical interconnects that constrain AI systems. At its core is the world's smallest laser, enabling dense integration on silicon and unprecedented scalability without disrupting existing processor architectures.

This breakthrough allows chipmakers to pack supercomputer-level power into a single processor, paving the way for faster, more efficient AI hardware. This fundraising will accelerate industrialisation of the platform, including an industrial pilot to demonstrate compatibility with advanced packaging techniques.

With this round, NcodiN will also establish a Silicon Valley presence, expand its R&D capacity, and scale its team in preparation for large-scale manufacturing partnerships – bringing new technology to break the copper wall and redefine AI hardware performance.

"This funding marks a pivotal milestone for NcodiN. We are delivering the missing piece for the industry's most pressing challenge: enabling extremely high-memory bandwidth to power the AI factories of tomorrow. Our technology unlocks wafer-scale superchips by providing the most energy-efficient interconnects for networking across tens of chiplets – an essential component in the architectures everyone is chasing. As new generations of GPUs and AI accelerators emerge to keep pace with rapidly evolving GenAI algorithms, NcodiN is laying the photonic foundation that makes them possible," said Francesco Manegatti, CEO and Co-founder, NcodiN.

"Memory bandwidth has become a defining bottleneck in AI, with copper interconnects struggling to deliver the reach and efficiency required for next-generation systems. NcodiN's photonic interposers unlock memory bandwidth and capacity beyond copper's limits. We are excited to support NcodiN as they enable architectures that will define the future of AI hardware," explained Josh Miner, Maverick Silicon.

Over the past 18 months, NcodiN has earned broad industry recognition for its vision and breakthrough work addressing AI's interconnect bottlenecks. The company has demonstrated proof-of-concept nanolasers with record energy efficiency below 0.1 pJ/bit, integrated nanodetectors, and full optical links, all on silicon. In parallel, NcodiN has established an independent cleanroom that now serves as a hub for rapid prototyping and joint development with industry partners.

To strengthen its foundation, NcodiN has expanded its network of strategic advisors, welcoming, among others, Eli Yablonovitch, Gus Yeung and Peter de Dobbelaere. Yablonovitch is a pioneer of photonic crystals and cofounded of Luxtera, Ethertronics, Luminescent, and Alta Devices.

Yablonovitch remarked: "NcodiN is addressing the next big opportunity in silicon photonics, the silicon photonic interposer, which permits high-bandwidth communication in a multi-chip system, particularly for AI and Machine Learning. To do this, they embed high-performance nanolasers in silicon, thereby combining physics elegance with manufacturability. This has the likelihood of revolutionising all future large scale cyber systems."

Oliver Kahl, Principal, MIG Capital, added: "NcodiN is working at the centre of the AI infrastructure market, a sector experiencing rapid, significant growth driven by the surging demand for generative AI, the proliferation of big data, advancements in specialised hardware like GPUs, and the widespread adoption of cloud computing. The company's ambitious team is shaping and empowering the future of computing to drive innovation across multiple industries."

"At Elaia, we've been proud backers of NcodiN since it's early days when it was a CNRS spin-off. While copper interconnects struggle to keep up, NcodiN is rewriting the rules with the world's smallest laser and a revolutionary optical network. This isn't just innovation; it's the key to unlocking the next leap in AI and hyperscale performance," added Clément Vanden Driessche, Elaia.

GlobalFoundries licenses GaN tech from TSMC

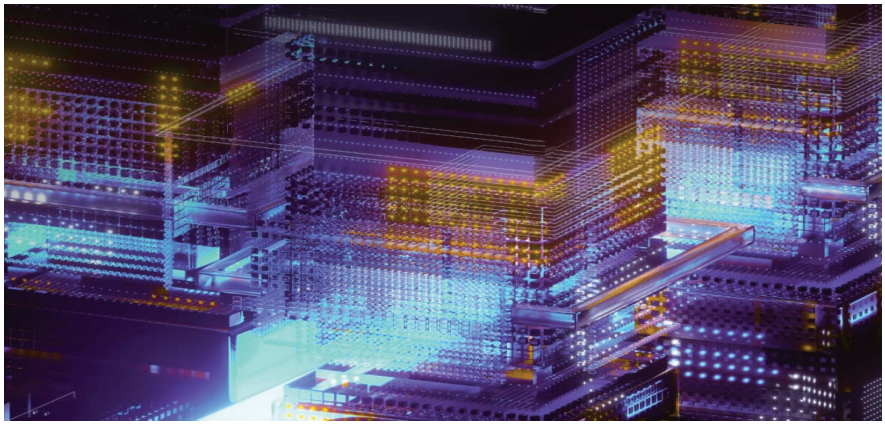
Deal aims to accelerate US-manufactured power range for data centre, industrial and automotive customers

GLOBALFOUNDRIES (GF) has entered into a technology licensing agreement with TSMC for 650 V and 80 V GaN technology.

This move aims to accelerate GF's next generation of GaN products for data centre, industrial and automotive power applications and provide US-based GaN capacity for a global customer base.

GF will qualify the licensed GaN technology at its manufacturing facility in Burlington, Vermont, using the site's expertise in high-voltage GaN-on-silicon technology to accelerate volume production for customers seeking next-generation power devices.

Development is set for early 2026, with production to begin later in the year.



"This agreement reinforces GF's commitment to innovation and its strategic focus on differentiated technologies that address essential power devices that we use to live, work and connect," said Téa Williams, senior vice president, power business at GlobalFoundries.

She added: "With the addition of this proven GaN technology, we will accelerate the development of our next-generation GaN chips and deliver differentiated solutions that address critical power gaps for mission critical applications from the data centre, to the car, and to the factory floor."

CEA-Leti looks to microLED for AI data links

Multilateral project aims to increase high-performance computing speed and efficiency with ‘orders-of-magnitude’ data-transfer gains

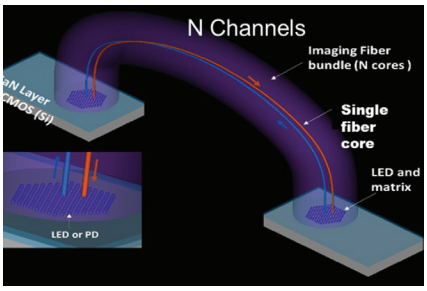
CEA-LETI is launching a multilateral programme on microLED technology for ultra-fast data transfer, with a focus on accelerating AI growth. The lab-to-fab initiative draws on the institute’s deep expertise in microLED process technology. The three-year initiative was announced at SEMICON Europa in Munich.

Set to begin in January 2026, it aims to engage manufacturers of microLEDs, optical fibres, photodiodes, and interconnects, as well as chipmakers, system integrators, and hyperscalers.

“Over the past decade, the computing power required to train leading-edge AI models has exploded by factors of millions, doubling roughly every three-to-four months as systems become more complex and data-hungry,” said CEA-Leti CEO Sébastien Dauvé.

“Supercomputers demand ever-faster communication links with very high energy efficiency and ultra-low latency – but interconnect performance is lagging behind compute power. That gap calls for a paradigm shift capable of boosting high-performance computing speed by orders of magnitude.”

Currently the tech industry is using slower copper-based data systems and



costly laser-based solutions. MicroLEDs, supported by a mature technology base, offer a compelling alternative – consuming less energy than either copper- or laser-based systems.

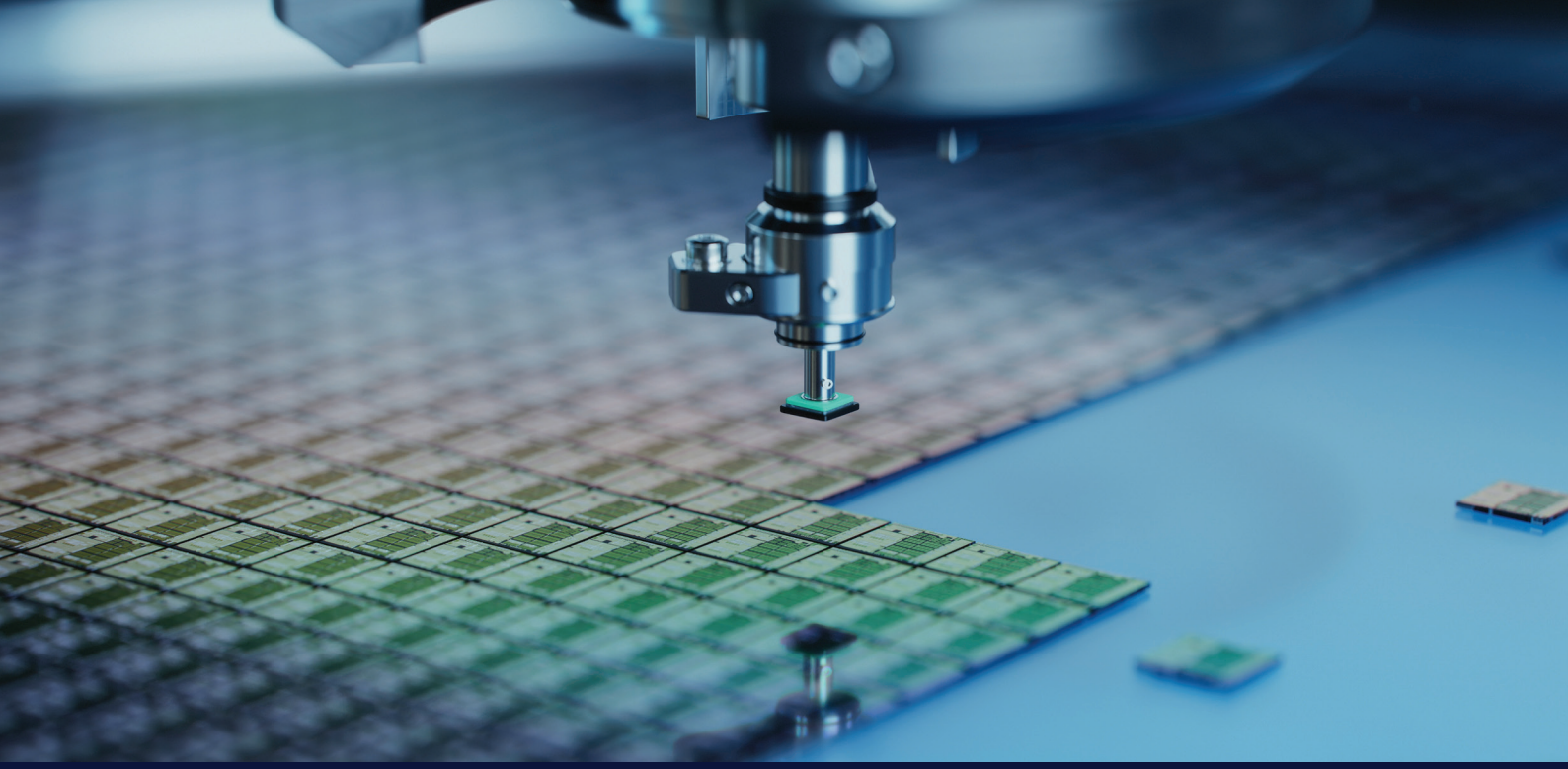
In a recent report on MOSAIC, Microsoft’s novel optical-link technology, a Microsoft team noted that ‘microLEDs are significantly smaller than traditional LEDs (and) can be modulated at several Gbps using a simple on-off scheme’.

The report, *MOSAIC: Breaking the Optics versus Copper Trade-off with a Wide-and-Slow Architecture and MicroLEDs*, also noted that the technology ‘achieves ten times the reach of copper, reduces power consumption by up to 68 percent, and offers one hundred times higher reliability than today’s optical links’.

“MicroLED represents a true paradigm shift for short-range optical, point-to-point data interconnects,” Dauvé added. “It delivers extremely high data-density transfer rates with far better energy efficiency than current technologies. Unlike silicon photonics or VCSELs, the microLED is scalable for massive parallel communication. By combining the complementary expertise of our programme members, we aim to break through the interconnect power and density bottlenecks that limit next-generation computing.”

CEA-Leti has been developing microLED technology for more than 15 years. The institute holds roughly 100 patents. Its use of silicon wafers and standard processes to produce microLEDs both scales and transfers easily to standard microelectronics foundries.

The institute will lead the Multilateral MicroLED Data Link Program with financial backing from its industrial partners. Together, members will map out a technical roadmap that sets clear objectives, milestones, and deliverables, and will track progress closely – adjusting course as needed to keep the collaboration on pace and on target.



AP INTERNATIONAL CONFERENCE

ANGELTECH

20-22 April 2026

Sheraton Brussels Airport Hotel, Brussels, Belgium

CONNECTING THE ADVANCED PACKAGING INDUSTRY

The 1st Advanced Packaging International builds on the momentum driving the next era of semiconductor innovation. Over two days, industry leaders and academic experts will deliver around 40 presentations across four key themes:

- Heterogeneous Integration
- Getting the Best Out of Incumbent Solutions
- Advancing Thermal Management
- Optimising Packaging Architectures

Conference attendees will gain insights into the materials, methods, and technologies reshaping chip-level packaging and system integration.

From cutting-edge thermal solutions to the reimagination of wirebond and leadframe formats, the event provides a comprehensive look at how packaging is enabling system-level innovation.

The two-day conference also includes expert panels and a dedicated poster session, creating multiple avenues for peer-to-peer engagement and technical exchange across the packaging ecosystem - from researchers and R&D teams to product engineers and system architects.

Advanced Packaging International is part of AngelTech, which delivers a portfolio of insightful, informative, and highly valued chip-level conferences.

Bringing together an Innovation Summit and four co-located conferences with more than 120 presentations, 700+ delegates, and over 80 exhibitors, AngelTech is the premier global event covering compound semiconductor, photonic integrated circuit, power electronic, and advanced packaging technologies. With significant overlap between the conferences, attendees benefit from exposure to full supply chains, customer bases, and partner ecosystems.

SPECIAL Event Discount:

10% OFF

Register before 31 January 2026 and get 10% OFF!

Registration to AngelTech allows you to access both days of **PIC International**, **Advanced Packaging International, CS International** and **PE International.**

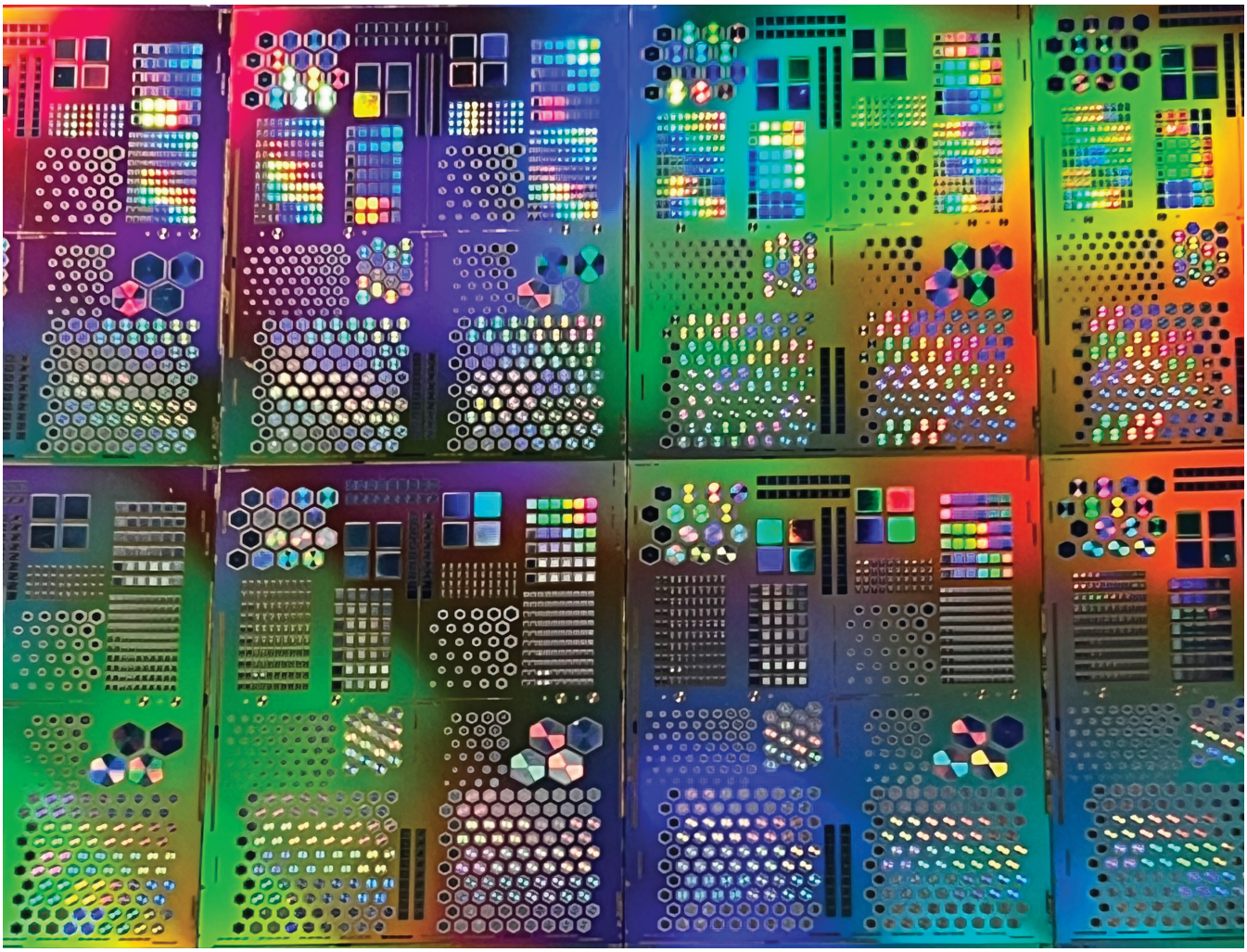
To find out more about our sponsor and speaker opportunities contact us today on:
+44 (0)2476 718970 or email: info@angel-tech.net https://ap-international.net

CO-LOCATED WITH:

CS INTERNATIONAL CONFERENCE
PIC INTERNATIONAL CONFERENCE
PE INTERNATIONAL CONFERENCE

ORGANISED BY

Angel BUSINESS COMMUNICATIONS
ANGEL EVENTS



The vertical GaN transistor: Time for take-off

Using 200 mm foundries, MIT start-up Vertical Semiconductor will produce finFETs on engineered substrates

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THERE'S a lot to be said for the vertical GaN transistor. Compared to its horizontal sibling, it delivers a higher breakdown voltage and current for a given footprint, while offering superior reliability, and simplifying thermal management.

However, efforts by start-ups to commercialise the vertical GaN transistor have flopped, and today it is the lateral variant that enjoys commercial success, thanks in part to establishing a 'killer' application, the fast-charging of mobile devices.

Holding back the success of the superior geometry is its native foundation. As well as a high price tag, the GaN substrate is limited in size, with a typical diameter of just 50 mm. This prevents device fabrication on established 200 mm lines that benefit from economies of scale, as well as the use of more modern processing equipment.

Trailblazing a solution to these limitations is Vertical Semiconductor, a spin-out of Tomás Palacios' group at MIT. Vertical is pioneering the use of 200 mm engineered substrates for the manufacture of GaN finFETs, an approach that allows the outsourcing of chip production to numerous foundries with silicon CMOS capabilities.

Founded last year, Vertical initially maintained a low profile, before announcing this October that it's secured $11 million in funding. This investment will be used to develop commercial devices on foundry lines that will enable the start-up to target the data-centre market. Here there is a much-publicised ramp in energy demand, due to the growth of AI, and GaN finFETs promise to make an impact by trimming energy losses and simplifying infrastructure. According to Vertical, its devices can increase efficiency by up to 30 percent, and enable a 50 percent reduction in the footprint of the power supplies.

It should be noted that the finFET is not the only class of vertical GaN transistor. For well over a decade, the global GaN research community has been exploring different designs, including the current-aperture vertical electron transistor and the trench MOSFET.

A significant weakness of both those designs is the demand for either epitaxial regrowth or the inclusion of *p*-type GaN layers – requirements that lead to a hike in fabrication complexity and cost, or an inferior channel carrier mobility.

Vertical is pursuing a different design, the finFET. This class of transistor only requires *n*-type GaN layers, so it can be produced without epitaxial regrowth.

Another strength of the finFET is the much-coveted normally-off operation, resulting from narrow fin channels that ensure all electrons are depleted at zero bias.

Back in 2019, benchmarking of the 1.2 kV GaN-on-GaN finFETs produced in Palacios' group, using a figure-of-merit for power switching that included all possible conduction and switching losses, highlighted the superiority of this design over all the state-of-the-art silicon and SiC power transistors and large-area GaN R&D devices.

This success has provided the core technology for Vertical, co-founded by Palacios and the company's CEO and CTO, Cynthia Liao and Joshua Perozek.

The backstory

While Perozek's path to CTO is a familiar one, involving the progression from a researcher in Palacios' group to technical lead in the start-up, Liao has arrived from a markedly different background.

After completing a degree in business administration at Western University, Ontario, she spent the first ten years of her career working in energy infrastructure, as well as energy and climate policy.

"I came to MIT as a mid-career MBA student in the Sloan-Fellow programme. And my goal was to actually pivot my experiences into a more entrepreneurial journey, and specifically using technology that I felt was quite exciting at MIT to make an impact around climate and energy."

Through a class at MIT, Liao met Perozek and Palacios. Enthused by the technology and its potential, she started supporting this lab, talking to potential customers. And after the class ended, the collaboration continued with much success, including the winning of competitions, the securing of initial support, and entry into an accelerator programme.

When Liao and Perozek graduated in summer 2024 they decided to incorporate the company.

Over the last year or so, Vertical has secured capital that will support its efforts to develop its first prototype packages, slated for sampling by the end of this year, before progressing to launch what's described as a fully integrated solution.

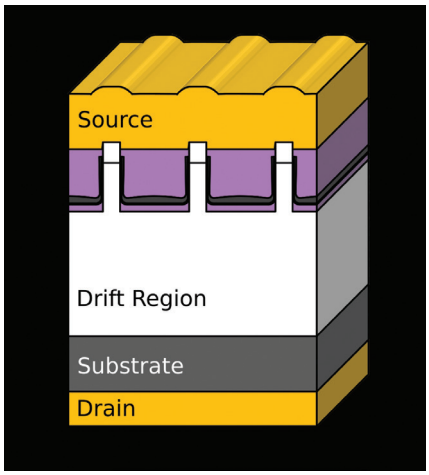
To execute these plans, Vertical will be working with suppliers of engineered substrates, and providers of epiwafer and foundry services.

Helping to bridge the transition between R&D and volume production is the work Perozek undertook during his time in Palacois' group, involving transfer of the technology from the research lab to the MIT Lincoln Laboratory. These efforts led to the fabrication of the first GaN finFETs on 200 mm wafers.

Targeting data centres

Another goal that Liao and her colleagues have been focusing on is generating demand with customers.

"We are engaging across the data centre power value chain, and working with customers to understand how that architecture is continuing to evolve, in order to serve the demands of these XPUs going into the future," says Liao.



Vertical's GaN finFETs feature a bottom contact on the backside of a 200 mm engineered substrate.

Data centres have various requirements for power, ranging from lower-voltage point-of-load to solid-state transformers and solid-state circuit breakers.

"We're excited about plugging ourselves into these different application areas, which go into industrial power supplies, grid interfaces, and renewable energy technologies," remarks Liao.

She also sees opportunities for the team's finFETs in electric vehicles, where they promise to extend the driving range while offering a smaller form factor than the incumbents.

But there is a downside of this market from Vertical's perspective: this is the relatively long qualification times, which hamper the start-up from establishing itself in the power market.

"Our goal is to get these devices into customers' hands, and then work on the reliability and qualification needed for automotive production," explains Liao, before adding that despite this priority, Vertical has started to engage with customers in the mobility and vehicle space.

The team at Vertical, now totalling six employees and expected to increase in number over the coming months, is developing a portfolio of devices with blocking voltages from 100 V to 1,200 V.

These GaN finFETs will be shipped as packaged die. "If people want bare die, we're happy to provide that. But we find that package is preferred," says Liao.

Over time, Vertical will expand its range, introducing devices with higher blocking voltages. That's relatively easy to do, as thanks to growth on engineered substrates, the thicker GaN layers needed to withstand higher voltages do not introduce significant bow and warp.

But for the next 12 months, Vertical's focus will be on producing working devices at scale with a foundry partner, and creating a clear path towards qualification. "That's our number one target," says Liao.

GaN's stalwart sector: Consumer electronics

While makers of GaN power electronics enthuse about the opportunities associated with AI and EVs, fast chargers will be the dominant application throughout this decade and beyond

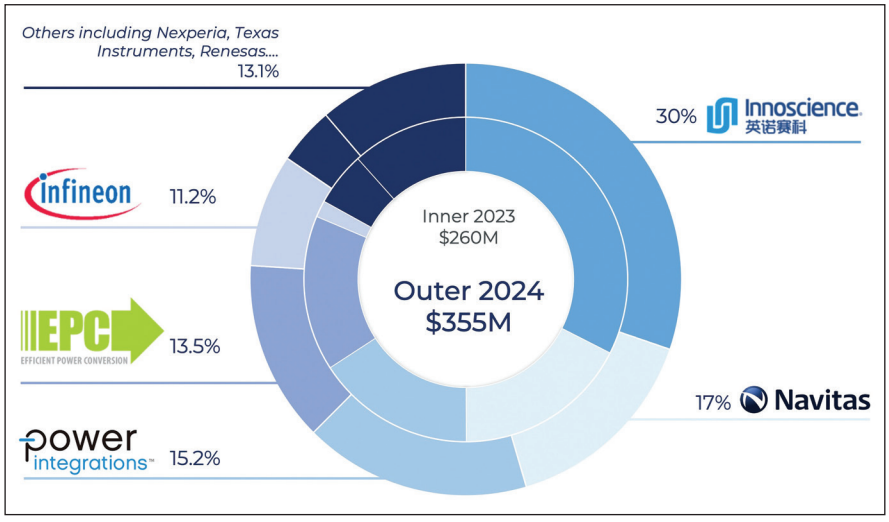
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

PICK UP a handful of press releases from the leading makers of GaN power devices and it's easy to spot a common theme – the tremendous opportunities associated with AI, and to a lesser extent, EVs. Both these applications demand efficient delivery of high voltages at high power densities, a task GaN is great at fulfilling.

Given the frenzied excitement and great importance ascribed to AI and EV by leading manufacturers of GaN power devices, it would be easy to fall into the trap of assuming that these applications are already significant – and if they are not dominating now, they soon will be.

So, given this state of affairs, the latest GaN report from Yole Group delivers a valuable, much-needed reality check. Yes, the EV and AI markets are growing very fast – but they are dwarfed by that of consumer electronics, and that's not going to change throughout this decade.

According to Yole Group's latest forecast, detailed in its *Power GaN 2025* report, in 2024 sales associated with the consumer electronics market totalled $250 million, and they will climb with a compound annual growth rate (CAGR) of 35 percent to $1.53 billion by 2030. In comparison, the CAGRs for the 'telecom & infrastructure' and 'automotive, mobility' sectors will be much higher over the same timeframe. They are forecast to have CAGRs of 53 percent and 73 percent, respectively, with corresponding annual revenues rising to $384 million and $540 million by 2030.



➤ GaN device players' market share in 2023-2024. Source: *Power GaN 2025* report, Yole Group

Offering insight into these trends, Yole Group's Roy Dagher, who holds the role of Technology and Market Analyst, Compound Semiconductors, explained that in 2024 about 70 percent of GaN power device revenue came from the consumer segment, a figure that will fall to 53 percent in 2030.

Dominating sales within the consumer sector are fast chargers, accounting for a share of around 90 percent in 2024. However, this sector is diversifying, with GaN power devices seeing increasing deployment in 'white goods', which includes home appliances, such as fridges, freezers and TVs. "We believe that it's going to grow massively in the next few years," remarks Dagher.

The consumer electronics sector also includes GaN devices for overvoltage protection. It's an application Innoscience is championing, in the form of a bi-directional switch technology that allows two devices to be replaced with just one.

To put the current status of the AI market in perspective, sales of GaN power devices to the telecom & infrastructure sector totalled just $29 million in 2024. In today's data centres, these devices provide DC-to-DC and AC-to-DC conversion.

The sector that Yole Group refers to as 'automotive, mobility' is even

smaller, with last year's revenue worth just $20 million. In this market, GaN devices are used for DC conversion in automobiles, and in power supplies for lidar systems. For the latter, Yole Group forecasts sales of GaN power devices to generate revenues of around $200 million by 2030.

Margins matter

For any chipmaker, sales are only part of the equation. Profit margins are also critical, and this accounts for the high levels of interest in the AI and EV markets.

According to Dagher, consumer electronics is the go-to market for newcomers. One of is appeals is its fast time-to-market.

"There's a lot of competition," says Dagher. "Margins are low, because there's a lot of players there. Prices get cut down."

Promises of higher profits are not limited to sales in EV and data-centre markets, and extend to industrial applications. They include motor drives, a sector that EPC and Infineon are targeting, as well as photovoltaics, with Enphase deploying GaN power devices in its micro-inverters.

The big players

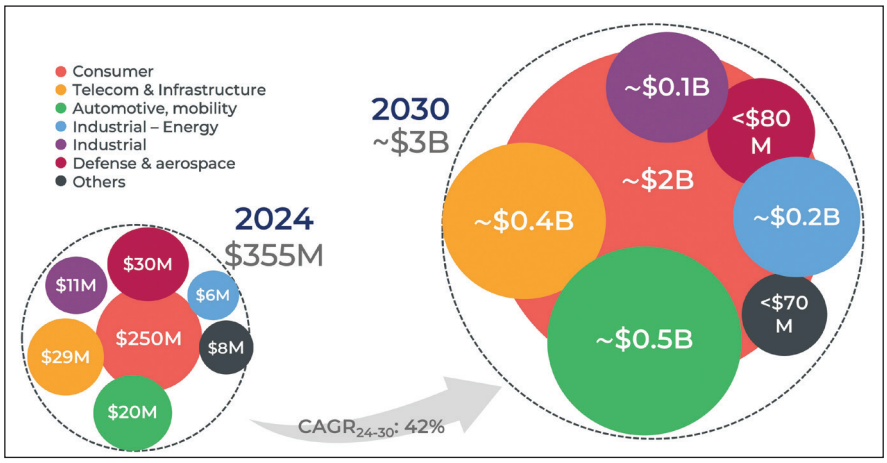
Topping the list of producers of GaN power devices is the Chinese chipmaker Innoscience, which enjoyed a 30 percent market share in 2024, a figure expected to nudge a little higher this year.

Dagher attributes this success to a number of factors, including a high production capacity and Innoscience's migration to 200 mm substrates ahead of all its rivals.

"They have this strategy to capture market share by cutting down prices and increasing volume," argues Dagher, who points out that Innoscience also benefits from a strong domestic supply chain.

Leaders of the chasing pack include: Navitas; Power Integrations; EPC; Infineon, which acquired GaN Systems in March 2023; and Renesas, which bought Transphorm in summer 2024.

When considering all those on this list, plus smaller players, Dagher notes that



➤ GaN power device market, by end markets. Source: *Power GaN 2025* report, preliminary results, Yole Group

one trend is the move towards vertical integration. "Companies are trying to control the supply chain, from epitaxy to packaging."

Backing up this claim, Dagher notes that the fabless company Navitas recently hired a senior epitaxy director. He also points out that EPC, which has a fab-lite business model and partners with Vanguard and Episil, has its own epitaxial lines; and that Power Integrations is undertaking its own epitaxy.

"There exist some foundry services that could help these companies go a long way. But in future, the IDM model will control most of the market."

While those looking for a foundry partner can no longer work with TSMC, there are many other companies offering these services for the production of GaN power devices, including a number of new entrants, such as Global Foundries, PSMC, Polar Semi and Samsung.

Topping the list of producers of GaN power devices is the Chinese chipmaker Innoscience, which enjoyed a 30 percent market share in 2024, a figure expected to nudge a little higher this year

Another trend that Dagher is forecasting for the coming years is an increase in the blocking voltage provided by GaN products, so that they can start to compete directly with SiC MOSFETs and diodes.

Efforts in this direction, which will propel GaN to 1200 volts and beyond, include the introduction of multi-level topologies. There's also EPC's stacking of devices, an approach it refers to as series output parallel topology that's employed to increase the blocking voltage of products for data centres. Further innovation on this front includes Onsemi's release of GaN-on-GaN vertical transistors, and Power Integration's devices that are grown on sapphire.

"[Power Integration] has today already commercialised 1,250 volts. They plan to use it in the data centre," says Dagher, who points out that this company has also produced a variant operating at 1700 volts – but it can only handle low powers.

Gains in performance and/or pricing may also results from the introduction of engineered substrates, such as the QST platform from Qromis, and Infineon's efforts to produce devices on a 300 mm line.

So, while the dominant application for GaN is unlikely to change in the next five years, this part of the power electronics industry will certainly not be standing still.

AlScN: A nitride for computation?

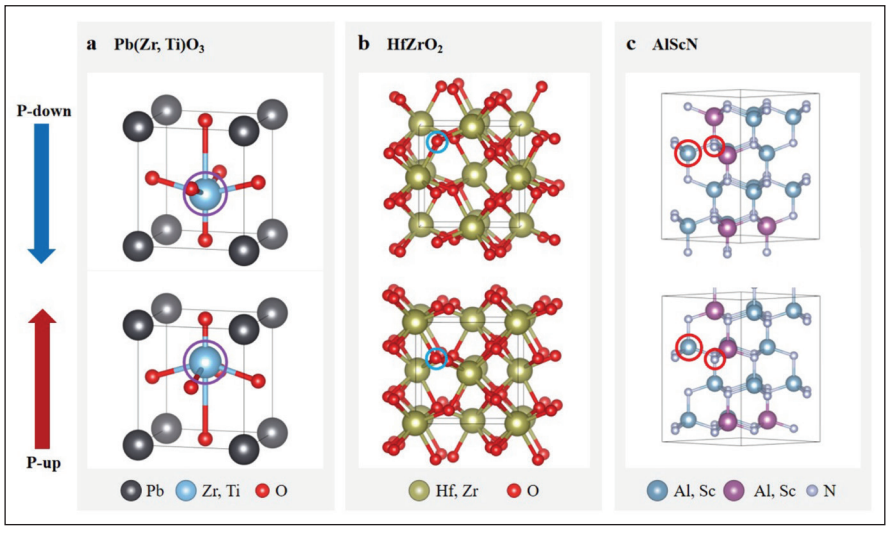
The novel ternary AlScN enables a silicon-compatible, wake-up-free ferroelectric memory for next-generation AI hardware

BY MINGRUI LIU, XIAOJUAN SUN AND DABING LI FROM STATE KEY LABORATORY OF LUMINESCENCE SCIENCE AND TECHNOLOGY, CHANGCHUN INSTITUTE OF OPTICS FINE MECHANICS AND PHYSICS, CHINESE ACADEMY OF SCIENCES

DUE to rapid advances in AI, the traditional computing architectures, which separate storage and computation, are facing critical speed and power bottlenecks. The latter is not helped by frequent data migration between processors and memory, accounting for more than 60 percent of total power consumption, while energy efficiency for actual computation remains below 10 percent.

Note that we literally do far better. By utilising synaptic networks for information transmission and processing, our brains provide highly parallel storage and computation. This leads to advanced intelligence, far surpassing that of computers, with a power consumption of just 20 W. Imagine if computer memory could emulate neural synapses – such a breakthrough would revolutionise the global electronics industry.

Offering much promise on this front are ferroelectric materials. Featuring electric-field-tuneable polarisation, ferroelectrics enable information writing via electrical pulses, and non-volatile storage/computation through remanent polarisation. And they have another key asset, multi-domain state regulation, that enables high-precision linear conductance modulation, and ultimately multi-level storage, closely mimicking synaptic weight updates in biological learning. These strengths ensure that ferroelectrics are an ideal platform for energy-efficient neuromorphic devices.



➤ Figure 1. (a) In ABO_3-type perovskite ferroelectrics represented by $Pb(Zr,Ti)O_3$, polarisation reversal involves the movement of B-site atoms. (b) In hafnium-based ferroelectrics, polarisation reversal involves the movement of oxygen atoms. (c) In wurtzite nitride ferroelectrics represented by AlScN, polarisation reversal involves the simultaneous movement of nitrogen and metal atoms.

Why wurtzite ferroelectrics?

Unfortunately, most ferroelectrics are oxides. This makes them challenging to integrate into mainstream semiconductor platforms. But there's hope, with recent advances in wurtzite-structured ferroelectric nitrides providing new opportunities to overcome this dilemma. This class of materials breaks new ground by combining a compatibility with silicon platforms with: enhanced remanent polarisation, a key metric that is 2-6 times higher than that for HfO_2 or perovskite ferroelectrics; sustainable thickness scaling; a high Curie temperature of more than 1100°C; and a stable ferroelectric phase.

Although the discovery of wurtzite nitride ferroelectrics has promise, there are concerns, related to high coercive fields that result in an increased switching voltage and degraded endurance and 'wake-up effects' – they cause devices to require repeated electrical cycling to reach peak performance.

The root cause of these issues lies in microscopic domain evolution, as the polarisation direction of these ferroelectrics is governed by the stacking order of the metal and nitrogen atoms. Unlike oxide ferroelectrics, where polarisation reversal involves a more straightforward single-atom movement, simultaneous motion of metal and nitrogen atoms is required.

This leads to larger energetic switching barriers, manifesting as wasted power and operational instability. Due to this, it is critical to clarify real-time domain dynamics under external electric fields and manipulate, at low fields, the motion of the domain walls – they are the boundaries between oppositely polarised regions.

Our team at the Chinese Academy of Sciences has addressed these challenges in wurtzite ferroelectrics by focusing on real-time domain wall motion in representative $Al_{0.75}Sc_{0.25}N$ films. Our primary tools are dark-field transmission electron microscopy and first-principles simulations.

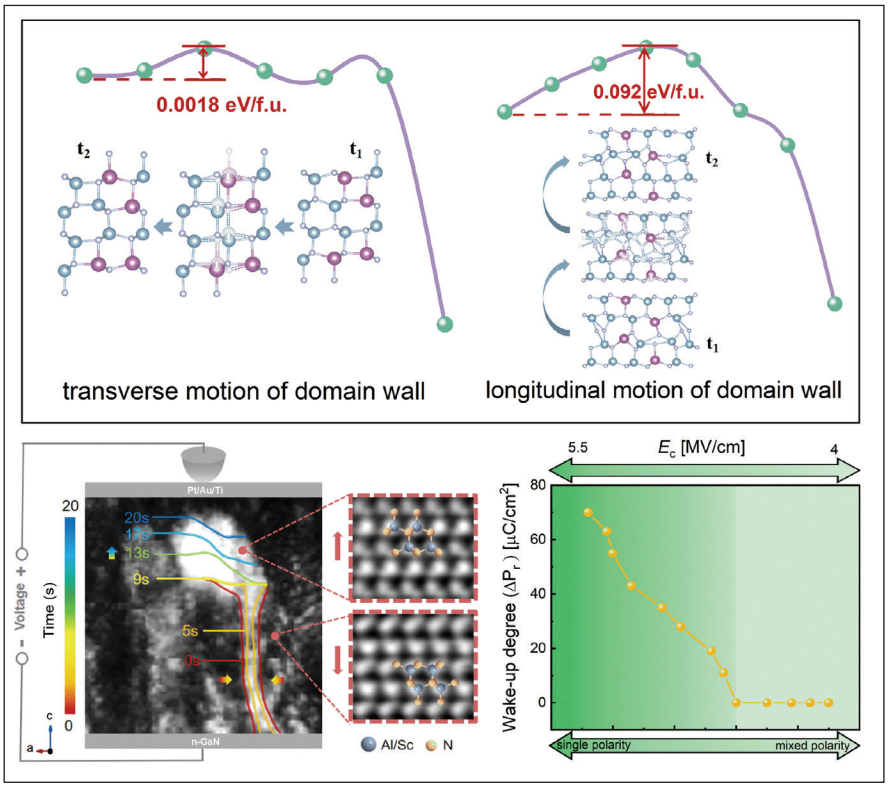
We have found that under the same bias, the transverse motion of the domain wall (perpendicular to the *c*-axis [0001] direction) invariably precedes the longitudinal motion (along the *c*-axis), due to a 98 percent reduction in energy barriers. This is a game-changing finding, fundamentally breaking the traditional ferroelectric switching model and providing a new framework for polarisation reversal in complex lattice systems.

Based on our observations, it is possible for high-domain-wall-density AlScN, ideally with a mixed polarity penetrating the entire film, to realise polarisation reversal through transverse motion of the domain wall. However, single-polarity films need additional reversed-domain nucleation and longitudinal motion with higher energy barriers, thereby exhibiting high coercive fields and wake-up behaviour.

This is an exciting discovery. It implies that a promising pathway for reducing the overall polarisation reversal energy of wurtzite ferroelectrics is to maximise lateral domain wall movement while suppressing longitudinal migration.

Engineering the breakthrough

Guided by the underlying mechanism, we have cut the overall energy cost by promoting the transverse motion of domain walls, realised by regulating the mixed polarity penetrating the entire film. This strategy delivers a 25 percent reduction in the coercive field strength while maintaining a high remanent polarisation and completely eliminating wake-up effects across 150 mm-diameter films. To the best of our knowledge, these results are setting a new benchmark for ferroelectric properties and crystal quality.



➤ Figure 2. Top: The energy barriers of the transverse and longitudinal motions of the domain wall calculated by first principles simulations. Bottom left: Contour plots of the domain wall motion versus time, integrated differential phase contrast scanning tunnelling electron microscopy images of the dark (N polarity) and light (metal polarity) regions. Bottom right: Regulation of wake-up effect and the coercive electric field.

Our work establishes a universal framework for optimising polarisation switching in wurtzite ferroelectrics. It is a particularly timely advance, offering a solution for addressing the growing demand for energy-efficient computing architectures in the AI era, and providing a clear pathway from fundamental research to industrial applications in memory, logic, and sensing devices.

It's worth noting that ferroelectric domain walls have been regarded as nanoscale functional interfaces, exhibiting reduced dimensionality and a different symmetry from the host material. Due to this, they give rise to physical properties that do not exist in the surrounding uniformly polarised domains.

We will now pivot our research, switching our focus to harnessing conductive domain walls as programmable functional elements that could enable precise control over multi-level resistance states and emulate memristive behaviours that are critical for neuromorphic computing. Success will not only pave the way for sub-nanometre device scaling, but also revolutionise integration, by merging memory and computation at the atomic interface. By leveraging domain wall conductivity for synaptic weight modulation, we foresee a new generation of ultra-dense neuromorphic architectures – they could finally bridge the gap between traditional systems and biological brain efficiency. The ability to engineer intelligent nanointerfaces may well define the next frontier in post-Moore's-law electronics.

FURTHER READING

➤ M. Liu *et al*. "Low-Field-Driven Domain Wall Motion in Wurtzite Ferroelectrics" Adv. Mater. **37** 2505988 (2025)

Progressing the PCSEL towards high-volume production

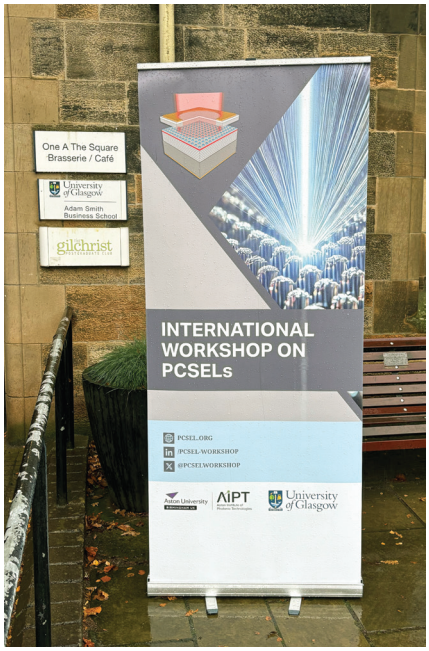
By developing and refining the PCSEL, manufacturers of optoelectronic device are laying the foundations for the commercial success of this very promising class of laser

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

TAKING a device from its inception to lucrative, high-volume production is a lengthy, complex journey. Following the eureka moment that spawns a promising idea for a new class of device, there's the fabrication of the first chip and then its development, demanding many years of funding, often secured by identifying a potentially 'killer' application. Design and processing must then improve, so that this device satisfies a long list of requirements, including those related to performance, yield, cost and reliability, prior to the commercial launch of a competitive product that will net significant sales. That last step is particularly tricky to navigate if the fledgling device will only succeed in the marketplace by displacing an incumbent, as then it's critical that the new contender outperforms its rival by significant margins to win over the wavering minds of system engineers that are responsible for placing orders.

Against this backdrop, how much progress has been made by the PCSEL, the surface-emitting single-mode laser with a photonic structure that's renowned for its exceptional beam profile, incredibly narrow divergence, and a power that scales with the size of the emitting region?

While it's never possible to offer a definitive answer to this crucial question, those attending the recent second International Workshop on the PCSEL could offer an informative, well-considered answer. At that gathering, held on 10-12 November in Glasgow, UK – and co-located with the 14th International Symposium on Photonic and Electromagnetic Crystal Structures – a number of companies and universities detailed advances in the performance of the PCSEL. And during networking events, including a delightful visit to a local distillery, a number of low-profile delegates disclosed that they were also pursuing the development this promising surface-emitting laser, either at a company looking to diversify its laser portfolio or a new start-up formed to champion this device. So, what's clear is that there's tremendous momentum behind the PCSEL, with much effort directed at preparing the ground for commercial success.



➤ The second International Workshop on the PCSEL, held on 10-12 November, was co-located with the 14th International Symposium on Photonic and Electromagnetic Crystal Structures. Some talks were held at Glasgow University, while others, along with two posters session, took place at the nearby Grosvenor Hotel.

Laying much of the foundation for progress to date is Susumu Noda, the leader of PCSEL development at Kyoto University, and a co-author of the first ever paper outlining this device, published back in 1999 in *Applied Physics Letters*. Since that ground-breaking conception, Noda's group has made a great deal of progress on many fronts, including the production of numerous devices, featuring higher powers and an expansion of material systems and spectral ranges.

Noda delivered the keynote session at the joint conference, with a presentation describing many potential applications for the PCSEL. They include using this device as the optical source for lidar employed in automobiles, farm machinery and robots; the deployment of PCSELs in material processing; and using this source for free-space communication, both underwater and over vast distances in space. In fact, there are so many applications where the PCSEL could serve that this situation may be viewed as an embarrassment of riches – with such a vast number of opportunities, it can be a challenge to know quite where to focus.

As one would expect in a keynote presentation, Noda covered a great deal of ground, highlighting key milestones from more than two decades of trailblazing research. While much of this would be familiar to many in the audience, the latest results, yet to be published, would be new to them. Building on powerful sources with an emission diameter of

3 mm, Noda and co-workers have just introduced variants with a diameter of 10 mm, emitting at around 940 nm. Initially, these sources produced more than 500 W of optical power when driven with pulses of 1000 A, and very recently continuous-wave outputs of 500-1000 W have been developed, with the PCSEL's thermal management benefitting from its bonding to a sub-mount.

Today, the most efficient PCSELs have a wall-plug efficiency of around 25-30 percent. Noda suggested that far higher values, potentially up to 60 percent, might be realised by turning to multi-junction PCSELs.

Offering a tantalizing glimpse into the future, the PCSEL pioneer claimed that it may be possible to produce 15-20 kW devices with an emission diameter of 3 cm. Such sources would be a very attractive alternative to today's CO_2 lasers, which are bulky – typical dimensions are around 1.5 by 0.4 m by 0.5 m – and have an efficiency of about 10 percent.

A key member in Noda's group, Takuya Inoue, focused on one of the applications mentioned in the keynote address, giving a presentation on the dynamic control of PCSELs for satellite communication. Inoue explained that satellite communication involves transmission over distances of more than 1000 km at data rates between 1 Gbit s^{-1} and 100 Gbit s^{-1}. As only a fraction of the light leaving the transmitter will hit the detector, due to beam divergence, the source must produce an optical power of at least 1 W.

Outlining the requirements for the transmitter, Inoue remarked that "the size, weight and power must be as small as possible". But these are not the attributes of a conventional transmitter, which incorporates an erbium-doped fibre amplifier that's large and heavy. This transmitter also features a number of components, hindering reliability.

PCSELs have much promise for this application, thanks to their high power and incredibly narrow beam divergence. But what modulation speeds are possible?

Inoue and colleagues have been investigating this matter for a few years, with initial efforts determining watt-class operation with a direct bandwidth of more than 3 GHz. Turning to quadrature amplitude modulation has enabled transmission of 256 QAM signals at 2 Gbaud.

More recently, this team has investigated coherent free-space optical communication, realised with two-section PCSELs featuring a pair of photonic crystals with slightly different lattice constants in their gain sections. By injecting an anti-phase modulation current with the same bias current in both sections, the team have generated watt-class frequency-modulated signals with supressed amplitude modulation. This success provided the foundation for employing this PCSEL as a coherent free-space optical transmitter delivering Gbit s^{-1} signal transmission, even when laser power is attenuated by 80 dB. Success with such a degree of attenuation, corresponding to the link loss in satellite communication, allows Inoue to claim that the team's directly modulated PCSELs have the potential to provide compact free-space optical transmitters for tomorrow's satellite communication systems.

As well as running the world's leading group on PCSEL development, Noda has inspired and supported a number of Japanese optoelectronic manufacturers in their development of this device. They include Hamamatsu Photonics, which launched the first commercial PCSEL in 2017 (a data sheet for this product, the L13395-04, can be found on the internet, but there is no price, suggesting it's been discontinued).

Hamamatsu is continuing to develop its PCSELs, targeting applications requiring a patterned light source. During development of its lasers, one of the issues that's been addressed is what's described as 'mesh noise' – this arises from an anti-crossing of photonic bands between the fundamental mode and higher modes in the layer direction.

At the PCSEL workshop, company spokesman Yoshitaka Kuorsaka told delegates that these modes have now been eliminated. Details surrounding the solution were scant, but involved changes to the epitaxial structure. Another issue that's been addressed is zero-order noise, removed by modifying the photonic crystal structure to introduce an additional phase. Recent efforts by Kurosaka and co-workers have focused on a structure with two embedded regions in the same square lattice. The team have produced horizontal stripe patterns with a phase difference of 90° that have a stripe intensity ratio for each pattern region that changes continuously when the beams are superimposed. Based on this demonstration, Kurosaka claims that this work paves the way to a dynamically changeable light pattern consisting of multiple channels.
In related work, Kurosaka's colleague Kazuyoshi Hirose detailed micro-pattern projection from a PCSEL-based on-chip pattern generator. These projections could be deployed for 3D profilometry – that's the measurement of surface profiles – with high-quality patterns needed for practical application.

InP PCSELs

Another Japanese optoelectronics powerhouse that is partnering with Noda's team for PCSEL development is Sumitomo Electric Industries. This firm is directing efforts at improving the performance of InP PCSELs emitting at 1.3 μm and 1.55 μm, viewing such devices as promising candidates for sensing, free-space communication and sources for optical communication networks.

The power of Sumitomo's PCSELs has increased significantly over the last few years. Back in 2022, designs featuring a double-lattice produced an optical output of 200 mW. The introduction of a metal mirror the following year doubled output, and the latest PCSELs are emitting 700 mW, thanks to the introduction of an in-plane heterostructure.

➤ On the first evening of the conference, delegates were offered a guided tour of Clydeside Distillery.

Sumitomo spokesman Yuhki Itoh told delegates that the team began by switching from a single-lattice to a double-lattice to increase vertical radiation and hit 200 mW. This refinement produced a 25-fold hike in slope efficiency.

Introducing a metal mirror provided the next jump in output power, with this move enhancing carrier injection and reducing emission in unwanted directions. Thanks to these benefits, InP PCSELs emitting at around 1330 nm produce: a slope efficiency of 0.4 W A^{-1}; output powers of more than 400 mW and 150 mW at 25°C and 70°C, respectively; a wall-plug efficiency of more than 24 percent at 25°C; and a side-mode suppression ratio exceeding 70 dB. Variants with the same design emitting at 1.5 μm produce a continuous-wave output of 300 mW at 25°C, and a peak power of 32 W when driven with short pulses.

To address limitations associated with self-heating that led to the leaking of light, Itoh and co-workers have recently introduce an in-plane heterostructure. This refinement is accomplished by reducing the size of the air holes near the device periphery, a change that leads to a lowering of the photonic band-edge frequency and ultimately an enhanced in-plane optical confinement. With this modification, output power climbs to 700 mW, and wall-plug efficiency is 27 percent at 25°C.

Itoh and co-workers have also investigated the reliability of their PCSELs. Results are encouraging, with no degradation observed when driving these devices for 2,500 hours at 105°C.

Benchmarking these PCSELs against high-power DFB lasers also leads to promising findings, including a superior wall-plug efficiency, a higher side-mode suppression ratio and a much narrower beam divergence.

Into the blue

Most of the development of the PCSEL has involved GaAs and InP material systems. But to reach shorter wavelengths, these emitters must be formed with the GaN-based material system.

In Japan, much effort has been devoted to the development of surface-emitting lasers based on GaN and its alloys. More than a decade ago, Nichia made a number of early breakthroughs in GaN VCSEL performance, including the first device producing more than a milliwatt. And more recently, other Japanese leaders in optoelectronics have grabbed the headlines, with impressive output powers of 15.4 mW and 22.2 mW, announced at Photonics West 2019 by Sony and Stanley Electric, respectively. Later that year, Stanley followed this up with a paper in *Applied Physics Express*, detailing a Watt-class blue-emitting array of 16 by 16 VCSELs.

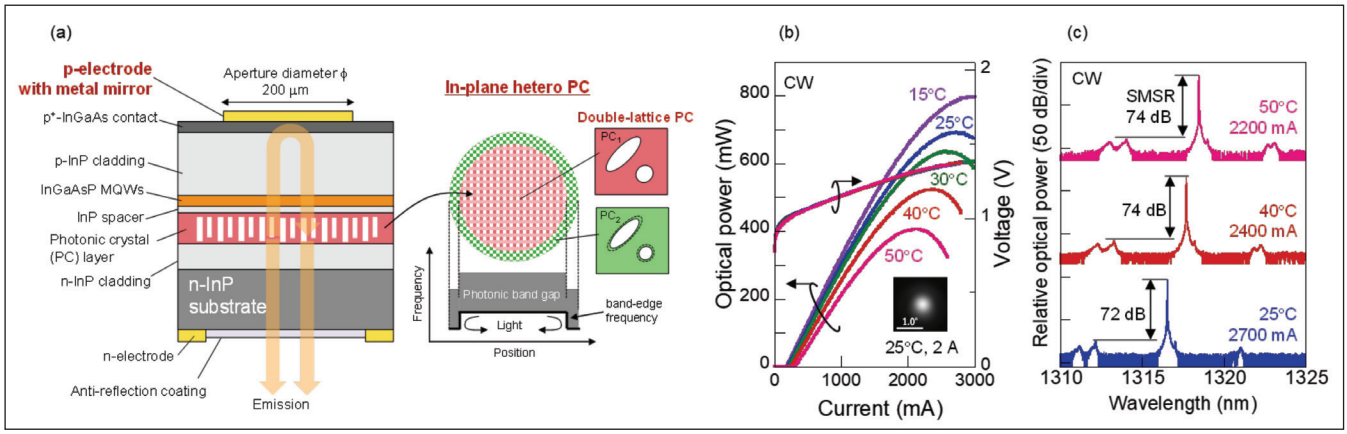
Given how hard it is to make progress with GaN-based VCSELs, mainly due to issues associated with producing the mirrors – there's no ideal lattice-matched pairing with a high refractive index contrast and good electrical conductivity – it's not that surprising that Stanley Electric has also started to develop GaN-based PCSELs. Efforts on this front were presented in Glasgow by Mei Emoto, who described the progress of a collaboration between researchers at Stanley Electric and Kyoto University.

Emoto began by putting recent efforts in context, explaining that Noda's group produced the first ever GaN-based PCSEL, reporting that success in 2008. That breakthrough emitter, featuring a triangular lattice and air holes, had a very high threshold of around 70 kA cm^{-2}. Weaknesses of that pioneering PCSEL included insufficient resonance, a large scattering loss and a low slope efficiency.

To produce a higher-performance device, Emoto and co-workers switched to a square lattice to enhance optical confinement, optimised the size of the resonator, and developed a SiO_2-free fabrication method. In addition, they have worked to improve crystal quality, aided by the use of GaN substrates. With these changes, PCSELs with a period for the holes of around 200 nm have a threshold current of around 2.6 kA cm^{-2}.

Further improvements have resulted from the introduction of a double lattice that enhances vertical emission and in-plane resonance. With this refinement the team produced a single-mode PCSEL with an output of 1 W, emitting at 431 nm from a circular region with a diameter of 300 μm.

Even higher powers have come from an increase in the emission area to a diameter of 500 μm. With this change, output power exceeds 2 W, realised with a slope efficiency of 0.5 W A^{-1}. Emoto revealed that one of the issues with that generation of PCSELs is that as the current through the device is cranked up, there is a slight widening of



➤ Sumitomo Electric Industries has been developing InP PCSELs emitting at 1.3 μm and 1.55 μm. (a) Schematic of these InP-based PCSELs. (b) Light-current-voltage characteristics with far-field pattern (inset) and (c) lasing spectra under continuous-wave operation.

the beam divergence angle. To address this, the team modified the design of its high-power PCSELs, increasing destructive interference to cut off the higher modes. With this optimisation, PCSELs have a stable fundamental mode, a threshold current of around just 1.8 kA cm^{-2}, a slope efficiency of 0.6 W A^{-1}, and an output power of more than 2 W.

The most recent results may be even more impressive. While Emoto failed to divulge many details, emitting area has increased to a diameter of 1 mm, and the divergence angle is just 0.5°.

Emoto concluded his talk by showing how the team's PCSELs can be used for underwater lidar, operating in systems with a 10 m range, and revealing that they have just started to collaborate with Nichia on the development of these devices.

UK efforts

Within the UK, the host nation for the workshop, there are efforts at developing PCSELs. This includes engineers at Huawei investigating these devices at the legendary facility in Ipswich, previously owned by BT and Corning, and recently renamed as the Bragg Research Centre. Here, efforts are focused on InP PCSELs, primarily for optical communication.

Speaking on behalf of PCSEL efforts at Huawei, Samir Rihani argued that the communication sector has fuelled laser innovation for many decades, driving the development of distributed Bragg reflector lasers in the 1970s; and in the data era that started in the 1990s, the first killer application of the VCSEL. And now with the growth of machine learning and AI, applications that demand massive parallel data transfer, there's an opportunity for a compact, high-power laser, ideally operating at multi-wavelengths – and these requirements could be fulfilled by the PCSEL.

Working towards this, Rihani and co-workers have developed an InP-based multi-wavelength PCSEL with four channels, operating at around 1330 nm. This source has a wall-plug efficiency of 16 percent, and a power-per-channel of 45 mW at a drive current of 250 mA channel. Operating at up to 85°C, the slope efficiency for this PCSEL is 0.24 W A^{-1}.

According to Rihani, the team's quad-PCSEL has good channel uniformity, with a channel flatness of less than 1 dB, meeting the requirement for a multi-wavelength light source. The researchers have demonstrated a channel spacing of 0.6 nm, laying the foundations for a 32-channel PCSEL.

Rihani's colleague, David Moodie, outlined the development of a 1550 nm PCSEL with a hetero-lattice design, created in collaboration with researchers at the University of Nottingham. Moodie explained that the motivation behind this design is an increase wall-plug efficiency, realised by reducing in-plane loss.

In addition, Moodie and co-workers have tried to optimise the round-trip phase from the photonic crystal to the *p*-metal reflector. This investigation involved etching of the *p*-type InP by either 0 nm, 61 nm, 122 nm or 183 nm, prior to addition of *p*-contact layers.

To produce the hetero-lattice PCSEL, the team defined an inner lattice, occupying a 200 μm square area, and featuring a double-lattice design – one lattice is shifted vertically and horizontally by a quarter of the 477 nm pitch. In addition to this inner lattice that has a 12.6 percent fill factor, the engineers formed a second photonic crystal that occupied the remainder of the 300 μm by 300 μm area. For this photonic crystal, there's a 15.5 percent fill factor, and circular holes with half the pitch of the inner fill factor.

According to Moodie, the best results came from PCSELs with no *p*-type etching. For these devices, the introduction of the hetero-lattice increased the slope efficiency by 34 percent, boosted the output power, improved linearity, and ensured that the laser continued to operate in single-mode at higher current densities. Hetero-lattice PCSELs produced single-mode lasing at up to 85°C.

Measurements of these PCSELs recorded powers of 249 mW and 145 mW at 25°C and 55°C. Driven at 2.5 A, side-mode suppression ratio exceeded 65 dB at both these temperatures. Moodie told the delegates in Glasgow that the team are also developing 1300 nm PCSELs, and getting "good" results.

Given the location of the workshop – it's in the backyard of Vector Photonics, a pioneer of the PCSEL – an absence of any presentations from the start-up, including any posters, will have raised a few eyebrows, particularly as this company initially had a very public profile. Over its first five years it has undergone major changes, including the departing of two of the four co-founders, including the CEO, as well as a Sales and Marketing Director. While such an upheaval might suggest a company in turmoil, it would be wrong to read too much into these developments. Vector is taking on new staff, with some at the conference, and it is making progress. As efforts are commercially sensitive, this restricts opportunities to details successes, accounting for the restricted engagement in Glasgow.

State of play

The second International Workshop on the PCSEL concluded with a discussion between all delegates on potential stumbling blocks to the commercial success of this laser. There are no major concerns related to the manufacturability of this device, and when its production moves to larger substrates, this will enable the use of better tools that increase yield and performance.

Proving reliability may not been a significant stumbling block either. Initial results are encouraging. As well

The biggest issue facing the PCSEL is what will be its 'killer' application. But rather than identifying this, maybe there's a need to walk before running – that is, find a market that will allow a ramp to relatively modest volumes, providing a platform to targeting bigger successes.

A converted church, now known as Òran Mór, provided the setting for the conference dinner.

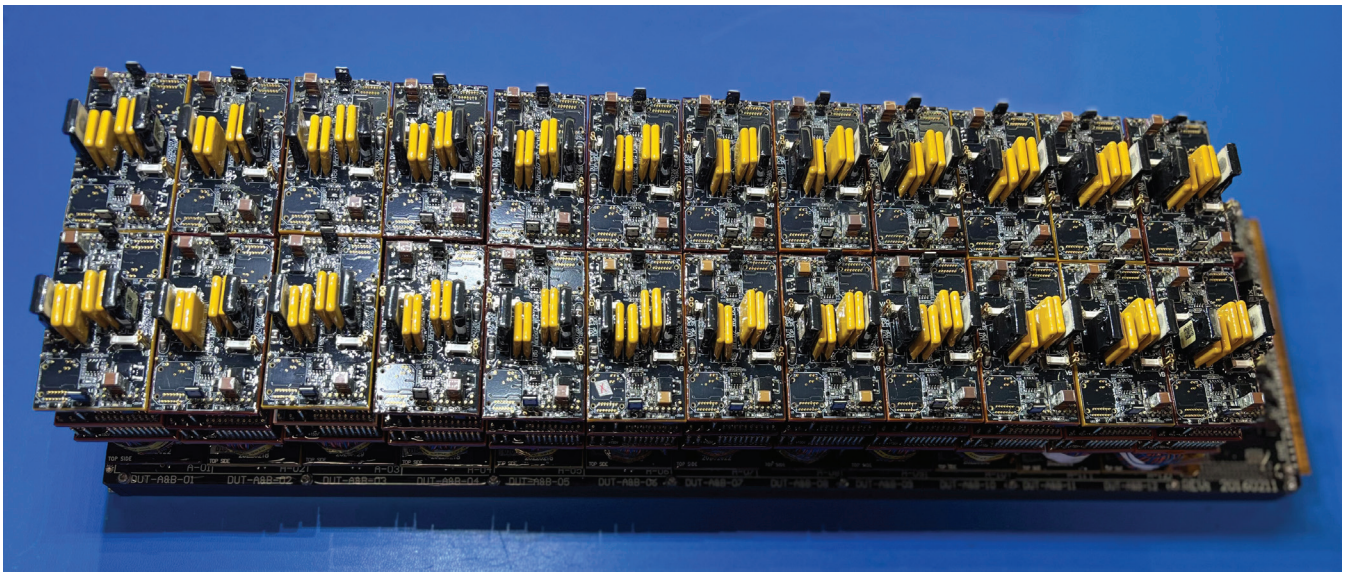
as findings by Sumitomo, already described in this conference report, investigations by Changchun Institute of Optics, Fine Mechanics and Physics are encouraging – they determined an extrapolated lifetime of just over 8,000 hours, based on pulsed operation at 25°C (10 kHz, 4.75 ns); and an accelerated aging lifetime test at 85°C using the same pulse conditions led to no obvious degradation over 240 hours, indicating a life span of 3,288 hours. However, there is no standard for lifetime testing, an issue that may hamper commercial success.

In many applications, the wall-plug efficiency is a critical metric. For PCSELs, the best efforts have been around 30 percent. In contrast, for GaAs-based laser diodes, this figure is above 70 percent. For that class of laser, efficiencies increased about 20 years ago, spurred on by a DARPA-funded programme known as SHEDS – super high-efficiency diode sources. This effort, which included identification and quantification of loss mechanisms, provided funding for US companies to increase efficiencies from around 50 percent to 65 percent within 18 months. If successful, further funding followed, for an 80 percent target. Maybe a similar focus on the origins of losses in PCSELs, and addressing them, could spur improvements in this area? Offering hope, Noda revealed that his team have recently delivered a substantial hike in efficiency, with results soon to be published.

The biggest issue facing the PCSEL is what will be its 'killer' application. But rather than identifying this, maybe there's a need to walk before running – that is, find a market that will allow a ramp to relatively modest volumes, providing a platform to target bigger successes.

While a lack of answer to this key question may seem deflating, it's worth noting that many in the audience are industrial researchers. If they have identified a potential market for the PCSEL, why would they share this crucial advance with their competitors?

So, it's possible that when delegates reconvene in 2027 for the third International Workshop on the PCSEL, at least one of the commercial pioneers will be starting to enjoy commercial success with this most promising class of laser, which continues to advance on many fronts.



GaN HEMTs enter SiC territory

Rigorous testing demonstrates the reliability and robustness of commercial 1250 V GaN HEMTs paired with a low-voltage silicon MOSFET to ensure normally-off operation

BY KAMAL VARADARAJAN, ALEXEI ANKOUDINOV, ROBERT YANG, ALEXEY KUDYMOV, BHAWANI SHANKAR, KARTHICK MURUKESAN AND SORIN GEORGESCU FROM POWER INTEGRATIONS

MATERIAL PROPERTIES govern the performance of power devices. And due to the superior properties of GaN, power devices made from this semiconductor are ideally suited for high-efficiency power conversion. Thanks to this, GaN HEMTs are being adopted in increasing number in commercial power-supply designs covering a broad range of applications, where they take advantage of this wide bandgap technology's fast switching capability with low losses.

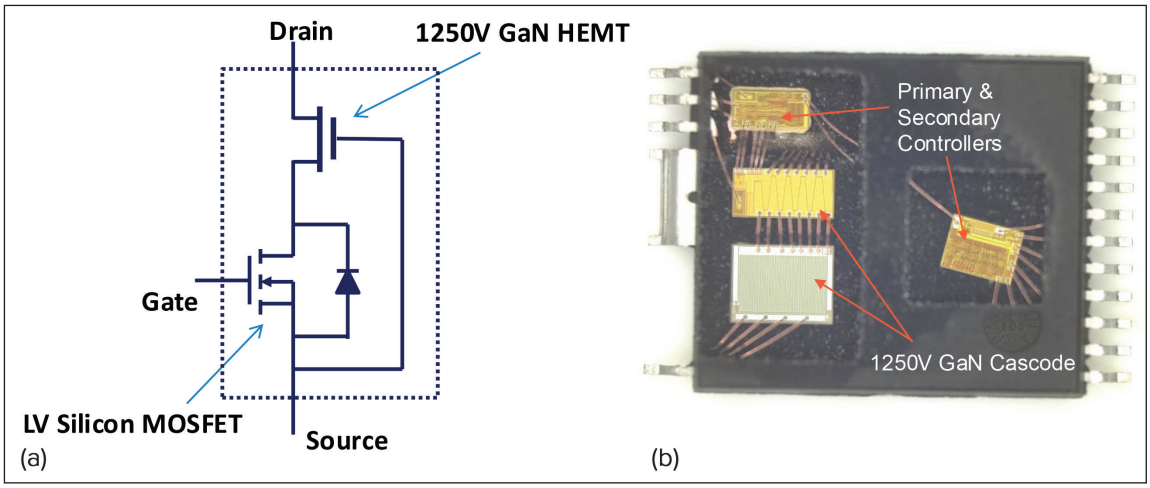
Today's designers have a broad choice, when it comes to the manufacturer of the GaN HEMT, but blocking voltages are limited. Many products on the market operate below 200 V, or in the 600 V - 650 V range. But beyond 650 V, only a few manufacturers have released devices with a rated voltage of 900 V or more. Part of the reason behind this limitation is that GaN HEMT technologies tend to employ silicon substrates, a foundation that hampers scaling to voltages beyond 900 V, due to the need for very thick buffer layers that add significant processing challenges.

Due to this, designers needing wide-bandgap power devices with a rating of 1200 V or more have been constrained to using SiC switches. However, this is an expensive choice, with cost still providing a significant barrier to SiC adoption.

To address this shortcoming, our company, Power Integrations, is breaking new ground by offering high-voltage GaN devices. Our proprietary technology enables extension beyond 900 V purely by device design and with no modification to the underlying epitaxial layer structure. These readily available products are a compelling alternative to SiC at 1200 V and beyond.

If a high-voltage power-conversion switch is to enjoy market success, lower cost and excellent performance has to go alongside reliability. We have devoted much effort on this front, involving high-voltage reliability qualification tests of a 1250 V GaN cascode switch, with a focus on some of the most critical aspects associated with high-voltage evaluation. Read on to discover our findings.

Power supply designers can reliably specify an operating peak drain-to-source voltage of 1000 V when employing a 1250 V GaN cascode device, as this caters for the industry-standard 80 percent de-rating. For industrial applications, this extent of de-rating provides significant headroom, and is particularly beneficial in challenging power grid environments where robustness provides an essential defence against grid instability, surge, and other power perturbations. Another market for the



➤ Figure 1. (a) Circuit schematic for the 1250 V GaN cascode switch. (b) Flyback switcher IC with the 1250 V GaN cascode, primary, and secondary controllers.

1250 V rated GaN switch results from the prevalence of 800 V bus architectures, with this device enabling cost-effective, significant performance improvements in various sub-systems in electric vehicles while providing the derating needed to ensure high system reliability.

A cascode configuration

Our 1250 V GaN HEMT is a normally-on, depletion-mode device. To realise effective normally-off operation, which is essential for safe operation of power electronic systems, it is connected in series with a low-voltage silicon MOSFET in a cascode configuration (see Figure 1 (a), which provides a circuit schematic for the cascode switch, comprising 1250 V GaN and a low-voltage silicon MOSFET). The 1250 V GaN cascode is incorporated as the primary side switch in a flyback switcher IC, which also includes primary and secondary side controllers (see Figure 1 (b)).

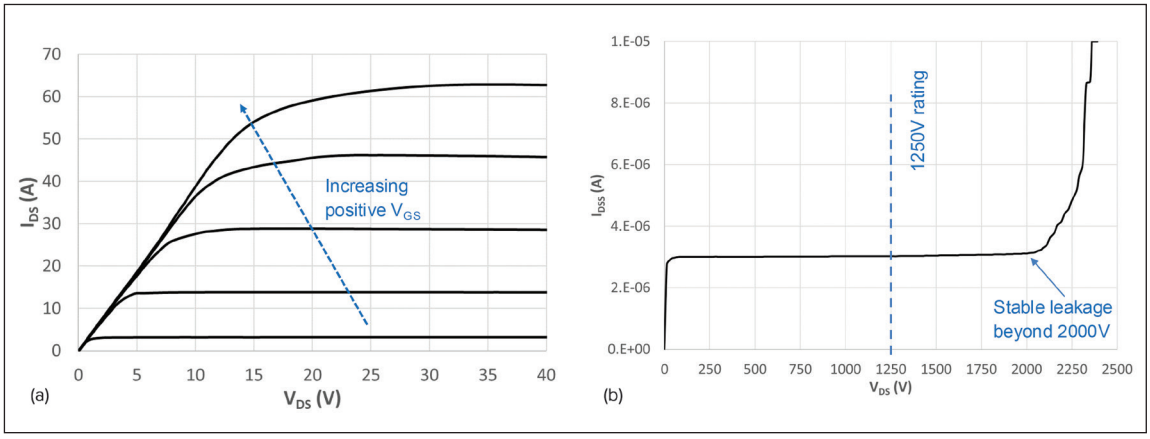
Measurements of pulsed output characteristics of a typical 330 mΩ, 1250 V GaN cascode device demonstrate its high-current capability and device scalability, assets that aid the addressing of high-power applications (see Figure 2 (a)). Our 1250 V cascode devices also exhibits excellent off-state characteristics, with measurements on a typical HEMT showing stable leakage to beyond 2000 V, ensuring excellent transient overvoltage capability (see Figure 2 (b)). This strength shows that our 1250 V devices offer a significant safety margin when compared with silicon and SiC devices with similar voltage ratings.

Ensuring field reliability

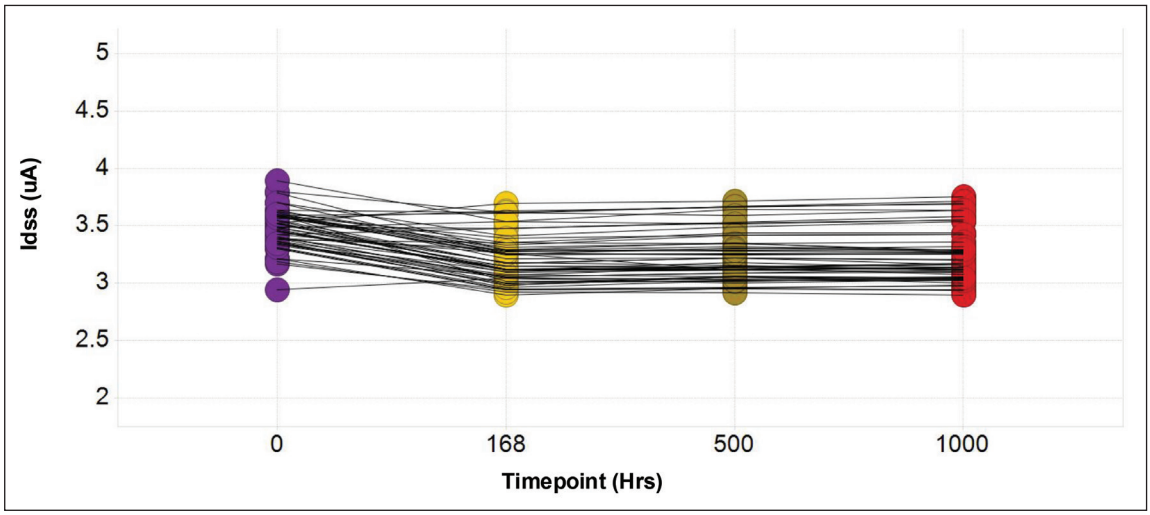
While good on-state and off-state characteristics are valued, they must go hand-in-hand with meeting and exceeding industry-standard reliability qualification requirements, in order to ensure reliable operation in the field. Here we share results meeting this goal, obtained from critical high-voltage reliability stress evaluations, covering both static and dynamic conditions. These tests were performed as part of our qualification of the 1250 V GaN HEMT for power-conversion applications.

One common test is the high-temperature reverse-bias (HTRB) test. This is an off-state reliability stress test that evaluates the long-term stability of the power device under a high drain-to-source bias, with a high temperature employed to accelerate thermally activated failure mechanisms under high electric-fields over an extended period.

We performed the HTRB stress test of our 1250 V GaN cascode device in a 150°C ambient environment, using an off-state drain-source voltage of 1000 V (80 percent of 1250 V rating) for 1000 hours. Our device passed this test, fulfilling all



➤ Figure 2. (a) Output characteristics of a 330 mΩ, 1250 V GaN cascode device illustrating high current capability. (b) Typical off-state characteristics demonstrating leakage remaining stable beyond 2000 V.



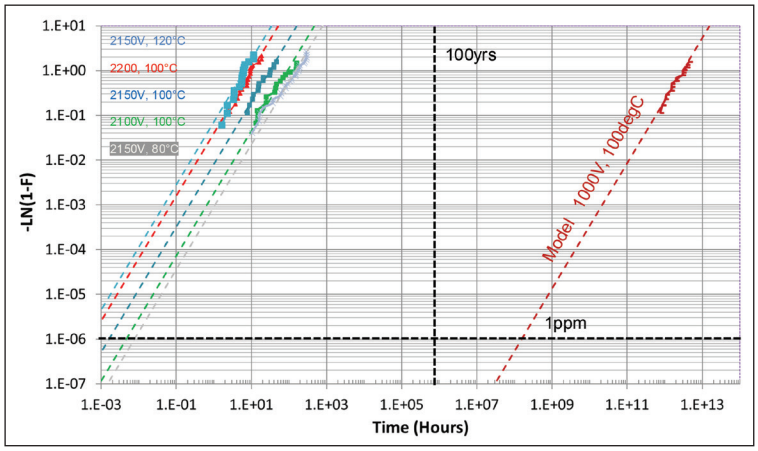
➤ Figure. 3. Stable off-state drain leakage through 1000 hours of high-temperature reverse-bias stress at 1000 V/150 °C.

Voltage / Temperature	80°C	100°C	120°C
2100V		✓	
2150V	✓	✓	✓
2200V		✓	

➤ Table 1. Accelerated evaluation conditions in the off-state.

specifications defined in JEP198 – it is the JEDEC guideline for reverse-bias reliability evaluation procedures for GaN power-conversion devices. One critical parameter to monitor during the HTRB stress test is the off-state drain-to-source leakage current. We observed excellent device leakage stability, validating the suitability of our cascode devices for high-reliability applications at high voltages (see Figure 3).

In addition to the HTRB qualification test, we determined intrinsic off-state failure rates, extracted by running tests on a large number of units under accelerated drain-source voltage conditions (2100 V to 2200 V) across multiple temperatures (80°C to 120°C). Test conditions are shown in Table 1.



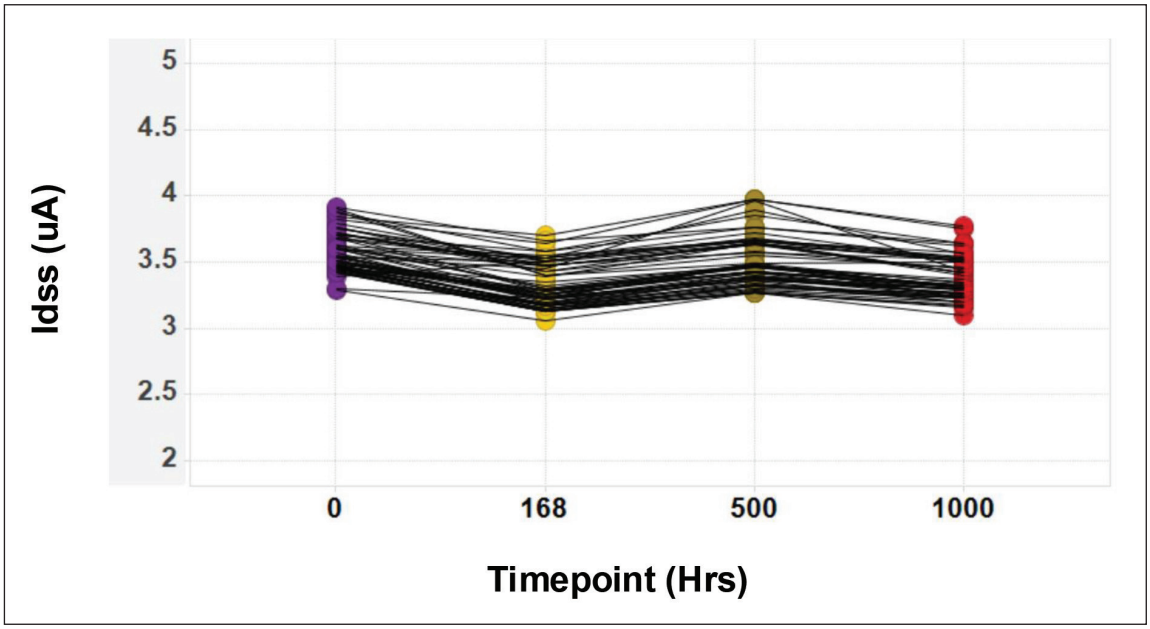
➤ Figure 4. Weibull distributions indicating time-to-failure under multiple accelerated stress conditions and the projected distribution at 1000 V/100 °C.

Based on the time-to-failure Weibull distribution obtained from this set of experiments, we extracted: a voltage acceleration factor, using an exponential model; and a temperature acceleration factor, via an Arrhenius model. These factors enabled a projection of failure rate under typical use conditions. Our model predicts a cumulative failure rate of 1 part per million in more than 15,000 years of operation at 1000 V/100 °C (see Figure 4), indicating a significant built-in reliability margin for our 1250 V GaN cascode power device.

For many high-reliability deployments, such as industrial applications, reliability requirements go beyond just passing the HTRB-based off-state reliability qualification stress test. That's because HEMTs are often exposed to harsh external environmental conditions, where they have to operate continually, or for extended periods of time, in extreme mission-critical applications. In these demanding conditions, it is crucial for HEMTs to pass the HV-H3TRB test, which involves a controlled high humidity environment, an additional stressor to the original HTRB test. This stress test, incorporating additional failure modes produced by moisture penetration, examines all aspects of the device, including its passivation layer, active and termination design, and underlying structures.

We undertook the HV-H3TRB stress test of our 1250 V GaN cascode device in an 85°C ambient environment with a relative humidity of 85 percent, stressing with an off-state drain-source voltage of 1000 V for 1000 hours. These conditions follow JEDEC standard JESD22-A101.

Clean passing results were obtained for this stress test. We paid particular attention to the most critical



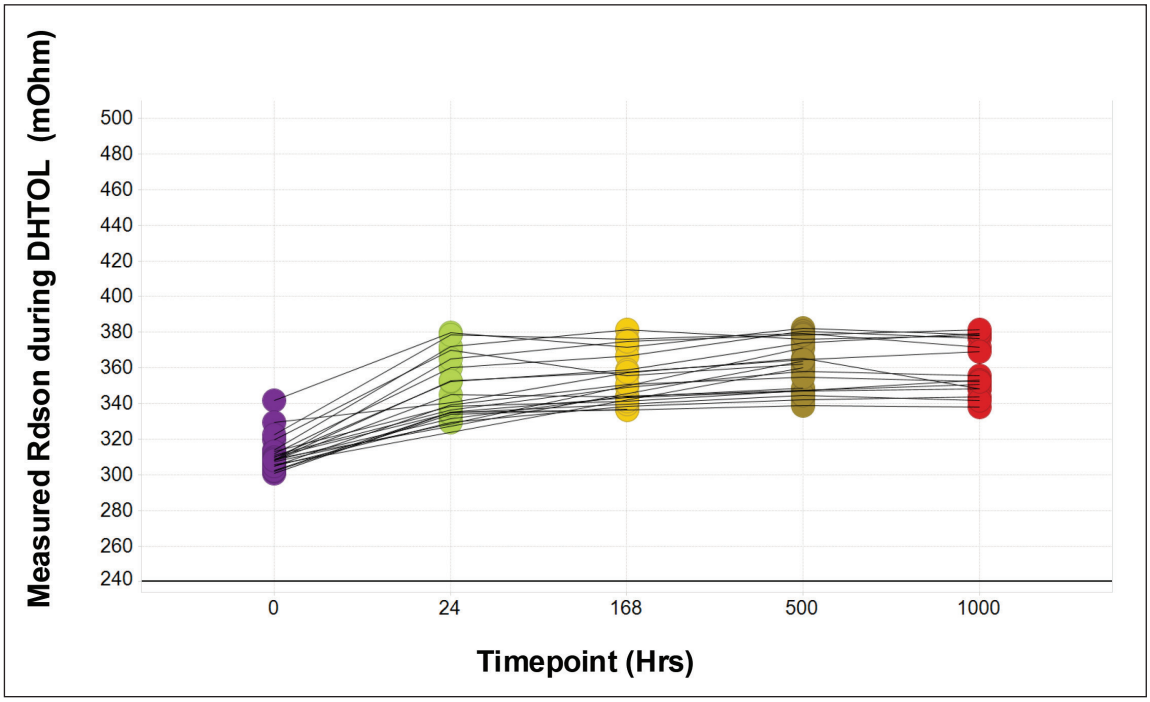
➤ Figure 5. Stable off-state drain leakage through 1000 hours of HV-H3TRB stress at 85 percent relative humidity/85 °C/ 1000 V.

parameter, the off-state drain-to-source leakage current, monitoring this at various times during the HV-H3TRB stress test. Our device exhibited excellent leakage stability, validating its suitability for high-reliability industrial applications (see Figure 5).

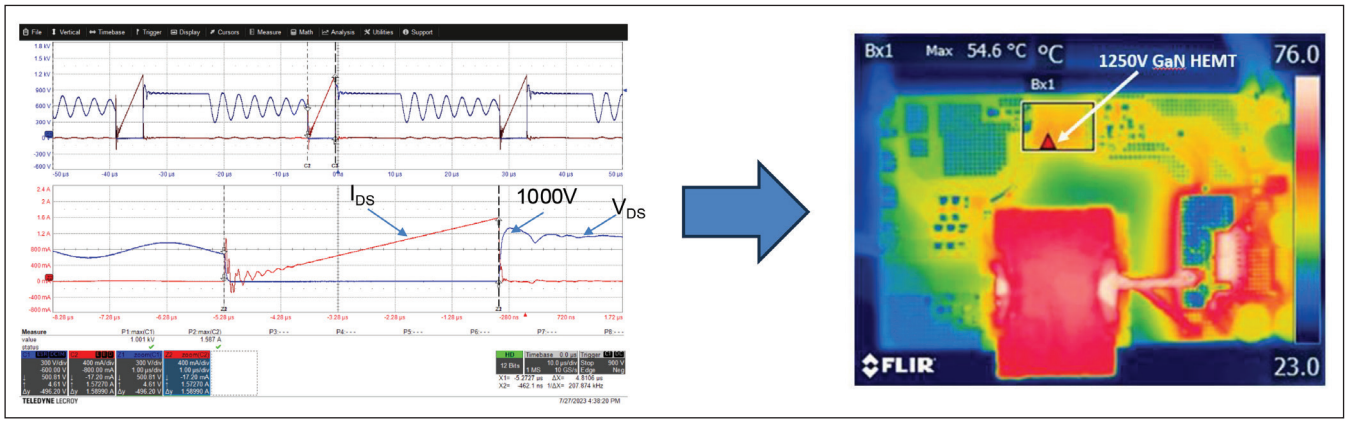
A key concern that initially delayed the commercial introduction of GaN HEMTs by many of its manufacturers is reliability when switching in high-voltage applications. Studies would show that the device's on-resistance increased immediately after turn-on compared with the DC condition. This phenomenon, known as dynamic $R_{DS(ON)}$, is widely attributed to charge-trapping effects within the device under high electric-field strengths. A number of techniques have been employed to address this issue, including epitaxial structure engineering and carefully optimised processing techniques.

In response to the field reliability implication, JEDEC recently introduced a guideline JEP180, detailing dynamic high-temperature operating life (DHTOL) testing. This document specifies switching reliability evaluation procedures for GaN power-conversion devices.

Using the JEP180, we evaluated switching reliability of our 1250 V GaN cascode in a custom testbed with the capability to evaluate multiple units in parallel at 125°C. For this test we employed the most stringent operating conditions – hard-switched turn-on and turn-off at 1000 V – based on the



➤ Figure 6. Stable $R_{DS(ON)}$ observed during 1000 hours DHTOL with minimal shift (less than 20 percent).



➤ Figure 7. (a) Steady-state switching waveform illustrating 1000 V Peak V_{DSv}. (b) Steady-state thermals indicating temperature rise below 30 °C during continuous switching and a $V_{DS(PK)}$ of 1000 V.

switching locus described in JEP180. The dynamic $R_{DS(ON)}$ during high-voltage switching is of particular interest. Improperly designed GaN HEMT devices tend to exhibit a significant increase in $R_{DS(ON)}$ during high-voltage switching transitions due to additional electron trapping, which can have a detrimental effect on the converter efficiency, or in extreme case, result in hard failure.

We have monitored variations in the $R_{DS(ON)}$ of our 1250 V GaN cascode over the course of 1000 hours of DHTOL stress at 1000 V, a peak current of 2 A, and a junction temperature of 125°C. This test shows stable performance from the earliest timepoint, with a minimal shift of less than 20 percent (see Figure 6). It's a degree of stability that's on par with state-of-the-art 650 V GaN HEMTs tested under similar hard-switching conditions.

A key implication of this result, and the others described in this article, is that GaN HEMTs can be scaled to more than 1200 V without any compromise in performance, including critical hard-switching capability. Rigorous testing demonstrates their robustness to meet all potential high-reliability use cases.

A real-life application

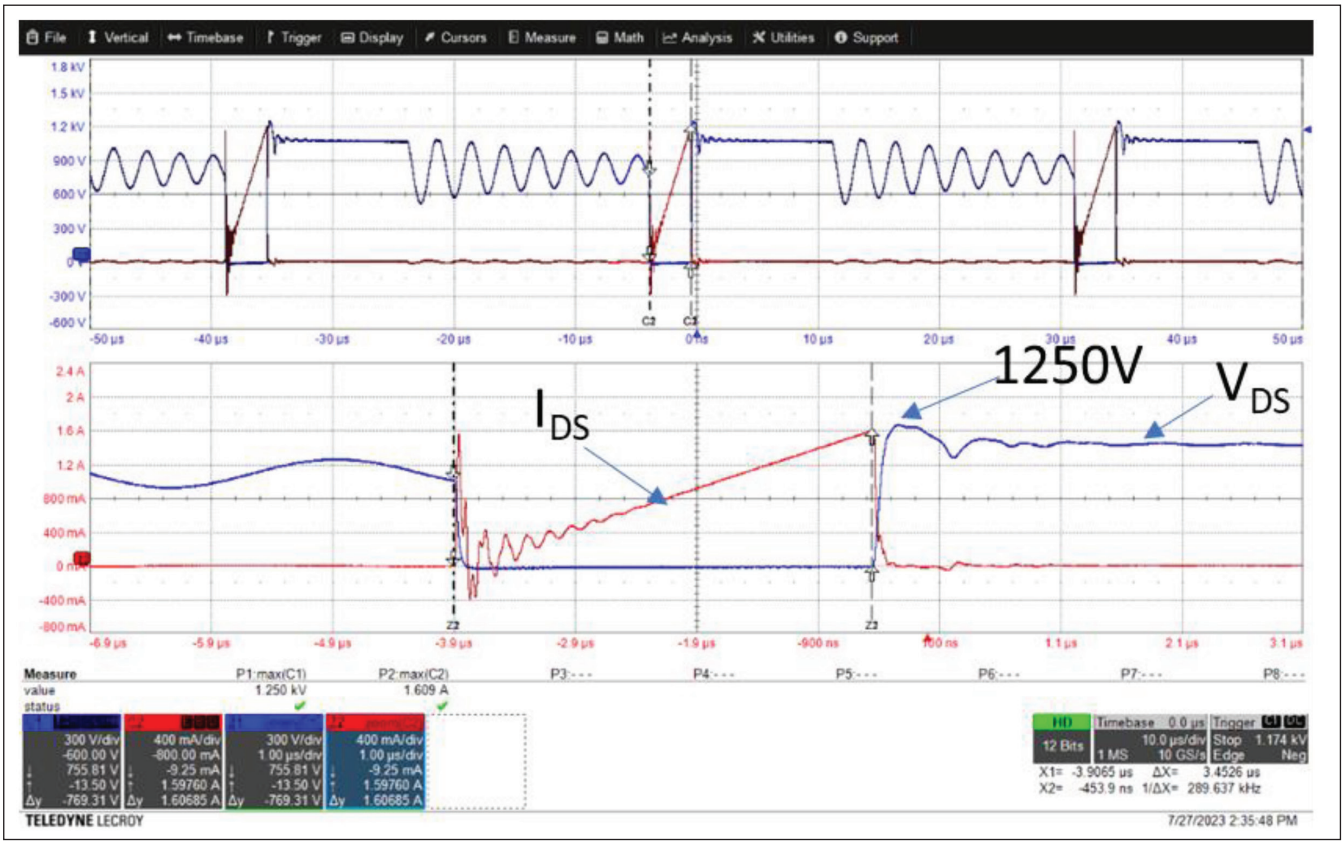
To highlight the capability of our 1250 V GaN HEMT in real-life applications, we have deployed this device in a 60 W, 24 V/2.5 A flyback power supply, built using the switcher IC (see Figure 1 (b)). By evaluating the steady-state operation of the flyback power supply running at a peak drain-source voltage of 1000 V, we confirmed stable operation with corresponding switching waveforms (see Figure 7 (a)).

Measurements have determined low, stable operating temperatures for the power supply, realised without any external cooling over long periods of continuous operation, with a peak drain-source voltage of 1000 V. This is an encouraging result, validating the minimal magnitude and effect of the shift in $R_{DS(ON)}$ during DHTOL stress evaluation. The maximum temperature of the 1250 V GaN HEMT remained below 55°C (see Figure 7 (b)), indicating a temperature rise of only 30°C in this application compared to ambient.

While the GaN cascode is designed to operate with a peak drain-source voltage below 1000 V in a continuous mode, it can accommodate momentary increases in supply voltage up to a peak of 1250 V. This transient voltage capability allows the GaN cascode to continue to switch through the surge event for short periods without suffering a hard failure. We demonstrated this attribute by increasing the input voltage until the peak drain-source voltage during switching reached the maximum rated value of 1250 V without running into any abnormal operation (see Figure 8).

As well as being extremely robust, the flyback

While the GaN cascode is designed to operate with a peak drain-source voltage below 1000 V in a continuous mode, it can accommodate momentary increases in supply voltage up to a peak of 1250 V. This transient voltage capability allows the GaN cascode to continue to switch through the surge event for short periods without suffering a hard failure



➤ Figure 8. Switching waveform illustrating transient overvoltage capability up to a peak V_{DS} of 1250 V.

power supply designed with the 1250 V flyback switcher IC operates with a best-in-class full-load efficiency exceeding 92 percent at a 700 V input (see Figure 9).

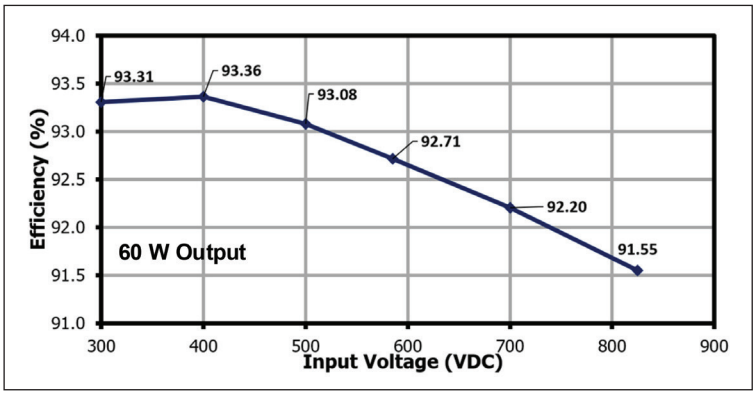
High-voltage GaN HEMT roadmap

Our work demonstrates the capability of 1250 V GaN HEMTs as a credible alternative to SiC. We also offer flyback switcher IC products based on a 1700 V GaN HEMT, clearly establishing that our technology can be scaled to even higher voltages.

With our proprietary and improving GaN HEMT technology, particularly suited to ultra-high voltages, devices with ratings beyond 2000 V that are currently catered for by SiC are now within close reach. For power supply designers, the portfolio of reliable, alternative wide-bandgap power switch is expanding.

Though lateral GaN device structures have a fundamental limitation in matching the specific-on-resistance – that's the on-resistance per unit area – of vertical devices, it is possible to significantly increase power levels through improvements in packaging and thermal management.

When higher switching frequencies, improved efficiency, high reliability and lower costs compared with SiC are factored in, high-voltage GaN HEMTs are compelling candidates in industrial, data centre, automotive and other high-reliability applications over a wide power range.



➤ Figure 9. 1250 V GaN-based flyback power supply efficiency versus input voltage.

FURTHER READING

- K. Varadarajan *et al.* " Reliability Qualification of 1250 V Lateral GaN HEMTs for High Reliability Industrial Applications," IEEE International Reliability Physics Symposium proceeding, 3A2.1-3A2.6 (2025)
- K. Varadarajan *et al.* "Reaching Beyond 1200 V: Lateral GaN HEMTs for High-Reliability EV and Industrial Applications" PCIM Europe proceeding, 1593-1598 (2024)
- K. Murukesan *et al.* "State of the Art 1.7 kV Lateral GaN HEMTs, an Alternative to SiC", IEEE Applied Power Electronics Conference proceeding, 180-184 (2025)

ANGELTECH

CS INTERNATIONAL CONFERENCE

20-22 APRIL 2026
BRUSSELS
BELGIUM

CONNECTING, EDUCATING & INSPIRING THE COMPOUND INDUSTRY

CS INTERNATIONAL is part of the AngelTech series of events, which has produced for over 16 years, a portfolio of insightful, informative, and highly valued chip-level conferences.

Attracting more than 800 delegates and 80+ exhibitors consisting of co-located Advanced Packaging, PIC International, and PE International, plus a single exhibition area, delegates can dip in and out of every session to put together their own tailor-made programme by selecting from over 130+ invited talks, delivered by leaders of the most innovative global companies of today.

With a significant overlap between the three conferences, attendees and exhibitors are exposed to the full relevant supply chains and customer and supplier bases.

Key Themes for 2026

Growing revenues in GaN Power Electronics
Sales of GaN transistors are tipped for tremendous growth throughout this decade and beyond. But what are the optimum strategies for exploiting this opportunity?

microLEDs: How to gain market traction
The potential of the microLED is beyond question. But what's needed to ensure that this miniature marvel starts to generate significant sales?

Revitalising the SiC industry
With profit margins shrinking, makers of SiC devices cannot rest on their laurels. But what are the key innovations to ensure success, in terms of production processes, fab operations and new device architectures?

Advancing surface-emitting optoelectronics
What's needed to increase the spectral range and speed of the VCSEL, so it can target new applications? And how can the performance of PCSELs and UV LEDs improve, to drive their commercial success

Unlocking the potential of ultra-wide bandgap materials
Offering some tremendous characteristics, ultra-wide bandgap materials are poised for success. But which one is going to have the biggest impact? Will it be AlN? Or diamond? Or one of the oxides?

ANGELTECH

CS INTERNATIONAL CONFERENCE | PIC INTERNATIONAL CONFERENCE | PE INTERNATIONAL CONFERENCE | AP INTERNATIONAL CONFERENCE | AIS ANGELTECH INNOVATE SUMMIT

Sponsorship / Exhibition / Speaker OPPORTUNITIES AVAILABLE!

Sponsorship, exhibition, and speaker opportunities at CS International, enable and empower you to educate and penetrate compound semiconductor industry using a plethora of marketing tools.

Demand is high, with sponsorship, exhibition and speaking slots already being secured for 2026, so to avoid disappointment, please get in touch today.

SPECIAL Event Discount:

10% OFF

Register before 31 January 2026 and get 10% OFF!

Registration to AngelTech allows you to access both days of **CS International, PIC International**, **Advanced Packaging** and **PE International.**

SPONSORS

PLATINUM

AIXTRON | BRUKER | DCA INSTRUMENTS | EBNER GROUP Driving Green Technologies | EVG | Malvern Panalytical | RAITH NANOFABRICATION | Rigaku | siconnex | ThermoFisher SCIENTIFIC | Veeco

GOLD

ANNEALSYS | CS CLEAN SOLUTIONS | CS connected | FerroTec | spm | vistec Electron Beam

STARTUP

InPHRED

OPENING RECEPTION

EPIC

REGISTRATION

LUCEDA PHOTONICS

LANYARD

Lam RESEARCH

MEDIA PARTNERS

CS COMPOUND SEMICONDUCTOR | Microwave Journal | PIC PHOTONIC INTEGRATED CIRCUITS | SEMICONDUCTOR DIGEST | SIJ

SUPPORTING PARTNER

LAPMASTER WOLTERS

ORGANISERS

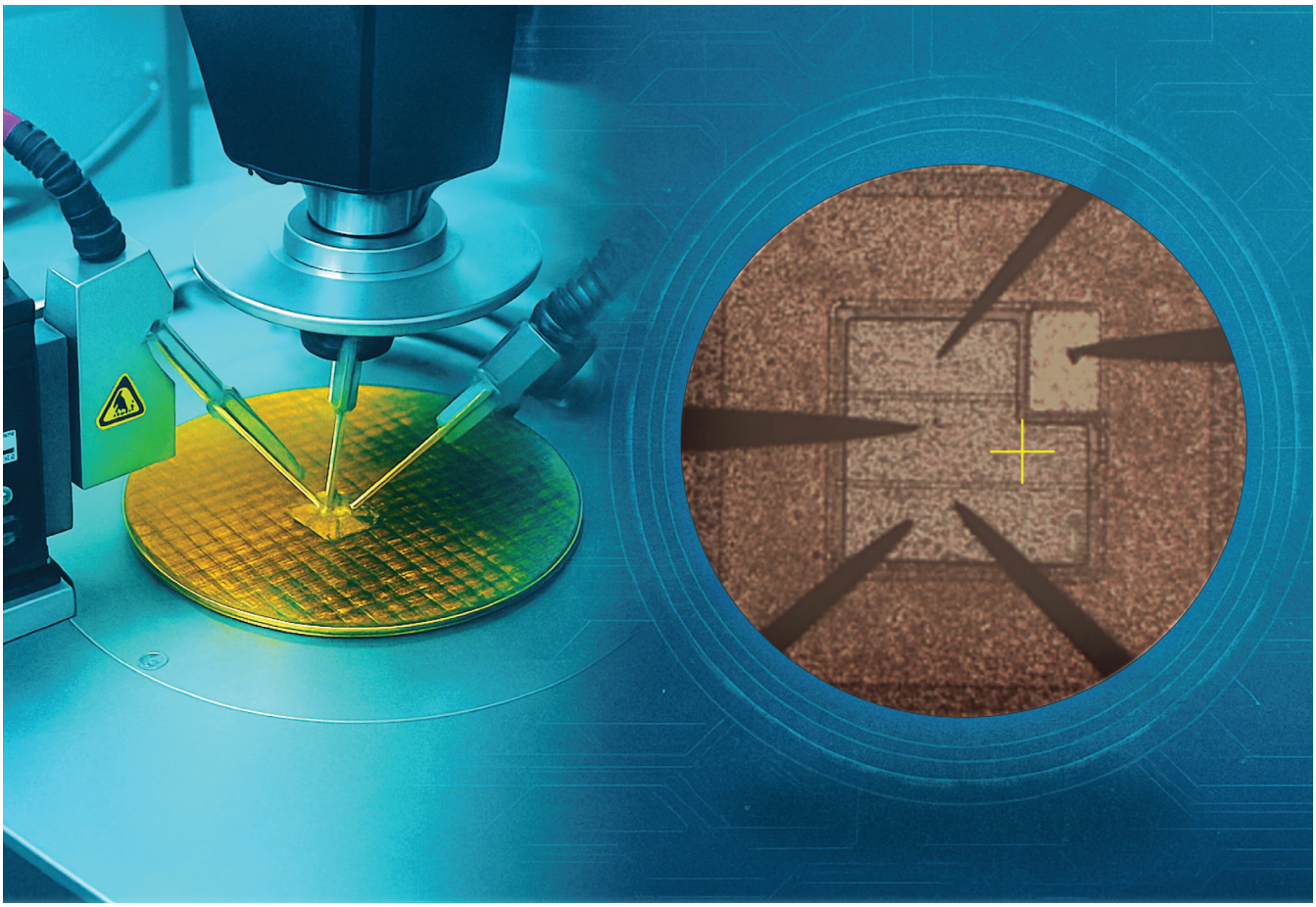
Angel BUSINESS COMMUNICATIONS | ANGEL EVENTS

To find out more about our sponsor and speaker opportunities, contact us today on:

+44 (0) 2476 718970
info@csinternational.net
csinternational.net

ORGANISED BY

Angel BUSINESS COMMUNICATIONS | ANGEL EVENTS



Driving the electric revolution with SiC IGBTs

FOR²ENSICS, an EU-funded initiative, is targeting the simplification of medium-voltage DC converters with ultra-high-voltage SiC IGBTs

BY NAZARENO DONATO, UNIVERSITY OF CAMBRIDGE

THE GLOBAL DRIVE to trim carbon emissions and reach climate neutrality is rapidly transforming electricity supply and grid infrastructure. Critical to succeeding in this endeavour is the introduction of a new generation of power devices, delivering higher efficiencies at reduced costs, through a smart combination of reduced epitaxial layer thickness and a smaller form factor.

One promising route towards this goal is DC distribution, well matched to renewable sources and modern loads, such as solar arrays and battery systems, which already operate in DC. But the power electronics market still lacks low-cost, compact, high-performance DC-to-DC converters that are capable of handling voltages from below 1.5 kV to well over 10 kV.

Aiming to close that gap with a commercial-grade DC-to-DC converter featuring a medium-voltage stage based on ultra-high-voltage SiC IGBTs is our Horizon Europe-funded project entitled Future Oriented Renewable and Reliable Energy SiC Solutions (FOR²ENSICS). By turning from series-connected medium voltage (1.2 kV - 6.5 kV) SiC MOSFETs or silicon IGBTs to ultra-high-voltage SiC IGBTs, we promise to unleash a number of key benefits, including lower conduction losses, simpler drive requirements, a smaller footprint and reduced costs. However, delivering such technology demands coordinated expertise in device fabrication, passivation, packaging and converter assembly – goals realised by a joint effort, drawing on a broad range of expertise from industry and academia.

SiC IGBT technology

Silicon-based IGBTs have long been a mainstay in traction, industrial, automotive and high-voltage DC systems, typically operating from 900 V to 6.5 kV. Their bipolar conduction helps overcome MOSFET limitations, improving the trade-off between the static voltage drop and turn-off losses.

With the arrival of 4H-SiC unipolar devices in the 1.2 kV -3.3 kV range, silicon IGBTs – still extremely

cost-competitive – are losing ground in medium-voltage applications. However, for 6.5 kV and beyond, SiC MOSFETs are up against scaling and cost limits, even with superjunction concepts. On one hand, yield and defect density limit the maximum achievable die area; on the other, scaling of the drift region resistance makes the SiC MOSFET less suitable for medium- to high-current applications.

For ultra-high-voltage applications – that's more than 10 kV – operating at moderate switching frequencies of tens to hundreds of kilohertz, the SiC IGBT offers a compelling alternative. Its advantages include avoiding some of the drawbacks of series-connected SiC MOSFETs, which are more susceptible to voltage imbalance and require more complex gate driving. In addition, SiC IGBTs benefit from a reduced drift-region thickness, compared with their silicon siblings. This gives the SiC IGBT a fundamental advantage, resulting from a lowering of stored charge that ensures reduced switching losses.

Enjoying the benefits of the SiC IGBT is not easy, as its design brings significant challenges, due to intrinsic material constraints. One issue is the higher forward voltage drop, stemming from a delayed bipolar turn-on. This drop – measured at room temperature it's 2.8 V for 4H-SiC, versus 0.7 V for silicon – leads to increased conduction losses at low and medium currents. The other noteworthy drawback is the limited minority-carrier lifetime – only recently extended into the microsecond range – that reduces the benefits of bipolar conduction when the diffusion length is smaller than the drift region thickness. The peak minority-carrier lifetime achieved in the last ten years also limits the maximum drift-region thickness between 100 μm to 200 μm, placing the optimal performance window between 10 kV and 20 kV – the target range for our FOR^{2}ENSICS project.

The backside processing conundrum

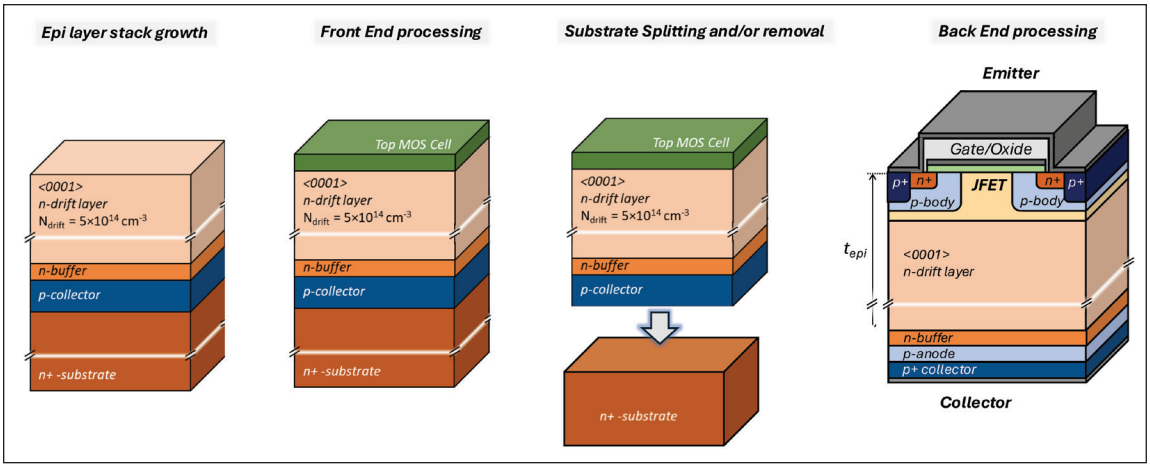
Manufacturing *n*-type SiC IGBTs for ultra-high-voltage applications is a non-trivial task. Challenges arise, due to the absence of high-quality *p*-type SiC substrates, and the need for thick, high-quality epitaxial layers to support blocking voltages beyond 10 kV. In recent years, researchers have explored different fabrication routes, like the flip-type process – this involves removing the n^+ substrate and forming the device channel and the gate oxide on the carbon face – alongside careful process and design optimisation. However, this promising route is yet to yield a commercial SiC IGBT, largely due to cost and performance constraints (as well as mechanical stability).

Our project is pursuing a more streamlined approach, which retains the thick epitaxial layer and substrate throughout processing. Starting with an n^+ substrate, our flow involves forming a highly doped *p*-type collector, adding a buffer layer, growing the epi, and then fabricating the top MOS cell. Backend processing includes substrate splitting or removal – using a combination of back grinding, chemical mechanical polishing and etching – to enable either reuse of the substrate (laser cut achieved through Kabra split or similar methods) or backside access (see Figure 1), prior to metallisation.

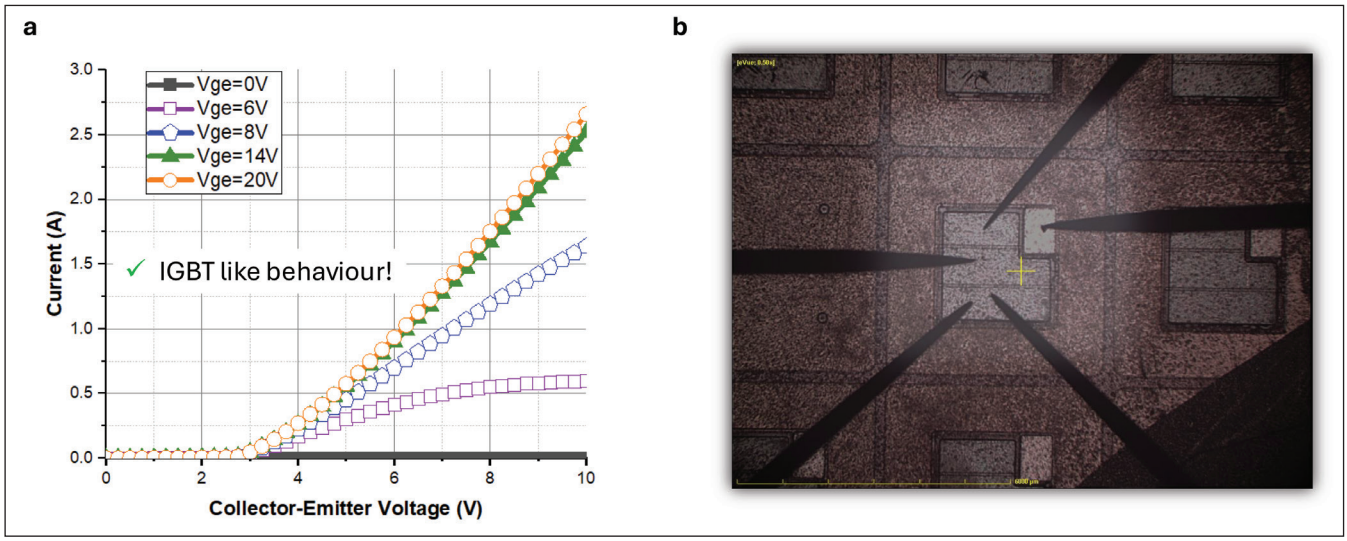
The consortium

FOR^{2}ENSICS is a Horizon EU-funded project that runs for four years, from January 2023 to December 2026. This effort is organised into eight work packages. The project brings together a consortium of leading European institutions and renowned semiconductor companies, each contributing complementary expertise to the development of disruptive ultra-high-voltage semiconductor devices and technologies. The overarching aim is to place European industry at the forefront of the energy transition, competing with efforts from semiconductor supply chains in the US and Japan.

Consortium members include: CSIC (Spain, coordinator), Coherent Corp. (Sweden), University of Cambridge (UK), Hitachi Energy (Switzerland), Deep Concept (France), University of Bremen (Germany), EPFL (Switzerland), and SuperGrid Institute (France). Together, these partners cover the full spectrum from materials and device design to packaging, system integration, and testing.



➤ Figure 1. Schematic process flow for the fabrication of ultra-high-voltage SiC IGBTs.



➤ Figure 2. (a) IGBT characteristics prior to thick metal deposition and (b) a microscopic image of the IGBT under test in the Henry Royce High Voltage Characterisation Suite (Cambridge University).

Early trials have delivered encouraging results, indicating that our approach is a viable manufacturing route. Our first batch of SiC IGBT devices is currently under test, with preliminary results show promising gate modulation and successful backside substrate removal (see Figure 2).

In parallel, we are producing SiC MOSFETs rated at 3.3 kV, 10 kV and 15 kV to benchmark against our IGBTs in a DC-to-DC converter dual-active-bridge demonstrator.

Leading this high-voltage SiC device fabrication effort are our consortium members at The University of Cambridge, Coherent, CNM and Hitachi Energy.

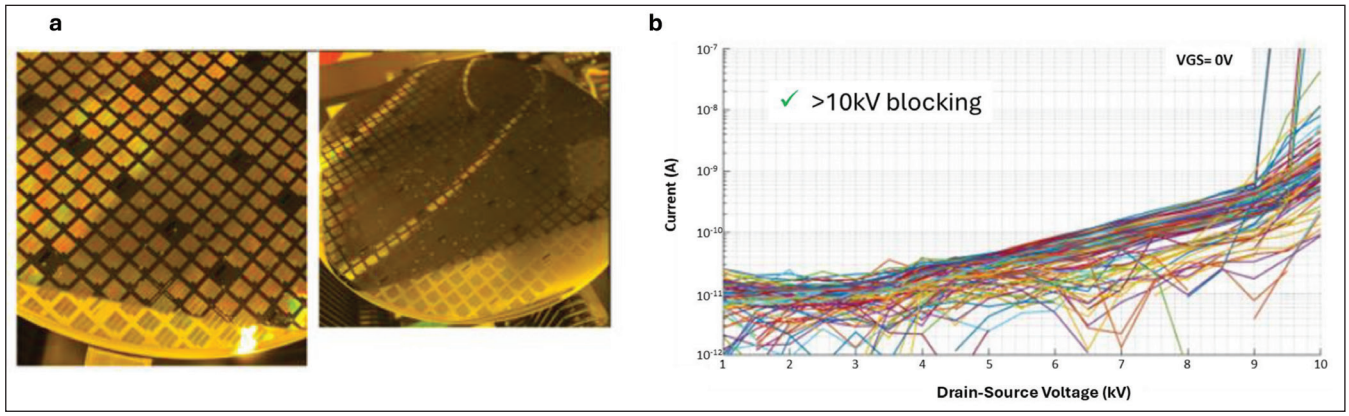
Edge termination design

For ultra-high-voltage SiC devices with ratings above 10 kV, it is critical to employ an efficient edge termination. Conventional termination designs capable of withstanding such voltages tend to require large die areas – and that's a costly design solution when working with epiwafers over 100 μm-thick that must deliver tens of Amps. The aim is to minimise the termination footprint while maintaining robust blocking performance and avoiding any compromise to passivation and oxide reliability.

Testing of a SiC MOSFET platform has already demonstrated edge terminations capable of blocking more than 10 kV during on-wafer measurements (see Figure 3). We have also developed a new test platform for packaged devices that evaluates up to 20 kV, along with a double-pulse test system operating above 10 kV using a dedicated DC supply. The next stage is to prove these termination concepts on IGBTs.

Packaging and reliability

To unlock the full potential of high-voltage SiC technology, packaging must combine electrical performance with long-term reliability at 15 kV. Our package design uses high-field passivation and gel materials to withstand extreme voltages, temperatures and humidity without degrading device performance. This package supports both the integration of high-voltage SiC MOSFETs



➤ Figure 3. (a) Photo of 10 kV SiC MOSFET wafer and (b) wafer-level forward-blocking characteristics for MOSFETs implementing D3 termination design, measured at room temperature with a gate-source voltage of zero.

and IGBTs (in parallel or series connection) with a high-voltage SiC diode – a MOSFET in diode mode – providing wide flexibility for all the devices manufactured within the project.

A PCB mezzanine within the module carries integrated passive components, such as gate driver resistors, a negative-temperature-coefficient sensor and an RC snubber (see Figure 4 (a)). Leading this work are Deep Concept and the SuperGrid Institute.

We have used a number of standard approaches to evaluate reliability. They include high-temperature reverse-bias tests, investigation of time-dependent dielectric breakdown and the high-humidity, high-temperature and high-voltage reverse-bias test. Results confirm the robustness of our high-voltage SiC IGBTs. In addition, there's a multi-die test platform for bipolar degradation studies – capable of testing up to 16 devices in parallel – that's now operational at the University of Bremen.

Gate drivers and converters

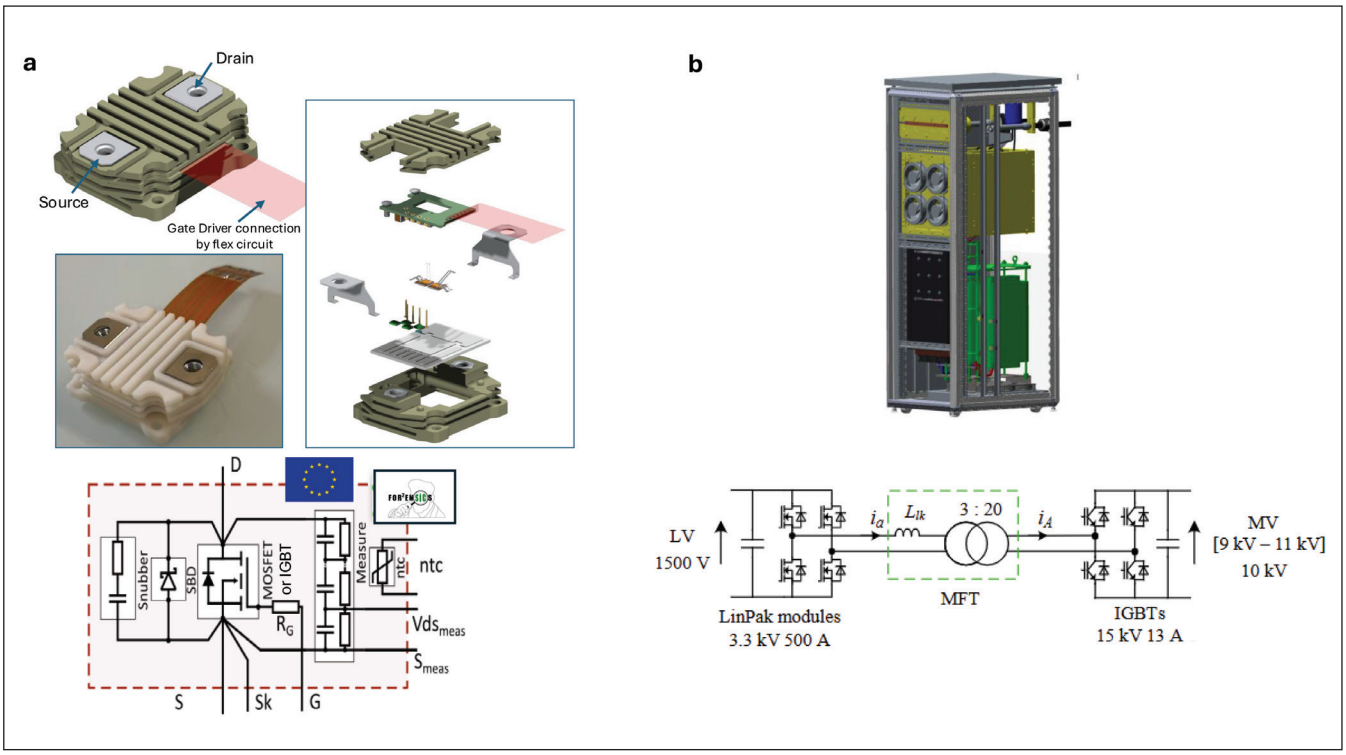
A major demonstration target for our project is the dual-active-bridge converter, selected for its efficiency and adaptability in medium-voltage DC applications. The first prototype, showcased this November at the SuperGrid Institute in Lyon, uses a series-connected 3.3 kV SiC MOSFET (see Figure 4 (b)). This platform serves as our baseline for a follow-up demonstrator in 2026, using the project's 15 kV SiC IGBTs.

Our single-phase dual-active-bridge converter comprises two full bridges – one connected to the low-voltage bus, designed with LinPak SiC MOSFETs from Hitachi Energy; and the other to the medium-

Upcoming events and demonstrators

KEY upcoming milestones for the FOR^{2}ENSICS project include the medium-voltage DC converter demonstrator, using series-connected SiC MOSFETs. After showcasing this at the SuperGrid Institute in Lyon in November 2025, a follow-up system demonstrator based on SiC IGBTs will take place in 2026 to mark the end of the project. The consortium will also host a Summer School on Power Semiconductors in Cambridge, UK, in 2026, aimed at training the next generation of researchers with a series of talks on power devices and electronics from worldwide experts. Results from the project have been presented at the ECPE Workshop in Lyon in November 2025.

All these events welcome participation from PhD students and postdoctoral researchers, including those from EU sister projects AdvanSiC and SiC4GRID. These gatherings can foster knowledge exchange across the European power semiconductor community.



➤ Figure 4. (a) Ultra-high voltage packaging concept for SiC IGBT and (b) dual active bridge demonstrator.

voltage bus – linked through a medium-frequency transformer. The converter benefits from the opportunity to operate at elevated switching frequencies of tens of kilohertz, because it is not tied to the grid's 50/60 Hz. Thanks to this freedom, the convertor can operate at a higher power density and be constructed from smaller passive components.

Moving to ultra-high-voltage SiC devices on the medium-voltage side also demands advanced gate driver technology. As well as translating control signals into required drive levels, the driver has to handle short-circuit events, limit over-voltage, and employ active Miller clamping to avoid parasitic turn-on. For series-connected switches, it's also critical to ensure precise voltage sharing during static and dynamic conditions. Fulfilling all these requirements enables the design to integrate voltage-balancing measures alongside tuned gate resistances. Leading this work are EPFL and the SuperGrid Institute.

Features of our dual-active-bridge converter include galvanic isolation of the gate driver's power supply, employed to withstand high common-mode transients, and a layout that's optimised to minimise parasitics that could impair superior switching performance. Together, these design choices ensure that the converter exploits the high efficiency and robustness of ultra-high-voltage SiC devices, and provides a strong platform for validating SiC IGBTs in demanding medium-voltage DC systems.

Next steps

As the project enters its core phase, with new IGBT devices emerging from the fab and packaging activities underway, our consortium is moving into a more mature stage of development. Our recent research efforts have focused on making additional improvements to backside metallisation contact resistance and substrate removal, as well as developing multi-die packaging solutions – connecting up to four devices in parallel – to meet the higher current requirements of the final dual-active-bridge demonstrator. We are also progressing modelling and simulation activities in parallel, efforts that will help enhance IGBT performance in upcoming batches, particularly in terms of current capability and temperature coefficient.

Successful proof-of-concept demonstrations at both the device and system levels have encouraged our consortium to pursue new ideas. They include: advanced device concepts, such as reverse-conducting SiC IGBTs; further reductions in the edge termination footprint; novel packaging approaches, using ultra-high-field-strength passivation materials; and the development of larger active areas, as yields continue to improve. If you want to say informed, follow the project updates on our website and social media platforms.

FOR²ENSICS has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No 101075672.

FURTHER READING

➤ https://for2ensics.imb-cnm.csic.es/ (FOR²ENSICs webpage)

Low-pressure CVD of Ga_2O_3: Growth and beyond

Advances in low-pressure CVD-based growth of Ga_2O_3 and its *in-situ* etching address two critical bottlenecks: high-quality, high-growth-rate films; and damage-free patternability

BY ANHAR BHUIYAN FROM UNIVERSITY OF MASSACHUSETTS LOWELL

THE WORLD of power electronics is undergoing a radical transformation. Silicon's long reign is nearing its limit and wide and ultra-wide bandgap semiconductors are taking centre stage, thanks to a number of strengths that include the capability to withstand high electric fields, switch at higher frequencies, and survive harsh environments.

At the forefront of this revolution is gallium oxide (β-Ga_2O_3), an emerging oxide semiconductor with an ultra-wide bandgap of 4.8 eV and a breakdown field exceeding 8 MV cm^{-1}.

These are incredibly impressive numbers – they representing orders-of-magnitude advantages in power density and efficiency over not just legacy materials like silicon, but also the two leading wide bandgap champions, GaN and SiC.

Yet, for all its promise, Ga_2O_3 is still navigating the hurdles of real-world, scalable adoption. Its distinct material properties and complex crystallographic structure have introduced nuanced barriers that challenge conventional process strategies – especially when it comes to materials engineering at scale.

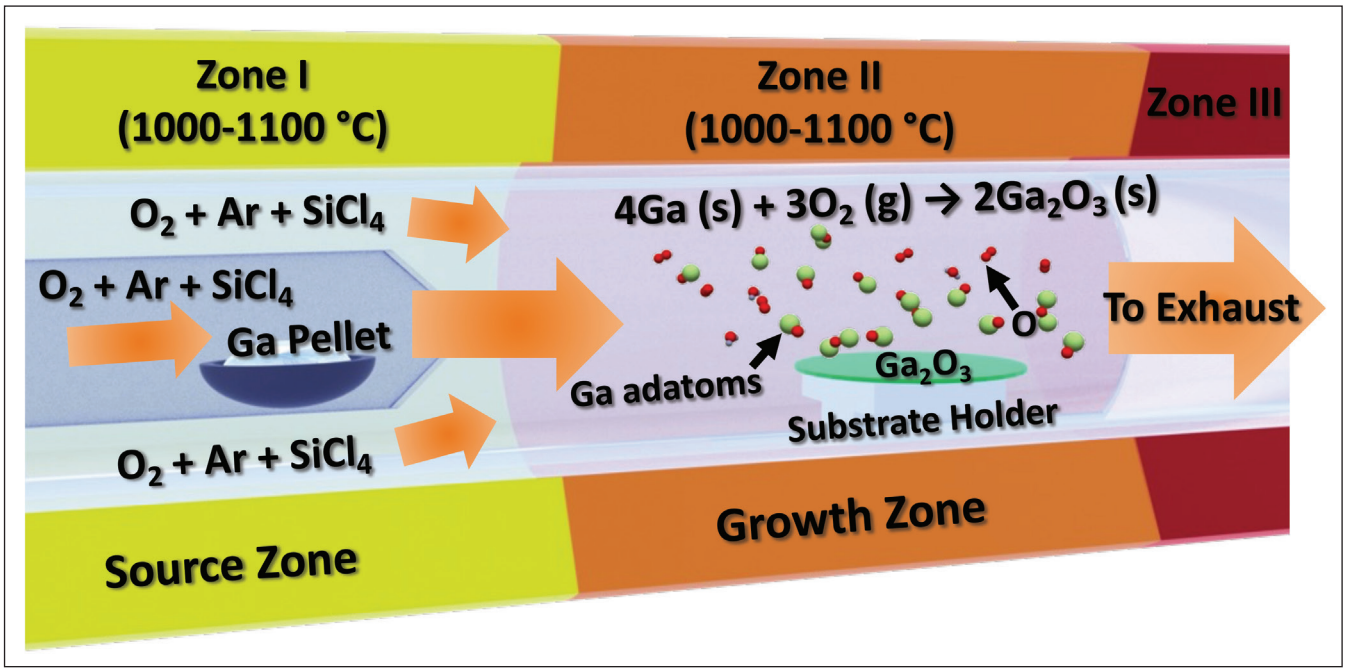
Two of the most persistent obstacles that are stopping this oxide from fulfilling its promise are growth and patterning.

On the growth side, it's a formidable challenge to produce thick epitaxial layers with a low background doping and smooth surface morphology, traits that are crucial for the construction of vertical power devices. A high mobility, a smooth surface and a high growth rate rarely go hand-in-hand, and managing impurity incorporation at scale is far from trivial.

The other obstacle occurs on the processing side – etching Ga_2O_3 into precise three-dimensional architectures is a major bottleneck. Etching, in essence, is the controlled removal material to allow flat layers to be shaped into vertical devices with trenches, mesas, and other critical three-dimensional structures. It is as important as growth itself, because without well-defined etch steps, it's impossible to realise advanced device geometries.

Unfortunately, Ga_2O_3, with its anisotropic and complex monoclinic crystal structure, is notoriously difficult to etch with precision. Different crystal planes respond very differently to chemical or plasma environments, leading to rough sidewalls, undercutting, or material damage.

While conventional plasma-based dry etching can define vertical features, this comes with collateral damage – oxygen vacancies, deep trap states, and stoichiometric imbalances that degrade device reliability. And while wet etching is gentle, it has major limitations: it is typically isotropic, it lacks directional control, and it poses challenges for fabricating vertical, high-aspect-ratio structures.



➤ Figure 1. In the LPCVD system for Ga_2O_3 epitaxy, gallium pellets in the source zone are heated and transported downstream by argon carrier gas. In the growth zone, gallium adatoms react with oxygen at the heated substrate surface to form crystalline β-Ga_2O_3 films. In the etch mode, operated with only gallium and argon (without O_2 or $SiCl_4$), gallium reacts with Ga_2O_3 to produce volatile Ga_2O, enabling smooth, damage-free material removal.

The growth bottlenecks on one side and etching challenges on the other hinder the development of scalable Ga_2O_3 devices. This leaves those standing at this crossroads to ponder this question: Could there be a more unified approach to processing Ga_2O_3, one that addresses growth and patterning together?

Our team at the University of Massachusetts Lowell has been considering this, and we think we have an answer, obtained by exploring an underutilised yet powerful technique – low-pressure CVD, or, for short, LPCVD.

This deposition technology has a number of strengths that are worthy of deeper investigation. Thanks to the reliance of LPCVD on an ultra-high-purity solid-source metallic gallium precursor, there's a cleaner reaction environment than conventional metal-organic approaches, significantly reducing the risk of carbon, hydrogen or chlorine contamination and parasitic impurity incorporation – these are issues often observed in MOCVD and HVPE systems. Operating under high-temperature, low-pressure conditions, LPCVD supports rapid epitaxial growth and finely tuned surface kinetics, making it particularly well-suited for the deposition of thick, low-doped β-Ga_2O_3 layers with ultra-high purity.

What began as an exploration of growth efficiency soon revealed something more. As we pushed LPCVD to deliver high-purity, high-mobility β-Ga_2O_3 films, we realised the same environment could also be leveraged for etching. By shifting our conditions, we transition our process from deposition to the controlled removal of material, opening the door to a plasma-free, *in-situ* etching technique that carves smooth, anisotropic features into Ga_2O_3 with unprecedented control. In a single system – without plasma, without corrosive halides, and without organometallic precursors – we grow and pattern this oxide, effectively sculpting the foundations of power devices. This dual capability is not an incremental improvement – it's a transformational step toward redefining how ultrawide-bandgap semiconductors like Ga_2O_3 can be processed at scale.

The growth bottleneck

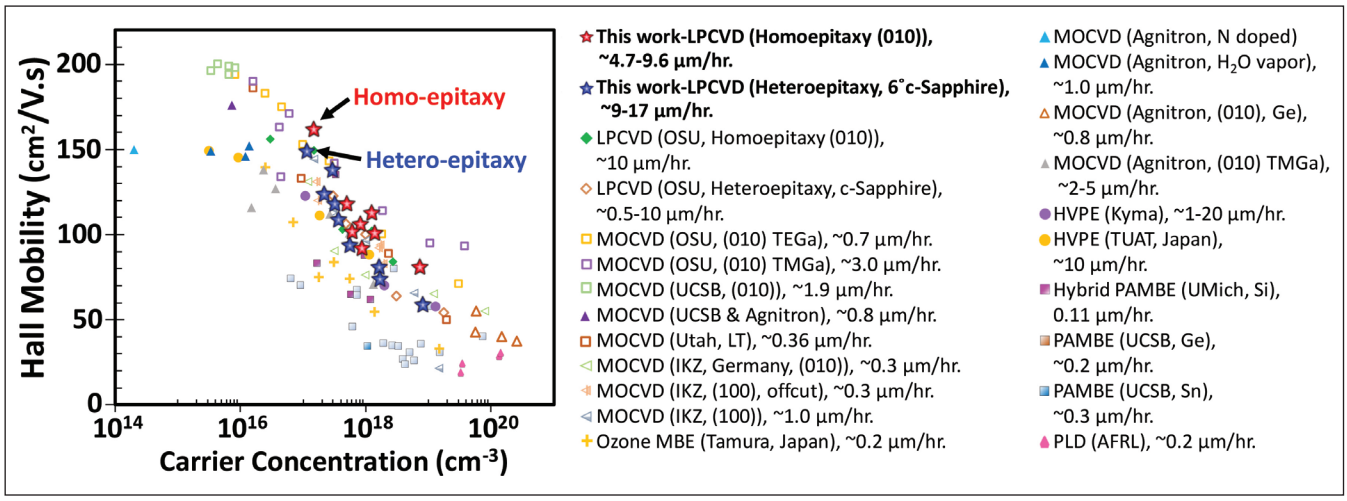
High-quality drift layers are the bedrock of vertical Ga_2O_3 devices. But the path to growing them at scale has been littered with compromise. MOCVD, while widely adopted, involves metal-organic precursors that introduce carbon impurities with surface defects and cracks, particularly when cranking up the growth rate. The hallmark crystalline quality of this deposition technology is offset by sluggish growth rates and parasitic reactions that erode yield. HVPE, on the other hand, accelerates growth, but leaves behind rough surfaces that necessitate chemical-mechanical polishing. The other obvious contender, MBE, provides atomic precision and tight doping control, but is impractical for thick-layer growth, due to painfully slow deposition rates and high operating costs.

This is where LPCVD begins to shift the narrative.

Our team is using a home-built LPCVD reactor that's fed with elemental gallium and oxygen precursors (see Figure 1). Ultra-high purity argon provides the carrier gas.

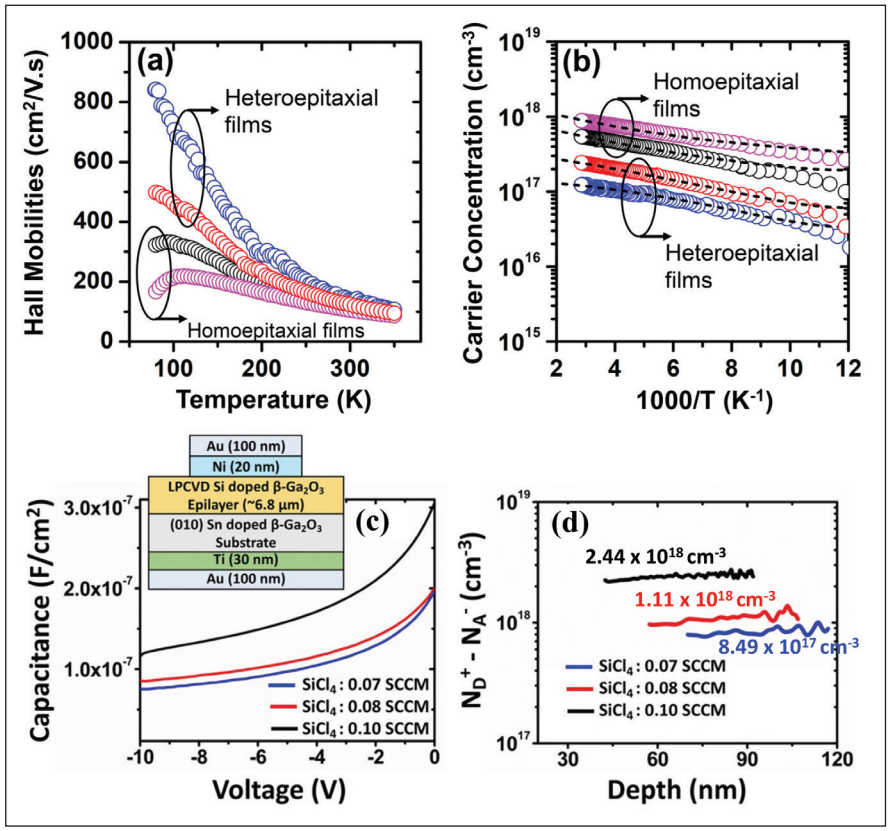
Using this reactor, we observe a confluence of purity, growth rate, and control that is difficult to achieve in Ga_2O_3 epitaxy. Operating at 1000°C and 1.5 Torr, with a carefully optimised source-to-substrate spacing for uniformity, we realise growth rates as high as 17 μm hr^{-1}. These rates are an order of magnitude higher than typical MOCVD and MBE, and are on par with HVPE, but with smooth surfaces and ultra-clean material quality.

The electrical performance of these films breaks new ground. Our homoepitaxial (010) β-Ga_2O_3 films have



➤ Figure 2. Room-temperature Hall mobility versus carrier concentration for β-Ga_2O_3. LPCVD-grown films show mobilities up to 162 $cm^2 V^{-1} s^{-1}$ for homoepitaxy on (010) β-Ga_2O_3 native substrates, values comparable to the best reports, but realised at higher growth rates. For heteroepitaxial ($\bar{2}01$) β-Ga_2O_3 films on *c*-sapphire, a mobility up to 149 $cm^2 V^{-1} s^{-1}$ is achieved – the highest reported by any growth method. For more details, see Khan *et al*. Appl. Phys. Lett. **126** 012103 (2025).

room-temperature Hall mobilities of 162 $cm^2 V^{-1} s^{-1}$ at a carrier concentration of 1.5 × 10^{17} cm^{-3} – these values are fully comparable with the best reported from state-of-the-art growth techniques, but obtained using far higher deposition rates (see Figure 2). Even more striking, our heteroepitaxial ($\bar{2}01$) β-Ga_2O_3 films on 6° offcut *c*-plane sapphire have mobilities of 149 $cm^2 V^{-1} s^{-1}$ at 1.15 × 10^{17} cm^{-3}, representing the highest reported for β-Ga_2O_3 grown by any method. Meanwhile, our low-temperature Hall measurements reveal peak mobilities exceeding 843 $cm^2 V^{-1} s^{-1}$ at 80 K for heteroepitaxial ($\bar{2}01$) β-Ga_2O_3 films. This result reflects minimal ionised impurity scattering and a high material quality (see Figure 3).



➤ Figure 3. Transport and doping characteristics of LPCVD-grown silicon-doped β-Ga_2O_3. (a) and (b) Temperature-dependent Hall measurements show peak mobilities of 843 $cm^2 V^{-1} s^{-1}$ for heteroepitaxial ($\bar{2}01$) films and up to 332 $cm^2 V^{-1} s^{-1}$ at 80-110 K for homoepitaxial (010) films. (c) and (d) Capacitance-voltage and depth profiling demonstrate uniform silicon doping by controlling $SiCl_4$ gas flows.

We enjoy great versatility when using a $SiCl_4$ gas precursor to provide silicon doping. Adjusting the flow rate tunes the carrier concentration across more than two orders of magnitude, from × 10^{17} cm^{-3} to beyond 1 × 10^{19} cm^{-3}, while preserving excellent crystal quality. Results from structural analysis are unambiguous: X-ray diffraction shows rocking curves as narrow as 63 arcsec, Raman confirms phase-pure β-Ga_2O_3 with no secondary phases, and atomic force microscopy scans offer evidence of atomically smooth surface morphologies.

But beyond numbers, what makes LPCVD truly powerful is how it handles purity. According to secondary ion mass spectrometry, our films have extremely low levels of carbon, hydrogen, and chlorine, well below the detection limits of this technique (see Figure 4). This strength is especially notable when comparing the purity of our films with those grown by trimethylgallium-based MOCVD processes, which struggle with residual carbon, even under aggressive purging. Note that the absence of carbon is not just a purity metric; it directly impacts compensation, carrier scattering, and long-term reliability.

Taken together, our results highlight that

LPCVD is more than just another growth method. It is a scalable, tuneable, and remarkably clean platform for producing high-quality thick β-Ga_2O_3 films.

But we soon discovered that's only half the story. The real power of LPCVD lies in its duality: not just growing Ga_2O_3, but shaping it. Read on to discover of how LPCVD also provides plasma-free, orientation-selective etching.

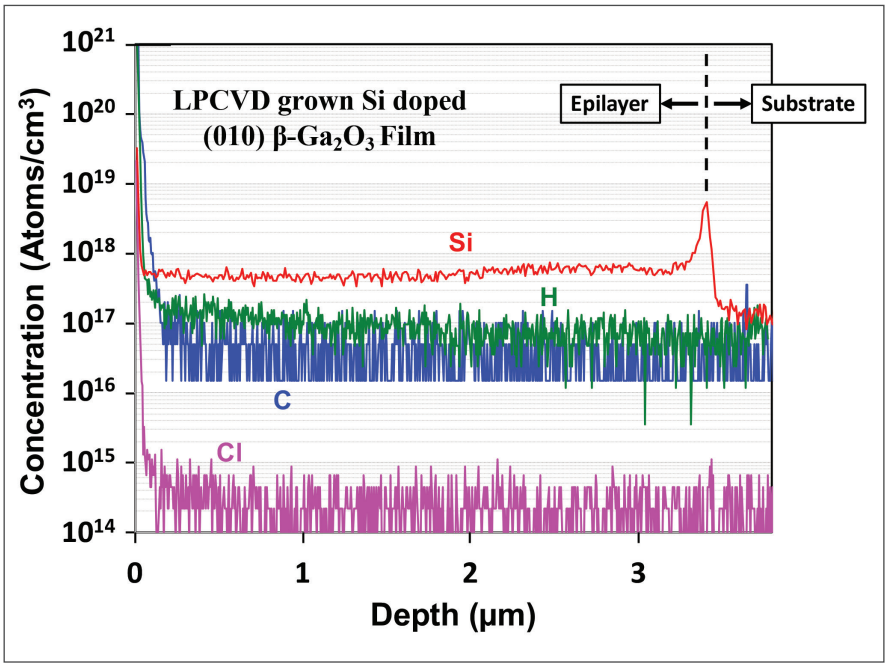
Etching without scars

Etching β-Ga_2O_3 has long been one of its most persistent processing challenges. While plasma-based etching with BCl_3/Cl_2 produces vertical profiles, they tend to suffer from surface damage, oxygen vacancies, and trap states that degrade device performance through premature breakdown and higher leakage. Turning to wet etching avoids plasma-induced damage, but this technique is isotropic, slow, and lacks the control needed for vertical, high-aspect-ratio structures. There are other approaches, such as metal-assisted etching, but challenges remain, including relatively low etch rates and a reduced Schottky barrier, due to surface oxygen loss and reconstruction. Even emerging *in-situ* approaches based on MBE or MOCVD encounter challenges, with researchers grappling with gallium droplet formation and the need for additional cleaning/etching steps before regrowth.

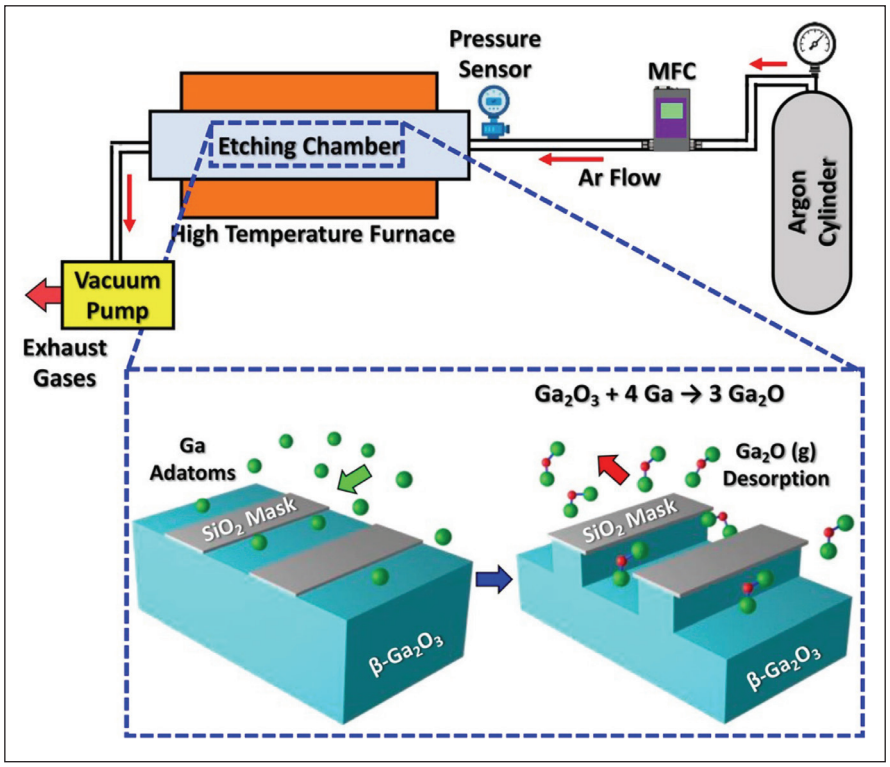
These persistent hurdles raise an intriguing possibility: could Ga_2O_3 be etched in the same controlled, damage-free way that it is grown?

That's what we set out to explore, using our LPCVD platform developed for Ga_2O_3 growth and pivoting it toward etching. To accomplish this switch, we introduce metallic gallium in the upstream zone, heating it in tandem with the substrate. These conditions cause a vapour-phase suboxide reaction to take place *in situ*, with gallium and Ga_2O_3 reacting to produce the volatile suboxide Ga_2O. Under a flow of argon, Ga_2O is swept away to leave etched features, crucially without the telltale scars of plasma damage (see Figure 5). There's no ion bombardment and no reactive radicals. Just a thermodynamically driven surface reaction that respects the underlying crystal structure.

Our experiments have involved etching temperatures between 1000-1100°C and pressures around



➤ Figure 4. Secondary ion mass spectrometry profile of a silicon-doped LPCVD β-Ga_2O_3 (010) film. Data show uniform silicon incorporation across the epilayer, while background levels of carbon, hydrogen, and chlorine remain below detection limits, highlighting the high purity of LPCVD growth.



➤ Figure 5. The LPCVD system can provide in-situ etching of β-Ga_2O_3 via the selective reaction of gallium adatoms with exposed β-Ga_2O_3 surfaces to form the volatile Ga_2O suboxide. This enables anisotropic, plasma-free etching through SiO_2 mask-defined regions.

0.5-2.1 Torr. These conditions enable etch rates as high as 2.25 μm hr^{-1} – that's orders of magnitude faster than a typical wet etch, and competitive with plasma-based dry etches, but without the collateral damage. This clean, controllable performance highlights the promise of our approach.

Beyond the high etch rate and clean surfaces, our gallium-assisted etching reveals a striking directional dependence. We discovered this by patterning radial trench arrays across (010) β-Ga_2O_3 substrates. Results reveal a stunning dependence on in-plane orientation. We found that trenches aligned with (100) orientations produce the cleanest, most vertical sidewalls – smooth, sharp, and nearly ideal. In contrast, those aligned along orientations such as (101) show lateral undercut, roughened sidewalls, and curvature at the trench bottom (see Figure 6).

We attribute this directional dependence to the surface energy and chemical stability of different Ga_2O_3 facets. The (100) plane, known for its low surface energy and high thermodynamic stability, offers minimal reactivity and promotes layer-by-layer removal. Meanwhile, planes like (101) possess higher surface energies, are less stable, and are thus more prone to lateral etching and microfacet formation.

Rotating trenches away from the (100) plane allowed us to observe a progressive evolution of sidewall morphology. This investigation determined that intermediate orientations produce stepped sidewalls, made up of competing crystal facets; and as the direction shifts further, one facet family begins to dominate, stabilising the etch profile along that orientation.

In other words, the anisotropy isn't imposed by a plasma sheath or a lithography trick; it emerges naturally from the crystal structure. This self-selecting behaviour, a kind of thermodynamic 'etch relaxation', offers fresh insight into gallium-assisted Ga_2O_3 etching in LPCVD systems, and highlights a controllable, damage-free path for building vertical device structures.

The most exciting aspect is that this plasma-free process opens new doors to the monolithic integration of vertical 3D structures. There is the tantalising prospect of growing and etching Ga_2O_3 in the same chamber, and tuning anisotropy through the judicious selection of crystal orientation, temperature, carrier gas flow and source-to-substrate spacing. That level of control, realised without the usual damage, is what scalable Ga_2O_3 device manufacturing needs.

Sculpting devices

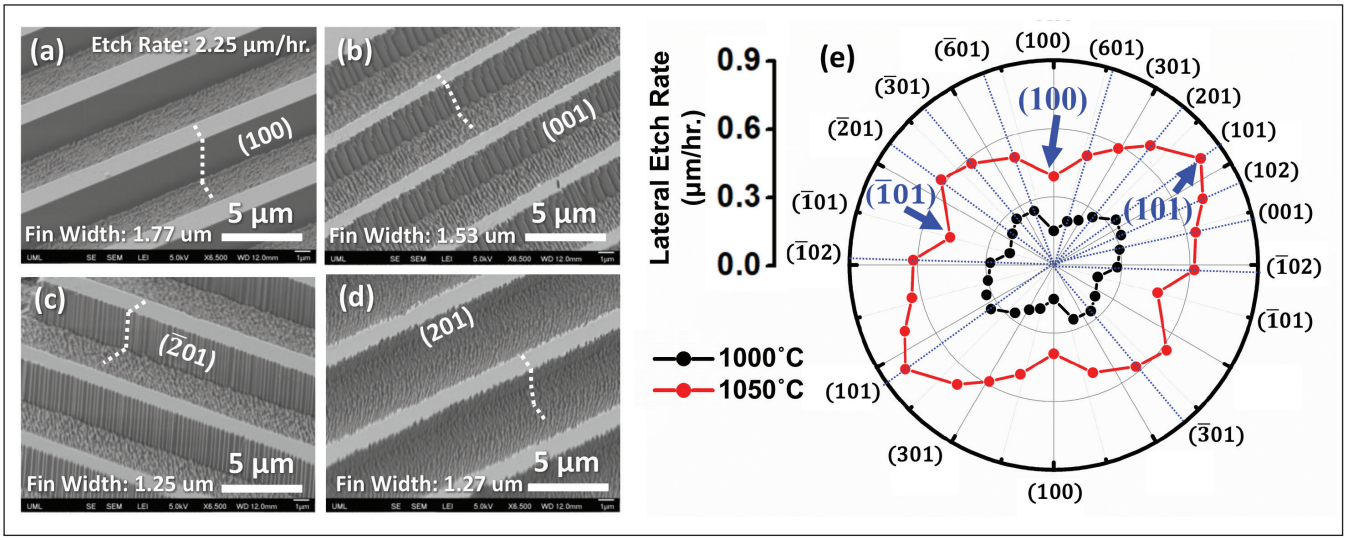
However, what good is a new processing technique if it can't deliver real devices?

That's the question we asked ourselves after validating LPCVD as a platform for high-purity growth and plasma-free etching. With those successes under our belt, it was time to move from concept to consequence. But could this dual-purpose platform do more than simply demonstrate elegant chemistry and impressive materials data? Could it, in fact, aid the fabrication of real, vertical Ga_2O_3 power devices, on affordable substrates, with minimal processing steps and zero exposure to plasma?

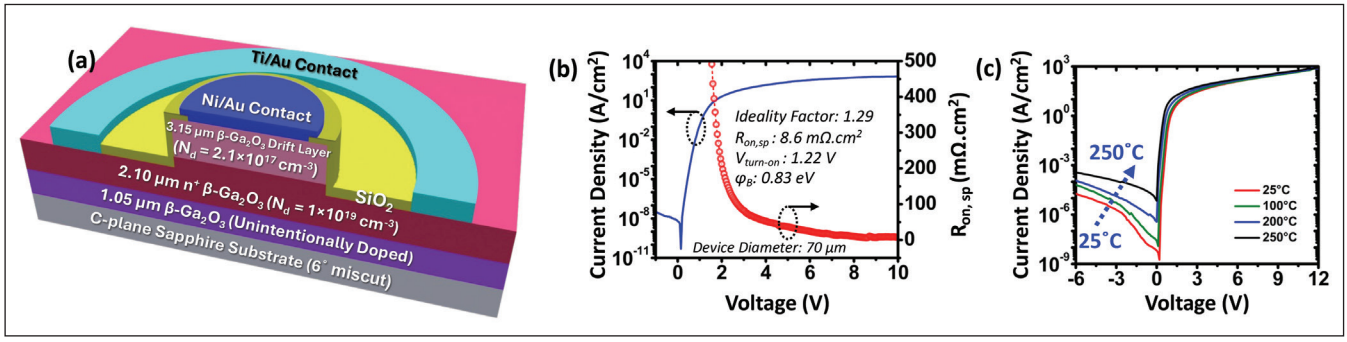
Our goal was ambitious: the fabrication of quasi-vertical β-Ga_2O_3 Schottky diodes, entirely within the confines of an LPCVD-based process flow, starting from film growth on sapphire and ending with *in-situ* mesa isolation via gallium-assisted etching. No ion bombardment. No dry etch residues. No need for damage control. Just epitaxy, etching, and forming electrodes.

We began by loading *c*-plane sapphire, a readily available and cost-effective substrate, into our LPCVD reactor. Using a 6° miscut, we realised step-flow growth of ($\bar{2}$01)-oriented β-Ga_2O_3 epilayers, forming a 6.3 μm-thick epitaxial stack with a clean architecture: a buffer layer, a heavily doped n^+ contact region, and a lightly doped drift layer. By precisely tuning $SiCl_4$ flows, our structure featured carrier concentrations ranging from 1×10^{19} cm^{-3} to 2×10^{17} cm^{-3} (see Figure 7).

Next came the etch. Using the same reactor, we introduced solid gallium



➤ Figure 6. Tilted field-emission scanning electron microscopy images of etched trench arrays along different crystallographic orientations on (010) β-Ga_2O_3, showing variations in fin width and sidewall morphology. The polar plot of lateral etch rates at 1000 °C and 1050 °C highlights strong anisotropy: the (100) orientation shows the most stable, vertical sidewalls, while (101) exhibits the fastest lateral etching, consistent with its higher surface energy and lower stability. For more details, see Khan et al. Appl. Phys. Lett. **127** 102105 (2025).



➤ Figure 7. Quasi-vertical β-Ga_2O_3 Schottky barrier diodes fabricated entirely within an LPCVD process flow on a sapphire substrate. (a) Device schematic showing the epitaxial stack and contacts. (b) Forward current-voltage characteristics show a low turn-on voltage of 1.22 V, a differential on-resistance of 8.6 mΩ cm^2 and an ideality factor of 1.29, reflecting solid diode performance. (c) Temperature-dependent measurements up to 250 °C show stable forward conduction and rectification ratios consistently above 10^5. For more details, see Khan et al. APL Electronic Devices **1** 036125 (2025).

upstream to perform *in-situ* mesa isolation at 1050°C. This allowed the volatile suboxide Ga_2O reaction previously studied to serve a new role: carving out 3D device topographies. With a SiO_2 mask in place, we etched 3.6 μm-deep mesas.

Our next step involved fabrication of quasi-vertical Schottky barrier diodes, featuring Ni/Au Schottky contacts atop the etched mesa and Ti/Au cathodes contacting the recessed n^+ layer. These devices delivered strong, clean forward characteristics. The turn-on voltage landed at 1.22 V, the ideality factor hovered at 1.29, and the Schottky barrier height was 0.83 eV. Importantly, these diodes handled forward current densities up to 252 A cm^{-2} and exhibited a differential specific on-resistance of just 8.6 mΩ cm^2.

And they held up under stress. When ramping from room temperature to 250°C they didn't flinch. The ideality factor rose only slightly, and the reverse leakage remained modest, climbing from 5 μA cm^{-2} at 25°C to just 170 μA cm^{-2} at 250°C. Even at the highest temperatures tested, the rectification ratio remained above 10^5. Under reverse bias, our devices exhibit blocking voltages of up to 100 V, corresponding to electric fields approaching 2 MV cm^{-1}. While these values are still below the theoretical potential of Ga_2O_3, they are primarily limited by the drift layer design, and specifically, the relatively high doping in the drift layer. According to TCAD simulations, electric field crowding near the anode perimeter also plays a role in early breakdown. Much higher blocking voltages can be readily achieved with optimised edge termination, thicker drift layers, lower doping profiles and the introduction of a high-permittivity dielectric.

Even so, our results clearly validate the LPCVD processing platform: within a single system we demonstrate high-quality growth, damage-free etching, and the fabrication of β-Ga_2O_3 Schottky diodes on low-cost sapphire – all without plasma exposure or post-etch recovery.

From process to platform

What makes LPCVD uniquely powerful is not just its ability to grow or etch, but to unify both in a single platform. Instead of relying on separate tools for deposition, doping, and patterning, one can undertaken growth and orientation-selective etching in a continuous flow with LPCVD, without breaking vacuum. This brings clear advantages in yield, cost, and scalability.

Our approach is intrinsically modular and scalable. By using solid-source metallic gallium, many impurity risks inherent in metal-organic chemistries are eliminated. The absence of a plasma ensures preservation of surface integrity, critical for Schottky interfaces, gate dielectrics, and regrown junctions. And as devices increase in complexity – through the introduction of deep trenches, vertical fins, or dielectric caps – the value of our low-damage, chemically selective etch-and-regrowth strategy will become even more pronounced.

As the power device community pushes toward deeper verticality, higher voltages, and more thermally demanding systems, platforms like LPCVD – modular, directional, and clean – will not just be useful, but essential. By uniting growth and etching in one coherent process, LPCVD will transform Ga_2O_3 fabrication from a collection of disconnected steps into a scalable platform – and one that's capable of shaping the next generation of ultrawide-bandgap power electronics.

We gratefully acknowledge funding support from National Science Foundation (ECCS Awards 2501623 and 2532898) for this work.

FURTHER READING

- S. A. Khan *et al.* "Low-pressure CVD grown Si-doped β-Ga_2O_3 films with promising electron mobilities and high growth rates" Appl. Phys. Lett. **126** 012103 (2025)
- S. A. Khan *et al.* "Plasma damage free *in situ* etching of β-Ga_2O_3 using solid-source gallium in the LPCVD system" Appl. Phys. Lett. **127** 102105 (2025)
- S. A. Khan *et al.* "Quasi-vertical β-Ga_2O_3 Schottky diodes on sapphire using all-LPCVD growth and plasma-free Ga-assisted etching" APL Electron. Devices **1** 036125 (2025)

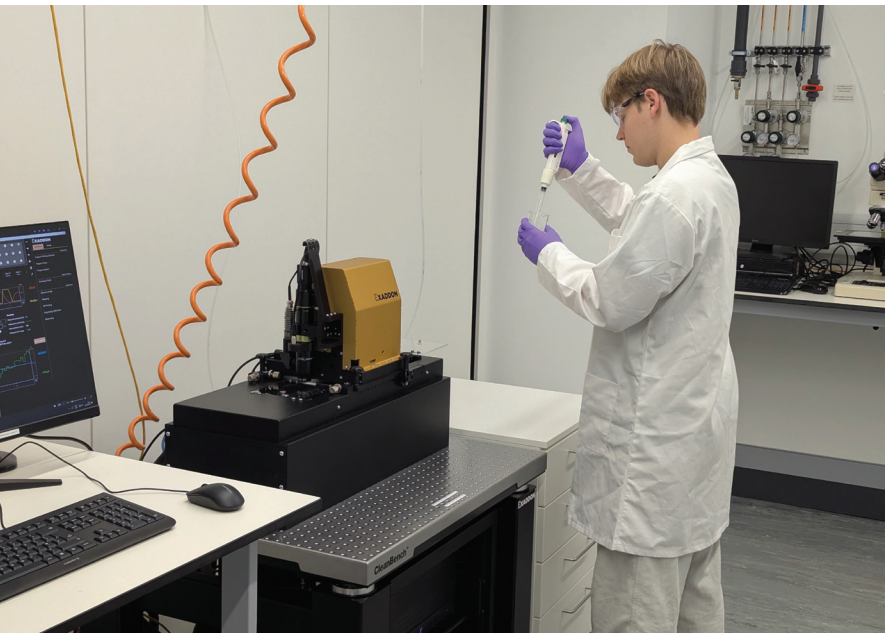
Sculpting at the micro-scale

Emerging fabrication techniques are re-writing the rulebook for on-chip components

BY ARTHUR COLLIER, ABDALLA EBLABLA AND KHALED ELGAID FROM CARDIFF UNIVERSITY

FROM next-generation wireless to autonomous vehicles, there's a race to higher frequencies that's reshaping the demands on electronic hardware. At the heart of this pursuit is an urgent need for components that as well as being smaller and faster, are capable of handling the unforgiving realities of the millimetre-wave and sub-terahertz domain. At such high frequencies conventional fabrication methods struggle to fulfil these requirements, an issue that creates restrictions for designers trying to tackle the engineering challenges of next-generation systems. But progress is underway, with a new wave of innovation redefining the constraints for the design and fabrication of active and passive devices.

These advances are needed for emerging applications, which are increasingly pushing into millimetre-wave and sub-terahertz frequencies to access the wide bandwidths required. Such high frequencies demand low-loss, high-performance passive components, from filters and couplers to antennas and resonators.



In this high-frequency domain, GaN has established itself in active devices, due to its efficiency and high-power density. But it must be accompanied by surrounding passive structures, which must evolve just as quickly. In addition to addressing this goal, due to the drive for miniaturisation and system-in-package integration, there's a need to develop highly compact passives with complex geometries that can be integrated monolithically. Here, the limitations of established methods for fabricating MMICs are becoming increasingly apparent.

Until recently, conventional IC fabrication methods constrained the geometry of on-chip metallic structures. It's a restriction that's re-enforced by the IC design process, which ensures a planar approach, with layout files defined as sequential layers of two-dimensional shapes. Engineers have extended these methods to produce quasi-3D structures, such as air-bridges that allow circuit connections to cross one another. However, geometric freedom is severely limited by a reliance on temporary dielectric layers and resist chemicals as scaffolding during fabrication. Structures produced with this approach are constrained in span and height, with industry processes typically limited to just 1 μm - 2 μm above the substrate to maintain yield.

Breaking these shackles are recent advances in metal-additive micromanufacturing (μAM), which enable new possibilities in on-chip passive component design and fabrication. And within this new manufacturing technology is a particularly promising technique, localised electrodeposition, exemplified by commercial tools, such as the Exaddon CERES system. Localised electrodeposition enables highly conductive, fully three-dimensional structures with sub-micron feature sizes – an ideal platform for millimetre-wave passive components. Strengths of this form of localised deposition include its capability to produce, with sufficient reliability, complex geometries with horizontal and vertical aspect ratios of up to 100:1. The adoption of such methods in MMIC fabrication promises to rewrite

the rulebook for millimetre-wave passive design and system-in-package integration.

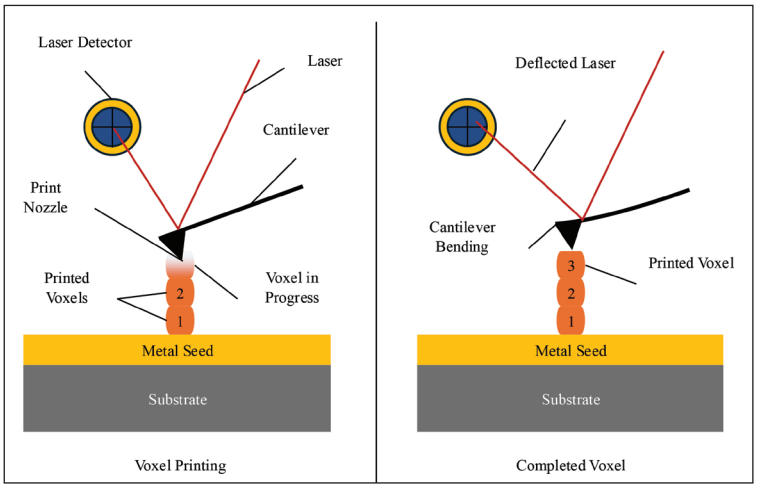
Printing principles

The operating principles of localised electrodeposition μAM are fundamentally different from those associated with conventional planar fabrication methods. Illustrating this point are tools such as the CERES μAM – employing a cantilever tip with a microfluidic channel, it delivers an aqueous solution that's rich in metal ions directly to the intended site of electrodeposition (see Figure 1). The deposition occurs at the surface of a semiconductor sample, which must have either a metal seed layer or pre-existing metal features from prior fabrication. When using the CERES μAM, engineers place their samples in a chamber filled with electrolyte solution that provides a conductive medium between a potential applied at the sample surface and a counter electrode. The resulting electrochemical circuit ensures that electrodeposition take places, with microfluidic delivery through the cantilever providing the means to guide deposition to the desired location.

With localised electrodeposition μAM, a feedback mechanism must monitor the growth of each structure. Much like conventional 3D printing, designs are divided into individual voxels, which can be thought of as volumetric elements, representing the smallest unit of a 3D digital dataset. As each voxel forms, the deposited metal beneath the microfluidic nozzle causes the cantilever to bend upward. The tool detects this deflection using a laser, providing real-time confirmation of voxel completion. Once a voxel is finished, high-precision actuators reposition the stage in all three dimensions for the next voxel. Repeating this process enables the fabrication of arrays of on-chip passive components. Structures that have already been demonstrated range from helical antennas to shielded bond wires.

Possibilities for RF circuits

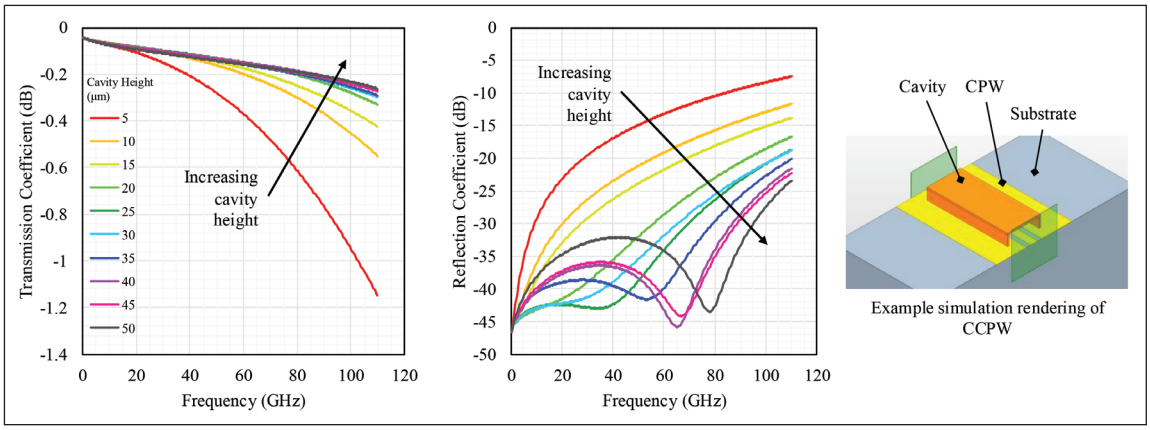
Our team at Cardiff University is able to access a recently installed μAM tool at The Institute for Compound Semiconductors. This new tool is a complimentary addition to this state-of-the-art nanofabrication facility.



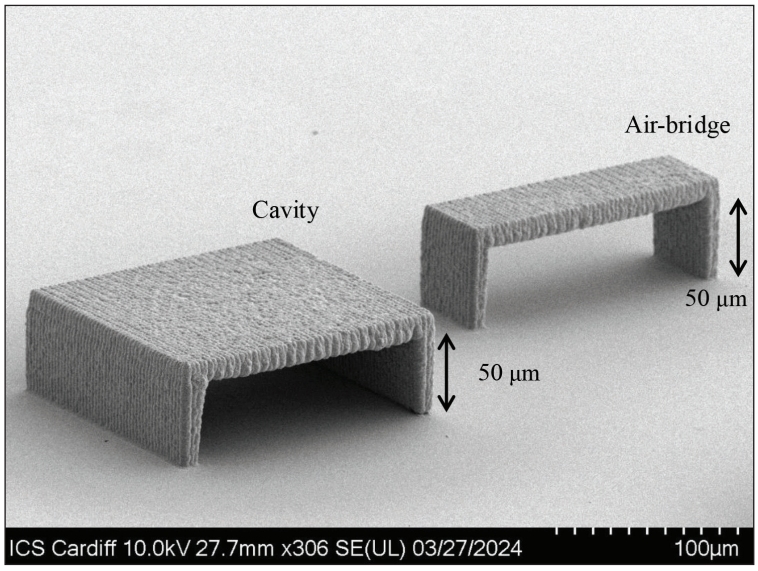
➤ Figure 1. Localised electrodeposition printing process control through laser deflection on a cantilever.

Drawing on our GaN MMIC process, we have worked to extend its capabilities with the μAM tool, with the air-bridge stage quickly identified as a strong candidate for improvement. Air-bridges are essential in coplanar-waveguide MMICs – as well as enabling signals to cross, they preserve efficiency and signal integrity at impedance discontinuities. Critically to GaN technology, air-bridges are an attractive option for forming multi-finger transistors that ultimately allow devices to deliver the high-power-density devices that systems are demanding increasingly. While conventional air-bridges have helped engineers advance their MMICs, they have a major limitation, as they introduce parasitic effects on the coplanar waveguide beneath them.

To explore opportunities that might overcome this issue, our team has undertaken simulations that consider geometries well outside of the scope provided by conventional fabrication. By turning to μAM, we are able to construct air-bridges that reach greater heights, span wider gaps, and extend longer distances across waveguides. One design concept even enclosed an entire waveguide beneath a suspended cavity structure, effectively forming a ground plane above the coplanar



➤ Figure 2. Simulated scattering parameters of cavity waveguides, illustrating improved matching and reduced insertion losses for taller cavities.



➤ Figure 3. Scanning electron microscope images of prototype air-bridge and cavity with a height of 50 µm, printed on a copper seed substrate on silicon.

waveguide – an idea that gave rise to the cavity coplanar waveguide.

We have found that the additional height provided by µAM is critical. Taller cavities improve matching and reduce insertion loss (see Figure 2). What's more, we are able to engineer a null in the reflection coefficient, enabling enhanced matching within a specific bandwidth, with the null's centre frequency tuneable through cavity geometry.

Voxels into structures

Following on from our device simulations, we have developed a process for printing an air-bridge using µAM. This structure comprises two supports and a connecting span – effectively three boxes, each built from individual voxels. To optimise the printing of these boxes, we balanced two key variables: the pitch, or spacing, between voxels; and the pressure applied during delivery of copper ions to the deposition site. For a fixed voxel pitch, we employed a higher pressure to improve filling and reduce gaps, but avoided the use of excessive pressure, as this causes voxels to merge, degrading print quality. We identified the optimal balance with test boxes, formed by varying pitch and pressure. Examining these boxes under a microscope revealed the optimal process, then used to construct the three boxes that are combined to form air-bridge or cavity structures.

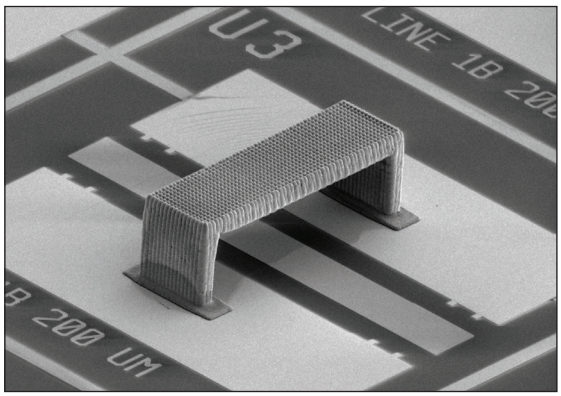
Unfortunately, localised electrodeposition introduces challenges not seen in conventional 3D printing. One significant issue is that not all ions that exit the nozzle are deposited exactly where intended; some accumulate on nearby features – a phenomenon we call 'spray deposition'. This unintended deposition must be factored into the design strategy. For example, if the first support is printed, followed by the second, prior to the connecting span, it's critical to consider the spray that's deposited on the first support during the second print as this alters its height. When returning to connect the span, this mismatch risks a tip crash. To avoid this, we leave an intentional small gap in the design, so the span can connect reliably without interference.

After taking these considerations into account, we printed final prototypes of an air-bridge and a cavity on a copper seed substrate. Scrutinising these structures with a scanning electron microscopy revealed impressive results: structures towering 50 µm above the surface – well beyond the limits of conventional air-bridge fabrication. Using optimised pressure, our voxels pitched 3 µm apart were densely packed, and provided seamless connections between the supports and span to yield robust, mechanically sound constructions.

Integration with circuits

Following these excellent printing results, we shifted our focus to implementation at the circuit level. These efforts involved the design of a planar layout, consisting of arrays of co-planar waveguides. We diced a 150 mm diameter GaN-on-SiC wafer into 25 mm by 25 mm tokens and employed photolithography to transfer the layout onto each token. Our next steps involved evaporating layers of titanium and gold, with titanium providing strong adhesion between the semiconductor surface and gold, before patterning a second resist layer to define the base positions of each bridge support. We have found that while not essential for printer operation, this resist pattern greatly improves optical alignment when positioning the printed structures on the existing waveguides. After patterning a second resit layer, we loaded the sample into the µAM tool for printing, with arrays of air-bridges and cavities aligned in a single step and printed sequentially. Finally, we removed the protective resist mask to reveal the finished sample.

Using these steps, we have printed a 50 µm-tall air-bridge on a co-planar waveguide that connects two



➤ Figure 4. Scanning electron microscopy image of a printed air-bridge aligned to a co-planar waveguide on a GaN-on-SiC substrate.

The development of μAM to advance the fabrication capabilities of active and passive components marks a new era in the way we consider both the design and the fabrication of millimetre-wave wave ICs

ground planes (see Figure 4). When implemented at an impedance discontinuity, this electrical connection prevents parasitic modes, preserving signal integrity and efficiency. In our scanning electron microscopy image, shown in Figure 4, one can see dark rectangles at the base of the bridge supports, protruding above the gold waveguide surface. This observation indicates spray deposition through openings in the resist mask, which may additionally enhance adhesion of the air-bridge to the waveguide.

Performance potential

Scattering parameters are an essential tool for diagnosing the performance of RF components. Specifically for components that propagate signals within an IC, reflections of signal power may be indicative of poor impedance matching, and threaten to result in reductions in system efficiency, as well as posing a risk to signal integrity. As sensitivity to impedance matching becomes even more profound as operating frequencies push into the millimetre-wave and sub-terahertz domain, the reflection coefficient of interconnect structures is a very important parameter.

So how do co-planar waveguides with printed air-bridges or cavities perform in the millimetre-wave domain? To answer this, we turned to a vector network analyser to measure the reflection and transmission of signal power at each end of the co-planar waveguide. By sweeping frequencies from 1 GHz to 110 GHz, we covered the bands relevant to emerging and future wireless communications applications. Three devices were characterised: a bare co-planar waveguide; and variants with an air-bridge and a cavity.

Our results show that transitioning from the air-bridge to a cavity covering the co-planar waveguide increased reflection and transmission coefficients across the entire measured frequency range. At 110 GHz, the reflection coefficient increased by 35 percent without compromising insertion loss. Another encouraging experimental result is that we observed the wide-bandwidth null in reflection coefficient predicted by simulations, a finding that highlights the potential for engineered matching within a specific bandwidth. Simulations also indicate that the position of this null is proportional to cavity dimensions, suggesting that careful design of the cavity geometry could enable tuneable performance in future devices.

To conclude, we have successfully integrated our μAM process into our GaN MMIC fabrication workflow, to demonstrate significantly enhanced geometries attainable for passive structures. Notable triumphs within this work include: the construction of air-bridges spanning 50 μm above the surface, far exceeding the limits of conventional fabrication methods; and an initial exploration of co-planar waveguides enclosed within a cavity, a study that reveals the potential for improved matching at impedance discontinuities in the millimetre-wave domain.

The development of μAM to advance the fabrication capabilities of active and passive components marks a new era in the way we consider both the design and the fabrication of millimetre-wave wave ICs. There is good reason to believe that metal additive micromanufacturing can play a pivotal role in delivering the intricate structures required by miniaturisation and system-in-package integration. Our demonstration of localised electrodeposition μAM within the GaN MMIC process represents a key step toward implementations that could redefine the performance potential of millimetre-wave applications.

The authors would like to thank Exaddon AG for their technical support and IQE PLC for provision of GaN epitaxial material support. We would like to acknowledge the Institute for Compound Semiconductors (ICS) for usage of their facilities.

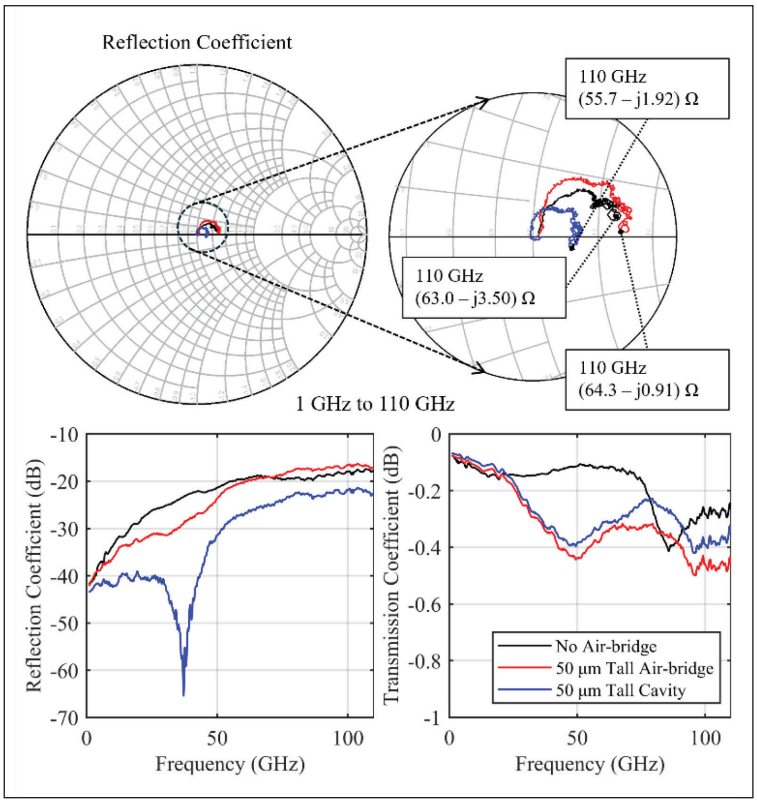


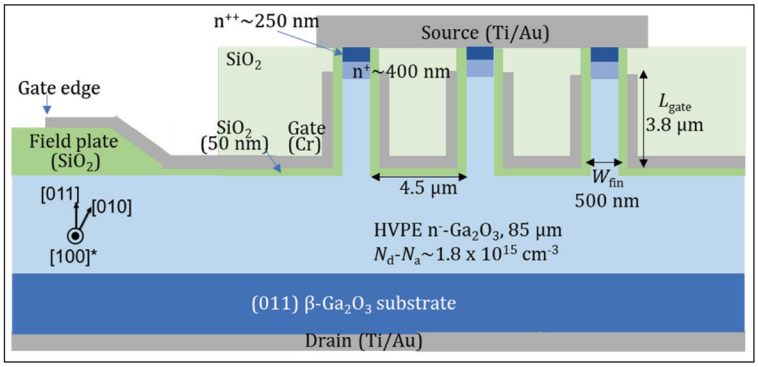
Figure 5. Scattering parameters comparing a bare co-planar waveguide (CPW), a CPW with a printed air-bridge, and a CPW with a printed cavity.

Breaking through the 10 kV barrier

A multi-fin FET formed by HVPE is the first vertical Ga_2O_3 transistor with a breakdown voltage exceeding 10 kV

ENGINEERS from Novel Crystal, Japan, are claiming to have produced the first vertical Ga_2O_3 transistor with a blocking voltage of more than 10 kV.

According to the team, which produces the epitaxial layer of its device by HVPE, a switch in the growth plane from (001) to (011) is critical to their success. This move, supressing chlorine incorporation, enabled the formation of an epitaxial layer with a thickness of more than 50 μm and a donor concentration of less than 5 x 10^{15} cm^{-3}.



➤ A number of deposition, lithography and etching steps were employed by Novel Crystal to produce its record-breaking multi-fin FETs.

Fabrication of Novel Crystal's multi-fin β-Ga_2O_3 FETs began by loading heavily doped *n*-type (011) Ga_2O_3 substrates into a HVPE chamber and depositing a lightly doped *n*-type layer of 85 μm-thick Ga_2O_3. According to capacitance-doping measurements, the doping concentration in this epilayer is 1.8 x 10^{15} cm^{-3}.

Silicon implantation and thermal diffusion, via annealing, produced a heavily doped *n*-type layer on the top of this film with a depth of 650 nm and a dopant concentration of around 1 x 10^{16} cm^{-3} to 8 x 10^{18} cm^{-3}. Subsequent silicon implantation and activation annealing at 900°C for 1 minute under nitrogen gas created a 200 nm-deep source contact layer with a silicon concentration of around 6 x 10^{19} cm^{-3}.

The next steps of the fabrication process involved plasma-enhanced CVD of a layer of SiO_2 and the patterning of chromium masks via electron-beam deposition and lithography, to define the size and location of the fin channels.

Dry etching, realising a near-vertical sidewall profile, defined the fin channels, prior to HF treatment for 15 minutes to remove the SiO_2/chromium masks and the plasma-damaged layer.

To complete the multi-fin transistors (see figure for details of the structure), the engineers: employed plasma-enhanced CVD and atomic layer deposition to grow layers of SiO_2; defined chromium masks, removed by dry etching; and added a Ti/Au source electrode on the fin top and a Ti/Au drain electrode on the backside of the substrate.

Novel Crystal's engineers employed a scanning electron microscope to inspect their device, which has a fin width of 0.5 μm, a pitch of 5 μm, and a length of 70 μm.

The layout of the team's device features 14 inner fins, surrounded by 4 outer fins. Of the 14 inner fins, 10 are covered with source electrodes and operate as the active layer of the multi-fin FET. With this layout, all fins under the source electrode exhibit the same FET characteristics.

One precaution taken by the engineers is to set the source electrode back from the fin edge by a few microns. This action prevents contact between gate and source electrodes at the deformed fin edge, an impairment caused by micro-loading effects during dry etching.

The team's transistor, which has an active area of 45 μm by 70 μm, according to the arrangement of the source electrode and fin, has a maximum drain density of 15.1 kA cm^{-2} and a specific on-resistance of 289 mΩ cm^2 at a gate voltage of 3 V.

This device exhibits normally-off characteristics, with a threshold voltage of 0.68 V. Drain current on-off ratio exceeds 10^7, and the sub-threshold slope is around 77 mV dec^{-1}.

To prevent early breakdown through air when conducting three-terminal off-state breakdown-voltage measurements, the team used a flourinert solution. Testing revealed a blocking voltage in excess of 10 kV, the limit of the equipment, and enabled an estimation of the electric field at the centre of the trench of 2.55 MV cm^{-1}.

Spokesman for the team, Daiki Wakimoto, told *Compound Semiconductor* they are now focusing on achieving a power figure-of-merit that exceeds that of SiC. Efforts will involve introducing an edge-termination structure that combines a magnesium guard ring and hetero *p*-type materials.

REFERENCE

➤ D. Wakimoto *et al*. Appl. Phys. Express **18** 106502 (2025)

Slashing the sheet resistance of ScAlN

An indium surfactant aids MBE of ScAlN/GaN heterostructures with an incredibly low sheet resistance

A CHINESE collaboration is claiming to have broken new ground in reducing the sheet resistance of ScAlN/GaN heterostructures grown on sapphire.

The success of the team – a partnership between researchers at Peking University, the Songshan Lake Materials Laboratory in Dongguan, and the Collaborative Innovation Centre of Quantum Matter, Beijing – attributes its low sheet resistance, just 137 Ω/sq, to employing an indium surfactant and introducing an ultrathin AlN interlayer.

According to the spokesperson for these researchers, Ping Wang from Peking University, their work addresses a critical bottleneck in the development of ScAlN-based high-frequency and high-power electronics – their breakthrough is the realisation of a high carrier density and high carrier mobility simultaneously on large-area, low-cost wafers.

Wang told *Compound Semiconductor* that the team's work demonstrates a scalable route to integrating scandium-based semiconductors with mainstream GaN, silicon and CMOS technologies.

"Our findings will most directly benefit high-frequency and high-power GaN HEMTs, RF front-end modules, and microwave amplifiers, where low sheet resistance and high 2DEG mobility are essential for improving gain and power efficiency," remarked Wang.

Additional strengths of the heterostructures produced by the Chinese collaboration are a sharp interface between ScAlN and GaN and excellent structural coherence. These traits are advantageous for ferroelectric transistors, non-volatile memories, and reconfigurable logic devices that exploit the strong polarisation and emerging ferroelectricity of ScAlN.

Researchers at Peking University have previously employed an indium surfactant for the growth of ScAlInN alloys and ScAlInN/GaN heterostructures.

"We observed that even trace indium incorporation during low-temperature growth could drastically improve interface quality, domain structure, and promote step-flow epitaxy," explained Wang.

During that study, Wang and co-workers discovered that indium could act as a volatile surfactant for enhancing adatom diffusion of scandium and aluminium without being incorporated into the lattice.

The latest success is the culmination of a comprehensive investigation, involving the production of a wide portfolio of heterostructures, each including the ternary alloy ScAlN. All these samples were produced in a plasma-enhanced MBE system featuring Knudsen effusion cells for the supply of elemental gallium, aluminium and scandium. A Veeco RF plasma source provided active nitrogen species.

Wang and co-workers acquired atomic force microscopy maps of samples with a 20 nm-thick ScAlN layer with a scandium content ranging from 0.18 to 0.23. Scans revealed smooth morphologies and well-defined atomic steps. Increases in scandium content resulted in a change from GaN-like step-spiral features, indicative of step-flow growth, to a more metal-rich surface with clearer atomic surfaces, and eventually the emergence of island-like features.

To build on their indium-surfactant-assisted growth, the team introduced an AlN interlayer between the ScAlN barrier and GaN channel to improve interfacial quality. It's claimed that this interlayer supresses interface roughness scattering by promoting a more abrupt transition between ScAlN and GaN layers, and thereby enhancing electron mobility.

Electrical measurements on a range of samples with a ScAlN barrier just 10 nm-thick, trimmed to account for the influence of the AlN interlayer on electron mobility and sheet carrier density, revealed that the best results are realised with an AlN layer that's 1 nm-thick and 10 nm-thick $Sc_{0.21}Al_{0.79}N$. For this structure, a sheet resistance of just 137 Ω/sq is realised alongside an electron mobility of 10^{20} cm^2 V^{-1} s^{-1} and an electron sheet density of 4.5 x 10^{13} cm^{-2}.

Wang explained that the team's next step is to integrate their high-quality ScAlN heterostructures into functional prototypes, including HEMTs, ferroelectric FETs, and multi-state non-volatile memories.

Another goal is to explore polarisation-engineered ScAlN heterostructures and domain-wall-controlled ferroelectric devices. The latter could merge high-frequency performance with non-volatile programmability.

"In parallel, we are expanding the indium-assisted growth strategy to larger wafer formats and alternative ultrawide-bandgap substrates, such as SiC, Ga_2O_3, and diamond, aiming to bridge advanced ScAlN materials research with industrial-scale GaN electronics and future ultra-low-power intelligent systems," added Wang.

REFERENCE
➤ L. Yang et al. Appl. Phys. Lett **127** 152101 (2025)

Platinum: A promising contact for *p*-type SiC

Switching from a conventional contact to one made from platinum reduces the annealing temperature required for forming a low resistivity *p*-type contact

ENGINEERS at Kyoto University have unveiled a promising process for producing low resistivity *p*-type contacts for SiC power devices.

Forming a low-resistivity ohmic contact on *p*-type SiC is far from easy – it requires an electrode metal with a work function larger than that of *p*-type SiC. As that condition is rarely met, when electrode metals are deposited on *p*-type SiC, this tends to create a high Schottky barrier with a high contact resistivity.

The standard approach for realising a low resistivity is the annealing of Ti/Al-based contacts at 1000°C. However, the low resistivity that results – it's in the range 10^{-6} Ω cm^2 to 10^{-4} Ω cm^2 – is accompanied by a number of downsides, including electrode melting, surface roughening and device degradation.

Offering an attractive alternative, the team from Kyoto is advocating platinum contacts and an annealing process at just 600°C. Evidence for the merits of this approach comes from their recent study, involving the evaluation of the characteristics of platinum contacts formed on both circular transmission line model structures and vertical Schottky barrier diodes.

Production of the circular transmission line model structures began with epitaxial growth of 10 μm-thick nitrogen-doped *n*-type SiC layers on *n*-type 4H-SiC (0001) substrates. Implantation of aluminium ions into these epitaxial layers at 500°C created box-shaped profiles with a depth of about 200 nm.

According to secondary ion mass spectrometry, after post-implantation annealing at 1750°C for 20 minutes under argon, the aluminium doping densities were 8.2×10^{19} cm^{-3}, 1.8×10^{20} cm^{-3}, 2.2×10^{20} cm^{-3}, and 3.0×10^{20} cm^{-3}, depending on the implant dose. Corresponding aluminium atom densities, based on capacitance-voltage measurements of Schottky carrier diodes and estimated Hall-effect measurements, were 3.4×10^{19} cm^{-3}, 5.8×10^{19} cm^{-3}, 6.2×10^{19} cm^{-3} and 8.3×10^{19} cm^{-3}.

The engineers turned to oxidation at 1300°C for 120 minutes to remove the surface region of SiC, due to its lack of uniformity in aluminium atom density, prior to cleaning the sample and adding 150 nm-thick platinum electrodes by sputtering. Annealing at either 400°C, 600°C or 800°C created a portfolio of samples.

Formation of Schottky carrier diodes began with the growth of a *p*-type SiC layers on *p*-type 4H-SiC (0001) substrates. The addition of platinum electrodes involved the steps employed for the circular transmission line model structures.

Surface profiles, obtained with a white-light interferometer, revealed a root-mean-square roughness of 1.41 nm and 7.04 nm for the platinum electrodes annealed at 600°C and 800°C, respectively. This led the team to conclude that annealing at 600°C significantly suppresses surface roughening of platinum electrodes to far lower values than those for Ti/Al-based contacts annealed at 1000°C – they have a typical roughness of between 10 nm and 40 nm.

Current-voltage plots were obtained for a range of circular transmission line model structures with an aluminium atom density of 8.3×10^{19} cm^{-3}. These measurements, on structures with various annealing temperatures, as well as no annealing, determined that the platinum contact annealed at 600°C produced the largest current and an ohmic current-voltage curve.

The team also measured contact resistivity under various annealing temperatures, as well as no annealing, using circular transmission line model structures with an aluminium atom density of 8.3×10^{19} cm^{-3}. As expected, contact resistivity depends on annealing temperature, with the lowest value occurring for annealing of the platinum contacts at 600 °C. Under this condition resistivity is just 3.2×10^{-5} Ω cm^2, a value that's said to be as low as that for Ti/Al-based contacts annealed at 1000°C.

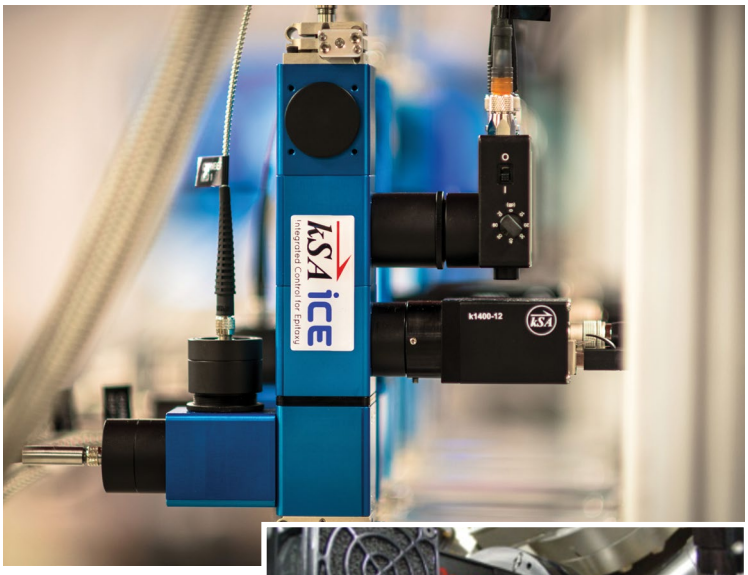
Subsequent capacitance-voltage measurements on Schottky barrier diodes revealed that a higher contact resistivity is associated with an increase in barrier height. Based on this insight, the researchers analysed their contacts with X-ray diffraction, observing peaks from platinum silicides. While the silicon atoms in SiC react with platinum atoms during annealing, that's not the case for carbon atoms, which are thought to remain near the Pt/SiC interface.

X-ray photoelectron spectroscopy determined the composition of the SiC-metal contact at various depths.

Drawing on all their work, as well as other studies, the team concluded that the platinum silicides are not behind the lower resistivity. Instead, it's suggested that sp^2 carbon, present in an amorphous state, creates several levels in the lower half of the bandgap of *p*-type SiC that trap holes and shift the Fermi level towards the valence band maxima – and this holds the key to low resistivity.

REFERENCE
➤ K. Kuwahara *et al*. Appl. Phys. Express **18** 101003 (2025)

Putting light to work since 1992



k-Space is the leading manufacturer of in situ, in-line, and ex situ metrology tools for the semiconductor, thin-film, and photovoltaic (PV) industries.

k-Space tools are used for monitoring nearly all thin-film deposition processes, including MBE, MOCVD, PLD, PVD, sputtering, and evaporation.

Measure carrier emissivity, wafer and film temperature, thin-film stress and strain, wafer curvature, wafer bow, wafer tilt, surface roughness and quality, film thickness and deposition rate, optical band gap, and atomic spacing with k-Space thin-film metrology tools.

k-Space tools are used worldwide in both research and full production environments. And we offer the best technical support in the industry.

www.k-space.com

kSA

k-space.com

Best-in-Class MOCVD Reactors. Exceptionally Stable Performance.

Featuring unique chamber concepts and robust reactor design, Taiyo Nippon Sanso offers MOCVD reactors that can be used flexibly for research, small-scale production, or high-volume manufacturing. Taiyo Nippon Sanso technology enables fabrication of superior quality AlGaN for UV light emission as well as enriched indium content InGaN films for microLEDs.

TAIYO NIPPON SANSO CORPORATION (TNSC) was the first company to develop and introduce commercial metal organic chemical vapor deposition (MOCVD) systems to produce compound semiconductors utilized in LEDs, lasers, and high-performance electronics for applications such as mobile phones, advanced lighting, and optical communications systems.

TNSC's product lineup includes:

- UR Series Reactors for Mass Production of GaN and related alloy processing for wafer diameters up to 200 mm.
- SR Series Reactors for Research and Small-Scale Production of GaN and related alloy processing with integrated low vapor pressure source delivery capability for novel alloys (e.g., $Al_xSc_{1-x}N$) for wafer diameters up to 150 mm.
- FR Series Reactors for Research and Small-Scale Production of Ga_2O_3 and related alloy processing for wafer diameters up to 100 mm.
- BRC/BMC Series Reactors for Research and Mass Production GaAs, InP, and related alloy processing for wafer diameters up to 150 mm.

www.tnsc-innovation.com

TAIYO NIPPON SANSO

CORPORATE PARTNERS DIRECTORY

agnitron technology
Tel: +1 952 937 7505
Email: sales@agnitron.com
www.agnitron.com

AIXTRON
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

APC Brought to you by: LUMINUS
Tel: +1 (408)-429-2774
Email: apc-e@luminus.com
www.luminus.com/products/APC-SiC-MOSFETs

APPLIED ENERGY SYSTEMS
Tel: +001 610-647-8744
info@appliedenergysystems.com
www.appliedenergysystems.com

ARM PURIFICATION
BY APPLIED ENERGY SYSTEMS
Tel: 1 610-647-8744
purification@appliedenergysystems.com
www.armpurification.com

BRUKER
Tel: +44 (0)191 332 4700
Fax: +44 (0)191 332 4800
sales.semi@bruker.com
www.bruker.com

CS CLEAN SOLUTIONS
Tel No: +49 (89) 96 24 00-0
Fax No: +49 (89) 96 24 00-122
Email: sales@csclean.com
www.csclean.com

MBE Komponenten | Dr. Eberl
www.mbe-komponenten.de

ECM GREENTECH
GORDON BANISH
586-945-3606 | gordonbanish@ecm-usa.com
WAFER PROCESSING FURNACES
www.ecm-usa.com/greentech

Efab
Tel: +886 4 2534-7800
Fax: +886 4 2534-8869
Email: sales@efab.com.tw
www.efab.com.tw

evatec process systems
Tel: + 41 81 403 8000
Fax: + 41 81 403 8001
www.evatecnet.com

Freiberg Instruments
Driven by Innovation
www.freiberginstruments.com

Greene Tweed
SEALS | CONNECTORS | COMPONENTS
gtweed.com

HAMAMATSU
PHOTON IS OUR BUSINESS
www.hamamatsu.com

HORIBA
Tel: +1 732 494 8660
joanne.lowy@horiba.com
www.horiba.com/scientific

III/V-Reclaim
Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.com

kSA
k-Space Associates, Inc.
Email: requestinfo@k-space.com
www.k-space.com

nel®
Tel: + 1 203 949 8697
Email: info@nelhydrogen.com
www.nelhydrogen.com

Experience the Power of Connected Thinking
onto innovation
ontoinnovation.com | info@ontoinnovation.com

RABOUTET SA
T. +33 (0)4 50 98 15 18
info@raboutet.fr
www.raboutet.fr

RIBER
www.riber.com

TAIYO NIPPON SANSO
Tel: + 1 908-403-3304
Email: info@tnsc-innovation.com
www.tnsc-innovation.com

Temescal
Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

Create Future! TES Technology Engine of Science
Tel: +82 10 9671 9675
Email: oesales@hites.co.kr
www.www.hites.co.kr

Showcase to the Compound Semiconductor industry for 12 months

COMPOUND SEMICONDUCTOR MAGAZINE is the primary information resource for professionals working with compound semiconductor materials and devices.

Each issue of the magazine is distributed in print and digitally to over 60,000 professionals worldwide.

With the largest and most diverse global audience of qualified buyers served by any compound semiconductor focused magazine, secure a corporate partnership and buyers guide entry and receive 12 months of promotion and exposure to the compound semiconductor industry across the magazine portfolio including:

- 12 months of promotion in nine issues of the print and digital versions featuring your company logo and company details
- 12 months of promotion and exposure on the Compound Semiconductor website compoundsemiconductor.net featuring a Buyers Guide entry and hyperlinked company logo
- Sponsorship of one e-news alerts sent out to over 60,000 industry professionals with text and a standard web banner.

Ranjodh Shergill
T: +44 (0)2476 718970
E: ranjodh Shergill@angelbc.com

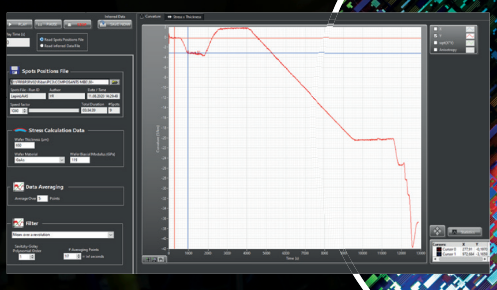
Solutions for Compound **semiconductor epitaxy**

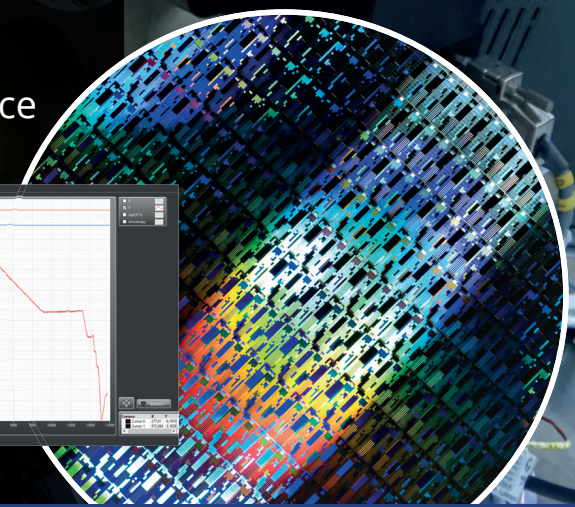
In situ real time curvature

RIBER
EZ-CURVE®

Tool for process monitoring: yield enhancer

- In situ measurements of bow, stress and curvature
- Real time detection of growth events
- Comparison with reference curve





RIBER

INNOVATIVE SOLUTIONS FOR SEMICONDUCTOR INDUSTRY

info@riber.com
www.riber.com