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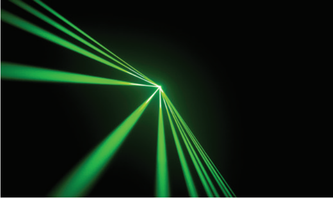

IEDM: Improving the performance of GaN

Increasing the spectral coverage of SLEDs

Printing GaN transistors on silicon CMOS

Could this be the first silicon and CS foundry?

EpiGaN

GaN-on-silicon: Primed for RF power

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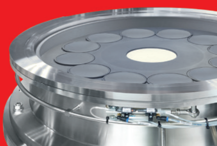

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Viewpoint

By Dr Richard Stevenson, Editor

In the right place at the right time

OFTEN it's a combination of luck and judgement that can lead to being in the right place at the right time.

That's probably the case for the recently reformed Newport Wafer Fab. This time around, its creation results from Infineon's decision to part with this South Wales facility and put it up for sale.

Credit is due to those that are leading the site for grabbing the opportunity. They have raised the investment to buy it, secured a two-year supply deal with Infineon, and had the vision to see great opportunity, thanks in part to be able to sit at the heart of the newly-forming compound semiconductor cluster (see p.28 for details).

The challenge, now, is to make a success of this venture, and form the world's first foundry that processes both silicon wafers and compound-semiconductor-on-silicon wafers.

Today this foundry is just processing silicon, and the obvious place to begin the foray into the compounds is the processing of GaN-on-silicon epiwafers. The site has a legacy in this material system, stretching back to the days when it was owned by International Rectifier.

Getting a foothold in the sector would be a timely move, given the great future that lies ahead for GaN as a key material for both power electronics and RF devices. And although there could be battles surrounding IP, as this is predominantly bound up in the epi, Newport Wafer Fab should be able to steer clear of the courts.

Over the coming months one of the goals for the leaders at Newport Wafer Fab will be trying to figure out what other types of compound-semiconductor-on-silicon technologies could provide a good fit for their foundry. There are options on the opto side. One is silicon photonics, a market that is tipped for explosive growth, and there is the possibility of processing GaN-on-silicon LEDs.

In addition, there could be exciting new technologies emerging from the cluster. With Newport Wafer Fab – and IQE just a few miles down the road – a supply chain is forming that could help to spur the success of any number of start-ups with exciting new ideas.

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International team offers one-stop-shop for InP PICs

Global Communication Semiconductors (GCS), a US compound semiconductor wafer fabrication foundry; Intengent, a Canadian consultancy in III-V photonics; and VLC Photonics (VLC), a photonic integrated circuit (PIC) design house based in Spain, will jointly offer fabless development into production services for customised PICs in InP.

GCS provides a broad range of wafer foundry services, based on a proprietary regrowth-free process in InP. Originally developed as a state-of-the-art Opto and heterojunction bipolar transistor (HBT) processes, it also allows for prototyping and volume-scalable production of PICs.

The key enabler is a photonic integration platform that is compatible with the foundry's regrowth-free process and yet suitable for a variety of applications. Intengent has developed such a platform, termed Taper Assisted Vertical Integration (TAVI), which is regrowth-free, based on the GCS process, and enables for decoupling of epitaxial growth and wafer fabrication. TAVI covers many PIC applications, including those in growing and emerging markets, like optical interconnects and switching markets.

It also offers complimentary solutions to silicon photonics, which is considered by many the technology of choice for a high-scale integration but lacks amplifying, lasing, and other functions naturally implementable in InP. In a three-way partnership with GCS and VLC, Intengent is working towards making TAVI a generic platform while preserving its flexibility and openness to PIC customisation.

VLC Photonics is an expert in generic photonic integration platforms and, as a fabless and independent design house for PICs, has been developing design libraries and process design kits (PDK) for different foundry platforms and customers.

A PDK for the TAVI platform drastically reduces the PIC design effort and risk, by shifting the focus towards circuit level simulations. The evolving PDK is based on a number of verified active and passive building blocks, and is already used in commercial PIC designs carried out by the partnership.

Brian Ann, CEO of GCS, says: "Our well-established Opto and RFIC processes have great synergies with the TAVI PIC platform. Our 4-inch, and 6-inch wafer capability as well, based on a commercially supplied one-step-growth epitaxy, creates a unique opportunity for PICs in InP. We truly believe that the GCS – Intengent – VLC partnership can fully utilise this opportunity and generate a significant business for PICs in various markets.

"By leveraging the infrastructure and expertise that we have gained through years of serving high-volume RF electronics and optoelectronics markets, this partnership offers time- and cost-efficient PIC development into production".

Valery Tolstikhin, CEO of Intengent, adds: "GCS is an advanced III-V foundry with a high InP wafer throughout both in RF electronics and optoelectronics markets. The TAVI platform takes advantage of GCS' process maturity and extends it to PICs in InP. To make the technology suitable for a fabless PIC development, one more thing is needed: the PDK.

This is where VLC comes in, bringing experience in PIC design and characterisation. The fabrication process, the integration platform, and the PDK, together, make a versatile generic platform for PICs in InP that allows the end users to access the commercial-grade technology under the fabless model".

GaN technology helps to shrink DC-DC converter

OSAKA-BASED Diamond Electric has developed a business card-sized, thin isolated bi-directional DC-DC converter (IBDC) that uses GaN technology. in recent years, requirements of large-capacity batteries for EVs and smart grids require rechargeable batteries to have higher voltages. Therefore, demands are growing for a higher-level isolation of DC-DC converters to ensure safety and meet safety standards. In response, Diamond Electric has developed the new IBDC by using a patent-pending control technology. The IBDC (which combines both charger and discharger circuits) has an output power -1,000 to +1,000 W (bidirectional), a voltage range of 270 to 330 V, and a current range -3.7 to +3.7 A.

The ultra-compact IBDC (93.5 mm x 60 mm x 10.5 mm excluding control circuit and heatsink) combines high-frequency switching technology (up to 2 MHz) with GaN power semiconductors to achieve a conversion efficiency up to 95 percent. By using these technologies, the company expects to downsize the final product to 25 percent of other existing models.

SMI gets DoE grant for gallium oxide research

STRUCTURED MATERIALS INDUSTRIES (SMI) has received a US Department of Energy Small Business Innovation Research (SBIR) award where it will evaluate the energy bandgap tunability of Ga_2O_3 by alloying the material with Al_2O_3 and In_2O_3.

The ongoing effort is being conducted in collaboration with Lisa Porter and Robert Davis of Carnegie Mellon University. An assessment of the Ga_2O_3 energy bandgap tunability is required in order to increase the selectivity of sensors for UVA, UVB, and UVC bands, which is a focus of the project. The materials are grown using MOCVD.

SMI research scientist and leader of Ga_2O_3 efforts, Serdal Okur commented: "Tuning the energy gap of Ga_2O_3 will establish an even broader range of applications for the material, such as graded heterostructures for optoelectronic devices, photo diodes with tunable cutoff wavelengths, as well as optical filters with tunable transmission range, to name just a few.

"We believe that In_2O_3 and Al_2O_3 are good candidates to realise the bandgap engineering of Ga_2O_3. Additionally, we decided to use the MOCVD technique as it offers many advantages for ultimate device fabrication, including high growth rates, conformal deposition over device topography, and the capability for scale-up to high volume production."

Okur added: "In our current DOE project, SMI will demonstrate Gallium Oxide, Aluminum Gallium Oxide, and Indium Gallium Oxide based UV sensors that cover the whole UV spectrum. These devices will be very important to detect UV photons from liquid Ar and Xe scintillators, both at 128 and 175 nm, respectively, in particle physics experiments. SMI will further develop the MOCVD growth parameters and hardware to extend control of energy bandgap tuning of Ga_2O_3 with good quality crystals. The company, in collaboration with CMU, will continue to explore the potential of large-area Ga_2O_3 based alloys with the intention of making the aforementioned sensors more economical and readily available than competing materials in UV sensing applications."

SMI's proprietary rotating disc oxide MOCVD reactor technology will be used in this project to demonstrate that Ga_2O_3 films can be deposited uniformly on large-area substrates.

SMI, with over 10 MOCVD and ALD process demonstration tools in-house, has extensive result oriented experience in providing materials, hardware, and device assistance to other businesses as well as research organisations.

We are a leading provider of thin film research and development deposition systems for electronic, optical and electro-optic device fabrication.

Plessey shows microLED-based AR and VR at CES 2018

PLESSEY SEMICONDUCTORS has successfully demonstrated how its monolithic microLED technology can be used to deliver the next-generation of Head-Up Displays (HUDs), enabling new AR and VR applications. MicroLEDs are emerging as the only technology that can provide high luminance in a small format.

All leading manufacturers of wearable technologies are currently pursuing manufactures that can deliver an ideal microLED solution. With this demonstrator, Plessey has confirmed it is ready to enable its partners to move into production of a monolithic display based on microLEDs using the company's proprietary GaN-on-silicon approach.

Commenting at CES 2018, Keith Strickland, CTO at Plessey, stated: "Monolithic microLED technology is the only viable solution that can enable products that are not only compact enough to be worn without restricting

the overall experience for AR and VR applications and in HUDs, but also provide the size, weight, power and luminance needed."

The demonstrator, which has been produced in collaboration with Artemis Optical, combines Plessey's monolithic display, based on an array of microLEDs integrated alongside an active matrix backplane, with the patented film technology and a single lens arrangement from Artemis.

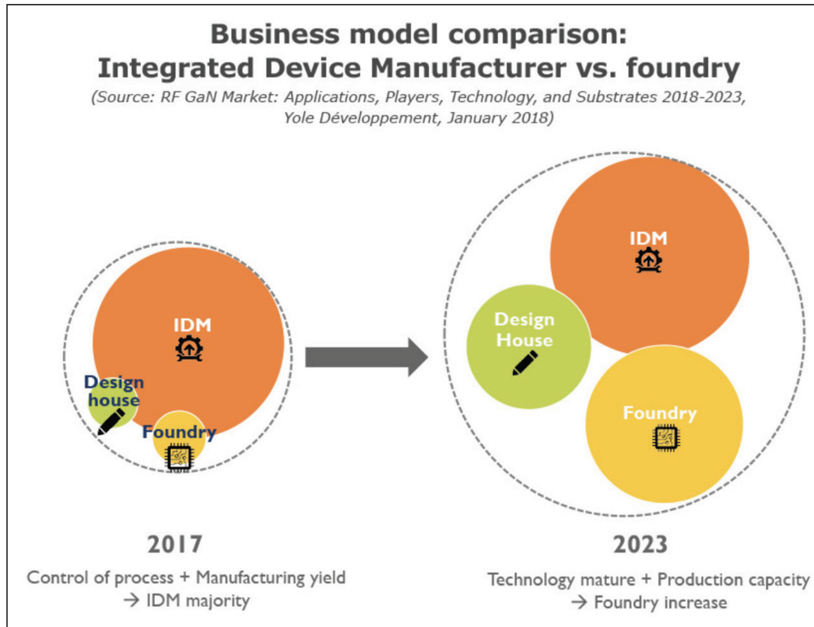
The combination of technologies removes ambient light in the wavelength matching the microLED display output, resulting in a HUD that delivers very high display brightness with low power consumption, in a format that is considerably smaller than existing HUD designs, yet still offers significant cost savings.

During CES 2018, Plessey Semiconductor and Artemis Optical presented the demonstrator to many leading companies developing VR and AR electronics. Headsets and eyewear outfitted for AR and VR applications are set for record sales this year of $1.2 billion in the US market alone, according to the Consumer Technology Association (CTA).

Plessey's was recently announced as 'Company of the Year' at the Elektra Awards 2017, an annual awards programme organised by the publisher of UK-based *Electronics Weekly* magazine. The highest accolade was awarded to Plessey for its achievements and innovation in the development LEDs using it's GaN-on-silicon technology.

RF GaN market will be boosted by 5G

IN THE LAST COUPLE OF YEARS, the RF GaN market experienced an impressive growth and has reshaped the RF power industry landscape. By the end of 2017, the total RF GaN market was close to $380 million, according to Yole Développement (Yole) in a new report titled *'RF GaN Market: Applica tions, Players, Technology, and Substrates 2018-2023'*.



According to the analysts, the penetration rate in various markets, and in particular telecom and defence applications, had a breakout period in the last two years: CAGR in these two markets is more than 20 percent.

Yole says that another strong boost will occur around 2019–2020, led by the implementation of 5G networks. The total RF GaN market size will be a factor of 3.4 larger by the end of 2023, posting a 22.9 percent CAGR from 2017-2023 Yole's RF GaN market report describes GaN's presence and development in different markets, including wireless infrastructure, defence and aerospace, satellite communication, wired broadband, both in coaxial cables used in cable TV (CATV) and fibre-to-the-home, and other industrial, scientific and medical radio band applications. It also offers a complete analysis covering different emerging GaN players: Sumitomo Electric, Wolfspeed, and Qorvo, These companies and more are part of Yole's study.

2017 has been undoubtedly a good year. Recognised by the industrial players, the RF GaN technology is becoming the current mainstream within the RF industry. Mostly dominated by the IDM companies, Sumitomo, Qorvo and Cree, the industry is at a critical stage. Tomorrow might be different with the penetration of the foundries. Since Yole's previous technology and market report, there has been the failed acquisition of Wolfspeed by Infineon. Wolfspeed is now reintegrated into Cree's business. Also, Ampleon announced an acquisition offer by a Chinese LED company, named Aurora Sapphire. This company is a competitor of San'an Optoelectronics. In addition, companies like M/A-COM and Sumitomo have begun using silver sintering as the die attach material, it helps thermal control and improves the device quality. It's been confirmed that the next step will be using pure copper as flange material for the package.

In the coming years, Yole Développement sees telecom and defence markets acting as the mainstay of the industry. The telecom market, thanks to the increasing development pace of 5G networks, will bring a huge opportunity for GaN devices beginning in 2018. Compared to existing silicon LDMOS and GaAs solutions, GaN devices are able to deliver the power/efficiency level required for next generation high frequency telecom networks. Also, GaN's broadband capability is one of the key elements for enabling important new technologies, such as multi-band carrier aggregation. GaN HEMTs have been the candidate technology for future macro base station power amplifiers.

Yole Développement estimates most sub-6 GHz macro network cell implementation will use GaN devices because LDMOS can no longer hold up at such high frequencies and GaAs is not optimum for high power applications. However, because small cells do not need such high power existing technology like GaAs still has advantages.

At the same time, market volumes will increase faster because higher frequencies reduce the coverage of each base station, and thus more transistors will be implemented.

The defence market has been the major driving force for GaN development in the past decades. Originating in the US Department of defence, GaN devices have been implemented in new generation aerial and ground radars. GaN's high power capability improves detection range and resolution, and designers are becoming increasingly familiar with this new technology.

Nevertheless, this military-related technology is very sensitive. And as GaN devices are becoming popular in defence applications, the development of the nonmilitary part could be affected. This is especially true in terms of mergers and acquisitions. Governments could block deals if businesses target military applications, as in Aixtron's acquisition by FGC Investment Fund, or Wolfspeed's by Infineon.

GaN transistor prices are still relatively high today. According to Yole's analysts, in the near future, more and more players should penetrate the market ensuring volumes increase and prices decrease. In parallel, Yole highlights significant issues related to the packaging.

An effort in packaging could also strongly bring price reduction to an attractive level. Today, more players are choosing a plastic package: the industry is showing some movement on new types of packaging material and new die attach methods.

Startup demonstrates ultra-high resolution micro-LED micro-displays

JBD, a Hong Kong based technology start up, reports that its researchers have created the first monochromatic red, green and blue active matrix micro-LED (AMμLED; also referred to as mLED or ILED) micro-displays with greater than 5,000 dpi pixel density by utilizing a wafer scale monolithic hybrid integration process.

The company said it believes it's AMμLED micro-displays have the highest pixel density of its kind and offer high brightness and contrast ratios at low power consumption and in a small device footprint.

The company also claims its technology demonstrates a clear path for mass production of AMμLED micro-displays using existing mature semiconductor infrastructure and processes for emerging applications such as wearable electronics and augmented reality (AR) headsets.

Compared with existing technologies such as LCD and OLED micro-displays, micro-LED micro-displays offer significant performance improvements in brightness/contrast, energy efficiency, response time and reliability. Currently, micro display panels are typically hybrids of micro-LED arrays with CMOS active matrix (AM) driver ICs that utilize flip-chip technology. However, several drawbacks exist in this manufacturing method: first, flip-chip processes typically suffer from low throughput, resulting in higher costs compared with other semiconductor technologies; second, the built-in stress of producing hybrid chips due to thermal mismatch between the LED epi substrate and silicon substrate of ICs during the bonding process may lead to manufacturing yield loss and long-term reliability issues.

Furthermore, manufacturers have found that the alignment accuracy of bonding equipment can be a limiting factor that makes it difficult to push the pixel pitch down to a few microns, which is highly desired for some applications such as AR, the company stated.

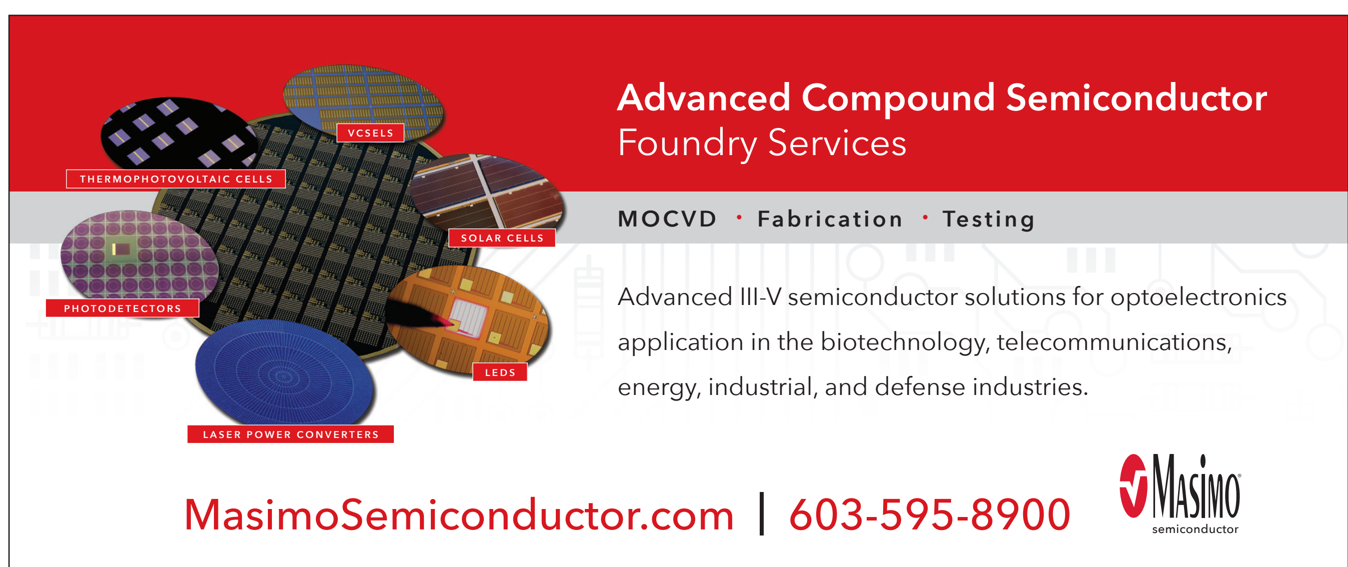
To address those challenges, JBD has developed a new monolithic hybrid integration technology. Through wafer bonding followed by substrate removal processes, JBD said it has successfully transferred the functional compound semiconductor epi layers onto silicon IC wafers. Such wafer-level blank epi transfer eliminates the need of precise alignment as required in flip-chip based processes. JBD said its approach provides higher throughput, making it suitable for large volume and low-cost production.

JBD's epi-on-IC templates are subsequently subjected to the standard semiconductor fabrication processes with high alignment accuracy to produce monolithic hybrid optoelectronics integrated circuit (OEIC) chips.

Using JBD's monolithic hybrid integration technology, monochromatic red, green and blue micro-LED micro-displays have been successfully demonstrated on silicon based active matrix micro-display IC backplanes.

The company's AMμLED micro-displays have achieved high resolution with 5 μm pixel pitch. The brightness of the AMμLED micro-display (green) in test circuits well exceeds 5×10^5 cd/m^2, representing an improvement of over 500-times compared to the existing self-emissive micro-displays.

JBD said that it believes with further optimization of the device design and fabrication process, its solution can lead to AMμLED micro-displays with resolution of over 10,000 dpi, which will make it the most desirable and promising solution for various wearable electronics and AR applications.



Hybrid headlight LEDs: Lighting up the way ahead?

WITH fatal traffic incidents more likely to occur at night, advances in automotive lighting – in particular smart headlighting driven by multi-pixel LED technology – will become key to making the roads safer for drivers and passengers in the future, says Osram Opto Semiconductors.

Historically, traditional headlighting in the automotive industry has had its challenges. For example, driving with low beam so as not to dazzle other road users can increase discomfort and increase risk in complex driving situations. Popular adaptive automotive headlighting today uses a matrix of LEDs, which are operated with individually

controlled chips for each illuminated area. They operate at full energy consumption, but simply 'mask out' the LEDs that are not needed with a mechanical function.

The trend today is towards LED chips with micro-structured pixels, which can shine, or be turned off individually. The high resolution – a leap from 84 pixels to more than 1000 – delivers a smooth and dynamic driving beam. The evolution of multi-pixel LED technology has initiated a giant leap in the development of smart lighting systems, which have the most viable applications in the automotive industry.

The development of the world's first hybrid LED (announced in September 2017), based on the conclusions from the FMER-project μAFS led by Osram Opto Semiconductors, enables enough fine resolution and precise control to realise smart, adaptive headlighting that is highly energy efficient, scalable and compact (1024 pixel in just 4 mm by 4 mm).

In the μAFS research project (pronounced 'micro AFS'), a group of German companies worked for three and a half years until September 2016 on the groundwork for a new class of adaptive front lighting systems achieving several thousand light segments based on energy-efficient highly integrated LED headlamps.

"Osram Opto Semiconductors is continuously shaping the future of light day by day, and night by night. With the first commercially-viable multi-pixel LED for smart headlighting in automotive vehicles, we hope to help improve safety records as well as make driving a better experience, with much more control in the driver's hands," commented Stefan Groetsch, principal key expert for applications at Osram Opto Semiconductors.

Eviyos is the first prototype of a hybrid LED that combines a light emitting diode array chip and an individual silicon pixel control IC. Several thousand LEDs in the Eviyos, each just 0.125 mm x 0.125 mm in size, receive their brightness and current setting from an electronic control unit merging various sensor information and the camera input.

The camera acts as the 'eyes' of the system, capturing the information about the surrounding environment, and forwarding it to the controller. The controller processes the image data information and forwards a suitably adapted light distribution pattern to the pixels in digital format. As well as exceptional adaptive capability, Eviyos demonstrates energy efficiency thanks to an active electronic control, which ensures that the only pixels turned on, are only those that are needed at that moment in time.

Finisar co-founder retires

FINISAR, a maker of optical subsystems and components for fibre optic communications, has announced the retirement of chairman and CEO Jerry Rawls and the appointment of Michael Hurlston as CEO.

Hurlston and Rawls will work together to ensure a smooth transition. Rawls will continue to serve as a director of the company. The company's lead director Robert Stephens has been appointed chairman of the board.

"After a thorough and thoughtful search process, we are pleased to welcome Michael Hurlston to Finisar as CEO and a member of the Board of Directors," said Robert Stephens, Finisar's chairman of the board of Directors. "Michael has broad experience as a highly-successful technology industry executive and we know Michael is the right leader to build on our success and market-leading position."

"Under Jerry's leadership, Finisar has grown from its founding in Quonset hut in Menlo Park, California to a world-leading optics company with cutting-edge products and approximately $1.4 billion in revenues in its most recently completed fiscal year. We are deeply grateful to Jerry for his innumerable contributions to Finisar's growth and success to-date and are confident that he has positioned the Company solidly for the great opportunities in our industry today."

Rawls said: "Michael's experience, proven technical skills, and leadership abilities will serve Finisar, our customers, employees, and stockholders very well. At Finisar, we have built a great company with fantastic employees dedicated to serving our customers' needs and developing world-leading, cutting-edge technology products. I am confident that Michael is the right person to lead us to even greater success."

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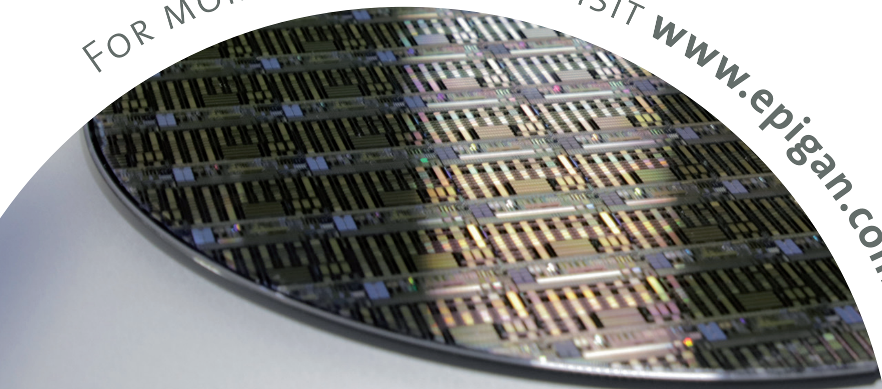
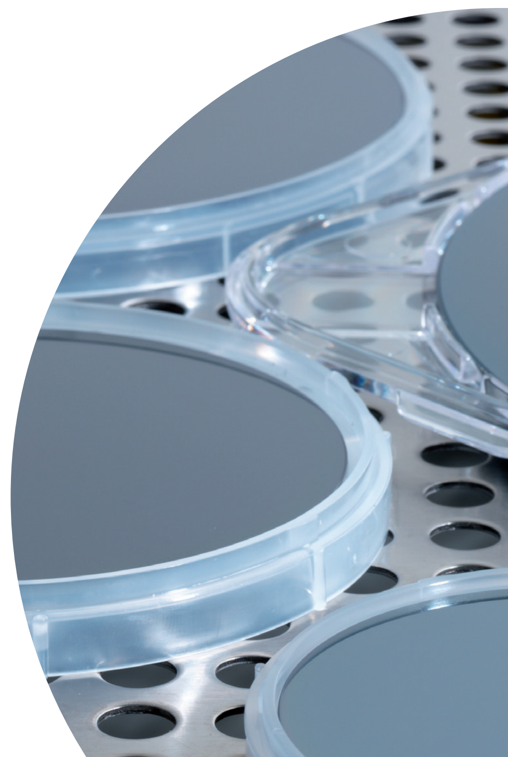




Lockheed Martin demonstrates GaN-based radar

LOCKHEED MARTIN has connected key components of its GaN-based Aegis Ashore and Long Range Discrimination Radar (LRDR) technologies, validating the ability to increase operational performance, efficiency and reliability of Aegis Ashore.

"Connecting these systems is more than a technological advantage – it's a way to provide the warfighter with earlier intelligence and expanded situational awareness," said Tony DeSimone, vice president and chief engineer of Lockheed Martin Integrated Warfare Systems and Sensors.

"Integration of these technologies allows us to deliver the most advanced solid-state radar system in LRDR with the proven tested capability of Aegis. For the warfighter this combination provides an increased capability, in terms of additional performance and reaction time, to safely protect the people and nations they defend."

Lockheed Martin Solid State Radar (SSR) is a scalable GaN-based radar building block, which in addition to cutting edge performance provides increased efficiency and reliability.

The Department of Defense's newest Ballistic Missile Defense sensor, LRDR, will use thousands of Lockheed Martin SSR building blocks to provide enhanced target acquisition, tracking and discrimination data to the US Ballistic Missile Defense System. LRDR completed its critical design review in 2017 and is on track to be operational in Alaska in 2020.

Connecting the two mature systems, amounts to a low risk 'technology refresh' of the legacy SPY-1 antenna, according to the company, resulting in: ability to detect targets at longer distances; ability to combat larger numbers of targets simultaneously; additional target engagement opportunities; higher performance in complicated land environments; minimised interference with civilian or military radio emitters and receivers; and increased use of the new SM-3 Block IIA missile's performance Aegis Ashore is the land-based ballistic missile defence adaptation of the Aegis Combat System, currently based in Romania and soon to be fielded in Poland.

The research and development demonstration proved that current and future versions of Aegis can simultaneously command tasking of the Lockheed Martin SSR and receive target tracks from the radar. The next phase of activity is to demonstrate simulated missile engagements with live tracking, scheduled for the first half of 2018.

These tests build on multiple previous demonstrations in 2015 and 2016, in which Aegis software variant Baseline 9 already tracked live targets using a prototype version of Lockheed Martin SSR hardware powered by multi-purpose Fujitsu GaN from Japan.

The Aegis software has evolved over time and is now compatible with multiple radars. Recently, Australia and Spain selected Aegis configurations featuring their own solid-state radars.

Weaving existing systems together is becoming more common to stay ahead of threats efficiently, by leveraging prior or concurrent investments in advanced technology.

"The Aegis Combat System is adaptable and flexible to address warfighting needs, which is one of the reasons the system is so widely used around the world," said Michele Evans, vice president and general manager of Lockheed Martin Integrated Warfare Systems and Sensors.

"As our customers look to update their technology with the help of their industrial bases, they are increasingly choosing alternative radars to equip their platforms. In challenging threat environments, we can deliver advanced capability at lower cost if we can be flexible and connect a variety of existing technologies."

IQE purchases QPC patents

IQE, global supplier of advanced wafer products and services has secured purchase and assignment of patents from Luxtalktek through its subsidiary, NanoGaN.

The portfolio of 54 patents secured covers a range of novel technologies and applications based mainly on Quasi Photonic Crystals (QPC). This advanced materials technology complements the Group's organic development of NanoImprint Lithography ("NIL"), and broadens the potential application of NIL beyond IQE's current focus on advanced DFB lasers.

The patents acquired have applications in o ptical components including VCSEL and edge emitting lasers,modulators, silicon photonics, fibre optic systems, micro LED displays, image sensors including Diffractive Optical Elements (DOE) and biosensors. NanoGan has agreed to a one-off payment of (USD) $500,000 for the purchase.

IQE Chief Executive, Dr Drew Nelson said: "Over the last few years, IQE has developed an exciting and strong IP portfolio, which, coupled with the expertise and manufacturing capability to commercialise these new materials technologies have uniquely positioned IQE as the clear global leader in providing advanced compound semiconductor technology solutions. This significant addition to our IP portfolio provides the Group with additional competitive advantages that will secure our entry and maintain our leadership across a range of new and emerging technology applications, and offer our customers access to a unique portfolio of materials expertise."

Transphorm's GaN chips move into PC gaming

TRANSPHORM, a maker of hi-res, high voltage GaN semiconductors has confirmed that its GaN FETs are used in Corsair's new AX1600i Power Supply Unit (PSU).

Corsair supplies the gaming community with high-performance products used in custom PCs. The company's latest product establishes a new class of AC-to-DC PSUs, as it is the first to use GaN and achieves 99 percent efficiency.

Transphorm's GaN increases the PSU's power output by 6.5 percent in an 11 percent smaller package at the same temperature.

The AX1600i uses Transphorm's TPH3205WS 650 V FETs in a bridgeless totem-pole power factor correction (PFC) — the topology that complements GaN's performance and efficiency potential. With an increase of 6 percent within this topology, Corsair's PSU efficiency now earns a better-than an 80 PLUS Titanium rating. (Previous Corsair power supplies used silicon superjunction (SJ) MOSFETs in a 2-phased interleaved PFC, reaching 93 percent efficiency.)

"Our objective was to take an already award-winning PSU and make it better," explained Jon Gerow, PSU R&D Manager, Corsair. "We aimed to maximise output from any PC running on a 115V mains. To do this, we had to adopt innovative methods and materials.

Transphorm's GaN ultimately gave us the boost in performance, efficiency and size we wanted along with the high quality and reliability we needed to confidently release the AX1600i to our customers."

After researching market-available GaN devices, Corsair chose Transphorm's FETs as they enabled the AX1600i to deliver new benchmarks compared to the previous AX1500i. The power output of 1600 W, 6.5 percent increase; size reduction: 20 mm shorter, 11 percent smaller; thermal impact: equivalent 50°C continuous output; and audible noise impact: slower fan speed with less noise at full load.

Corsair noted that Transphorm's packaging also played a role in its selection process. The TPH3205WS comes in a commonly used TO-247 package, reducing some design complexity.

"Corsair's brand is built on products that give our customers a competitive edge, inside and outside of the gaming PC. And, Transphorm's GaN presented an invaluable opportunity to advance the PSU – to make it smaller, quieter, cooler, and, most importantly, more powerful," added Gerow.

Founded in 1994, Corsair supplies high-performance products purchased primarily by PC gaming enthusiasts who build their own PCs or buy pre-assembled customised systems.

Seoul Semi achieves record $1.04 billion revenues

LED COMPANY Seoul Semiconductor has announced 2017 fiscal year consolidated revenues of $1.04 billion and an operating profit of $92 million, an increase in 16 percent and 71 percent year-on-year respectively.

The rise in revenue for the general lighting segment was largely due to an increase in sales of 220 V and 370 V Acrich MJT products for household and industrial applications. Other notable revenue increases were reported for WICOP, an innovative product line of package-less LEDs, as well as for the Acrich NanoDriver, which incorporates step drive methods that achieve results greater than those of conventional SMPS technology.

In addition to offering these differentiated technologies, Seoul expects its SunLike natural spectrum LED technology, which may offer health benefits for human eyes, to lead the future of LED lighting and become a large contributor to the future sales and profit for the company. Researchers who won the Nobel Prize in 2017 were recognised for their new findings of the impact of light on circadian rhythm in humans.

This has proven to be an important topic in society and generated great attention for Charles Czeisler, the Harvard professor that has dedicated his research to this particular area. He is now conducting research study with NASA on how light affects the circadian rhythms of astronauts.

According to new research, myopia (near-sightedness) increased from 20 percent in the 1950s to 80 percent in 2010 among populations in Asia. Fluorescent lights and conventional LED light sources emit a strong blue light that is known to cause eye fatigue, which may later result in retinal damage.

Seoul Semiconductor, together with Toshiba Materials of Japan, has jointly developed SunLike natural spectrum LED technology, which provides lighting conditions most similar to actual sun light and can be seen as a solution that helps

to protect human eyes from this potential damage.

The company provided a revenue guidance of KrW 270 to 290 billion for the first quarter of 2018. This figure is in range of 5 percent to 13 percent on a year-over-year basis. Although first quarter is normally considered to be an off-season, the company is showing a positive outlook for growth from last year for this 2018 fiscal year.

The ultimate magnetic sensor?

A new UK project, CS-MAGIC, is set to thrust wide bangdap magnetic field sensors into the commercial limelight, reports Rebecca Pool.

LATE LAST YEAR, joint IQE-Cardiff University venture, the Compound Semiconductor Centre, bagged just over £350,000 in UK government funds to develop ultra-sensitive magneto-sensors with integrated electronics based on GaAs and GaN materials.

The InnovateUK award to the new CS-MAGIC project comes at a time when industry analysts predict astonishing growth in the magnetic field sensor sector. MarketsandMarkets forecasts that today's $3 billion global market will mushroom to more than $5 billion by 2023, with a compound annual growth rate of 8.8 percent. Similarly, Technavio forecasts a 10 percent CAGR from now until 2020.

Right now, demand is largely coming from the automotive industry, requiring highly sensitive, robust Hall Effect sensors to map ever-smaller magnetic fields across larger temperature ranges in engine control management, anti-lock braking systems and more. However, the sensors are increasingly demanded in aerospace and industrial sectors to measure rotation, speed and linear position.

As Mohamed Missous, Professor of Semiconductor Devices and Materials at the University of Manchester and one of the award recipients, puts it: "We're now developing sensors for harsher environments than ever before."

"When today's commercially available silicon Hall Effect integrated circuits reach 150 °C, they just stop working, so devices made of III-V semiconductors are attracting a great deal of interest," he adds.

What's more, conventional silicon-based devices can also suffer from low magnetic field sensitivity, limited operating frequency and temperature ranges, and high power consumption. So, for his part, Missous has been developing Quantum-Well Hall ICs based on GaAs-InGaAs-AlGaAs systems, having also founded UK-based Advanced Hall Sensors (AHS) to take his 2DEG Hall sensors to market.

Devices are fabricated using MBE to deposit the thin films onto GaAs wafers, which are then processed into Hall sensors via subsequent lithography, etching, annealing and metal evaporation steps before being sliced and packaged.

Crucially, quantum wells are generated by inserting a thin InGaAs film between two thicker AlGaAs layers. Electrons – in the form of a two-dimensional gas or 2DEG – are confined within this thinner layer, rather than being left to roam free in conventional Hall Effect sensors, boosting electronic properties.

Indeed, silicon-based linear Hall ICs can detect magnetic fields down to around 600 nanoTesla in a 10 Hz bandwidth. But AHS has already produced quantum well Hall 2DEG GaAs-based devices that detect magnetic fields as low as 177 nT in a 10 Hz bandwidth. And while the former devices have a maximum cut-off frequency of 10 kHz, the wide bandgap versions stretch this figure to 200 kHz.

To date, AHS has already shipped more than 15 million discrete sensors, but thanks to the latest funds, Missous and his company now intend to commercialise single-chip sensors with a wider dynamic range that can operate in harsher environments.

"Our all-integrated chip will be a single chip that has the quantum well Hall effect sensor in it with all the drive electronics," says the researcher. "This will be

totally new; a single chip GaAs Hall Effect sensor just doesn't exist right now."

The drive electronics will also be based on GaAs, which means the entire chip will be more radiation resistant and will operate across a wider temperature range than existing devices. Indeed, on temperature range, Missous is aiming for -200°C to 200°C with the single chip, while today's silicon devices cover -50°C to 150°C.

Right now, AHS is working with industry partners, TWI and Renishaw, to develop a generic structure based on GaAs-InGaAs-AlGaAs layers. This should be confirmed come April next year, and by the following November, the sampling of packaged devices should be underway.

"We want to produce generic ICs that operate over the higher temperature range, and once we have achieved this, TWI and Renishaw will test the devices and feedback on performance," says Missous. "We are relying on the companies to do this so we can tailor the chip to whatever they require."

"We do not want a very complicated circuit, but we need to ensure that all the electronics are in sync with the sensor," he adds. "The circuit will work over enormous temperature ranges without losing any sensitivity or functionality across these."

Raising the bar

Meanwhile, in a second strand of the CS-MAGIC project, Petar Igic from the Electronic Systems Design Centre at the University of Swansea is developing what could be described as the next wave of magnetic sensing based on GaN.

Igic has fabricated GaN HEMTs for power applications, but now, with the latest InnovateUK funds, intends to develop discrete sensors based on his magnetic HEMT concept.

"Our aim has been to develop a sensor that is fully compatible with existing HEMT technology," he says. "We don't need different starting materials or extra processing steps but the layout is different to the HEMT so that the device is sensitive to magnetic fields."

Crucially, GaAs-based sensors can operate up to 220 °C, but sensors based on GaN HEMTs could maintain performance up to around 400 °C, subject to, as Igic puts it, 'the development of adequate packaging and soldering'.

Right now Igic is working on proving the concept and optimising device layout, which he hopes will be achieved within the next twelve months. After this, he will be looking to tailor the device for specific applications, and will also be working with packaging companies.

Clearly, CS-MAGIC's GaAs-based Hall sensor is c loser to commercialisation than the second, GaN-based device. But the potential performance gains of GaN in harsh environment applications are undisputed.
According to Igic, initial results indicate that the GaN-based sensor detects magnetic fields as low as 100 nT. What's more, device sensitivity will not change with magnetic fields and high temperatures.

"We cannot beat silicon on price but this GaN device will reach aerospace and automotive applications as it will work at very high temperatures and is less sensitive to radiation," highlights Igic. "We will have to implement the device in standard manufacturing processes, but its unique selling point is that when GaAs stops working, this still is."

GaN: small, efficient and market-ready

After trials, tests and much talk, GaN is set to charge into mainstream markets, reports Rebecca Pool.

FROM INDUSTRY ANALYSTS to Physics Nobel Laureates, myriad compound semiconductor players are asserting that GaN is the material to watch right now.

Late last year, Ana Villamor, from Yole Développement, highlighted how data centres are now adopting GaN products including DC/DC converters with point-of-load supplies at a ‘phenomenal speed’.

Meanwhile, talking at the University of Hyderabad, India, in January, Hiroshi Amano asserted the material will soon be playing a big role in IoT and 5G communications.

For UK-based Dialog Semiconductor, the latest raft of proclamations confirms what company presidents have highlighted in recent months: mainstream market adoption is nigh.

In late 2016, as the company was sampling GaN power ICs in fast charging power adapters, senior vice president of development and strategy, Mark Tyndall, told *Compound Semiconductor*: “When TSMC started to offer GaN as a standard process on six inch wafers, we saw that as a signal that the time was right to enter the market.”

Since this time, the company has been collaborating with TSMC to bring its high voltage GaN power IC plus controller to market. The power management IC, with Dialog’s digital ‘Rapid Charge’ power conversion controller, is designed to deliver more efficient, smaller and higher power density power supplies compared to today’s silicon FETs.

Indeed, the company claims the latest product nearly halves the power loss and size of power supplies, factors that are so very important to the consumer adapter that the mobile communications industry craves for its smartphones, notebooks and more. And right now, pre-production of Dialog’s device is underway, with product launches coming very soon.

“We expect to launch our first GaN power IC this quarter and then our second power IC for consumer power adapters in the middle of this year,” says Tomas Moreno, director of corporate development at Dialog Semiconductor.

Crucially, Moreno reckons this year will be the turning point for GaN, with the consumer adapter sector being the company’s first target market.

“GaN addresses a more than $5 billion market encompassing PCs, TVs, gaming, data centre, automotive, clean energy, industrial and other segments,” he says. “We are focused on the consumer space first, as it is large with very short design cycles, so we can get to scale quickly and send many wafers through our lines.”

“This will really drive down costs... which will in turn mature the technology so the market will continue to adopt GaN,” he adds. “Our goal is to use the consumer power adapter market as a launchpad for other applications.”

Seeing the signs

Moreno reckons overall market adoption is starting to happen, having noted many design-ins, based on GaN devices, in data centres, industrial, and even automotive applications. “We are seeing all this momentum already,” he says.

What's more, he believes market trends, including the shift to USB Type C connectivity and USB Power Delivery as well as increasing dependence on rapid charge batteries, are set to kick-start GaN's entry into the consumer power adapter market.

"We have this window of opportunity where the adapter for your smartphone and the adapter for your PC will be one," he highlights. "And with GaN we can make this universal adapter very, very small."

And while industry players such as Navitas Semiconductor and Innergie, both of the US, have delivered GaN-based 65 W adapters, Moreno reckons Dialog can deliver a system with a lower bill-of-materials.

"Some companies have [delivered] the technology but with topologies that use expensive components," he says. "We are creating a chip that will allow you to get the bill-of-materials costs down and can be implemented more rapidly."

But what about customer concerns over reliability? Moreno thinks these issues are being addressed, highlighting how devices from Dialog and competitors have passed stringent reliability test requirements. In addition, he believes supply chain bottlenecks, namely around epitaxial layer deposition and packaging, are being overcome.

Dialog's manufacturing partners are expected to have the necessary MOCVD reactors, and as he adds: "Consumer applications tend to be lower power and use QFN packaging; there is no bottleneck for this type of packaging."

"Dialog is a strong incumbent in the consumer application space and we are very familiar with this market," he says. "We can bring this technology here with a better performance and a competitive bill of materials."

"Very soon you will have a nice little power supply in your hand that you can carry anywhere," he adds.

GaN on silicon
Primed for RF power

Can GaN-on-silicon move on from just serving 600 V and below power management systems, wireless charging and LIDAR, to win deployment in next-generation RF applications, such as 5G and the Internet of Things?

BY MARKUS BEHET AND JOFF DERLUYN FROM EPIGAN

FOR SEVERAL DECADES, innovations in electronics have tended to draw on silicon and GaAs-based technologies, devices and integrated circuits. Take cellular infrastructure: its increases in complexity from 2G to 4G-LTE have been underpinned by continuous improvements in GaAs HEMTs, HBTs and silicon LDMOS devices.

One downside of all these incumbent semiconductor technologies is that they are now encroaching their theoretical limits. Consequently, any improvement at the system level requires a huge effort by design engineers, and draws on ever increasing developments costs. Given this state of affairs, there is an urgent need for a new RF semiconductor technology to step in and fulfil the promises of 5G RF systems – and it is here that GaN technology comes to the stage.

Wideband GaN technology is definitely not a newbie to the semiconductor market. It is already being deployed in the likes of power supplies and motor drives, which are benefitting from highly efficient 600 V GaN-on-silicon HEMTs. In addition, there are GaN-on-SiC RF products that are being used in base stations, Satcom, military and CATV systems. Due to all this activity, on both of these formats of GaN, the total addressable market in 2017 was worth $400 million.

Another opportunity for revenue growth will come with the dawn of the next generation of cellular infrastructure – 5G. Initial deployments, which will take place by 2020, promise to lead to: peak data rates of 20 Gbit/s; a large number of users or sensing nodes for any given area; a high power efficiency, enabling less power per transmitted bit; a latency of less than 1 ms; and ubiquitous connectivity. This revolution will not only enhance existing telecom services drastically, but enable emerging applications, such as virtual/augmented reality, autonomous cars, massive IoT, and mission critical services.

These changes have led market analysts ABI to argue that 5G should be viewed as a general purpose technology that will act as a catalyst for transformative changes of work processes, and will establish a new set of rules of competitive economic advantages. The impact will be so great, says ABI, that by 2035 it will trigger a global economic output of $12.3 trillion – that's comparable to current levels of annual US consumer spending.

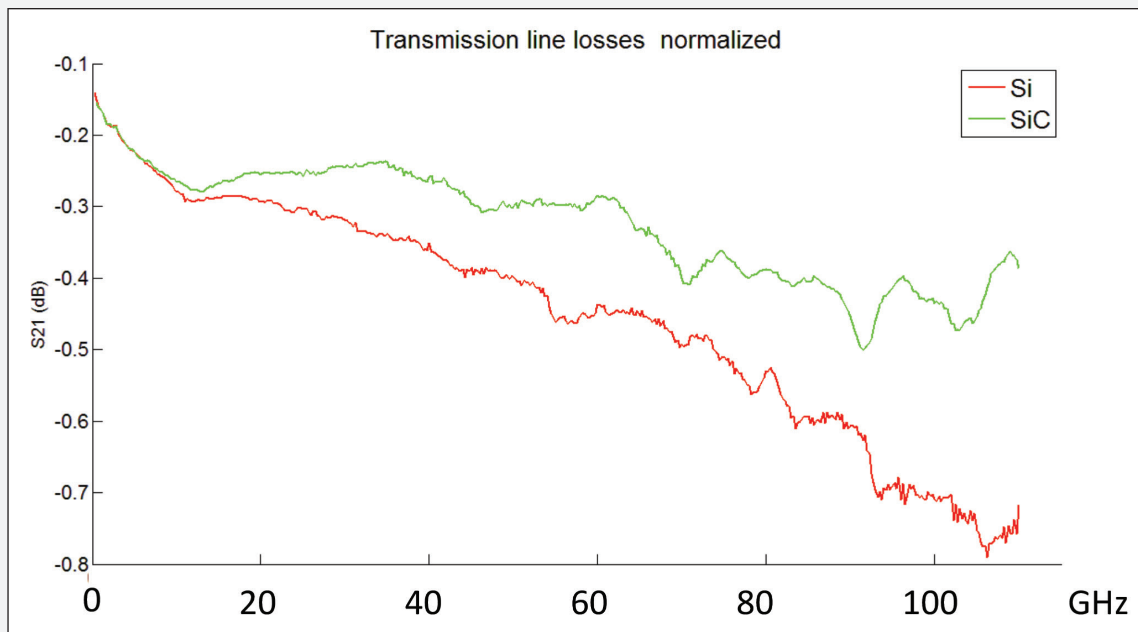


Figure 1. EpiGaN's optimized RF GaN-on-silicon HEMT structure produces very low RF losses, according to measurements on transmission line structures.

The pillars of 5G

To meet stringent user requirements, workgroups defining the 5G roadmap have devised a novel architecture for the 5G network. One of its three key features is the use of many small network cells, known as pico- and femto-cells. They will allow a high user density and low latency. Another key ingredient in 5G systems is the use of transceivers that operate at a higher baseband frequency and have a very large (analogue) bandwidth that can meet digital bandwidth requirements. The third important innovation associated with the introduction of 5G is the move from omni-directional broadcasting to the use of directional beams for each connection. This will enhance energy efficiency, and enable more efficient use of the RF spectrum.

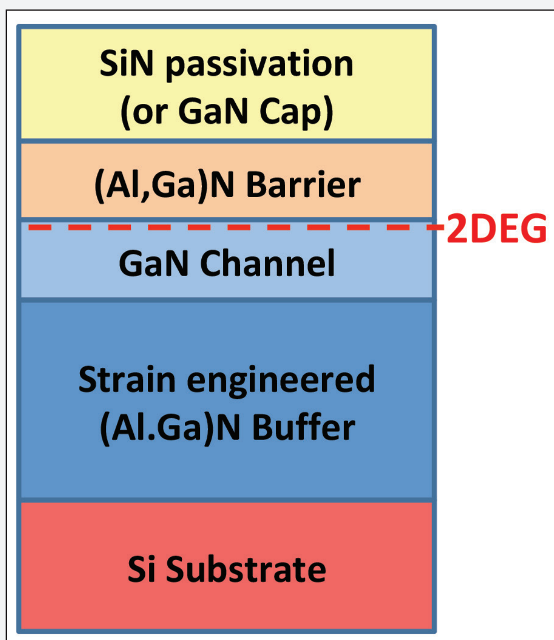


Figure 2. A typical structure for a GaN-on-silicon HEMT includes a GaN channel, a barrier made from AlGaN, and either a GaN cap or a SiN passivation layer.

What are the requirements for the RF technology that can serve 5G architecture? Firstly, it will need to support RF networks operating at much higher frequencies. This domain is less congested than that used today, but spans 6 GHz to as high as 100 GHz. New frequency bands within this domain will have a much higher useable bandwidth, and will ideally be covered with a single amplifier module.

Another major change is the introduction of massive MIMO (multiple-in, multiple-out) beamforming. This technology features multiple transmit and receive chains for each antenna element in the phased-array configuration of the transceiver system. Compared with a single omni-directional antenna, the power per antenna element is reduced, so it is possible to trim the size of the amplifier.

One of the challenges with MIMO is that the antenna elements must all emit signals that have a well-defined phase relationship with one another. Due to this criterion, the technology adopted for the RF amplifier must allow close integration with the driving digital controllers. Note that it is much easier to realise this using silicon substrates than those made from SiC.

The requirements listed above define the mandatory attributes for power amplifier technology for 5G infrastructure and its associated handset architectures. These requirements imply the need for devices that combine compactness with low cost, high power density, linearity at millimetre-wave frequencies and integratability with CMOS technology.

Here GaN-on-silicon technology comes to the fore. It is a fundamentally superior RF semiconductor technology that is ideally placed for fulfilling demanding performance targets. Compared with GaAs, the key, proven attributes of GaN are: a power

density, per millimetre of gate periphery, that is ten times higher; a higher efficiency; operation at a higher voltage, leading to a reduction in impedance transformation challenges; and a superior broadband operation at high frequencies. What's more, GaN can operate at higher device operating temperatures than GaAs. Thanks to this, cooling requirements are easier, maintenance costs lower, and there is an increase in device reliability.

Improving the foundation

Within the technology toolbox, there are at least two variants of GaN to choose from. One is GaN-on-SiC, a pairing of materials that provides the ultimate power levels in the most demanding applications. The common alternative is GaN-on-silicon. This can serve cost-sensitive, high-volume markets that may require large-diameter wafers; and it can deliver an RF performance that is vastly superior to low-frequency silicon LDMOS and expensive, low-power GaAs HEMT technology.

At EpiGaN of Hasselt, Belgium, we are at the forefront of developing GaN-on-silicon epiwafer technologies for RF devices. Since our founding in 2010, we have achieved significant technological milestones that will help to drive the adoption of GaN-on-silicon for the next stage of cellular infrastructure – 5G.

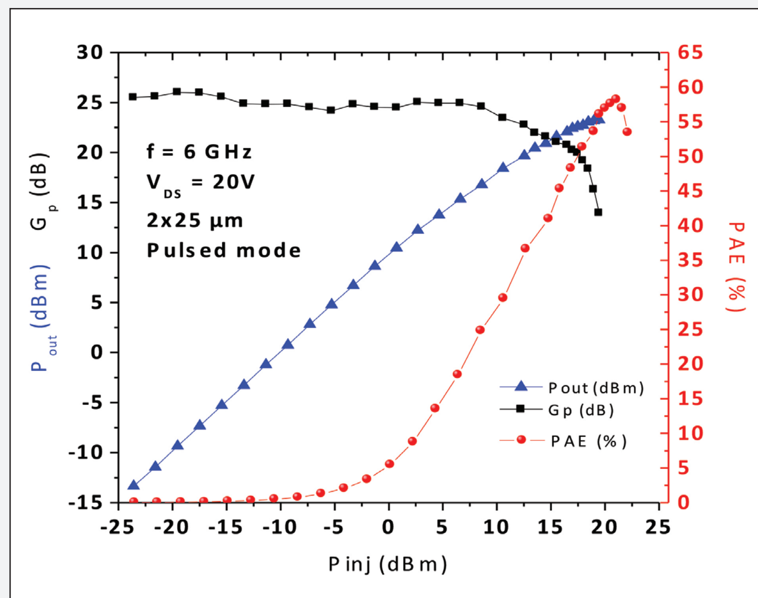


Figure 3. Researchers at IEMN-CNRS have used EpiGaN material to produce 0.15 µm gate length AlN/GaN-on-silicon prototype transistors that deliver encouraging levels of power, gain and power-added efficiency at 6 GHz; courtesy of F. Medjdoub, IEMN, Lille.

Several hurdles must be overcome if GaN-on-silicon is to compete directly with GaN-on-SiC in high-end RF applications. Some are intrinsic, such as the lower thermal conductivity of silicon compared to SiC, which can be countered by slashing the substrate thickness to 50 µm during device processing; and the need to minimize the conductive interface between the silicon substrate and the III-nitride buffer layer by an optimized process during the initial stages of epitaxial growth. A too conductive interface causes a parasitic conduction path for the RF signals, which leads to an undesired dissipation of those signals that is exacerbated at higher frequencies. It is paramount to avoid this, as transistors manufactured on such lossy substrate/buffer combinations will never attain good performance at high efficiencies.

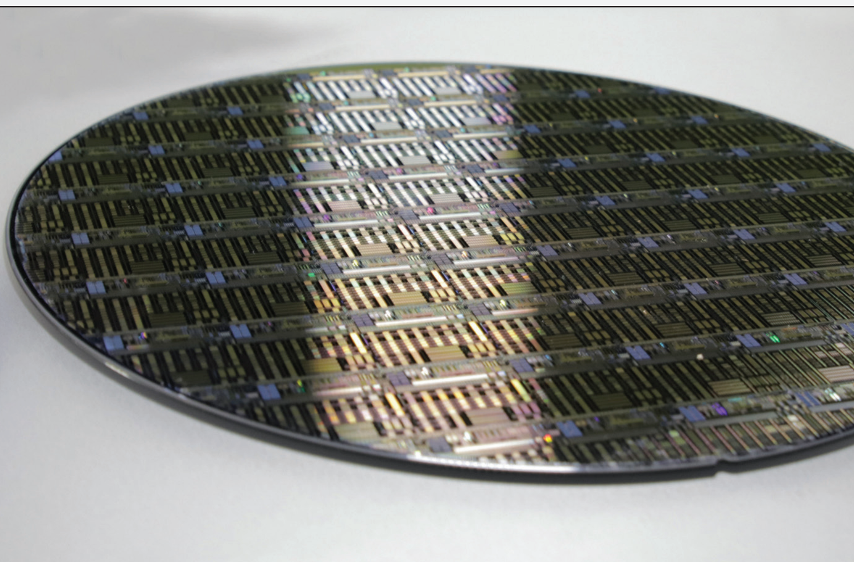
To mitigate this conductive path, we have developed a robust, optimized interface technology. It trims the RF signal loss on GaN-on-silicon material to below 0.2 dB/mm for today's basestation frequencies, which is very close to the value obtained on the much more expensive GaN-on-SiC material. Even in the E-band up to 100 GHz, where future 5G networks may operate, RF signal loss is well below 1 dB/mm (see Figure 1).

Today, the most common platform for manufacturing low-loss RF GaN-on-silicon technology is resistive, float-zone silicon substrates with a diameter of up to 150 mm. We are breaking new ground, having recently released this RF GaN process on high-resistive 200 mm silicon substrates produced by the Czochralski process. Devices formed with these epiwafers deliver comparable performance and showcase the potential for further reductions in the cost of RF power GaN-on-silicon technology. Another asset of these larger epiwafers is that they will ease entry into today's mainstream 200 mm lines at silicon IDMs and foundries.

Beautiful binary barriers

At the heart of the most common structure for an RF GaN HEMT is a ternary AlGaN barrier, typically 20 nm thick and sporting an aluminium content of around 25 percent. This barrier is capped and protected by an ultra-thin GaN layer, having a thickness of between 2 nm and 3 nm (see Figure 2).

> The results obtained by engineers at IEMN-CNRS and Ommic add further weight to the view that RF GaN technology will come to the masses – in fact, there is no doubt about that. Both GaN-on-SiC and GaN-on-silicon are set to enjoy success.



We developed a markedly different structure. To enable the ultimate high-frequency RF performance, we combine pure AlN barrier layers, rather than AlGaN ternaries, with an *in-situ* SiN cap layer. Armed with this pairing, the thickness of the barrier can be slashed from typically 20 nm to just 4 nm to 6 nm, allowing the transistor's gate to be positioned very close to the densely populated channel, and maximising the electrostatic coupling between the two – in other words, improving gate control.

These modifications create superior transistors. Bringing the gate closer to the channel maximises the transistor's transconductance, a key characteristic for RF amplifiers. There is also a dramatic suppression in the so called 'short channel parasitic effects', unwanted effects that include the reduction of the transconductance in transistors with gates that are below 0.15 μm and have a poor aspect ratio for the gate length to gate-to-channel distance – ideally, it should be 15 or more.

Another merit of the switch from an AlGaN barrier to one made of AlN is an increase in the inherent piezoelectric effect to the maximum possible value. Due to this, carrier densities exceed 2 x 10^{13} cm^{-2} in the two-dimensional electron gas in the channel, leading to an increase in power density. If a well-considered thermal chip layout is adopted, significant reductions in chip size can follow.

New device features

We have developed and optimized a process for sealing the top of GaN-on-silicon wafers directly after growth. To do this, we use an *in-situ* grown SiN passivation layer. This approach prevents exposure of (Al,Ga)N layers to the fab environment – that's a major concern for CMOS fabs, which are far more willing to process our epiwafers than standard GaN-on-silicon structures.

That's not the only benefit of our SiN passivation layer, however. It can also serve far broader purposes, including the creation of a unique gate dielectric with a smooth, contamination-free surface. By controlling the filling of surface states during device operation, our SiN layer can provide enough charge to neutralize the surface charge of the AlGaN barrier layer in a GaN-on-silicon device, so that its surface potential no longer contributes to depletion of the two-dimensional electron gas – a phenomenon known as current collapse. Another benefit of the SiN layer is that it improves device stability at elevated temperatures.

Using *in-situ* SiN deposition, the AlGaN barrier may be replaced with pure AlN without any material degradation. For such a SiN/AlN/GaN heterostructure the sheet resistance falls well below 350Ω/sq. Such a low value enables the fabrication of transistors with higher current densities – thus smaller, cheaper devices for the same current rating.

We have collaborated with researchers at IEMN-CNRS, who have produced prototype transistors with our GaN-on-silicon RF wafers. The resultant devices, on un-thinned silicon substrates, have a power-added efficiency approaching 60 percent at 6 GHz (see Figure 3).Great performance continues at higher frequencies.

At 40 GHz, *in-situ* SiN capped AlN/GaN transistors with a 120 nm gate length can deliver a peak output power density of 4.5 W/mm, and an associated power-added efficiency of 46.3 percent (see Figure 4). And that's not the limit: optimising the buffer to refine heat dissipation has enabled the power-added efficiency at 40 GHz to climb to more than 50 percent, with an associated gain exceeding 10 dB.

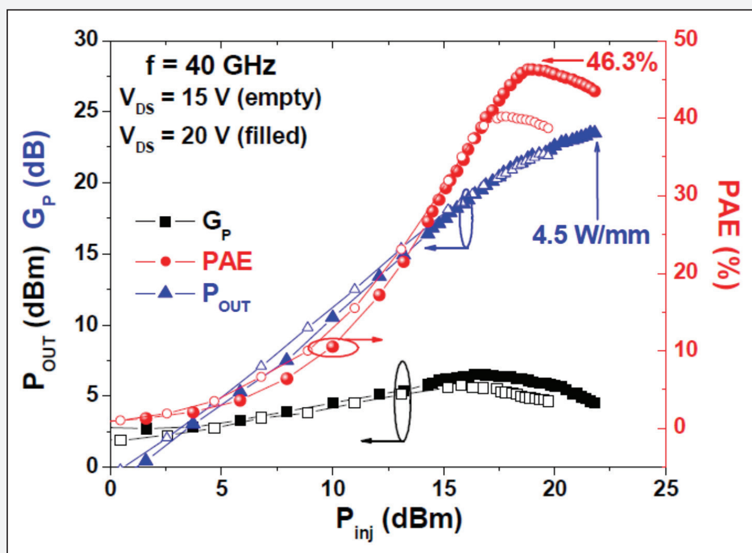


Figure 4. The CW power performance of a 2 × 25 μm AlN/GaN HEMT produced by a team at IEMN-CNRS. The device is operating at a frequency of 40 GHz, and drain-source voltages of 15 V and 20 V. Results are reproduced courtesy of F. Medjdoub, IEMN, Lille.

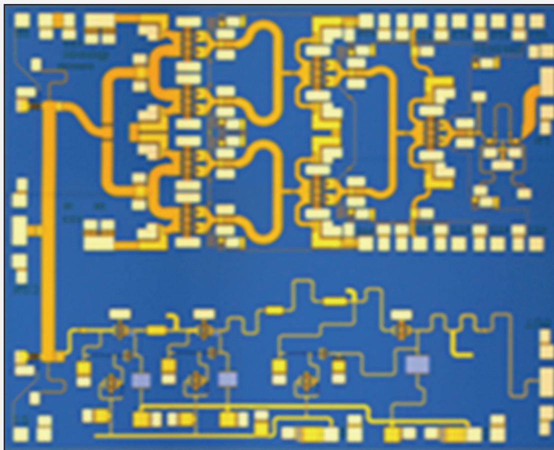


Figure 5. A fully integrated Ka-band transmit/receiver built at Ommic, utilizing EpiGaN's SiN/AlN/GaN-on-silicon RF HEMT epiwafer technology. The PA is located at the top side of the chip, while the LNA is at the bottom side and the switch at the left side (antenna port). Image produced courtesy of Ommic, Limeil Brévannes, France.

We have also partnered with Ommic, a leading European GaN foundry. It has used our unique technology to develop a 100 nm gate-length, open foundry MMIC process with a complete design kit.

Compared to standard GaAs pHEMT processes, the RF GaN-on-silicon devices produced by this process have a far higher breakdown voltage – it is 40 V. Thanks to this, the output power density in the K_a-band is much higher, with a typical value of 3.3 W/mm and a peak of up to 5.7 W/mm. What's more, the device features far greater robustness to input mismatch conditions.

Designers at Ommic have demonstrated the capability of our technology with a fully integrated transceiver operating in the K_a-band. It has a chip size of just 11 mm^2. Operating at 30 GHz, the output power of the power-amplifier-and-switch transceiver is above 35.5 dBm, while the power amplifier alone offers 37 dBm. Meanwhile, gain of the low-noise-amplifier-and-switch transceiver part, evaluated in receive mode, exceeds 18 dB (see Figure 6).

The results obtained by engineers at IEMN-CNRS and Ommic add further weight to the view that RF GaN technology will come to the masses – in fact, there is no doubt about that. Both GaN-on-SiC and GaN-on-silicon are set to enjoy success, with levels of sales of the two formats depending on the cost-to-performance trade-off for the specific RF application.

Today, we are already seeing GaN-on-SiC HEMTs displacing incumbent GaAs pHEMT and silicon LDMOS technology in 4G-LTE infrastructure systems, while GaN-on-silicon is rapidly closing the performance gap and offering an increasingly tempting bang-per-puck. The benefits that RF GaN technology brings to the table are simply too attractive to ignore, and they are already spurring innovations in many existing applications.

To reach true mass-market adoption of RF GaN technology for 5G, there will need to be a mature supply chain and ecosystem. While this not in place today, big industry players – that is, IDMs and pure-play foundries – are positioning themselves to build up a strong supply chain for RF GaN device manufacturing. It is becoming ever more evident with GaN that the dawn of a new RF technology has begun, and that the incumbent silicon and GaAs devices will lose considerable market share in next-generation cellular RF infrastructure applications.

Last but not least: will RF GaN-on-silicon technology win deployment in future smartphones? It works with relatively high voltages of 10 V or more today, so it is not the most suitable technology for handsets, which currently use between 3 V and 5 V. But it could quickly become a viable candidate, as standards evolve, carrier aggregation is introduced to increase bandwidths, and there are ever increasing performance requirements for multi-mode, multi-band PAs.

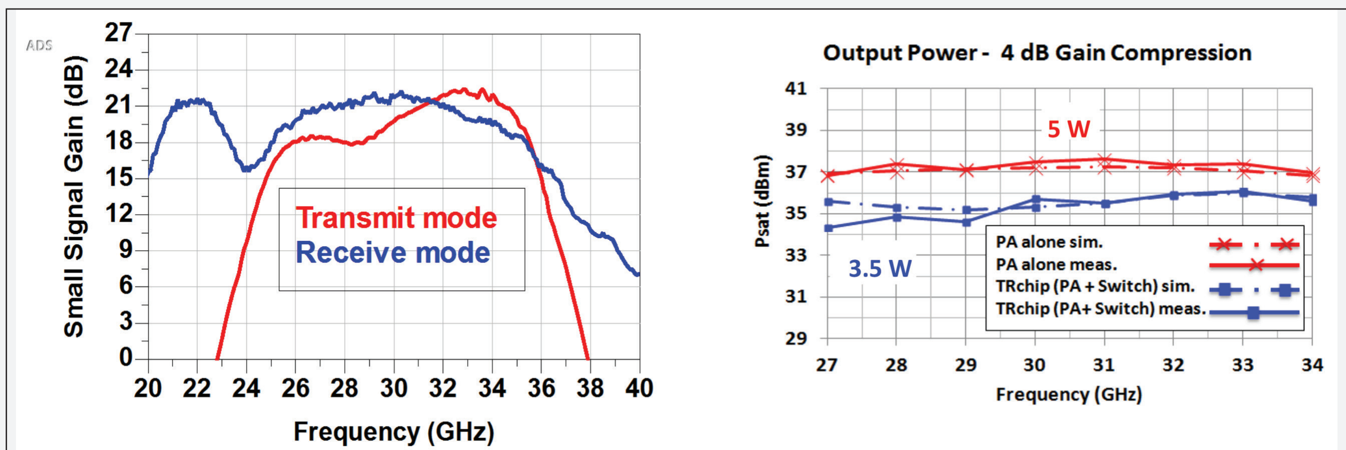


Figure 6: Transmit and receive small-signal gain (left) and transmit PA output power (right) of a K_a-band transceiver MMIC (with and without switch), for the chip in Figure 5; courtesy of Ommic, Limeil Brévannes, France.

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Speakers announced to date

Wrestling Market Share from Silicon Power Devices

What are the next opportunities for SiC? And how can GaN gain significant traction in the market place?

ANALYST

- **Richard Eden: IHS Markit**
  The SiC & GaN power semiconductor market: Forecasts and drivers

SPEAKERS

- **Felix Grawert: AIXTRON**
  Accelerated adoption of wide bandgap devices in automotive applications
- **Philip Zuk: Transphorm**
  Shifting gears: The “GaN-ification” of automobiles
- **Peter Friedrichs: Infineon**
  Exploiting the merits of GaN and SiC
- **Hiroyuki Handa: Panasonic**
  Trimming the losses in GaN GITs
- **Tamara Baksht: VisIC Technologies**
  High efficiency at high power density: realisation of GaN’s promise for power electronics
- **Andy Sellars: Catapult**
  Accelerating the commercial application of compound semiconductors
- **Mohamed Alomari: IMS Chips**
  Fast-loop assessment of GaN/AlGaN epitaxial layers for power applications
- **Cem Basceri: Qromis**
  ‘Status updates: Volume manufacturing of high performance & scalable GaN power devices on 8-inch diameter QST platform’
- **Samantha Reese: National Renewable Energy Laboratory, USA**
  A techno-economics look at SiC WBG from wafer to motor drive
- **Phil Greene: Ferrotec**
  Efficient metal deposition with the Ferrotec UF6100 200mm lift-off evaporator
- **Sarah Okada: Revasum**
  Simplified SiC backside thinning
- **Mikko Soderlund: Beneq**
  High-capacity wafer-scale solutions for More than Moore Applications

5G: Where are we and What’s Next?

What form will 5G take? And how good will 5G be for GaAs and GaN?

ANALYST

- **Eric Higham: Strategy Analytics**
  Is 5G roll-out a certainty? And will it be good for GaAs and GaN?

SPEAKERS

- **Roger Hall: Qorvo**
  Building the industry’s first 5G front-end
- **Liam Devlin: Plextek RFI**
  MMICs - what is needed to get mmWave 5G to work?

Ramping Revenues from RF Devices

What are the opportunities for III-Vs in defense and civilian markets? Will higher frequencies open up new sales?

ANALYST

- **Asif Anwar: Strategy Analytics**
  Defense sector trends and the associated market outlook for compound semiconductors

SPEAKER

- **Nick Cataldo: Efficient Power Conversion**
  Wireless charging with GaN devices
- **Timothy Boles: MACOM**
  Industrializing RF GaN/S

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Finding Solutions with Heterogenous Integration

Where will the growth of compound semiconductors on silicon deliver a fundamental change? And what are the tricks to ensure success?

ANALYST

- **Zhen Zong: Yole Développement**
  Presentation TBC

SPEAKERS

- **Thomas Uhrmann: EV Group**
  Wafer bonding of compound semiconductors: Achieving desired interface properties
- **Jean-Pierre Locquet: GaNonCMOS EU Project**
  Dense integrating GaN power switches with CMOS drivers
- **Wolfgang Stolz: NAsP III-V**
  Building III/V-devices on CMOS-compatible Si (001)
- **Lars-Erik Wernersson: Lund University**
  Integrating III-V nanowires to advance CMOS system-on-a-chip technologies
- **Speaker TBC: Nanotronics**
  Topic TBC
- **David Lishan: Plasma-Therm**
  Plasma dicing: Value added to the advanced packaging supply chain

LEDs: Magnifying Margins

Which sectors offer the best returns? Does the bottom line get the biggest benefit from streamlining manufacturing, or from optimising the chip?

ANALYST

- **Pars Mukish: Yole Développement**
  Revolutionising displays with MicroLEDs

SPEAKERS

- **Samuel Sonderegger: Attolight**
  Improving LED manufacturing by full wafer cathodoluminescence
- **Andreas Weisl: Seoul Semiconductor**
  Improving LEDs with a Wafer Level Integrated Chip on PCB (WICOP) architecture
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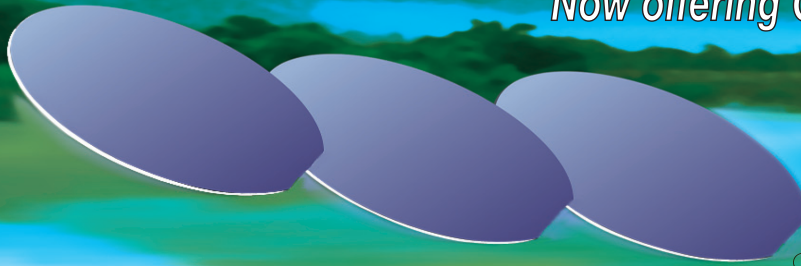

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Newport Wafer Fab is tailored toward power technologies, produced with 0.18 μm processes.

Branching out from silicon

Will Newport Wafer Fab become the world's first silicon and compound semiconductor foundry?

RICHARD STEVENSON REPORTS

IT'S UPLIFTING to take control of your own destiny. Just ask the leaders of Newport Wafer Fab. They have worked at this site for many years, including those when it was owned by Infineon Technologies for processing silicon and GaN-on-silicon wafers. And now, following the purchase of the facility from the German electronics powerhouse in September 2017, they are delighting in taking the helm.

"It's a very exciting time for everybody," remarks General Manager Paul James, who started work at the facility as a consultant just over five years ago, took a permanent position in November 2013 to lead the engineering teams, and has been subsequently promoted to run the site.

Part of this excitement is that the acquisition – supported by financing from HSBC, the Welsh government and a private investors – has led to the securing of around five hundred jobs. But that's by no means the only reason that James is upbeat.

"We've also got a clear roadmap to move within the [compound semiconductor] cluster environment in South Wales to new and novel technologies. They typically command a higher margin, and from an

engineering perspective, are more interesting."

Today, efforts at Newport Wafer Fab are focused on fulfilling orders from Infineon's two-year supply deal, which could be extended if it is mutually convenient for both parties. The work involves producing thinned, back-metalised tested wafers in which the die have been singulated.

As Infineon has shifted its GaN-on-silicon production to another foundry, only silicon wafers are now being processed at Newport Wafer Fab. However, James and his colleagues are planning to soon branch out into the processing of wafers that feature compound semiconductor heterostructures on silicon.

"What excites us is that is we are in the right space at the right time in the cluster," enthuses Sam Evans, Director of QM and External Affairs.

For the team at Newport Wafer Fab, given their experience, the obvious starting point for this endeavour is the processing of GaN-on-silicon wafers.

There is much to be said for this move, given the great market potential for GaN-on-silicon. And although many firms are claiming to own key intellectual property and patent disputes could follow, this should not be detrimental to Newport Wafer Fab.

"In our case, we're a foundry," argues James. "We expect our customers to indemnify us against any IP claims arising from processing wafers on their behalf. Typically, the patents around the GaN are more in the epi itself, and particularly the lattice-matching layers. We don't have epi, and we rely on other sub-contractors to provide that."

While efforts may begin with GaN-on-silicon, the aim is to expand to cover other compound semiconductor technologies. "We are in the process of assessing a number of opportunities, to see where they coalesce around particular compound semiconductor solutions and particular wafer sizes," argues James.

As the more complicated technologies will require capital investment and some niche pieces of equipment, he says that it will take some time before these services can be offered.

The good news, however, is that the cost of introducing this may not be that high. "It could be relatively modest," claims James," depending on which flavour of technology we choose to invest in."

Graham Neil, Director of Sales and Marketing, adds: "One of the key things there is that we have got some procedures in place when introducing compound semiconductor materials into an existing fab." Fail do this, and there is the risk that contamination can take place, leading to degraded device performance.

Experienced employees

Customers that chose to work with Newport Wafer fab will benefit from the tremendous level of experience of many of the engineers.

"The average experience in semiconductors is fifteen years, so that's a huge benefit," argues Neil. "A lot of those were engineers when Newport was operating as a foundry many years ago, and it's bringing back all those skills to develop new technologies."

Many of these employees will have seen a great deal of change while they have worked at the 28 acre campus. While most would not have been there in 1982, when Inmos opened the site, a good number would have been there in the 1990s when it operated as a silicon foundry, prior to being bought by International Rectifier for developing GaN products in 2005 (see "A brief history of Newport Wafer Fab" for more details).

The workforce has showed considerable loyalty during the last few years. Uncertainty over their future would have surfaced in early 2015, when Infineon decided that the fab did not fit in to its long-term plans: it would use it for production for two years, and then try to find a buyer.

"We lost a handful of employees during the Infineon phase, once the scheduled closure and sale was announced," says James. "There was a retention program in place from Infineon, which retained the majority of the staff."

In the last few months some staff have left, and Newport Wafer Fab is now actively recruiting equipment, process and device engineers. "We need them for not only supporting the existing technologies under the supply agreement, but also transferring in and developing new ones," explains James.

There is a campus-feel to the Newport facility, which will support the development of the compound semiconductor cluster in South Wales.

As the compound semiconductor cluster takes off, it is possible that some of the engineers from Newport Wafer Fab will be tempted to take up exciting new opportunities at other firms just a few miles down the road.

James accepts that although this might happen, a successful compound semiconductor cluster in South Wales will actually help to improve the quality of the workforce in all the local firms.

"The key thing is having a critical mass that attracts people to South Wales," argues James. "Getting people to up sticks and move to a region, if you're a one-trick pony, is actually quite difficult." However, when a highly specialised skill is valued by several companies in a region, relocating offers less risk and greater reward.

Looking ahead

James has identified two primary goals for the fab for 2018: successfully transferring in new silicon technologies from other customers, and finalising which compound semiconductor opportunities will be pursued.

The silicon customers that Newport Wafer Fab will target are those that benefit from partnering with a foundry that is tailored toward power technologies, produced with 0.18 μm processes. "[The fab is] running trench FET technologies, IGBTs, and IC products that are used for the control circuitry, which is based effectively on a 0.35 micron technology," says James. Production capacity is currently 8,000 per week. "It could be relatively easily expanded to 11,000 wafer within the existing cleanroom space, and indeed we have a number of tools left over from the 6-inch line that are 8-inch compatible, that could be utilised to do exactly that," says James. And the current cleanroom, which has a 3650 m^2 footprint, could be extended by 480 m^2, to propel capacity to 14,000 wafers per week.

Note, however, that regardless of the number of tools in place, capacity should not be thought of as fixed. Instead, it varies with the mix of products. "So, if there is a different mix of products, that number could go up," adds Neil.

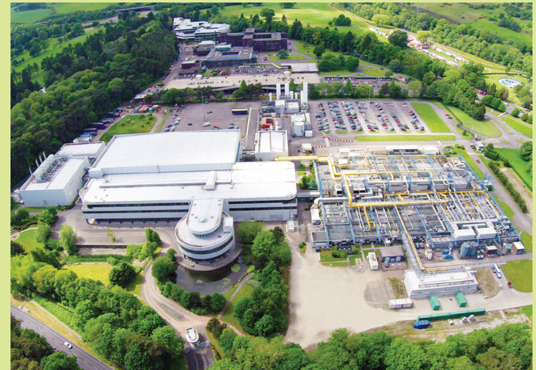
Hopefully, within a year or so that product mix will not be limited to silicon. "By 2020, I would expect that those compound semiconductor opportunities have come to fruition, and are running in volume in the facility," says James.

Success on that front will be welcomed by many. It will not only have enabled Newport Wafer Fab to have become the first silicon and compound semiconductor foundry – it will also have provided a key ingredient in the creation of the compound semiconductor cluster in South Wales.

A brief history of Newport Wafer Fab

CONSTRUCTION of the 8,900 m^2 single-story building, originally a microprocessor facility for Inmos, began in 1980 and was completed in 1982. The striking design comes from Sir Richard Rogers, an award-winning architect with an illustrious career that included work on the Pompidou Centre in Paris.

Inmos did not hold on to the building for long, selling it to Thorn EMI in 1984. In 1989 the site was bought by SGS-Thomson Microelectronics, a company now known as STMicroelectronics. It used the facility to produce fast SRAM and microprocessors products.



Built in 1982 for Inmos, the facility now owned by Newport Wafer Fab sits in 28 acres of land on the outskirts of Newport, South Wales.

In 1992, QPL International Holdings in Hong Kong bought the site, financing the launch of Newport Wafer Fab. This operated as a foundry for ten years, serving customers that included International Rectifier, Motorola, Samsung and STMicroelectronics.

The next owner was International Rectifier, which acquired the site in 2005, using it as its principle R&D and manufacturing centre for launching the majority of its silicon and GaN technologies. In January 2015 Infineon bought International Rectifier, and after reassessing its global operations, decided that it would use the Newport facility for two years, before putting it up for sale.

The subsequent purchase in September 2017 led to the re-birth of Newport Wafer Fab. This incarnation, however, has plans to not just be a foundry for silicon, but also for compound semiconductors.

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Improving the performance of **power transistors**

Researchers at IEDM offers insights into how to make GaN transistors switch faster, produce higher blocking voltages, exhibit a very low on-resistance and completely supress dynamic on-resistance

BY RICHARD STEVENSON

THERE is still much work to do to improve the performance of the GaN power transistor. While its commercialisation is netting sales, far greater revenues could follow if this device switches more efficiently, handles higher voltages and currents, and offers greater stability.

Options for succeeding on all these fronts were outlined at the recent International Electron Devices Meeting (IEDM), held in San Francisco from 2-6 December 2017. At that gathering researchers detailed: improvements in the switching performance of transistors that feature a gate insulator over the junction; the tremendous capability of vertical power transistors with fins and trenches; and the elimination of dynamic on-resistance through proton irradiation.

Speedier switching

A device architecture for providing superior switching was presented by Satoshi Nakazawa from Panasonic Corporation. Working with colleagues from Osaka University and Hokkaido University, he and his co-workers developed a GaN transistor with an AlON gate insulator that combines fast switching with a low leakage current.

"The proposed device exhibits a two-to-four times faster switching speed compared to a typical silicon super-junction-MOS with the same drain current rating," says Nakazawa. "This suggests a reduction in switching loss to half or less in high-frequency switching operations."

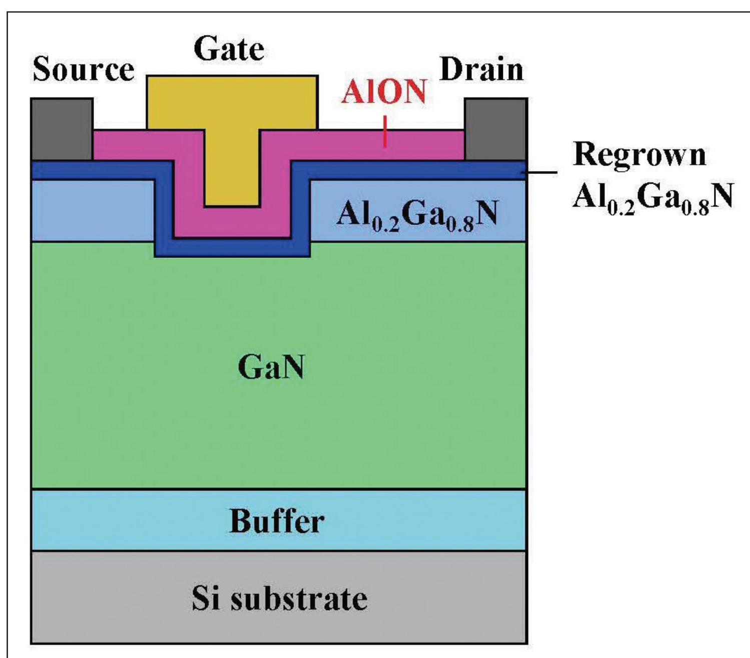

Figure 1. A team from Panasonic, Osaka University and Hokkaido University have developed a GaN transistor with an AlON gate insulator. This device combines fast switching with low leakage.

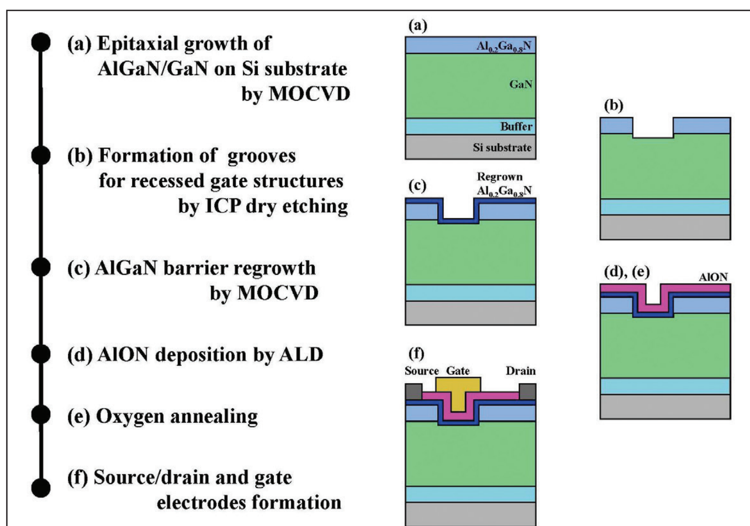

Figure 2. The fabrication steps employed for the fabrication of a GaN transistor with an AlON gate insulator. This transistor is being pioneered by a team from Panasonic, Osaka University and Hokkaido University.

What's more, improvements wrought by the addition of the AlON gate should be applicable to all forms of GaN transistor, argues Nakazawa. "Those with a vertical architecture should expect similar results – such as stable gate characteristics with low gate leakages and a large gate voltage swing – ensuring gate-driving compatibility with conventional silicon power devices."

The team from Japan had to modify the standard HFET design to realise high-current, high-voltage switching. Their approach, introducing an insulator over the gate, has often been discussed as a way to to reduce leakage current and enable normally-off operation. However, success with this approach has not been reported prior to the work of Nakazawa and co-workers – instability of gate characteristics has probably hampered previous efforts.

Fabrication of the team's device (see Figure 1) began with growth, by MOCVD, of GaN and AlGaN layers on a silicon substrate (see Figure 2 for an overview of the fabrication process). Subsequent etching created a recessed gate structure, introduced to trim series resistance. After this, a thin AlGaN layer was added by MOCVD – this is highly beneficial, removing damage on the grooved structure caused by dry etching.

The next step involved adding AlON by atomic layer deposition, a growth process that combines great uniformity with an absence of processing damage. Annealing followed, to remove dangling bonds of gallium and/or aluminium at the AlGaN surface and ultimately ensure a positive shift of the threshold voltage. To realise a breakdown voltage in excess of 600 V, transistors were formed with a 2 μm gate length and a 10 μm gate-to-drain spacing.

Measurements of transfer characteristics reveal that the hysteresis of the team's annealed device is far less than that for a transistor with a gate made from Al_2O_3, a more conventional gate dielectric. The curves for transfer characteristics for the device with an AlON insulator do not change for gate voltages up to 10 V, leading Nakazawa and co-workers to claim that a high gate voltage can be applied to realise high-speed, on-state switching.

Further evidence for the benefits of AlON over Al_2O_3 come from capacitance-voltage measurements. They show that dispersion is smaller for the novel oxide, and thus suggest a superior interface. Further encouraging signs come from values for interface trap densities, extracted from the capacitance-voltage measurements, that show that imperfections are lower for AlON, especially in the mid-gap.

Devices with a chip size of 2.3 mm by 2.3 mm are capable of a maximum drain current of 20 A, a breakdown of 730 V, and turn-on and turn-off transitions at 78 V/ns and 169 V/ns, respectively. "We are planning to demonstrate some practical

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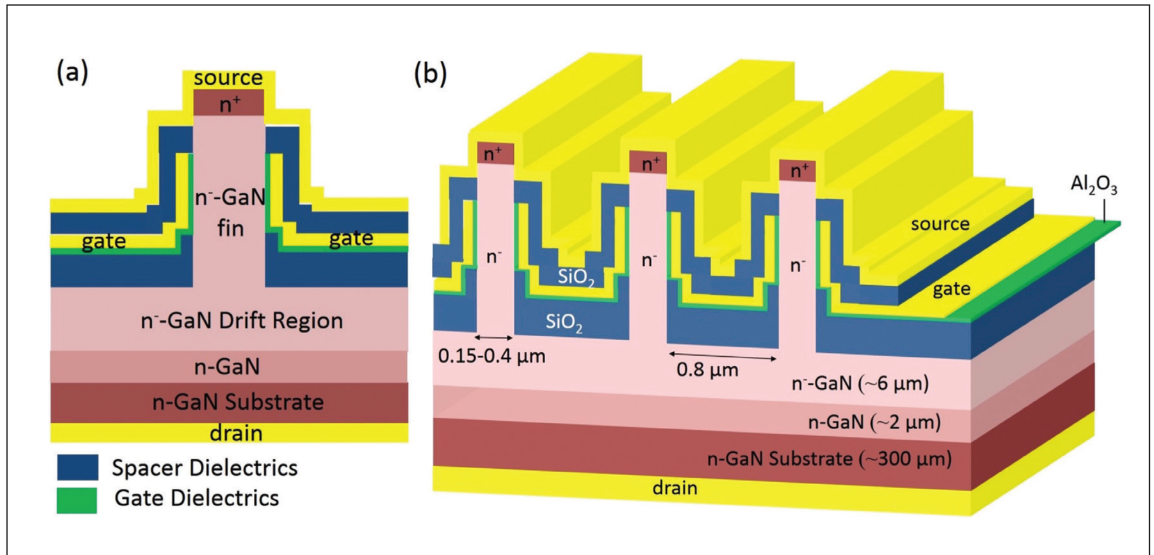

Figure 3. Vertical fin power FETs are being developed by a partnership between researchers at MIT, the Singapore- MIT Alliance for Research and Technology, IQE RF and Colombia University. A key feature of these devices is that they don't require *p*-type material.

applications," says Nakazawa. This will include converters formed with the team's devices.

Fantastic fins

Supporting some US-based efforts at developing vertical GaN transistors with high-current, high-voltage capability is the ARPA-E SWITCHES programme. Working within this is a team involving researchers from MIT, the Singapore-MIT Alliance for Research and Technology, IQE RF and Colombia University.

Together, they have produced vertical fin power FETs that combine an on-current in excess of 25 kA cm^{-2} with an off-current of less than 10^{-4} A at 1200 V.

In the paper given at the conference by Yuhao Zhang from MIT, it is stated that vertical devices have three key advantages over their lateral cousins: for a given chip area, a higher breakdown voltage and current; a superior reliability; and simplified thermal management.

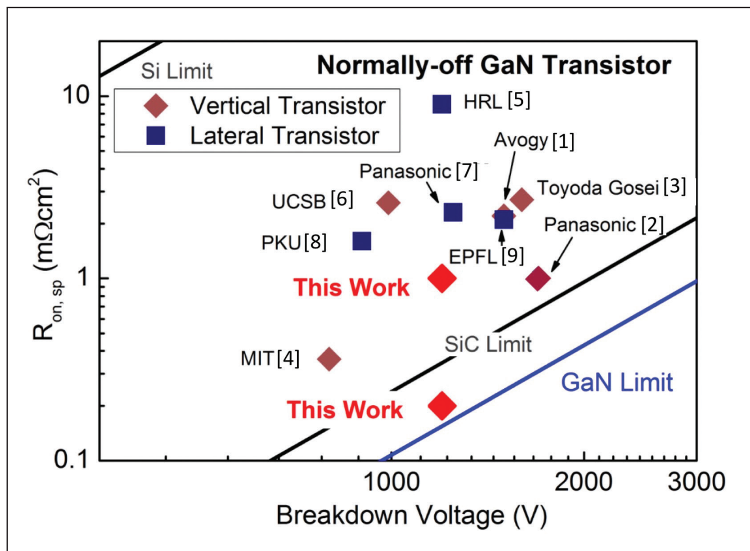

Figure 4. Vertical fin power FETs produced by the team from MIT, the Singapore-MIT Alliance for Research and Technology, IQE RF and Colombia University produce a very competitive performance when compared to other vertical GaN transistors. The numbers in brackets refer to: [1] H. Nie *et al*. IEEE Electron Dev. Lett. **35** 939 (2014) [2] D. Shibata *et al*. IEEE IEDM 10.1 (2016) [3] T. Oka *et al*. ISPSD 459 (2016) [4] M.Sun *et al.* IEEE Electron Dev. Lett. **38** 509 (2017) [5] R. Chu *et al*. IEEE Electron Dev. Lett. **32** 632 (2011) [6] C. Gupta *et al*. IEEE Electron Dev. Lett. **38** 353 (2017) [7] M. Ishida *et al.* IEEE Trans. Electron Dev. **60** 3053 (2013) [8] M. Wang *et al*. IEEE Trans. Electron Dev. **61** 2035 (2013) [9] J. Ma *et al*. IEEE Electron Dev. Lett. **38** 367 (2017)

However, according to the team, the majority of vertical architectures are held back by either the need to undertake an epitaxial re-growth step, or to have to grow *p*-type GaN. For devices such as current-aperture vertical electron transistors, epitaxial re-growth is essential, and it greatly increases the cost and complexity of device fabrication.

Meanwhile, *p*-type material is plagued by poor activation and a low carrier mobility. These impediments make it extremely difficult to produce a high-mobility intrinsic carrier channel, and they manifest themselves in a substantial increase in device on-resistance.

"Also, the need for *p*-GaN activation after MOCVD growth makes the overall wafer epitaxial growth complicated: on one hand, the thickness of *p*-GaN and the top layer is typically limited; on the other hand, the following growth of the top layer in MOCVD could easily passivate the *p*-GaN layer and make it *n*-type" argues Zhang.

With the approach he and his co-workers adopt, the need for *p*-type material is eliminated. "[Our devices] can achieve a normally-off operation without *p*-GaN, which is needed in many normally-off lateral HEMTs and vertical trench MOSFETs," says Zhang. "In addition, this threshold voltage can be well tuned by fin width, doping concentration and gate metal."

In the team's device, the current is controlled by fin-shaped, *n*-type GaN channels, which are surrounded by gate dielectrics and metal electrodes (see Figure 3). Due to the difference in the values of the work function for the gate metal and GaN, the electrons in the fin channels are depleted at zero gate bias. Once the fin width is reduced below 500 nm, the depletion regions induced by the two free surfaces of the fin merge to form a fully depleted fin channel that enables normally-off operation.

Back in April 2017, the team reported an early form of their device, which combined a blocking voltage of 800 V with an on-resistance of 0.36 mΩ cm^2. Since then they have improved the device, with the latest results reported at IEDM.

Zhang says that the recent device benefits from refinements to the wafer structure, especially engineering the doping level and thickness of the drift region – this can lead to a better trade-off between on-state conductivity and off-state breakdown capability. The process for making ohmic contacts has also moved on, allowing "excellent" ohmic contacts to be formed on top of the narrow fins, even without the need for post-annealing. What's more, the team has refined the design so that the peak electric field has shifted from the fin to the device periphery. "This makes electric field management much easier," says Zhang.

Fabrication of the transistors began by taking free-standing GaN substrates and growing, by MOCVD, a 2 μm-thick *n*-type layer, followed by a 7 μm-thick *n*-type GaN drift layer that is doped with carbon to compensate the non-intentional doping in GaN, and finally a 300 nm-thick *n*-type GaN cap.

Fins were formed by dry-etching, before additional structures were formed between and on top of the fins, using plamsa-enhanced CVD of SiO_2 spacer layers, atomic layer deposition of an Al_2O_3 gate dielectric, and sputtering of a molybdenum gate layer.

Measurements on a device with 60 fins, each with a width of 200 nm and a length of 100 μm, revealed a threshold voltage of about 1 V, an on-off ratio for current of 10^{10}, and an on-resistance of 0.2 mΩ cm^2. Breakdown voltage exceeded 1200 V, and drain and gate currents were below 1 nA at high drain bias.

Zhang and co-workers also produced a larger device with a 10 A current rating. Featuring 600 fins with widths of 250 nm, this chip required a gate drive of 5-6 V to produce 10 A, and had a breakdown voltage of 800 V. The team claims that this chip, which is 0.8 mm by 0.55 mm in size, is significantly smaller than other 10 A-class GaN vertical and lateral transistors.

Benchmarking of the team's devices against those of

Vertical fin power FETs on a 2-inch GaN-on-GaN wafer.

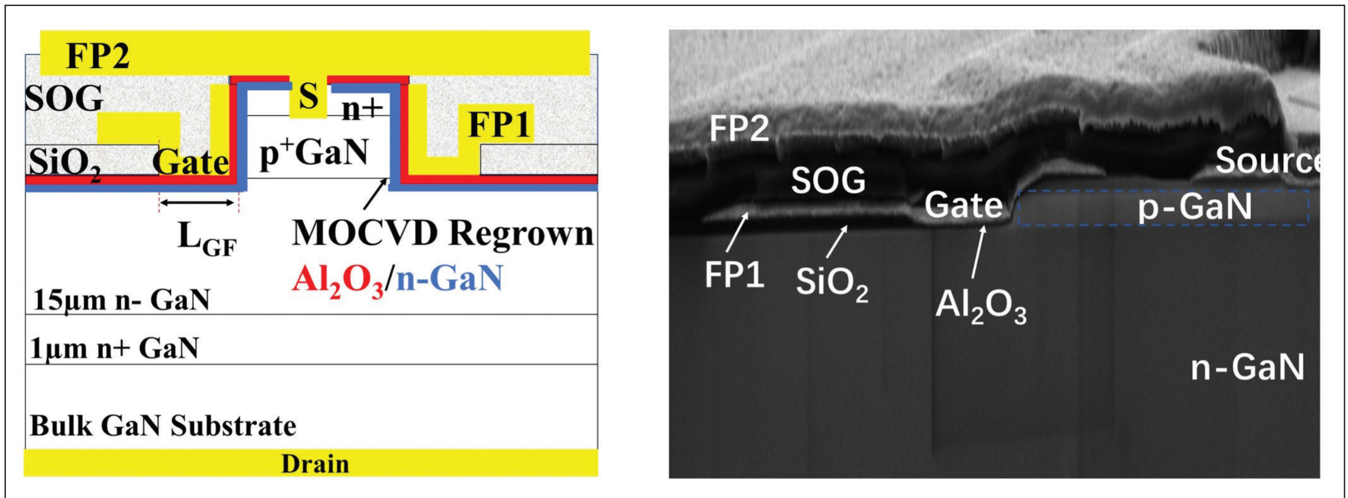

Figure 5. A team from the University of California, Davis, and the University of California, Santa Barbara, is developing oxide-GaN interlayer FETs under support from the ARPA-SWITCHES programme. These FETs, which can deliver blocking voltages in excess of 1.4 kV, feature trenches and double field plates.

other groups underlines the impressive performance of the vertical fin power FET (see Figure 4). And even better results are sure to follow.

"We have already made devices capable of sustaining 2000 V reverse bias," says Zhang. "We are now incorporating additional edge termination structures to achieve even higher breakdown voltage uniformly on a wafer-level."

The researchers from MIT are also collaborating with IBM and Columbia University, with the aims of accomplishing wafer-level device transfer and providing circuit demonstration. "The goal is to recycle the expensive GaN substrate, to greatly reduce the cost of the power modules built from our novel vertical GaN transistors," explains Zhang.

Vertical trenches

THE ARPA-SWITCHES programme is also supporting a team from the University of California, Davis, and the University of California, Santa Barbara. This partnership is pioneering the development of oxide-GaN interlayer FETs. Unit devices are capable of blocking voltages of more than 1.4 kV, while the figure for large-area devices is 900 V.

Spokesperson at IEDM meeting, Dong Ji from the University of California, Davis, says that they are pursuing this device architecture, rather than the current aperture vertical electron transistor, because although the latter is capable of a high current density, it is a normally-off device. Another alternative, the trench MOSFET, has a good normally-off behaviour, but it has been shunned, due to its a low current density that stems from the low channel electron mobility.

"The novelty in an oxide-GaN interlayer FET lies in using a ten-nanometre, MOCVD-regrown unintentional doped GaN interlayer as the channel region, which improves the channel electron mobility without hurting the normally off behaviour," says Ji.

According to him, the team's device, which has a channel mobility of 185 $cm^2 V^{-1} s^{-1}$, has the highest mobility of any reported oxide-based GaN or SiC power transistor.

"For the conventional GaN trench MOSFET and SiC trench MOSFET, the channel electron mobility is limited to 50 $cm^2 V^{-1} s^{-1}$, which is limited by the high doping density in the *p*-base region," says Ji. "However, because the oxide-GaN interlayer FET

Dynamic on-resistance is strongly dependent on the leakage through the unintentionally doped layer. However, eliminating leakage by improving the growth of this layer is very challenging, making proton bombardment a more practical approach.

uses unintentionally doped GaN as the channel, the channel mobility is improved."

Devices were formed by taking epiwafers, grown by IQE, and etching 550 nm deep trenches. Following a clean with HF acid, MOCVD added a 10 nm-thick, unintentional grown GaN layer, followed by a 50 nm-thick layer of Al_2O_3. These two layers serve as the channel and gate insulator, respectively. The addition of source, gate and drain electrodes and field plates completed FET fabrication.

"We used a double field plate structure," says Ji, who explains that one of the field plates is connected to the gate contact, and the other to the source contact. "Compared to the single field-plate structure, which protects the source-to-drain *p-n* junction, the double-field-plate structure can protect the gate insulator to improve the breakdown voltage, and improve the gate insulator reliability."

Measurements on single unit cell devices, which have a circle layout with a 22 μm diameter, reveal a saturated current density of 850 A cm^{-2}, an on-resistance of 2.2 mΩ cm^2, a breakdown voltage of 1435 V and a threshold voltage of 4.7 V.

"4.7 V is an excellent value for power devices," says Ji, who attributes this success to the doping density in the GaN interlayer.

The team also produced larger transistors, with an area of 400 μm by 500 μm. These devices produce a breakdown voltage of 900 V and a saturation current of 0.185 A under a 12 V gate bias.

Ji says that the next steps will be to demonstrate a single device with a current of more than 10 A, and to study its switching characteristics. "Commercialization of the device is our goal." All the fabrication steps are commercially viable, argues Ji, pointing out that all growth steps can be undertaken with MOCVD, which is preferred for mass production.

Proton perfection

One of the weaknesses of the GaN transistor is its dynamic on-resistance. This downside can result in an increase in total on-resistance of up to 30 percent, following exposure to a high drain bias.

At IEDM, Matteo Meneghini from the University of Padova, Italy, outlined an approach for completely eliminating dynamic on-resistance: proton irradiation. Working with departmental colleagues, as well as researchers from ON Semiconductor, he has shown that GaN HEMTs can undergo complete suppression of the dynamic on-resistance over the voltage range of 0 V to 600 V when given an optimal dose of protons.

Meneghini says that dynamic on-resistance is strongly dependent on the leakage through the unintentionally doped layer. However, eliminating leakage by improving the growth of this layer is very challenging, making proton bombardment a more practical approach.

The time taken to carry out the irradiation of protons is "short", say Meneghini, and depends on the fluence.

Experiments by the team, using conventional devices, show that there is no change in the dynamical behaviour for fluences of 10^{12} cm^{-2} and below. Increase the fluence to 10^{13} cm^{-2} and there is a slight reduction in dynamic on-resistance; and this reduction is substantial for a fluence of 5 x 10^{13} cm^{-2} and completely suppressed when the fluence is 1.5 x 10^{14} cm^{-2} (see Figure 6).

Meneghini believes that proton irradiation could be used during the manufacture of GaN transistors. He points out that irradiation/implantation is used in the optoelectronics industry to create highly resistive regions in laser diodes.

Work on this topic will continue, with Meneghini and co-workers aiming to study and optimise treatment conditions, investigate the impact of different epitaxial processes, and study the trade-off between leakage and dynamic on-resistance.

These efforts, along with further progress from the teams working in the ARPA SWITCHES program and for Panasonic, will help to improve the performance and capability of GaN transistors. Reports of more breakthroughs in this field can be expected at this year's IEDM, which will be held in San Francisco from 3-5 December.

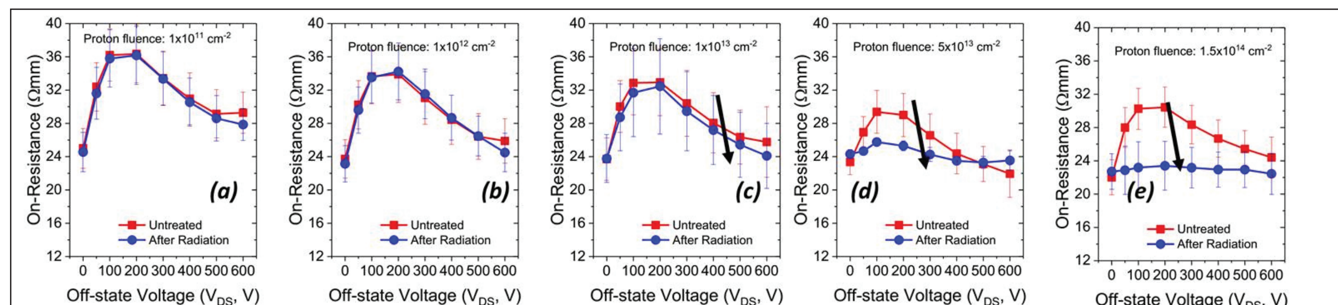

Figure 6. Researchers at University of Padova, Italy, and ON Semiconductor have shown that increasing the fluence of proton irradiation can completely eliminate dynamic on-resistance.

Superluminescent

LEDs target displays

Superluminescent LEDs with record-breaking output powers and efficiencies underscore the promise of these devices for head-up displays and pico-projectors

BY MARCO MALINVERNI FROM EXALOS

One of the hottest research topics right now is the development of energy-efficient display technologies for augmented-reality head-up displays and pico-projectors.

Today, these technologies tend to use laser diodes or LEDs for their light sources – but neither is ideal. LEDs are held back by their Lambertian emission profile that translates into low directionality, which hampers coupling to optical elements, such as fibres and waveguides. Laser diodes are better in this regard, because they emit a narrow beam of light that enables simple, efficient coupling to optical elements. What's more, they have a reduced output dimension, so are much closer to an ideal point-like source, aiding optical system design. However, their monochromatic spectral emission, arising from the Fabry-Pérot cavity that is required for optical feedback, results in a high degree of temporal coherence. This is undesirable: when the laser is used to form an image, it is plagued by an interference pattern, commonly referred to as speckle. This is a particularly troublesome for augmented-reality applications, where high-fidelity images are critical. Despeckling solutions have been developed to minimize interference. But success is limited, and the hardware that is required is often too bulky or expensive to incorporate into consumer electronic devices.

What's needed is a source that combines the best attributes of the laser and the LED. And the good news is that this device already exists, in the form of a superluminescent LED (SLED). It provides a directional light source with a broadband emission spectrum that yields a low degree of speckle noise and a high image quality (see Figure 1).

We are pioneering SLEDs at Exalos, Switzerland. One of our milestones came in 2009, when after three years of development, we introduced the industry's first blue-violet (420 nm) SLED in collaboration with the Ecole Polytechnique Fédérale de Lausanne. Fast-forward to today and we are still the only manufacturer of violet and blue SLEDs. That's not our only product, however – we are also the leading supplier of a wide range of infrared SLED devices, having shipped more than 300,000 devices for use in a diverse range of applications, from current sensing to fibre-optic gyroscopes and optical coherence tomography.

Recently, we have focused our efforts on increasing the emission wavelength of our SLEDs. If blue and green devices, made from the III-nitride material system, can be paired with red SLEDs based upon more well-characterized GaAs structures, then this triumvirate can be used to form a full-colour display. There is much work to do, though, as the performance of blue SLEDs can still be improved, while those in the green are still in their infancy.

The SLED design

All our SLEDs share the edge-emitting, ridge-waveguide architecture of the laser diode. However, to prevent optical feedback and lasing, cavity effects are limited by increasing mirror losses at the output facet. There are several options for realizing this: tilting the output facet by several degrees, applying an anti-reflection coating to this facet, or adopting a combination of the two. By inhibiting the laser

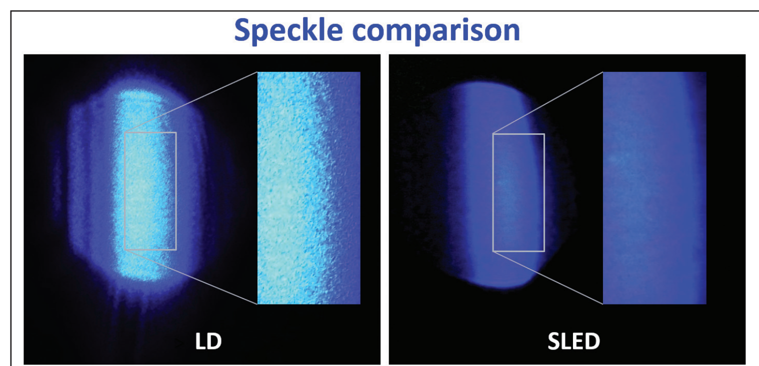

Figure 1. The speckle noise in the far-field pattern of a blue laser diode (left) is far higher than that produced by an SLED (right).

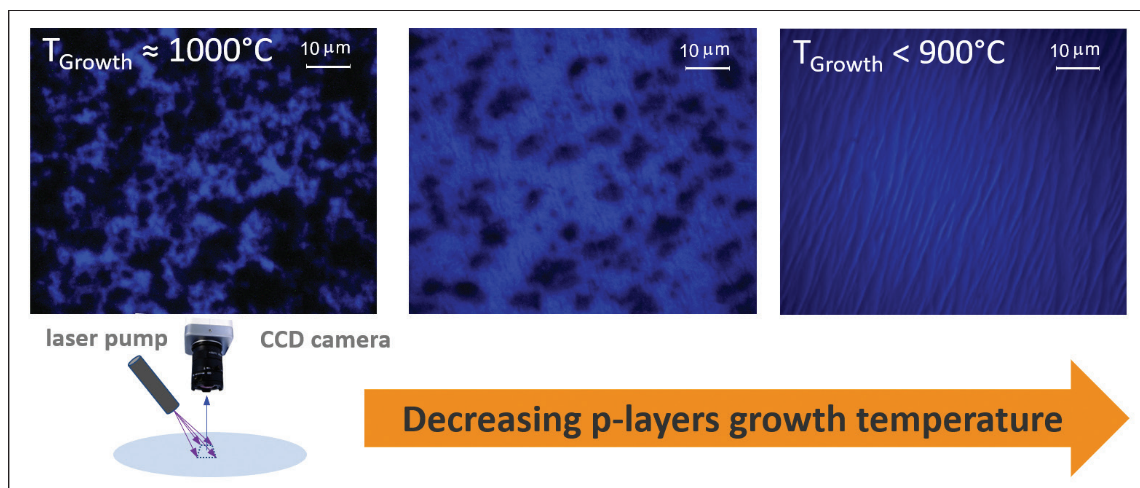

Figure 2. Fluorescence images of InGaN active regions with *p*-doped layers show that growth at lower temperatures does not have to lead to a decrease in material quality.

action, a directional, broadband emission beam is realized through the stimulated emission of carriers. The spectral bandwidth is far broader than that of a laser, and governed by the gain characteristics of the semiconductor material.

Our efforts at developing blue and green SLEDs are building on the success we had in 2015 with 405 nm devices. Back then we demonstrated a continuous-wave, high-power, single-mode 405 nm SLED that delivered a record output power of 350 mW at room-temperature under a drive current of 500 mA. The ex-facet optical powers falls to 20 mW, while the associated bandwidth, full width at half maximum, is 3.5 nm, when the current is reduced to 100 mA and the device operated under the same conditions.

Another attribute of those devices from 2015 is their low forward voltage: it's just 5 V at 100 mA. We accomplished this by optimising the magnesium doping levels in the *p*-type layers. The presence of magnesium impacts the electro-optical characteristics of the device and its reliability, but by fine-tuning the magnesium, we produced continuous–wave, 10 mW SLEDs with a projected lifetime of about 5000 hours (for a case temperature of 25 °C, and applying a failure criterion of a 35 percent increase in drive current).

With all III-nitride-based devices – and laser diodes in particular – there are technical and historical reasons why violet emitters emerged first, followed by blue and eventually green variants. Historically, development focused on 405 nm violet laser diodes, because the short wavelength allowed an increase in optical data storage and was selected as the Blu Ray standard. More recently, interest has grown in blue and green lasers, due to their suitability for displays.

Shifting the emission wavelength of any III-nitride emitter from the violet to the blue or green is far from trivial. There are several challenges associated with realising sufficient crystal quality within the light-emitting layers, and finding a suitable combination of compounds for creating efficient waveguide structures.

Better blues

At the heart of all III-nitride emitters are active regions with InGaN quantum wells sandwiched between GaN

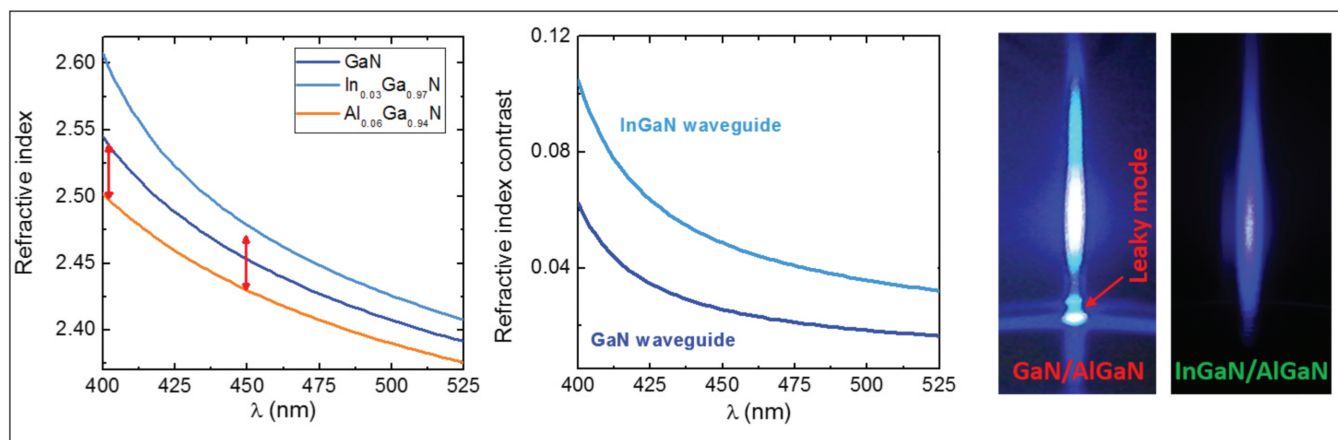

Figure 3. (Left) Refractive index evolution as a function of wavelength for GaN, $In_{0.03}Ga_{0.97}N$ and $Al_{0.06}Ga_{0.94}N$. (Centre) Refractive index contrast evolution for GaN/AlGaN, and InGaN/AlGaN waveguide/claddi ng combinations. (Right) Far-field pattern for the two different architectures showing strong substrate leakage for the GaN/AlGaN architecture.

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  What form will 5G take? And how good will 5G be for GaAs and GaN?
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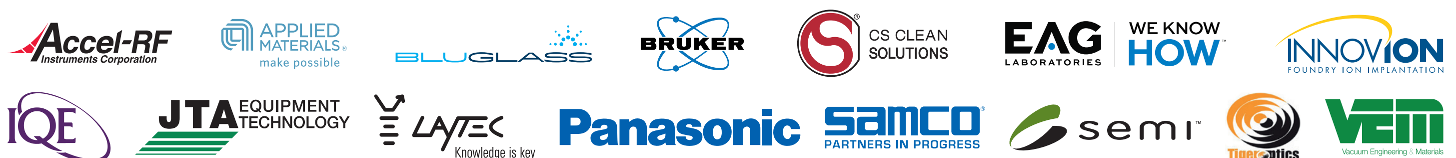

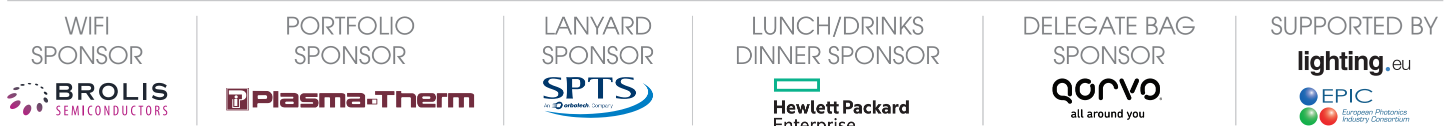

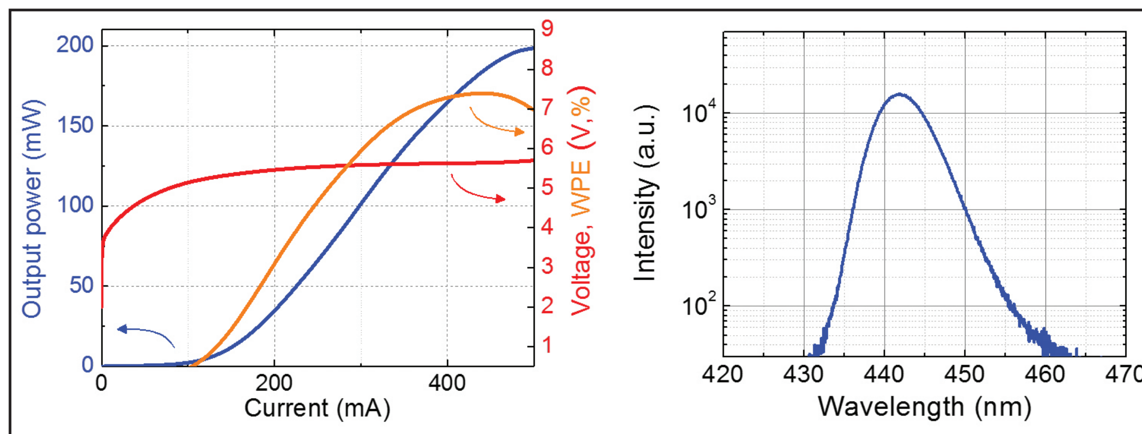

Figure 4. (Left) Light-current-voltage characteristics and wall plug efficiency of Exalos blue SLEDs under continuous-wave operation. Emission spectra at 200 mA (right).

barriers. To increase the emission wavelength, more indium must be added to the quantum well. The indium content is moderate in a blue-emitting well, and high in one emitting in the green.

Adding more indium to a quantum well has its downsides. Lattice mismatch to other layers increases, dragging down device performance and trimming the critical thickness of the well, which in turn reduces gain. More indium also means more defects, and a higher electric field in the active region. If growth of the device is undertaken along the polar direction (*c*-axis), these fields can pull apart electrons and holes, impairing radiative efficiency. What's more, to incorporate more indium in the wells, the epitaxial growth is performed at a lower temperature – and this can result in the degradation of crystal quality, and also unwanted contamination.

Another issue is that as the indium content is increased in the quantum wells, there is a fall in the thermal stability of the active region. After the active region is grown in a SLED structure (and also a laser diode), the growth temperature is raised for the deposition of the *p*-type waveguide and cladding layers. The higher temperature can degrade the wells. While growth temperatures for the p-type layers of typically above 1000°C are suitable for the production of 405 nm devices, they degrade the performance of blue and green emitters.

To address this particular issue, we have worked on reducing the temperature for the growth of the *p*-type layer while ensuring that it still provides good electrical conduction. Lowering the growth temperature has its drawbacks, including reductions in both the incorporation efficiency of the *p*-type dopant, magnesium, and the conductivity of the *p*-layers. However, there is a sweet-spot below 900°C, where *p*-type waveguide and cladding layers with good electrical characteristics can be grown that do not lead to the creation of extended defects in the quantum wells (see Figure 2). This growth condition is suitable for both blue and green SLEDs.

Unlike the laser, the SLED relies on single-pass amplification of light. The output produced by this device depends on the material properties of the active region, and also on the light-guiding effects that are related to the architecture.

One way to improve performance is to increase the optical confinement within the device. This is accomplished by cladding the active region and the waveguide with a lower refractive index material, typically AlGaN. However, when moving from violet to longer wavelengths, the difference between the refractive index of this cladding and the waveguide diminishes, leading to a lower optical confinement and a compromised output power (see Figure 3). This means that the traditional combination of a GaN waveguide and an AlGaN cladding, used in violet devices, is unsuitable for blue and green devices.

Our solution is to switch from GaN waveguides to those made from InGaN. To determine the best design, we have undertaken extensive simulations on waveguide-cladding architectures, uncovering ideal layer thicknesses and compositions. This effort has also led to an improvement in output beam quality, due to a dramatic reduction in the leakage of light towards the substrate. To realise this benefit, we had to increase the material quality of InGaN, so that this could guarantee low optical and carrier losses in

Our recent results reveal that considerable progress has been made in the development of blue SLED devices. However, further improvement is required for mainstream adoption.

the waveguide. Note that we still use AlGaN in our devices, in the cladding layers. In fact, the bottom cladding is a much thicker layer than it would be in a violet device, in order to reduce the leakage of the optical mode to the substrate.

One of the challenges of incorporating AlGaN into the device is that it has a smaller lattice parameter than GaN, so when this ternary is grown on high-quality GaN freestanding substrates used for laser diode and SLED epitaxy, tensile strain builds up in this layer. Consequently, strain management is critical to prevent cracking in the thick AlGaN layer needed to reduce optical leakage. By applying strain release technologies, we can manage the strain so successfully that we can double the thickness of the AlGaN bottom cladding layer.

Optimising devices

One of the similarities between the SLED and the laser diode is the areas of focus for optimising performance: both devices require low optical losses, high injection efficiency, and high gain. However, gain-guided laser diode processing is extremely rapid, while single-mode SLED processing is complicated and time consuming. So, to speed development, we have processed our epiwafers into both SLEDs and gain-guided laser diodes. The latter device provides fast feedback on the lasing characteristics of the quantum-well structure, such as laser threshold and slope efficiency. By varying the reflectivity of the facet coating, it is also possible to uncover internal device parameters, such as optical losses, modal gain, and carrier injection efficiency.

Using this approach we have developed and optimised blue laser diodes and SLEDs with operating wavelengths of more than 440 nm. Initially, the threshold current densities in uncoated gain-guided laser diodes were as high as 7 kA cm^{-2}. However, these fell to below 3 kA cm^{-2} after we addressed numerous challenges related to optical confinement, active region stability, and the more-general crystal quality of the layers.

These refinements also led to an increase in slope efficiency, with output from a single facet jumping from 0.3 W/A to more than 0.6 W/A for uncoated devices. Turning to a high-reflectivity rear-facet coating and an uncoated front facet provided further improvement, with the slope efficiency exceeding 1.2 W/A in the latest gain-guided devices. Even lower threshold currents are possible by partially coating the front facet. This enabled threshold currents below 1 kA cm^{-2}.

Using the variable facet coating method, we observed a constant decrease in internal losses during the epitaxial development. Improvements in material quality resulted in a 50 percent reduction in these losses, from above 12 cm^{-1} to below 6 cm^{-1}.

We have processed our optimized epiwafers into single-mode SLEDs. Housed in a TO-can and driven in continuous-wave mode at room-temperature, these blue-emitting devices have current-voltage characteristics that are comparable to 405 nm devices – voltages are only few tenths of a volt higher, despite growing the *p*-doped layers at far lower temperatures.

The ex-facet output powers for our SLEDs exponentially increase above 60 mA. This is encouraging, because it is a typical signature for the appearance of gain in the structure. When the current is increased to 120 mA and then on to 200 mA, the output power rises to 5 mW and 30 mW, respectively, with emission centred at 442 nm. Even higher output powers are possible – the maximum is just short of 200 mW without any specially designed heat sink. These powers levels, along with wall plug efficiencies of more than 5 percent, are the highest reported values for any blue SLEDs.

As the next wave of consumer devices for augmented reality applications evolves, the various, competing display architectures will be evaluated. The SLED will surely be a leading candidate, thanks to its unique spectral and spatial properties that give it compelling advantages as an illumination source, especially for near-to-eye architectures.

Our recent results reveal that considerable progress has been made in the development of blue SLED devices. However, further improvement is required for mainstream adoption. We are on track to delivering higher-efficiency devices at 450 nm, and will strive to extend the emission to longer wavelengths. Once emission exceeds 510 nm, SLEDs can provide the ultimate source for red-green-blue illumination.

Further reading
Castiglia et al., Proc. of SPIE Vol. 9748 (2015)

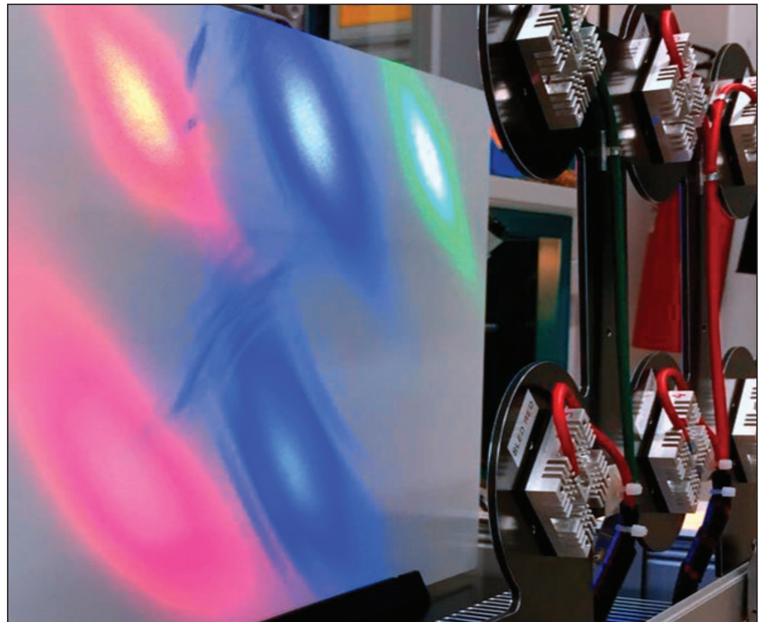

Figure 5. Exalos demonstrator presented at Display Week 2017 comparing red-green-blue laser diodes (top row) to Exalos red and blue SLEDs (bottom row).

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  Meeting the challenge of producing PICs at high-volume
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  CORNERSTONE: Silicon photonics fabrication capability based on DUV lithography
- **Michael Geiselmann: LIGENTEC**
  Silicon nitride for new PIC applications
- **Florent Gardillou: Teem Photonics**
  Photonics on glass : The ioNext PIC platform
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  The Zettabyte is not enough: Volume handling for InP, silicon photonics, and hybrid photonic integration
- **Radha Nagarajan: Inphi**
  Silicon Photonics for distributed data centre interconnects
- **Weiming Yao: JePPIX/PITC**
  III-V photonic integrated circuits for telecoms and beyond
- **Peter Winzer: Nokia Bell Labs**
  Massive array integration and the need for a holistic digital/analog optics/electronics co-design
- **Eric Mounier: Yole Développement**
  Data centre technology - the big PICture, opportunities for energy efficient photonics

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PIC Design, Simulation and Packaging: A Blueprint for Future Success

How can we implement ideas faster and what needs to be considered to keep the final device cost on track?

SPEAKERS

- **Peter O'Brien: Tyndall National Institute**
  PIXAPP – Open Access Opportunities for Advanced PIC Packaging
- **Robert Scarmozzino: Synopsys**
  PIC Design: From concept to manufacture
- **Christopher Cone: Mentor Graphics**
  From schematic to layout – overcoming today's PIC design challenges
- **André Richter: VPIphotonics**
  Scalable design of integrated photonic and optoelectronic circuits

PIC Horizons: New and Emerging Applications for Integrated Photonics

How can developers capitalize on opportunities for optical platforms in growth areas such as medical diagnostics, industrial sensing and biological analysis?

SPEAKERS

- **Milan Mashanovitch: Freedom Photonics**
  Low size, weight and power (SWaP) instruments for sensing applications - cutting edge PICs
- **Sascha Geidel: Fraunhofer ENAS**
  Adding the 'tech' to biotech - opportunities for photonic integrated circuits
- **Andrew Sparks: Analog Devices**
  Lidar for autonomous driving: Key technological opportunities

Panel: Has Silicon Photonics got the Required Scalability to Displace InP?

Silicon photonics has attracted the interest of many in large corporations, SMEs, and academics as a potential replacement to the incumbent PIC technology InP. Given these conditions, the question remains to ask if SiP can be truly scalable towards $1/Gbps at 400Gbps data rates and above (for any distance)?

Bert Jan Offrein – IBM
Di Liang - Hewlett Packard Enterprise
Robert Blum – Intel
Sean Anderson – Cisco

Panel: High Volume Transceiver Opportunities for PICs

Will transceivers ever achieve super high volumes to allow scalability in cost and performance, and if so, what would be the common large volume platforms, and more specifically, what would be the transceiver format/form factor?

Aref Chowdhury – Nokia
Drew Nelson – IQE
Vipul Bhatt – Finisar

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3D integration

unites InP, GaN and silicon CMOS

Devices in multi-material stacks deliver uncompromised performance, thanks to active substrates, wafer bonding and thermal vias

BY ANDREW CARTER AND MIGUEL URTEAGA FROM TELEDYNE SCIENTIFIC AND IMAGING

COMPARED with silicon-based technologies, devices made with III-Vs offer superior high-frequency performance and better power handling characteristics. However, that's not to say that silicon does not have a role to play. Electronic platforms made from III-Vs lack integrated low-power digital logic, so when they are used to make complex mixed-signal III-V-based systems, they have to interface with silicon CMOS at some level.

If these two material systems are united through intimate heterogeneous integration, this can unlock the door to new classes of microsystems that combine the performance of III-V transistors with the vast IP and manufacturing resources of CMOS. One of the key challenges is to ensure that the heterogeneous integration process does not impair the intrinsic performance of the III-V devices.

There are many different approaches to realising the heterogeneous integration of compound semiconductors and silicon (see Figure 1 for an overview). One option is to simply tile devices made from different materials onto an interposer.

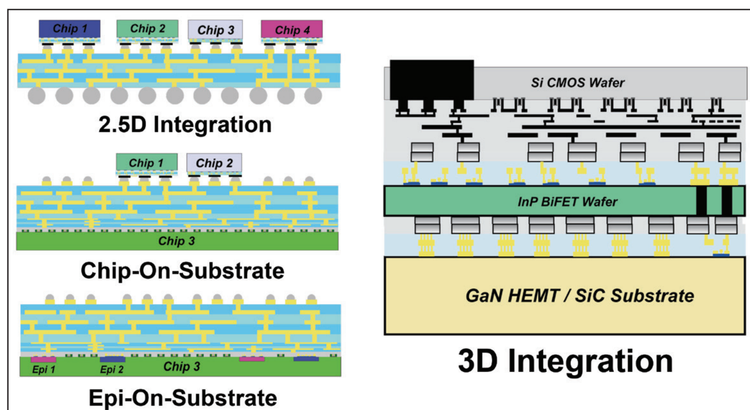

Figure 1. There are various options for realising the heterogeneous integration of compound semiconductors.

With this scheme, known as 2.5D integration, all the materials must form suitable mechanical and electrical interfaces. In general, this is not too tricky, thanks to technologies such as bump bonding and thermocompression bonding. However, the underlying interposer can be prohibitively expensive if the wiring density is too high.

A variation that may address this weakness is the use of an interposer that is also a common active device substrate, such as silicon CMOS. With this approach, some of the interposer cost may be deferred, because it is pre-populated with a technology. Another merit is the dense wiring environment. However, both these benefits can be overshadowed by interchip parasitic losses, which can prevent the system from accessing each technology's intrinsic performance.

This pitfall can be avoided through the epitaxial growth of all technologies on a common substrate. Another advantage with this approach is that the devices can then share a common wiring environment. However, the host substrate is costly; and there is the potential for poor device thermal management, due to thick epitaxial buffer layers.

At Teledyne Scientific and Imaging, we have recently shown that the latter issue is not insurmountable. Using hybrid fusion wafer bonding for electrical interconnection, we form stacks that integrate silicon CMOS with InP and GaN technologies. These stacks feature a high thermal conductivity SiC substrate to improve heat management.

Our three-technology stack combines silicon CMOS with InP BiFETs (HBTs and HEMTs on the same substrate) and GaN HEMTs. Virtues of our technology include minimal inter-technology electrical parasitics and adequate heatsinking for all types of device.

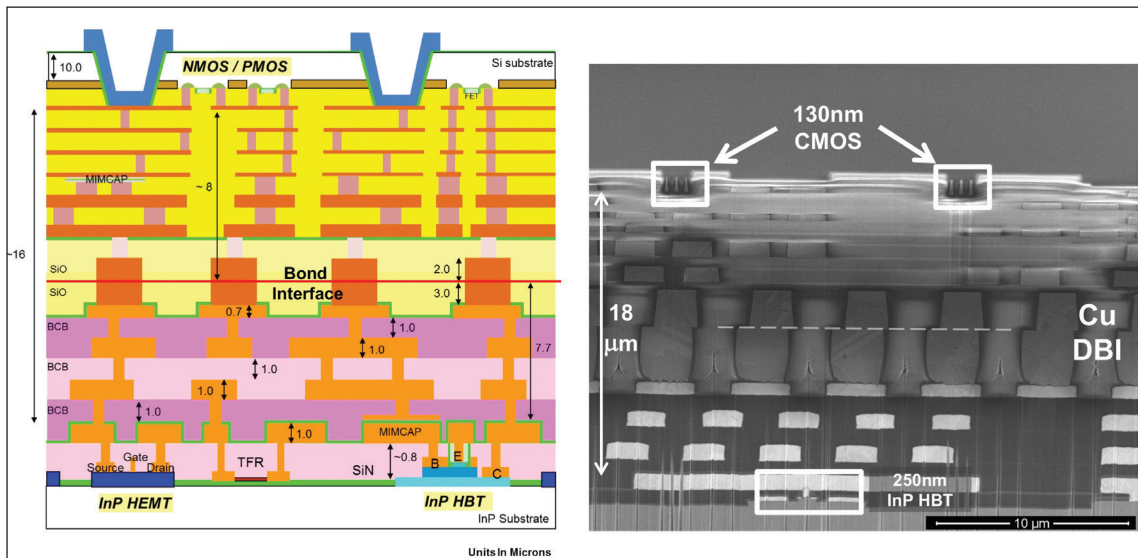

Figure 2. Silicon/InP wafer stacking: schematic cross-section of the technology, and a FIB/SEM cross-section of the completed process.

At the top of our three-technology stack sits silicon CMOS. This is populated with lower power devices, so minimal heatsinking is required. Below this is the InP device technology, with the InP substrate thinned to 10 µm and bonded face-up to a GaN-on-SiC substrate, which sits at the bottom of the stack to ensure optimal thermal dissipation.

We use Tessera Direct Bond Interconnect (DBI) technology to adhere one material system to another. This approach employs copper vias embedded in a dielectric – in this case silicon dioxide – and electrical contacts between each substrate, which is aligned to another in either a face-to-face or back-to-face orientation. The pitch for the heterogeneous interconnect via is just 5 µm, so for a chip size of 1 cm^2, it is possible to have as many as 4 million interconnects. To connect InP to GaN, a tungsten through-substrate-via is formed in InP, and a Direct Bond Interconnect is formed on the back of the thinned InP and the top of a GaN-on-SiC substrate.

Our efforts at developing our triple-stack technology have been divided into two separate but complementary directions: silicon/InP face-to-face bonding, and InP/GaN back-to-face bonding.

InP and silicon CMOS

The face-to-face bonding of silicon and InP enables a form of 3D heterogeneous integration that offers a significant benefit in space-constrained microsystems. Consider, for example, RF beamformer ICs currently in use for radar and high-data-rate communications systems. They consist of an array of gain- and phase-controlled receiver and transmitter channels. By controlling the gain and phase of each channel, it is possible to steer the electronic beam of the major lobe of the beamformer's radiation pattern. To generate the largest scan angle, all the transmitter/receiver antennae are placed on a grid and spaced apart by a distance equal to half the free-space wavelength of the centre frequency of the beamformer. With these RF systems, the trend is to move to higher frequencies, so antennae must be placed closer together. One consequence is that system packaging constraints come into play. That's not a major issue for our technology, however, because our form of 3D integration brings silicon control logic in close proximity to the InP, and can realise ideal grid spacing at millimetre-wave frequencies.

A key building block for our beamformers operating at millimetre-wave frequencies is our 250 nm InP HBT technology. These devices, which have a 250 nm emitter width, combine maximum values for f_t and f_{max} of 360 GHz and 700 GHz, respectively, with a common-emitter breakdown voltage of 4.5 V.

We have also developed an InP BiFET process, with

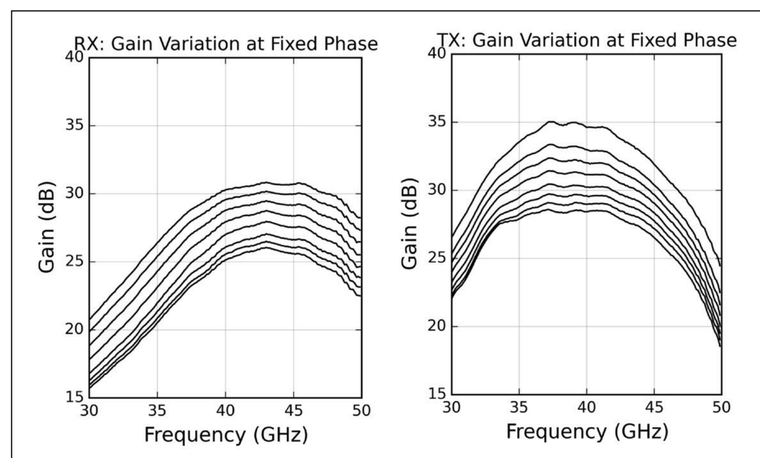

Figure 3. InP/silicon Q-band receiver and transceiver channel RF gains over all states for a fixed phase state.

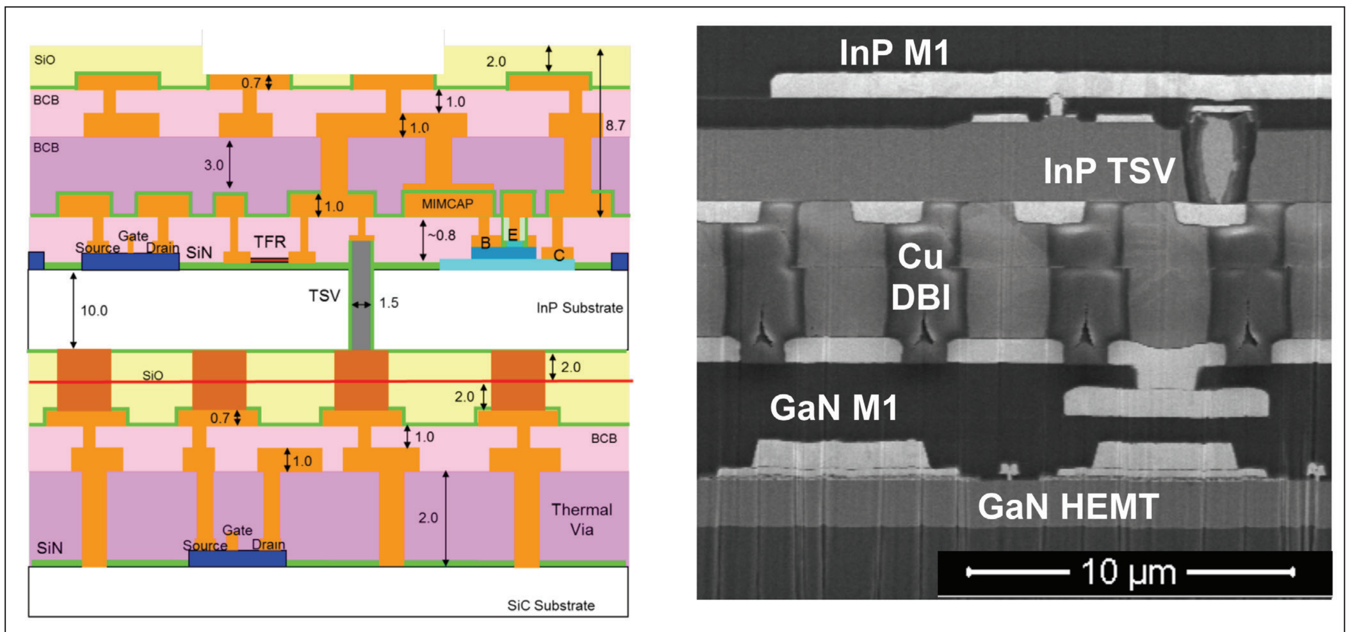

Figure 4. InP/GaN wafer stacking: schematic cross-section of the technology, and a FIB/SEM cross-section of the completed process.

InP/InGaAs HBTs and InGaAs HEMTs co-planar on the same InP substrate. The HEMTs enable low-noise amplifiers and RF switches for switched transmit/ receive channels.

Our standard InP HBT wiring environment utilizes: a benzocyclobutene insulator, which has a dielectric constant of 2.7; three levels of electroplated gold wiring; and thin-film resistor and metal-insulator-metal capacitor passive elements. The InP device is complemented by one made from silicon, using the 130 nm silicon CMOS process at GlobalFoundries. This CMOS technology offers six levels of copper metal wiring and passive circuit elements.

To design the InP and CMOS device layout and simulate the resulting circuit, we use an integrated Cadence process design kit. Its merits, which can be applied to both technologies, include design-rule checking and layout-versus-schematic checking.

To apply Direct Bond Interconnect technology to InP, we modified the standard back-end-of-line wiring environment. Adjustments included improving dielectric adhesion to the substrate and gold wiring, and developing chemical mechanical polishing process for the 100 mm InP substrate. We found that applying successive rounds of plasma-enhanced CVD of silicon dioxide, followed by chemical mechanical polishing, helped to remove non-planarities on the top of the processed wafer. After this, we pattern and etch the polished silicon oxide, and fill with electroplated copper to form the interconnects.

Thanks to our RF beamformer R&D efforts, using various heterogeneous integration strategies, 3D stacking has been shown to provide compact circuit designs for RF and mixed signal millimetre-wave applications.

With silicon CMOS wafers, we use a similar process. In this case, once the wafers are bonded, the silicon wafer is ground and polished until it is just 10 μm thick, before bond pads are formed on the backside of the wafer, connecting to CMOS M1.

We have scrutinised the resulting structure with a scanning electron microscope (see Figure 2). Cross-sectional images reveal the InP HBT and CMOS FET, and show that the M1-to-M1 vertical distance between the technologies is approximately 18 μm. This is short enough to ensure a low parasitic interconnect between the metallization layers.

Our structure has been used to make receiver and transmitter beamformer channels operating in the Q-band at 40 GHz. The receiver channel includes an InP HBT low-noise amplifier, an InP HBT/silicon CMOS 3-bit variable gain amplifier, and a InP HBT/ silicon CMOS 4-bit phase shifter. Within the transmitter channel there is an InP HBT/silicon CMOS 4-bit phase-shifter, an InP HBT/silicon CMOS 3-bit variable gain amplifier, and an InP HBT power amplifier.

Characterisation of DC and RF performance reveals that the receiver consumes 240 mW, while the transmitter draws 1 W. For the receiver, variable gain control at 40 GHz is 25.1 dB to 30.3 dB, while for the transmitter it is 28.4 dB to 34.6 dB (see Figure 3). In this configuration, the highest gain state's 1-dB

bandwidth at around 40 GHz is 10 GHz for the receiver and 8 GHz for the transmitter. The root-mean-square phase error for the receiver and transmitter at 40 GHz are 4.6 and 4.8 degrees, respectively. For the transceiver channel, the saturated RF output power is 20.3 dBm (107 mW) at 40 GHz. According to measurements with a Keysight PNA-X equipped with factory-installed noise figure hardware (impedance tuner and low-noise receiver front-end), the channel noise figure at 40 GHz is approximately 4.2 dB. This is in close agreement with simulations of the standalone low-noise circuit, including bond pad loss, that show a noise figure of 4.0 dB.

Uniting GaN and InP

Thanks to its high bandgap of 3.4 eV, the GaN HEMT combines excellent high-frequency performance with high breakdown voltages. However, these amplifiers can have low-to-moderate gain at millimetre-wave frequencies, so high-power input signals are required to drive them into compression.

One potential solution is to insert a high-efficiency InP driver amplifier before the GaN stage. The large bandwidths available in InP HBT technology permit high power-added efficiency designs at millimetre-wave frequencies.

To ensure optimal heat dissipation for both devices, InP and GaN technologies must be stacked with a back-to-front wafer bond. Another pre-requisite is the use of through-substrate-vias, to electrically interconnect the substrates.

We create the vias by dry etching the InP substrate with a Cl_2-based gas. Using optimized conditions, aspect ratios as high as 8:1 are possible. During the construction of our hybrid structures, we target a 10 μm-deep through-substrate via. After etching, CVD fills the via with tungsten. Any excess is removed with chemical-mechanical polishing, to leave a tungsten via recessed from the InP surface.

Following the formation of the through-substrate vias, we adopt a standard InP device process flow. After back-end-of-line low-κ dielectric and metallization steps, we prepare the topmost wafer surface for planar SiO_2 bonding to a temporary silicon handle wafer. The strength and planarity of this bond allow the InP substrate to be thinned to just 10 μm, revealing the tungsten through-substrate vias.

The next step is the addition of a copper Direct Bond Interconnect pattern on the thinned backside of the InP substrate. This is united to the GaN-on-SiC substrate with an electrically active bond, before the silicon handle is removed with a combination of grinding and dry etching.

Inspecting a cross-section of this structure, using scanning electron microscopy, reveals that the final InP thickness is less than the 10 μm target – it is

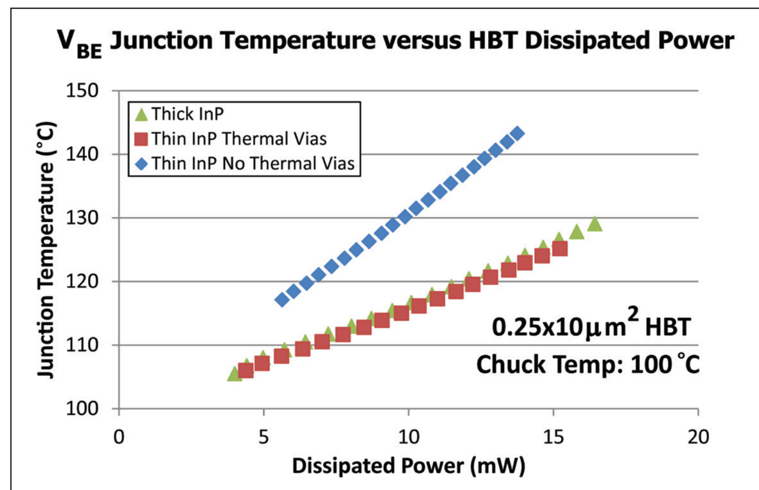

Figure 5. Thermal vias allow thinned InP to provide the equivalent degree of thermal management as a baseline device, according to measurements of the temperature of the base-emitter junction.

just 4 μm (see Figure 4). This shortcoming will be addressed with a modified through-substrate via reveal process that will ensure a consistent wafer thinning for future lots.

Our InP HBTs and GaN HEMTs have been characterized for DC and RF performance. Measurements on pre- and post-bonding structures reveal that characteristics remain similar before and after integration.

Despite thinning InP to well below its target value, devices retain their performance, even though they sit on top of high thermal resistance materials, such as SiO_2 and benzocyclobutene. Success stems from the thermal vias, which shunt heat from the InP substrate into the low thermal resistance SiC substrate.

Our work highlights the benefits of 3D wafer stacking in compound semiconductor circuit designs. Thanks to our RF beamformer R&D efforts, using various heterogeneous integration strategies, 3D stacking has been shown to provide compact circuit designs for RF and mixed signal millimetre-wave applications.

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

Further reading

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Printing GaN HEMTs onto silicon CMOS

A micro-transfer printing technique could boost the efficiency of integrated power electronics by uniting high-performance GaN HEMTs with highly integrated silicon CMOS

BY STEFAN EISENBRANDT AND RALF LERNER FROM X-FAB

LYING AT THE HEART of the majority of today's power ICs are three classes of silicon transistor – those with either a laterally diffused metal-oxide-semiconductor design, an insulated-gate bipolar architecture, or a super-junction configuration. All these workhorses can handle high voltages, high currents, or a combination of both.

It is known from Moore's law that miniaturising these transistors would deliver an evolutionary improvement in performance, but at the expense of spiralling development efforts. Better still is a revolutionary performance gain. This is possible, via the integration of III-V materials.

One of the most promising III-V devices for power electronics is the GaN HEMT. Compared to all forms of silicon device, it sports superior switching speeds, and it also has the upper hand when considering the trade-off between the on-resistance and the breakdown voltage. Thanks to these merits, the GaN HEMT can enable new, highly efficient power conversion topologies that would be unthinkable with state-of-the-art silicon based devices.

Let's not write silicon off just yet, however. Note that bipolar-CMOS-DMOS and high-voltage CMOS technologies have realised high levels of diversification, leading to the highest design complexities. These devices can be used in Smart power ICs, which enable an interface between digital control logic and the power load. By using monolithic integration to position output power devices next to digital and analogue circuitry, it is possible to combine signal processing, sensing and protection circuitry on the same chip. Further benefits of this approach are a trimming of the number of interfaces, the volume, and electromagnetic interferences. The upshot is increased efficiency, performance and reliability.

Engineers working with compound semiconductor technologies are also trying to realise the high-level of functional integration seen in these silicon-based, Smart power ICs. Several technologies for integrating GaN HEMTs with digital and analogue circuitry are currently being pursued: GaN-based Smart power ICs; monolithic integration of GaN on silicon; wafer bonding of GaN on silicon; and the approach that we are investigating at X-FAB Semiconductor Foundries of Erfurt, Germany: heterogeneous integration, enabled by micro-transfer-printing (see Figure 1).

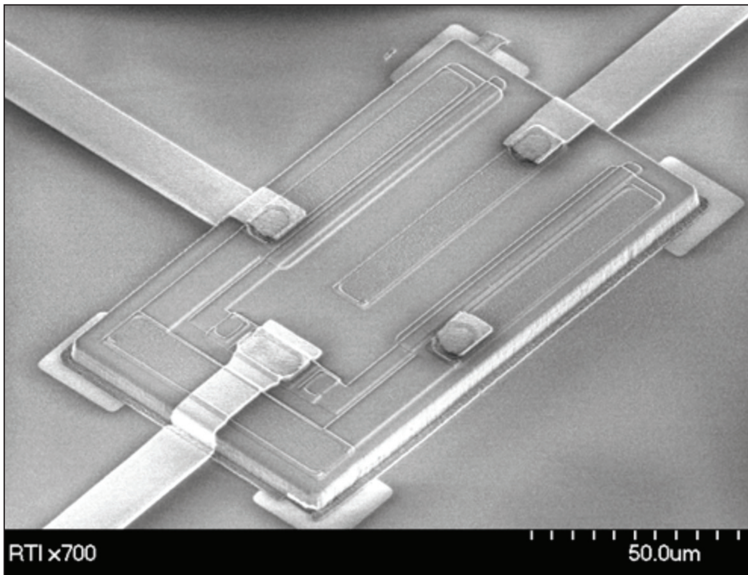


Figure 1. Micro-transfer-printing can position a GaN HEMT on a silicon CMOS wafer, prior to subsequent on-wafer metallization.

Rival approaches

Several groups are working on integrating GaN power devices with GaN digital and analogue circuitry on the same substrate. The downside of this approach is the lack of feasibility of standard silicon-CMOS-like circuit topologies, due to an inferior hole mobility and the absence of high-performance *p*-channel GaN devices. Due to these weaknesses, it may take years to realise high integration densities and functional diversification with GaN-based logic.

Monolithic integration of GaN and silicon CMOS is another option for uniting GaN-based transistors with CMOS logic. Both devices can be fabricated on the same silicon substrate, with custom silicon-on-insulator wafers providing tiers for each technology: <100> oriented silicon for CMOS and <111> oriented silicon for GaN. The GaN and silicon transistors are not vertically integrated, but are arranged laterally side-by-side.

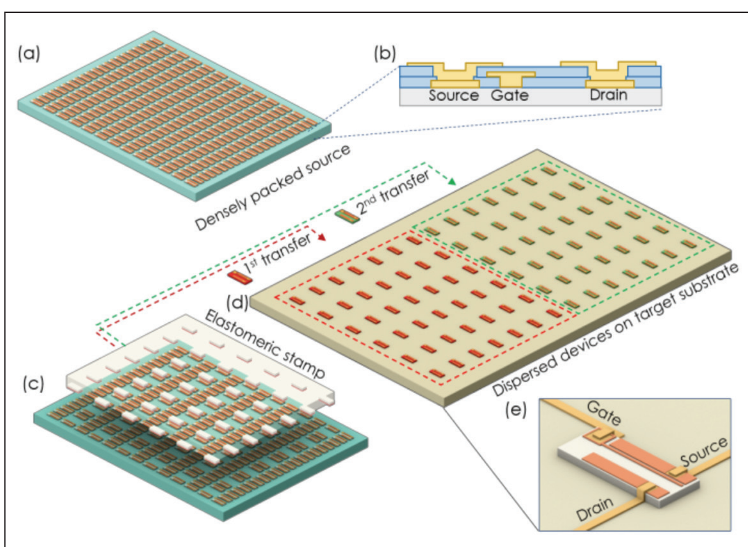


Figure 2. An overview of the micro-transfer-printing process for GaN HEMTs. (a) Source wafer with dense array of HEMTs, (b) HEMT cross-section, (c) elastomeric stamp removes an array of HEMTs from source wafers, (d) first and second printing process on new target substrate, for example a CMOS Wafer, (e) wiring of printed GaN HEMT on wafer.

A team from Raytheon has pioneered this approach. To reduce the thermal budget, they deposited the GaN layers by MBE, rather than MOCVD. The price to pay for this is a lower throughput, making this approach unfavourable for mass production of higher voltage devices, which require thicker buffer layers.

Additional drawbacks of this approach are: material incompatibilities, such as significant differences in lattice constants and thermal expansion coefficients; device constraints, such as thermal budgets and the restriction of contact metallization materials to CMOS-compatible metals; and high costs. Note that due to the partitioning issue associated with monolithic integration, costs can skyrocket. For example, for an integrated circuit with a total area of 10 mm^2 – comprising 9 mm^2 of logic and 1 mm^2 of GaN HEMT – the costs for the epitaxy process are similar to those for a full-wafer process, but the epitaxial layer is only used on the 1 mm^2 GaN area. Thus, the costs per GaN area, and also the costs per Amp, are ten times higher.

Another option for combining the merits of GaN power devices with those of silicon CMOS is to fabricate each in its dedicated manufacturing environment, before uniting them densely at the chip level. With this approach, every device is designed to its full potential, irrespective of material and processing constraints. That's because integration takes place by wafer bonding in a post-process step.

We have been pursuing this type of approach through a multi-partner project GaNonCMOS, funded by the European Union's Horizon 2020 Research and Innovation programme. Supported by €7.4 million of investment, this effort that kicked-off in January 2017 is aiming to bring GaN power electronic materials, devices and systems to the next level of maturity by providing densely integrated materials. A key goal within the project is to realise long-term reliability improvements over the full value chain of materials, devices, modules and systems.

Micro-transfer printing

One of the key technologies in our project is micro-transfer-printing. Like wafer bonding, it facilitates the post-process integration of GaN power and silicon CMOS devices, but it also allows the deterministic assembly and integration of microscale, high-performance semiconductor devices onto non-native substrates.

The key process with micro-transfer-printing is the picking-up of large arrays of microscale devices from their source wafer with an elastomer stamp, and the subsequent printing of these devices on a retrieving wafer. This is accomplished by housing the stamps

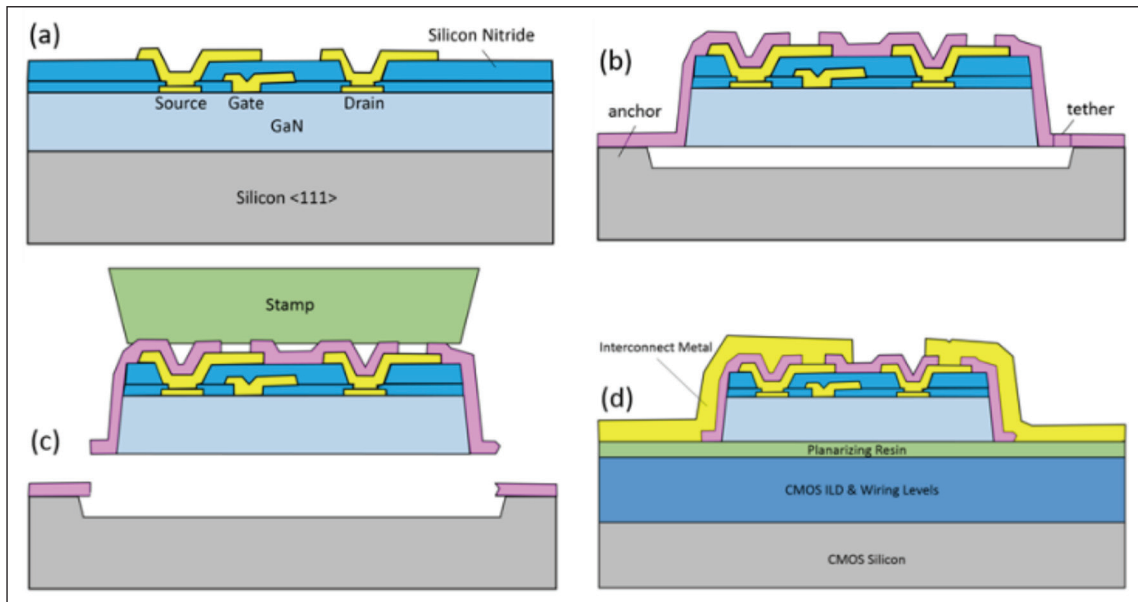


Figure 3. The process flow for heterogeneous integration of GaN HEMTs. (a) The transistors are fabricated on a <111> silicon substrate. (b) The devices are isolated, passivated and then undercut. (c) The devices are retrieved with an elastomer stamp. (d) The devices are printed to a silicon CMOS wafer and then interconnected using thin-film aluminium traces.

on high-precision, motion-controlled print-heads. With this parallel process, many small chiplets carrying GaN HEMTs can be printed onto fully processed silicon CMOS wafers in one go (see Figure 2).

The majority of GaN HEMTs are grown and manufactured on <111> oriented silicon wafers. To prepare them for the micro-transfer-printing process, these devices then need to be released from their native substrate.

In the project that we are involved with, this step is undertaken by reactive ion etching through the device layers and down to the underlying silicon substrate (see Figure 3 (a)). Then, to passivate the sidewalls and form an anchor that tethers the structures, a SiN layer is added by plasma-enhanced CVD (see Figure 3 (b)).

After this, the <111> oriented silicon underneath the device is wet-etched using a high-selective, anisotropic etchant (see Figure 4 (a)). As the etch rate in the {110} family of directions is more than one hundred times faster than it is in the orthogonal directions, regions where the silicon does not undercut remain as anchors for the release process (see Figure 4(c) for an optical microscope image of two fully undercut, print-ready GaN HEMTs with different tether configurations).

Utilising the viscoelastic nature of the elastomer stamp, GaN devices are then picked-up from their source wafer and printed on the CMOS wafer. Due to the high adhesion between the stamp and the GaN device, when the stamp is then moved rapidly away from a bonded interface, the tethers are broken, enabling the pick-up of microscale devices from their native substrates. A different approach is used to print the devices. This time the stamp is gently moved away from the bonded interface, causing the adhesion between the stamp and the device to be lower than that of the bond forces. Due to this, the stamp separates from the chips, which stick on the new, non-native substrate.

Following the micro-transfer-printing process, interconnections are added with standard wafer fabrication processes, such as thin-film deposition and photolithographic patterning (see Figure 3 (d)). With this approach, which involves on-chip wiring, process temperatures do not exceed 175 °C, permitting the use of complex Smart power designs.

Promising results

Small GaN HEMTs have been manufactured with various gate finger configurations, channel widths and

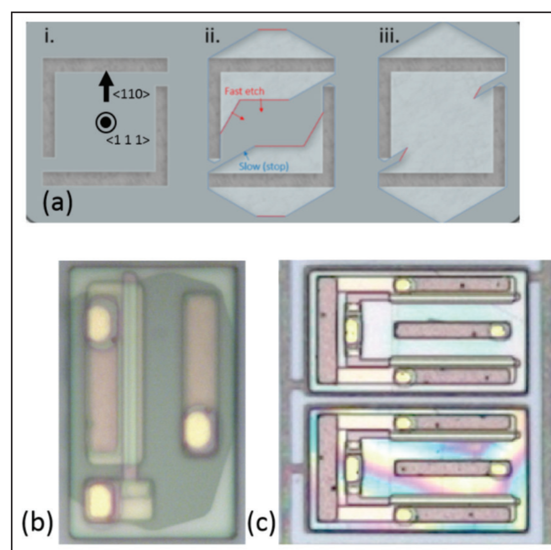


Figure 4: (a) Silicon <111> wet-etching underneath a device. (b) The etch-fronts can be seen by looking through a GaN HEMT that is only partially etched. (c) Optical micrograph of GaN HEMTs that have been fully undercut, with two different tether designs.

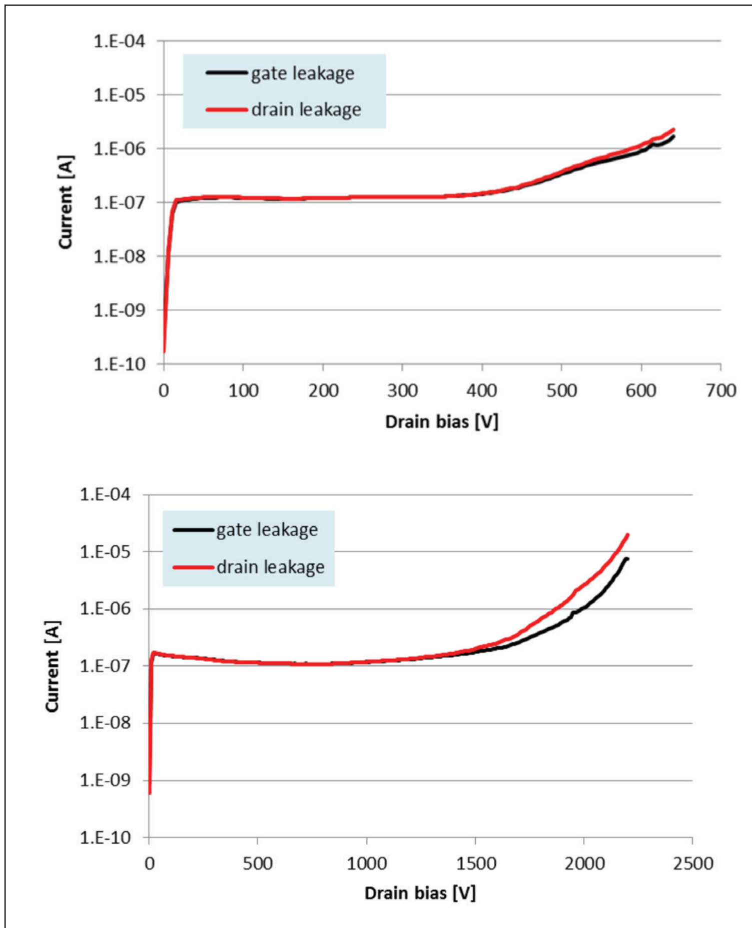


Figure 5: Blocking characteristic of HEMT with gate-to-drain distances of 6 µm (top) and 17 µm (bottom).

gate-to-drain spacings (see Table 1 for an overview). All of these HEMTs have been produced with the same set of processes, and made from the same substrate wafer, which features a GaN epitaxial structure that is about 4 µm-thick. Using the processes described above, the HEMTs have been transferred to two types of wafer: completely processed silicon CMOS wafers; and trench-isolated, silicon-on-insulator high-voltage CMOS wafers.

The benefits of printing HEMTs directly on top of CMOS are not limited to a smaller footprint for the final device – they also enable shorter wiring between the logic and the HEMT, reducing parasitic inductances and capacities (see box "Strengths of micro-transfer-printing" for a detailed list of benefits).

Initial results include characteristics for a 20 V NMOS transistor that are undisturbed by the printed HEMT, and promising room-temperature, drain-source blocking mode characteristics for the printed GaN HEMT device (see Figure 5). Using a fluorinert protection layer to avoid surface flash overs and premature breakdowns, printed HEMTs have achieved blocking voltages of between 600 V and 1800 V, dependent on the drain-gate spacing.

During the release etching, the conducting silicon substrate is removed, allowing the printing of the HEMT on top of the isolating CMOS dielectric. This eliminates a vertical leakage path through the silicon, and it restricts the breakdown mechanism, so that

Gate fingers	Total gate width [µm]	Gate-Drain spacing [µm]	Active device area [µm²]	Printed device area [µm²] *)
1	50	17	2279	4956
1	50	6	1696	3983
1	100	17	4429	7614
1	100	6	3296	6063
2	150	17	5694	12264
2	150	6	3978	9052
2	200	17	7519	14280
2	200	6	5253	10540
4	300	17	10374	24675
4	300	6	6942	21000

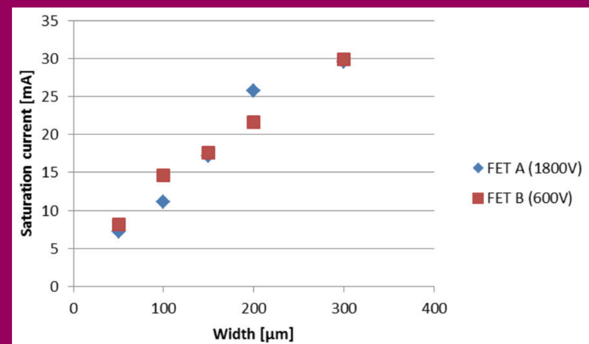
*) including gate pads, source finger shorts etc.

Table 1: GaN HEMT geometry overview

Strengths of micro-transfer-printing

THERE are many merits associated with micro-transfer-printing:

- The GaN buffer thickness can be significantly thinned without sacrificing the breakdown voltage of the printed devices
- Growth times for the GaN buffer can be shorted, and the related mechanical stress issues can be reduced.
- With thinner GaN, the topology step is decreased when routing the printed HEMTs on the surface i.e. when a metal track has to bridge the printed HEMT's edge.
- A scaling of the breakdown voltage with gate-drain distance enables the manufacture of GaN devices with different breakdown voltages in the same process, and even on the same wafer.
- A scaling of the on-state parameters on-resistance and saturation current is possible with the designed channel width (see figure on the right)
- By removing printing-related mechanical design restrictions, the placement of the printed HEMTs can be realised relative to certain logic blocks. For example, a very close proximity of HEMT and cascode NMOS or gate driver circuitry below the HEMT can be realized.



Current scaling versus transistor width for GaN HEMTs in two voltage classes

breakdown only occurs laterally in the GaN. Due to this, the breakdown voltage is solely determined by the gate-drain distance.

Another task undertaken has been to carry out a thermal TCAD Design of Experiment, in order to identify the main contributors to the thermal resistance of GaN HEMTs printed on top of a CMOS circuit. This effort revealed that there is only a small increase in the thermal resistance due to the CMOS dielectric layers – it is far less, for example, than the thermal contribution of wafer and metallisation thickness. Under AC conditions the thickness of the HEMT has a larger effect on the thermal resistance than the CMOS dielectric layers. Consequently, if silicon is removed in the manner that we have described, along with possible thinning of the GaN buffer layers, the CMOS oxide layers do not increase the total thermal resistance.

The results detailed here have been achieved within device level investigations. The next steps will be undertaken in an ongoing project MIIMOSYS, funded by the German ministry for education and research.

This project – involving Electronic Design Chemnitz GmbH, Fraunhofer Institute for Applied Solid State Physics, TURCK duotech GmbH (TDU), University of Erlangen-Nuremberg, Chair of Electron Devices, and X-FAB Semiconductor Foundries with support from X-Celeprint – is targeting the first ever demonstration of hetero-integrated GaN transistors onto silicon CMOS control electronics at the system level. Topics of future investigations will be the next steps towards a manufacturing process for micro-transfer-printing, the reliability of the involved GaN and CMOS devices and the packaging of micro-transfer-printed devices for bridge drivers and controller ICs for motor and LED driver applications.

The authors acknowledge the contributing work from the Fraunhofer Institute of Applied Physics in Freiburg, Germany (Richard Reiner, Patrick Waltereit and Heiko Czap) as well as from the teams at X-Celeprint in Cork Ireland and Research Triangle Park, NC, USA (Christopher Bower, Salvatore Bonafede, Alin Fecioru, Matthew A. Meitl, António Jose Trindade). The ongoing work is supported by the German ministry for education and research.

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Propelling the GaN VCSEL to the green

Introducing quantum dots enables GaN VCSELs to penetrate the 'green gap'

BY BAOPING ZHANG FROM XIAMEN UNIVERSITY

WHAT DO YOU BELIEVE is most desired in a laser? Is a high modulation speed? Or is it a low-threshold, a high efficiency, or a circular emission profile that tops your wish list?

The good news is that there is a class of laser that can fulfil all of these attributes and more: the VCSEL. Thanks to its all-round capability, sales are flourishing, with devices based on GaAs being deployed in optical mice, sensors and optical networks.

To grow revenues even more, this device must serve even more applications. That's possible by broadening the range of VCSEL emission wavelengths. When GaAs VCSELs emitting in the red and infra-red are joined by GaN-based cousins covering the blue and green, VCSELs can be used in projectors, displays, and solid-state lighting.

Unfortunately, making a GaN-based VCSEL is far more challenging than making a GaAs-based one. That's not to say that there has been no success – several groups have reported electrically driven GaN-based VCSELs that have InGaN/GaN quantum well active layers and produce room-temperature, continuous-wave emission in the near ultra-violet and the blue. But in the green, only Nichia of Japan has made any significant progress. Its team of researchers has succeeded in producing pulsed emission from a VCSEL emitting at 503 nm. However, even this is not true green, but cyan.

The green gap

Propelling InGaN-based devices from the blue to the green is not easy. The problem is well known, and has been given the moniker 'the green gap'.

One of the reasons why it is so difficult to produce efficient emitters between 500 nm and 600 nm is that there is a lattice mismatch between InGaN and GaN. This gives rise to strain during epitaxial growth of InGaN on GaN, and culminates in the creation of a piezoelectric field. This causes band inclination, and pulls apart electrons and holes to different sides of the quantum well, reducing their chances for radiative recombination. Efficient emission is also impaired by defects in the InGaN layer. These imperfections, which are prevalent when the InGaN layer is too thick or the indium content is too high, can capture freely-moving carriers.

Another impediment to producing a high-performance, green-emitting VCSEL is the large effective masses of the carriers in the GaN-based material system. With InGaAs and its related alloys, carrier masses are far lower, leading to a lower transparent carrier density and a lower threshold current.

Due to all the issues detailed above, the threshold current in the GaN VCSEL is relatively high. But it doesn't need to be. Efforts by our team at Xiamen University, China, have shown that green GaN VCSELs can produce a great performance when their active region is made from quantum dots, rather than quantum wells. Note that this idea is not new, and has already led to some very impressive results with GaAs- and InP-based lasers. In the GaN material system, the introduction of quantum dots transforms the device. Formation of these structures undergoes strain relaxation, leading to the elimination of electric fields that peg back radiative recombination. What's more, the dots tightly freeze the carriers, so they are no longer captured by defects; and their energy is quantized into restricted values, so the issues associated with a large effective mass disappear. And last but by no means least, the dots have a far higher differential gain than the wells do. The upshot of all these factors is the promise of low-threshold lasing.

VCSEL designs

VCSELs are formed by surrounding an active region with a pair of mirrors, in the form of distributed Bragg reflectors, which are capable of a reflectivity in excess of 99 percent. The production of GaAs-based VCSELs involves the epitaxial growth of the mirrors, which are based on the pairing of GaAs and AlGaAs. This duo is very good, combining lattice matching with a significant difference in refractive index.

Fabricating GaN-based VCSELs is far more challenging. The only option for making a lattice-matched distributed Bragg reflector with the nitrides is to pair GaN with an AlInN alloy with a specific indium content. This combination is not ideal, however, because the mirrors that result have a narrow stop band, due to the small difference in refractive indices. In addition, it is not easy to control the alloy content in the whole of the distributed Bragg reflector. Note that switching to the combination of AlGaN and GaN only makes matters worse, as it leads to strain accumulation, which causes defects.

In our view, it is better to form mirrors from dielectric materials, such as SiO_2, Ta_2O_5 and TiO_2. These oxides are well used in optical coatings, and they can be deposited by mature methods, such as electron-beam evaporation and magnetron sputtering. In addition, the stop band of reflectivity of a dielectric distributed Bragg reflector is much broader than that of GaN-based variant, making it much easier to achieve optical alignment.

Incorporating the dielectric distributed Bragg reflectors into the VCSEL requires a thinning of the wafer. For the team at Nichia, which grows the epitaxial layers on a native substrate, GaN must be thinned from a few hundred microns to just a few microns. This is a very complicated task, and it is easy to cause damage to the active region.

We employ an alternative approach, growing epilayers on sapphire, before removing this substrate by laser lift-off. To liberate the GaN epistructure, light from a violet laser impinges on the epiwafer through its backside. This radiation is absorbed at the interface with GaN. Thanks to a very high photon density, GaN is heated beyond its melting point, allowing the epitaxial layers to detach from sapphire.

One of the merits of this approach is that the liberated structure is just a few microns thick. As that's close to the thickness of the cavity, there is no need to undertake a complicated thinning process.

A key step in the fabrication of our green VCSELs is the growth of a quantum-dot-based active region. Our approach for this draws on the work of Jianping Liu's group from Suzhou Institute

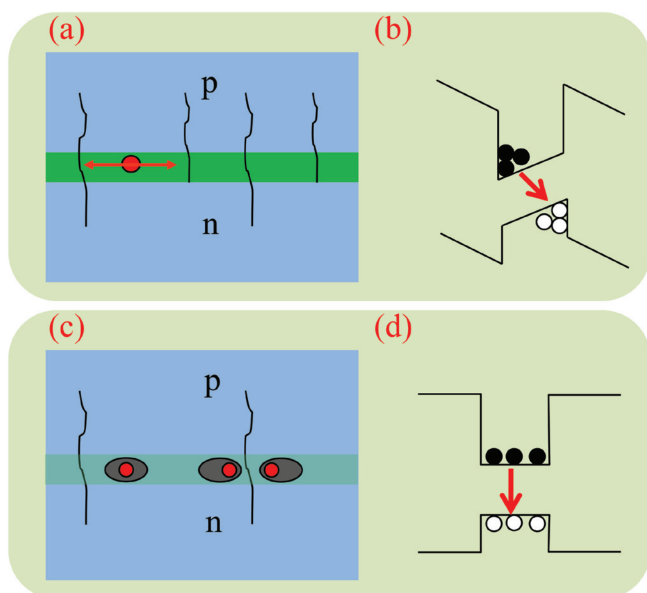

Figure 1. (a) InGaN quantum wells contain defects that can trap freely moving carriers. (b) The radiative efficiency in InGaN quantum wells is impaired by the internal electric field, which pulls apart electrons and holes. (c) Although there are defects in quantum dot structures, radiative recombination can still be high, thanks to strongly localized carriers. (d) InGaN quantum dot devices have a band structure that is free from an internal electric field.

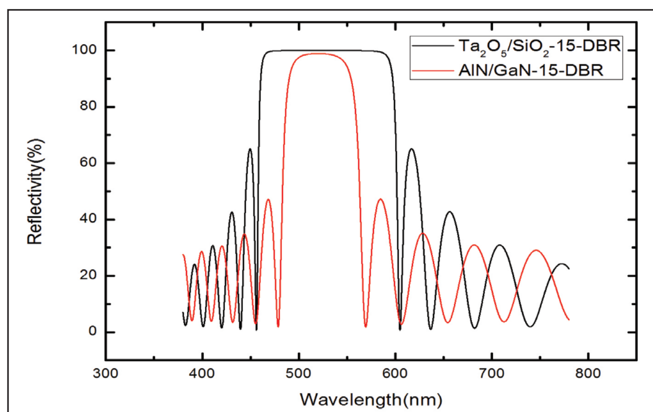

Figure 2. Distributed Bragg reflectors formed from Ta_2O_5/SiO_2 have a better stop bandwidth and a higher maximum reflectivity than those made from AlN/GaN. Note that both reflectors are formed from 15 pairs.

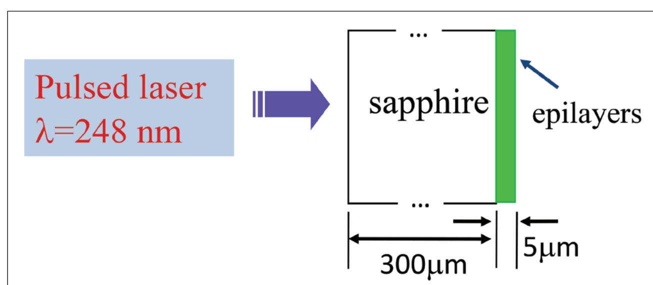

Figure 3. Laser lift-off can separate sapphire from the nitride epilayers of the VCSEL. A key merit of this approach is that it avoids the complicated, damaging, thinning process that is required when using a thick GaN substrate.

of Nano-tech and Nano-bionics, Chinese Academy of Sciences. This team produces its green-emitting quantum dots via MOCVD at relatively high temperatures, which lead to superior material quality. The dots that self-form along step edges on the surfaces of the *c*-plane GaN show no evidence of internal electric fields, indicating that they are free from strain. Due to its absence, internal quantum efficiency is as high as 41 percent. The efficiency is not the only merit of these dots. They also provide far greater carrier confinement than the wells, with an estimated localization energy of 105.9 meV; and the density of the non-radiative recombination centres in the dots is far less than it is for wells emitting at the same wavelength.

Cutting losses

Key device characteristics, such as threshold gain and current, are determined by the optical loss within the cavity. For GaN-based planar cavities, the optical loss is caused by a combination of mirror loss, absorption loss and scattering loss. Mirror loss results from imperfect reflectivity of the distributed Bragg reflector, while absorption loss comes from the indium tin oxide and multi-quantum well regions, and scattering loss is associated with dislocations and surface/interface roughness.

The importance of absorption in the indium-tin oxide layer has been highlighted by Shing-Chung Wang's group from National Chiao Tung University, Taiwan. This team reported the first GaN-based VCSEL lasing under continuous current injection at low temperature, using a VCSEL with a 240 nm-thick indium-tin oxide layer. By trimming this thickness to just 30 nm in a subsequent device, they obtained continuous-wave lasing under current injection at room temperature.

Loss in the multi-quantum well region results from a non-uniform carrier distribution. This state-of-affairs is also seen in LEDs, where the carrier density is not uniform, and hole concentration is highest in the well nearest to the *p*-GaN region. This inhomogeneity contributes to efficiency droop in LEDs driven at high injection currents. In VCSELs, this mechanism for efficiency loss is even more prevalent, due to the need for even higher injection currents.

When it comes to scattering loss, the dislocations in GaN play a dominant role. The density of these imperfections is particularly high in GaN-based VCSELs with dielectric mirrors. In this class of device, which involves the growth of epitaxial layers on sapphire substrate, the large lattice mismatch leads to a high density of dislocations that cause significant scattering loss.

To minimise all these losses, we have investigated the performance of four different devices. This study revealed that a thin indium-tin oxide layer and a coupled quantum well active region are the key ingredients for forming a low loss, high Q-value cavity. Using this combination, we could form devices with a Q-value as high as 3570. These efforts also revealed that a low-loss quantum well design is particularly important in fabricating high-Q value, GaN-based planar cavities, and in reducing the threshold current of GaN-based VCSELs.

Keeping cool

As VCSELs operate under high current densities, inadequate thermal management can lead to overheating. That's highly undesirable, as it leads to degradation of device threshold

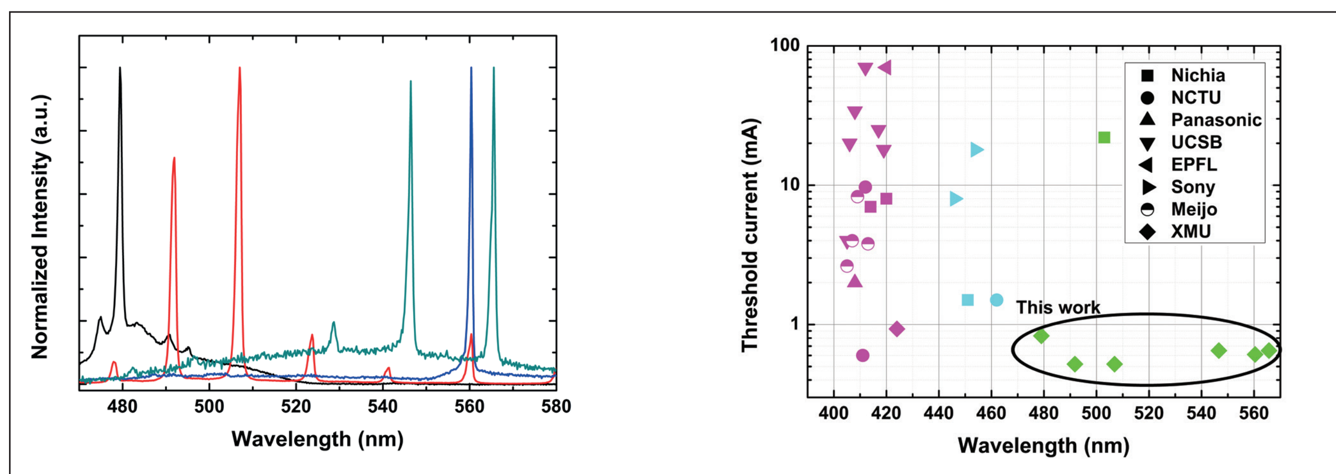

Figure 4. (left) Lasing spectra obtained from different VCSELs made from the same quantum dot wafer. Wavelengths can be controlled by the cavity length, which modulates the profile of the optical field in the cavity and the interaction between photons and electrons. (right) Threshold current as a function of wavelength reported by different groups.

and power, and can ultimately impair device performance and restrict the number of applications that the VCSEL can serve. To ensure that our VCSELs can dissipate the heat they generate efficiently, we transfer them to a silicon substrate via metal bonding. Sample degradation is prevented by our use of a low-temperature, tin-fusion bonding technique.

Studying the emission of quantum wells bonded at various temperatures reveals that if this step is undertaken at 250 °C or less, there is no degradation to the optical properties of the wells. We use tin for bonding, because this melts below 250 °C, while other metals used for bonding have higher melting temperatures.

To further improve the thermal dissipation, we replace silicon with a copper plate. This not only enhances the efficiency of thermal diffusion, and in turn significantly reduces the threshold current – it also simplifies the fabrication process for these VCSELs. Adopting these technologies has enabled us to produce a portfolio of VCSELs with emission wavelengths of 479.6 nm to 565.7 nm. Note that this range, which covers a substantial proportion of the green gap, uses the same quantum dot active region, but different cavity lengths. That's a much neater solution to realising lasers with different wavelengths than that employed for edge emitters, which use differences in material growth to tune the wavelength.

Our next step is to optimize our VCSEL architecture and our fabrication process. Success on both these fronts should lead to practically usable green VCSELs that can serve many applications.

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Markets for GaN VCSELs

Market analysts are tipping sales for the GaN VCSEL to rocket, and to net hundreds of millions of dollars per year. As the bandgap of nitride semiconductors spans the ultra-violet to the infra-red, the emission wavelength of the GaN-based VCSEL could cover the same domain.

GaN VCSELs emitting in the UV and near UV could replace cumbersome, costly gas and solid-state lasers, such as the 325 nm He-Cd laser and the 355 nm excimer laser. They could also be deployed in accurate, chip-sized atomic clocks based on ytterbium ions that require a 375 nm source. At the slightly longer wavelength of 405 nm, GaN VCSELs could replace GaAs-based VCSELs in laser printers, where they would enable a finer resolution. Opportunities for blue VCSELs, emitting at 445 nm, include: laser lighting, which has a higher efficiency and brightness than LED lighting; and visible light communication, where this source promises to offer a very high modulation speed. And bio-sensing applications could be served with a 488 nm VCSEL.

Green VCSELs can serve other markets, including short-distance optical communication using low-cost plastic fibre. They can also be employed alongside GaN-based blue VCSELs and GaAs-based red VCSELs, to create full-colour, high-resolution, portable laser displays and projectors, including those used in lasers TV and mobile-phone projectors.

There are also novel applications for yellow-emitting VCSELs, while two-dimensional arrays of these devices have opportunities in sensing, 2D imaging and 3D printing.

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Targeting LiDAR with stacked GaN lasers

Stacking GaN laser diodes with tunnel junctions could create powerful, UV sources for LiDAR

MAKERS of LiDAR systems operating in automotive and industrial fields are looking for laser diodes that deliver high peak powers.

For long-distance sensing, these sources should ideally deliver peak powers of several watts – but that is not always permissible, due to legislation that sets the maximum possible exposure to human eyes. This limit is far lower in the infra-red than in the UV, so it is shorter-wavelength, high-power sources that are particularly valued for LiDAR.

To address this opportunity, researchers at Hamamatsu Photonics KK, Japan, are trying to develop more powerful sources by stacking GaN-based laser diodes on top of one another. Recent efforts have led them to claim that they are the first to develop a two-laser-diode stack, joined with a tunnel junction.

According to team spokesperson Satoru Okawara, this approach to increasing the output power from the source is preferable to widening the emitter stripe of the laser diode. That's because wider stripes lead to higher operating currents – and in turn, the suppression of efficient short-pulse operation, due to a high reverse voltage that stems from electrical inductance.

Okawara believes that an important aspect of the team's work is the use of lateral hydrogen diffusion: "The lateral diffusion method, which has been reported by Meijo University, is one of the key technologies for realizing for nitride-based devices with tunnel junctions."

Fabrication of the team's lasers began by taking a free-standing GaN substrate, loading it into an MOCVD chamber, and growing an epiwafer with one laser on top of another. Both lasers are identical in structure, and designed to fully confine the optical mode within the guiding layer, preventing optical crosstalk.

Each laser features two $In_{0.06}Ga_{0.94}N$ quantum wells and an electron-blocking layer. Inserted between the lasers is a tunnel junction, formed from the combination of a heavily doped *p*-type layer of InGaN that is 5 nm-thick and a 30 nm-thick layer of *n*-type GaN.

Following the growth of the heterostructure, the engineers partially etch the wafer down to the *n*-type layer of the lower laser.

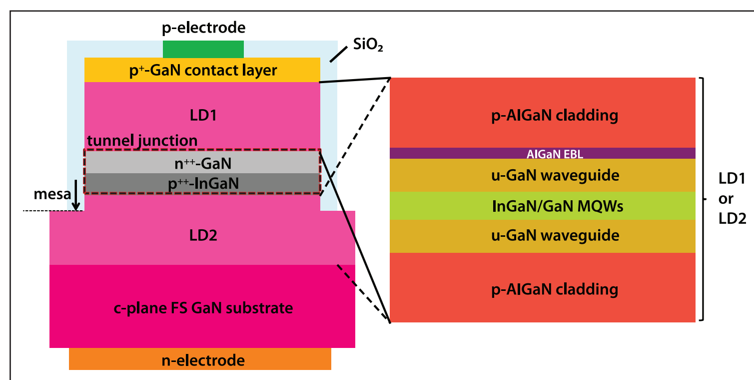
"The partially etching process is not for current confinement, but for fabricating a path for residual hydrogen atoms from high resistant *p*-type layers under the tunnel junction," says Okawara.
Lateral hydrogen diffusion follows, removing hydrogen atoms from the *p*-type layers of the tunnel junction and activating the material.

After adding electrodes to the wafer, and then forming lasers by cleaving, measurements were made on the two-laser chip and a single laser control. Dynamic series resistance for the double-laser structure was far higher – 45 Ω, compared with just 3.5 Ω for the control. Okawara and co-workers attribute this to insufficient removal of hydrogen from the *p*-type layers of the tunnel junction and the lower laser diode. The team are addressing this issue by optimising the annealing conditions for *p*-type activation.

Pulsed measurements showed that the stacked device, which emits at 394 nm, has slope efficiencies for the upper and lower laser of 0.8 W/A and 0.3 W/A. In comparison, the slope efficiency of the single emitter is 1.5 W/A.The poor slope efficiency for the lower laser is blamed on thermal degradation of its active region during the growth of the second device.

"We are considering introducing partial growth by MBE," says Okawara. According to him, the team is also planning to increase the power of these sources, and develop multiple-colour, nitride-based laser diodes.

Tunnel junctions offer a promising route to increasing the output power of GaN-based sources.



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Improving the gate in GaN transistors

Rapid thermal annealing of SiO_2 produces high-quality gates that will help to improve the performance of GaN power devices

TO OVERCOME the large gate leakage currents that impair the performance of GaN HEMTs, researchers are turning to variants with a gate dielectric. Although it's not easy to realise a high-quality, reliable gate, significant progress has just been made by a team from Japan that combines CVD with optimised rapid thermal annealing.

The partnership between researchers at Osaka University, the GaN Advanced Device Open Laboratory, the Advanced Power Electronics Research Centre, and Japan Atomic Energy Agency, is able to form high-quality gates by depositing a SiO_2 layer with a plasma-enhanced CVD process, and annealing at 800 °C.

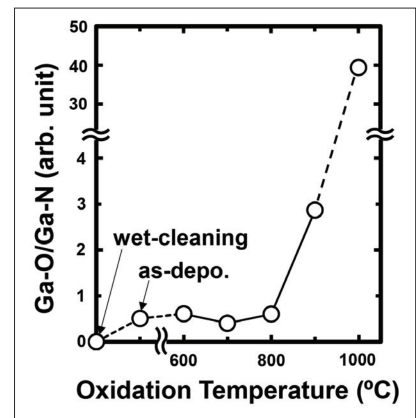
To determine optimal conditions for CVD of SiO_2 and its annealing, the researchers have scrutinised films that are produced under a variety of conditions with synchrotron radiation X-ray photoelectron spectroscopy and electrical measurements that offer an insight into interface properties and reliability.

Spokesperson for the team, Takahiro Yamada from Osaku University, told *Compound Semiconductor* that the most significant aspects of the team's work are the realisation of excellent properties at the interface between the insulator and GaN, and improved reliability. Crucially, both these virtues are possible with practical processes.

The technology that's been developed could aid both lateral and vertical GaN transistors. "With the progress of GaN wafer technology, vertical MOSFETs fabricated on free-standing GaN wafers have gained considerable interest as next-generation, ultra-high voltage GaN MOSFETs that surpass SiC power devices," says Yamada.

He and his co-workers are by no means the first to have fabricated GaN transistors with a gate dielectric. However, most teams use Al_2O_3. Yamada and co-workers shun this oxide, arguing that it leads to electron trapping and ultimately instability in the threshold voltage. The team prefers SiO_2, pointing out that it has a wider bandgap and superior stability against charge trapping.

Efforts at identifying the optimum conditions for forming a gate dielectric began by taking an epiwafer, formed from a free-standing GaN substrate and a 5 μm-thick GaN layer with a doping concentration of 1×10^{18} cm^{-3}, and cleaning its surface with a 5 percent hydrochloric acid solution. Deposition of a 20 nm-thick layer with plasma-enhanced CVD followed, prior to thermal annealing in dry oxygen at a variety of temperatures.



Photoelectron spectroscopy exposes the relative density of Ga-O and Ga-N bonds, and shows that annealing above 900 °C leads to intense interface oxidation.

In these samples, a thin layer of GaO_x forms between SiO_2 and GaN. To examine this, the researchers used synchrotron radiation X-ray photoelectron spectroscopy to detect the presence of Ga-O and Ga-N bonds. Examining a sample that had been thinned to about 2 nm by etching in HF acid – so that the surfrace-sensitive spectroscopy would be successful – Yamada and co-workers found that the initial structure is preserved up to 800 °C, but intense oxidation occurs at higher temperatures.

A key figure of merit for the gate is the hysteresis associated with capacitance-voltage sweeps. Measuring samples annealed at various temperatures revealed that the sweet spot for annealing is around 800 °C.

Confirmation of this came from measurements of interface trap density, using a conductance method at 200 °C. This technique determined an interface trap density below 2×10^{10} cm^{-2} eV^{-1} for samples annealed to 900 °C, and below 10^{10} cm^{-2} eV^{-1} for samples annealed to 800 °C.

Based on these results, the team argues that the fabrication of high-quality GaN transistors with a gate dielectric demands defect termination at the interface between GaN and the insulator, and subsequent thermal annealing.

To ensure a high breakdown voltage for the dielectric, annealing must be rapid. The reserachers found that reducing the time from 30 minutes to 30 s increases the breakdown from around 3 MV to two-to-three times that value.

The team's next goal is to produce vertical GaN MOSFETs. "We are expecting high carrier mobility and threshold voltage stability with the high-quality GaN MOS structures."

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T. Yamada *et al.* Appl. Phys. Express **11** 015701 (2018)

Efficient membrane lasers target silicon photonics

Membrane distributed-reflector lasers are now operating at a low enough cost-per-bit for on-chip optical communication

RESEARCHERS at Tokyo Institute of Technology are claiming to have set a new benchmark for the energy per bit of membrane distributed-feedback and distributed-reflector lasers.

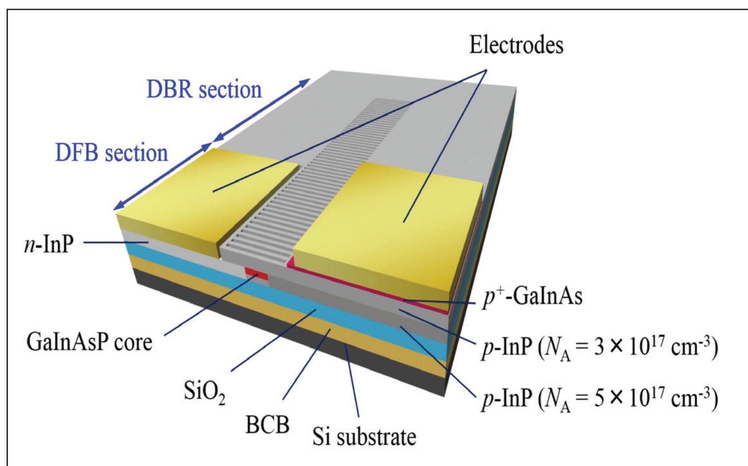
Operating under direct modulation at 20 Gbit/s, the team's InP-based membrane distributed-reflector laser had an energy cost of just 93 fJ/bit.

The team hopes that this form of laser can help to improve the performance of large-scale silicon circuits. The wires in these circuits are limiting data transmission speeds and contributing to escalating power consumption – and a switch to optical data transmission, supported by efficient membrane lasers, promises to address both issues.

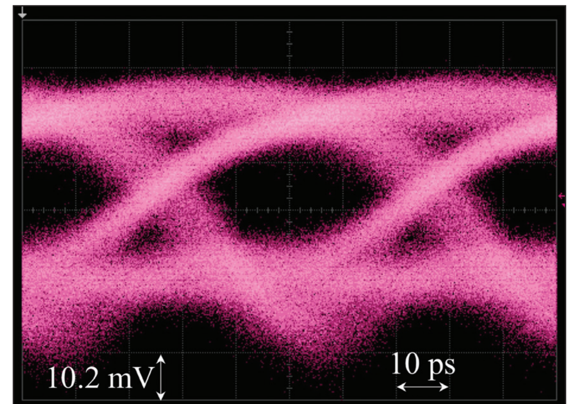
If lasers are to be used in integrated circuits, their power consumption needs to be ultra-low, equating to no more than 100 fJ/bit. The laser from Tokyo is just inside that limit.

Several other forms of laser are also candidates for on-chip optical communication. "Microdisk and photonic crystal lasers can achieve low threshold current operation by strong optical confinement," says team spokesman Shigehisa Arai. "However, due to such strong optical confinement, the output power as well as the efficiency were quite low. In contrast, our distributed reflector lasers have low threshold current operation and high output power efficiency simultaneously."

That's not to say that photonic crystal lasers can't produce eye-catching results. A device by a team from NTT had an energy cost of just 4.4fJ/bit.



The membrane distributed feedback laser developed by Tokyo Institute of Technology can operate at 20 Gbit/s with an energy cost of 93 fJ/bit.



The InP-based membrane distributed-reflector laser is capable of a clear eye-diagram when driven with a non-return-to-zero modulation scheme with a 2^{11}-1 word-length pseudorandom bit sequence.

"However, because the output power was as low as several microwatts, they used an avalanche photodiode, which requires a bias voltage of 10-30 V – hence it consumes a lot of power at the receiver side." says Arai.

According to him, their team's laser is powerful enough to allow the use of a conventional *p-i-n* photodiode, which requires a bias voltage of around 1 V. "Therefore, total system energy should be lower for our case."

Arai's group has been developing InP-based membrane distributed-reflector lasers for several years. The recent progress, in terms of the energy cost per bit, has resulted primarily from a reduction in waveguide loss, thanks to optimization of the doping profile. This move has also led to an increase in series resistance between the *p*-side electrode and the active region, so, to address that issue, the engineers reduced the distance between the edge of the *p*-side electrode and the active section from 3 μm to 1.6 μm.

One plan for the future is to reduce the energy cost to just several tens of fJ/bit. In parallel, the group will work on the development of an "amplifier-less" photo detector with a similar membrane technology. "Once we develop both, we will integrate all these devices on a real CMOS circuit," says Arai

Reference

T. Tomiyasu *et al.* Appl. Phys. Express **11** 012704 (2018)

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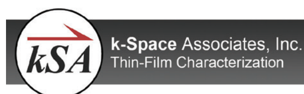

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