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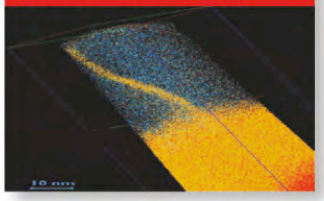
Building better GaN PAs for space

Hollow cavities aid light extraction

Superior switching with tunnel FETs



Slashing the cost of GaN substrates

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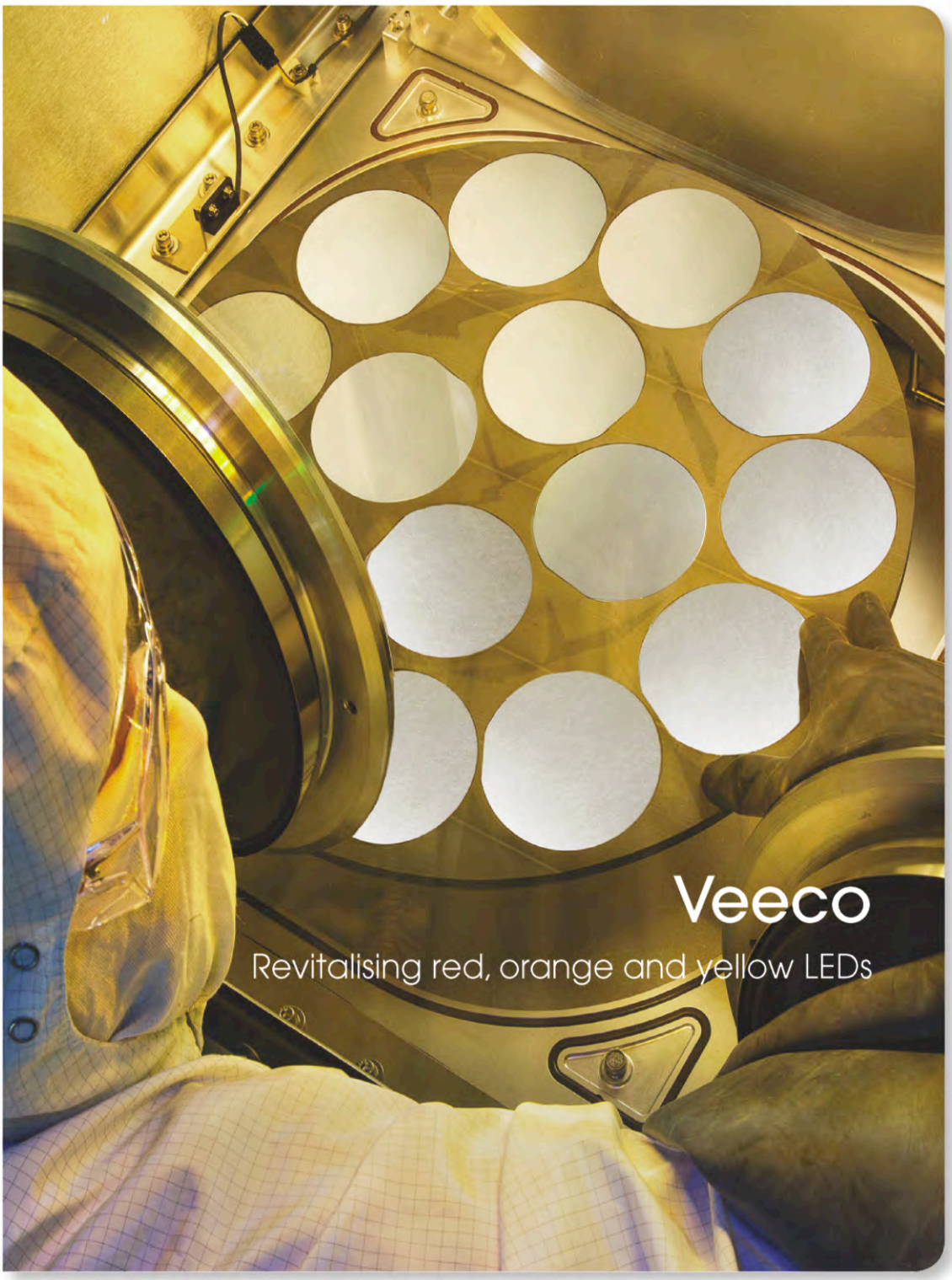

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editorial view

by Dr Richard Stevenson, Editor

Getting the most out of gallium oxide

IF YOU WERE given the job of selecting suitable power electronics components, you would need to know priorities. If affordability mattered most, you would restrict your selection to a silicon device – but performance would be compromised. And if great efficiency topped the agenda, SiC and GaN devices would be preferred, despite their additional cost.

The ideal, of course, is a device that excels on all fronts. And although that's not possible, a chip developed by Japanese start-up Flosfia promises to get closer to this goal than anything that has come before it.

Flosfia is making its devices from gallium oxide. This material has a bandgap of around 5 eV, which makes the wide bandgap devices of SiC and GaN look more like middleweights than heavyweights. Armed with this attribute, gallium oxide diodes and transistors could have an on-resistance that is one-tenth of that of SiC, and a footprint that is around one-seventh.

While all of this is very encouraging, success requires gallium oxide devices to be cost-competitive with silicon, while providing good thermal management. That's not easy – but it is possible, thanks to Flosfia's novel growth technology and device architecture.

Engineers at Flosfia deposit the layers of the gallium oxide device with a low-cost atmospheric process. Directing ultrasound at a gallium halide source, in the form of either a water-based or alcohol-based solution, yields a mist that is swept into a chamber on a carrier gas. Here, oxygen reacts with the mist to form a film on a heated sapphire substrate.

Choosing a sapphire substrate is unusual – but very wise. The more common option is gallium oxide, but sapphire offers low-cost, widespread availability, and a small difference in lattice mismatch that causes the device to separate from the substrate. The latter is hugely beneficial, aiding thermal management. The Achilles heel of gallium oxide is its low thermal conductivity, and bonding it to a carrier with high thermal conductivity is a great way to extract heat out of the device.

Flosfia is making great strides with its devices. It has already produced diodes that are outperforming what is theoretically possible with SiC, and transistors with record-breaking performance should follow.

To find out more about this company, see its feature on p.28. And if you want to follow progress over the coming months, come along to CS International 2017, where Flosfia will deliver the keynote talk in the session Perfecting Power Electronics.

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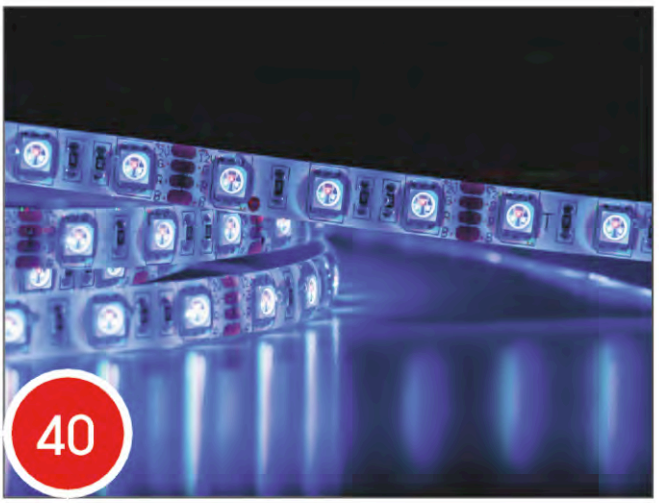

EU project targets multi-terabit chip-to-chip comms

THE EVER-GROWING demands of mega datacentres and high-performance computers for increased bandwidth at a fraction of real estate and power consumption are pushing current pluggable optics interconnection solutions to their limits.

ICT-STREAMS, a new project in the European Union Horizon 2020 program, is now working on developing a set of innovative transceiver and routing technologies to increase server-board density by over 400 percent, throughput by 1600 percent, and to reduce energy consumption tenfold.

The research efforts are aligned with next generation embedded optical transceivers, placed on-board and in close proximity to the electronic modules, as a way to drastically reduce the required physical space and power budget. The aim is to enable multi-terabit on-board chip-to-chip communications. To this end, the three year research project will exploit silicon photonics technology in order develop ultra-powerful, compact, Dense Wavelength Division Multipling (DWDM), high channel count and dense embedded optical engines with the ability to exhibit aggregate throughputs beyond 1Tb/s.

ICT-STREAMS will also develop a thermal drift compensation system employing a non-invasive wavelength monitoring and control technology to guarantee real-life applicability of the proposed multi-channel silicon photonics technology. On the board level, a single mode polymer-based electro-optical PCB will be developed to serve as the host platform that will efficiently route both optical and high frequency electrical data across the board.

As a way to relax manufacturing time and cost requirements associated with complex optical assembly processes, optical engines will rely on novel III/V-on-silicon in-plane lasers for optical sourcing while adiabatic coupling will be employed for I/O interfacing with the electro-optical PCB host platform.

Finally, ICT-STREAMS will assemble the new optical engines on the polymer EOPCB together with a 16x16 AWGR-based routing component to leverage WDM technology from just a parallel transmission tool to a massive any-to-any, collision-less and low latency routing platform with 25.6Tb/s aggregate throughput capability. Photonic crystal based III/V-on-silicon nano-amplifiers will be introduced as a new amplification

paradigm to enable optical power balanced links with advanced features and smart routing functionalities. The project is scheduled to run for three years bringing together three leading industrial partners, one small-medium enterprise and five academic and research institutes in the optical interconnects value chain.

Project partners are Aristotle University of Thessaloniki (Greece) that is also coordinating the project, Centre National de la Recherche Nationale (CNRS) - Laboratoire de photonique et de nanostructures (LPN) (France), IBM Research Zurich GmbH (Switzerland), Interuniversitair Micro-Elektronica Centrum - IMEC (Belgium), Politecnico di Milano (Italy), STMicroelectronics (Italy), iMinds (Belgium), Vario Optics AG (Switzerland), FCI Connectivity (Germany).

Cree delivers 25 percent higher lumens-per-watt

CREE has made improvements to its XT-E LED family to include a new high efficiency option that the company says delivers a 25 percent increase in efficacy compared to the previous XT-E LED and a guaranteed minimum efficacy of 164 LPW at 85°C and 350mA.

Using elements of its SC5 Technology Platform, the upgrade means that 130 lm/W or higher is achievable at the system level under real operating conditions, according to Cree. This will enable existing customers to quickly upgrade system performance of applications, such as outdoor and industrial lighting, while still achieving the lowest total cost.

"We are committed to building the most energy-efficient industrial lighting systems and the newly improved High Efficacy XT-E LED enables us to do that without any additional investment or requalification," said Colin Piepgras, vice president of engineering at Digital Lumens. "With the new XT-E LED, we are able to leverage existing optical, mechanical and electrical design elements to quickly improve our portfolio of intelligent lighting solutions."

The enhanced XT-E LED improves the brightness, voltage characteristics and optical performance in the same, proven 3.45 mm x 3.45 mm XT package. Demonstrating the excellent long-term reliability of Cree's high-power ceramic LEDs, the XT-E LEDs now have more than 10,000 hours of LM-80 data available, delivering reported L90 lifetimes of greater than 60,000 hours, at 105°C, 1A.

These reliability figures make the LED suitable for applications like outdoor and high bay lighting were long lifetimes at high ambient temperatures matter. For example, XT-E's improved efficacy and reliability make it well-suited for the recently updated DesignLights Consortium DLC 4.0 requirements.

"Our customers rely on Cree for innovations that allow them to upgrade their existing products to both gain a competitive edge and meet increasing industry requirements," said Dave Emerson, vice president and general manager for Cree LEDs. "Cree's improved XT-E LED provides an immediate solution that eliminates the time and cost of redesign around other unproven alternatives."

US DoE invests over $10 million in lighting R&D

BUILDING on the new commitments to the Global Lighting Challenge announced during the Clean Energy Ministerial, the US Energy Department is announcing funding for nine projects that will support solid-state lighting (SSL) core technology research, product development, and manufacturing research and development.

The projects will help accelerate the development of high-quality LED and organic light-emitting diode (OLED) lighting products that can significantly reduce energy costs for American families and businesses by using less electricity than products currently in use and ensure that the US remains globally competitive.

"Solid-state lighting research and development has contributed to more than $2.8 billion in US energy cost savings over the past 15 years, and further improvements in the technology will increase those savings even more in the years to come," said Secretary of Energy Ernest Moniz.

"By 2030, solid-state lighting could reduce national lighting electricity use by nearly half-which would equate to the total energy consumed by 24 million American homes today and could save American families and businesses $26 billion annually."

Department-funded research and development will foster technology breakthroughs to unlock new levels of solid state lighting performance and energy savings. For example, DOE targets aim to increase the efficiency of today's LEDs by an additional 66 percent. LED lighting also offers new potential for advanced lighting control, including colour tuning and intelligent, adaptive lighting.

In total, the nine selected projects will receive more than $10.5 million and will make a cost-share contribution for a total public-private investment of over $13.5 million, as they help to further reduce the cost and improve the quality of SSL products:

- **Cree (Durham, North Carolina) -** Developing a high-efficacy LED lighting fixture that has good colour rendering as well as advanced features such as the ability to tune the colour of the light;

- **Columbia University (New York, New York) -** Developing improved quantum dots to increase the efficiency and lower the cost of LEDs;
- **GE Global Research (Niskayuna, New York) -** Developing an efficient LED fixture that features interchangeable modules and allows for simplified manufacturing and customised performance specifications;
- **Iowa State University (Ames, Iowa) -** Demonstrating a method to significantly increase the light output of white OLEDs by changing their internal features;
- **Lumenari (Lexington, Kentucky) -** Developing a narrow-bandwidth red phosphor to improve the efficacy of phosphor-converted LEDs;
- **Lumileds (San Jose, California) -** Improving the design of an LED to make it more efficient by using a patterned sapphire substrate flip-chip architecture;
- **North Carolina State University (Raleigh, North Carolina) -** Developing a way to get more light out of OLEDs using low-cost corrugated substrates;
- **Pennsylvania State University (State College, Pennsylvania) -** Developing a way to better understand and predict the occurrence of short circuits in OLED lighting panels in order to reduce failure rates; and University of Michigan (Ann Arbor, Michigan) - Developing three innovative methods to harness the light within OLEDs.

POET completes BB Photonics acquisition

POET TECHNOLOGIES has announced the completion of its acquisition of all of the shares of BB Photonics, a private designer of integrated photonic devices for the datacoms market. POET completes the transaction owning 100 percent of BB Photonics and its assets, including intellectual property and technologies.

BB Photonics develops photonic integrated components for the datacentre market using embedded dielectric technology that is intended to enable on-chip a thermal wavelength control and lower the total solution cost of datacentre photonic integrated circuits (PICs).

This acquisition is designed to provide POET with additional differentiated intellectual property and know-how for product development, enable POET to better service it's first identified commercialisation market – the end-to-end data communications market – and augment its sensing roadmap. "The addition of BB Photonics significantly enhances our integrated photonic solution set and advances our commercialisation initiative," said Suresh Venkatesan, POET's CEO. "By internal development and acquisition, we are accelerating our drive from technology leadership to market entry in differentiated photonics."

The POET platform and process technology continue to be the focal point of the company's commercialisation strategy. The POET team continues to make progress toward its previously announced goal of demonstrating an integrated product prototype by the end of 2016 using the POET platform. POET says that its recent acquisitions are meant to serve as a logical continuum of the roadmap by enabling immediate market entrance into its first identified commercialisation market – datacoms.

Kyma and Quora announce GaN partnership

KYMA TECHNOLOGIES and Quora Technology have announced a strategic partnership in the development and commercialisation of GaN substrate materials.

Kyma is a developer of wide bandgap semiconductor (WBGS) materials solutions, including GaN, AlN, Ga_2O_3, and diamond. Kyma's GaN materials products include free-standing GaN substrates and GaN templates.

Quora Technology is a new privately held fabless technology startup, located in Silicon Valley, California, focusing on energy efficient and high performance wide bandgap semiconductor materials and device solutions.

Quora Technology is currently commercialising its QST substrate technology which is fully diameter scalable (6-inch, 8-inch,12-inch and beyond) and engineered to alleviate stress from epi layers, allowing deposition of tens of microns of high quality and low dislocation density GaN on 6-inch or larger diameters.

According to Quora, the QST substrate technology is poised for rapid adoption in WBGS industry with the validated performance results in LED, power and RF applications by the major GaN device manufacturers.

Kyma and Quora have teamed to demonstrate that Kyma's high growth rate GaN processes can be used to realise a low defect GaN on QST template, which uses the QST properties and provides a very high quality epi-ready surface for GaN epitaxy growth and device fabrication.

Kyma confirmed that it could produce uncracked, low defect density ($<10^8 cm^{-2}$) 6-inch diameter GaN on QST templates that have up to 40 percent narrower X-ray diffraction line widths, smoother surface morphology, and much lower bow than for similar structures grown on sapphire.

Low bow is important, as well as other wafer shape issues, for achieving high yielding and advanced device fabrication. Wafer shape control, including GaN cracking or entire wafer breakage, is a major problem with traditional approaches on large diameter wafers and as such is one of the major obstacles in front of WBGS industry which limits achievable economies of scale.

The companies have already succeeded in winning support on two separate US federal research projects, the first to develop manufacturing processes for making cost-effective large diameter high growth rate GaN on QST templates up to 8-inch diameter, and the second to take that approach to the next level to create 4-inch and 6-inch diameter free-standing GaN substrates.

In the first project, Kyma is developing an 8-inch diameter GaN growth tool that is designed to produce uniform low defect density GaN on QST wafers in GaN thicknesses up to 100 μm at a fast-cycle time which will support a low tool cost of ownership.

Kyma is already teamed with a leading OEM tool manufacturer to support rapid market penetration of the technology once the team further advances the growth process and proves its ability to support high performance device manufacturing. Kyma's device partners include leading US universities and multiple large device manufacturers.

In the second project, Kyma will create low defect density GaN boules and fabricate 4-inch and 6-inch substrates therefrom. The substrates will be made available to leading US device developers to prove out their ability to support high performance 1200 V vertical power electronic device operation.

Quora Technology president and CEO Cem Basceri commented: "We are very excited for Kyma to integrate its rapid GaN growth process on our high performance substrate technology, QST, for delivering low defect density and large diameter GaN wafers to the device manufacturers. This special class of material will hopefully improve the existing device processes, designs, and performances, and also unlock new applications."

US team sheds light on semiconductor processing

UNIVERSITY OF UTAH materials science and engineering associate professor Mike Scarpulla and senior scientist Kirstin Alberi of the National Renewable Energy Laboratory in Golden, Colorado, have developed a theory that adding light during semiconductor manufacturing can reduce defects and potentially make more efficient solar cells or brighter LEDs.

Scarpulla and Alberi reported their findings in a paper titled 'Suppression of Compensating Native Defect Formation During Semiconductor Processing Via Excess Carriers' published June 16 in the journal, *Scientific Reports*. The research was funded by grants from the US Department of Energy Office of Basic Energy Sciences.

The theory developed by Scarpulla and Alberi is most interesting for compound semiconductors such as GaAs, CdTe, and GaN which are more susceptible to defects in the material at an atomic scale.

The team discovered that if you add light while firing the material in a furnace at high temperatures, the light generates extra electrons that can change the composition of the material.

For nearly a century, researchers have usually assumed that the numbers of these defects in semiconductors were uniquely defined by the temperature and pressure during processing. "We worked out a complete theory that couples light into that problem," Scarpulla says. "We ran simulations of what happens," Scarpulla says. "If you put a piece of a semiconductor in a furnace in the dark, you would get one set of properties from it. But when you shine light on it in the furnace, it turns out you suppress these more problematic defects. We think it may allow us to get around some tricky problems with certain materials that have prevented their use for decades. The exciting work is in the future though – actually testing these predictions to make better devices."

The team is working to apply their theory to as many semiconductors as possible and testing the real world results. For example, the team believes this could improve the efficiency of solar panels that use thin films of CdTe and even those made from silicon.

Samsung introduces chip scale LEDs for cars

SAMSUNG ELECTRONICS has introduced Fx-CSP, a range of LED packages which feature chip-scale packaging and flexible circuit board technology, for use in automotive lighting applications.

The new LEDs were recently selected for a compact car headlamp project from one of the major global automotive manufacturers.

Samsung's new Fx-CSP provides a combination of chip-scale packaging and flexible circuit board technology, which together enable more compact chip sizing and a higher degree of reliability, according to the company.

The use of a flexible circuit board also enables more heat to dissipate, which leads to lower resistance and brings about a greater degree of lumen-per-watt efficiency than using a ceramic board.

In addition, the new Samsung automotive LED line-up allows car designers to use a variety of chip arrangements such as a single chip, a 1 by 4, or a 2 by 6 multi-chip arrangement to suit different lighting configurations. The Fx-CSP line-up can be widely used in automotive lighting

applications that include position lamps and daytime running lamps as well as headlamps that require higher luminous flux and reliability than other automotive lamps.

The Fx-CSP line-up consists of single packages, Fx1M and Fx1L, with 1-3 W each, as well as packages with a 14 W high voltage array, Fx4 and a 40 W high voltage array, Fx2x6. The variation in wattage levels allows Samsung LED lighting packages to work well with a wide range of exterior automotive lighting.

Samsung plans to introduce more CSP technology-based LED components such as the new Fx-CSP line-up for automotive lighting, later this year.

RF GaN revenue increases sharply

The growing adoption of GaN technology in RF applications, coupled with the widespread deployment of LTE base stations in China drove an increase in RF GaN revenue of nearly 50 percent in 2015.

The Strategy Analytics Advanced Semiconductor Applications (ASA) service report, *RF GaN Market Update: 2015 – 2020* indicates that the growth in the base station segment pushed the commercial portion of the RF GaN revenue to more than 60 percent of the total in 2015.

The report concludes that continuing growth in base station and defence applications will propel RF GaN revenue to nearly $690 million in 2020. Eric Higham, service director, advanced semiconductor applications service commented:

"The performance advantages of GaN fit nicely with the requirements of new LTE base station power amplifiers". He added, "Despite an anticipated decline in the base station power market, we anticipate that GaN revenue will increase as more equipment manufacturers convert to the technology".

UTAC, Sarda and AT&S collaborate on datacentre voltage regulators

SARDA TECHNOLOGIES, a US power management component supplier and UTAC Holdings, an Asian semiconductor assembly and test services provider, have announced that Sarda will implement its Heterogeneous Integrated Power Stage (HIPS) in UTAC's 3D system-in-package (3D SiP) based on ECP technology from Austrian high-end PCB firm AT&S. The aim is to improve datacentre energy efficiency.

Designed to address the rapidly escalating power consumption in datacentres, Sarda's HIPS replaces silicon switches with GaAs in voltage regulators that increase switching frequency by ten times, improve transient response by 5 times and reduce size by 80 percent. With these fast, small voltage regulators, it enables granular power delivery to reduce data center power consumption by 30 percent.
The collaboration was announced at the International Symposium on 3D Power Electronics, Integration and Manufacturing Symposium (www.3D-PEIM.org) in Raleigh, North Carolina, USA.

"UTAC's 3D SiP enables Sarda to integrate GaAs switches, silicon driver and passive components in a compact, low-profile package that minimis es parasitics for efficient, high speed operation," said Bob Conner, CEO and co-founder of Sarda. "UTAC's collaboration with AT&S also provides a full turnkey supply chain assembly and test flow with much needed alignment of roadmaps as well as design rules for 3D SiP solutions with embedded chip in substrate technology."

"System manufacturers are moving from use of discrete components to highly integrated power management solutions to improve power density and energy efficiency. UTAC is very excited in working closely with Sarda and AT&S to demonstrate the benefits of using 3D SiP to reduce footprint and improve electrical and thermal performance," said Lee Smith, VP of UTAC's advanced package product line.

"Our collaboration with UTAC maximises the benefits of utilising AT&S' ECP technology for the Sarda HIPS Solution", stated Michael Lang, CEO of advanced packaging at AT&S. "The major ECP advantages compared to standard IC packaging and PCB assembly include a significant form factor reduction, higher reliability, improved thermal management and a fast and easy system integration with high efficiency."

Servers, routers and communications systems require new power management technology to keep up with the growth in data consumption and mobile connectivity. But power delivery and heat removal issues constrain system performance. Moreover, each system board uses dozens of voltage regulators which consume precious board space.

Small, fast voltage regulators enable granular power, which reduces system power consumption through dynamic power management of each load. Miniaturising the voltage regulators also frees up board space for more processors and memory to increase system performance. Increasing system performance-per-watt decreases the system cost-per-workload.

Chinese University orders Veeco R&D MBE system

VEECO has received the first order from a Chinese customer for its GENxplor R&D MBE System. Nanjing University is scheduled to receive the system in the second quarter of 2016. The GENxplor system is the number one selling MBE system worldwide since its introduction in August 2013.

Led by Hong Lu, Nanjing University purchased the system as an addition to its Materials Science and Engineering research program. The system will enable the epitaxial growth of high quality materials of III-V semiconductors for applications including optoelectronic devices and thermoelectric energy conversion.

"With the development of the GENxplor, Veeco has become the recognized leader in innovative MBE R&D technology," said Lu. "The open-architecture design and superior technology of the GENxplor system is a welcome addition to the research facility of National Laboratory of Solid State Microstructures and College of Engineering and Applied Sciences at Nanjing University. We are proud to receive the first system in China."

The GENxplor system deposits epitaxial layers on substrates up to 3inch in diameter and is used for a wide variety of applications such as developing high-speed transistors, fibre lasers for material processing, and wireless technology. Its

single frame design combines all vacuum hardware with on-board electronics to make it up to forty percent smaller than other MBE systems, saving valuable lab space, according to Veeco.

"Since its introduction, the GENxplor has enabled essential semiconductor research at top universities and institutions around the world," said Gerry Blumenstock, VP of Veeco's MBE Operations. "The endorsement from Nanjing University and Lu firmly reinforces GENxplor as the leading R&D MBE system in the industry. After launching the system at the 2013 China MBE Conference, we are excited that Nanjing University, a leading materials science and condensed matter physics research university, is the first customer to install a GENxplor in China."

ADVA joins EU lasers-on-silicon consortium

ADVA OPTICAL NETWORKING has announced that it is playing a key role in the EU-funded Directly Modulated Lasers on Silicon (DIMENSION) project. DIMENSION, which brings together a consortium of research and industry partners from four European countries, aims to create a platform for single-chip electro-optical integration.

The breakthrough technology it produces will involve lasers built with active III-V materials embedded into silicon photonics chips. This will generate the versatile, cost-efficient components needed to optimise datacentre interconnect (DCI) transport and create the next generation of datacentre.

The four-year project (funded by the European Union's Horizon 2020 research and innovation program) aims to take electro-optical integration to a new level by producing silicon chips built with active laser components. The consortium of partners also forms a complete value chain for the production of the new technology, from research through to innovative package design and assembly. The project will run until the end of January 2020.

"DIMENSION unites specialists from different fields and enables us to address the complete value chain of directly modulated lasers, from materials research to application," said Bert Offrein, manager, photonics, IBM Research – Zurich. "What we're bringing to the table is a lot of experience with transformational datacentre innovation. We're focusing on incorporating highly efficient III-V materials into silicon chips. Our role is to design and produce the integrated active optical components. "This technology will bring the optics to where the data is generated and that leads to improvements in every part of the datacentre. By enhancing interconnections at different reaches, from centimetres up to kilometres, we'll be able to reduce size, cost and power on links between boards, computers and facilities."

The DIMENSION project is coordinated by Dresden University of Technology and involves partners from Germany, Switzerland, Greece and the UK. The two research centres included are Innovations for High Performance Microelectronics and Athens Information Technology. The large industry partners are ADVA Optical Networking, Optocap and IBM Research - Zurich. "Improving efficiency in the DCI couldn't be more vital given the increasing demand for cloud computing and the growing scale of the internet of things," commented Michael Eiselt, director, advanced technology, ADVA Optical Networking.

"Much of our recent innovation has centred on enhancing the DCI, such as our FSP 3000 CloudConnect solution. By integrating the three distinct technologies of silicon photonics, electronics and active photonics, we're giving data centres what they need to meet tomorrow's demands. It's great to be working closely with other European companies and institutions to make this vital breakthrough a reality. It also provides fantastic opportunities for university students who get to be at the forefront of innovation and help make a significant impact on the industry."

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GaAs: Safe for now

Technavio analyst, Sunil Singh, provides insight to the future of GaAs in the complex communications landscape. Rebecca Pool reports.

As rising sales of smartphones worldwide fuel demand for GaAs power amplifiers, device vendors are jostling for more and more market share. GaAs semiconductors are already the incumbent and state-of-the-art technology in cellular handsets that use at least one GaAs-based power amplifier, and industry can expect more of the same in the coming years.

In his recent report *Global GaAs devices market 2016 to 2020* Technavio analyst, Sunil Kumar Singh, points out the leading players and highlights those that he believes have an edge.

"All vendors in this market are focusing on cellular communications due to the deployment of 3G, 4G and LTE networks and the trend towards 5G," he says.

"Global wafer capacity for GaAs devices is increasing with every company operating at, at least, an 85 percent production rate," he adds. "So competition is intense but Skyworks and Qorvo are the key vendors and cover a substantial amount of market share."

According to Singh, right now Skyworks can produce around ten million chips a day using proprietary processes. And while its key market driver is data traffic, the company also has a huge product portfolio from amplifiers and attenuators to power management devices and voltage regulators covering defence, aerospace, automotive markets and more.

Meanwhile, the merger of RFMD and TriQuint Semiconductor sees Qorvo also delivering a vast product portfolio of GaAs-based devices serving mobile device, network infrastructure as well as aerospace and defence markets.

But, as Singh highlights, Qorvo's recent acquisition of GreenPeak Technologies, a developer of CMOS wireless controller chips for the Internet of Things markets, signals more change is afoot.

With GreenPark in tow, Qorvo could diversify into CMOS technology, joining the ranks of Skyworks, Avago Technologies – now a Broadcom company – and other competitors. Indeed, Skyworks, claiming proficiency in both technologies, promotes GaAs for its linearity and its power efficiency and CMOS for its easy integration, low cost and low power consumption.

And, with more industry players owning competing technologies, convergence becomes a real possibility.

"I'm not saying this will happen but could we see GreenPeak CMOS chips equipped with broadband GaAs power amplifiers?" asks Singh.

"In this case, GreenPeak is a fabless company so Qorvo may have to first develop a foundry for CMOS chips which could take time," he adds. "But in the near future, [the company] could be looking at technology convergence here."

Convergence aside, according to Singh, Avago Technologies, recently merged with Broadcom, is the other key player in the GaAs device market space. And at the same time, Advanced Wireless Semiconductor, Anadigics, MACOM and Analog Devices, having acquired Hittite Microwave, all provide stiff competition.

"Analog Devices has such a strong financial background I can now see it becoming one of the top competitors for Skyworks and Qorvo," he highlights. "At the same time, MACOM sells directly to companies without third party sales channels and if it can deliver the volumes in accordance with current market demand I definitely see it taking more market share in the future."

CMOS threat?

Without a doubt, cheaper silicon CMOS power amplifiers provide the prime

Smartphones are set to drive future demand for GaAs power amplifiers.

threat for GaAs devices in this market. And thanks to developments such as envelope tracking, the performance gap between the two technologies has narrowed. Still, Singh is adamant GaAs is safe for now.

"If CMOS was to rapidly increase in RF front-end modules, the vendors operating in this space would struggle with [the existing] manufacturing capacity to mass produce these CMOS devices," he says. "But when it comes to GaAs devices, vendors such as Qorvo, WIN Semiconductor and Anadigics do have the capacity [to ramp up production], which is a huge advantage."

At the same time, other power amplifier technologies are gathering market momentum. For example, Skyworks, has revealed plans to use SiGe power amplifier technologies in RF front-end modules to boost power and efficiency in future wireless communications devices.

Still, Singh believes GaAs devices will remain ahead of up and coming power amplifier technologies based on GaN-on-SiC as well as SiGe for now.

"GaAs can be directly substituted with these emerging technologies but this isn't happening in the near future, at least until 2020," he says. "Device manufacturers will be considering, for example, form factors, load requirements, matching and filtering... and GaAs devices are ahead of the game here, compared to any other technology."

CREE: GUIDING LIGHT

Without a doubt, Cree has raised performance standards for high-power LEDs across lighting markets worldwide. Can the US-based manufacturer continue to deliver throughout tough times? Rebecca Pool investigates.

EARLIER THIS YEAR, Cree unveiled a single high-power R&D LED that delivered nearly 1600 lumens at 134 lumens per watt.

At the time, the US-based lighting industry leader claimed a LED lumens-per-watt record compared to production LEDs with a similar colour quality. And crucially, that colour quality was a warm white, on par with the incandescent light bulb.

"If you look at the big lumens-per-watt numbers that are out there, these are for cooler light LEDs that emit towards the more blue end of the spectrum," points out Paul Scheidt, leader of product marketing, LED components, at Cree.

"These LEDs make great headlines, but light quality is sacrificed for efficiency and this just isn't the kind of light people will use in life," he adds. "So now we think there is a lot more room [for development] with warmer colour temperatures and practical lighting."

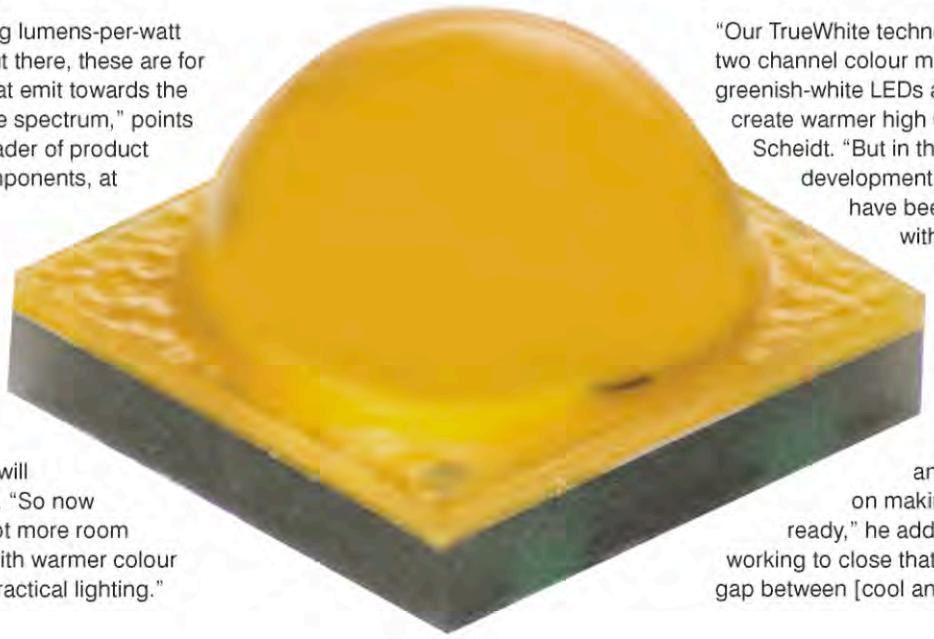
According to Scheidt, researchers at Cree are currently focusing on improving the spectral content and efficacy of warmer colour temperature LEDs, while, as always, looking to increase the lumens per watt under real-world operating conditions.

"For LEDs with a warm correlated colour temperature and a high colour rendering index, we've boosted efficacy by 25 percent [in the R&D LEDs]," he says. "By the laws of physics losses exist that we can't get rid of, but there are other losses that we still think we can overcome."

To date, the company's 'TrueWhite LEDs' have been testament to this, boasting a high colour quality and high efficacy with a high lumen output. But Cree has taken a different approach with the latest R&D LEDs.

"Our TrueWhite technology has used two channel colour mixing... we take greenish-white LEDs and red LEDs to create warmer high CRI lighting," says Scheidt. "But in the research and development announcement we have been experimenting with a single LED so we don't require, for example, two separate control schemes."

"We've achieved results in the lab and are now working on making this production ready," he adds. "We're really working to close that [lumens-per-watt] gap between [cool and warm] LEDs.



LED backbone

At the heart of many of Cree's LEDs lies the so-called SC5 Technology platform. Launched in late 2014, the platform is based on the company's SiC substrates alongside intellectual property in epitaxy, chip architecture and light conversion systems.

The platform has spawned myriad LEDs, including the company's first Extreme High Power (XHP) LEDs, claimed to reduce systems costs by up to 40 percent while providing the necessary lumens per watt and lifetimes at high operating temperatures.

More XHP LEDs have since followed, including Cree's single-die device, the XHP 35, which according to Scheidt, is based on a 'breakthrough in chip design' that operates at 12 V on a single die.

The product manager remains tight lipped on the detail surrounding the company's platform and LEDs, but highlights: "We delivered the first XHPs in late 2014 and from the beginning it's been about driving these LEDs to higher temperatures than seen before."

"At the time, we were using the latest of everything we had with the SC5 platform providing improvements in packaging construction, from the materials used to how the chip was packaged," he says.

"And for the actual die, this included the latest phosphors and encapsulants."

LED breakthroughs aside, and following its single die approach, the company is clearly focusing on minimising component count within its LED systems. Many in the industry point to the high cost of LEDs as hampering the widespread adoption of solid-state lighting.

But as Scheidt asserts, LEDs contribute to only around 20 percent of the total lighting system cost, and in terms of lumens per dollar, LED light sources are at least as cheap as the fluorescent tube.

"The cost lies with the remaining 80 percent [of components] that make up the full luminaire... which include plastics, heat sinks, power converters, which are all very mature from an electronics point of view," he says.

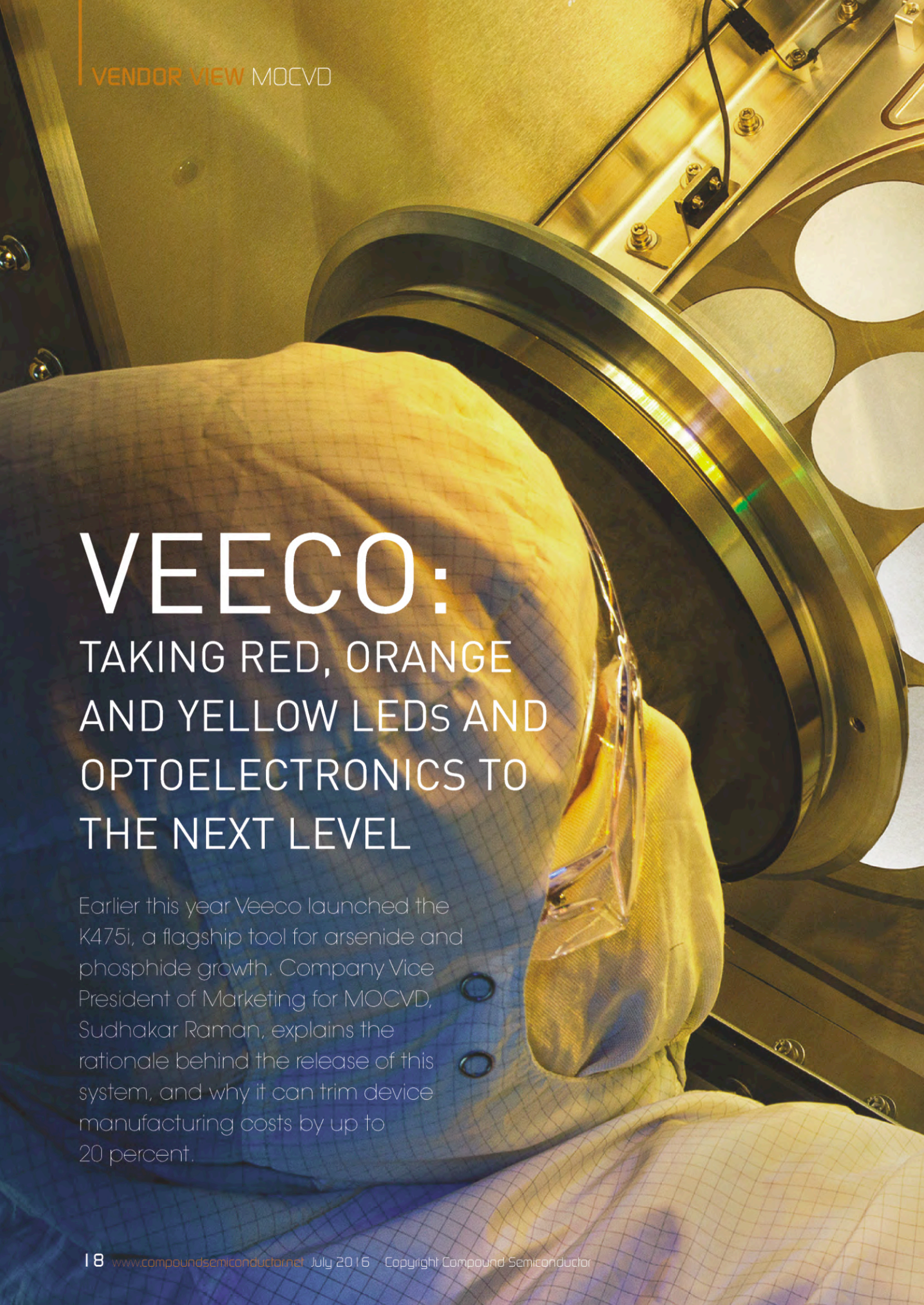
Cree now intends to strip away this content, and drive costs down further. "People point at LED systems, and especially packaged LED manufacturers, and think here is the problem, but nothing could be further from the truth," he says.

In the meantime, Scheidt is certain packaged LEDs, as well as the more affluent luminaire market, will remain important to Cree. But, like other packaged LED manufacturers, Cree is still grappling with tough market conditions.

A strong US dollar in 2015 combined with low-cost LEDs coming from China- and Korea-based companies, saw revenues declining for Cree, LG Innotek, Nichia and more.

As Scheidt puts it: "Talk to any market analyst about packaged LEDs in 2015, and it was a bad year for everyone. It's been more a case of how well did you survive and I think Cree has done OK."

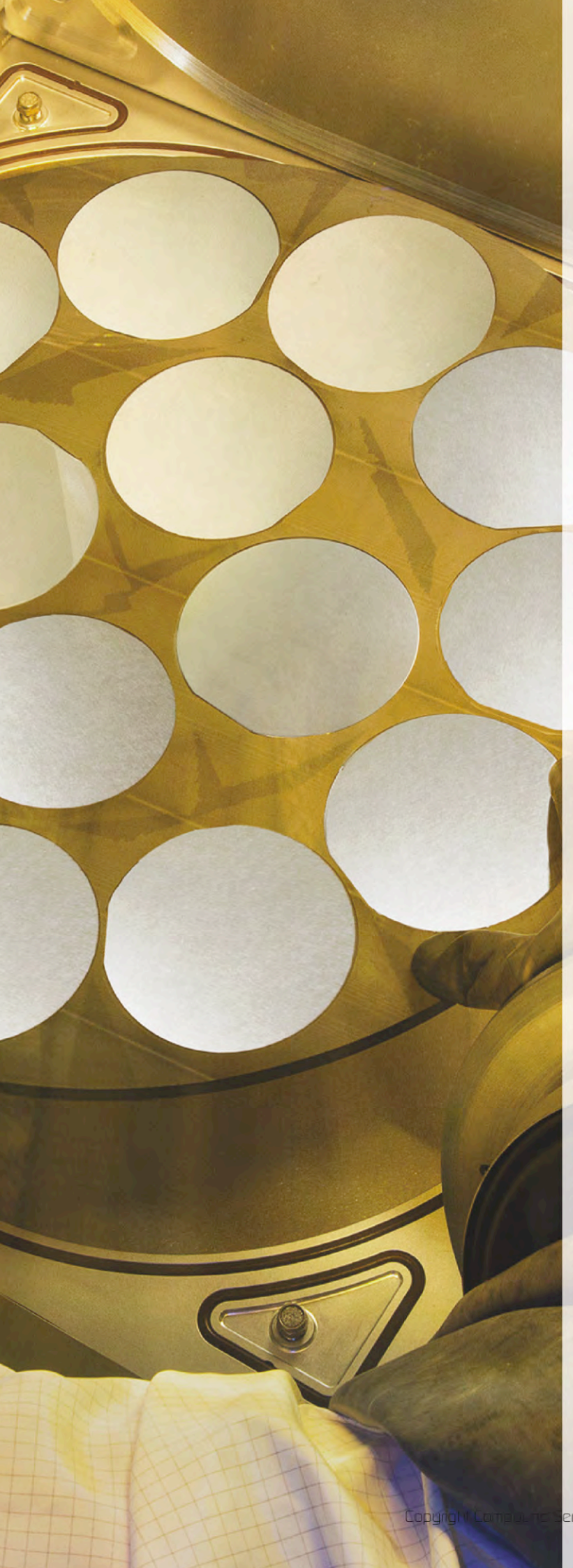
Scheidt points to aggressive pricing continuing from many suppliers but adds: "A company can't keep running on little to no margins with infinite capacity so it's really a question of when will [these manufacturers] hit their limits."



VEECO:

TAKING RED, ORANGE AND YELLOW LEDs AND OPTOELECTRONICS TO THE NEXT LEVEL

Earlier this year Veeco launched the K475i, a flagship tool for arsenide and phosphide growth. Company Vice President of Marketing for MOCVD, Sudhakar Raman, explains the rationale behind the release of this system, and why it can trim device manufacturing costs by up to 20 percent.



The K475i system is capable of processing four or six-inch wafers for high-volume manufacturing.

Q What are the main markets that the K475i will serve?

A The markets are: red, orange and yellow LEDs, which are primarily driven by displays and signage, automotive, and some of the lighting market; and the solar cell market, which is triple-junction solar cells that are mostly used in space applications. The other market that is up and coming is in optoelectronics – it is the laser telecom market.

Q Currently there is a great deal of interest in wearable applications. Are your customers optimistic about this? And are there specific products or product applications that you, or they, are particularly excited about?

A Wearables is an interesting area. The way I see wearables is not just from a display perspective. There are a variety of wearables and the primary driver that we can see enabling the future is very similar to one of the market segments that I just talked about, the optoelectronics segment. A bunch of sensors are going to get integrated into these wearables, enabling more accurate biometric sensing and gesture recognition. That's where you will need both arsenic/phosphide-based devices and GaN-based devices.

From a light-generation perspective, we don't see a huge market for wearables, because the number of LEDs in a wearable is very small.

Q Primary markets for red, orange and yellow LEDs include outdoor displays and signage. Are the end markets growing, in terms of volumes and revenue?

A Typically, we are seeing close to a 10 percent compound annual growth rate in the red, orange, yellow (ROY) market. It is primarily driven by, as you say, displays and signage, automotive, and some lighting-based devices.

In terms of LED unit count, the ROY market is probably a one-to-eight to a one-to-ten ratio of the blue LED market.

Q The manufacture of red, orange and yellow LEDs dates back far further than that of their blue cousins, which are now used extensively in general lighting. How does the production of these two types of devices compare, in terms of the requirements to deliver a competitive product?

A For a competitive product, you have to look at how to develop a certain level of thickness uniformity.

Red, orange and yellow LEDs have a Distributed Bragg Reflector (DBR) beneath the active region. The thickness uniformity of these layers is extremely critical to meeting the right wavelength of light. What we pay attention to is the DBR uniformity and the repeatability of those layers.

In a blue LED, you use a multi-quantum well (MQW), and if that uniformity shifts you will have a big binning issue. In the GaN-based LED, we pay attention to the wavelength uniformity and thickness uniformity of the MQW layers, primarily.

Q Judged in terms of profit margins, is it better to be making blue LEDs, or red, orange and yellow variants?

A It depends. The reason why I say it depends is that even in the red, orange and yellow, there is one segment, automotive, that's a pretty high-margin, high-revenue segment for our customers. The requirements there are very much more demanding, in terms of reliability and brightness.

In very low-end toys, and very low-end signage and displays, profit margins are razor thin. Comparing the blue LED versus the red LED, I think profit margins are very similar if you are just competing in the low-end to mid-end range.

If you go to tier one manufacturers, like Nichia, Lumileds and Osram, they are going into more speciality lighting and automotive. Their profit margins are very different.

Q How does the K475i build on your previous tool for arsenide and phosphide growth, the K475?

A Our core technology is the TurboDisc platform. In the GaN space, we had a K465. We then developed a uniform flow flange, based on TurboDisc technology, and launched the K465i. From then on we have scaled to MaxBright and EPIK, and gained market share leadership.
We are doing exactly the same with arsenides/phosphides. Our core system is the K475. The K475i is fundamentally a much better high-uniformity, highly repeatable tool.

At the heart of the K475i system is Veeco's production proven TurboDisc reactor technology.

Q What are the pros and cons of the K475i compared to rival tools for the growth of arsenides and phosphides?

A The fundamental advantage is a strong TurboDisc technology. Repeatability of the uniformity is very, very high, and because of TurboDisc technology – it is a laminar flow – the

"Our core technology is the TurboDisc platform. In the GaN space, we had a K465. We then developed a uniform flow flange, based on TurboDisc technology, and launched the K465i. From then on we have scaled to MaxBright and EPIK, and gained market share leadership. We are doing exactly the same with arsenides/phosphides. Our core system is the K475. The K475i is fundamentally a much better high-uniformity, highly repeatable tool"

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Veeco introduced the TurboDisc K475i As/P MOCVD System to meet demand for red, orange, and yellow (ROY) LEDs for displays, signage and automotive markets as well as for solar and optoelectronic manufacturing.

time between preventative maintenance (PM) is very long. What this means is that you can go for long campaigns, with highly repeatable results, within the wafer, wafer-to-wafer and run-to-run, for every batch of wafers that you put in and take out.

Another advantage of the TurboDisc technology is inherently less defects and particles, for better device performance. So you don't need to clean every run or every few runs – you can go through hundreds of runs without any cleaning inside the chamber. That's a core advantage that is fundamental to the new applications that are coming along. But even with ROY, when LEDs go into higher-end automotive, particle performance is really critical.

Q You claim that the new K475i system has been able to reduce the cost-per-wafer by 20 percent. That's a substantial margin. How have you achieved this?

A It's based on the advantages of longer campaigns, longer intervals between PMs, and much higher uniformity. You not only increase productivity – you add yield. When you combine those two, you get to a 15 to 20 percent range of cost-of-ownership benefits (see "Calculating cost-of-ownership for MOCVD capital equipment" for more details).

Q The K475i can be configured as a 15 x 4-inch tool, or a 7 x 6-inch tool. What do you expect to be the most common configuration?

A Most of the tier one customers are using this in 6-inch, and most of the rest of the world is in 4-inch.

Q To what extent is the K475i future-proof?

The K-platform was built future-proof, which means with future upgradability in mind. The K475 can be upgraded to the K475i. Beyond the K475i, if we have to improve certain parameters inside the tool to improve performance, we would take a very close look at it. We protect the initial investment of the capital for the customer. It's very important.

Q You have worked with Changelight on the development of the K475i. What are the benefits of working with this LED maker when developing the reactor?

A The reactor and the core technology we developed ourselves. I would say that's the fundamental core IP for Veeco. Why we work with Changelight, and why Changelight has been very helpful, is that they were our beta-partner in qualifying the K475i. They used the tool from the initial process runs all the way to chip-level data, to prove that this reactor is equal or better than their current system. It's also very important to validate customer qualification and acceptance. Veeco has a strong track record of meeting demo specifications and obtaining positive customer endorsements.

Q China is accounting for an increasing proportion of LED chip production. Is this the primary market for the K475i?

A It is one of the primary markets for the K475i. China has a lot of ROY LED production by unit volume, but there is also a pretty healthy volume of production of ROY LEDs/arsenide/phosphide devices outside China. Our expectation for this tool is that it will go into multiple applications beyond ROY LEDs and help us to compete very effectively against the competition, having made this investment in furthering the product roadmap.

Q The K475i can be used to make lasers, solar cells, pHEMTs and HBTs. Do you expect to sell many tools to the producers of these devices?

A In each of these segments, the market trends are different. If you take lasers or solar cells, versus pHEMTs and HBTs, they are in different parts of the market adoption curve. pHEMTs and HBTs are a lot more mature from a market perspective, but one of the growing segments that we see, and what we call the opto market, is the laser market. Talking to our customers, it has primarily been driven by the megatrend of cloud computing, data storage and big data, driving the need for higher-speed communication. People are downloading a lot of videos and data, so there is a lot of bandwidth that is needed to keep up, because data transfer is going higher and higher. Communication lines are moving from copper to optical, which drives the need for lasers.

Q What does that mean from the perspective of Veeco?

A We expect to sell, over the next few years, several tools into this segment. At this moment we are also trying to map what this growth trend means in the long-term – and how big the market can be.

Q Earlier this year you teamed up with imec, starting work on a project to accelerate the development of GaN-on-silicon power devices, using your Propel Power GaN System. What progress have you made to date, and what are your next targets?

A The goal is to further validate with industrial partners, through the imec consortium, that the Propel system, which is our single-wafer-based MOCVD technology, delivers highly cost-effective GaN-based power devices.

The Propel Power GaN System is akin to what has happened in the semiconductor industry. Early in the semiconductor industry batch systems were the tools of choice, and as the node size got smaller and smaller, companies migrated from batch tools to single-wafer tools, which gave significantly superior on-wafer performance. This is fundamental to the device, even though it was 'expensive'. The device values trumped, and enabled customers to go to the next level.

We believe the same thing is going to happen in the power electronics space, on the GaN-based power devices. That's the fundamental reason we developed the Propel technology – to further enable the market to cross over the chasm.

Q How big do you think the GaN-on-silicon power market could be?

A We believe the GaN-on-silicon power market is going to have strong play in the sub 650 V operating range. One of the things that we see – that is creating a need in the consumer space – is wireless charging. Large companies are trying to create wireless charging devices, so you don't always need to connect your device, or even place it on a mat.

We see more steady growth and steady penetration for the GaN-on-silicon power market. What the market research guys say is the end market is going to be somewhere between $300 million and $500 million in the next five years. But my personal belief is that there will be an inflection point, and when it happens, it can be a lot bigger than people predicted.

Q The Propel is a single-wafer, 8-inch tool. Why are you advocating this configuration for GaN-on-silicon, but a multi-wafer approach for arsenide and phosphide epitaxy?

A For arsenide/phosphide-based epitaxy for ROY LEDs or lasers, from an epitaxial perspective, it is primarily flow uniformity that we have to work on. So long as you get your flow uniformity, then by design you will get the uniformity of the DBR layers, which means that your yield will be high. So the batch works perfectly.

When it gets to the next level of complexity, you need to have very good flow uniformity and extremely good thermal uniformity, so you probably want to go towards a single-wafer platform for GaN-based devices. It is the same argument for blue LEDs, for the mid-power range. The EPIK 700 multi-wafer platform is the flagship, and will continue to remain so. If there is a need to get extremely tight wafer uniformity levels, then probably the industry will move to single wafer.

Q With the EPIK 700, the K475i and the Propel Power, have you got all the bases covered?

A We believe we have all the bases covered. We have three platforms: we have an EPIK platform for GaN-based devices for blue LEDs; we have a platform K475i, which is arsenides/phosphides-based; and we have a Propel platform – power is the first segment we will address, and we believe that there are future segments that we can address using Propel.

You will see more products coming out of the Propel platform that are single-wafer based. Epitaxy is like lithography, you've got to get it right before you can get your device right.

Calculating cost-of-ownership for MOCVD capital equipment

LED MANUFACTURERS are constantly looking for ways to improve profitability. One way to do this is to trim manufacturing costs by reducing expenditure on capital equipment. However, it is folly to select equipment solely on its price. Instead, one must balance the initial purchase and installation costs with other critical factors that determine the cost of ownership. Over the life of an MOCVD system, throughput rates, equipment reliability and yield have a greater impact on cost-of-ownership than initial purchase costs.

To make an informed decision when purchasing an MOCVD system, the lifetime cost-of-ownership must be considered. This is the same as the cost per wafer.

$$\text{Cost per wafer} = \frac{\text{total cost (fixed costs + varaiable costs)}}{\text{throughput x utilization x yield}}$$

In this equation fixed costs include purchase, installation and facilities costs that are normally amortized over the life of the equipment; variable costs include materials, labour repair, consumables, floor rent, utility and overhead expenses incurred during equipment operation; throughput is the time needed to meet a process requirement, such as depositing a nominal film thickness; utilization is the ratio of production time to total available time; and yield is a measure of defects and the uniformity of key quality parameters on the wafer. In the case of an LED, this would include peak wavelength and forward voltage.

There are five key benefits associated with using a cost-of-ownership model:

- It creates a common standard for LED manufacturers to objectively scrutinize operations
- It provides an objective analysis method for evaluating decisions
- It offers a clear tool estimate for the cost of ownership
- Equipment suppliers can use common decision-making elements to make better-informed decisions on future product offerings
- It helps to foster greater cooperation between equipment suppliers and users, to provide input parameters and data that will benefit the industry

ERADICATING ERRORS IN GaAs FABS

To increase yield and throughput in high-volume GaAs fabs, engineers should obtain more data from suppliers, introduce better approaches to analysing process data, and understand how different statistical methods handle outliers.

BY RICHARD STEVENSON

EVEN FOR an established GaAs fab, it is far from easy to master high-volume manufacture of a high-class product. One of the keys to success is to develop a competitive prototype that appeals to customers and leads to substantial orders. But that isn't all that is needed. Generating a healthy profit margin month-in, month-out requires engineers to guard against anything that could lead to a drop in yield.

Several approaches that can be taken to ensure a high yield in a GaAs fab were discussed at this year's CS Man Tech Conference. At this meeting, held in Miami from 16-19 May, speakers described: the benefits resulting from greater information about incoming materials; a route to more insightful, speedier trouble-shooting via a new approach to handling process tool data; and the most appropriate methods for treating outliers within data sets.

Working with suppliers

When Marie Le Guilly took over as supplier quality engineer for epiwafers and metals at Qorvo's Hillsboro fab she was in no doubt that there had to be greater control of incoming materials: "I needed the supplier data in order to trouble shoot issues quickly and continuously learn," says Le Guilly, who believes that speed is vital to Qorvo's business. "We continuously make product, so if there is a material issue, we need to contain it and resolve it very quickly."

Before adopting this approach, there were many instances when product failures could be traced back to material that was compromised, but still met a purchasing specification. To try and address this loophole, Le Guilly convinced suppliers to share their data that they kept internally. While a small shift in one characteristic of a material may not concern suppliers, it can have a profound impact on device performance.

Although some suppliers have been more reluctant than others at disclosing information, they are now sharing their data – and doing so without increasing their prices.

From a supplier's perspective, disclosing more data has pros and cons. One supplier shipped a metal to Qorvo that is outside 'ship-to-control' limits, but within purchasing specifications. This source is now under evaluation at the Hillboro fab.

"This is putting a burden on the supplier as they wait for our results," admits Le Guilly, who points out that there are also benefits for them – the supplier improves internal control of material and control of suppliers.

In the CS Man Tech paper, Le Guilly and co-workers offered two illustrations that highlight the benefits a chipmaker obtains when receiving more data from a supplier. The first example involved a supplier of metals, which present a high risk to a GaAs fab, because a shift in material characteristics may only be detected during electrical testing – and at that stage the fab will have processed hundreds of wafers that will have to be subsequently scrapped.

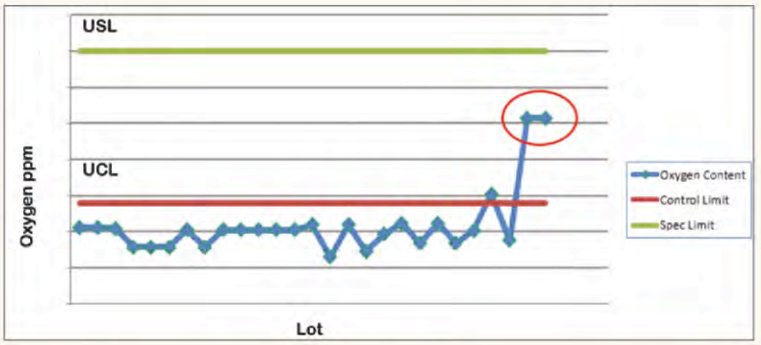


Figure 1. Qorvo's supplier of titanium caught the uptick in oxygen content in the titanium target, thanks to the ship-to-control specification. The hike was traced back to the titanium powder supply. USL is the upper shipping limit and UCL is the upper control limit.

By monitoring its composition, the supplier exposed a hike in oxygen content in its titanium target, and traced the issue back to the raw material supplier. Qorvo evaluated this material – it was above the upper control limit but inside the upper shipping limit – before releasing it to production.

The second example involved Qorvo's partnership with an epiwafer supplier, which shared a great deal of data that had been previously restricted to internal use. By accessing data that goes beyond what is included in purchasing specifications, Qorvo's engineers have been able to connect supplier data to device parametric data in real time.

Several benefits have resulted. When Qorvo made the

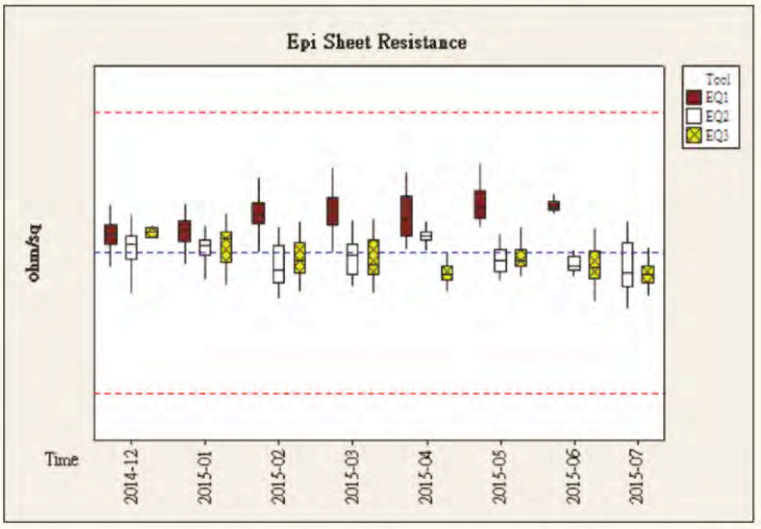


Figure 2. Process control monitoring of the sheet resistance of an epilayer at WIN Semiconductor revealed an increase in variation in February 2015. Insight provided by an internally developed computer programme, considering 'analysis of variance', identified the process behind this – a post-metal surface clean. Engineers traced the problem to a dilution of a cleaning solution in a particular tool.

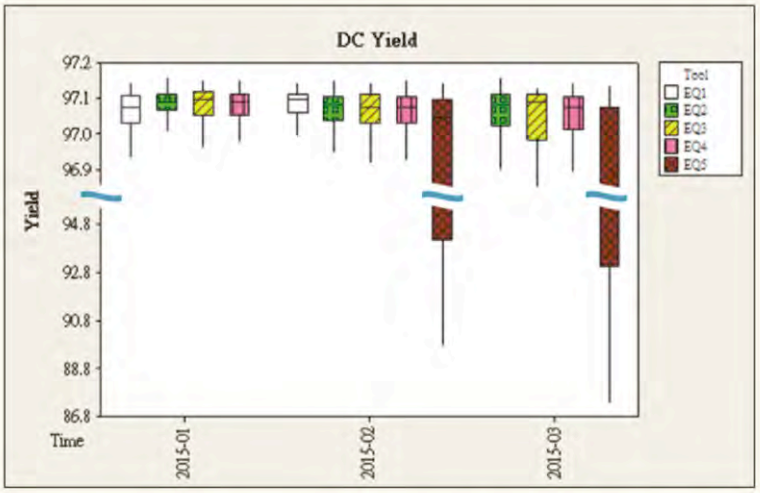


Figure 3. At WIN Semiconductors, engineers noted that the DC yield variation of a customer product increased in the middle of February 2015. The problem was traced to a photolithography exposure tool, EQ5. It had a different chuck configuration to the other tools, and caused a different thin-film resistor critical dimension uniformity at the wafer edge for specific mask sets.

transition to a new supplier for MBE pHEMT epiwafer production, correlating epi and parametric data slashed the time taken to establish a ship-to-control specification. When devices started to fail due to a low pinch-off voltage, this could be correlated to a low pinch-off measured by the supplier, and it led to an increase in the ship-to-control specification; and when RF failures were correlated with on-resistance, and traced back to variations in the aluminium content of the Schottky device layer, Qorvo added a photoluminescence measurement to the specifications to control composition.

Historically, one of the advantages of being a vertically integrated chipmaker, rather than one that outsources the epi, has been the close cooperation that can be fostered between the process and device engineers. But that gap can be bridged when supplier data is handed over to the chipmakers, argues Le Guilly. "[It] enables successful outsourcing."

Digging in the data

When large GaAs fabs are running close to capacity, they are churning out millions of die and creating a colossal amount of data. So, to try and deal with all that data in an efficient and effective manner – and to empower engineers to troubleshoot quickly and successfully – a pair of engineers at WIN Semiconductors have spent three years developing an in-house data analysis program.

At WIN the majority of semiconductor processing steps are performed on one of several tools that may be nominally the same, but produce slightly different results. So, to account for these differences, engineers used a test known as analysis-of-variance. It determines the difference produced by a set of tools performing a particular process. By applying this test to all process steps, they can be ranked using statistical criteria. This exposes the steps with the greatest variations.

One of the pair of engineers involved in developing the computer program, Ming-Wei Tsai, spoke about this work at CS Man Tech. He says that the computer program, which was ready about a year ago, is designed for off-line monitoring, rather than real-time process monitoring. "We are promoting this software tool to our process engineers, and encouraging them to use it for identifying the source of parametric performance variations."

Sources of the greatest variations are identified using F-statistics. This is a common statistical approach for qualifying a new tool. It involves comparing the results produced by their tool with those produced by a baseline tool. "However, the idea of ranking the F-statistics for all the interactive process steps originates from us," says Tsai.

The F-statistics generate a figure-of-merit known as a p-value. The lower it is, the larger the variation. So, by listing p-values for various processes, engineers at WIN can quickly uncover the origin of the most significant process variations and address them. Tsai believes that the money saved by identifying and solving issues more quickly will have already outweighed that spent on developing the computer program.

One example of its capability, described by Tsai in his CS Man Tech paper, involved identifying the cause of an increase in the variation of sheet resistance of an epitaxial layer. Empowered by the program, engineers took less than five minutes to analyse 170 wafer lots fabricated over a six-month period. The software then enabled engineers to scrutinise more than 400 process steps, which were listed by p-value. This identified the culprit as a post-metal cleaning step. Armed with this insight, plots were produced for individual pieces of equipment, exposing 'EQ1' as the troublesome tool. Eventually, engineers determined the root cause: dilution of the cleaning solution by residual deionised water, which came from wafers subjected to another process on the same cleaning tool.

Tsai's paper offers a second example of the benefits of the in-house program – uncovering the cause of a DC variation in a customer product, which deteriorated in the middle of February 2015. WIN's program generated p-values for several processes, with the lowest coming from a visual inspection that could not correlate to the yield drop. After this, the most promising candidate was the photolithography step for producing the thin-film transistor.

Plotting charts of individual tools for this step revealed that one of them, EQ5, produced a lower yield than the others. Engineers then identified the origin of this reduction in yield as a difference in chuck configuration. This caused a difference in thin-film resistor critical dimension uniformity at the wafer edge, but only for some mask sets. Note that this behaviour was not observed during the collection of DC yield data, for a qualification that involved a different chuck configuration.

The software has also helped to identify another issue, which was not described in Tsai's CS Man Tech paper. This recent issue is that an etching process for forming

a via has produced several out-of-control events.

"Etching photo engineers had checked their process tools, and all of them were normal," explains Tsai. So they then checked all the manufacturing steps with their computer program. This identified the problem as a measurement recipe associated with the scanning electron microscope.

After restoring the recipe, the via etching process returned to normal. "Our engineers are still trying to find out the real root cause and prevent it from happening again," remarked Tsia.

Although the program built by Tsia and his co-worker is powerful, it does have its limitations. A major one of these is that problems cannot be picked up immediately. That's because sufficient data has to be collected from different machine tools after the abnormal process has begun before enough data has been generated to create a low p-value. Another weakness is that the selections of initial lot lists can impact the p-value rankings. The consequence is that an engineer might have to investigate several steps with low p-values.

Dealing with outliers

When devices are manufactured in high-volumes, it is inevitable that a few parts will have characteristics that are significantly different from the majority. Even though these outliers may still conform to specifications, their difference may indicate a defective part, or one that is less reliable.

That was the case for power amplifiers made by leading GaAs chipmaker TriQuint, which merged with RFMD in 2015 to form Qorvo. TriQuint used 'part-average testing' to screen for outliers, and in December 2013 this led engineers to note an increase in leakage on a high-band input pin of a GSM/EDGE power amplifier. Further investigation revealed that the failures associated with this part-average testing methodology originated from a highly localised fab defect on the base contact of a diode on the high-band HBT die.

Qorvo's Thortsen Seager recalled this investigation in his CS Man Tech paper, which discussed methods to deal with outliers. Here, he also offered another compelling need to deal with outliers – if they are ignored, they can make a mockery of data analysis. For example, if they are included when generating an equation for a set of data, the best-fit line may fail to pass between the majority of points and compromise predictive powers. Another arguement for developing a good approach to dealing with outliers is associated with the ever-growing complexity of RF products. Ten years ago mobile phones had two or three bands, now they contain 40 or more, and 5G will lead to even more RF components.

"This represents major manufacturing challenges, since the yield of each component geometrically impacts the stacked yield of the module," says Seager, who adds that the outlier component wastes the cost of all the other components in the module. So, if efforts to increase integration are to be successful, they must be accompanied by tighter tolerances and a reduction in variation.

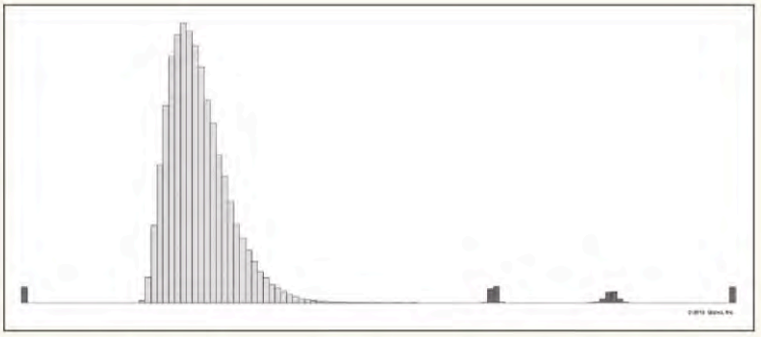


Figure 4. This histogram shows the results of the same in-house measurement on about 100,000 parts produced by Qorvo

When looking at data, such as that shown in Figure 4, it is easy to spot the outliers. They can be defined as observations not connected to the main distribution. However, care must be taken, as there can be instances when many of the data points that are not connected to the main distribution are clumped together. When that happens, it is more appropriate to consider a second mode.

The data shown in Figure 4, produced by making the same measurement on roughly 100,000 parts, has a main distribution with a positive skew and four minor peaks of outliers. The two extremes are unimodal – that is, all the data is in a single bin. That could be due to clamping of the test system – it may have been programmed to a fixed range, or have a set minimum value and a set maximum value. Meanwhile, the two peaks immediately to the right of the main distribution could be due to a process or assembly issue.

Based on the results of this test, Seager and co-workers took the measurements on five products, ranging from PA modules to filters, and applied five statistical methods to them. They concluded that modified part-average-testing is the best method for dynamic screening at the package part test, while for other scenarios, such as data analysis, the adjusted boxplot offers a reliable method.

These findings, along with those highlighting the gains of sharing data between suppliers and chipmakers, and the benefits of superior methods for handling processing data, will help engineers at GaAs fabs to have greater mastery over their chipmaking. While improvements to running a fab may not receive as much attention as the development of superior chip designs and record-breaking device developments, they make a massive contribution towards profitable, high-volume manufacture of great GaAs products.

Further reading

M. Le Guilly *et. al.* CS Mantech 127 (2016)
M. Tsai *et. al.* CS Mantech 123 (2016)
T. Saeger *et. al.* CS Mantech 135 (2016)

Mist Epitaxy:

The key to a great gallium oxide power device

Growing gallium oxide on sapphire can fulfil the promise of cheap, efficient, high-voltage power devices

BY MASAYA ODA, TOSHIMI HITORA AND NAONORI KUROKAWA FROM FLOSFIA

IN POWER CONVERSION SYSTEMS, the key components for transferring electricity between its AC and DC forms and changing its voltage and frequency are the power transistor and the diode. For this pair of semiconductor devices, silicon dominates, generating sales of more than $20 billion per annum.

Yet despite this success, these silicon power devices are far from perfect. When deployed in power systems, 10 percent of electrical energy can be wasted as heat – and addressing this weakness is not easy, because silicon devices are approaching their theoretical limit.

Moving to higher efficiencies requires the radical step of building devices with new materials with a higher bandgap. This move, which also unleashes higher operating voltages, has already delivered some success. GaN and SiC transistors and diodes are now on the market, with sales on the rise. However, the gains in performance that they are delivering go hand-in-hand with higher prices, and this is hampering a substantial increase in shipments of these wide bandgap power electronic products.

Another class of materials that has been attracting attention from the electronics industry is the ceramic oxides. Thin-film transistors made from InGaZnO are already being used in flat panel displays, where they offer low power consumption; and single crystals of $LiTaO_3$ and $LiNbO_3$ are being used as piezoelectric materials in surface acoustic wave devices, where they form filters in smart phones. There is also Ga_2O_3, a very promising material for power devices, thanks to its ultra-high bandgap of 5 eV.

This really high bandgap – it dwarfs those of SiC and GaN, which are 3.3 eV and 3.4 eV, respectively – is a tremendous virtue for any power device. It is not just that a wider band gap can withstand a stronger electric field, and ultimately enable a thinner device for a given operating voltage; it is also that a thinner device has a lower resistance, and thus a better conversion efficiency.

Another attractive feature of the Ga_2O_3 power device is that it can address the cost concerns that plague its SiC and GaN cousins. Very strong electric fields can be accommodated by this oxide, enabling a step-change in current density for a given footprint. So, for a given operating current, the footprint of a Ga_2O_3 power device can be substantially smaller than an equivalent made from SiC or GaN – and far, far smaller than a silicon variant. Thanks to this, Ga_2O_3 diodes and transistors have the potential to be cost-competitive with silicon incumbents, while delivering much higher performance.

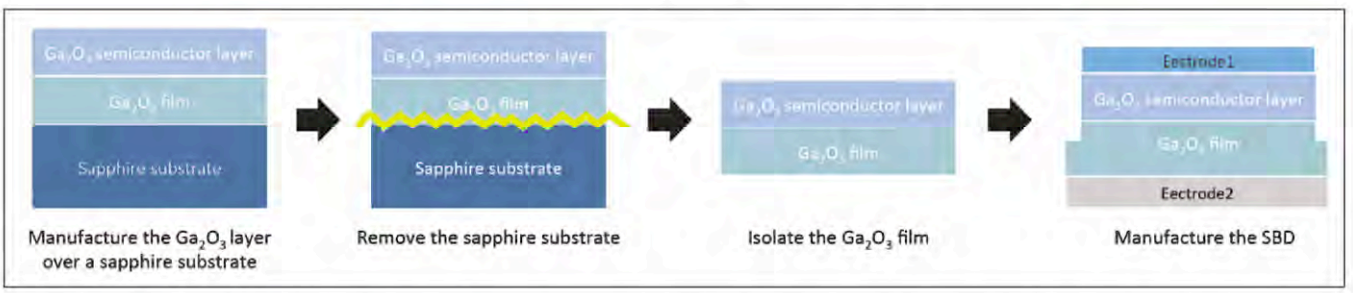


Figure 1. Flosfia's proprietary mist epitaxy technology, using a corundum-structured sapphire substrate, enables the growth of a high-quality, corundum-structured monocrystalline film of α-Ga_2O_3. Process steps that follow, which lead to the production of a Schottky barrier diode, include the removal of the insulating sapphire substrate.

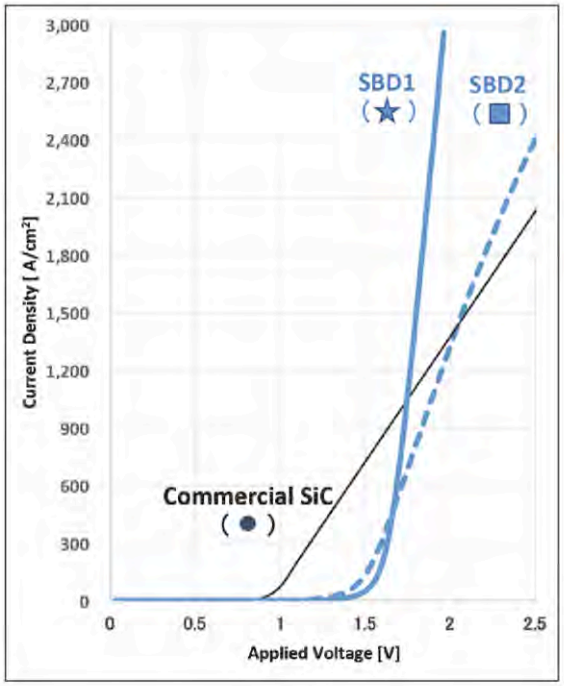


Figure 2. The turn-on voltage of Flosfia's α-Ga2O3 Schottky barrier diode is a little higher than that of an equivalent made from SiC. Lower values should result from an optimised contact.

An alternative way to view the extent of the superiority of Ga_2O_3 over other semiconductor materials is to consider Baliga's figure-of-merit (see Table 1). The on-resistance of a Ga_2O_3 device is more than 3000 times lower than that of a silicon equivalent, and one-tenth of that made from SiC. The Ga_2O_3 device can also be smaller, with values for resistance suggesting a footprint that can be one-seventh of SiC.

One of the pioneers of Ga_2O_3 power devices is the National Institute of Information and Communication Technology (NICT), Japan. It has produced Schottky barrier diodes and MESFETs using the oxide's β-phase (this is one of five phases, the others being α, γ, δ and ε). By fabricating these devices, NICT is helping to transform the potential of Ga_2O_3 power devices into a reality.

Another promising phase of this material is the corundum form, α-Ga_2O_3. It is this variant that we are using at Flosfia, a start-up in Kyoto that is collaborating with a team at Kyoto University lead by Shizuo Fujita and Kentaro Kaneko.

Sapphire: A fine foundation

We begin device production by growing α-Ga_2O_3 epilayers on sapphire with a novel deposition process known as mist epitaxy, which has been developed by ourselves and by the team at Kyoto University. Although sapphire is an unusual choice of substrate – many researchers prefer Ga_2O_3 – there is much to recommend it. First, α-Ga_2O_3 and sapphire share a trigonal (hexagonal) corundum crystal structure, and thanks to a lattice mismatch of just 3-5 percent, it is possible to form epilayers that combine excellent crystal material with an absence of fatal dislocations. In addition, due to sapphire's widespread use in the LED industry, it is affordable, well developed, and available in a variety of diameters, including 4-inch and 6-inch. Attractive pricing is very important, because it helps our devices to realise cost parity with those made from silicon.

Unfortunately, sapphire fails to excel in all areas. Its greatest weakness, when it comes to providing a platform for the α-Ga_2O_3 power device, is its poor thermal conductivity. That flaw can cause devices to deteriorate and even malfunction. To address this critical weakness, we have developed a proprietary technology that allows the α-Ga_2O_3 power device to be lifted off of the sapphire substrate and transferred to a metal support with good thermal conductivity (see Figure 1 for details of our manufacturing process). This improves thermal management, increasing heat extraction from the device, so that the chip can run at a lower temperature. What's more, by adopting this approach, it is possible to avoid the high series resistance that plagues SiC and GaN power devices that are compromised by their thick native substrates.

Along with the use of sapphire, the other key to our realisation of cost-competitive, high-performance Ga_2O_3 power devices is our proprietary growth technology, mist epitaxy. This novel deposition technology, developed by Fujita and co-workers at Kyoto University at first, involves a carbon-free gallium halide source. It is in the form of a water and/or alcohol solution.

Prior to deposition, this gallium halide source – it could be gallium chloride, gallium bromide, or gallium iodide – is atomised by ultrasound to form a mist. A carrier gas sweep this into a reaction chamber, which contains a heated sapphire substrate. Here, the constituents of the mist, particles with diameters of typically several microns, undergo a pyrolytic reaction with an oxygen source. This may be water, alcohol, or oxygen gas.

A merit of this process is that it takes place under atmospheric pressure. This eliminates the need for expense monolithic vacuum systems, thereby reducing equipment costs and slashing process times. Such gains are enviable, because they are impossible to realise for semiconductor crystal

Table 1 Material properties of various semiconductors highlight the superiority of Ga_2O_3 over SiC, GaN and silicon.

	Si	4H-SiC	GaN	β- Ga_2O_3	α- Ga_2O_3
Substrate	Si	SiC	Sapphire Si GaN	β-Ga_2O_3	Sapphire
Bandgap (eV)	1.1	3.3	3.4	4.8	5.1
Breakdown field (MV/cm)	0.3	2.5	3.3	8	9
Baliga's FOM (to Si)	1	340	870	3444	5000

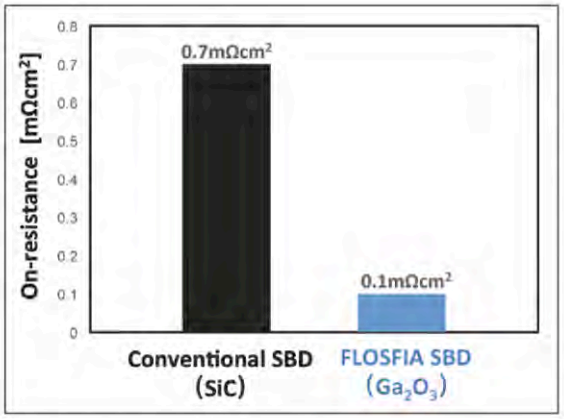


Figure 3. Flosfia's α-Ga_2O_3 Schottky barrier diode has an on-resistance that is one-seventh that of SiC. That's a significant advantage, because there is the promise of a reduction in footprint by a similar factor, enabling cost-parity with the silicon Schottky barrier diode.

growth under a high vacuum. The idea of growing semiconductor crystals under atmospheric pressure, particularly in the presence of water, is incredibly counter intuitive. It raises concerns over impurities and crystal quality. However, we have shown that these concerns are addressed by fine-tuning the process. For example, the residual impurity concentrations are beyond the lower detection limit of secondary ion mass spectroscopy (SIMS), while the X-ray rocking measurements of a film of α-Ga_2O_3 deposited on 4-inch sapphire produce a peak for the (0006) plane with a full-width-at-half-maximum of less than 50 arcsec. Morphology is also excellent, with atomic force microscopy revealing a one-monolayer step and an atomically flat terrace on the surface of this oxide. Device results are also very promising, with Schottky barrier diodes setting a new record for on-resistance for any device.

The production process

Production of these diodes begins with the growth of a thin film of α-Ga_2O_3 on sapphire (see Figure 1). We use our proprietary lift-off technique to separate this film, which had a thickness of less than 20 μm, from the sapphire substrate. After transferring this free-standing film to a metal support, we complete the fabrication of a vertical α-Ga_2O_3 Schottky barrier diode with the likes of etching and metallization.

The current-voltage characteristics of our diodes compare favourably with commercial equivalents made from other materials (see Figure 2). Although the turn on voltage of 1.5–1.6 V is slightly larger than equivalents made from both β-Ga_2O_3 and SiC, lower values should be possible by optimising the contact metals.

Our devices excel in their on-resistance, with values ranging from 0.1 mΩ·cm² to 0.4 mΩ·cm². SiC, in comparison, has a typical value of 0.7 mΩ·cm². Thanks to an on-resistance that can be as low as one-seventh of that of SiC, there is a promise of a reduction in footprint by a similar factor, enabling cost-parity with the silicon Schottky barrier diode.

Despite a lack of passivation, our pair of α-Ga_2O_3 Schottky barrier diodes produces impressive breakdown voltages of 500 V and 855 V (see Figure 4 for a benchmarking of the performance of our devices and those made from SiC, along with the theoretical limits for various materials). These values, when considered in tandem with the on-resistance, are very encouraging. Compared to a commercial SiC diode, one of our devices has a superior on-resistance and breakdown voltage and the other device is even more impressive: it has an on-resistance and break down voltage that surpasses the limit of what is possible with SiC. All these results stem from the combination of the ultra-high bandgap of α-Ga_2O_3 and an architecture that is made possible by our lift-off approach.

Our work has shown that it is possible to tackle the Achilles heal of the Ga_2O_3 power device – its low thermal conductivity – and target cost-parity with silicon, thanks to a footprint that can be one-seventh that of SiC. Our next steps on the road to commercialisation are to increase the breakdown voltage and the stability of our device by improving the metal contact and introducing a passivation technology. We plan to sample α-Ga_2O_3 Schottky barrier diodes in a standard power package later this year, and then increase our portfolio, by developing and launching power transistors.

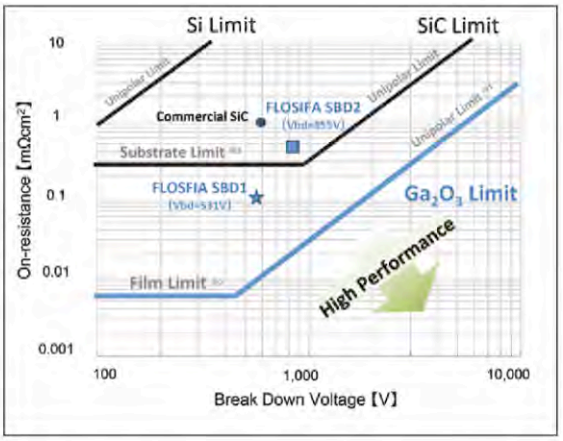
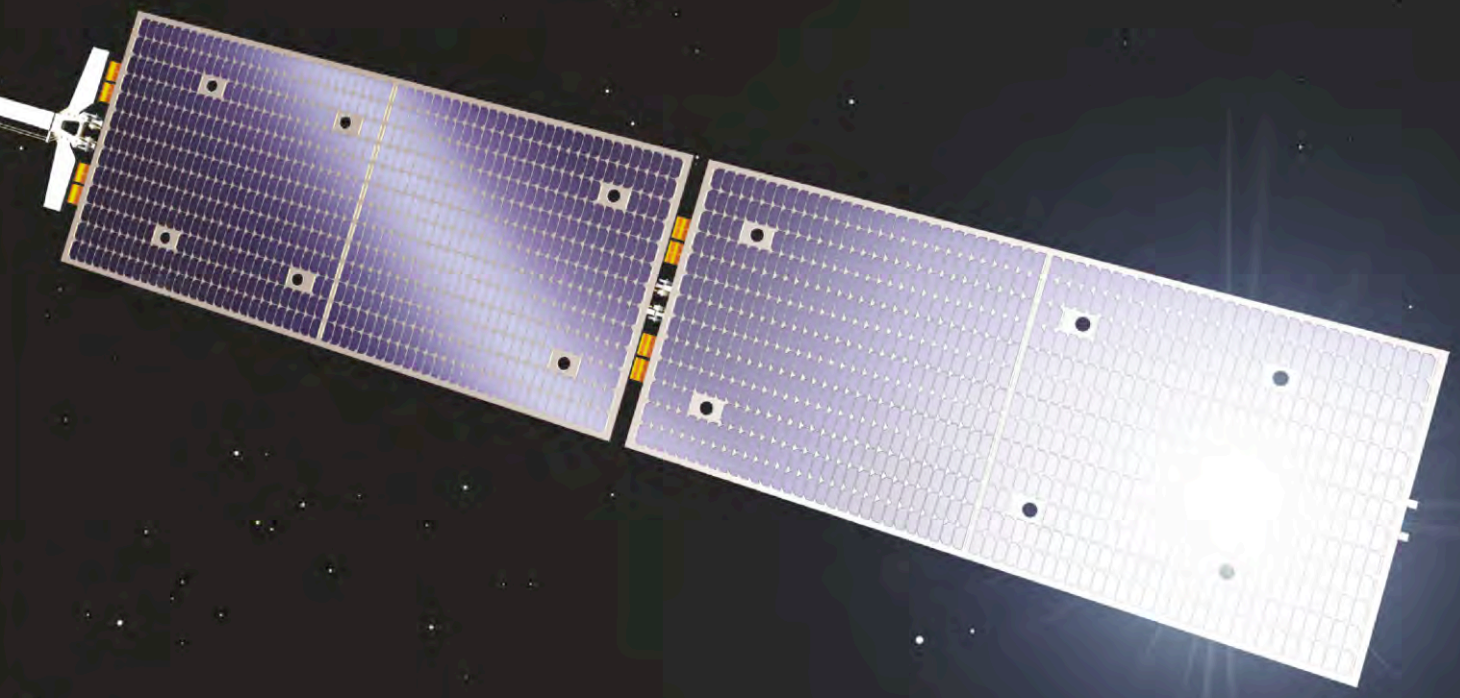


Figure 4. Flosfia's best device delivers a performance that is not only superior to a commercial SiC device, but also better than its theoretical limit. The unipolar limit is set by the physical properties of the material, and by a limit that is related to the resistance of the base material (substrate, film). Flosfia's prototyped SBD1 realized the world's smallest on-resistance of 0.1mΩ·cm². The breakdown voltage exceeded 531 V, while the SBD2 realised an even higher breakdown voltage of 855 V. Note that: (1) It is assumed that electron mobility is 300 cm²/Vs, breakdown voltage is 8 MV/cm, and relative permittivity is 10; (2), the film thickness is 20 μm, and resistivity is assumed from measured values of mobility and carrier concentration; and (3), it is assumed that resistivity of the SiC wafer decreases by half by being thinned.

GaN HEMTs are ideal for making high-power amplifiers for satellite communication, because they are lightweight, compact, efficient and capable of delivering a high output power and uniform gain over a broad bandwidth

BY ROCCO GIOFRÈ AND PAOLO COLANTONIO FROM THE UNIVERSITY OF ROMA TOR VERGATA AND LAURA GONZALEZ, FRANCISCO DE ARRIBA AND LORENA CABRIA FROM TTI, SCIENTIFIC AND TECHNOLOGICAL PARK OF CANTABRIA

DEMONSTRATING THE CAPABILITY OF GaN HEMTs FOR **SATELLITE COMMUNICATION**



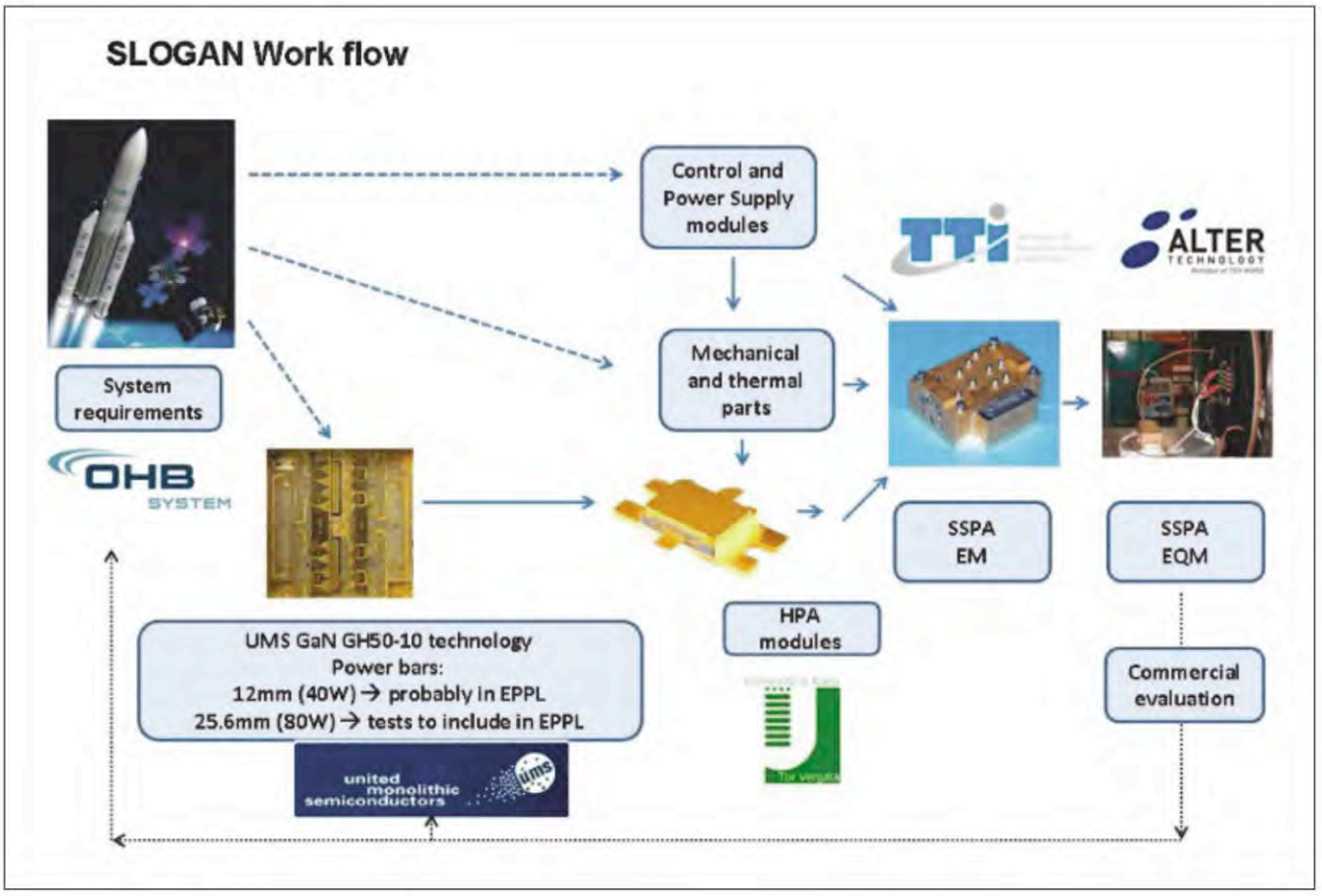
WHEN ELECTRONIC SYSTEMS are deployed in satellite payloads they have to negotiate several severe constraints. That's partly because space is such a harsh environment, and it is partly because there is a need to incorporate redundancy, so that it is possible to overcome potential electronic failures.

These criteria mean that robustness and reliability are essential for ensuring mission success. But these requirements are not the only ones that matter. In stark contrast to ground-based systems, small sizes and low masses are incredibly desirable, because they can slash the cost of getting objects into orbit – it can cost thousands of dollars to put a kilogram into space. There is also a third key consideration, efficiency, which arises because available power on a spacecraft is limited.

Unfortunately, it is not possible to optimise all the characteristics that matter simultaneously and create an incredibly rugged, ultra-efficient, incredibly lightweight electronic system. So compromises must be made, with a quest to identify the most desirable sweat spot.

Within the payload, tremendous scrutiny is directed at the mass, size and power consumption of the High Power Amplifier (HPA), along with its thermal and mechanical management. For space-borne HPAs, there are essentially two options: solid-state PAs and traveling-wave tube amplifiers.

Tubes are the incumbent technology, offering greater maturity and impressive output powers and efficiencies, especially in the high-frequency domain of the Ka-band and beyond. However, they suffer from several significant drawbacks. They command very high DC voltages, and they take up a large volume, especially in the lower frequency bands. What's more, expensive realization processes have to be employed to avoid unwanted electron resonance, known as multipaction, as well as corona effects, which can lead to device breakdown via gas ionisation.



These weaknesses are motivating research and industrial communities to investigate potential successors to travelling wave tubes.

Alternatives that are being pursued include devices based on GaN and related materials – they can deliver a significant improvement in output power performance. This advantage should enable GaN technology to replace travelling-wave tube amplifiers in next-generation satellite systems.

Solid-state PAs based on GaN have the upper hand over travelling-wave tube amplifiers on multiple fronts. They are smaller and lighter; they operate at lower voltages; they are less susceptible to hot electron phenomena; and there are no issues surrounding heating times. In addition, these devices degrade gracefully over time and offer a far higher degree of reconfigurability, which allows different power levels to be realised by combining a varying number of basic modules.

> “Within Europe, effort is being directed at demonstrating the capability of GaN technology applied to HPAs for satellite systems. While the promise of GaN is beyond doubt, devices made from this wide bandgap semiconductor cannot be deployed in space with confidence until the technology is proven at various stages, beginning with the breadboard and ending with the version that is prepared for launching into space”

Within Europe, effort is being directed at demonstrating the capability of GaN technology applied to HPAs for satellite systems. While the promise of GaN is beyond doubt, devices made from this wide bandgap semiconductor cannot be deployed in space with confidence until the technology is proven at various stages, beginning with the breadboard and ending with the version that is prepared for launching into space.

One of the projects that has been running in Europe and addressing these challenges is SLOGAN: Space quaLification Of high-power solid-state power-amplifer based on GAllium Nitride technology. The aim of this effort – that started in September 2013, runs to this August, and is backed by €2.4 million from the European Union Seventh Framework Programme – is to evaluate and apply European GaN-based technology provided by United Monolithic Semiconductor. More specifically, the primary goal of the project is the realization of a GaN solid-state PA for next-generation of Galileo satellites with a Technology Readiness Level equal to 6, which equates to the demonstration of technology in a relevant environment.

Results within SLOGAN are already showcasing the feasibility of implementing a high output power

Requirement	Unit	Value
Freq. band	-	E1
Center freq.	MHz	1575.42
Max. drain Voltage	V	45
Bandwidth	MHz	50
Output power	dBm	53.6
Output power	W	230
Max. Gain	dB	65
Gain Step	dB	1/30
Min. input power	dBm	-23
Max. input power	dBm	-11
Efficiency	%	55
Mass	Kg	<2.2
Size	mm	300x200 H=200

SLOGAN is developing GaN PAs that can serve in Galileo staellites. Europe's 13th and 14th of these lifted off on Tuesday, 24 May 2016 from Europe's Spaceport in French Guiana.

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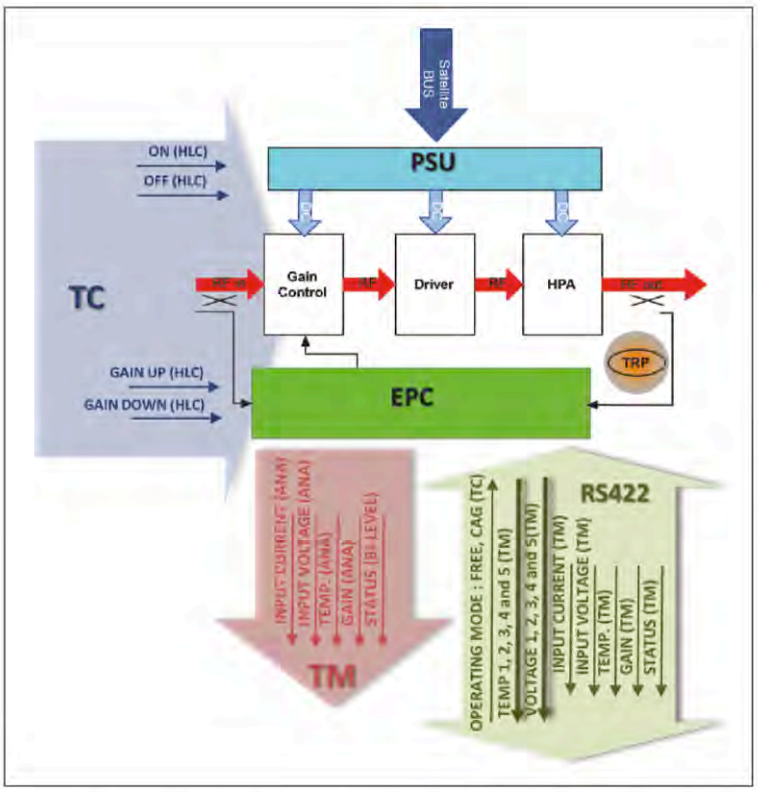

Figure 1. The SLOGAN solid-state PA includes an electronic power controller (EPC), a power supply unit (PSU) and a temperature controller (TC).

GaN PA for Galileo, which is a growing collection of satellites that will provide Europeans with a navigation system delivering horizontal and vertical precision of 1m. Note, however, that the success with GaN has already shown that this technology is capable of serving many other applications, including radio broadcasting, and transmit/receive modules for earth observation and airborne radar.

The tremendous progress of SLOGAN can be attributed to the leadership of TTI Norte S.L. from Spain, and strong contributions from five additional partners: Alter Technology from Spain, UMS from France, University of Rome Tor Vergata from Italy, OHB System AG from Germany, and Active Space Technologies from the Netherlands.

Every collaborator has expertise in a key technology and is performing a different role in the project: UMS leads GaN technology development and manufacture; TTI Norte is responsible for designing power electronics and firmware; the University of Rome Tor Vergata heads the design of microwave and millimetre-wave systems; Active Space Technologies is leading the thermo-structural and mechanical design; Alter Technology is taking responsibility for environmental characterization of space-borne systems; and OHB System is driving the development of satellites, and their building and launching.

The first task within the project was to identify the potential adoption and corresponding requirements of next-generation Galileo HPAs. As OHB Systems is responsible for integrating flight Galileo satellites, it determined the engineering qualification model for the PA operating in the E1 band on board the Galileo spacecraft (see the table on page 35 for a list of these electrical, mechanical, thermal and environmental requirements).

Building blocks for developing RF power modules are GaN HEMTs with 0.5 μm of gate length. Formed with a UMS GH-50 process, these transistors deliver 3.2 W/mm at a 50 V drain voltage.

Two power bars were made with these HEMTs. The shorter, a 12 mm device, had already been inserted in the European Space Agency's European preferred parts list at the beginning of the project. The longer cousin, 25.6 mm in length, has recently joined this list, following evaluation in the SLOGAN project.

The PA that has been built during SLOGAN consists of three sub-units: an RF unit, a power supply and an

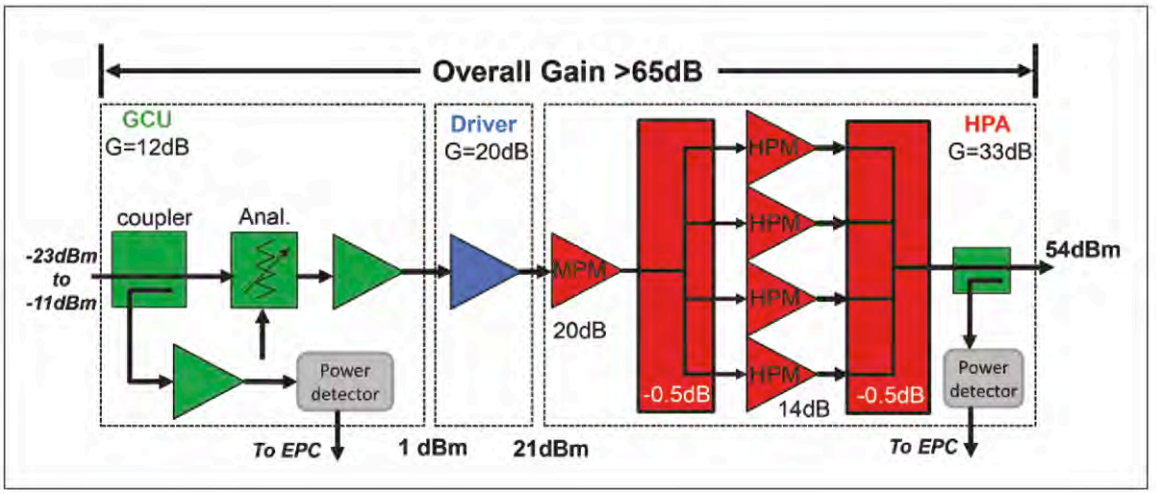

Figure 2. The architecture of the SLOGAN RF unit.

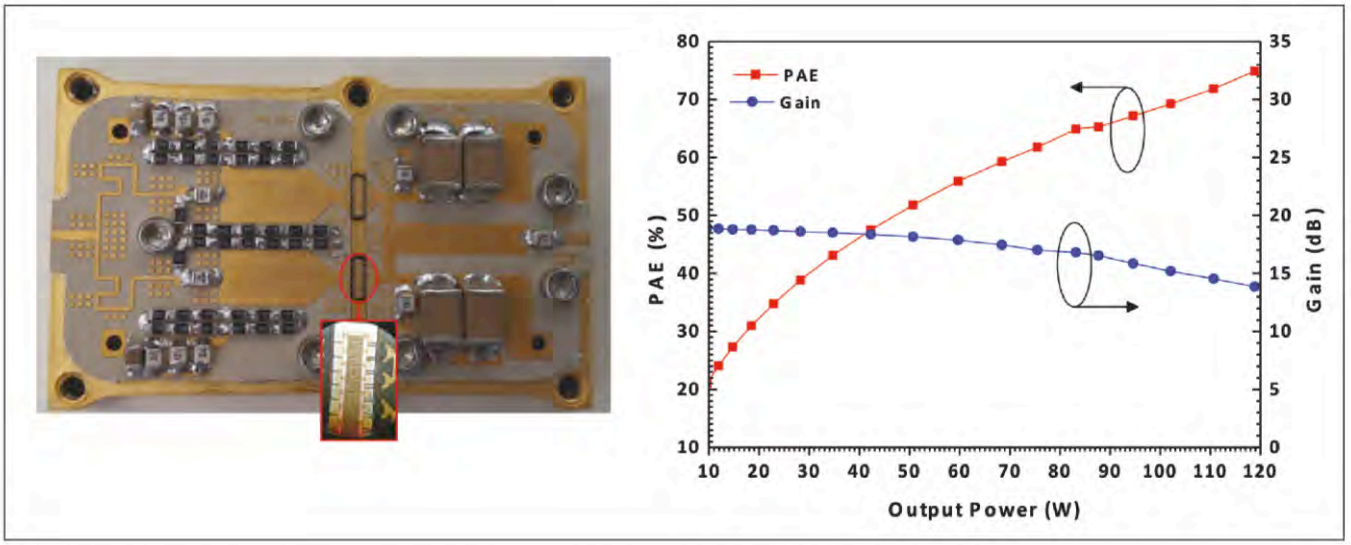

Figure 3. (a) photo and (b) performance of the 80 W power module based on a pair of 25.6 mm power bars

electronic power conditioner (see Figure 1). The role of the RF unit is to amplify the Galileo signal to up to 230 W across a 1550.42 MHz to 1600.42 MHz band, while providing a minimum gain of 65 dB. Within this section, there is a gain control unit for managing the gain of the overall power amplifier. This has to compensate for variations in temperature, aging and operating conditions. The job of the power supply is to convert the 50 V satellite primary bus voltage to internal required DC values, which can be positive and negative. Meanwhile, the electronic power conditioner is there to implement the telemetry and telecommand functionalities; properly control PA operation, while compensating against thermal and/or lifetime variation; and to control the current and the voltage applied to the RF power stages.

To realise the required power level at the output of the RF unit, four identical PAs are employed in parallel. They are in the form of two 25.6 mm power bars (see Figure 2 for the architecture of the RF unit, and Figure 3 for an image).

Completion of the RF chain of the PA is via: the introduction of two cascaded driver stages, using the 12 mm power bar; forming a gain control unit from linear amplifiers (UMS CHA3801-99F); and using fixed attenuators, designed for this project, and a commercial analogue attenuator (Hittite HMC346MS8G).

Requirements for the mechanical design of the systems include appropriate accommodation of the three sub-units and shielding of RF modules. Another key requirement involved accounting for the larger thermal dissipation required behind the power bars of the final stages, in order to avoid hot spots. This was accomplished by undertaking a thermal analysis into the thermal distribution of the PA. Results of this enabled identification of a suitable temperature reference point for monitoring the amplifier's operating temperature.

To determine the best foundation for the amplifier, a comprehensive analysis was conducted that accounted for multipaction and thermal issues. Emphasis was placed on the high-power final stage, and the selection of bonding and ribbon technologies for linking the different units or the external connectors (SMA at the input, TNC at the output).

These steps also prevented corona effects. The investigation led to the selection of Roger laminates

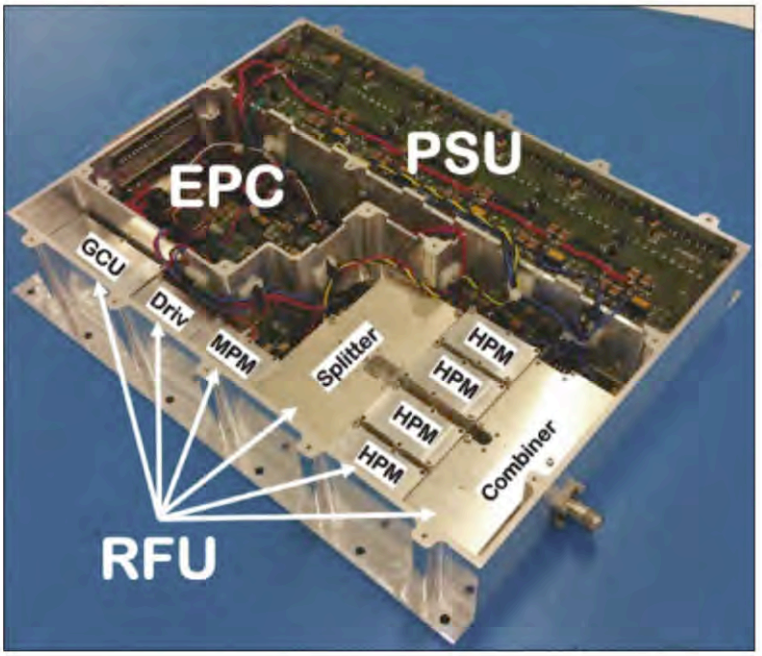

Figure 4. The first SLOGAN PA combines a RF Unit (RFU) with an electronic power control (EPC) and a power supply unit (PSU).

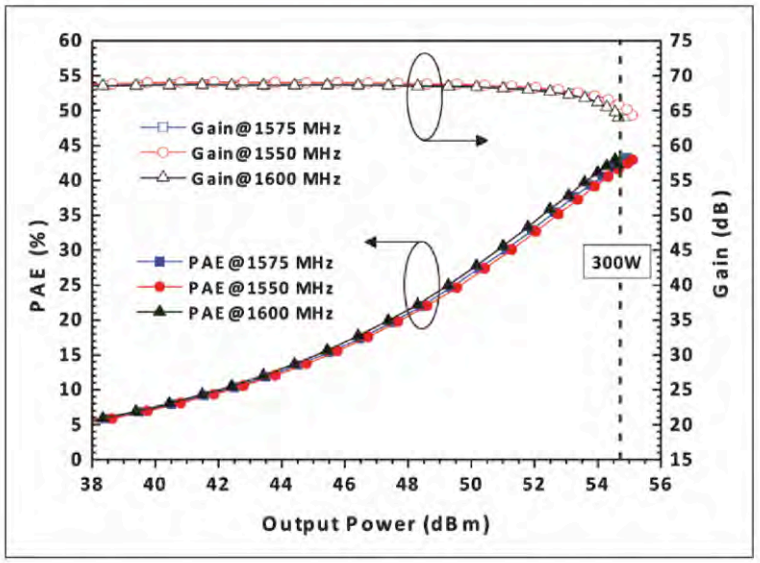

Figure 5. The power amplifier built in the SLOGAN project can produce an output in excess of 300 W at an efficiency exceeding 45 percent.

with low outgassing characteristics. Roger RT/duroid 6035HTC laminates were employed for the high-power section.

The three sub-units – the RF unit, power supply and electronic power conditioner – have been united in a power amplifier box (see Figure 4) to create a system with a mean-time-before-failure of almost 600,000 hours. This level of reliability implies a probability of failure during a useful life of 12 years of only 16.2 percent. Characterisation of this unit reveals that it can deliver a CW output exceeding 300 W at a power-added efficiency that is close to 45 percent (see Figure 5). The gain delivered by the unit is incredibly flat (see Figure 6).

Life testing also produces some impressive results. Operating in CW mode at 1575 MHz, with fixed input power of -11 dBm that correspondingly to roughly 2dB of compression, the output power is incredibly stable. It varies by less than 0.15 dBpp during 500 hours of operation. Moreover, the amplifier has been subject to vacuum tests, and no failures due to multipaction have been observed.

The SLOGAN team is still to complete its characterisation of the unit. During the next few months, the amplifier will undergo thermal cycles, and characterization of performance over temperature. If the results are anything like those realised in testing to date, they are sure to underscore the great potential of GaN HEMTs for space applications.

The SLOGAN project has received funding from the European Union Seventh Framework Programme for research, technological development and demonstration under grant agreement 606724.

To probe further
http://www.fp7-slogan.eu/
https://www.youtube.com/watch?v=9_PLYwOaCXM
https://www.linkedin.com/grp/home?gid=8128951&trk=my_groups-tile-grp
Twitter account (Slogan_FP7)

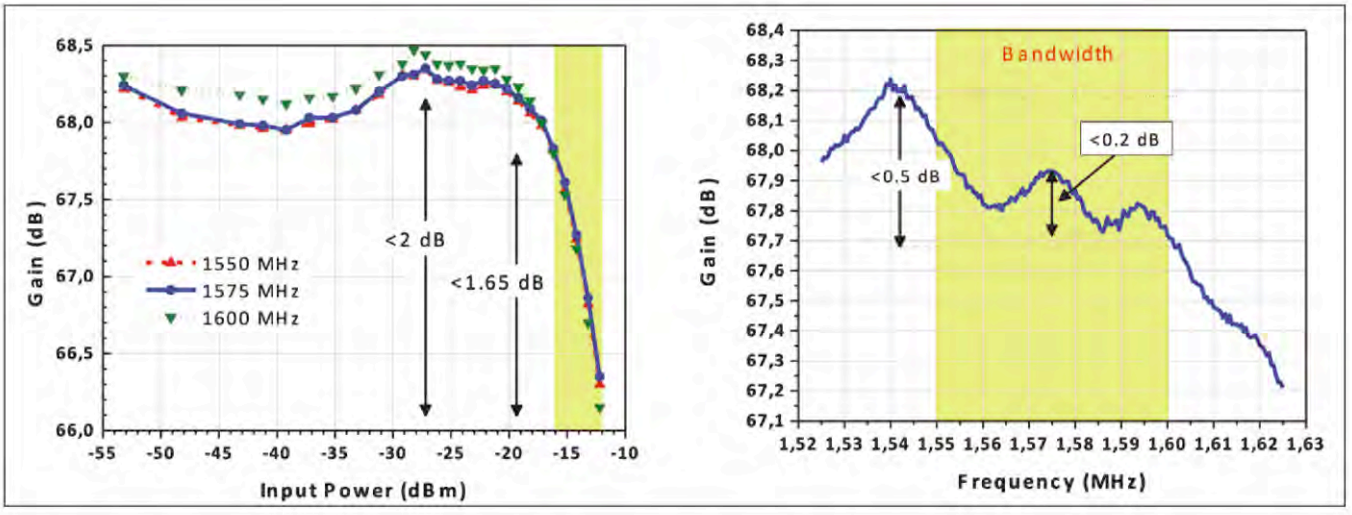

Figure 6. The gain of the SLOGAN power amplifier is incredibly flat. It is less than 1.6 dB in the range of -3 dB, +1 dB of input power back-off, and less than 0.2 dBpp over a 10 MHz frequency span.

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BOOSTING BRIGHTNESS WITH HOLLOW CAVITIES

GaN-based LEDs are more efficient and cost-effective when they contain an array of embedded hollow cavities in the sapphire substrate

BY DUKKYU BAE AND YONGJO PARK FROM HEXA SOLUTION

The LED industry is in the doldrums. There is a worldwide oversupply of LED chips and penetration is sluggish into the latest 'killer application', general lighting. Compounding the matter, the other major multi-billion dollar market, backlighting units for screens, is failing to grow at a healthy rate. As those within the industry increase LED performance to give their company an edge of their rivals, the number of chips required to backlight a screen falls – and with it, ironically, a fall in the volumes within this market.

Fortunately, there is some good news: the market for high-power LEDs, which typically produce 2-3 W, is expanding, and should continue to do so. With these devices – that are used in industrial lighting applications, such as fixtures in factories that are attached in high ceilings – a premium is placed on high efficiencies. That's because the higher the efficiency, the lower the heat dissipation, and ultimately, the simpler and cheaper the thermal management.

Given the state of the LED industry, it is of no surprise that many chipmakers are striving to increase the efficiency of their devices, and enjoy more success in the high-power sector that offers a higher profit margin. Even if these device makers only outperform their peers by a few percent, their superior efficiency will give them a considerable edge. This positions them to make good money, because a substantial proportion of profit margin comes from high-end LED chip production.

Another advantage of being able to produce very high efficiency devices is that if they also have a proven reliability, they can challenge for success in the automotive headlight sector. Where they will not have success, however, is in general lighting. Here, medium and low efficiency LEDs are being used, with the

many makers of these devices fighting for survival.

Extracting photons

One of the key requirements for an efficient LED is that it extracts a high proportion of the photons generated within it. Realising this is not trivial, because the refractive index of GaN is far higher than that of air, leading the majority of photons to be trapped inside the device by total internal reflection.

A common approach for overcoming this issue is to produce devices on patterned sapphire. A corrugated surface can scatter photons in many directions, increasing the probability for light to escape from the chip.

These substrates are formed by taking a piece of planar sapphire and etching a pattern into it with a photoresist mask and an inductively coupled plasma. With this process, the mask gradually erodes, leading to a dome-shaped surface. If cones are preferred, they can be formed by adjusting the etching conditions.

When light propagates through LEDs formed on patterned sapphire, it is reflected and diffracted, due to differences in the refractive index. The propagation of light undergoes the greatest change at interfaces with the most substantial difference in refractive index, which occurs at boundaries between GaN and air. Due to this, many research groups have tried to incorporate high-index-contrast cavity structures within their LED. This has been successful, with light extraction increasing, but up until now there have been no reports of the use of a production-level, cavity-forming process within the LED industry.

One of the research groups that have made a considerable contribution to cavity-incorporating LEDs is the team of Euijoon Yoon and co-workers from Seoul National University, Korea. After devoting several years to the fabrication of LEDs with nanometer-scale cavities, formed using hollow silica nanospheres, they have increased light extraction by incorporating a cavity within an LED. What's more, they have reduced wafer bow, thanks to relaxation of compressive stress in the GaN around the cavity. The implication is that thinner sapphire wafers can be used for LED manufacture, trimming production costs.

There is still room for improvement, however. The increase in light extraction is not as high as it could be, due to the low density of the hollow cavities and their random positions. These weaknesses must be addressed in order to create a better, more reliable cavity-forming process for LED manufacture.

From lab to fab

Addressing these weaknesses is one of the challenges that we have set ourselves at Hexa Solution Co., Ltd. of Korea. Our core technology is the cavity-engineered sapphire substrate, which we plan to sell to LED chipmakers. Several of them are

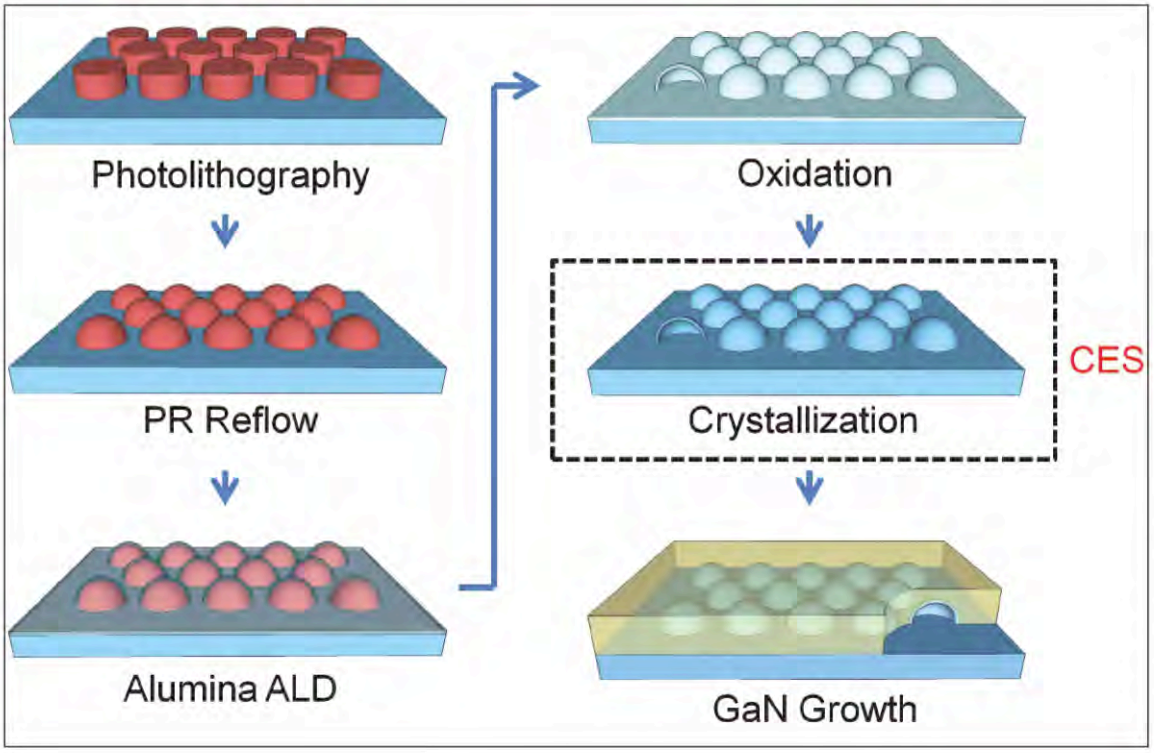

Figure 1. The manufacturing process for forming cavity-engineered substrates involves complete crystallisation of amorphous alumina, so that it turns into sapphire. This greatly simplifies subsequent growth of GaN.

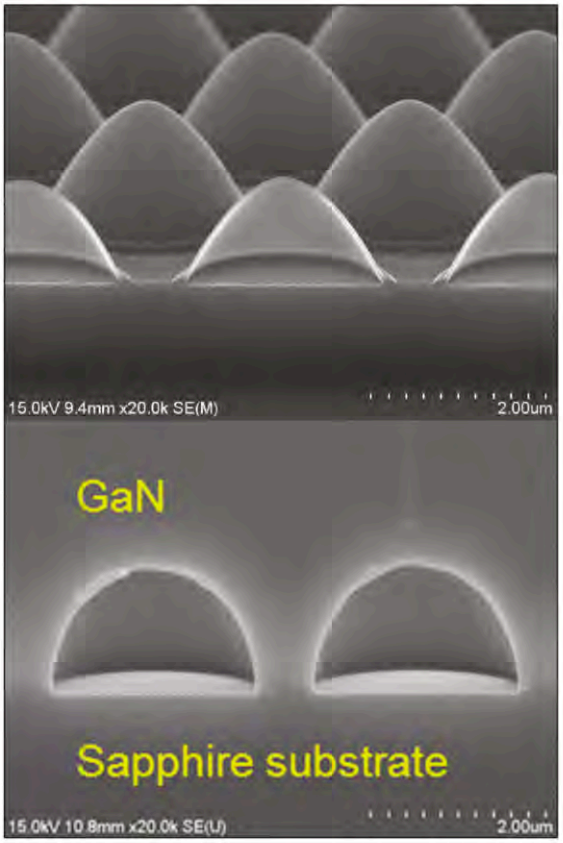

Figure 2. Scanning electron microscopy reveals embedded cavities of hexagonal domes formed after GaN growth.

currently evaluating our products, which they could either buy from us in volume, or produce themselves after licensing our technology.

Our technology originates in Yoon's group, but has been refined in a partnership between that team and another research group at the same university – the latter is based in the Energy Semiconductor Research Center, Advanced Institutes of Convergence Technology. Together, these two groups have carried out a feasibility study, with lab-scale production revealing that LEDs incorporating cavity-engineered sapphire substrates outperformed equivalents made on patterned sapphire.

In 2014, to spur its commercialisation, the cavity engineered sapphire substrate technology was transferred to our company. By the start of the following year, we had successfully prototyped 2-inch cavity-engineered substrates for initial pilot plant production, and since then we have made further progress. Highlights include shipment of 2-inch, 4-inch and 6-inch products to LED chipmakers throughout the world. They are currently evaluating our technology.

Our process for producing cavity-engineered sapphire substrates is robust and scalable (see Figure 1). It begins with photoresist patterning, which allows the shape of a cylindrical photoresist to be easily tailored to that of a dome by a reflow process. This is followed by atomic layer deposition of an 80 nm-thick amorphous alumina layer at 120 °C over all the exposed surface. The alumina partly covers sapphire, and partly covers the photoresist.

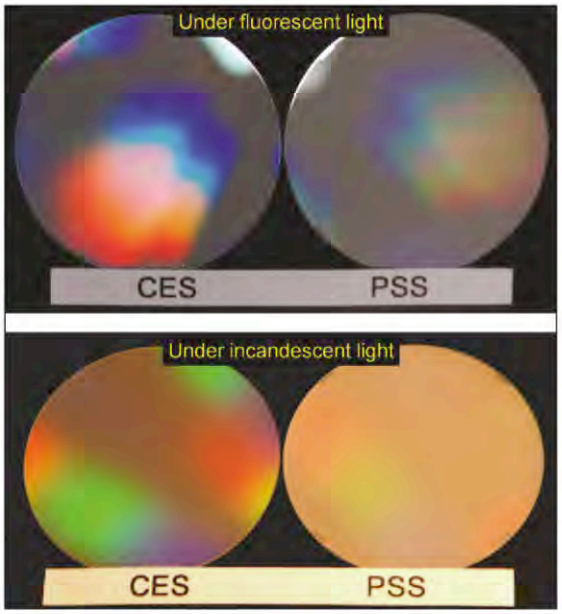

Figure 3. Stronger diffraction in cavity-engineered sapphire, compared with patterned sapphire, leads to brighter colours under illumination.

The next step is thermal treatment in an oxidation atmosphere. This allows in-diffusion of oxygen through the porous alumina layer and out-diffusion of the oxidation by-product. The result: the creation of dome-shaped cavities.

At the same time, the amorphous alumina becomes completely crystallized. This starts at the sapphire-contacting area, and is completed at the apex of the dome over the photoresist. A very pleasing aspect of this process is that the crystalline phase of amorphous alumina is sapphire. Consequently, since alumina is crystallized to sapphire during thermal treatment, there is no need for additional processing steps to expose the sapphire seed layer and initiate GaN growth (see Figure 2 for a cavity-engineered sapphire substrate with a two-dimensional hexagonal cavity array, and a preserved cavity after GaN growth).

A great strength of our cavity-engineered substrates is their unique optical properties. They produce strong

interference, leading to a range of colours that can be seen by the naked eye. Compared to patterned sapphire, more vivid interference colours are produced under both incandescent and fluorescent illumination, thanks to strong diffraction by the cavity (see Figure 3).

Experimental and theoretical investigations into the strong diffraction produced by our substrates have been undertaken by Sun-Kyung Kim's research group at Kyung Hee University, Korea. Their work included careful transmission experiments, which revealed that cavity-engineered sapphire produces higher transmission than patterned sapphire over a wide range of wavelengths.

A key insight provided by the finite-difference time-domain simulations of the team of Sun-Kyung Kim is that the high-index-contrast cavity interplays very strongly with the in-coming plane waves. The upshot is that the cavity is effective at changing the propagation direction of the light (See Figure 4).

Another consequence of the air cavity is that it acts as an optical disturbance against the plane waves, imparting significant phase distortion inside and outside the structure. The array of embedded air cavities is able to extract more light out of the LED, because each individual air cavity generates a strong secondary wave, according to Huygens' principle. Light generated within the LED interacts strongly with the high-index-contrast cavity array, so, rather than being trapped by total internal reflection – as it would be in a conventional device – it leaves the chip, due to interaction with the periodic array of cavities. Or to put it another way, the light is diffracted (see Figure 5 for finite-difference time-domain simulations that clearly visualize that the cavity-engineered sapphire substrate is better than patterned sapphire at extracting light out of the chip, particularly under total internal reflection conditions).

Proven performance

To demonstrate the superb performance of lateral and flip-chip LEDs on cavity-engineered sapphire, compared with those formed on patterned sapphire, we have partnered with Semicon Light Co., Ltd. Korea. Together we have simultaneously produced device epistructures on the two types of substrate in an MOCVD reactor. Following this, both wafers were processed concurrently to produce large-area, lateral-type blue-emitting InGaN/GaN LEDs with dimensions of 1075 μm by 750 μm.

The features in both types of sapphire were markedly different. The cavity-engineered sapphire contained hemispheres 1.5 μm high and 2.4 μm in diameter,

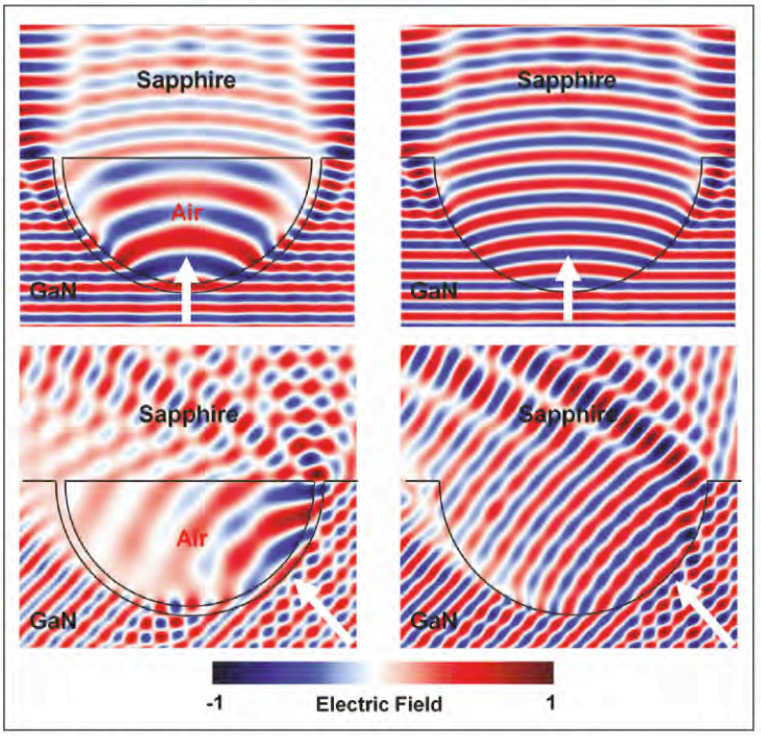

Figure 4. Finite-difference time-domain simulations show that there is stronger scattering in cavity-engineered sapphire than patterned sapphire. Plane waves with an incident angle of 0° (top) and 45° (bottom) are used in the simulations.

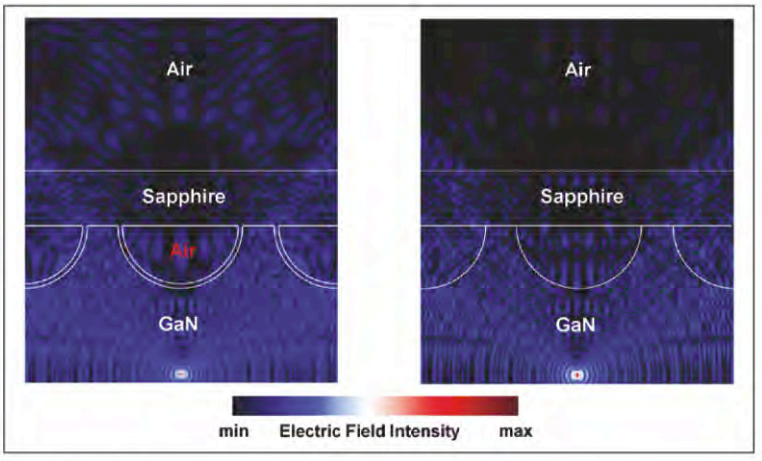

Figure 5. Finite-difference time-domain simulations show that LEDs incorporating cavity-engineered sapphire are more efficient at extracting light than equivalents with a patterned sapphire foundation.

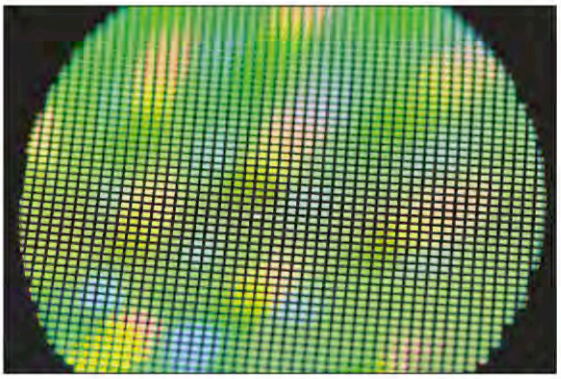

Figure 6. Lateral LEDs, with dimensions of 1075 μm by 750 μm, incorporating cavity-engineered sapphire technology.

while the cones on the patterned sapphire were 1.7 μm high and 2.7 μm in diameter. LED chips were diced from these wafers (see Figure 6), with individual chips mounted on the same package.

Measurements of optical power, using a standard integrating sphere, showed that the power produced by LEDs on cavity-engineered sapphire were typically significantly higher than those made on patterned sapphire (see Figure 7). Collecting spectra of individual LED chips, driven at 240 mA, revealed that those made on cavity-engineered sapphire deliver peak emission at 468 nm, and produce optical power almost 40 percent higher than variants formed on patterned sapphire. Devices grown on cavity-engineered sapphire that emit dominant wavelengths of 456 nm and 462 nm also outperformed cousins on pattern sapphire, but by a smaller margin (see Figure 8).

A great virtue of our cavity-engineered technology is that the surface of our substrates is made entirely of sapphire. This means that the chemical reactions associated with MOCVD growth are identical to those for planar and patterned sapphire. Although a slight adjustment in growth temperature might be needed to optimise device performance, no significant alternation to the manufacturing process is required to adopt our technology, and to produce more competitively priced LEDs.

Lower prices, compared to LEDs made on patterned sapphire, stem from a lower-cost process. Patterning

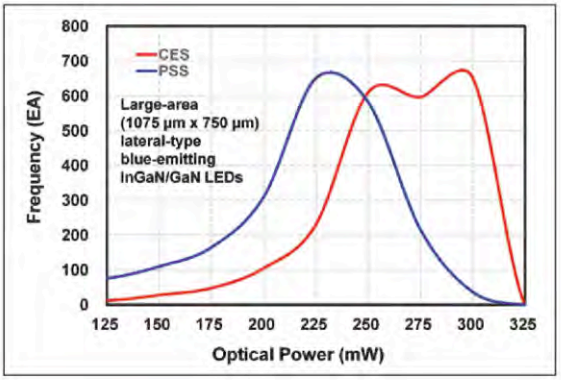

Figure 7. The optical power distribution of batches of LEDs produced with cavity-engineered sapphire and patterned sapphire technologies.

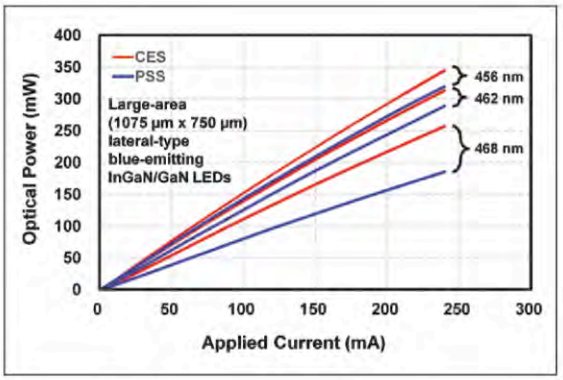

Figure 8. LEDs incorporating cavity-engineered sapphire produce more power than those formed with patterned sapphire at the three dominant wavelengths of 456 nm, 462 nm and 468 nm.

sapphire by plasma etching is relatively expensive, due to the incredible hardness of sapphire, which leads lengthy etching times under harsh conditions. Making matters worse, yields for patterned sapphire are unsatisfactory. In comparison, a batch of cavity-engineered sapphire substrates can be mass-produced using a combination of a more stable, less expensive atomic layer deposition process and thermal treatment in a furnace.

We are confident that in the next few years our cavity-engineered sapphire substrates will form the foundation for a new generation of high-performance LEDs. We have proven that they can deliver a significant increase in light extraction in lateral LEDs, and we anticipate that the benefits will be even greater in more powerful flip-chip designs. Here the distance between the bottom mirror and the active layer is comparable to the wavelength of light, so it is possible to exploit resonant cavity effects. We are exploring this opportunity with Semicon Light Co., Ltd. through a joint development of silver-free, flip-chip, cavity-engineered sapphire LEDs.

Other exciting opportunities of our technology include the fabrication of ultrathin sapphire membranes. These could be used for less defective GaN growth and the mechanical lift-off and bonding of individual processed, dicing-less LED chips on to arbitrary substrates, including those that are flexible. Our technology is clearly in its infancy, and has a great deal to offer in helping to rejuvenate the LED industry.

Further reading

J. Kim *et. al.* Scientific Reports **3** 3201 (2013)
J. Jang *et. al.* J. Cryst. Growth **430** 41 (2015)
D. Moon *et. al.* J. Cryst. Growth **441** 52 (2016)
Y.-J. Moon *et. al.* Nano Lett. **16** 3301 (2016)

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Creating and strengthening links between chipmakers and network builders

Slashing the cost of the GaN substrate

Production of affordable, high-quality GaN substrates could result from HVPE of GaN on a native surface

BY MALGORZATA IWINSKA FROM THE INSTITUTE OF HIGH PRESSURE PHYSICS, POLISH ACADEMY OF SCIENCES

IMAGINE, for a moment, that you could make thousands of substrates from a high-quality GaN boule just a few millimetres thick. Such a feat is conceivable, requiring resulting wafers to be as thin as 150 nm.

Armed with this incredibly thin, very high-quality substrate, you would have the potential to revolutionise GaN chip production. Thanks to homo-epitaxy, the quality of the epilayer would match that of its foundation, making this approach ideal for growing of bulk GaN and for the production of high-quality devices. Note that these substrates would be in high demand, as alternatives to GaN are not an option for the manufacture of GaN lasers and vertical high-power transistors, because they lead to imperfections that degrade device performance.

Unfortunately, such substrates are just a dream for today's chipmakers, who must make do with GaN substrates that are pricey, limited in availability, and have a quality that depends on the retail price. If they want the best material, they must seek substrates produced by the ammonothermal method, but diameters are limited to 2-inch. HVPE can provide cheaper substrates with diameters of up to 4-inch, but crystallographic quality is far worse.

What is encouraging, however, is that in the research community, a GaN layer just 150 nm-thick has been used to form a free-standing, 1 mm-thick HVPE-grown GaN crystal. This triumph has been achieved by our team at the Institute of High Pressure Physics, Polish Academy of Sciences, working within a European project called the Development of Advanced GaN substrates & Technologies (AGATE). This effort, led by the French firm Soitec, a worldwide leader in engineering substrates, opens a new path to the production of GaN substrates and the multiplication of high-quality GaN crystals.

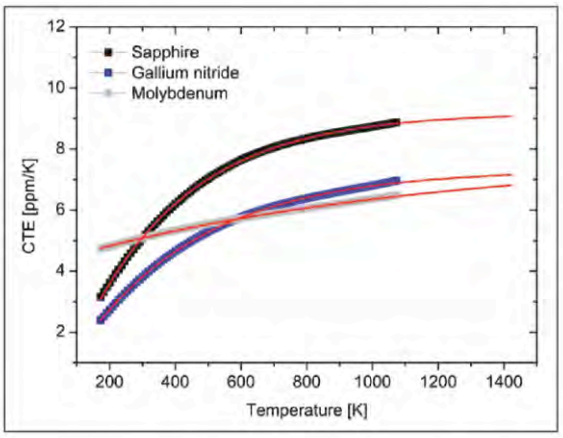

Figure 1. In terms of the coefficient of thermal expansion, molybdenum is a far better match for GaN than sapphire. Red lines are a fit performed and extrapolated to higher temperatures (courtesy of M. Seiss, Plansee).

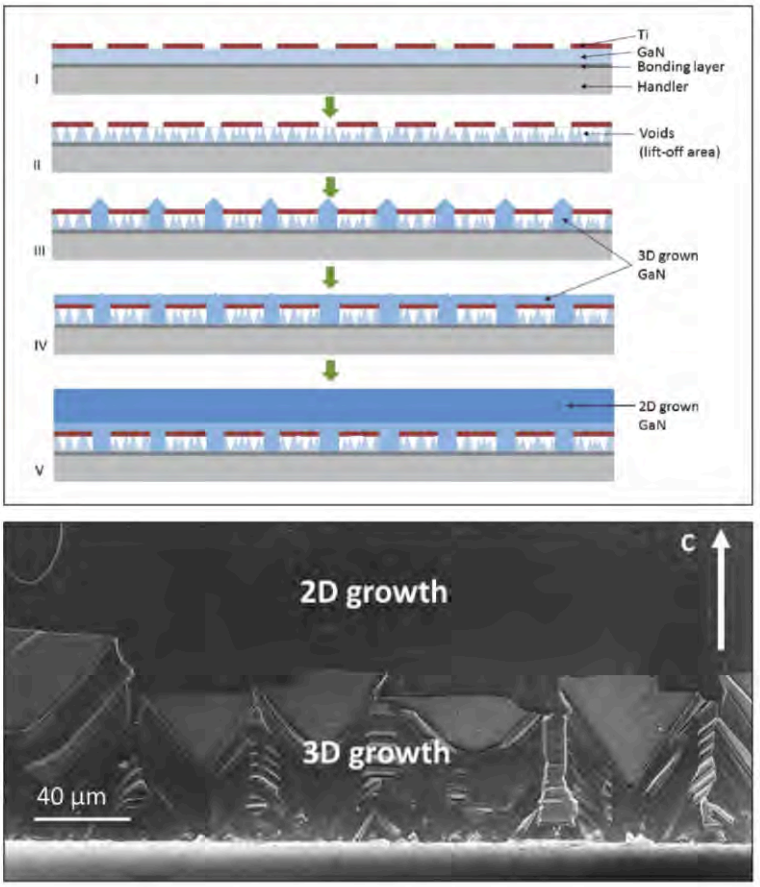

Figure 2. (top) The HVPE process used by the team from the Institute of High Pressure Physics, Polish Academy of Sciences, involves: I, forming an opening in a titanium mask; II, decomposing a GaN layer beneath the mask to form voids (this is critical for subsequent self-lift-off); III, three-dimensional GaN growth in openings in the mask – pyramids appear above the titanium mask; IV, coalescence of GaN, involving three-dimensional growth; and V, two-dimensional growth of GaN after full coalescence. (bottom) A cross-sectional scanning electron microscopy image of GaN that has been grown on a mask by HVPE.

The GaN-based substrates that we use for our work, which have diameters that can reach 6-inches, are prepared by Soitec. These advanced substrates are similar to that of a template, but they have a unique feature – a very thin GaN layer that has been separated from starting material by ion implantation.

Today, the origin of this GaN layer is an MOCVD-grown, GaN-on-sapphire template. But this advanced substrate can be improved by turning to high-quality GaN wafers as the starting material. If this route is

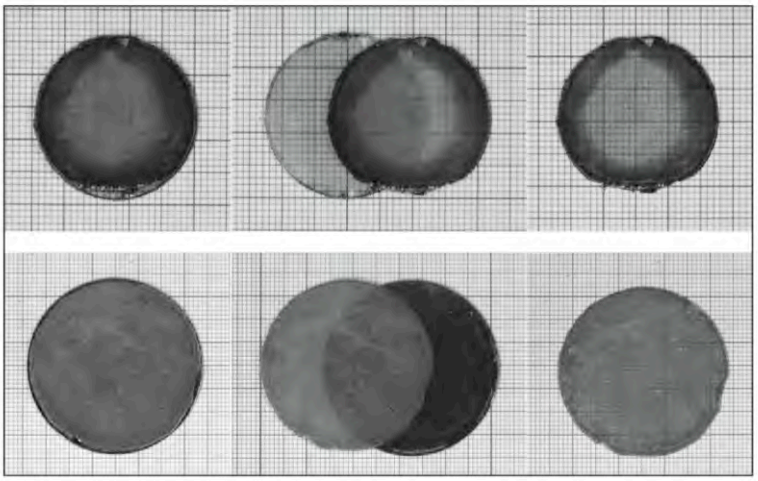

Figure 3. Free standing, HVPE-grown GaN from: (top) a 1-inch, GaN-on-sapphire seed and (bottom) a 1.5-inch, GaN-on-molybdenum seed.

taken, the final product is no longer limited by the quality of the GaN grown on a different foundation.

To create an advanced substrate, a silicon-oxide-based layer is used to bond GaN to a new handler that is just a few hundred microns thick. Governing the selection of the handler are the desired properties of the advanced substrate. There are many different possibilities for the handler, and we have chosen two kinds of Ga-polar advanced substrates as seeds for our HVPE growth. They are the relatively common combination of GaN-on-sapphire, and the more esoteric pairing, GaN-on-molybdenum. We have chosen molybdenum because it has a very good thermal match to GaN (see Figure 1 for the thermal coefficients of GaN, sapphire and molybdenum).

The HVPE method that we use to deposit GaN involves crystallization from the gas phase. At relatively high temperatures, such as 1100 °C, gallium chloride reacts with ammonia to form GaN.

We are by no means alone in using HVPE to create layers of GaN. Due to a lack of native GaN, often the starting point is a foreign wafer, such as an MOCVD-grown, GaN-on-sapphire template. The downsides of working with foreign wafers are the mismatches in lattice constants and thermal expansion between the seed and the crystallized material. These differences lead to significant strain, and cracking can result when the thickness of the layer exceeds a few hundred microns.

One way to minimize this stress is to intentionally introduce voids and create a rough layer at the onset of growth. To realise this and promote three-dimensional growth, the seeds must be specially prepared prior to HVPE growth.

We have done this, depositing a 20 nm-thick titanium mask on the GaN layer, and then using photolithography to create round openings with sizes of 3-10 μm, separated by 9-16 μm. A great strength of this approach, which is similar to the void-assisted separation technology developed at Hitachi Cable, is that it can form un-cracked GaN crystals via a self-lift-off process.

With our approach, the surface of the processed wafer is prepared for growth by controlling the decomposition of the GaN layer beneath the titanium mask. Get this right and GaN can deteriorate in a uniform, non-excessive manner across the entire surface. Once this is accomplished, growth begins, with GaN initially crystallizing in the openings of the

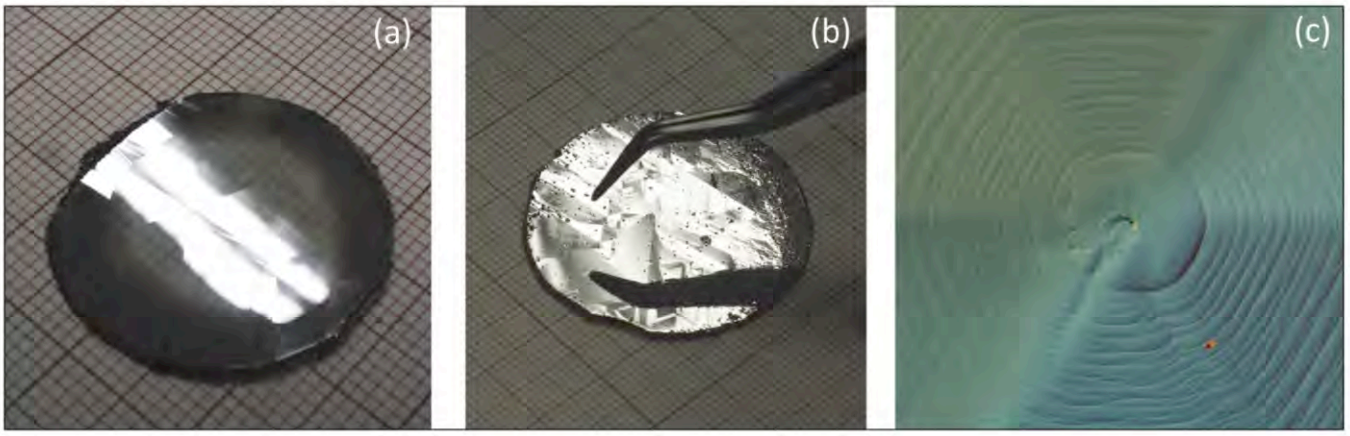

Figure 4. (a) A free-standing, as-grown crystal from a 1-inch GaN-on-sapphire seed, with a hillock visible on the surface. (b) A free-standing, as-grown crystal from 1.5-inch GaN-on-molybdenum seed, with many hillocks on the surface; pits visible on the surface are shallow and are removed during surface preparation. (c) A differential interference contrast image of the morphology. The hillock growth mode and macrosteps are visible on the side of the hillock.

mask, before pyramids start to appear. Coalescence of GaN then takes place above the titanium layer, with growth proceeding in a three-dimensional mode until full coalescence.

At that point in the growth there is a switch to a two-dimensional mode, with macrostep flow. This occurs on either the entire surface, or from the centres of hillocks already formed on the surface. Initially, the surface contains a large number of hillocks, but they 'consume' one another to create a surface with either just one of them, or possibly a few.

The crucial step in this entire process is the decomposition of the GaN layer. It is this that creates the voids between the seed and the new-grown material, and ultimately enables the self-lift-off process during wafer cool down. The quality of the HVPE crystal is also influenced by three-dimensional GaN growth. This creates layers that can realise a relatively low threading dislocation density, because dislocations can propagate in directions other than that of the growth.

As our HVPE reactors are designed to accommodate seeds with diameters of up to 2-inch, we have prepared 1-inch and 1.5-inch samples from 4-inch GaN-on-sapphire and GaN-on-molybdenum wafers. After placing a mask on the GaN surface, we have used HVPE to grow GaN layers with a thickness of up to 1 mm. Finally, we prepared substrates for epitaxy from the obtained crystals.

Visual inspection of these crystals reveals that they are crack-free (see Figure 3), implying that the self-lift-off process occurred during the cool-down phase. As expected, the crystals have the desired *c*-plane growth morphology. Hillocks, with macrosteps flowing from their sides, provide the growth centres.

Etching the surfaces of these samples enabled an estimate of the threading dislocation density. In both types of seed, this density is typically 5×10^8 cm^{-2}; while in HVPE-grown crystals, the threading dislocation density is far lower, never exceeding 1×10^7 cm^{-2}.

We have scrutinised the structural properties of our crystals by X-ray diffraction. For GaN-on-molybdenum, the full-width-at-half-maximum for the rocking curve of the symmetric (002) reflection is 380 arcsec, and for GaN-on-sapphire it is just 180 arcsec. Both these values are much smaller than those for the used seeds: 645 arcsec for GaN-on-sapphire, and 755 arcsec for GaN-on-molybdenum.

In the absence of intentional doping in the growth process, the crystals have a very low level of impurities. The main dopant, oxygen, has a content

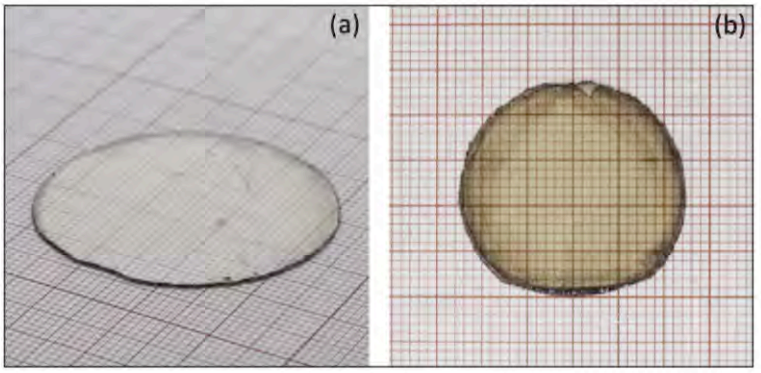

Figure 5. Wafers prepared from HVPE-grown GaN, grown on: (a) a 1.5-inch, GaN-on-molybdenum and (b) a 1-inch GaN-on-sapphire.

below 10^{17} cm^{-3}, leading to a comparable value for electron concentration.

For optoelectronic devices, and electronic ones with a vertical conduction path, an increase in the free-carrier concentration is required. We achieve this by doping with silicon, a process performed on a 1-inch GaN-on-sapphire seed. HVPE growth produced 300 μm of undoped GaN, followed by 500 μm of GaN that is doped with silicon. A free-standing crystal containing both of these layers is created by self-lift-off.

The characteristics of our doped wafer include a threading dislocation density in the doped material of 7×10^8 cm^{-2}, and a concentration of silicon of $5\text{-}7 \times 10^{18}$ cm^{-3}, according to secondary ion mass spectrometry. The presence of silicon increased the free-carrier concentration, with Raman spectroscopy

“We have scrutinised the structural properties of our crystals by X-ray diffraction. For GaN-on-molybdenum, the full-width-at-half-maximum for the rocking curve of the symmetric (002) reflection is 380 arcsec, and for GaN-on sapphire it is just 180 arcsec”

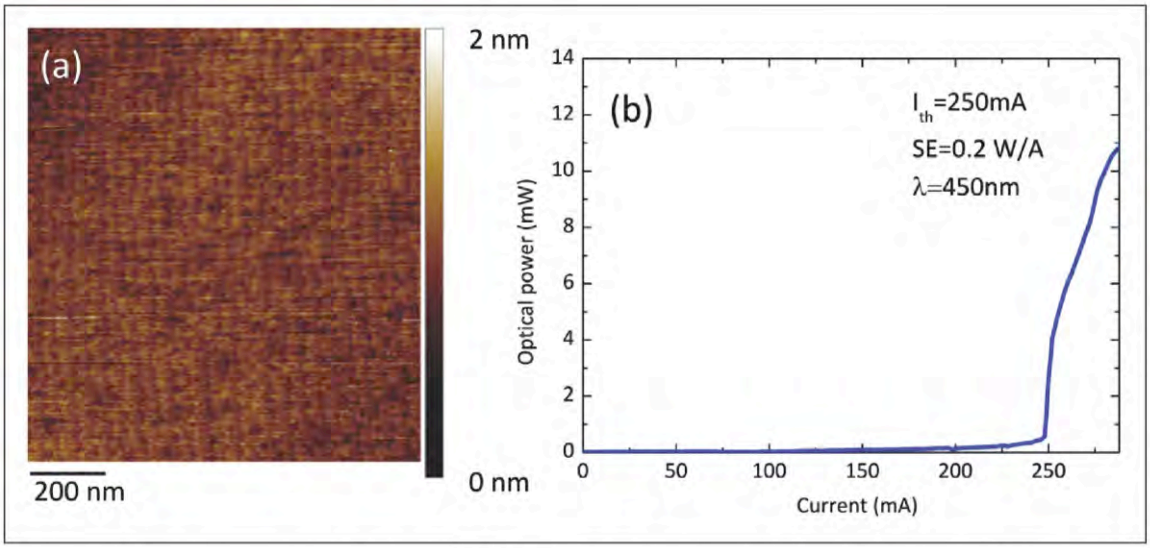

Figure 6. (a) An atomic force microscopy image of a HVPE-grown, silicon-doped GaN substrate. The root-mean-square surface roughness is 0.146 nm (courtesy of A. Feduniewicz-Zmuda, IHPP PAS). (b) Light-current characteristics of a laser diode formed on HVPE-GaN, grown on GaN-on-sapphire (courtesy of C. Skierbiszewski, IHPP PAS).

indicating a value of 4 x 10^{18} cm^{-3}, and verification from Hall measurements suggesting 5.7 x 10^{18} cm^{-3}. Substrates with this level of free-carrier concentration are suitable for making laser diodes.

We have produced wafers from our GaN crystals (see Figure 5 for examples). They include a doped wafer that is a suitable foundation for making a laser diode. This wafer's Ga-polar face has been treated by mechanical and chemo-mechanical polishing to provide a surface suitable for epitaxy. According to atomic force microscopy, the surface has bilayer steps, and a root-mean-square roughness of 0.146 nm (see Figure 6). Note that the equivalent figure for the GaN starting layer is 0.197 nm.

A 450 nm, CW laser has been formed via MBE growth on our doped substrate. This device has a threshold current of 250 mA and a slope efficiency of 0.2 W/A. These values are not as good as those of commercially available devices, but that could be due to the design of our heterostructure, which was a novel architecture under evaluation.

Our work, which is on-going, is an important step towards the fabrication of affordable, high-quality GaN substrates. We have shown that by starting with advanced substrates, formed with Soitec's Smart Cut technology, HVPE can be used to grow thick layers of GaN, which have a crystal quality that is superior to that of the starting layer. Although the handler materials that we have used – sapphire and molybdenum – were selected for their similar thermal expansion and lattice constant parameters to GaN, even high crystal quality and better devices should result from using a GaN handler.

That approach is our ultimate goal. It will involve separation and transfer of GaN layers from high-quality GaN crystals to a GaN handler of lower quality, such as free-standing GaN that is grown on the likes of an MOCVD-grown, GaN-on-sapphire template. We are already laying the foundation for this, with the production of 2-inch high-quality, HVPE-GaN (see Figure 7). This is an attractive approach that we will pursue to multiply the number of high-quality GaN substrates.

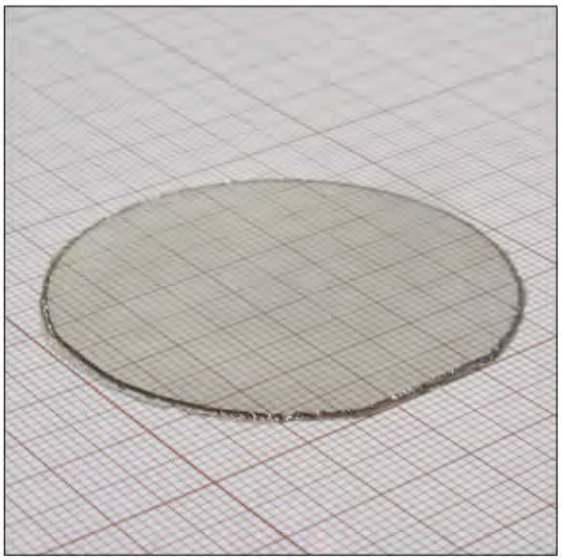

Figure 7. 2-inch, free-standing HVPE-grown GaN with a high crystal quality. The threading dislocation density is only 5 x 10^{4} cm^{-2}.

Further reading

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M. Bockowski and Z. Sitar, Compound Semiconductor, July 2014
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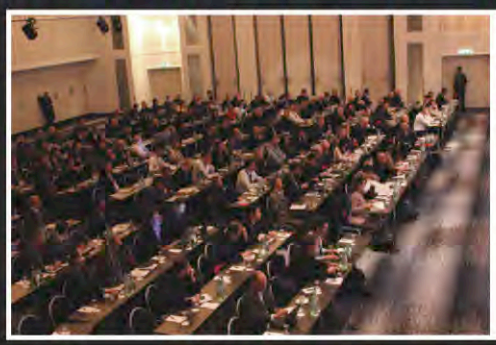

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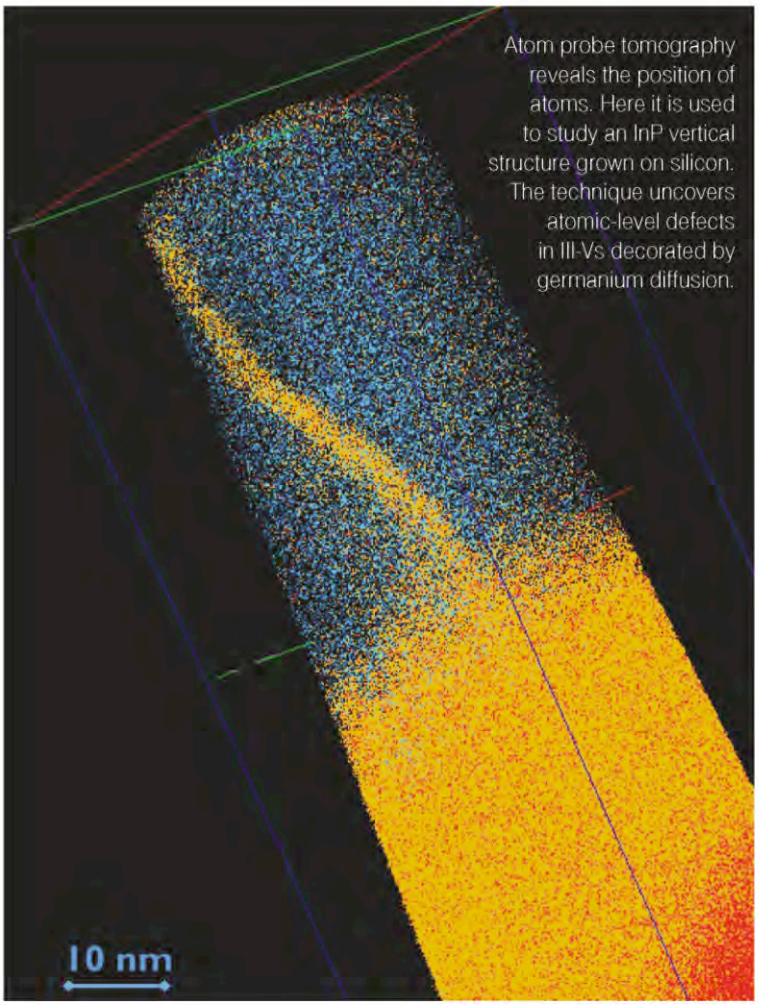
TUNNEL FETs:

The key to greener microprocessors

Increasing the indium content in the InGaAs channel boosts the drive current of a tunnel FET while maintaining its great switching behaviour

BY ALIREZA ALIAN AND AARON THEAN FROM IMEC



Atom probe tomography reveals the position of atoms. Here it is used to study an InP vertical structure grown on silicon. The technique uncovers atomic-level defects in III-Vs decorated by germanium diffusion.

IF THE SILICON INDUSTRY keeps pace with Moore's law, the state-of-the-art microprocessors of the 2020s will contain hundreds of billions of transistors packed onto a chip no bigger than a postage stamp. This is a staggering hike in transistor count since the birth of the IC, taking their number to a level that is comparable to that of neurons in the human brain.

However, due to circuit energy dissipation and power budget constraints, it may not be possible to switch all the transistors most of the time. Instead, much of the silicon may remain dark – that is, not all the devices can switch together at once due to power limits, so a lot of them should remain off while only part of them are operational at any given time. The solution is the introduction of a more energy-efficient switch.

The origin of substandard efficiency is an inherent weakness of the MOSFET, the workhorse switch for the chips of today. This class of transistor forms a far from ideal switch, with a steepness of switching action – known as the sub-threshold swing – that is quite far from abrupt.

Making matters worse, the sub-threshold swing deteriorates with scaling, because as the gate and channel get shorter, there is diminishing control of electrons via the field-effect. Unwanted consequences result, including increased leakage and challenges that arise that are associated with lowering the operating voltage, which is needed to cut the power-consumption per transistor.

To address all these issues, the silicon industry has

switched from a single-gated planar transistor to a double-gated vertical MOSFET that is also known as a FinFET. This move to a three-dimensional device architecture has delivered two significant benefits: it has improved the sub-threshold swing; and it has enabled the chip's operating voltage to drop below 1 V while maintaining its performance [1].

Another merit of the switch from a planar device to a FinFET has been a trimming of transistor leakage. This move to 'greener' transistors must continue, because chip power non-scalability is becoming by far the biggest concern surrounding the future for energy-conscious electronics [2,3].

The MOSFET limit

For the regular MOSFET, there is a fundamental limit to the sub-threshold swing – at room-temperature, it can't fall below 60 mV/decade (at this value, changing current by a decade requires a 60 mV shift in gate voltage). Far lower sub-threshold swings can be reached, however, by moving to different classes of transistor, including the tunnel FET(TFET) (see Figure 1).

Many research groups have fabricated this form of transistor. There has been some success to date, including a demonstration of steep switching in a silicon-based TFET [4]. However, no reports have emerged of a circuit made with these devices. To date, the steeper swing in the TFET comes at the expense of a low drive current, which is exacerbated when the device is operated below 0.5 V. To address this, the tunnelling resistance has to be trimmed while increasing gate action as much as possible, so that these devices can switch at reasonably fast speeds.

Success on this front requires the introduction of a new semiconductor material. The ideal candidate has to combine a high mobility and small bandgap, because this will deliver a hike in drive current via an increase in the tunnelling rate, which governs current capacity. Amongst the options for improving the TFET, the compound semiconductor material system offers great potential.

Unfortunately, turning promise into a reality is far from simple. For starters, it is far more challenging to process and build III-V devices than it is to make them with the more mature silicon CMOS material systems. And making the situation even harder, on top of the many challenges of designing and engineering III-Vs, TFETs are fundamentally more sensitive to material defects. These imperfections in the crystal lattice result from broken atomic bonds, which may

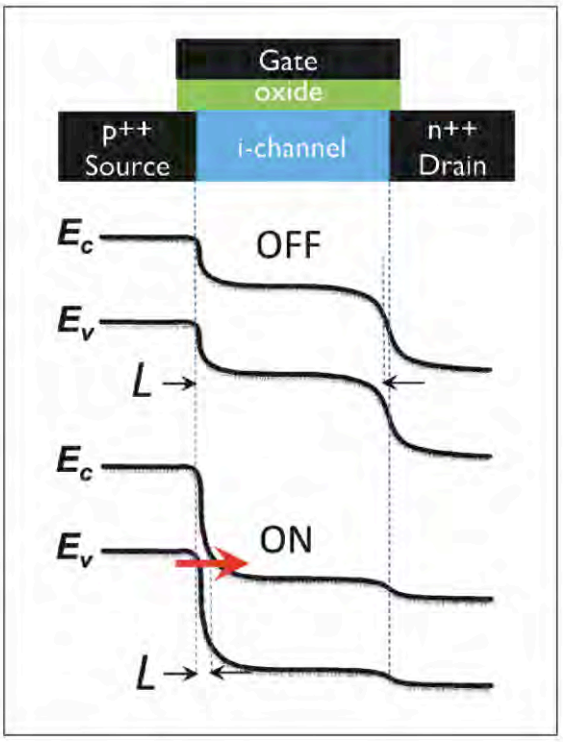


Figure 1. TFET operation for an *n*-type device with a *p*-type source and an *n*-type drain. The gate voltage in the off state is such that the tunnelling distance, *L*, is large, and no current flows through the device. A positive gate voltage bends the bands in the channel, shrinking the tunnelling distance *L*. This allows tunnelling to start and current to flow. The doping in the source is usually high because this creates a steeper band bending in the on state and boosts the current, thanks to a narrower tunnelling distance *L*. A smaller bandgap trims the tunnelling barrier height, while a higher mobility means lighter carriers. These modifications increase the tunnelling rate and consequently boost the drive current. Note that E_c and E_v denote conduction and valence band edges respectively.

exist in the form of extended line structures that span regions in the crystals and create electron traps. These imperfections may occur at interfaces between different materials, or in the bulk volume of the device – and they may be occurring naturally, or induced during device processing.

A major drawback of these imperfections is that they lead to trap-assisted-tunnelling, which hampers a steep sub-threshold swing. This tunnelling process – occurring in parallel with the favourable direct band-to-

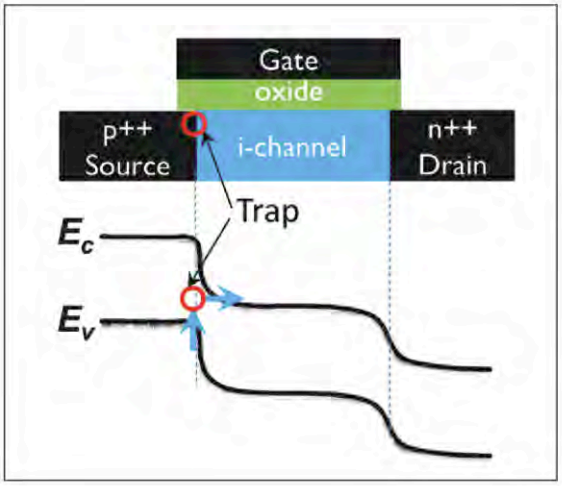


Figure 2. Trap-assisted tunnelling: In an ideal TFET, as shown in figure 1, electrons only tunnel directly from one band to another; however, in the presence of traps within the bandgap and in the tunnelling region, electrons can be thermally excited into the trap and then tunnel into the conduction band (note that the inverse is also possible, such as tunnelling into a trap and thermal excitation into the band). This has a detrimental impact on the sub-threshold swing, because it creates a parallel parasitic current that destroys steep switching. Since the process involves thermal excitation into a trap, it is strongly temperature dependent, which means in the presence of a significant amount of trap-assisted tunnelling, the sub-threshold behaviour of the current-voltage characteristics will be significantly changed with temperature, as demonstrated in figure 5.

band tunnelling process – takes place at the tunnelling junction, which is located at the source-channel junction (see Figure 2). The implication is that the performance of the TFET is governed by the quality of the source-channel junction and its local interface with the gate oxide.

Trap-assisted-tunnelling has been a significant impediment to realizing steep switching in all forms of TFET. Its signature is a variation in the device's input characteristics – that is, the change in drain current with gate voltage at a range of temperatures – when the transistor is operated above the off-state leakage current. When trap-assisted-tunnelling is absent, these characteristics are almost temperature independent; but when they are there, the variations with temperature are easy to spot (see Figure 3).

In late 2013, a group from the University of Tokyo reported a breakthrough in InGaAs TFET performance. They produced negligible trap-assisted-tunnelling, thanks to a novel approach for fabricating the source of the device, where tunnelling takes place [5]. The source is formed by diffusing zinc from zinc-doped spin-on-glass. Note that the use of zinc is common, as it is widely used for *p*-doping InGaAs layers. In the case of the TFET, zinc diffusion creates a highly *p*-doped source, and a clean source-channel junction with low defectivity.

One downside of the work by the Tokyo team is that their device had other weaknesses. Despite negligible trap-assisted-tunnelling, their device is still not able to produce sub-threshold swing below 60 mV/dec, possibly due to non-optimized design or other non-idealities.

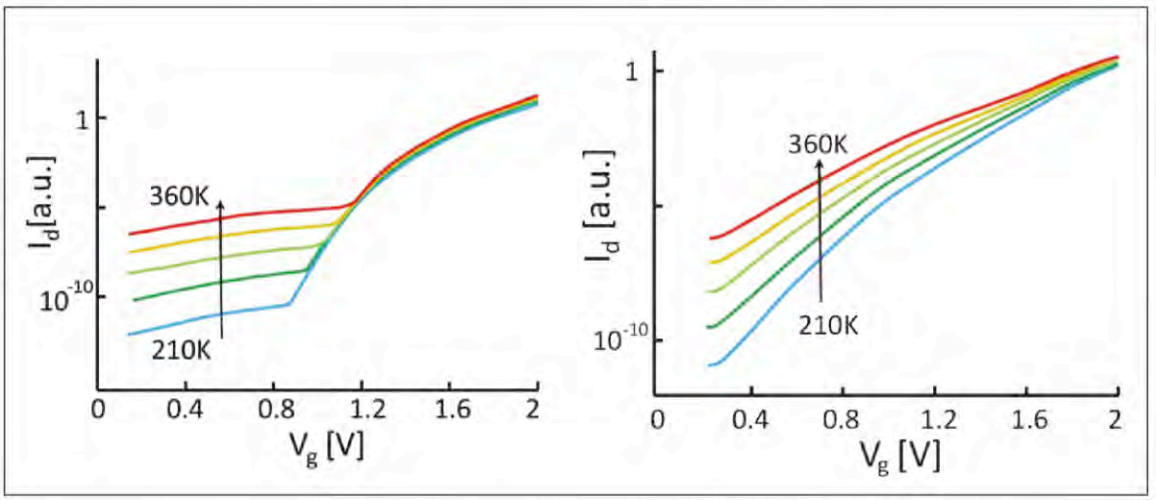


Figure 3. The temperature-dependence of current-voltage can expose trap-assisted tunnelling. The graph on the left shows a simulation of TFET behaviour without trap-assisted tunnelling. The device behaviour above the leakage floor is temperature independent. The leakage floor is dominated by the Shockley-Read-Hall process, so it is strongly temperature dependent (see Noguchi *et. al.* , IEDM 2013, for an example of experimental device behaviour of this kind). The graph on the right shows a simulation of the TFET behaviour with trap-assisted tunnelling. The behaviour varies significantly with temperature, which is the signature of substantial trap-assisted tunnelling.

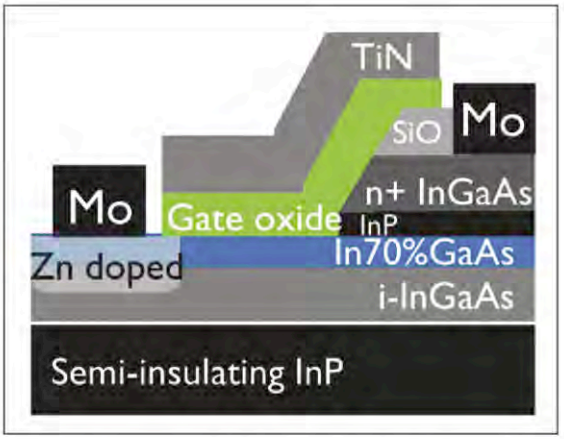


Figure 4. Increasing the indium content in the channel from 53 percent to 70 percent improves device performance. Experimental details, as well as the process flow, can be found in [6].

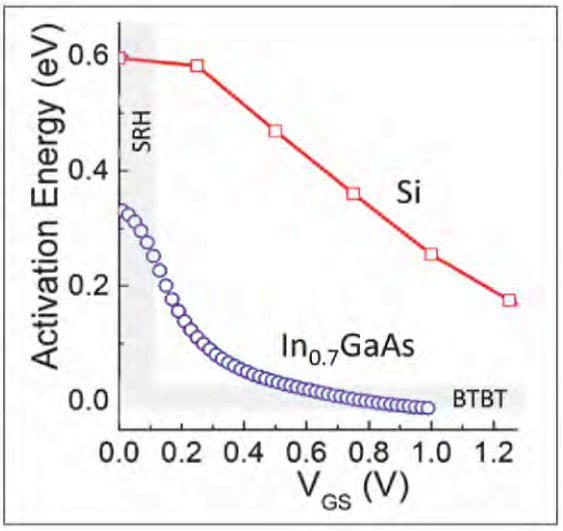


Figure 5. Activation energy varies with gate voltage. The plot is obtained from measurements of current-voltage at temperatures from 77K to 400K. In the off state, the activation energy is around half the bandgap – this is the signature of a Shockley-Read-Hall-dominant process. The low activation energy is advantageous, leading to low variations with temperature. This is a signature of dominance of a band-to-band-tunnelling process. A sharp transition step from band-to-band-tunnelling to Shockley-Read-Hall processes reveals that there is little trap-assisted tunnelling. Also shown is an example of a silicon-based device with a significant amount of trap-assisted tunnelling, characterized by a gradual transition between the two processes.

Increasing indium

Our team at imec are admirers of the work of this group from Tokyo. We are using the zinc diffusion process for our study of III-V TFETs, because we believe that this *p*-doping process is the most promising way to date to realize negligible trap-assisted-tunnelling in this class of devices.

To increase the TFET's drive current, which is its Achilles heel, we have made two modifications: we have introduced a 8 nm-thick $In_{0.7}Ga_{0.3}As$ layer in the channel, and we have developed a self-aligned diffusion process to trim the gate-source overlap (see Figure 4).

The device that results produces very little trap-assisted-tunnelling. This is seen in the small variations with temperature of the device's input characteristics above its off-state leakage current (see Figure 3 for simulations of drain current as a function of gate voltage at various temperatures, and Figure 5 for extracted values of activation energy, based on this data).

A very pleasing aspect of our work is the significant hike in drive current that results from the insertion of the $In_{0.7}Ga_{0.3}As$ layer. We attribute this gain to a combination of a higher mobility, a smaller bandgap material in the channel and an increase in carrier confinement (see Figure 6). Carrier confinement is partly aided by a favourable band alignment between $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$, and it also gets a helping hand from the thin thickness of the $In_{0.7}Ga_{0.3}As$ channel.

The sub-threshold swing of our transistors is similar to those produced by the Tokyo group, and does not penetrate the sub 60 mV/dec barrier. However, the combination of a sub-threshold swing approaching 60 mV/dec and a high drive current positions our

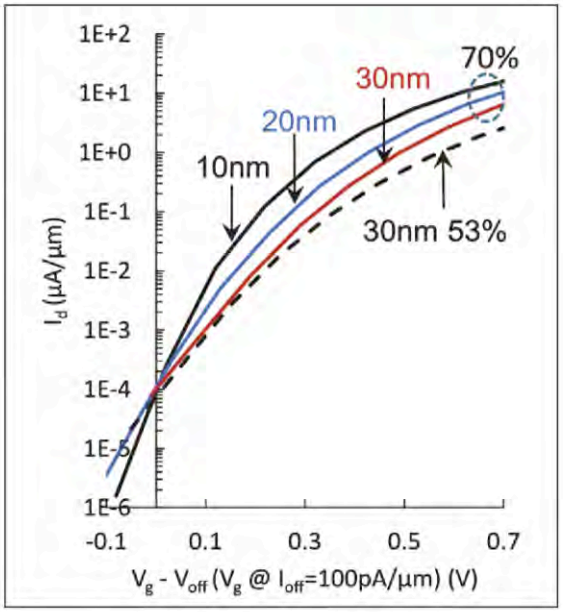


Figure 6. Simulations of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ double-gate TFETs with different channel thicknesses. The smaller band gap, as well as the confinement in the 8 nm channel, improves device performance. The impact of the confinement is significantly stronger than the bandgap.

A stumbling block to producing all III-V MOS devices is the realisation of a reliable gate stack. Despite decades of work, there is yet to be a report of clear success. Operation of a TFET is markedly different from that of a MOSFET, making it interesting to compare the reliability of both classes of device, when they sport identical gate stacks

$In_{0.7}Ga_{0.3}As$ quantum-well channel TFET as one of the very best devices of its kind (see Figure 7 for a comparison of its performance to that of other leading tunnel FETs).

A stumbling block to producing all III-V MOS devices is the realisation of a reliable gate stack. Despite decades of work, there is yet to be a report of clear success. Operation of a TFET is markedly different from that of a MOSFET, making it interesting to compare the reliability of both classes of device, when they sport identical gate stacks. Intuitively, if gate stacks are identical, both devices should be similar, in terms of reliability and in the physics associated with charging and discharging.

Measurements confirm this hypothesis. Both classes of device produce similar shifts in threshold voltage with stress voltage and duration, implying that they have similar lifetimes. Differences are noted, however, when comparing the degree of degradation of sub-threshold swing as a function of the induced threshold voltage shift (caused by stressing the device). With the TFET, this degradation is slower than it is with the MOSFET (see Figure 8). This is an interesting observation, given that the kinetics of the oxide trapping and de-trapping are identical in both classes of transistor.

To understand the origin of this variation, we have studied plots of capacitance and current, both as a function of voltage (see Figure 9). The graphs offer a valuable insight into device behaviour: despite the similar flat band voltages, which are clear from the plots of capacitance as a function of voltage, the threshold voltages of the two devices differ significantly. It is the TFET that has a much higher threshold voltage than the MOSFET.

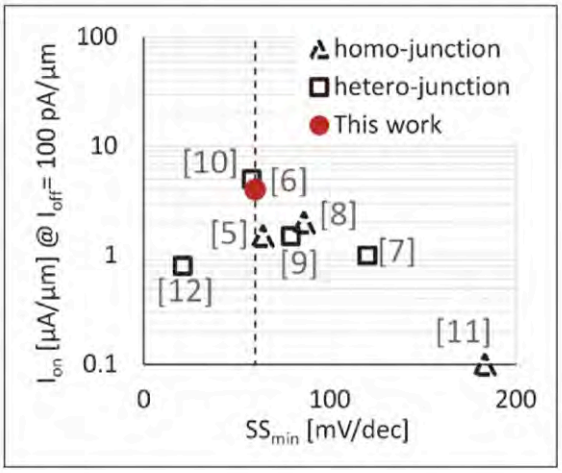


Figure 7. Benchmarking of imec's $In_{0.7}Ga_{0.3}As$ TFET to other reported III-V TFETs reveals that the performance of its device approaches that of the best reported heterojunction III-V TFET. I_{on} is extracted assuming a V_{dd} of 0.5 V and at I_{off} of 100 pA/ µm – these are values that are relevant for low standby power applications. Where the target I_{off} level was not reached, I_d-V_g was extrapolated. Where available, a V_d of 0.5 V was used – otherwise it was 0.3 V. The impact of V_d on I_{on} is not significant, except for [12] where the data point for V_d is 1 V.

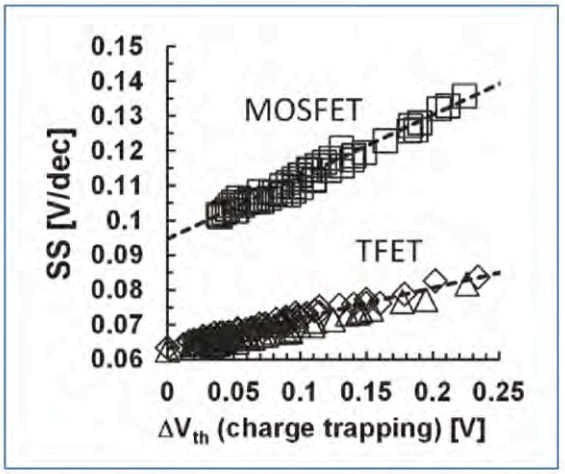


Figure 8. The sub-threshold swing of the TFET degrades far less than that of the MOSFET for the same amount of positive-bias, temperature-instability-induced threshold voltage shift (V_{th}). An explanation for this is provided in figure 9.

Based on this insight, and considering the equivalent operating energy range in the band structure, it can be concluded that the operating energy range of the TFET is much narrower than that of the MOSFET. While the TFET operates at/inside the conduction band edge, the MOSFET operates over the full upper-half of the bandgap, as well as inside the conduction band. A key consequence of this is that the range of border trap energy levels interacting with channel charges during the current-voltage sweep is more limited with a TFET, so is less prone to degradation of the sub-threshold swing. Another implication of the difference in the operating bandgap energy ranges of the two classes of transistor is that the TFET operates away from the mid-bandgap of InGaAs. This is an advantage, because the interface state density is usually high around the mid-bandgap of InGaAs.

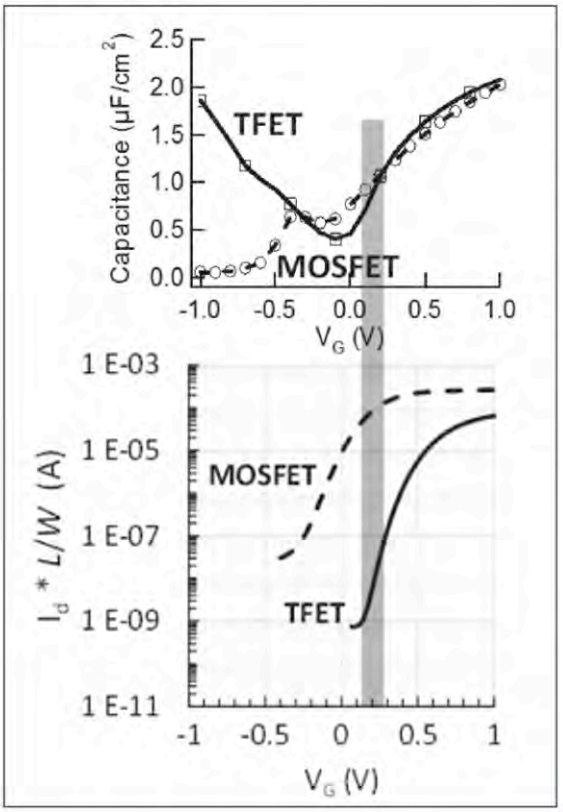


Figure 9. Despite having similar flatband voltages (shown by the grey area), the TFET has a significantly larger threshold voltage than the MOSFET. In terms of the operating energy range, this implies that the TFET operates close to the conduction band edge and inside the conduction band, while MOSFET operation starts from about midgap. In other words, the TFET operates over a significantly narrower energy band than the MOSFET. This means that the TFET is less sensitive to interface states at the midgap, which are usually large in III-V devices. Another consequence is that the TFET interacts with a smaller proportion of traps inside the gate oxide (border traps), thanks to its smaller operating energy range. This latter is believed to be the reason for the slower degradation in sub-threshold swing in the TFET, as observed in figure 8.

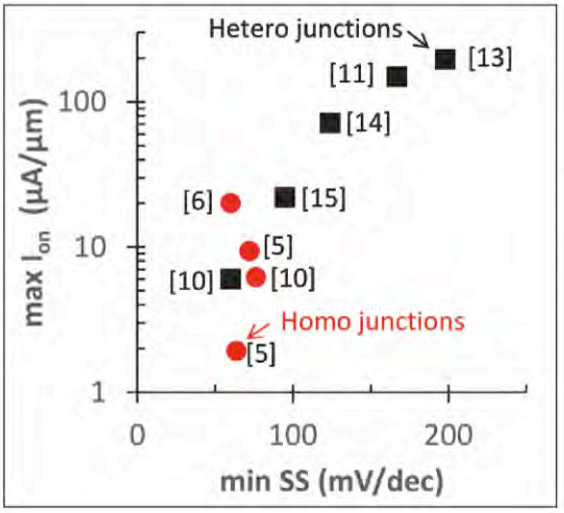


Figure 10. Moving from a homojunction to heterojunction TFET increases drive current, but can also result in a hike in sub-threshold swing.

Our observations to date suggest that the TFET has the same lifetime, measured in the form of time-to-failure, as the MOSFET. However, its strength is its superior immunity to interface traps at midgap, which historically plague III-Vs.

To make TFETs more appealing, there is a need to address their biggest weakness – the low drive current. One option is to turn to a heterojunction. However, with this modification, gains in current are so far at the expense of an inferior sub-threshold swing (see Figure 10). What's needed is to improve this substantially and get the sub-threshold swing to plummet to significantly below 60 mV/dec. This will be tough, but maybe it can be accomplished within a decade, and enable the TFET to become a worthy greener alternative to the MOSFET.

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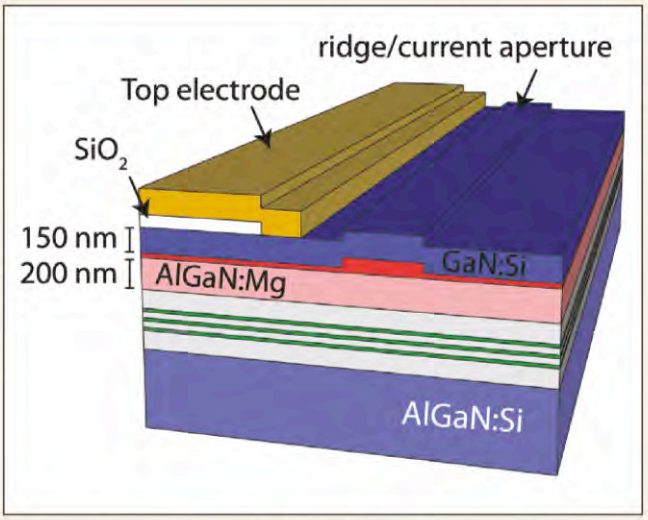
RESEARCHERS in Switzerland have developed a novel GaN laser architecture that addresses two of the biggest weaknesses of this class of device: poor *p*-type doping and limited optical confinement.

By turning to a transparent *n*-type GaN top layer, a top metallic contact beside the ridge, and carrier injection via a tunnel junction, the new device promises to increase GaN laser performance. It could lead to increased sales of these devices, which are now widely used for solid-state lighting and high-density data storage.



Researchers at EPFL and Exalos have produced a 400 nm laser that injects carriers into the device via a lateral top contact.

Spokesman for the team from EPFL and Exalos, Marco Malinverni, told *Compound Semiconductor* that the design of a conventional GaN laser is severely limited by issues relating to *p*-doping and optical confinement.

"Concerning *p*-type doping, the relatively high resistivity limits the possibility of creating current apertures and hinders the current spreading in *p*-doped layers," says Malinverni.

The Swiss team has spent several years overcoming this performance bottleneck. In 2015 it reported a significant milestone, the development of tunnel junctions that allow switching from *p*-type to *n*-type material. This breakthrough enabled the construction of current apertures.

"At this stage it became clear that introducing tunnel junctions in laser diodes had great potential," recollects Malinverni. He and his co-workers considered using these junctions with suspended membrane structures, such as one- or two-dimensional photonic crystals. Great optical confinement would result from the high refractive index contrast at GaN-air interfaces, but air would limit thermal dissipation, hampering the performance of the edge-emitting lasers.

"As a consequence, while keeping the bottom cladding unchanged for thermal dissipation, we have designed the structure to benefit from air confinement on top of the structure," explains Malinverni.

Another feature of the design is removing metal from the top of the ridge. This avoids optical losses resulting from an overlap of the top metal with the confined mode.

The Swiss team constructs its novel laser by taking a free-standing GaN substrate, loading it into an MOCVD chamber, and growing a laser structure up to the magnesium-doped GaN cap. After defining a ridge and current aperture with a standard patterning technology, they transfer the structure to an MBE reactor and deposit 150 nm of highly doped *n*-type GaN.

Adding a SiO_2 isolation layer, introducing a lateral top contact and bottom electrode, and creating cavities via cleaving completes device fabrication.

Malinverni accepts that these devices are more difficult to produce than their conventional cousins, due to an additional MBE re-growth step. The devices reported in the paper involved a rough re-growth, resulting from non-optimised processing of the current aperture. "Nowadays, we can make smooth re-growths, which will result in even better device characteristics."

Growing the entire structure by MOCVD would be preferable, but it is far from easy to implement, due to hydrogen passivation of the magnesium acceptor. Rapid thermal annealing is often used to activate magnesium, but this approach can degrade the electrical characteristics of the tunnel junction.

The 400 nm laser reported by the team has an 8 μm-wide ridge and a 1000 μm-long cavity. When mounted with indium on a copper plate heat sink, this chip has a threshold current density of 2.4 kA cm^{-2}, a slope efficiency of 0.4 A/W, and produces a CW output in excess of 100 mW.

Slope efficiency is 40 percent less than that of a conventional laser, while threshold current density is 20 percent higher. Both deficiencies are thought to result from the rough surface created during MBE growth of the reported devices, and greater optical losses, resulting from differences in optical confinement.

Malinverni says that the team will now focus on optimizing the growth of the tunnel junction so that its specific resistance falls to 10^{-6} Ω cm^{-2}.

M. Malinverni *et. al.*
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Increasing deep UV LED extraction with sapphire lenses

Bonding a sapphire lens to a deep UV LED chip propels external quantum efficiency beyond 10 percent

ENGINEERS from Nichia are claiming to have set a new benchmark for deep UV LED extraction efficiency by bonding a chip to a sapphire lens.

Thanks to the higher extraction efficiency, the team's 280 nm and 255 nm LEDs deliver peak external quantum efficiencies of 10.1 percent and 4.5 percent, respectively.

Higher external quantum efficiencies hold the key to realising high output powers, and to ultimately making devices that are more attractive for sterilisation and polymer curing.

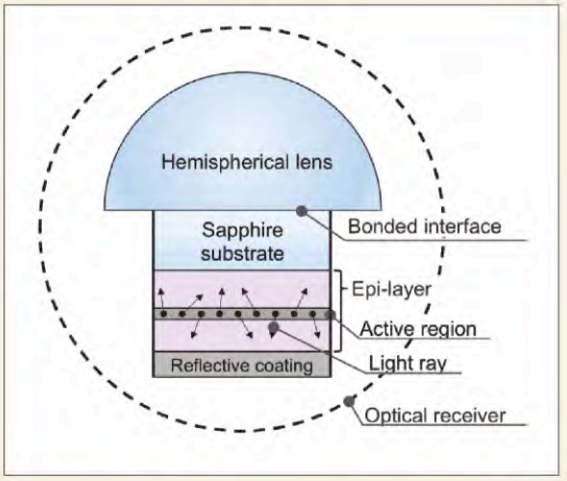
The low extraction efficiency of the conventional deep UV LED – it is typically below 5 percent, compared with 70 percent for its visible cousin – is a problem that has vexed researchers for many years. Improvements have already resulted from: growing the epilayers on low-dislocation-density substrates and templates; changing the structure of the active region; and optimising crystal growth. However, none of these address the absorption of light in the *p*-type contact.

To prevent light absorption in this region, the device must incorporate a flip-chip architecture, with light extracted through the substrate. External efficiency is enhanced by encapsulating this device in a transparent material with an intermediate refractive index, because this suppresses multiple reflections within the chip.

Unfortunately, the leading contenders for an intermediate refractive-index media, epoxy and silicone resin, are strong UV absorbers. This has led one group to investigate a fluorine resin. It increases extraction efficiency, but could hamper long-term reliability.

The more promising approach, being pioneered by Nichia researchers, is to use room-temperature bonding to attach a material with an intermediate refractive index to the deep UV LED chip.

Two different approaches have been investigated for this step. One option is atomic diffusion bonding, which involves sputtering a thin metal film onto a mirror-polished surface, such as sapphire or SiO_2. Room-temperature bonding at moderate pressures results from the high surface energies of the metal films and the large atomic diffusion coefficients at grain boundaries and film surfaces. The downside, however, is optical absorption at bonding interfaces.



Bonding a deep UV LED chip to a sapphire lens increases extraction efficiency by a factor of up to 2.8.

This is not the case with the second option explored by the team from Nichia, surface-activate bonding. With this approach the bonding surfaces are sputter-etched and activated using an argon fast ion beam. The weakness is that the bonding strength depends on the materials involved, and this rules out the use of SiO_2.

Nichia's engineers calculated extraction efficiencies for deep UV LEDs that feature hemispherical lenses with diameters from 1.5 mm to 6 mm, and a refractive index ranging from 1.43 to 2.0. These calculations reveal a lens diameter of ideally 3 nm or more and an optimal refractive index of 1.83, which is equal to that of sapphire.

Based on these findings the team used both room-temperature bonding techniques to attach sapphire lenses with diameters of 3 mm and 5 mm to deep UV LEDs with dimensions of 1 mm by 1 mm. For atomic diffusion bonding, a 0.2 nm-thick aluminium layer was deposited prior to the uniting of the surfaces.

Both types of LED, plus a control, were mounted on AlN submounts. Driven by a pulsed current at 350 mA, conventional 255 nm LEDs produced a 25.6 mW output under 7.9 V, while those with lenses added with atomic diffusion bonding and surface-activated bonding produced 64.6 mW at 7.9 V and 73.6 mW at 8.0 V, respectively. Similar results occurred with 280 nm LEDs. In this case, adding a lens with atomic diffusion bonding produced a 1.9-fold increase in output to 125.8 mW, and surface-activated bonding increased the output by a factor of 2.3 to 153.4 mW.

For both the 255 nm and 280 nm devices, the lower output for lenses added by atomic diffusion bonding, rather than surface-activated bonding, is probably due to the metallic layer at the interface.

Lifetime measurements on 280 nm LEDs featuring a lens added by atomic diffusion bonding indicate that the device is robust. Driven by 350 mA at 52 °C, the output power remained above 90 percent of its initial value after 1000 hours of operation.

M. Ichikawa *et. al.* Appl. Phys. Express **9** 072101 (2016)

GaN *p*-doping without a dopant

Careful selection of InGaN's alloy thickness and grading profile can control the three-dimensional hole density

RESEARCHERS at the University of California, Santa Barbara (UCSB), are pioneering a new approach for producing *p*-type nitride layers. With their technique, judicious selection of the grading and composition of an undoped InGaN layer can a realise three-dimensional hole density of between 1 x 10^{16} cm^{-3} and 1 x 10^{19} cm^{-3}.

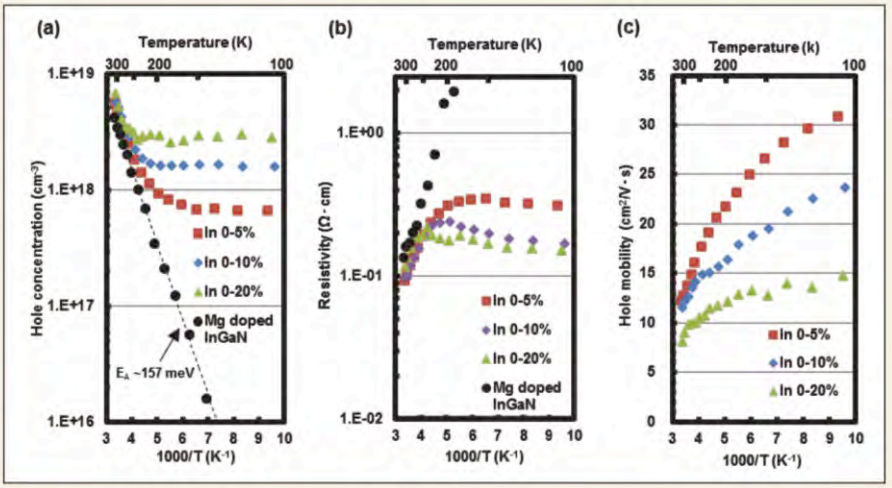
"As far as I know, this is the first demonstration of a three-dimensional hole gas, without doping, using an InGaN alloy on a gallium face," says corresponding author Yuuki Enatsu, who holds positions at UCSB and Mitsubishi Chemical Corporation.

Qualifying this claim, Enatsu says that although a team from Meijo University in Japan reported a *p*-type layer in undoped, graded AlGaN in 2013, they did not demonstrate a relationship between the density of the three-dimensional hole gas and alloy composition and thickness.

Enatsu believes that the team's technology could improve the performance of power devices, including vertical FETs that utilise a buried *p*-type layer for normally off operation and for the control of the threshold voltage. Magnesium doping in this layer is typically 3 x 10^{19} cm^{-3}, due to the low level of ionisation, and the hydrogen passivation of this layer during regrowth and processing places restrictions on design, growth and fabrication. It is claimed that the approach adopted by the UCSB team lifts these restrictions.

"Moreover, this technique could be useful for the super junction structure, which is used in silicon technology for accurate carrier control," argues Enatsu.

The west-coast team have realised a range of three-dimensional hole gas densities in InGaN layers grown by MOCVD on GaN substrates. With foreign substrates, such as sapphire and SiC, forming a three-dimensional hole gas should still be possible, but the surface morphology will be inferior – many pits will form on the surface, due to a high dislocation density in the layers.



Hall effect measurements on 100 nm-thick InGaN layers with a graded indium content increasing from 0 percent to either 5 percent, 10 percent or 20 percent, and a control sample of magnesium-doped $In_{0.05}Ga_{0.95}N$.

"The pit formation might reduce the three-dimensional hole gas density, since impurities such as oxygen and silicon are more incorporated," warns Enatsu.

Various samples were produced at UCSB. They included three with 100 nm-thick InGaN layers that had compositions graded from no indium content to either 5 percent, 10 percent or 20 percent. In addition, a second series of samples were grown that were graded from 0 percent to 5 percent and had thicknesses of either 100 nm, 300 nm or 800 nm. For comparison, the team also produced a control – a 100 nm-thick, $In_{0.05}Ga_{0.95}N$ layer with a magnesium doping level of 8 x 10^{19} cm^{-3}.

X-ray diffraction measurements on several samples produced experimental data that matched well with simulations, thereby confirming the presence of compositionally graded InGaN layers. Sample surfaces are atomically flat and free from V-defects, according to atomic force microscopy.

Hall measurements on the 100 nm-thick samples with differing indium content revealed that increasing the rate of change in polarisation charge across the layer propelled the hole concentration from 6.6 x 10^{17} cm^{-3} to 2.8 x 10^{18} cm^{-3} (see Figure 1 (a)). Note that these values are very close to those calculated.

The resistivity of the undoped samples exhibits a markedly different behaviour from that of the control (see Figure 1(b)). According to the team, the decrease in resistivity below 250 K in the undoped samples is due to holes induced in the polarization field in the graded InGaN layer.

Mobility of the holes is higher for a lower indium content (see Figure 1 (c)), probably due to a decrease in alloy scattering.

Enatsu and co-workers have already made a range of devices that incorporate their novel *p*-type layers. They will begin by reporting the results of vertical power *p-n* junction diodes in the *Japanese Journal of Applied Physics*. "After that, we will show vertical MOSFET and LED data in other journals."

Y. Enatsu *et. al.*
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