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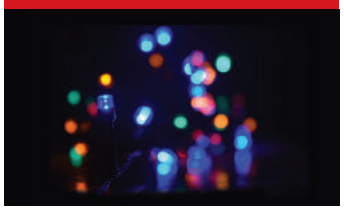
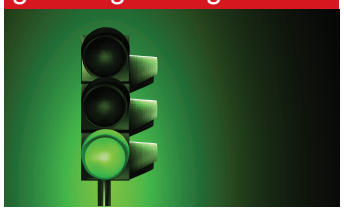
Understanding the low efficiency of GaN lasers

MicroLED displays: How good are their prospects?

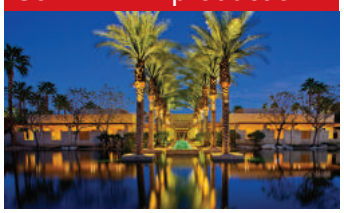
Bridging the green gap with novel substrates

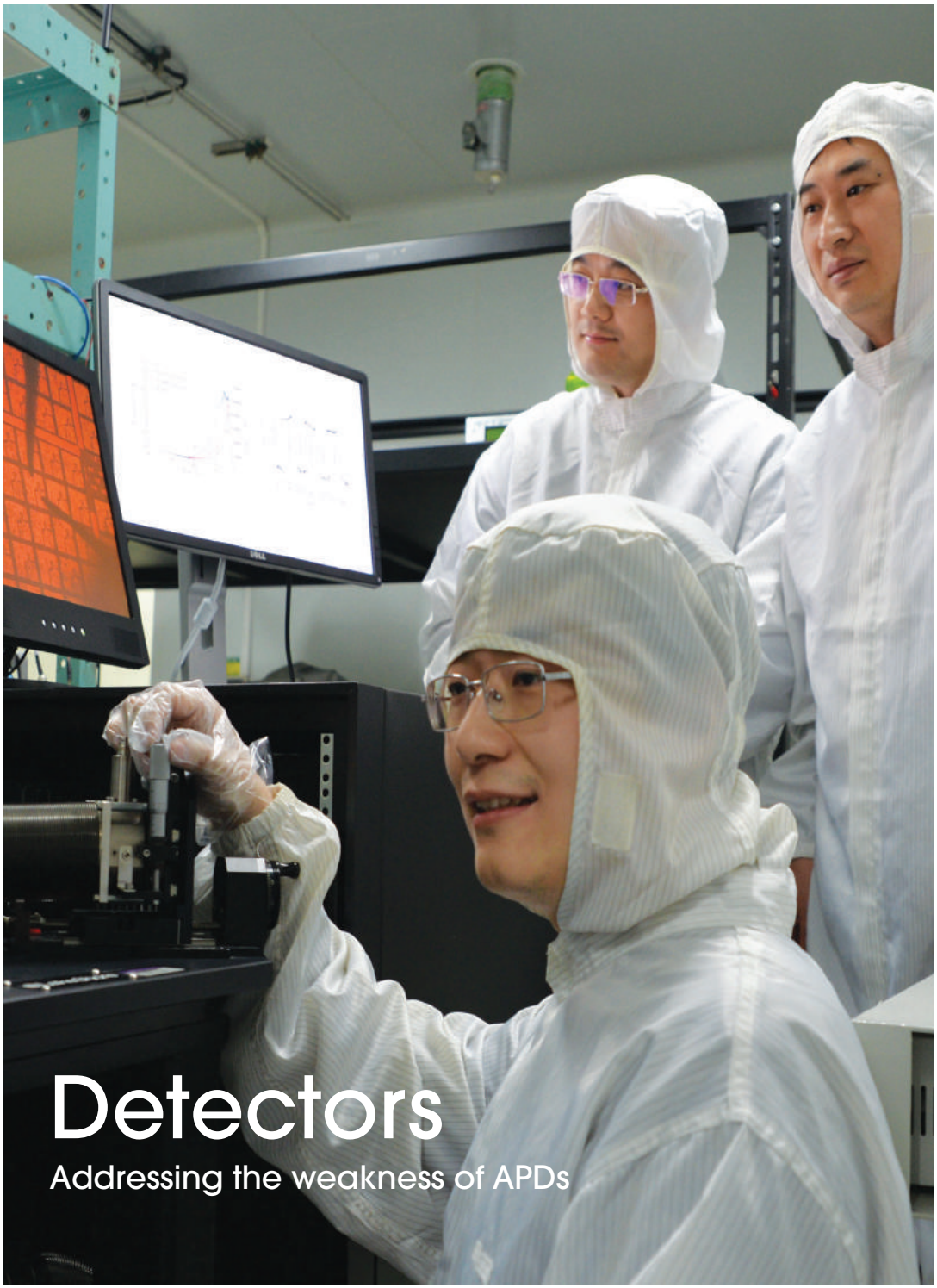


GaN-on-silicon devices get the green light



CS Mantech: Refining GaN HEMT production





Detectors

Addressing the weakness of APDs

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Viewpoint

By Dr Richard Stevenson, Editor

Lighting with lasers?

SEVERAL EXPERTS have suggested that the GaN-based laser will supersede the LED as the dominant source for solid-state lighting.

The most famous figure indicating that this could happen is Shuji Nakamura. In the lecture he gave for winning the Nobel Prize for Physics in 2014, he pointed out that GaN lasers operating at high current densities could create white light sources with a staggering light output.

Others enthused by the potential of laser-based lighting include Jonathan Wierer and Jeffrey Tsao from Sandia National Labs. They have evaluated the capability of a white light source that mixes several lasers emitting at different wavelengths. Their calculations suggest that the resultant source, which would include GaN lasers emitting in the blue and green, could be very attractive, partly due to its freedom from droop.

Commercialisation of white-light, GaN-based laser sources is already underway, with headlights of high-end cars, such as premium models made by BMW, providing the best-known success. In this application, the laser's directionality enables illuminated of the road far ahead with a carefully chosen beam.

So, given the progress made to date, is laser-based lighting of homes and offices just around the corner? Well, probably not, according to theorist Joachim Piprek from the NUSOD Institute.

In this month's issue, in his piece entitled *What is to blame for the low efficiency of GaN-based lasers?* (see p.34), Piprek presents the results of calculations that suggest that lasers may never get close to the efficiency of LEDs – so there is no change in the status quo on the horizon.

According to Piprek, the best blue LEDs can now hit an efficiency of 84 percent, while lasers are limited to just 43 percent. The latter is held back by various loss mechanisms: Joule heating, due to a high series resistance; losses inside the quantum well, predominantly resulting from Auger recombination; electrical leakage; and optical absorption.

Piprek points out that higher laser efficiencies could be reached with a novel architecture that has been pioneered by Nakamura and co-workers. Out goes the *p*-doped cladding, replaced with a tunnel junction and a highly conductive *n*-doped layer. Turning to this unconventional design slashes cladding and contact resistances on the *p*-side, leading to far lower bias and self-heating. Fewer carriers are then needed for lasing, reducing Auger recombination and delivering a three-fold hike in peak power. Another benefit is a narrowing of the efficiency gap with the LED, but the difference is still significant – so it would appear that LEDs bulbs are safe for the foreseeable future.

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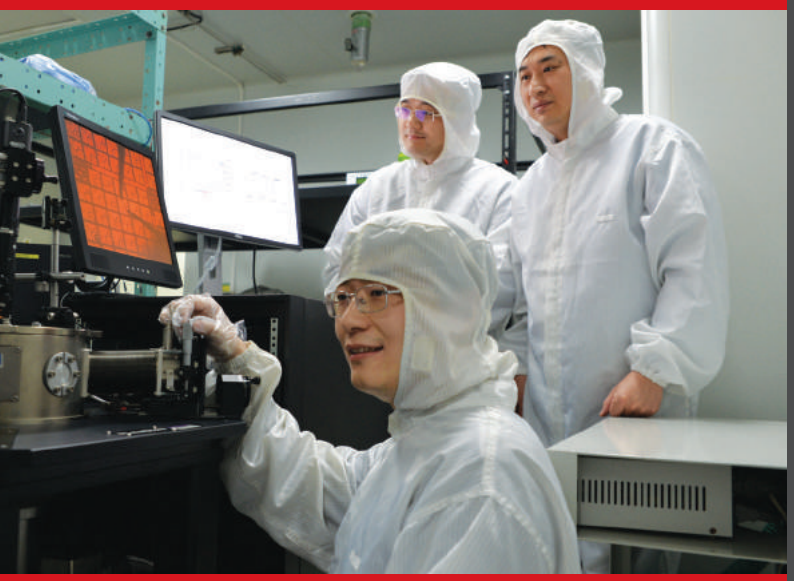

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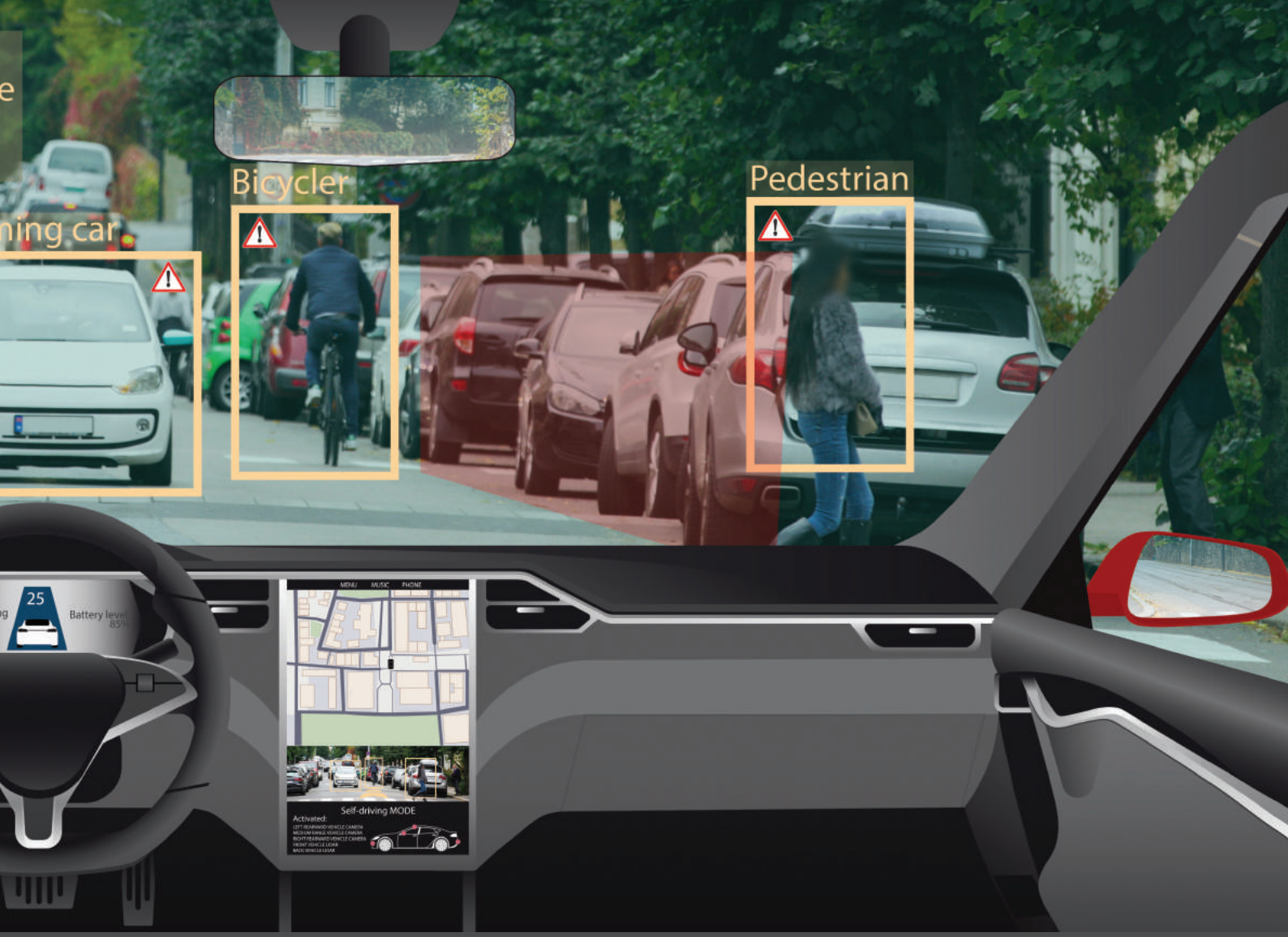

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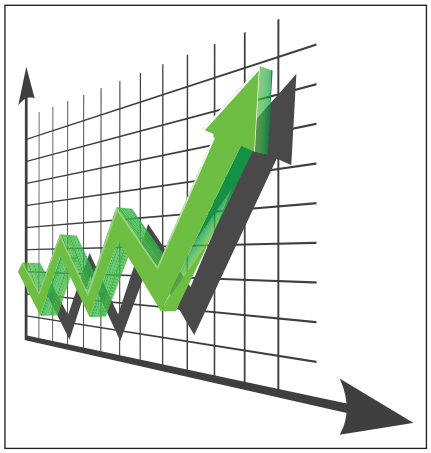
Compound semi market growing 8 percent CAGR

IN A NEW REPORT covering 2017 to 2021, market research analysts at Technavio predict that the global compound semiconductor market will grow at a CAGR of over 8 percent by 2021.

This market research identifies the rising global adoption of smartphones as one of the primary growth factors, driven by the availability of low-cost smartphones and the increased penetration of the Internet.

An increase in mobile devices drives the market for components such as GaAs amplifiers and switches. Additionally, says Technavio, smartphone manufacturers are trying to develop solar-powered smartphones by using GaAs. This will drive the production of smartphones powered by GaAs-based solar cells, which will subsequently drive the growth of the compound semiconductor market.

Growth in industry automation will also drive the market in the coming years, according to the report, because compound semiconductors (such as



GaN and SiC) are playing a key role in increasing the efficiency of power consumption.

The report identifies leading vendors in the market as Broadcom, Skyworks Solutions, Cree, and Qorvo. Other prominent vendors include Analog Devices, Osram Opto Semiconductors, GaN Systems, Infineon Technologies, NXP Semiconductors, Advanced Wireless Semiconductor, STMicroelectronics, Microsemi, Texas Instruments, WIN Semiconductors, and AXT.

APAC will be the major revenue contributor to the market by 2021.

This is due to the increased demand for power applications and the economic growth in developing countries such as South Korea, China, India, Taiwan, and Malaysia. Additionally, the increasing demand for wireless infrastructure will also boost the growth of the compound semiconductor market in this region.

The report also considers the growth of similar markets such as epi wafers and semiconductor chip packaging, which are expected to grow at a CAGR of 12 percent and 31 percent, respectively, for the forecast period of 2017 to 2021.

In another new report, Technavio predicts that the SiC market will grow steadily at a CAGR of over 14 percent between 2017 and 2021, driven by the growing demand for power inverters for electric vehicles.

Automotive inverters and advanced semiconductor devices based on SiC FETs can save low energy losses and result in improved electric vehicle performance, says Technavio.

New Lumileds CoBs deliver up to 30000 lumens

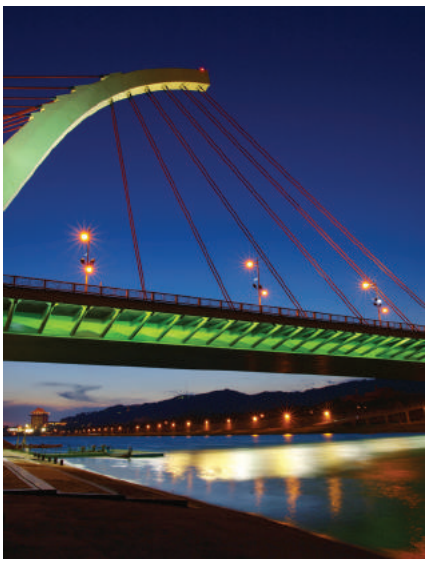
LUMILEDS has announced the addition of three new products to its Luxeon CoB Core Range to satisfy high lumen output applications such as streetlights, stadium lights and high bay and low bay fixtures.

“We now have the ability to address not only 40 and 50 W applications but up to 100 W and 120 W applications with these high lumen packages, at the same high efficacy as our Luxeon CoB Core Range (Gen 3) products,” said Eric Senders, product line director for the Luxeon CoB Family.

The high lumen extension of the Luxeon CoB Core Range (Gen 3) features light emitting surfaces (LES) of 23, 29 and 32 mm, nominal fluxes of 8,800, 11,000 and 16,000 lm at drive currents of 1.2, 2.1 and 2.2 A, plus efficacy up to 161 lm/W. The arrays are offered over a colour temperature range of 2700K to 5700K and CRI of 70, 80 or 90, with an efficient 70 CRI solution in warmer 3000K for outdoor lighting as well as a special colour requirement for studios and stadiums where cool colour temperatures and high (>90) CRI are required.

The CoBs are mounted on square Metal Core PCBs (MCPCBs), which are claimed to provide the industry’s lowest thermal resistance, enabling smaller heat sinks and optics for lower overall system cost.

“Feedback from many CoB customers indicates that heat sinks alone make up a substantial portion of system cost. By keeping the LES as small as possible and having a low thermal resistance substrate, a smaller heat sink can be used and a good portion of the cost has been removed from the system,” said



Senders. The Luxeon CoB Core Range (Gen 3) CoBs are compatible with an existing ecosystem of optic, drivers and holders.

Raytheon GaN radar surpasses 1000 operational hours

RAYTHEON has announced that its GaN-powered Active Electronically Scanned Array (AESA) proposed upgrade to the Patriot Air and Missile Defense has surpassed more than 1,000 hours of operation in just over a year – half the time of a typical testing program.

"We achieved this milestone so quickly because of our successful experience developing and maturing GaN for programs like the US Navy's Air and Missile Defense Radar," said Doug Burgess, director of AESA programs at Raytheon's Integrated Defense Systems business. "We're ready to take the next step and get this radar into the hands of our customers."

During the course of the 1,000 hours, Raytheon's GaN-based AESA prototype radar routinely demonstrated 360-degree capability by working together with a second GaN-based AESA antenna that was pointed in a different direction.

As targets flew out of one array's field of view and into another, the two arrays seamlessly passed information back and forth, tracking the target continuously. The main array also detected and tracked tactically manoeuvring fighter jets and thousands of other aircraft, according to the company.

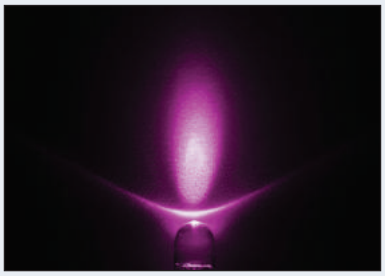
"Raytheon's GaN technology is backed by 19 years of research and $300 million in investment, while our competitors are either new to the market or primarily build GaN for commercial applications," said Ralph Acaba vice president of Integrated Air and Missile Defense at Raytheon's Integrated Defense Systems business. Raytheon's GaN-based AESA radar will work with the Integrated Air and Missile Defense Battle Command System and other open architectures. It maintains compatibility with the current Patriot Engagement Control Station and full interoperability with NATO systems.

A number of current and expected future Patriot Air and Missile Defense System partner nations in Europe and Asia have expressed interest in acquiring GaN-based AESA. Poland submitted a Letter of Request for GaN-based AESA Patriot on March 31. Raytheon's GaN-based AESA technology also meets Germany's requirements for the German Taktisches Luftverteidigungssystem, or TLVS, tactical air and missile defence system.

Dowa to mass-produce high Output UV LEDs

DOWA ELECTRONICS MATERIALS has developed a deep ultraviolet LED chip it says features the industry's highest output power, with a peak wavelength of 280 nm, output of 75 mW and dimensions of 1 mm x 1 mm. The company will be mass-producing these new products, with capacity equivalent to one million LED chips per month.

Since deep ultraviolet lights with a wavelength of 280 nm have a high efficiency of disinfestation, replacing the conventional mercury lamps with these LEDs enables facilities to be smaller and mercury-free. With other advantages, such as power saving, this product is expected to find new smart applications.

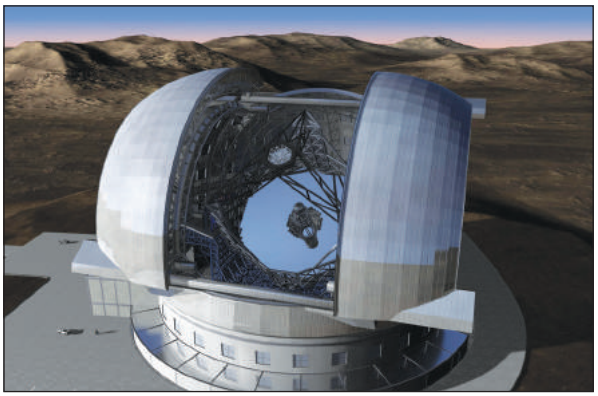


Combining an AlN template with crystal growth technology, Dowa Electronics Materials successfully began to mass-produce robust, deep ultraviolet LED chips in 2010.

Its development of what it believes is the world's highest output power deep UV LED chip is thanks to better luminous efficiency, by applying improved crystal growth technology together with an optimised LED chip design of dimension and structure.

The new UV products may provide light source manufacturers with a greater flexibility for selection of package formats, such as lamps and chip-on-board (COB). Dowa will also supply some finished products such as various kinds of the surface mount device (SMD) and conventional TO-Can package.

Sofradir designs supersize short wave IR detector



IR DETECTOR specialist Sofradir has announced it is developing its first very large format (2048x2048) 15 µm-pitch near infrared detector.

The supersize IR detector is designed for future scientific space observation equipment and state-of-the-art Extremely Large Telescopes (ELT) for ground observation aimed at tackling major scientific challenges.

The ALFA 2Kx2K (Astronomy Large Focal Array) 15µm pitch short-wave infrared detector will provide the highest levels of performance in Quantum Efficiency (QE), dark current and noise in order to optimize IR observations for astrophysicists.

The NIR detector is based on a compound semiconductor material, HgCdTe, as the absorbing material. It includes a readout circuit (ROIC) with a source follower per detector (SFD) at the input stage.

Sofradir is collaborating with leading French research centres CEA-Leti in Grenoble and CEA-IRFU in Paris to develop the ALFA near-infrared detector through an ESA initiative. Sofradir plans to deliver a fully characterized low-flux, low-noise ALFA prototype in Q1 2019.

"Sofradir is pleased to work with partners CEA-Leti and CEA-IRFU in developing a truly evolutionary very large-format infrared detector that will contribute to the detailed study of matter in the universe," said Philippe Chorier, space activities manager at Sofradir.

"Sofradir has a long and successful track record for delivering IR detectors with proven performance, robustness and reliability. We believe ALFA 2Kx2K will enable OEMs to build new instruments, opening up new opportunities for us in astronomy and other sciences, where every single infrared application needs very low flux and low noise compatibility."

Large format infrared detectors, greater than 1024x1024, are highly complex devices that only a handful of manufacturers in the world can produce to space-grade standards.

This new low-flux, low-noise near infrared (NIR) 2Kx2K detector for space astrophysics is the result of developments the ESA initiated several years ago, under its Near Infrared Large Format Sensor Array (NIRLFA) program. This is a program that Sofradir, CEA-Leti and CEA-IRFU have been working on since 2009.

The development of the detector will benefit from Sofradir's experience as one of the leading worldwide manufacturers for IR detectors deployed in space; totaling more than 82 flight models to date. Space programs include: Sentinel 2 and Sentinel 5 (Copernicus), MTG (Meteosat Third Generation) and Exomars, among others.

"Thanks to ALFA detector, Sofradir will be able to offer a new up-to-date solution for applications in space, science and astronomy," Chorier added. Details of the development were presented in the paper 'Development and Characterization of MCT Detectors for Space Astrophysics at CEA' at the International Conference on Space Optics in 2014.

Sofradir and its subsidiaries ULIS and Sofradir-EC exhibited a selection of top-of-the-line infrared detectors for airborne, naval, ground vehicle and space applications at the Paris Air Show.

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Imec announces GaN-on-silicon breakthrough

BELGIAN research company Imec has announced that it has developed 200 V and 650 V normally-off/enhancement mode (E-mode) power devices on 200 mm/8-inch GaN-on-silicon wafers, achieving a very low dynamic R_{on} dispersion (below 20 percent) and state-of-the-art performance and reproducibility.

Imec says it technology is ready for prototyping, customised low-volume production as well as for technology transfer. Imec's GaN-on-Silicon device technology is Gold-free and compatible with the wafer handling and contamination requirements for processing in a silicon fab. A key component of the GaN device structure is the buffer layer, which is required to accommodate the large difference in lattice parameters and thermal expansion coefficient between the AlGaN/GaN materials system and the silicon substrate.

Imec says it has achieved a breakthrough development in the buffer design (patent pending), allowing it to grow buffers qualified for 650 V on large diameter 200 mm wafers. This, in combination with the choice of the silicon substrate thickness and doping increased the GaN substrate yield on 200 mm to competitive levels, enabling low-cost production of GaN power devices.

Cleaning and dielectric deposition conditions have been optimised too, and the field plate design (a common technique for achieving performance improvement) has been extensively studied. As a result, the devices exhibit dynamic R_{on} dispersion below 20 percent up to 650 V over the full temperature range from 25°C to 150°C. This means that there is almost no change in the transistor on-state after switching from the off-state, a challenge typical for GaN technology.

"Having pioneered the development of GaN-on-silicon power device technology on large diameter substrates (200mm/8-inch), imec now offers companies access to its normally-off/E-mode GaN power device technology through prototyping, low-volume manufacturing as well as via a full technology transfer," stated Stefaan Decoutere, program director for GaN technology at Imec.

Osram announces multi-chip LED with lens for camera flash

OSRAM OPTO SEMICONDUCTORS has integrated two LED chips and a lens into a single module for camera flash applications. With its brightness of 125 lux, the Oslux S 2.1 is designed to provide uniform illumination of photos and video recordings from mobile devices such as smartphones.

The Oslux S 2.1 for camera flash applications combines two chips of different colour temperatures: a cold white chip with 6,000 K, and a warm white chip with 2,250 K (Dual-CCT), providing both a multi-chip LED and a lens for the first time. This not only makes manufacturing easier by saving a step, but also produces excellent results. The chip has a maximum deviation of 300 K, resulting in good colour fidelity and uniformity across the target scene. While dimensions of 5.0 mm x 5.0 mm x 1.15 mm make the Oslux S 2.1 with its lens slightly taller than previous models, it requires less space on the board and has a smaller exposed aperture than two single LEDs, making it overall a more compact solution.

The silicone lens also allows this module to be reflow solderable, allowing the module to be easily integrated into standard manufacturing flows."With the new Oslux S 2.1 we were able to achieve very high quality. We have subjected it to both electrical and optically demanding testing and are very happy with the results. It definitely meets our high quality standards," said Russell Willner, product marketing manager at Osram Opto Semiconductors.

Northrop Grumman introduces 5G MMIC range

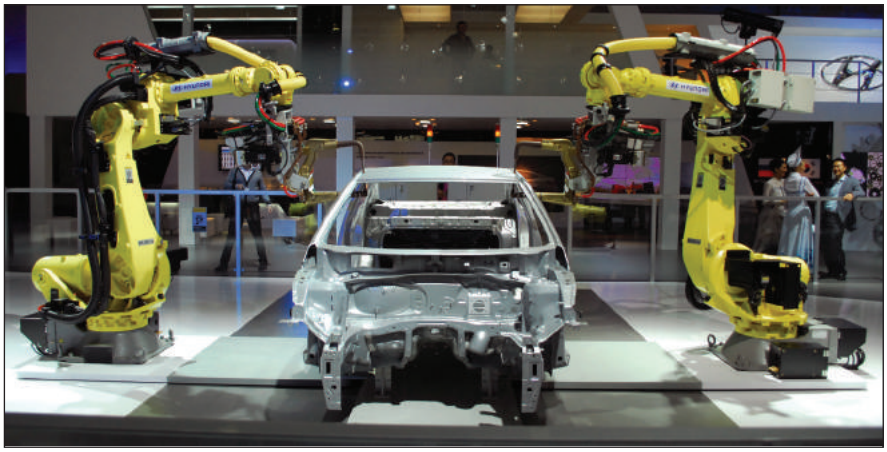
NORTHROP GRUMMAN has announced that a range of MMICS produced by its MPS (Microelectronics Products and Services) division meet the Federal Communications Commission's (FCC) 5G frequency allocations at the International Microwave Symposium (IMS) 2017.

"MPS's low noise and high power technologies and products provide a differentiating advantage that allows operators the ability to maximize the number of users and revenue generation,"said Chris Brown, general manager, Northrop Grumman MPS.

"The Northrop Grumman power amplifiers provide the high-linearity performance near peak output power levels required for complex modulations, which optimizes the data throughput within the FCC allocated bandwidth" said Brown. "This same performance advantage is realised in the 5G receivers using the Northrop Grumman low noise amplifiers utilising our GaAs and InP technologies. Between the power amplifiers, the low noise amplifiers and the mixers, we can address all of the 5G frequency bands."

Also at IMS 2017, Northrop Grumman engineers presented on high power and high efficiency chipsets for Ku-Band, Ka-Band, V-Band, Q-Band, E and W-band communications, and on optimising ground, airborne and space-based communication links using Northrop Grumman's advanced semiconductor products and technologies.

TI GaN design drives 200V AC servo drives with 99% efficiency



TEXAS INSTRUMENTS has introduced a three-phase, GaN-based inverter reference design that helps engineers build 200 V, 2 kW AC servo motor drives and next-generation industrial robotics with fast current-loop control, higher efficiency, more accurate speed, and torque control.

The reference design features TI's newest LMG3410 600 V, 12 A GaN power module with an integrated FET, gate driver and protection, announced last year. The GaN module allows the design to switch up to five times faster than silicon FETs, while achieving efficiency levels greater than 98 percent at 100 kHz and greater than 99 percent at 24 kHz pulse width modulation (PWM) frequency.

With GaN, designers can optimise switch performance to reduce power loss in the motor, and downsize the heat sink to save board space. Operating the inverter at 100 kHz significantly helps improve torque ripple when used with low-inductance motors. According to TI, the reference design will help engineers design 200 V, 2 kW AC servo motor drives and next-generation industrial robotics with fast, more precise torque control and 99 percent efficiency.The GaN inverter power stage interfaces with microcontrollers (MCU), including TI's TMS320F28379D drive control system-on-chip to help dynamically adjust voltage frequency and achieve ultra-fast current loop control.

TI has also introduced its new Design DRIVE Fast Current Loop software with innovative sub-cycle PWM update techniques that help push current-loop performance in servo drives to less than 1 microsecond, potentially tripling motor torque response. The Fast Current Loop software outperforms traditional MCU-based current-loop solutions, and is available free with controlSUITE software. In addition to the GaN module, the reference design relies on TI's AMC1306 isolated delta-sigma modulators with current sensing to increase motor control performance. TI's ISO7831 digital isolator also provides reinforced isolation between the MCU and the design's six PWMs.

GREEN LIGHT FOR GaN DEVICES

Exagan and X-Fab prepare for mass production after delivering GaN-on-silicon devices with a 200 mm CMOS process. Rebecca Pool investigates.

IN A BREAKTHROUGH for GaN-on-silicon device markets, industry partners X-Fab and Exagan have produced transistors with a 200 mm, CMOS process.

With substrate fabrication taking place at Exagan's 200 mm epi-manufacturing facility in Grenoble, France, followed by device processing at X-Fab's CMOS foundry in Dresden, Germany, prototype 650 V G-FETs are currently with first customers.

Crucially, plans to ramp production are underway, with mass production well within the companies' sights.

"We are the first to transfer and produce devices on 200 mm wafers, with manufacturing quality, in a CMOS fab using standard silicon production equipments and process steps," claims Frédéric Dupont, president and chief executive at Exagan.

"Importantly, we have established our technology and products on the most competitive wafer size; taking advantage of the mature, 200 mm, and highly productive, manufacturing environment."

"Once our product is established on the market, we will be able to work with X-Fab to ramp up capacity very quickly," he adds.

Exagan's GaN-on-silicon technology has been under development since the late 1990s. Researchers at France-based hetero-epitaxy research centre, CNRS-CRHEA spent more than a decade grappling with the different thermal coefficients of silicon and GaN that cause materials stresses, and ultimately cracking, when a GaN film is grown on silicon. By 2003, a GaN-buffer – for the growth of thick, high-quality GaN layers on silicon – had been developed and patented by wide bandgap semiconductor business, Picogiga, France, later acquired by semiconductor material manufacturer, Soitec, also of France. In 2012, Soitec joined forces with electronics research institute, CEA-Leti, France, to develop a 200 mm, CMOS-compatible GaN-based FET process for 650 V power switching devices, with the technology then being transferred to Exagan for commercialisation.

Collaboration with X-Fab began in 2015 and in just two years several barriers to 200 mm CMOS process success have been overcome. Importantly, says Dupont, Exagan has developed its so-called G-Stack material technology, based on the CNRS-CRHEA buffer layer and including GaN insulating layers and strain management layers. These layers relax the GaN crystal stresses, improving crystal quality and yielding crack-free, flat wafers for CMOS manufacture.

"The larger the diameter, the more challenging it is to get a perfectly flat wafer, and managing cracks and bowing has been a huge challenge," he says. "But G-Stack has addressed this and we can manufacture wafers that are fully compliant with the CMOS process."

Frédéric Dupont, President, CEO and Co-Founder of Exagan (right) with X-Fab chief technology officer, Jens Kosch (left).

The GaN-on-silicon fabrication process adheres to the strict contamination rules of a standard CMOS process. "We also use fully-automated, epitaxy equipment for our eight inch process – including automated wafer handling – to avoid any contact and wafer contamination," says Dupont.

Crucially, not a single, additional processing step or tool is required to support GaN-on-silicon device fabrication. "We really wanted full compatibility with the CMOS line with no extra process steps of specific tools," highlights Kosch. "Our common goal from day one was to avoid additional capital expenditure and we can now use a standard CMOS manufacturing line, running at volume production levels, for this new GaN material."

Right now, Exagan is sampling 650 V G-FETs to its first customers. Devices have been described as having a high breakdown voltage, low vertical leakage and a high operating temperature, although according to Dupont, specific performance figures cannot yet be revealed. The company has also been working with Germany's certification services business, TÜV Nord, to achieve product qualification meeting automotive and aerospace industry standards.

Electric vehicle charging will be amongst the initial targeted applications for Exagan's 650 V G-FETs; a growing market already under scrutiny from other SiC and GaN suppliers. "There are many companies working on GaN but our technology and business model are unique; we control the full technology flow from the epitaxy to system level," asserts Dupont.

"Critically, our partnership with X-Fab gives us the capacity to ramp very quickly to high volumes and with very cost competitive devices," he adds. "I believe we will soon be recognised as the GaN market accelerator."

Infineon:

SiC modules and more

With volume production of SiC devices underway, what next for Infineon and compound semiconductors asks Rebecca Pool.

IT'S NO SECRET that higher efficiency, increased power density and a smaller footprint are just a few advantages that SiC MOSFETs offer over the silicon IGBTs. So as photovoltaic inverter, uninterruptible power supply and electric vehicle charging markets finally look set to adopt the technology, industry players have a raft of products ready.

Rohm recently unveiled an all-SiC, 1200 V, 600 A power module optimised for inverters and converters in solar power conditioners, UPS, and industrial power applications, just as Wolfspeed claimed its all-SiC 1200 V power model had met harsh environment qualification tests.

In the last two years, STMicroelectronics has delivered a series of 650 V and 1200 V SiC MOSFETs. And last month Infineon revealed it had started volume production of its full-SiC module while delivering new module platforms and topologies for its 1200 V CoolSiC MOSFET family.

For Peter Friedrichs, Senior Director of Silicon Carbide at Infineon, the time is right to ramp up production. As he puts it: "We are definitely seeing a tipping point for certain applications – solar power conversion, UPS and electric vehicle charging – thanks, in part, to a very attractive total system cost."

According to Friedrichs, inductive components make up a relatively large part of the bill of materials in many applications, including solar power conversion. However, SiC enables higher switching frequencies, allowing the use of smaller external components, including inductors and capacitors, saving board space and overall component cost.

"This reduction in the bill of materials was the tipping point for the use of SiC Schottky diodes more than fifteen years ago," highlights Friedrichs. "And these SiC devices were extremely highly priced at the time."

But looking beyond system costs, the time is also right to ramp up production as the industry transition from 100 mm to 150 mm SiC wafers is well and truly underway.

In May, last year, STMicroelectronics announced it was scaling up its production of SiC MOSFETs and diodes on 150 mm wafers, predominantly to drive down manufacturing costs and deliver volume to the automotive industry. Now Friedrichs confirms that Infineon has made the transition from 100 mm to 150 mm wafers for SiC diode production.

From word go, the company has also developed its SiC MOSFETs on 150 mm wafers, forging a strong connection between technology development and wafer availability. And right now, the company is sourcing its 150 mm wafers from a handful of vendors worldwide – 'the known companies' says Friedrichs – that can offer volume capability.

"The move from 100 mm to 150 mm is a major change and as always, some customers are more reluctant than others to change their products, but we are nearly there," he says.

"For 150 mm, we still see slight quality differences from supplier to supplier, whereas with 100 mm wafers quality is comparable," he adds. "But we believe we will move beyond this very soon and it isn't a sticking point at all."

Chasing markets

Infineon now intends to ease its first full-SiC module based on 1200 V MOSFETs – Easy 1B – into volume production this year. This module will target solar, UPS and charging applications.

Meanwhile, a larger module – Easy 2B – will follow. This version is designed for higher power ratings in target applications. Friedrichs reckons the latest module configurations will also soon be used in industrial drives, medical applications and auxiliary power supplies for the railway sector.

"We are definitely seeing a tipping point... thanks, in part, to a very attractive total system cost."

Peter Friedrichs, Senior Director of Silicon Carbide at Infineon:

"We have already seen our hybrid modules – which combine silicon IGBTs with silicon carbide diodes – being used in solar power conversion applications, and these will now be partially replaced with the silicon carbide switch," explains Friedrichs. "Silicon carbide is also going to be highly appreciated in the emerging electric vehicle fast-charging infrastructure market, but we do not expect to see modules in actual electric vehicles until at least 2020."

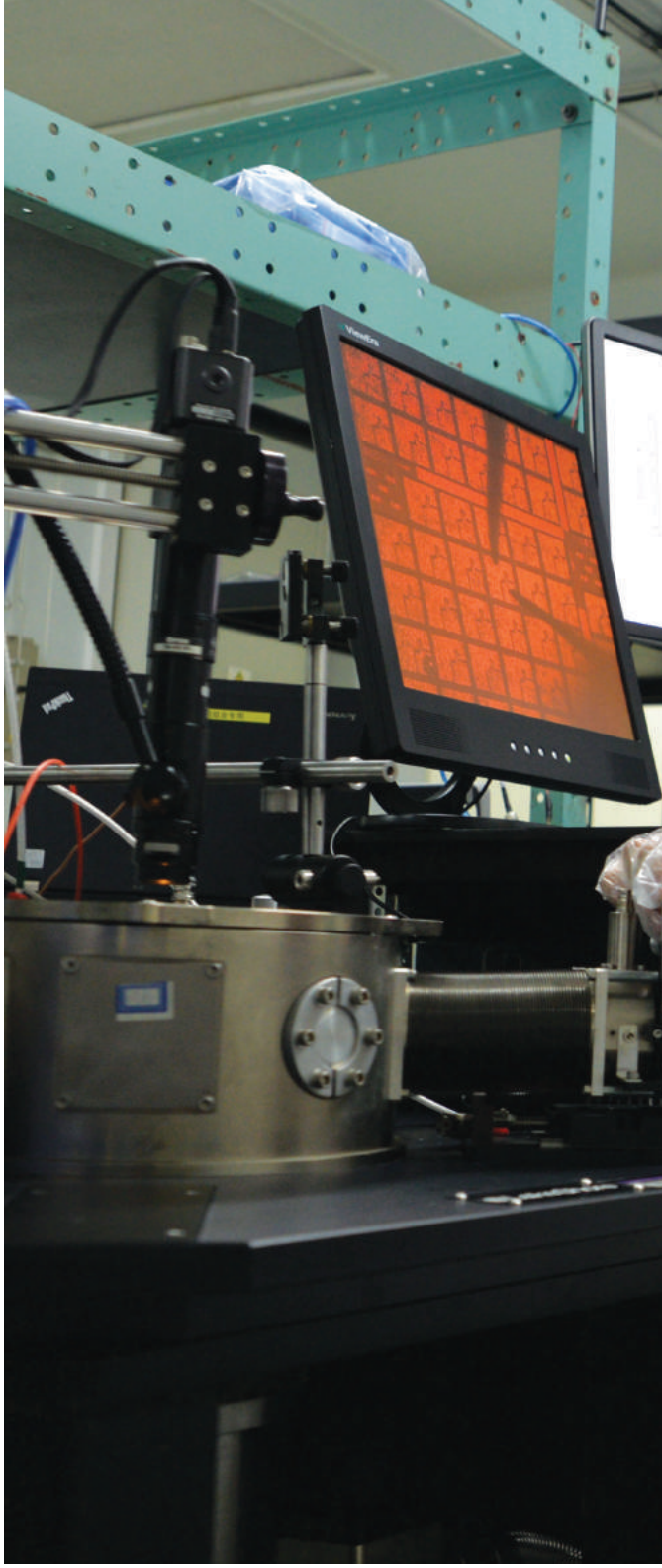
For now, customer acceptance is not a huge issue. According to Friedrichs, some customers are more conservative than others and wish to see field data first, which can be difficult with a new technology. And while faster switching devices bring EMC issues, the Senior Director is confident the necessary support can be offered here.

Crucially, Friedrichs reckons the company can keep pace with future leaps in demand. "We expect market growth to be around 20 percent [year-on-year], which is a lot greater than total power semiconductor growth," he says. "But we have good flexibility regarding volume manufacturing. We already have three-and-a-half-million SiC modules in the field – hybrid modules dominate so far – but we expect similar figures for the full-SiC modules as well."

Manufacturing aside, Friedrichs is also certain that SiC very much has its place amongst the rise of silicon semiconductor alternatives. "We believe, for example, that the playground for GaN HEMTs is very much 600 V while SiC can compete with silicon IGBTs at 1000 V and above," he says.

And looking to the future, Infineon has a roadmap in place for higher voltage systems; Friedrichs expects demand for 1700 V full SiC MOSFET modules to be driven by solar power conversion and traction applications, and eventually 3.3 kV modules will follow."We have frequent discussions about 10 kV and 15 kV parts but are still in 'observation mode' for such devices," he says. "We want to understand that there is a real market here, and that this [development] wouldn't be an academic exercise to simply achieve a world record."

Easy2B in half-bridge topology targets solar inverters, quick-charging systems and uninterruptible power supply applications.



Building better low-light detectors

A stack of alternating layers of GaN and AlN creates an avalanche photodiode with high sensitivity and excellent controllability

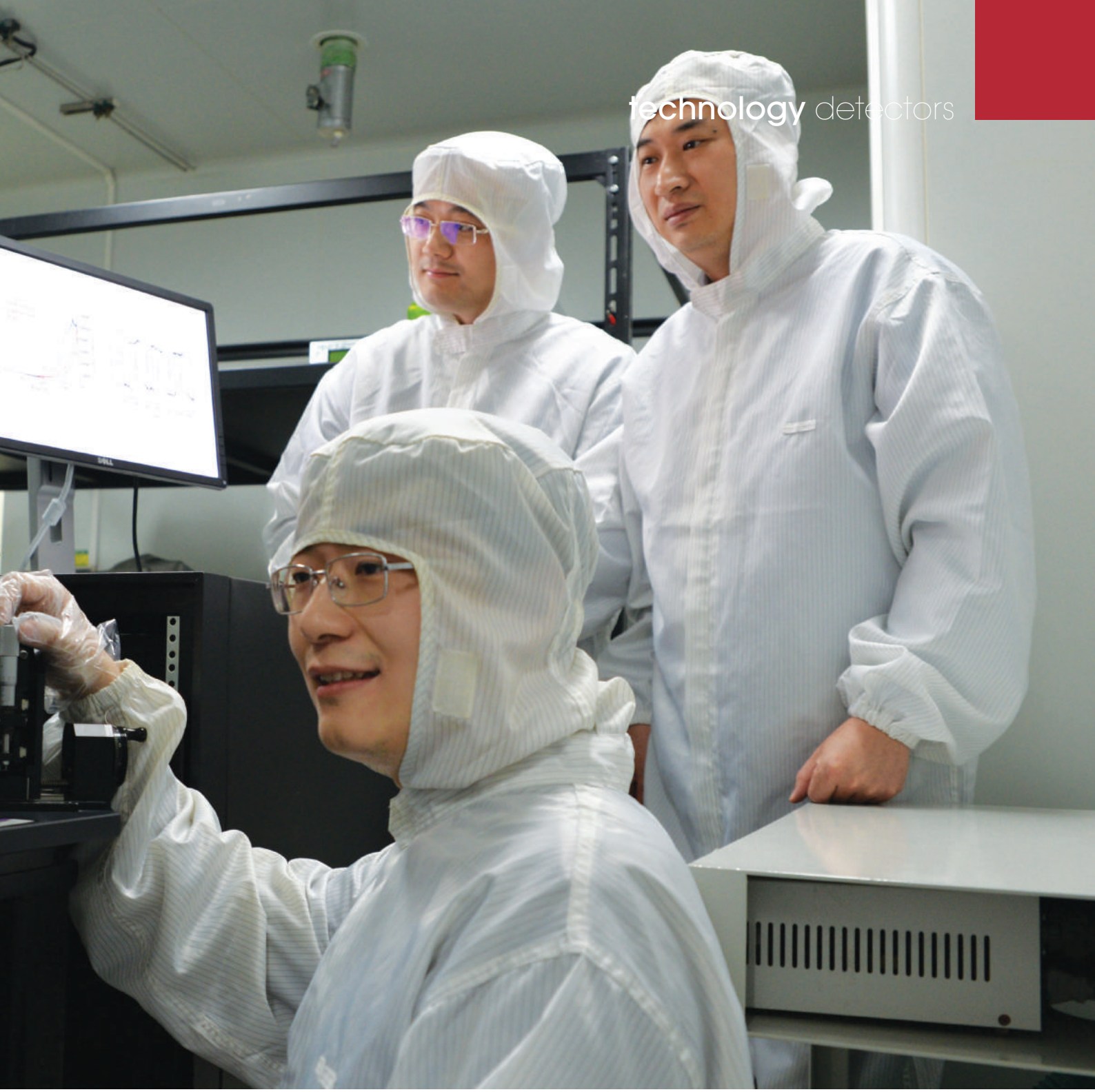
BY LAI WANG, JIYUAN ZHENG, ZHIBIAO HAO AND YI LUO FROM TSINGHUA UNIVERSITY

IF YOU NEED to measure incredibly low light signals, you have to make a compromise. If you want the best performance, you must select a photomultiplier tube. However, it is fragile and bulky. The alternative, addressing these weaknesses, is the avalanche photodiode (APD), but it is let down by its poor controllability.

The good news, however, is that this lack of controllability will not be plaguing the APD for much longer, thanks to a recent breakthrough by our group at Tsinghua University, working in partnership with researchers at CNRS-CRHEA, France, and the Chinese Academy of Sciences. Together we have developed a novel APD that delivers a record-breaking stable linear gain of over 10^4 under constant bias – that's almost two orders of magnitude higher than that of silicon APDs.

With conventional APDs, producing high multiplication gain requires operation under extremely high bias. When controlled in this manner, there is a drastic rise in the response current, known as 'breakdown'. This breakdown will not stop until the bias is reduced below its breakdown value.

What this means in practice is that when using an APD, it needs to be periodically quenched below its breakdown bias, with photons only detected when these diodes are under breakdown. It is a compromise between high gain and sustainable detection, and requires the use of complex control circuits. This



intrinsic limitation has been plaguing researchers for years, who want an APD that works like a PMT, with a controllable avalanche and the opportunity to operate the device under a simple constant bias with high gain. This is what you get with our device.

It is important to note that avalanche and breakdown are actually two completely different concepts. Breakdown is a compromise, used to ensure that a conventional APD delivers high gain. In this type of device, a significant proportion of the carrier energy that's drawn from the electric field is thermalized by intense scattering. As a result, these diodes have to work under extremely high bias, because this enables electrons and holes to both trigger ionization (see Figure 1(a)). Multiplication proceeds along two opposite directions, forming positive feedback chains that lead to a drastic rise in the response current.

A better approach would be for just one kind of carrier to trigger ionization, leading to an avalanche march in just one direction (see Figure 1 (b)). If that were the case, the avalanche could stop by itself when all the carriers move out of multiplication region. Thanks to this, the APD could provide a suitable response to the signal when it is operated under constant bias, simplifying its use and the accompanying circuitry.

Our device works on this principal, as do several others. In fact, in general, there are three conventional approaches to improving the sensitivity of linear-mode APDs: using materials with a great difference in

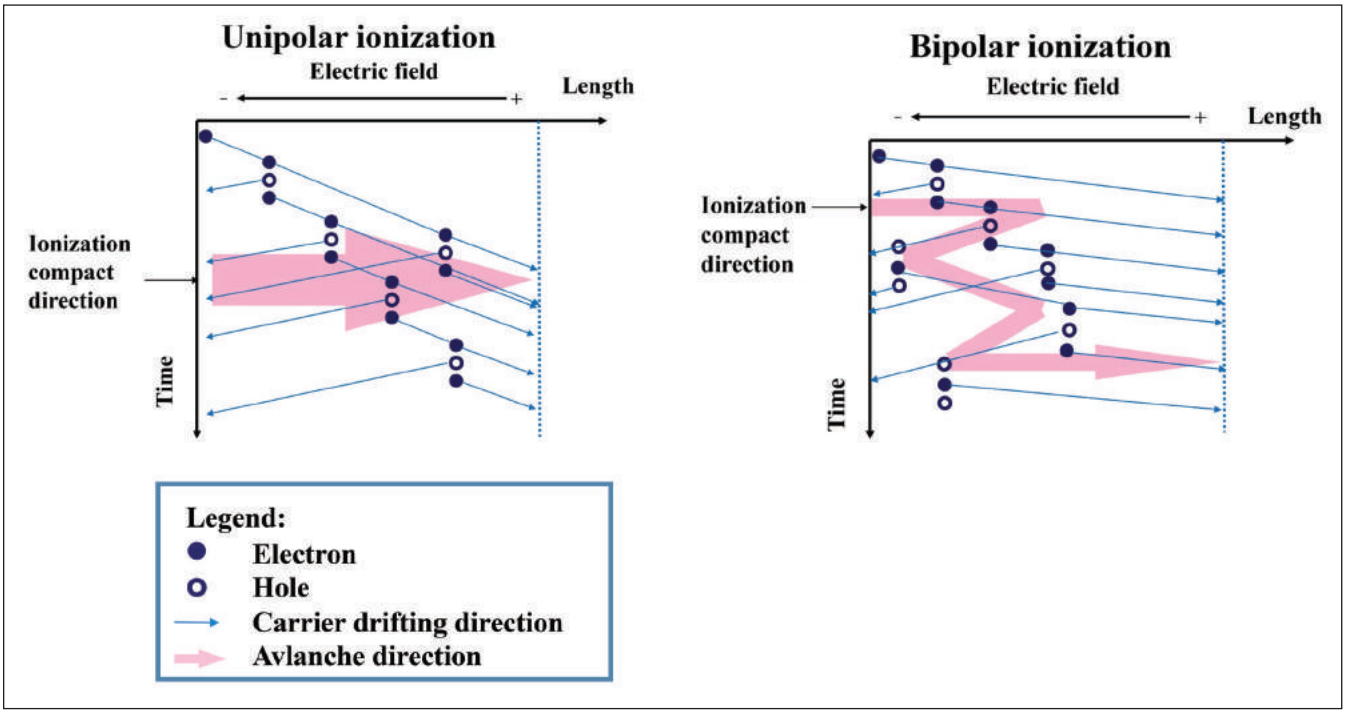


Figure 1. Unipolar ionization and bipolar ionization. (a) In a unipolar ionization APD, only one kind of carrier can trigger ionizations. Avalanche proceeds unidirectionally. (b) In a bipolar ionization APD, all carriers can trigger ionization. Avalanche proceeds bi-directionally. The solid and hollow circles represent electrons and holes, respectively; and the small and large arrows represent the carrier drifting direction and the avalanche direction, respectively.

conduction band and valence band profiles, narrowing the ionization region, and turning to impact ionization engineering.

With the first of these, suitable materials are silicon, InAs and HgCdTe. For these semiconductors, the first energy valley of the conduction band is very deep, and electrons traversing it can increase in energy, triggering ionizations without inter-valley scattering. This means that the ionized electrons have far higher energies than the holes in this material. In these devices, gain is relatively high – but it is not high enough. If the APD is made from silicon, the effective mass for the conduction band is relatively large, inner-valley scattering cannot be ignored, and the efficiency of electron-triggered ionization is not high enough; and if this device is made from InAs or HgCdTe, the narrow bandgap leads to a risk of Zener breakdown, particularly under high electric fields. What's more, the gain is not that high.

The second option, narrowing the ionization region, can be accomplished with the 'dead space' effect. By localizing the position for ionization, triggering of ionization is restricted to just one type of carrier. There is a price to pay, however – limited ionisation time, and ultimately diminished gain.

The third approach is impact ionization engineering, a technique that involves deploying periodic doping layers and heterojunctions. Here, the challenge is that the active region for ionization is so thick that it is hard to grow many cycles. Gain is limited to around 1000.

If commonly used semiconductors are adopted to construct APDs with either a conventional homojunction or an impact ionization engineering architecture, inter-valley scattering disrupts the transport of carriers. This prevents them from hitting the ionization threshold energy, resulting in a low ionization coefficient.

However, it is possible to overcome scattering and realise a high gain with the GaN material system. For both GaN and AlN, there is a deep Γ valley with a depth of about 2 eV in the first conduction band, and no such valley in the valence band. Due to this, electrons transporting within the Γ valley of either GaN or AlN experience a relatively weak scattering.

When using GaN to make an APD, the ionization threshold energy for electrons is 5.3 eV. Although this is significantly higher than the depth of the Γ valley, the conduction band offset between GaN and AlN is 2 eV. So, when electrons travel from GaN to AlN, along the (0001) direction, they enter into the Γ valley of AlN and are given an increase in energy to more than 4.0 eV. As this is quite close to the ionisation threshold, only moderate electric fields can trigger ionization impact.

We are pioneering the development of this APD architecture, using a GaN/AlN periodically stacked structure to realize controllable electron multiplication

(see Figure 2 (a) for the bandstructure of our device). To kick-start this effort, we used Monte Carlo simulations based on first-principle theory to model the behaviour of both a conventional GaN-based heterojunction APD and our novel variant – it has a periodic structure, containing alternating AlN and GaN layers with a thickness of 10 nm.

Simulations suggest that our new device delivers a tremendous hike in the ionization coefficient for electrons, while realising a negligible increase for holes. When the electric field exceeds 2.8 MV/cm, the electron ionization saturates at around 3.96×10^5 cm^{-1}. Under these conditions, the probability of electron-triggered ionization within each 20 nm-thick GaN/AlN period is nearly 80 percent. Such a high ionization coefficient has never been realized in APDs with either heterojunction or impact ionisation engineering structures.

To validate the capability of this APD, we have built a prototype that features 20 periods of 10 nm-thick GaN and AlN layers. This replaces the conventional multiplication layer in a GaN-based, *p-i-p-i-n* device with separate absorption and multiplication regions.

A Riber 32 P MBE reactor was used to grow this structure on a 2-inch, *c*-plane template produced by Suzhou Nanowin Science and Technology. On this foundation, a 4 μm-thick AlN layer on sapphire, we grew a 50 nm-thick AlN layer, followed by a silicon-doped 500 nm-thick GaN layer, 20 periods of GaN (10 nm) and AlN (10 nm), a magnesium-doped 10 nm-thick GaN layer, a 300 nm-thick non-intensively-doped GaN layer and 100 nm-thick magnesium-doped GaN. Cross-sectional transmission electron microscopy reveals that the layers are uniform, with a thickness that coincides with the designed value (see Figure 2 (b)).

To prevent edge leakage and breakdown, we create a double-mesa architecture, using inductively-coupled-plasma, dry etching. The mesa has an outer diameter of 35 μm, and an inner diameter of 25 μm that

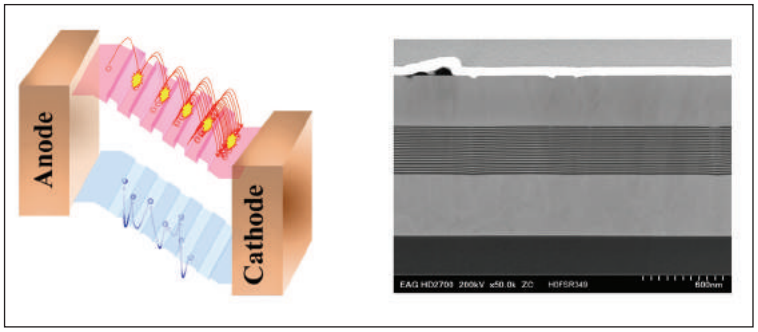


Figure 2. (a) Applying a relatively weak field to an APD with a periodically stacked GaN/AN structure allows electrons to reach the ionisation threshold of 5.3 eV. (b) Transmission electron microscopy reveals the high quality of this MBE-grown structure.

provides the light absorption surface. A layer of SiO_2 is added by plasmas-enhanced CVD to passivate the device. A *p*-type transparent ohmic contact is formed from Ni (2.5 nm)/Au (8 nm), and an *n*-type ohmic contact is created with Cr (25 nm)/Au (200 nm). A 100 nm-thick layer of gold provides the electrode pads that complete device fabrication (see Figure 3 (a)).

We have evaluated the performance of our APDs by measuring current-voltage curves, in the dark and under illumination, with an Agilent Type 4155C semiconductor analysis meter. Illumination of the front of our chip comes from a 350 nm source, with emission from a xenon lamp directed through a monochromator. The light power density is 51 $\mu W/cm^2$, equating to 250 pW of power coupled into the chip.

Unlike conventional APDs, the external quantum efficiency of our device increases steadily with bias voltage (see Figure 3 (b)). Gain saturates at 1×10^4. This number can be expressed as about 2^{14}, implying that photon-generated electrons are repeatedly multiplied at least 14 times during a single-pass transport. From this data we can determine that the probability for electron-triggered ionization at each period of the APD is about 70 percent. This is quite close to the simulation result of 80 percent at the

This collection of results demonstrates that electron-triggered ionisation in our GaN/AlN APDs is highly-efficient and controllable. What's more, even better performance is possible. Since the electron ionization coefficient is extremely high, and the multiplication performance is determined by the number of GaN/AlN stacks, simply increasing the number of periods of GaN and AlN, or optimising their thicknesses, should yield a higher gain

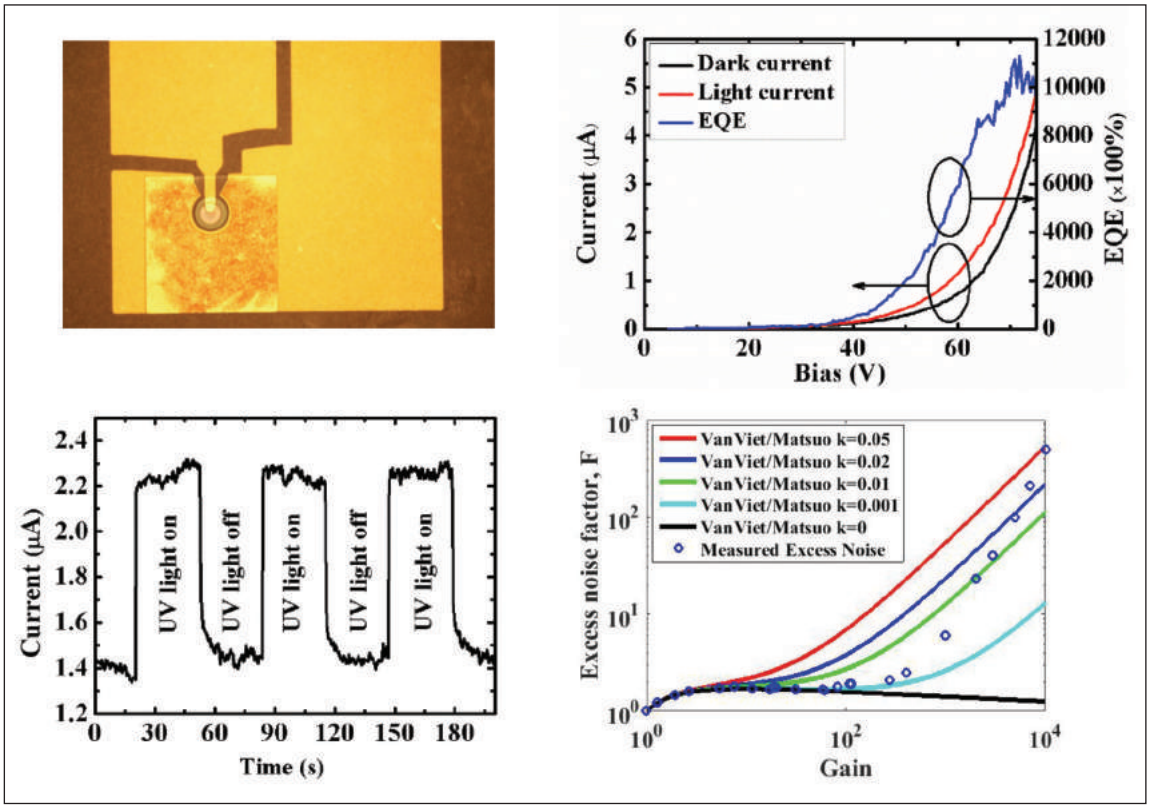


Figure 3. (b) The GaN/AlN periodically stacked APD features a double-mesa design. (b) I-V curves and external quantum efficiency (EQE) of the device. (c) Response of the device under constant bias. (d) Excess noise of the APD under different values of gain.

saturation electric field.

To confirm that our APD can work under constant bias with high gain, we have recorded the room-temperature response under a constant bias of 65 V (see Figure 3(c)). This current responds well with the switching on and off of the incident ultraviolet light, while the external quantum efficiency hits 10^4. This result showcases the superiority of our APD, as conventional devices working under constant bias cannot reach such high gain.

This collection of results demonstrates that electron-triggered ionisation in our GaN/AlN APDs is highly-efficient and controllable. What's more, even better performance is possible. Since the electron ionization coefficient is extremely high, and the multiplication performance is determined by the number of GaN/AlN stacks, simply increasing the number of periods of GaN and AlN, or optimising their thicknesses, should yield a higher gain. An additional insight into the workings of the APD is provided by analysing excess noise (see Figure 3 (d)). Evaluating the ionization coefficient ratio *k*, by comparing the excess noise with data calculated by the VanVliet/Matsuo model, using different fitting parameters of *k*, shows that ionization originates purely from electrons – that conclusion can be drawn, because the excess noise factor fits well with the curve for a value of *k* of zero, when the gain is below 100.

For a gain that is higher than 100, there is a slight feedback from holes during the ionization process. However, even when the gain is as high as 10,000, the value of *k* is still just 0.05, which is comparable to the value for a silicon APD working under linear mode. That's not to say, however, that performance is similar: our APDs deliver a better linear performance, because their gain is over 10,000, while for silicon it is only about 100. When gain is 10,000, the excess noise factor is only 500.

Our results are very encouraging for the future of low-light signal measurements. They show that there will come a time when there is no need to select between fragile, bulky photomultiplier tubes and APDs that are difficult to control, thanks to our development of high-performance, periodically stacked structures based on the pairing of AlN and GaN.

Further reading

J. Zheng et. al. Appl. Phys. Lett. **109** 241105 (2016)
J. Zheng et. al. Sci. Rep. **6** 35978 (2016)

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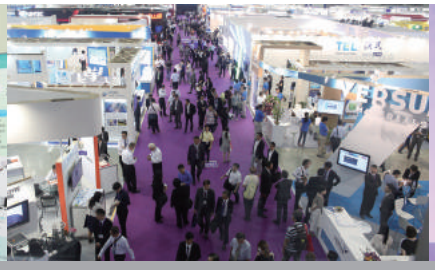
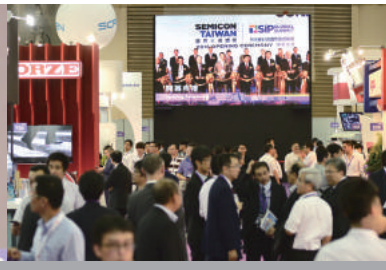




DESPITE THE RAPID GROWTH in solid-state lighting, the backlighting of displays remains a substantial market for the LED. For more than a decade, screens have been illuminated with these devices – initially housed in a traditional package, and more recently the chip-scale package – and they are now the omnipotent lighting source in LCDs.

A related success story for the packaged LEDs is as the illumination source in large video billboards, which are a common sight in stadiums, malls and video facades. Here, discrete-packaged LEDs containing red, green and blue chips form individual pixels, with pitches typically ranging from 1 mm to 40 mm, depending on the size of the display and its resolution.

As of today, LEDs have never been used as the direct emissive element – that is the pixel – in small-pitch consumer displays. Many issues prevent this from happening, including concerns related to cost and manufacturability. However, the idea of building a display with microLEDs and sub-millimetre pixel pitches can be traced back to the time when the LED was in its infancy.

Is the microLED

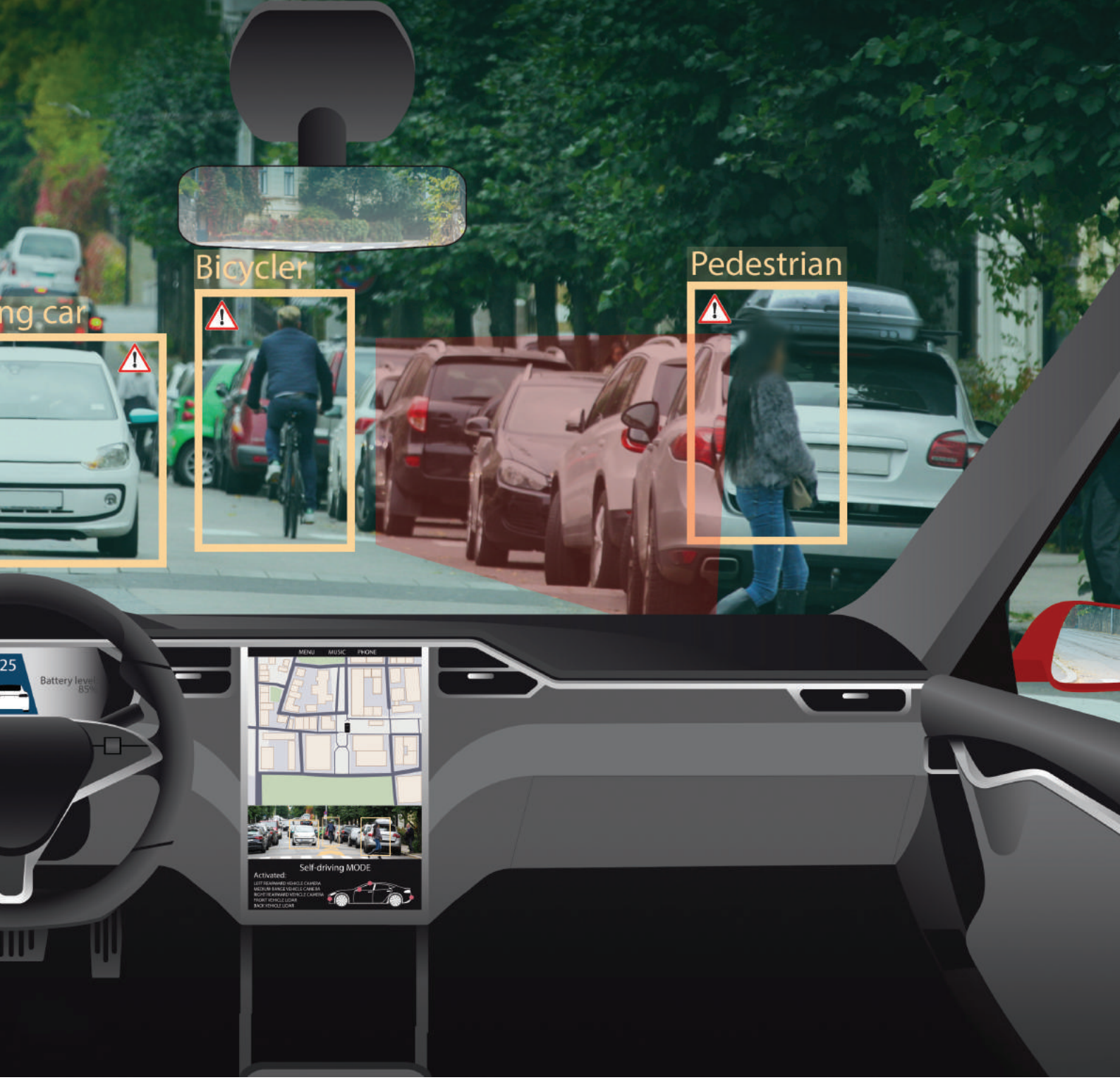
the next display revolution?

Displays based on microLEDs combine exceptional contrast with a vast colour gamut, tremendous brightness and a great deal of ruggedness, but will production be held back by their complexity?

BY ERIC VIREY FROM
YOLE DÉVELOPPEMENT

During the last five years, interest in developing microLED-based displays has taken off. In 2014, excitement in the tech and display communities skyrocketed after Apple acquired Luxvue, a microLED display start-up. Last October, Oculus, the augmented reality/virtual reality (AR/VR) arm of social networking behemoth Facebook, bought microLED start-up InfiniLED and this May, Sharp, now part of the Hon Hai Foxconn group acquired eLux, another microLED outfit.

Given these acquisitions, the technology is not just a lab curiosity. What is driving this tremendous interest by consumer electronic OEMs and leading brands? It is that this technology, which features individual red, green and blue sub-pixels as independently controllable light sources, is capable of forming displays with high contrast, high speed, and wide viewing angles – attributes also found in the pricey OLED displays.



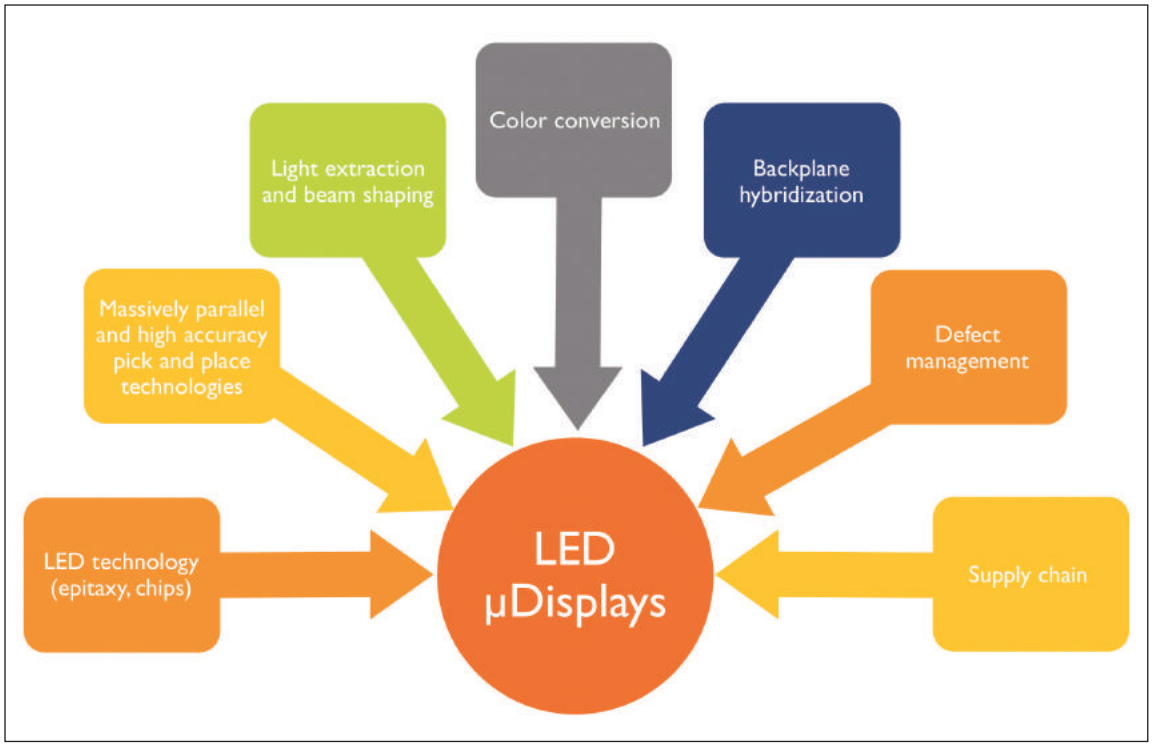
In fact, microLED displays should have the upperhand over OLED rivals, thanks to a wider colour gamut, a brightness that is orders of magnitude higher, a significantly reduced power consumption, a longer lifetime, greater ruggedness and superior environmental stability. What's more, as illustrated by Apple's recent patent filings, microLEDs could allow the integration of sensors and circuits, enabling thin displays with embedded sensing capabilities, such as fingerprint identification and gesture control.

Although microLEDs are still to reach the market, they are far more than just an idea on a drawing board. Back in 2012, at the Consumer Electronic Show, Sony showcased a full HD 55-inch television that featured microLEDs. This display, which received rave reviews from video enthusiasts walking by the booth, contained 6.2 million sub pixels – each an individually controllable microLED chip. However, Sony was noncommittal regarding a commercialisation timeline, and as of today, no microLED TV has ever made it into market.

An inherently complex technology

Today, there isn't a commonly accepted definition for microLEDs. However, in general, they are considered to be LED die with a total surface less than 2500 μm^2. This corresponds to a 50 μm x 50 μm square, or a circular die with a diameter of 55 μm. Based on this definition, microLEDs are on the market today – they were unveiled again by Sony, in 2016, in the form of a small-pitch, large LED video wall, with traditional packaged LEDs replaced by microLEDs.

The big question for both the LED and display industries is this: how far off is the small-pitch,



Multiple challenges must be overcome before it is possible to realise the potential of microLEDs.

consumer microLED display? It is this that can target cell phones, smartwatches, TVs, laptops and, more recently, virtual, augmented, and mixed reality, head-mounted devices.

Getting there will not be easy. The art of making microLED displays involves processing of a bulk LED substrate into an array of microLEDs that are poised for pick-up and transfer to a receiving substrate, for integration into a heterogeneously integrated system: the display, which integrates LEDs, pixel-driving transistors, optics and so on. The epiwafers accommodate hundreds of millions of microLED chips, compared to just thousands for traditional LEDs.

There are two leading options for realising a display with microLEDs. One is to pick up and transfer the microLEDs individually, or in groups, onto a thin-film transistor driving matrix that is similar to the ones already used in OLED displays; and the other is to unite a full monolithic array of hundreds of thousands of microLEDs with a CMOS driving circuit.

If the first of these two approaches is adopted, assembling a 4K display requires picking up, positioning and individually connecting 25 million microLED chips (assuming no pixel redundancies) to the transistor backplane. Manipulating such small devices with traditional pick and place equipment produces a processing speed of around 25,000 units per hour. That's far too slow – assembling a single display would take over a month.

To address this concern, companies such as Apple, X-Celeprint and dozens of others have developed massively parallel pick and place technologies. They can process tens of thousands to millions of microLEDs simultaneously. However, when microLED sizes are just 10 μm, handling and positioning them with sufficient accuracy is very challenging.

There are also issues to overcome with the LED chip. When its dimensions are very small, its performance is held back by nefarious sidewall effects related to surface and subsurface defects, such as open bonds, contamination and structural damages. These imperfections lead to a hike in non-radiative carrier recombination. Sidewall effects can extend over distances similar to the carrier diffusion length, typically 1 μm to 10 μm: that's not a big deal in conventional LEDs, which have sides of hundreds of microns, but it's a killer in microLEDs. In these devices, it can limit the efficiency of the entire volume of the chip.

Due to these flaws, the peak efficiency of a microLED is often below 10 percent – and it can be less than 1 percent when device dimensions are below 5 μm. That's far lower than the best traditional blue-emitting 'macro' LEDs, which can now produce peak external quantum efficiencies exceeding 70 percent. Making matters even worse, microLEDs often have to be operated at very low current densities. They are typically driven way below the 1-10 A cm^{-2} peak efficiency region, where traditional mid-power LEDs operate, because even at this low efficiency the LEDs are incredibly bright. If a cell phone had microLEDs operating at their peak efficiency, its display would deliver a brightness up to tens of thousands of nits, which is more than an order of magnitude higher than

the brighter phones on the market today. The screen would be so bright that it would dazzle any user bold enough to look at it.

When LEDs operate at a very low current density, their efficiency is so low that the technology cannot fulfil its promise of trimming energy consumption. Consequently, addressing this issue is a key priority for companies involved in microLEDs. Options for increasing efficiency include the introduction of new chip designs and improved manufacturing technologies. Both approaches could reduce sidewall defects and keep electrical carriers away from the edges of the chip.

Developers of microLEDs also face challenges related to colour conversion, light extraction and beam shaping. All are subjects of intense research, licensing, and merger and acquisition activities.

Another requirement for modern displays is the elimination of dead or defective pixels. It is nothing short of utopia to realise a 100 percent combined yield in epitaxy, chip manufacturing and transfer. So microLED display manufacturers must develop effective defect management strategies. They could include pixel redundancies and individual pixel repair, with the approach governed by the characteristics and the economics of the display.

Low hanging fruits

MicroLED are capable of being deployed in any display application, from the smallest to the largest. In many cases, they would be even better than the ultimate combination of LCD and OLED displays. But feasibility and economic realities will initially limit the reach of displays to devices where they offer a significant or disruptive gain in performance and functionality, at a cost that is acceptable to the product.

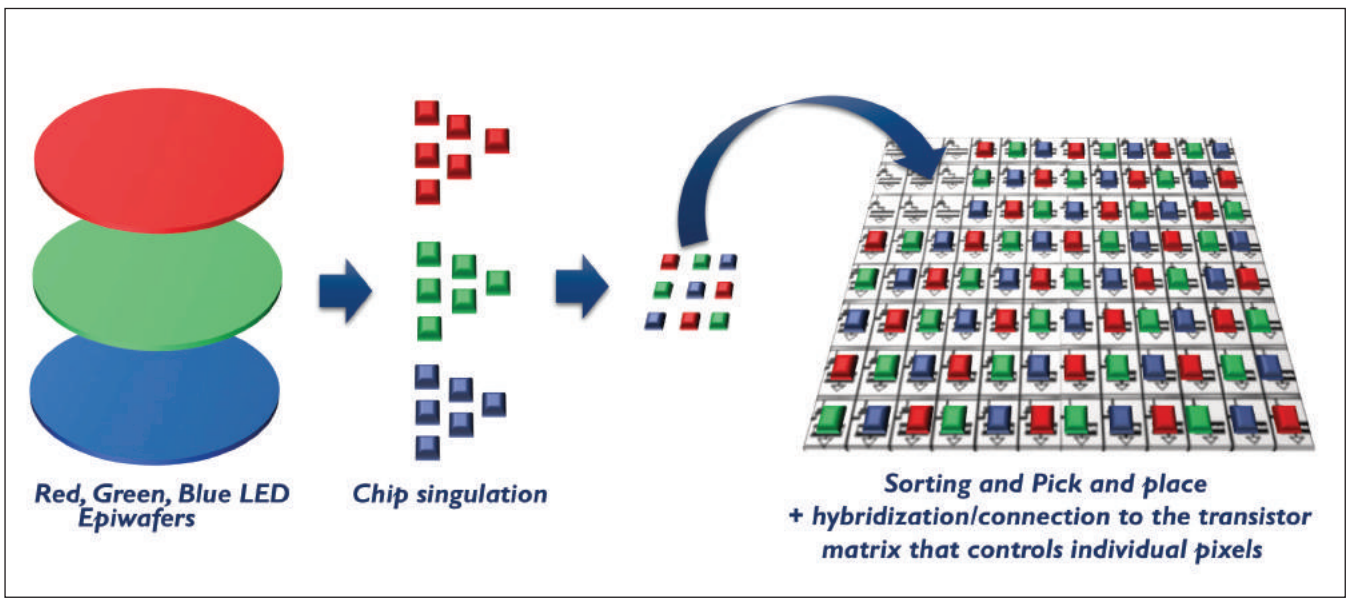
Examining in detail the strengths, weaknesses, opportunities and threats for every single application that the microLED display could serve is well beyond the scope of this article. However, detailed analysis indicates that smartwatches and other wearables, such as microdisplays for AR/MR applications, are the most likely applications to initially showcase the capability of microLED displays.

Of these, it is the smartwatch that represents the lowest hanging fruit: it has a relatively small number of pixels and a mid-range pixel density. These characteristics lead to high cost efficiency at the chip and the assembly level. Due to this, displays are nearly within reach of the current technological development status of the microLED – and they have potentially differentiating features, including a reduced power consumption that allows for a longer battery life, and a higher brightness that enables outstanding outdoor readability.

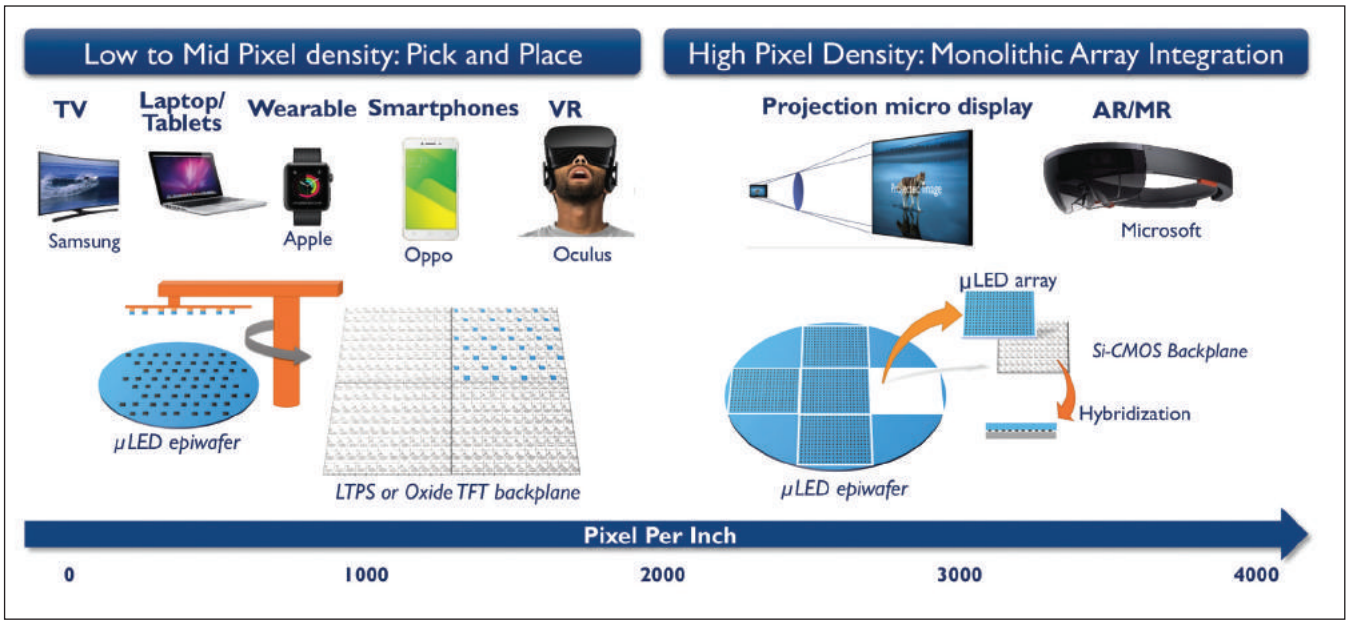
If these displays start to take off, the technology may advance, with the introduction of various sensors within the display front-plane, such as those that can read fingerprints and provide gesture recognition.

Another major opportunity for microLEDs is in augmented- and mixed-reality headsets. Unlike virtually reality, where the user wears a fully enclosed head-mounted display that visually isolate them from the outside world, AR and MR applications overlay computer-generated images onto the real world.

One of the requirements for these applications is that the overlaid image is bright enough to compete with ambient light, especially in outdoor applications. Another criterion is that the display must not be physically located in front of the eye – there it would obstruct the user's vision of the real world. To satisfy these conditions, the display must be



MicroLED displays are made by dicing wafers into tiny devices, and tranferring them with a parallel pick-and place technology to a transitor backplane.



MicroLEDs can target a range of applicatrons, which require different pixel densities.

located in an unobtrusive location, with the image projected onto the eye, using either complex projection or waveguide optics with an optical efficiency of less than 10 percent. These requirements dictate that the display brightness ranges from 10,000 to 50,000 Nits, which is more than 10 times to 50 times that of the brightness of the best cell phone on the market.

Today, the microLED is the only candidate that has the potential to offer these levels of brightness while maintaining a reasonable power consumption and compactness. Encouragingly, the same reasoning can be applied to head-up displays in automotive and other environments – this class of display can be considered as a form of AR.

A market where the microLED will struggle to make an impact is that of the smartphone. Here OLED displays are already delivering outstanding performance at a very competitive cost. If microLEDs are to be in the game, the size of the subpixel must be reduced to just a few microns. That will make it even harder to deliver acceptable efficiencies, and implement a parallel transfer approach. Success could come more easily in the TV. In this case, the drawback is that pixel densities are relatively low, with a spacing of around 100 µm in a 4K, 55-inch set. The low density hampers the efficiency of the transfer technology, because each cycle needs to move several thousand chips, rather than the hundreds of thousands needed for smartphones or smartwatches. Thriving in this market requires the development of alternative high-throughput assembly techniques.

But where's the supply chain?

There are many large companies and multiple start-ups working on microLEDs, from LED makers such as Epistar, Nichia and Osram; to display makers like Sony, AUO, BOE and CSOT; and original equipment manufacturers such as Apple and Facebook/Oculus. Undertake a thorough patent search and analyses and you'll find more than a hundred companies that have filed for patents related to microLEDs.

Success in this market requires three major disparate technologies and supply chain elements to be brought together: LEDs, thin-film transistor backplanes and chip transfer. This creates a supply chain that is more complex and involved, compared to that of traditional displays. Each process is critical, and it will be challenging to manage every aspect effectively.

No single player is going to solve all the issues, and it's unlikely that a fully integrated manufacturer will emerge. In the smaller markets, such as augmented

A market where the microLED will struggle to make an impact is that of the smartphone. Here OLED displays are already delivering outstanding performance at a very competitive cost. If microLEDs are to be in the game, the size of the subpixel must be reduced to just a few microns. That will make it even harder to deliver acceptable efficiencies, and implement a parallel transfer approach

reality, small companies could bring together the different technologies needed for the product. But that's unlikely to happen in high-volume consumer applications, such as mobiles or TVs, where a strong push from a leading OEM is probably needed to establish a supply chain. Today, Apple has enough leverage and financial strength to be able to bring all partners together. Others that might also be capable of doing this include Oculus, which has invested in microLEDs, with a focus on AR/MR applications.

Within the supply chain, each player will try and capture as much added value as possible. For LED makers, two requirements particular to the microLED – very low levels of defects and high-resolution features – imply large investments in new clean room and lithography equipment. These are criteria that might be better suited to CMOS foundries. Traditional display makers will also come up against new challenges. They are used to manufacturing back and front planes in an integrated fashion, before delivering finished panels to OEMs.

A move to microLEDs could result in these players just providing a thin-film transistor backplane to producers of the final display assembly: either OEMs or outsourced semiconductor assembly and test players. There will be some winners from the introduction of microLED displays, regardless of the shape of the supply chain. Equipment manufacturers, including makers of MOCVD equipment, will increase their sales, as will suppliers of wafers.

How long will we have to wait until we see the first consumer applications? The science is established, but the microLED is an inherently complex display technology, with cost drivers different to those of incumbents, namely LCD and OLED displays. Based on the latest developments, and the level of maturity in the supply chain, it will be 2019 at the very earliest before a high-volume application hits the market.

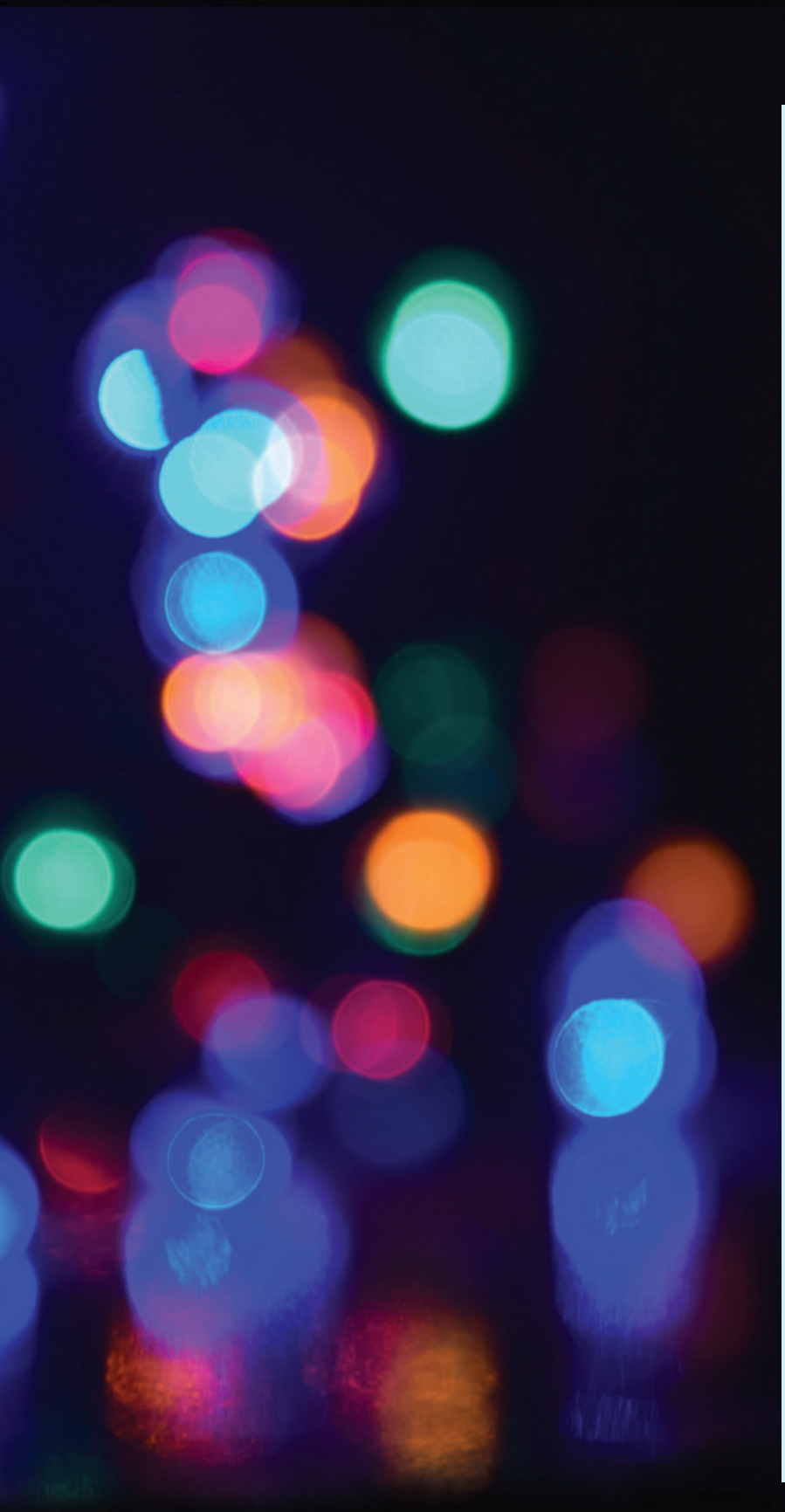
There is a good chance that the microLED will succeed in various sectors. However, it is still too early to say whether it will take the industry by storm, or will crash and burn like many other 'promising' technologies of the past. In any case, the vast accumulated and ongoing research and development on the topic should bear fruit and cross pollinate into other applications. It should lead to better, more efficient LEDs; high speed Li-Fi communication; and micro-device transfer technologies that aid other industries.

Market trends and figures have been extracted from the Yole Développement report MicroLED Displays (Feb. 2017)

Bridging the green gap with a new foundation

Relaxed InGaN substrates open the door to high quality lighting and full colour displays based on III-nitride LEDs

BY AMÉLIE DUSSAIGNE FROM CEA/LETI AND DAVID SOTTA FROM SOITEC



THE MAJORITY of commercial white LEDs are based on a blue-emitting chip that pumps a phosphor. This combination has generated tremendous sales, but it does have two major weaknesses: an energy loss of typically 25 percent, associated with the phosphor down conversion; and a colour rendering index that is not that high.

Both these drawbacks can be addressed by direct colour mixing, using LEDs with a variety of emission wavelengths. The ideal way to accomplish this is to use one material system that spans the blue to red, because this simplifies colour control. Do this, and the technology could also find deployment in high-brightness displays.

Fulfilling this dream is not easy, however. The main issue is the material. Although the InGaN alloy can theoretically cover the whole visible range, its quantum efficiency plummets above 500 nm as emission shifts from green to red. Switching to the AlGaInP material family allows the production of high-performance amber and red LEDs, but in this case efficiency takes a nose dive as emission stretches to wavelengths shorter than 570 nm.

The 500 nm to 570 nm spectral range, where it is difficult to realise efficient emission, has its own name: the green gap. For GaN-based LEDs, lack of success stems from a reduction in material quality with increasing indium content in the InGaN alloy. This issue can be traced back to low miscibility of indium in GaN, and the high lattice mismatch between the GaN buffer layer and the InGaN quantum wells.

Our team at CEA/Leti and Soitec has tackled this issue head on with a novel substrate technology that allows InGaN quantum wells to combine a high indium content with great material quality. This is accomplished with substrates that are better suited to the growth of InGaN than the most common one used for nitride LEDs, sapphire.

Growth of GaN-based LEDs on sapphire often begins with the deposition of a GaN buffer layer. That's not a great start, as the buffer layer leads to strong compressive strain. Making matters worse, when InGaN quantum wells are added, the strain gets even higher. Compounding these

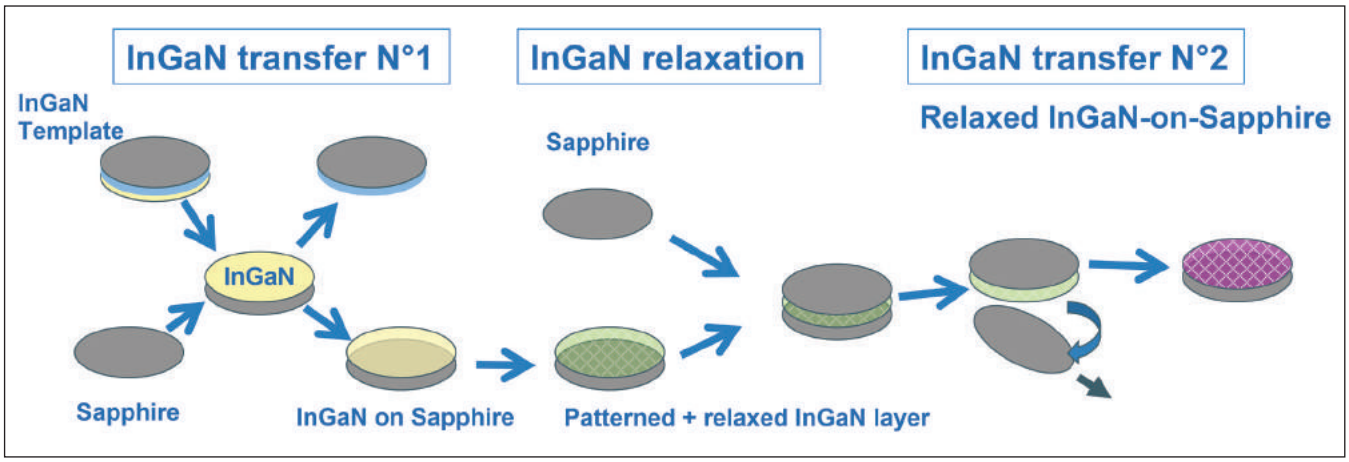


Figure 1. The fabrication process for making InGaNOS substrates helps to increase the emission wavelength of InGaN-based quantum wells.

issues, internal electric fields in the InGaN/GaN heterostructures hamper LED efficiency when wells are widened, or indium content increased.

The electric field can be eliminated by switching to non-polar GaN planes. But it's not a great solution, as more indium is needed to realise the same emission wavelength.

If concerns over electric fields are put to one side, and the focus placed on limiting the strain, one way forward is to insert AlGaN layers in an InGaN buffer or an InGaN active zone. This has been tested, but no reports of highly efficient LEDs have followed.

Our idea is to grow the LED on a relaxed InGaN substrate, as this reduces the strain between well and buffer. Additional merits of this platform are an increase in the indium incorporation rate and a reduction in the internal electric field for the same emission wavelength.

This particular substrate is not available - but we have something similar, an InGaN pseudo-substrate called InGaNOS, based on Soitec's Smart Cut technology. Development of this foundation, formed by transferring a thin layer of InGaN to a sapphire substrate, has been motivated by efforts to reduce the efficiency droop in high-brightness blue LEDs. However, through our work, led by CEA-LETI, we are showcasing the capability of this platform in another arena – its potential to form the base for structures emitting at long wavelengths. Emission can span blue to amber when InGaN LEDs are grown on an InGaNOS substrate, thanks to the increase in the indium incorporation rate.

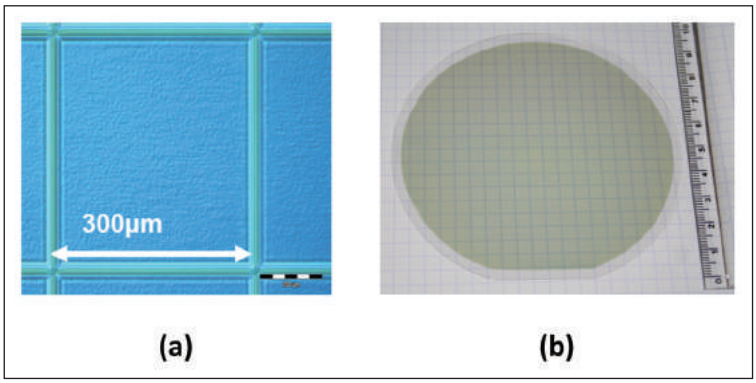


Figure 2. (a) Microscopic view of a 300 x 300 µm² pattern with a top partially relaxed $In_xGa_{1-x}N$ layer. (b) An 100 mm InGaNOS substrate with an $In_{0.08}Ga_{0.92}N$ layer and 300 x 300 µm² patterns at 3.205 Angströms. The brown area is the patterned $In_{0.08}Ga_{0.92}N$ layer.

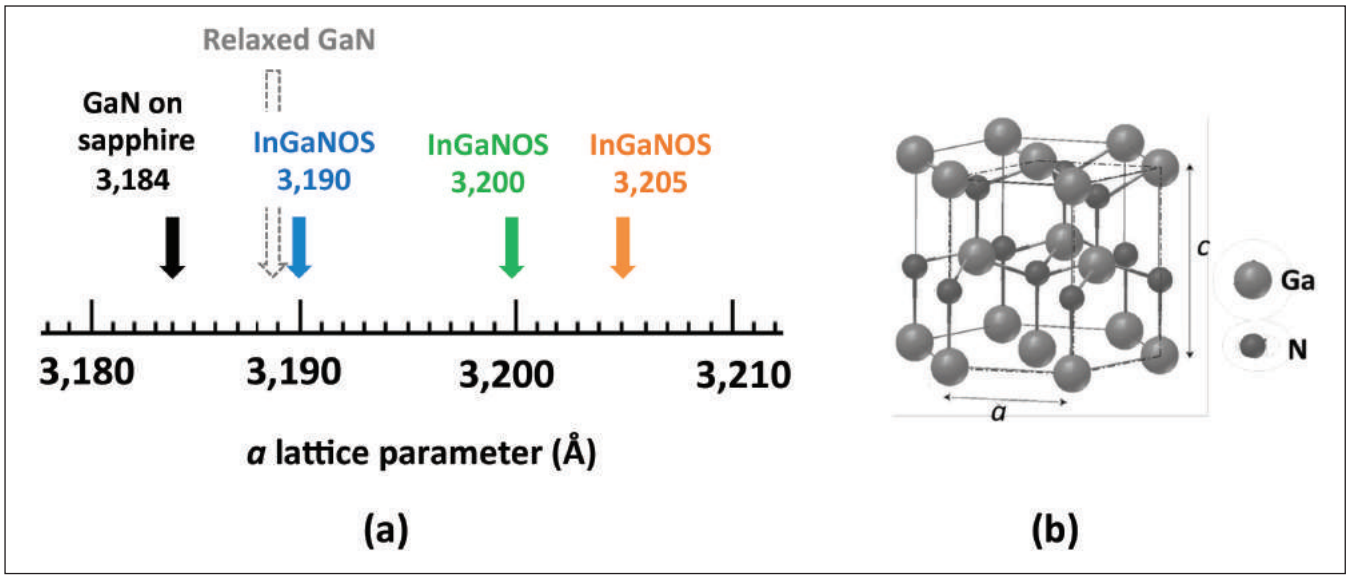
Forming the foundation

Our starting material for making InGaN pseudo-substrates is an InGaN donor template. This template is formed by growing a 3 µm-thick GaN buffer layer on a 100 mm sapphire substrate, followed by an $In_xGa_{1-x}N$ layer that is typically 200 nm-thick and has an indium content, x, of between 1.5 percent and 8 percent. This InGaN donor template, which is strained due to lattice mismatch between GaN-on-sapphire and the $In_xGa_{1-x}N$ layer, is hydrogen implanted. In parallel, a compliant layer is deposited onto a sapphire substrate, before molecular bonding unites the InGaN donor template and sapphire handle substrate.

The next step is to transfer the donor strained $In_xGa_{1-x}N$ layer to the compliant layer of the sapphire handle substrate, using Smart Cut technology. Photo-lithography and dry etching follow to create strained patterns, which are then relaxed, thanks to the compliant layer. This relaxation process proceeds via successive thermal annealings (see Figure 1 for an overview of the entire process).

It is not easy to produce a uniform relaxed $In_xGa_{1-x}N$ layer while maintaining a flat surface. A competitive relaxation mechanism is at play that can cause buckling, and lead to wavy, cracked surface. But we can avoid this by optimising the process, to produce flat patterns from 100 x 100 µm² up to 1000 x 1000 µm² and a partially relaxed $In_xGa_{1-x}N$ layer with a value of x of up to 8 percent. It is also possible to process patterns down to 10 x 10 µm² with this technology.

The relaxation process produces $In_xGa_{1-x}N$ patterns with N-face polarity. That's not ideal, as a top Ga-



face is needed for standard GaN growth. So the full patterned wafer is bonded to a second sapphire handle substrate by molecular bonding, before laser lift-off removes the first sapphire substrate.

To evaluate the roughness of our partially relaxed $In_xGa_{1-x}N$ layers, we have inspected them with atomic force microscopy. This reveals that the roughness is equivalent to that of the donor (see Figure 2(a) for a microscopic view of a 300 x 300 μm^2 pattern with a top partially relaxed $In_xGa_{1-x}N$ layer).

In the relaxation process, a key characteristic is the lattice parameter of the $In_xGa_{1-x}N$ layer. The GaN buffer fixes the strained $In_xGa_{1-x}N$ layer *a* lattice parameter of the donor at 3.184 Angström. According to the indium content of the donor and the relaxation process, the InGaNOS *a* lattice parameter can be tuned up to 3.205 Angström, with a uniformity within the wafer of +/- 0.0005 Angström.

We have used our technology to produce wafers that feature partially relaxed $In_xGa_{1-x}N$ square patterns on a sapphire substrate. The thickness of the $In_xGa_{1-x}N$ layer in each pattern is 100 nm, and it has a standard deviation of 4 nm. This level of uniformity ensures a continuous seed layer for LED growth within the pattern. The surface is epi-ready, and it has the preferred Ga-face polarity (see Figure 2 (b) for an example). Note that at Soitec, there is a InGaNOS pilot line for 100 mm and 150 mm wafers, and the technology can be scaled to 200 mm.

Multicolour emission

To evaluate the benefits of the relaxed InGaN substrate, we have characterized full InGaN structures that are grown on the InGaNOS substrates by MOCVD. The impact of lattice mismatch on indium incorporation in InGaN quantum wells is assessed with three different InGaNOS substrates – they have *a* lattice parameters of 3.190 Å, 3.200 Å, and 3.205 Å (see Figure 3). Note that no surface preparation is needed, as InGaNOS substrates are epiready.

The structure that we have grown consists of a 200 nm-thick $In_yGa_{1-y}N$ buffer layer, followed by $In_zGa_{1-z}N/In_yGa_{1-y}N$ (with z > y) active region with five quantum wells (see Figure 4).

In order to assess the impact of a relaxed InGaN substrate on the indium incorporation rate, it is imperative to apply exactly the same growth conditions to all three InGaNOS substrates. To achieve this, we co-load all the samples in the same run.

We have selected an indium content in the InGaN buffer layer of 4 percent, because this equals the average indium content in the three InGaNOS substrates. Three different growth conditions are then employed for the active region: those that we use in a conventional structure, as well as those with a higher InGaN growth rate and a lower growth temperature. The latter two variants increase indium content, and ultimately shift emission to longer wavelengths. To provide a benchmark for this study, we compare the results with a reference sample – a conventional structure that is grown on a GaN template and features GaN barriers.

Figure 3. (a) *a* lattice parameter of relaxed or strained GaN and of the three type of InGaNOS. (b) GaN wurtzite structure showing a lattice parameter position.

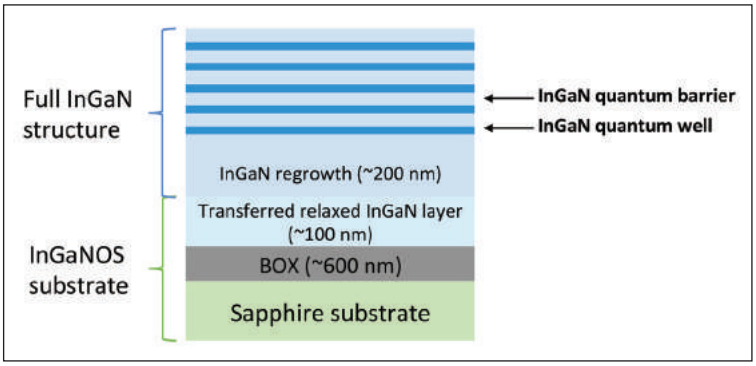


Figure 4. The full InGaN structure on InGaNOS that is used to highlight the capability of this substrate for long-wavelength emission.

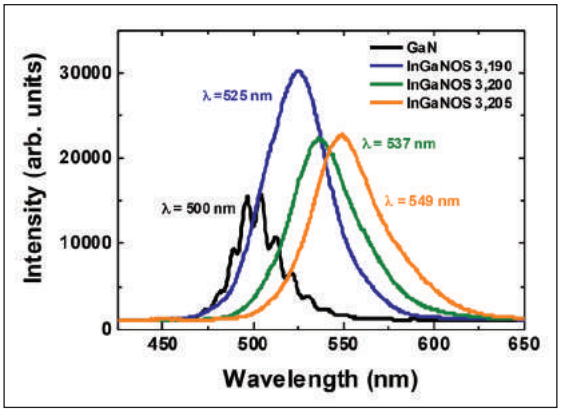


Figure 5. Photoluminescence spectra at room temperature of full InGaN structures (green conditions) grown on InGaNOS 3.190 Å (blue curve), InGaNOS 3.200 Å (green curve), and InGaNOS 3.205 Å (orange curve). The reference sample on a GaN template has been added for comparison (black curve).

The superiority of our InGaNOS substrates at incorporating indium has been validated by plots of photoluminescence redshift as a function of the InGaNOS *a* lattice parameter. Using 325 nm excitation, and measuring spectra produced by samples with just an InGaN buffer layer on either an InGaNOS substrate and on the GaN template, we have found that the higher the *a* lattice parameter, the longer the emission wavelength. According to measurements, indium content increases from 4 percent on the GaN template to 6 percent to 7.5 percent on an InGaNOS substrate. The only possible explanation for the increase in indium content is the relaxed InGaN substrate, which has a different *a* lattice parameter. This is a very encouraging result, showing that the InGaNOS substrate is beneficial at the buffer stage, even for low indium content.

After this, we went on to measure the spectra produced by our $In_zGa_{1-z}N/In_yGa_{1-y}N$ multi-quantum wells, using excitation at 405 nm, because this directly pumps the active region. Results show a red shift as high as 62 nm when the active region is grown in a conventional manner on the InGaNOS substrate, rather than a GaN template (see Figure 5 for an example in green range).

Whether the quantum well is emitting in the blue, green or amber, there is a significant red-shift in emission wavelength with an increase in the InGaN *a* lattice parameter (see Figure 6 (a)). Note that it is easy to obtain amber emission at 594 nm with InGaNOS 3.205 Å.

With all these InGaN-based heterostructures, the internal electric fields can cause a red-shift in emission with increasing quantum well thickness, even if the indium content is maintained. According to transmission electron microscopy, our samples have well widths of around 2.8 nm. That's a value we expected, is the same as for a conventional structure, and is thin enough to prevent the internal electric field from playing a strong role on determining the emission wavelength.

What then, must be the explanation for the redshift in emission? It is the increase in indium content with *a* lattice parameter. As the lattice mismatch between the buffer and InGaN wells is smaller with InGaNOS than it is with GaN – and with InGaNOS, the value of the *a* lattice parameter is unusually high – the indium incorporation rate is enhanced. With the relaxed InGaN buffer, the indium compositional pulling effect is diminished, allowing growth on InGaNOS substrates to incorporate more indium for the same growth conditions.

To determine the quality of our material, we have undertaken internal quantum efficiency measurements. For material emitting at 536 nm, the efficiency is 31 percent, which is a very respectable

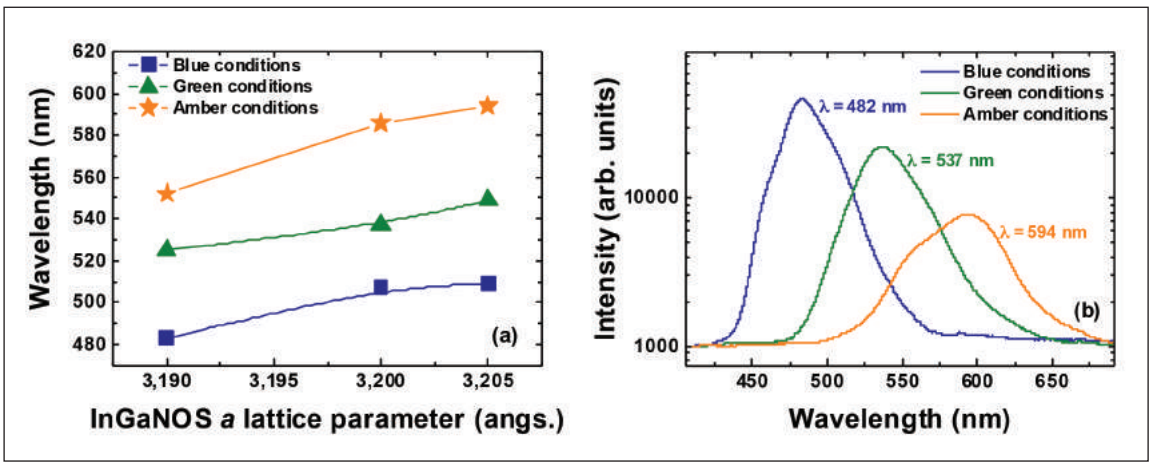


Figure 6. (a) Room-temperature photoluminescence of full InGaN structures grown on InGaNOS for emission wavelength versus InGaNOS *a* lattice parameter for the different growth conditions. (b) Photoluminescence spectra from blue to amber emission on InGaNOS 3.190 Å (blue curve), InGaNOS 3.200 Å (green curve), and InGaNOS 3.205 Å (orange curve), respectively.

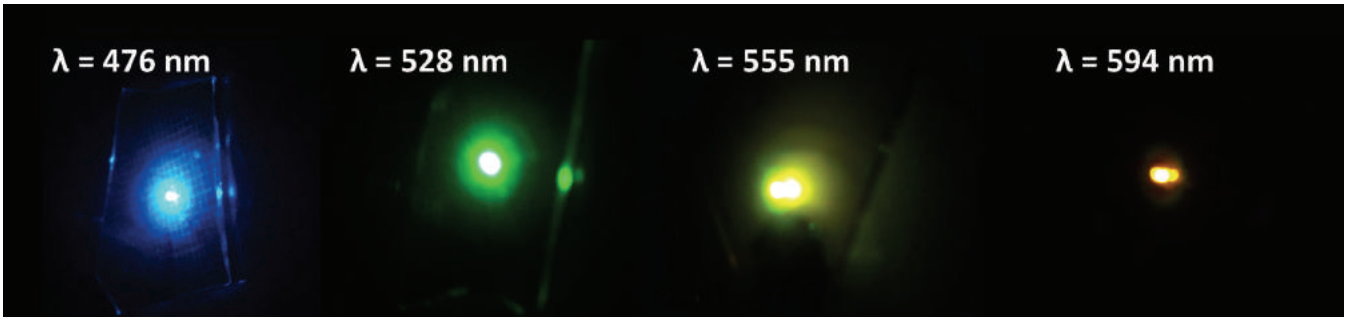


Figure 7. A full InGaN structure grown on InGaNOS samples can span from blue to amber.

value, considering that there has been no particular optimization of the structure's growth conditions. This result provides further evidence of the promise of the InGaNOS substrate and InGaN active regions, which together are capable of multicolour photoluminescence emission (see Figure 7).

Our next step, which we will soon complete, is to fabricate green LEDs with our technology. We anticipate promising results, which will take us ever closer to the use of full InGaN structures on relaxed InGaN for delivering ultra-high-quality lighting and multi-colour displays.

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Further reading

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What is to blame for the low energy efficiency of GaN-based lasers?

Why is the power conversion efficiency of the leading GaN lasers just half of that of the best LEDs?

BY JOACHIM PIPREK FROM THE NUSOD INSTITUTE LLC

Back in 2014 Shuji Nakamura received a Nobel Prize for Physics for the invention of the efficient GaN-based blue LED, a device that has enabled energy-saving white light sources. At the time he predicted that this device could soon be usurped by the GaN-based laser. But this is yet to happen – and it's not going to any time soon.

Although such lasers are being implemented in the headlights of high-end cars, such as BMWs, they are failing to make much impact in the general solid-state lighting market. That's predominantly because the blue LED's power conversion efficiency can hit 84 percent, while that for the laser is, at best, just 43 percent (the power conversion efficiency is defined as the fraction of electrical input power emitted as light output power).

If lasers are to displace LEDs in solid-state lighting, this gap will have to close. And if this is going to happen, efforts must begin with a comprehensive understanding of the physical mechanisms that are behind the low laser efficiency. At the NUSOD Institute we have been trying to do just that: read on to discover our findings.

To uncover a deeper understanding of the efficiency deficit, we have used advanced laser simulations to reproduce and analyse measured laser characteristics. These efforts have focused on a study of Panasonic's 7.2 W laser that emits at 405 nm. It delivers a record-breaking output power, due in part to a novel double-heat-flow packaging technology that trims the thermal resistance to about 7 K W^{-1}.

Another attribute of Panasonic's laser is its minimal internal optical loss (see Figure 1 for vertical profiles of refractive index and lasing mode intensity). Thanks to a small overlap between the lasing mode and the highly absorbing *p*-doped AlGaN cladding layer, the modal absorption coefficient falls to a record-low value of just 2.5 cm^{-1}.

One insight from our numerical analysis is that most of the remaining absorption is caused by free carriers inside the waveguide layers, which are located between the quantum wells and electron blocker layer (this is shown in the dashed line in Figure 1). Triggering free-carrier absorption is electron leakage from the quantum wells, which rises with increasing current injection.

Self-heating of the laser diode is behind the escalation in electron leakage. Despite the device's low thermal resistance, the temperature of the quantum well increases by 120 degrees when the injection current hits 4 A. It is well-known that self-heating is detrimental, reducing gain in the quantum well, so more carriers are required to maintain lasing (see Figure 2 for plots of laser power and carrier density with and without self-heating).

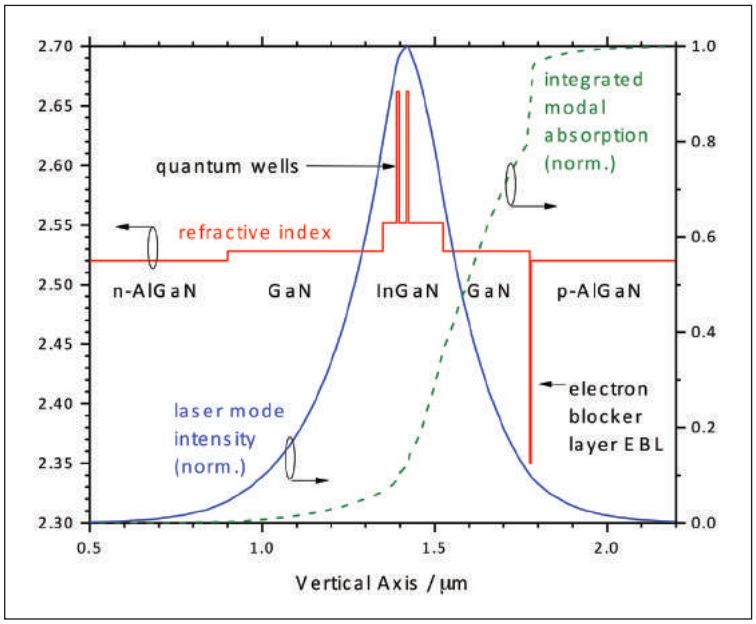

Figure 1. A vertical profile of the refractive index (red), normalized optical mode intensity (blue) and the integrated modal absorption (green, dashed) of the high-power Panasonic laser investigated by NUSOD. The internal optical wave peaks at the two quantum wells (QWs) that transform electrons into photons. But some electrons leak into the *p*-side InGaN/GaN waveguide, between QWs and the electron blocking layer (EBL), where they attract holes and cause free-carrier absorption of the laser light. The light wave suffers some more absorption in the highly *p*-doped EBL and *p*-AlGaN layer.

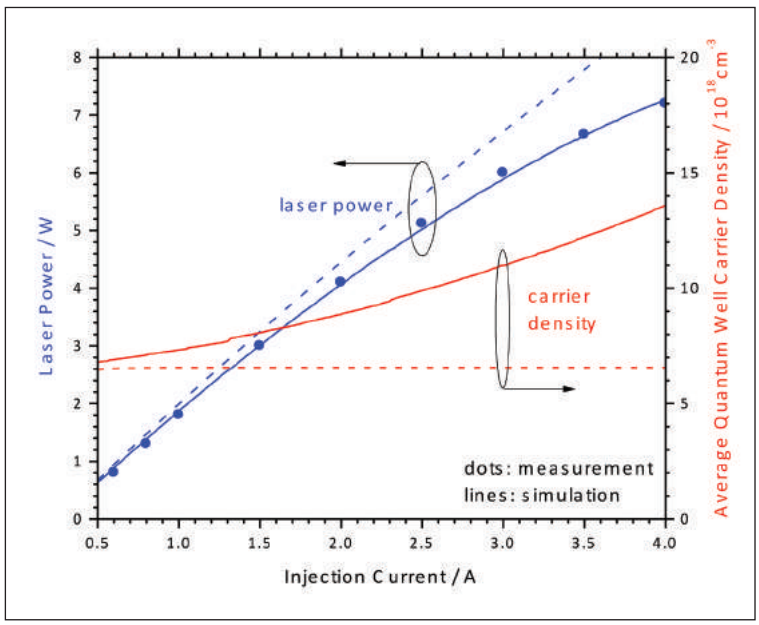

Figure 2. Laser power (blue) and quantum well (QW) carrier density (red) as a function of injection current above lasing threshold. The widely held view that the QW carrier density remains constant is only true if the internal laser temperature is kept constant (dashed lines). But high-power lasers typically suffer from strong self-heating, causing declining QW optical gain. So, QW carrier density must rise to maintain lasing, which eventually leads to a declining lasing power (dots and solid lines).

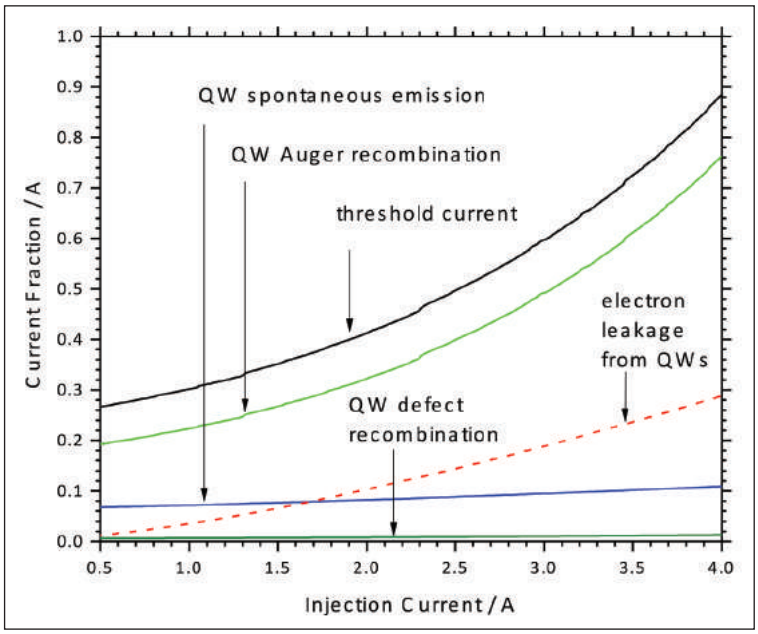

Figure 3. Simulated contributions of different carrier loss mechanisms to the total injection current. The highest loss is caused by Auger recombination (light green line), which rises most strongly with carrier density (see Figure 2). Together with spontaneous photon emission and defect-related recombination, it adds up to the threshold current, which compensates for all carrier losses inside the quantum wells (QWs). Due to self-heating, the threshold current keeps rising above the initial lasing threshold. The leakage current (dashed line) lowers the slope efficiency of the laser.

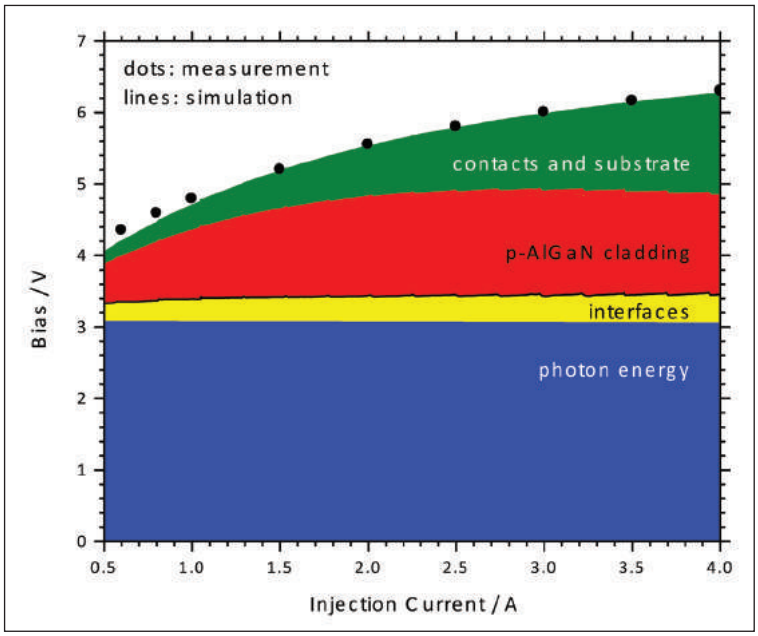

Figure 4. Contributions to the total laser bias, part of which is consumed by the photon energy of the laser light (blue area). The remaining bias is considered excess bias, attributed to the series resistance of the diode, which is dominated by the poor conductivity of the *p*-AlGaN waveguide cladding layer (see Figure 1). Simulations at NUSOD reveal that the *p*-AlGaN contribution is actually shrinking with higher current, because the higher temperature activates more free carriers from the deep magnesium acceptor levels. Hetero-interfaces create a relatively small resistance (yellow area). The remaining excess bias (green area) is mainly caused by the *p*-side contact resistance.

It is often assumed that the carrier density in the quantum well is constant. However, this cannot be the case when the temperature in the well changes. If it rises, the density of carrier increases. In turn, there is an increase in carrier losses inside the quantum wells via Auger recombination, defect-related recombination, and spontaneous photon emission. Of these three, Auger recombination rises the fastest, because it is proportional to the third power of the carrier density.

When carrier losses escalate, fewer carriers are available for stimulated photon emission, a fundamental process for laser emission. However, the threshold current compensates for all carrier losses inside the quantum wells (see Figure 3 for plots of the current components, as well as the resulting threshold current as function of the total current). Unfortunately, such a rise in threshold current is usually neglected in the efficiency analysis for high-power lasers. This has led several groups, including that of Nakamura at UCSB, to incorrectly assume that Auger recombination is irrelevant at high lasing powers.

We have also investigated the need for a high bias for GaN laser operation. For Panasonic's device, the 7.2 W output requires a 6.3 V bias – that's high, considering that only about half of this value is needed for the emitted photons (see Figure 4). So where does the rest go? It is consumed by the high series resistance, which is primarily attributed to the extremely low electrical conductivity of the *p*-type AlGaN cladding layer.

A high electrical resistance should be expected, given that hole conduction in *p*-doped layers has always been a problem in GaN-based devices. Due to the large magnesium acceptor ionization energy, the density of free holes is only about 1 percent of the acceptor density at room temperature, so magnesium has to be incorporated at a very high density. That diminishes hole mobility.

However, our numerical analysis reveals that the contribution of the *p*-AlGaN cladding layer shrinks at higher current (see the red area in our simulation results in Figure 4). This stems from the strong self-heating of the laser, which enhances conductivity by activating more free holes. In addition, there is significant contribution to the excess bias from the *p*-side contact and substrate, and a small contribution from the hetero-interfaces (see the green and yellow areas, respectively, in Figure 4).

To summarise the results of our efficiency analysis, we have plotted the contributions of the various mechanisms as a function of the drive current of the laser (see Figure 5). Device efficiency peaks at 39 percent at a relatively low current near 1.5 A, and falls as current increases. At the peak power output, 7.2 W, efficiency is less than 30 percent.

Another way to look at this is that at a drive current of 4 A, more than 70 percent of the electrical input power is wasted by various loss mechanisms. The greatest villain is Joule heating, caused by high series resistance. Second on this list is carrier losses inside the quantum wells (mainly Auger recombination), which dominate the power budget at lower currents. Additional power losses come from electron leakage and optical absorption.

What can we do about the high excess bias, which is mainly behind this high energy loss? Well, one solution, recently demonstrated by Nakamura and co-workers from UCSB, is to replace the majority of the *p*-doped waveguide cladding layer with a tunnel junction and a highly conductive *n*-doped layer (see Figure 6 for the energy band diagram of a tunnel-junction laser). With this architecture, electrons are injected from the right-hand side contact into the conduction band – and the tunnel junction transforms them into holes traveling in the valence band to the quantum wells, where they meet the electrons injected from the left-hand side, as before.

Merits of this design included the elimination of much of the *p*-cladding resistance and the high *p*-contact resistance. Thanks to this, excess bias plummets (see Figure 7). Reducing the resistance is highly beneficial, because it lowers self-heating. Consequently, fewer quantum well carriers are required for lasing, and Auger recombination falls. The upshot is that the maximum lasing power is now almost three times higher than before (see Figure 7).

With the introduction of the tunnel junction, power conversion efficiency increases to nearly 60 percent at low current – but it is only about 35 percent at peak power (see the blue area in Figure 8). Joule heating now consumes less than 30 percent of the input

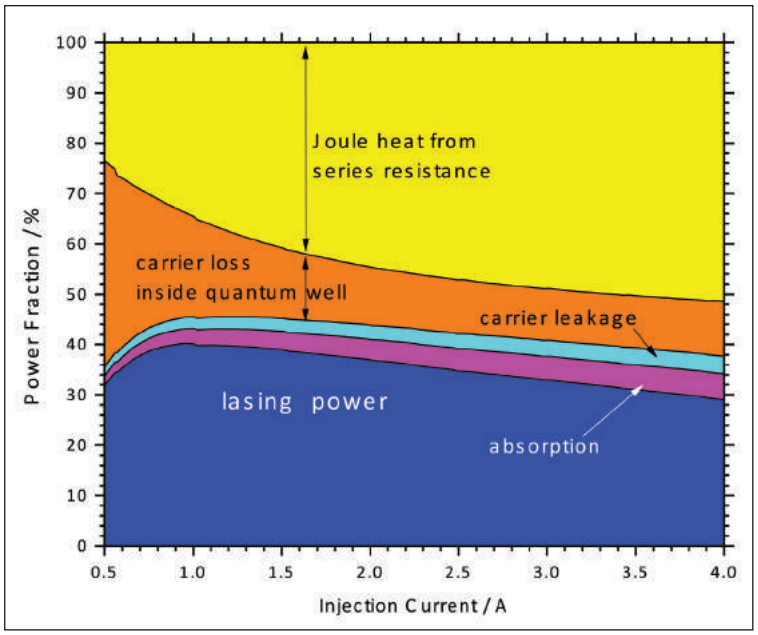

Figure 5. Relative power consumption by different mechanisms above lasing threshold. The power conversion efficiency of this laser remains below 40 percent (blue area). At low current, carrier losses inside the quantum wells consume most of the power (orange area). With increasing current, Joule heating takes over as the leading power loss mechanism (yellow area). Carrier leakage and internal absorption are less important in this case; however, other GaN-lasers exhibit much higher absorption.

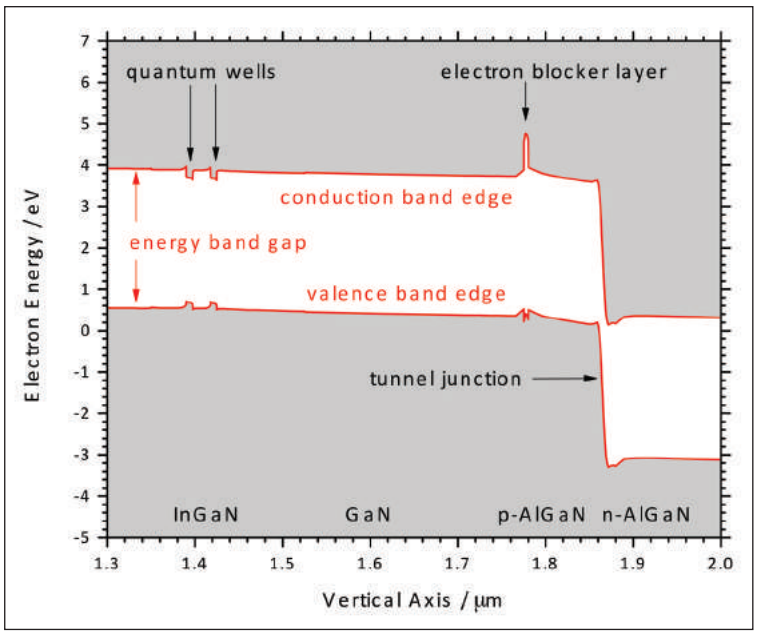

Figure 6. An energy band diagram of the simulated tunnel-junction laser. The *p*-doped AlGaN cladding layer is partially replaced by an *n*-doped AlGaN layer that exhibits a much higher electrical conductivity and a much lower contact resistance. The *p*/*n* interface is highly doped to form a tunnel junction. It allows *n*-AlGaN electrons in the conduction band to become *p*-AlGaN holes in the valence band, which eventually generate photons inside the quantum wells by recombining with electrons injected from the left-hand side.

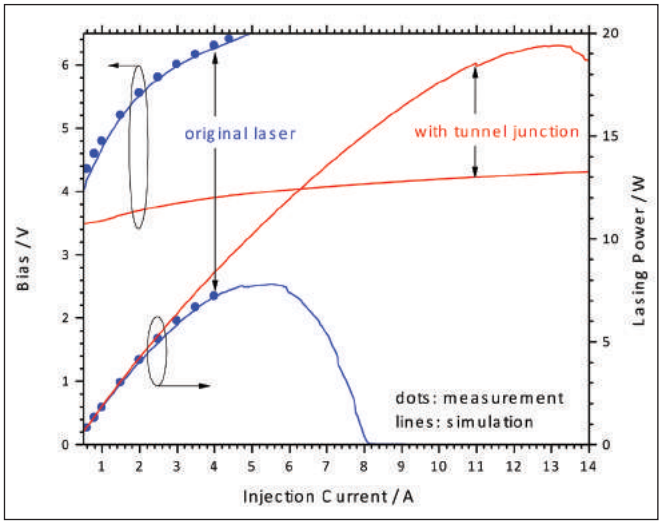

Figure 7. Performance of lasers with and without a tunnel junction. The proposed tunnel-junction laser is represented by the red lines and exhibits an almost three-times higher peak lasing power than the original device. This improvement is mainly attributed to the smaller series resistance, which lowers the Joule-heating and thereby reduces the rise of carrier density (compare with Figure 2) and threshold current (compare with Figure 3).

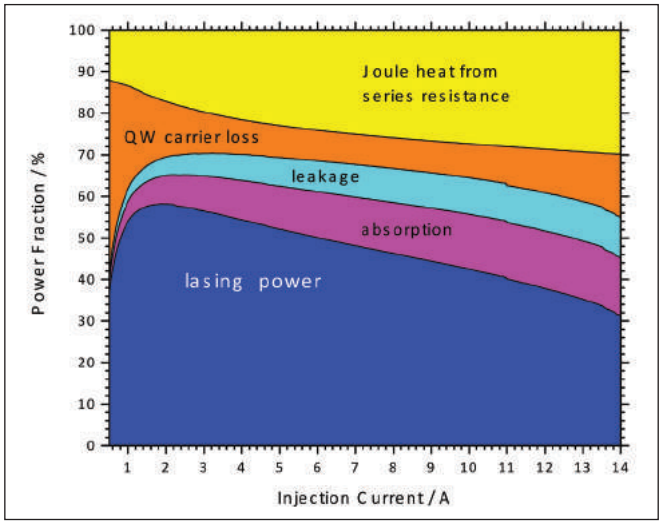

Figure 8. Relative power consumption by different mechanisms in the tunnel-junction laser above lasing threshold. Power conversion efficiency of the laser (blue area) reaches almost 60 percent at low current, but drops to 35 percent at the peak lasing power (13 A). With this design, Joule heating consumes less than 30 percent of the input power. However, due to the high doping of the tunnel junction, absorption loss has increased (pink area). Carrier loss inside the quantum wells (orange area) and electron leakage from the quantum well (cyan area) add up to about 20 percent power loss at the lasing peak.

power, but absorption loss has increased, due to the high doping of the tunnel junction. At the lasing peak, about 20 percent of the loss now comes from the wells, where carrier loss and electron leakage occur.

It is important to note, however, that lasers are usually operated well below the peak power. If this tunnel-junction device is operated at 8 A, it produces an output of 15 W at 46 percent efficiency. That's much more than the conventional device. So, while it's likely that GaN lasers will never get close to the very high efficiencies of GaN LEDs, significant improvements over today's best devices can be expected with the introduction of tunnel-junction contacts.

Further reading

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AN ANGEL EVENT

EMPOWERING SILICON WITH VERTICAL-CAVITY LASERS

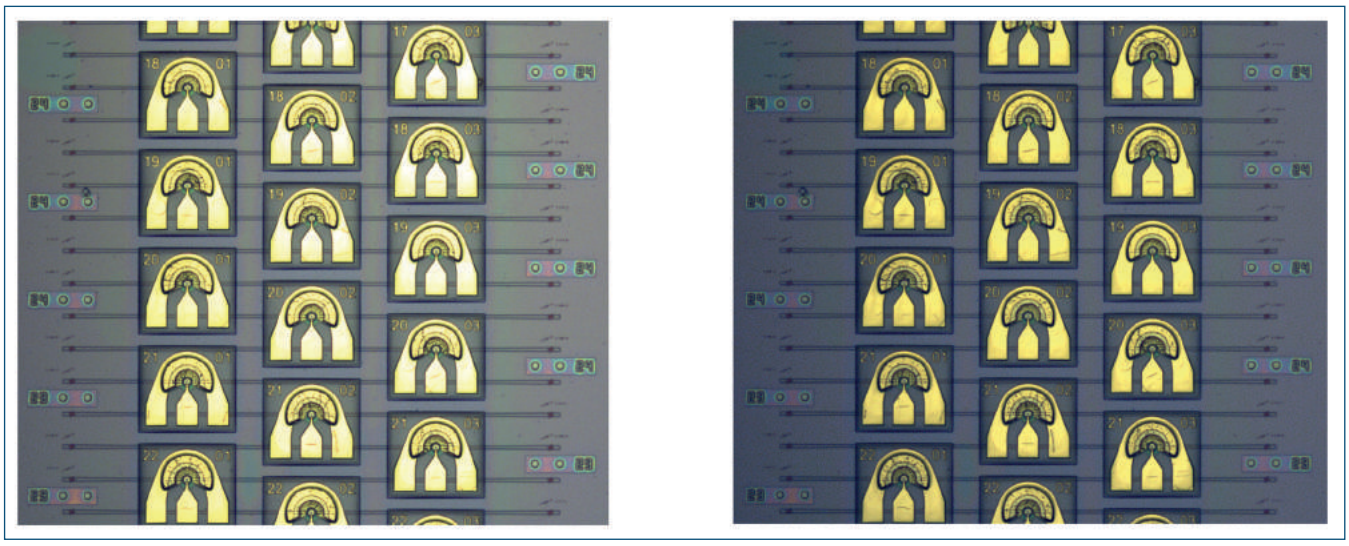
Bringing the advantages of the VCSEL to silicon photonics with vertical-cavity lasers

BY ANDERS LARSSON, EMANUEL HAGLUND AND JOHAN GUSTAVSSON FROM CHALMERS UNIVERSITY OF TECHNOLOGY, GÖTEBORG, AND SULAKSHNA KUMARI, GUNTHER ROELKENS, AND ROEL BAETS FROM GHENT UNIVERSITY-IMEC

PHOTONIC INTEGRATED CIRCUITS (PICs) have many merits. Their attributes include a high degree of functionality, a capability to realise a great deal of complexity, a small footprint and a low cost.

The two leading platforms for the production of PICs are InP and silicon. The primary advantage of the former – predominantly used in transceivers for wavelength division multiplexed telecom systems – is the monolithic integration, on a single chip, of all active and passive elements, including lasers as light sources. In contrast, the latter – commonly referred to as silicon photonics – has the advantage of a far lower propagation loss in the waveguide. With this material system, there is the benefit of the use of CMOS fabrication processes, which are suited to high-volume, low-cost manufacturing.

Waveguides for silicon photonics are often made from silicon or SiN. Silicon is transparent at wavelengths beyond 1.1 μm, so this technology, which is based on silicon-on-insulator structures, is the most common platform for telecom and datacom transceivers. If transparency in the visible range or near-infrared (below 1.1 μm) range is required, silicon is unsuitable, and SiN waveguides tend to be adopted. SiN



Arrays of hybrid vertical-cavity lasers with intra-cavity SiN waveguides

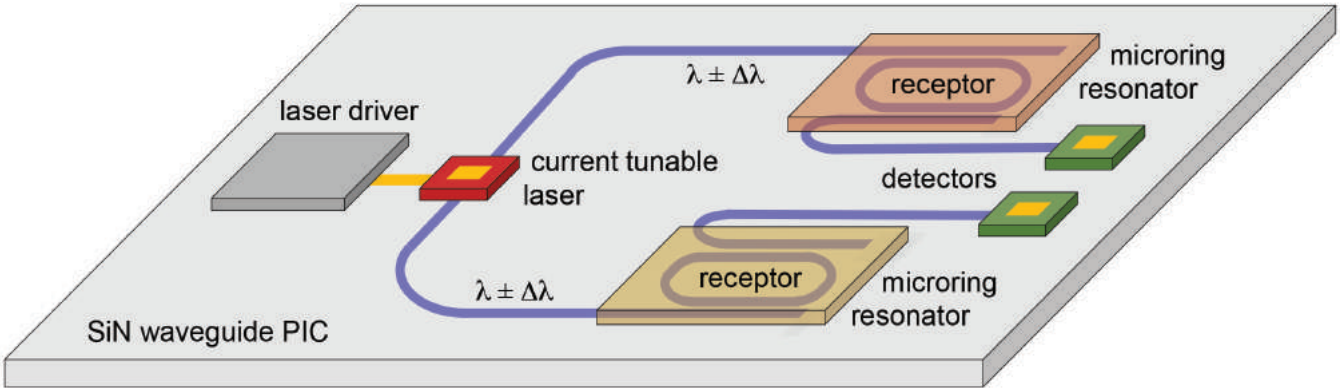


Figure 1. A bio-photonic SiN PIC sensor chip with integrated micro-ring resonators coated by receptor layers, a heterogeneously integrated current tuneable laser, and flip-chip integrated laser driver and grating coupled photodetectors.

technology is often used to fabricate PICs for bio-photonics and life sciences, where wavelengths in the visible and very-near-infrared are of particular interest.

One major challenges for any PIC made with silicon photonics is the integration of the light source. Difficulties arise from the lack of a direct bandgap for silicon and its compatible compounds, such as SiGe and SiN. A direct bandgap material is essential, as it is a prerequisite for efficient light generation and amplification.

Most of the producers of silicon PICs select one of three approaches to integrate the lasers to the chips. Their least mature option is monolithic integration, which involves hetero-epitaxial growth of compound semiconductors on to silicon. One alternative is heterogeneous integration, which involves attaching epitaxial compound semiconductor structures to silicon using either die or wafer bonding. The resulting structure is processed to form lasers, allowing the merger of otherwise incompatible materials to yield a high-performance laser. There is also a third

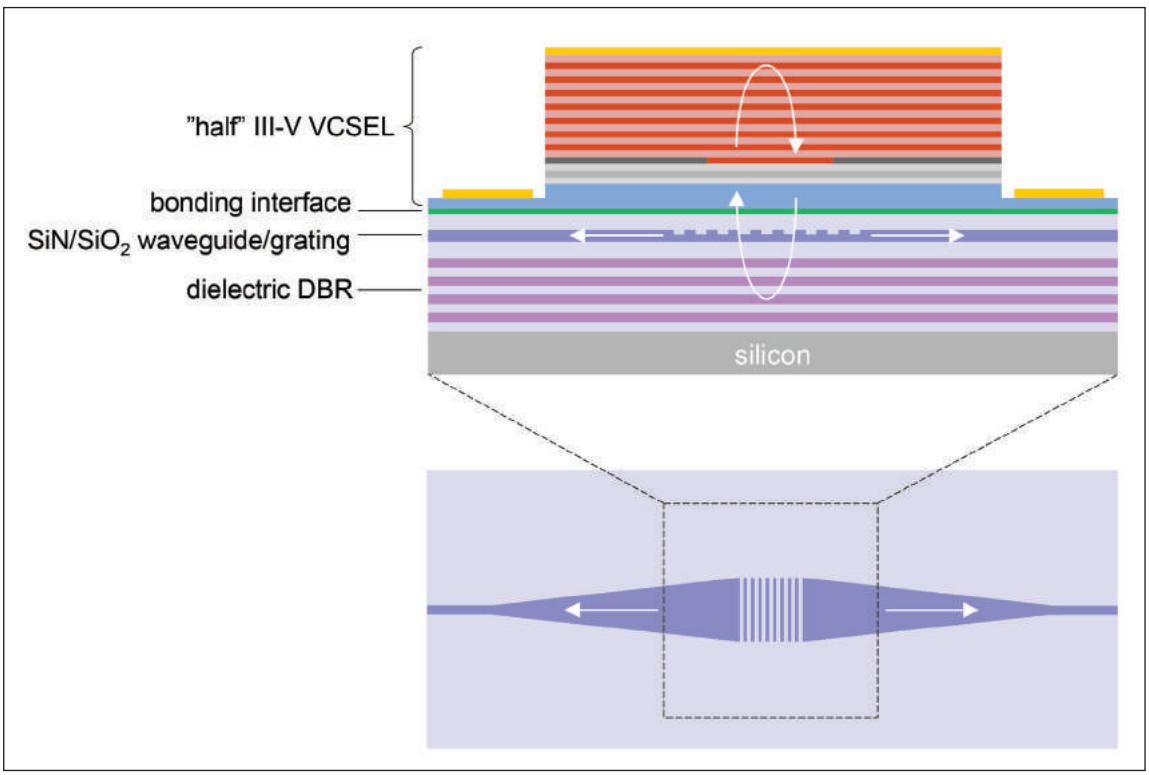


Figure 2. The concept of hybrid vertical-cavity laser integration on SiN PICs. Upper: Cross-sectional view of the 'half III-V VCSEL' bonded to a dielectric DBR on silicon with an intra-cavity SiN waveguide with a weak diffraction grating on top. During each round-trip in the vertical cavity, a certain fraction of the photons stored in the cavity is tapped off to the in-plane intra-cavity waveguide. Lower: Top view of the SiN waveguide and grating onto which the 'half III-V VCSEL' is bonded.

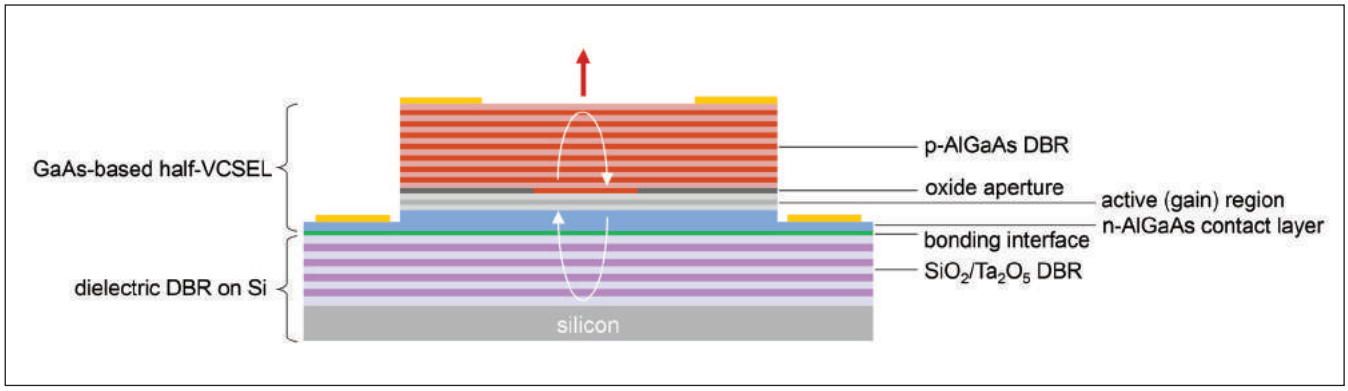


Figure 3. The GaAs-based surface-emitting version of the hybrid vertical-cavity laser, lacking the intra-cavity SiN waveguide and grating for in-plane emission.

approach: hybrid integration. In this case, light from a stand-alone laser is coupled to the on-chip silicon or SiN waveguide.

Regardless of the approach, most engineers incorporate an in-plane laser in their PIC. However, its performance is not ideal: it has high bias and modulation currents, it operates with a low power conversion efficiency, and it has a large footprint.

VCSEL virtues

For data communication, sensing and some high-power applications, the most common laser used today is not an in-plane device, but a VCSEL. Its success stems from: its small optical mode and gain volumes, enabling efficient operation and high-speed modulation at low currents; and its vertical geometry, which provides surface emission and enables dense two-dimensional arrays and low-cost fabrication and testing.

The success of VCSELs raises an obvious question: can it, or a device like it, provide the light sources for silicon photonics? If it could, it would empower silicon photonics with a class of lasers that offer a low current, a high efficiency and a small footprint.

Given all this promise, it is of no surprise that many groups have tried to develop silicon PICs that feature flip-chip integration of long-wavelength (InP-based) and short-wavelength (GaAs-based) VCSELs over optical coupling elements, such as gratings and mirrors. However, this approach does not deliver a wafer-scale process. Instead, it involves accurate, time-consuming alignment of individual VCSELs in a back-end process.

What's needed is a wafer-scale compatible process. Fulfilling this goal is our partnership between researchers at Chalmers University of Technology and Ghent University-imec. Together we have developed a process for the heterogeneous integration of hybrid vertical-cavity lasers.

At the heart of our technology is the formation of a hybrid vertical-cavity laser via the bonding of an epitaxial III-V structure – it contains the upper reflector and an active region that provides optical gain under current injection – to a lower reflector on the silicon substrate. This approach forms a hybrid vertical cavity.

With our technology, light is coupled to an in-plane silicon or SiN waveguide with an optical element in the cavity. This element taps off power to the waveguide.

Our technology is applicable to many material

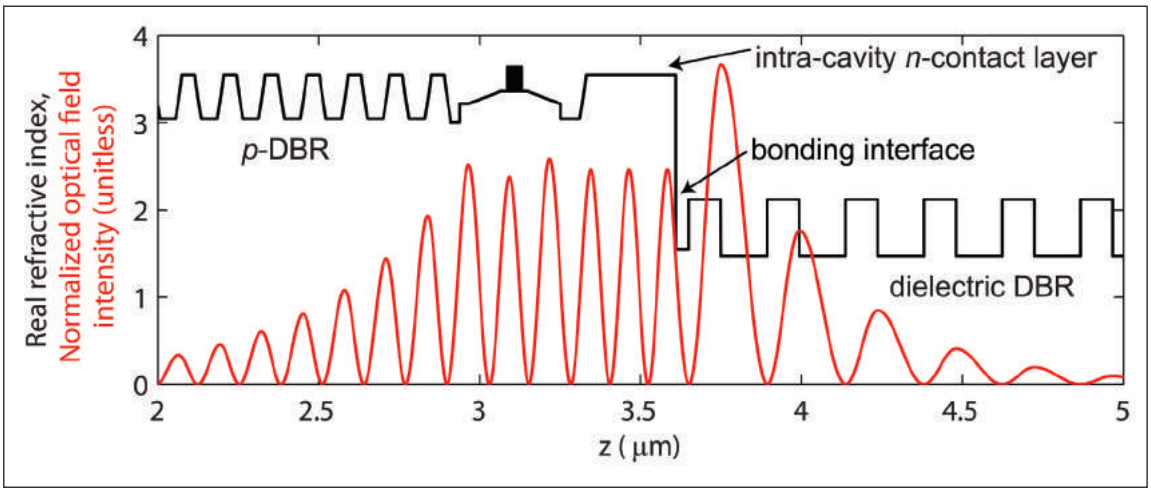


Figure 4. Optical field intensity and refractive index along the optical axis of the hybrid vertical-cavity laser.

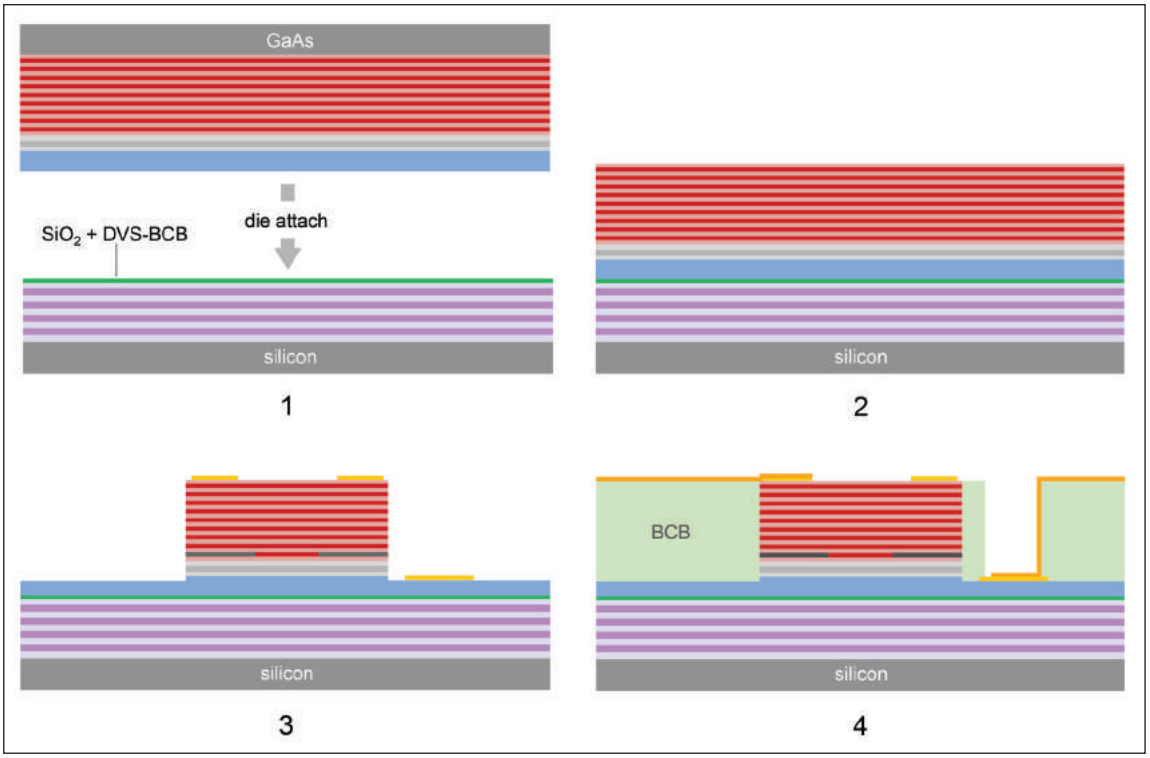


Figure 5. Illustration of the fabrication process for the GaAs-based hybrid vertical-cavity laser. (1) Bonding of III-V die on the silicon part using adhesive bonding. (2) Removal of the GaAs substrate. (3) Top contact metallization, mesa etching, selective oxidation, and bottom contact metallization. (4) Planarization with BCB and deposition of pad metals.

systems. It is compatible with GaAs, InP, and GaSb-based materials, for emission in the very-near-infrared, near-infrared, and mid-infrared, respectively; and with the development of GaN-based materials, it may become useful for visible light sources.

We are not the only team pursuing this type of approach. However, we distinguish ourselves by working with GaAs-based materials and targeting light source integration for the very-near-infrared. Meanwhile our peers, the group of Connie Chang-Hasnain at the University of California at Berkeley and the group of Il-Sug Chung at the Technical University of Denmark, use InP-based materials as near-infrared sources.

The GaAs-based, hybrid vertical-cavity laser technology that we are developing forms part of the European Horizon 2020 project PIX4life. The project, co-ordinated by imec and involving 15 partners across Europe, aims to establish a SiN PIC pilot-line for life science applications in the visible and very-near-infrared. An intended outcome of our efforts is a line that will aid product development for a broad range of industrial customers.

One example of a device developed on this line is a bio-photonic sensor (see Figure 1). This chip contains micro-ring resonators coated by receptors. The receptors selectively bind target analytes, leading to a shift in the micro-ring resonance frequency. Sensing these shifts is an on-chip current tuneable laser, which interrogates multiple sensors with different receptors. For this kind of sensing PIC, the hybrid vertical-cavity laser is potentially the ideal light source.

To enable on-chip integration of hybrid vertical-cavity lasers, we are developing an integration platform that features a dielectric distributed Bragg reflector (DBR) buried under the waveguide on the silicon substrate (see Figure 2). We accomplish this by bonding the epitaxial structure with the upper DBR and the active region to the silicon wafer to form the hybrid vertical-cavity. A shallow grating etched in the intra-cavity waveguide diffracts light to the in-plane waveguide. Note that an additional benefit of the buried DBR is that it can improve the efficiency of grating couplers used to couple light from the PIC into the likes of optical fibres or flip-chip integrated detectors.

Surface-emitting lasers

An ultimate goal of our project is to demonstrate on-chip waveguide-coupled integration of hybrid vertical-cavity lasers. However, we begin by taking a step towards this: a surface-emitting version, which is a VCSEL. By taking this route, we can develop and implement the integration architecture, and then investigate its performance characteristics and limitations.

Our intermediate structure features a SiO_2/Ta_2O_5 DBR

on silicon for the lower reflector, on which we bond a GaAs-based epitaxial structure with a *p*-type AlGaAs DBR, an active region with strained InGaAs quantum wells, and an intra-cavity *n*-type AlGaAs contact layer (see Figure 3). As is often the case for GaAs-based VCSELs, we use selective oxidation to form an oxide aperture for transverse current and optical confinement.

We have designed our hybrid vertical-cavity laser for 850 nm emission. With the design we are pursuing, the optical field extends over the GaAs-based and silicon-based parts of the hybrid cavity (see Figure 4).

Fabrication of our developmental structure begins with the preparation of its two parts (see Figure 5). They are formed by depositing the dielectric DBR on the silicon wafer and growing the epitaxial structure on the GaAs substrate by MOCVD. An additional thin layer of SiO_2 is deposited on the dielectric DBR, followed by spin-coating a film of the polymer DVS-BCB, which acts as an agent for adhesive bonding.

With our approach, the thickness of the bonding interface is defined by the combined thicknesses of the SiO_2 layer and the polymer. The polymer thickness is fixed at 40 nm, while the thickness of the SiO_2 layer is varied to control the interface thickness. Careful control of the thickness of the bonding layer is crucial, because it determines the length of the resonator and thus the emission wavelength.

After this step, dies of the GaAs-based epi-structure are bonded to the dielectric DBR on silicon, before the GaAs substrate is removed. Standard fabrication techniques for oxide-confined VCSELs are then employed, including mesa etching down to the intra-cavity contact layer, selective oxidation, and deposition of contact and pad metals. To cut capacitance,

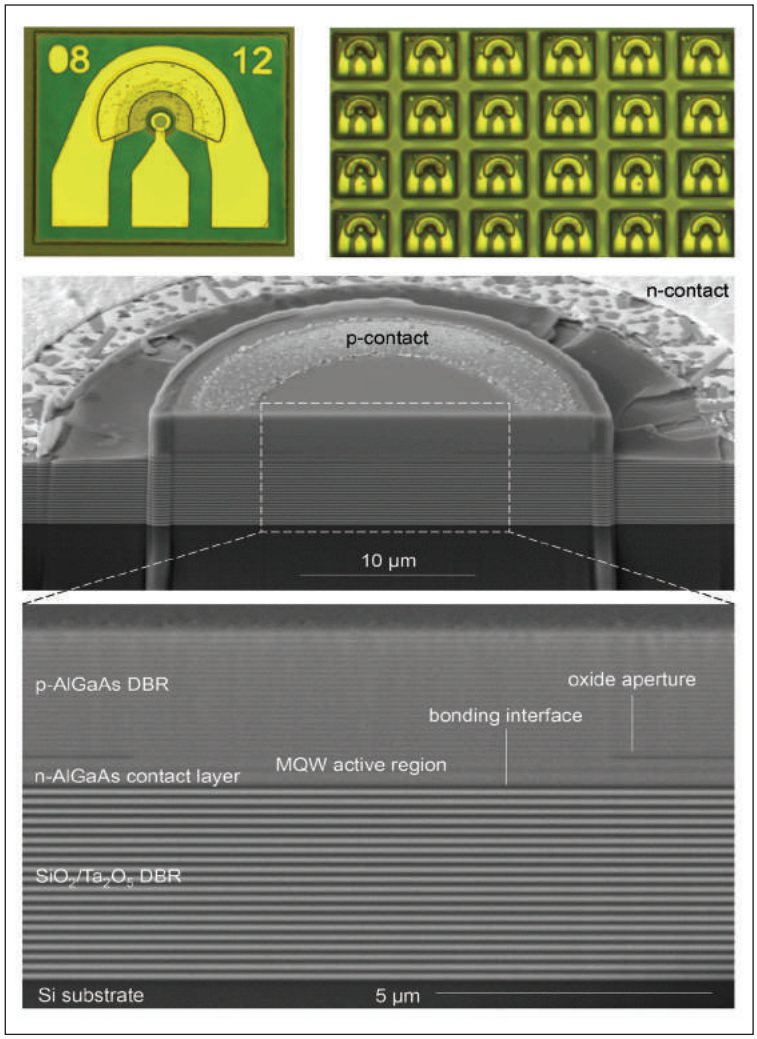


Figure 6. Upper: Optical microscope images of a single hybrid vertical-cavity laser and an array of such lasers. Lower: Scanning electron microscope images of a focused ion beam cross-section through the hybrid vertical-cavity laser (before BCB planarization).

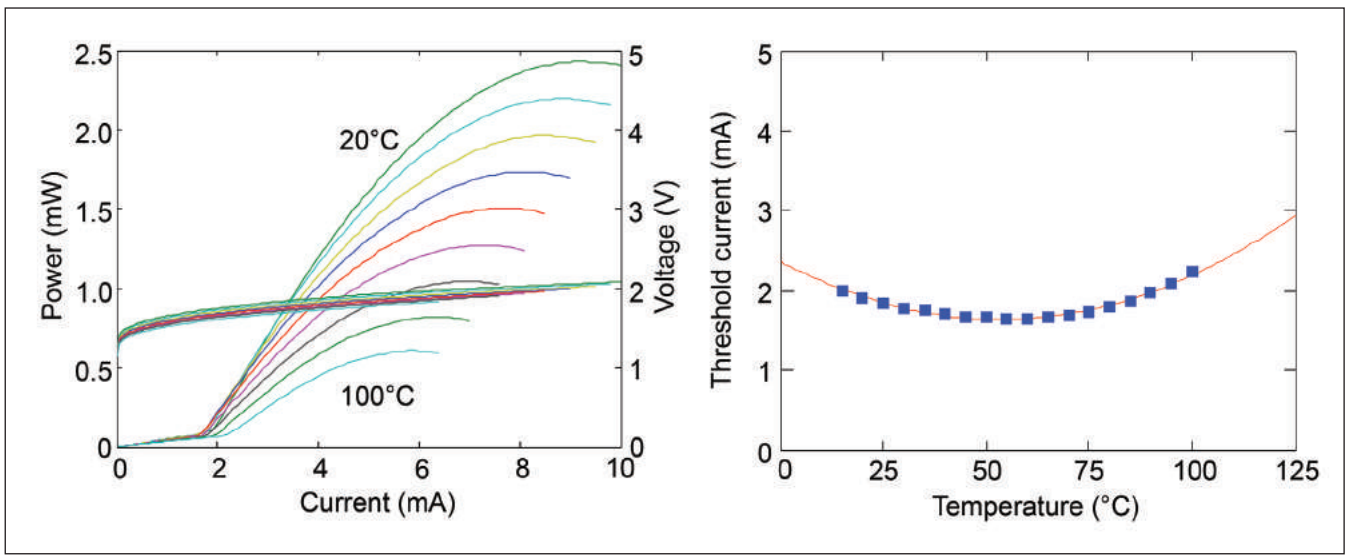


Figure 7. Left: Output power and voltage as a function of drive current at temperatures from 20°C to 100°C for an 850 nm hybrid vertical-cavity laser with an oxide aperture diameter of 10 μm. Right: Dependence of threshold current on temperature.

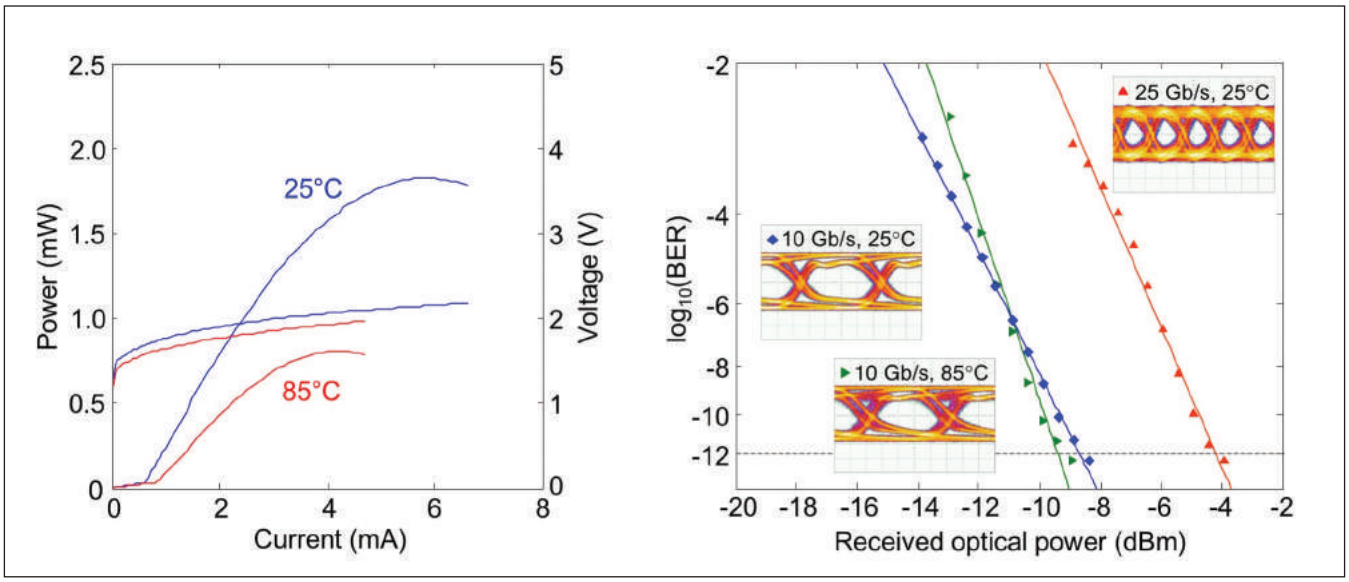


Figure 8. Left: Output power and voltage as a function of drive current at 25°C to 85°C for an 850 nm hybrid vertical-cavity laser with an oxide aperture diameter of 5 μm. Right: Results from data transmission experiments at 10 Gbit/s up to 85°C and 25 Gbit/s at 25°C.

necessary for investigating high-speed modulation capabilities, we planarized the structure with BCB. To study the uniformity of the bonding interface, we expose a cross-section through the hybrid vertical-cavity laser with a focused ion beam. The image that results allows identification of all parts of the laser, and reveals that the interface is highly uniform (see Figure 6).

Basic performance characteristics are obtained by measuring the optical output power and voltage as a function of current at temperatures up to 100°C. Plots show that performance, evaluated in terms of the temperature-dependent threshold current and slope efficiency (see Figure 7(a)), is similar to that of an ordinary oxide-confined VCSEL. This demonstrates the potential of our approach to integration.

We have found that if an appropriate thickness is used for the bonding interface, the threshold current is only weakly dependent on temperature (see Figure 7(b)). However, the output power saturates at relatively low currents, due to the high thermal impedance - it stems from the low thermal conductivity of the dielectric DBR. One way to address this is to integrate metallic heat spreaders or thermal shunts. These modifications increase the efficiency that heat is conducted to the silicon substrate, leading to reduced thermal impedance and ultimately a higher output power.

Another promising application for our short-wavelength, hybrid vertical-cavity laser is as the light source in integrated transmitters for wavelength division multiplexed optical interconnects, where the SiN PIC is used for multiplexing. To evaluate its potential, we have studied the dynamics, measuring the modulation bandwidth and data transmission rates. We found that we could transmit data at up to 25 Gbit/s at room temperature and 10 Gbit/s at 85°C by using a smaller aperture and a modulation bandwidth exceeding 10 GHz (see Figure 8).

Our results showcase the potential of our hybrid vertical-cavity laser for the integration of low-current, high-efficiency, small-footprint light sources on silicon PICs. However, there is still work to do. We must demonstrate that a similar performance is possible with in-plane emission, by incorporating an intra-cavity waveguide and diffraction grating. The good news is that the signs are promising, with simulations suggesting that the lower waveguide/grating/DBR combination can be designed to pin the polarization of the cavity mode in the direction needed for controlled, efficient coupling to the waveguide.

The authors would like to acknowledge the financial support from the European Union's Horizon 2020 research and innovation program under grant agreement number 688519 (PIX4life), the Swedish Foundation for Strategic Research (SSF), and the FP7-ERC-InSpectra Advanced Grant.

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Refining production of the GaN HEMT

At CS Mantech, engineers revealed how to build GaN HEMTs with greater gain, higher efficiency and increased mobility

BY RICHARD STEVENSON

The GaN HEMT has many virtues. Its leading attributes are its ability to operate at very high power densities and deliver efficient switching, but it is also favoured for its capability to perform at elevated temperatures.

Thanks to it great set of characteristics, sales of the GaN HEMT are on the rise. It now nets hundreds of millions of dollars per year – and it is tipped to generate even more as its bang-per-buck increases through a trimming of production costs and further advances in performance.

Driving these refinements are teams of engineers. They tend to share experiences at CS Mantech, and did so at this year's conference, held in late May at the Hyatt Regency Indian Wells Resort and Spa. Within this beautiful setting, they highlighted the tremendous reliability of existing products; revealed how to

Hyatt Regency Indian Wells Resort & Spa hosted CS Mantech 2017

increase power-added efficiency with individual source vias; offered insights into how to optimise channel mobility in HEMTs grown on silicon; and showcased the promise of growth on engineered substrates.

Great GaN reliability

At the meeting, a paper presented by Bruce Paine from Boeing Network and Space Systems extoled the great level of reliability now provided by GaN HEMTs. He and his co-worker, Neil Kubota, found no evidence for any of the widely-reported degradation modes when conducting tests on GaN-on-SiC HEMTs produced by a commercial vendor, formed with a technology marketed for several years that has now been superseded. Paine and Kubota found no deterioration in device performance from 'reverse piezoelectric' effects, surface pitting, charge trapping and hot electron effects.

"When these are gone, the parts last a very long time, until eventually the gates start to deteriorate with loss of gold," says Paine. Loss of gold is claimed to be a new failure mode for these devices.

The new loss mechanism emerged from a series of tests on 4 GHz, 2W FETs with a single layout cell. When carrying out an RF lifetest, sudden drops in RF power were observed. Most of the parts stopped functioning completely, with optical inspection revealing major melting that obliterated the FETs.

Although a smaller number of parts could still function, their gate resistance had increased from 20 Ω mm to a value of several hundred. Examining these parts with a scanning electron microscope revealed a near-complete loss of gold from sections of the gate. These losses, which involved removal of tens of microns of gold, occurred at random locations. Note that these absences were not concentrated near gate feeders, where the current density along the gate metal is at its highest.

Paine is keen to reassure producers and consumers of GaN HEMTs that device failure by loss of gold is not a great concern: "It's the failure mode that would show up eventually, long, long after any conceivable application or product life is finished." For devices tested at a channel temperature of 200 °C, the mean-time-to-failure, with a confidence of 90 percent, is 1.5×10^7 hours.

The engineers at Boeing will now to scrutinise the devices more closely, after they have been subjected to different stress conditions. "This will be an effort to observe the phenomenon [of gold loss] more thoroughly," says Paine.

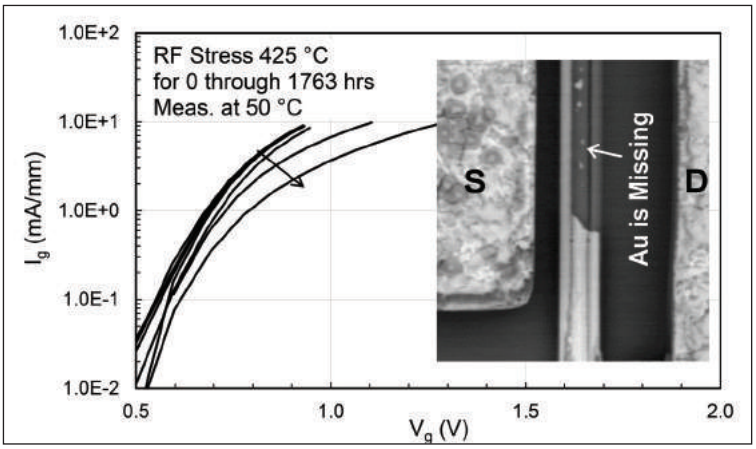


Figure 1. Engineers at Boeing have carried out lifetests on commercial devices, recording forward gate current-voltage curves. This graph for a single specimen, using source and drain voltages of 0 V, has several plots, with the arrow indicating the progression with stress time. The inset shows a 20 kV backscatter scanning electron microscopy image of a gate after a large gate-resistance increase. This is taken close to the end of the gate, at the opposite end from the gate feeder.

Improving efficiency with vias

To enable GaN HEMTs to operate at higher frequencies, manufacturers have moved to shorter gate lengths. Qorvo, for example, has introduced a 150 nm process for making products for the Ka-band.

One of the benefits of trimming gate length is an increase in device gain, which is predicted to be propelled even higher by cutting source inductance. At this years' CS Mantech, Yongie Cui from Qorvo revealed that this reduction in inductance can be accomplished by introducing individual source vias that allow a short source pad to ground.

Using the company's 0.15 μm GaN technology, Cui and co-workers fabricated devices with 30 μm by 30 μm individual source vias, and compared that performance to those with end vias. The switch to individual source vias reduced source inductance from 0.0145 nH to 0.0099 nH, leading to a higher extrinsic stable gain and an increase in the maximum oscillation frequency by more than 10 GHz.

To make the via size as large as possible and ensure a benefit from this technology, the team at Qorvo had to reduce misalignment between the backside and the frontside. They succeeded – the introduction of a new process reduced misalignment from as high as 7 μm to less than 4 μm.

Another challenge facing the team was to address the low yield of traditional via plating steps. It can be less than 50 percent, due to rough side walls and nodules that result from sub-optimal cleaning and pre-wetting steps. Developing a new process has increased yield, so that it now exceeds 90 percent (see Figure 2). According to Cui, the new process does not introduce a substantial increase in either manufacturing time or cost. "We always have vias for our GaN technologies."

Measurements of large-signal performance at 30 GHz on 4 x 50 μm transistors, using a drain bias of 20 V and a current of 20 mA, revealed that the device with individual source vias has a 47 percent power-added efficiency, an output power of 3.15 W/mm and a gain of 7.9 dB. In comparison, the equivalent chip with end vias has a 45.9 percent power-added efficiency, an output power of 3.08 W/mm and a gain of 7.4 dB.

The difference between these two sets of figures is small, and it might lead one to fail to appreciate the extent of the benefits that can be realised with individual source vias.

"The example given in the paper is for four finger devices, where we compared results from a three via device with a two via device," says Cui. "If we have a device with more fingers, such as eight fingers, then we will have five vias for the individual source vias device, which is three more than the end via device." When that happens, the difference in performance will be much larger.

It is also worth noting that measurements were made on a single stage, while more stages will be used in a MMIC; and that the impact of source inductance is frequency dependent. "We showed device performance at 30 GHz," argues Cui. "The higher the frequency, the more the benefit with individual source vias."

Increasing mobility

Another highlight from this year's CS Mantech was the paper given by Cam Bayram and co-workers

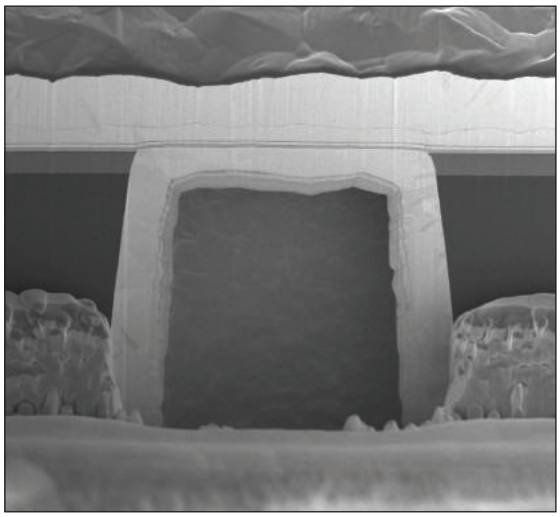


Figure 2. Cross-sectional scanning electron microscopy shows that Qorvo's process for adding individual source vias can realise smooth sides walls and plating of the bottom of the via.

from the University of Illinois at Urbana-Champaign (UIUC). These engineers showed that when AlGaN/GaN HEMTs are produced on silicon substrates, which are used to reduce manufacturing costs, interface roughness can limit channel mobility and ultimately high-frequency performance.

The team came to this conclusion after measuring a variety of structures with different buffer layer configurations. Measurements revealed that it is the in-plane stress in the GaN layer, rather than surface defectivity, that governs the characteristics of the two-dimensional electron gas. Reduce the in-plane stress and there is a cut in the concentration of the two-dimensional electron gas via a lowering of piezoelectric polarisation – and the mobility of this gas increases, thanks to a reduction in interface roughness scattering in the channel.

Lead author of the paper describing the work, Hsuan-Ping Lee, told *Compound Semiconductor* that many groups have evaluated the impact of defects on the characteristics of the two-dimensional electron gas. However, these prior investigations have been limited to conventional substrates, such as SiC and sapphire.

"With the emergence of silicon substrates, and the need for complex buffer layers, stress management becomes a prominent factor, particularly for 200-mm-and-above wafer scaling," explains Lee.

Lee and co-workers employed three different buffer layer structures for the fabrication of AlGaN/GaN HEMTs on standard single-side polished silicon (111) wafers. One buffer structure had three periods consisting of a thick layer of GaN, followed by AlGaN and GaN; another adopted the same layer, but reduced the total thickness by a factor of three; and the third just involved a relatively thin layer of GaN on AlN.

To evaluate the quality of the surface, the engineers scrutinised all three samples with optical microscopy, atomic force microscopy and cathodoluminescence (see Figure 3). Together, these three techniques identified similarities in the structures – freedom from surface cracks and similar levels of surface roughness – and showed that the thicker the buffer, the lower the threading dislocation density.

These dislocations, which can be categorised as edge-, screw-, and mixed-types, deteriorate device performance. However, in the samples produced by

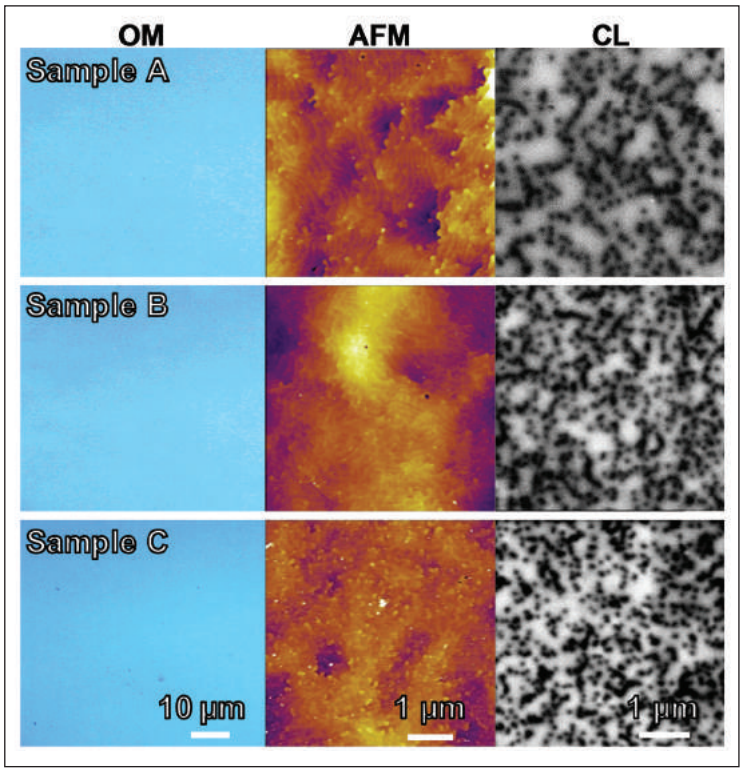


Figure 3. Engineers at the University of Illinois at Urbana-Champaign have investigated the impact of differing buffer layers on the surfaces of AlGaN/GaN-on-silicon HEMTs. The team employed three different buffer layer structures: (A) three periods consisting of a thick layer of GaN, followed by AlGaN and GaN; (B) three periods consisting of a thinner layer of GaN, followed by AlGaN and GaN; and (C) a relatively thin layer of GaN on AlN. (Left) Optical microscopy reveals crack-free surfaces. (Middle) Atomic force microscopy reveals different surface morphologies. (Right) Cathodoluminescence panchromatic scanning highlights defects as dark spots.

Lee and co-workers, which had defect densities in the range 2-3 x 10^9 cm^{-2}, by far the greatest influence on channel mobility is strain. "It is always desirable to minimize such defects, but our work points that given the same defect levels, stress management is critical in achieving high two-dimensional electron gas mobilities," remarked Lee.

Hall measurements, using a Van der Pauw configuration, revealed a room-temperature electron mobility of 1802 cm^2 V^{-1} s^{-1} in the thinner sample with AlGaN in the buffer structure. This is higher than that in the two other samples: 1295 cm^2 V^{-1} s^{-1} in the thicker sample, and 1593 cm^2 V^{-1} s^{-1} in the sample with a buffer structure made from just GaN and AlGaN.

With the emergence of silicon substrates, and the need for complex buffer layers, stress management becomes a prominent factor, particularly for 200-mm-and-above wafer scaling

"Our goal is to move forward with high-frequency RF devices using our best strain-engineered samples having 1,802 $cm^2 V^{-1} s^{-1}$ room-temperature mobility," says Lee.

Engineered substrates

One way to avoid the need for complex buffer layers is to turn to an engineered substrate. One manufacturer of such a platform is Quora Technology of Santa Clara, CA: it has developed an engineered substrate that features a core with a coefficient of thermal expansion matched to that of GaN, and an epi-ready silicon (111) surface for the growth of GaN. Thanks to this, issues of wafers bow are eliminated, and there are no restrictions on buffer layer thickness, which can restrict the breakdown voltage.

At this year's CS Mantech, results of GaN HEMTs formed on these substrates were given in a paper presented by Karl Hobart from the US Naval Research Laboratory, and co-authored by engineers at Quora and George Mason University. According to Hobart, HEMTs grown on Quora's engineered substrates have material and thermal properties and electrical characteristics that compare favourably with those of today's GaN-on-silicon devices.

With these engineered substrates, Hobart and co-workers employed growth recipes that are very similar to those for making GaN-on-silicon HEMTs. However, the buffer layer stack is far more simple, thanks to far easier strain management.

Hobart says that the foundation for growth is so good that it can hold up to tens of microns of GaN material, deposited by either MOCVD or HVPE, without cracking or breaking. "This unique capability will enable vertical power device architectures as well."

D-mode HEMTs were formed by growing a 5 μm-thick layer of GaN on 150 mm Quora substrates, and then adding a 6 μm-thick, carbon-doped buffer, 100 nm of undoped GaN, a 20 nm-thick AlGaN layer and a 2 nm-thick GaN cap. Conventional processing of the epiwafer followed, before transistors were constructed with an ohmic gate and source-to-drain spacings varying from 5 μm to 15 μm.

Characterisation of the HEMTs revealed a maximum drive current of 0.376 mA/mm, a maximum transconductance of 155 mS/mm, a breakdown voltage of 570 V and a Hall mobility of 1859 $cm^2 V^{-1} s^{-1}$.

Hobart believes that these results are very encouraging, and highlight the great potential of Quora's substrates. The team are now optimising the epilayers and the device structure for HEMTs built on this platform.

"In addition, our industry partner has demonstrated E-mode HEMT devices on Quroa substrate technology in a commercial fab environment," say Hobart.

Manufacturers that are considering the switch from silicon substrates to Quora's platforms may be concerned by the additional cost of the engineered platform. Hobart offers reassurance, arguing that a wide portfolio of power devices can be produced on Quora's 200 mm substrates at less than $0.03 per amp. These devices can include switches, vertical diodes and other products with operating voltages ranging from 100 V to 1500 V.

"The cost of less than $0.03/A is not only favourable to existing GaN-on-silicon and GaN-on-GaN solutions," says Hobart, "but highly competitive with conventional silicon-based power discretes, such as MOSFETs and IGBTs." The wide appeal could accelerate the adoption of GaN.

As well as trying to improve the HEMTs produced at the Naval Research Laboratory, Hobart and co-workers are planning to demonstrate their own E-mode devices, and evaluate other devices produced on Quora's platform, such as vertical diodes and FETs. Additional aims are to fabricate vertical switches and RF devices and to continue their work with partners to demonstrate Quora's 300 mm substrates. Success with the latter will demonstrate a long-term roadmap associated with this engineered platform.

The efforts by the engineers at US Naval Research Laboratory, and those at Quora, Boeing, Qorvo and the UIUC, suggest a very promising future for the HEMT. It is already well-positioned, thanks to its high reliability and good performance, and it is on track to get better and cheaper.

As well as trying to improve the HEMTs produced at the Naval Research Laboratory, Hobart and co-workers are planning to demonstrate their own E-mode devices, and evaluate other devices produced on Quora's platform, such as vertical diodes and FETs. Additional aims are to fabricate vertical switches and RF devices and to continue their work with partners to demonstrate Quora's 300 mm substrates

Deep UV LEDs: Increasing extraction with nanoscale patterns

Growing deep UV LEDs on AlN nanorod arrays increases LED output

RESEARCHERS from Korea have increased the extraction efficiency of deep UV LEDs by introducing periodic nanoscale patterns with air voids. Their 280 nm-emitting structures, which improve crystal quality and light extraction, were created by nanoscale lithography and epitaxial layer overgrowth on 4-inch sapphire substrates.

Spokesman for the team, Euijoon Yoon from Seoul National University, believes that one of the most important aspects of this work is the use of epitaxial layer overgrowth at a temperature of just 1050 ˚C.

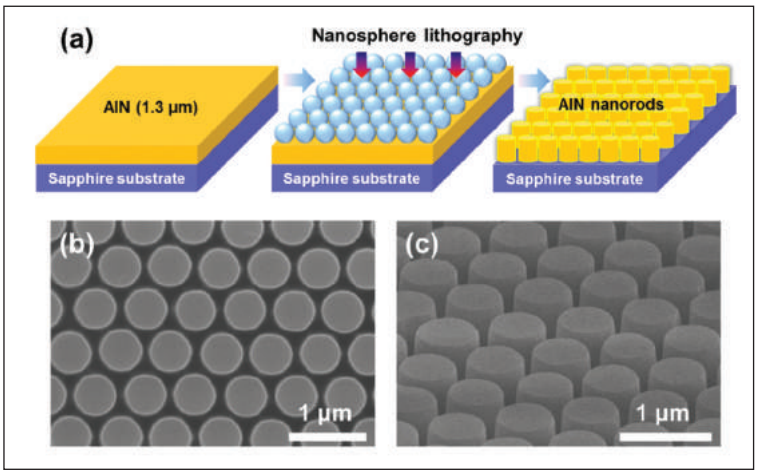
"As far as we know, 1050 ˚C is the lowest temperature that was ever reported for AlN epitaxial layer overgrowth," says Yoon. According to him, typical temperatures for microscale epitaxial layer overgrowth in an MOCVD chamber are between 1300 ˚C and 1400 ˚C, while those for nanoscale variants range from 1100 ˚C to 1200 ˚C.

Yoon's team from Seoul National University, working with researchers from Pohang University of Science and Technology and Samsung Electronics, began the fabrication of their deep UV LEDs by loading 4-inch, *c*-plane sapphire substrates into an MOCVD chamber and depositing a 1.3 μm - thick layer of AlN.

After this, silica nanospheres with an average diameter of 700 nm were spin-coated on the AlN layer, before chlorine-based etching transferred the pattern to underlying AlN (see Figure). This created an array of 1.3 μm-high nano-rods with a typical diameter of 630 nm. Residual nanospheres were removed by dipping the substrate in hydrofluoric acid.

Researchers loaded the patterned substrate into an MOCVD chamber and grew a 5.2 μm-thick AlN film on top, followed by an LED epistructure. Despite the low growth temperature, full coalescence occurred within 2 μm of overgrowth. Such a thin film promises lower manufacturing costs.

There are two significant benefits associated with periodic air voids that surround the AlN nanorods, which are located between the overgrown AlN layer and the sapphire. One is that they relieve stress in the AlN film by trimming the contact layer between the epilayer and the underlying sapphire; and the other is that they create a periodic refractive index contrast between AlN and air, leading to increased extraction efficiency. On these periodic structures, Yoon and co-workers have produced 300 μm by 300 μm LEDs



(a) Nano-patterning an AlN-on-sapphire template forms the basis for improved deep UV LEDs. (b) and (c) Scanning electron microscopy of nano-patterned sapphire.

with a five-period multi-quantum well and a 15 nm-thick, magnesium-doped AlGaN electron-blocking layer. They also fabricated a control, grown on an un-patterned AlN template.

Introduction of nanoscale patterns cuts the density of threading dislocations in the *n*-type AlGaN layers from 6 x 10^{19} cm^{-3} to 4.4 x 10^{19} cm^{-3}, according to scanning electron microscopy images.

Room-temperature measurements on 50 LEDs, driven at 20 mW, reveal a 67 percent increase in light output power, thanks to the introduction of tiny voids.

The voids also led to a reduction in operating voltage, which fell from 10.8 V to 9.3 V. Despite this reduction, the voltage is still high, due in part to the use of *n*- and *p*-contacts for visible LEDs.

"We are trying to improve the electrical properties of our deep UV LEDs by introducing low-resistance ohmic contact schemes, as well as by optimising the growth and doping conditions of *n*-type AlGaN and *p*-type GaN contact layers," explains Yoon.

Another option for increasing the efficiency of the deep UV LED is to house the device in a package. "We expect improved performance, due to improvement in light extraction efficiency and heat dissipation."

Reference

D. Lee. *et al.* Appl. Phys. Lett. **110** 191103 (2017)

Exposing oxygen defects in GaN HEMTs

Cathodoluminescence unveils oxygen-related defects in the Al_2O_3 dielectric on a GaN-based HEMT

A TEAM OF ENGINEERS from Japan has refined the performance of its metal-oxide-semiconductor HEMT with an air annealing step that trims imperfections in and around the Al_2O_3 layer.

Annealing the InAlN/GaN HEMT in air for 12 hours at 300 ˚C improved transconductance linearity and the subthreshold slope. However, the greatest significance of this work by researchers at Fujitsu Laboratories and Hokkaido University is not the improved device performance – it is the exposing and categorizing of oxygen-related defects with cathodoluminescence, a technique that is based on probing a sample with an electron beam and measuring the resultant emission spectrum.

The technique may attract many followers, because oxide films in InAlN/GaN HEMTs reduce high leakage currents. Al_2O_3 is a popular choice, thanks to its great set of characteristics: a very wide bandgap, a high dielectric constant and a high breakdown voltage.

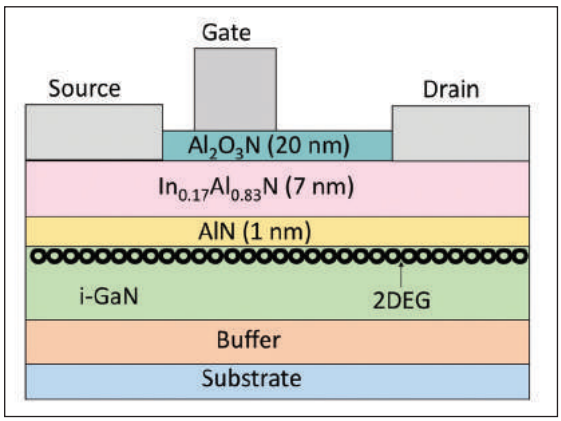
To prevent Al_2O_3 from decreasing transconductance and hampering RF performance, it must not be too thick. To realise this, it is formed by atomic layer deposition.

Another requirement for Al_2O_3 is a low electronic state density at its interface with InAlN – realising this enables a stable threshold voltage and gate controllability. Ensuring a low density is not easy, and today's devices are often held back by relatively low drain currents, high gate leakage, a large decrease in transconductance at forward bias, and severe current collapse.

To investigate these issues, the team evaluated the performance of InAlN/GaN HEMTs with air-annealed Al_2O_3 films. Annealing aims to control defect levels within Al_2O_3 and electronic states at the Al_2O_3/InAlN interface.

HEMTs were formed with a 0.5 μm gate length, 50 μm gate width and a 10 μm gate-drain length. Atomic layer deposition at 300 ˚C added a 20 nm-thick Al_2O_3 film.

In previous studies, the team investigated several different approaches to improving both the defect level in Al_2O_3 and the electronic states at the Al_2O_3/InAlN interface. Techniques included post-deposition and post-metallisation annealing at various temperatures, under different gases and durations.



Cathodoluminescence exposes oxygen-related defect levels within Al_2O_3 and the electronic states at the Al_2O_3/InAlN interface.

"At present, the best result was obtained under post-metallisation annealing in air at 300 ˚C for 12 hours," explains Fujitsu's Shiro Ozaki. These conditions were used to improve the performance of the latest devices.

Measurements on a control and an annealed device showed that annealing increased the maximum drain current from less than 900 mA/mm to more than 1100 mA/mm at a gate voltage of 2 V, and trimmed on-state resistance from 7 Ω mm to 5.3 Ω mm. Annealing also improved the sub-threshold swing: it fell from 127 mV/dec to 75 mV/dec.

Cathodoluminescence studies on Al_2O_3-on-sapphire films grown by atomic layer deposition pinpointed the benefits of annealing. It produced falls in peaks in the cathodoluminescence spectra associated with oxygen vacancies featuring one and two trapped electrons. This indicates that annealing reduces the number of oxygen vacancies in the Al_2O_3 films.

Interestingly, this behaviour was not observed after annealing in nitrogen gas. This led Ozaki and co-workers to postulate that air annealing enhances the relaxation and passivation of dangling bonds in Al_2O_3 films, including oxygen vacancies.

Another impact of air annealing is a 10 percent shrinkage in the Al_2O_3 film, leading to a significant increase in tensile stress. This shrinkage enhances the piezoelectric field and accounts for a reduction in sheet resistance with annealing.

Ozaki believes that one issue that still needs addressing is a relatively large voltage shift of their HEMT compared with AlGaN/GaN equivalents.

Reference

S. Ozaki *et al.* Appl. Phys. Express **10** 061001 (2017)

Gallium oxide transistors target RF

Delta-doped Ga_2O_3 FETs produce promising characteristics for RF applications

ENGINEERS AT THE OHIO STATE UNIVERSITY are starting to unleash the potential of a novel Ga_2O_3 FET that could be used to make power amplifiers for RF and mm-wave applications.

One attraction of using Ga_2O_3 is that it has a far wider bandgap than GaN, the incumbent material for making high-performance RF amplifiers. The wider bandgap promises to lead to superior performance, thanks to higher breakdown voltages and higher channel charge densities.

The Ga_2O_3 transistors formed by the team from Ohio incorporate delta-doping. This is a major asset, because it allows the creation of high-charge-density layers, which are essential for the construction of high-frequency FETs with short gate lengths and an appropriate aspect ratio.

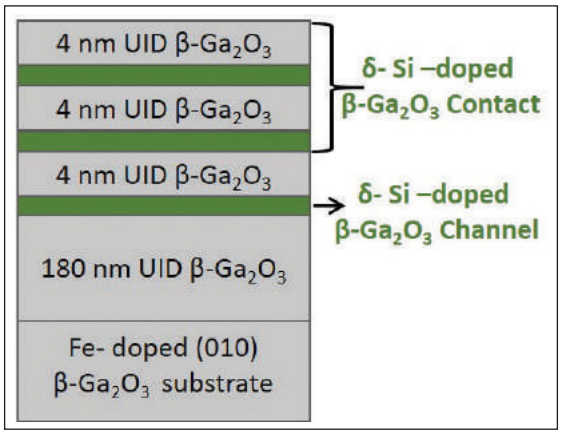
"The aspect ratio between the gate length and the gate-channel spacing determines critical device parameters, such as the output conductance and power gain," says corresponding author Siddharth Rajan. "To get higher frequency operation, we shrink the gate length and at the same time reduce the gate-to-channel spacing to maintain the aspect ratio of the transistor."

Rajan and co-workers form their devices on native substrates produced by Japanese company Tamura. "Their cost is similar to GaN substrates," says Rajan, "but the price of these substrates is expected to get significantly lower in the future, since the pulling methods used are inherently more scalable than the methods used for GaN bulk growth."

To investigate the electrical characteristics of delta-doped layers, the team loaded iron-doped, semi-insulating (010)-orientated β-Ga_2O_3 substrates into an MBE chamber, where they produced epistructures with an un-doped β-Ga_2O_3 buffer layer and delta-doped layers (see Figure). To avoid source oxidation and ensure a flat doping profile, they pulsed the silicon source, while the shutters for the oxygen and gallium sources remained open throughout the growth.

Ohmic contacts with a contact resistance of 0.35 Ω mm and a specific resistance of just 4.3×10^{-6} Ω cm^2 were formed by adding a Ti/Au/Ni metal stack and annealing it. According to the team, these values demonstrate that delta-doped layers can provide excellent contact layers.

Hall measurements on a range of samples with multiple delta-doped layers revealed a mobility of 77-81cm^2 V^{-1} s^{-1} and a sheet charge density of



Delta-doped structures were formed by MBE growth on commercial substrates made by Tamura.

2.7×10^{14} cm^{-2} to 3.5×10^{14} cm^{-2}. "The total charge is close to the record values achievable in GaN," remarks Rajan.

FETs were formed by taking epistructures with three delta-doped layers (see Figure) and removing the top two with inductively coupled plamsa, reactive-ion etching. Engineers added an Al_2O_3 gate dielectric by atomic layer deposition, and an Pt/Au/Ni gate stack.

Electrical measurements revealed a current of 236 mA/mm at a drain-source voltage of 7 V and a gate voltage of 2 V; a peak transconductance of 26 mS/mm at a gate bias of -3.8 V; and a three terminal off-state breakdown voltage of 51 V.

The team claims that the current and transconductance values are far higher than those previously reported for β-Ga_2O_3 FETs.

"The device current and transconductance are lower than GaN, but these are currently limited by the lower mobility, which could be improved, and the relatively large device size," explains Rajan.

Two weaknesses of the β-Ga_2O_3 FET are its poor thermal conductivity, which could be addressed by layer transfer, and its poor surface passivation.

"Surface passivation using dielectrics has been addressed in materials with similar field strengths, such as GaN," says Rajan. "In the case of gallium oxide also, we think surface passivation techniques will eventually be developed after careful investigation."

Reference

S. Krishnamoorthy *et. al.* Appl. Phys. Express **10** 051102 (2017)

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VENDOR VIEW Proton Site

On-site hydrogen generation: smart choice to improve process results

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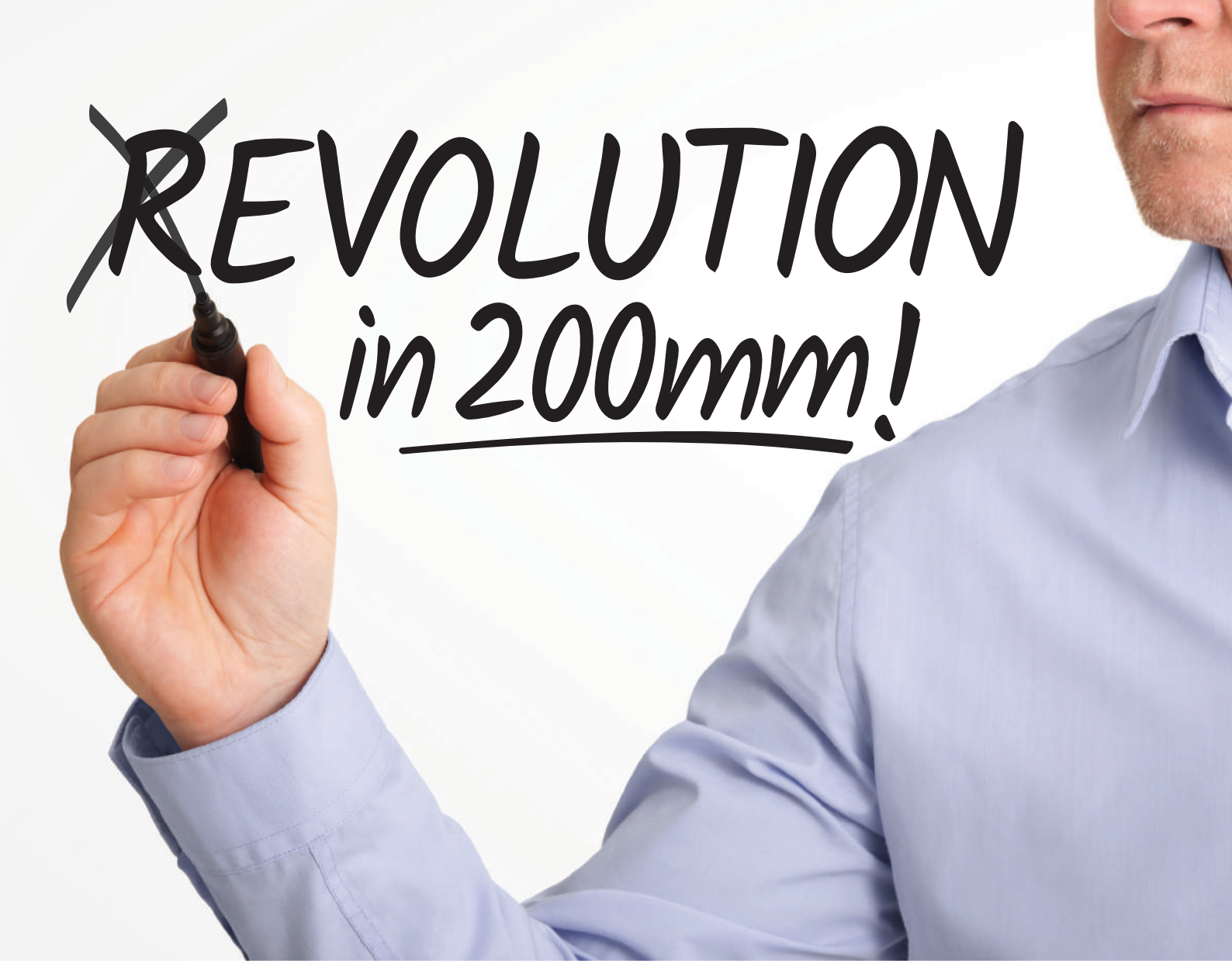

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