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VOLUME 30 ISSUE IV 2024

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INSIDE
News, Analysis, Features, Editorial View, Research Review and much more

A new approach to education

Compound semiconductor innovation requires an overhaul of engineering education and talent development

Monolithic power integration

Sapphire substrates with ultra-thin buffer layers hold the key to 1200 V GaN-based monolithic power integration

Silicon's positive influence

Sales to silicon fabs are behind the greatest gain in share price within the compound semiconductor industry

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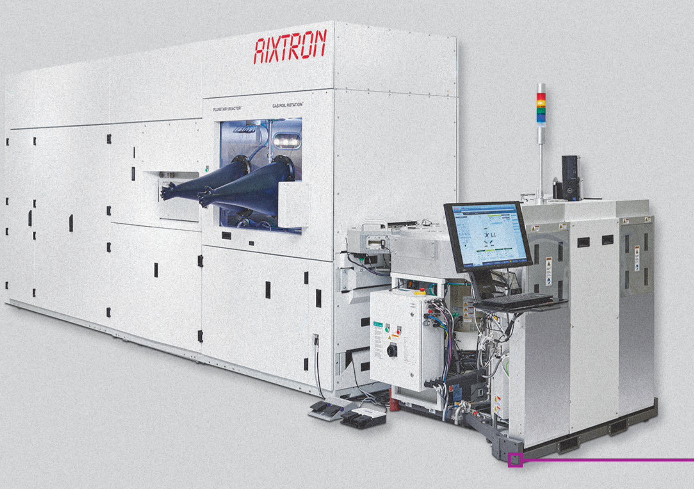

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VIEWPOINT

By Richard Stevenson, Editor

Green credentials?

What have you done to help to tackle climate change? It's a question rarely asked today. However, fast-forward a decade or more and we can expect interrogation from younger generations, demanding an answer, possibly along with an apology.

If you are limiting foreign travel, trimming meat consumption, or are an early adopter in electric vehicles (EVs), you may avoid the harshest criticism. And you might also defend yourself by pointing out that you have been involved in an industry that's introduced new technologies, which are playing a valuable role in slashing carbon dioxide emissions.

Within the compound semiconductor industry, there are certainly some great success stories involving substantial energy savings.

Arguably the biggest to date is in general illumination. The incumbent of the twentieth century, the incandescent bulb, is notoriously inefficient, with around 90 percent of electricity converted into heat. It's initial rival, the fluorescent, has the upper hand in this regard, but takes time to warm up and fails to light a room with flattering form of white. Accounting for the demise of both of these forms of lightbulb is that based on the LED. It has no major weaknesses and delivers hikes in efficiency and lifetime.

The other example easily coming to mind of compound semiconductor chips giving a helping hand to the environment is role that they play in EVs. Power semiconductors based on SiC are increasing the efficiency with which the energy from the battery provides transportation. As well as reducing the energy per mile, the uptake of SiC is increasing the driving range, and ultimately helping to accelerate adoption of a new generation of automobiles through reduced range anxiety.

While EVs are helping to tackle climate change, there are concerns over the production of their batteries. Mining the key ingredients for their manufacture is detrimental to the environment, and production is energy intensive.

Studies suggest it takes 30-55 kWhr of energy for every kWhr of battery. This soon adds up, given that EVs can be powered by batteries with a total energy capacity of 100 kWhr.

Within the battery production process, nearly half of all the energy that's consumed is involved in a heating process, with ovens employed to dry a thick, wet, lithium-containing slurry that's applied to a metal foil during the production of electrodes.

At this year's CS International, CTO of Trumpf Photonics, Roman Koerner, revealed that energy savings could come from heating with vast arrays of VCSELs. According to Koerner, the established oven-based process has an efficiency of 10-20 percent, while laser drying is more than 40 percent efficient (for more details, see "New vectors for the VCSEL" on p 28).

This opportunity for the VCSEL is yet another example of how compound semiconductors are positioned to play an increasing role in tackling climate change. While our community's devices are only a small part of the solution, all contributions are welcome in the struggle to prevent overheating of our planet.

Free weekly e-news roundup go to: compoundsemiconductor.net

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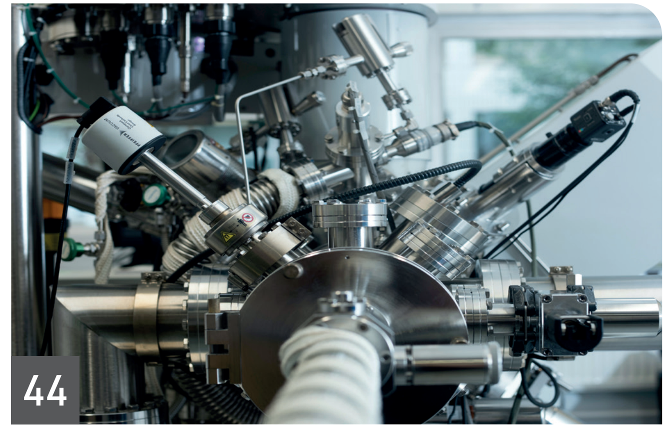

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What's next for SiC?

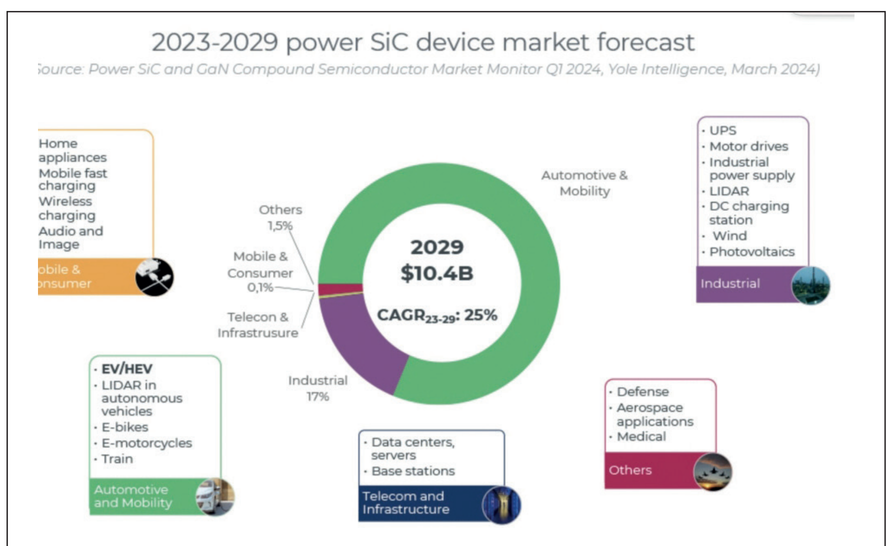
Shipments are slowing down due to the weakness of the global economy, according to Yole

POWER ELECTRONICS based on SiC is on track to reach $10 billion in revenue by the end of this decade, and the strong growth in 2023 was a crucial step in multiple applications, according to the market research firm Yole Group.

BEV remains the key market driver, with Tesla's 1.8 million cars shipped in 2023, while major OEMs such Hyundai, BYD, Xpeng, Nio and many others are increasingly launching 800 V BEVs. All the major SiC device players are supplying this application, helping it achieve record revenue in 2023.

In the meantime, other applications, such as EV chargers, power supplies and photovoltaics, are waiting for sufficient volume at a competitive cost for the next generation of SiC device designs. It was the same in the SiC wafer and epiwafer businesses, with record 2023 revenues.

However, Yole says there is a concern that shipments are slowing down due to the weakness of the global economy. Many players are re-evaluating the timing of the return to growth; could it be in Q3 of 2024 or later? The SiC supply chain is closely monitoring it, as 2024 results will be highly impacted.



In the meantime, the supply chain is reshaping. This is seen in the ranking of players by revenue in 2023: currently, Yole sees at least two Chinese companies ranked in the top five in SiC wafer and epiwafer. This also indicates the maturity of equipment supply supporting this rapidly growing SiC market. Another critical consideration is the demand-supply issue. In the past years, SiC wafer was in tight supply; a long-term agreement with a wafer supplier being essential to secure access to SiC wafers. However, following significant capacity expansion in the past two years, the discussion is moving to price and the risk of overcapacity, says Yole.

Power Integrations to acquire Odyssey assets

POWER INTEGRATIONS has agreed to acquire the assets of Odyssey Semiconductor Technologies, a developer of vertical GaN transistor technology. The transaction is expected to close in July 2024, after which all key Odyssey employees are expected to join Power Integrations.

The acquisition supports the company's ongoing development roadmap for its proprietary PowiGaN technology, which is featured in many of the company's product families, including InnoSwitch ICs, HiperPFS-5 power-factor-correction ICs and the recently launched InnoMux-2 family of single-stage, multiple-output ICs.

The company introduced 900 V and 1250 V versions of PowiGaN technology and products in 2023.

According to Radu Barsan, Power Integrations' vice president of technology, PI's roadmap is to achieve cost parity with silicon MOSFETs and expand the voltage and power capabilities of PowiGaN.

Barsan said: "Our goal is to commercialise a cost-effective high-current and high-voltage GaN technology to support higher-power applications currently served by SiC, at a much lower cost and higher performance enabled by the fundamental material advantages of GaN over SiC. The experience of the Odyssey team in high-current vertical GaN will augment and accelerate these efforts, and we are delighted to add them to our team."

Richard Brown, Odyssey co-founder and CEO said: "The Odyssey team and I are excited to join Power Integrations in accelerating their GaN technology roadmap. As the first company to commercialise high-voltage GaN, Power Integrations continues to lead the industry in driving the technology forward in terms of cost, voltage and current, as well as the design of system-level products that take full advantage of the capabilities of GaN."

Q-Pixel debuts highest resolution colour display

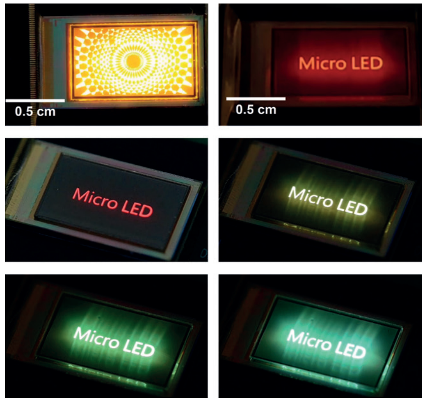
Q-Pixel believes it has produced the highest resolution, active-matrix colour display in the world

Q-PIXEL'S breakthrough display boasts 6,800 pixels-per-inch (ppi), far surpassing current state-of-the-art displays, such as the Apple Vision Pro (around 3,380 ppi). The display is made entirely using microLED pixels.

Unlike most advanced VR displays, which use micro-organic LEDs (micro-OLEDs), Q-Pixel's displays consist entirely of III-V compound microLED pixels. Synthesised from inorganic materials, III-V microLEDs offer many advantages over OLEDs, including a faster response time, higher brightness, longer lifetime, and superior energy efficiency. From a physics perspective, inorganic III-V microLEDs have long been considered the ideal display technology, but have lacked a clear path to commercial viability.

The main challenges to commercialising microLED displays arise from the traditional approach of assembling full colour pixels using individual monochromatic red, green, and blue (RGB) LEDs. For high-resolution displays requiring small (less than 50 µm) pixels, the assembly, testing, and repair of millions of RGB microLED subpixels is a complicated, labour-intensive, and expensive process. Moreover, the physical space required for three RGB subpixels restricts the display's pixel density, posing an obstacle to realising high-resolution displays. Q-Pixel's overcomes both hurdles by replacing three RGB subpixels with individual, fully colour-tunable pixels.

The enabling technology is based on a disruptive tunable polychromatic LED (TP-LED) pixel: a single pixel capable of emitting light across the full colour spectrum, without any use of subpixels, quantum dots, colour filters, polarisers, or mechanical stacking. In addition to possessing all the benefits inherent to III-V LED technology, Q-Pixel's single TP-LED greatly simplifies display assembly,



reduces manufacturing costs, and enables world-record pixel densities.

In May 2023, Q-Pixel unveiled its world-record 5,000 ppi full-colour microLED display, and in November 2023 surpassed its world record with the simultaneous announcement of a passive 10,000 ppi microLED display made from the world's smallest full-colour pixels (1 µm diameter), all based on its TP-LED technology.

Now by delivering the world's highest resolution (6,800 ppi) active-matrix colour display, Q-Pixel has accomplished two major milestones. First, it has proved that it is possible to produce ultra high-resolution, active displays based on the microLED technology. Secondly, it has shown that its TP-LED pixel technology surpasses more mature display technologies, such as OLEDs, to attain world-record breaking pixel densities.

With these latest achievements, Q-Pixel says that it has established itself as a trailblazer in the microLED field and will embark on the commercialisation of dazzling displays.

Q-Pixel demonstrated its technology and prototype at the Society for Information Display's annual symposium and tradeshow, SID Display Week, held on May 14-16, 2024.

We cordially invite you to join the Institute of Novel Semiconductors at Shandong University

1. About Us

The Institute of Novel Semiconductors is a key academic special zone supported by Shandong University. Leveraging the solid foundation of Shandong University in the field of semiconductor material research, the institute aims at the future development direction of semiconductor material technology. It focuses on the major demands in energy, information, rail transit, and other fields, cultivating the development of new generation wide bandgap and ultra-wide bandgap semiconductor single crystal materials, enhancing breakthroughs in key technologies of semiconductor devices, and promoting application demonstrations in typical application fields.

2. Application Conditions

(A) Basic Conditions

1. Born after January 1, 1969 (inclusive);
2. In principle, should have a Ph.D. degree;
3. Have obtained a formal teaching or research position at overseas universities, research institutions, or corporate R&D institutions;
4. Have-obtained researchor technical-achievements recognized-by peers in the field,and havethepotential-to-becomea leading-academic-or-outstanding-talent-inthefield.

(B) Research Directions and Professional Fields

Growth of new generation semiconductor single crystal materials such as silicon carbide, gallium nitride, gallium oxide, diamond, aluminum nitride, boron arsenide, thin film growth, substrate processing, advanced laser technology; fabrication of power devices, optoelectronic functional devices, acoustic devices, microwave devices; and the related technology fields of packaging testing, modules, etc.

3. Compensation and Benefits

(A) **High Starting Point for Career Development:** Eligible for appointment as a professor and doctoral supervisor;
(B) **Competitive Salary:** Comprehensive annual salary not less than 600,000 RMB, with no cap on total income;
(C) **Sufficient Research Funding:** Research funding ranging from 3 to 10 million RMB during the employment period;
(D) **Excellent Working and Living Conditions:** Offers a settling-in and housing subsidy of 2.5 million RMB for the National talents;
(E) **High-Quality Team Resources:** Provides full quotas for recruiting PhD students and postdoctoral researchers during the employment period;
(F) **Additional Support:** Offers first-class medical and healthcare services for talents, and provides leading domestic basic education for the children of talents. Assistance in resolving spouse employment issues.

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Vishay chooses Aixtron SiC tech for Newport fab

G10-SiC epitaxy production platform supports transition between 150 mm and 200 mm wafers

VISHAY INTERTECHNOLOGY has chosen Aixtron's G10-SiC epitaxy production platform for the automotive-certified Newport fab in South Wales, UK, which it has recently acquired.

With its flexible dual wafer size configuration of 9 x 150 mm and 6 x 200 mm, the G10-SiC supports the transition between the wafer diameters.

"The new G10-SiC epi production tool delivers a leading cost structure for 200 mm epitaxy, which meets Vishay's productivity goals. This, in combination with an excellent uniformity performance on 200 mm wafers, has made us choose Aixtron technology," said Danilo Crippa, senior director R&D for SiC development, Vishay Intertechnology.

"The Aixtron team has developed a unique solution for the tightest control of doping levels and uniformity on 200 mm SiC wafers. This performance is maintained across the entire 6 x 200 mm wafer batch with an impressive run- to-run stability," said Frank Wischmeyer, VP SiC, Aixtron SE.

He added: "We are very grateful for the opportunity to partner with Vishay and deliver our state-of-the-art epi production system with flexible 150 mm and 200 mm SiC wafer configuration

for Vishay's automotive-certified Newport fab in South Wales. Our strong customer service team in the South Wales Compound Semiconductor Cluster is dedicated to fully support the production ramp of Vishay's SiC inhouse epitaxy to the highest productivity within a short period of time."

SweGaN announces strategic partnership with RFHIC

SweGaN AB, a European semiconductor manufacturer that develops and produces engineered high-performance GaN-on-SiC epitaxial wafers, has announced it has entered strategic partnership with South-Korea-based RFHIC Corporation. RFHIC is a global leader in designing and manufacturing GaN RF and microwave semiconductors for communications and defence applications. The new, pivotal agreement encompasses an undisclosed equity investment from RFHIC. The two companies will focus on joint R&D and product development moving forward.

Over the last decade, SweGaN has been developing and producing high-performance GaN-on-SiC epitaxial solutions for RF and power devices that can be used in various applications such 5G telecommunications infrastructure, defence radars, satellite communications, on-board chargers, and data centres.

The new strategic investment by RFHIC is said to manifest the recognition of SweGaN's QuanFINE epitaxial solutions as a standout differentiator among GaN-on-SiC materials available on the market. In partnership with RFHIC, SweGaN gains additional resources to expedite market penetration and to achieve its business goals.

RFHIC Corporation believes that the partnership with SweGaN and its investment strategy will strengthen RFHIC's GaN semiconductor supply chain and further fortifying its competitiveness of RF and microwave products within the compound semiconductor arena.

Jr-Tai Chen, CEO and Founder at SweGaN, remarked: "With the accelerating demand for high-performance semiconductor materials to power a multitude of applications and increase the efficiency in an energy-conscious world, the new equity investment will support SweGaN's capacity expansion plan of its best-in-class GaN-on-SiC epitaxial wafers and tap joint product developments with RFHIC."

He added: "We are very proud to partner with RFHIC, a leading RF GaN innovator who has the passion and commitment to amplify the world by providing top-efficiency and cutting-edge GaN solutions."

As market requirements for high-power, highly efficient semiconductors are spurred by the rapid growth of a wide array of applications such as 5G communications, defence radars and data centers, SweGaN is moving swiftly to address the growing demand by expanding its in-house manufacturing capacity and R&D capability.

The new strategic partnership with RFHIC has the potential to significantly invigorate SweGaN's position in multiple geographical areas important for the company as it aims to lead a transition from legacy material solutions to its innovative GaN semiconductors.

Samuel Cho, CTO and co-founder of RFHIC Corporation, said: "As RFHIC maps its future strategy for GaN semiconductors, including accelerated market demand for products in 5G, 6G, satellite communication and more, SweGaN's high-performance 6-inch GaN epiwafers for RF and power semiconductors – with exemplary high-power efficiency – provide a strong fit for our technological roadmap and diversification of gallium nitride epitaxial wafer suppliers."

MicroLED firm Kubos raises $2 million

UK-based firm to use funding to double red microLED efficiency for AR/VR displays

KUBOS SEMICONDUCTORS, a UK-based microLED material technology company, has raised $2 million to accelerate development of its cubic GaN technology, which can double the efficiency of red microLEDs.

It brings the company's total funding to $5.5 million and will enable Kubos to enter the microLED display market within three years through IP licensing.

Kubos says its technology will enable clearer, brighter, more efficient displays to be manufactured for augmented reality and virtual reality (AR/VR) applications.

The company has secured support from three of the most prolific and experienced veterans of the (UK) compound semiconductor industry and three strategic investors. Martin Lamb, Drew Nelson, and Geoff Haynes have a combined tenure of over 100 years in compound semiconductor materials development. Strategic investors are the Development Bank of Wales, FOV Ventures, and S4C Digital Media.

Caroline O'Brien, CEO of Kubos, commented: "Any UK compound semiconductor business would be thrilled to have just one of these movers and shakers in the industry supporting it and Kubos can now draw on the experience of all three. In addition, the strategic investor group that we have assembled brings vital insight into how the metaverse, digital content and AR/VR products drive display and microLED requirements. This, coupled with our unrivalled experience in compound semiconductors means that Kubos is now fully equipped and ready to deliver."

Martin Lamb, formerly CEO of Wafer Technology (acquired by IQE in 2000) and an angel investor with several successful exits, was instrumental in the formation of Kubos, and an early investor, and has guided and shaped the team. He has served as chairman since its inception and will continue in this role.

Drew Nelson, founder of IQE who stepped down as CEO in January 2022, has invested in Kubos and joins the board of directors.

Geoff Haynes also participated in this investment round and is a GaN semiconductor expert. A company he co-founded in 2008 to address the power semiconductors market, GaN Systems, was acquired by Infineon for $830 million last year.

The Development Bank of Wales has a track record of supporting breakthrough technologies and compound semiconductor businesses. FOV Ventures is focussed on spatial computing and S4C Digital Media plays a key role in the delivery of digital content to consumers. This investor group brings experience and knowledge that touches on all aspects of the AR/VR opportunity that Kubos aims to exploit.

Carl Griffiths, fund manager in the Technology Venture Investments team at the Development Bank, said: "Kubos' proprietary technology has the potential to improve the user experience for lighting and displays and accelerate the adoption of microLEDs across a wide range of applications. We are proud to be working with this exciting company of highly acclaimed engineers and scientists, and to have helped them re-locate to Wales to make use of the compound semiconductor expertise and infrastructure in the region."

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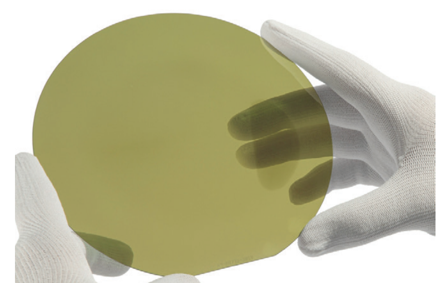
SiCrystal and ST expand SiC wafer agreement

A multi-year agreement with STMicroelectronics is helping to drive an increase in SiCrytals' production of SiC substrates manufactured in Nuremberg

ROHM and STMicroelectronics have expanded an existing multi-year, long-term 150 mm SiC substrate supply agreement involving SiCrystal, a Rohm group company.

The new agreement governs the supply of larger volumes of SiC substrates manufactured in Nuremberg, Germany, for a minimum expected value of $230 million.

Geoff West, EVP and chief procurement officer, STMicroelectronics, commented: "This expanded agreement with SiCrystal will bring additional volumes of 150mm SiC substrate wafers to support our devices manufacturing capacity ramp-up for automotive and industrial customers worldwide. It helps strengthen our supply chain resilience for future growth, with a balanced mix of in-house and commercial supply across regions."



"SiCrystal is a group company of Rohm, a leading company of SiC, and has been manufacturing SiC substrate wafers for many years. We are very pleased to extend this supply agreement with our longstanding customer ST. We will continue to support our partner to expand SiC business by ramping up 150 mm SiC substrate wafer quantities continuously and by always providing reliable quality," said Robert Eckstein, president and CEO of SiCrystal, a Rohm group company.

US SiC R&D facility celebrates topping out

THE UNIVERSITY OF ARKANSAS has celebrated a milestone with the topping-out of the Multi-User SiC Research and Fabrication Facility. The new semiconductor facility will enable the federal government – via national laboratories – businesses of all sizes and other universities to prototype with SiC, a capability that does not presently exist elsewhere in the United States.

Work at the facility is intended to bridge the gap between traditional university research and the needs of private industry. The aim is to accelerate technological advancement by providing a single location where chips can go from developmental research to prototyping, testing and fabrication. The 21,760-square-foot facility, located next to the National Center for Reliable

Electrical Power Transmission at the Arkansas Research and Technology Park, will feature approximately 8,000 square feet of clean rooms for fabrication and testing.

Education and training within the facility will also accelerate workforce development, helping supply the next generation of engineers and technicians in semiconductor manufacturing.

Arizona State University to explore potential of AlN

ARIZONA STATE UNIVERSITY'S Houqiang Fu, an assistant professor of electrical engineering, has received a US 2024 National Science Foundation Faculty Early Career Development Program (CAREER) Award to explore the potential of the ultrawide bandgap semiconductor AlN in power electronics.

Fu aims to develop AlN power FETs that control power flow with greater efficiency and can handle higher temperatures and more voltage than those made with silicon, SiC or GaN.

While AlN has promising properties, a lack of knowledge regarding how to effectively use the material for power electronics prohibits it from reaching its full capabilities.

Fu will lead a five-year investigation to determine how best to overcome the main problems facing the use of AlN.

This will focus on how best to grow the crystals needed for manufacturing AlN, refine it, fabricate it into power electronic devices and integrate the devices into electrical systems.

"The new AlN power electronics can offer superior performance and significantly impact grid modernisation, transportation electrification and greenhouse gas emissions," Fu says.

"The electronics will also dramatically increase the current grid infrastructure's resilience, reliability and efficiency. They will also help mitigate power disruptions' health and economic impact and improve energy security."

China's IP office validates GaN patents filed by EPC

EPC delights in the ruling of two foundational patents by the China National Intellectual Property Administration

US GaN company Efficient Power Conversion Corp (EPC) has announced that the China National Intellectual Property Administration (CNIPA) has validated the claims of an EPC patent titled *Compensated gate MOSFET and method for fabricating the same* (Chinese Patent No. ZL201080015425.X) for enhancement-mode GaN semiconductor devices.

The decision on April 30, 2024 follows an April 2, 2024 announcement from the CNIPA that confirmed the validity of key claims of EPC's Chinese patent titled *Enhancement mode GaN HEMT device and method for fabricating the same* (Chinese Patent No. ZL201080015388.2).

Both EPC patents were challenged by the Chinese company Innoscience.

Chinese Patent No. ZL201080015425.X covers the fundamental design and configuration of EPC's proprietary enhancement-mode GaN FETs with reduced gate leakage. Most industry participants employ the GaN gate technology covered by this patent.

"These are two of the foundational patents supporting our broad portfolio of innovations, and we are pleased that the CNIPA has again confirmed the validity of our valuable intellectual property," said Alex Lidow, CEO and co-founder of EPC. "Quick, fair and efficient decisions such as these reinforce the confidence in legal systems that companies need to operate globally."

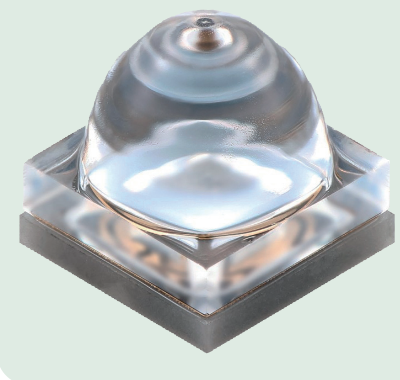
In May 2023, EPC filed complaints in the US federal court in Los Angeles and in the US International Trade Commission, asserting that Innoscience and its affiliates infringe patents of its foundational patent portfolio, which include the US counterparts of EPC's Chinese Patent Nos. ZL201080015425.X and ZL201080015388.2. In response, Innoscience had petitioned the CNIPA to invalidate the two Chinese patents.

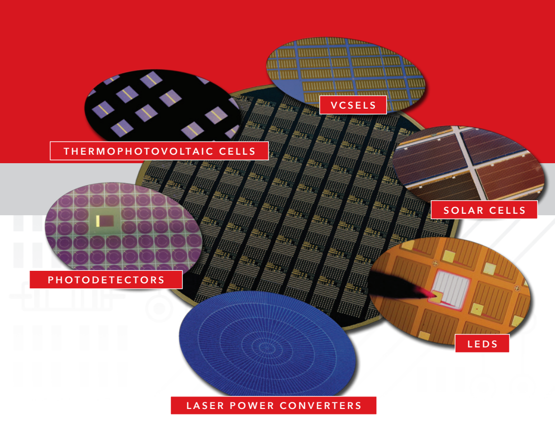
Toyoda Gosei develops high output UVC LEDs

TOYODA GOSEI has used its expertise in crystallisation and design of blue LEDs for lighting to develop UVC LEDs with a light output of 200 mW from a single chip driven by 350 mA.

Toyoda Gosei says these performance figures mean the LEDs can be used as a future alternative to mercury lamps.

By improving the LED structure and composition, the company says it has quadrupled the amount of light that can be extracted. Disinfecting capability is said to be about three times higher than previously available UVC LEDs.





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Infineon SiC modules to power Xiaomi EV

SiC power modules and bare die products will be used in new SU7 until 2027

INFINEON will provide SiC power modules HybridPACK Drive G2 CoolSiC and bare die products to Xiaomi EV for its recently announced SU7 until 2027.

Infineon will provide two HybridPACK Drive G2 CoolSiC 1200 V modules for the Xiaomi SU7 Max. In addition, Infineon is also supplying Xiaomi EV with a broad range of other products per car, including EiceDRIVER gate drivers and more than ten microcontrollers in various applications.

The two companies have also agreed to further cooperate on SiC automotive applications using Infineon's SiC portfolio.

Zhenyu Huang, VP of Xiaomi EV and general manager of the supply chain department, said: "Infineon is an important partner with leading technologies and resilient manufacturing capabilities in power semiconductors as well as a highly scalable microcontroller product portfolio. The cooperation

between the two companies will not only help stabilise the supply of SiC for Xiaomi EV, but also help us build a high-performance, safe and reliable luxury car with leading-edge features for our customers."

Peter Schiefer, president of Infineon's automotive division, said: "We are very pleased to work with dynamic players such as Xiaomi EV and provide them with SiC products designed to enhance the performance of electric cars even further. As the leading partner to the automotive industry, we are well positioned with our broad product portfolio, system understanding and multi-site manufacturing base to shape the mobility of the future."

According to the latest data from TechInsights, Infineon is the largest semiconductor supplier to the automotive industry. In addition to its number one position in automotive power semiconductors, Infineon also took the lead in the field of automotive microcontrollers last year.

UK's CSConnected appoints new managing director

HOWARD RUPPRECHT will take over as managing director of CSconnected with effect from 1 June 2024. Rupprecht will take over from Chris Meadows who has led CSconnected Ltd since its formation in 2017.

Meadows will continue to support a number of committed activities during the remainder of the year and will remain on the CSconnected board as a non-executive director.

Rupprecht has been working as a director of CSconnected since January; he brings a wealth of semiconductor industry and business development experience from both the public and private sectors.

Rupprecht said: "I would like to thank Chris for his relentless efforts in developing CSconnected and ultimately building a strong and highly recognised global brand for the Welsh Compound Semiconductor Cluster. It's good to be building on such a solid foundation as the team introduces new initiatives to support future cluster growth".

Wyn Meredith, chair of CSconnected, commented: "We are entering a new phase of expansion of the South Wales Semiconductor Cluster driven by the rapid growth of our industrial partners and a global semiconductor industry forecast to surpass $1 trillion per annum by 2030."

Meredith added: "Howard's appointment heralds an expansion of the CSconnected team to support the Welsh position in UK semiconductor initiatives such as the £160 million South Wales Investment Zone, and the £1 billion UK Semiconductor strategy."

CSconnected represents organisations who are directly associated with research, development, innovation and manufacturing of compound semiconductor related technologies as well as organisations along the supply chains whose products and services are enabled by compound semiconductors.

SEMILAB Metrology Solutions for Wide Bandgap Materials Characterization

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Implanted SiC characterization

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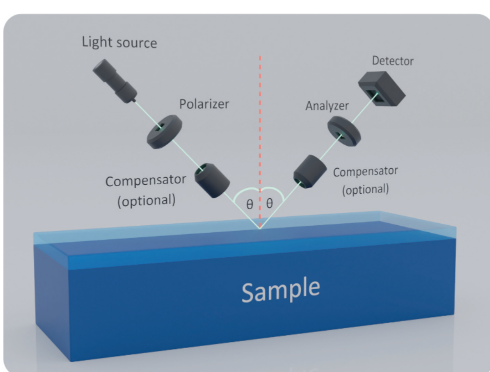


Microspot Spectroscopic Ellipsometry

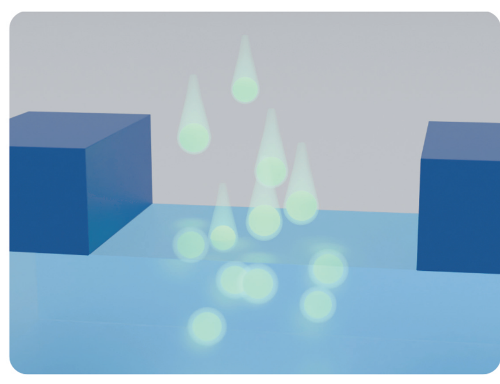
Thin film thickness and surface characterization

Al content measurement for GaN HEMTs

Layer thickness and homogeneity

Dielectric characterization

Bow/warp monitoring



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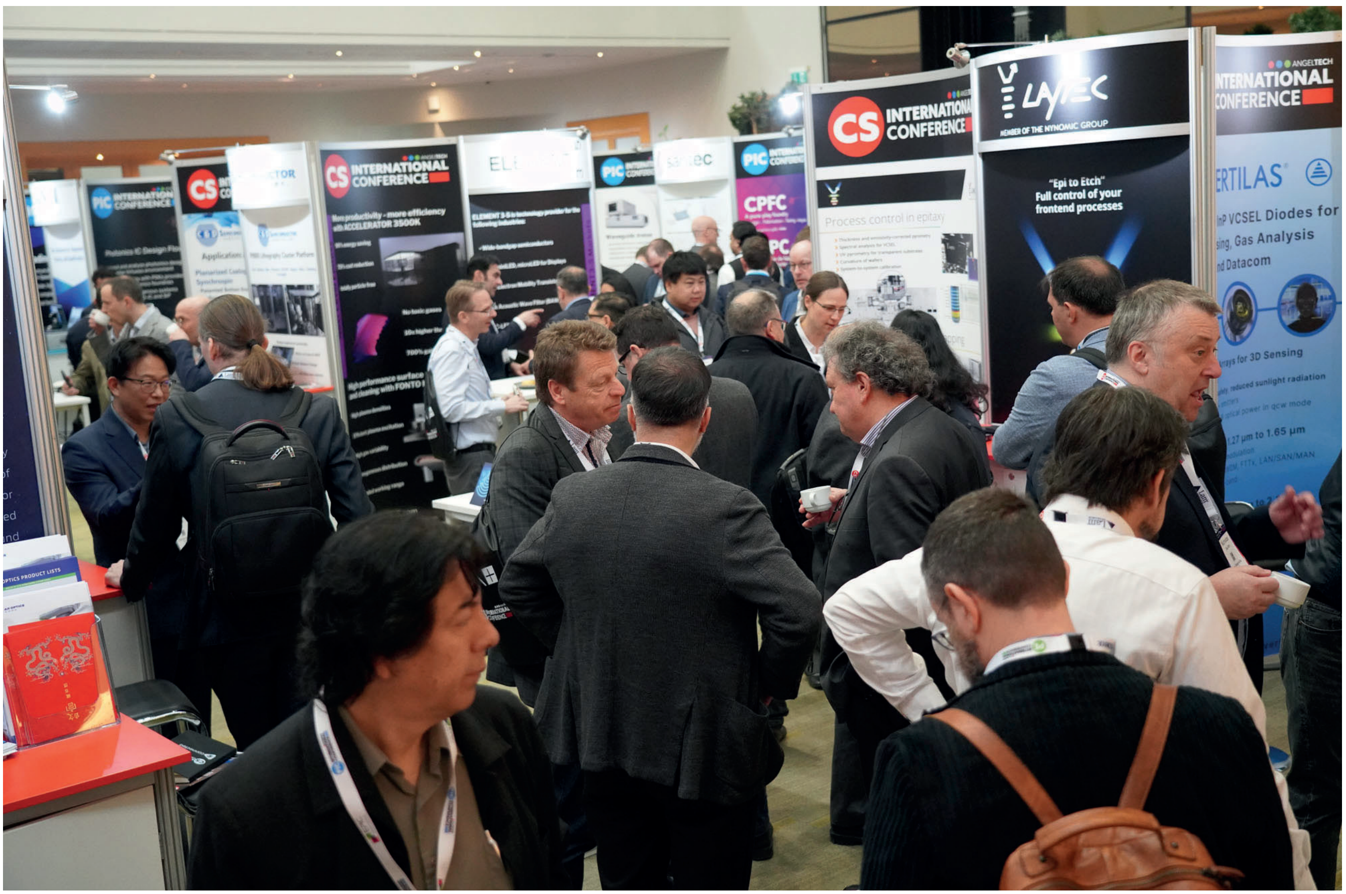

CS International champions a green agenda

Compound semiconductors are the driving force behind the more efficient use of electricity, reduced energy consumption for battery manufacture, and photovoltaic systems with integrated energy storage

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

TACKLING CLIMATE CHANGE understandably gets less media attention these days, with the focus shifting to the coverage horrendous conflicts around the globe. But the need to cut carbon footprints and get a grip on global warming is still of vital importance – and got the justifiable prominence it deserves at this year's CS International.

At this conference, held in Brussels on 16 and 17 April, many speakers detailed efforts to streamline the production and increase the volume of energy-efficient wide bandgap devices, while others outlined how optoelectronic devices can play their part in tackling climate change.

Significant progress in cutting emissions can come from increasing the electrification of our world, greater adoption of renewable forms of generation, and improving electrical efficiency. Around half of the world's electrical energy is used to drive motors, a proportion that's only going to increase.

Here there is a tremendous opportunity to boost efficiency, according to the International Energy Authority: this body claims that if energy is used more effectively in motors, around 25 percent of global electricity use could be saved, a goal that would be helped through increased adoption of devices with a wider bandgap.

➤ Delegates at Angeltech, which includes CS International, Power Electronics International and Photonics Integrated Circuits (PIC) International, benefitted from discussions in the exhibition hall, packed with around 80 sponsors.

Assisting in this endeavour is the ramp in worldwide production of SiC and GaN power devices, a trend that will continue, thanks to efforts by many manufacturers to increase their capacity. These chipmakers include STMicrolectronics, which has plans for expansion that were outlined at CS International by Mario Saggio, Company Fellow and R&D Design Director.

Saggio extolled the "outstanding characteristics" of SiC, arguing that while this class of device costs more than silicon rivals, it still delivers savings at the application level.

ST is a well-established player in the SiC industry. It started investing in SiC more than 25 years ago, and last year sales of its SiC devices generated $1.14 billion. The company dominates the SiC MOSFET market, with a share of more than 50 percent, according to Saggio.

This global player in the power industry has an incredible degree of vertical integration, stretching from raw materials to the design and manufacture of SiC products. It has a SiC substrate plant in Norrköping, Sweden, which manufactures 150 mm substrates and produces 200 mm variants with industrial quality and yield; and a new integrated plant in Catania, Italy, producing devices from 150 mm substrates. In Catania, pilot production started this year, and big plans for this plant include volume production in 2024, the migration to manufacture on 200 mm wafers, and the addition of 700 staff.

ST continues to evolve its SiC planar MOSFET technology. Second-generation devices were launched in 2017, followed by third and fourth generations that have benefitted from a reduced JFET and improved epitaxy, followed by an optimised edge alongside additional improvements to epitaxy. ST's fifth generation of SiC MOSFET, now in development, will benefit from reduced contact dimensions.

Comparing the second generation of MOSFET to that in development, specific on-resistance for the 650 V and 1200 V variants are lower by almost 40 percent and 50 percent, respectively. Additional improvements, supporting further energy savings, may come from the introduction of a superjunction design, which Saggio said is under consideration. Another company with big plans for SiC is Sanan Semiconductor, which is better known as the biggest producer of LED chips and epitaxial wafers in China.

Speaking on behalf of this company, Ajay Poonjal Pai, Director of Wide Bandag Innovation and Applications Engineering, told delegates that Sanan started developing SiC technology in 2014, and has become China's first vertically integrated manufacturer of these devices. The company has control of the complete supply chain, from SiC crystal growth to the packaging of power devices.

Backed by $2.3 billion of investment, Sanan is building what Pai describes as a state-of-the-art mega-fab. It's first phase is now complete, enabling a ramp in production to 200,000 wafers per year. Following further work, capacity is expected to increase to 500,000 wafers per annum. Current production is on 150 mm SiC, but the company will switch to 200 mm wafers by the end of this year.

Sanan entered the SiC power device market with the diode, and shipped more than 100 million in 2022. Based on its third generation of diode, the company has recently released a fourth generation that majors on a low forward voltage, and a fifth that boasts high surge-current capability.

Later this year Sanan will launch its first range of SiC MOSFETs. This automotive-qualified product portfolio will offer blocking voltages of 650 V, 1200 V and 1700 V.

Another champion of SiC is Wolfspeed. Speaking on its behalf at CS International, Pranjal Srivastava, who is responsible for strategic business development at the global level, detailed benefits realised by using SiC devices, rather than those made from silicon, in 25 kW three-phase motor drives.

This opportunity, which offers "immense market potential", can trim losses by up to 50 percent.

To arrive at that figure, Srivastava and colleagues compared the efficiency of power-factor-correction units with a silicon IGBT design, operating at 20 kHz and having a power density of 3.5 kW/litre, with a design using SiC MOSFETs operating at 45 kHz and providing a power density of more than 4.6 kW/litre. The unit using devices with a wider bandgap enables an increase in peak efficiency from 97.2 percent to

➤ Over the 16 and 17 April, delegates at CS International could hear from more than 40 presenters, covering a wide variety of topics within the compound semiconductor industry.

98.5 percent. In addition, the team have considered gains in the performance of an inverter, with SiC providing a 1.1 percent improvement in efficiency.

Taken together, the efficiency gains total 2.4 percent, equating to 600 watts. Srivastava has calculated that this enables a financial saving of more than €7,000, based on today’s electricity costs in Germany and assuming that this motor runs almost continuously for 15 years.

Galloping GaN

While SiC attracted the greatest coverage at CS International, it could be argued that GaN offers at least as much promise in the long term.

➤ CS International is co-located with Power Electronics International and Photonics Integrated Circuits (PIC) International a trio that proceeds the Executive Summit.

Covering both technologies is market analyst Richard Eden from Omdia. He explained that his forecasts for the GaN market are getting more and more positive. Back in 2020, he forecast this market to be worth about $1.5 billion by 2029 – and in 2021 and 2023, he revised this figure to just over $2 billion and then just over $3 billion.

What applications will account for all these sales by the end of this decade? Eden expects deployment to be broad, seeing opportunities in power supplies, electric vehicles, and a number of industrial applications. Offering detail, he suggested that GaN will win sales in telecom power supplies, such as those used for cell phones and cellular base stations, as well as power supplies used in TVs, consumer audio, data centres and AI servers. In the electric vehicle sector, Eden has identified opportunity in niche powertrains, such as those involving 96 V batteries and 48 V mild hybrid vehicles, as well as on-board chargers. GaN may also find deployment in motor drives for the likes of delivery drones, robotic lawn mowers and vacuum cleaners, as well as power tools and precision motors for surgical robots.

The phenomenal growth of GaN, now tipped by Eden to climb to more than $6 billion in 2032 from this year’s base of below $1 billion, may be even faster if QPT impacts the market. Its CEO, Rupert Baines, argued that his company is offering revolutionary technology that will stop GaN being limited to low powers and soft switching. Pointing out that faster switching saves more energy, he championed a future that combines kilowatt powers with gigahertz switching frequencies.

Baines believes that QPT’s technology can deliver energy savings for motors of at least 5 percent. This translates to a cut in global CO_2 emissions by 400 million tonnes per year and a trimming of electricity bills by $66 billion per annum.

Optoelectronic opportunities

Two of the consequences of greater electrification are an increase in the demand for batteries, and the need to supply more electrical energy when it is needed. Compound semiconductors have a role to play on both fronts, with opportunities outlined at CS International.

Battery production is an energy-intensive process, with 47 percent associated with the drying of a thick, wet, lithium-containing slurry that’s applied to a metal foil. The incumbent approach for drying this slurry involves convection, in ovens 60 m long.

One promising alternative, described by the CTO of Trumpf Photonics, Roman Koerner, is to turn to vast arrays of VCSELs. He explained that this could reduce the heating system for battery manufacture to just 10 m in length, while improving efficiency (for more details, see “New Vectors for the VCSEL”, p. 28.)

For the generation of renewable energy, concentrated photovoltaics has much promise. Tremendous falls in the price of silicon panels around the time of the global credit crunch thwarted the success of the first generation of pioneers, but now more than a decade on, this technology is seeing a resurgence, thanks to important innovation by RayGen of Australia. Detailing its novel approach to CPV, Kira Rundel, Head of Strategic Projects, explained that the key to success is supplying energy when it’s needed, rather than just when the sun is shining. That’s realised by combining electricity generation with thermal energy, with the later coming from the cell’s cooling water that’s used to heat a thermal store. This store can then generate electricity when it’s needed, via a turbine. A 4 MW plant has now been built with this technology, and bigger projects are in the pipeline.

While the likes of RayGen, Trumpf and the producers of wide bandgap power devices will gain the plaudits for enabling compound semiconductor devices to green our planet, they need the support of strong supply chains. Such companies also featured at CS International, with manufacturers of epitaxial growth and metrology systems updating delegates via conference presentations and discussions in the exhibition hall, accommodating around 80 sponsors.

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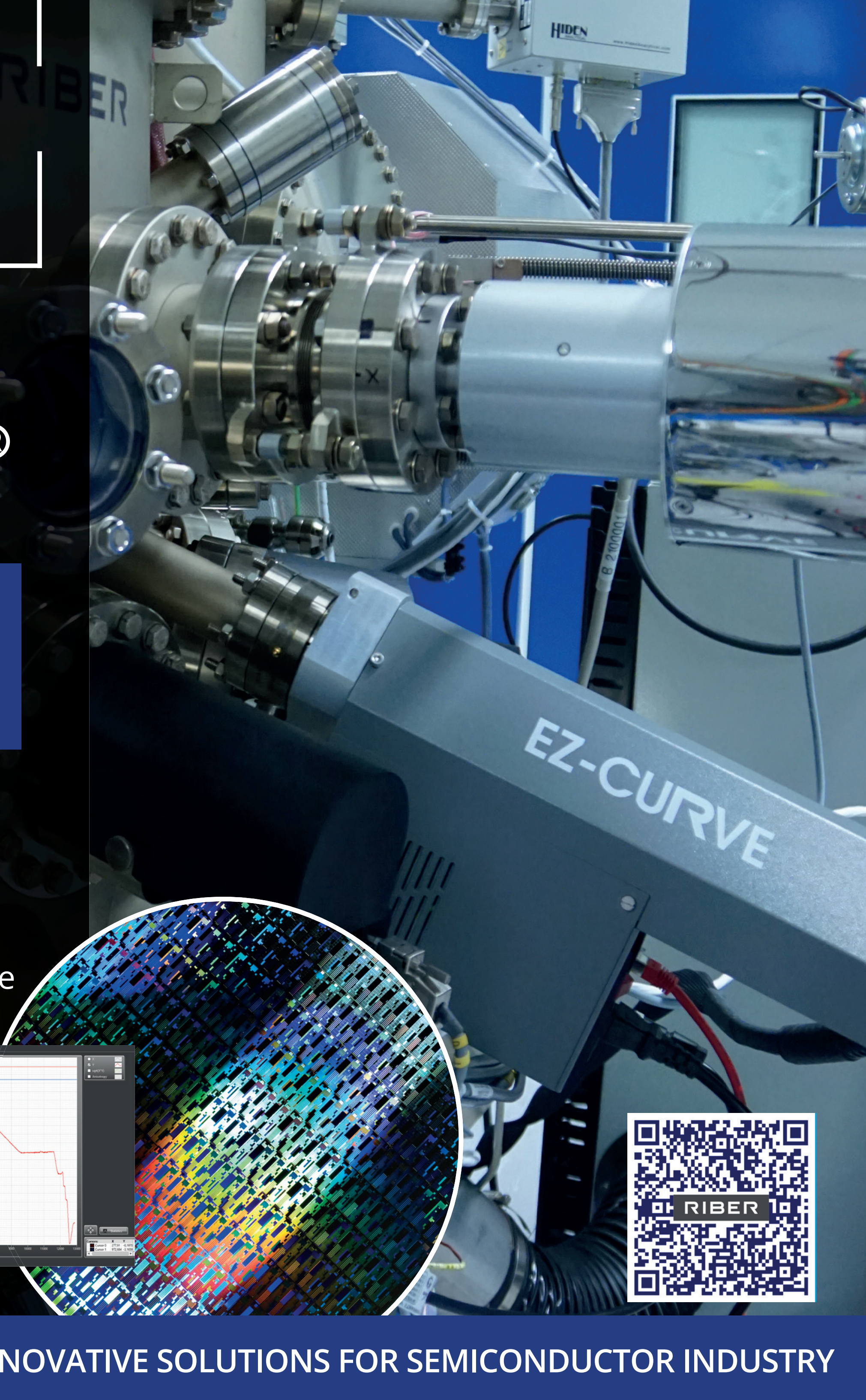

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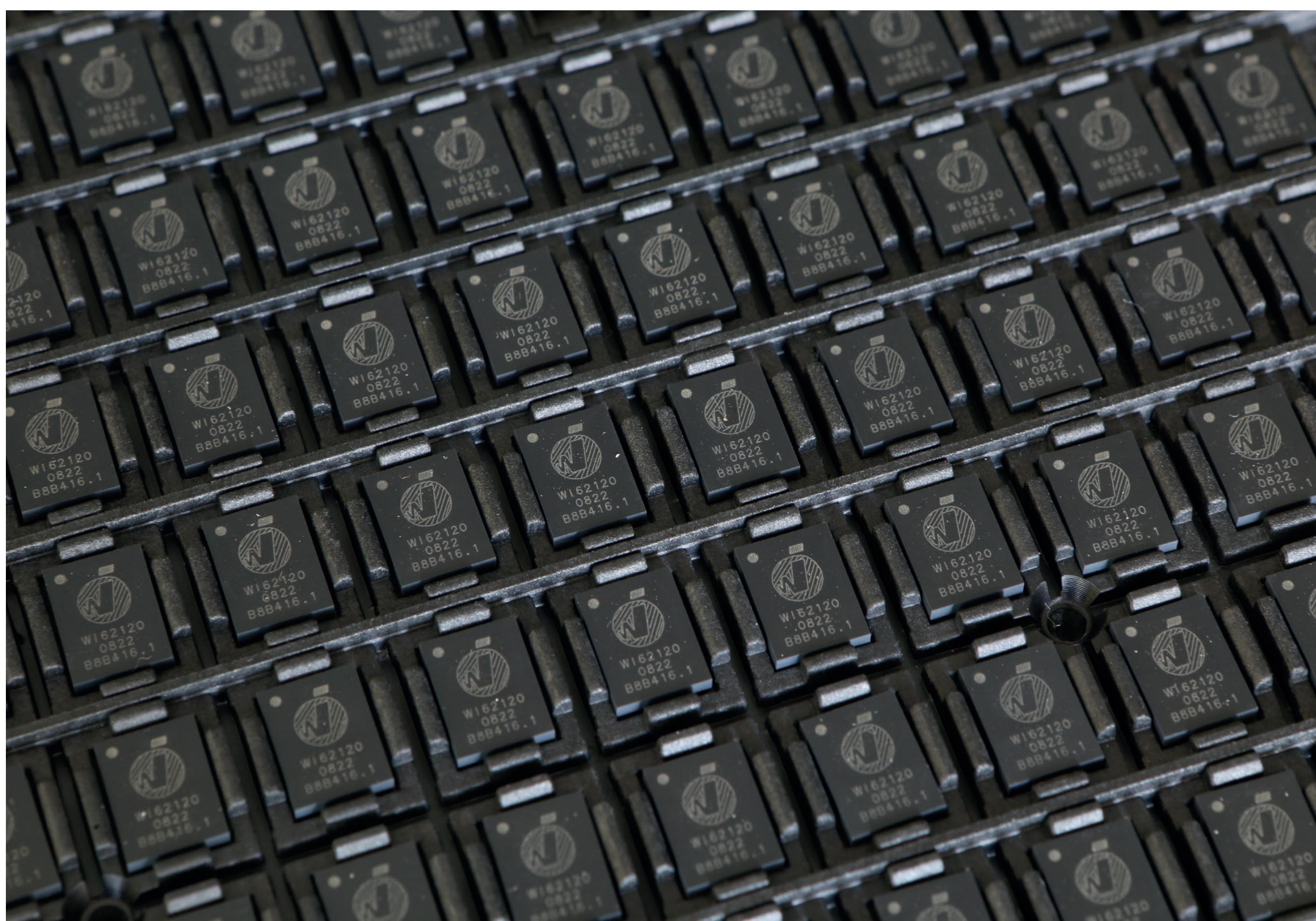


A wise investment in the **GaN IC**

French start-up Wise-Integration has raised an additional €15 million to expand its commercialisation of the GaN IC

BY RICHARD SATEVENSON, EDITOR, CS MAGAZINE

OVER THE LAST FEW YEARS, GaN has become more familiar with the general public than ever, thanks to its success in fast chargers for mobile devices. Products on sale trumpeting the use of this wide bandgap material are widely promoted, such as the Anker 120 W GaN Charger and the Wavlink 100 W GaN Charger. There is no doubt that the fast-charging market has been great for growing sales of GaN devices, but commoditisation has now kicked in, creating a need for diversification.

To open up new opportunities for the GaN transistor, its producers need to increase its power-handling capability, a move that would enable the introduction of this material in power supplies in telecom, industrial and electric vehicle markets. Another strategy is to enhance the functionality of GaN – gains on this front will also drive its deployment, and help it displace the incumbent, silicon.

One company that's simultaneously pursuing both these opportunities – higher powers and greater functionality – is Wise-Integration, the fabless spin-off of CEA-Leti. An initial funding round of €2.5 million led to the development and commercialisation of two product families: a GaN IC; and a silicon-based control chip, which can drive GaN with digital signals. And this February Wise-Integration raised an additional €15 million to expand its commercial activities.

"We are now moving to market, and we need to push the technology to customers," claims company CEO Thierry Bouchet, who says that while the level of recent investment may not be that high by US standards, it is significant, and will fund Wise-Integration until the middle of 2026.

One of the company's primary objectives is to win sales for its digital control technology, a goal that

will be targeted by supporting customers with application engineers. The French start-up has developed embedded software that's implemented on standard microcontrollers, and it aims to use this to promote digital control of GaN devices in the power supply market.

"It's a differentiation versus the competition," argues Bouchet. "We are not only providing GaN – we also leverage all the GaN performance with digital control."

The company's other big plan is to drive its technology into higher-power applications.

"Today we target consumer, low-power applications," says Bouchet. "We need to move now to industrial, server, telecom and also automotive products."

While GaN ICs are not as mature as their discrete cousins, they are on the market, with suppliers limited to not just Wise-Integration. There is also Navitas, the first company to introduce the GaN IC, in the form of a charger for the smartphone. For all, the challenge is to now produce successful products providing far higher powers.

What distinguishes Wise-Integration from its competitors is its approach to integration. "We focus on the digitalization," remarks Bouchet, pointing out that rivals drive GaN with analogue signals.

Benefits of a digital drive include the opportunity to turn to very high frequencies, and to produce incredibly thin power supplies with a low bill of materials.

"A key targeted market for us is the power supply for monitors and TVs," says Bouchet. "You have a very small, very thin display, and all the OEMs are looking to introduce power supplies inside the panel, so they need to have a very thin power supply. Our technology allows this requirement, thanks to digital."

Wise-Integration has produced a demonstration board for a 300 watt TV power supply that involves switching GaN at 1 MHz. Such high frequencies threaten to produce electromagnetic interference and noise, potential problems that have already been addressed.

Supply chains

To produce its products, Wise-Integration partners with TSMC, one of the first open foundries for GaN technology. TSMC's expertise includes the epitaxial process, allowing fabless firms to use a relatively short supply chain. For Wise-Integration, alongside TSMC it uses AEC for packing and testing and Alter, a French firm, for device qualification.

Bouchet and colleagues are now trying to secure a second source for chip production, to increase the robustness of their supply chain. This would allow Wise-Integration to cater for all eventualities, including unforeseen production problems at TSMC, or a decision by this giant to devote its capacity to other companies.

While GaN ICs are not as mature as their discrete cousins, they are on the market, with suppliers limited to not just Wise-Integration. There is also Navitas, the first company to introduce the GaN IC, in the form of a charger for the smartphone. For all, the challenge is to now produce successful products providing far higher powers

"The second source could be far closer to home, with options including a European GaN foundry," says Bouchet.

While working on that, Wise-Integration plans to ship a million GaN devices this year, and then a million digital controls. These products will be offered as bundles, which will accelerate sales, by enabling the company's digital controller to be sold alongside up to four of its GaN ICs.

The company clearly has many exciting plans for the next year or so that could open the door to a new era for GaN power devices.

➤ Thierry Bouchet, CEO and co-founder of Wise-Integration, previously led Adis Innovation, a manufacturer of high-performance discrete and integrated power devices.

Overhauling engineering education

To ensure the future of compound semiconductor innovation, a new approach is needed to engineering education and talent development

BY RODNEY PELZEL FROM IQE

MUCH HAS BEEN WRITTEN about compound semiconductor innovation and the vital role it plays in shaping the devices that underpin modern life. However, there is little substantive information on the most critical component of this innovation – technical people who are also adept at critical thinking. Few would deny that the single most important factor for successful innovation is maintaining a world-class talent pipeline that fosters teamwork while supporting diversity, equity and inclusion.

During my career in compound semiconductor technology, which spans more than 20 years, I have been responsible for hiring and managing all levels of operational and technical staff, from operators to Ph.D. engineers and scientists. This experience has imparted within me a universal truth that may surprise you – it's not possible to rely upon a person's educational background to predict their technical proficiency and their effectiveness. These findings have led me to conclude that the problem does not lie with any individual, but is deeply rooted in the way we train our technical workforce. And the solution? Without doubt, it has to be a radical overhaul of our education system.

All this may sound rather strange, given the success I've enjoyed from following the 'traditional' educational path. I hold a B.S. and Ph.D. (both in chemical engineering) from established, reasonably prestigious universities, a foundation that has served me well in steadily progressing my career as a technologist.

Throughout this time, I have been passionate about progressing technology. Advances on this front depend on people equipped with the right skills, a requirement that can only be ensured through change. So that I avoid any confusion, let me state my position in simple terms: the educational system is too formulaic, and it fails to foster the type of innovative mindset that's required to make a person a top-notch technical thinker. The unfortunate reality is that we are not teaching students how to become effective problem-solvers, or how to think about open-ended situations.

To truly break the above-noted paradigm requires a complete change in how we educate future generations, with a shift in focus from strictly linear to lateral thinking.

Note, though, that I'm not saying that there is no place for fundamental science and engineering education. In fact, the opposite is true. My point is that by teaching fundamentals in isolation, students fail to gain the required proficiency to use

information in real-world situations. This is an issue for all levels of education, from school through to Ph.D. programmes. What's needed is an overhaul in how we teach the fundamentals. The downside of the current approach is that people are leaving formal education ill-prepared to make a true impact in innovation.

Fixing this will require a significant change in our technical education programmes. It is essential that they are revolutionised to incorporate close collaboration between industry and academia.

What I am envisioning is an extreme version of collaborative on-the-job training, with book-learning supporting real problem solving, rather than problem solving following book-learning.

Let me be clear that I am talking about more than internships, or short placements in industry. Rather, I am advocating a radical overhaul to the entire programme, with a shift in focus.

In an extreme scenario, a person might attend Company X University, who has partnered with an academic institution to provide the fundamentals. To be fair, pockets of such programmes already exist. However, they are far from the norm, with formal school education entrenched as the more prestigious/accepted credential.

Shifting the training of engineers along the lines I recommend would have a number of interesting 'side effects'. One is fostering team-work, as the approach I am championing would demand this to ensure that a member of a team succeeds. Today, teamwork is neither required nor rewarded, and one can obtain an extremely prestigious degree without understanding how to effectively collaborate. Using my own Ph.D. education as a reference, I was rewarded for getting to the answer as quickly as possible on my own – and experience has shown that this is not unique to me.

Another side-effect of my proposal is that it would impact the designation of degrees, causing them to become more 'general'. For example, students would work towards an engineering degree with a focus on semiconductors, rather than an electrical engineering degree. This shift would also alter what is meant by advanced degrees, such as the MS and Ph.D., and their level of applicability to a differently educated workforce.

One great benefit of what I'm suggesting is that it would lead to improvements in diversity, equity and inclusion. This would stem from lowering barriers to entry for the educational system. What's more, it could accommodate those with a different background, or a different style of learning that does not fit well within the current system. Such students may even thrive and flourish in a system rewarding an 'out of the box' approach.

As we seek to push the frontiers of innovation, there is no doubt that we need a different type of technical workforce. Real innovation hinges on collaborative lateral thinking, and the ability to solve ill-defined, open-ended problems. To excel in this regard, there must be significant change in how the technical workforce is trained and educated.

Uncovering the secrets of **SiC epilayers**

Comprehensive characterisation of SiC layers is accomplished with an enhanced form of Fourier transform infra-red spectroscopy

BY ESZTER ÉVA NAJBAUER FROM SEMILAB

➤ Above: Semilab's EIR-2300 FTIR-based metrology system

TECHNOLOGY continues to progress, influencing our daily lives and impacting humanity's efforts to preserve our environment. Against this backdrop, one force for good is the electric vehicle (EV), which benefits from modern power devices; these vehicles are six times more energy-efficient than those incorporating a combustion engine. But not all advancing technologies are good for the ecosystem. The acceleration in the data that is generated online every second contributes significantly to carbon dioxide emissions. Here, power supplies are required to run continuously, while demanding efficient cooling and significant storage space.

At first glance, these two domains – EVs, and the power supplies for maintaining the internet – appear to be disparate. But they share common imperatives, which are the pursuit of a higher efficiency and greater reliability through further improvement to one key component: SiC.

For high-power applications, SiC is superior to silicon on several fronts. Thanks to its high performance-to-size ratio, its greater energy efficiency, its low switching losses and its long lifetime, systems based on SiC are lighter, charge faster, and have fewer components. All these factors are valued by the EV industry. Additional benefits include high operating frequencies and temperatures, a low thermal expansion and a high thermal conductivity that reduces cooling requirements. These are strengths that deliver a huge advantage when SiC devices are deployed in data centres.

EVs and server parks are just two examples of the many ways in which SiC is making an important contribution to our daily lives. Due to its remarkable properties, there is an ever-growing demand for these compelling devices, which are amplifying waves of continuous technological improvement.

Price, however, is still a bottleneck in many SiC applications. Based on figures from May 2023, the cost of a single SiC MOSFET inverter is double that of a silicon IGBT with an equivalent performance (that is for transistors capable of withstanding 1200 V and delivering 200 A). Accounting for the lion's share of the cost of the SiC MOSFET is its native substrate, indicating that high value is added early in the process. Due to this, it is vital to closely monitor each step in the process flow while developing highly stable production technologies. It is the norm for substrates to undergo rigorous inspection steps focusing on geometric properties, resistivity, defect assessment, surface roughness, and crystal orientation, and for epi wafers to be monitored for their epilayer thickness, doping concentration, level of defects, degree of surface roughness, and for any presence of contamination.

A critical determinant of performance and functionality is the thickness of the epitaxial layer. This directly governs crucial electrical parameters, such as junction capacitance, and impacts several parameters in the fabrication process, including etch rates. As one of the key roles for the epilayer is to isolate the current-carrying components of the device, even small variations in epilayer thickness can have profound repercussions on the performance of diodes and MOSFETs.

To fulfil the growing demand for SiC power electronics, while executing high yields and retaining competitiveness, manufacturers of these devices are having to address the challenge of migrating from 150 mm to 200 mm wafers while maintaining uniformity in both layer thickness and electrical properties.

Often optical monitoring techniques are chosen for measuring the thickness of SiC epitaxial layers. They include Fourier-transform infrared (FTIR) reflectometry, a non-destructive technique that provides fast and accurate values for epitaxial thickness from the sub-micron to several-hundred-micron range, while avoiding risks of additional defects and contamination.

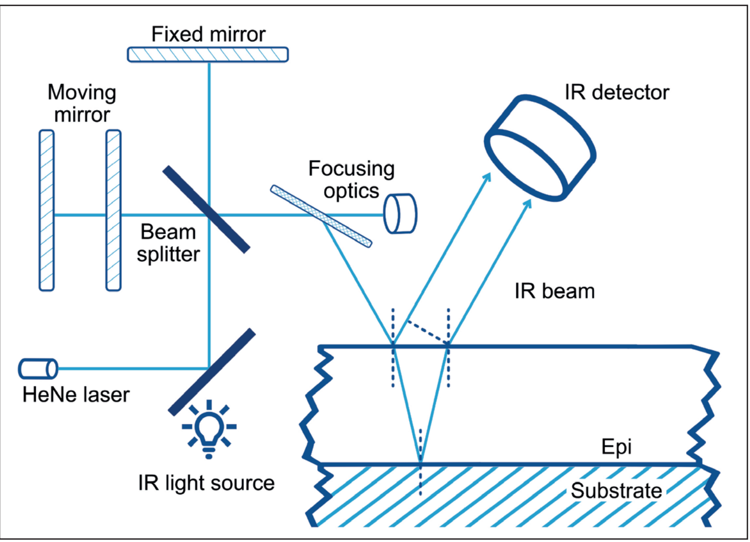


Figure 1. Measurements with a Michaelson interferometer involve reflection of infra-red light from an epitaxial sample. Infrared light is reflected off the top of the epilayer as well as the interface between two layers (epi-substrate or epi-buffer). Interference of these two rays enables the epitaxial layer thickness to be calculated.

Principles of FTIR

FTIR is a non-contact measurement technique that provides the the semiconductor industry with a wealth of information. Its capabilities include industry-standard rapid interferogram measurements of epitaxial thickness, reflectance spectrum measurements for multilayer analysis and dielectric composition measurements, and transmission measurements for absorption peak analysis.

At the heart of every FTIR spectrometer is a Michaelson interferometer (see Figure 1), which consists of a beam splitter and two mirrors: one is moveable and the other static. The position of the moving mirror is changed gradually when measuring a sample. Measurements are made of the light transmitted through and reflected from the sample. Detected signals create interferograms,

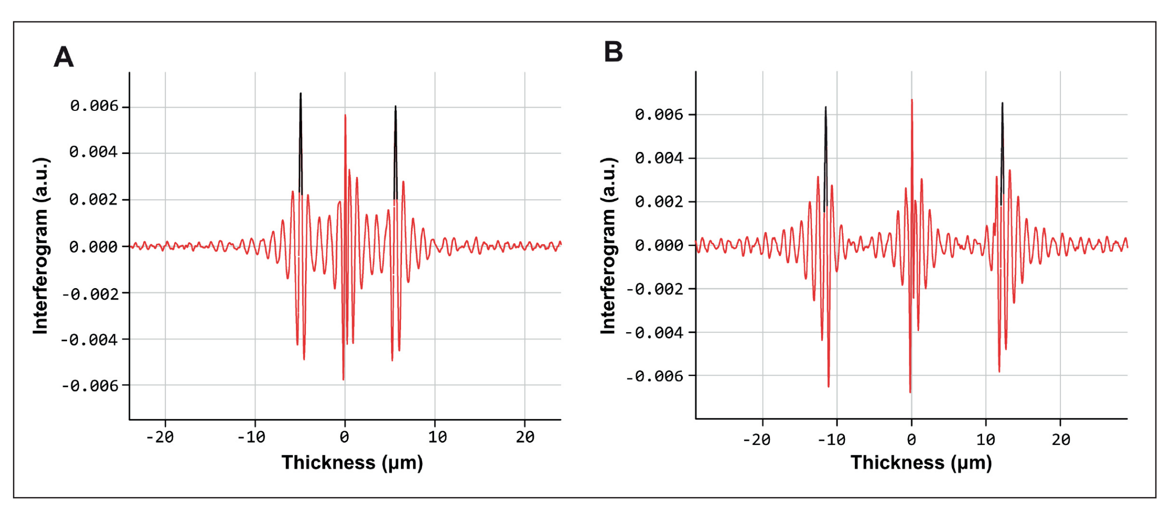


Figure 2. Interferogram of 5 μm (a) and 12 μm (b) SiC epi-samples. Fits of the sideburst maxima are shown in black.

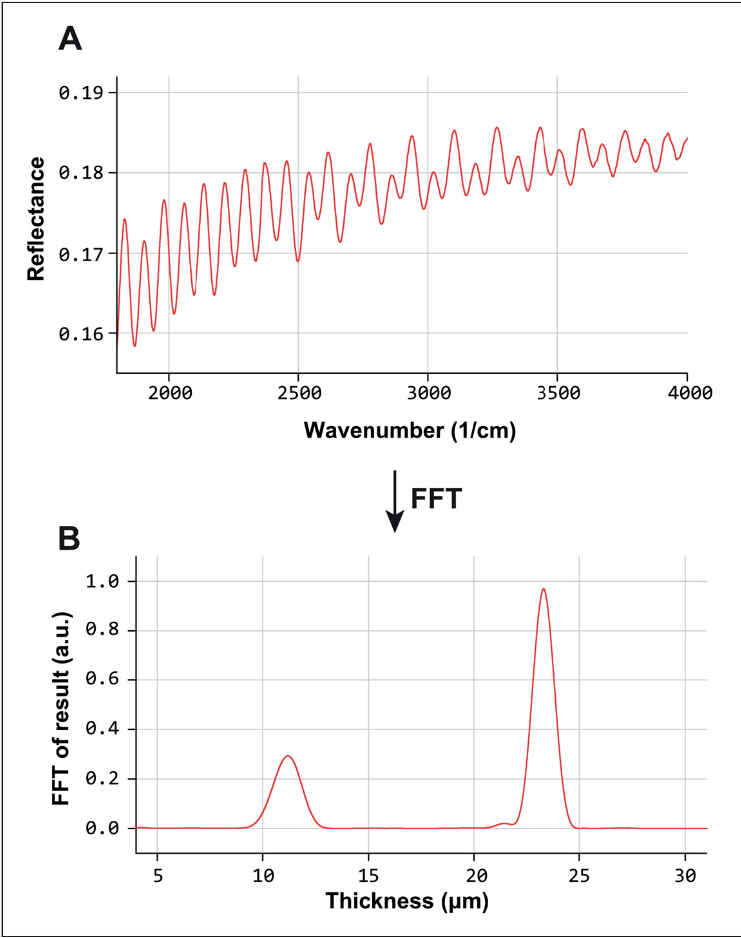


Figure 3. Baseline fringes in the reflectance spectrum of a SiC epi-sample (top), and the thickness peak obtained by FFT (bottom). Spectra were measured on a regrown epi-sample in collaboration with Fraunhofer IISB, Erlangen. The FFT result shows two peaks: a total thickness peak at around 23 µm, and a peak at the thickness of the top epilayer, at around 11 µm. The thickness of the bottom epilayer, around 12 µm, can be obtained as a difference of the two.

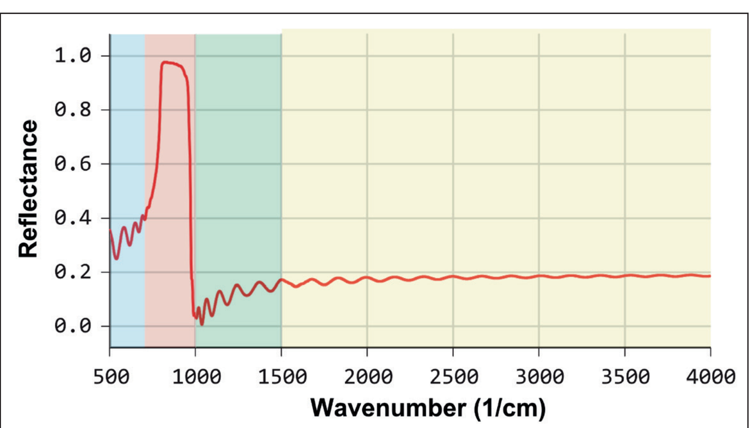


Figure 4. Reflectance spectrum of a SiC epi sample, with the four spectral regions marked with different colours. Blue: 500-700 cm^{-1} shows thickness oscillations. This region is most sensitive to the effect of dopant concentration. Red: 700-1000 cm^{-1} is the reststrahlen band, a highly absorptive region. Green: 1000-1500 cm^{-1} is a transient region between an absorptive and a transparent region. 1500- cm^{-1} is a transparent region showing thickness oscillations.

with the intensity of outcoming light a function of the moving mirror's position. For every point in the interferogram, all wavelengths in the spectrum are monitored simultaneously.

Metrology methods

Although a typical SiC epitaxial structure consists of only a high-resistivity SiC epilayer and a buffer layer on a low-resistivity substrate, there can still be large variations in layer thickness, dopant concentration, and the number of layers. When analysing any sample, its architecture will influence the most suitable method of analysis, which will also be governed by the most important characteristics to uncover.

At Semilab, we produce FTIR-based Enhanced Infrared (EIR) systems that offer a choice of three different analysis methods. Each has different capabilities and advantages for SiC epitaxial thickness measurements. We now consider, in turn, these three methods: interferogram subtraction, fast Fourier transformation (FFT), and optical modelling.

Interferogram subtraction is a widespread, robust method for determining the thickness of the epilayers. Quick and easy to set up, this approach provides information on a single layer's thickness. Analysis is based on determining the position of the interferogram's secondary maxima, known as sidebursts. These arise when the optical path difference between the interferometer's mirrors matches the path difference of the rays reflected from the top of the epilayer and the epi-substrate interface. The thickness of the epilayer is proportional to the sidebursts' position, and is easy to calculate by taking into account the sideburst position, the incidence angle of the infra-red light, the wavelength of the laser, and the refractive index of the sample.

It should be noted that it is more challenging to analyse interferograms for SiC than silicon. Due to wavelength dispersion in SiC, there are several secondary maxima in the interferogram. So, to ensure reliable analysis, there is a need for post-processing of the interferograms.

Our software is more than up to this task, providing advanced SiC interferogram analysis features, including filtering, as well as various algorithms for finding and fitting maxima/minima. Depending on the sample structure, our tools for interferogram analysis may also be used to determine the total thickness of the layers for multilayer samples. However, we advise validation of the results by other analysis methods. An example of interferogram analysis of two epi structures to determine the total thickness of the buffer and the epilayer is shown in Figure 2.

More details of the epi structure can be uncovered in reflectance spectra by considering details in characteristic baseline oscillations, also referred

to as fringes, that arise from interference of light reflected from each layer's surface. It is these baseline fringes that 'encode' thickness information in the reflectance spectrum. Thickness values can be extracted from reflectance spectra in a fast and unambiguous manner by undertaking FFT of these fringes. As a result, we obtain the frequencies present in the signal. These can easily be converted into thickness values using the refractive index of the layer in question. For a one-layer epistructure, FFT produces a single peak that reveals the layer thickness, while measurements on multi-layer samples may produce several peaks, including those uncovering the total thickness of the stack.

To illustrate this point, see the FFT analysis of a two-layered regrown epi-sample (see Figure 3). There are two peaks, corresponding to the total thickness and the thickness of the top layer. Subtracting one from the other provides the thickness of the bottom layer.

While FFT is great way to get quick information on epiwafer thickness, using analysis that's easy to undertake, this technique has some limitations. For samples with several layers, the result is ambiguous, in terms of the order of the layers. Another downside is that the baseline curvature in the SiC reflectance spectra causes a strong artefact to appear close to zero thickness that may obscure peak(s) of interest. Due to this issue, FFT analysis has to be restricted to samples with relatively thick epilayers, such as more than 2-3 μm.

Compared with the other two techniques, interferogram subtraction and FFT, optical modelling is the most comprehensive. This approach begins by making assumptions of a structure, using estimated thicknesses and dopant concentrations. From this starting point, a reflectance spectrum is predicted, using physical laws. Depending on the modelling approach, this may involve the use of the Drude dispersion law, employed to model the effect of free-carrier concentration and using Lorentzians to model the background. By changing input parameters, one can fit the predicted spectrum to the measured reflectance spectrum, and extract important information related to the characteristics of the epilayers.

SiC epi (Phase 2)
Thickness = 1735.2 nm

SiC buffer (Phase 1)
Thickness = 412.2 nm

SiC substrate (Substrate)

➤ Figure 5. Structure of a typical SiC epi-sample with a 0.4 μm buffer layer (phase 1) and a 1.7 μm epi layer (phase 2).

From a seed of an idea to state-of-the-art metrology solutions

GLOBAL DIGITALIZATION and technological transformation are fuelled by the semiconductor industry, and its evolution and further development is heavily dependent on cutting-edge measurement and testing equipment. A key supplier of these critical metrology tools is Semilab, which continues to invest in research and development.

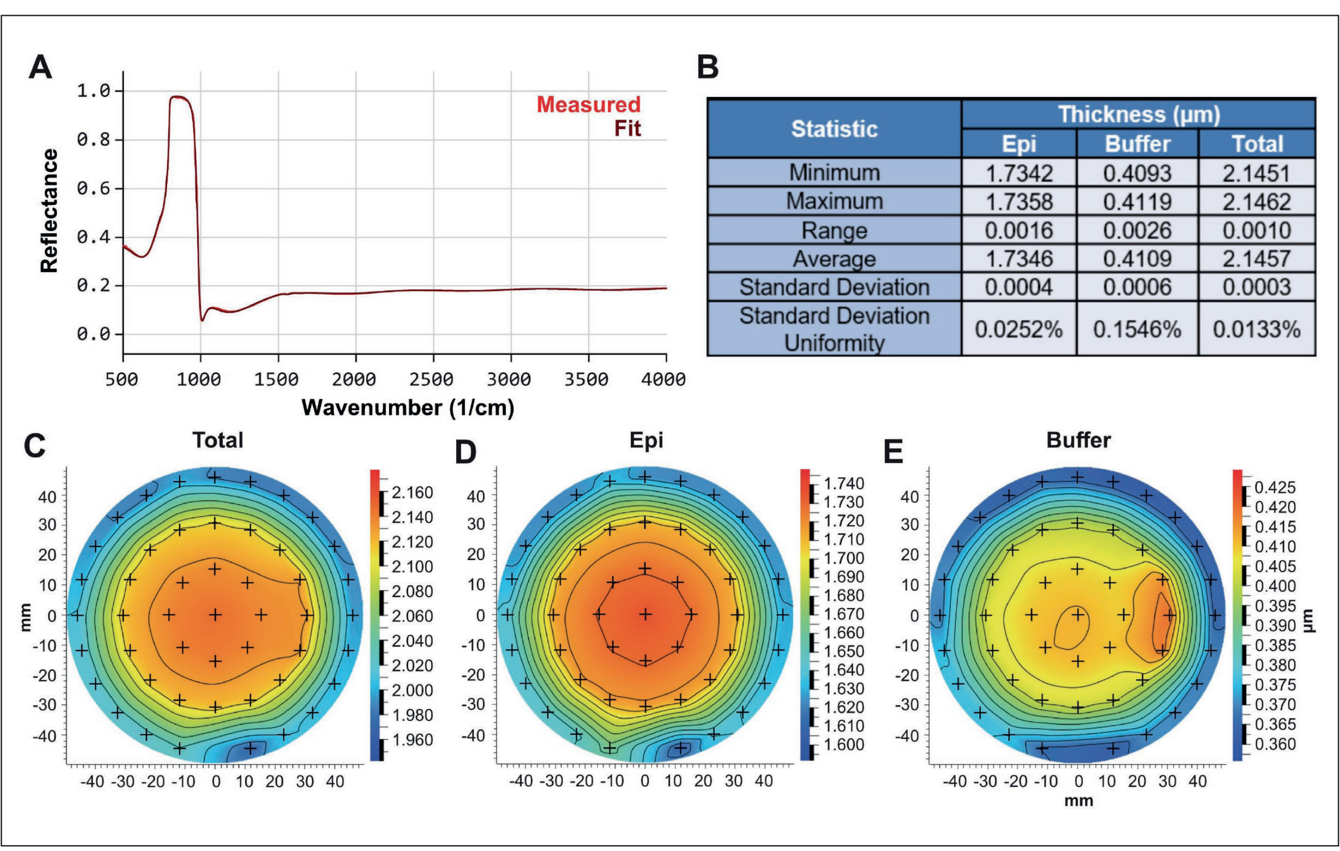
Founded in 1990 in Budapest, Hungary, by a handful of researchers, Semilab is drawing on more than 30 years of scientific expertise and know-how in electrical and optical measurement methods to create a strong portfolio of industrial metrology systems. These widely used systems, which provide advanced process control, are narrowing the gap between industry requirements and metrology capabilities.

Semilab is pursuing the development of measurement techniques based on a deep understanding of the key processes and requirements for microelectronics production. It is already providing state-of-the-art metrology solutions to leading wafer manufacturers, IC device makers in the more-than-Moore market segment, and solar and display industries worldwide. These instruments are contributing to more efficient production and control.

At Semilab, key industry needs are met by creating solutions, going from an original idea to a finished product that transforms new ideas into reality. Through an in-depth analysis of the methodology, intricacies of instrumentation, and nuanced data analysis techniques, Semilab works to unveil the transformative potential of this innovative approach within the compound semiconductor landscape. A smarter future beckons, thanks to these initiatives.

There are four distinct regions in the SiC reflectance spectrum, each sensitive to different layers and parameters (see Figure 4). Between 400-700 cm^{-1} there are thickness oscillations associated with the epitaxial structure, and this is the region most sensitive to free-carrier absorption. Next to this is a spectral domain known as the reststrahlen region, spanning 700-1000 cm^{-1}, where high levels of absorption occur for wide bandgap semiconductors. This part of the SiC reflectance spectrum is most sensitive to the top layer of the sample. Beyond this, from 1000-1500 cm^{-1}, is a transient region, positioned between a highly absorptive and a transparent one. In the transparent region above 1500 cm^{-1} thickness oscillations dominate the spectrum.

If FTIR measurements are to differentiate between different layers, there has to be sufficient contrast between their optical properties. Often this contrast stems from a difference in doping – according to the Drude model, a layer's absorption coefficient changes linearly with free-carrier concentration.



Statistic	Thickness (µm)		
	Epi	Buffer	Total
Minimum	1.7342	0.4093	2.1451
Maximum	1.7358	0.4119	2.1462
Range	0.0016	0.0026	0.0010
Average	1.7346	0.4109	2.1457
Standard Deviation	0.0004	0.0006	0.0003
Standard Deviation Uniformity	0.0252%	0.1546%	0.0133%

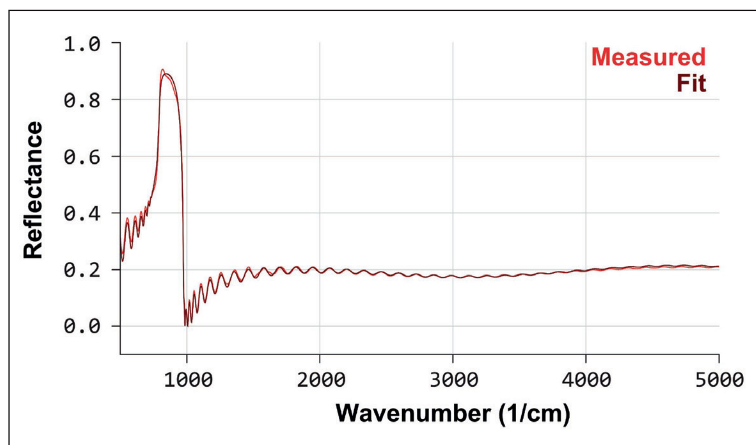
➤ Figure 6. (a) Fit of a thin epiwafer's reflectance spectrum. The measured spectrum is shown in light red, the fitted spectrum in dark red. The goodness of fit is R^2=0.9995. (b) Statistics of a 15-fold centre repeat measurement. Wafer maps with (c) total, (d) epi, and (e) buffer thickness obtained by optical modelling.

However, contrast can also come from partial amorphization of a layer, originating from ion implantation. Depending on the sample's optical characteristics, optical modelling can extract multiple layer thicknesses, such as those of the buffer and multiple epilayers, as well as higher dopant concentrations from the reflectance spectrum.

Another strength of optical modelling is that, unlike the other two methods outlined, this technique can accurately measure layers as thin as a few hundred nanometres. Care is needed, however, since in a simultaneous fit of multiple parameters correlation may appear between them, so models must be validated with repeatability and map measurements.

To illustrate the capability of optical modelling, let us take a look at results obtained with a typical SiC epi structure (see Figure 5 for the structure, and Figure 6 for: (a), the reflectance spectrum's fit; (b), the statistics of a centre repeat measurement; and (c), thickness maps). For this thin two-layered sample, optical modelling provides the only way to accurately determine the thickness of both the layers.

Due to ion implantation inducing partial amorphization, results of optical modelling that draw on FTIR measurements can uncover the depth of these implants. This is illustrated in Figure 7, which shows the reflectance spectrum of an ion-implanted epi structure. The spectrum contains low-frequency oscillations associated with the amorphous layer on the sample surface, as well as high-frequency oscillations, stemming from the epilayer.



➤ Figure 7. Optical modelling of an ion-implanted epiwafer. The thickness of the top layer is 0.6095 µm, and the goodness of fit, R^2, is 0.9969.

Semilab's new FTIR metrology system

To ensure effective SiC device manufacturing, there is a need for accurate metrology, supported by

seamless in-line integration features. Offering all this and more is our EIR-2300. This tool, designed for fully automated SiC fabs, has the smallest possible footprint, allowing back-to-back or to-the-wall placement. Configured with a mini environment and a faster robot for higher troughput, it has verstile loapdort and automation configuration, including standard mechanical interface (SMIF) or open cassette loadports, and overhead hoist transfer (OHT) or automated guided vehicle (AGV) compability. The EIR-2201 and EIR-2202 are economical alternatives with manual loadports and an AGV option, or a SMIF loadport with an OHT or an AGV option.

Note that all these tools are shipped with a new second-generation metrology head, offering increased throughput, longer lifetime, and long-term stability. There are also advanced software features, including wafer sorting, a report for tool status and performance checks, and improved analysis for SiC interferograms. The EIR tools can also provide additional information – as well as being used for SiC measurements of epitaxial layer and buffer thickness, multilayer analysis, and higher dopant concentrations, they can determine epilayer thickness and provide transition-zone measurements in silicon structures, offer dielectric composition analysis, and uncover contaminants, such as interstitial oxygen, substitutional carbon, and hydrogen levels in SiN.

In short, our second-generation EIR systems provide increased accuracy, efficiency, and uptime to the semiconductor industry for a wide variety of applications. Featuring versatile configuration options, these tools can integrate into existing facilities and new fabs, while supporting the latest standards.

FURTHER READING / REFERENCE

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- P. Gammon “Taking Stock of SiC, Part 1: a review of SiC cost competitiveness and a roadmap to lower costs” PGC SiC Blog (2021)
- E. Najbauer *et al.* “Comprehensive optical metrologies of implanted SiC wafers” International Conference on Silicon Carbide and Related Materials (ICSCRM) (2023)
- EV fuel efficiency advantages over conventional vehicles: www.fueleconomy.gov/feg/evtech.shtml

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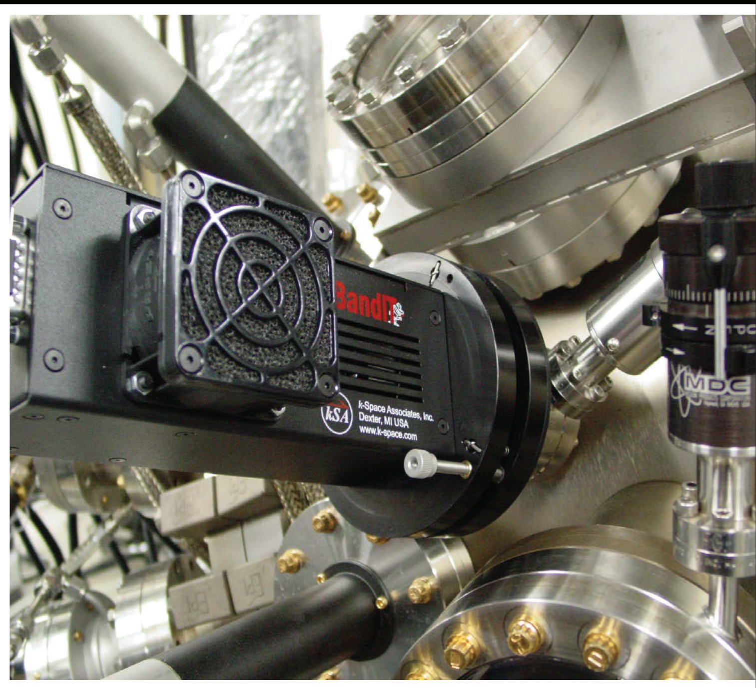


Left: As well as presentations on VCSELs, delegates at CS International were informed of some of the latest developments in superluminescent LEDs, microLEDs, multi-junction solar cells, GaN RF devices, and GaN and SiC power devices.

New vectors for the VCSEL

The VCSEL is assured of a promising future, with growth in established markets to continue alongside success in new applications

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

WHAT'S THE DREAM of every chipmaker? It surely focuses around winning sales in growing, established markets. However, as any particular market may raise and fall, device makers will ideally increase revenue in large and existing markets while pursuing lucrative opportunities in new applications.

Based on a handful of presentations at this year's CS International, held in Brussels on 16-17 April, this envious state-of-affairs is being enjoyed by makers of the VCSEL. According to Ali Jaffal, Technology & Market Analyst at Yole Group, established markets related to datacomms and smartphones will continue to grow over the coming years, during which time sales will increase in other areas. New opportunities for the VCSEL exist at slightly longer wavelengths that are approaching the 'eye-safe' domain, a topic outlined by Julien Boucart, Senior Director Product Management at Coherent, and there are plans to deploy VCSELs to significantly cut the energy associated with the production of batteries for electric vehicles (EVs), an idea championed by Roman Koerner, CTO of Trumpf Photonic Components.

As well as looking at what lies ahead, Jaffal provided some history of the commercial success of the VCSEL. He pointed out that communication applications provided the main driver for this surface emitter from its commercial launch in the mid 1990s until 2017, when Apple started to use this class of laser for face identification and proximity sensing. Strong uptake of this consumer application fuelled a hike in demand for the VCSEL, with production migrating from 100 mm to 150 mm GaAs-based wafers. Jaffal added: "For those of you wondering about 8-inch GaAs diameters, that's basically for microLEDs."

Yole is forecasting growth in established markets, along with many others. The lion's share of sales will come from the mobile and consumer sector, which will grow at a modest rate from 2022 to 2028, increasing from \$798 million to \$974 million. Over that timeframe the second biggest market, telecom and infrastructure, will expand from \$126 million to \$232 million. The only other significant markets are automotive and mobility, rocketing from \$4 million to \$108 million from 2022 to 2028, and the industrial

sector, increasing in value from $44 million to $78 million over that timeframe.

The small growth in the mobile and consumer sector between 2022 and 2028 results from decisions by Apple, the leading consumer of these sources on this sector. Other OEMs, such as Huawei and Honor, have much lower shares and volumes. Ali adds "We are not witnessing major VCSEL adoption from the Android camp in smartphones".

The GaAs VCSEL is located in the notch of the smartphone – that's the small, non-display area located at the top of the device.

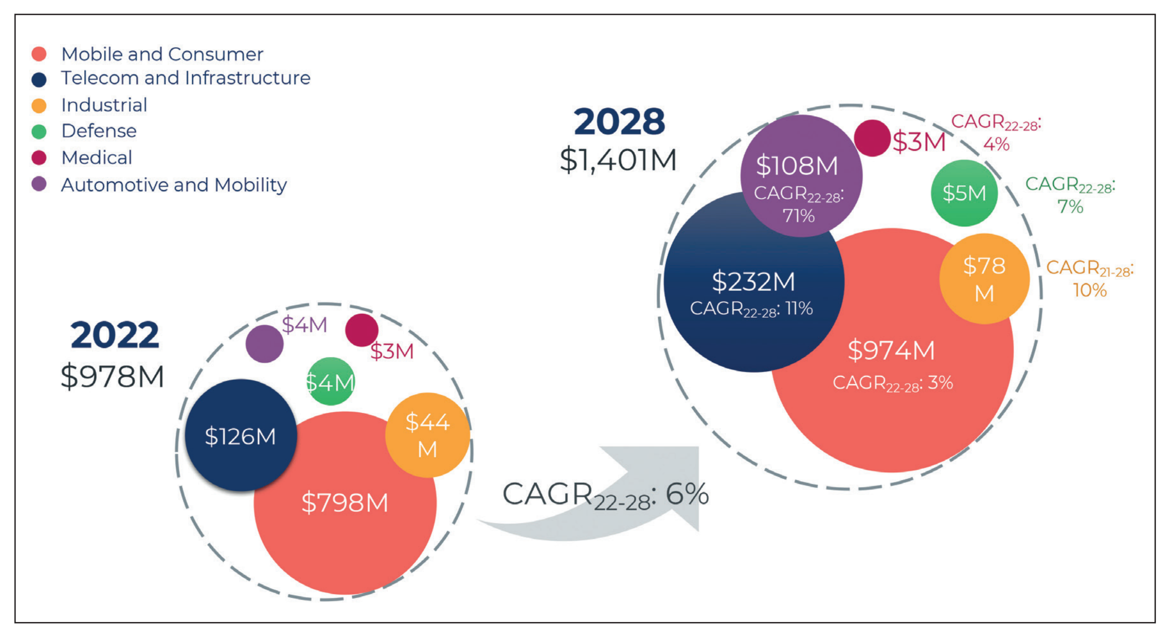
"We know that the trend is to make this notch smaller," remarked Jaffal, who questioned whether there will come a time when it is removed altogether. He explained that in 2022, the notch decreased in length to 21 mm in iPhone Pro models, a move that involved the introduction of InP edge-emitting lasers for the launch of the 14 Pro. As InP lasers operate at longer wavelengths than GaAs-based VCSELs, these edge-emitters could be incorporated behind the screen. But for all the 15 models, while the size of the notch has remained, the GaAs VCSEL has returned, with all the facial recognition optoelectronics miniaturised and incorporated within this space.

In the Yole presentation, Jaffal offered a number of explanations for this move by Apple. He pointed out that the supply chain for InP edge-emitters is not as established as it is for GaAs VCSELs, and the cost of the full modules is more expensive. In addition, it is more challenging to incorporate an InP laser beneath the display, than to place a VCSEL within the notch.

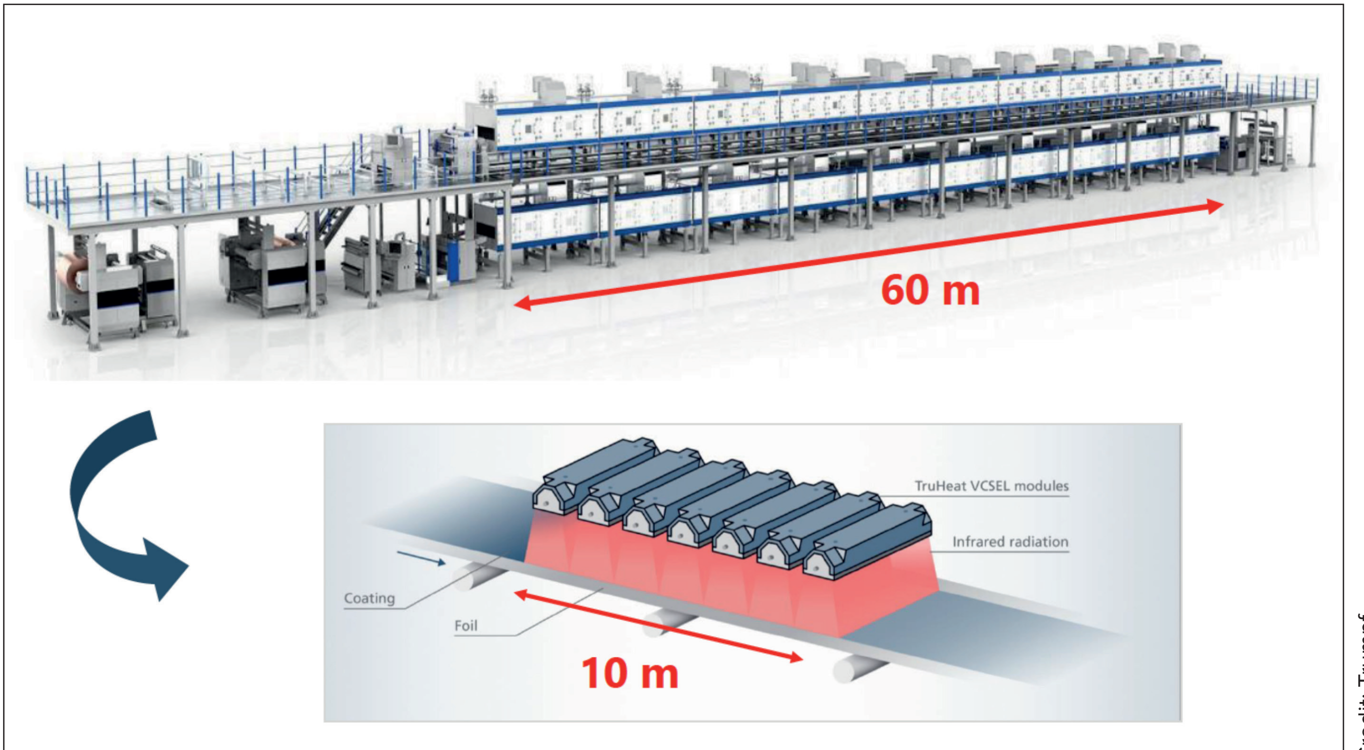
New generations of iPhone have also involved changes to the VCSEL-based lidar technology that's on this smartphone's rear side. For the family of iPhones spanning the 12 to 14 models, wire bonds connect this laser to the drive electronics. But these wires have been eliminated in the iPhone 15, thanks to the introduction of a flip-chip technology featuring a back-side emitting VCSEL.

All this increased functionality is realised while trimming costs, with the bill of materials falling by 36 percent, according to Jaffal. "Part of it comes from the VCSEL, but also big part of it comes from the image sensor."

➤ Apple has devoted much effort to reducing the size of the notch in the iPhone, as can be seen by comparing Pro Max models of the 13 and 14. For the 14, Apple moved away from the GaAs-based VCSEL to the edge-emitting InP laser. But for the 15, with an even smaller notch, it has reverted to using the GaAs-based VCSEL.



➤ Yole Group's 2022-2028 VCSEL market forecast. Source: *VCSEL report*, Yole Intelligence, 2023.



Credit: Trumpf

➤ As well reducing the energy required to produce batteries for EVs, VCSEL-based heating trim the space that is required to carry out this task.

For the second biggest market, telecom and infrastructure, 850 nm VCSELs are used for datacoms over multi-mode fibre, both within racks and between them, with the devices supporting optical links of up to 100 m. Today, VCSELs are being deployed in 800G optical transceivers, with eight devices operating at 100G. Sales are driven mainly by AI applications. In future, datacomms will employ transceivers operating at 1.6T, using eight VCSELs operating at 200G. Such sources are being developed by the leading players, with Coherent already having reported results.

Yole Group is forecasting that the total shipment of VCSELs to the datacom market will increase at a compound annual growth rate of around 14 percent between 2023 and 2029. The majority of the production will continue to focus on 100 mm GaAs substrates, thanks to high yields and small device sizes realised with this format.

Jaffal also spoke about the market where Yole is predicting the biggest compound annual growth rate for the VCSEL: automotive lidar. This expansion is driven by Chinese OEMs using Hesai's AT128 lidar, featuring multi-junction GaAs VCSELs. Back in 2018, automobiles fitted with this technology tended to feature a single, forward-facing long-range lidar. By 2028, cars could be equipped with the combination of long-range lidar for front and rear, and short range-variants for left and right; and early into the next decade, they may incorporate as many as six units. Lidar might also be deployed inside the car, to monitor the driver and/or the passengers.

There are a number of options for the light source for lidar. For 2023, Yole has estimated that edge-emitters lasers occupied the largest share of the market, accounting for 45 percent, followed by VCSELs with 39 percent and fibre-lasers with 16 percent. Fast forward to 2033 and Yole forecasts that VCSELs will have crept ahead of edge-emitters, with 45 percent compared to 43 percent, while the share for the fibre laser will have fallen to 12 percent, due to its high cost and bulkiness.

Longer-wavelength opportunities

One of the biggest names in GaAs-based VCSELs is Coherent. It has now shipped more than 200 billion of them, according to Boucart, who pointed that the company's roots in this technology date back to the 1990s. He explained that one of the commercial pioneers, Honeywell, is now part of Coherent via acquisitions by Finisar and then II-VI; and another trailblazer, Avalon Photonics, came into the company's fold via Bookham, Oclaro and II-VI.

Boucart remarked that today the primary emission wavelengths for VCSEL products are 850 nm, for use in data communication, and 940 nm, for consumer applications. One of the major benefits of having a 940 nm source is that it operates within a spectral window where sunlight is filtered by the atmosphere. Due to the reduction in the strength of sunlight around 940 nm, low-cost silicon sensors can be used to detect signals produced by the VCSEL.

Engineers at Coherent are now starting to develop VCSELs at longer wavelengths, which overlap other spectral windows where the atmosphere filters sunlight. Moving to longer wavelengths can open up new applications, some of which may invoke concerns over eye-safety that are reduce by heading further into the infrared.

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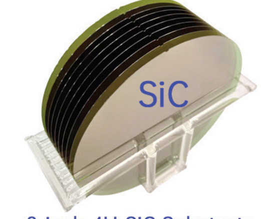

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8-inch 4H-SiC Ingot

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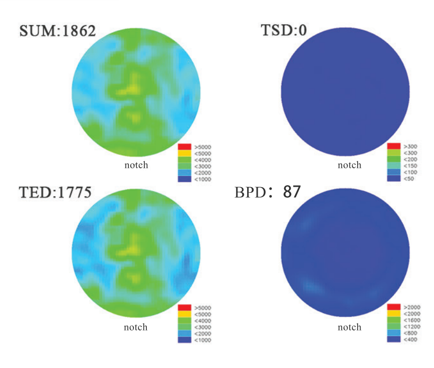

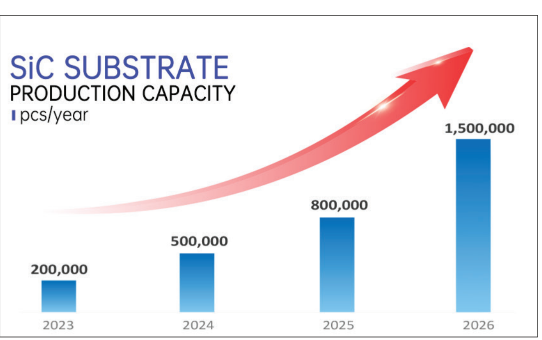

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One longer-wavelength VCSEL that Boucart discussed is a 1130 nm emitter, produced on the company's high-volume 150 mm line. This laser's output power peaks at about 4 mW, and it has a power-conversion efficiency that can exceed 25 percent. Reliability is impressive, with a time to 1 percent failure of 1 million hours at a junction temperature of 70°C.

To stabilise the polarisation of the emission, a grating has been integrated into these devices.

A noteworthy attribute of these lasers is their very high current densities, suitable for lidar. Using short pulses, current densities can reach up to 150 kA cm^{-2}, while realising polarisation extinction ratios exceeding 10 dB.

Engineers at Coherent have also produced VCSELs at 1380 nm, by combining expertise in GaAs and InP. Emission at this eye-safe wavelength can be used to measure water absorption. Operating at 25°C, these VCSELs produce up to 2.9 mW of power, and have a peak power-conversion-efficiency of 10 percent.

Better battery production

A promising option to help curb climate change is to increase the uptake of EVs. Going hand-in-hand with this, efforts must be directed at minimising the energy required to produce this form of transportation, as this will improve the environmental benefits of this vehicle.

Batteries are a key component in EVs, and producing them requires substantial energy. For every kWhr of battery, its production requires 30-55 kWhr, and in an EV with long-range capability the energy stored by the battery system can total 100 kWhr.

Analysis of the battery production process shows that almost half of the energy that's consumed is used to power ovens. Heating drives the drying of a thick, wet slurry to create a lithium-containing coating on the thin metal foils that form electrodes in the batteries.

Koerner explained that while the convection-based oven drying process is simple, it has many weaknesses. Efficiency is just 10-20 percent, regulation and flexibility is limited, and the process takes up a lot of space, with ovens accounting for a 60 m-long section in a EV battery factory.

To address these concerns, Koerner and his co-workers are championing a switch to VCSEL-based drying. This move could deliver a hike in efficiency to more than 40 percent, increase flexibility, enable precise regulation, and slash the space required for heating, with a 10 m-long section of the factory adequate for this purpose. The VCSEL-based approach does have a downside, as it increases complexity, but only to what Koerner describes as "moderate", as no optics are needed.

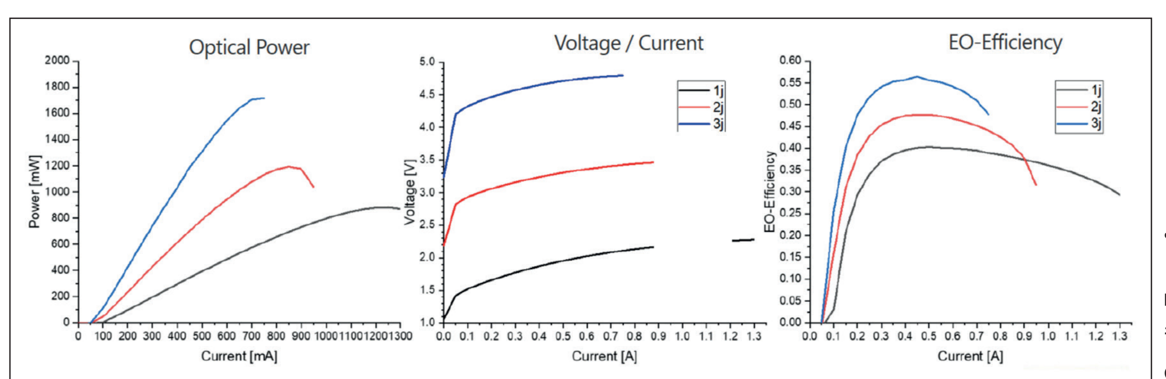
Heating would be provided by modules around 1 m by 1 m in size, populated by VCSELs with multiple junctions, to increase the output power of these emitters. As the working distance between the VCSELs and the foil is relatively short, there is no need for any optics.

"We can use a wavelength around 980 nanometres, which is quite efficient," said Koerner, who added: "It's perfectly absorbed by the metal foil." He explained that the maximum power density for the heating process is limited by the foil, which must not melt.

Koerner described experiments to verify the approach, with an array of 50 million VCSELs positioned between 150 mm and 300 mm above a moving foil. These VCSELs, with a total output power of 5.4 kW, projected light over a 16.5 cm by 15 cm area, applying a power density to the foil of up to 8 W cm^{-2}. This investigation determined good drying at 8 W cm^{-2}, using an exposure time of 9 s and a belt speed of 1 m/minute. In production, there's a need for a 60 m/minute belt speed, implying an exposure length of 9 m.

Simulations of the intensity profile produced by the 5.4 kW module, and not involving any optics, have been produced by engineers at Trumpf.

"The centre is very homogeneously illuminated, with an average light intensity of around 2.5 watts per square centimetre," said Koerner, who pointed out that higher intensities were possible, with considerations governed by how much energy the foil can absorb.



➤ Adding junctions to Trumpf's VCSELs boosts output power and efficiency.

Credit: Trumpf

The homogeneity of the optical power produced by the module is ± 2 percent. "That's very hard to achieve with other systems like fibre lasers," remarked Koerner, who claimed that there are no dark spots in the intensity profile.

Using vast arrays of VCSELs to make modules for heating offers tremendous flexibility. The intensity of heating is easy to adjust, enabling pre-heating of the foil, followed by full heating at a later stage. And if a particular module is not providing enough power, it's relatively easy to replace it with another.

Like many other VCSEL producers, Trumpf can increase the power produced by its VCSELs by adding more junctions, with electrons cascading through the device. For the heating of foils in an EV battery production plant, VCSELs could be operated in continuous wave, using relative low current densities and an efficiency close to its peak value.

Koerner shared a comparison of the performance of VCSELs with a single junction and a triple junction. Increasing the number of junctions boosted the power-conversion efficiency from 49 percent to 62.5 percent.

"The downside is a higher voltage, which is sometimes a problem for consumer applications," said Koerner, before adding that this is not a concern for industrial usage.

Comparisons have been made of the power and efficiency of arrays of 99 VCSELs, with either a single junction, two junctions or three junctions. Adding junctions increases both the total optical power and the electro-optical efficiency, with the peak of the later increasing from around 40 percent to 55 percent when moving from a single junction to a triple junction.

Koerner and his co-workers have also evaluated the reliability of their VCSEL-based heating modules. When delivering a total output power of around 4.3 kW, power drift is below 0.04 percent.

Accelerated lifetime tests have also produced very encouraging results, with VCSELs with a triple junction held at 145°C running for more than 8,000 hours before their output power falls by 20 percent. For a junction temperature of 70°C, and a maximum drive current of 7 mA, the mean-time-to-failure is more than 12 years.

Trumpf is planning to launch its laser-based heating modules to market in early 2025. This compelling product should increase the number of applications where the VCSEL can serve, and strengthen sales for the makers of this device.

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Silicon's positive influence

While most players in the CS industry are suffering from significant falls in their share prices over the last 12 months, a few companies have risen in valuation, in one case due to opportunities within the silicon industry

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WHEN GLANCING at this year's compound semiconductor share price leaderboard, please heed the following advice: Don't judge a book by its cover. By taking note of this English idiom you can avoid making an incorrect assumption as to why Veeco is at the top of the table, with a share price that has soared by more than 80 percent over the last 12 months.

I give this warning because it is tempting to think that Veeco, a well-known and significant supplier of epitaxial growth equipment, has grabbed top spot by increasing its market share in MOCVD tools, MBE tools, or possibly both. However, this part of its business, which not long ago provided a very considerable proportion of its sales, has actually suffered a small fall in revenue. The reason for the rocketing valuation of Veeco is ramping sales of equipment to the silicon industry, which accounts for the lion's share of its revenue.

Commenting on this success in an earnings call on 14 February, 2024, to discuss results for the most recent fiscal year, Veeco's CEO, Bill Miller, remarked: "Revenue from our semiconductor business reached a record in 2023, outperforming wafer fab equipment growth for the third consecutive year. Our strong results included multiple laser-annealing systems for advanced DRAM devices, despite industry-wide 'capex' reductions, as well as our first high-volume manufacturing laser-annealing systems to our third leading Logic customer."

Veeco's sales to the silicon industry are dominating its revenue, and brought in $413 million in fiscal 2023, which ending on 31 December last year.

Sales from this part of the business have climbed 12 percent year-over-year to now account for 62 percent of total revenue. On these sales, totalling $666 million and up 3 percent year-over-year, Veeco had a gross margin of 43.5 percent, and realised a profit of $98 million.

Meanwhile, compound semiconductor revenue for fiscal 2023 declined to $87 million, contributing just 13 percent of total revenue. According to company CFO, John Kiernan, this decline is due to a fall in wet processing systems for 5G RF devices, resulting from softness in the handset market.

Veeco also generates revenue in other markets. Data storage contributed $88 million in fiscal 2023, over which time the company generated $78 million from what is described as scientific and other revenue.

During the February earnings call, Miller championed two strategic milestones. "First, we launched our next-generation nanosecond annealing solution. And second, we launched our ion-beam deposition system for low-resistance metals." Both technologies are claimed to support the production of devices with a higher performance and a lower power consumption.

"Our nanosecond annealing technology offers a substantial opportunity to expand our served available market to a broad range of new advanced node applications," remarked Miller. "Due to our unique laser and architecture, our system can achieve a lower thermal budget and a shorter dwell time versus today's most advanced annealing solutions."

This tool produces a shallow anneal, impacting just tens to hundreds of nanometres into the wafer. It is argued that this attribute could be ideal for backside power delivery, and contact anneal for advanced nodes and three-dimensional devices.

"Our system has the capability to change the structure and properties of the device, enabling steps like void removal, re-crystallization, and grain growth," informed Miller, who pointed out that Veeco shipped its first two nanosecond annealing evaluation systems to two leading logic customers at the end of last year. The company is anticipating initial high-volume manufacturing orders in 2025.

The other tool that Miller has high hopes for, the new ion-beam deposition system, could see deployment in 300 mm fabs. He argued that as device geometries shrink, lower resistance materials are needed to maintain performance, a goal that is difficult to meet with traditional deposition technologies, such as PVD.

According to Miller, results from its tier-one customers have determined that compared with traditional PVD, films of tungsten and ruthenium have a resistance that's around 20 percent lower.

"For DRAM, this enables tungsten bit-line scaling while maintaining electrical performance of the device," said Miller. He pointed out that for those working on logic, ruthenium-based metallization can enable new integration schemes at future nodes.

In the last quarter of 2023, Veeco shipped its first two IBD300 evaluation systems to DRAM customers. "As we look ahead, we see potential for initial high-volume manufacturing orders in 2025," added Miller.

He is also upbeat regarding long-term opportunities for the company in the compound semiconductor sector, viewing 2024 as one for evaluations. This year the company anticipates that customers will be evaluating two SiC systems, as well as a 300 mm GaN-on-silicon system, plus another for making microLEDs.

Veeco is anticipating an increase in sales for fiscal 2024. Revenue is forecast to be between $680 million and $740 million.

Riber's ramping revenue

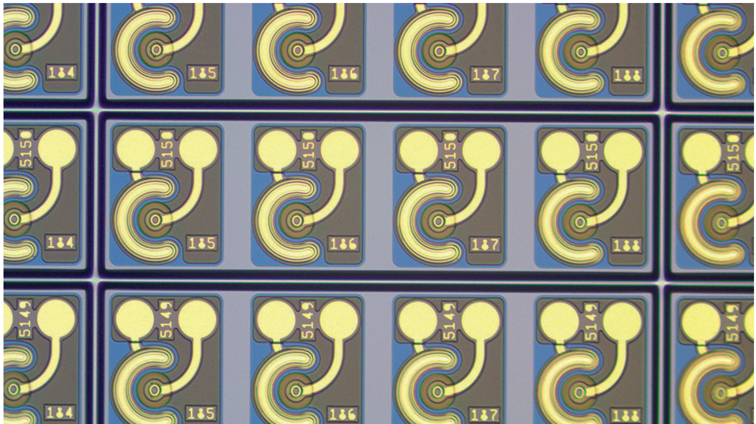
In second place on this year's leaderboard is Riber, the French manufacturer of MBE tools. The rise in

***Compound Semiconductor* Shareprice Leaderboard**

Rank	Company	Ticker	Share value, April 27, 2023 ($)	Share value, April 26, 2024 ($)	% appreciation	Change in Rank
1	Veeco	VECO	18.55	34.28	84.8	7
2	Riber (Paris)	RIB	1.85*	3.08*	66.5	+1
3	Coherent	COHR	33.64	53.13	57.9	+8
4	NASDAQ composite	IXIC	11913.00	15821.34	32.8	0
5	Qorvo	QRVO	90.34	114.70	27.0	+2
6	IQE (London)	IQE	0.320*	0.337*	5.3	0
7	Skyworks	SWKS	102.18	102.70	0.5	-2
8	AXT	AXTI	3.20	2.90	-9.4	+6
9	Lumentum	LITE	47.56	42.16	-11.4	+3
10	Aixtron (Frankfurt)	AIX	28.10*	24.60*	-12.5	-8
11	Infinera	INFN	6.20	4.98	-19.7	-1
12	IPG Photonics	IPGP	110.98	88.24	-20.5	-11
13	WIN Semiconductor (Taipei)	3015.TWO	4.91*	4.41*	-22.3	-4
14	Wolfspeed	WOLF	56.60	24.85	-56.1	-2
15	ams OSRAM	AMS.SW	3.48*	1.12*	-67.8	0

* Converted to dollars using the exchange rates on 26 April of 1 EURO = 1.0687 USD, 1 GBP = 1.2472 USD. 1 CHF = 1.0938 and 1 TWD = 0.03066

➤ Over the last 12 months many companies in the compound semiconductor industry have seen a fall in their share price.



Released in February 2023, sales of Coherent's 100G VCSELs are growing fast, with revenue already at $100 million per quarter.

its share price can be attributed to increases in both its global sales of MBE tools, and its share of this market.

Riber reported results for the first fiscal quarter on 26 April. Sales totalled €4.5 million, up 20 percent over the equivalent quarter of the previous year.

The company, which is celebrating its fiftieth anniversary this year, has a growing order book. At the end of March this totalled €34.4 million. Orders for 10 machines, including 7 production machines, accounted for €27.9 million, with the remaining €6.5 million associated with service and accessories.

Riber does not discuss results in quarterly earnings calls, so less insight is provided into the drivers behind the company's financial position and its prospects. However, when reporting the latest results, Riber revealed it expects further growth in revenue and earnings for 2024.

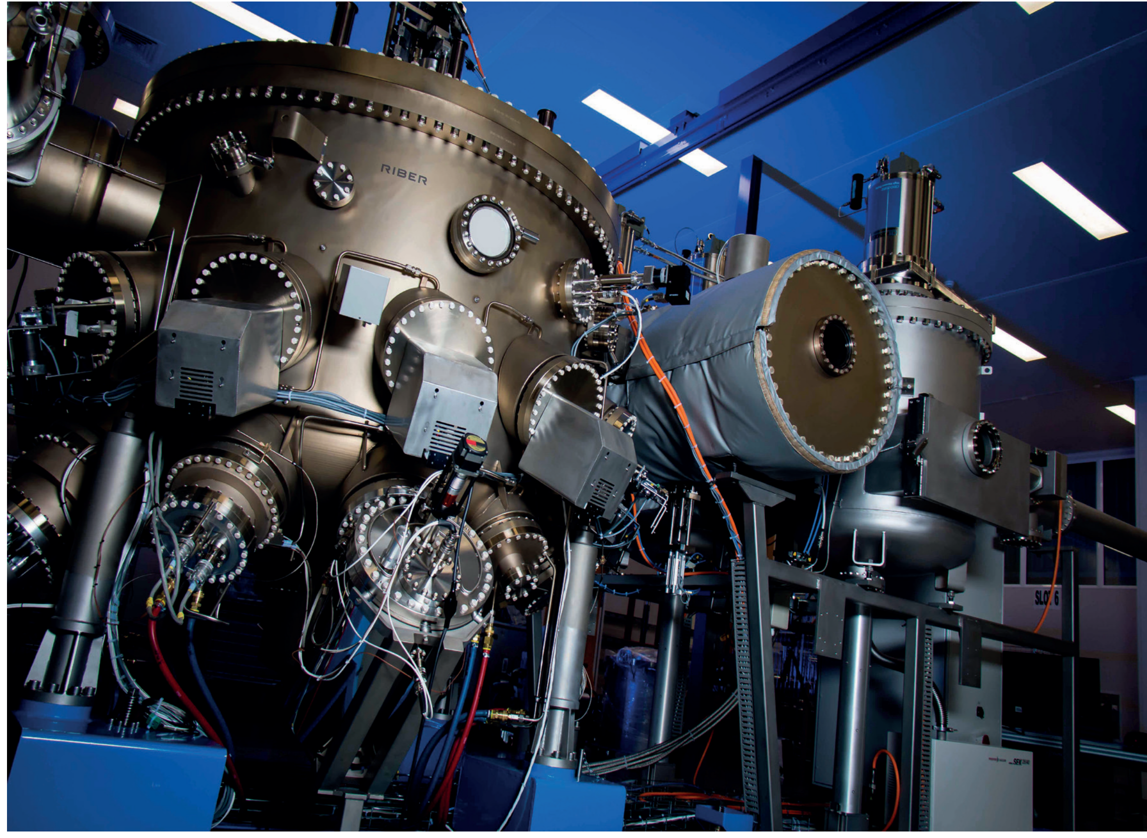
Coherent benefits from AI

Third on this year's leaderboard is Coherent, a company that combines activities in the compound semiconductor sector with a number of other ventures, particularly related to optics.

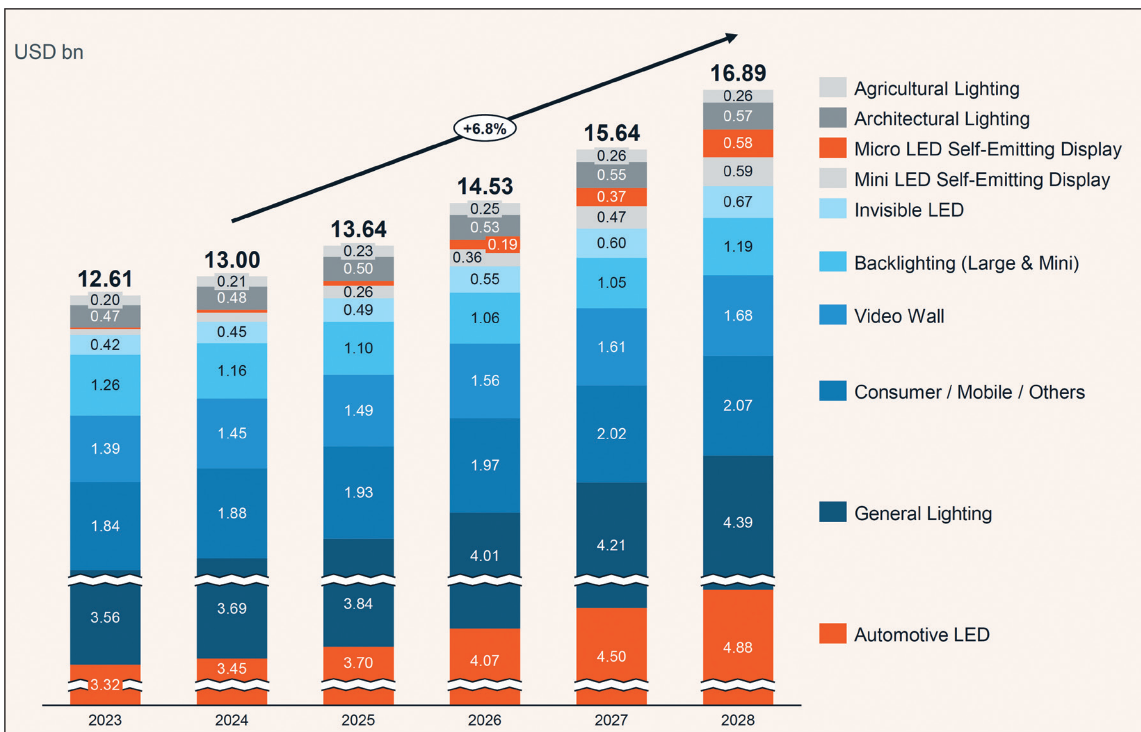
This February, in a letter to shareholders that coincided with the release of results for the second fiscal quarter, Coherent identified five recent highlights: improving margins; increasing its position in the AI-driven datacom market; improving its ramp for its 800G datacom transceivers; increasing demand in telecom and communications markets; and closing SiC transactions with Mitsubishi Electric and Denso, an activity that lays the foundation for a new business.

The later involves a total investment of $1 billion, with 75 percent from Coherent and 12.5 percent from Mitsubishi Electric and from Denso. For the two smaller investors, the new venture will support their demands for SiC substrates and epiwafers.

Commenting on this venture on 6 February, 2024, during an earnings call to discuss results for the



A significant proportion of Riber's revenue is coming from the sale of its production tools. The company continues to expand this portfolio, with the recent addition of the MBE 8000, developed in collaboration with US epiwafer provider Intellepi and targeting the growth of VCSEL epiwafers.



➤ Figure 1. The automotive industry is now the most significant market for the LED. Source: TrendForce LED Industry Demand and Supply Database 1Q24

second fiscal quarter, Sohail Khan, Executive Vice President Silicon Carbide LLC, the newly created subsidiary for the SiC business, remarked: “We are quite bullish about the silicon carbide market and the growth prospects over the next five to ten years. The announcement with Mitsubishi and Denso has strengthened our position, and we are seeing more engagements, and especially a lot of interest, from both existing and new customers for 200 millimetre [material]”.

Due to these encouraging prospects, the plan to invest and expand proceeds. “We will continue to see the growth of our business quarter-over-quarter and year-over-year.”

While this divesture is an important element of Coherent’s future, its leaders, and the investment community, are more excited by the prospects of the company’s 800 G datacom transceivers. Quarterly revenue for this product portfolio, which only started to ship just over a year ago, has increased sequentially by over 100 percent to cross the $100 million mark, driven by orders related to AI and machine learning. This phenomenal growth is set to continue, with Coherent forecasting that the market will expand at an compound annual growth rate of 65 percent over the next five years, fuelled by AI.

Such strong growth in demand is not always easy to fulfil. However, Coherent is well placed to deal with this, according to Giovanni Barbarossa, the company’s Chief Strategy Officer and President Materials segment. “We are the most vertically integrated player in the space,” argued Barbarossa, who pointed out that concerns within the industry over a VCSEL shortage are not worrying Coherent, because it is the biggest supplier of these devices in the world.

“We think that we will have always the best margin profile, versus those that have to pretty much buy everything on the merchant market,” claimed Barbarossa. He believes that Coherent has the most comprehensive profile of 100G and 200 G devices, which will continue to expand.

Another area where Coherent is active is in the nascent microLED industry. The company has received multiple orders from China, Taiwan and Korea for a laser-based tool that transfers microLEDs from a wafer to a display. These microLEDs can be as small as 10 μm, and in future could be just 5 μm in size.

“We’re seeing increasing customer engagement and are very excited about the impact of microLEDs on the television market,” remarked Chris Dorman, Executive Vice President, Lasers. “This is a very high level of engagement now and a market that will be growing over the next three-to-five years.”

The total revenue from all of Coherent’s activities is on an upward trajectory. For the second fiscal quarter, ending on 31 December, 2023, sales totalled $1.131 billion, above the mid-point of guidance. The company posted a gross margin for those three months of 36 percent, with much effort being devoted to improve this figure, according to the soon-to-retire CEO Mattera.

Commenting on this, Mattera explained that actions have been implemented across virtually all of Coherent’s businesses, in a drive to enhance

operational efficiency. "These actions, along with rigorous cost and expense control across the company, helped drive our sequential improvement in gross and operating margin in the second quarter."

While progress has been made, there's more to do. "We are on a roll, but we're far from done," argued Mattera. "As we continue to transform the company to improve operating performance, we will optimise our production footprint and enhance operating resiliency, while completing the integration of legacy Coherent."

The third fiscal quarter will probably produce an increase in revenue, with guidance in the range $1.12 billion to $1.20 billion. Earnings per share is also likely to increase. For fiscal 2024, the latest revenue guidance is $4.55 billion to $4.70 billion.

Osram: microLED misfortunes

Footing this year's leaderboard is ams Osram. Its opportunities for long-term growth were dealt a hefty blow earlier this year when Apple cut it ties with this chipmaker, which had invested $1 billion in the construction of Kulim 2, the world's first high-volume 200 mm LED fab. This fab had been built to produce microLEDs for Apple products, particularly smartwatches, and the breaking of the deal led to a 40 percent fall in Osram's valuation. Even before then, the share price had been trending downwards, possibly over concerns related to the microLED venture with Apple.

Commenting on the future for the company on 26 April, when Osram released its results for the first fiscal quarter, 2024, CEO Aldo Kamper remarked: "We intend to step out of the 8-inch factory and focus our microLED development on automotive needs."

More than 500 employees in Malaysia and Germany were involved in microLED development. Some have now moved to working on automotive LEDs, which has recently become the largest segment of the LED market, according to the analyst TrendForce (see Figure 1).

One of Osram's priorities is to exit its sale-and-lease-back contract for Kulim 2. If successful, it will reduce the company's long-term debt by €400 million.

Osram has initiated a 're-establish-the-base' programme, designed to deliver cost savings, partly by exiting some non-core semiconductor businesses that provided revenues of between €300 million and €400 million in 2023. The company will focus on its core portfolio in automotive, industrial and medical markets, where it holds strong positions, according to TrendForce. Figures by this market research firm indicate that Osram is: the second biggest LED supplier in the world, behind Nichia; the leader in light sensors, with more than 29 percent of the market; and the leading supplier of traditional automotive lamps and bulbs.

For the first fiscal quarter of 2024, Osram reported revenue of €847 million, and a loss of €35 million. For the next quarter, sales may decline, due to typical seasonality. Revenue is forecast to be in the range €770 million to €870 million.

It will take time for Osram to execute its strategy, revive its fortunes, and drive growth in its share price. If it progresses on these fronts over the next 12 months, it's unlikely that it will foot the table in 2025.

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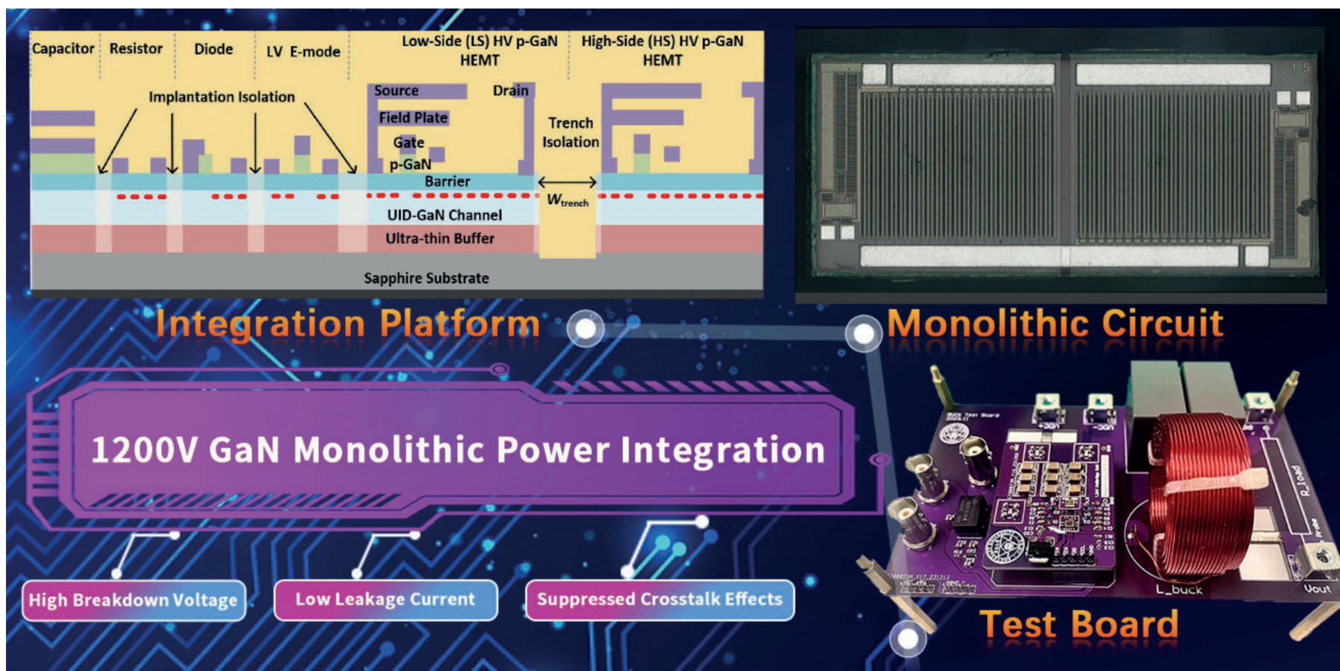


1200 V GaN monolithic power integration

Sapphire substrates with ultra-thin buffer layers provide a foundation for fabricating systems offering 1200 V GaN-based monolithic power integration while supressing crosstalk

BY SHENG LI, SIYANG LIU AND WEIFENG SUN FROM SOUTHEAST UNIVERSITY AND TINGGANG ZHU FROM CORENERGY SEMICONDUCTOR

OUR ELECTRIFIED WORLD contains countless examples of energy conversion. Within this sector the GaN-based power device attracts extensive attention, thanks to its capability to switch high voltages at high speeds. However, there are concern associated with this wide bandgap technology. In power systems featuring GaN, inductive elements generate rings and spikes during switching, ultimately leading to an increase in fault risk.

One increasingly popular way to address this concern is to eliminate the parasitic inductive elements by turning to a monolithically integrated gate driver and half-bridge configuration. However, this approach is compromised, with state-of-art GaN based monolithic integration limited to 650 V. That's far from ideal, given the rapid development of power electronic systems requiring power devices with a rated voltage above 1200 V.

The conventional foundation for GaN power devices is the silicon substrate. While it is low in cost and widely available, it is impaired by a conductivity that is to blame for the vertical breakdown and crosstalk in conventional 650 V GaN-on-silicon platforms. These are significant limitations, hampering efforts to increase the rated voltage of monolithic integration.

Progress demands a more radical approach, such as the one we are taking at Southeast University and CorEnergy Semiconductor. Our partnership is pioneering an ultra-thin buffer technology with shallow trench isolation on a sapphire substrate. Using this approach, we have realised a 1200 V monolithic half-bridge integration platform that supresses crosstalk.

Fabrication of our platform begins by loading sapphire substrates into an MOCVD reactor and depositing a 100 nm-thick undoped ultra-thin buffer, followed by a 300 nm-thick undoped GaN channel layer and a 15 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier layer ((see Figure 1(a)). This epitaxial structure is capped with a 100 nm-thick *p*-GaN cap layer, magnesium doped at a level of 2×10^{19} cm^{-3}.

To produce devices from this epilayer, we define a trench with a dry etching process based on BCl_3/Cl_2 – this follows an implantation process (see Figure 1(b)). We suppress the influence of

sidewall traps along the trench by surrounding it with an implantation area. Our other fabrication processes are consistent with those of a normal *p*-GaN HEMT (see Figure 1(c) for an overview of our key fabrication processes).

Our ultra-thin buffer technology allows us to realise wafer-level integration of high-voltage (HV) and low-voltage (LV) enhancement-mode *p*-GaN gate HEMTs with LV passive elements, including diodes, resistors, and capacitors. Undertaking shallow trench isolation by etching the ultra-thin buffer is a relatively easy process, which supresses crosstalk between high-side and low-side HV *p*-GaN HEMTs. Following etching, we fabricate our monolithic half-bridge circuits with gate buffers (see Figure 1(d)). The formation of our integration platform is relatively quick and material costs are low, making this an attractive technology for mass production.

Ultra-thin buffers

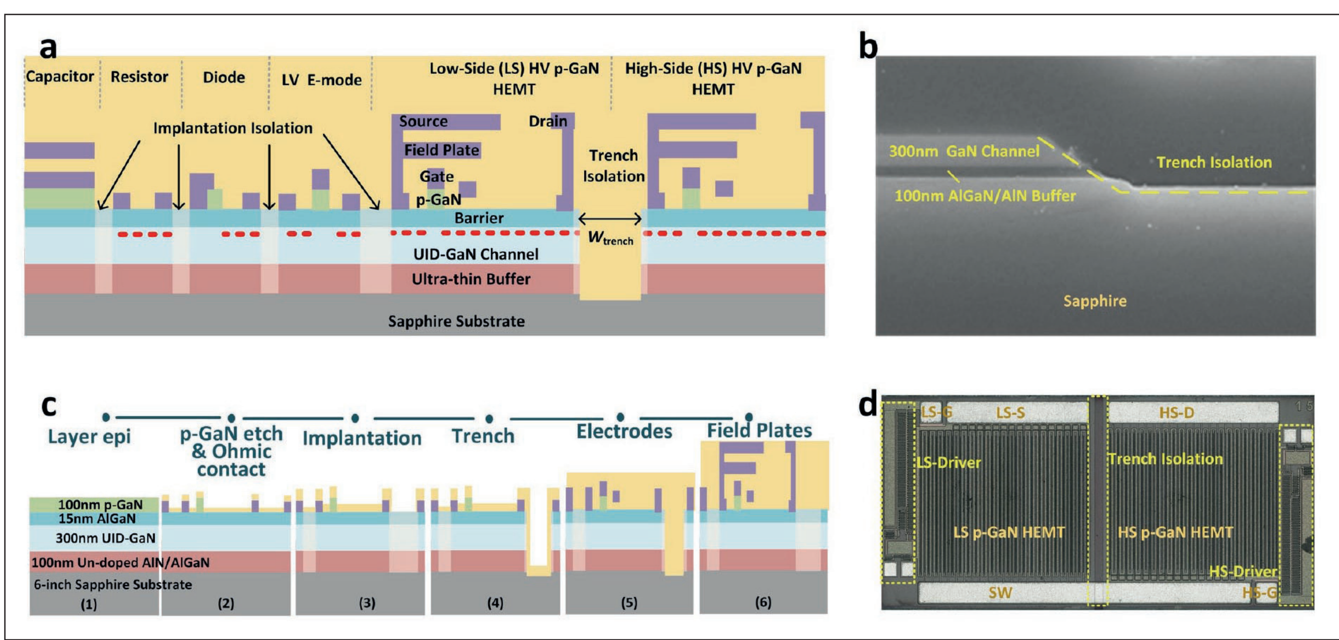
It is essential to eliminate the traps caused by heteroepitaxy, as they threaten to impair mobility in the GaN channel. With conventional GaN-on-silicon HEMTs, traps are typically suppressed by combining a nucleation layer with a thick buffer layer. Switching to a sapphire substrate reduces lattice mismatch with the GaN-based epilayers and enables a 100 nm-thick undoped ultra-thin buffer layer to suppress traps from the substrate and ensure a high-quality GaN channel.

Additional attractive features of our architecture are that it provides a low lateral leakage current and a high lateral breakdown voltage, thanks to the ease of depletion of the thin buffer and the channel under the gate region. What's more, due to the isolated sapphire substrate, the vertical blocking voltage can be increased without needing a thick buffer.

Electrical measurements underscore the superior blocking characteristics of our HV *p*-GaN HEMTs, which benefit from an ultra-thin buffer. We have realised a blocking voltage of more than 1400 V for a gate-to-drain length of just 10 µm in our *p*-GaN HEMT (see Figure 2(a) and 2(b)). This equates to 140 V/µm, which is 140 percent of that of a SOI-based *p*-GaN HEMT. To ensure a healthy safety margin, for devices rated at 1200 V we propose a gate-to-drain length of 22 µm – this geometry offers a blocking voltage of over 2300 V.

Other encouraging results from our HV *p*-GaN HEMT include its capability to withstand transient voltages higher than 1400 V for 10 ms, an attribute that helps improve reliability when an overvoltage event occurs. At a drain-source voltage of 1200 V, the drain leakage current is less than 100 pA/mm and 100 nA/mm at 25 °C and 175 °C, respectively. That's a leakage current level about two orders of magnitude smaller than that for GaN-on-silicon HEMTs. For those devices, the leakage current at high voltages rapidly increases with drain voltage, due to parasitic channels and vertical leakage caused by the conductive substrate. Our devices offer an extremely low drain leakage current, due to the isolated substrate and the undoped ultra-thin buffer, and they benefit from successful suppression of the parasitic channel at the interface between the epitaxial layers and the substrate.

We have also evaluated the dynamic electrical performance of our HV *p*-GaN HEMT (see Figure 2(c)-(e)). At high temperatures there is variation in terminal capacitances, but the influence on switching speed can be neglected, according to double pulse test results. Values for the turn-on delay time and rise time indicate fast switching



➤ Figure 1. (a) 1200 V E-mode GaN based monolithic half-bridge integration platform on sapphire. (b) Photos of trench isolation. (c) Key fabrication processes. (d) Scanning electron microscopy of 1200 V GaN-HEMT monolithic half-bridge integration.

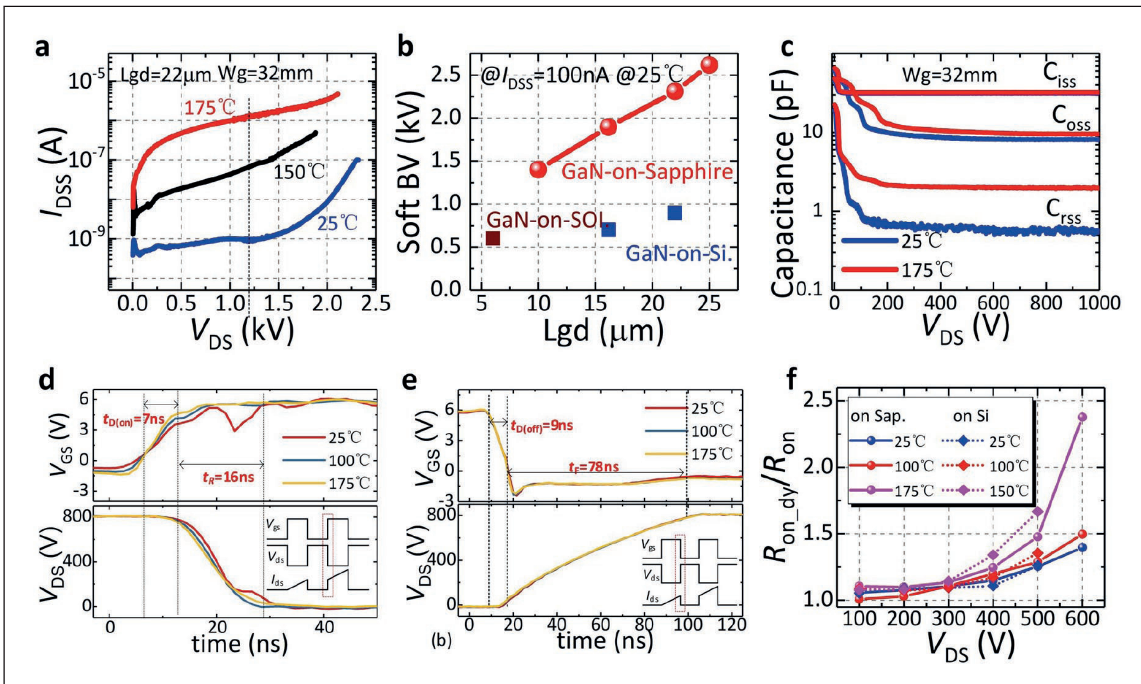


Figure 2. (a) Blocking characteristics of a HV *p*-GaN HEMT. (b) Extracted blocking voltage with different gate-to-drain lengths (L_{gd}). (c) Terminal capacitances at different temperatures. (d) Double pulse test switching characteristics of the turn-on process. (e) Double pulse test switching characteristics of the turn-off process. (f) Comparisons of the dynamic on-resistance between GaN-on-sapphire and GaN-on-silicon HEMTs.

speeds, even at 800 V. The turn-off delay and fall times are longer than they might be, due to a large external turn-off resistance of 30 Ω and a small switching current 1.5 A.

A big concern for all power GaN HEMTs is the dynamic on-state resistance, with higher values increasing conduction loss and junction temperature. We have used a test circuit to provide a highly accurate comparison of the dynamic on-state resistance of conventional GaN-on-silicon HEMTs and our HV *p*-GaN HEMTs. This investigation revealed that our devices have the upper hand in this regard, thanks to a reduction in the general trap activation energy, resulting from the undoped ultra-thin buffer technology (see Figure 2 (f)).

Trench isolation

The monolithic integration of GaN power systems on a single chip has much appeal. There is the promise of suppressed parasitic inductance, reduced die size and greater design flexibility.

However, it's far from easy to fulfil this dream with GaN-on-silicon, due to the common conductive silicon substrate. There are reports that when the high side (HS) transistor and low side (LS) transistor are built on this conventional platform, the system suffers from back-gating and crosstalk effects, coupled through the common silicon substrate.

A number of substrate technologies have been proposed to address this issue, such as Qromis' engineered platform, as well as silicon-on-insulator substrates and engineered bulk silicon substrates. However, for all these platforms the rated voltage is restricted to no more than 650 V, due to vertical breakdown. With all these platforms, it may be tempting to try and increase the vertical breakdown voltage by introducing a thicker buffer, but this is not practical, due to wafer warpage, traps and high costs.

Offering a far better way forward is our ultra-thin buffer technology, based on insulated sapphire substrates. Crosstalk effects are avoided with

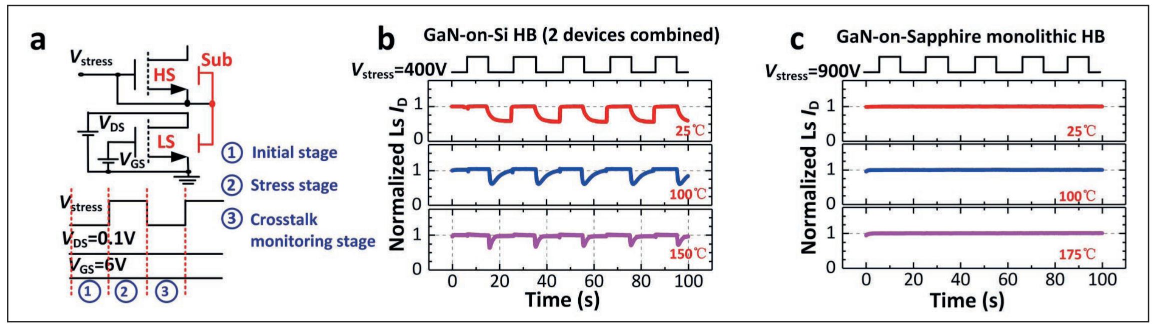


Figure 3. Crosstalk evaluation: (a) test setups, (b) crosstalk of two separated GaN-on-silicon devices with the substrate connected together, (c) no crosstalk observed on GaN-on-sapphire half-bridge devices.

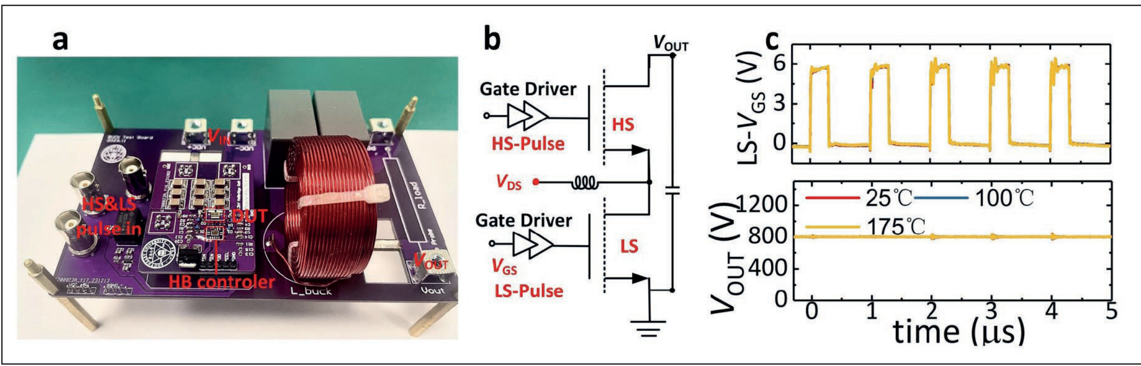


Figure 4. Boost converter performances: (a) experimental printed circuit board, (b) circuit, (c) 800 V/1 MHz output waveforms.

shallow trench isolation, realised by etching the ultra-thin buffer layer (see Figure 1 (b)). With this architecture, the breakdown voltage of the trench isolation structure exceeds 3000 V at 175 °C, while maintaining an acceptable increase in leakage current and thus ensuring safe isolation between HS and LS devices. Another strength of this design is that it provides effective suppression of the substrate biasing effect, due to the insulated substrate withstanding the voltage drop between the electrodes and substrate.

To characterise the crosstalk between the HS and LS devices, we apply a small drain-source voltage to the LS *p*-GaN HEMT, and then apply a pulsed high-voltage stress to the HS devices and substrate (see Figure 3(a)). Due to high-voltage stress, trapping occurs in the LS *p*-GaN HEMT during the stress stage. We are then able to quickly monitor crosstalk after the stress stage.

For the conventional GaN-on-silicon platform, we observe a build-up in the dynamic positive voltage between the HS source and the LS source when the HS in ‘on’ and the LS is ‘off’. Following this, there is a dynamic positive substrate-to-source stress voltage during the transition to HS ‘off’ and LS ‘on’ that drives electrons injection into the buffer of the LS *p*-GaN HEMT. When the half-bridge circuit switches so that it is also in this phase – that is, HS ‘off’ and LS ‘on’ – electrons trapped in the buffer region of the LS *p*-GaN HEMT cannot be emitted in time, and tend to partially deplete the 2DEG channel of the LS *p*-GaN HEMT, resulting in la ower drain current. That’s not the case for our platform, however, thanks to suppression of crosstalk between HS and LS HV *p*-GaN HEMTs, due to shallow trench isolation into the sapphire substrate.

The superiority of our platform is highlighted by our measurements of the drain current of a conventional GaN-on-silicon device and our proposed half-bridge device (see Figure 3(b) and 3(c)). Our results uncover obvious crosstalk in GaN-on-silicon devices at a 400 V stress voltage at room temperature, and demonstrate effective elimination of crosstalk by shallow trench isolation with our GaN-on-sapphire platform, even at a 900 V stress voltage and a temperature of 175 °C. These results indicate that trench isolation enables high-temperature operation of a monolithic GaN half-bridge device at a high voltage – the aim is 1200 V.

Monolithic ICs

To evaluate the performance of our 1200 V monolithic half-bridge circuit, we have constructed a boost converter (see Figure 4(a) and 4(b)). The output results, shown in Figure 4(c), reveal that our converter can operate under 800 V/1 MHz conditions at 175 °C.

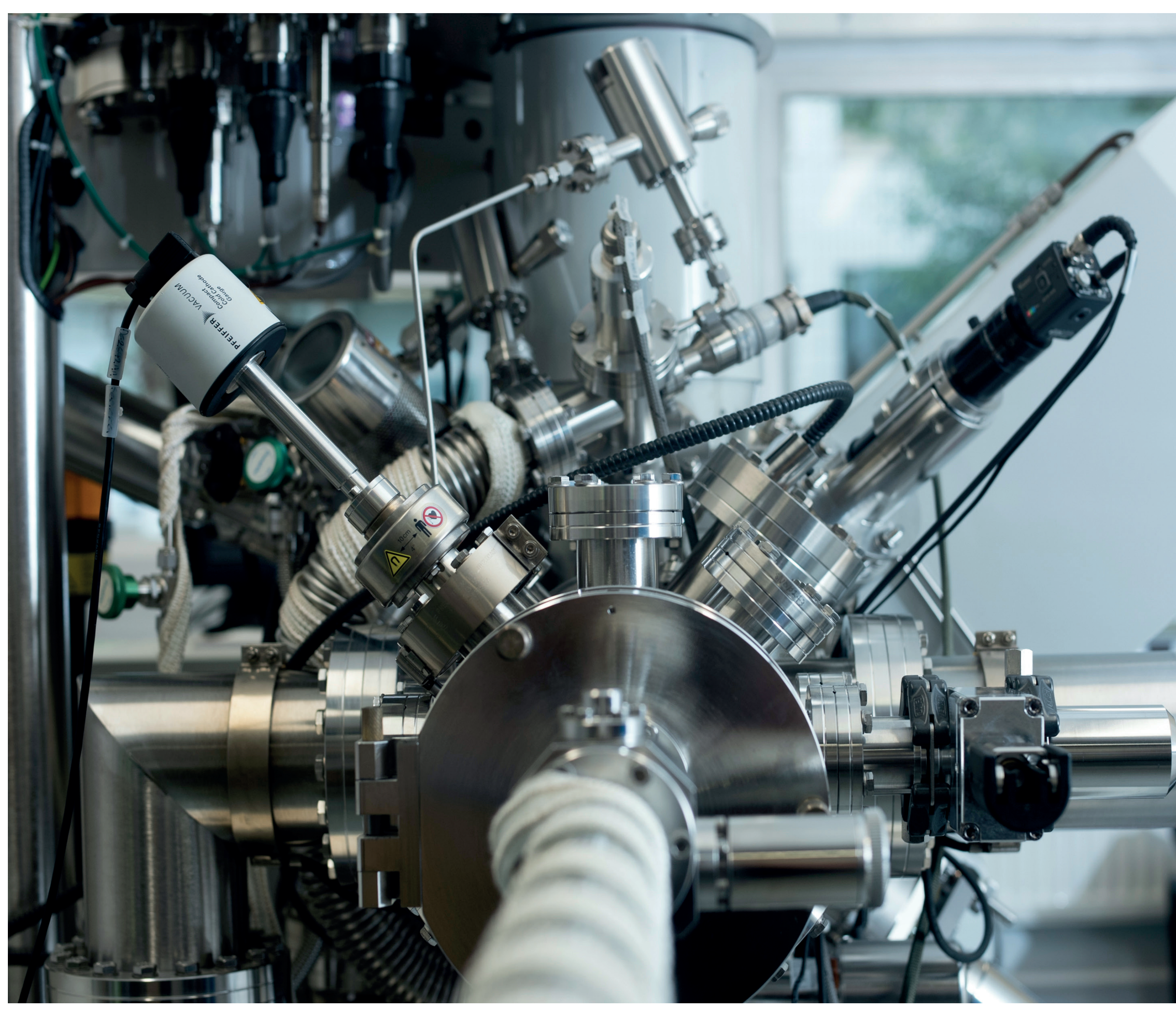
These results indicate that our proposed GaN-on-ultra-thin buffer technology is a compelling candidate for producing GaN devices for high-temperature, high-voltage power systems (see Table 1 for a comparison of our technology and that involving other foundations).

Adding to the appeal of our approach are cheap substrates and simple epitaxy, merits that slash costs and enable GaN HEMTs to target a wider range of applications. They include electric vehicles and renewable energy markets, both of which would benefit from our proposed monolithic half-bridge integration platform that combines high temperatures and high voltages with supressed cross talk.

	Maximum Rated Voltage	Normalized Device BV*	HB Isolation	HB Crosstalk	Device Leakage @25℃	Device Leakage @175℃
This work	1200V	>110V/µm	>3000V	No	<0.1nA/mm@1200V	<100nA/mm@1200V
on QST	650V	94V/µm	~1700V	No	~100nA/mm@650V	unknown
on SOI	200V	100V/µm	~1300V(trench) <1000V(box)	No	~20nA/mm@200V	unknown
on EBUS	200V	51V/µm	~1200V	No	~100nA/mm@200V	unknown
on Si	100V	--	--	--	--	--

*BV is normalized by L_{gd}.

Table 1. Comparison of *p*-GaN HEMT based monolithic integration with high blocking voltages



Gate to the future

Reliability benefits from deploying deposited gate oxides in SiC MOSFETs

BY ARNE BENJAMIN RENZ, PETER GAMMON, OLIVER VAVASOUR, VISHAL SHAH AND MARC WALKER FROM THE UNIVERSITY OF WARWICK, SUPPORTED BY JAMES GOTT FROM WARWICK MANUFACTURING GROUP AND ANDREW NEWTON AND MICHAEL POWELL FROM OXFORD INSTRUMENTS PLASMA TECHNOLOGY

THE POTENTIAL of wide bandgap power devices to deliver efficient, compact and light power conversion has been known since the 1980s. However, it was not until the late 2010s that the first SiC power converters from Tesla, BYD, Hyundai and others demonstrated the reliability and viability of the material for mass adoption. In the wide bandgap boom that followed, numerous press releases from OEMs and IDMs announced SiC chip supply agreements and joint ventures. In turn, multiple SiC IDMs have announced major billion-dollar expansion plans and supply agreements from SiC substrate manufacturers. The result is an industry that is predicted by Yole to reach $8.9 billion in 2028 at an average compound annual growth rate of 31 percent.

With a SiC MOSFET based inverter expected to be 5 percent more efficient than a silicon IGBT equivalent, the fact that the SiC chips can be up to three times more expensive is more than compensated for by the potential battery reduction. However, as OEMs become more familiar with the technology, and competition between SiC

IDMs mount, so the pressure for cost reductions increase. This is fuelling the development and adoption of 200 mm diameter substrates, the move to automated fabrication, and a move to reuse substrates.

However, many of the tools of cost reduction sit with the device designer, for whom every milliohm of resistance in their design contributes to the size of the finished die. By minimising the specific resistance of a die, a given product will be smaller, in turn increasing yields. As such each of the yields shown in Figure 1 need to be minimised, including the MOSFET channel, which is the subject of this work.

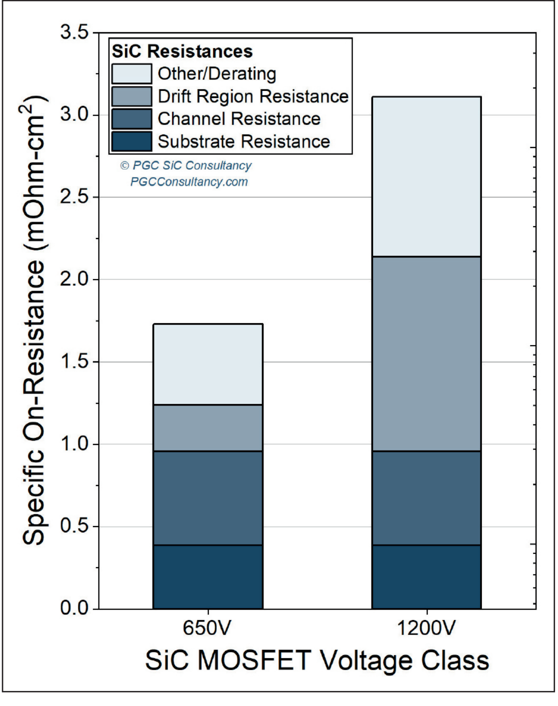


Figure 1. Individual series resistance contributions to total specific on-resistance in 650 V and 1200 V planar MOSFETs.

Challenges in gate structures

With up to one third of a SiC MOSFET's resistance originating from the channel, shown in Figure 2, this is one of the dominant resistance components in 650 V or 1200 V MOSFETs for EV systems. The main reason for this highly resistive channel is the high density of defect states at the interface between the semiconductor and dielectric. For the SiO_2/SiC interface, the density of interface defect states is typically between a hundred and a thousand times higher than it is for SiO_2/silicon. These unwanted states, and the charges trapped in them, enhance scattering at the interface. In turn, the increased scattering drags down channel mobility and significantly increases the channel resistance. The channel mobility in today's commercial MOSFET applications is just 20-40 $cm^2 V^{-1} s^{-1}$, far lower than the theoretically achievable bulk mobility of SiC, which is around 1000 $cm^2 V^{-1} s^{-1}$.

Ironically, the root cause of the high channel resistance in the SiC MOSFET is related to one of its biggest strengths: unlike GaN and diamond, SiC can be thermally oxidised to form SiO_2. However, the presence of carbon causes problems.

During regular oxidation, occurring at temperatures of more than 1200 °C, SiO_2 initially forms through the consumption of SiC, and carbon is dispersed as CO_2. However, as the SiO_2 get thicker, not all carbon can diffuse through it, causing carbon to accumulate at the SiC/SiO_2 interface (see Figure 3). This trapped carbon creates charge states in the channel region of the SiC MOSFET that scatter electrons and impair the channel mobility of this transistor.

One option for improving channel mobility is post-oxidation annealing in NO or N_2O. Alternatively, the oxide can be grown using NO or N_2O directly. The origin for this improvement is disputed, but a popular and widely accepted explanation is that the nitrogen attaches itself to dangling bonds and other atomic defects, rendering them passive and inactive. Of the two sources of nitrogen, NO gives the highest channel mobility. However, as it is toxic and difficult to handle safely, N_2O is often used instead.

Over the past decade, a number of processing solutions have been developed to circumvent the inherent disadvantages arising from thermal oxidation. Efforts have focused on deposition-based processes, such as atomic layer deposition (ALD) and low-pressure CVD. With these approaches, the entire oxidation process is based entirely on the chemical reaction between silicon and oxygen precursors, with no consumption of the underlying SiC or residual carbon at the interface.

Our team, a partnership between Warwick University, Warwick Manufacturing Group and Oxford Instruments, is developing one such process. Our solution for improved gate oxide reliability focuses on ALD.

Controlling conformal depositions

All ALD processes involve the delivery of one precursor into the chamber in a short pulse. This

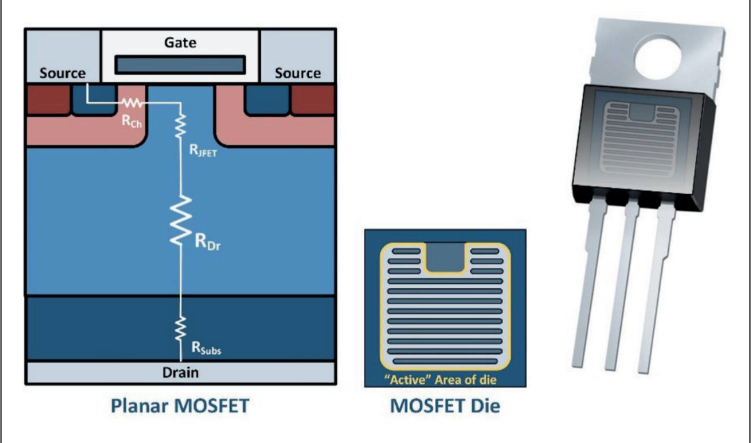


Figure 2. (left) Cross-sectional image emphasising the individual resistance contributions and (middle and right) an image of a packaged device.

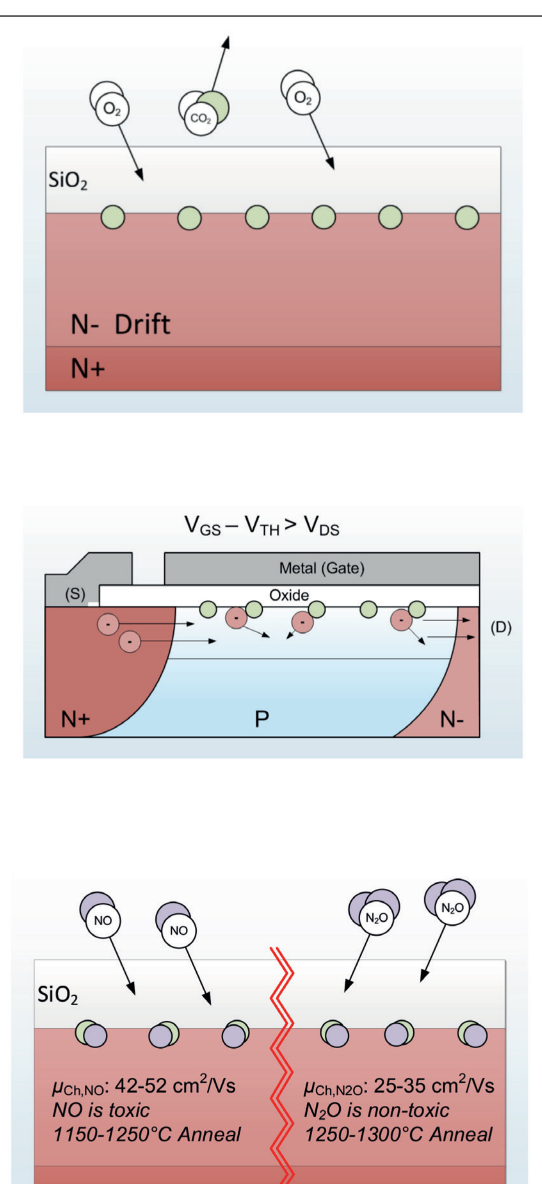


Figure 3. (Top) Interface states build-up due to incomplete carbon transfer away from the interface and (middle) interfacial charge scattering in the channel, causing a decrease in channel mobility; (bottom) common post-oxidation anneals to improve channel mobilities.

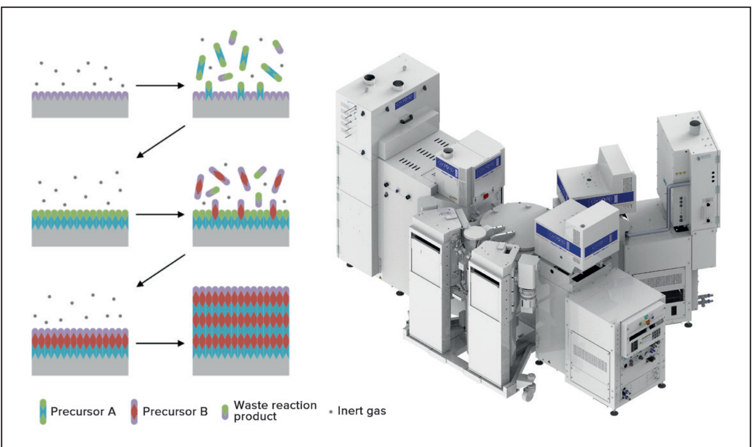


Figure 4. (Left) The ALD process shown diagrammatically. Precursors adsorb and react in a layer-by-layer manner to build up films in steps of individual atomic layers; (right) example of a fully automated ALD tool, e.g., Oxford Instrument Plasma Technology's ASP Cobra tool.

precursor is adsorbed onto the samples surface, with molecules remaining on the surface after the pulse is complete. A second precursor is then pulsed into the chamber. This additional precursor reacts with the adsorbed layer, ideally to form a single atomic layer of the desired material. Unlike thermal oxidation, this approach avoids any consumption of the underlying semiconductor material. Cycling of this process stops after reaching the desired oxide thickness.

Unfortunately, as is the case with as-grown thermal layers, the quality of the as-deposited gate dielectrics is not ideal. Weaknesses include high leakage currents, large hysteresis voltages and substantial mobile charges in the oxides. To address these issues, it's the norm to anneal the dielectric in a furnace heated to between 1000 °C and 1200 °C. While an inert gas such as argon is commonly used for the post-process anneal, forming gas adds 5 percent hydrogen for reducing chemistry, in contrast to the oxidising chemistry of NO and N_2O (see Figure 4 for an illustration of the current state of the art).

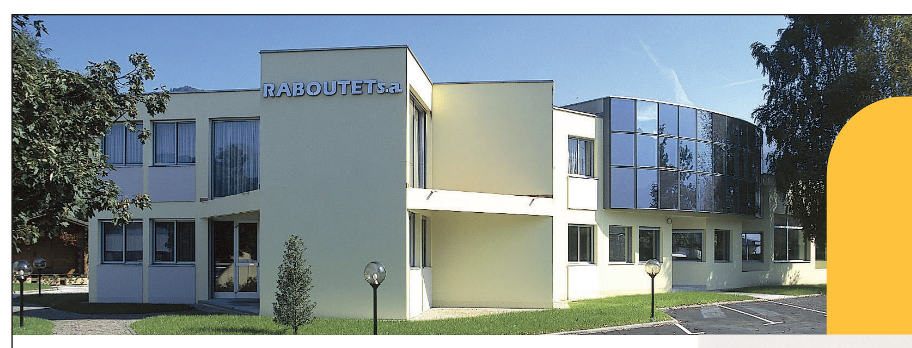
Our team has spent several years developing SiC MOSFETs with low channel resistances. This can be achieved with a fully automated ALD kit produced by Oxford Instruments.

We have taken a slightly different approach from the one that most commercial entities would have pursued, deciding to shy away from using thermal oxides. We have avoided them because our view is that a deposition-based process is better suited to realising high channel mobilities – it offers greater control, as well as the opportunity to draw on the wealth of experience from very similar silicon passivation techniques that have been used to improve the interface.

Our approach begins with the deposition of a 40-50 nm-thick SiO_2 layer by ALD, followed by annealing for 1 hour in forming gas at 1,100 °C. More details of our process have been reported in the papers listed in the reading list at the end of this article (see (Figure 5 (a)) for a picture of a 200 mm wafer during the RCA 1 & 2 standard clean, and a fully patterned wafer during inspection (see Figure 5 (b)).

Measurements of the electrical characteristics of our devices have produced excellent results. In our lateral MOSFETs, the maximum field-effect mobility is 110 $cm^2 V^{-1} s^{-1}$ (see Figure 7 (a), outperforming any commercially available SiC MOSFET. If industrial producers of SiC MOSFETs adopt our process, they could trim the total specific on-resistance by more than 10 percent, and have the opportunity for a die shrink while maintaining the blocking voltage and current rating.

When introducing any new processing technology, there is a need to assess whether it has any impact on device reliability. To investigate this, we began



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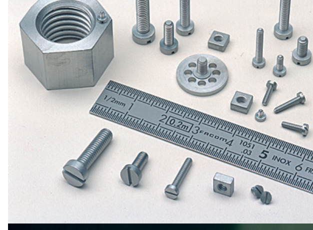

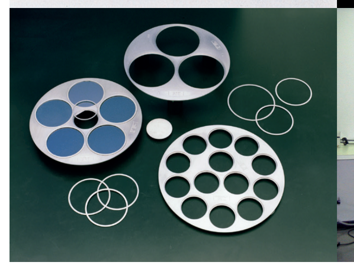

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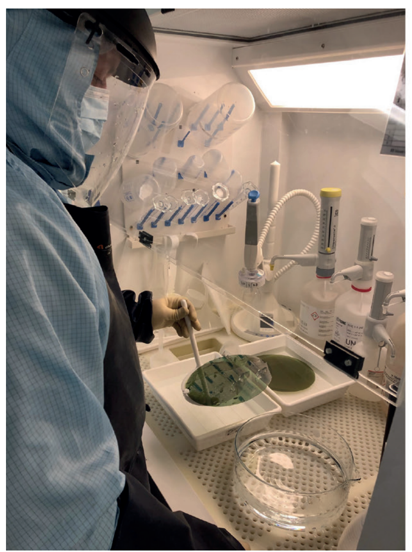

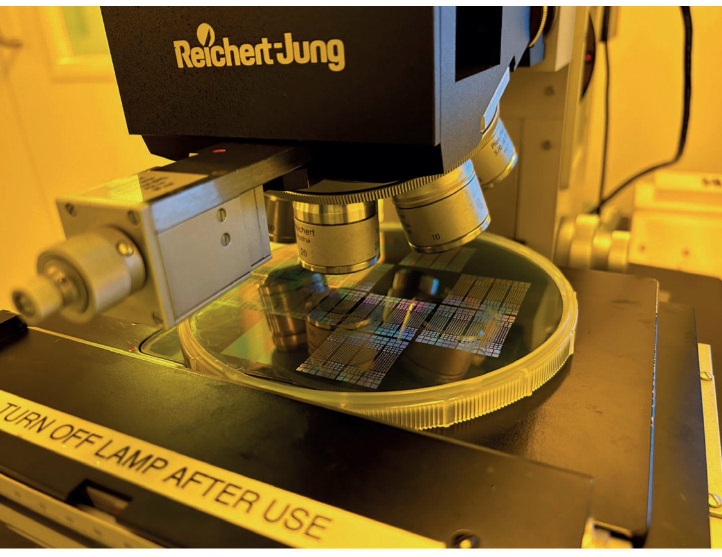

Figure 5. (Left) RCA clean of an 200 mm SiC wafer prior to device fabrication and (Right) Optical microscopy inspection of a fully patterned 150 mm SiC MOSFET wafer, showing multiple test cells.

by stressing our power devices at constant voltages until we detect oxide breakdown (see Figure 6 for the test setup for static characterisation of our SiC devices).

Compared with the more conventional approaches to forming an oxide, such as direct thermal growth or low-pressure CVD, gate oxides produced with our ALD process consistently show the most promising results. Our extracted channel mobilities offer a path to lower-resistance MOSFETs (see Figure 7 (a)), and we realise the best breakdown performance, allowing devices to be stressed at higher voltages before they fail (see Figure 7(b), which shows the current-voltage results of the investigated devices). What's more, our MOSFETs are more robust, evidenced by the longer time that a device can be stressed before it breaks down (see Figure 7 (c)). Extrapolations from stress tests at multiple electric fields demonstrate that our devices can operate at higher voltages while providing the same lifetime as their thermally oxidised counterparts.

To put our efforts into perspective, let's consider the planar 1.2 kV SiC MOSFET. When produced with our process, this device can operate at higher electric fields, provide a reduction in on-resistance by 30 percent, and guarantee a sufficient dielectric lifetime.

How does it work?

An immense advantage of our collaboration is that we have access to world-leading physical characterisation expertise, as well as a direct pathway to the market.

Over the last ten years there has been the development of the Warwick Photoemission

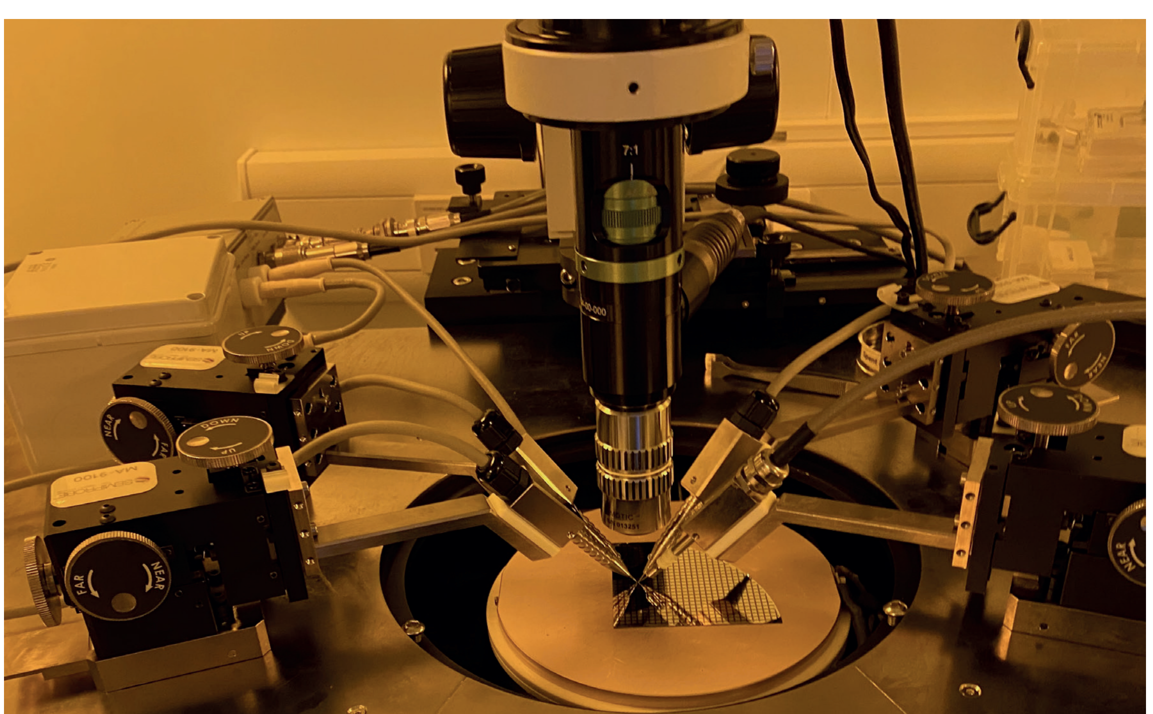

Figure 6. Quarter of a 150 mm MOSFET wafer on a Semiprobe semi-automatic probe station. Measurements were carried out using a Keysight B1505A parameter analyser. Automated measurements connecting both the stage and analyser were programmed using standard LabView software.

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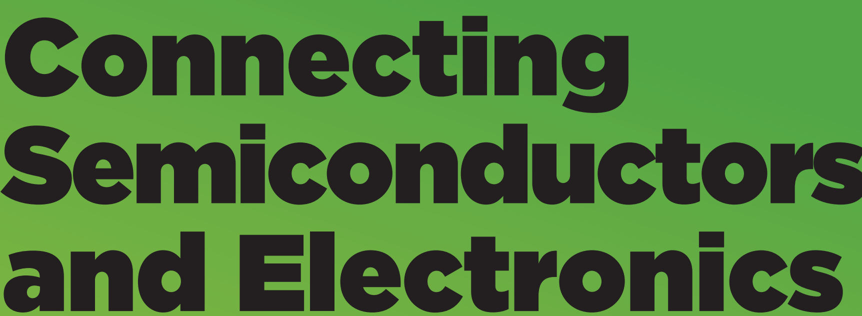

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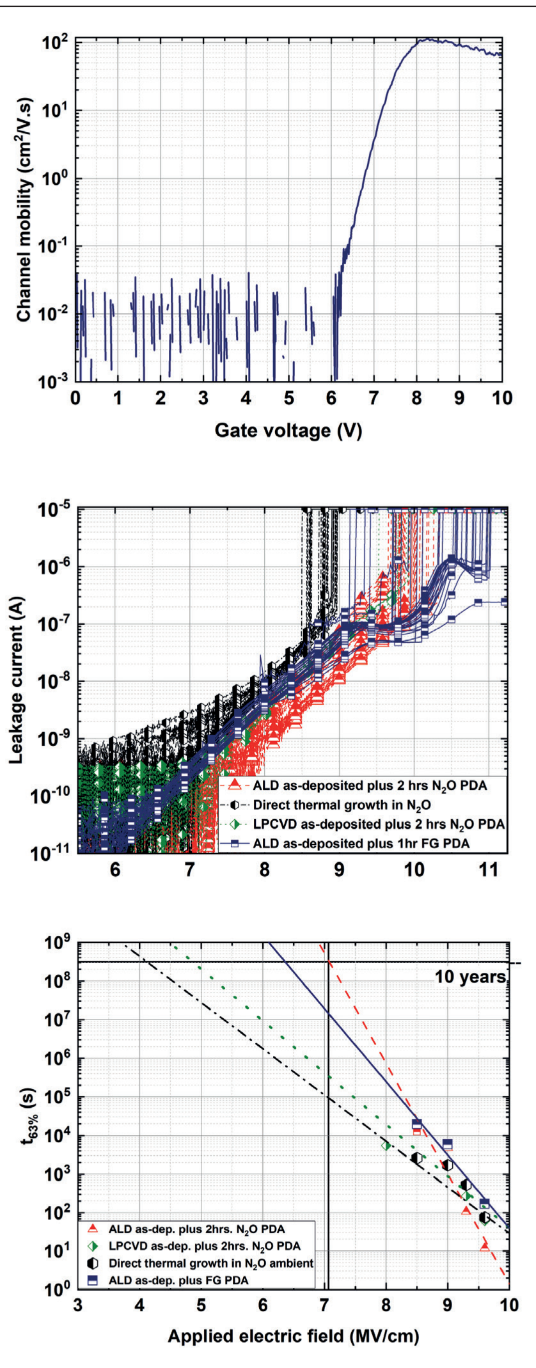


Figure 7. (Top) Extracted channel mobility of a representative lateral MOSFET structure with a channel length of 100 μm. (Middle) I-V measurements of the investigated samples at 175 °C with a device area of 3.14×10^{-4} cm². (Bottom) Time to breakdown versus applied voltage/electric field of measured devices. It is evident that the presented deposited oxides offer a path towards more reliable SiC products.

Research Technology Platform under the leadership of Marc Walker, a co-author of this feature. This suite of photoemission kit, which can be applied to semiconductor interface analysis, includes X-ray photoelectron spectroscopy specifically tailored towards the analysis of the SiC MOSFET, including the SiO_2/SiC interfaces.

One of the strengths of X-ray photoelectron spectroscopy is that it can be used to analyse the chemical bonding environment at the SiO_2/SiC interface. By comparing thermally oxidised and ALD-deposited oxides with this form of spectroscopy, we can reveal potential approaches to passivate defects.

With our Kratos Axis Ultra delay-line detector and ScientaOmicron multiprobe instruments, we are gaining additional insight into the origins of improvement brought about by the ALD process (see Figure 8 (a)). With this tool we have been able to determine whether an interface is richer in silicon or carbon by looking at the stoichiometric ratio of Si-C in the silicon 2p spectrum and C-Si in the carbon 1s spectrum.

This approach has revealed a C:Si ratio below 1 for all deposited samples, indicating that the interface is silicon-rich. Our samples produced using ALD and a forming gas anneal have the most silicon-rich bonding environment (see Figure 8 (b)). Previous work from our group has established that this arises from the creation of a silicon-rich environment near the interface after ALD deposition of SiO_2, a situation that makes it easier to passivate silicon dangling bonds.

Alongside the revealing X-ray photoelectron spectroscopy analysis, our team has employed transmission electron microscopy to scrutinise the sharpness, cleanliness, chemical composition and, generally, the quality of the oxide/semiconductor interface (see Figure 9 (a) for an image of our scanning transmission electron microscope, the Thermo Scientific Talos F200X).

Using our scanning transmission electron microscope, we have undertaken structural and chemical analysis of our samples with sub-nanometre resolution. Operating at 200 kV, the F200X delivers high-resolution imaging in both transmission electron microscopy and scanning transmission electron microscope modes with a spatial resolution smaller than 0.14 nm. This instrument also provides fast, precise chemical mapping, using the Super-X quad energy dispersive X-ray spectroscopy detectors.

After preparing our samples with a focused-ion beam scanning electron microscope (see Figure 9 (b), we loaded them into the F200X to investigate the interfaces. We were keen to determine the presence of materials, the order of the semiconductor-oxide transition, and to see if

Our research has demonstrated the value and readiness of ALD gate dielectrics on SiC. Channel mobility and reliability analysis shows substantial improvements on the current state of the art.

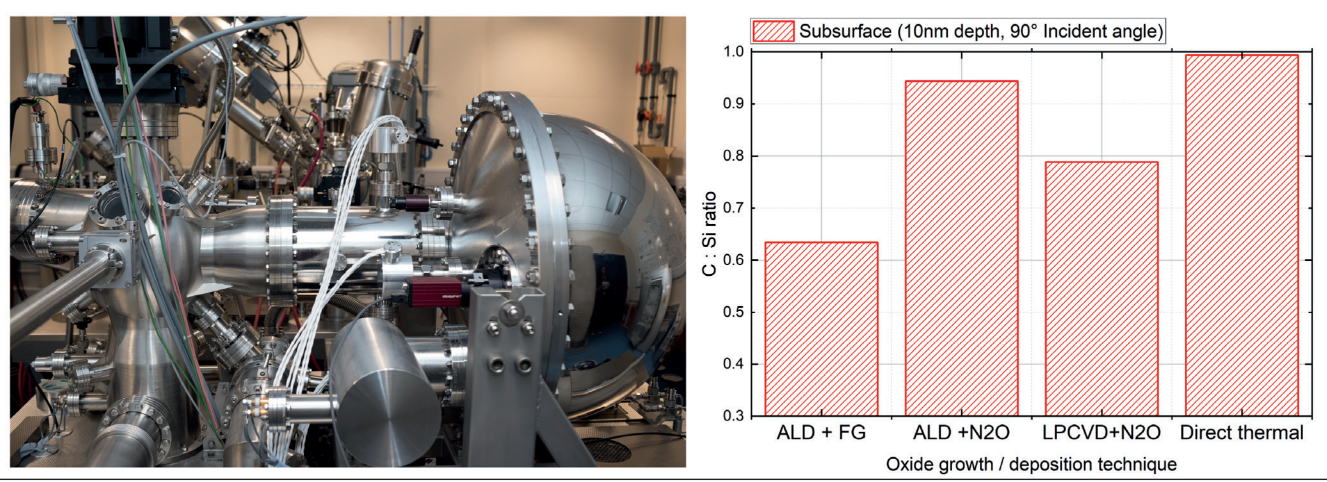


Figure 8. (Left) The Scienta r4000 ARPES analyser mounted on the ScientaOmicron multiprobe photoemission system. Samples are illuminated with Al Kα X-rays. Any spectra were analysed at take-off angles of 90 ° and 15 °, giving a measurement depth of 10 nm and 3 nm, respectively. Photoelectrons were detected in the SPHERA hemispherical analyser mounted on the same instrument, and on the Kratos Axis Ultra DLD instrument (not shown). (Right) Extracted C:Si ratios of the investigated samples.

there were any obvious surface decorations. We are encouraged by our findings, which reveal that our annealed gate dielectric formed by ALD has excellent interface quality.

Our research has demonstrated the value and readiness of ALD gate dielectrics on SiC. Channel mobility and reliability analysis shows substantial improvements on the current state of the art. Physical characterisation has identified a chemical foundation of the performance gains and excellent physical morphology. The superb controllability of ALD processes offers further scope to improve gate oxide, on-resistance, yield and cost. Our next step is to perform a pilot of the process and verify its reliability in commercial devices, paving the way to large-scale production.

The authors wish to thank Marc Walker, Akif Yildirim, Gerard Colston, Qinze Cao, Kyrylo Melnyk, Xinkai Tian and Richard Jefferies from the University of Warwick, Geoff West from Warwick Manufacturing Group and Grant Baldwin from Oxford Instruments Plasma Technology.

Figure 9. (Left) Thermo Scientific Talos F200X scanning transmission electron microscope. (Right) Sample after thinning back by means of focused-ion beam scanning electron microscope.

β-Ga_2O_3 RF power FETs

A promising candidate for tomorrow's high-voltage, high-power RF applications, the β-Ga_2O_3-on-SiC RF power FET is already amplifying signals up to 8 GHz with output power density approaching 1 W mm^{-1}

BY MIN ZHOU, HONG ZHOU, JINCHENG ZHANG AND YUE HAO FROM XIDIAN UNIVERSITY

THERE ARE a number of applications that require amplifiers with a high power and a high efficiency producing mega-watt powers within the UHF to X-band. Those applications where these amplifiers can serve include: airport surveillance; particle accelerators for scientific or industrial systems; and weather, marine and military radar systems.

Since power is the product of current and voltage, the options for realising a high-power, solid-state RF transistor are to use either a very high current or a very high voltage. Of these two, there are many downsides associated with a large current. This approach involves a large gate periphery and hence a substantial chip size – and that brings the downsides of high cost, low load-impedance and increased network loss. Using a high voltage is favoured for several reasons, now discussed.

The benefits of a higher voltage include realising higher powers and minimising network loss. A higher supply voltage leads to a proportionally higher output power, enabling a smaller chip size for the same power output, a major attribute for multiple-input, multiple-output (MIMO) systems.

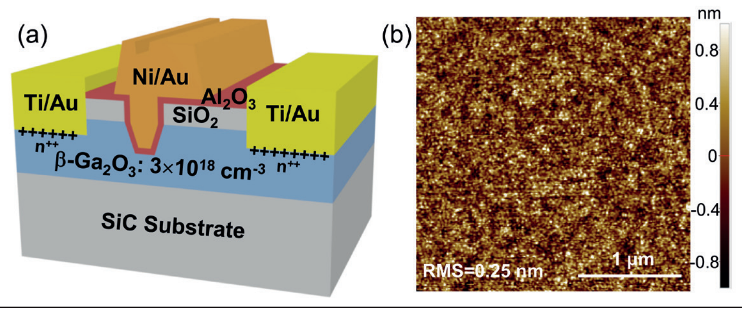


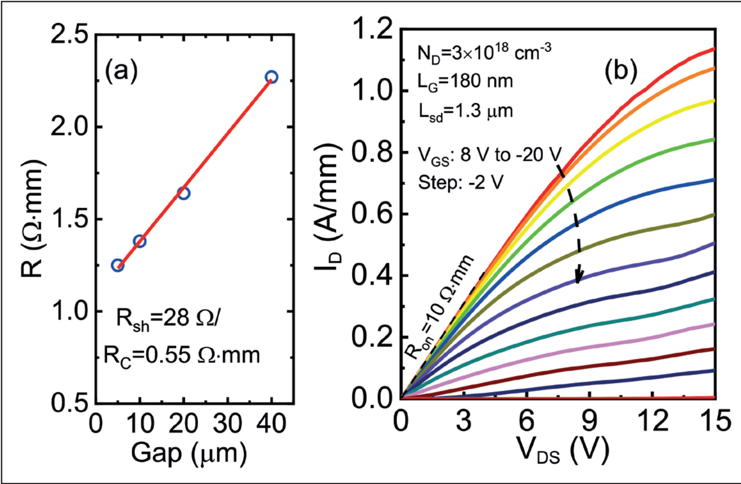
Figure 1. (a) β-Ga_2O_3 RF power FETs on SiC substrates realise efficient heat extraction, a low on-resistance, a high maximum drain current, a high blocking voltage, and high values for f_T and f_{max}. (b) Atomic force microscopy image of the piranha-solution-treated β-Ga_2O_3 thin film.

What is more, in accordance with Ohm's law, operating at a higher voltage results in an equal increase in load-line resistance. To illustrate this benefit, let's consider a given output power of 1 kW, while, for simplicity, neglecting the knee voltage of the transistor. When the operating voltage increases from 50 V to 200 V, the load impedance increases from 1.25 Ω to 20 Ω. Due to this, the corresponding transformation ratio for matching to 50 Ω is far more favourable, improving from a factor of 40 to just 2.5. In conjunction, there is a decrease in the total gate periphery of the transistor. In turn, this avoids more complicate matching networks for very-high-power devices, and minimises network loss.

The use of high voltages also enables a high efficiency at high frequency. This is most valued, because the delivery of sufficient output power requires a system with thousands of modules, a condition leading to a degradation in efficiency. Another concern is the shunt RC-circuit, created by the combination of load-line resistance and output capacitance – the latter dominates the output impedance at high frequency and results in a quasi-short-circuit.

To design a high-efficiency amplifier, engineers tend to exploit harmonic termination technology. Consider, for example, the class B amplifier, which has a theoretical maximum efficiency of 78.5 percent, realised by shorting all harmonics. When engineers adopt harmonic termination technology they match the network with the second and third harmonic frequency, and possibly higher ones, rather than simply matching the fundamental frequency. Note that it is possible to reach a theoretical maximum efficiency of 100 percent with the likes of a Class E or Class F amplifier.

When engineers consider harmonic termination technology, they take into account that the higher the fundamental frequency, the greater the number

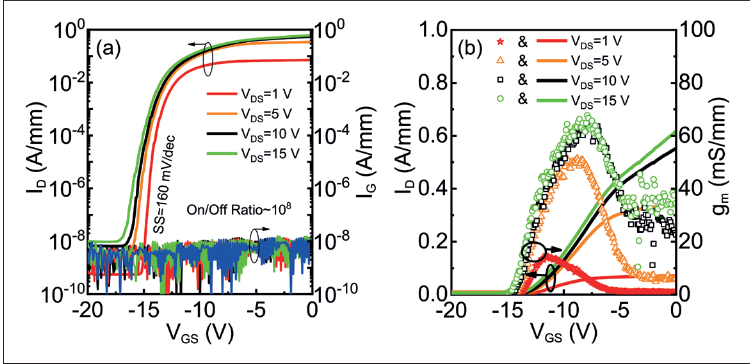


➤ Figure 2. (a) Contact resistance (R_c) extraction through transmission-line measurements. (b) Output characteristics of the β-Ga_2O_3 RF power FET.

of harmonics that tend to be intrinsically shorted by the output capacitance. This is an important consideration, as it limits the theoretical achievable efficiency, resulting in Class-B-like operation. Since higher operating voltages offer the opportunity to decrease the total gate periphery of the transistor and improve the load impedance, they can ensure lower parasitic capacitances and a smaller system loss.

Over the last decade or so there has been greater uptake of GaN HEMTs in ultra-high-voltage RF amplifiers. The primary appeal of this wide bandgap material is that offers a far higher power density than that of silicon equivalents. However, it has its weaknesses, including a high dislocation density and, when used to make transistors, a current collapse that occurs at high operating voltages.

These weaknesses are spurring interest in other materials for meeting power-versus-bandwidth demands. This begs the question: Within the portfolio of wide bandgap material systems, which is best at providing a high power density, alongside reductions in size, weight, capacity and loss, that will ultimately enable smaller, lighter and more efficient systems?



➤ Figure 3. Log-scale (a) and linear-scale (b) transfer characteristics.

The potential of β-Ga_2O_3

A strong contender within this portfolio is the ultra-wide bandgap semiconductor β-Ga_2O_3. With this oxide, the focus has been the power device. However, β-Ga_2O_3 also offers much potential for RF electronics. The prowess of this oxide evident in its values for two key figure of merits: the Baliga figure of merit, used to evaluate DC conduction losses; and the Johnson figure of merit, a guide to evaluating power-frequency capability. Judged against both yardsticks, β-Ga_2O_3 is three times better than GaN and eight times better than SiC, thanks to a bandgap of 4.6-4.8 eV, a critical field of 8 MV/cm, and a saturation velocity of 1.5-2 × 10^7 cm/s.

As well as these superior physical characteristics, β-Ga_2O_3 promises a lower cost for device production. Affordable native β-Ga_2O_3 substrates can be produced from melt-grown bulk single crystals, highlighting the potential for low-cost, low-defect density β-Ga_2O_3 material, a significant asset for future commercialisation.

In general, the attributes of an ideal RF device are a high current density with a low on-resistance, a high breakdown voltage to maintain high power, high values for the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) to ensure high-frequency operation, a high gain, and good heat dissipation. Transistors formed with β-Ga_2O_3 have the potential to excel on many of these fronts. The combination of a high critical-field-induced high breakdown voltage, a high saturation-velocity-induced frequency, and a low resistance, possible through controllable *n*-type doping up to 10^{19} cm^{-3}, offer a strong foundation for developing high-performance RF power transistors.

Some may question the promise of the β-Ga_2O_3 RF device, given that carrier mobility is limited to 200-250 cm^2 $V^{-1}s^{-1}$. However, it's important to understand that during RF operation, mobility only plays a meaningful role in low electric field regions prior to velocity saturation. During operation at high voltages, high electric fields are induced, accelerating electrons to a high velocity that allows the device to deliver a high gain at high frequencies.

Recent demonstrations of lateral and vertical β-Ga_2O_3 Schottky barrier diodes have underscored the potential of this material system. Highlights include a blocking voltage of more than 10 kV, and a performance that surpasses the one-dimensional unipolar limit of SiC and GaN. There are also impressive results reported for high-power β-Ga_2O_3 lateral FETs, including a breakdown voltage of up to 10 kV and a Baliga figure-of-merit approaching 1 GW cm^{-2}.

While advances in β-Ga_2O_3 RF devices have been overshadowed by those in the power domain, some progress has been made. Highlights include values for f_T and f_{max} of 47 GHz and 51 GHz, respectively, for devices with a gate length of 0.1 μm produced by Jiandong Ye's group at Nanjing University; and

an average breakdown field of 5.4 MV cm^{-1}, which exceeds the theoretical limit of GaN and SiC, for devices made by Chinmoy Nath Saha's group at the University at Buffalo. These results reveal the immense potential of β-Ga_2O_3 for future high-voltage, high-power, high-frequency RF electronics.

One weakness needing to be addressed is the large signal performance of the β-Ga_2O_3 RF power transistor. Output power densities are below 0.8 W mm^{-1}, even for devices operating in pulsed mode at a frequency of around just 1 GHz. It is generally considered that two factors are holding back this aspect of the device: the low output current density induced high on-resistance; and self-heating, stemming from the low thermal conductivity of β-Ga_2O_3 substrate.

β-Ga_2O_3 RF MOSFETs

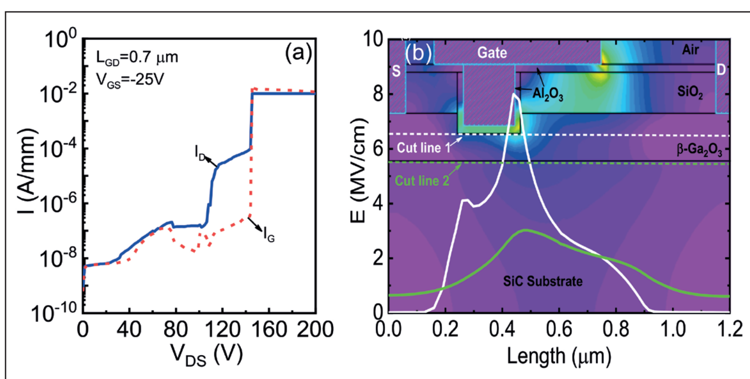
Tackling both of these issues is our team from Xidian University, China. We are breaking new ground by transferring a heavily doped film of β-Ga_2O_3, which is subsequently subjected to silicon-ion implantation, to a substrate with a higher thermal conductivity.

Our process begins by transferring a β-Ga_2O_3 thin film, tin-doped to a level of 3 × 10^{18} cm^{-3}, from a (-201) bulk substrate to a SiC substrate. This is accomplished with steps that are similar to ion-cutting and exfoliation (see Figure 1(a)). They involve planarizing the surface with chemical mechanical polishing, before thinning down the channel layer from around 500 nm to between just 100 nm and 110 nm by dry etching with BCl_3.

The critical foundation for our high-performance transistors is great material quality. To realise this, we apply a piranha solution to our β-Ga_2O_3 thin film on SiC, a step that reduces the root-mean-square roughness of the material to just 0.25 nm (see Figure 1(b)).

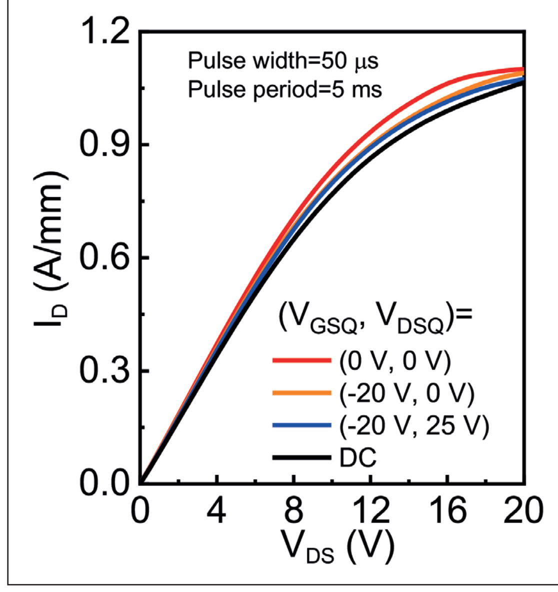
Our next step involves lowering the contact resistance, realised by silicon implantation with a dose of around 10^{15} cm^{-2}. According to transmission line measurements, this ensures a contact resistance of just 0.55 Ω mm (see Figure 2(a)). By combining with a heavily doped channel layer to reduce the device on-resistance, we have obtained well-behaved output characteristics for our β-Ga_2O_3RF power FET, including an on-resistance of 10 Ω mm and a maximum on-current of 1.1 A mm^{-1} (see Figure 2(b)).

To suppress short channel effects, we employ a gate recess technology. Plots of transfer characteristics, involving measurements of the drive current as a function of the gate-source voltage, provide proof of great gate control, with a subthreshold swing of 160 mV/dec and a transconductance of 70 mS mm^{-1} (see Figure 3). Incorporating a T-gate field plate aids electric field management, with a β-Ga_2O_3 RF power device with a gate length of 180 nm and a gate-to-drain distance of 0.7 µm realising a breakdown voltage of 150 V – that translates to an average electric field of 2.15 MV cm^{-1}. We have used TCAD simulations of the electric field to assess our device design. These simulations show that our T-gate field plate suppresses the peak electric field at the gate edge. Extracted peak electric fields in the β-Ga_2O_3 channel and SiC substrate are 8 MV cm^{-1} and 3 MV cm^{-1}, respectively, suggesting a full exploitation of the high critical field of these materials (see Figure 4).



➤ Figure 4. (a) Three-terminal off-state breakdown characterization of the device. (b) TCAD simulation of the electric-field contour of the same device at a blocking voltage of 150 V.

For RF power transistors, the output power under high-voltage operation can be pegged back by current collapse. It is generally accepted that this occurs when carriers are captured by traps, either at the interface or present in bulk material. We have investigated if current collapse is an issue in our devices by undertaking pulsed measurement at various quiescent bias points. Our measurements show minimal current collapse (see Figure 5). Compared with the DC curve, all the pulsed maximum drain currents are only slightly higher, even at a high drain-source voltage of 20 V. This lack of variation is evidence of excellent heat dissipation from the high-thermal-conductivity SiC substrate. Another encouraging result is that



➤ Figure 5. Pulsed I_D-V_{DS} characteristics of the device with a 50 µs pulse width and a 1 percent duty cycle.

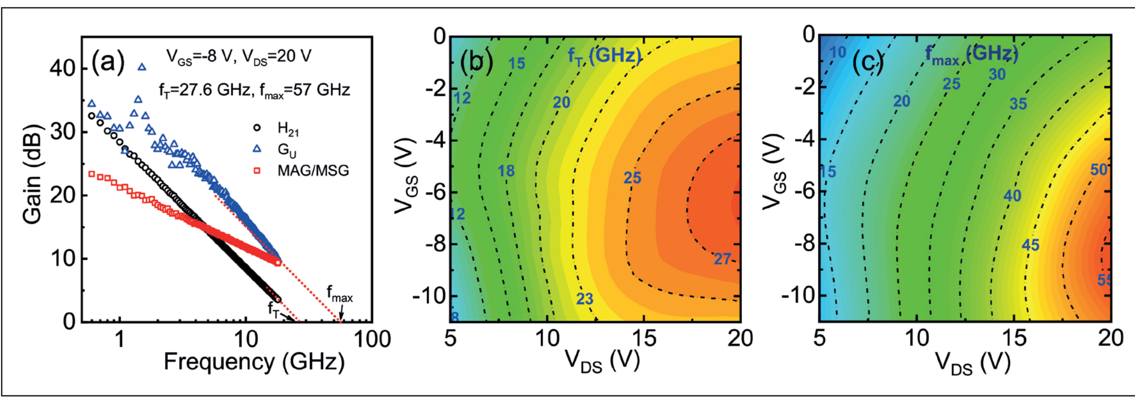


Figure 6. (a) Small-signal RF performance of the β-Ga_2O_3 RF power FET with a gate length of 180 nm. Extracted f_T (b) and f_{max} (c) dependence on the V_{GS} and V_{DS} mapping contour.

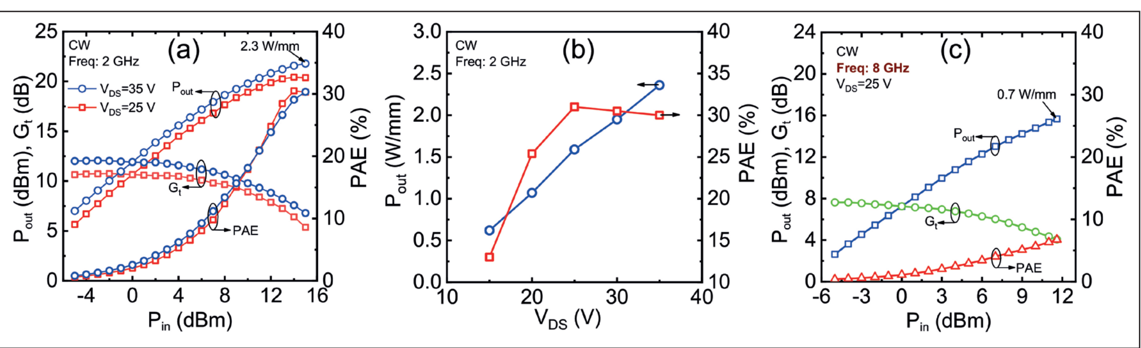


Figure 7. (a) Continuous-wave large-signal class-AB performance of the device with a power sweep at 2 GHz. (b) Output power (P_{out}) and power-added efficiency (PAE) dependence on the drain-source voltage (V_{DS}). (c) 8 GHz large-signal performance of the β-Ga_2O_3 RF power FET.

compared with the cold channel state, gate and drain pulsed on-current show no obvious change. The lack of current collapse verifies the high quality of our MOS interface and our β-Ga_2O_3 materials, which provide the foundation for realising a high output power and a high power-added efficiency at a high drain-source voltage.

Drawing on great DC characteristics and a high-quality β-Ga_2O_3-on-SiC material platform, our β-Ga_2O_3 RF devices have values for f_T and f_{max} of 27.6 GHz and 57 GHz, respectively. Additional impressive results are a value of around 5 GHz μm for the product of f_T and the gate length, and 39.7 GHz for $(f_T \times f_{max})^{0.5}$. We find that the values for f_T and f_{max} increase with drain-source voltage, due to an increased electric field along the channel that boosts carrier velocity. This trend is beneficial, as operating a power amplifier at a higher drain-source voltage increases its gain (see Figure 6).

Measurements of our device's large-signal load pull characteristics using an input signal under continuous-wave mode show that introducing the β-Ga_2O_3-on-SiC material platform and a highly-doped β-Ga_2O_3 channel enables an output power density of more than 2.3 W/mm, realised with a power-added efficiency of 30 percent at 2 GHz (see Figure 7(a)). Output power density increases by 0.5 W mm^{-1} for every 5 V increase in the drain-source voltage (see Figure 7(b)).

Our efforts have included an expansion of the signal amplification range from 2 GHz to 8 GHz, with an output power density of almost 1 W mm^{-1} realised at 8 GHz. Note that this is the first demonstration of an oxide semiconductor RF power FET amplifying a signal of up to 8 GHz (see Figure 7(c)).

A key conclusion from our work to date is that high-voltage β-Ga_2O_3 RF power devices can operate at a high frequency with a high power density. Through innovation – the combination of a β-Ga_2O_3-on-SiC material platform, a highly-doped β-Ga_2O_3 channel, and a T-gate with field plate – we are concurrently realising efficient heat extraction, a low on-resistance, a high maximum drain current, a high blocking voltage, and high values for f_T and f_{max}.

Our results verify the great promise of β-Ga_2O_3-on-SiC RF FETs for future high-voltage, high-frequency, high-power and high-efficiency applications. Our next steps are to optimise the fabrication process, scale the gate length, and produce hundreds-volt-class β-Ga_2O_3 RF devices.

FURTHER READING / REFERENCE

- M. Zhou *et al.* "1.1 A/mm β-Ga_2O_3-on-SiC RF MOSFETs with 2.3 W/mm Pout and 30% PAE at 2 GHz and f_T/f_{max} of 27.6/57 GHz" IEDM, p. 38.4, 2023.

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GaN VCSELs: Refining the production process

Superior control of the cavity thickness enhances the capability to target an emission wavelength

ENGINEERS from Japan have developed a ground-breaking process for producing incredibly efficient VCSELs that emit very close to their target wavelength.

This development, by a partnership between researchers at Meijo University and the National Institute of Advanced Industrial Science and Technology, will help efforts to commercialise GaN-based VCSELs – they are promising sources for deployment in adaptive headlights, retinal scanning displays, and systems providing point-of-care testing and visible-light communication.

The lasers produced by this team have an emission wavelength of 417.7 nm, just 0.3 nm from the target value, and they produce a wall-plug efficiency that peaks at more than 20 percent.

➤ A 5 nm-high mesa ensures lateral current and optical confinement.

For GaN VCSELs, that's a very impressive efficiency. Putting that figure in perspective, team spokesman Tetsuya Takeuchi from Meijo University told *Compound Semiconductor* that he is not aware of any other team that has broken the 20 percent efficiency barrier for a GaN-based VCSEL.

The latest triumph for Takeuchi and co-workers follows many years of work directed at improving their process for producing GaN-based VCSELs. This class of laser features either a pair of dielectric mirrors, or a dielectric top mirror and a bottom mirror formed from alternating layers of AlInN and GaN. The latter simplifies the fabrication process, as there is no need to remove the substrate. However, growth of a high-quality mirror from 40 pairs of AlInN and GaN is far from trivial.

To improve the quality of this mirror, Takeuchi and colleagues initially cleaned the AlInN surfaces with thermal hydrogen processes, before more recently adding an *in-situ* measurement of the reflectivity spectra, to increase control over the cavity thickness. Prior to the latter refinement, a ± 2 percent deviation in growth rate threatened to deviate the cavity resonance wavelength by ± 8 nm, potentially shifting the resonance wavelength towards the edge of the stop band for the mirror. This concerning state-of-affairs, which could impede device performance, has recently been addressed with the introduction of *in-situ* monitoring, which ensures a cavity length within 0.5 percent of the target wavelength.

Building on this breakthrough, the team is now calibrating the thickness of the ITO layer and the N_2O_5 spacer layer, using vertical-cavity test structures.

Part of the reason for taking this particular approach is that the engineering team does not have access to a sputtering system featuring *in-situ* monitoring, according to Takeuchi: "Another is that the total thickness is just one-tenth of the total thickness of GaN-based layers in the cavity, so that the thickness deviation of ITO/N_2O_5 is not very critical."

Investigations featuring 10 mirror pairs of AlInN and GaN determined that when sputtering ITO and N_2O_5, the control accuracy, in terms of resonance wavelength, is ±3 percent. However, as the team's VCSEL design employs a 4λ-cavity, and the thickness for the two oxide layers is just 0.3λ, the actual thickness deviation resulting from this pair of oxide layers is roughly half that for the GaN-based 3.7λ cavity.

The team incorporated this design of cavity into a portfolio of VCSELs featuring 5 nm-high mesas with diameters of 5 μm, 8 μm, 10 μm, 15 μm and 20 μm. Defined by dry etching with BCl_3, the mesas ensure lateral current and optical confinement.

On-wafer measurements by the team revealed lasing at 417.7 nm, just a 0.1 percent deviation from the target of 418 nm. The variant with an 8 μm-diameter aperture produced the most powerful emission, peaking at 13.1 mW, three times higher than the team's previous best. For wall-plug efficiency, the design with the 5 μm-diameter aperture delivered the most impressive performance, with efficiency peaking at 21.3 percent – realised at 8.44 mA, a drive current that produced an output power of almost 10 mW.

Takeuchi believes that packaging would improve device performance, but not by much. He and his colleagues are now trying to increase the wall-plug efficiency to around 40 percent.

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➤ R. Watanabe *et al*. Appl. Phys. Lett. **124** 131107 (2024)

Realising a low contact resistance on N-polar GaN

Surface reaction between liquid-phase gallium and nitrogen radicals promises to provide superior contacts for vertical GaN devices

A TEAM from Nagoya University and Ulvac is claiming to have developed a novel low-temperature process for producing ohmic contacts on N-polar GaN surfaces.

Forming an ohmic contact on these surfaces is far more challenging than it is on Ga-polar surfaces, present in the more mature forms of GaN transistor. However, a process for adding ohmic contacts to N-polar GaN surfaces is needed when producing vertical power devices, as well as N-polar HEMTs, a promising class of device for RF amplification.

To produce ohmic contacts on the more common Ga-polar surface, engineers grow heavily doped epitaxial layers of GaN on the topmost surface, before depositing metals and sintering and annealing them. But that's far from ideal for N-polar surfaces. During fabrication of vertical GaN-based devices, the substrate is ground and polished to trim thermal and electrical resistance, before attempting to add a low-resistance contact to this layer. For the last step, a temperature below 600°C is required to prevent processing from degrading device performance. This rules out: using MOCVD on *n*-type GaN on N-polar surfaces, as that requires temperatures in excess of 1,000°C, and ion-implantation, which involves activation annealing at temperatures beyond 1,000°C.

Offering a promising alternative is a sputtering-based approach employed by the team from Japan. According to spokesman Shinji Yamada from Nagoya University, their technique for forming GaN is unique, involving a surface reaction between liquid-phase gallium and nitrogen radicals.

Yamada is not the first to sputter GaN on N-polar surfaces, with success reported on that front last year by Hiroshi Fujioka's group from the University of Tokyo. Results from that team focused on crystallinity, carrier concentrations, mobilities, surface morphology and photoluminescence.

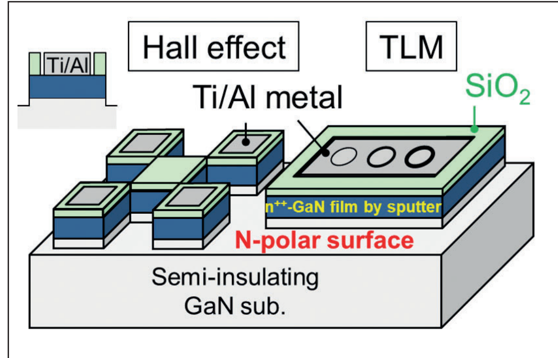
"On the other hand, our report focused on properties such as contact resistances, considering the contact formation process for GaN devices."

Yamada and co-workers formed heavily germanium-doped *n*-type GaN films on an N-polar GaN surface using radical-assisted reactive GaN sputtering. Liquid-phase gallium and a nitrogen radical gun were used as the sputtering sources, and a germanium target provided an *n*-type dopant. After reaching the substrate surface, the sputtered gallium and germanium particles, and the nitrogen radicals, undergo chemical reactions to form a GaN film.

To assess the quality of the GaN films produced by this process, the researchers took semi-insulating substrates produced by HVPE and thinned them to 50 μm by grinding and chemical mechanical polishing the N-polar surface. Cleaning with organic solvents and acid solutions followed, prior to the addition of GaN via sputtering, using a range of conditions.

For sputtering, the team varied the germanium-to-gallium sputtering ratio from 0 to 0.15 while maintaining a constant gallium sputtering power, and used substrate temperatures of 500 °C and 600 °C.

Following GaN growth, the team created structures for electrical measurements (see Figure) that featured a Ti/Al metal stack, deposited by an electron-beam evaporator. Sintering at 475°C under nitrogen gas for 5 minutes created an ohmic contact.



➤ To assess contact resistance, structures were produyced for Hall effect and transmission line measurements.

Transmission electron microscopy revealed that the GaN film sputtered at 600°C is epitaxial, while that deposited at 500°C is only epitaxial in most parts, and riddled with many defects, including stacking faults and inversion domains.

According to Hall-effect measurements on contacts formed at 500 °C, increasing the proportion of germanium to gallium increased the carrier concentration, with a sputtering ratio of 0.15 producing a concentration of 2.6 x 10^{20} cm^{-3}. The corresponding contact resistance is 9.4 x 10^{-5} Ω cm^2, a value indicting a low specific contact resistance. For contacts formed at 600°C, the researchers only considered a sputtering ratio of 0.11, which led to a carrier concentration of 1.8 x 10^{20} cm^{-3} and a contact resistance of 2.0 x 10^{-5} Ω cm^2.

Yamada and co-workers are now considering the application of heavily-doped *n*-type GaN films to a range of GaN devices.

REFERENCE
➤ S. Yamada *et al.* Appl. Phys. Express **17** 036501 (2024)

Ga_2O_3: Improving the gate dielectric

Annealed films of $HfSiO_x$ possess the critical attributes for forming a high-quality dielectric for β-Ga_2O_3 devices

TO UNLOCK their full potential, β-Ga_2O_3 Schottky barrier diodes and various forms of FET demand a high-quality dielectric.

Claiming to meet this need is a team of engineers from the US. These researchers have developed a process for forming $HfSiO_x$, an oxide that is said to combine a high dielectric constant with a large band offset, negligible gate leakage, a low density of interface and bulk traps, and a large breakdown field.

Crucially, the breakdown field for $HfSiO_x$ is as high as 8.7 MV/cm, significantly beyond the theoretical breakdown field for β-Ga_2O_3, of 8 MV/cm. By ensuring that the dielectric has a higher breakdown field than the device, the latter can realise its full potential.

Cr/Ti/Au
HfSiO 20 nm
HVPE n-Ga_2O_3 10 µm
(001) n^+ Ga_2O_3 640 µm
Ohmic (Ti/Au)

➤ Metal-oxide-semiconductor capacitors are used to determine the characteristics of the $HfSiO_x$ dielectric.

The process for producing a high-quality $HfSiO_x$ dielectric on β-Ga_2O_3 has been developed by a partnership between researchers at the University of Michigan, Union College, and the University of California, Los Angeles. This collaboration has built on its previous work, involving the development of an MOCVD process for producing an AlSiO dielectric on β-Ga_2O_3. That earlier work produced a dielectric with a breakdown field of around 7.8 MV cm^{-1}.

The increase in breakdown that has resulted from switching to $HfSiO_x$ involves a different deposition process. For the latest work, the dielectric is added by atomic layer deposition, prior to an annealing step that ensures significant improvements in important characteristics.

Interest in $HfSiO_x$ dates back many years, with previous studies considering its use as a dielectric for devices based on silicon and GaN. Prior work has also shown that by adjusting its composition, the dielectric constant for $HfSiO_x$ can range from 3.9 to 27, and the conduction band discontinuity between $HfSiO_x$ and β-Ga_2O_3 can be as high as 2.38 eV.

The engineers from the US used metal-oxide-semiconductor capacitors to investigate the performance of the $HfSiO_x$ dielectric on β-Ga_2O_3. They began with epiwafers featuring a 10 µm-thick layer of β-Ga_2O_3 grown on a heavily n-doped β-Ga_2O_3 substrate, and turned to atomic layer deposition to add a film of $HfSiO_x$, using a ratio of HfO_2 to SiO_2 of roughly 1:1. To realise this ratio, two cycles of HfO_2 with a deposition rate of 1 Å/cycle were alternated with three cycles of SiO_2, with a deposition rate of 1 Å/cycle.

To assess the impact of annealing, the team produced three types of capacitors with 20 nm-thick dielectrics (see figure). One class avoided any form of heat treatment, while the other two were annealed in nitrogen gas at temperatures of 400°C and 900°C.

Breakdown measurements determined that for the unannealed capacitors, low-leakage operation occurs at up to around 3 MV cm^{-1}. Meanwhile, for those annealed at 400°C and 900°C, leakage is not seen until 6.2 MV cm^{-1} and 4.5 MV cm^{-1}, and breakdown fields are as high as 8.4 MV cm^{-1} and 8.7 MV cm^{-1}, respectively.

Capacitance-voltage measurements, using a deep-UV lamp emitting at 254 nm to provide sufficient hole generation, offered an insight into the level of traps within the dielectric.

Profiles of the unannealed capacitors showed that they fail to reach the accumulation region at low electric fields. The team attributes this observation to an exceptionally high electron-trap-density, both in bulk $HfSiO_x$ and at its interface with β-Ga_2O_3.

Capacitance-voltage measurements determined the total trap densities for both annealed samples. The team reported average values of 2.72×10^{12} cm^{-2} eV^{-1} and 1.06×10^{12} cm^{-2} eV^{-1} for samples annealed at 400°C and 900°C, respectively, indicating that a higher temperature trims the trap density. This led the team to speculate that annealing at 900°C in an ambient environment reduces oxygen vacancies in $HfSiO_x$ and reduces the density of bulk and interface traps.

The engineers have scrutinised their dielectrics with cross-sectional scanning transmission electron microscopy. This technique uncovered partial ordering in the deposited $HfSiO_x$, with annealing at 900°C creating a fully amorphous dielectric that is behind the reduced leakage current and increased breakdown voltage.

REFERENCE

➤ X. Zhai. *et al*. Appl. Phys. Lett **124** 132103 (2024)

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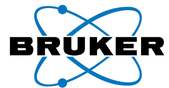

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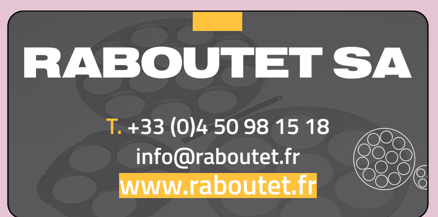

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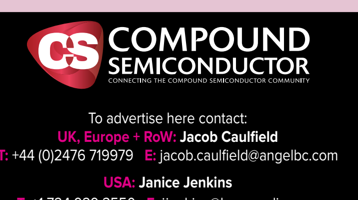

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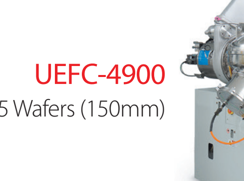

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