COMPOUND SEMICONDUCTOR

Connecting the Compound Semiconductor Community

Volume 23 Issue 8 November/December 2017 @compoundsemi www.compoundsemiconductor.net

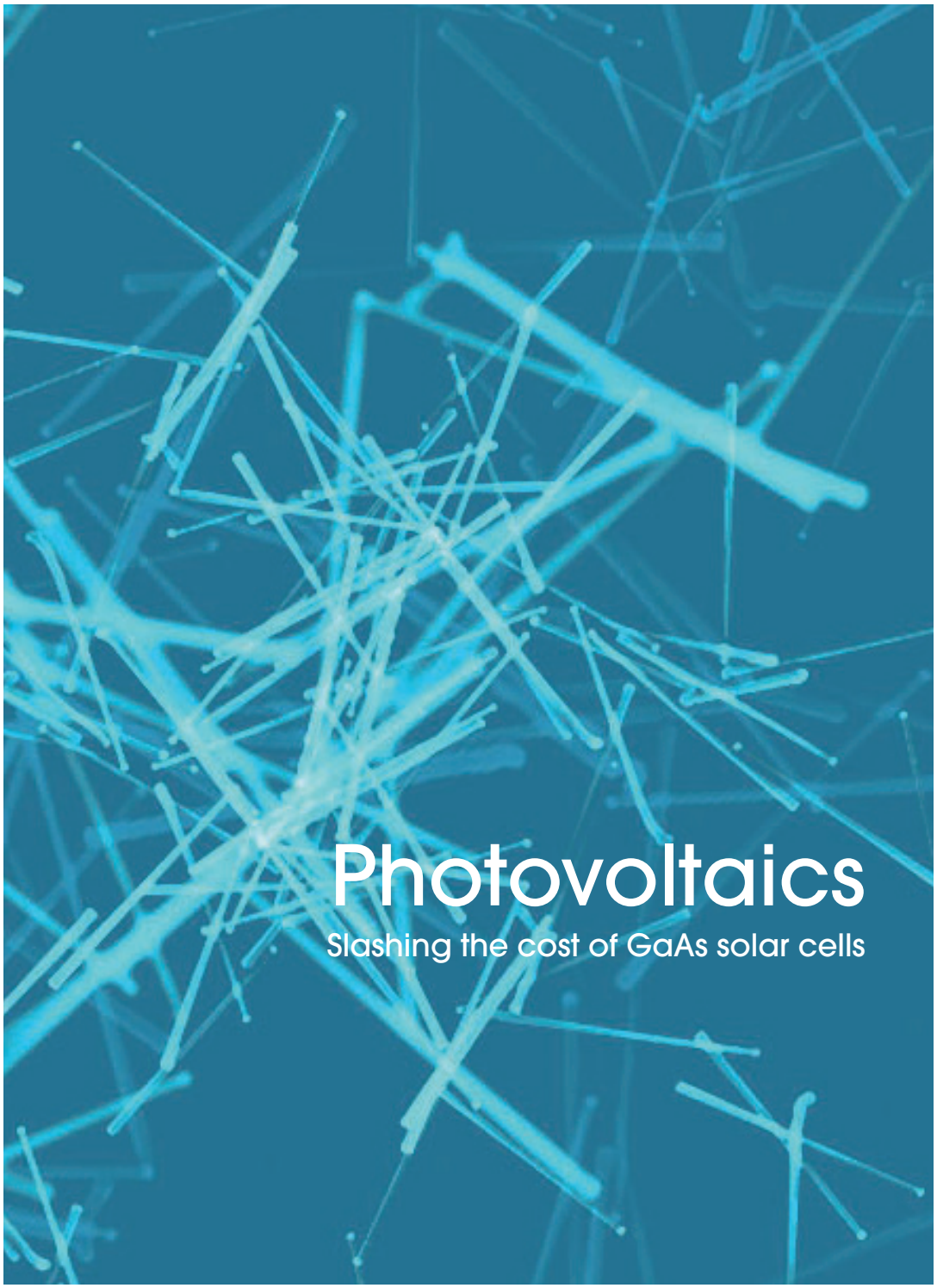
Antimonide LEDs target gas sensing applications

Is there now a watertight theory for LED droop?

5G phones: providing the key ingredients

Accelerating production ramps for CS chipmakers

Amec shatters Aixtron and Veeco dominance



Photovoltaics

Slashing the cost of GaAs solar cells

inside

News Review, News Analysis, Features, Research Review, and much more...
Free Weekly E News round up go to: www.compoundsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

AIXTRON

Our technology. Your future.

YOU THINK,

GLOBAL MEGA TRENDS REQUIRE BEST PERFORMANCE III-V MATERIALS

WE THINK THAT TOO.

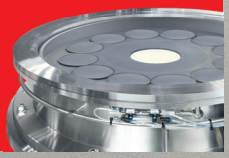
THE AIX 2800G4-TM

3D-SENSING
AUGMENTED REALITY
AUTONOMOUS DRIVING
CLOUD COMPUTING
INTERNET OF THINGS/5G
NEXT GENERATION DISPLAYS

DISCOVER THE AIX 2800G4-TM.

Tool of Record for all AsP-based materials for next generation applications.

Market leading technology delivering best yield combined with highest productivity in the industry.



AIXTRON SE
info@aixtron.com · www.aixtron.com

Viewpoint

By Dr Richard Stevenson, Editor

Cost-competitive GaAs solar cells?

IT IS NO SECRET that the great success of the silicon cell is down to its low cost. But it is not strong on all fronts, converting only around one-fifth of the energy that impinges upon it into electrical power.

One option for increasing the efficiency of the silicon cell is to cover it with several microns of gallium arsenide. This creates a second junction, improves the conversion of light into energy, and can deliver a hike in cell efficiency of more than ten percentage points.

But is this approach economically viable? Certainly not, according to Frank Dimroth from the Fraunhofer Institute for Solar Energy Systems. In a talk he gave at CS International 2016, he reasoned that the costs associated with epitaxy, substrate preparation and waste treatment of materials would need to plummet by a factor of about one hundred before this technology could become a serious contender for terrestrial PV.

So can we rule out the prospects for roofs filled with tandem cells, formed from GaAs epilayers on silicon? No: it is just that the cost associated with GaAs needs to plummet, due to the introduction of a radically different approach.

Pioneering a technology that could succeed is Swedish start-up Sol Volatics. It has a novel, low-cost deposition process, based on the efforts of Lars Sameulson's group at Lund University, that allows the continuous production of aligned nanowires. Thanks to photonic effects, these nanowires produce an efficient structure with just 20 percent of the material required for a thin-film.

Sol Volatics' technology is clearly impressing investors. It has helped the company to raise a total of $58 million at a time when alternative forms of PV have had a very bad reputation.

The funding is now being used to optimise the growth process, with a focus on increasing the up-time of reactors and reducing costs.

One goal for the end of 2018 is to deliver the first samples to customers. What happens after that, though, is not yet clear. When interviewed, SolVoltaics' CEO Erik Smith would not elaborate on business plans (see p.22), but they could include a ramping of production and various licensing deals.

However, whichever way he and his team choses to go, it is great to hear that gallium arsenide could still have a role to play in generating electricity for our homes and offices.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Sales Executive Jessica Harrison jessica.harrison@angelbc.com +44 (0)2476 718209
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Executive Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970
Directors Bill Dunlop Uprichard – EC, Stephen Whitehurst – CEO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway

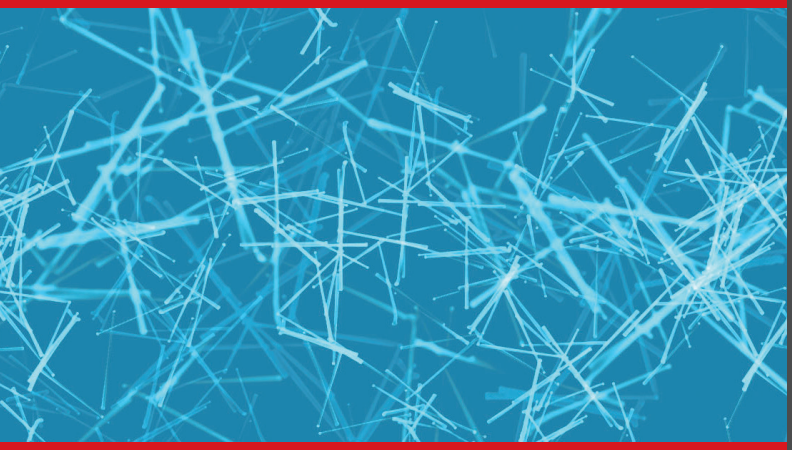
Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 E: ask@angelbc.com

Accounts & Multi Media Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 E: info@angelbc.com

Volume 23 ISSUE 8 NOVEMBER / DECEMBER 2017

CONTENTS

COVER STORY



news

news analysis

research review

Osram's new LED chip factory goes into operation

OSRAM'S new LED chip factory in Kulim, Malaysia, begins operation on time. "Given our enormous recent growth rates of 19 percent in the LED business, we are pleased to have the new production capacities. Our investment in Kulim also attests to the technology shift and our transition to becoming a high-tech corporation: At the beginning of this decade, conventional lighting still accounted for 80 percent of Osram's business. Today, two-thirds of our sales are based on optical semiconductors," said Olaf Berlien, CEO of Osram Licht AG at the opening ceremony.

In November 2015, as part of its Diamond innovation and growth initiative, Osram announced plans to build the new LED chip factory in Kulim and to have it up and running by the end of 2017. The modular, expandable factory has now been put into operation just two years after the announcement one and a half year after groundbreaking. A total of €370 million were invested in the first stage of completion. Osram can expand the factory in two additional stages, entailing total investment costs of up to one billion euros including expansion of the LED assembly capacities in Osram's global factory alliance.

Aldo Kamper, CEO of Osram Opto Semiconductors business unit, underscores the enormous production capacity in Kulim: "With one week's production we could completely retrofit the street lighting of the metropolises New York, Rio, Hong Kong and Berlin with LEDs." To upgrade the entire street lighting worldwide, Kulim would have to produce LEDs five and a half years long exclusively for this purpose. Energy savings of up to 80 percent, compared to conventional street lights, can be achieved with LED lighting.

In addition, LED has better light colour stability and can be more quickly dimmed and adjusted, so that empty streets or sidewalks do not always have to be illuminated with full brightness.
The Osram factory in Kulim will produce blue LED chips which, by means of a converter layer, can generate white light. They are produced for general lighting purposes, such as the previously mentioned public street lighting, but also for façade lighting, private and commercial interior and exterior lighting, or for billboards – as well as for special applications such as horticulture lights.

The global LED market for general lighting is estimated to be €6 billion in 2018, roughly six percent of which is for street lighting. An average growth rate in the market of seven percent per annum is foreseen through 2020. The overall market for optoelectronic components – including general lighting – will be €17.5 billion in 2018.

The plan is to also produce LED chips in Kulim in the medium term for premium applications, such as automotive lighting and video projection. Thanks to the new facility at a green-field location, no compromises had to be made in the design of the factory, in addition it features the latest technology. In comparison with the 4-inch technology, the production systems for 6-inch wafers produce 125 percent more LED chips per wafer in a single cycle.

Osram is currently investing worldwide in the expansion of the existing six sites in its LED production network. Therefore, Osram is also expanding its plant in Regensburg, which currently has about 2,500 employees, and will additionally hire up to 1,000 employees. Premium LED chips and laser diodes, which are used, for example, in high-quality car headlights, will be manufactured there as well as infrared diodes for sensors that can be used in applications including facial recognition in mobile phones, or in cars for intelligent assistance systems (such as proximity control). Furthermore, Osram will be expanding its site in Schwabmünchen. In the future, Osram will manufacture LED primary materials in clean rooms there. In addition, Osram also has another plant for LED primary products in the U.S. city of Exeter. In Wuxi, China, Osram is expanding its capacity for assembling LED chips into complete LEDs – i.e. light-emitting diodes with a housing and partly with primary optics too. In Penang, Malaysia, located near Kulim, LED chips are also manufactured and assembled.

Leti to coordinate EU electric drivetrain project

LETI, a French research institute of CEA Tech, has announced a new European Horizon 2020 project to develop innovative electric drivetrains for third-generation electric vehicles.

Bringing together ten European research institutes, key members of the automotive-industry value chain and universities, the three-year, €7.2 million ModulED project will focus on boosting drivetrain performance to meet vehicle-owner requirements, making manufacturing more efficient and reducing environmental impact and vehicle cost.

Wide bandgap semiconductors central to €7.2 million Horizon 2020 ModulED project

The project team will use recent innovations from diverse industries. These include integrating the frequency, voltage and high-temperature benefits of wide-bandgap semiconductors fabricated with GaN. These devices allow the electronic circuitry that changes direct current to alternating current (DC-AC) to be integrated directly into the motor.

Other recent innovations the project will develop for the new drivetrains include processes for manufacturing magnetic materials for the magnetic part of the motor, lowering the density of the rare-earth element; motor architecture that allows modularity in production; transmission and cooling systems that are compatible with hybrid vehicles; and optimisation of braking systems to recover energy in the braking phase. "Electric vehicles are a key component of the EU's commitment to limit climate change, but current electric vehicles face challenges preventing large market acceptance, including consumer resistance due to cost and limited driving ranges," said Bernard Strée, project coordinator at Leti.

"ModulED will target these challenges via the manufacturing process, including the mass-production context, increased value-chain involvement and lifecycle analysis for optimised duration and minimised environmental impact."

Coordinated by Leti, the project includes the companies BRUSA Elektronik AG (Switzerland), Punch Powertrain NV (Belgium), ZG GmbH (Germany), Siemens (France), Efficient Innovation (France); universities RTWH Aachen University, Chalmers University and Eindhoven University of Technology, and Leti's sister institute, Liten.

Veeco injunction against SGL remains

VEECO INSTRUMENTS has announced that the US District Court for the Eastern District of New York has denied SGL Carbon (SGL) motion to suspend the November 2, 2017 preliminary injunction issued by the court prohibiting SGL's sale of wafer carriers for use in MOCVD systems made by Advanced Micro-Fabrication Equipment (AMEC).

SGL had filed a motion requesting that the court suspend, or 'stay' the preliminary injunction pending a forthcoming appeal by SGL to the US Court of Appeals for the Federal Circuit (CAFC).

"We are pleased that the court confirmed its prior ruling and denied SGL's request to stay the injunction," said John R. Peeler, chairman and CEO of Veeco. "We are confident that we will prevail before the appellate court in any appeal by SGL, and will continue to take steps in the US and abroad to enforce Veeco's IP rights."

The court's order means that the preliminary injunction, which prohibits SGL from shipping wafer carriers using Veeco's patented technology, will remain in place during the appeal by SGL. The appeal process at the CAFC usually takes over a year to complete.

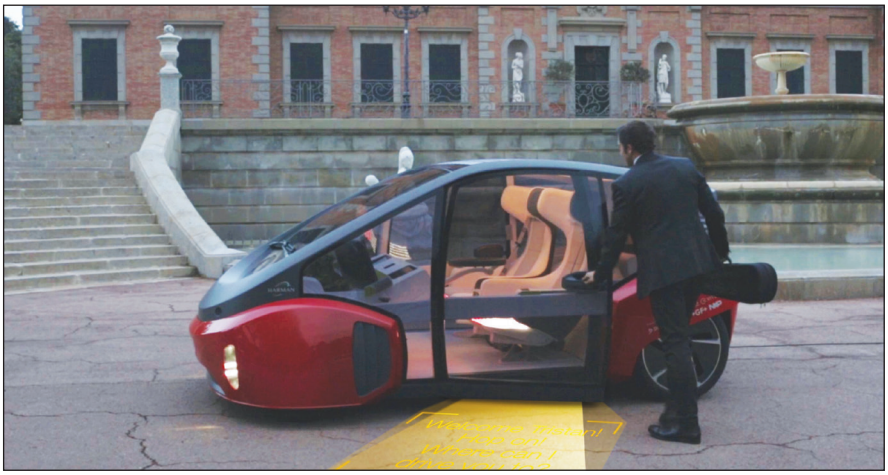
In its appeal, SGL will bear the burden of convincing the CAFC that the preliminary injunction should be overturned. Appeals of preliminary injunctions are evaluated by the CAFC under the highly deferential "abuse of discretion" standard of review. As a result, Veeco believes that it is highly unlikely that the CAFC will overturn the preliminary injunction, especially in light of statistics showing that a substantial majority of preliminary injunctions are affirmed by the CAFC on appeal.

This action for patent infringement was commenced by Veeco against SGL Carbon, LLC and SGL Carbon SE on April 12, 2017 in the federal court for the Eastern District of New York.

SGL manufactures wafer carriers which are used in susceptorless MOCVD systems. In addition to the preliminary injunction, Veeco is seeking a post-trial permanent injunction, monetary damages and other relief.

Osram and Continental plan automotive lighting venture

GERMAN LIGHTING firm Osram and Continental, a US vehicle technology company, have announced their intention to establish a joint venture. The idea is to combine innovative lighting technology with electronics and software to develop, manufacture and market intelligent lighting solutions for the automotive industry.



50:50 venture will combine lighting technology with electronics and software to develop intelligent lighting solutions for the automotive industry.

The global joint venture will operate under the name Osram Continental GmbH and have its registered office in the Munich region. Osram and Continental will each have a 50 percent stake in the joint venture. The aim is to generate annual sales in the mid-triple-digit-million-euro range with a workforce of around 1,500 employees and 17 locations worldwide. Dirk Linzmeier (CEO) from Osram and Harald Renner (CFO) from Continental have been named as designated managing directors. The joint venture is scheduled to start in 2018 subject to final agreement on the binding contracts and antitrust approvals.

Osram will be transferring its automotive Solid State Lighting (SSL) module business over to the joint venture. Continental will be incorporating its light control business from the Body & Security business unit. This will lead Osram Continental to combine semiconductor-based lighting modules, advanced electronics, optics and software expertise with access to sensor technology and innovative light sources. Osram Continental will therefore be able to offer a broad range of end-to-end, innovative lighting solutions, designed especially for headlight and tail light applications. The intention is to work together to design perfectly coordinated and innovative products and solutions, and bring them to market more quickly.

The joint venture will operate on the market as a standalone company. "The joint venture is a sign that Osram is focusing its efforts consistently on digitalisation. Continental's expertise in software and electronics is the perfect complement to our technology leadership in automotive lighting. It will create a forward-looking company for digital automotive lighting," said Stefan Kampmann, CTO of the Osram Licht AG. "The pace of innovation in the automotive industry lighting segment is rapid, and software is strengthening this dynamic," explained Helmut Matschi, member of the Continental Executive Board.

"While conventional lighting expertise remains important to our customers, the addition of electronics to enable new light functions is taking on increased significance. The joint venture will systematically combine these two areas and raise them to a new level."
The automotive industry lighting market is in the grip of technological change. Similar to the situation with general lighting, this market is moving toward semiconductor-based lighting solutions.

Thanks to increasingly intelligent light functions in vehicles as well as new light-based design and application options, semiconductor-based technology, software and electronics are gaining progressively in importance. Each year, growth in the market for semiconductor-based front lighting solutions is somewhere in the double-digit range. Market studies indicate that by as early as 2025 more than half of new cars worldwide could be fitted with semiconductor-based lighting solutions.

"Intelligent lighting solutions allow vehicle manufacturers a greater degree of flexibility when it comes to design, and help them to optimize development costs," commented Andreas Wolf, head of Continental´s Body & Security business unit. "The global presence of the Osram Continental joint venture is allowing us to cooperate closely with our customers in order to develop solutions exactly tailored to their needs. In the case of Continental and Osram, we have two technology companies combining their complementary expertise in the context of a joint venture to offer customers a unique range of solutions," added Wolf. "Digitalization is bringing about new potential applications in automotive lighting and hence tremendous opportunities that we want to take advantage of with Continental. Thanks to our combined offering of lighting and electronics solutions, we will be able to offer automotive sector customers cutting-edge products from a single source," explained Hans-Joachim Schwabe, CEO of Osram's Specialty Lighting business unit.

"By joining forces, we will be in an even better position to drive forward innovations by working closely with the automotive industry to integrate lighting, sensor technology and electronics seamlessly in a single application. This will allow us to drive forward new intelligent light functions, such as the combination of lighting and sensor technology in a module or light-based communication between the driver, other road users and the vehicle surroundings," added Schwabe.

LED light bulb prices continue to slide

LEDinside, a division of TrendForce, reports that the global average selling price (ASP) of LED light bulbs continued its slide in October. Compared with September, the ASP of 40 W equivalent LED light bulbs fell by 1.7 percent to $6.20. The 60 W equivalent counterparts also saw a 1.7 percent decrease in their ASP to $7.40.

"Some brand vendors of LED light bulbs have decided to lower their prices at the start of this fourth quarter for the purpose of boosting their sales," said LEDinside analyst Allen Yu. "Consequently, the worldwide price trend continued to move downward during October."

Prices of LED components were stable in October as package suppliers introduce new products. Prices were generally stable in China's LED package market in October. Compared with August and September, October was a period of recovery for the LED chip and component sections of the supply chain. Inventories for chip suppliers rose, but this was within the normal range and prices remained steady. The package market in turn did not experience noticeable price fluctuations. Also, some package suppliers have released new products in October. In the mid-power segment, Lumileds launched the Luxeon Stylist Series for lighting in fashion retail stores, supermarkets and restaurants.

The FreshFocus Technology, which is featured in 2835 and 3014 LEDs of the Luxeon Styles Series, offers wider colour gamut and better light quality. In the high-power segment, Honglitronic has recently

unveiled more advanced solutions under the AT Series, such as AT50 and AT70. According to Honglitronic, the AT Series has an anti-vulcanization technology that increases the reliability and lifespan of LEDs. Other major international LED suppliers including Cree and SSC have also released new products that seek to achieve greater brightness, more compact form and higher colour rendering index.

RF GaAs device revenue surpasses $7.5 billion

STRATEGY ANALYTICS reports revenue for RF GaAs devices increased by slightly less than 1 percent in 2016. An anticipated drop in cellular revenue nearly offset gains in other market segments, but GaAs device revenue still managed to surpass $7.5 billion for the first time.

"RF GaAs Device Forecast and Outlook: 2016 – 2021" from Strategy Analytics' Advanced Semiconductor Applications (ASA) service, forecasts that gigabit LTE and emerging 5G applications will drive GaAs device revenue past $9 billion in 2021.

"The RF GaAs device market is so dependent on cellular terminals that declining growth rates in smartphone sales has put the brakes on total revenue growth," commented Eric Higham, director of the Advanced Semiconductor Applications (ASA) service.

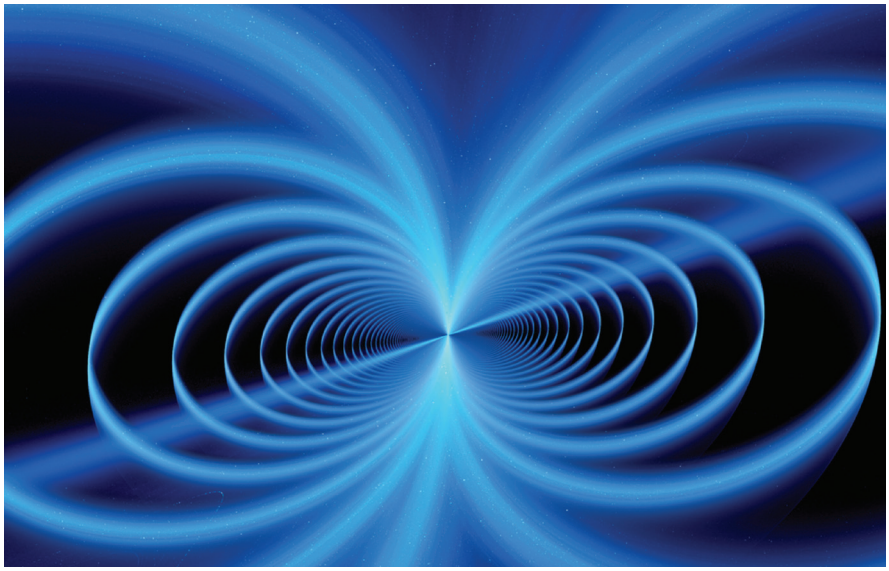
"The good news for the industry is that growing adoption of gigabit LTE networks and devices, coupled with emerging 5G opportunities will restart the GaAs growth engine. We are seeing new platforms and major program upgrades starting to ramp toward production and these developments will maintain the growth of GaAs device revenue in the defence sector," noted Asif Anwar, director of the Advanced Defence Systems (ADS) service.

UK consortium to develop unique sensor technology

THE UK's Compound Semiconductor Centre (CSC) has been awarded a collaborative R&D project by InnovateUK.

The project called CS MAGIC: (Compound Semiconductor MAGnetic Integrated Circuits) will focus on the development of new ultra-sensitive magneto-sensors with integrated electronics. It will use technology based on GaAs Quantum Well Hall Effect (QWHE) magnetic sensing technology developed by Mohamed Missous, founder of Advanced Hall Sensors Ltd (AHS), and a novel GaN device based on a high electron mobility transistor (magHEMT) concept developed by Petar Igic at Swansea University.

The consortium comprising CSC (Cardiff), AHS ltd (Manchester), TWI (Port Talbot), Renishaw (Edinburgh) and Swansea University will collaborate to deliver commercial grade sensing solutions for a diverse range of challenging applications in automotive current sensing, high resolution metrology, non-destructive inspection and test, and security screening applications. Missous, inventor of the QWHE technology, commented:



CS MAGIC project will use technology based on GaAs Quantum Well Hall Effect (QWHE) magnetic sensing technology and a novel GaN HEMT

"AHS has had considerable success in commercialising the core technology with over 15 million discrete sensors shipped to date, and this project will extend the functionality of sensing platform for harsh environment and ultra-wide dynamic range requirements to service a $3 billion market in magnetic sensing solutions'.

CSC Director, Wyn Meredith commented: 'This project will deliver an 'all UK' developed and manufactured solution which leverages world class compound semiconductor materials and device expertise in the consortium matched with the deep applications understanding of TWI and Renishaw'.

IDT introduces SiC humidity sensors

Integrated Device Technology (IDT) has announced the addition of family of SiC-based relative humidity (RH) sensor chips to its portfolio of advanced sensor products.

The IDT HS300x family of relative humidity sensors feature a ±1.5 percent RH accuracy and six-second response time (rated over a 20 percent to 80 percent RH range in still air and does not require airflow). Since humidity sensors consume the most power when they are taking a measurement, the fast response time to a stable measurement reduces the amount of sampling needed. This is especially important for battery-powered applications, where lower power consumption equates to longer battery life.

In addition to high-accuracy and fast response times, the HS300x family features excellent long-term stability of 0.1 percent RH per year as a result of a robust SiC construction and an innovative design. This improves useful lifetime and lowers its effective cost. IDT's humidity sensors are suitable for a wide range of applications, including measurement of water vapour content in medical oxygen, measurement of humidity in appliances such as refrigerators, as well as monitoring the humidity of air in industrial processes, climate control systems (HVAC), weather stations, and portable personal health devices.

"We're excited to add high-performance humidity sensors to our portfolio of industry-leading sensor products," said Sailesh Chittipeddi, executive vice president global operations and chief technology officer at IDT. "IDT's humidity sensors can be used alone or integrated with IDT's gas and flow sensors to provide a complete environmental sensing solution. These products each provide a compelling value proposition that, when coupled with IDT's long-standing reputation for quality and support, make IDT's products the preferred solution for many industrial, medical, and automotive applications."

The HS300x family consists of four devices – the HS3001, HS3002, HS3003, and HS3004 offering RH measurement accuracy of ±1.5 percent, ±1.8 percent, ±2.8 percent and ±3.8 percent, respectively. All devices feature an extremely low 1uA quiescent current for additional power savings, and an extra wide 5 percent to 95 percent sensing range for more precise control at the humidity extremes. The devices are offered in a compact 3.0 × 2.4 × 0.8 mm LGA package. The HS300x devices and evaluation boards are available now.

SEMICON® JAPAN

DREAMS START HERE

CONNECT | COLLABORATE | INNOVATE

The Premier Exhibition for
the Electronics Manufacturing Supply Chain in Japan

December 13 – 15 | Tokyo Big Sight, Tokyo, Japan

Co-located with

WORLD OF IOT

Organized by

semi™

Register Now ▶▶▶ www.semiconjapan.org

Chengdu HiWafer chooses SPTS platform for GaN line

SPTS TECHNOLOGIES, an Orbotech company and supplier of wafer processing solutions, has won an order for its Omega plasma etch system from Chengdu HiWafer Semiconductor Co., Ltd (HiWafer), China's first pure-wafer foundry, to establish their new 6 inch GaN on SiC production line.

SPTS's Synapse and ICP process modules on an Omega c2L platform will etch SiC backside vias (BSV) and GaN epitaxial layers to manufacture high power RF devices. The high rate Omega system was selected over the competition because the Synapse provided superior SiC etch rates while the ICP module delivered improved selectivity for GaN etch.

"HiWafer is already a well-established Chinese foundry producer of GaAs based pHEMT and HBT RF devices currently used in 4G communication, and they are an early adopter of SiC and GaN materials for use in high-end RF devices that target the worldwide 5G protocol," stated Kevin Crofton, president of SPTS Technologies and corporate executive VP at Orbotech.

He added: "This leadership position is important as Power and RF applications are high on the 'Made in China 2025' agenda for promoting domestic production of semiconductor devices, and companies like HiWafer are well-positioned to contribute to realising this national initiative. Our leadership in high rate etching of SiC and other dielectric materials will support HiWafer to provide manufacturing solutions for the coming 5G wave."

Nengwu Gao, general manager of HiWafer, stated: "Orbotech's SPTS Technologies is a recognised leader in compound wafer processing solutions to the global power and RF device industries. The addition of SPTS's Omega plasma etch system gives us the tools to compete in GaN on SiC RF technology in telecoms and transportation applications, including railway systems.

Acquiring this capability enables us to explore new applications and supports our ambitions to become a highly profitable and successful semiconductor foundry."

Chinese pure-wafer foundry selects Omega plasma etch solution for production of high power RF devices

GaN device market to reach $22.47 billion by 2023

The GaN semiconductor device market is expected to reach $22.47 billion by 2023 from $16.50 billion in 2016, at a CAGR of 4.6 percent between 2017 and 2023, according to a new report from Research and Markets.

The major factors driving the growth of the GaN semiconductor device industry include the vast addressable market for GaN in consumer electronics and automotive, wide bandgap property of GaN material encouraging innovative applications, success of GaN in RF power electronics, and increasing adoption of GaN RF semiconductor device in military, defence and aerospace applications.

However, the preference of SiC in high-voltage power semiconductor devices is expected to be a potential restraint for the overall GaN semiconductor devices market. This is expected to limit the market growth over the next few years. Optoelectronic devices held the largest market share in 2016. This is attributed to its wide application in consumer and enterprise, industrial, and automotive industry. GaN LEDs are widely used in laptop and notebook display, mobile display, projectors, televisions and monitor, signs and large displays, etc.

The use of GaN-based LEDs for the interior and exterior lightings such as headlights and signal lights, car interior lighting, fog lights, stop lights, and dome lights in the automotive industry has also contributed to the larger market size.

The market for GaN-based power drives is expected to grow significantly during the forecast period attributed to its superior features such as minimum power loss, high-speed switching miniaturization, and high breakdown voltage as compared with the silicon-based power devices.

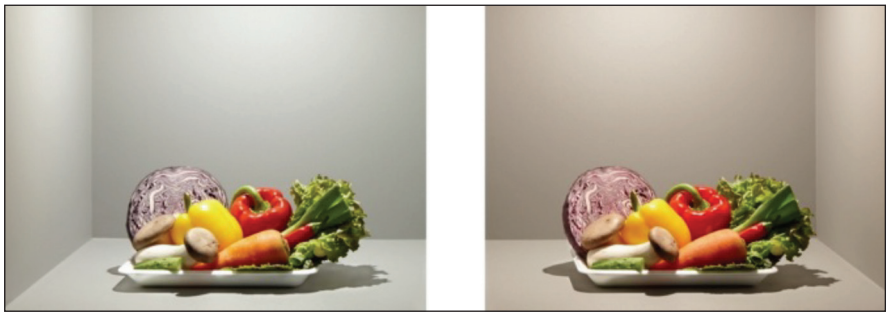
Also, the large total addressable market such as power distribution systems, industrial systems, heavy electrical systems, turbines, heavy machinery, advanced industrial control systems, and electromechanical computing/computer systems; and is also inclusive of several new power applications (clean-tech) such as high-voltage direct current (HVDC), smart grid power systems, wind turbines, wind power systems, solar power systems, and electric and hybrid electric vehicles are among the prime reasons for its faster growth.

APAC held the largest market share in 2016 is expected to hold the largest share of the GaN semiconductor device market during the forecast period. This is attributed to the increasing demand for LEDs in various industries such as consumer and enterprise, industrial, and automotive.

Further, EV charging, and electric vehicle production markets, and increasing renewable energy generation are driving the market in APAC.

Samsung introduces colour-optimised chip-on-board LEDs

SAMSUNG ELECTRONICS has announced a new family of chip-on-board LED lighting packages, called the 'Samsung D-series Special Color'. The packages are engineered to bring out the most desirable colour tones of objects whose viewing is particularly colour-sensitive, making them optimal for many commercial lighting applications.



New colour packages are engineered to bring out the most desirable colour tones of illuminated objects (see picture on the right)

Through spectrum engineering, colour spectrums within the D-series have been tuned to deliver high colour vividness, without the use of harmful ultraviolet (UV) lighting chips. The packages deliver a TM-30 Gamut Index (R_g) of over 110, a level that ensures lighting with outstanding colour and whiteness.

Today, to provide almost as vivid colour, many LED lamps instead use 'near-UV' chips, which can damage the human eye and clothing after repeated exposure. Near-UV rays can display vivid colours, but only when the whites in the object being illuminated contain fluorescent brightening agents. An alternative is to use expensive ceramic discharge metal-halide (CDM) lamps that do not last nearly as long. As colour has a significant influence on consumer purchase decisions, the new D-series now offers lighting options for three of the most important segments of commercial goods: fashion (stylish clothing), meat and vegetables.

The LED packages for each segment have been designed with the most effective combination of phosphors to illuminate what is being sold in the most appealing way. To determine the most attractive colour rendering and saturation levels based on subjective perceptions, Samsung ran extensive preference tests among many demographic groups worldwide. "Our new 'D-series Special Color' brings much greater value to the commercial lighting industry, reaching far beyond the ordinary image-rendering benefits of LEDs," said Jacob Tarn, executive vice president of the LED Business Team at Samsung Electronics. "We are determined to continue to be the leading innovator in LED component solutions that are not only outstanding in quality, but which also bring the most practical benefits to the ultimate user – consumers."

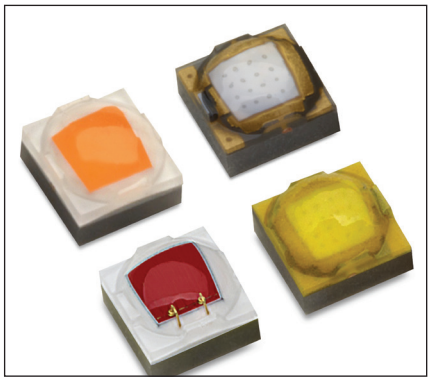
Packages generate from 13 W to 33 W to create the best combination of LEDs and phosphors for each commercial segment. Furthermore, they come in the same shapes and sizes as the standard Samsung D-series to simplify retrofitting of existing luminaires.

Lumileds upgrades colour LEDs

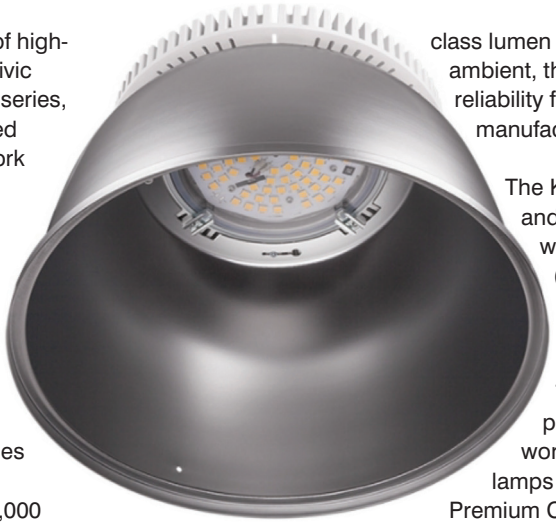
LUMILEDS says it has considerably improved the flux across its colour LED family. Performance improvements to the flagship Luxeon C Color Line includes 20 percent higher lumen output in its Luxeon C Green and Cyan compared to the previous generation; the Luxeon C Red-Orange features a 12 percent flux increase and the Luxeon C Red an 8 percent flux increase.

"As the demands on our customer's fixtures become more challenging, we need to ensure our colour portfolio enables them to meet these demands. This increase in flux across several key colors will give our customers a significant boost in performance in existing designs as well as allow them to start from a higher level of performance in new designs," said Jennifer Holland, product line director of the Luxeon C Color Line. Specifically engineered for colour mixing through its standard focal length, the Luxeon C Color Line is suited for use in architectural, stage lighting, emergency vehicle lighting, and colour tunable lamps and fixtures.

All Luxeon C Color Line LEDs are hot tested at 85°C. Its thermal resistance, claimed to the lowest in the industry at 2.8°C/W, also helps reduce heat sink cost - or allows LEDs to be driven harder for higher output than is achieved with a competitor's LEDs, according to Lumileds. Extending these performance upgrades to other lines within the Luxeon Color LED family, Lumileds has also announced 20 percent flux improvements for the Green and Cyan colours on Luxeon Z Color Line and Luxeon Rebel Color Line.



Cree launches new high-bay LED lighting



CREE has introduced a new range of high-bay LED lights for industrial, retail, civic and athletic venues. Called the KBL series, it is said to have dramatically reduced glare for a safer, more productive work environment.

The new high-bay is engineered to deliver maximum savings and industrial-strength performance with up to 150 lumens per watt (LPW) and a payback as fast as 1.5 years, according to Cree.

"Cree's new KBL LED High-Bay Series is the ideal solution for the high-bay market and delivers an average of 2,000 lumens more than the nearest competitor," said David Elien, Cree senior vice president, lighting. With best-in-class lumen maintenance in applications up to 50°C ambient, the KBL Series offers unprecedented reliability for the rigours of retail, industrial manufacturing and warehouse applications."

The KBL Series is available in 18,000 and 24,000 nominal lumen output options with correlated colour temperatures (CCTs) between 3000K and 5000K, and is virtually maintenance free with zero warm-up or restrike time.

The new series offers increased productivity and safety by minimising work stoppages and maintenance to replace lamps and ballasts, and is eligible for DLC Premium Certification to advance corporate sustainability goals.

Kyma demonstrates 200mm GaN-on-QST templates

KYMA TECHNOLOGIES, a developer of wide bandgap semiconductor materials technologies, has used its new K200 hydride vapour phase epitaxy (HVPE) growth tool to produce high quality 200mm diameter GaN on QST (Qromis Substrate Technology) templates.

This follows the company's announcement in 2016 of its demonstration of 150 mm diameter GaN on QST templates in partnership with Qromis (formerly Quora Technology) and its recent announcement of the commissioning of Kyma's K200 HVPE growth tool.

Pictured right, one of the demonstrated 200mm diameter HVPE GaN on QST templates which consists of 10 μm of HVPE GaN grown on a 5 μm MOCVD GaN on QST wafer provided by Qromis.X-ray diffraction rocking curve line-widths for the templates fall in the range of 250 and 330 arc-sec for the symmetric {002) and asymmetric {102} XRD peaks, respectively, which is consistent with high structural quality.

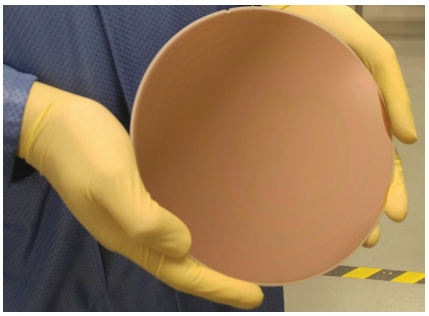
Low wafer bow (~50 μm) and smooth surface morphology suggest these materials should support high performance device manufacturing. Kyma's newly constructed K200 HVPE tool is said to represent a first for the industry and was designed by Kyma engineers to enable uniform and rapid growth of high quality GaN on a number of different substrates.

"We have successfully transferred the process for making high quality GaN to our K200 HVPE tool. The structural quality of the GaN produced on Qromis' QST substrate is excellent. We are currently engaging with customers interested in large diameter GaN on QST templates," said Keith Evans, Kyma's president and CEO.

Kyma and Qromis are partnered for this work under a Kyma-led US DOE Phase IIB SBIR with award number DE-SC0009653.

Qromis recently began manufacturing 200 mm QST substrates and GaN-on-QST wafers using its foundry partner Vanguard International Semiconductor (VIS). VIS is planning to offer GaN power device manufacturing services on 8-inch diameter QST platform in 2018.

Qromis co-founder and CEO Cem Basceri added: "Qromis' CMOS fab-friendly 200-mm diameter QST substrates and GaN-on-QST wafers represent a disruptive technology, enabling GaN



epitaxy from a few microns to hundreds of microns for GaN power applications from 100 V to 1,500 V or beyond GaN power devices, in lateral, quasi vertical or vertical forms, on the same 8-inch or 12-inch production platform at silicon power device cost.

Kyma's K200 HVPE technology represents an important value-add to QST-based GaN power device manufacturing by enabling the low cost deposition of a thicker and lower defect density GaN surface than is practically achievable using MOCVD growth alone."

Kyma is also teamed with a world-class semiconductor equipment OEM to manufacture K200 HVPE tools for customers who prefer to bring Kyma's leading HVPE GaN growth process in-house.

VCSEL HOME RUN FOR IQE

Is IQE ready to supply the wafers that will take VCSELs to mass market, asks Rebecca Pool.

JUST FIVE DAYS after the release of Apple's much-awaited iPhone 8, IQE revealed plans to make VCSELs a mass-market product by 2022.

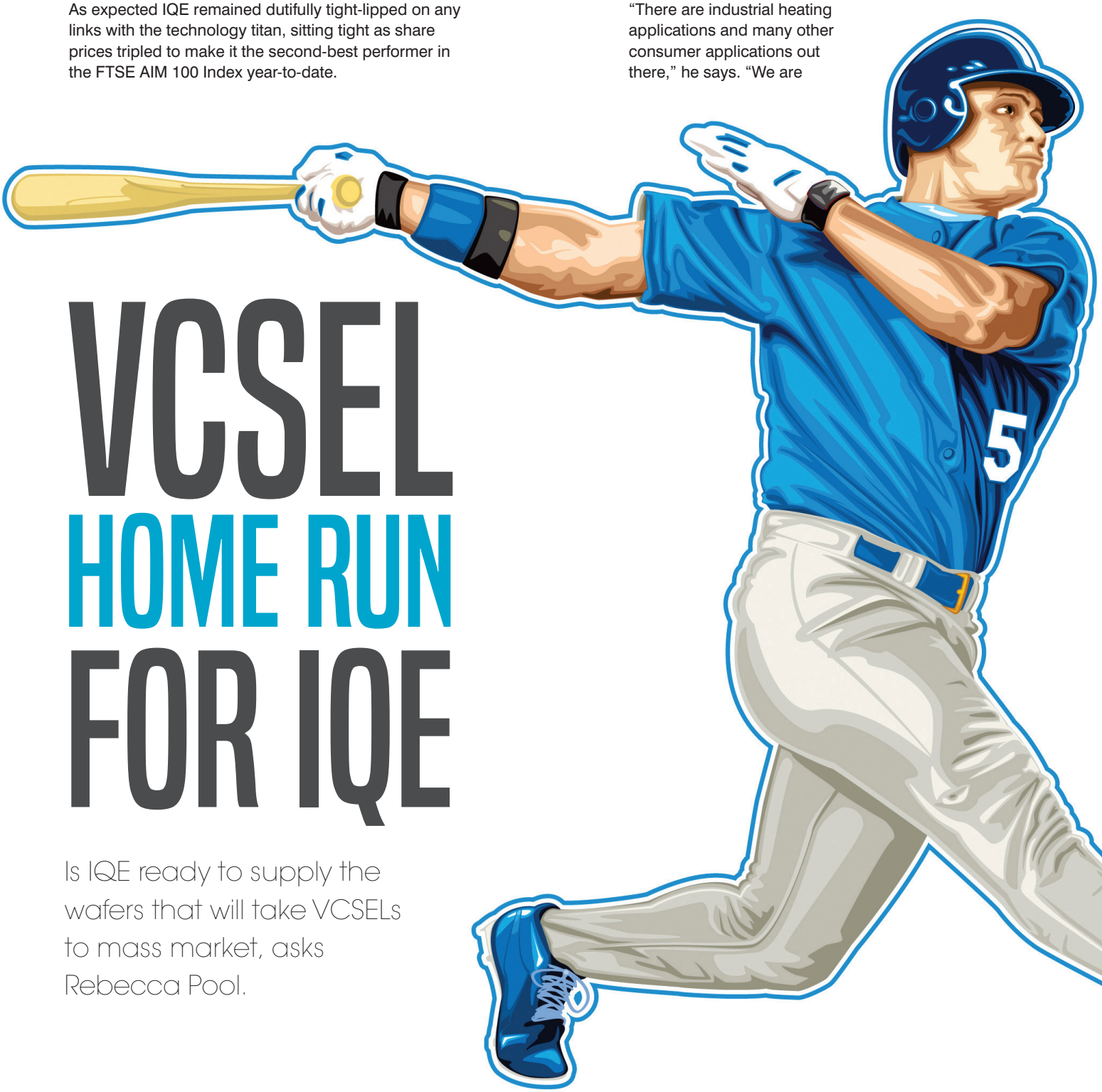
The announcement came amid widespread media reports that the Wales-based wafer manufacturer was at the heart of the all-important VCSEL-driven facial recognition in Apple's latest incarnation.

As expected IQE remained dutifully tight-lipped on any links with the technology titan, sitting tight as share prices tripled to make it the second-best performer in the FTSE AIM 100 Index year-to-date.

Iwan Davies, group technology director at IQE, is pragmatic about IQE's latest success.

His company's photonics sector has experienced 'extremely rapid growth' largely thanks to VCSEL wafer sales; he expects sensing to be the largest application for some time; yet he is clear that IQE will supply wafers into any mass market application.

"There are industrial heating applications and many other consumer applications out there," he says. "We are



ramping up production, have signed a lease on more manufacturing premises and are ordering new epitaxy tools."

"We expect rapid growth in this market and hopefully will be involved," he adds.

Modesty aside, Davies is very clear that IQE's VCSEL wafer success has been helped by the €23 million, EU-funded 'VIDaP' project.

In May 2014, 'VCSEL pilot line for IR Illumination, Datacom and Power applications' set out to establish a pan-European supply chain capability for high volume VCSEL production, targeting infrared illumination, data communications, gesture recognition and industrial heating applications.

Led by Philips Technologie, Germany, the consortium included: IQE; chip giant STMicroelectronics; packaging equipment manufacturer Sidel Blowing and Services of France; Germany-based industrial sensor maker Sick; Israeli computer networking business Mellanox Technologies; as well as Philips Electronics and the Technical University of Eindhoven, both from The Netherlands.

As Davies highlights: "At the time, we essentially had a very unstable process and had to employ experienced epitaxy engineers to oversee the process and use expertise to bring it up to a standard."

"This hands-on engineering monitoring process meant there could be a tendency to over-engineer the process, and we wanted to move away for this," he adds.

Fast-forward three years, and the project has established a fully automated production line for 4-inch GaAs wafers.

Manufacturing standards are said to match those of other high volume semiconductor processes. And Philips, which had been producing VCSELs on 3-inch wafers for many years, claims to have now produced more than 500 million devices in the last two years, up from 200 million across the previous decade. The company also claims to be ready to migrate to 6-inch wafer processes.

According to Davies, a key part of the project was understanding the dependence between IQE's epitaxy and device fabrication from Philips. Project researchers scrutinised materials characterisation data, such as luminescence and reflectance, alongside device performance parameters including output power, efficiency and emission wavelength. From here, they developed an *in-situ* monitoring process to better control epitaxy processes, while state-of-the-art *ex-situ* characterisation equipment was used to check wafer specifications, after epitaxy.

Crucially, come the end of the project, the original Aixtron G3 reactor had been replaced by a G4 reactor, doubling wafer throughput per production run.

As Davies points out, the robust statistical process control system was critical to mapping control charts, minimising process drift and increasing wafer yields. "Statistical process control, manufacturing execution systems and IT resources have all helped us to collect and compare data in a more statistical way, so we could move away from the hands-on engineering monitoring process," he emphasises.

As a result, the process now churns out the larger 4-inch wafers, more quickly, and in greater quantities per production.

Davies will not be drawn on absolute yield figures – simply stating yields are up by more than 25 percent – but emphasises the faster wafer processing speeds.

"The cycle time became a little shorter between runs as we gained more confidence in the stability of the process," he says. "So essentially we doubled wafer throughput in a run and also doubled the throughput per unit time."

"And given this is just after a year of running the new tools, we could have yet more wins, giving us an even higher throughput again," he adds.

Importantly project success comes just as industry analysts predict global VCSEL market revenues to mushroom from today's multi-million dollar levels to at least $1 billion in 2022.

A crucial part of the VIDaP project was to create mass market applications for VCSELs, and judging from the latest iPhone 8 developments, facial recognition in mobile phone handsets is a winner.

"Some of our end-user partners were extremely successful in using VCSELs; this is especially true in datacoms and 3D sensing applications," says Davies. "So we are ramping up production, have ordered five new Aixtron G4 reactors giving us fourteen [reactors], with our new site having the capacity for 100 such tools."

"The exploitation of VIDaP is clearly already there to be seen," he adds.

Building a barrier against **oxidation**

Does Finnish start-up, Comptek Solutions, have a novel answer to the age-old problem of oxidation in compound semiconductors? Rebecca Pool takes a look.

IN AN INDUSTRY DEVELOPMENT that could solve the thorny issue of oxidation in III-V compound semiconductors, Finland-based University of Turku spin-off Comptek Solutions has just won €450,000 to commercialise its novel surface treatment process.

Designed to passivate the epi-layer surfaces that quickly oxidise when exposed to air, the process boosts material quality and is set to raise power efficiencies in optoelectronic and RF devices.

During semiconductor device fabrication, oxidation at III-V epi-layer surfaces leaves an amorphous layer riddled with electrically active defects. Some manufacturers employ cleaning techniques, from controlled chemical etching to *in situ* ion sputtering, to better prepare the semiconductor surface for later processing, but many players simply live with the problem and the less-than-ideal device performances that ensue.

"Industry has been trying to solve this problem, without success, for many, many years," highlights Comptek chief executive, Vicente Calvo Alonso. "But our treatment process represents a breakthrough with customers saying they get improved device performance, for instance in HEMT applications, as well as an increase in the number of amplifiers per wafer."

Alonso and colleagues remain tight-lipped on detail, but describe 'Kontrox' as a passivation process

Comptek is now completing construction of its 40m² state-of-the-art laboratory.

based on novel atomic-level surface engineering that is fully compatible with MBE processes and can be implemented alongside other epitaxial methods.

Oxidised III-V surfaces are first cleaned, and then thermally oxidised in very precise conditions to produce a crystalline, almost defect-free, III-V oxide layer, ready for the next stages of fabrication. According to Alonso, the team has proven up to 98 percent reduction of defect state densities at technologically essential III-V dielectric interfaces.

Crucially, the improvement in crystal ordering at the surfaces as well as reduced defects enable manufacturers to narrow the gap between theoretical and practical device efficiencies. Meanwhile, better material homogeneity coupled with stability under air exposure boosts the manufacturing yields of subsequent processes.

"For example, side-wall passivation of III-Vs is a huge problem for laser manufacturers, especially as wafers are moved from one process step to the next, and we have seen no practical solution yet," points out Alonso. "But we have optoelectronics manufacturers that are now willing to work with us in different applications and I believe this will be a huge breakthrough for them."

Optoelectronics manufacturing aside, Comptek is also seeing interest from the manufacturers of GaAs-based PHEMTs for power amplifiers in RF applications. As Comptek's chief technology officer, Jouko Lång, highlights: "Manufacturers want to deposit insulator materials on top of the III-V barrier layers before gate deposition, making a more CMOS -type transistor structure called the MIS-HEMT. However, the insulator-III-V interface has been very poor so far and our process is a key enabler here," he adds. "Some of our customers have said they can gain up to 50 percent better transistor characteristics in their enhancement mode HEMTs when using our technology."

With its latest funds in tow, Comptek will complete construction of its 40m^2 state-of-the-art laboratory, which will house a cleanroom, custom ultra-high-vacuum reactors and characterisation equipment. According to Alonso, the reactors are designed to handle wafer sizes up to four inches and produce high quality III-V-based structures.

"A few industry players are already fabricating chips on six inch wafers but many applications are still based on two and three inch wafers," says Alonso. "With our four inch capability, we will be able to work quickly with the evolving industry."

According to the chief executive, Comptex hopes to license its technology to epi-manufacturers, foundries and integrated device manufacturers, so will first provide samples and then work with customers to implement its process into production lines.

Meet the team: CEO, Vicente Calvo Alonso (left), CTO, Jouko Långe (middle) and Johnny Dahl, chief of research, (right).

"For molecular beam epitaxy reactors, implementation is pretty straightforward; our process is compatible with MBE and we are already in discussions with equipment manufacturers to develop equipment together," he says.

Here, Comptek will develop an 'add-on module' that can be quickly implemented to MBE reactors to perform the passivation process. Meanwhile, the company also intends to develop standalone equipment for MOCVD reactors.

"MOCVD is the industry's biggest market and we will be working with customers here on a case-by-case basis," says Alonso. "For example, as part of one request, we are looking at developing standalone equipment with a specific oxide removal process plus an atomic layer deposition capability. Introducing new processes to [users of] MOCVD is going to take time, but I am convinced that once the benefits of our process are known, we will then be able to work with partners to speed up implementation," he adds.

Right now, Comptek's passivation process is compatible with the majority of III-V compound materials such as GaAs, InP, InAs, InSb and GaN. Customer sample production is the priority right now, but with good results already emerging, equipment development and implementation looks set to follow in the next year. And while the company currently comprises six employees, it is in the process of hiring and is already looking to its next round of venture capital funds.

"Industry has been trying to solve the oxidation problem for many years without success and our technology is giving very good results and interesting improvements," says Alonso. "We are already getting traction from industry and whenever we explain what we do, the interest is very big, which has to be a good sign."

China MOCVD players break Veeco-Aixtron dominance

All change for MOCVD market as Amec prepares to overtake Veeco in China equipment sales, reports Rebecca Pool.

AS THE DEMAND FOR LEDs continues to grow, Chinese vendors up and down the supply chain are scooping up the business.

In his latest IHS Markit Ranking, analyst Jamie Fox, highlights how Nationstar has become the second packaged LED maker from mainland China to break into the LED top ten revenue earners, following in the footsteps of MLS. But for the first time ever, China-based MOCVD players are also muscling in on the market.

As Fox points out, this year, MOCVD suppliers Amec and Topec have seen a sharp increase in sales and are the first companies to seriously challenge longstanding industry heavyweights, Germany-based Aixtron and Veeco, US.

"A couple of years ago Aixtron and Veeco had complete market dominance with more than 90 percent of the market between them," says Fox. "Many other companies had tried to compete and failed, but this year has seen a drastic change."

As the analyst highlights, while only last year Amec was a minor market player with few shipments relative to the big two, its actual shipments are now catching up with Veeco.

"Veeco will remain ahead across the entire year, but Amec could rival or even overtake Veeco in the second half of this year," says Fox.

"One to two years ago, Amec wasn't perceived as being ready for the market," he adds. "But the company has taken years to develop a good system and now appears to have done this and convinced customers as well."

Right now, Amec's revenue-recognised shipments of its Prismo A7MOCVD tool chambers are estimated to come in at between sixty and seventy units for 2017. But as Fox emphasises, total shipment figures, not just those based on received revenue, are significantly larger. Indeed, latest figures from the company indicate shipments have already reached 100 since the product's introduction last year, and this figure is set to rise to 120 by the end of this year.

And while Topec's figures, of five to ten units, are much lower than Amec's mighty numbers, Fox also anticipates growth from this China-based MOCVD supplier.

But what makes these results all the more important is that only China is seeing rocketing MOCVD demand.

"Nowhere else is seeing this MOCVD growth," highlights Fox. "Veeco and Aixtron still have shipments outside of mainland China – you have Epistar and Osram – but apart from these companies, hardly any other company is buying."

Fox also expects more of the same in the next few years. "I do think Epistar will have to add some capacity at some point, but the majority of the market is going to stay in China," he says. "We might see some of the Tier 1 companies such as Lumileds and Seoul Semiconductor adding a few units but it is most likely that sales outside of China will stay at the same fairly low levels."

Market reaction

So how exactly are industry players reacting to the rise of the China-based MOCVD suppliers? Fox reckons Aixtron, for one, is putting more effort into producing systems for materials other than GaN LEDs, including

power semiconductors and AlInGaP LEDs. “It could be possible that Aixtron is beginning to accept it may have to step out of this specific market because of the competition from China,” he says.

And while the likes of Amec and Topec claim to own extensive IP – Amec reports the technology embedded in its Prismo A7 system is protected by 155 patents – the patent disputes have started.

Earlier this year, Veeco filed a patent case against Germany-based chemical company, SGL Group, which supplies graphite wafers for systems to MOCVD manufacturers worldwide.

In a move that could choke MOCVD component shipments to Chinese players, Veeco alleges infringement of patents that cover the entire MOCVD equipment and wafer carrier design.

Industry sources claim sales of the alleged components have stalled for the time being, which could eventually have a detrimental effect on production from MOCVD manufacturers in China.

Still amid the patent spats, Amec has just reported ‘brisk’ sales, and China-based LED manufacturing heavyweight, San’an Optoelectronics, has publicly commended the company on its tools.

“With Amec, we have a partner that can meet our advanced technical requirements,” stated San’an Vice Chairman, Kechuang Lin. “What’s more, as a local China-based company known for developing leading-edge process technology, we benefit from close proximity to Amec’s rich process expertise, as well as fast response times from the company’s field support teams.”

Indeed, Fox is certain that success from the likes of San’an is helping the nation’s MOCVD players. “The fact that these Chinese LED companies have done so well in the last two years has been very good for the Chinese MOCVD companies, especially Amec,” he says. “So now, we’re seeing market share changes and explosive growth from Amec.”

Slashing the cost of the GaAs solar cell

Sol Voltaics aerosol growth process promises to kick-start a market for terrestrial solar cells based on GaAs

RICHARD STEVENSON INTERVIEWS SOL VOLTAICS CEO ERIK SMITH

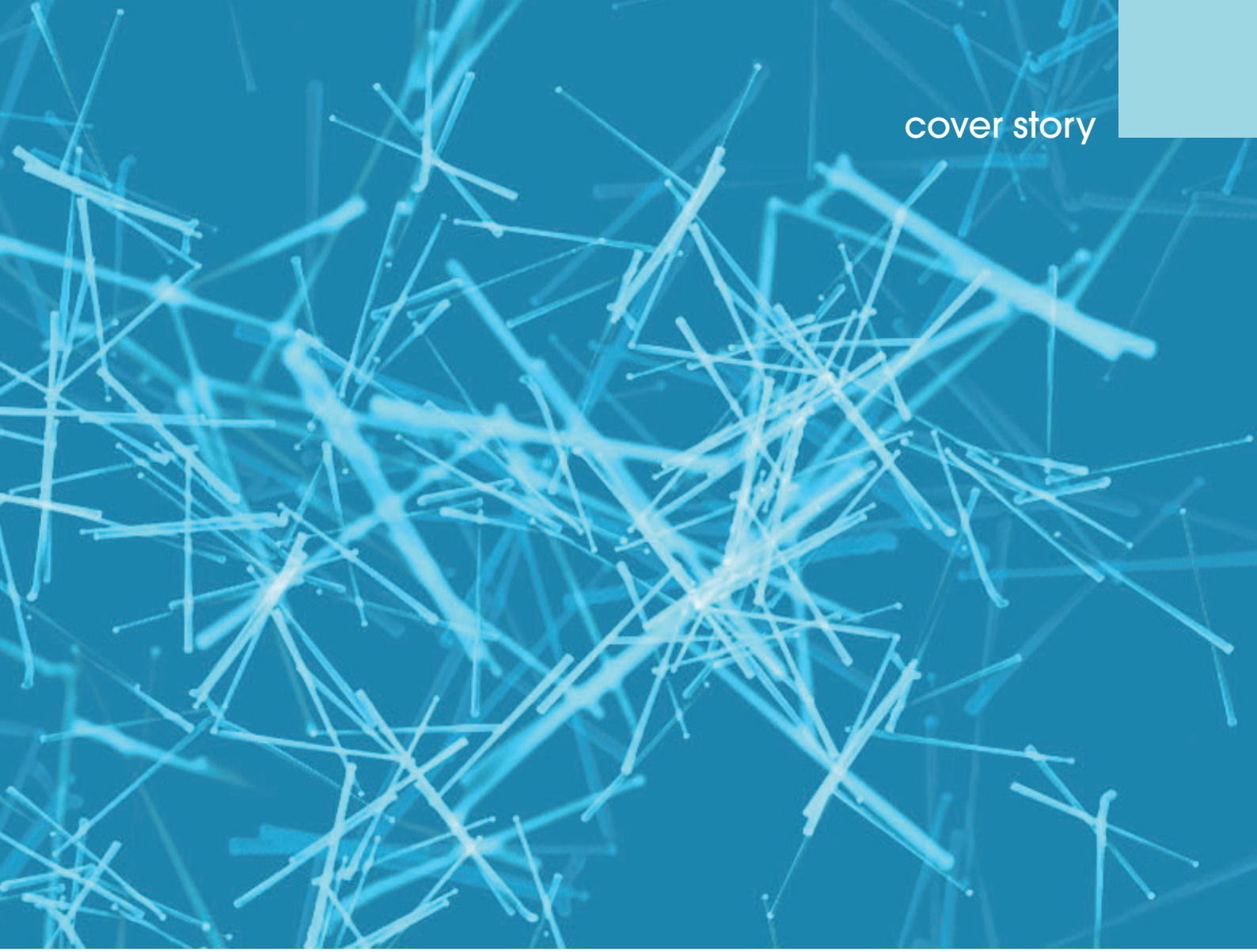
Q Your company is developing GaAs nanowire solar cells that are produced with an aerosol-based growth technology. Do you see the primary market for your technology as a low-cost solution to increasing the performance of silicon solar cells, via the creation of tandem cells? Or is your technology going to be used for the manufacture of standalone nanowire cells?

A The end product of our technology is basically a solar film. It can be used standalone, terrestrial, or it can be used in tandem cells.

Typically, penetrating the household rooftop [market] is the beginning for new materials, because you don't have as many bankability issues. When it's rooftop you can still go single-junction, which is just standalone, or tandem, depending on what your output needs to be. The single-junction will be extremely cost-per-Watt competitive. Tandem is upper 20 percent efficiencies, at costs equivalent to silicon. So it depends what your goal is.

Q What's the attraction of a III-V-and-silicon cell in the terrestrial market? Why not just deploy silicon cells?

A III-Vs have always been considered one of the highest efficiency cells on the market in a single junction. III-Vs also benefit significantly from what [cadmium telluride solar cell manufacturer] First Solar benefits from, which



is a very good temperature coefficient. So in very hot climates the cells don't degrade nearly as much as silicon.

Q Back in 2016, at the CS International Conference, speaker Frank Dimroth from the Fraunhofer Institute for Solar Energy Systems included in his talk an evaluation of the market opportunity for III-V-on-silicon cells. He presented calculations based on the MOCVD growth of a five micron-thick III-V film, and concluded that costs would need to fall by two orders of magnitude before this technology could make an impact. Do you agree with this view that if III-Vs are to have a place in the terrestrial solar cell market, the technologies that are to be used need to be many tens of times lower in cost than they would be with traditional techniques?

A There's no way that you can grow an MOCVD-based film and have a tandem that is cost effective. It's not going to work. I can't comment on tens or twenties, or multiple orders of magnitude, because I don't know what I'm orders of magnitude against. But all I know it has to be cost effective. We have done bottom-up cost models, and we're going to be extremely effective.

I also know that other III-V companies have, for example, been bought by Chinese companies. They are not cost-effective. That's the reason they were bought for pennies on the dollar.

Q Is the business plan to license the process and sell aerosol-based growth reactors?

A Our business plan can go in a number of ways, and I'm not going to comment, but all of those that you can imagine are viable. They all have pros and cons.

Q What is the essence of your growth technology?

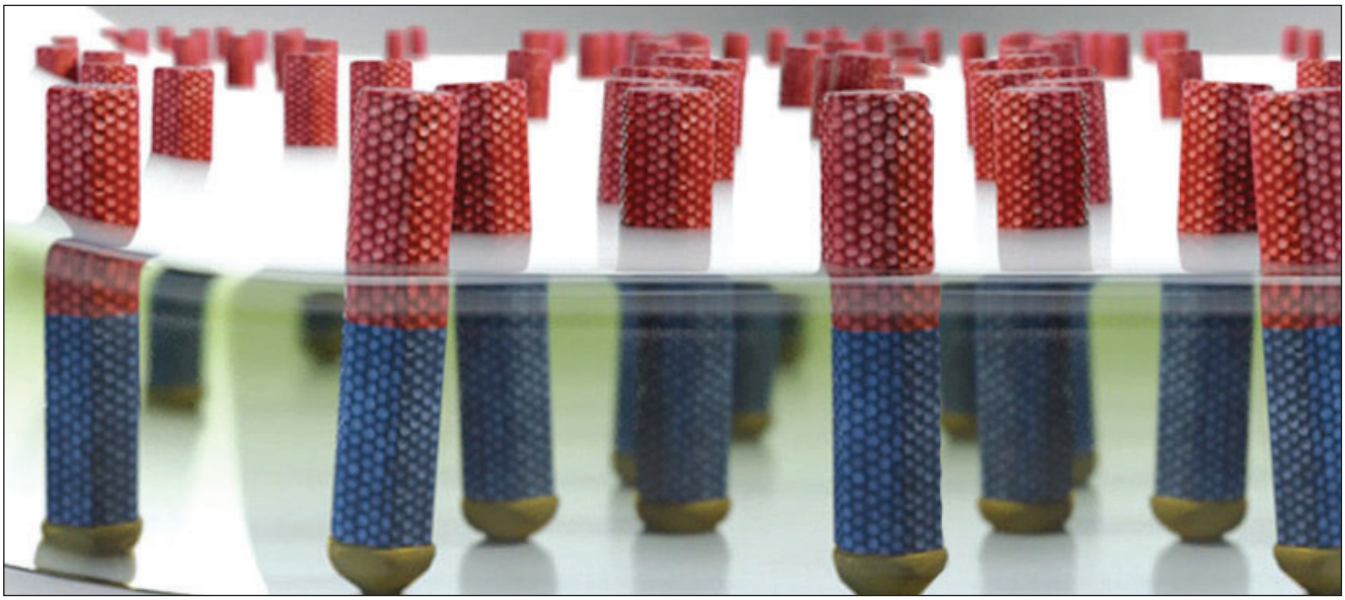
A It's extremely similar to MOCVD growth methodology – but without the wafers, which are expensive, and without the high costs of MOCVD.

Q Why are production costs lower than they are for the likes of MBE and MOCVD, growth technologies that are suitable for high-volume manufacturing?

A It's a combination of the fact that we can rain nanowires in a continuous process, that the nanowires grow at one thousand times the rate that they grow in an MOCVD tool, and the fact that we use 80 percent less material than wafer based solar cells, because of the photonic effects. [Note that] we make a solar film – it is not wafer based.

Q How do you ensure homogeneity when growing the nanowires?

A Well, it's a single crystal, and it's the same growth mechanism as MOCVD. Growth starts from a seed.



SolVoltaics' process produces a film of doped, aligned gallium arsenide nanowires. Once passivated, they can form a film with an efficiency of more than 15 percent.

Once we produce those nanowires, they come out like a dust. You have mis-orientated nanowires, and you have to align them. We do that beautifully, with over 99 percent alignment and orientation.

This ability to make nanowires and control their alignment, whether they are gallium arsenide, gallium arsenide phosphide or amorphous silicon nanowires, could be more than solar.

Q You passivate the nanowires. Have you optimised this process?

A Yes, passivating the nanowires is critical to making a good solar cell. You could have a solar cell in gallium arsenide that is not passivated, but it's a pretty poor solar cell. The fact that we have demonstrated a 15.3 percent nanowire solar cell is indicative of good passivation.

Q What are the optimal dimensions for your nanowires?

A Typically, diameters are somewhere between 150 and 200 nanometres, and the length of the nanowires between two and three microns.

Q What is your current record for nanowire efficiency, and how high an efficiency is possible?

A Our record is 15.3 percent. The roadmap for efficiency from that point on is very clear on what needs to be changed. How to change those things and how to improve those things is also clear. For example, optimising the emitter length, the TCO, and the contact etch. Within the gallium arsenide community it is known how to improve all those things. Right now, 24 percent is the clear, visible roadmap. And Alta Devices has had cells at 28, 29 percent.

Q Are your aerosol-based reactors now ready for solar cell manufacture?

A Actually, we have not announced some things so I don't want to say too much, but we have two different aerosol reactors up and running right now. One is more advanced than the other. They are producing wires.

Q With your reactors, how long can they run for before they require any maintenance?

A That's the whole optimisation that we are going through as a company right now. When our newest tool came up, it was running at a certain number of hours a day, and now it's running at a much better number of hours per day.

We have basically done the R&D, and now it's about optimising everything. So to optimise the equipment you change an injection flow, you change a material here, and

We have basically done the R&D, and now it's about optimising everything. So to optimise the equipment you change an injection flow, you change a material here, and you change an exhaust type there – you do all of these things to start optimising the equipment

you change an exhaust type there – you do all of these things to start optimising the equipment.

Q One of the substantial costs associated with epitaxy is the capital cost of the growth reactor. How does this compare to the cost of building your tools?

A I'm familiar with MOCVD tools and CVD tools. If you look at the cost of the tool, there's lots of steal, there lots of pneumatic panels, there are lots of pumps and gases used.

All I can say with respect to cost is the cost of the tool itself is not the significant part. It's still mostly the materials and the integration of the cells. The fact that it's a non vacuum, continuous process [with our approach] enables us to be lower in cost than a standard batch semiconductor process.

Q What are the waste products in your process, and how do you treat them?

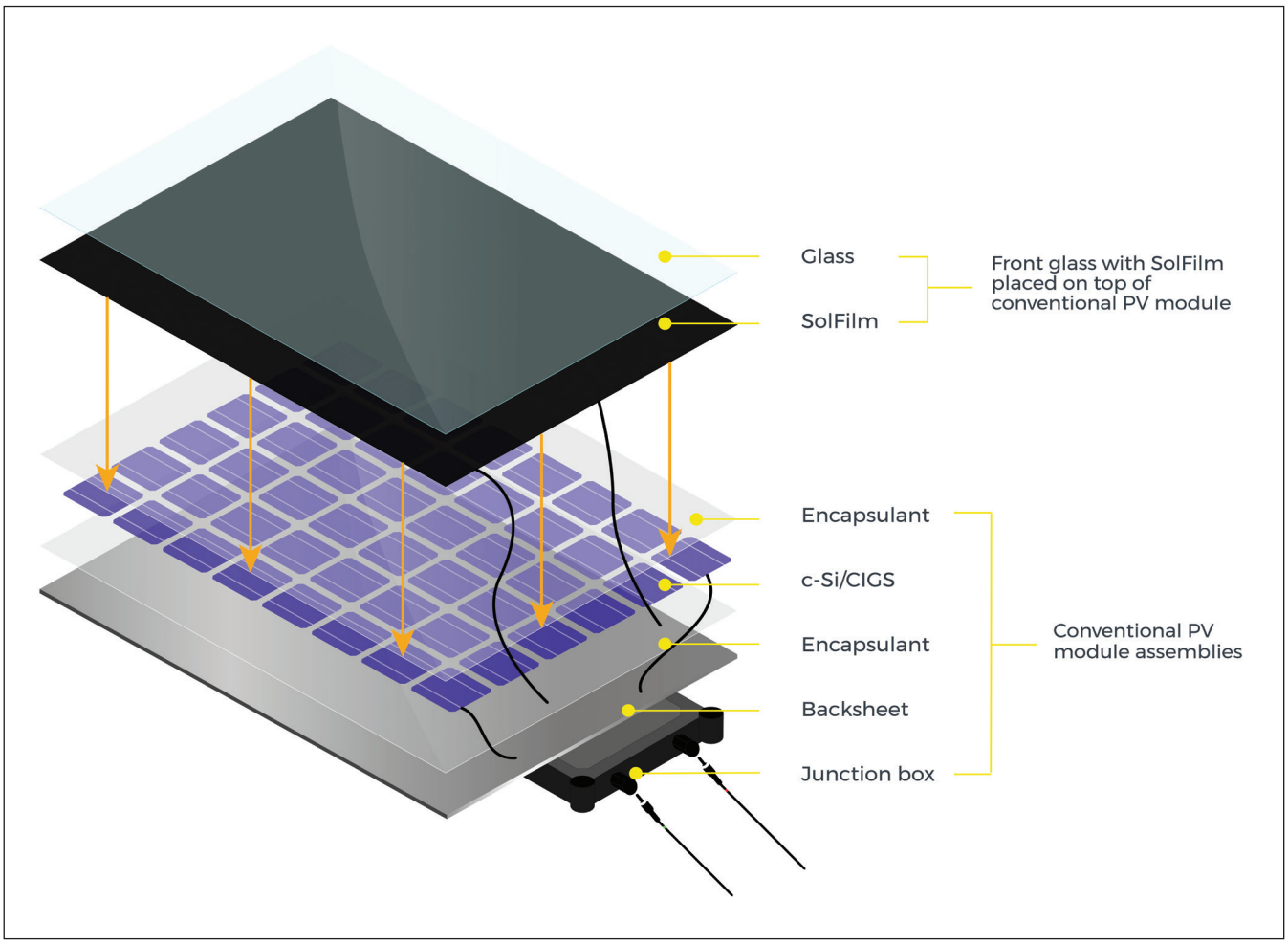
A Everything is recycled. Every solar manufacturer has to have a methodology to recycle the modules after their lifetime. We have programs ongoing now that will meet that criteria when the product comes to end of life. We have to do all that stuff. There are waste gases in the process, because you are not utilising all your materials. And those are also recycled.

Q You have raised tens of millions of dollars in funding. How far can this take you?

A Starting from 2011, we have raised $58 million, but that also includes a lot of non-diluted funding. About 25 percent of that is non-diluted, so non-equity type money. It is from the EU, or from the Swedish Energy, or from the other Scandinavian programmes. If we were in Silicon Valley, it would have cost a lot more to get where we are today. We would have needed almost double that what we need here.

Q What do you need to do before you start generating sales?

A It depends somewhat on where you initially go with generating sales. If you go after the utility sector, then that takes longer. The spectrum for solar is anywhere from little dinky consumables to utility and space stuff. But samples for customers are going to be coming out in 2018, and then it depends on the business model. The preliminary business model may be a little different than the mid-range business model, versus the long-range business model. Our business model, it might be where our customers decide to take it.



Sol Voltaics' GaAs nanowire film could be used to boost the efficiency of silicon and CdTe solar cell via the formation of a tandem architecture.

CS INTERNATIONAL CONFERENCE

10-11 APRIL 2018
Sheraton Airport Hotel Brussels

Connecting, informing and inspiring the compound semiconductor industry.

CS INTERNATIONAL 2018 CONFERENCE
SPEAKERS ANNOUNCED!

With a record breaking number of speakers and sponsors secured, the eighth CS International Conference is set to be the biggest and best yet!

Held at the Sheraton Airport Hotel in Brussels on 10 -11 April 2018, CS International will once again be the must-attend event for the global compound semiconductor community.

Highlights include talks by the leaders of power electronics pioneers Transphorm, Panasonic and VisIC; presentations on the integration of compound semiconductor and silicon technologies by NAsP III-V and the co-ordinators of two multi-partner European projects; plus a talk by Seoul Semiconductor on its pioneering efforts at chip-scale LEDs amongst many others.

Delivering over 30 presentations CS International will provide comprehensive coverage of the global semiconductor industry exploring 5 core themes

- Wrestling market share from silicon power devices
- Finding solutions with heterogeneous integration
- 5G: Where are we and what's next?
- LEDs: Magnifying margins
- Ramping revenues from RF devices

For each theme a keynote presentation and market analyst talk will be given by the leading decision makers and influencers within the industry.

Book your place NOW!

www.cs-international.net/register to secure your place

It's set to be another sellout

PLATINUM SPONSORS

AIXTRON attolight beneq CATAPULT Compound Semiconductor Applications EPIGAN evatec process systems EVG

FerroTec htt GROUP. ims chips KLA-Tencor nanotronics Nanowin 苏州纳维科技有限公司 Revasum YOLE Développement

GOLD SPONSORS

Accel-RF Instruments Corporation BLUGLASS CS CLEAN SOLUTIONS INNOVION FOUNDRY ION IMPLANTATION IQE LAYTEC Knowledge is key Panasonic semi VEM Vacuum Engineering | Materials

WIFI SPONSOR PORTFOLIO SPONSOR LANYARD SPONSOR DELEGATE BAG SPONSOR SUPPORTED BY

BROLIS SEMICONDUCTORS Plasma-Therm SPTS qorvo all around you lighting.eu EPIC European Photonics Industry Consortium

This two day event covers five themes

Speakers announced to date

Wrestling Market Share from Silicon Power Devices

What are the next opportunities for SiC? And how can GaN gain significant traction in the market place?

ANALYST

- **Richard Eden: IHS Markit**
  The SiC & GaN power semiconductor market: Forecasts and drivers

SPEAKERS

- **Philip Zuk: Transphorm**
  Shifting gears: The "GaN-ification" of automobiles
- **Peter Friedrichs: Infineon**
  Exploiting the merits of GaN and SiC
- **Hiroyuki Handa: Panasonic**
  Trimming the losses in GaN GITs
- **Tamara Baksht: VisIC Technologies**
  High efficiency at high power density: realisation of GaN's promise for power electronics
- **Andy Sellars: Catapult**
  Accelerating the commercial application of compound semiconductors
- **Mohamed Alomari: IMS Chips**
  Fast-loop assessment of GaN/AlGaN epitaxial layers for power applications
- **Cem Basceri: Qromis**
  'Status Updates: Volume Manufacturing of High Performance & Scalable GaN Power Devices on 8-inch Diameter QST Platform'

Finding Solutions with Heterogenous Integration

Where will the growth of compound semiconductors on silicon deliver a fundamental change? And what are the tricks to ensure success?

ANALYST

- **Zhen Zong: Yole Développement**
  Presentation TBC

SPEAKERS

- **Jean-Pierre Locquet: GaNonCMOS EU Project**
  Dense integrating GaN power switches with CMOS drivers
- **Wolfgang Stolz: NAsP III-V**
  Building III/V-devices on CMOS-compatible Si (001)
- **Lars-Erik Wernersson - Lund University**
  Integrating III-V nanowires to advance CMOS system-on-a-chip technologies

5G: Where are we and What's Next?

What form will 5G take? And how good will 5G be for GaAs and GaN?

ANALYST

- **Eric Higham: Strategy Analytics**
  Is 5G roll-out a certainty? And will it be good for GaAs and GaN?

SPEAKERS

- **Roger Hall: Qorvo**
  Building the industry's first 5G front-end
- **Liam Devlin: Plextek RFI**
  MMICs - what is needed to get mmWave 5G to work?

LEDs: Magnifying Margins

Which sectors offer the best returns? Does the bottom line get the biggest benefit from streamlining manufacturing, or from optimising the chip?

ANALYST

- **Pars Mukish: Yole Développement**
  Revolutionising displays with MicroLEDs

SPEAKERS

- **Andreas Weisl: Seoul Semiconductor**
  Improving LEDs with a Wafer Level Integrated Chip on PCB (WICOP) architecture
- **J.C.Chen - Ostendo Technologies**
  The monolithic full-colour LED and its applications
- **Keith Strickland – Plessey Semiconductors**
  Horticultural lighting offers growth opportunities

Ramping Revenues from RF Devices

What are the opportunities for III-Vs in defense and civilian markets? Will higher frequencies open up new sales?

ANALYST

- **Asif Anwar, Strategy Analytics**
  Defense sector trends and the associated market outlook for compound semiconductors

SPEAKER

- **Nick Cataldo, Efficient Power Conversion**
  Wireless charging with GaN devices




GaAs provides the key ingredient for

5G phones

GaAs can meet all the requirements for the power amplifiers used in front-end 5G modules

BY BEN THOMAS FROM QORVO

When will the roll out of 5G begin? Until recently, that was anyone's guess. However, the timing has now become clearer, and it could be as early as 2019.

Driving the acceleration in the deployment of this communication technology is a recent advance in global broadband standards: the non-standalone radio. It enables operators to deliver 5G data speeds more quickly and affordably, via an enhancement to existing 4G infrastructure, rather than a replacement. There are implications, though, including complex new challenges for mobile RF front-ends. They will need to support 4G and 5G waveforms, unprecedented bandwidth and new high-frequency bands.

These efforts will be worthwhile, because when the build-out of 5G networks takes place, it will make a significant impact. It will lead to: enhanced mobile broadband for smartphones and other mobile devices, which will enable carriers to provide much higher peak data rates and expand network capacity to support more users at higher densities; ultra-reliable, low latency communications for critical applications requiring very low latency, such as self-driving cars and industrial control systems; and massive machine type communications for a vast number of Internet-of-Things devices that require low-power, relatively low-bandwidth communications.

To realise all of this, 5G networks will use a much wider range of frequencies than today's 4G networks, including millimetre-wave frequencies. And to support the divergent requirements of the differing applications, they will adopt a technique known as network slicing, which allocates to each device a varying degree of latency, data rate and security level, based on their specific needs.

When it comes to enhanced mobile broadband, 5G will complement 4G, rather than replacing it. Operators are already enhancing their existing 4G networks with LTE Advanced and LTE Advanced Pro capabilities. This should lead to peak data rates of up to about 1 Gbit/s via carrier aggregation (CA), a technique that combines multiple data carriers and leads to greater bandwidth. However, to meet the anticipated growth in mobile broadband, networks will need to combine even greater capacity with higher speeds than LTE can provide.

An indication of the extent of these increases in capacity and speed is given by the predictions provided by the Cisco Visual Networking Index. According to this source, data consumption for the average smartphone user is expected to quadruple to nearly 7 GB per month by 2021. Most of that growth will be driven by video traffic, together with emerging applications, such as augmented reality and virtual reality. To support these capabilities, 5G enhanced mobile broadband is planned to deliver peak network data rates of up to 10 Gbit/s.

The pressure to accelerate the 5G standards process, which will be driven by these advanced capabilities, culminated in the definition of non-standalone radio in March 2017. The mobile standards organization 3GPP agreed to divide the development of the 5G new-radio specifications into two phases. The non-standalone specification, designed primarily for mobile broadband, is being fast-tracked as part of 3GPP Release 15; and the 5G standalone new-radio specification will be in Release 16.

With non-standalone radio, the 4G LTE band provides an 'anchor' for carrying control and signalling information, while the 5G band acts as a data pipe. In contrast, with 5G standalone radio, the new 5G network architecture is used for both the control plane and the user plane, which carries the data.

Thanks to the development of the non-standalone radio, early delivery of 5G enhanced mobile broadband is more economically viable for network operators. That's because these operators can leverage the existing 4G LTE modems and transceivers in devices and infrastructure along with the existing evolved packet core. Or, to put it another way, operators can deliver non-standalone radio by enhancing existing 4G LTE infrastructure, rather than complete building out of next gen core, standalone radio 5G networks. It is this approach that is enabling large-scale 5G, enhanced mobile broadband trials and deployments for as soon as 2019, rather than the 2020 timeline, previously slated.

Initially, the deployment of enhanced mobile broadband is expected to focus on frequencies below 6 GHz. That's because this frequency domain supports broader coverage, and it is better suited than millimetre-wave frequencies for the support of network connections in mobile devices. Helping the transition is the allocation of new global frequency bands – 3.3 GHz and 5 GHz have already been allocated or are under consideration, due to near-global availability. These efforts should lead to the re-farming of TDD-LTE bands, such as 42 and 43, that will also be used as 4G anchor bands in different regions; and the introduction of new bands n77, n78 and n79. The latter three will be the first 5G bands that are allocated solely for 5G data transmission.

RF front-end challenges

Equipping handsets with 5G non-standalone radio and complex 4G LTE Advanced CA functionality will be a challenge for both device and chipset makers. Their efforts will be directed at producing non-standalone, RF front-ends that support 4G and 5G requirements in a single module, and enable global coverage, as this minimizes the need for handset localization. These

requirements will create an unprecedented set of technical challenges for the RF front-end, especially on the transmit side. Challenges will include the delivery of high-power efficiency and linearity for 4G and 5G waveforms, while supporting very wide bandwidth and delivering high output power, including the new Power Class 2 standard. Power Class 2, or HPUE, has recently been adopted as a method to improve coverage for handsets, but increasing the power by 3dB over the traditional Power Class 3 mobile device standard.

These various standards are now well underway, with two 5G uplink waveforms moving toward formal approval within 3GPP: Cyclic Prefix Orthogonal Frequency Division Multiplexing (CP-OFDM) and Discrete Fourier Transform-spread-OFDM (DFT-s-OFDM). Front-ends for 5G, including non-standalone radio, will have to support both of these waveforms. Of these two, CP-OFDM presents the greatest challenges, but has the most promise, offering several key advantages for network operators. Its attributes include providing the most efficient spectral packing of resource blocks (it is up to 98 percent), and offering benefits in spatial multiplexing, so that it can support multiple input, multiple output (MIMO) technologies. Thanks to these merits, CP-OFDM is the leading candidate when the priority is to maximize network capacity, such as in cities and within buildings. The challenge is that CP-OFDM generates much higher peak-to-average power ratios than 4G LTE. The implications are the need for greater power back-off in the power amplifier and high linearity over a wide range of power levels.

The alternative, DFT-s-OFDM, provides less-efficient spectral packing – it is up to 90 percent – and it is less effective for MIMO. However, this form of 5G uplink, which has the same waveform as the LTE uplink in use today, offers a greater operating range, thanks to lower peak-to-average power ratios. Due to these characteristics, one would expect the use of DFT-s-OFDM when the priority is to maximize coverage, such as in less densely populated areas.

Massive bandwidth

One of the big differences between 4G LTE and 5G is the bandwidth of the signals: it will be typically 100 MHz per carrier, compared with up to 20 MHz per carrier with LTE (although up to 60 MHz has been supported using CA). The combination of the wider bandwidth and the new 5G waveforms propels peak-to-average power ratios to far higher levels than they are in any preceding cellular communications standard. Consequently, the RF front-end needs to maintain sufficient gain and high linearity across very wide channels within high-frequency bands.

There are power efficiency challenges associated with the wider-bandwidth signals. To maximize efficiency for 4G LTE, common approaches are to introduce envelope tracking and digital pre-distortion. If envelope tracking is adopted, efficiency is optimized by continuously adjusting the supply voltage of the power amplifier, so that it tracks the RF envelope.

Unfortunately, today's envelope trackers can only support a bandwidth of up to 40 MHz. Due to this limitation, envelope tracking is unsuitable for 100 MHz 5G signals. Instead, the power amplifier has to be operated in average power tracking mode (with a fixed voltage), while providing high linearity operation across the entire frequency range. The upshot is a substantial fall in the efficiency for the transmit chain, along with a very challenging high linear power requirement for the power amplifier design.

As is the case for LTE, 5G requires a multi-gain state PA with relatively quick gain settling times. If the most complex downlink modulation scheme is adopted, 256QAM, high linearity is required in the low-noise amplifier as well. Key figures of merit are a superior error vector magnitude, and an improved second-order intercept point over that needed for 64QAM LTE signals of today.

Higher output powers

To maximize the operating range of the handset, efforts are being directed at increasing the RF output power, as this can compensate for greater propagation losses at high frequencies. This requires support for the 3GPP Power Class 2 standard, which doubles handset output power at the antenna – it increases from 23 dB, the previous standard, to 26 dB. By turning to Power Class 2, operators are able to use

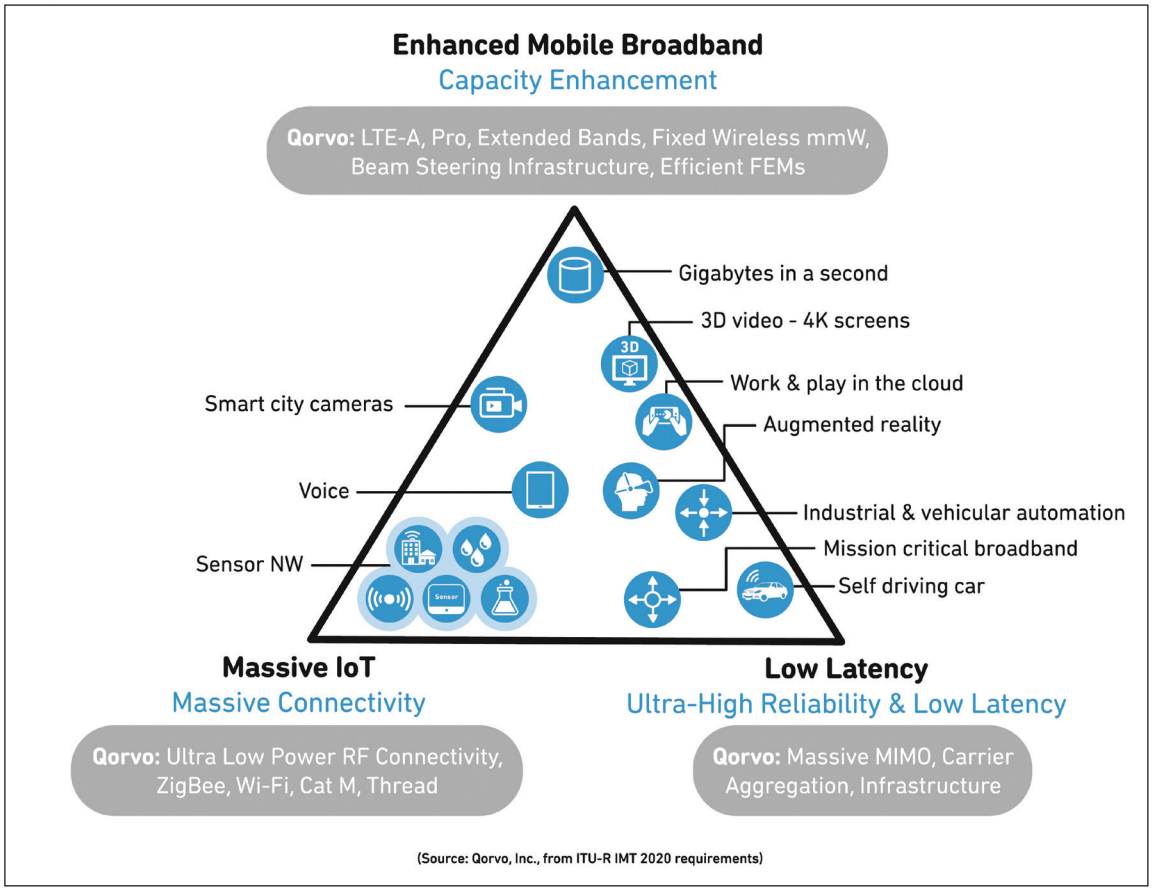


Figure 1. 5G application categories

high-frequency bands to realise an operating range comparable with that provided by lower-frequency bands, without the need to build extensive new wireless infrastructure.

That's not the only benefit, however. Power Class 2 also improves in-building reception. In contrast to 4G LTE, where the 3GPP Power Class 2 standard is only utilized in a limited set of TDD-LTE bands, with 5G, Power Class 2 is a baseline requirement across all new bands of operation. Consequently, all 5G RF front-ends will have to support this high output power, while managing the associated thermal challenges, including heat dissipation.

On top of these thermal challenges, the move to 5G non-standalone radio will give device manufacturers the tricky task of having to cram even more complex RF content into the already crowded space allocated to the RF front-end. Unlike 4G LTE, where MIMO is optional, 5G implementations are expected to use 4 x 4 MIMO in the downlink as per the standard; some devices may use 2 x MIMO for the uplink as well, providing an unprecedented 200 MHz of uplink bandwidth for extremely high data rates. Accommodating the additional RF chains within the handset will require highly integrated modules. In some cases, additional antennae may need to be introduced in some handsets to support the high-frequency bands, leading to further size and RF isolation challenges.

RF front-end design

Engineers must take great care when designing the RF front-end, so that they can fulfill the extraordinary set of efficiency, bandwidth, linearity, and output power requirements demanded by 5G non-standalone radio. Meeting the overall requirements hinges on optimization of the performance of key components within the RF front-end, such as the power amplifier, low-noise amplifier and filter.

The key to success is to combine class-leading components, manufactured with different process technologies. Using advanced packaging techniques, these components can be united into integrated modules that save space, increase power efficiency and improve thermal performance.

At Qorvo, we have designed an RF front-end that meets the global requirements of 5G non-standalone radio (see Figure 2). This front-end, our QM19000 that was unveiled at this year's Mobile World Congress, features a filter with a very wide passband to support the allocated 4G and 5G bands – it supports a 900 MHz range, spanning 3.3 GHz to 4.2 GHz.

One attribute that this filter does not have to have is 'steep skirts', which are needed in other designs to avoid interference in lower-frequency regions of the spectrum that are more congested. Thanks to this, it is not necessary to use bulk acoustic wave

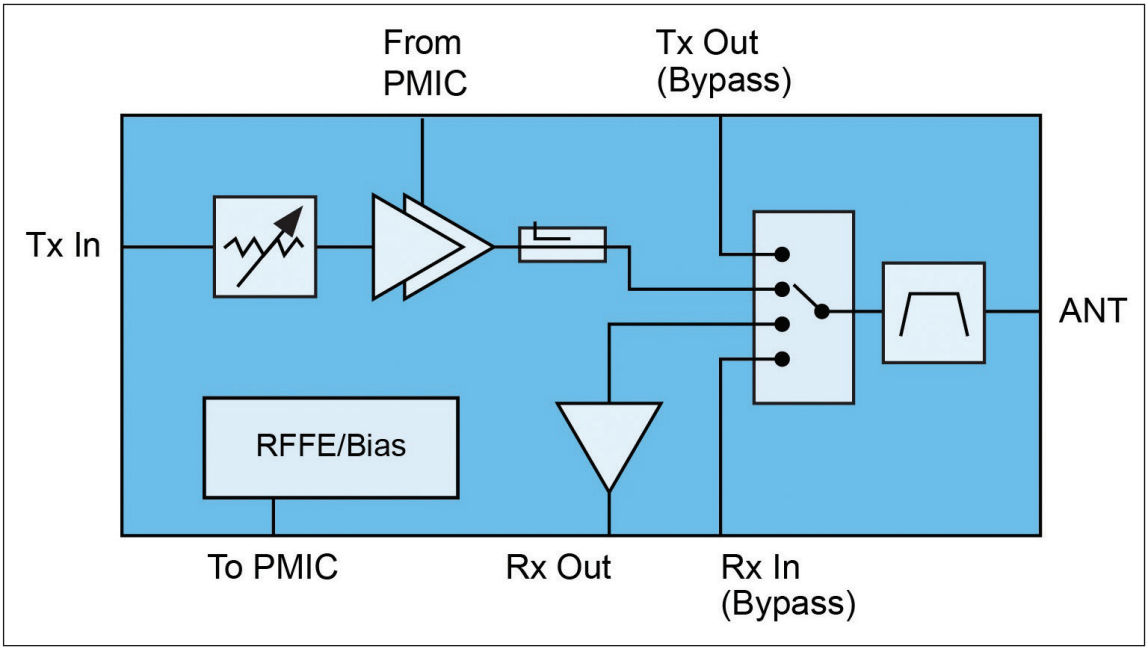


Figure 2. The Qorvo QM19000, a 5G non-standalone radio mobile RF front-end.

filter technology, although this could be used as requirements evolve in future.

For the low-noise amplifier, a variety of technologies are available, including silicon-on-insulator, but the GaAs pHEMT has been the ideal choice, as it offers advantages in meeting the strict linearity requirements.

For meeting 5G non-standalone radio requirements, the power amplifier is critical. It has to handle both 4G and 5G transmissions. In the first implementations, envelope tracking will be used for 4G LTE to maximize overall system efficiency. However, this technology is unsuitable for 5G, due to the much greater bandwidth, typically 100 MHz. Due to this, the power amplifier has to support multiple power management schemes: envelope tracking for 4G, and average-power tracking for 5G. As it must meet performance requirements in both modes, it needs to combine high saturated efficiency in envelope-tracking mode with linear efficiency in average-power tracking mode. This amplifier must also meet linearity and gain requirements when supporting both 4G and 5G transmissions. That includes when it is operating with the power back-off, a necessary condition for CP-OFDM, due to the high peak-to-average power ratio.

To meet all the requirements for 4G and 5G, including saturated and linear efficiency, it is necessary to use a power amplifier manufactured with a compound semiconductor technology, such as our HBT5 GaAs process. Successive generations of this process have delivered increased gain and power output to meet new requirements, such as Power Class 2, while improving efficiency. Power amplifiers produced with our HBT5 process offer high thermal performance, with excellent heat dissipation characteristics, thanks to the use of our copper-bump packaging technology.

Even with a two-stage power amplifier built with our HBT5 process, additional amplification may be required to meet requirements for higher output power, such as when supporting Power Class 2 and during use of CP-OFMD waveforms (where transceiver drive levels are anticipated to decrease by up to 3 dB). To meet these needs, our QM19000 includes an additional variable gain amplifier. This product also features sophisticated power management, for switching between envelope-tracking mode and average-power tracking mode.

Additional merits of the QM19000 include high saturated power-added efficiency, while also maintaining good linear efficiency across a wide range of positive supply voltages. The module maintains efficiency across the entire 3.3-4.2 GHz frequency range, with the use of GaAs, rather than SiGe, providing higher gain than other technologies at these high frequencies. Consistent gain is provided across the supported frequency range when transmitting a 100 MHz CP-OFDM signal, while maintaining high linearity.

It is clear that establishing a non-standalone radio standard for mobile broadband has enabled operators to accelerate plans for 5G. At the same time, it has created challenging new mobile RF front-end requirements, including the need to support both 5G and 4G waveforms and massive bandwidth while providing high gain, efficiency and linearity under a wide range of conditions. Integrated RF front-ends, including high-performance PAs based on compound semiconductor technology, are key to solving these challenges. As the other 5G application areas advance toward deployment, they will generate other RF challenges, requiring innovative high-performance solutions for devices and wireless infrastructure. These solutions are likely to leverage the unique performance characteristics of compound semiconductors.

EVG®

invent
innovate
implement

www.EVGroup.com

Solutions for

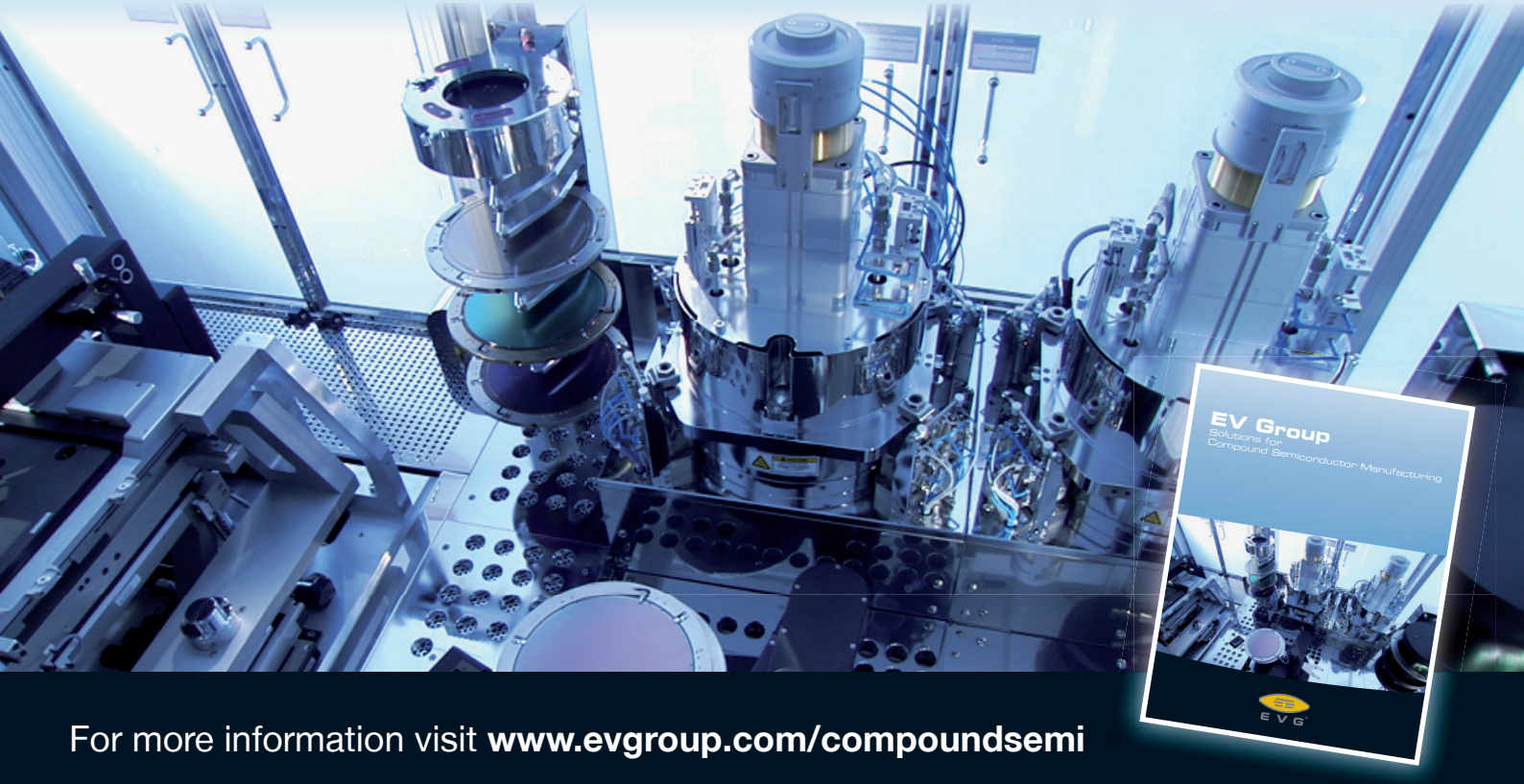
COMPOUND SEMICONDUCTOR MANUFACTURING

Wafer Bonding
for Heterogeneous Integration, Layer Transfer and Advanced Packaging

Optical and NanoImprint Lithography
for Device Patterning and Advanced Packaging

Advanced Resist Processing
for Dielectrics, Thick / Thin Resist Layers, Through Vias and High Topography

Temporary Bonding and Debonding
of Thinned and Fragile Compound Semiconductor Substrates



For more information visit **www.evgroup.com/compoundsemi**

Improving SiC epilayers

A six-inch single-wafer tool with high rotation speeds yields uniform, high-quality SiC epilayers

BY YOSHIAKI DAIGO, HIDEKI ITO AND SHINICHI MITANI FROM NUFLARE TECHNOLOGY

TREMENDOUS ENERGY SAVINGS can result from a switch to more energy efficient power electronics. So great can those savings be that if the adoption of high-efficiency devices were to exceed 90 percent, it could cut consumption by as much as 25 percent. This would be great news for humanity, as it would trim carbon footprints and cut utility bills.

The key to introducing more efficient power electronics is to replace silicon devices with those made from wider bandgap materials. The most established alternatives are those made from SiC and GaN. To ensure their high performance, these devices must be manufactured using growth tools that yield uniform wafers that contain very low levels of defects.

At NuFlare of Japan we have developed a family of single-wafer CVD tools that do just that – the EPIREVO range. These tools employ single-wafer, high speed wafer-rotation technology and are capable of providing high-speed growth of silicon, GaN and SiC epilayers. In all cases, the epitaxial films have high in-wafer uniformity.

Recently, we have optimised the growth of epilayers on 6-inch 4H SiC using our EPIREVO S6 tool. It is designed to yield epilayers that combine a high level of uniformity, in terms of thickness and doping concentration, with minimal surface and crystalline defects [1, 2].

Our EPIREVO S6 contains: an upper gas inlet; a hot-wall; a rotation holder; and resistive heaters, positioned on the sides and the bottom of the chamber (see Figure 1). One feature of this tool is that the position of gas injection nozzles in the gas inlet can be adjusted. By fine-tuning them, it is possible to optimise the uniformity of both the thickness and the doping concentration of the epiwafers [3]. Prior to growth, a wafer is loaded into the chamber by a fully automated robot.

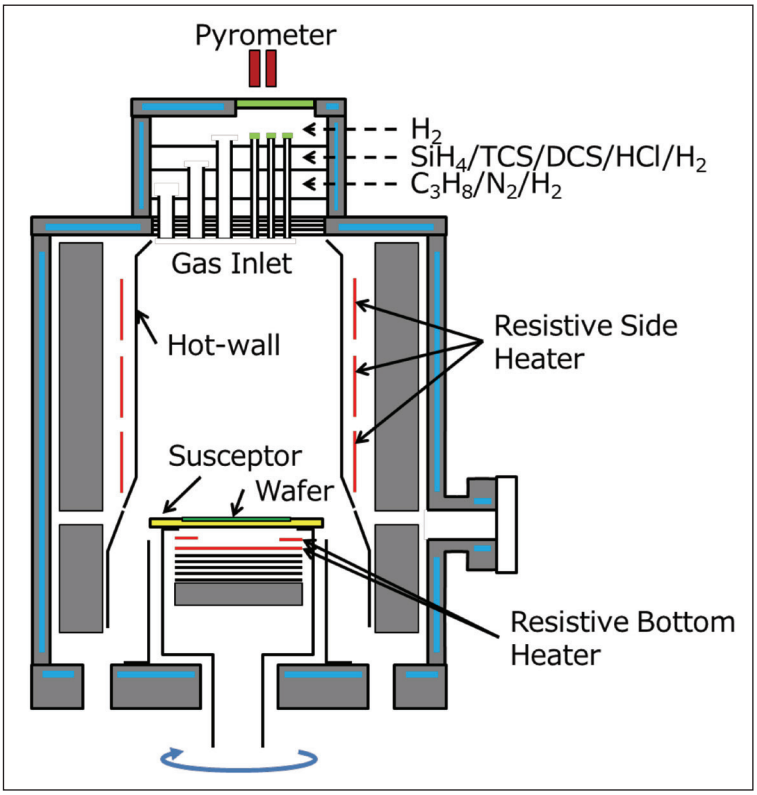


Figure 1. The CVD chamber of the EPIREVO S6.

With our tool, growth is typically undertaken at 1600 °C, using a wafer rotation speed of 600 rpm, a growth pressure of 26.7 kPa, and a chlorine-to-silicon ratio of typically 10. The process gases used are: C_3H_8 (carbon-source), SiH_4 (silicon source), H_2 (carrier gas), N_2 (dopant) and HCl (to suppress the formation of silicon-related clusters).

Minimising defects

To minimize surface defects produced by our tool, we have investigated the influence of the rotation speed during the temperature ramping step. During this ramp, two of our samples, A and B, have a rotation speed of 50 rpm; and the other two, C and D, have a rotation speed of 300 rpm (see Figure 2).

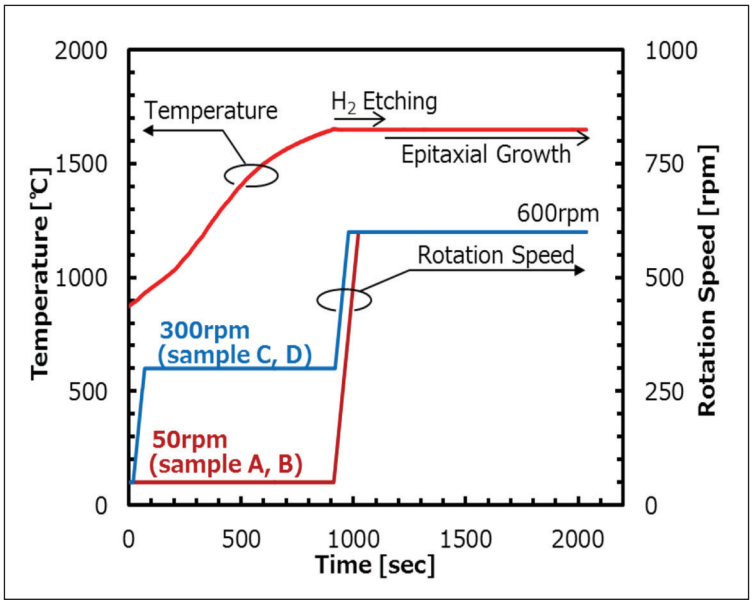


Figure 2. The rotation speed and temperature for initial process steps

Measurements of the surface defect density and inspection with an optical microscope image analysis tool reveal that the density of all forms of defect fall when faster wafer rotation speeds are used during the temperature ramping step (see Figure 3). The greatest of these reductions is associated with triangles, which are the majority of surface defects.

We also note that when a higher rotation speed is used during the temperature ramp, this shortens the length toward the step-flow direction of defects categorized as Down-Fall-triangles (DF-triangles) and triangles. This implies that a higher rotation speed should be employed during the temperature ramping, because it reduces the chances of DF capture on the wafer surface.

Two well-known imperfections that exist within the crystal structure of 4H-SiC, rather than on the surface, are stacking faults and basal plane dislocations. The latter can be reduced by growing a highly *n*-doped buffer layer prior to the growth of a drift layer. We have adopted that approach, producing epiwafers that have a 9.5 μm-thick drift layer with an *n*-type doping level of 8 x 10^{15} cm^{-3} on a 0.5 μm-thick, highly doped buffer layer with an *n*-type doping level of 1 x 10^{18} cm^{-3}. Doping levels of these buffer layers were the same, but grown with different ratios between the flow rates of SiH_4 and C_3H_8.

To expose the stacking faults and basal plane dislocations, we use photoluminescence to scrutinise

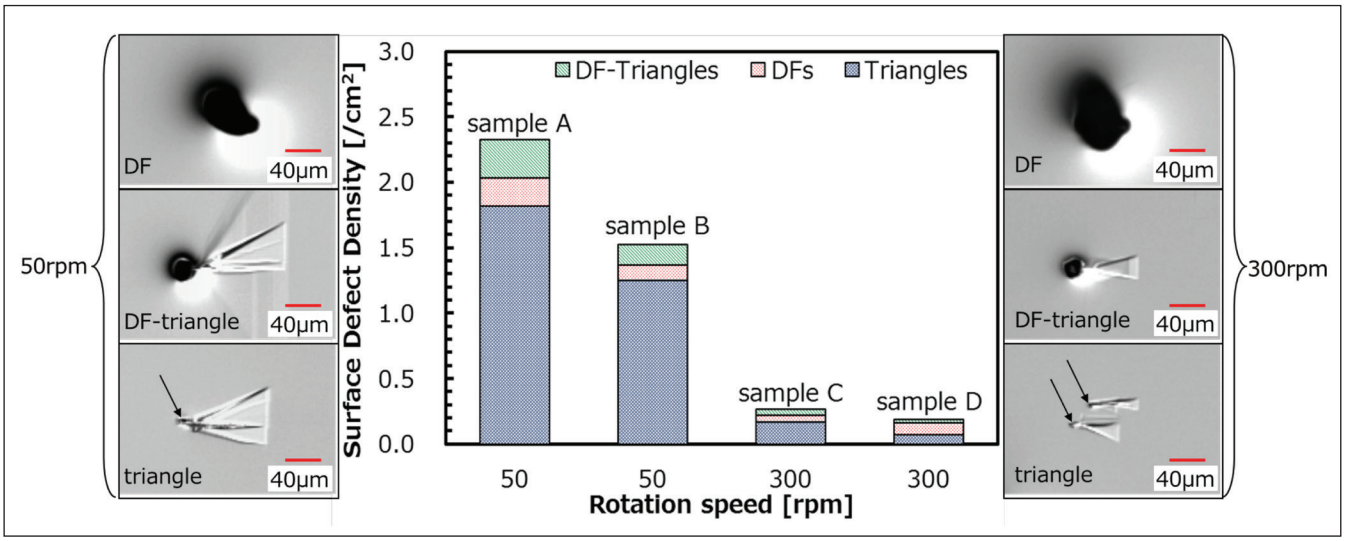


Figure 3. Surface defect density and typical surface defects on four samples. A and B were formed using a wafer rotation speed of 50 rpm during the temperature ramp phase; for C and D the wafer rotation speed was 300 rpm. Small pits generating triangles are indicated by arrows.

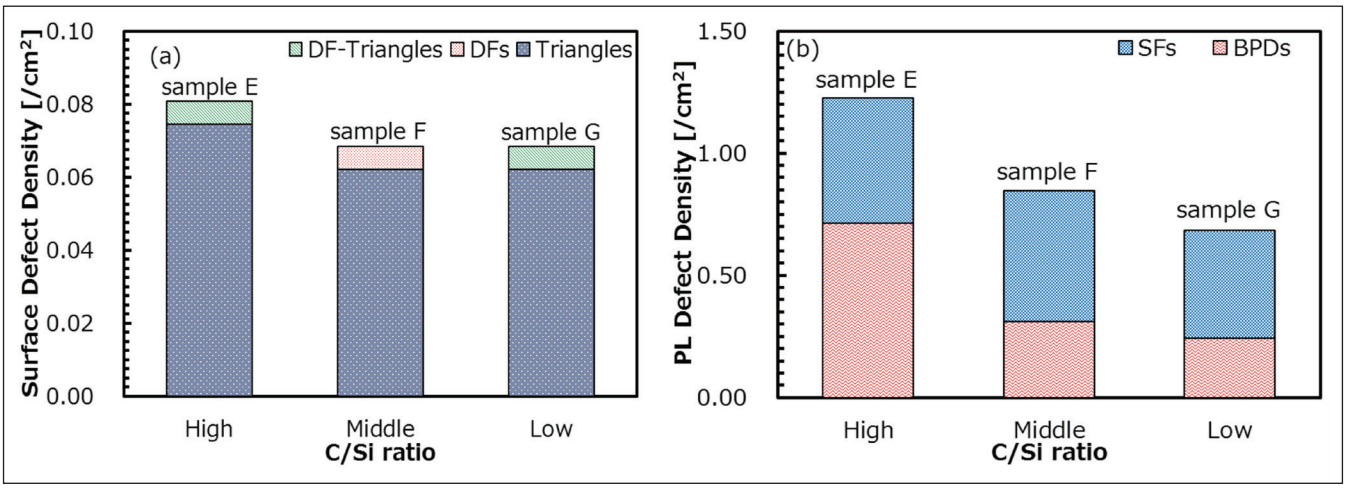


Figure 4. Summary of surface (a) and photoluminescence (b) defect densities of the SiC stacks with a highly *n*-doped buffer layer grown with different carbon-to-silicon ratios. The rotation speed during the temperature ramping was 600 rpm.

three samples, grown with different carbon-to-silicon ratios. This optical technique revealed that in all cases, the surface defect density is negligibly low compared with the crystal structure defect density. In addition, photoluminescence determined that lowering the carbon-to-silicon ratio can reduce basal plane dislocations in the drift layer. Take this approach, and the defect density can be as low as 0.75 cm^{-2}, including DFs, triangles, DF-triangles, stacking faults and basal plane dislocations.

Optimising uniformity

As expected, we have found that our tool's growth rate is fairly proportional to its SiH_4 flow. That's good news, because it indicates a suppression of silicon-cluster formation, thanks to the introduction of HCl into SiH_4 [4]. Using this approach, we can achieve growth rates as high as about 1 μm/min.

By adjusting the position of the gas injection nozzles in the gas inlet, we have been able to fine-tune the distribution of the local gas phase concentration of SiH_4 and C_3H_8 near the wafer surface, along the radial direction. This allows us to tune uniformity of thickness and doping concentration simultaneously, by optimizing the total carbon-to-silicon ratio.

We have realised a growth rate of 54.7 μm/h, with a uniformity of ±2.53 percent (1.75 percent (σ/mean). For doping, the concentration and its uniformity are 5.46 ×$10^{15}$$cm^{-3}$ ±3.24 percent (1.53 percent (σ/mean).

These values, and the defect-related studies, show that our EPIREVO S6 is capable of producing very high quality films of SiC that will aid the makers of power electronic devices.

References

[1] H. Fujibayashi *et al.* Appl. Phys. Express **7** 015502 (2014)

[2] S. Mitani, Compound Semiconductor, volume 22 (2016) issue 4, p 42

[3] H. Fujibayashi *et al*. U.S. Patent, No. US20160138190 A1 (May 19, 2016)

[4] T. Tanaka et al., Materials Science Forum **821-823** 135 (2015)

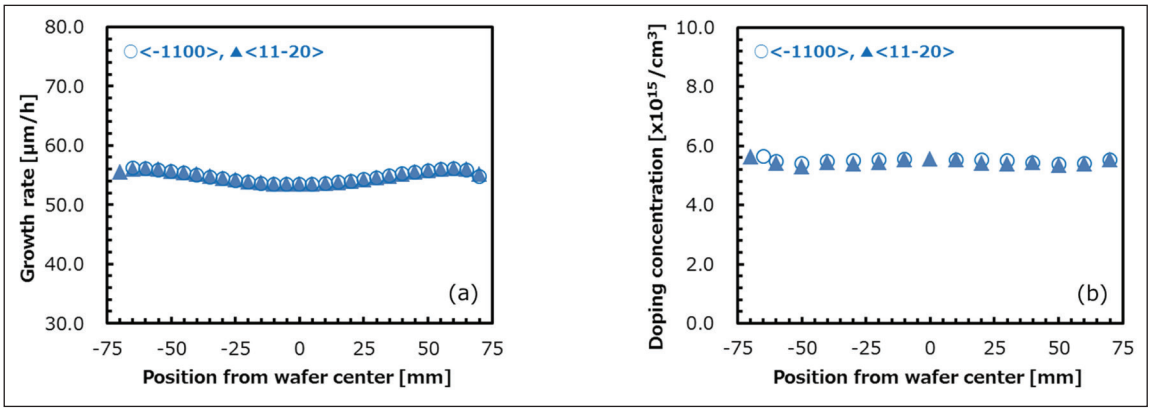


Figure 5. Optimized distribution of growth rate (a) and doping concentration (b) of an *n*-type SiC film.

Connecting the photonic integrated circuits community

PIC Magazine

B2B specialist publisher and event organiser Angel Business Communications, publisher of Compound Semiconductor Magazine and organiser of CS International and PIC International conferences launched in 2016 the sister publication Photonic Integrated Circuits (PIC) Magazine, a quarterly digital magazine which provides timely, comprehensive coverage of every important sector within the photonic integrated circuits industry.

PIC Magazine provides comprehensive coverage of all aspects of this industry, and each issue carries features and research from the full spectrum of the integrated photonics community.

So whether you focus on system integration, developing and manufacturing components, financing this sector, or providing the materials and equipment needed to support this industry, PIC Magazine is your essential magazine.

Editorial themes will cover the entire supply chain to include:

IT
Telecom
Health & Life science
Security & Defence
Manufacturing
Optical Sensing, Lighting & Energy, Displays

Register to receive the magazine free of charge: **www.picmagazine.net/register**

Advertise/Editorial enquiries: **info@picmagazine.net** or call **+44(0)2476 718970**

PIC INTERNATIONAL CONFERENCE

10-11 APRIL 2018
Sheraton Airport Hotel Brussels

Creating and strengthening links between chipmakers and network builders

PIC INTERNATIONAL 2018 CONFERENCE
SPEAKERS ANNOUNCED!

With a record breaking number of speakers and sponsors secured, PIC International 2018 is set to be the biggest and best yet

On Tuesday 10 and Wednesday 11 April 2018 in Brussels at the Sheraton Airport Hotel, PIC International will once again be the must-attend event for the global integrated photonics community.

Highlights include talks by Facebook, Nokia-Labs, imec, PhoeniX Software, Finisar, IBM, NEC Corporation, Hewlett Packard Enterprise, Intel, plus many more...

Delivering over 30 presentations PIC International will provide comprehensive coverage of the PIC industry exploring 5 core themes

- Moving the data: PICs for cloud computing and telecoms
- Refining the PIC: achieving the next milestone in performance
- Delivering the goods: advances in PIC manufacturing
- PIC Design, simulation and packaging: A blueprint for future success
- PIC horizons: new and emerging applications for integrated photonics

For each theme a keynote presentation will be given by the leading decision makers and influencers within the industry.

Book your place NOW!

www.picinternational.net/register to secure your place

It's set to be another sellout

PLATINUM SPONSORS

ColorChip SystemOnGlass · EVG · ficonTEC micro assembly machines · LIGENTEC Light Generating Technologies · LioniX International · LUCEDA PHOTONICS · Multiphoton Optics · PhoeniX Software · PI · SMART PHOTONICS · SYNOPSYS · teem photonics · VPIphotonics · YOLE Développement

GOLD SPONSORS

bay photonics · Fraunhofer Heinrich Hertz Institute · IQE · lumerical · VTT · Yenista OPTICS

MEDIA SPONSORS

DCS Europe Datacentre Solutions · Electro Optics · FIBRESYSTEMS · GO Photonics · Laser Optics & Photonics · Laser Manufacture News · optical connections · optics.org · Photonex · SILICON SEMICONDUCTOR · technology SCOTLAND

WIFI SPONSOR: BROLIS SEMICONDUCTORS

DELEGATE BAG SPONSOR: SMART PHOTONICS

LANYARD SPONSOR: IQE

SUPPORTED BY: EPIC European Photonics Industry Consortium · imec · PIC International magazine

This two day event covers five themes (Speakers announced to date)

Refining the PIC: Achieving the Next Milestone in Performance

What are the leading approaches for integrating key building blocks at the chip-level and how can we bring together electronics and photonics more efficiently?

SPEAKERS

- **Michael Lebby: Lightwave Logic**
  Scalable PIC platforms: The impact of using polymer PICs for 100 and 400Gbps datacom applications
- **Wim Bogaerts: Ghent University/imec**
  Programmable photonic ICs: making optical devices more versatile
- **Luis Henrique Hecker de Carvalho: BrPhotonics**
  Converging photonics and microelectronics: applying advanced technologies to ramp up PIC performance
- **Tan Yong Tsong: Institute of Microelectronics**
  Coupling electronics and photonics – promising paths for device-makers to explore
- **Radha Nagarajan: Inphi**
  Highly integrated silicon photonics to push PICs to the next level
- **Sasan Fathpour: CREOL, The College of Optics & Photonics**
  Silicon photonics beyond silicon-on-insulator - emerging solutions for integrated photonics
- **Yvain Thonnart: CEA-Leti**
  Integrating photonic building blocks towards complete electro-optical computing
- **Shinji Matsuo: NTT Photonics**
  III-V membrane lasers on silicon for datacom and computercom applications

Moving the Data: PICs for Cloud Computing and Telecoms

Data centres and networks need smart solutions to manage the sharp growth in traffic. What can integrated photonics bring to the table and how can developers make sure their products appeal to key customers?

SPEAKERS

- **Vincent Zeng: Facebook**
  PIC opportunities for datacentres
- **Yuichi Nakamura: NEC Corporation**
  Big data analysis - a golden opportunity for silicon photonics
- **Martin Schell: Fraunhofer HHI**
  The Zettabyte is not enough: Volume handling for InP, silicon photonics, and hybrid photonic integration
- **Weiming Yao: JePPIX/PITC**
  III-V photonic integrated circuits for telecoms and beyond
- **Peter Winzer: Nokia Bell Labs**
  Massive array integration and the need for a holistic digital/analog optics/electronics co-design
- **Eric Mounier: Yole Développement**
  Data centre technology - the big PICture, opportunities for energy efficient photonics

PIC Design, Simulation and Packaging: A Blueprint for Future Success

How can we implement ideas faster and what needs to be considered to keep the final device cost on track?

SPEAKERS

- **Peter O'Brien: Tyndall National Institute**
  PIXAPP – Open Access Opportunities for Advanced PIC Packaging
- **Christopher Cone: Mentor Graphics**
  From schematic to layout – overcoming today's PIC design challenges
- **André Richter: VPIphotonics**
  Scalable design of integrated photonic and optoelectronic circuits

PIC Horizons: New and Emerging Applications for Integrated Photonics

How can developers capitalize on opportunities for optical platforms in growth areas such as medical diagnostics, industrial sensing and biological analysis?

SPEAKERS

- **Milan Mashanovitch: Freedom Photonics**
  Low size, weight and power (SWaP) instruments for sensing applications - cutting edge PICs
- **Sascha Geidel: Fraunhofer ENAS**
  Adding the 'tech' to biotech - opportunities for photonic integrated circuits
- **Andrew Sparks: Analog Devices**
  Putting liquid crystal waveguides in the fast lane automotive applications for PICs

Delivering the goods: Advances in PIC Manufacturing

What are the latest tools and techniques that can be deployed in the fab? And what are the options when it comes to evaluating the output?

SPEAKERS

- **Jessie Rosenberg: IBM**
  Inline wafer-scale photonic testing to boost PIC manufacturing efficiency
- **Jack Xu: Finisar**
  Meeting the challenge of producing PICs at high-volume
- **Arne Leinse: LioniX International**
  Silicon nitride based TriPleX PIC modules in a broad range of applications
- **Henk Bulthuis: Kaiam Corporation**
  Vertical integration: bringing key elements together to match PICs to the market
- **Scott Jordan, Physik Instrumente**
  Presentation title TBC

Panel: Has Silicon Photonics got the Required Scalability to Displace InP?
Silicon photonics has attracted the interest of many in large corporations, SMEs, and academics as a potential replacement to the incumbent PIC technology InP. Given these conditions, the question remains to ask if SiP can be truly scalable towards $1/Gbps at 400Gbps data rates and above (for any distance)?
Bert Jan Offrein – IBM
Di Liang - Hewlett Packard Enterprise
Robert Blum – Intel
Sean Anderson – Cisco

Panel: High Volume Transceiver Opportunities for PICs
Will transceivers ever achieve super high volumes to allow scalability in cost and performance, and if so, what would be the common large volume platforms, and more specifically, what would be the transceiver format/form factor?

Aref Chowdhury – Nokia
Drew Nelson – IQE
Vipul Bhatt – Finisar

Removing GaN from GaN

Photoenhanced wet etching of InGaN leads to lift-off of high-quality heterostructures

BY CHRIS YOUTSEY AND ROBERT MCCARTHY FROM MICROLINK DEVICES AND ANDY XIE FROM QORVO

In the early days of the compound semiconductor industry, device production involved the growth of lattice-matched epilayers on GaAs and InP substrates. Now the range of materials has expanded to include GaN, which may be grown on mismatched substrates such as sapphire, SiC and silicon.

For all these material systems, the substrate plays an essential role in the growth process, serving as a crystalline template for building up a device structure, layer by layer. But once the growth is complete, the substrate is merely an expensive handle. It can even be suboptimal, with the device delivering a better performance – such as superior light extraction, reduced weight, enhanced thermal conductivity or increased flexibility – when its layers are transferred intact to a new, better handle.

One way to enjoy these benefits is to mechanically thin the substrate. However, that's not ideal, as it's a destructive process. Better is the use of an epitaxial lift-off (ELO) process, as this does not damage the substrate during the removal of the epilayers. This technique uses a sacrificial release layer that is selectively etched to separate the epitaxial layers from the substrate. By taking this approach, it is possible to reuse the substrate many times, promising considerable cost savings.

For the past ten years our team at Microlink of Niles, IL, has been pursuing this approach by developing an ELO technology for compound semiconductor materials. Our successes during that time have led to the use of ELO in the volume manufacture of inverted metamorphic multi-junction solar cells with a 6-inch diameter. These cells combine an exceptionally high efficiency of more than 30 percent in AM0 conditions with a specific power exceeding 3000 W/kg. The removal of the substrate holds the key to such a high specific power, and it also trims costs through its re-use. The very high efficiencies and specific powers of our cells make them strong candidates for serving the emerging market of high-altitude, long-endurance unmanned aerial vehicles. With this solar technology, flights can last for weeks and even months.

We are now breaking new ground by extending the capability of our technology so that it can be applied to GaN. In this material system we have pioneered the development of a relatively fast wafer-scale photochemical lift-off process that does not have to draw on an exotic material for the release layer – instead, it uses InGaN.

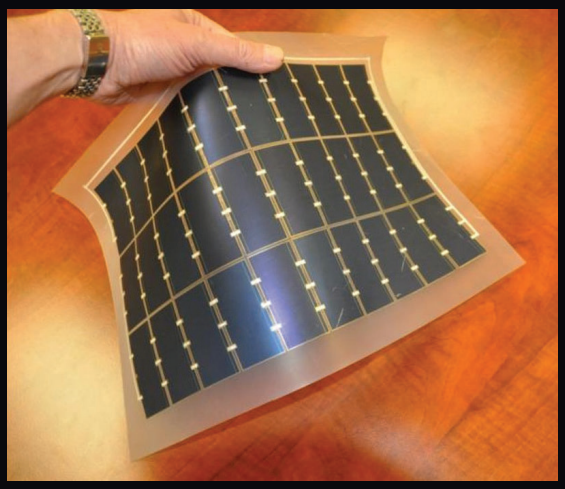


Figure 1. A flexible solar array fabricated using MicroLink ELO multi-junction solar cells (left). High-altitude long-endurance (HALE) aircraft such as the Airbus Zephyr require very lightweight, high-specific-power solar cells enabled by MicroLink's ELO technology (main image).

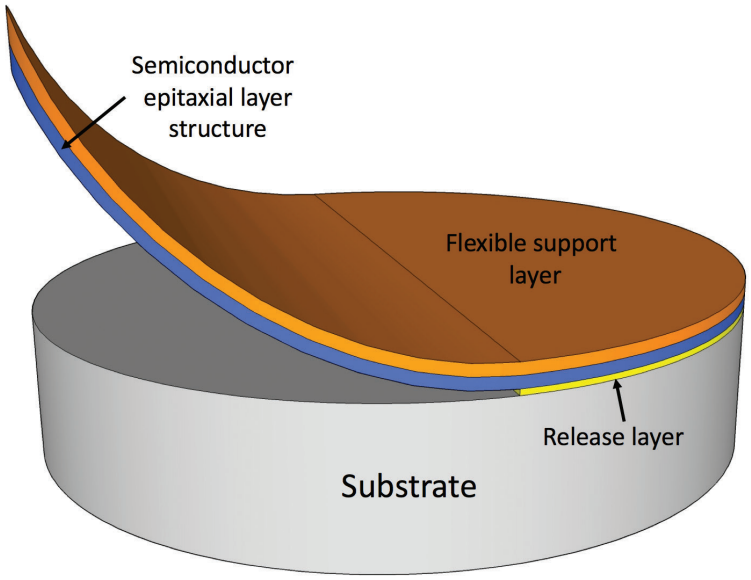


Figure 2. The ELO process begins with an epitaxial structure that has a sacrificial release layer between the substrate and device layers. A flexible carrier is attached to the top of the device layers, and wet chemical etching dissolves the release layer to achieve lift-off.

GaN: Opportunities and challenges

To date, foreign substrates have not hindered the commercial progress of GaN devices, which are second only to silicon in market size. Thanks to the success of LEDs and HEMTs grown on sapphire, silicon and SiC – all these devices perform remarkably well, considering their high dislocation densities that stem from the use of mismatched substrates.

However, despite this success, epitaxial lift-off and layer transfer processes can be a major asset for GaN devices, improving their performance through the use of a native substrate. Many would agree that the widespread availability of high-quality, low-cost GaN heterostructures, grown on native GaN substrates, can lead to a new generation of transformative power devices. They include vertical GaN devices, such as vertical-junction FETs and HBTs, that need low dislocation densities to realise high current densities. Compared with the conventional silicon power devices, these power switches, which are based on vertical GaN architectures, will deliver a far lower on-resistance and a much higher operating frequency. These strengths will propel efficiency to new highs.

With GaN-on-GaN device technology, epitaxial lift-off is highly synergistic. The primary motivation is economic; GaN substrates are inherently expensive, and substrate reuse after the ELO process promises to slash substrate costs.

However, just as important as the cost savings is the ability to transfer the device to a substrate with superior thermal characteristics. That's because the performance of a high-power GaN-on-GaN device is then limited by the thermal conductivity of the native GaN substrate. The improved thermal performance that results from layer transfer can enable either an increase in power densities or a trimming of die size. According to our modelling, when a GaN vertical-junction FET is fabricated with an ELO process, this improvement can trim the chip size by more than 50 percent.

In addition to the benefits associated with the use of ELO from native GaN substrates, this technology can separate an LED from its sapphire substrate. This step, which increases light extraction, is normally accomplished by laser lift-off. A high-power laser is rastered over the wafer, vaporising the interface between GaN and sapphire. With our ELO process, there is far less damage at the interface, and lift-off can take place at the wafer scale.

Realising release

With any ELO process, the central challenge is to identify a suitable material for the release layer. This layer is inserted between the substrate and the active layers of the device, and sacrificially removed using wet chemical etching, to enable lift-off.

The release layer must fulfil several key requirements: it must be etched with high selectivity to prevent damage to the surrounding substrate and device

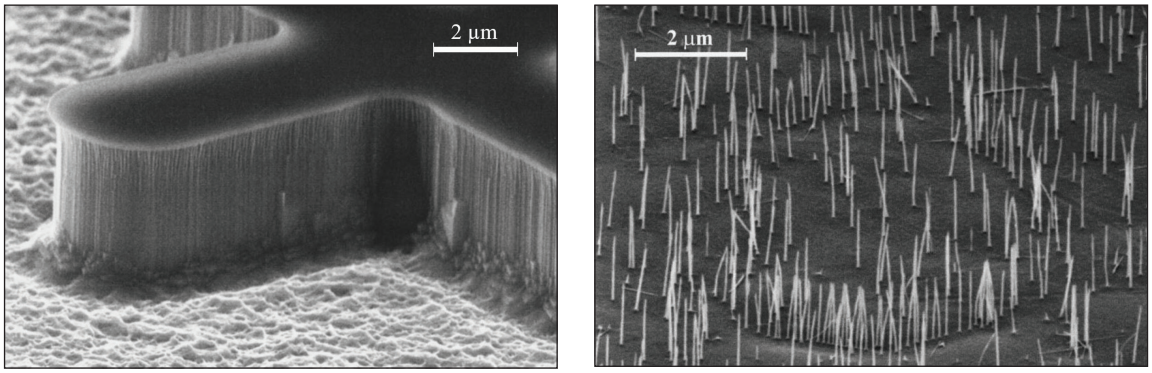


Figure 3. GaN is resistant to conventional wet etchants, but ultraviolet illumination can enable rapid photoenhanced wet etching. On the left is shown a cross-shaped feature, etched 5 μm deep by photoenhanced wet etching using a titanium metal etch mask. Under certain conditions, the etch process can be highly selective to material defects. The image on the right shows threading dislocations, revealed as 'whiskers' formed by photoenhanced wet etching of a GaN-on-SiC structure. Reproduced from C. Youtsey *et al*. Appl. Phys. Lett. **71** 2151 (1997) and C. Youtsey *et al.* Appl. Phys. Lett. **74** 3537 (1999)

layers; it must have a high enough lateral etch rate to ensure that it does not take too long for large areas to be released; and its insertion must not degrade the quality of the material grown on top of it.

Applying ELO to GaAs materials is relatively easy. In this case, AlAs and InGaP can be used as lattice-matched release layers, which can be etched with a very high selectivity relative to GaAs. With GaN, however, the situation is far more tricky, because the usual rules do not apply to nitride materials.

Due to the high bonding strength between atoms in the crystal, group-III nitrides are highly impervious to the conventional wet etchants commonly used to etch other III-V semiconductors. Etching is possible, however, by using energetic radiation to break bonds in the crystal. This is accomplished by illuminating nitride semiconductors with ultraviolet light during etching. Photogenerated electron-hole pairs enhance this process.

We have shown that photoenhanced wet etching of GaN can produce a vertical etch profile, thanks to the directional nature of the incident illumination (see Figure 3, left, which shows a 5 μm deep etch with potassium hydroxide, on a cross-shaped feature with a titanium metal etch mask). By turning to different conditions, our etching process can be made highly selective to dislocations threading through the GaN material (see Figure 3, right, which reveals GaN material etched away around the threading dislocations. They have a very high density around 10^9 cm^{-2}, due to the epitaxial growth on a SiC substrate.)

The release layer that we have chosen for our GaN ELO process exploits an effect known as bandgap-selective etching. When the sample is illuminated from the backside, light passes through the substrate and is absorbed in the lower bandgap InGaN release layer, where photoenhanced wet etching takes place (see Figure 4). Note that this approach works equally well for GaN structures that are grown on sapphire substrates, which are also transparent.

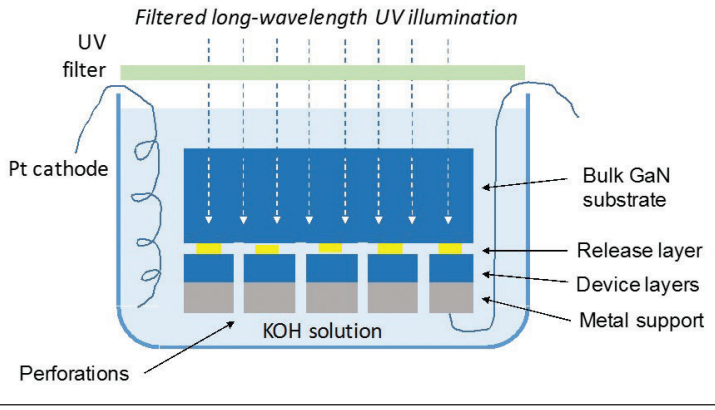
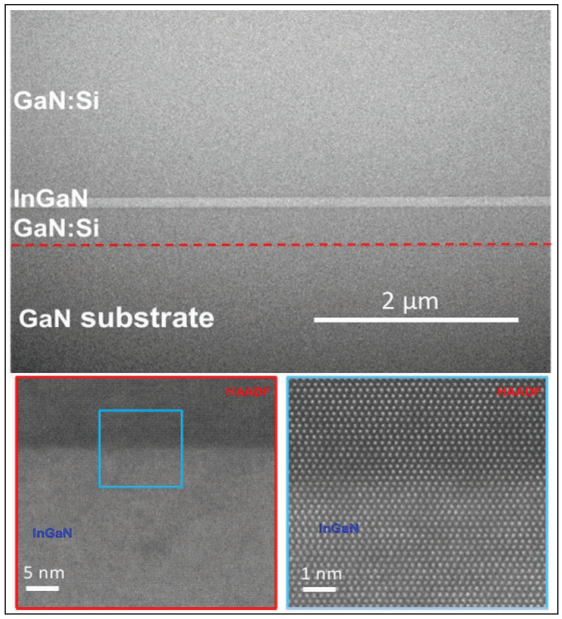


Figure 4. MicoLink's approach to ELO of GaN is based on bandgap-selective, photoenhanced wet etching using an InGaN release layer. Filtered UV illumination is transmitted through the backside of the GaN substrate and absorbed in the InGaN release layer (shown in yellow), driving selective etching of that layer. The frontside of the wafer is metallized and patterned with perforations to accelerate the ELO process. Reproduced from C. Youtsey *et al*. Phys. Status Solidi b, 10.1002/pssb.201600774, (2017)

One of the benefits of using a release layer made from InGaN is that this ternary is a standard alloy, so growth conditions for MBE and MOCVD are well known. Although there is a small mismatch with GaN, if the layer is thin enough it can be grown in a pseudomorphic manner, preventing the introduction of any new dislocations into the device structure that is grown on top. This absence of defects is demonstrated in a scanning transmission electron



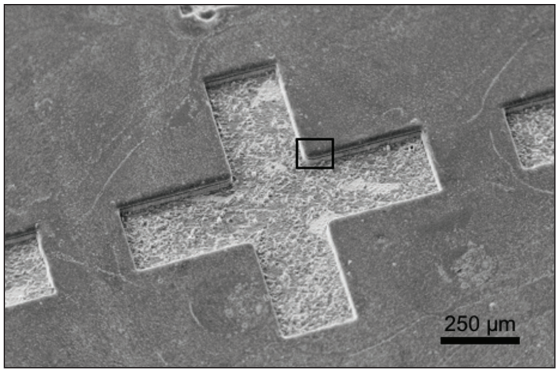


Figure 5. A cross-sectional, scanning transmission electron microscopy image of a GaN-on-GaN ELO epitaxial structure with an InGaN release layer. The interface between the GaN substrate and epitaxial layers is shown with a red dashed line. The material grown above the release layer is free of defects and has high-quality interfaces. Reproduced from C. Youtsey *et al.* Phys. Status Solidi b, 10.1002/pssb.201600774, (2017)

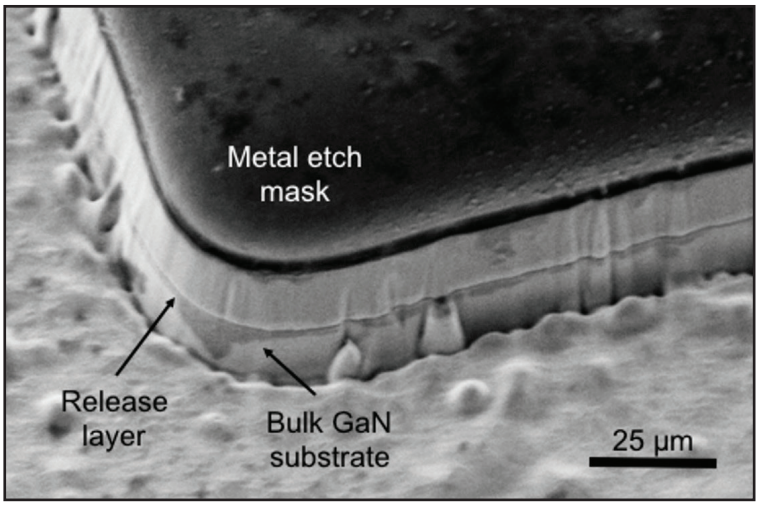


Figure 6. After growth of the GaN epitaxial structure, a metal support layer is applied to the top of the wafer. Cross-shaped perforations, patterned in the metal layer, are etched through the epi structure down to the release layer, as shown in the top scanning electron microscopy image. The high-magnification image on the bottom shows the vertical sidewall of the etched perforation, with the release layer interface clearly visible. Reproduced from C. Youtsey *et al.* Phys. Status Solidi b, 10.1002/pssb.201600774, (2017)

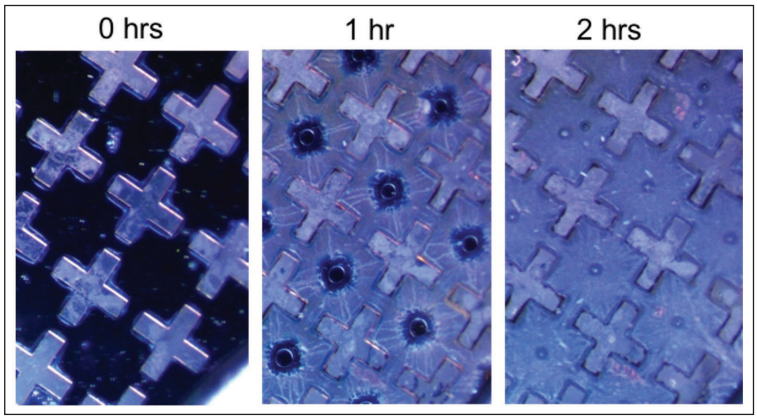


Figure 7. The lateral etching of the release layer during the ELO process can be directly observed through the transparent GaN substrate. Shown are images taken after zero, one and two hours of etching. The film has partially released after one hour (the dark regions at the centre of each unit cell are unetched), and has completely lifted off after two hours. Reproduced from C. Youtsey et al. Phys. Status Solidi b, 10.1002/pssb.201600774, (2017)

microscope image of a GaN/InGaN ELO structure grown on a bulk GaN substrate (see Figure 5).

After we grow the full epitaxial device structure, including the release layer, we add a thick metal support layer to the topside of the wafer. This metal layer provides mechanical support to the GaN film after it has been fully released, as well as electrical contact to the GaN. During the etch process, electrons are conducted from the metal support layer to the platinum counter electrode in the potassium hydroxide etch solution. The metal layer is patterned with cross-shaped perforations (see Figure 6), typically on a 1-4 mm pitch. The perforations accelerate the removal of large, wafer-scale films by enabling etching to occur from many locations across the wafer. Photoenhanced wet or dry etching transfers the perforation patterns through the entire epi structure and into the bulk GaN, to enable access of the etching solution to the buried release layer (such structures are shown in Figure 4). If our device structure contains InGaN layers with a similar indium composition to the release layer, we modify our process – prior to etching, we passivate the sidewall of the etched via hole with a dielectric layer. This prevents unintentional etching of the device layers during the ELO process.

Thanks to the optical transparency of the GaN substrate, the ELO process can be seen in real time (see Figure 7, which shows a sequence of images). After one hour there is material still to be etched – it is visible as dark diamonds, at the centre of each 1 mm x 1 mm unit cell – but after two hours the film has been fully released. While etching is relatively slow compared to other device fabrication steps, the ELO process is low cost, and can be performed in large batches to achieve high throughput.

We have used our ELO technology to completely remove a 4-inch GaN epitaxial layer from a 4-inch sapphire substrate (see Figure 8). The film of GaN, just 5 µm-thick, is supported by the metal backing layer.

Our ultimate objective is to realise the lift-off of GaN films from native GaN substrates. This has been accomplished, using 2-inch GaN substrates made by the SCIOCS Company Limited and Sumitomo Electric, Inc, using cross-shaped perforations with a 1 mm pitch (see Figure 9).

Device demonstration

Following our demonstration of the capability of ELO to remove full-wafer films of GaN, we have gone on to validate the quality of the lifted-off GaN material through the fabrication and testing of devices in Patrick Fay's research group at the University of Notre Dame. This effort began with the fabrication of planar

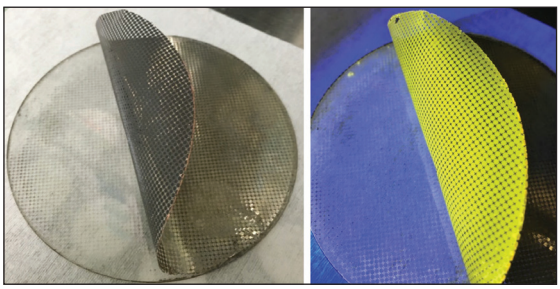


Figure 8. Shown is a GaN film fully released from a 4-inch sapphire substrate, supported by the frontside metallization. Under UV illumination the GaN material luminesces bright yellow-green, as seen on the right. Reproduced from C. Youtsey *et al*. Phys. Status Solidi b, 10.1002/pssb.201600774, (2017)

Schottky diodes on GaN-on-sapphire structures (see Figure 10).

Reverse-bias current-voltage plots on a diode before and after the ELO process show a fall in leakage after lift-off of more than an order of magnitude (see Figure 10). Results were obtained by fabricating and testing the diode on the original substrate, and then encapsulating it with metal, applying the lift-off process, bonding the device to a new carrier using an insulating adhesive, and then retesting it after the removal of the metal support layer.

Dislocations in the device account for the dramatic reduction in the reverse-bias leakage current after ELO and layer transfer. The dislocations are prevalent, due to growth on sapphire, with vertical dislocations intersecting both the ohmic and Schottky contact pads (as illustrated in Figure 11). As these dislocations can be conductive, high-power vertical GaN devices must have a low dislocation density to work well. That's not the case prior to the ELO process, due to a conductive path that threads between the Schottky and ohmic contact pads, and laterally through the n^+ GaN layer beneath the release layer. The lateral current path through the n^+ GaN layer is eliminated after ELO. Leakage is then far lower, thanks to the bonding of the device to an insulating carrier.

We have also fabricated and tested *p-n* junction diodes, using GaN-on-GaN structures. These devices, which have a planar contact structure that is similar to that for the Schottky diodes, produce a very similar reverse leakage current before and after the ELO process (see Figure 12). This is not surprising, given that the dislocation density in the bulk GaN substrates is in the range of 10^6 cm^{-2}, which is at least three orders of magnitude lower than that for GaN-on-sapphire. No defect-related leakage current mechanisms were observed in these diodes.

From now on we will focus on optimising the bulk GaN substrate reclaim process, and establishing how many times a substrate can be reused. Working in collaboration with Sumitomo Electric, Incorporated, we have already successfully reclaimed a bulk GaN

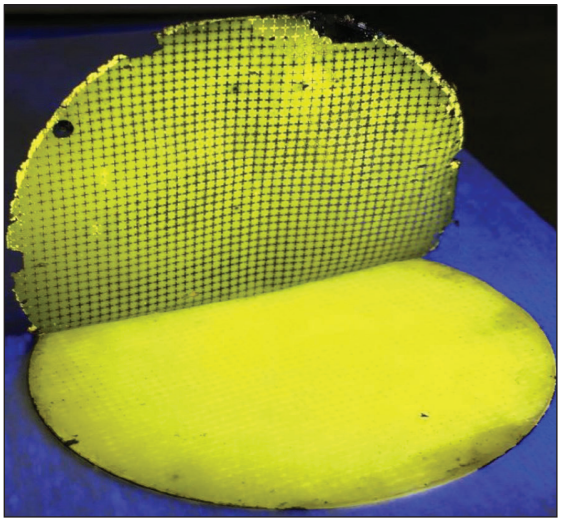


Figure 9. Epitaxial lift-off from a 2-inch bulk GaN wafer. Yellow luminescence is emitted from both the released GaN film on top and the GaN substrate beneath.

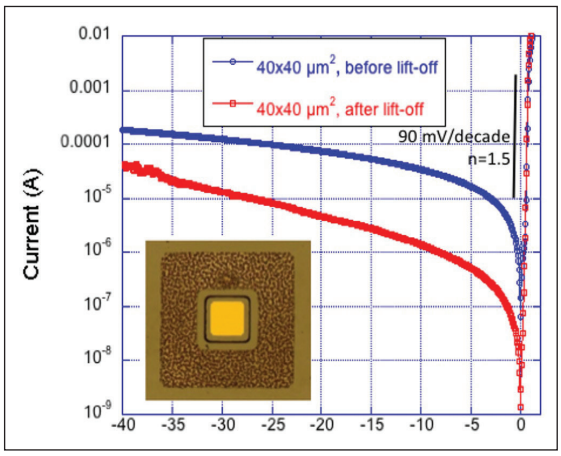


Figure 10. Current-voltage (I-V) curves for GaN-on-sapphire Schottky diodes measured before lift-off (blue curve) and after lift-off (red curve). The diodes feature a square Schottky contact in the centre and an annular ohmic contact around the perimeter. Permission for reproduction granted by IEEE. Reproduced from J. Wang *et al*. in: Proceedings 74th Annual Device Research Conference (DRC), Newark, DE, 2016, pp: 1 – 2.

Dislocations in the device account for the dramatic reduction in the reverse bias leakage current after ELO and layer transfer. The dislocations are prevalent, due to growth on sapphire, with vertical dislocations intersecting both the ohmic and Schottky contact pads. As these dislocations can be conductive, high-power vertical GaN devices must have a low dislocation density to work well

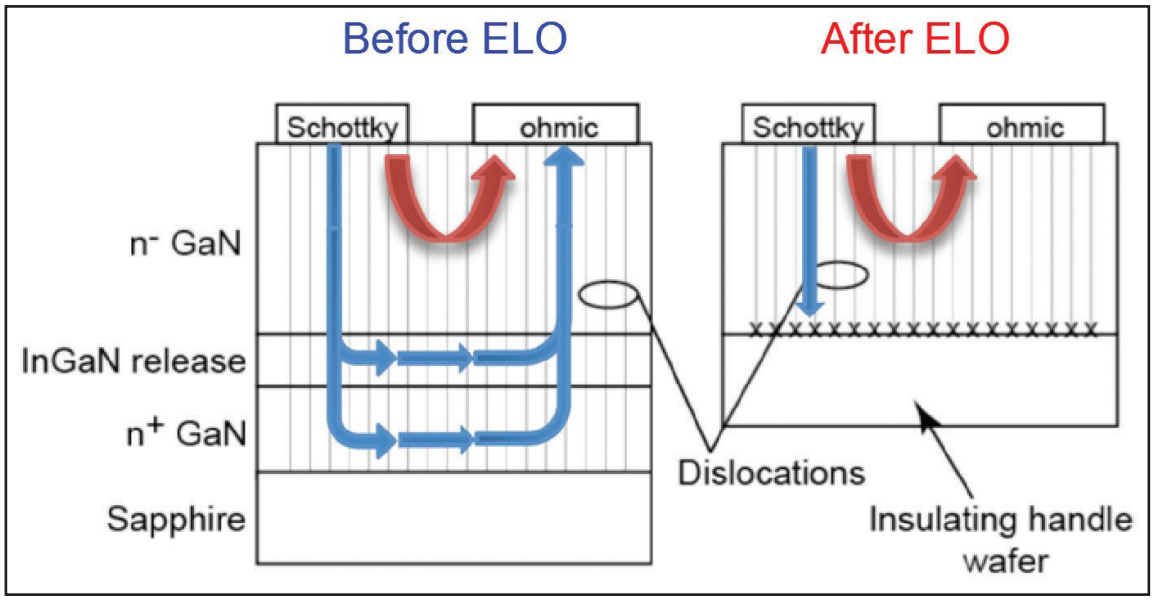


Figure 11. Dislocations provide a vertical current path for leakage between the Schottky and ohmic contacts, with a lateral current path through the n^+ GaN layer beneath the release layer (shown near right). After ELO, the lateral current path has been removed, leading to the reduced leakage current (far right). This illustrates the importance of low-dislocation density bulk GaN for vertical power devices. Permission for reproduction granted by IEEE. Reproduced from J. Wang *et al.* in: Proceedings 74th Annual Device Research Conference (DRC), Newark, DE, 2016, pp: 1 – 2.

substrate after ELO. Results will be published shortly. Our initial estimates indicate that a substrate can be reused at least five to ten times. If that's the case, this will slash the effective substrate cost.

Another of our goals is to develop effective methods for bonding lifted-off films to new substrates with high thermal conductivity. These new processes will be integral to a GaN ELO technology that has the potential to substantially improve the economics and performance of GaN-on-GaN power and optoelectronic devices.

The authors are grateful for support provided by the ARPA-E SWITCHES program under grant number DE-AR0000446 (program managers Tim Heidel and Isik Kizilyalli). We'd also like to acknowledge the work of our team members. GaN epitaxial layer structures in this project were grown by Andy Xie and Ed Beam at Qorvo, Inc., and Professor Louis Guido at Virginia Tech. Device fabrication and testing was carried out at the University of Notre Dame by Jingshan Wang and Professor Patrick Fay. Rekha Reddy at MicroLink Devices developed GaN layer transfer and bonding processes.

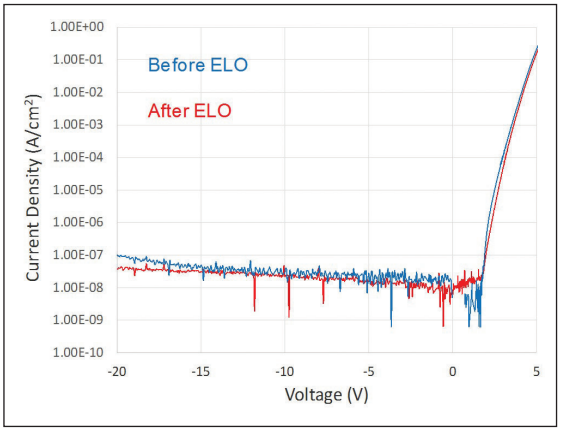


Figure 12. Current-voltage (I-V) curves for GaN *p-n* diodes grown on bulk GaN substrates, measured before and after epitaxial lift-off. No change in device performance was observed during the layer transfer process. Reproduced from C. Youtsey *et al*., in: Proceedings CSMANTECH Conference, Indian Wells, CA, 2017

Further reading

D. Cardwell *et al.* in: Proceedings 44th IEEE Photovoltaic Specialists Conference, Washington, D.C., 2017
I. C. Kizilyalli *et al.* IEEE Trans. Electron Dev. **62** 414 (2015)
C. Youtsey *et al.* Appl. Phys. Lett. **71** 2151 (1997)
C. Youtsey *et al.* Appl. Phys. Lett. **74** 3537 (1999)
A. Rajan *et al.* J. Phys. D: Appl. Phys. **49** 315105 (2016)
D. Meyer *et al.* IEEE Trans. Semicond. Manuf., **29** 384 (2016)
D. Hwang *et al.* Opt. Express **24** 22875 (2016)
C. Youtsey *et al.* Phys. Status Solidi b, 10.1002/pssb.201600774, (2017)
C. Youtsey *et al.* in: Proceedings CSMANTECH Conference, Indian Wells, CA, 2017
J. Wang *et al.* in: Proceedings 74th Annual Device Research Conference (DRC), Newark, DE, 2016, pp: 1 – 2.

Book your place at the third

Photonic Integrated Circuits Conference

Tuesday 10 & Wednesday 11 April 2018

Sheraton Brussels Airport Hotel, Belgium

Co-located with CS International Conference & High-End Sensors International

FIVE KEY THEMES:

Over 30 inspiring presentations

- Moving the data: PICs for cloud computing and telecoms
- Refining the PIC: achieving the next milestone in performance
- Delivering the goods: advances in PIC manufacturing
- PIC Design, simulation and packaging: a blueprint for future success
- PIC horizons: new and emerging applications for integrated photonics

Book your place NOW!

www.picinternational.net/register to secure your place

It's set to be another sellout

PLATINUM SPONSORS

ColorChip SystemOnGlass · EVG · ficonTEC micro assembly machines · LIGENTEC Light Generating Technologies · LioniX International · LUCEDA PHOTONICS · Multiphoton Optics · PhoeniX Software Solutions for Micro and Nano Technologies · PI · SMART PHOTONICS · SYNOPSYS · teem photonics · VPIphotonics Design Automation · YOLE Développement

GOLD SPONSORS

bay photonics · Fraunhofer Heinrich Hertz Institute · IQE · lumerical · VTT · Yenista OPTICS

MEDIA SPONSORS

DCS Europe Datacentre Solutions · Electro Optics · FIBRESYSTEMS · GO Photonics · Laser Optics & Photonics · Laser Manufacture News · optical connections · optics.org · Photonex · SILICON SEMICONDUCTOR · technology SCOTLAND

WIFI SPONSOR: BROLIS SEMICONDUCTORS

DELEGATE BAG SPONSOR: SMART PHOTONICS

LANYARD SPONSOR: IQE

SUPPORTED BY: EPIC European Photonics Industry Consortium · imec · PIC International magazine

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

HES INTERNATIONAL CONFERENCE

10-11 APRIL 2018
Sheraton Airport Hotel Brussels

Connecting, informing and inspiring the HIGH END SENSOR industry

HIGH END SENSORS INTERNATIONAL CONFERENCE 2018

The inaugural High End Sensors conference will be held at the Sheraton Airport Hotel in Brussels on 10 -11 April 2018. HES International will be held alongside CS international and PIC International.

High-end sensor devices are an increasingly significant share of the global machine sensory market that is expected to exceed 30 billion devices by 2020 with revenue of (USD) $20 billion. We will explore opportunities for the most advanced sensors that deliver higher performance, ruggedness and longer operational lifetimes. We will examine new technologies that are cutting costs while increasing effectiveness. We will explore product development within major high-end sensor categories and ways that researchers and manufacturers are investigating to enhance performance, reduce power consumption, and improve efficiency.

Two days, 10 topics, over 25 inspiring presentations

The presentations will be based around ten topics which collectively provide complete coverage of the high-end sensor market.

- Defence, Security, Aviation and Aerospace High-End Sensors
- Imaging and Optical Sensing Advances
- Maximizing Sensor Data Acquisition and Analysis
- Optimizing IoT and IIoT Sensor Networks and Security
- New Approaches for Power Control and Energy Harvesting
- Radar and LiDAR Innovations
- Advances in MEMS Sensor Development
- Metrology and Test for High-End Sensors
- Enhancing Sensor Performance: Embedded, SoC and Machine Learning
- Emerging Opportunities and Applications

https://highendsensors.net/home

- Bernhard Straub **Infineon Technologies**
- Rainer Minixhofer **AMS AG**
- Tristan Rousselle **Aryballe Technologies**
- Henry White **BAE Systems**
- Pierre-Damien Berger **CEA-Leti**
- Nicholas Burgwin **Fibos**
- Wilmuth Muller **Fraunhofer IOSB**
- Richard Dixon **IHS Markit**
- Denis Pasero **Ilika Technologies**
- Wim Van Thillo **imec**
- Marianne Vandecasteele **imec**
- Sergey Yurish **IFSA**
- Speaker TBC **IST AG**
- Sergio Nicoletti **MIRPHAB**
- Johan Pedersen **Sigma Designs**
- Speaker TBC **Evatec**
- Pim Kat **Technobis**
- Peter O'Brien **Tyndall National Institute**
- Iwan Davies **VIDaP Consortium**
- Iñigo Artundo **VLC Photonics**




Book your place NOW!

It's set to be a sellout

CS INTERNATIONAL CONFERENCE

The 8th CS International conference will build on the success of its predecessors, with industry-leading insiders delivering more than 30 presentations spanning five sectors.

Together, these talks will detail breakthroughs in device technology; offer insights into the current status and the evolution of compound semiconductor devices; and provide details of advances in tools and processes that will help to drive up fab yields and throughputs.

Attendees at this two-day conference will gain an up-to-date overview of the status of the CS industry, and have opportunities to meet many other key players within this community.

PIC INTERNATIONAL CONFERENCE

Photonic Integrated Circuits International

Sales of PICs are soaring, with their deployment helping to boost the capacity of networks and data centres. To aid this industry, we are strengthening the relationships between the makers and the users of these integrated circuits by organising the 3rd PIC International, a global conference dedicated to this industry.

Attendees to the conference will hear industry-leading insiders delivering more than 30 presentations spanning five sectors. The conference will equip the delegates with an up-to-date overview of the status of the PIC industry, and provided them with many opportunities to meet other key players within this community.

3/2/1 Register for one conference and gain access to **THREE** cutting edge complimentary events plus **ONE** dedicated exhibition featuring leading industry players from across the globe.

Registration at one conference allows access to all other conference sessions

PLATINUM SPONSORS

evatec process systems

IST INNOVATIVE SENSOR TECHNOLOGY

MEDIA SPONSORS

GeoConnexion

inVISION

sensorland.com

WIFI SPONSOR

BROLIS SEMICONDUCTORS

SUPPORTED BY

CS COMPOUND SEMICONDUCTOR

化合物半导体 CHINA

EPIC European Photonics Industry Consortium

IFSA

PIC INTERNATIONAL magazine

SILICON SEMICONDUCTOR

Accelerating the production ramp

When customers come knocking at your door, wanting massive quantities of your products in just six months, can you quickly react, change, and deliver by the deadline?

BY MARIO FARIA, ILIA KAPLAN, AND ARIEL MEYUHAS FROM THE MAX GROUP

MARKETING CAMPAIGNS encourage us to go out and buy the latest gizmos and gadgets. For those of us that want to have the latest laptop, every two years a new model will come out and tempt us, sporting attractive functions and better performance. New generations of camera come around even faster, at typically every 18 months, while new iPhones are launched every year – and right now, even faster than this – and for Androids, less than a year is already the norm.

The rapidity of launches of electronics goods, often too much fanfare that drives healthy pre-orders, puts a great deal of pressure on component suppliers. They include the makers of compound semiconductor chips used for connectivity that have to ramp production fast without compromising product margins. And they cannot afford significant time-to-supply delays, as this could jeopardize their position as a top-tier supplier, by missing out on contracts in years that come. Avoid all this and it is still possible to run into problems: companies tend to deal with shorter cycles by over-stocking finished products, and when these don't sell, profit margins head south.

The good news, however, is that with a carefully planned approach it is possible to avoid all these pitfalls. And one manufacturer of compound semiconductor chips has recently done just that, thanks to support by our team at The MAX International Engineering Group, a company based on Old Tappan, NJ, that has expertise in operations improvement, new facility design and build, and management consulting. After working together, we ramped the factory output by 250 percent.

Our expertise has taught us that manufacturing agility is critical to achieving shorter time-to-supply cycles in environments where manufacturing takes place alongside development – a typical situation in a compound semiconductor fab. To realise sufficient manufacturing agility, often a culture change must take place, with a shift of emphasis away from a development-centric mentality, to one that focuses on manufacturing-centric practices.

Ideally both cultures are already co-existing during the development and ramp-to-volume phases in manufacturing. But if they are not, we work with clients, taking them on a managed and expedited path to benchmarked operational excellence and significantly shorter time-to-supply cycles.

During the last ten years, we have worked with many compound semiconductor manufacturers, deploying approaches to increase manufacturing agility. These methods focus on addressing the three key pillars required for any successful, high-volume compound semiconductor chipmaker: operational practice, engineering practice and organisational structure. Excelling in all three areas produces pillars that provide a foundation for growth, flexibility and a manufacturing-centric infrastructure. The result is a cohesive team, aligned around applicable key-performance indicators, that can create a very highly focused organisation that is underpinned by precision of teamwork, standard work methods and execution in planning, operations, and engineering.

Increasing operation efficiency

Our first step, associated with the first pillar, involved increasing the operational efficiencies of the compound semiconductor chipmaker. We began with this, because operational changes yield faster results than activities related to engineering or organizational changes. We assessed, made recommendations and implemented new approaches in many different areas, including those associated with: key-

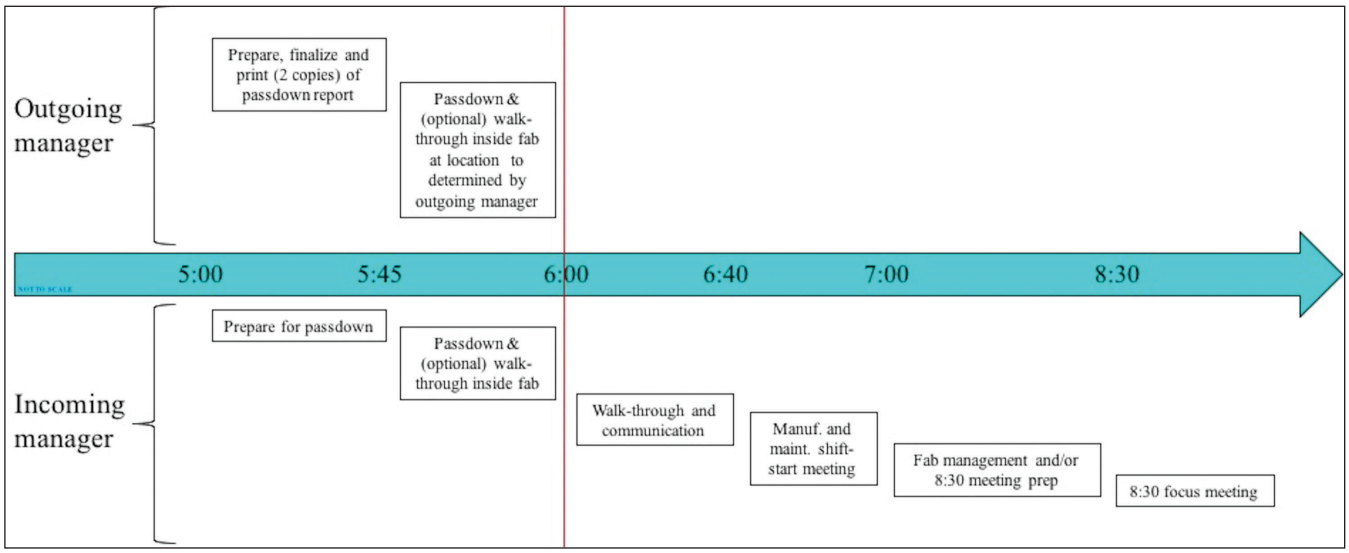


Figure 1: Daily detailed shift schedule for Production Managers

#	Duration (min)	Category	Topic	Details	KPI	New Item?
1	5	General	Safety	Major events (accidents or incidents)	n/a	Yes
2			Quality	Excursions or major scrap	n/a	Yes
3	15	Last 24-hour performance	**Past**: last 24 hours of major items and lingering effects - After a holiday and/or weekend, include the performance since the last regular business day - Highlight the impact from disruptions / interruptions such as facilities work	Key tools (metrology, pinch-points, etc), DefCon4, potential DefCon4	Availability	No
4					Moves	No
5					Drumbeat	No
6					UPH losses	Yes
7					Dispatch compliance	Yes
8					Utilization or idle with WIP	No
9		Present situation	**Present**: current line conditions	WIP and mix conditions and impact	WIP distribution, quantity (delta to target) and mix	No
10					Priority lots	No
11					Held lot > 24hrs	No
12					Aging WIP	Yes
13				Key tools (metrology, pinch-points, etc), DefCon4, potential DefCon4	Key tool status and ETAs	No
14		Next 24-hour performance	**Future**: next 24-hour forecast performance highlighting major activities and their impact - Include any expected performance during an upcoming holiday and/or weekend - Impact of upcoming projects or tasks such as tool install/moves, disruptions / interruptions and/or facilities work	Upcoming PMs, long/difficult repairs, holiday shut-down, tool install/moves, or facilities work	Moves	No
15				Staffing	Manuf., maint., PTs, LTs, engineers	Yes
16				Proactive or key plans, such as preparing for a WIP bubble and any recovery effort	WIP re-balance duration	Yes
17				Review and align on priorities	n/a	Yes
18	5	Other	Additional topics	Escalations	n/a	No
19				Action items	n/a	No
20				Request for help or support	n/a	Yes

Figure 2. Dynamic Snapshot of Tools Idle with WIP – Highlights Equipment ready to process but missing inventory

performance indicators; roles and responsibilities; work-in-progress management; factory management and supervisory effectiveness; line balance and dispatch; industrial engineering practice benchmarking; shift escalation, rounds, and passdowns; break management; hot and hold lot policies; and six-sigma and quality policies.

All these areas are covered by our highly renowned and successful SuperKit tool, which we have perfected during its use in over 60 fabs all over the world. Using SuperKit, we were able to identify several opportunities to improve the management of the fab, and could recommend how to implement the solutions. In addition, we could manage the implementation of many of these suggestions for improvement.

To start, we established a shift agenda for supervisors and a clear production meeting agenda to followed by a detailed description of frequent routines to monitor constraint areas and toolsets. Figure 1 illustrates an example. Our customer was busy hiring and training new supervisors, operators, and technicians to be able to support their ramp. They relied on organically grown knowledge on how to run shifts, production meetings, and setting expectations on the production floor.

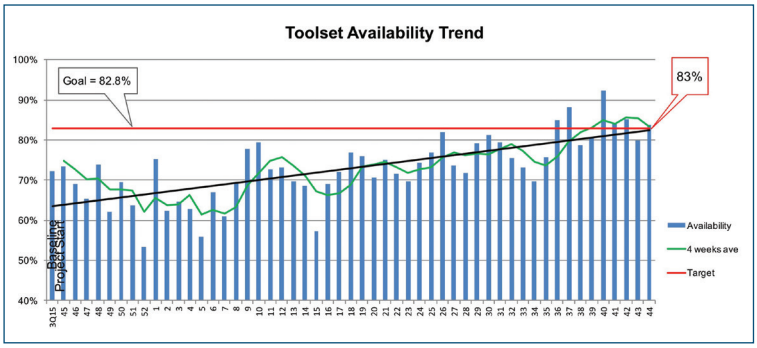


Figure 3. The use of MAX Group's Precision Maintenance Programs enabled a 24 percent improvement over a 12-month period in the output of critical PVD toolsets.

Gaps were discovered, highlighting little continuity work and standard work from shift to shift. We also observed that supervisors managed their shifts to their personal style and lacked common prioritization to daily key-performance indicators, and production meetings were not efficient and served as a forum to present information to management. All of these issues required change, with our SuperKit providing the ideal tool.

In any strong manufacturing organization, the use of key performance indicators drives a level of expectation. In the compound semiconductor fab we recently worked with, we focused efforts on implementing indicators that matter to those that are operating and maintaining the tools, and characterising wafers and devices. Here, key performance indicators are easy to establish, and they help to set a higher level of efficiency when it comes to manufacturing performance. In this case, the focus was directed at wafer output, with critical toolsets coming under scrutiny, using key performance indicators to monitor overall equipment effectiveness (OEE) losses and identify opportunities for improvement within work-in-progress inventory management.

Improving engineering and maintenance

Following our efforts at improving operational practices, we turned our attention to the second of these pillars, engineering and maintenance. In these realms changes are harder to implement, and the benefits take longer to appear.

Working with the compound semiconductor chipmaker, we considered the availability of equipment for some critical process toolsets that are bottlenecks to production. Our efforts involved measuring and improving maintenance effectiveness, using our own Precision Maintenance Programs.

The two outcomes we sought were to increase the equipment availability, and to increase the coefficient of variation of availability – that is, the variability of availability. Success on both fronts led to higher output on critical PVD toolsets in the fab (see Figure 3).

Another way that we looked at availability involved applying our own scoring methodology specific to every preventative maintenance event. This gives the Perfect PM Score, or, for short, the P-Score. The P-Score categorizes planned maintenance work as follows: preventative maintenance planned or unplanned, target interval between preventative maintenances sustained or not, event achieved first time right or not, failures right after the event or not, and next planned event performed per target or not. For root cause analysis we used a 5Y methodology, a known method to derive cause-and-effect. We would drill-down to every category, and scrutinise cause and effect, before determining the corrective actions needed to deliver continuous improvement.

We have also made several recommendations related to equipment and maintenance practices. These vary from improving the engineering and technician skills of fab maintenance teams to the successful management of spare-parts; and the efficient leadership of the site, to take it from an R&D/engineering-centric mindset to one emphasizing high-volume manufacturing. To ensure effectiveness, we worked with the fab when defining the most important items for our team to focus on. Together, we developed a matrix of activities for us to deliver best-practices, and make sure that the fab adapted within its culture.

Enhancing organisational effectiveness

The third and final pillar for improving the capability of a fab to ramp production quickly and successfully is to excel with organisational effectiveness. We adopted a four-pronged strategy to ensure excellence in this regard. This involved: identifying organisational strengths and weaknesses; evaluating the leadership skills of the fab management team and making recommendations for improvement; suggesting a set of metrics to be adopted by senior management; and defining a roadmap to transform the organization from R&D to high-volume manufacturing – that is, to undergo a cultural change.

To undertake this assessment, we held discussions with the site manager, six senior managers, 14 mid-level managers, supervisors and individual contributors. We also observed many different types of meeting and witnessed decision-making processes and responses crisis and conflicts. What's more, we reviewed samples of key documents, including project plans, organisational charts, repeatability and reliability studies, and roadmaps.

A key finding that emerged from all of this effort is that the focus of the compound semiconductor fab was on R&D. That's not surprising, as it is a typical position for most compound semiconductor companies, which will eventually evolve from having an emphasis on technology to a balance between R&D and manufacturing. To drive a shift in culture, we placed the chipmaker into an agreement matrix, which is a chart that measures leadership, power, management,

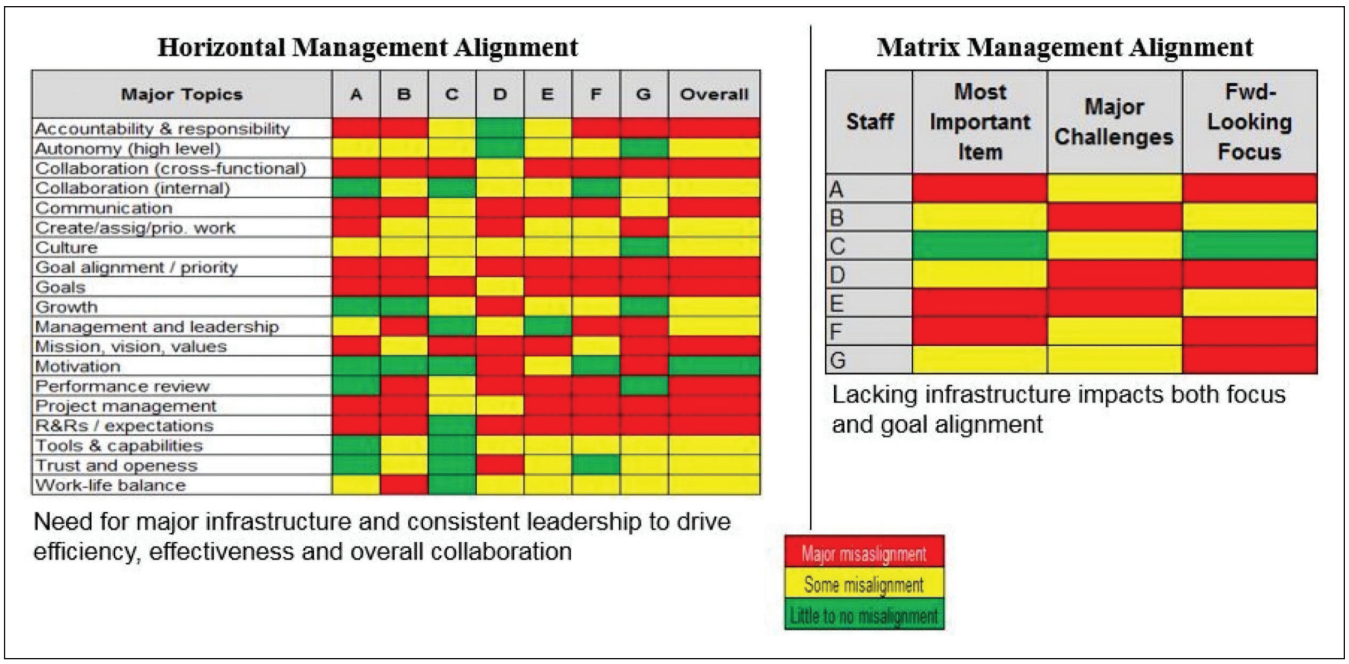


Figure 4. Fab Management Assessment: Highlights skills and alignment across organization, focus on gaps (red) as weakness of teams.

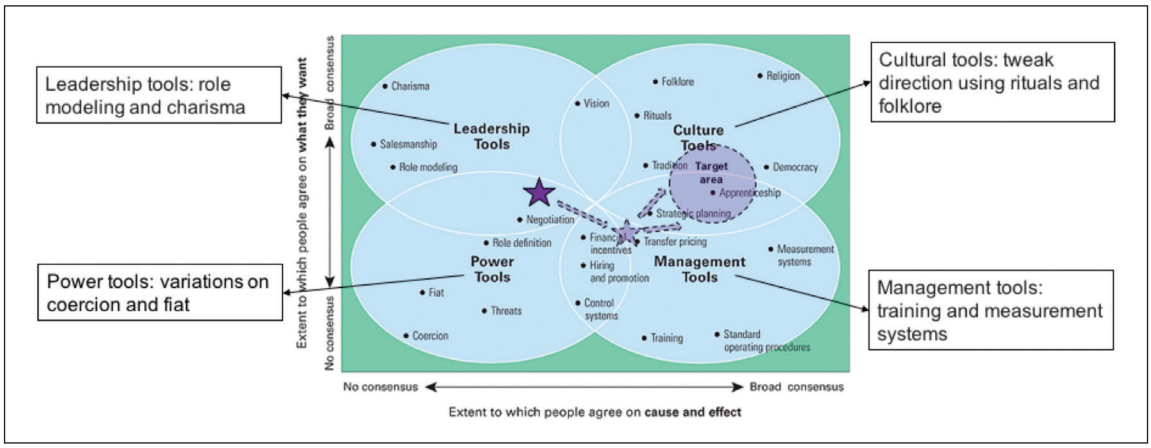


Figure 5. Organization Agreement Matrix: A know methodology to identify where the organization lies and where it should be targeting to be based on the future state (ramp)

and cultural tools (see Figure 4). This chart helps us to identify where organizations fall short and where they should be targeting improvement. This revealed that the best way forward would involve the use of cultural tools (see Figure 5).

By and large, those leading the compound semiconductor fab agreed on what they wanted. However, they couldn't identify a clear path to achieving this. Executing on this from required a combination of power tools, such as coercion and fiat, in conjunction with management tools, such as training and the use of measurement systems. Drawing on all of these tools enabled a move from agreement to cooperation.

The final piece of the third pillar – organisational effectiveness – involved an assessment on project management skills. Successful chipmakers are good at managing and executing improvement activities.

The company that we were working with fell short of this and suffered from weak and absent project management practices, which are needed to provide accountability and bring discipline to the organization. They are by no means alone, as many compound semiconductor companies focus heavily on R&D, while neglecting project management, a key requirement for successful ramping of production.

Changes implemented by the compound semiconductor chipmaker that we worked with will serve it well in an industry that is sure to grow, but will face challenges, as the release cycles for phones, tablets, laptops and cameras get shorter and shorter.

By pairing with us, our client has increased the factory output by 250 percent (see Figure 6). This was accomplished during an 18-month period, where efforts were not just driven by the work with us, but also included a combined effort program to reduce risk.

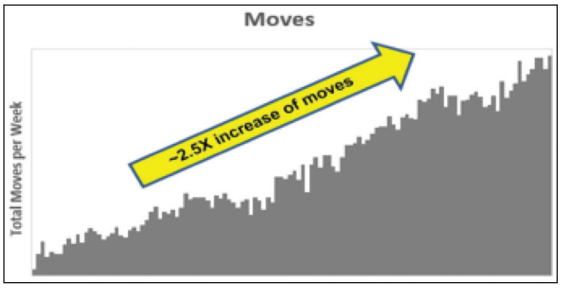


Figure 6. Project Results: 250% increase in wafer starts

Ramping production faster is not the only beneficial outcome of our efforts with the chipmaker. They have also been able to trim their inventory level by 15 percent, benefit from sustainable or faster cycle times, and undertake a cultural change roadmap to sustained factory expansion while realising manufacturing capabilities never seen before.

R&D is a very important part of any compound semiconductor company – but to exploit the breakthroughs that are made there, there must also be an emphasis on implementing the best manufacturing practices, built on the three pillars of good operation practice, strong engineering practice, and having an effective organisational structure.

Further reading

K. Ishikawa, *What is Total Quality Control?* Prentice Hall, 1985, pp.14-23

C. Christensen, M. Marx and H. Stevenson. *The Tools of Cooperation and Change*. Harvard Business Review

Lencioni, P., (2002). *The five dysfunctions of a team: A leadership fable*. San Francisco, CA: Jossey-Bass

3 EVENTS
2 DAYS
1 TICKET

10-11 April 2018

Sheraton Brussels Airport Hotel, Belgium

One ticket gives you access to a 2 day event which will see 3 groups of device makers gathered under one roof.

Hear over 90 presentations covering the entire spectrum of the compound semiconductor, integrated photonics and high-end sensors value chain.

Over 80 speakers CONFIRMED so far.

Book your place now, as it will be another sellout

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

www.cs-international.net

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

www.picinternational.net

HES INTERNATIONAL CONFERENCE

High-end sensors: Market opportunities

www.highendsensors.net

REGISTER NOW, AND SECURE YOUR PLACE. REGISTRATION ALLOWS ACCESS TO:
CS INTERNATIONAL, PIC INTERNATIONAL AND HES INTERNATIONAL

AN ANGEL EVENT

Antimonide LEDs target **gas sensing**

Ventilation systems can consume less power when they incorporate gas sensors with infra-red LEDs delivering ground-breaking performance

BY KOICHIRO UENO, HIROMI FUJITA, OSAMU MOROHARA, EDSON CAMARGO, HIROTAKA GEKA, YOSHIHIKO SHIBATA AND NAOHIRO KUZE FROM ASAHI KASEI MICRODEVICES CORPORATION

TO TRY AND STOP you from feeling sleepy at work, fresh air is brought into your office through the heating, ventilation and air-conditioning system. However, because this process is not controlled, it often wastes energy. Much better is to introduce just the right amount of fresh air, determined by gauging the quality of the air in the office by its concentration of CO_2.

An ideal component for accomplishing this is a CO_2 sensor that combines a low power consumption with a high measurement resolution. Both requirements can be meet with a gas sensing technology based on non-dispersive infra-red absorption. Such sensors utilize the absorption of infrared light in the 3 μm to 6 μm spectral range, with specific wavelengths identifying specific gases (see Figure 1). Low power operation may be realised by pairing a photon detector with an LED, operated with a high frequency, low-duty cycle.

At Asahi Kasei Microdevices Corporation of Japan we have already developed and commercialised one of these two key ingredients – a mid-infrared quantum photon detector. Our device, which is based on an InSb hetero-epitaxial structure, is an attractive alternative to conventional thermal detectors, such as thermopiles and pyro-electric detectors.

Our next step is the development of a high-intensity mid-infrared light source. To this end, we are developing an efficient mid-infrared LED, which is a device that dates back many decades.

One of the key milestones in the development of this device came in the late 1990s, when a partnership between Lancaster University, UK, and the Ioffe Physico-Technical Institute in St. Petersburg, Russia, produced an LED with a strong room-temperature emission at 4.6 μm. This device, suitable for carbon monoxide detection, features an InAsSb/InAsSbP double-heterostructure grown by liquid phase epitaxy. Another key breakthrough from around this era, coming from a team at Grenoble, France, was the development of a resonant cavity structure that improved light extraction.

More recently, a UK-based team from QinetiQ and the University of Bristol, and another collaboration that has been led by researchers at the University of Glasgow, have both shown that the internal quantum efficiency in this class of device can be increased by turning to strong quantum well carrier confinement structures, such as InSb/AlInSb and GaInSb/AlGaInSb.

Drawing on all of this work, we have developed a

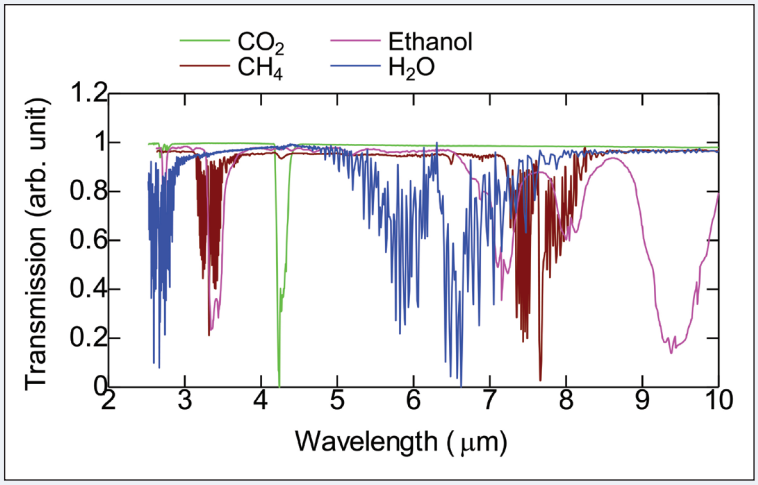


Figure 1. Infrared transmission spectrum of tested gases. Data source is NIST Chemistry WebBook (http://webbook.nist.gov/chemistry).

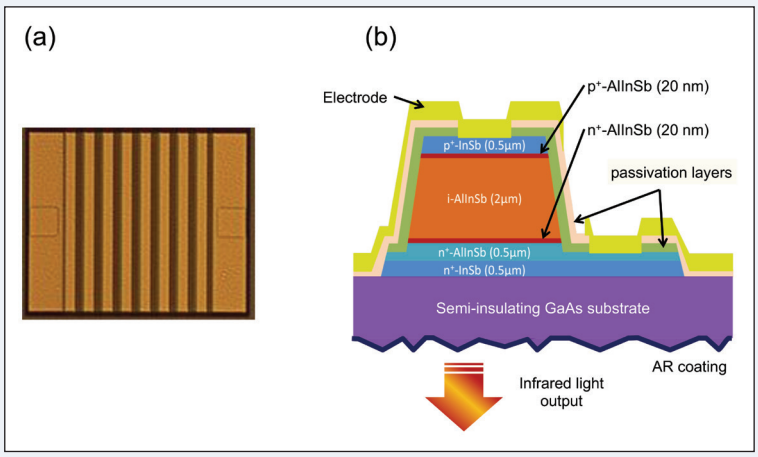


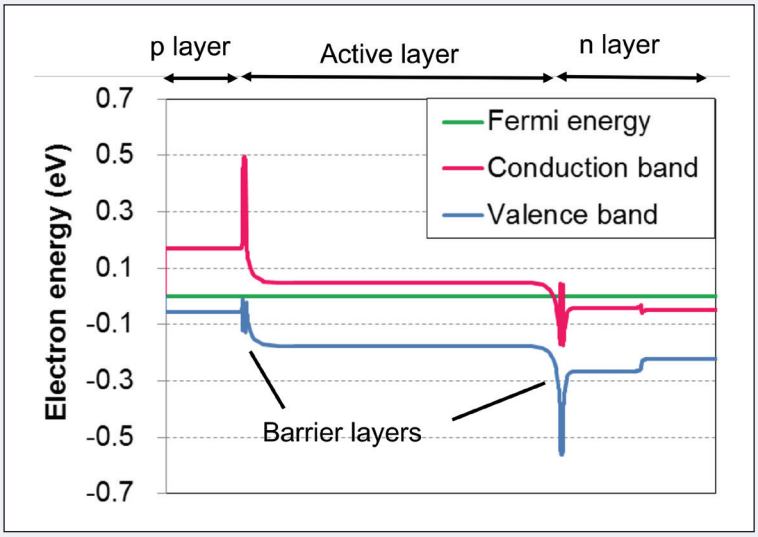
Figure 2. (a) A top view of the eight series-connected mid-infrared LED chip produce by Asahi Kasei Microdevices Corporation. (b) A cross-section of the AlInSb mid-infrared LED, which is formed by growing a 0.5-μm-thick InSb buffer layer with tin doping at a level of 7×10^{18} cm^{-3}; followed by a 2.0-μm-thick intrinsic $Al_xIn_{1-x}Sb$ active layer, sandwiched between the tin doped (n^+) and zinc doped (p^+) 20 nm-thick $Al_{0.22}In_{0.78}Sb$ hole/electron barrier layers; and finally, a 0.5 μm-thick, Zn doped p^+ $Al_xIn_{1-x}Sb$ top layer (2.0×10^{18} cm^{-3}). In the top layer, the aluminium concentration (x) is varied from 3.9 percent to 7.6 percent.

high-intensity AlInSb mid-infrared LED. Its key features are InSb/AlInSb double buffer and electron/hole double barrier layers, and a highly efficient, light-extracting backside emission structure.

We produce our devices by loading semi-insulating GaAs (100) substrates into in Riber MBE 49 tool, thermally cleaning them, and then depositing a heterostructure (see Figure 2 for details). This design provides efficient carrier confinement: there are barrier heights of up to 0.3 eV for holes/electrons, due to the bandgap for the *n*/*p* $Al_{0.22}In_{0.78}Sb$ barrier layers being higher than that for the $Al_{0.05}In_{0.95}Sb$ active layer (see Figure 3).

Figure 3. Energy band diagram of the $Al_{0.03}In_{0.97}Sb$ mid-infrared LED.

Epiwafers were processed into eight series-connected diodes, using Au/Pt/Ti as the electrodes (see Figure 2(a)). To increase light extraction, the backside of the wafer was thinned and roughened with a conventional back-grinding process, and then covered with a TiO_2 anti-reflection coating. Finally, the devices were cut into chips with a 0.5 mm^2 area, using a dicing process, and then assembled into a plastic-mould quad flat non-leaded package. It has dimensions of $2.6 \times 1.9 \times 0.4$ mm.



Blocking dislocations

Transmission electron microscopy offers an insight into the quality of our heterostructures (see Figure 4). Due to the large lattice constant mismatch between the InSb buffer layer and GaAs substrate – it is 14.6 percent – there is the threat that misfits and dislocations at the interface lead to threading dislocations within the film. But that's not the case in our material. Instead, a significant proportion of the threading dislocations are blocked at the AlInSb/InSb buffer layer and at the AlInSb barrier/active layer. Thanks to this, the threading dislocation density in the active layer is limited to $2.9 \pm 0.3 \times 10^8$ cm^{-2}. Although that value is quite large compared to a lattice-matched or a pseudomorphic system, it is still quite low for an antimonide-based system heteroepitaxially grown on a GaAs substrate.

To ensure a high light extraction, we roughen the backside of our device with a conventional back grinding technique. This creates a coarse surface with a root-mean-square roughness of 200 nm. On this roughened surface we deposit a TiO_2 insulating film that has two benefits: it forms an anti-reflection coating; and it passivates the GaAs, prevent surface oxidation.

Compared to a mirror-polished surface, the combination of roughening and deposition of a TiO_2 film produces a 25 percent hike in emission intensity (see the inset to Figure 5). Our approach also has the merit of being simple and effective. While other methods can also increase light extraction efficiency, they are difficult to implement with a top-emitting device architecture.

We have recoded the emission spectra for a range of LEDs with different levels of indium content (see Figure 5). As expected, as the aluminium content increases and the bandgap increases, the emission peak shifts to a shorter wavelength.

To benchmark the power produced by our devices, we have compared the power conversion efficiency of our $Al_{0.061}In_{0.939}Sb$ LED with a reference, chosen because it has the highest level of efficiency of all those currently available on the market (see Figures 6 and 7). Our device has the upper hand, delivering about 75 percent higher emission efficiency than the reference.

It is not surprising that our LED has a lower power conversion efficiency than its shorter-wavelength

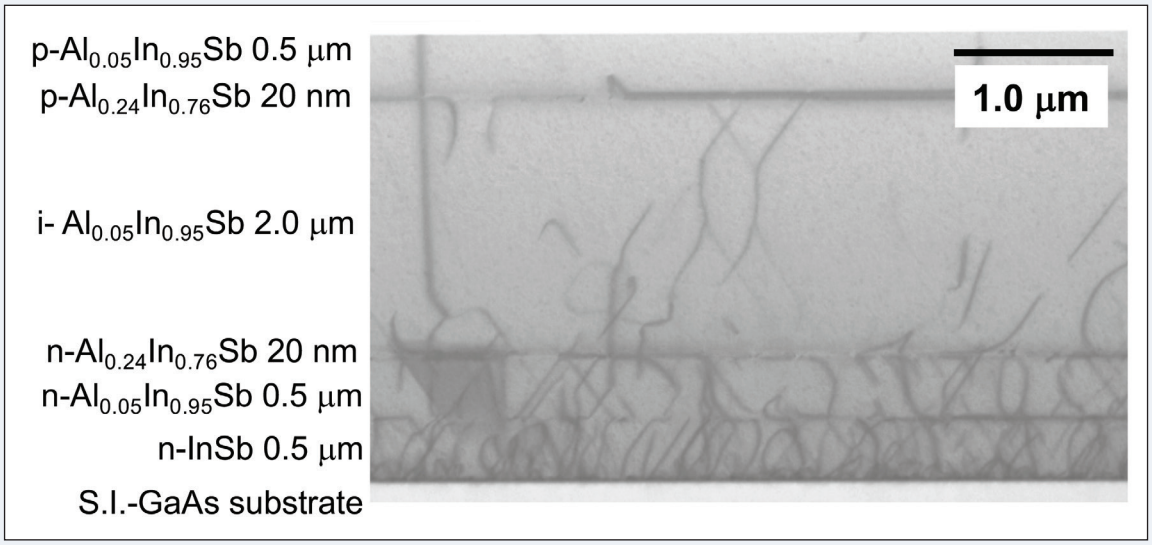


Figure 4. Cross-sectional transmission electron micrograph of the AlInSb mid-infrared LED structure. This image reveals that threading dislocations do not propagate through the heterostructure.

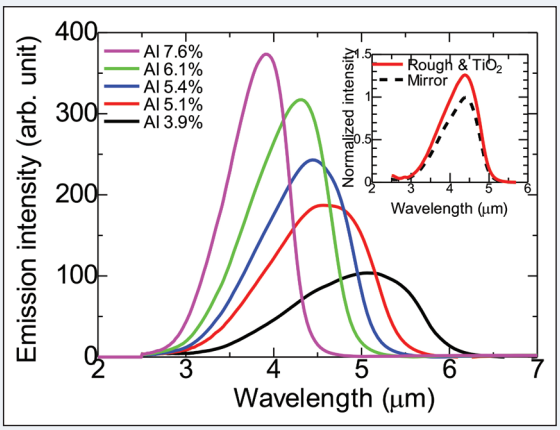


Figure 5. Room-temperature emission spectra for $Al_xIn_{1-x}Sb$ LEDs (x=3.9, 5.1, 5.4, 6.1, and 7.6 percent) made by Asahi Kasei Microdevices. Spectral characteristics were measured with a Fourier transform infrared spectrometer with a HgCdTe detector. The device was driven with a peak injection current of 100 mA and a duty cycle set to 5 percent at 2 kHz.

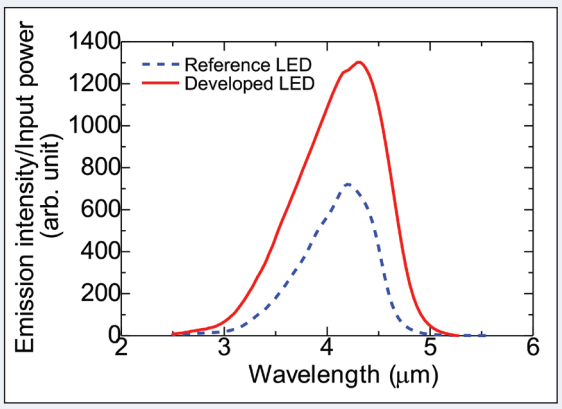


Figure 6. Room-temperature emission spectra for an $Al_{0.061}In_{0.939}Sb$ LED made by Asahi Kasei Microdevices and a reference LED.

cousin, because in the mid-infrared spectral domain, efficiency is known to decrease significantly as wavelength increases. The two primary reasons for this are that Auger recombination is more prevalent in narrow bandgap semiconductors, and that the packaging technology for this class of LED is relatively immature. The packaging technology that is adopted is quite different from that for visual light LEDs, which tend to be housed in bullet-shaped transparent plastic-mould packages with a high light extraction efficiency. Instead, the mid-infrared LEDs are often placed into a metal can package.

We have paired our mid-infrared LED with our infrared sensor to create a gas sensor with an optical path length of about 90 mm (see Figure 8). This gas sensor also has an integrated circuit, which has a dual role, driving the LED and providing signal processing from the IR sensor output. With this gas sensor, the

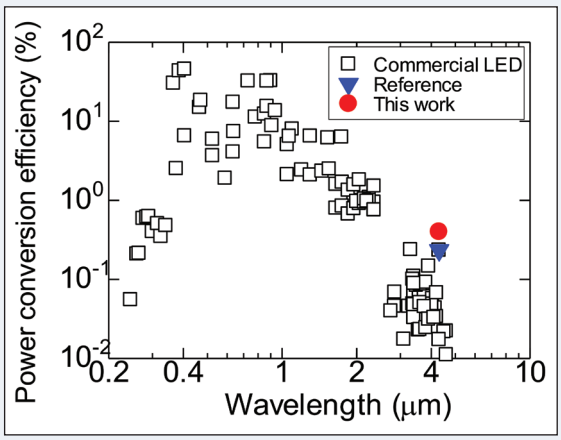


Figure 7. Power conversion efficiency for a range of LEDs, from the ultraviolet to mid-infrared. Data is extracted from commercial LED datasheets. The efficiency for the Asahi Kasei Microdevices' LED, which is estimated from the comparison data with the reference LED in Figure 6, is also shown.

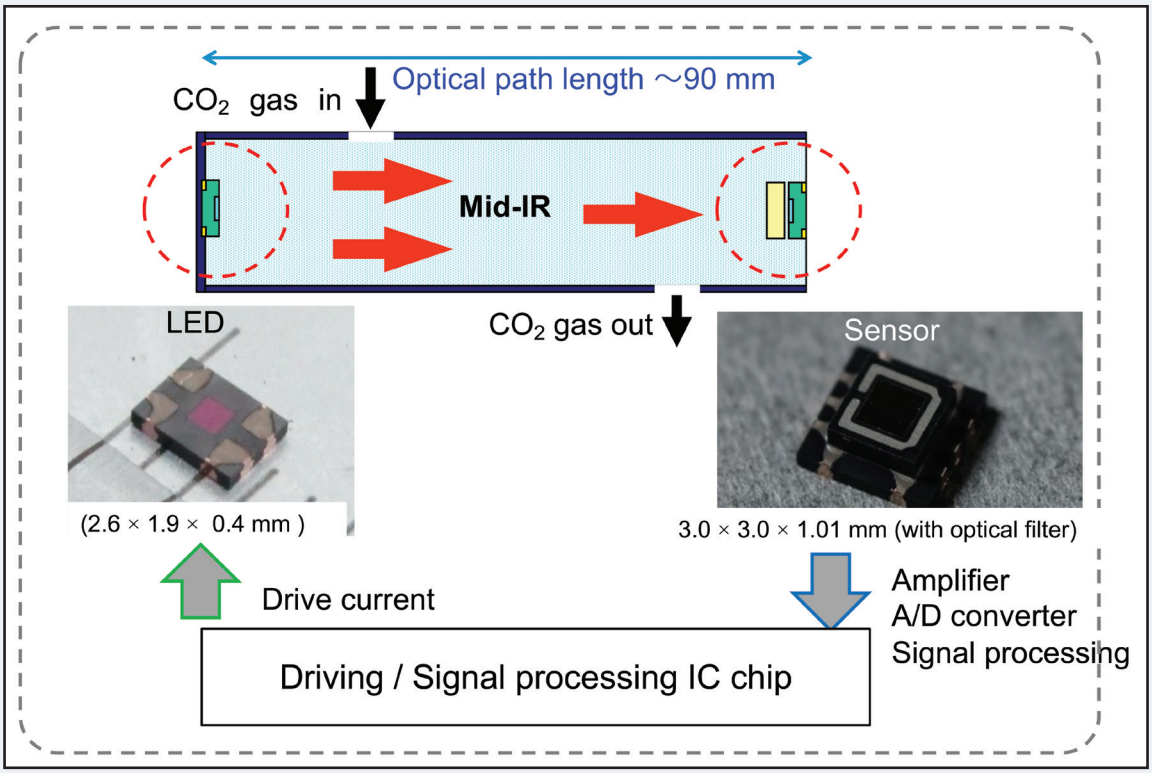


Figure 8. Gas sensor experimental setup. Photographs are for an InSb quantum type mid-IR sensor (AK9710) and a mid-infrared LED assembled in a plastic-mould package (the optical emission window can be observed at the centre of the package, surrounded by four electrode terminals).

calculations for CO_2 concentration are based on the extent of the decrease in the infrared sensor signal intensity.

To assess the output provided by our CO_2 sensor, we have turned to calibration gases with CO_2 concentrations of 0, 1000, 2000, 3000 and 5000 ppm (see Figure 9). During these measurements, LEDs were driven at 100 mA at room temperature, using a duty cycle set to 0.13 percent (the on-time is about 0.2 ms).

Results indicate that the output of our sensor is in good agreement with the calibration gas concentration. We have found that the resolution of our sensor is about 15 ppm at a CO_2 concentration of 1000 ppm. Under these conditions power consumption averages below 1 mW, which is, to the best of our knowledge, the lowest power consumption of any currently available non-dispersive infrared gas sensor.

Our next step is to develop LED/sensor devices for detecting other gases with absorption wavelengths in the mid-infrared, such as methane and ethanol. That will not only enable our sensors to efficiently provide great air-quality at your desk – it will also help detect: leaks of methane gas, which has a greater potential for global warming than CO_2; and prevent drunk motorists from driving.

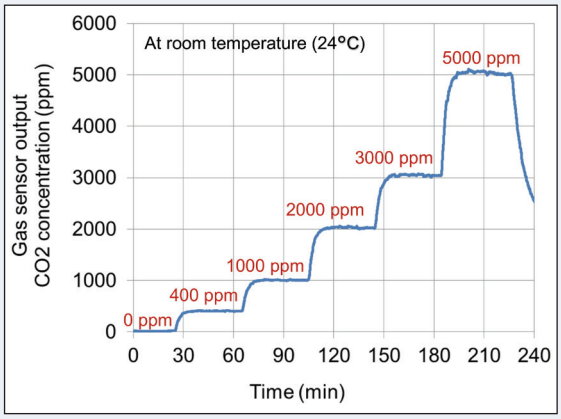


Figure 9. Results of gas sensor output, measured using calibration gases (0, 1000, 2000, 3000, 5000 ppm CO_2 concentrations).

Further reading

T. Lawrence, ASHRAE Journal, Dec, 117 (2004)

T. Dinh *et al.* Sensors and Actuators B: Chemical 231, 529 (2016)

A. Krier *et al.* J. Phys. D, **32** 3117 (1999)

B. I. Mirza *et al.* Appl. Phys. Lett. **89** 131110 (2006)

Y. Ding *et al.* Procedia Engineering **140** 36 (2016)

E. Hadji *et al.* Appl. Phys. Lett. **67** 2591 (1995)

B. I. Mirza *et al.* J. Appl. Phys. **104** 063113 (2008)

Book your place at the

CS International Conference

10 - 11 April 2018

Sheraton Brussels Airport Hotel, Belgium

Co-located with Photonic Integrated Circuits International and High End Sensors International Conferences

In its eighth year CS International 2018 will provide timely, comprehensive coverage of every important sector within the compound semiconductor industry.

The eighth CS International conference will build on the success of its predecessors, with industry-leading insiders delivering more than 30 presentations spanning five sectors.

Highlights of this must-attend event for the compound semiconductor industry will include talks by the leaders of power electronics pioneers Transphorm, Panasonic and VisIC; presentations on the integration of compound semiconductor and silicon technologies by NAsP III-V and the co-ordinators of two multi-partner European projects; and a talk by Seoul Semiconductor on its pioneering efforts at chip-scale LEDs.

These presentations are part of 30+ great talks that will be secured by the organising committee of CS International. A full list of presentations to date can be found at: **www.cs-international.net**

FIVE KEY THEMES:

- **Wrestling market share from silicon power devices**
  What are the next opportunities for SiC? And how can GaN gain significant traction in the market place?
- **Finding solutions with heterogenous integration**
  Where will the growth of compound semiconductors on silicon deliver a fundamental change? And what are the tricks to ensure success?
- **5G: Where we are and what's next?**
  What form will 5G take? And how good will 5G be for GaAs and GaN?
- **LEDs: Magnifying margins**
  Which sectors offer the best returns? Does the bottom line get the biggest benefit from streamlining manufacturing, or from optimising the chip?
- **Ramping revenues from RF devices**
  What are the opportunities for III-Vs in defense and civilian markets? Will higher frequencies open up new sales?

Attendees at this two-day conference will gain an up-to-date overview of the status of the CS industry, and have many opportunities to meet many other key players within this community.

"A tremendous line-up is already taking shape for CS International 2018. Our speakers reflect the global nature of our industry, and the diversity of devices, from LEDs and lasers to power electronics and power amplifiers"

Richard Stevenson, Programme Manager and Editor of Compound Semiconductor

PLATINUM SPONSORS

AIXTRON · attolight · beneq · CATAPULT Compound Semiconductor Applications · EpiGaN · evatec process systems · EVG · FerroTec · htt GROUP. · imschips · KLA-Tencor · nanotronics · Nanowin 苏州纳维科技有限公司 · Revasum · YOLE Développement

GOLD SPONSORS

Accel-RF Instruments Corporation · BLUGLASS · CS CLEAN SOLUTIONS · INNOVION FOUNDRY ION IMPLANTATION · IQE · LAYTEC Knowledge is key · Panasonic · semi · VEM Vacuum Engineering | Materials

WIFI SPONSOR: BROLIS SEMICONDUCTORS

PORTFOLIO SPONSOR: Plasma-Therm

LANYARD SPONSOR: SPTS An orbotech Company

DELEGATE BAG SPONSOR: qorvo all around you

SUPPORTED BY: lighting.eu · EPIC European Photonics Industry Consortium

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

LED droop

The role of saturation

Saturation of the radiative recombination rate is the primary cause of droop, according to differential carrier lifetime measurements

BY DONG-SOO SHIN AND JONG-IN SHIM FROM HANYANG UNIVERSITY

WHEN DESIGNERS incorporate LEDs into their products, they need to know the output power of these devices. In an ideal world, they would then select an LED with an efficiency that peaks at this power. But in practice that's not possible for LEDs emitting in the white, blue and green. With these devices – made from GaN and its related alloys – the internal quantum efficiency peaks at a relatively low current density, and when the current is cranked up to a value needed to ensure a suitable output power for a particular application, efficiency falls, dragged down by a malady known as droop.

Fathoming the origin of droop will help to combat it and yield better LEDs. For that reason, many researchers have been trying to unveil its origin. They have offered many different proposals, leading to lively debate. Strong contenders for the cause of droop include: carrier overflow, enhanced by the internal polarization field; carrier delocalization from indium-rich regions and non-radiative recombination at high defect sites; and, most notably, Auger recombination.

This debate on droop has been going on for more than a decade. But any consensus on the cause of droop remains elusive, because the proposed mechanisms fail to explain all the experimental droop phenomena comprehensively and consistently.

What unites all of the conjectures named above is that droop is accounted for as an additional increase in the non-radiative recombination rate. What is ignored is the possibility that the radiative recombination rate is altered by increases in current density.

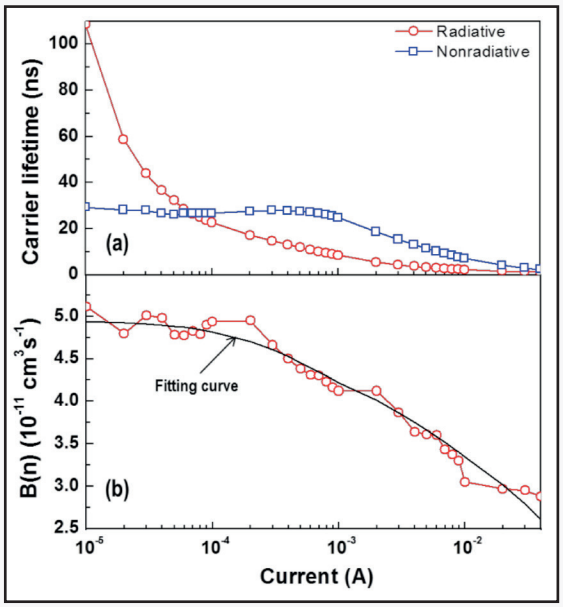
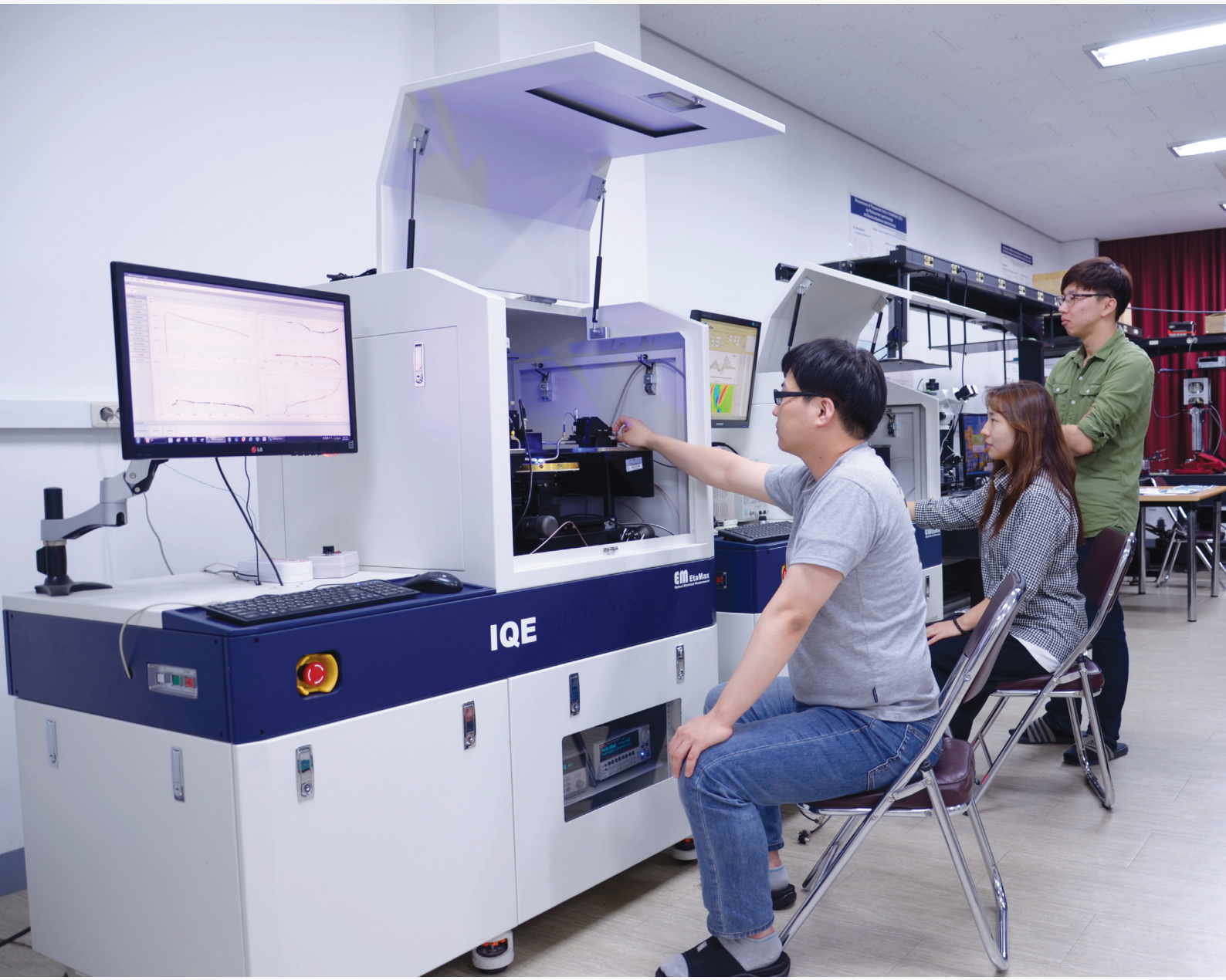


Figure 1. (a) Radiative and non-radiative carrier lifetimes and (b) radiative recombination coefficient B against the injection current, extracted from combined differential carrier lifetime and internal quantum efficiency measurements. The fitting curve for the radiative recombination coefficient uses the theoretical formulation of the phase-space filling, given by $B(n)=B_0[1+\alpha n]^{-1}$. The fitting parameters of $B_0 = 5\times10^{-11}$ cm^{3}s^{-1} and $\alpha = 1\times10^{-19}$ cm^3 fit the experimental result very well.



One of the features of non-radiative electron-hole recombination processes is that they transfer the excess electron energy to particles other than photons. In the case of direct Auger recombination, the process excites electrons or holes to higher energy levels within the same band. The theoretical probability of this Auger process decreases exponentially with both increasing bandgap energy and decreasing operating temperature.

Due to this behaviour, there has been doubt over whether Auger recombination can have an impact in III-nitride semiconductors. However, experimental efforts have yielded similar efficiency droop curves in resonant photoluminescence and electroluminescence, adding weight to the claim that Auger recombination is the dominant non-radiative mechanism behind efficiency loss at high carrier densities.

Many groups have estimated the extent of the impact of Auger recombination by using the well-known *ABC* model in the semiconductor carrier rate equation. This had led to reports of room-temperature Auger coefficients in InGaN-based LEDs ranging from 3.5×10^{-31} cm^6/s to 3.2×10^{-29} cm^6/s. In comparison, theoretical values are generally smaller, spanning about 10^{-34} -10^{-30} cm^6/s.

With just one fitting process, obtaining exact values for the *A*, *B*, and *C* parameters simultaneously is not easy. Consequently, it is common practice to fit the *A* and *B* coefficients in the low current injection regime and the *C* coefficient in the high current injection regime.

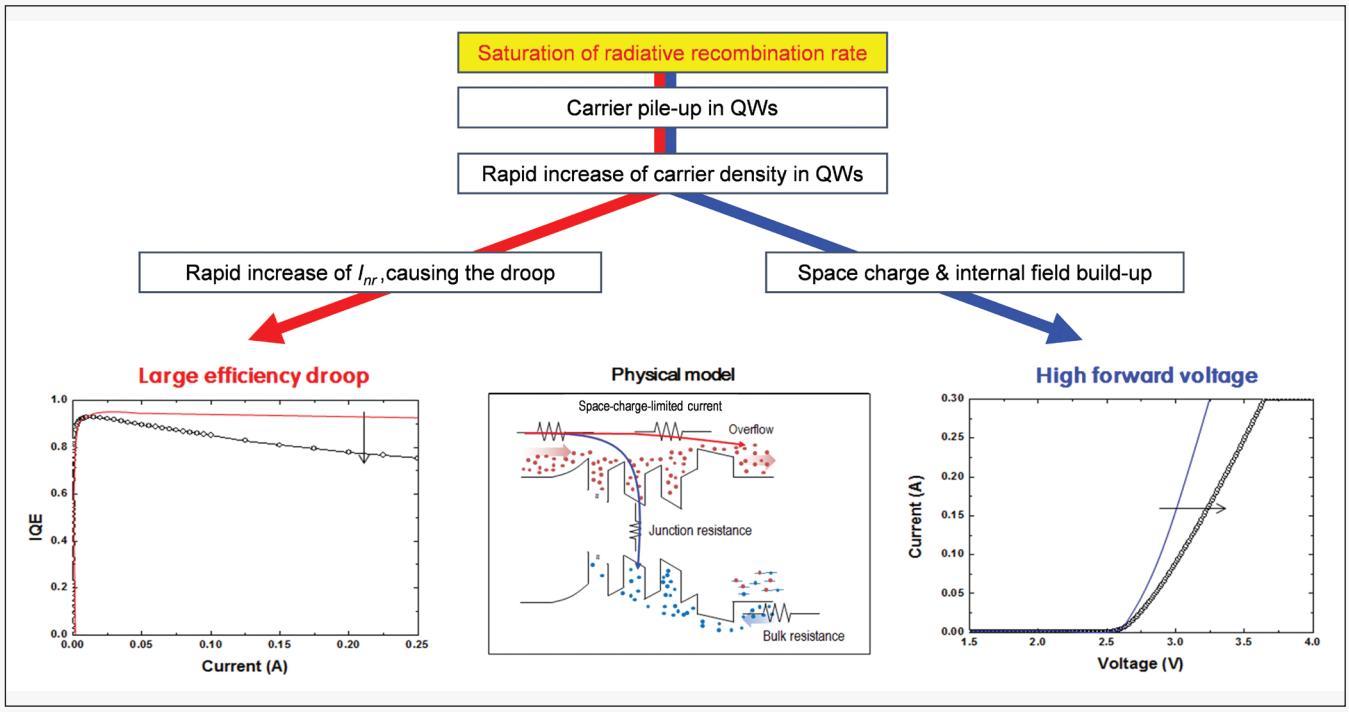


Figure 2. The consequences of the saturated radiative recombination rate.

With this approach, the influence of carrier leakage is neglected – or, to look at it another way, the injection efficiency is considered as unity. However, resonant photoluminescence experiments suggest that many carriers can overflow the active region, rather than recombining within the quantum wells.

Saturation effects

Our team at Hanyang University in Ansan, Korea, has recently proposed an alternative mechanism for droop: saturation of the radiative recombination rate, and the subsequent increase of the non-radiative recombination rate. This conjecture is able to explain droop more comprehensively, including its temperature dependence.

A key piece of evidence supporting our view of droop is our observation of a decline in the open-circuit voltage of the LED when this device is cooled to cryogenic temperatures, operated as a solar cell, and subjected to increases in incident optical power. The temperature-dependent behaviour of the open-circuit voltage is quite similar to that of the internal quantum efficiency, and can only be explained by carrier overflow.

As explained before, the majority of proposals for droop are based on the non-radiative recombination rate increasing faster than the radiative recombination rate. If that's the case, combatting droop involves unmasking the important non-radiative recombination processes and eliminating them.

However, it is our view that droop results from the radiative recombination rate increasing more slowly than the non-radiative recombination rate. That may appear to be no different from the previous explanation – but it is. That's because the emphasis has shifted from the additional increase in the non-radiative recombination rate, while ignoring any changes in the rate of the radiative recombination, to a focus on a saturation in the radiative recombination rate at high carrier density. Once carriers are saturated, they accelerate the non-radiative recombination rate. To combat droop caused by this, there is a need to increase the radiative recombination rate so that it doesn't saturate, even at high current densities.

We unveiled the cause of droop by undertaking differential carrier lifetime measurements, which reveal the carrier recombination dynamics within the LED. Determining the differential carrier lifetime offers an insight into the total recombination rate, which is the sum of the radiative and non-radiative recombination rates. Once the differential carrier lifetime and the internal quantum efficiency are known, radiative and non-radiative recombination rates can be determined, and carrier dynamics within the device known.

Our experiments have been undertaken on blue LEDs, grown by MOCVD on a *c*-plane sapphire substrate. These devices feature an AlGaN electron-blocking layer and an active region with five $In_{0.15}Ga_{0.85}N$ wells separated by GaN barriers. The wells emit at 450 nm at 300 K. Device fabrication involves extracting 200 µm by 800 µm chips from the epiwafer, adding lateral electrodes, and housing the resultant structure in a surface-mount-device package.

We are able to determine the differential carrier lifetime from just electrical measurements. Small-signal impedance is measured as a function of driving current, using an Agilent 4294A impedance analyser.

By adopting the four-terminal-fixture method for calibration, we ensure accurate impedance values over a frequency range spanning 40 Hz to 110 MHz.

The internal quantum efficiency of our LEDs is determined by conventional temperature-dependent electroluminescence measurements. This approach, which is used by many groups, exploits the 'freezing out' of non-radiative recombination centres in the active region at cryogenic temperatures. To obtain the internal quantum efficiency at room temperature, we first find the maximum intensity for electroluminescence at the lowest cryogenic temperature – in our case, 25 K – and then assume that the internal quantum efficiency in those conditions is 100 percent.

Normalising the data reveals that at 300 K, internal quantum efficiency peaks at about 78 percent at 3 A cm^{-2}. Increase the current density and the internal quantum efficiency rapidly decreases, as expected. Light extraction efficiency is estimated to be 65 percent. Note that this value, and that for the internal quantum efficiency, are typical for blue LEDs.

These measurements have enabled us to determine radiative and non-radiative carrier lifetimes as a function of drive current (see Figure 1 (a)). We have also determined the radiative recombination coefficient, and fitted the data with a formula that takes into account phase-space filling (see Figure 1(b)).

Our results allow us to conclude that phase-space filling is behind the saturation of radiative recombination. They also reveal that the non-radiative carrier lifetime has a constant value in the current range 10^{-5} - 10^{-3} A, before gradually decreasing as the driving current increases further. In the low current regime, the non-radiative carrier lifetime varies very little, due to Shockley-Read-Hall non-radiative recombination in the active region – this is represented by *A* in the rate equation. However, when the carrier density in the active region reaches a certain value, the carrier injection rate exceeds the carrier recombination rate, due to saturation of the radiative recombination rate. Once this happens, carriers leak out (or overflow) from the active region, inducing a rapid decrease in the non-radiative carrier lifetime, and leading to the onset of droop. Note that the non-radiative carrier lifetime is shortened, due to the establishing of an additional non-radiative recombination path at the *p*-GaN clad layer.

Further evidence for the role of saturation of the radiative recombination rate as the primary cause of droop comes from measurements of forward voltage as a function of drive current. Using data for internal quantum efficiency, we separate the non-radiative recombination current from the total current. This reveals that the non-radiative recombination current exhibits a peculiar behaviour: we call it the space-charge-limited current. Instead of observing a typical ohmic current, we find that the current is proportional to the voltage squared. That indicates that electrons are not consumed efficiently within the active layer, but overflow to the *p*-clad layers. The overflown carriers eventually lead to an increase in the forward voltage, observed in the current-voltage characteristics.

> The majority of proposals for droop are based on the non-radiative recombination rate increasing faster than the radiative recombination rate. If that's the case, combatting droop involves unmasking the important non-radiative recombination processes and eliminating them

Note that if the Auger recombination were the dominant non-radiative recombination behind droop, this kind of behaviour would not be seen, because all the carriers would be consumed efficiently in the active layer. We believe that the behaviour of LEDs at increasing drive currents involves saturation of the radiative recombination rate, causing carriers to pile up and non-radiative recombination to be induced more severely. The upshot of this is seen in the efficiency droop and the forward voltage increase (see Figure 2 for a pictorial summary).

So how can we combat droop? We know that it is caused by saturation of the radiative recombination rate via phase-space filling, which triggers carrier overflow. So, since high carrier densities induce the phase-space filling, one solution is to increase the effective active volume. As the active volume is reduced by piezoelectric fields, asymmetric carrier distributions and potential fluctuations, all three of these factors must be considered when attempting to diminish droop.

Further reading

J.-I. Shim *et al.* J. Korean Phys. Soc. **58** 503 (2011)
D.-S. Shin *et al.* Appl. Phys. Lett. **100** 153506 (2012)
D.-P. Han *et al.* Phys. Status Solidi A **210** 2204 (2013)
T.-Y Seong *et al.* eds. III-Nitride Based Light Emitting Diodes and Applications, Ch. 7 (Springer, 2013)
D.-P. Han *et al.* Appl. Phys. Lett. **105** 191114 (2014)
D.-P. Han *et al.* Appl. Phys. Express **10** 052101 (2017)
D.-P. Han *et al.* Appl. Phys. Express **10** 122101 (2017)

High-temperature, low-cost GaN VCSELs

Depositing dielectric mirrors on GaN-based active region, grown on sapphire, yields low-cost VCSELs with a high-operating temperature

IF GaN VCSELs could combine low cost with a high operating temperature, they would be an ideal source for smart sensors and compact display projectors. Although such devices are not available on the market today, the good news is that they are now one step closer to production, thanks to the efforts of a team from National Chiao Tung University, China.

"In our approach, we use a rather simple, cost-effective epitaxial growth method, directly on a sapphire substrate," explains team spokesperson Tien-Chang Lu.

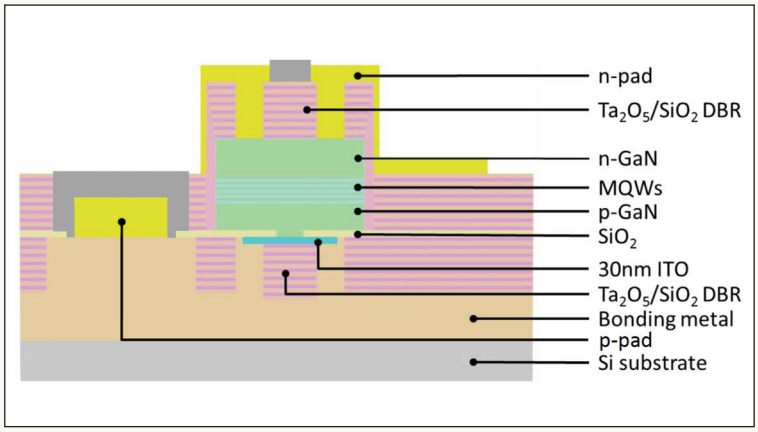
He and his co-workers are not the first to report the high-temperature operation of a GaN VCSEL. At the 2016 International Workshop on Nitrides, a group from Meijo University, Japan, detailed this achievement. However, they used substrates made from GaN rather than sapphire. According to Lu, by switching from GaN to sapphire, the cost of the substrate plummets from $2000 to just $10.

"In addition we systematically analysed the temperature-dependent electroluminescence and lasing peaks of GaN VCSELs," says Lu. This analysis provides important information concerning the characteristics of the GaN microcavities, including the gain-mode offset, which is the difference in wavelength between the gain peak and the cavity mode peak.

"When current is injected into the device, the temperature increase leads to a red shift of both gain and mode peaks," explains Lu. However, as the shift in the gain peak with temperature is greater than that for the mode peak, the researchers intentionally de-tune the two.

"That is one of the reasons why our VCSEL could operate at high temperature," argues Lu.

An electron-beam gun adds the distributed Bragg reflectors to the VCSEL.



He and his co-workers produce their devices by sandwiching a GaN-based active region between a pair of dielectric DBRs.

Fabrication begins by growing, by MOCVD, a GaN-on-sapphire epistructure comprising a thin GaN nucleation layer, a 2 μm-thick GaN spacer, and a *p-i-n* diode structure. The latter consists of: a 2 μm-thick silicon-doped spacer; ten pairs of 3 nm-thick $In_{0.1}Ga_{0.9}N$ quantum wells, surrounded by 8 nm-thick GaN barriers; and a 9 nm-thick, magnesium-doped $Al_{0.2}Ga_{0.8}N$ electron-blocking layer.

On this structure the team add a 45 nm-thick SiO_2 dielectric, grown by atomic layer deposition, before defining a 10 μm current aperture that acts as planar gain guides.

The next steps involve adding a 30 nm-thick indium tin oxide layer with a reactive plasma deposition system, and annealing the wafer for 10 minutes at 500 °C under oxygen. After this, an electron-beam gun adds a 60 μm diameter, circularly patterned 12-period distributed Bragg reflector (DBR) of Ta_2O_5 and SiO_2. Completion of the VCSEL involves: bonding the structure upside down to a silicon substrate; removing the sapphire by laser lift-off; etching and polishing the exposed surface, which is then coated with a 12-period DBR of Ta_2O_5 and SiO_2; and adding metal contacts.

The team's 402 nm VCSEL has an output of more than 20 μW at room-temperature, and a lasing threshold of 8.9 kA cm^{-2}. This latter value is quite high, with blame directed at high absorption loss in the ITO and unpopulated wells in the active region.

The VCSEL's threshold current increases with operating temperature over the range 300K to 350 K. Lu and co-workers believe that this behaviour can be attributed to numerous factors, including a temperature-dependent gain-mode offset mismatch in the short laser cavity, and increases in either the leakage current or the non-radiative recombination rate with temperature.

"We plan to improve the yield and the VCSEL structure, to achieve a low threshold and a high output power," says Lu.

Reference

T. -S. Chang *et al.* Appl. Phys. Express **10** 112101 (2017) (2017)

Double drift layers improve GaN diodes

A double drift layer equips the Schottky barrier diode with a low on-resistance and a high breakdown voltage

ENGINEERS at Arizona State University have developed a novel GaN Schottky barrier diode that combines a low on-resistance with a high breakdown voltage.

"For conventional GaN power Schottky barrier diodes, there is always a conflict between the two: to achieve high breakdown voltages, Schottky barrier diodes require low doping in the drift layer, but this increases the on-resistance and induces more power loss," explains team spokesperson Yuji Zhao.

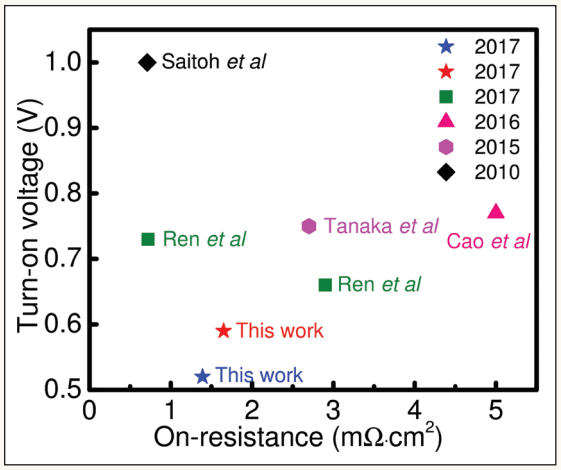
A strong performance on both fronts results from the introduction of a pair of drift layers. A low-doped top layer increases the breakdown voltage for the device, while high doping in the bottom layer trims the on-resistance. "Therefore, GaN Schottky barrier diodes with a double-drift layer can achieve optimal overall performance," claims Zhao.

He and his co-workers use standard fabrication technologies to produce their devices, enabling their process to be suitable for low-cost, high-volume production. Fabrication of the diodes begins with growth, by MOCVD, of the device structure on Sumitomo n^+ GaN bulk substrate with a carrier concentration of 1.6×10^{18} cm^{-3}. A 400 nm-thick n^+ buffer layer is grown first, followed by a 5 μm-thick unintentionally grown GaN layer and a 4 μm-thick GaN layer, doped with silicon to a concentration of 2×10^{16} cm^{-3}.

To assess material quality, the team undertakes X-ray diffraction measurements on the epistructures. Values for the full-width half maximum of the rocking curve peaks reveal that screw dislocations are more common than edge dislocations, and that the dislocation density is in the low 10^6 cm^{-2}. In comparison, the dislocation density for devices grown on sapphire is typically three orders of magnitude higher.

Using atomic force microscopy, Zhao and co-workers determine a root-mean square roughness for a 10 μm by 10 μm scan area of just 0.13 nm.

Conventional optical photolithography and lift-off processes led to the fabrication of Schottky barrier diodes, which had metal contacts added by electron-beam evaporation. Measurements of current-voltage characteristics reveal a turn-on voltage of just 0.59 V, which is claimed to be a record low value for GaN-on-GaN diodes. The ideality factor for this device is just 1.04, indicating that its behaviour is very close to optimal. Meanwhile, the on-to-off ratio is of the order of 10^{10}, which is, according to the team, amongst the highest values ever reported for vertical GaN diodes.



The vertical GaN Schottky barrier diodes from Arizona State University are setting a new benchmark for the performance of this class of device. The on-resistance and turn-on voltage are slightly better for the variant with the single drift layer, but the double drift layer leads to a far higher breakdown voltage, making it the best all-rounder.

At a current of 0.1 A, the on-resistance for the diode is 1.65 mΩ. This is higher than that for a diode with a single drift layer that has been produced for comparison (it has a 9 μm-thick single drift layer doped with silicon to a concentration of 2×10^{16} cm^{-3}). The lower on-resistance for the device with the single drift layer – it is just 1.39 mΩ – is attributed to the higher density of electrons in the drift layer.

Another attribute for both these diodes is their high electron mobility in the drift layer. It is 1045 cm^2 V^{-1} s^{-1} in the device with the double drift layer, and 886 cm^2 V^{-1} s^{-1} in the diode with the single drift layer.

Based on all these results, the team argues that the introduction of the double drift layer gives the diode forward-device characteristics that are comparable to, if not better than, those of single drift layer equivalents. However, when it comes to reverse bias behaviour, the additional drift layer has a big impact: it propels breakdown from 340 V to more than 500 V.

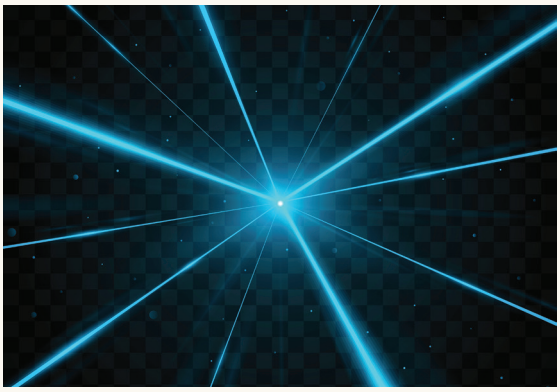
"Several aspects of the device still can be optimised, such as carrier concentration and thickness of the drift layers, and field plate design," says Zhao. However, investigating the benefit of multiple drift layers is the next goal.

Reference

H. Fu *et. al*. Appl. Phys. Lett. **111** 152102 (2017)

Simplifying the production of GaN substrates

Self-separation promises to ease the production of HVPE-grown, free-standing GaN substrates



Degradation in GaN-based laser diodes could fall by switching the substrate from sapphire to $ScAlMgO_4$

A PARTNERSHIP between researchers at Tohuku University and Nichia Corporation is turning to $ScAlMgO_4$ to simplify the production of HVPE-grown, GaN substrates.

With their approach, self-separation follows HVPE growth of GaN on $ScAlMgO_4$. The GaN that is liberated has a higher material quality than that produced by HVPE growth on the more common foreign platforms, GaAs and sapphire.

Improving the quality of GaN substrates is highly valued, because it leads to better devices. Degradation in high-power and high-frequency transistors and laser diodes diminishes when these devices are grown on substrates with lower dislocation densities.

Ideally, GaN substrate production would begin with crystal growth. This is possible, but the growth rates are very low.

HVPE addresses this issue, but GaN has to be removed from the foreign substrate that it is grown on. If sapphire is used, laser lift-off and the void-assisted method are suitable; and if GaAs is used, chemical etching is employed to extract GaN.

However, for both GaAs and sapphire, there is a large lattice mismatch with GaN. This is undesirable, giving rise to a high density of dislocations in the HVPE-grown layer.

Switching to $ScAlMgO_4$ allows the team to grow GaN on a substrate with a far lower lattice mismatch – it is just 1.9 percent. What's more, $ScAlMgO_4$ has excellent *c*-plane cleavability characteristics, so the GaN that is grown can be easily separated from the underlying material.

The potential of $ScAlMgO_4$ for the growth of GaN has been known since the 1990s. However, although it has previously been used to deposit GaN by MBE and MOCVD, the team from Japan believes that it is the first to report its use for HVPE growth of GaN.

Prior to HVPE growth, the researchers used MOCVD to deposit a buffer layer and a 2 μm-thick film of GaN on an as-cleaved, *c*-plane $ScAlMgO_4$ substrate. They loaded this template into a HVPE growth chamber, where growth of GaN took place at 160 μm/hour, using a pressure of 600 Torr and a template temperature of 1033 °C.

Using this approach, the team produced GaN films with total thicknesses of 160 μm, 320 μm, and 400 μm.

On cooling after growth, the 320 μm-thick film of GaN naturally separated from the substrate, due to differences in thermal expansion coefficients that induced stress at the herterointerface. However, stress did not lead to self-separation in the other two films – these were parted from $ScAlMgO_4$ by using a pair of tweezers to lightly apply mechanical stress.

With only the middle-thickness film self-separating, it is unclear what the value is for the critical thickness of GaN on $ScAlMgO_4$. According to the team, this could be determined by quantitative analysis of the interface stress. However, identifying this is impaired by a lack of knowledge of the mechanical properties of $ScAlMgO_4$.

To determine the threading dislocation density in the material, the researchers turned to two-photon excitation photoluminescence. Images revealed dark spots, corresponding to threading dislocations. The dark spot density in the GaN films grown on $ScAlMgO_4$ can be as low as 3×10^6 cm^{-2}. According to the team, this value is about 30 percent lower than that for a GaN wafer formed using sapphire.

This indicates that compared to the incumbent HVPE-based methods for GaN production, the team's technology can yield higher quality material by a simpler approach.

Reference

K. Ohnishi *et al.* Appl. Phys. Express **10** 101001 (2017)

Angel
BUSINESS COMMUNICATIONS

WE'VE BUILT AN APP FOR THAT.

Many companies are now thinking of offering their customers and potential customers an app.

Angel Online are one of the UK's leading app development companies providing both iPhone and Android app development. We have specialist industry knowledge of vertical B2B markets. We can help you build an app for your sales, marketing or internal communications purposes.

Visit **www.angelbc.com/online** to think outside the box.

E: sukhi.bhadal@angelbc.com **T:** +44 (0)24 76718970

- WEBSITE DEVELOPMENT
- MARKETING AND SEO
- EMAIL MARKETING
- ONLINE MARKETING
- APP DEVELOPMENT
- WEBCASTS

green pages directory

VENDOR VIEW Proton Site

On-site hydrogen generation: smart choice to improve process results

Hydrogen is widely used to support a variety of industrial applications worldwide, due to its ability to meet the specific needs of high purity industrial applications, ranging from semiconductor manufacturing and epitaxy to heat treating and materials processing.

Relying heavily on hydrogen to maintain process results, many operations personnel are responsible for evaluating which gas supply method will best suit their operation. Over time, this task can become daunting, because as businesses grow, increasing amounts of hydrogen are needed to satisfy elevated levels of production demand. This spike in hydrogen usage has translated into a collection of issues for facility operation.

Hassles such as inefficient production practices, fire permit restrictions, space limitations, increased costs, dangerous hydrogen storage and handling can make gas sourcing especially problematic.

Offering clear advantages over older, conventional methods of hydrogen supply such as delivered gas, dissociated ammonia and exo or endo gas, hydrogen generated on-site is a drier and safer alternative.

A high performance solution to suit businesses small and large, on-site gas generators satisfy demand by producing hydrogen at its point of use with no inventory of flammable or poisonous gas. Hydrogen generation systems are easy to permit, easy to install, and operate automatically.

Market data shows more and more stakeholders are making the switch to gas generators, eliminating the need for delivery and storage of hazardous gases within the industry.

With more than 2,500 systems installed in over 75 countries, Proton OnSite hydrogen generators are consistently creating value around the world. Utilizing advanced Proton Exchange Membrane (PEM) electrolysis, with a high differential pressure design, our on-site hydrogen generators produce very pure hydrogen in a safe, reliable, and cost effective package.

Our industrial customers are particularly impressed with the fact that they are able to realize rapid paybacks while dramatically improving facility safety. The on-site generators eliminate the need for stored hydrogen, while meeting the daily requirements of various industrial processes. Thus, providing an attractive return on investment for customers and improving site security, safety and personnel productivity.

Want to learn more about the ways hydrogen generation enables reducing, non-carburizing atmospheres without hydrogen or ammonia inventory? Interested in 99.9995%+ purity, -65°C dewpoint, 200+ psig hydrogen for use pure or blended? Our compact, packaged systems can do that, and then some. Improve your facility safety, minimize storage and handling, and improve your process results!

Visit: **www.protononsite.com** for details.

your

EPITAXIAL GROWTH

partner

Enabling advanced technologies

- World leading technology
- Complete materials range
- MOCVD, MBE, CVD
- Advanced semiconductor wafer products
- Advanced R&D capabilities
- Multiple, manufacturing sites (Europe, Asia, USA)

IQE

www.iqep.com