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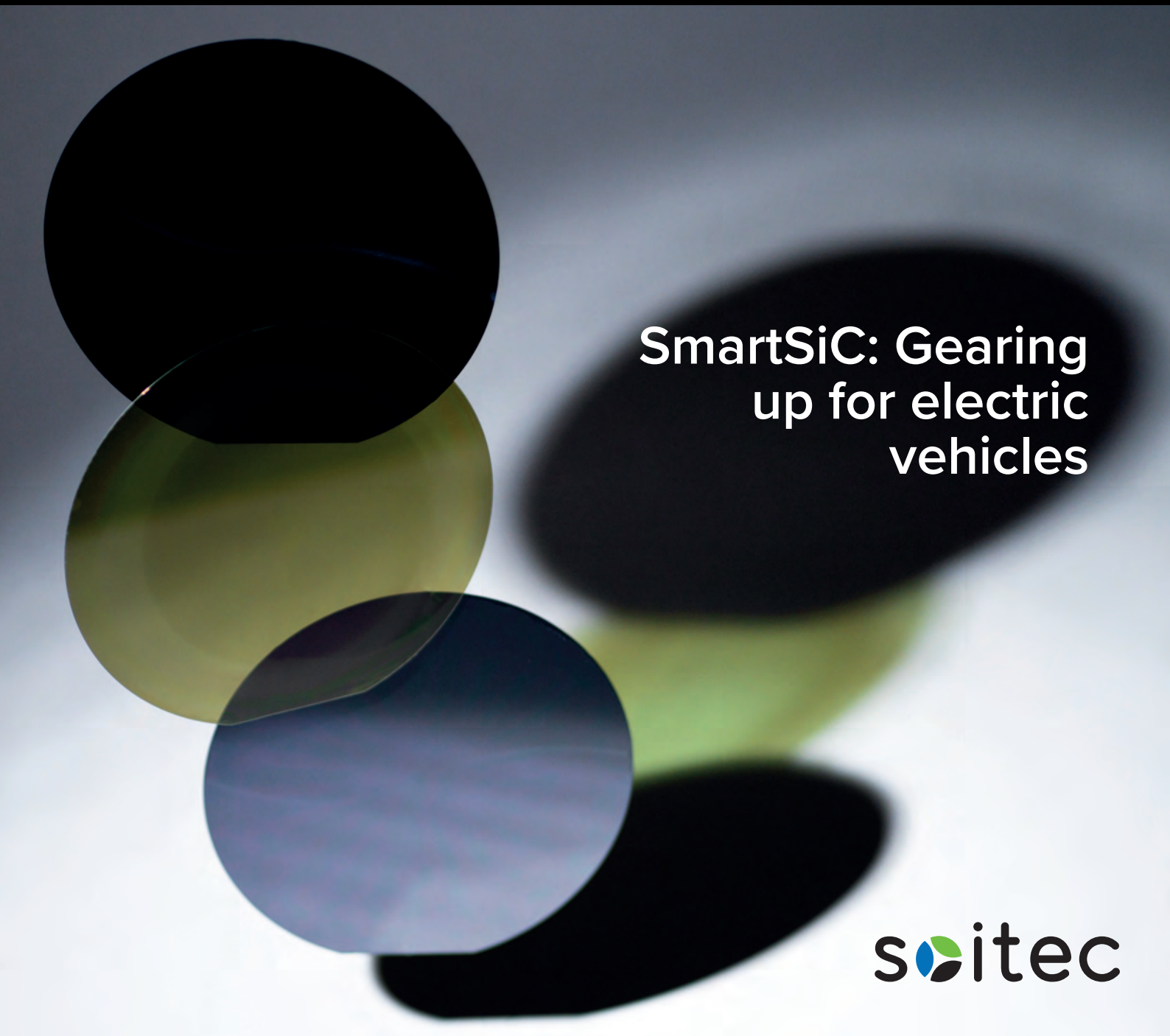

SmartSiC: Gearing up for electric vehicles

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VIEWPOINT

By Dr Richard Stevenson, Editor

Academia and industry

Within our community lies an incredibly strong bond between industry and academia. That's partly because universities offer such a fantastic training ground for those that work in industry, by providing great foundations in materials science and engineering for those that go on to make and design the likes of lasers, LEDs, and RF and power devices. But, in addition, there is much material and device development undertaken within university groups, with some of most exciting technology leading to spin-off companies.

Yet despite this symbiotic relationship between academia and industry, many conferences are entrenched on one side of the divide. You'll not find many academics attending the *European Conference on Optical Communications* or the *International Microwave Symposium*, while those from industry are thin on the ground at *InP and Related Materials* or the *International Conference on SiC and Related Materials*.

One academic bucking this trend is Bristol University's Martin Kuball, interviewed in this issue (see p. 36). He has built his career, and a 20 strong team of researchers, by attending and supporting industry-led conferences, such as *CS Mantech*, and collaborating with companies – primarily by applying novel metrology techniques to gain new insights into the behaviour of RF and power devices.

Recently, Kuball expanded his research programme to the fabrication, design and characterisation of gallium oxide devices. This has included the installation of a new tool for MOCVD growth of gallium oxide that prompted my visit. However, while I was with him, I also took the opportunity to discuss what might hamper partnerships between academia and industry. Kuball pointed out that differences in timescales can thwart collaboration. For example, there are times when industrial projects may be too short-term to garner academic interest.

Another common issue is that companies are keen to develop closely guarded IP, while those in academia are driven by publishing papers that reveal all the details of those crucial ground-breaking secrets.

At this year's *CS International*, those attending could see some of this at play. During a presentation by microLED developer Porotech, delegates were shown a video demonstrating the emission of all colours – including white – from a single GaN-based pixel. How could this be done? The speaker, Business Development Manager Ellie Galanis, would not say. However, as a holder of a PhD in materials science, there would have been a time in her life when she would have loved to have explained the details behind the success, ideally by publishing a paper in a highly prestigious journal.

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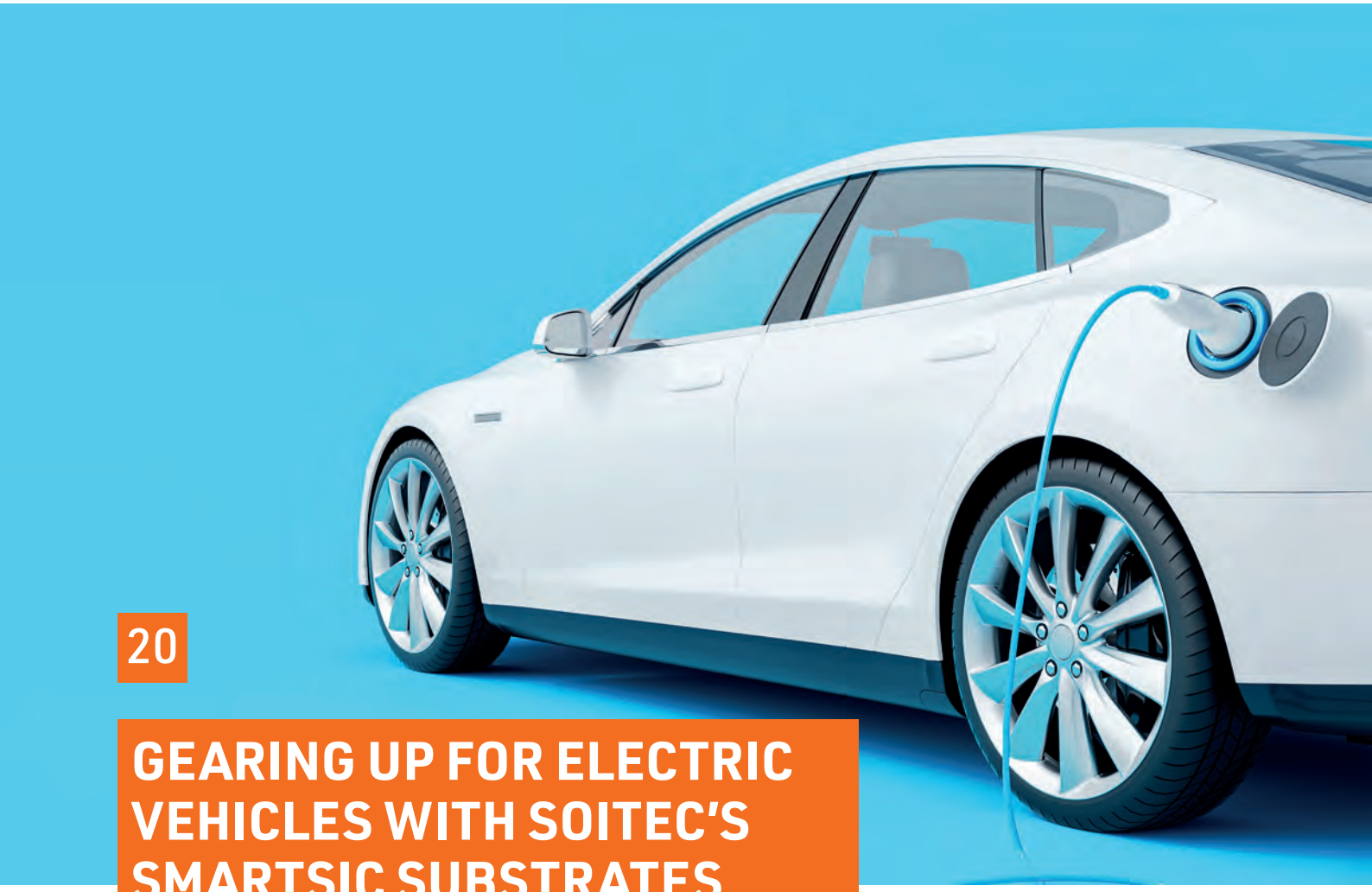

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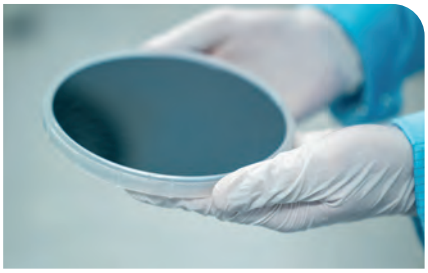

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Agnitron installs custom MOCVD system at Cornell

CUSTOM MOCVD manufacturer Agnitron Technology of Chanhassen, Minnesota, has successfully installed a custom MOCVD system for growing ultra-wide band gap oxides at Cornell University.

Agnitron installed and qualified the R&D gallium oxide MOCVD Agilis 100 system in July 2022. The system has demonstrated silicon-doped Ga_2O_3 homoepitaxial layers with a room temperature electron mobility of 150 cm^2/Vs and a free carrier concentration of 6×10^{16} cm^{-3}. The system has also demonstrated coherently strained epitaxial AlGaO with an aluminium concentration of up to 18 percent on native gallium oxide substrates.

The Agnitron Agilis 100 system at Cornell can perform processes up to a 1600 °C substrate temperature. The system has a GEN II remote-injection showerhead that provides significantly reduced gas-phase reaction and excellent thickness uniformity on a 2-inch diameter wafer. The system's design also supports the use of ozone as an oxidizer.

According to Agnitron, the Agilis 100 MOCVD platform is easily convertible to grow GaN and AlN epitaxial layers, enabling the dual capability on the hardware and control software levels.

Assistant research professor Hari Nair chose Agnitron Agilis 100 for his research on Ga_2O_3 because the proven platform, used by many other research groups, has demonstrated excellent quality material.

"We look forward to partnering with Agnitron to develop further epitaxial layers of ultra-wide bandgap Ga_2O_3 and other oxides for forming heterostructures with novel properties," says Nair.

Agnitron CEO Andrei Osinsky says, "Due to the unique fundamental properties of Ga_2O_3, it is attractive for making power switches operating at high-voltage and high-power densities. Because of its great potential for future commercial applications, it is important to continue making further advances in research."

Osinsky notes that the Agnitron Agilis 100 MOCVD has an excellent track record for growing gallium oxide and related alloys that hold world records in material purity and crystal quality. Osinsky says Agnitron is excited to support the new MOCVD at Nair's lab at Cornell University with their efforts to make advances in epitaxial growth of Ga_2O_3.

Agnitron has a large installation base of Agilis 100 systems that resulted since it's introduction in publishing over 30 research papers and delivering many scientific conference presentations.

AXT crosses milestone on Tongmei IPO

AXT, a maker of compound semiconductor substrates, has announced that its subsidiary in China, Beijing Tongmei Xtal Technology Co., Ltd, was approved by the Shanghai Stock Exchange for the listing of Tongmei's shares in an IPO on the SSE's Sci-Tech innovAtion boaRd (the STAR Market).

The STAR Market IPO remains subject to review and approval by the China Securities Regulatory Commission and other authorities. The SSE will now forward Tongmei's application to the CSRC for its review and approval.

"We consider this to be a major milestone in our effort to complete the STAR Market IPO," said Morris Young, chief executive officer. "The SSE review process is detailed, thorough, and lengthy. Its approval is an important step because we believe that the CSRC relies heavily on the work performed by the SSE. I want to congratulate our team for their hard work and diligence in getting to this point in the process. Although the timing for the IPO remains uncertain and depends upon many factors beyond our control, the achievement of this milestone adds to our confidence that Tongmei can complete the listing in this calendar year."

The process of going public on the STAR Market includes several periods of review and, therefore, is lengthy. AXT believes that the SSE review, which has just been completed, is typically the longest part of the process. Subject to the review and approval by the CSRC and other authorities, Tongmei expects to complete the listing in the second half of 2022, probably in Q4 2022.

Finwave Semiconductor raises $12.2 million

3DGaN innovator and MIT-spin-out Finwave Semiconductor has announced a $12.2 million Series A funding round led by Fine Structure Ventures with additional participation from Citta Capital, Soitec, Safar Partners and Alumni Ventures.

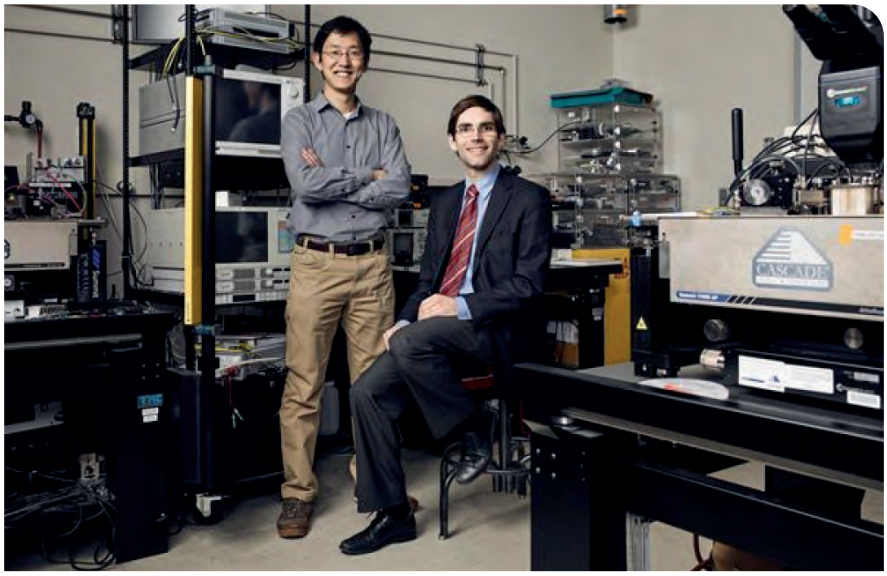
The Series A follows an award of $4.3 million in federal funding from the US Department of Energy Advanced Research Projects Agency-Energy (ARPA-E) SCALEUP (Seeding Critical Advances for Leading Energy technologies with Untapped Potential) grant, to help bring the company's technology to volume production.

The funds will be used to expand the company's team, product development activities and lab facilities – all in advancement of Finwave's mission to revolutionise the future of 5G communications with next-generation 3DGaN FinFET technology.

"Finwave's technology unlocks the promise of 5G," said Jennifer Uhrig, senior managing director at Fine Structure Ventures, a venture capital fund affiliated with FMR LLC, the parent company of Fidelity Investments. "The company combines best-in-class power amplification efficiency with high-volume manufacturing to overcome the performance and cost limitations that have together stymied widespread adoption of mmWave. We are thrilled to be working with Finwave to bring their revolutionary products to market."

mmWave is critical to the future of all wireless technology, but the realisation of its potential faces severe roadblocks. Weak uplink, high deployment costs, low 5G radio efficiency and soaring operating costs are all combining to thwart the promise of mmWave. Currently, 5G networks are being held back from realising their true potential due to a critical missing component: high-performance mmWave power amplifier technology.

High-performance GaN-on-silicon brings a new option to the table that could make 5G millimeter wave more practical. At mmWave frequencies, GaN-on-silicon amplifiers excel versus alternative solutions such as silicon RFSOI MOSFETs, GaAs pHEMTs, or SiGe devices. Finwave's award-winning 3DGaN technology significantly improves linearity, output power and efficiency in 5G mmWave systems – while greatly reducing costs for carriers. By leveraging high volume 8-inch silicon CMOS fabs for producing 3DGaN chips, Finwave's devices benefit from both the cost model and scalability of silicon technology.



"3DGaN FinFET technology is a result of over 10 years of research and development, initially developed at MIT and recognised with the coveted 2012 IEEE Electron Device Society George Smith Award," noted Bin Lu, Finwave's CEO and co-founder, pictured above with co-founder Tomas Palacios. "The enormous potential of GaN FinFETs has since been demonstrated by a growing number of researchers around the world.

"Finwave was founded with the mission to scale the technology from lab to high-volume products that benefit society, and 5G presents the perfect market opportunity for the scale, performance gains and cost advantages this technology brings. Having solved numerous manufacturing challenges and successfully created a fabrication process using standard 8-inch silicon CMOS tools, Finwave is leading the way in commercialising the 3DGaN technology for 5G."

Finwave chief strategy officer and executive chairman Jim Cable added, "After spending 30 years working in the silicon-on-insulator technology and being an early pioneer in getting this technology into every cell phone on the planet, the opportunities for Finwave's 3DGaN GaN-on-silicon technology are enormous, and I am very excited to be part of the team. I personally understand the challenges of ramping up a new technology into high-volume markets, and we are very focused on all aspects of enabling this. Closing this Series A round is a major step forward for us."

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Aixtron reports highest order intake since 2011

DEPOSITION equipment company Aixtron has recorded its highest quarterly order intake since 2011 in the second quarter of 2022.

The order intake was driven by broad based demand. Along with the underlying strong demand, Aixtron says its equipment for energy-efficient power electronics using GaN and SiC ensured an excellent order situation for supporting year-on-year increases in both revenue and profit in the second quarter.

Based on the current momentum of demand, and in expectation of a continuation of the high number of orders, the executive board reiterates growth guidance for the full year 2022 given this February.

The company says that overall, the current global crisis situations and market developments continue to only have a minor impact on its business. Logistics and supply chains are still challenging, but in its view, continue to be manageable.

The order intake in the first half of 2022 was €282.8 million, 7 percent above the order intake of the previous year's period. The strongest demand was recorded for tools for the volume production of microLEDs, followed by demand for efficient power electronics based on the material systems SiC and GaN.

At €152.6 million in Q2/2022, order intake even exceeded the strong level of the previous quarter, as well as of the prior-year quarter. The order backlog at June 30, 2022, increased to €314.4 million from €295.0 million in the previous year and €260.4 million as of March 31, 2022. Most of the order backlog is due for delivery in 2022.

Revenue increased significantly in H1/2022 by 63 percent to €191.1 million compared to the same period of the previous year.

In Q2/2022, revenue increased year-on-year by around 51 percent to €102.5 million (Q2/2021: €67.7 million).

As expected, deliveries of tools for manufacturing of traditional red LEDs accounted for a large share of this. Sales of tools for SiC power electronics in particular grew strongly.

Also strong was the revenue contribution from the optoelectronics area and optical data communication in particular.

In the first half of 2022, gross profit increased by 63 percent to €73.7 million at a gross margin of 39 percent. Gross profit development in Q2/2022 was driven by a comparatively low-margin product mix. In addition, higher costs incurred from projects to strengthen production and supply chains. Nevertheless, gross profit increased by 36 percent year-on-year to €37.8 million at a gross margin of 37 percent.

Operating expenses amounted to €42.3 million, slightly higher compared with the previous year's period.

The operating result (EBIT) increased year-on-year from €4.9 million to €31.4 million, corresponding to an EBIT margin of 16 percent.

This development was mainly the result of significantly higher year-on-year revenues and the corresponding gross margin in conjunction with the business and cost developments described above. Operating result (EBIT) in Q2/2022 more than tripled year-on-year to €17.2 million at an EBIT margin of 17 percent.

Net profit of Aixtron in H1/2022 increased to €31.1 million, and in Q2/2022 net profit more than doubled to €17.3 million.

Free cash flow increased to €26.4 million in H1/2022, mainly related to advance payments received for customer orders and the simultaneous increase in inventories.

Mainly due to the dividend payment of €33.7 million in May 2022, cash and cash equivalents, including financial assets, decreased to €346.2 million as of June 30, 2022, compared with €352.5 million as of December 31, 2021.

The high equity ratio of 78 percent as of June 30, 2022 (June 30, 2021: 73 percent) underlines Aixtron's financial strength, according to the company.

The number of employees in the Group increased to 772 as of June 30, 2022. The structural strengthening of the organisation for further growth is thus well on track, says Aixtron.

Due to the good business development in the first half of 2022 and in view of the expectation of a positive development of demand for the remainder of the year 2022, the Executive Board reconfirms the growth guidance issued. Accordingly, order intake is expected to be in a range between €520 million and €580 million.

With revenues in a range between €450 million and €500 million, the Executive Board expects to achieve a gross margin of approximately 41 percent and an EBIT margin of approximately 21 percent to 23 percent of revenues in fiscal year 2022.

As before, the expectations for 2022 are subject to the provision that global crisis situations continue to have no significant impact on the development of the business.

"Many years of research work are now paying off," says Felix Grawert, CEO of Aixtron. "This quarter marks another milestone, as we are not only showing continued strong growth on a broad basis in our addressed markets, but especially with the first order for our equipment for the volume production of microLEDs."

"We were able to grow as planned despite the challenging market environment with supply chains remaining constrained," said Christian Danninger, CFO of Aixtron.

"In addition, we are driving process improvements along the entire organisation in order to prepare Aixtron for the expected future growth."

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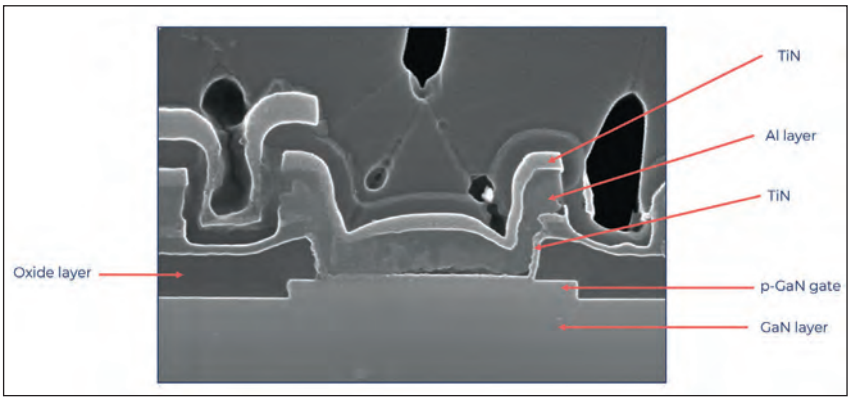
Who is playing the power GaN game?

In its new comparison report, *GaN Power Transistor Comparison 2022*, Yole SystemPlus presents an overview of state-of-the-art GaN power devices to highlight differences in design and manufacturing processes and their impact on device size and production cost. This report analyzes 34 devices from 12 of the leading suppliers.

Yole SystemPlus's comparison report also includes estimated manufacturing costs of the analyzed GaN devices and their selling prices. In addition, it provides physical, technological, and manufacturing cost comparisons between the devices.

Recent market reports have shown the continued growth of the GaN power device market, as well as the adoption of these devices in various applications ranging from consumer electronics to automotive applications. The GaN power market is expected to reach US$2 billion in 2027.



Since their first commercialization in 2010, the performance and added value of GaN devices have been gradually proven, and prices have become increasingly acceptable to end-users.

New major players like STMicroelectronics are entering the market, and there is increased adoption of monolithic power GaN ICs in various mobile charges, with a power rating up to 130 W at affordable prices.

However, GaN devices still have some technical and commercial challenges. Technically, improvements are required in manufacturing yield and electrical performance.

Commercially, there is a need for large-volume market adoption driven by targeted applications (for instance, automotive) to reduce further the cost of GaN devices and favour GaN adoption on a large commercial scale.

II-VI is renamed 'Coherent' after acquisition

II-VI INCORPORATED has successfully completed the acquisition of Coherent, to form a materials, networking and laser company. The combined entity will serve the four markets of industrial, communications, electronics, and instrumentation, which together represent a fast-growing total addressable market of $65 billion.

Under the terms of the merger agreement, each share of Coherent common stock was converted into the right to receive $220.00 in cash and 0.91 of a share of II-VI common stock.

Both organisations bring their own strengths. The combined business will be more distributed across the value chain from materials to components, subsystems, systems, and service. II-VI's scale, at the levels of the value chain where expertise in materials matters, is complementary to Coherent's scale where laser systems play. The combined company expects to leverage that complementary scale in ways that will really matter to its customers in strategic markets.

"Coherent is an innovator with a rich portfolio of some of the most advanced technologies in the world, which have been transformative in a broad range of markets," said Vincent Mattera, Jr., Chair and CEO of II-VI. "I would like to thank Andy Mattes for his leadership of Coherent and enabling a very successful integration planning process."

Mattera continued: "We will soon announce the date of the launch of our new brand identity. While the name Coherent has a strong association with lasers, the broader meaning of the word is 'bringing things together.' It represents our diversity in thinking distilled into our clarity of purpose, our unity in action, and our broader sense of engagement by connection to our mission, vision, and values."

"With our foundation in materials and our unstoppable imagination, we will enable the next evolution of the cloud, 3D sensing, electric vehicles, additive manufacturing, the commercialisation of space, and the personalization of health care, just to name a few."

"We are together on a journey towards a future that will be increasingly mobile, intelligent, and electric, accelerating the pace of innovation and enabling a stream of spectacular successes that will sustainably change the world around us," added Mattera.

Optical transceiver market to reach $24.7B in 2027

THE OPTICAL transceiver market will reach $24.7 billion in 2027, according to Yole Group's latest research. Social networking, business meetings, video streaming in UHD, e-commerce, and gaming applications continue to drive growth. In addition, expanding machine-to-machine applications, such as smart meters, video surveillance, healthcare monitoring, connected drives, and automated logistics, contribute significantly to device and connection growth and push the expansion of data centre infrastructure.

Martin Vallo, senior analyst, Photonics, specialising in optical communication and semiconductor lasers within the Photonics and Sensing division at Yole Intelligence, part of Yole Group said: "Revenue generated by the optical transceiver market reached around $10.4 billion in 2021 and is expected to reach $24.7 billion in 2027, which is a 15 percent CAGR for 2021-2027. This growth is driven by high-volume adoption of high-data-rate modules above 400G by big cloud service operators and national telecom operators requiring increased fibre-optic network capacity."

The evolution of multiple technologies has enabled data rates of 400G, 600G, 800G and beyond across data centre infrastructure and in long-haul and metro networks. 400GbE deployments are ramping across data centre networks. Many cloud providers and telecom operators are now starting to deploy an 800 Gbit/s optical ecosystem to increase bandwidth capacity and keep pace with the growing demand for data.

Optical modules have become an essential technology in telecommunication infrastructure. The development of semiconductor technologies such as lasers, modulators, and DSPs has enabled increased bandwidth and accelerated data rates.

Optical interconnects are ubiquitous and are intended to provide high bandwidth even for very short-reach applications, such as high-power computing and AI/ML applications within data centres. SiPh as a technology platform, co-packaged optics assembly as a new switch architecture, and coherence in compact form factors are the trends that will drive the market for the next five years.

Today's modern Ethernet-switch ASICs providing 25.6 Tb/s total capacity are running at a 50 Gbit/s SerDes lane rate driven by 50G PAM-4 modulation technology. In line cards, a re-timer is typically needed to synchronise PAM-4 data from the switch to the optical interface. In 400G optical modules, an additional silicon gearbox chip can be used to convert 50G PAM-4 electrical I/Os to 100G per wavelength optical I/Os to connect to 100G single-wavelength optics. The next generation of ASIC chips expected in 2023 will provide 51.2 Tb/s total capacity and run at a 100 Gbit/s SerDes lane rate.

Intel announces hybrid III-V / silicon 8-wavelength DFB laser array

Intel Labs has announced the demonstration of a hybrid III-V/ silicon eight-wavelength distributed feedback (DFB) laser array integrated on a silicon wafer. It delivers output power uniformity of +/- 0.25 dB and wavelength spacing uniformity of ±6.5 percent that exceed industry specifications.

"This new research demonstrates that it's possible to achieve well-matched output power with uniform and densely spaced wavelengths. Most importantly, this can be done using existing manufacturing and process controls in Intel's fabs, thereby ensuring a clear path to volume production of the next-generation co-packaged optics and optical compute interconnect at scale", said Haisheng Rong, senior principal engineer at Intel Labs

Recent co-packaged optics solutions using dense wavelength-division-multiplexing (DWDM) technology have shown the promise of increasing bandwidth while significantly reducing the physical size of photonic chips. However, it has been very difficult to

produce DWDM light sources with uniform wavelength spacing and power until now.

Intel says this new advancement ensures consistent wavelength separation of light sources while maintaining uniform output power, resulting in meeting one of the requirements for optical compute interconnect and DWDM communication. The next generation of compute I/O using optical interconnect can be tailor-made for the extreme demands of tomorrow's high-bandwidth AI and ML workloads.

The illustration above shows eight micro-ring modulators and an optical waveguide. Each micro-ring modulator is tuned to a specific wavelength. By using multiple wavelengths, each micro-ring can individually modulate the light to enable independent communication.

The eight-wavelength DFB array was designed and fabricated using Intel's commercial 300 mm hybrid silicon photonics platform, which is used to manufacture production optical transceivers in volume. Intel says this innovation marks a significant advancement in the capabilities of laser manufacturing in a high-volume CMOS fab by utilizing the same lithography technology used to manufacture 300 mm silicon wafers with tight process control.

For this research, Intel used advanced lithography to define the waveguide gratings in silicon prior to the III-V wafer bonding process. This technique resulted in better wavelength uniformity compared with conventional semiconductor lasers manufactured in 3-inch or 4-inch III-V wafer fabs. In addition, due to the tight integration of the lasers, the array also maintains its channel spacing when the ambient temperature is changed.

Innoscience opens European R&D Centre in Belgium's 'GaN Valley'

INNOSCIENCE, a company founded to make the global energy ecosystem greener and more sustainable using high-performance, low-cost GaN-on-silicon power solutions, has expanded its European office with a new R&D center in Leuven, Belgium.

The new GaN power device R&D activity in Belgium is headed by Jan Šonský, Vice President of R&D. Šonský will lead the development of next-generation technologies in close collaboration with the company's R&D team at Innoscience's headquarters.

Innoscience's new R&D activity is situated in Leuven, near imec, a highly recognized center of excellence for advance semiconductor technology, and KU Leuven, well known for its activities in power electronics. Thus the new R&D team of Innoscience becomes the latest addition to the so-called 'GaN Valley' of Belgium.

The company aims to attract the best talent to execute its ambitious technology roadmap and become the undisputed leader in GaN power solutions. The newly established R&D center in Europe will play an important role in improving Innoscience's core GaN device technology and products, both in terms of performance and reliability. This will help the company remain at the forefront of future GaN-based technology innovation.

Denis Marcon, General Manager of Innoscience Europe, said: "We welcome Jan to Innoscience, and we are looking forward to benefitting from the work he and his team will do. Our devices are already delivering excellent performance at both low-voltage (30 V to 150 V) and high-voltage (650 V) ratings. We expect the new R&D centre to deliver even better performance, smaller size and ultra-reliability."

"Innoscience is 100 percent committed to gallium nitride" added Šonský. "I see a wonderful opportunity to drive our next-generation technology, enabling power electronics designers globally and across different markets to enjoy the high performance that InnoGaN brings, and revolutionize power applications as a result."

Marelli launches 800 V SiC-based inverters

MARELLI, an automotive supplier, has developed a new, complete platform of 800 V SiC inverters, ensuring improvements in terms of inverter size, weight and especially efficiency, which is a critical parameter in electric vehicles.

Due to its excellent performance at high temperature and high voltage – enabling smaller, lighter and more efficient solutions – SiC is recognised as a technology of choice for power electronics. Thus, it is particularly suitable for inverters, which convert DC power derived from batteries to AC electric power used in electric vehicles' motors. In addition to this, Marelli's new 800 V inverter platform also features an optimised thermal structure, thanks to innovative structural and cooling channel designs that drastically reduce the thermal resistance between the SiC components themselves and the cooling liquid. This is a critical aspect in high-power applications, where the heat rejection of the power module is significant.

Among the main advantages, the new inverter platform presented by Marelli can extract more energy from the battery at a higher efficiency and secure a significant increase in the driving range of a vehicle. It also ensures faster charging times and better acceleration. Finally, a smaller and more efficient inverter allows a reduction in battery size, which delivers cost, weight and sustainability benefits.

"The new inverters platform based on our 800 Volt SiC power module technology allows to serve applications where energy use is optimised, the performance is maximised and efficiency is dramatically improved" said Razvan Panati, head of Power Electronics Technology of Marelli's Vehicle Electrification Division. "With a complete range of modular solutions, we are able to offer to our customers more flexibility in terms of packaging, cooling system design and energy storage."

The software for all the inverters in Marelli's range is developed in-house by the company and is hosted by an Electric Control Unit located in the same inverter case. The software is compliant with AUTOSAR (AUTomotive Open System ARchitecture) standards and specifically customised for the diagnostic standards required by car makers. Functional Safety requirements are compliant to ASIL D (Automotive Safety Integrity Level D) standard.

The new 800 V SiC platform completes the inverters range offered by Marelli, resulting from over ten years of experience that includes also 400 V solutions based both on IGBT and SiC, and GaN-based converters in development.

The inverters range is part of the solutions Marelli showcased at its booth at the 22nd edition of the International VDI Congress 'Dritev', one of the largest industry events in Europe in the field of drivetrain and transmission.

At the congress, the company exhibited its portfolio of technologies for vehicle electrification, that includes a full selection of single components, as well as subsystems, up to solutions for the complete integrated vehicle energy management system, applying a 'tier 0.5' approach, with the integration of thermal management into the electric powertrain. Alongside inverters, also electric motors, integrated e-axles systems, battery management systems, and solutions for managing all-vehicle thermal systems are part of the company's technological offering.

IQE steps up to VCSEL growth

Following its multi-year supply agreement with Lumentum, IQE is ready to take on more epiwafer supply deals. **BY REBECCA POOL**

IN LATE JUNE THIS YEAR, UK-based epitaxial wafer supplier IQE signed a multi-year agreement with California laser developer, Lumentum, to supply epiwafers for 3D sensing, automotive lidar and optical networking applications. The deal follows many years of development between the two companies – IQE has supported Lumentum's volume ramp of large-scale VCSEL arrays – and ensures Lumentum will have both a secure supply of wafers and development resources for future products.

At a time when OEMs are demanding more and more photonics systems rather than components, and photonics integration is driving vertical integration across the sector, Pelzel reckons that the latest partnership will ensure a swifter delivery of products to market. "We have been able to get products to market faster than our vertically integrated competitors," he says. "It's a little counter-intuitive but from our observations, if you can link your core competencies together with appropriate agreements and you have a good working

relationship... you will have dedicated capacity and you can reduce your time to market."

IQE now intends to secure more long-term wafer supply agreements with other partners, which combined with the Lumentum deal, can only spell good news for manufacturing in the UK. In recent years IQE has been installing MOCVD reactors at its Newport foundry in South Wales for 6-inch GaAs wafer production. The site currently has at least ten fully-qualified reactors and will be adding more in the future.

"Newport is our centre of excellence and preferred place for VCSEL manufacture, but we can also do this in Massachusetts and Taiwan," highlights Pelzel. "Our priority is to fill up Newport [first]."

According to Pelzel, 6-inch GaAs production could be easily ramped up at Newport, and the reactors are also upgradable to 8-inch wafer sizes. The furniture within the reactors could also be modified to handle 4-inch InP substrates. "We can produce eight-inch gallium arsenide epiwafers, but then of course these would need to go to a fab that has an eight-inch tool set – this is what I would call the rate-limiting factor here," he says.

VCSEL future

So what now for IQE and Lumentum? The partners are currently manufacturing 6-inch GaAs epiwafers and VCSELs for the high-volume 3D sensing smartphone market, but also have high hopes for automotive lidar applications, which are slated to present huge growth opportunities for players up and down the supply chain. Here VCSELs could be more widely used in driver monitoring and infotainment systems, and eventually find application in the advanced driver-assistance systems of autonomous vehicles.

These applications will demand longer-wavelength VCSELs, and development of epiwafers for these devices is well underway at IQE. The company has been working with dilute nitride materials for nearly two decades, adding small amounts of nitrogen to GaAs-based materials to stretch device wavelengths to 1500 nm. Near-infrared and visible wavelength photodetectors, edge-emitting lasers, and VCSELs have been demonstrated on wafer sizes up to 150 mm in diameter, and key target markets are smartphone sensors and lidar.

"No-one has found a way to [deposit dilute nitride layers] properly or effectively with MOCVD – to date, the only reliable material has come from MBE," explains Pelzel.

High-volume markets also demand larger wafer sizes. To this end, IQE has also been busy developing its IQGeVCSEL 150 technology for 6-inch VCSELs on germanium. The use of germanium to manage strain is critical to growing high quality, flatter epi-wafers, and as Pelzel says: "This becomes very, very important [at larger wafer sizes]."

And critically, the technology also provides a route for VCSEL growth on up to 300 mm silicon substrates via the company's germanium-on-silicon templates. As part of the larger wafer picture, IQE partnered with wafer manufacturer GlobalFoundries in late 2021, and earlier this year the company announced the world's first commercially available 200 mm VCSEL wafer, manufactured on germanium.

"Once you are on a 200 millimetre platform you can communicate with players that currently do not play in the compound semiconductor industry... you start to speak the language of the very large silicon foundries, such as Global Foundries," says Pelzel. "[Larger wafer sizes] also allow you to utilise leading-edge fabrication equipment."

Pelzel won't comment on whether or not IQE is working with Lumentum on dilute nitride and germanium technologies, but as he says: "Our strategic partners are prime candidates for test-beds.... and these [technologies] would be part of the toolbox we can offer to all of our customers."

Looking to the future, Pelzel is certain that the development of IQE's technologies for long-wavelength emission will continue at high speed as will the transition to larger and larger diameter wafers. "But we've also got an integration play," he says. "The VCSEL layer stack that we grow will need to look a little bit different so customers can integrate it with CMOS in different ways."

And he also expects GaN material systems to be a 'key focal point' of IQE's activities for both RF and photonics devices. For example, the company recently partnered with Porotech, to scale and commercialize GaN-based microLEDs. "Power electronics will be big in GaN, but in my view microLEDs will be the biggest pull for eight-inch volume for compound semiconductors," he says. "Then this will enable everything else."

Glorious GaN takes centre stage at CS International

Speakers at CS International highlighted how GaN devices are now combining higher blocking voltages with exceptional efficiency, delivering incredibly high power densities in the RF, and covering all of the visible spectrum in the form of the microLED

BY RICHARD STEVENSON

STRENGTHENING its well-established credentials, CS International continues to cover the biggest breakthroughs within the compound semiconductor industry.

At the most recent CS International, co-located with PIC International and Sensors International and held in Brussels on the 28-29 June 2022, leaders from industry and academia delivered almost 40 talks covering compound semiconductor devices and related materials. Those presentations were delivered in five sessions entitled: Faster, more fugal networks; Exploiting GaN's glorious potential; Building a multi-billion dollar SiC industry; Superior surface-emitters; and Multiple markets for the microLED.

The 600 or more delegates at AngelTech – the umbrella name for CS International and its two co-located events – also benefitted from tremendous networking opportunities in the exhibition hall. In this area, just outside the auditoria, those attending could converse with speakers or ask about the latest advances in equipment and support services provided by the 70 sponsors.

During the presentations at CS International, many widely held views within industry came under scrutiny. Those in attendance would have left pondering whether silicon really is the best substrate for GaN power devices, whether MOCVD is the most suitable technique for growing them, and whether AlInGaP is going to play a role in displays based on the microLED.

The switch to sapphire

For many years, SiC has been by far the most widely adopted foundation for making GaN RF devices. That's not the case for power devices – this substrate is too expensive, so silicon dominates. But what about sapphire, which underpins countless LEDs? Could this have a role to play outside the optoelectronic domain?

According to Transphorm's CTO Geetak Gupta, sapphire is a great option for extending the breakdown voltage of GaN power devices. He argued that for 1.2 kV transistors, FETs formed from GaN-on-sapphire can deliver an efficiency as high as 99 percent. That's enough to outperform SiC MOSFETs, and will enable GaN FETs to be in a strong position to serve in a new generation of electric vehicles, which will employ electronics with a breakdown voltage of around 1.2 kV in automobiles incorporating 800 V batteries – that's double the standard battery voltage used today.

Note that Transphorm has no intention of switching the substrate of its 650 V GaN FETs from silicon to sapphire. That's because these devices already have the upper hand over their SiC equivalents by offering an efficiency that's 25 percent to 38 percent higher when delivering powers just short of 10 kW. But at higher voltages the case for switching to sapphire is compelling. To produce a blocking voltage of 1.2 kV or more, the thickness of a GaN epilayer on silicon must exceed 10 μm. That adds cost, hampers throughout and threatens to distort the wafer.

Here sapphire is a great solution, championed Gupta. He explained that it is cheap, widely available in the 200 mm format, its insulating nature allows a reduction in the total epitaxial thickness for a given blocking voltage, and wafers can be run through a CMOS-compatible line. What's more, packaging and dicing can draw on GaN LED infrastructure.

The team at Transphorm have produced a normally off device by combining a HEMT with a low-voltage silicon MOSFET. This hybrid, sporting a threshold voltage of more than 4 V and a leakage current exceeding 2 μA at 1.4 kV (hard breakdown is 2 kV), can pass more than 160 A when driven in pulsed mode.

Sapphire's weakness is its low thermal conductivity, but this can be addressed by thinning the substrate. Transphorm has reduced this to 200 μm.

Benchmarking the 1.2 kV FET with a buck-converter, which steps down the voltage from 900 V to 450 V at a 100 kHz switching frequency, showcases the potential of this GaN-on-sapphire technology. Conversion losses are 8-9 percent higher with a SiC MOSFET – and there is still room for optimisation of the GaN device, according to Gupta.

From MOCVD to HVPE

At CS International Kyma's CEO, Heather Splawn, challenged the standard growth technique for making GaN transistors, advocating "HVPE for HVPE" – a catchy phrase that is short for the use of hydride vapour phase epitaxy for high-voltage power devices. Splawn argued that for higher blocking voltages, such as 1.7 kV, devices should be vertical. This requires thick layers, which are better to deposit by the "faster and cleaner" HVPE process. Growth needs to be on native GaN, which is pricey today, but costs should come down as volumes rise, according to Splawn.

Kyma has a very strong pedigree in developing HVPE reactors for the growth of GaN epilayers. It produced its first HVPE growth tool back in 1998, and is now offering its sixth-generation reactor, named Katharo. This tool can accommodate wafers with a diameter up to 200 mm, and form bulk layers with low levels of carbon at a growth rate of up to 150 μm/hr.

One criticism of HVPE is that it is inferior to MOCVD for the growth of sharp interfaces. Splawn and her colleagues are addressing this by developing technologies for moving from a high growth rate to a lower one, and from *n*-type to *p*-type material.

RF: Upping the voltage

For RF GaN, one handle for increasing performance is to turn to a higher supply voltage, as this provides a proportional boost to both the gain and the power density of the device. In addition, there is a change in the load-line resistance, generally making it easier to ensure impedance matching. The upshot of turning to a higher supply voltage is that it opens the door to a higher system efficiency at a lower cost.

A group at Fraunhofer IAF is pursuing this, developing GaN devices operating at 100 V. At CS International team spokesman Sebastian Krause described the challenges of going to higher voltages and the progress to date. He explained that shifting to a higher voltage increases the strength of the electric field, and in turn may lead to trapping of carriers, impaired reliability, a hike in leakage current and diminished current gain. While all these concerns can be combatted with the introduction of field plates, this may result in an additional output capacitance, which is a greater impediment at higher voltages.

The team from IAF have used 4-inch SiC as the foundation for producing AlGaN/GaN HEMTs with a dual field plate and through-substrate vias. The resulting 1.5 mm by 3.75 mm chips produce up to 600 W. "It's not that big a device, especially when considering the power it produces," remarked Krause.

RF measurements reveal a cut-off frequency of 10 GHz, suggesting the potential for operation through to the X-band. According to load-pull measurements at 7.2 GHz, power-added efficiency is 66 percent at 10 W/mm.

➤ Those attending CS International heard nearly 40 talks during the two-day meeting.

All across the visible

Production of full-colour LED-based displays involving direct emission tends to involve blue and green variants made with GaN an AlInGaP-based red emitters. A potentially simpler alternative is to just use GaN, but efficiencies plummet at longer wavelengths.

However, it is still possible to produce GaN LEDs covering the entire visible range. Demonstrating this at CS International, Ellie Galanis from Porotech presented a video that showed a tiny pixel covering all wavelengths, as well as producing white emission. The workings of this microLED technology, referred to as Dynamic Pixel Technology, were kept under wraps, despite attempts from the audience to extract those crucial details. However, Galanis did reveal that changes in wavelength came from variations in the driving conditions of the pixel.

The core technology behind Porotech's success is its porous GaN, which manipulates the strain threatening to thwart the efficiency of nitride LEDs in the red. Porotech has recently partnered with IQE to accelerate commercialisation of this approach.

Other materials

While GaN took centre-stage at this year's CS International, there were plenty of talks detailing important advances with other materials. They included: Infineon's expansion of SiC devices, occurring against a backdrop of a booming industry set to be worth $6 billion by the latter half of this decade (see p. 26); and NTTs development of InP membrane lasers to speed optical communication.

Further breakthroughs in various compound semiconductor technologies are sure to sit at the very heart of next year's CS International, which, following disruption from the Covid pandemic, will return to its traditional slot of early Spring. AngelTech is fixed for 18-19 April, 2023, located at The Sheraton Hotel in Brussels.

UK semiconductor inquiry: Government quizzes Nexperia, IQE, Rockley Photonics and more

Nexperia exec defends Newport Wafer Fab decisions while industry leaders look at UK's 'fragile' supply chain. **BY REBECCA POOL**

IN EARLY JULY some of the biggest names in the semiconductor industry gave evidence to the UK Business, Energy and Industry Strategy (BEIS) Committee, as part of a national security investigation into chip manufacturing.

The government probe follows the sale of UK's largest chip manufacturing plant, Newport Wafer Fab, to The Netherlands-based Nexperia, which is a subsidiary of China's Wingtech Technology. Critically, the South Wales factory supplies semiconductors to UK government, including under military contracts, which is believed to have triggered the government review.

During the latest round of questioning, Toni Versluijs, General Manager of Nexperia UK, was pressed at length by Committee member and Conservative Member of Parliament, Alexander Stafford, over the fallout that followed the deal. Why were members of the semiconductor community so 'clearly upset' with the takeover of Newport Wafer Fab by Nexperia, he asked. And was this linked to the perceived scrapping of plans for compound semiconductor manufacturing, came the follow-up question.

Unfazed, Versluijs was quick to highlight partial knowledge in the media on the complexities of Newport and the world of semiconductors.

➤ Top: Business as usual at Newport Wafer Fab?

"An illusion had been raised that there was a compound semiconductor open fab [at Newport]," he said. "Such a fab did not exist and does not exist – there were plans, and there were ambitions."

Versluijs also added that such plans could be 'realised' in the future, which led to Stafford raising the possibility of launching a spin-off company dedicated to compound semiconductor manufacturing. "We have provided such an option to use an unused building on the site of the Newport wafer Fab to start exactly such an activity," explained Versluijs. "What it would require is funding, a viable business case and a viable business plan – this option, to be honest, has been outstanding for almost a year."

Stafford went on to query rumours that the Newport Wafer Fab could potentially shut and move operations abroad within a year. Adamant that Nexperia had no plans to shut any of its operations, including Newport, Versluijs stated: "We invested big time in Newport, we created jobs, we are here to stay. We want to work in the local ecosystem and enable the local ecosystem and the UK semiconductor industry to be successful."

Still, the Newport buyout undoubtedly left some industry players disgruntled. In a separate session, Andrew Rickman, Chief Executive of photonics chip manufacturer, Rockley Photonics, told Committee member Paul Howell how his company has been forced to find an alternative manufacturing site following the acquisition. "We had intended to manufacture at Newport Wafer Fab, and we built part of the production line in there... [The fab] changed hands and the current owner, for business reasons known to themselves, does not want us to manufacture there," he pointed out. "They have honoured our relationship with them with regard to the development contract. We have had to move the volume manufacture elsewhere."

Rickman added how his company will now ramp manufacturing at a US foundry, but would be very happy to use a UK facility, if such a capability was available.

Semiconductor shortages

Nexperia aside, UK government has been keen to scrutinize the opportunities and vulnerabilities across its home-grown semiconductor industry following the global chip shortage. Throughout the latest inquiry session, UK industry leaders were repeatedly questioned over supply chain uncertainties.

Simon Thomas, Chief Executive of graphene device manufacturer, Paragraf, described the UK semiconductor supply chain as 'fragile', highlighting how assembly and testing have to be outsourced. "Advanced packaging does not really exist, although the Compound Semiconductor Applications Catapult is addressing that right now," he said.

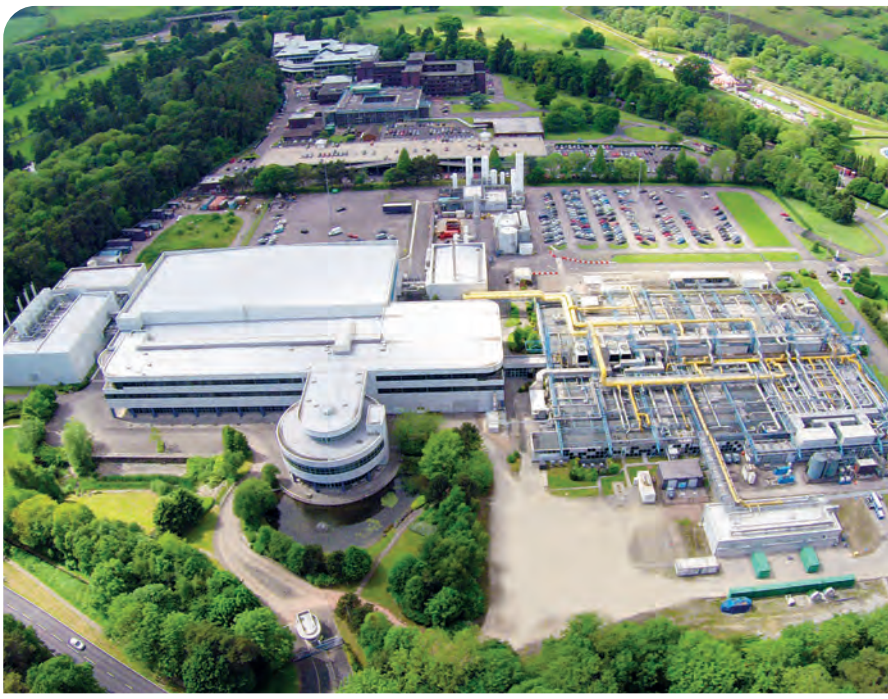
Meanwhile, Paul Williamson, Senior Vice-President and General Manager of Client Line of Business at Arm queried the rationale of a UK-only supply chain, given today's device complexities and development costs. "I agree that resilience in that supply chain is of strong importance but... there are at least 13 or 14 companies involved to create just a sensor cluster – it would be exceptionally challenging to think that we could make it fully resilient."

Indeed, Paragraf's Thomas emphasised the importance of having relationships with 'friendly countries'. "It comes back to that question about what it is the UK wants to secure. Which piece and which part do we want to secure? Which piece and which part can our friendly partners provide for us?" he said.

Ex-Global Foundries executive, Americo Lemos, now chief executive at IQE, explained how during the Covid-19 pandemic, the consumer electronics market scooped up available capacity for chip manufacturing, leaving little left for automotives when this sector recovered. "There was a surge in demand and then neither enough capacity nor investment going in," he said.

Lemos highlighted how plugging this gap isn't quick, saying "It takes three to four years to get a silicon fab up and running, and the investment is in the billions of dollars."

However, he did impress on the Committee how the UK is leading the world when it comes to creating a solid skills-base for compound semiconductors. "In this country there is the opportunity to create the same thing [as Taiwan and TSMC] in silicon but in compound semiconductors – the UK is really leading, that is why I'm here from California."



➤ Newport Wafer Fab: a site of controversy.

Gearing up for electric vehicles with Soitec's SmartSiC substrates

Offering a ten-fold reuse of single-crystal SiC and a ten times better conductivity than its conventional counterpart, SmartSiC is poised to revolutionise the production of power electronics for electric vehicles and industrial applications

BY OLIVIER BONNIN, ERIC GUIOT, WALTER SCHWARZENBACH, NOÉMIE BALLOT AND CÉLINE TRANQUILLIN FROM SOITEC

IF HUMANKIND has one task of utter urgency it is the reduction of carbon dioxide emissions. Following decades of spiralling emissions, we are now living in an age of catastrophic environmental and demographic damage, and without drastic action this situation is only going to get worse.

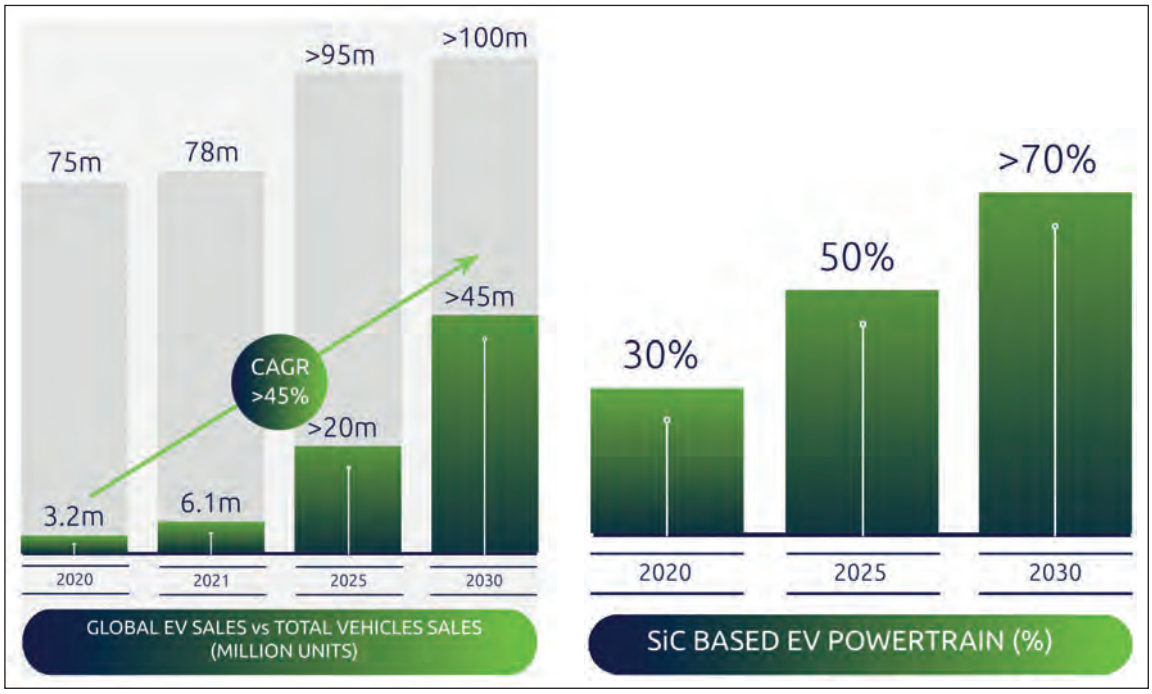
A significant share of today's greenhouse gas emissions come from transportation, traditionally a significant polluter. But this sector is embarking on a once-in-a-century transformation, driven by researchers, industries, institutions and customers – all stakeholders in the transportation ecosystem – coming together to shape a greener future. Sitting at the very heart of this industrial revolution are electric vehicles, the key driver to slashing carbon dioxide emissions associated with mobility.

Fuelling the uptake of the EV are falling prices, longer driving ranges and rapid charging times. Crucial to further advances in performance, which will spur sales to reach new heights, is the optimisation of the powertrain. It's a task attracting intense, cutting-edge R&D. In every EV the direct current from the battery is transformed into an AC form that drives the traction motors. The efficiency of the inverter that performs this function governs the efficiency of the drivetrain – increasing this is essential for improving EV performance..

Tesla, the world-famous pioneer of the EV, started introducing SiC devices into its vehicles in 2018. Since then, devices made from this wide bandgap semiconductor have been the undisputed and optimal choice for managing power conversion in drivetrains and on-board chargers. Note that the compelling case for SiC is only going to strengthen when the EV industry shifts from 400 V to 800 V systems for fast chargers. Due to this, penetration of SiC-based devices in EVs is to climb over the next decade from 30 percent to 70 percent, against a backdrop of an ever-increasing number of vehicles sold per year (see Figure 1).

With penetration of SiC-based devices and technologies climbing fast and EV sales skyrocketing in all major geographies, streamlined SiC supply chains are essential. Many power device manufacturers are fully aware of this need, and are responding with strategic moves, either investing in high-volume wafer manufacturing capabilities, or building vertical integration models and making strategic acquisitions to solidify supply chains.

While a shift to SiC may seem radical to some, the technology has in fact had an intensive maturation period with experts anticipating its arrival to the mass market for years. It's been just over 20 years since it emerged as a disruptive alternative to silicon in the power electronics industry. While chipmaking is more expensive and requires a more complex manufacturing process, this must be weighed against the increase in energy conversion efficiency. Over the last two decades, the cost of making SiC devices has fallen, partly through a migration from 25 mm wafers to ever larger diameters, with 200 mm now at the leading edge. Such gains have propelled the benefits-to-cost ratio for SiC to a level where there is no longer any discussion of whether this material is suitable for EVs. The breakthroughs have ensured that the SiC industry is an incredibly dynamic market, in terms of growth and design opportunities.



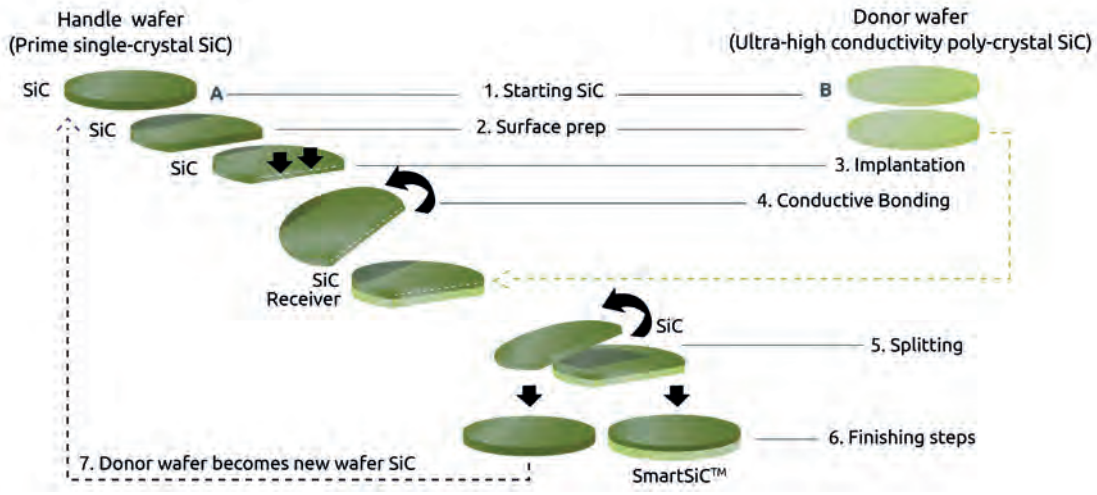
➤ Figure 1. Global EV's market trend and SiC penetration.

Yet despite all this promise and initial success, SiC has remained, until recently, a material that just serves in the high-end industrial sector, as well as other power-conversion applications. Expansion of the market has been hampered by a relatively narrow product offering from device manufacturers. There are only a few devices that have been specifically designed for EV applications, and their manufacturing yield has been compromised by the defectivity levels found in standard SiC wafers.

A physical barrier to realising a higher manufacturing yield is the range of intrinsic defects that arise during the manufacture of SiC boules using the incumbent process, physical vapour transport (PVT). These imperfections in the material prevent device manufacturers from hitting the required yield, causing chip production to be economically unviable. Yields are hampered by the large size of the chips. SiC MOSFETs with a unitary surface of at least 40mm^2 are required to ensure the handling of currents of 200 A, which are needed for the power levels of the EV traction inverter.

SmartSiC: the cutting-edge solution

Addressing this challenge is SmartSiC, the game-changing technology from Soitec. This is the latest expansion of our Smart Cut portfolio. Within this family, we ship more than 2 million wafers per year to a variety of product lines, including those for making devices for smartphones. It's a success story that has led us to be the largest pure-play supplier of engineered substrates for radio-frequency and mobile phone markets. Over the last few years we have laid the foundations to repeat that success in automotive and industrial markets with SmartSiC.



➤ Figure 2. The unique, patented Smart Cut process of Soitec, adapted to SiC material.

The strengths of SmartSiC

Christophe Maleville is CTO and SEVP Innovation, Soitec

Christophe, your SmartSiC technology is relatively young compared with SiC technology. How would you describe the maturity of SmartSiC?

CM: Soitec's SmartSiC technology is moving to the industrialization phase. We used our pilot line at CEA-Leti to develop, prototype and select a tool-of-record for high-volume manufacturing. We are now focusing on reducing variability, improving defectivity and yield, and optimizing the metrology sampling to start the high-volume manufacturing phase with an optimal process flow. We have 30 years of experience with Smart Cut in large volumes. Our advantage is that we can leverage this experience to now accelerate the maturation of our SmartSiC technology. And we are perfectly on time to get ready for manufacturing in 2023.

What level can you reach when considering product variability?

CM: Those who lead the development of SiC have done a fantastic job. They have introduced major improvements in SiC's crystal quality and diameter, and SiC devices are now already routinely powering electric vehicles that are driving on our roads. But every SiC boule and every wafer within each boule is different, bringing quite a significant variability to manufacturing. SmartSiC is lowering such variability by allowing us to use each single wafer more than ten times, thanks to our Smart Cut process. By using an epitaxy layer as a donor, I strongly believe that our next generation of SiC wafers, SmartSiC, will completely eliminate crystal-originated variability. By eliminating basal plane dislocations prior to layer transfer, every wafer sent for device manufacturing will be the same. This will be a major benefit for large-volume production and will close the gap with silicon technologies.

Can Soitec lead this revolution alone?

CM: This is indeed a revolution that will lead to major advancements in SiC device performance and metrics. But, of course, we are not doing it alone. We are collaborating with strategic partners on all fronts, from research and technology organisations to materials and equipment suppliers and leading device manufacturers. This is absolutely fundamental to accelerate the adoption of SmartSiC-based devices and the implementation of next generations. For the manufacturing of our first generation of SmartSiC wafers, which will kick off in 2023, the development cycle was extremely rapid: we went from initial development work to a volume ramp-up in only four years. This clearly demonstrates how efficient our model of close collaboration within the ecosystem is.

Drawing on 30 years of expertise with our Smart Cut process, through our SmartSiC wafers we offer a new and disruptive engineered substrate. This building block for making SiC devices introduces a new paradigm for the electrical performance of the wafer, the productivity of the supply chain, and the device power density. Merits of this engineered wafer, which creates significant value at both the device and the system level, include easing the adoption of eMobility and enabling enhancement of charging infrastructure and the renewable energy industry.

Our efforts at developing our Smart Cut technology have been driven by a team of engineers, working tirelessly at the Substrate Innovation Center of Grenoble, within CEA-Leti. Their success allows us to leverage: the exceptional physical characteristics of single-crystal SiC substrates, which are used as a donor and enable a ten times re-use capability; and an innovative, highly-electrically conductive polycrystalline substrate, acting as a handle wafer, that ensures a reduction in the device's on-resistance. We showcased our cutting-edge, high value-added engineered substrate technology last year, in issue VI of *Compound Semiconductor*. Here we go one step further, presenting the maturity of SmartSiC, the milestones towards its wide-scale adoption, and the steps we will take to drive further innovation.

Greener, faster, better

SmartSiC is a technology that is greener, faster and better in both its 150 mm and 200 mm formats. These strengths have put it on a trajectory to become one of the industry standards for the SiC market. It provides a plug-and-play solution that can seamlessly integrate into all existing power supply manufacturing lines and deliver significant commercial, environmental, and manufacturing benefits compared with traditional SiC substrates.

The greener footprint comes from the simple, energy-efficient manufacturing processes for making SmartSiC. Compared with traditional SiC, carbon dioxide emissions are reduced by up to 70 percent per wafer.

Faster deployment of these large size substrates stems from re-use of scarce, 200 mm single-crystal donors. By adopting this approach, we help to sustain market growth.

Our SmartSiC provides a better way to produce power electronics devices, by combining a superior manufacturing yield with better efficiency and a higher power density. Empowered by a higher conductivity compared with bulk SiC, SmartSiC enables an increase in current density of more than 20 percent for a range of power devices, including MOSFETs and diodes. This is the secret formula for unleashing a new generation of power devices.

We have two flavours of SmartSiC. One is SmartSiC-Performance, which is being prototyped and is moving through qualification trials with Soitec

customers. The other, SmartSiC-Advanced, provides a substrate that is free from basal plane dislocations (BPDs). This product, now in the sampling phase, is being developed by our innovation team.

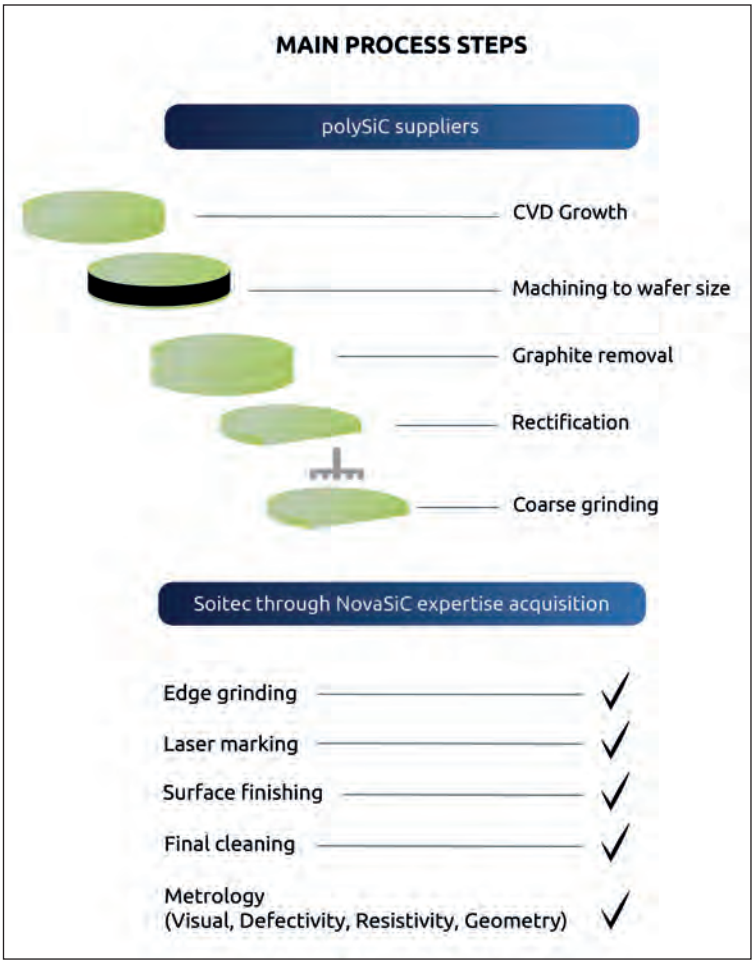
Employing an optimised design, our SmartSiC substrates feature a state-of-the-art single-crystal SiC layer that's thinner than 1 µm, on top of an ultra-high-conductivity polycrystalline SiC handle substrate. These engineered substrates, with diameters of 150 mm or 200 mm, have a total thickness of 350 µm or 500 µm, respectively. When producing a second SmartSiC wafer, we re-use the donor wafer, minus the few microns used for the first SmartSiC wafer. By repeating this process again and again, we yield a minimum of ten SmartSiC wafers per donor wafer.

The production of polycrystalline SiC, which provides a handle wafer for each SmartSiC, uses a CVD process. This is quicker and more environment-friendly than PVT, needed for high-quality single-crystal SiC wafers. Our polycrystalline SiC that we source from external suppliers has adequate doping to control the substrate's electrical conductivity while maintaining a highly competitive cost (see Figure 3). Drawing on a high level of maturity and expertise developed over many years, we are able to define and ensure the perfect geometry for our engineered SiC substrate, key for mastering the bonding of the wafers. Our acquisition of NovaSiC in November 2021 has equipped us with more than 25 years of experience in SiC wafering, strengthening our capabilities.

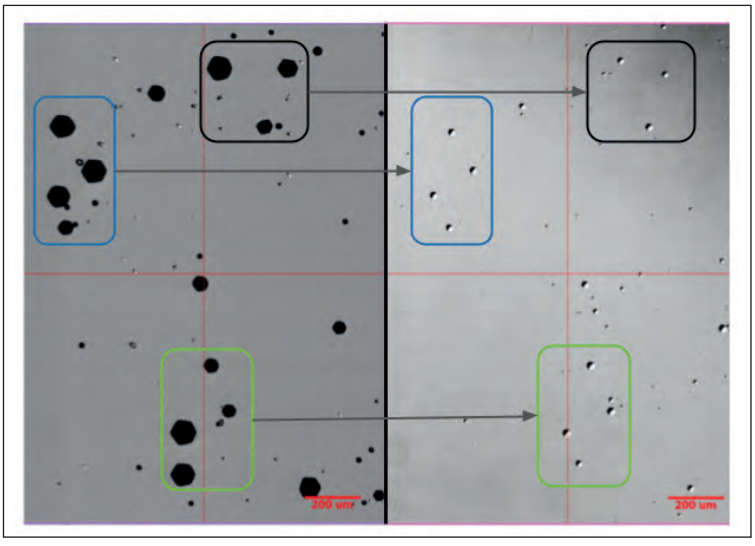
We now have a highly capable, stable process and design for our SmartSiC substrates. These wafers have been tested and prototyped intensively and at large scale; and we have confirmed the value they bring to the market, to power devices and to power systems. Measurements of MOSFETs and diodes incorporating our SmartSiC engineered substrates show significant, irrefutable performance improvements, as well as enhanced long-term reliability and high-temperature robustness. These attributes have motivated several device manufacturers to commit significant resources to adopting and implementing SmartSiC technology when qualifying their next-generation products.

Glimpsing into the R&D kitchen

A target for our R&D team is to take the manufacturing yield of SiC to the globally accepted standards applied to silicon-based power devices. This ambitious goal is within reach, thanks to the capability of the Smart Cut process to maintain the crystal quality of the incoming donor wafer. According to inspection of our engineered wafers etched with a potassium hydroxide solution, as the decorated crystal defects we observed on the donor and SmartSiC surface are at the same locations, we know that our technology does not introduce additional imperfections. To verify this and improve the defectivity level, we have performed the



➤ Figure 3. Main process steps for manufacturing polycrystalline SiC.



➤ Figure 4. Etching with potassium hydroxide enables crystal defect characterization. Decorations are easily visible with an optical microscope, allowing comparison between a single-crystal SiC donor (left) and SmartSiC (right).

Substrate	Standard 4H-mSiC	SmartSiC-Advanced
BPD density (/cm²)	~ 500	< 0.1

➤ Table 1. Basal plane dislocations and defectivity density in the donor SmartSiC-Advanced substrate.

Smart Cut process on a donor that is free from BPDs. Transferring a layer that is free from BPDs is behind our SmartSiC-Advanced substrates (see Table 1 for BPD density values for this class of engineered substrate).

One of the merits of having a BPD-free layer at the top of a SmartSiC-Advanced substrate is that it provides an excellent seed layer for drift epitaxy. This layer slashes the density of potential nucleation sites for killer defects, expands the epitaxy process window, and simplifies the epitaxial stack, which no longer needs a conversion buffer.

According to our simulations of yield and our experiments, the improvements that result from our BPD-free layer drive down the induced epi-grown killer-defect density by a factor of ten. The upshot is a hike in manufacturing yield of more than 20 percent for devices with areas of 20 mm^2 or more.

Removing BPDs also aids device reliability: it prevents dislocations from gliding and eliminates bipolar degradation. Insiders of the SiC industry expect the absence of BPDs to deliver a substantial improvement to the production process, with manufacturing yields expected to climb towards 90 percent.

Another asset of our SmartSiC, achieved through the high doping level of the polycrystalline SiC handle substrate, is the ease of forming a back-side ohmic contact for the SiC power device – either a MOSFET or a diode. Thanks to this, we recently demonstrated an annealing-free ohmic-contact process that can be easily implemented on SmartSiC substrates without compromising long-term die assembly reliability. We have started to sample our SmartSiC-Advanced 150 mm engineered substrates. Prototypes are under evaluation by our key customers, and they are available to other customers on demand. At this year's ICSCRM, to be held in Davos, Switzerland, in mid-September, we will present detailed data associated with our SmartSiC-Advanced technology, and deliver four papers.

Ramping production

Our next step is, of course, high-volume production. Paving a path towards this goal, in March 2022 we broke ground at our new factory site, Bernin 4. It will be dedicated to the large-scale manufacture of SmartSiC, with production slated to begin in mid-2023 (see Figure 5). Equipped with this state-of-the-art infrastructure, we will ramp-up SmartSiC production in 2024 and beyond, to reach a total annual capacity of 150 mm and 200 mm wafers of 1 million by 2030.

Production will be dominated by 200 mm SmartSiC. Part of the motivation for majoring on this format is that our experience, over several decades, indicates the exponential benefits of increasing wafer size. When we supply the SiC industry with 200 mm SmartSiC wafers, manufactured with ten-times re-usability, we will make a massive difference to optimising the use of resources. We will relieve pressure in supply chains and enable efficient, accelerated production and adoption of our engineered substrates in automotive and industrial markets. We have already laid the groundwork for this revolution. Multiple partners have evaluated our SmartSiC-Performance prototypes (see Figure 6), and are impressed with

➤ Figure 5. Soitec's new plant, Bernin 4, located in south-east France.

Figure 6. SmartSiC wafers in 150 mm and 200 mm formats.

them. Throughout this year we are enlarging and accelerating this qualification phase.

SmartSiC: A new industry standard

The electrification of the automobile is a once-in-a-century transformation that is generating a deluge of innovation. During the previous revolution in transportation, dating back to the early 1900s, it took 15 years for the world to switch from the horse-driven vehicle to mechanical mobility. Let's hope that the transition from gasoline-powered vehicles to EVs will be far faster, given the urgent need to cut carbon dioxide emissions and curb global warming.

We are already underway, as following in the footsteps of Tesla, many makers of EVs are now adopting SiC. Nevertheless, there are numerous hurdles to overcome, in terms of electrical performance, productivity, cost and yield, before SiC can take centre stage in the EV sector. We have anticipated these challenges and the upcoming demand from the EV industry, responding with the development of SmartSiC, a higher value-added alternative to the single-crystal SiC substrate. As our purpose statement says: 'In our soil grows an amazing future.'

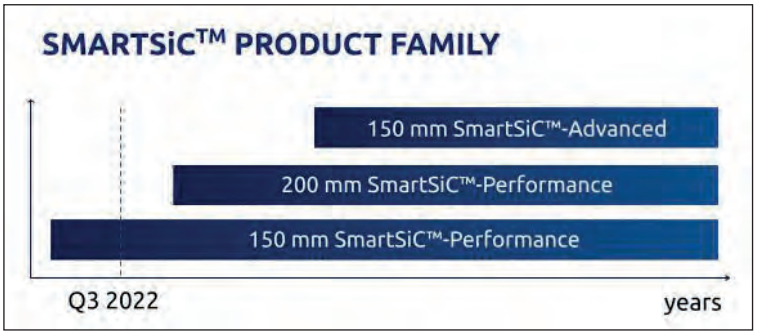


Figure 7. The SmartSiC industrialization roadmap.

Pierre Barnabé appointed new CEO of Soitec

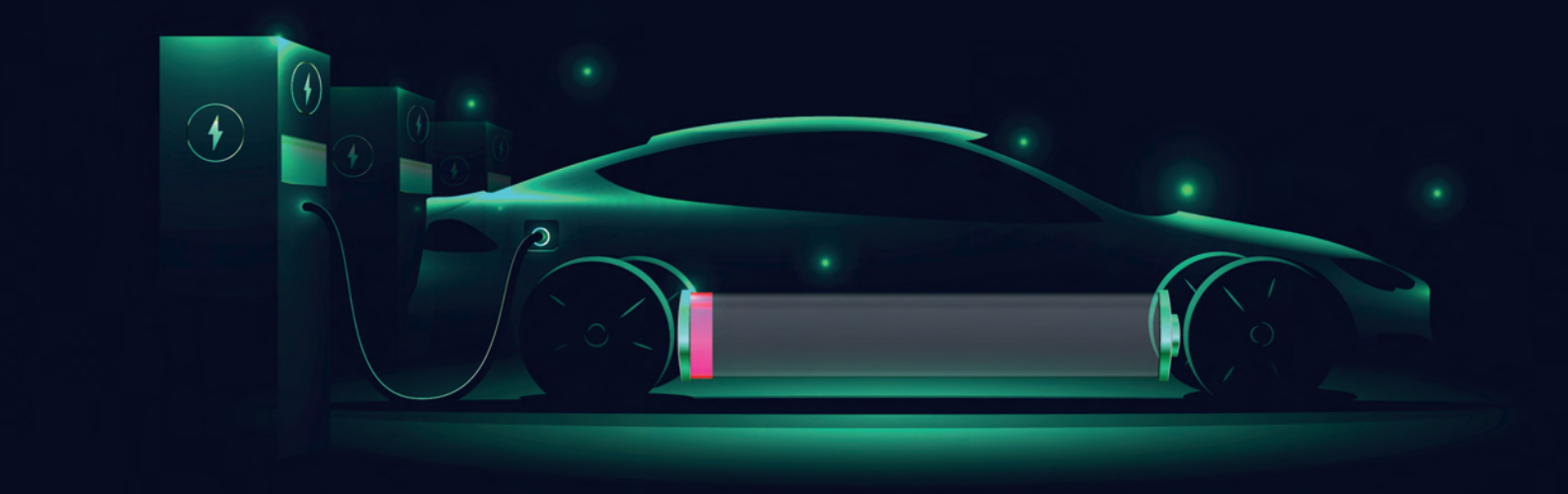
Pierre Barnabé took up the position of Chief Executive Officer of Soitec on 26 July, 2022, after joining Soitec in May 2022.

Between 2015 and 2021, Barnabé was Executive Vice-President of the Atos group in charge of the Big Data & Cybersecurity (BDS) division. He also managed the group's Public Services & Defense and Manufacturing activities and was interim group CEO in 2021. Before its acquisition by Atos in 2014, he was the Deputy CEO of Bull, the unique European leader in supercomputing, electronics for artificial intelligence, cybersecurity and cyberdefense from 2013 to 2015. From 2011 to 2013, he was Managing Director of the Enterprise branch of the French Telco SFR. Prior to this, he held various positions at Alcatel then Alcatel-Lucent.

Full speed ahead for SiC

As shipments of SiC substrates and devices soar over the next few years, several companies are setting their sights on annual revenues of more than a billion dollars from this sector

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR



➤ The ramp in sales of electric vehicles is driving a tremendous hike in revenue for the SiC industry.

There's no doubt that sales of SiC devices are going to climb over the coming years, driven by efforts to expand material supply and chip production. However, even when one has taken this on-board, it's still easy to overlook just how step a trajectory is anticipated.

Those that do have a good handle on the exceptional pace of growth that's expected for the SiC industry include those that attended this year's CS International, held at the Sheraton Hotel at Brussels Airport on 28-29 June. During a session entitled *Building a Multi-billion Dollar SiC Industry*, delegates heard from market analysts, producers of chips and equipment manufacturers – all of them underscored the rapid rate of growth in the SiC sector and the drivers behind it.

Billions and billions

According to Poshun Chiu, Technology and Market Analyst at Yole Intelligence, the SiC market will grow from around $1 billion in 2021 to more than $6 billion by 2027. Over that timeframe the compound annual growth rate will be an astonishing 34 percent.

Most sales of SiC power devices are associated with the automotive industry, explained Chiu, with chips being deployed in battery-powered vehicles, such as cars made by Tesla. He claimed that in 2021 this accounted for 63 percent of all SiC revenue, and forecast that by 2027 it will be worth a 79 percent share. The majority of the rest of the revenue is attributed to a combination of: industrial markets, including charging stations; the energy sector; telecom and infrastructure; and transportation, which includes the railways.

Tipped to dominate sales over the next few years are four companies with ambitions to generate annual sales from SiC activity of at least one billion dollars. The most prominent is Wolfspeed, a vertically integrated manufacturer of SiC products with expertise in the production of wafers, epiwafers, bare die, packaged chips and modules. It is setting its sights on sales of $1.5 billion by 2024/5, driven by a ramp in the shipment of devices. The other multinationals with big plans for SiC are: STMicroelectronics, a supplier to Tesla that also manufactures bare die, packaged chips and

modules, and is expecting its SiC revenues to total $1 billion or more by 2024; Infineon, a maker of bare die, packaged chips and modules, that is targeting $1 billion of sales by the middle of this decade; and onsemi, yet another producer of bare die, packaged chips and modules, that is aiming for $1 billion of SiC revenue by 2023 – with 70 percent of sales attributed to the inverter of the electric vehicle.

These four giants of this industry, plus some of the other leading players, are all making colossal investments in infrastructure over the next few years.

These two European heavyweights ST and Infineon previously announced total capital expenditures of $2.1 billion and $1.6 billion, respectively, in 2021.

This expenditure included investment in SiC production lines. ST used funds to expand the capacity of its 150 mm facilities in Catania and Singapore. Meanwhile, Infineon, which is investing a further $2.4 billion this year, is converting of a 150/200 mm silicon line in Villach, Austria, to SiC and GaN; and funding improvements to a facility in Kulim, Malaysia, that will expand wide bandgap epitaxy and 300 mm silicon capacity.

More modest amounts are currently being invested by onsemi and Wolfspeed, which began a $1 billion investment in its 200 mm fab back in 2018. The US SiC specialist is currently expanding its material and device level capacity, having spent around $0.5 billion in 2021, with plans to invest a similar figure this year. Meanwhile, onsemi paid $415 million last year to acquire SiC crystal boule maker GTAT, and in the 15 months running up to this spring it invested around $0.6 billion in a capacity expansion supporting SiC activity.

Rohm, which Chiu describes as a "very important Japanese player", has earmarked $3.5 billion for investment in the coming 5 years. This will fund the construction of a new 200 mm line at its Apollo facility. In addition, the company has set aside almost $440 million to secure SiC raw material.

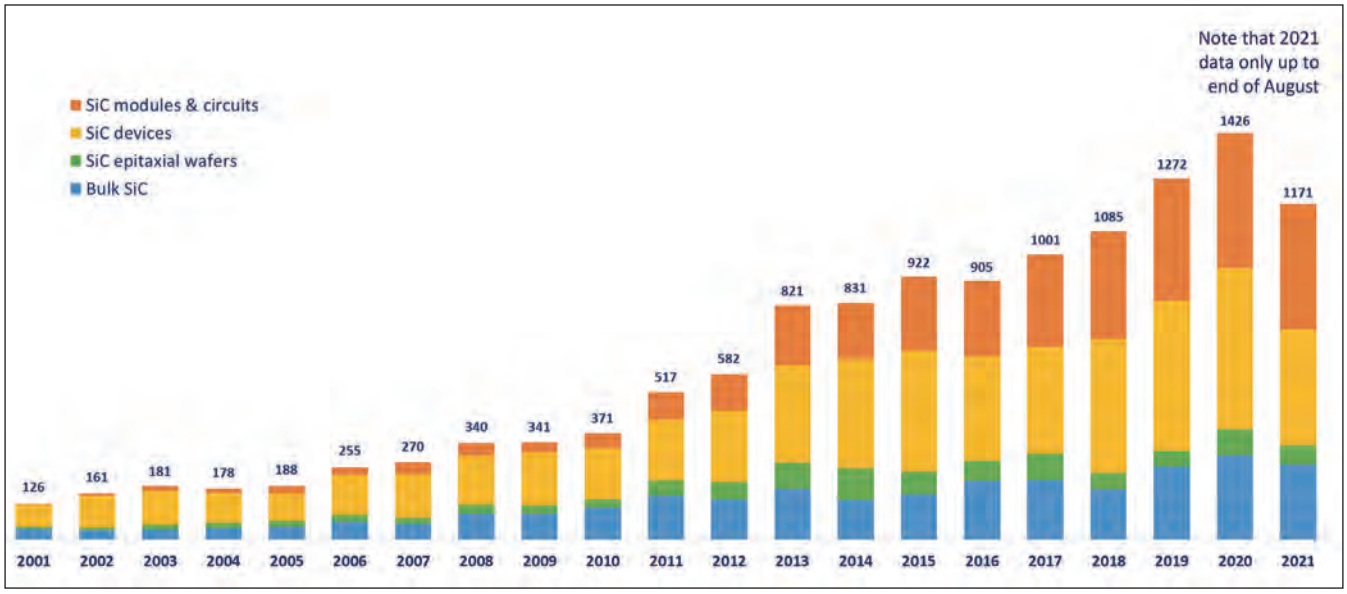
II-VI, which following an acquisition of Coherent is planning to trade under that name, also has an ambitious outlook. Over the next ten years it expects to spend $1 billion on its SiC activities, with strong interests in device business in the years to come.

It is of no surprise that the great prospects for SiC is leading to a number of mergers, acquisitions and partnerships. Chiu presented a timeline capturing this, which highlighted that there has been much activity over the last couple of years. While acquisitions tend to grab the headlines, such as Soitec's purchase of NovaSiC and Qorvo's buying of UnitedSiC, the sharing of IP plays a big role in the evolution of the industry. Examples include II-VI licensing technology from GE, and Vitesco Technologies, a maker of drive technologies, working with both Rohm and Infineon.

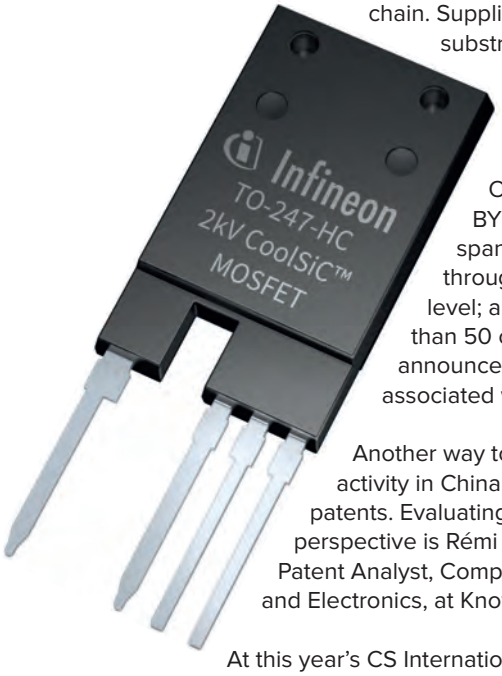
One trend that exists in every sector of the semiconductor industry is that as revenues increase, manufacturing shifts to larger wafers. That's taking place in the SiC industry, with several companies already demonstrating a 200 mm platform. But that's not the only important advance, according to Chiu: engineered SiC substrates are being pioneered by Soitec and Sumitomo, there is innovation in SiC growth technology at KISAB, and Infineon and Disco are breaking new ground in wafering processing.

China's charge

So far, China is yet to make a big impact in the SiC sector. But this is sure to change, as it's already laying the foundations for success, with companies now operating at all levels within the supply



➤ Figure 1. Patent filings reveal that China will become a major player in SiC in the coming years.



➤ Infineon is expanding its portfolio of SiC MOSFETs through the introduction of devices operating at 2 kV.

chain. Suppliers of SiC boules, substrates and epitaxy include the leading Chinese player in this sector, TankeBlue, and SICC and Sanan Optoelectronics; while BYD Semiconductor is spanning chip processing through to the system level; and there are more than 50 companies that have announced business plans associated with SiC.

Another way to monitor the growth of activity in China is through the filing of patents. Evaluating developments from this perspective is Rémi Comyn, Technology & Patent Analyst, Compound Semiconductors and Electronics, at Knowmade.

At this year's CS International, Comyn highlighted the dramatic growth in patent filing by Chinese companies over the last few years. It is his view that this country's patent activity took off in 2015, and by 2020 it started to lead the world (see Figure 1).

"While very few Chinese players are making products, we can see an ecosystem in the patent activity," remarked Comyn, who named a number of companies with IP for bulk and bare wafers, for epitaxial substrates, for devices, for modules and for circuits. He explained that the nascent SiC industry is supported by research at the country's universities, and the funding of projects that bring many partners together. Efforts are also aided by building on existing infrastructure in power electronics and in compound semiconductor technologies, such as optoelectronics.

Comyn has also considered the type of patent that's been filed, and how this has changed since the start of the millennium. He pointed out that if you go back more than a decade you will find that patents on bulk SiC and SiC devices dominated, while since 2015 there has been a shift to patents associated with SiC devices and modules. Filings associated with SiC epiwafer IP have remained relatively limited, but bulk SiC IP activity has been very active over the past decade.

➤ Aixtron's Senior Product Manager Nicolas Müsgens told delegates at CS International that the strengths of the G5WW C include very efficient consumption of metal-organics and high throughput, thanks to the opportunity to swap wafer carriers at temperatures in excess of 600 °C.

Infineon's expansion

Details from one of the big-four within the SiC industry, Infineon, were provided in a presentation by company Vice President of SiC, Peter Friedrichs.

Like many of its rivals, Infineon has a vast power portfolio, with devices made from silicon, SiC and GaN all spanning a wide range of voltages. Friedrichs explained that the company is complementing each of its silicon devices with an alternative based on a wide bandgap semiconductor: the OptiMOS silicon technology is now complemented with the GaN e-mode lateral HEMT; the silicon superjunction has both this GaN HEMT and the SiC MOSFET as alternatives; and the latter offers a second option to the silicon IGBT. Friedrichs argued that Infineon is well-positioned for success, claiming "experience is very useful". The company has been active in SiC for more than 25 years, and brought the first SiC diode to market back in 2001.

Over the years Infineon has expanded the markets it serves. Back in 2017 sales to makers of solar string inverters accounted for around 87 percent of all the company's SiC revenue. For 2021, this market still brought in more money than any other, but only accounted for 29 percent of all sales. Significant revenue has also come from sales to makers of uninterruptible power supplies, the transportation sector, the energy distribution and storage industry, and those working in transportation.

According to Friedrich's, in 2021 sales of SiC devices netted Infineon $200 million, and should climb by more than 90 percent this year. He told the delegates in Brussels that the company's target of $1 billion of annual revenue from SiC should be hit by the middle of this decade, by which time the automotive market will generate about half of these sales, with the other half attributed to the industrial sector.

Friedrich's claimed that Infineon has the broadest and best SiC portfolio. There are discrete products and modules for the industrial market spanning 600 V to 1.7 kV, and alternatives for the automotive market ranging from 650 V to 1200 V.

Supporting this portfolio is a range of other products. According to Friedrichs, controllers, drivers and switches can come together to produce systems that combine the highest lifetime and reliability with the fastest charging cycles, in a compact design that increases power density by up to 30 percent.

Friedrichs also championed the company's new die attach process, known as .XT technology. This award-winning process is said to enable a significant improvement in thermal impedance. Compared to standard technology, there is an increase in thermal dissipation capability from 145 W to 188 W.

The .XT technology is employed in Infineon's 2 kV SiC MOSFETs and diodes, released earlier this year to expand the variety of products that can serve in an ever expanding number of applications. The 2 kV power devices enable an increase in power density, leading to smaller units for energy storage, charging, and solar inverters. When replacing 1.7 kV products for applications operating at 1.5 kV DC, the MOSFETs combine additional headroom with a ten-fold fall in the cosmic-ray-induced failure rate and a lower on-resistance – for the MOSFET, it is either 12 mΩ or 24 mΩ, compared with 35 mΩ, 45 mΩ or 60 mΩ for the 1.7 kV range. The company has also released an isolated gate driver, which is claimed to provide the perfect match to its 2 kV MOSFET discrete and module.

Equipping chipmakers

The exceptional rate of growth in the SiC market is spurring the development of new tools and technologies to improve the manufacturing process. Speaking at CS International, Aixtron's Senior Product Manager Nicolas Müsgens spoke about the company's latest generation of MOCVD reactor for the growth of SiC layers, and Bernhard Botters, European Sales Manager at KLA, discussed his company's etching and metrology tools.

Aixtron's flagship for SiC epigrowth is the G5WW C, which can accommodate eight 150 mm wafers. Müsgens claimed that this tool offers very efficient consumption of metal-organics, and boosts throughput, thanks to the opportunity to swap wafer carriers at temperatures higher than 600 °C. Thickness uniformity for a 10 μm-thick layer on a 150 mm substrate is ± 2.26 percent, and doping uniformity of a layer with a doping level of 5×10^{15} cm^{-3} is ± 3.53 percent, which is a factor of two improvement.

Thanks to growth in the SiC industry, as well as the ramp in the production of VCSELs and interest in microLEDs, shipment of Aixtron's MOCVD tools is rising fast. To meet this demand, the German outfit has doubled its production capacity between 2020 and 2022, and plans for further expansion in the coming years.

With the SiC market growing so fast, it's easy to overlook the challenges associated with this material and ignore areas where improvement could lead to better devices, higher yields and reduced production costs. Helping to rid delegates of any complacency, Botters reminded them of the yield and reliability challenges facing SiC: this material has a much higher defect density than that for silicon; there is a high level of defect transfer from the substrate to the epilayer, and then to the device; there is a huge variation in the quality of SiC substrates produced by suppliers; there are heavy burn-in requirements; and the high cost of the starting material amplifies the cost of yield loss and excursions.

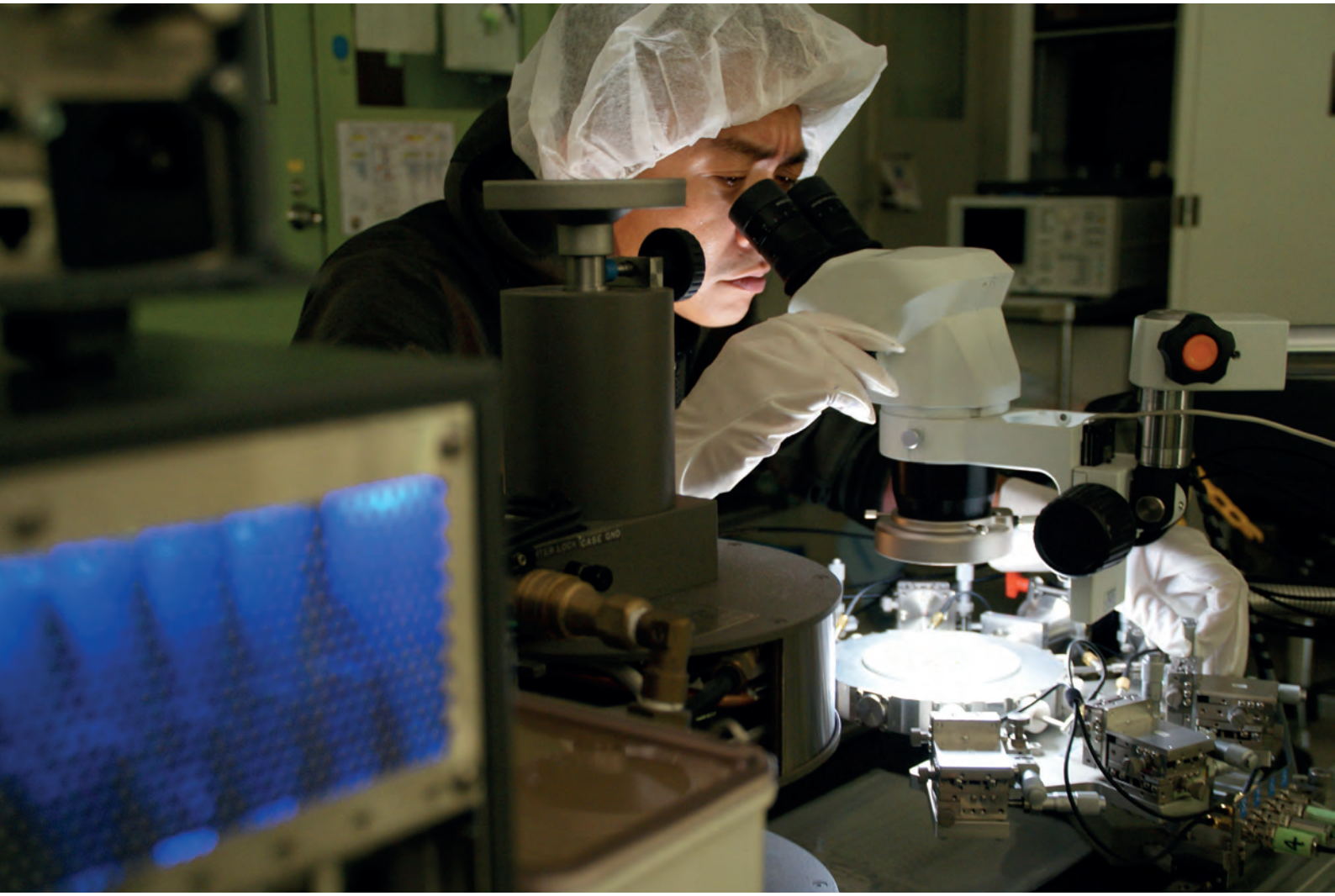
➤ Bernhard Botters, European Sales Manager at KLA, championed the company's broad portfolio of processing and metrology tools for SiC device production.

KLA has a broad portfolio of tools for processing, monitoring and measuring SiC epilayers, partly through its acquisition of the etching and dicing tool manufacturer SPTS back in 2019. According to Botters, one of the strengths of the SPTS etching process is that it enables rounded trench bases, key to the production of next-generation power devices that will not be held back by high peak electric fields, so can operate at higher voltages. He also claimed that the company's tools can provide a superior gate-oxide quality.

The SPTS tools can also be used for plasma-based wafer dicing. This approach is said to increase throughput by 75 percent, boost yield, and lower the cost-of-ownership, compared with the common alternative, blade dicing.

Within the KLA portfolio, there are also instruments for characterising defects and evaluating the mechanical properties of SiC. Using a range of technologies to detect and categorise defects, the Candela 8520 can provide incoming and outgoing quality checks, offer process control, compare the products of different vendors, and be used for tool monitoring and qualification. This instrument, which employs machine learning for multi-channel binning, draws on a large library of defects. Another tool in the portfolio is the company's Nano Indenter, which can be used to study defect propagation and optimise a process, thanks to the opportunity to measure the cracking threshold of SiC and its fracture toughness, elastic modulus, hardness and adhesion energy.

Thanks to strong support from equipment makers, the booming SiC industry is well-positioned for tremendous growth over the coming years. Stories of success are sure to feature at the next CS International, which will return to its traditional spring timeslot. Preparations are already underway for that meeting, to be held on 18 - 19 April 2023 at the Sheraton Hotel, located at Brussels airport.



Breaking new ground with the hybrid transistor

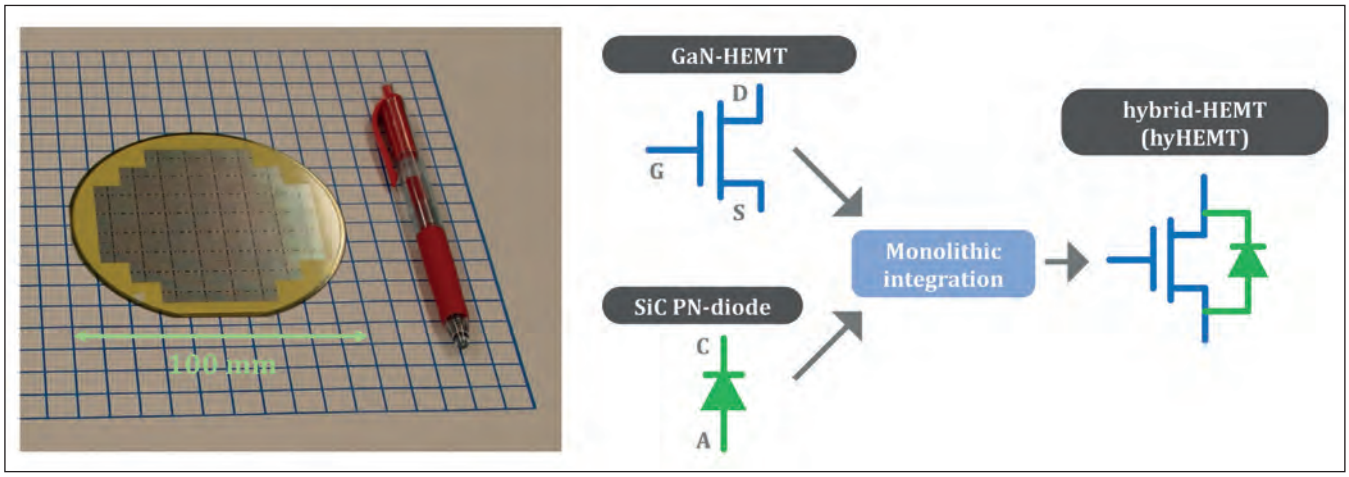
A unique integrated manufacturing process creates hybrid transistors that unite the low on-resistance of GaN HEMTs with the non-destructive breakdown of SiC diodes

BY AKIRA NAKJIMA FROM THE NATIONAL INSTITUTE OF ADVANCED INDUSTRIAL SCIENCE AND TECHNOLOGY

OUR PLANET'S TEMPERATURE is on track to rise to levels that will have horrendous consequences for humanity. Due to this, it is critical that global carbon emissions fall fast. To succeed, we must act on many fronts, including adopting new approaches to the way that energy is created, distributed and used.

If we are to move to a greener society, we will need to change the way we produce and use most of our electricity. Such efforts will have to consider the electrical power converters that step up and down the voltage and transfer it from DC to AC or vice-versa – these are the 'power bricks', extensively employed in a number of electronic applications, including the power supplies in PCs, telecommunications, electric vehicles and aerospace applications. Trim the power losses in these converters and boost their efficiency, and this will lead to energy savings at the system level.

Shifting to a low-carbon society will also require an increase in the uptake of electric vehicles, alongside the installation of far more wind turbines and solar farms. For all these green technologies, we need



power converters that are smaller, more efficient and more reliable than the incumbents. To realise this, there will have to be further technological innovation in the power transistors used in the converters.

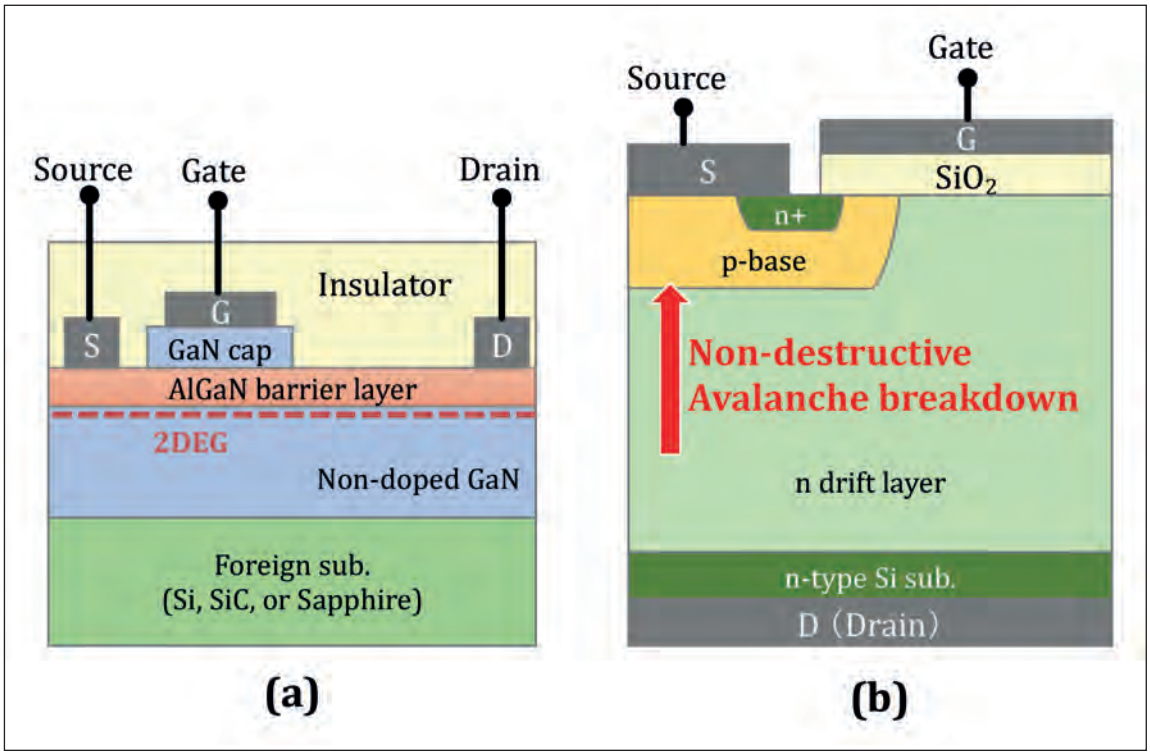
At the heart of power-conversion circuits are power transistors, performing the role of a switch. Ideally, these devices should combine a low on-resistance, to ensure a low conduction loss in the on-state, with a fast switching performance that trims switching losses.

Silicon power transistors are widely deployed in converter applications. Thanks to extensive research and development since the 1960s, their performance has improved, but now it is encroaching material limits. Thus, to deliver higher efficiencies, there's a need to turn to a different class of semiconductor.

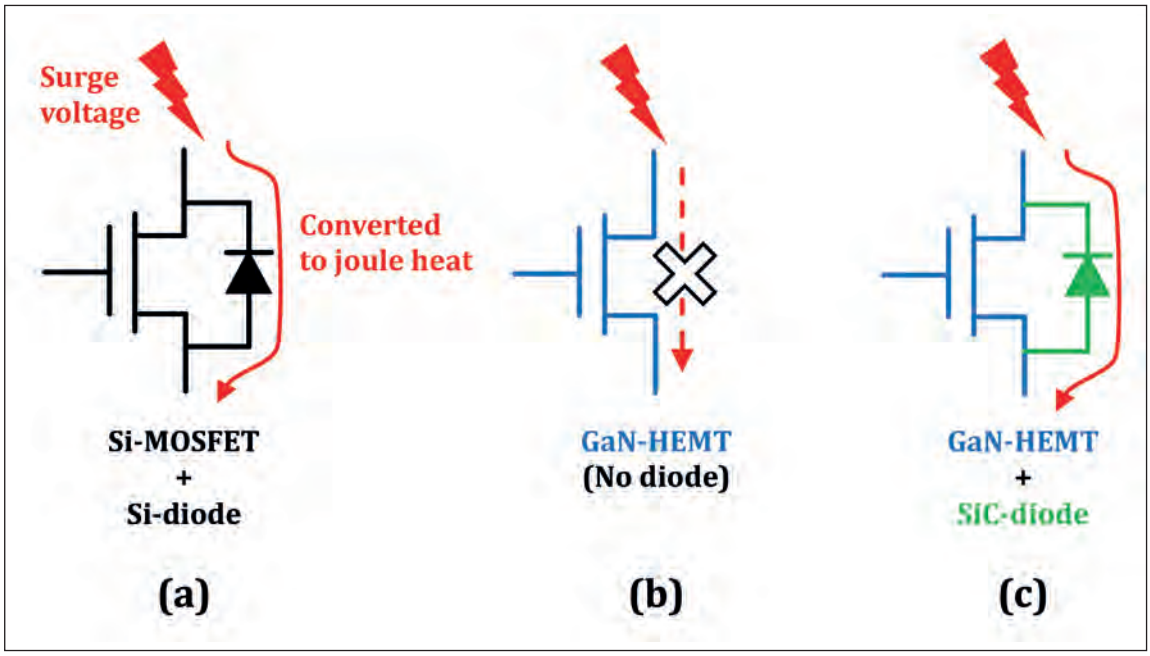
This has led to much interest in devices formed from semiconductors with a wider bandgap. One of them already enjoying commercial success is the GaN HEMT, which features a high-density, highly mobile two-dimensional electron gas (2DEG) as a channel, generated by the unique polarisation nature of the AlGaN/GaN heterointerface (see Figure 2(a)).

The mobility in this channel can exceed 1500 $cm^2 V^{-1} s^{-1}$, due to the generation of free electrons without impurity doping. Another strength of this transistor, resulting from the high electric field strength of the material, is that control of the 2DEG can be realised at a concentration as high as 10^{13} cm^{-2} – that's one order of magnitude higher than that for GaAs and silicon devices. Armed with these attributes, the GaN HEMT surpasses the silicon limit, in terms of low resistance and fast switching.

➤ Figure 1. Photograph of fabricated hybrid HEMTs on a 100 mm SiC substrate (left) and an equivalent circuit (right).



➤ Figure 2. (a) Schematic cross-section of a conventional GaN HEMT and a (b) silicon DMOSFET.



➤ Figure 3. Equivalent circuits in (a) silicon DMOSFETs, (b) GaN HEMTs and (c) hybrid HEMTs in this study.

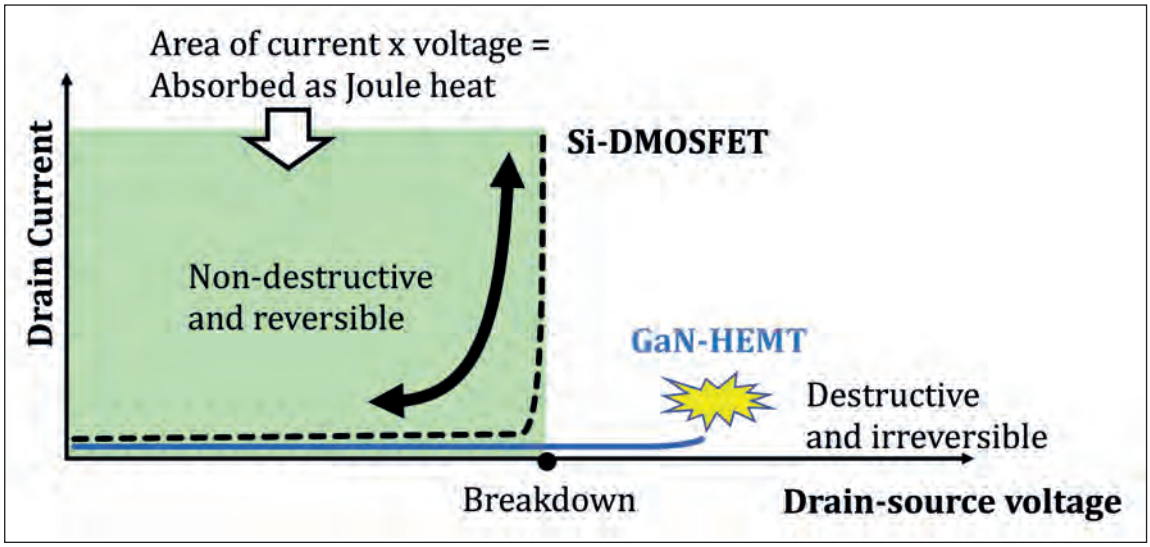
It is now many years since researchers reported the first GaN HEMTs in the 1990s. Subsequent development and commercialisation has led to their deployment in power converters of less than approximately 3 kW, such as compact AC adapters for smartphones, where they combine high efficiency with miniaturisation.

Unfortunately, GaN HEMTs suffer from reliability-related issues, hampering their deployment in high-power applications, such as electric vehicles. An impaired robustness arises from a behaviour that differs from the incumbent, the silicon double-diffusion MOSFET (see Figure 2 (b)). In this double diffusion MOSFET, there is a *p*-*n* junction between the *p*-type base region and *n*-type drift layer, as well as a *p*-*n* diode – known as the 'body diode' – that is connected in an anti-parallel configuration (the equivalent circuit is shown in Figure 3(a)). With this configuration, applying an overvoltage to the DMOSFETs under abnormal circuit operations causes the body diode to undergo a non-destructive avalanche breakdown, with the noise energy absorbed as Joule heat in the silicon chip. Due to this, when silicon power transistors are used in converter circuit topologies, they tend to prevent overvoltage during abnormal operations, thereby ensuring system reliability.

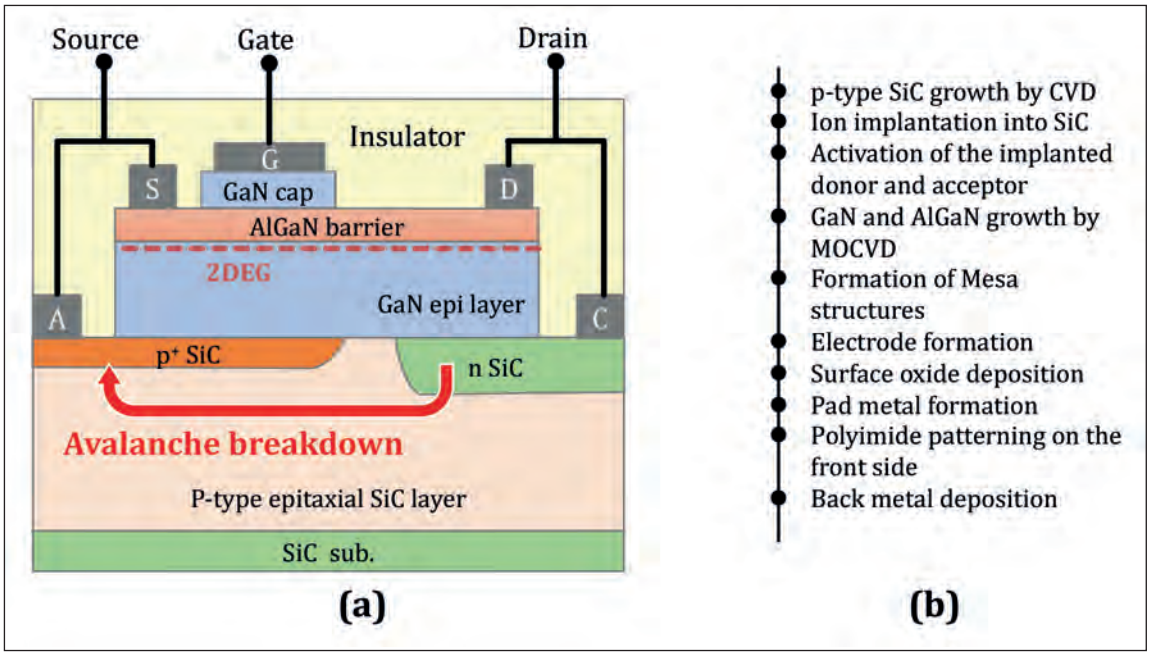
With GaN HEMTs, it's a very different state of affairs. The GaN HEMT does not have a body diode, so there is no pass for the noise energy to escape, causing this form of transistor to be destroyed by overvoltage. This weakness has limited the energy saving provided by the GaN HEMT to just low-power converters.

Uniting GaN and SiC

At the National Institute of Advanced Industrial Science and Technology our team has developed an approach to addressing this weakness, based on the introduction of a hybrid HEMT that combines



➤ Figure 4. Schematic of off-state breakdown characteristics in silicon DMOSFETs and GaN HEMTs.



➤ Figure 5. (a) Schematic of a GaN/SiC-based hybrid HEMT. Five electrodes: source (S), gate (G), and drain (D) in the HEMT; and anode (A) and cathode (C) in SiC diode. (b) Our fabrication process flow for GaN/SiC hybrid HEMTs.

GaN and SiC. This novel transistor, which solves the issue of destructive breakdown, features a SiC-based anti-parallel *p-n* diode, monolithically integrated to a GaN HEMT (see Figure 5(a)) for a diagram of this device, and Figure 3(c) for the equivalent circuit). This hybrid device has five electrodes: the source, gate and drain of the GaN HEMT structure; and the anode and cathode of the SiC diode structure.

Operated in its off-state, this hybrid can undergo non-destructive avalanche breakdown in the SiC body diode, ensuring robustness. Turn this device on and current flows through a 2DEG channel at the AlGaN/GaN interface, enabling a low on-resistance. So, thanks to these modes of operation, our hybrid HEMT combines the merits that really matter.

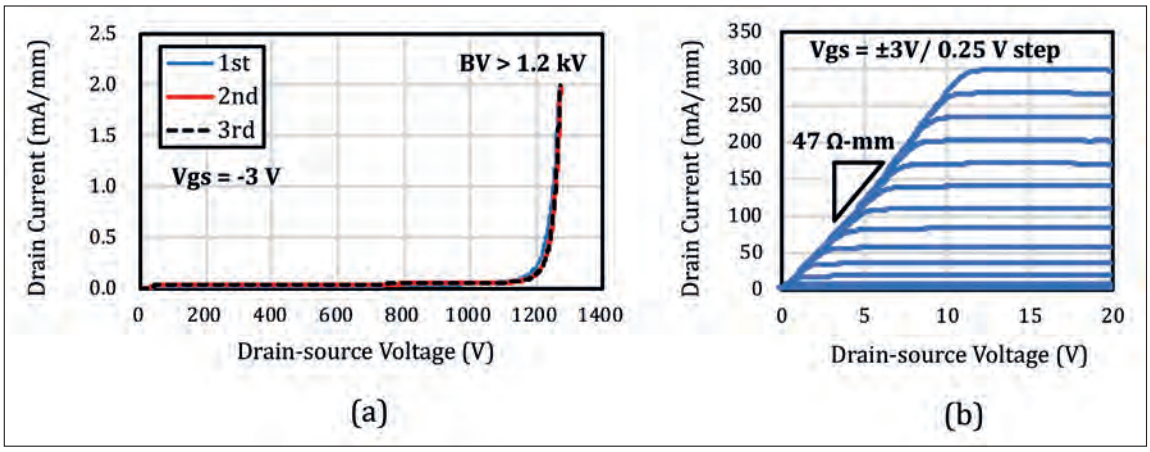
Operated in its off-state, this hybrid device can undergo non-destructive avalanche breakdown in the SiC body diode, ensuring robustness. Turn this device on and current flows through a 2DEG channel at the AlGaN/GaN interface, enabling a low on-resistance

To produce our novel devices, we expanded a 100 mm SiC-based prototyping line, located at an open innovation facility in Tsukuba, Japan. Our changes created a prototyping line for fabricating SiC, GaN and hybrid devices. With these modifications, we have been able to fabricate hybrid HEMTs that are small in size and have a gate width of 50 μm.

The steps we take to make our devices (summarised in Figure 5(b)) begin with the growth of *p*-type SiC via CVD. After this, we form *p*-type and *n*-type SiC regions by ion implantation and activation, before growing HEMT layers by MOCVD and defining the mesa structures by dry etching. Electrodes are then added, followed by deposition of a 3 μm-thick aluminium layer that provides the pad metal. Our final steps involve covering the surface with a polyimide and depositing a nickel-based alloy on the backside of the device.

Electrical measurements on our hybrid HEMT produce promising results. Unlike typical GaN HEMTs, they are not destroyed immediately after a breakdown, but undergo a non-destructive avalanche breakdown in the SiC diode – this is accomplished by designing the breakdown voltage of the SiC side to be slightly lower than that of the GaN side. The breakdown behaviour, associated with a breakdown voltage of about 1.2 kV, is shown in Figure 6(a). As the avalanche breakdown is non-destructive, our device offers a stable reversible breakdown during multiple sweeps. Operating under forward bias, our hybrid HEMT produces a drain current as high as 300 mA/mm and an on-resistance of just 47 Ω mm, thanks to current flow through a high-mobility 2DEG (see Figure 6(b)).

In addition to the low on-resistance and the non-destructive breakdown, our hybrid transistor offers excellent heat-dissipation characteristics. This



➤ Figure 6. (a) Measured off-state breakdown of the fabricated hybrid HEMT. Repetitive current-voltage (I-V) sweep curves up to 2 mA/mm show high stability against avalanche current stress. (b) On-state characteristics. Owing to current flow via the low-resistance 2DEG, a low on-resistance of 47 Ω-mm and high saturation current of 300 mA/mm were measured.

particular attribute comes from the excellent thermal conductivity of SiC, which is three times that of silicon.

Other marriages

Our hybrid HEMT has great potential, combining excellent traits under forward and reverse bias with excellent thermal management. These are very encouraging signs for a device that is still in its infancy, with much opportunity lying ahead for optimisation of the device structure and its fabrication process. Our next steps will be directed at demonstrating large-area devices, rated at 10 A or more, that can be used in actual power converters. We will also devote much effort to trying to commercialise this technology, by engaging with companies that have technical expertise in power devices.

Our work forms part of a global effort at developing power devices from materials with a much wider bandgap than silicon. SiC and GaN devices are now commercialised, while those with an even larger bandgap, such as the promising trio of Ga_2O_3, AlN and diamond, are attracting much attention. Of those three, diamond has the potential to be the ultimate semiconductor, due to its extremely high field strength and its superior thermal conductivity. However, heterogeneous integration of different semiconductors may offer new, unconventional opportunities.

Our hybrid HEMT highlights how integration can deliver performances not possible with a single material. There are numerous combinations to explore, opening the door to novel device concepts. We are aiming to investigate what may be possible with this approach, and how it could unleash a new generation of power devices.

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Branching out to gallium oxide

Bristol University academic Martin Kuball is expanding his areas of expertise from the analysis of wide bandgap devices to the growth and production of gallium oxide transistors

INTERVIEW BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

RS: *What excites you about gallium oxide, compared with the more common compounds for making power devices, silicon carbide and gallium nitride?*

MK: Gallium oxide has a greater bandgap and can be made quite cheaply. Researchers have already produced 4-inch to 6-inch gallium oxide substrates and grown on them. This opens a huge opportunity for this ultrawide band gap material to enable high-performance, low-cost power electronics. Devices could operate even in excess of 10-12 kilovolts; or maybe compete against silicon carbide in the 1-2 kilovolt range, with a little less performance, but greatly cheaper.

Maybe gallium oxide will also get more young people into semiconductors. This is an exciting field for careers. I was at a conference last week, and a lot of people asked me: Do you have people who could work for us in our semiconductor company?

RS: *Over many years, you and your team have provided great insight into the thermal management of wide bandgap devices, using techniques such as*

micro-Raman spectroscopy. These investigations have involved analysing devices provided by other groups. Rather than continuing this approach with gallium oxide, you've installed an MOCVD tool so you can make your own devices. What prompted you to move into growth when branching out into gallium oxide?

MK: When I came from Brown University to Bristol University in 1997 I started with optical spectroscopy. From this I built very strong expertise in the thermal management of devices. I worked at that time with QinetiQ, with TriQuint, which is now Qorvo, and with many other suppliers. We developed ways to measure the thermal characteristics of devices, such as the device temperature with a very high spatial resolution. From there we expanded into other techniques, such as how to measure the thermal conductivity of materials, and we spun out TherMap Solutions. For our next step, we built strong expertise in electrical characterization, device reliability and the design of devices.

Since it's at a very early level of development, gallium oxide device and material availability is limited. We have great collaborations with people in the US, in Japan and in Germany, but having growth directly here opens huge opportunities to fully benefit from our device expertise. We can grow the material structures we want with specific dopants, fabricate devices and analyse them. We can understand from the growth side what we need for the device side and vice versa, so we have this great interlinking of knowledge.

We will continue working with the people in the US, Germany, Japan, and other places who we worked with before. But we will also make new links, when we grow material and when we make devices. We're more than happy collaborating with people, because we want to help accelerate gallium oxide.

RS: *What facilities do you have for processing epitaxial materials into devices?*

MK: We have a sizeable cleanroom. It's in the same building, on the level underneath the MOCVD system. The cleanroom has all the necessary tools for photolithography. We have e-beam lithography, we have etching tools, and we have ALD for depositing oxides, and so on, so we do full device processing at Bristol University.

RS: *Gallium oxide can be grown by a variety of techniques, such as MBE, HVPE and mist-epitaxy. Why are you pursuing MOCVD?*

MK: To take full advantage of gallium oxide's properties, you need vertical devices, to push the breakdown voltages as high as you can. MBE is a very slow growth technique. We have lateral devices made by MBE, but our main focus is actually on vertical devices.

HVPE is the optimum technique to make very thick layers. It is a very fast growth technique, but you tend to have more impurities, at least in the nitrides – the oxides probably still need to be looked at.

With MOCVD, we have very good control of impurities and the possibility to make very sharp

➤ Earlier this year, Martin Kuball's group at the University of Bristol, UK, installed an Agnitron MOCVD reactor for the growth of gallium oxide and related materials.

interfaces. We're going to look at heterogenous integration of gallium oxide with other materials. This was a reason for doing MOCVD.

RS: *What considerations must be made when deciding to install an MOCVD reactor for gallium oxide growth?*

MK: Installation is quite easy to do. You don't need expensive scrubbers, as you would have on a gallium nitride system, for example, as the output is not that toxic.

To grow clean materials, you need to have very clean gas lines. Our installation involved a great team of local engineers and hired external contractors. Our pipework is designed to fulfil the highest specifications we need for growing very high-quality layers of gallium oxide and aluminium gallium oxide.

RS: *Did you consider building your own reactor?*

MK: We could have spent a few years building our own system, but I'm more interested in getting to the device side. It is much better for us to work with people who have spent a lot of time designing a good gallium oxide growth system. We worked with Agnitron. They have done a lot of prior research and investment, and have a very good track record in commercial gallium oxide MOCVD systems.

RS: *How easy is it to source substrates for the epitaxy of gallium oxide?*

MK: It's quite easy. We buy from a commercial supplier, NCT in Japan, and work with other suppliers. There's an emerging activity from Northrup Synoptics, and there are other upcoming suppliers.

➤ During 25 years at Bristol University, Martin Kuball (far right) has built up a team focusing on wide bandgap technologies that now numbers around 20 researchers. Key members of the team involved in gallium oxide growth are post-doctoral research fellow Indraneel Sanyal (centre) and PhD student Arpit Nandi (left).

RS: *What's going to be the first type of device you make?*

MK: The first devices will be lateral devices. They will be test structures, to understand the growth, to understand the interfaces, to understand trap densities and see what breakdown voltages we can get. The second type of device will be trench Schottky barrier diodes and FET devices, vertical devices.

We will first reproduce what other people have done, just seeing where we stand compared to published data.

The third generation will be the integration of gallium oxide with other materials to engineer some issues out, such as the low thermal conductivity of gallium oxide and its lack of workable *p*-doping.

This is a current plan. I'm pretty certain we will revise this plan as we go along to maximise the device performance, including reliability.

The ultimate goal would be a 10-12 kilovolt device. We will start aiming at 1, 2, 3 kilovolt devices and work ourselves upwards. We'll also make comparison against silicon carbide technology.

There's so little known about the reliability of gallium oxide devices, so we will definitely look at that side, with our track record in device reliability. We will look at how you optimise surfaces and how you optimise materials to minimise trap states. We will find ways to make optimal heat sinking.

The roadmap will say 'let's aim for a 12-kilovolt device', but there will be many, many steps in between.

RS: *You're also doing some growth on sapphire, aren't you?*

MK: Yes. Sapphire is naturally easy to source. This is a low-cost substrate.

We also have the intention to grow on other substrates. Recently, from the simulation perspective, we showed the benefits of integrating *n*-type gallium oxide with *p*-type diamond. There's a lot of other substrate materials we will look at in this context. Gallium oxide has a low thermal conductivity, it cannot easily be doped *p*-type; but even if you can dope it *p*-type, the valence bands are very flat, so you get hole trapping.

We've done a lot of gallium-nitride-on-diamond integration. That was mainly for RF devices; these will always generate a lot of heat. 20, 30, 40 percent of the power is going to be exiting as heat. But

we're looking here mainly at power devices. A good power device mainly generates heat at the point when you switch the device. So, in the optimal case, in the off-state there is no current flow; and in the on-state, the resistance is very small. So you won't actually have a lot of heat generation. When you switch it, you will have a voltage and current flow, so during the switching state you generate heat. The heat generation is much less than in an RF device and thermal management is less critical. But if you really push the Ampere rating of the device, you have to worry about that.

RS: *You're planning to make some heterostructures that combine gallium oxide with aluminium gallium oxide. Where might that lead?*

MK: There's very beautiful work by a group in Ohio, who looked at heterostructures and showed that you can get nice mobilities at interfaces. We will look into this. There's also work on multi-channel devices, and we will look at aspects of this.

There's also just the point of curiosity: how can you change material properties, if you do superlattices? How can you increase the potential of gallium oxide?

RS: *Is it easy to apply the techniques you developed to look at the thermal management of devices made from gallium nitride and silicon carbide to those made from gallium oxide?*

MK: Historically, we developed a lot of device and materials characterization techniques. Many of them focused on gallium nitride. All are applicable to gallium oxide, and we will use them – the thermal management characterization, Raman thermography; and transient thermoreflectance.

We recently developed a technique to map electric fields in gallium nitride devices, based on second-harmonic generation. We published an account of this in *Nature Electronics*, and we have an additional paper just accepted in *Applied Physics Letters*. A few smaller things will need to be modified in the setup for gallium oxide, but it's an exciting opportunity to, for example, optimise edge termination in gallium oxide devices.

The whole electrical characterization suite we have developed will naturally also apply to gallium oxide, from DLTS-style methods to look at trap states to dynamic R-on, pulse and double pulse IVs, as well as reliability assessments. They are easy to apply. It doesn't need much change.

RS: *As well as leading a large and expanding research group, you've taken a very active role in conferences. In 2019 you organised Diamond D Day, a one-day conference attracting 120 delegates, half from overseas. You have just come back to CS Mantech, where you held the role of technical programme chair. Obviously, in your mind, conferences are an important part of driving research?*

We recently developed a technique to map electric fields in gallium nitride devices, based on second-harmonic generation. We published an account of this in *Nature Electronics*, and we have an additional paper just accepted in *Applied Physics Letters*. A few smaller things will need to be modified in the setup for gallium oxide, but it's an exciting opportunity

MK: Conferences are an important part of bringing people together to discuss and move research forward, first presenting the latest data and then discussing it, brainstorming ways forward and getting new ideas.

A few years ago we ran *Diamond D Day* in Bristol. Covid has prevented us running this again. But I'm certain in a year or two we may run a *Diamond D Day Two*, on the integration of diamond with gallium nitride and other semiconductors, such as gallium oxide.

In different roles, I've been involved in *CS Mantech* for probably the last ten years. I was technical programme chair of the conference this year in Monterey, California. This conference brings a lot of industry together. From the attendees, it's probably 70, 80 percent from industry; and 20 percent students, faculty. It's very interactive, very positive, with lots of brainstorming, and this is extremely important.

Next year *CS Mantech* will be in Orlando. I will be overall chair, and I will push for more ultra-wide bandgap materials and devices in this conference. This year, I believe we had two, three or four talks on gallium oxide at *CS Mantech*.

RS: *Do you think that conferences that cover compound semiconductor technologies are well suited to helping those in academia and industry interact? Or are there are some barriers that need to be broken down?*

MK: There can be barriers. Some industries may be reluctant to work with academia for different reasons, for example, IP. Academia may be sceptical working with industry because the project may be too short term. Collaborations must find a sweet spot of interactions.

I have worked with industry probably since the day I started in Bristol, 25 years ago. Conferences are a useful tool to initiate that. *CS Mantech* has been very good in my own personal career, establishing links with industry. Some of my current industrial interactions go back to discussions I have had with companies at *CS Mantech*. This year I had very useful conversations with three, four, maybe five companies; this hopefully leads to interaction.

You'll find a good array of conferences. Some have a larger industry participation, like *CS Mantech*; and some, like *IWN* and *ICNS*, have less industry interaction. You need that balance, where in some cases you do blue sky research and maybe don't interact with industry. But still industry can listen to that. Maybe that doesn't lead to interaction – that's fine.

RS: *One of the motivations for developing and producing wide bandgap power electronics is to save energy and try and reduce carbon footprints, while many international conferences involve a lot of flying. Do you see that as a conflict? And what do you think lockdowns associated with Covid have taught us about pros and cons of online gatherings?*

MK: It's always a challenge to go to a conference developing carbon-emission-reducing technologies and having to fly. Conferences are important for face-to-face discussions. They can't replace Zoom or Teams meetings. On the other hand, not everything has to be done flying around the planet.

Covid had a lot of negative impact on people, personally, and on business and the economy. We're hopefully slowly moving to a point past Covid, where we can naturally return to conferences where people are present, such as *CS Mantech* this year. But equally, we must take advantage of all the online tools developed during the last two years. When Covid started, they were not as good as they are now. They have improved a lot.

Yesterday I had a meeting with people in the US. This brought six-to-seven people together for an online meeting. It was a perfect information exchange, brainstorming how we can collaborate together. I didn't need to do this as face-to-face, flying over.

Having a combination of conferences, but also taking advantage of the online tools, will hopefully reduce the amount of flights and travel people do, but equally provide an even better outcome. With this approach, I can actually talk to more people. I can talk to someone in Japan in the morning, and someone in the US in the afternoon. We should take this as the positive side from the Covid evolution, making use of the online tools developed.

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Progressing the photonic-crystal surface-emitting lasers

Thanks to a number of advances, photonic-crystal surface-emitting lasers (PCSELs) now combine a high output power with great beam quality, polarization, beam-pattern control and on-chip two-dimensional beam scanning

BY SUSUMU NODA FROM KYOTO UNIVERSITY

SEMICONDUCTOR LASERS continue to make important contributions to our society. They are deployed for many tasks and have made significant and lasting contributions to communication networks and optical storage. In these settings, much effort has been devoted to expanding the utility of this source by widening its range of emission wavelengths and increasing its modulation speed.

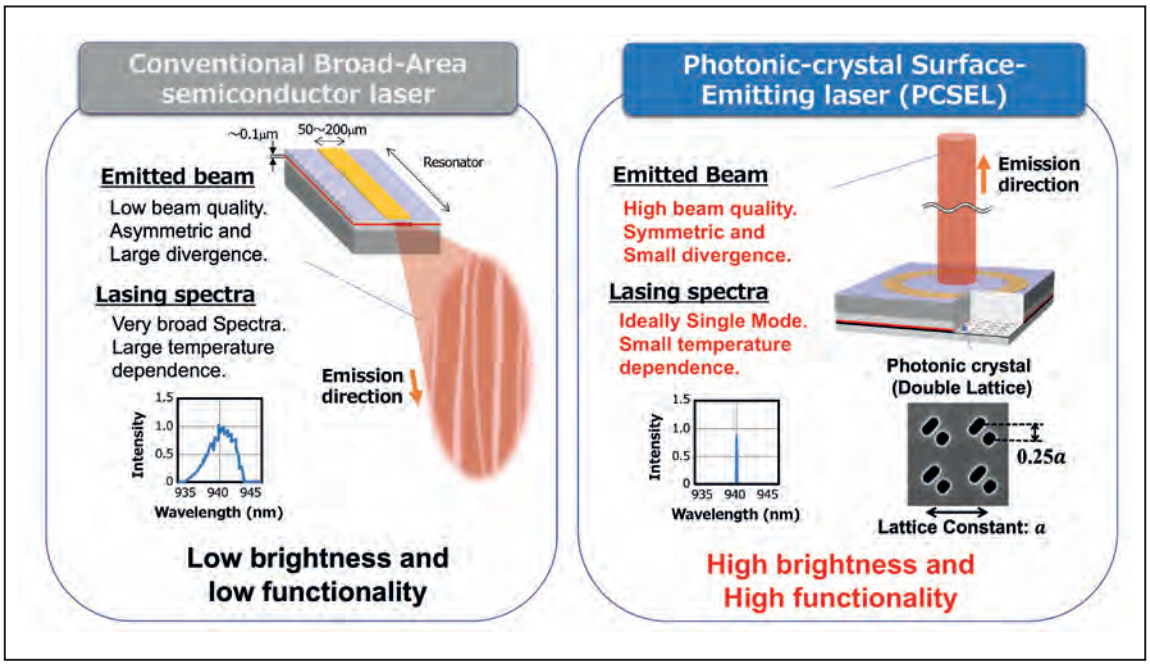
There are also opportunities for lasers in Smart Mobility and Smart Manufacturing. However, conventional lasers that are designed for these tasks produce a very broad spectral emission and struggle to meet the high output powers and high beam qualities that are required (see Figure 1 left).

Like many other classes of laser, those made from semiconductors have additional areas for improvement. Today's chips are incapable of providing an on-chip beam pattern, polarization and direction control. Failing to offer these functionalities is a significant weakness – these omissions have to be addressed with external elements, and this forfeits the advantage of compactness, for which semiconductor lasers are renowned.

Fortunately, this paradigm can change, thanks to the development of the PCSEL, an acronym for the photonic-crystal surface-emitting laser (see Figure 1 right). This device is currently attracting much attention, because it can realise simultaneously a high output power and a high beam quality, and offer functionalities that are not easily achievable with other types of laser, such as polarization and beam-pattern control, as well as on-chip beam-direction control, which eliminates the need for bulky external optics.

The remainder of this feature offers a brief overview of the history of the PCSEL, along with an account of recent progress, including success associated with newly developed photonic crystals.

➤ Top: PCSELs are expected to make a paradigm shift for Smart Mobility and Smart Manufacturing

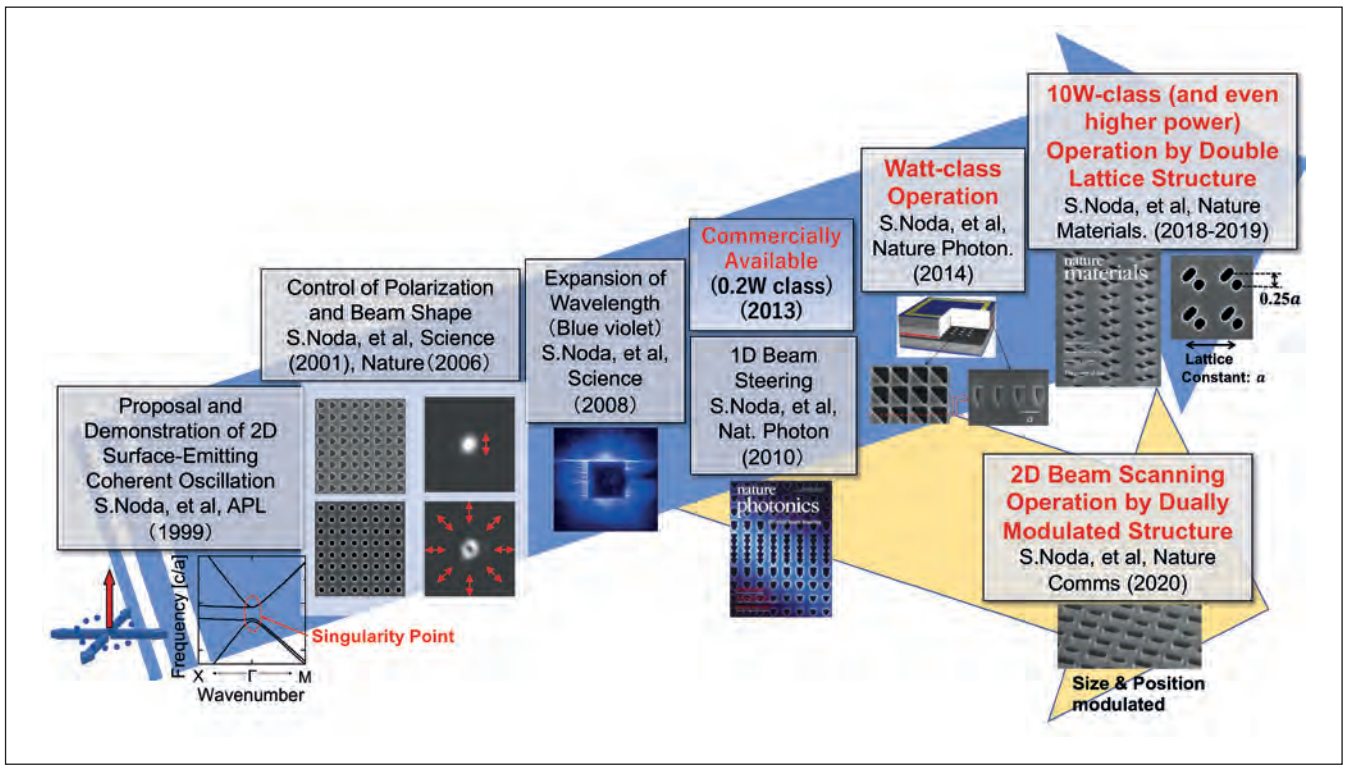


➤ Figure 1. Comparison of conventional broad-area semiconductor laser and a PCSEL.

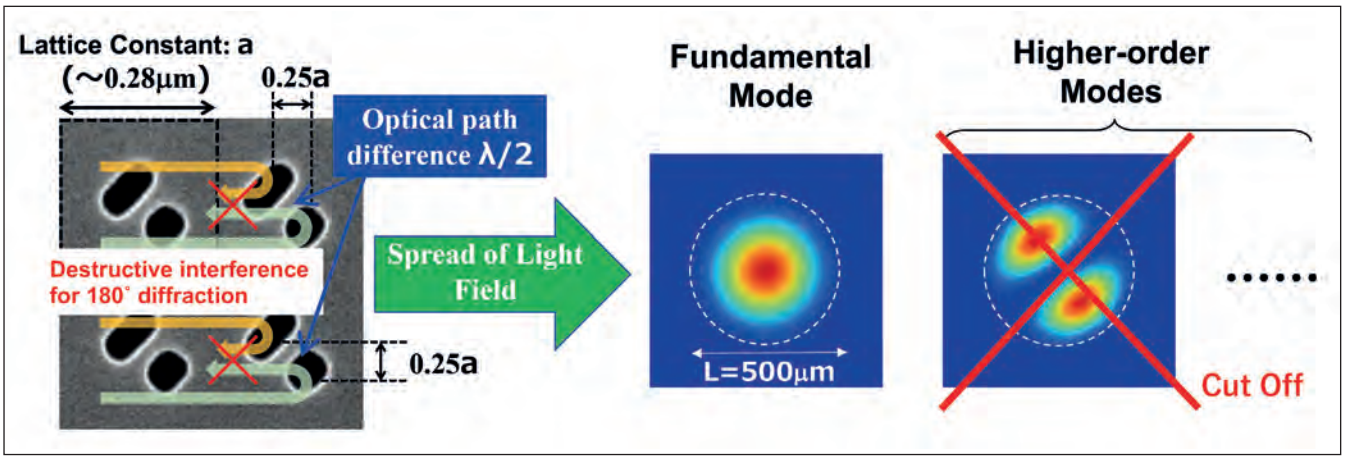
The PCSEL's past

Our team from Kyoto University proposed and demonstrated the concept of the PCSEL back in 1999. The key characteristics of this class of laser are its operation at a singularity point (Γ) of two-dimensional (2D) photonic crystal, which has a lattice formed from two types of materials with a large refractive index contrast, such as air and a semiconductor. In this high-contrast lattice – it could be square, triangular, or of another form – there is coupling of fundamental (first-order) Bloch waves and higher-order Bloch waves. Due to this interaction, the PCSEL is capable of a broad-area 2D coherent lasing oscillation. The nature of the Γ point ensures that emission comes from the surface of the photonic crystal; it is for this very reason that we named this laser the PCSEL.

It is worth noting that the PCSEL is different from the 2D distributed feedback laser. As the latter has a smaller refractive index contrast, due to alternating layers of differing semiconductor materials, coupling is only between fundamental waves. Due to this limitation, there is no coherent 2D resonance of the transverse-electric modes in square-lattice



➤ Figure 2. Progress of PCSELs.



➤ Figure 3. Impact of double-lattice photonic crystals.

structures. For this reason, it is difficult for an 'all-semiconductor' PCSEL to realise coherent operation over a 2D broad area.

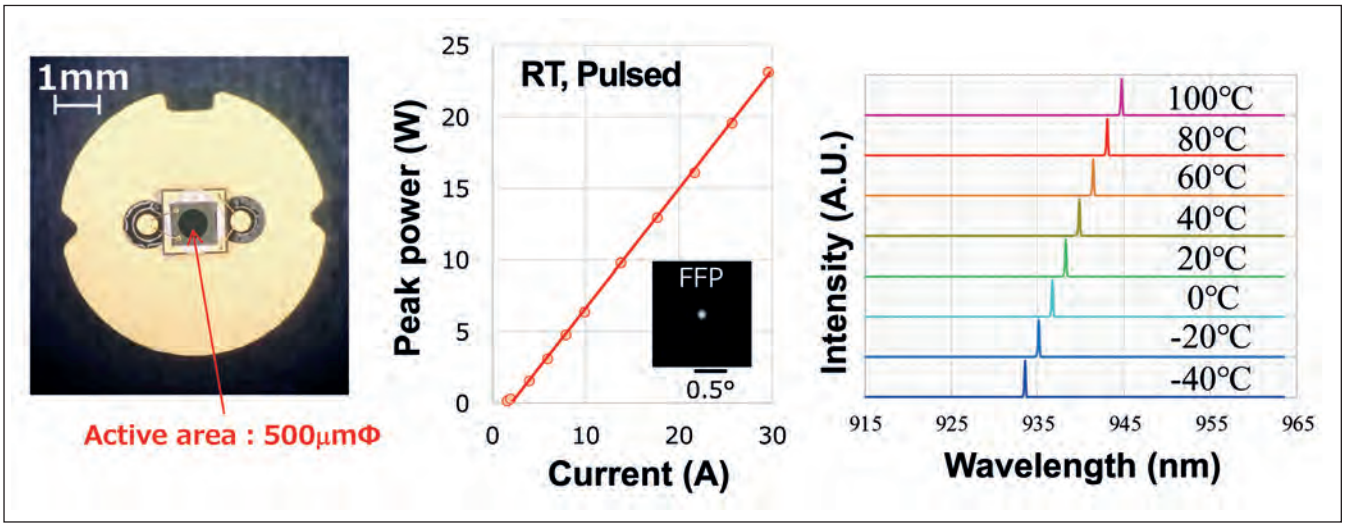
Following our initial demonstration of the PCSEL at the end of the last century, we have kicked on to develop its basic operating principles and a number of new functionalities. We reported our realisation of polarization mode control in 2001; the development of beam pattern control in 2006; our introduction of blue-violet wavelength emission, using GaN materials, in 2008; one-dimensional beam steering in 2010; and watt-class operation with a high beam quality in 2014. As well as the triumphs in the lab, a 0.2 W class device that's based on these photonic crystals has been commercially available since 2013 (see Figure 2 for a timeline of success).

In addition to all this success, recently we have enjoyed further breakthroughs, which have come from optimising the photonic crystal structure. In 2018-2019, we unveiled a unique photonic crystal structure that we call a 'double-lattice photonic crystal'. This architecture ensures a high beam quality and can realise a PCSEL output power of 10 W or more. We have also introduced, in 2020, a 'dually modulated photonic crystal' PCSEL. Its hallmark is to provide two-dimensional control of beam diffraction while simultaneously preserving two-dimensional resonance.

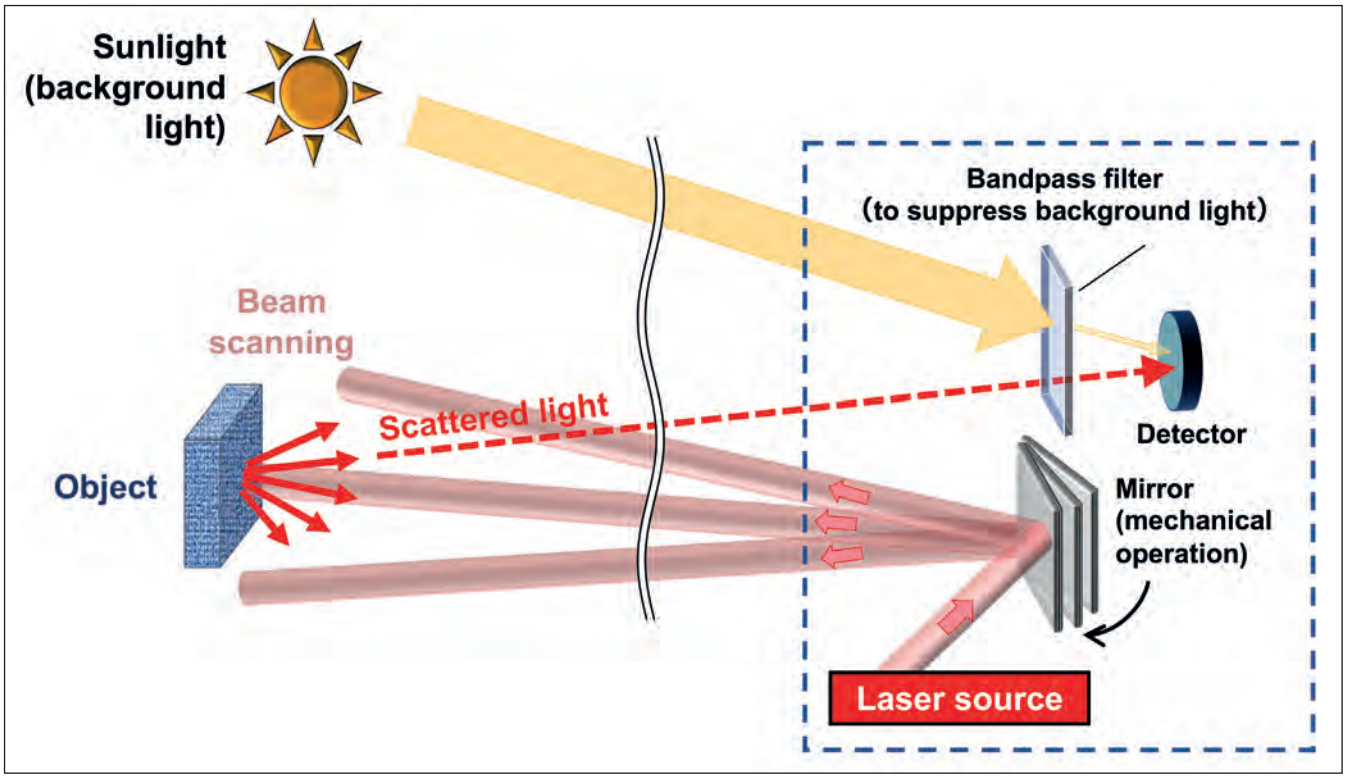
Boosting brightness

The merits of high power and high-beam-quality associated with the PCSEL come together to ensure high brightness. This characteristic is defined as the optical power, per unit area, per unit solid angle; this metric provides a figure-of-merit for how intensely a laser beam can be focused, and how narrowly an emitted laser beam diverges.

Brightness is proportional to the size of the device, and inversely proportional to the product of lateral modes in orthogonal directions. In conventional broad-area semiconductor lasers, the well-trodden path to realising a higher output power is to increase the size of the device, but this comes at the expense of an increase in the number of lateral modes. Consequently, this approach fails to boost brightness. It's a similar story with the VCSEL, but not with the PCSEL, because with this particular



➤ Figure 4. (Left) PCSEL mounted on 5.6 mm-diameter package, (middle) I-L characteristic (inset shows the far-field pattern (FFP)), and (right) temperature dependence of lasing spectra.



laser it is possible to have very few lateral modes – ideally, they can be single – while increasing the size of this device (see Figure 1 right, again). Thanks to this asset, PCSELs are expected to operate with a brightness of 1-10 GW cm^{-2} sr^{-1}, a level of performance associated with large lasers, such as CO_2 lasers and fibre lasers. What's more, PCSELs have the potential to produce a lasing spectrum that is very narrow, and ideally single mode, as well as a temperature dependence that is far smaller than that of conventional, broad-area semiconductor lasers.

To increase the brightness of our PCSEL, we have introduced a double-lattice photonic crystal. This consists of two square lattices with larger and smaller lattice points, whose positions are shifted by around one-quarter of the lattice constant. This design ensures that light waves are diffracted by individual lattices with an optical-path difference of half-a-wavelength. Due to this, destructive interference occurs for 180° diffraction, leading to a spreading of the light field (see Figure 3). As the antinode of the higher-order mode is close to the edge of the device, the higher-order mode is cut off, leading to a high beam quality and ultimately a high brightness.

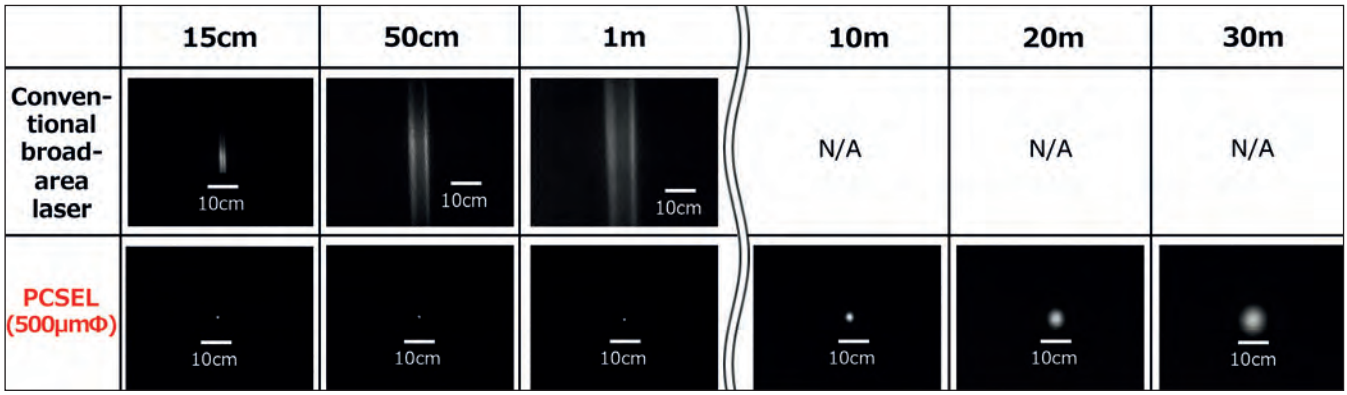
We have fabricated a PCSEL with a double-lattice photonic crystal, mounting this chip on a package in an up-side down configuration, with the output beam emitted from the substrate side (see Figure 4, left). Measurements reveal that when operating in pulsed mode, this source produces an optical output of more than 20 W at a slope efficiency of 0.83 W/A. Thanks to a very narrow beam divergence of 0.1°, brightness exceeds 1.5 GW cm^{-2} sr^{-1}. As well as these great characteristics, our PCSEL with the double-lattice operates stably in a single mode from -40°C to 100°C, and has a temperature dependence of just 0.08 nm/°C. If a higher slope efficiency is needed, PCSELs can be combined in series. By configuring a three-element array in this manner, we have increased the slope efficiency to more than 2.3 W/A.

One of the emerging opportunities for high-brightness PCSELs is in lidar, a technology needed for Smart Mobility of cars and robots (see Figure 5). To highlight the capability of a PCSEL for these applications we have provided a proof-of-concept demonstration, where this source lies at the heart of a compact, simplified time-of-flight lidar system.

Our evaluation of this system began by considering how small its beam diameter can be maintained when the emitted beam propagates in free space without the assistance of any external lens system. We projected the beam on a screen

➤ Figure 5. A typical lidar system (time-of-flight (ToF) type).

To increase the brightness of our PCSEL, we have introduced a double-lattice photonic crystal. This consists of two square lattices with larger and smaller lattice points, whose positions are shifted by around one-quarter of the lattice constant



➤ Figure 6. Comparison of a far-field beam propagation of a conventional semiconductor laser and a PCSEL.

placed at distances varying from 15 cm to 30 m, and compared our findings with those for a conventional broad-area laser (see Figure 6).

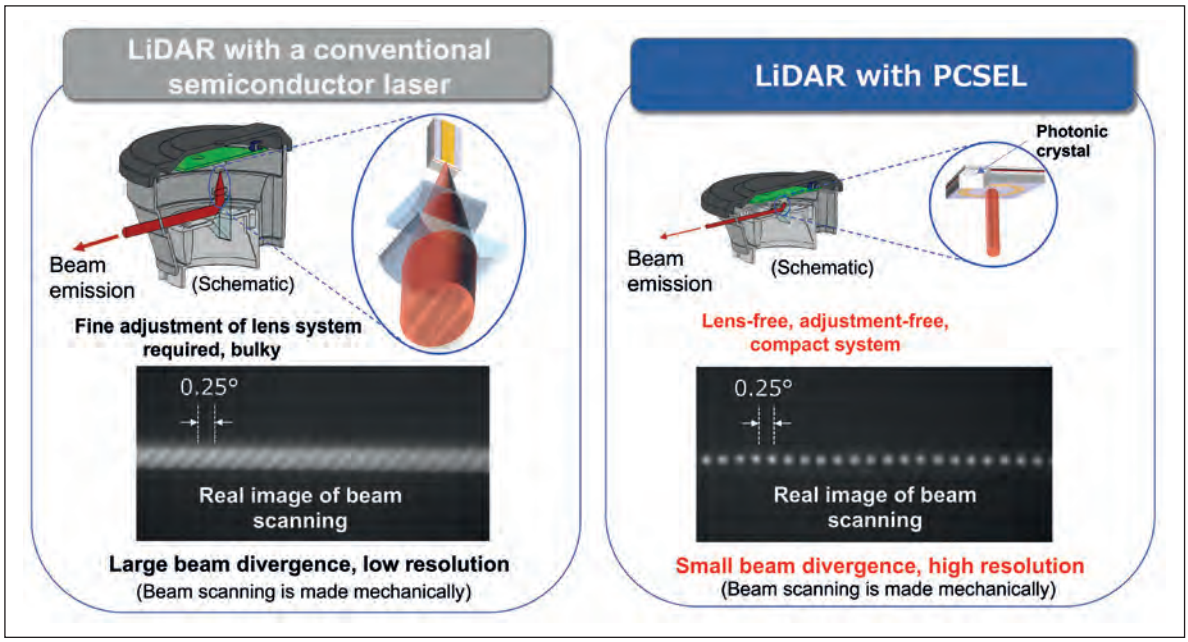
As one would expect, the beam from the conventional broad-area laser spreads out quickly, because its divergence angles are large and asymmetric. Due to this limitation, we could not discern the beam's pattern after it had travelled beyond 1 m. In lidar systems this weakness is addressed by employing an external, complicated lens arrangement alongside conventional lasers. However, this solution adds complexity and increases the size of this unit.

It's a markedly different situation with a PCSEL-based lidar. Thanks to far smaller divergence angles, the beam diameter is far smaller, even at distances far from the laser. Remarkably, even at 30 m, the diameter of the circular beam is below 5 cm, in terms of its full-width at half-maximum. This promising result indicates that when a PCSEL is used in a lidar system, it does not require an external lens system and its associated complicated adjustment process. This can cut the cost, weight and size of a lidar system.

Encouraged by our findings, we have gone on to develop lidar systems that incorporate our PCSELs (see Figure 7 for a comparison with a lidar system featuring a conventional laser). In these systems, laser beams are scanned in one dimension by mechanically rotating a mirror. Attempting this with a lidar featuring a conventional laser is hampered by a large, distorted beam spot, even after a complicated system of lenses is employed to reshape the beam. Due to distortions in that system, beam spots overlap during beam scanning, lowering the system's spatial resolution. In sharp contrast, our PCSEL-based lidar provides clearly separated beam spots during beam scanning, and ultimately a high spatial resolution.

Using a PCSEL-based lidar system that we built in 2020, we have undertaken distance measurements in real time (see Figure 8). This system captures fine details of the motion of Persons A and B, such as the movement of their hands, illustrating the superiority of a PCSEL-based light source. In 2021 we built on this success, slashing the volume of a PCSEL-based lidar by a factor of three (see Figure 9).

High-brightness PCSELs are not limited to pulsed operation. We have also produced continuous-wave



➤ Figure 7. Comparison of a conventional semiconductor laser and PCSEL light sources for lidar.

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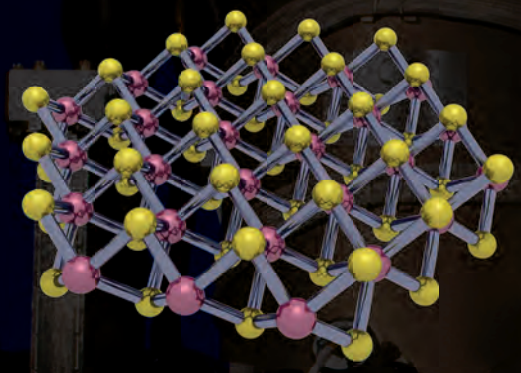

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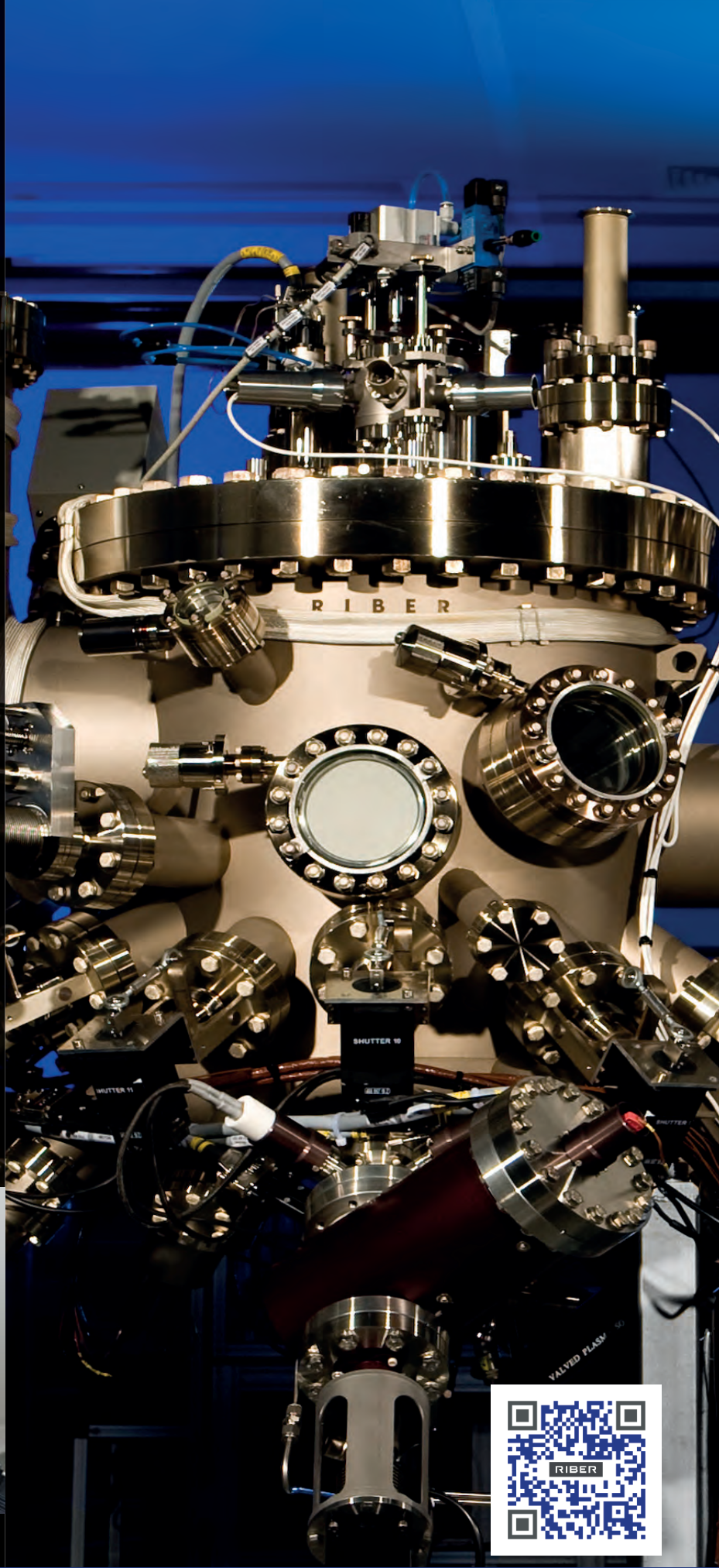

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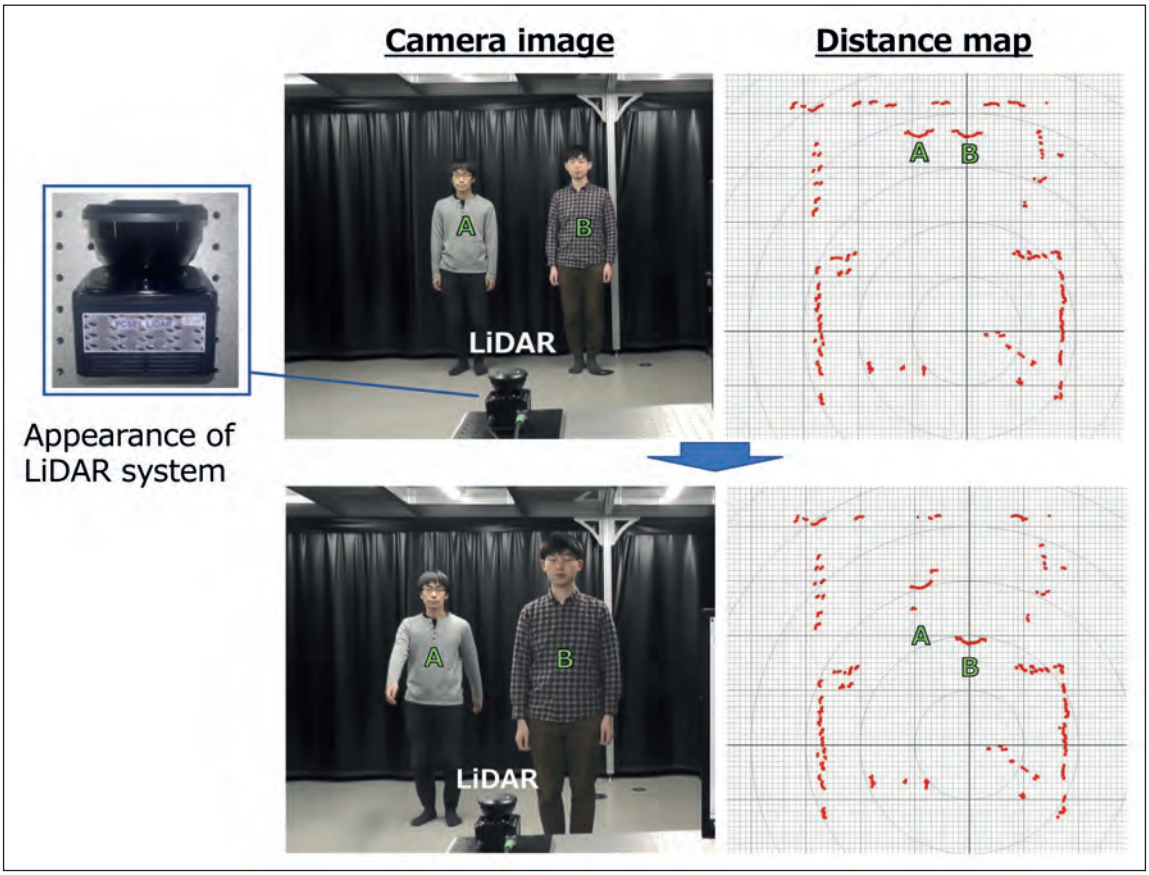
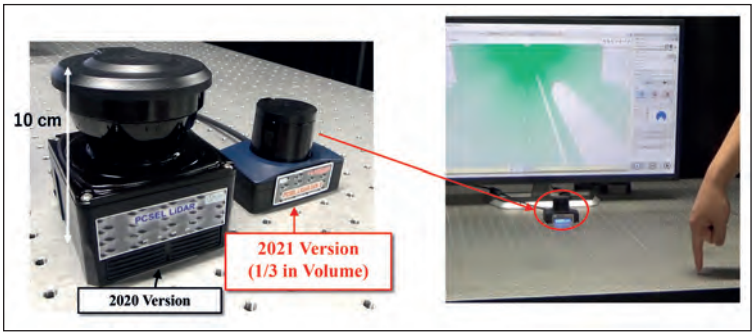
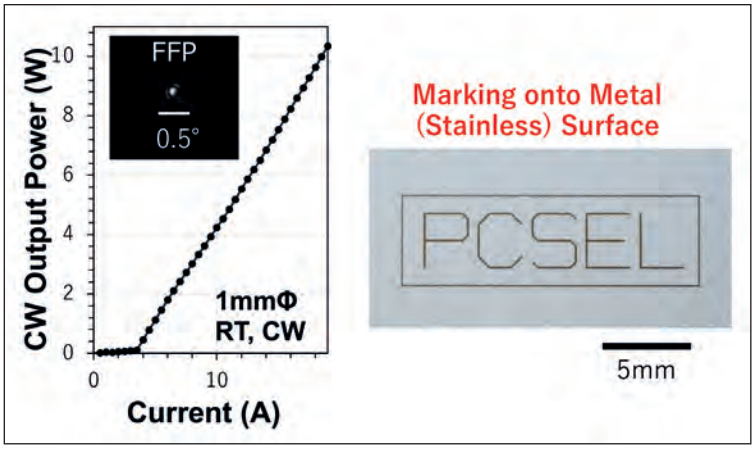


➤ Figure 8. Demonstration of lidar with a PCSEL light source.



➤ Figure 9. Further miniaturization of a lidar system. The 2021 version is just one-third of the volume of its predecessor from 2020.



➤ Figure 10. (Left) CW operation of PCSEL with a size of 1mm in diameter. (Right) Marking experiment onto metal (stainless) surface.

variants, increasing the diameter from 500 μm to 1 mm to aid heat dissipation. For this device, with a design optimised for its diameter, a 10 W CW output is possible while retaining a very narrow beam divergence angle.

We have applied this high-brightness CW PCSEL to the marking of a metal surface. If you look at Figure 10, you can see "PCSEL" written clearly.

Very recent progress by our team has led to the fabrication of a PCSEL that produces a 30 W output, realised by scaling the diameter of this emitter to 2 mm. This success offers a roadmap to 100 W and even 1 kW CW operation, by expanding the size of the PCSEL to 3 mm to 10 mm. Realising such higher powers would allow the PCSEL to replace very large lasers, such as CO_2 lasers and fibre lasers, and become the key light sources for Smart Manufacturing.

Armed with attributes

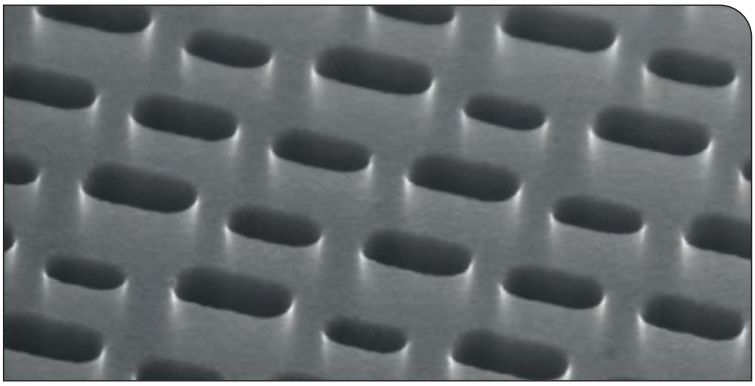
When used for lidar, one of the advantages of the PCSEL over the conventional laser is its superior beam quality that allows the use of a mechanically rotating mirror. But if rather than using a mechanical means for scanning, this could be accomplished with an electrical approach, the system would take a leap forward in terms of reliability, stability, and compactness.

Motivated by the potential to deliver a dramatic improvement in system performance, we have

recently developed a PCSEL that is capable of electrical beam scanning in two dimensions. This triumph has built on our electrical beam scanning in one dimension, reported in 2010. To progress from scanning in one direction to two, we have advanced our photonic crystal structure. By creating what we describe as a dually modulated photonic crystal, we have been able to produce a laser that emits a high-power, high-quality beam in an arbitrary direction in two dimensions.

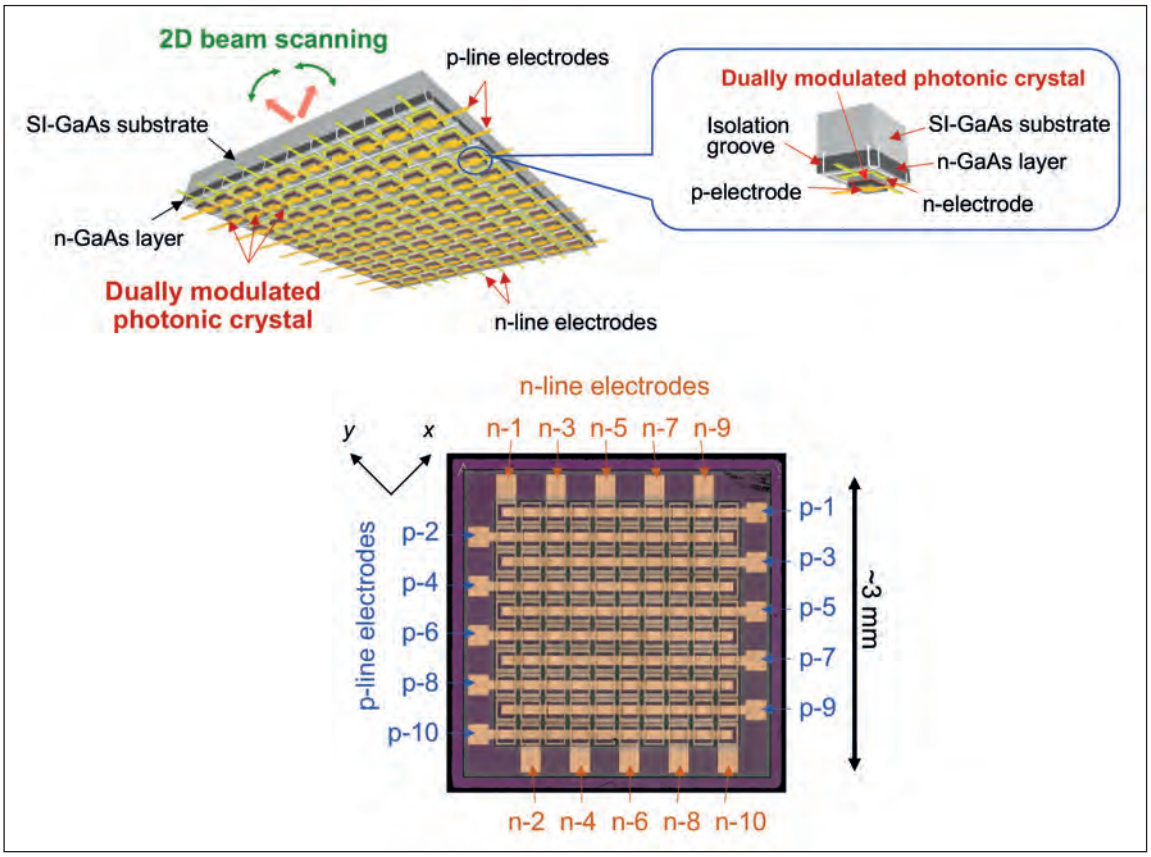
To produce a PCSEL that has electronic beam scanning in two dimensions, we simultaneously modulate the positions and sizes of the lattice points of the photonic crystal (see Figure 11). A crucial difference between the design of this particular PCSEL and its forefathers is that it has a different singularity, known as the *M* point, adopted to inhibit the emission of light prior to modulation. Introducing dual modulation to this design ensures that the beam is only emitted in the direction of one's choosing.

We have fabricated an on-chip 10 by 10 array of dually modulated PCSELs: each individual laser has a footprint of 150 μm^2 and a circular current injection area with a 100-μm diameter. All electrodes are integrated onto the back of the chip, so that the laser beams are emitted from the front without obstruction (see Figure 12). To address the array, PCSELs are electrically isolated from each other, and only the PCSEL(s) at the intersections of *p*- and *n*-line electrodes across which a voltage is applied are driven. Each PCSEL is encoded with its own unique beam emission direction. From each PCSEL two beams are simultaneously emitted at oblique angles, which are mutual reflections of each other about the surface normal.



➤ Figure 11. Scanning-electron-microscope image of a dually modulated photonic crystal (bird's-eye view). Lattice-point positions and sizes are simultaneously modulated. These modulations encode information about the beam emission direction. Also, the lattice constant (equal to the spacing between the lattice points) is set to $1/\sqrt{2}$ times the wavelength in the material (195 nm).

With our arrayed chip we can drive 100 PCSELs in any order, and at any speed. This capability, illustrated in Figure 13, offers just one example of beam scanning; in general, various beams can be scanned in any order, at any timing. It's also worth noting that the number of resolvable points is not limited to 100 – in fact, it can be increased to over 90,000 without



➤ Figure 12. On-chip array of dually modulated PCSELs for beam emission in various directions in two dimensions. (Top) schematic of the entire device. (Bottom) microscope image of the bottom of the chip.

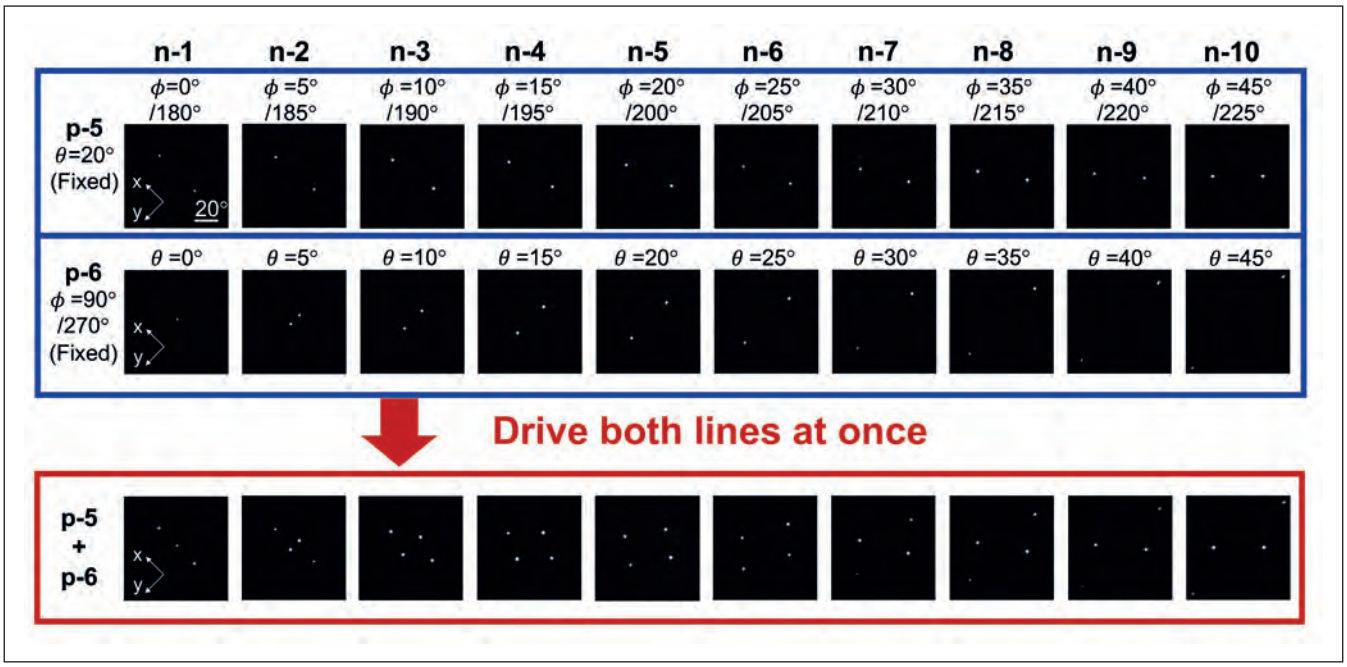


Figure 13. Example of multi-beam scanning using a lasing wavelength of 940 nm. The top row of snapshots show beam scanning when the n-line electrodes are driven in sequence from n-1 to n-10 while the p-line electrode is fixed to p-5. For this sequence, a fixed polar emission angle θ (from the surface normal) of 20 ° has been encoded, while azimuthal emission angles ϕ (from the positive x axis) have been encoded to vary from 0 °/180 ° to 45 °/225 °; these emission angles are precisely those observed in the snapshots. Next, the middle row of snapshots shows beam scanning when the same sequence of n-line electrodes is driven, but the p-line electrode is fixed to p-6. In this case, it is the azimuthal angles ϕ that have been designed to remain fixed to 90 °/270 °, while the polar angle θ has been designed to vary from 0 ° to 45 °; again, these emission angles are precisely those observed in the snapshots. Finally, the bottom row of snapshots shows beam scanning when the electrodes in the top and middle rows are driven at the same time to scan four beams simultaneously.

considerably increasing the chip area. Furthermore, it is possible to construct a new type of lidar system that leverages this beam-scanning technology; the combination of flash- and beam-scanning lidars, a topic we are planning to discuss elsewhere.

This latest success is yet another example of our efforts to strengthen the research and development of the PCSEL and drive its deployment. To support this endeavour, we have recently established the Center of Excellence for this device. We are keen to share what we have realised, and can provide PCSEL samples for testing, provided under a material transfer agreement.

This work constitutes a portion of the research performed by Noda's Quantum Optoelectronics Laboratory in conjunction with the Nano processing Lab at Kyoto University. The authors are deeply grateful to faculty members, researchers, and students of both laboratories. This work was carried out under the project of Council for Science, Technology, and Innovation, Cross-minesterial Strategic Innovation Promotion Program, Photonics and Quantum Technology for Society 5.0 (Funding agency: QST), and under the CREST program Next-generation Photonics commissioned by the Japan Science and Technology Agency .

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Advancing InGaN epitaxy for long-wavelength LEDs

Indium-rich InGaN, the established material of choice for green LEDs, is now starting to challenge traditional red-emitting materials in microLEDs for head-mounted displays

BY ROB ARMITAGE, TSUTOMU ISHIKAWA, TED CHUNG AND ZHONGMIN REN FROM LUMILEDS

THE AGE of LED lighting is now upon us. Today white LEDs, utilizing phosphor-converted InGaN blue pump sources, are ubiquitous in general illumination. Due to this, attention has shifted away from blue LED technology, with the focus now on improving InGaN epitaxy at longer wavelengths, as this holds the key to more efficient emission in this spectral domain. Such efforts are motivated by a desire to increase the wall plug efficiency (WPE) of green and amber LEDs, and ultimately improve phosphor-free illumination systems based on colour mixing. This approach has already gained some traction at current system-efficacy levels, thanks to the benefits that colour-tuneable lighting brings to human health and well-being. In future, there is the tantalising prospect of building next-generation systems that exceed the efficacy of phosphor-converted blue light sources, enabled by large improvements to the WPE of LEDs in the green-amber range. Getting there, though, will not be easy.

➤ Grand Place, Brussels

When increasing the emission wavelength of the InGaN LED, there is never an abrupt decline in the internal quantum efficiency (IQE). Instead, it gradually decreases – although this adds up to a large difference between the external quantum efficiency (EQE) of state-of-the-art blue and green emitters (see Figure 1). Inspect the plots of the EQE at various currents, and it is clear to see that the wavelength dependence of InGaN efficiency is intertwined with that of the widely discussed malady known as 'droop'. These phenomena are naturally interconnected, given that they are governed by fundamental recombination physics and non-radiative Auger recombination.

Another factor at play in InGaN LEDs, which explains many of its unusual characteristics, is the crystal polarization charges that exist at the interfaces between the quantum wells and barriers. Present in conventional devices formed by epitaxial growth along the c-axis orientation, these charges give rise to internal electric fields across the QWs – and as the indium content in these wells increases, the quantum-confined Stark effect (QCSE) get stronger.

It's worth noting that the strong QCSE in InGaN LEDs is actually a blessing and a curse. Its benefit is that by shifting both the electron and the hole energies, it is possible to realise green and even red emission with QW indium concentrations that are manageably low in terms of the challenges of crystal growth. But this blessing comes at the cost of a comparatively long radiative recombination lifetime, of the order of 100 ns. Due to this, degenerate hole densities arise in green LEDs at current densities below 10 A cm^{-2}, and the Auger process becomes the primary recombination mechanism at practical operating conditions. The higher carrier densities reached in longer wavelength InGaN LEDs impair performance, increasing the severity of IQE droop, inducing a blue shift, and broadening the emission spectra at higher

drive currents. Working in tandem, these drawbacks are so significant that they are holding back the large-scale deployment of green and yellow LEDs in solid-state lighting, especially for applications requiring high luminance.

To address all these technical challenges, our team at Lumileds has been participating in a project funded by the US Department of Energy that is trying to increase the efficiency of InGaN LEDs at longer wavelengths. Working with us are collaborators from the University of Michigan, the University of New Mexico, Ohio State University and Sandia National Laboratory.

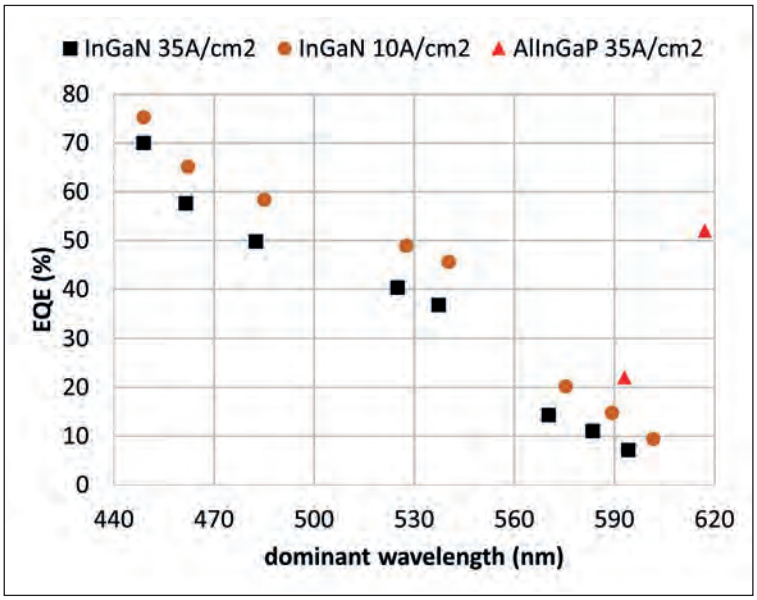
Our strategy for realising far-more-efficient green LEDs is to engineer the epitaxy so that we utilise many QWs, thereby reducing the average carrier density within the active region. While this may appear to simply involve increasing the number of QWs, it's actually more subtle. Success hinges on evenly distributing electrons and holes across multiple quantum wells – a goal that is frustrated by an imbalance of the respective carrier mobilities, as well as energy barriers to carrier injection and inter-well transport, associated with interface polarization charges.

To enjoy success, we exploit ever-present threading dislocations that arise from GaN epitaxy on substrates such as sapphire and silicon. By controlling growth conditions, we open or close pits around dislocations, as this allows us to produce devices that are three-dimensional at the microscopic scale and enhance hole injection through the lateral direction. With this strategy we have fabricated LEDs that have an EQE exceeding 40 percent and a dominant wavelength of 525 nm when driven at a current density of 35 A cm^{-2}. As well as diminished droop (see Figure 2), these optimized green multiple-QW designs offer reduced sensitivity of spectral characteristics to changes in current density (see Figure 3).

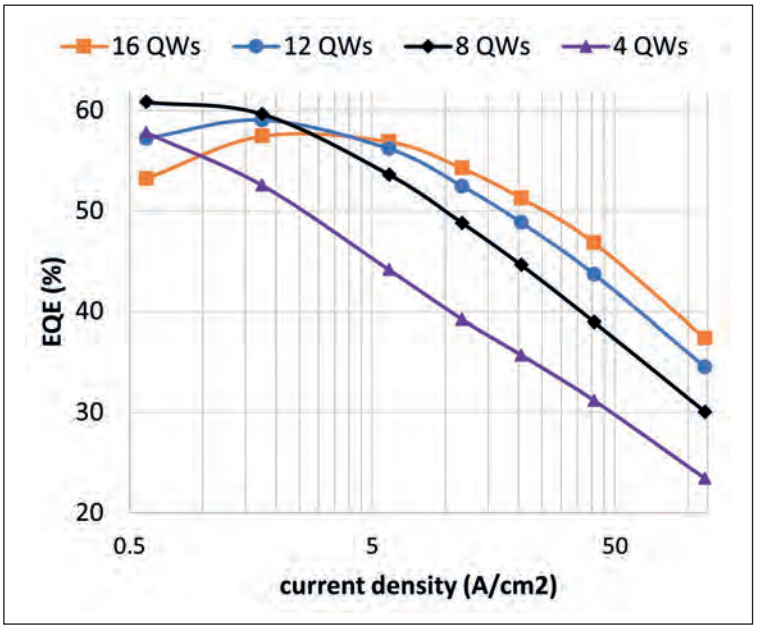
These observations are consistent with our understanding that non-radiative recombination and shifts in spectral properties have a common origin, namely a high carrier concentration, and that both these weaknesses can be addressed with LED designs that drive down the average carrier density. Note that even for our green LEDs, specifically optimized for high-power operation, employing a lower current density ensures large efficiency gains (see Figure 2).

From green to red

For wavelengths longer than 590 nm, today's AlInGaP LEDs have a much higher intrinsic efficiency than their InGaN cousins (see Figure 1). While this is likely to always be the case, the emergence of microLED display technology has generated considerable interest in InGaN red epitaxy. Partly fuelling this interest is a comparison between the respective efficiency levels for different colours – this identifies that regardless of the material system, the red LED consumes the majority of the power in a display.



➤ Figure 1. The external quantum efficiency of state-of-the-art visible wavelength LEDs with 1 mm by 1 mm dimensions and a hemispherical dome encapsulation.

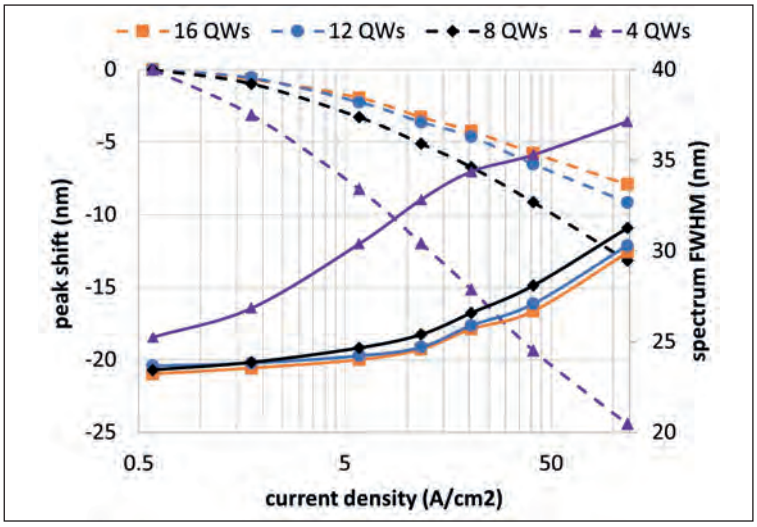


➤ Figure 2. External quantum efficiency as a function of current density for optimized green LEDs with various numbers of quantum wells in the active region.

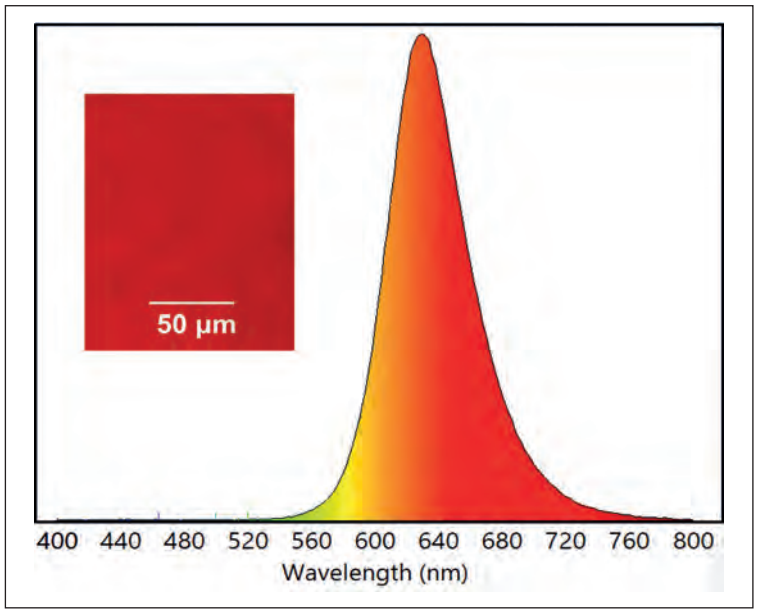
There are several arguments in favour of a switch from red AlInGaP LEDs to those made from InGaN. Moving to InGaN for the red content would simplify the complexity of integration, as all sub-pixels would be based on the same materials system. Attempts to realise monolithic integration would also face fewer hurdles. In some cases, these gains could be so compelling that they could counter the hit

to efficiency. Another consideration supporting a switch to InGaN is that despite its lower intrinsic efficiency, it might outperform AlInGaP at sufficiently small pixel sizes, due to its slower surface recombination velocity. Whether that's actually the case is an important question with an ever-changing answer, influenced by improvements to epitaxy and die passivation technologies.

We are continuing to consider this matter, updating our view as we advance both materials systems.



➤ Figure 3. Spectral parameters versus current density for green LEDs shown in Figure 2. Dashed lines indicate the full-width at half maximum (FWHM) and solid lines indicate the peak wavelength shift relative to its value at a low current density.



➤ Figure 4. Spectrum of an InGaN red LED operated at 40 A cm^{-2} with a peak wavelength of 638 nm and a dominant wavelength of 610 nm. The inset shows the emitting surface observed under an optical microscope at the forward voltage of 1.8 V, corresponding to the onset of light emission.

For InGaN, the process that we use to make red epitaxial wafers employs standard LED production substrates and reactors. By taking this approach, our InGaN wafers for blue, green and red LEDs are interchangeable in die fabrication. This contrasts with many exotic approaches for making red LEDs, such as selective-area epitaxy, porous GaN templates and InGaN pseudo-substrates. All are potentially interesting from a performance standpoint, but come with obvious disadvantages in manufacturing cost and complexity.

The emission of a representative InGaN red LED produced by our team is broad, but spatially homogenous at the microscopic scale, even for a very low injection current (see Figure 4). For such broad spectra the dominant wavelength is substantially shorter than the peak wavelength; due to this, in order for the eye to actually perceive this emission as red, the peak wavelength must sit well within the red. While InGaN LEDs with peak wavelengths as short as 600 nm have been referred to as 'red' in the literature, they actually fail to meet the minimum colour requirements for display applications. Our epitaxy is capable of producing LEDs with true red emission at current densities up to 50 A cm^{-2}. These devices have wall-plug efficiencies comparing favourably with those published for InGaN LEDs of similar dominant wavelengths.

One of the issues of a shift in wavelength with drive current is that it could lead to variations in the colours produced by a display at different brightness levels. While this is easy to overcome with pulse width modulation (PWM), the sensitivity of the InGaN red spectrum to the current density has implications for display applications. When deploying blue and green LEDs in displays, it is common practice to either plot the efficiency as a function of current density for one device, or for a group of devices with the same wavelength target (see Figure 5). But for InGaN red LEDs, a better way to visualize the accompanying data is to use a contour plot that captures the characteristics of many LEDs, with differences in wavelength obtained by controlled changes to the QW indium concentrations (see Figure 6). One of the merits of this plot is that it expresses the trade-off between efficiency and current density for a particular colour requirement, expressed by the dominant wavelength.

With red InGaN LEDs, the price to pay for maintaining acceptable colour characteristics at a higher current density is a plummeting efficiency. The workaround is to optimise the epitaxial process for making red LEDs for a very specific current density. There is the potential to exceed a 10 percent WPE at a sufficiently low current density, but LEDs driven in that manner may fall short of radiance requirements. The greatest opportunities to improve red InGaN LEDs through refinement to epitaxy are associated with increasing the IQE, narrowing the spectral width and minimising the blue shift. When driven at low current densities, the

operating voltage for the InGaN red LED is already near its theoretical minimum value expected for its emission wavelengths (see Figure 7).

The results described in the previous paragraphs are for 'macro' LEDs. The data shows the best performance possible for the epitaxy, using a die design that has a high light-extraction efficiency and is unaffected by surface recombination.

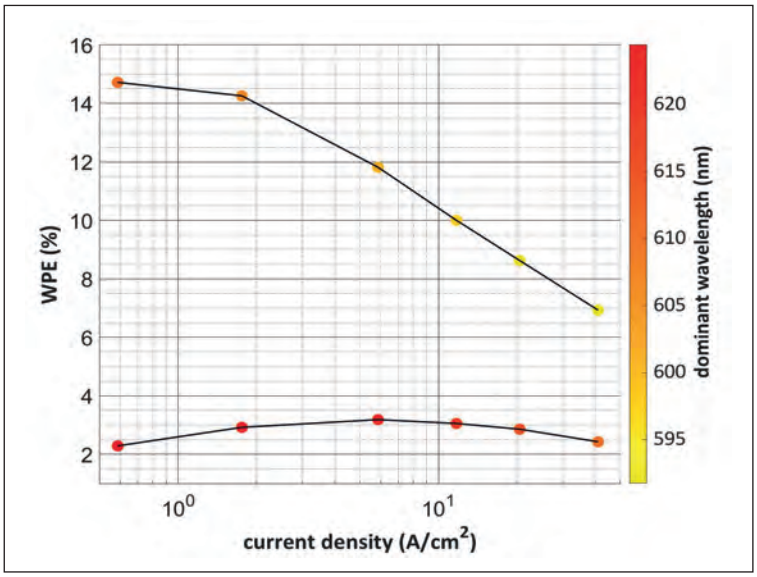
From macro to micro

We have also characterized the performance of a portfolio of microLEDs with various mesa sizes, produced from similar epiwafers. Earlier this year we reported the results of this study at the SPIE *Photonics West Conference* (see Figure 8 for a summary of our results). This investigation involved the fabrication of arrays with mesas that are all the same size, and connected in parallel to a continuous *n*-type semiconductor layer. To increase light extraction, we textured the *n*-type layer after removing the growth substrate. Both InGaN green and blue LEDs were produced for benchmarking purposes. Comparing our range of InGaN LEDs with our AlInGaP LEDs is not straightforward, as a different die fabrication process is needed that may influence efficiency. However, we have made every effort to minimise this impact.

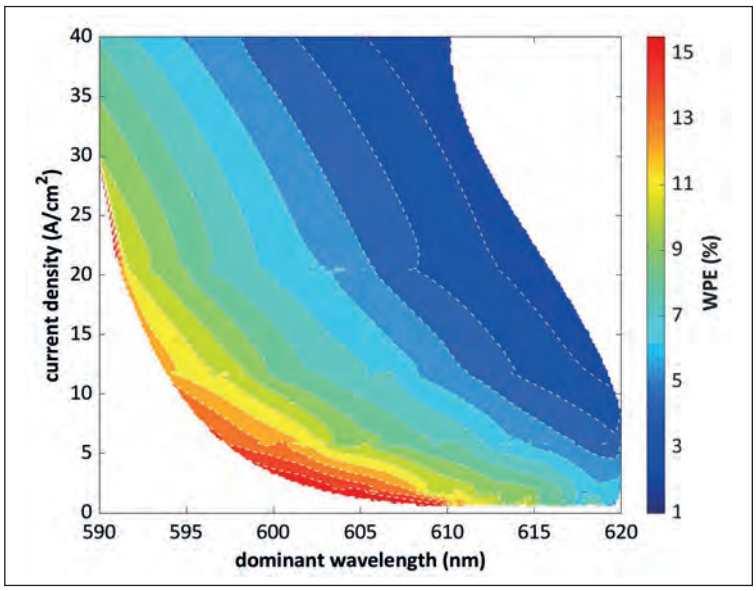
Our results are in line with those of other studies, showing that for InGaN microLED arrays there is a decrease in the sensitivity of efficiency to mesa size with increasing wavelength – and practically zero sensitivity for red. Some have speculated that this behaviour comes from differences in the lateral diffusion length within the QWs depending on carrier localization.

Another important finding of our study is that at a fixed current density the emission profile of the InGaN arrays is basically invariant with mesa size, down to the smallest size studied, which is just 2 μm. This observation is consistent with the conclusions of our finite element analysis, which suggest that the length scale of strain relaxation from the mesa edge is well below 1 μm.

For all colours of our InGaN microLED arrays, we find that the absolute WPE is significantly below that of the corresponding macro LEDs. We attribute this difference primarily to the higher extraction efficiency of the macro LEDs, resulting from their

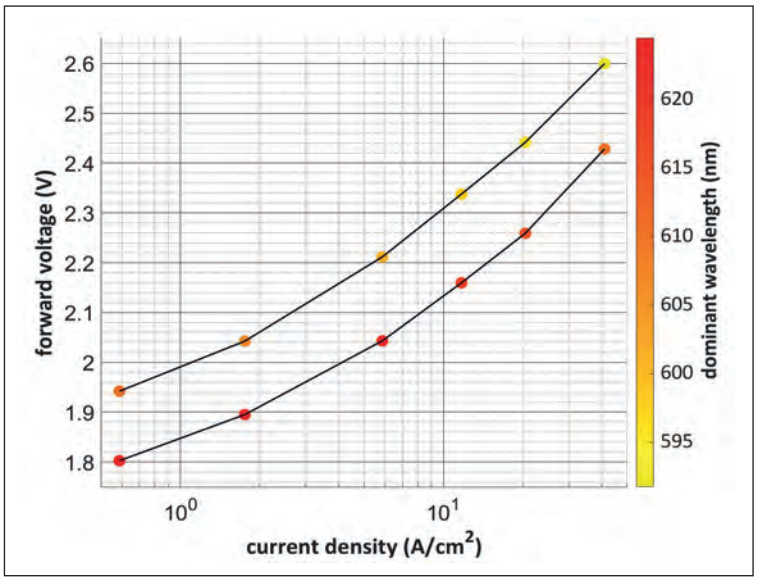


➤ Figure 5. Wall-plug efficiency (WPE) versus current density (J) for two representative encapsulated 1 mm by 1 mm InGaN red LEDs with different wavelength targets. The colour bar indicates the dominant wavelength of the emission spectrum at each point.

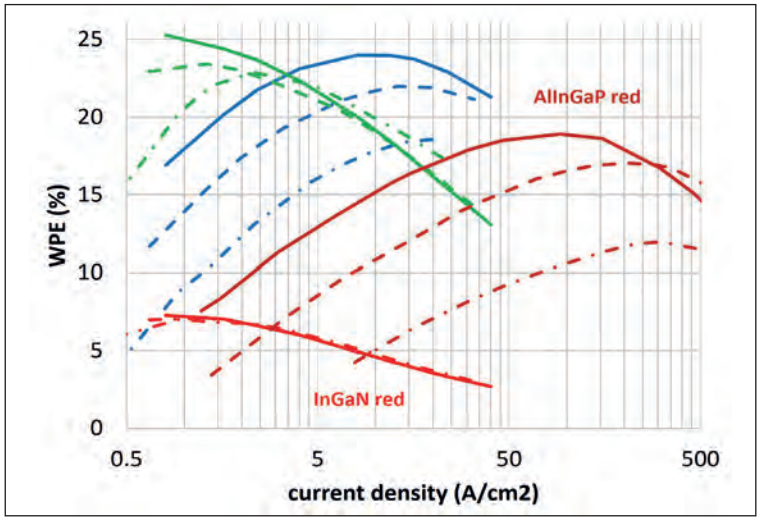


➤ Figure 6. Contour plot of the InGaN red wall-plug efficiency (WPE) as a function of current density and dominant wavelength at that current density. The plot is constructed from WPE and spectrum measurements versus current density for many encapsulated 1 mm by 1 mm LEDs of the same epitaxy design with varied quantum well indium concentrations.

The case for InGaN may strengthen, as our InGaN red epitaxy is still in its early stages of optimization. We believe there are further opportunities to diminish the droop of InGaN red LEDs and improve their spectral characteristics.



➤ Figure 7. Current density versus voltage (J-V) curves for two representative InGaN red LEDs with different wavelength targets. The colour bar indicates the dominant wavelength of the emission spectrum at each point.



➤ Figure 8. Wall plug efficiency as a function of current density for microLED arrays of different colours. Solid, dashed, and dashed-dot lines indicate data in order of decreasing mesa sizes (7 μm, 4 μm, and 2 μm for InGaN; and 9 μm, 6 μm, and 4 μm for AlInGaP). The dominant wavelengths corresponding to peak efficiency are 605 nm (InGaN red), 630 nm (AlInGaP red), 540 nm (green), and 460 nm (blue).

encapsulation and the use of die materials with lower optical losses. However, the efficiency of blue and green microLED arrays is also hampered by surface recombination.

So long as there is not a hard upper-constraint on the current density of an LED, those made from AlInGaP are capable of a much higher efficiency than their InGaN counterparts, for mesa sizes down to at least 4 μm. What's more, AlInGaP LEDs have much smaller colour shifts with current density, and their spectra are narrower, with a full-width at half maximum of around 20 nm. However, due to their higher surface recombination velocity compared with their InGaN counterparts, AlInGaP microLEDs have a significant sensitivity to mesa size; to maximize their efficiency, they must be driven at high currents and low PWM duty cycles. To minimise the resulting efficiency trade-offs at the system level, much research and development is now being directed at increasing the internal quantum efficiency of AlInGaP microLEDs at low current densities.

For direct-view applications, such as TVs, which have stringent requirements on the colour characteristics, relatively large pixel dimensions are employed for the displays. Here the advantage of AlInGaP is expected to persist in future, as it is rooted in fundamental physics. LEDs featuring AlInGaP QWs have the intrinsic advantage of a higher radiative recombination coefficient, primarily resulting from the absence of polarization and the QCSE. It's a different story for head-mounted displays, which require pixel dimensions of no more than a few microns. Based on the extrapolation of our results for both materials systems to smaller pixel dimensions, the indication is that InGaN could be the preferred red emitter material for head-mounted displays, due to the far higher surface recombination losses in AlInGaP.

The case for InGaN may strengthen, as our InGaN red epitaxy is still in its early stages of optimization. We believe there are further opportunities to diminish the droop of InGaN red LEDs and improve their spectral characteristics, drawing on optimization strategies that have brought us success with green LEDs.

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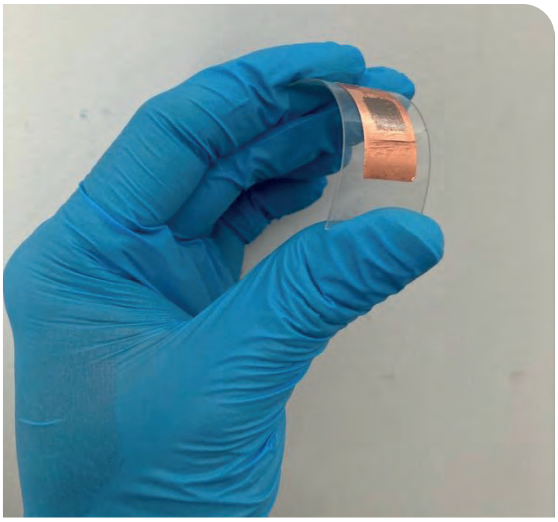
Laser lift-off yields superior flexible HEMTs

Flexible transistors with minimal degradation are produced with a lift-off process that involves a UV laser and GaN-on-sapphire HEMTs

MANY DIFFERENT APPROACHES can produce flexible GaN HEMTs via transfer technologies. But all lead to more damage to this device than laser lift-off, according to engineers from the University of South Carolina.

Using a 193 nm excimer laser, researchers at that university have recently transferred GaN-on-sapphire HEMTs to a copper tape that is mounted on a flexible, transparent plastic. It is a process that leads to a decline in the drain current of the HEMT by just 18 percent – that's far less than the fall in that figure-of-merit resulting from a range of other transfer techniques, all based on etching GaN-on-silicon HEMTs.



➤ Transferring GaN HEMTs to a copper tape, attached to a transparent substrate, introduces a significant degree of flexibility.

Flexible GaN HEMTs are attracting a great deal of attention because they can serve in many applications. Illustrating this point, team spokesman Md Didarul Alam remarks: "The device has great potential in applications for on-screen power amplifiers in mobile phones, strain-controlled power devices in bio-inspired electronics, such as acceleration-feedback-control in self-driving cars or robotic motion, and human-machine interfaces." There are also opportunities for flexible GaN HEMTs in high-frequency microwave power applications, such as reconfigurable antenna; and in high-power conformal and flexible RF devices that are compatible with 5G communication systems.

Most efforts at developing processes for transferring GaN HEMTs to a flexible substrate have focused on mechanical grinding of the GaN-on-silicon epiwafer, followed by XeF_2 etching and wet etching. One weaknesses of this approach is a degraded backside, caused by a harsh acidic environment, as well as the strong surface tension of water.

An alternative is to grow uniform large-area hexagonal BN between the AlGaN/GaN heterostructure and substrate, prior to peeling off the nitride membrane. But mechanical transfer is difficult, argues Alam, saying that it is hard to completely peel off a large-area AlGaN/GaN membrane.

There's also electrochemical etching, which involves a highly doped GaN sacrificial layer. However, this layer damages the effective area and compromises the integrity of the released GaN heterostructure.

As well as these issues, which lead to a far greater decline in the drain current after transfer to a flexible foundation, there is another drawback: the production of the epiwafers, all based on GaN-on-silicon, is complicated and time-consuming. Part of the problem is that the epitaxial growth of GaN-on-silicon demands additional growth steps, due to the significant mismatches in both the lattice constant and the coefficient of thermal expansion between the two materials families. In addition, the quality of the GaN epilayer is inferior to that formed on sapphire, SiC or bulk GaN.

Alam and co-workers produced their flexible HEMTs by depositing on a double-side polished sapphire substrate a 30 nm-thick GaN nucleation layer, a 1.8 μm-thick GaN buffer and channel layer, a 1 nm-thick AlN spacer, and a 17 nm-thick $Al_{0.24}Ga_{0.76}N$ barrier layer. Reactive-ion etching created mesas from the epiwafer, before electron-beam deposition and subsequent rapid thermal annealing formed source and drain electrodes, and electron-beam evaporation added a gate electrode. Devices were temporarily bonded to UV tape before an ArF 193 nm laser delivered a fluence of 800 mJ cm^{-2} to remove the sapphire. Etching with dilute HCl eradicated the damage to the GaN layer, prior to bonding to the flexible substrate.

Measurements showed that this HEMT's maximum drain current fell from 422 mA mm^{-1} to 347 mA mm^{-1}.

One of the next goals for the team is to fabricate flexible HEMTs with an AlGaN-channel. "Since the critical electric field of AlGaN is higher than that of the GaN, AlGaN-channel flexible HEMTs will be more suitable for high-frequency and high-power flexible electronics applications," says Alam.

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ANGEL EVENTS

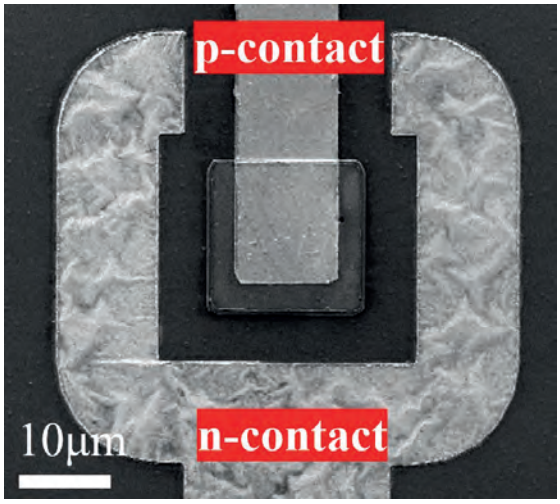
Deep UV microLEDs: Scaling boosts efficiency

Shrinking the size of deep UV microLEDs to tens of microns increases their external quantum efficiency

A TEAM from the University of California, Santa Barbara (UCSB), is claiming to have produced the most comprehensive study on the performance of deep-UV devices with differing dimensions and emission wavelengths.

"What's interesting about our work is that we saw an external quantum efficiency in microLEDs at least as good as in big LEDs, which is not so typically seen," remarks team spokesman Yfian Yao.

This is a promising finding for deep-UV LEDs, which have the potential to provide a more environmentally friendly alternative to mercury lamps for deactivating all known microorganisms and viral pathogens, including SARS-CoV-2, MERS and SARS.



A scanning electron microscopy image of a deep-UV LED produced by UCSB that has dimensions of 20 μm by 20 μm.

According to Yao, compared with previous studies of deep-UV microLEDs undertaken elsewhere, this latest work considers a broader range of wavelengths, a wider variety of sizes, and reports the highest value for external quantum efficiency.

The team were initially surprised by their observation that at higher current densities the peak external quantum efficiencies are higher in smaller devices than their larger siblings. But when they dwelled on this, they concluded that this could be expected. The reasoning is that from a materials perspective, AlGaN may be quite defect tolerant, due to its short diffusion length; the results of visible microLEDs produced by Yao's colleagues at UCSB show that they have an effective sidewall passivation technology; and it is well known that shrinking the dimensions of the devices should increase the likelihood that light can escape from this chip.

Yao and co-workers produced a range of deep-UV microLEDs by taking AlN-on-sapphire templates, loading them into an MOCVD reactor, and depositing heterostructures that feature four 1.5 nm-thick quantum wells, a 5 nm-thick magnesium-doped electron-blocking layer and a 40 nm-thick short period superlattice. Square microLEDs with sides either 300 μm, 80 μm, 40 μm or 20 μm in length were produced by using reactive ion etching to create mesas. These devices are equipped with a semi-reflective *p*-type contact and a 50 nm-thick SiO_2 passivation layer, added by atomic-layer deposition.

Measurements on a subset of microLEDs emitting at 277 nm show that increasing the mesa width from 20 μm to 300 μm results in an increase in forward voltage from 7.6 V to 9.1 V. This is attributed to improved current spreading in the *n*-AlGaN layer – although there is also a small effect due to increased current leakage.

Additional studies on deep-UV LEDs with emission wavelengths of 291 nm and 304 nm, realised by adjusting the AlGaN composition in the quantum wells, followed the trend of smaller devices delivering a higher external quantum efficiency at the drive current of 20 A cm^{-2}. The 304 nm microLED with a side of 20 μm produced the highest peak external quantum efficiency within the study, hitting 4 percent during on-wafer measurements.

Since reporting these results, the team has realised an external quantum efficiencies of around 5 percent on bare chips with similar structures, produced using a similar fabrication process. Hitting 5 percent is significant, as it is as high as the best commercial deep-UV LEDs, according to Yao. "But all of them are fully packaged, thin-film flip-chip bonded and transparently encapsulated on a reflective header, which we currently lack the expertise in."

Based on conversations with UV LED vendors, the team expects that the introduction of full packaging will roughly double the output power of their devices.

As well as reporting their better, more recent bare-wafer results, the team plans to incorporate additional structures into their deep-UV emitters, such as array of microLEDs with common contact. This will enable devices to combine a high external quantum efficiency with a high absolute power.

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New contacts enhance heteroepitaxial Ga_2O_3 MOSFETs

Ga_2O_3-on-sapphire MOSFETs raise the bar for the breakdown voltage

RESEARCHERS from South Korea are claiming to have broken new ground for the breakdown voltage of heteroepitaxial Ga_2O_3 MOSFETs. The transistors made by the team from Soongsil University, Korea Institute of Ceramic Engineering and Technology and the Korea Electrotechnology Research Institute are capable of blocking up to 2.3 kV.

The team attributes the record-breaking breakdown voltages of its MOSFETs to a new metal stack for the source and drain electrodes – it is Ti/Al/Ni/Au.

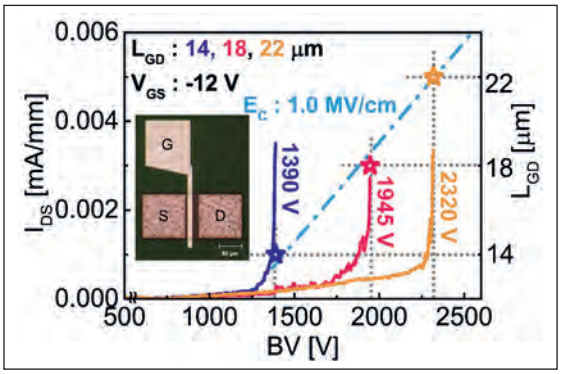
Team spokesman Geonwook Yoo from Soongsil University told *Compound Semiconductor* that in addition to the new metal stack, the record breakdown voltage may result from the relatively high temperature used to form the HfO_2 gate dielectric. "It successfully reduces not only a surface leakage path, but also a scattering effect induced from the rough silicon-doped α-Ga_2O_3 layer."

The α-Ga_2O_3 MOSFETs are formed on sapphire. It is argued that by avoiding a native substrate, the MOSFETs are not impaired by the poor thermal conductivity of this foundation. The switch to *c*-plane sapphire improves thermal management through superior thermal conductivity, while providing a platform that only has small differences in the thermal coefficient and lattice constant compared with Ga_2O_3.

Production of the α-Ga_2O_3 MOSFETs involved HVPE, a growth technique that offers many merits for high-volume production, including rapid deposition at a relatively low temperature.

Yoo and co-workers produced their devices by loading 2-inch (0001) sapphire into a HVPE chamber, heating this to 470 °C, and growing 0.9 μm of undoped α-Ga_2O_3 followed by 0.3 μm of silicon-doped α-Ga_2O_3 in just 10 minutes. Fabrication of the transistors involved: reactive-ion etching to form mesa structures about 500 nm-thick; the introduction of source and drain electrodes by electron-beam evaporation, patterning, lift-off and rapid thermal annealing; and the addition, by atomic layer deposition, of a 20 nm-thick HfO_2 gate dielectric that is capped with a Ni/Au stack. The team also produced a control with conventional Ti/Au source and drain electrodes.

According to atomic force microscopy scans of the source and drain electrodes, the new stack is far rougher than its conventional counterpart, with the value for root-mean-square roughness increasing from around 1.1 nm to 11 nm. This is attributed to Ni-Al alloy aggregation during the rapid thermal anneal.



➤ Increasing the gate-to-drain distance of the α-Ga_2O_3 MOSFET increases its breakdown voltage. The inset shows an optical microscopy image of the Ti/Al/Ni/Au metal gate stack.

Using transmission-line measurements, the team extracted values for the contact resistance. Switching the electrode from Ti/Au to Ti/Al/Ni/Au slashed the contact resistance from 1.9 kΩ mm to just 0.2 kΩ mm.

The low contact resistance, which even occurs for α-Ga_2O_3 layers with a low silicon doping level, results from diffusion of aluminium into the titanium layer during rapid thermal annealing. The resulting Ti-Al inter-metallic phase leads to the generation of many oxygen vacancies at the interface between α-Ga_2O_3 and the inter-metallic compounds.

Electrical measurements on the team's MOSFETs showed that the new gate stack leads to a significantly higher on current. For both types of device, off current is limited by leakage through the undoped α-Ga_2O_3 layer, rather than leakage through the gate oxide. The MOSFET with the new gate stack has a field effect mobility of 20.4 $cm^2\ V^{-1}\ s^{-1}$, which is claimed to be a record for heteroepitaxial Ga_2O_3 MOSFETs.

Yoo and co-workers have also conducted three-terminal off-state breakdown voltage measurements, investigating MOSFETs with gate-to-drain distances of 22 μm, 18 μm and 14 μm. They found that the breakdown voltage increases with distance to hit 2320 V, indicating a critical field of 1 MV cm^{-1}.

One of the plans for the team is to continue to develop hetero-epitaxial growth technology for substrate diameters of 6-inch or more. Another aim is to advance MOSFET design, introducing the likes of a field plate and a passivation layer. These refinements should boost the blocking voltage and enhance the figure-of-merit for power.

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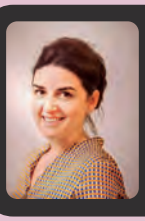

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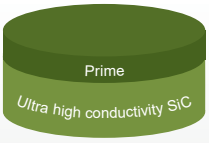

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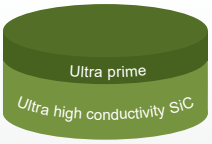

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