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ISSUE VII 2025

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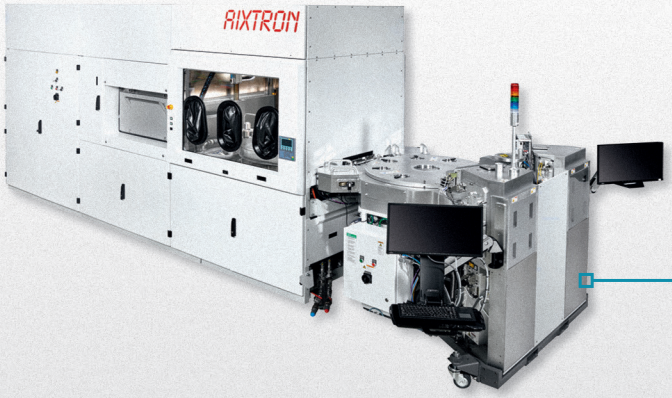

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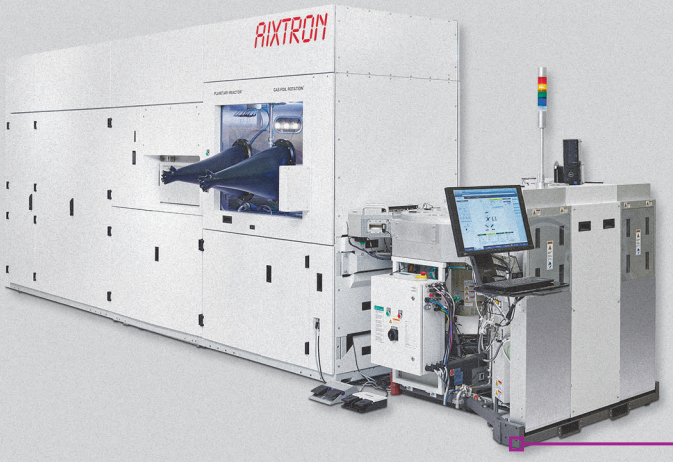

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VIEWPOINT

BY PHIL ALSOP
EDITOR

Power electronics at a tipping point

The past decade has been defined by incremental gains in efficiency and miniaturisation. But if the past few months of research breakthroughs are any indication, power electronics is now entering a true inflection point - one that could reshape everything from consumer devices to national grids.

At Northeastern University, scientists have made plastics behave like metals. Their 3D-printed plastic-ceramic composite conducts heat better than stainless steel while remaining electrically insulating - an extraordinary combination.

From data centres to EV batteries, this could mean cooler, safer systems without the weight or short-circuit risks of metal. In parallel, teams in Japan and the US are redefining how we manufacture and manage wide-bandgap semiconductors. Sumitomo Chemical's quartz-free HVPE GaN wafers and Nagoya University's first functional gallium oxide pn diodes suggest that long-standing bottlenecks in scalability and material science are finally breaking.

Even existing materials like SiC are being 'reinvented'. Osaka researchers have found a way to anneal devices without compromising reliability, while the US National Renewable Energy Laboratory's ULIS module demonstrates how clever design can yield fivefold energy density gains.

Meanwhile, recycling silicon sludge into SiC crystals at Tohoku University hints at a future where performance and sustainability go hand in hand.

Yet perhaps the most striking development is who is now steering the field. Nvidia -better known for graphics chips than power semiconductors - is dictating architectures for 800V AI data centres. Like Tesla's push for SiC in EVs, Nvidia's endorsement of GaN could accelerate adoption across the supply chain. Suddenly, the conversation is not about if GaN and SiC will dominate, but how quickly.

Meanwhile, the geopolitical dimension is impossible to ignore. China continues to expand its dominance in traction inverters. The UK eyes leadership in solid-state transformers for smart grids. US labs are racing to develop DC circuit breakers and modular, stackable power movers. Europe is investing in talent pipelines. Power electronics, once a niche materials science pursuit, is now industrial strategy.

What ties these advances together is not simply better chips, but systems thinking. Materials, design, manufacturing, and sustainability are converging. The sector is no longer asking whether it can catch up with demand from AI, EVs, and renewable grids - it is beginning to define the pace of that demand itself. We are witnessing the foundations of a new energy infrastructure, built not just on silicon, but on imagination, collaboration, and urgency. The question is no longer if these technologies will scale, it is who will control the future they enable.

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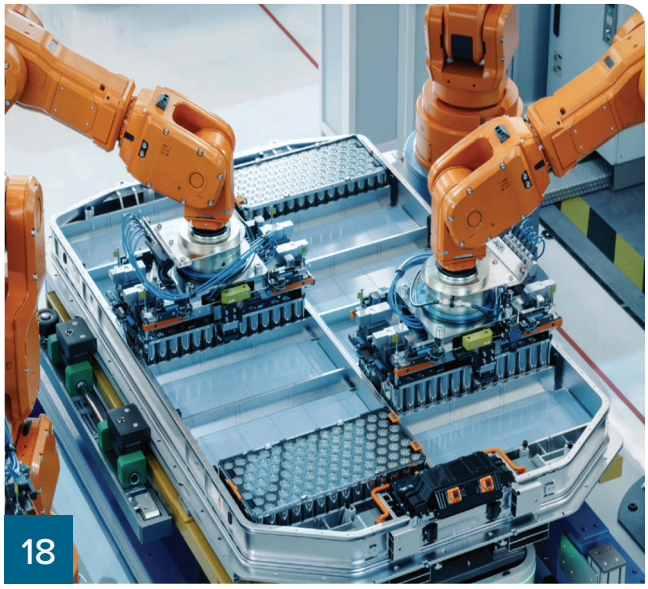

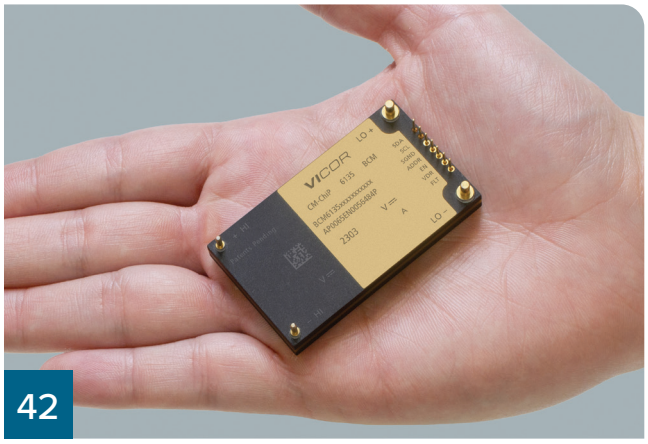

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Heat-conductive plastic could help cool power chips

3D printing allows a new, lightweight plastic-ceramic composite to be tailored to specific shapes and sizes

NORTHEASTERN UNIVERSITY researchers have developed a new, lightweight plastic-ceramic composite that conducts heat and can be used to more efficiently cool advanced power electronics in phones, data centres and cars.

“Managing heat is a big challenge for power electronics and devices like radar antennas,” says Northeastern Randall Erb, head of the university’s Directed Assembly of Particles and Suspensions (DAPS) Lab and lead researcher on the project.

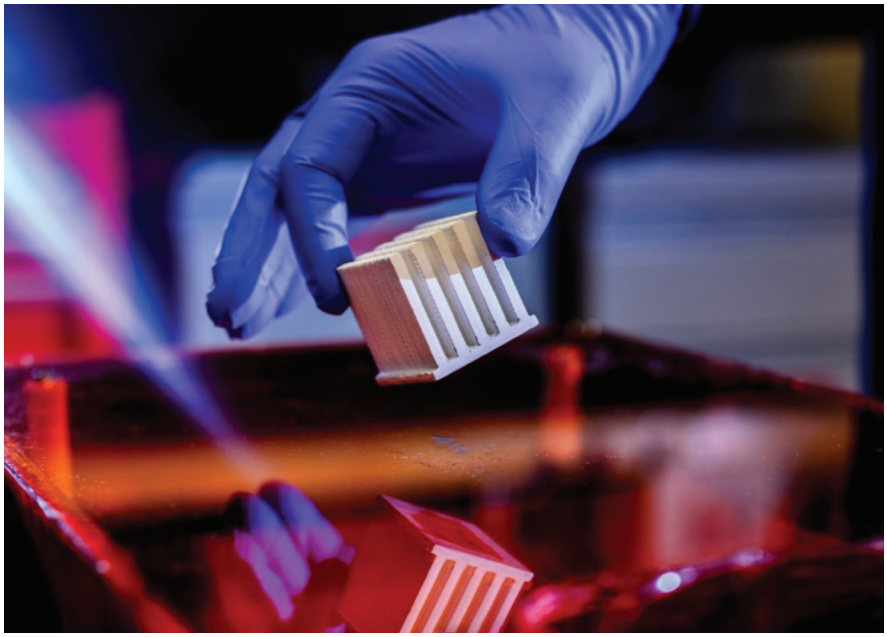
“When electronics overheat, you either have to slow them down or turn them off. That might be fine for a phone, but not for critical systems like radar.”

Northeastern researchers, in collaboration with the US Army Research Laboratory, developed the material that combines ceramics, polymers and additives into a 3D-printable plastic composite. It has a unique internal structure, ordered down to the nanoscale, that lets heat move through it easily.

“Plastics are normally terrible at conducting heat,” says Daniel Braconnier, a former PhD student in Erb’s lab. “Adding ceramic particles helps a bit, but the plastic still slows heat flow too much.”

The breakthrough was finding a way to precisely organise the material at every scale — from molecules all the way up to the printed part. Using 3D printing, the team carefully positioned ceramic particles, then used special heating steps to grow tiny bridges of crystalline polymer between them.

This connected network allows heat to travel efficiently, making the material



even more thermally conductive than stainless steel, while being four times lighter.

“These properties can enable much higher performance in many systems,” Erb says.

While metal materials like stainless steel can short out electronics if they touch them, the new material is an electrical insulator. It also doesn’t block radio frequency signals, which means it won’t interfere with 5G or radar systems.

“These new materials can cover and protect circuits without causing electrical shorts,” Erb continues. “They help pull heat away from advanced telecommunication devices without blocking their signals.”

“Industry keeps pushing for higher power in smaller packages, which means devices keep getting hotter,” Braconnier says. For example, he notes that an iPhone processor often doesn’t run at full speed in hot conditions to avoid overheating.

The team also sees potential far beyond phones.

“Data centres generate huge amounts of heat, and industry doesn’t have a sustainable solution yet,” Erb says. “Our material won’t solve it alone, but it could help by providing a better thermal interface with chips and other cooling systems.”

They’re also looking at electric vehicles, where overheating batteries can cause dangerous fires.

“Our material could be used around battery cells to spread out and remove heat, helping prevent thermal runaway events,” Erb says.

The team is now working to scale up production of the material in partnership with the US. Army Research Laboratory.

Scaling quartz-free HVPE of GaN-on-GaN epiwafers

Sumitomo Chemical targets the epiwafer market with 6-inch material produced in a quartz-free HVPE reactor that's designed for mass production

k increase the adoption of GaN power devices via a reduction in production costs, Sumitomo Chemical has developed a quartz-free HVPE reactor for mass production that can accommodate 6-inch substrates. This latest triumph builds on previous successes by the Japanese company, which has shown that quartz-free HVPE can grow GaN layers with record room-temperature mobilities. Epilayers also feature very low background concentrations of silicon, oxygen and carbon.

Spokesman for the team, Ryota Ito, told Compound Semiconductor that the quartz-free HVPE technology is now very close to full optimisation. "The mobility at room temperature is close to theoretical values, and the impurity concentration is below the detection limit as measured by secondary ion mass spectrometry."

To underscore the capability of their new tool, engineers from Sumitomo Chemical have used their reactor to produce 4-inch and 6-inch GaN epiwafers. This involved the growth of a silicon-doped GaN layer, subsequently scrutinised by various characterisation techniques.

The 4-inch substrate employed in this study was produced internally, using the void-assisted separation method. This substrate had a uniform threading dislocation density of 1-3 x 106 cm-2 and an off-angle of 0.4°, tilted from the exact + c-plane towards the m-direction. "The off-cut angle is intentionally used to prevent the occurrence of hillocks," explains Ito.

For growth on 6-inch wafers, the team at Sumitomo Chemical turned to a GaN-on-sapphire template. Note, though, that 6-inch free-standing GaN substrates are under development.

Growth conditions employed included atmospheric pressure, a growth rate of approximately 1 mm min-1, the use of ammonia and gallium monochloride as source gases, and a mixture of hydrogen and nitrogen for the carrier gas.

According to Fourier transform infrared spectroscopy, the silicon-doped GaN epilayer on the 4-inch native substrate has a thickness of 14.1 mm, with a standard deviation of 3.4 percent. Commenting on this, the team remarked in their paper that whereas conventional HVPE-grown GaN tended to exhibit a large thickness variation, the optimised quartz-free HVPE system led to a uniform distribution, similar to that of an MOCVD-grown epitaxial film. For the growth of epiwafers on 6-inch templates, the thickness uniformity is a little higher, with a standard deviation of 4.4 percent.

To evaluate doping, the engineers at Sumitomo Chemical considered the difference between the density of donors and acceptors, determined by a non-contact capacitance-voltage instrument. For MOCVD-grown GaN on 100 mm free-standing GaN, the standard deviation is 14.3 percent – and for GaN grown by quartz-free HVPE on 100 mm free-standing GaN it's just 3.0 percent.

The team also conducted photoluminescence measurements on their latest GaN epilayers, and compared the spectra with that obtained for an equivalent sample produced with a prototype reactor. The film grown with the more recent reactor, designed for mass-production, produces stronger near-band-edge emission, thanks to suppression of carbon contamination. Also encouraging is a reduction in green luminescence, indicative of a reduction in the density of point defects – this is attributed to a superior reactor design that supresses the leakage of gas from/into the growth area.

To demonstrate carrier control in their quartz-free HVPE reactors, the engineers at Sumitomo Chemical varied the silicon source rate, with a step change for every 600 nm of GaN growth. Analysing the doping profile via secondary ion mass spectrometry determined that the doping level is constant in each layer, and at the interfaces there is a steep change in silicon concentration.

This investigation also showed that with the latest quartz-free HVPE reactor there is linear doping with silicon concentration, over a wide range from 1 x 1014 cm^{-3} to 1 x 1018 cm^{-3}.

As many power devices operate in the kilovolt range, controlling the carrier concentration in the range below 1 x 1016 cm-3 is critical. Excelling in this regard, Sumitomo Chemical's latest quartz-free HVPE reactor offers the capability to produce devices with breakdown voltages of 10 kV or more. Sumitomo Chemical does not intend to produce and sell its quartz-free HVPE reactors. "We are a GaN substrate vendor, and we are planning to sell GaN-on-GaN epitaxial wafers produced by quartz-free HVPE," says Ito.

USTC team develops ultrafast junction temperature mapping of GaN PiN diode

Confocal thermoreflectance microscopy approach achieves time-resolved Tj measurement during extreme stress transients

RESEARCHERS from University of Science and Technology of China (USTC) have achieved dynamic junction temperature (Tj) mapping of a vertical GaN PiN diode during extreme stress transients up to 10000 A/cm^2, using ultrafast confocal thermoreflectance microscopy (CTRM) featuring a sampling rate of 105 Sa/s.

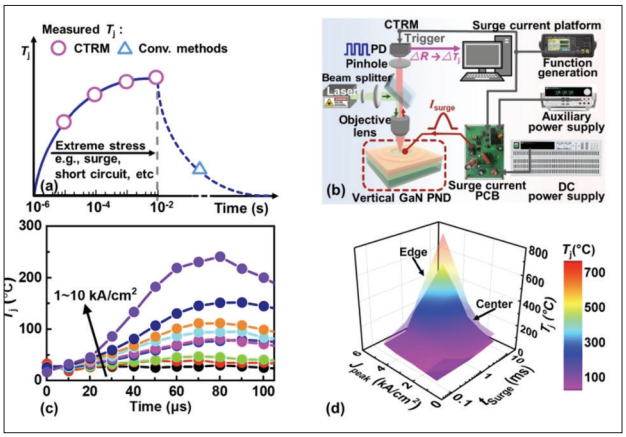
The approach, they say, enables time-resolved Tj measurement during extreme stress transients, enabling the identification of degradation/failure mechanisms.

When operating at high-frequency and high-power levels, the elevated Tj presents a critical challenge for GaN power devices. In particular, power devices are usually required to withstand extreme stress such as surge current, in which the heat generation during the high-power transient within a short duration (10^{-5}~10^{-2} s) would cause rapid Tj rise or even device failure.

However, conventional Tj monitoring techniques (e.g., thermocouple, infrared imaging) with relatively long response delay over milliseconds are unable to capture the abrupt change of Tj, which is an obstacle towards the identification of device degradation/ failure under extreme stress.

The USTC researchers say that thanks to the ultrafast Tj mapping with CTRM, they have identified device failure mechanisms under surge current stress, during which the dynamics of heat spreading/ accumulation is revealed. Moreover, to enhance the heat dissipation during surge current stress, they have developed thermal management with a bonded diamond heatsink, which can further boost the surge energy density from 323 J/cm^2 (without diamond heatsink) up to 390 J/cm^2 in a 10-ms surge current test.

The ultrafast Tj mapping and thermal management techniques in this work are valuable towards high-ruggedness GaN devices for high-power and high-temperature power electronics applications.



The figures above show the (a) Challenge in ultrafast Tj monitoring during extreme stress transient (e.g., surge current/voltage, short circuit, etc). (b) Tj mapping platform featuring time-resolved CTRM with synchronously triggered surge current excitation circuit. (c) Time-resolved Tj in vertical GaN PiN diode during surge current up to 10000 A/cm^2. (d) Measured peak Tj at the centre and the edge of vertical GaN PiN diode during surge current stress transient.

Scientists make first gallium oxide pn diodes

New method uses standard industrial processes to achieve higher voltage, increased stability, and energy efficiency

RESEARCHERS at Nagoya University in Japan have created the first functional pn diodes using Ga_2O_3.
Their method '*P*-type layer formation study for Ga_2O_3 by employing Ni ion implantation with two-step oxygen plasma and thermal annealing' was published in the Journal of Applied Physics.

SiC-based Schottky barrier diodes are replacing silicon devices in inverter applications. However, high production costs due to SiC substrates being deposited by PVD and high device processing temperatures are barriers to increasing their market scale. SiC also faces another difficulty in that it tends to degrade when used in bipolar pn junction devices.

Ga_2O_3 is a potential alternative because it is less expensive to produce than SiC as a result of its compatibility with melt-growth methods such as the film-fed growth or Czochralski method. Schottky barrier diodes based on Ga_2O_3 are under development; however, practical bipolar pn diodes have not yet been achieved.

The problem is that Ga_2O_3's crystal structure easily accepts the atoms needed to create n-type layers but rejects the atoms required for p-type layers. Previous methods to force them in either failed or required temperatures that destroyed the material. Without both types working together, Ga_2O_3 remained limited for practical applications.

To address this, the researchers injected nickel atoms into the Ga_2O_3 layer by shooting individual atoms at high speed into the surface of the material. They then heated the material twice, first at 300°C with activated oxygen radicals (oxygen atoms that have been given extra energy using proprietary plasma treatment) and then at 950°C in oxygen gas. This converted the embedded nickel into nickel oxide and properly integrated it with the Ga_2O_3 crystal structure.

"Since this method uses standard industrial equipment and processes, it can be scaled up for mass production," Masaru Hori from the Center for Low-Temperature Plasma Sciences at Nagoya University highlighted. "The implications for future energy efficiency and costs are substantial, particularly for electric vehicle and renewable energy industries."

Nagoya University spin-off company NU-Rei is now working to bring these advances to market.

Pictured above: Illustration of the new fabrication process: ion implantation of nickel atoms, followed by low-temperature plasma treatment and high-temperature annealing (heating) to create stable p-type layers in Ga_2O_3.

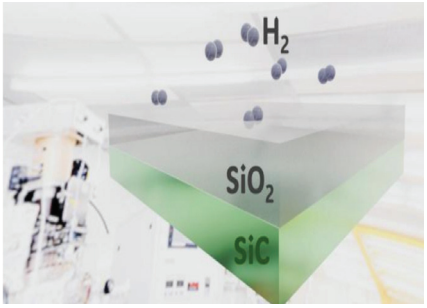
Novel annealing process improves SiC devices

RESEARCHERS at the University of Osaka in Japan have developed a novel technique to enhance the performance and reliability of SiC MOS devices.

This breakthrough uses a two-step annealing process involving diluted hydrogen, to eliminate unnecessary impurities and significantly improve device reliability.

SiC power devices offer superior energy efficiency compared to traditional silicon-based devices, making them ideal for applications like electric vehicles and renewable energy systems.

However, previous attempts to improve SiC MOS device performance relied on introducing impurities like nitrogen, which unfortunately compromised



reliability and limited operating voltage range.

This necessitated strict gate drive design, hindering wider adoption.
The team discovered that a two-step high-temperature hydrogen annealing process, performed before and after gate oxide deposition, could drastically improve both performance and reliability without the need for these problematic impurities.
This process effectively removes defects at the oxide/SiC interface, resulting in a lower interface state density and higher channel mobility. The devices demonstrated improved immunity against both positive and negative bias stress, expanding their operational voltage range.

"SiC MOS devices, despite being in mass production, haven't yet reached their full potential in terms of performance and reliability," explains Takuma Kobayashi, the lead researcher. "Our findings offer a solution to this long-standing challenge and open up exciting new possibilities for SiC power devices. We overcame many hurdles during this research, and I'm grateful to all my co-authors for their contributions."

NREL team constructs record-beating SiC module

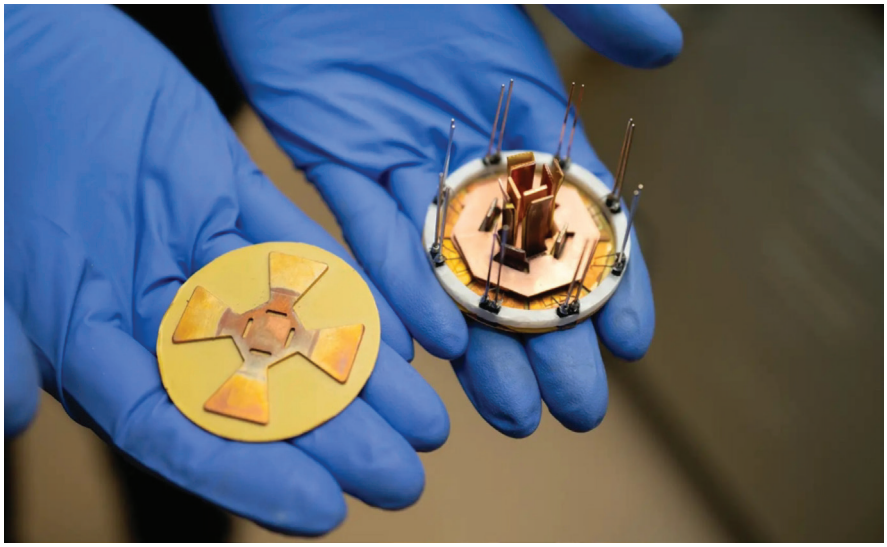
Ultra-Low Inductance Smart (ULIS) module can achieve five times greater energy density than predecessor designs

NREL has developed an Ultra-Low Inductance Smart (ULIS) SiC power module with a parasitic inductance seven to nine times lower than any current state-of-the-art SiC power module.

The 1200V, 400A module is capable of achieving five times greater energy density than predecessor designs in a smaller package, making it possible for to build and power more efficient, compact, and lighter technologies for applications such as data centres, power grids, microreactors, and even heavy-duty vehicles such as next-generation aircraft and military vehicles.

"We consider ULIS to be a true breakthrough," said Faisal Khan, NREL's chief power electronics researcher and the principal investigator for the project. "It's a future-proofed, ultrafast power module that will make the next generation of power converters more affordable, efficient, and compact." Furthermore, Khan explained, ULIS is uniquely suited for high-intensity applications, like aviation and military operations, because the powerful, lightweight module also monitors its own state of health and can predict component failure before it occurs.

Unlike a typical brick-like power module, ULIS winds its circuits around a flat, octagonal design. The disk-like shape allows more devices to be housed in a smaller area, making the overall package smaller and lighter. At the same time, novel current routing allows for maximum magnetic flux cancellation, contributing to the power module's clean, low-loss electrical output—in other words, its ultrahigh efficiency.



"Our biggest concern was that the device switches off and on very quickly, and we needed a layout that wouldn't create a chokepoint within the design," said Shuofeng Zhao, an NREL power electronics researcher who designed ULIS' flux cancellation architecture. One of the original layouts, Zhao said, looked like a flower with a semiconductor at the tip of each petal.

Another idea was to create a hollow cylinder with components wired to the inside. Sarwar Islam, another NREL power electronics researcher on the ULIS team, came up with the 2D structure, which made it possible to build the module balancing complexity with cost and performance.

"We squished it flat, like a pancake," Zhao said, "and suddenly we had a low-cost, high-performing design that was much easier to fabricate."

Where conventional power modules rely on bulky and inflexible materials, also ULIS takes a new approach. Instead of dissipating excess heat by bonding copper sheets directly to a ceramic base, ULIS bonds copper to a flexible polymer, called Temprion, to create a thinner, lighter, more configurable design.

Because the material bonds easily to copper using just pressure and heat, and because its parts can be machined using widely available equipment, ULIS can be fabricated quickly and inexpensively, according to the NREL team. Manufacturing costs total hundreds, rather than thousands, of dollars.

A further breakthrough allows ULIS to function wirelessly, as an isolated unit that can be controlled and monitored without external cables. A patent for this low-latency wireless communication protocol is pending. ULIS can scale to accommodate advancements in semiconductor devices using SiC, GaN, and even gallium oxide.

Our biggest concern was that the device switches off and on very quickly, and we needed a layout that wouldn't create a chokepoint within the design

UK can lead modern grid technology, says new report

UK's CSA Catapult highlights potential of solid-state transformers in providing a more intelligent and flexible energy grid

THE UK has all the ingredients to take advantage of a promising new semiconductor technology that will make our energy grids smarter, more reliable and less prone to blackouts, according to a new report published by Compound Semiconductor Applications (CSA) Catapult.

Solid state-transformers (SSTs) are an advanced type of transformer that use power electronics and high-frequency components to convert and control electricity.

They are extremely useful for integrating renewable energy sources and energy storage systems into the grid, as well as managing surges and disturbances, reducing the likelihood of blackouts.

In April this year, a major blackout occurred across Spain and Portugal, disrupting power for more than 10 hours and causing economic losses of an estimated $1.6 billion.

Compound semiconductors such as SiC and GaN, are the material of choice for this application as they can handle higher voltages, operate at higher frequencies, and perform better at higher temperatures.

Even though SSTs are still a nascent technology, the SST market is projected to grow at a double-digit compound annual growth rate (CAGR) through to 2030. Similarly, the market for SiC power devices is expected to grow at over 20 percent CAGR over the same period. The total global investment in power grid technology was projected to peak at nearly $400 billion in 2024, whilst global spending on renewables hit a record $735 billion in 2023.

In the UK alone, there are over 500,000 substations that could benefit from

new SST upgrades. Between 2020 and 2023, over 100,000 traditional dielectric transformers were sold in the UK, generating over £90 million in revenue. Compared to traditional transformers, SSTs are much smaller and lighter, better at regulating voltage and more flexible—they can also convert between AC and DC electricity and help send electricity back into the grid.

Outside of the energy grid, SSTs can also be used to manage power in EV chargers, data centres, and electric rail, marine and aerospace applications. SSTs will modernise EV charging by providing compact, efficient systems that support high-power, ultrafast charging solutions and a seamless link into renewable energy sources. Global companies are already developing SiC-based SSTs that can achieve up to 96.5 percent efficiency and reduce carbon footprint by 40 percent, weighing up to 70 percent less.

The report estimates that between 300,000 and 800,000 EV charges could be installed in the UK by 2030, providing a market opportunity of between £570 million and over £4.5 billion.

To overcome the hurdles facing the commercial development of SSTs, the report calls for a more coordinated between academia, industry, and government, improved funding and regulatory frameworks, and the development of large-scale pilot projects to test the technology in the real world.

Nick Singh, chief technology officer at CSA Catapult said: "As the energy landscape evolves and we introduce more renewables into the grid, SSTs have the potential to modernise our infrastructure and transform the way we move electricity around the system.

"Their ability to integrate seamlessly with distributed energy resources, bidirectional power flow, and real-time monitoring will place them at the heart of smart grids and create a whole host of new and advanced applications.

"The UK is in a strong position to take this technology forward with a flourishing power electronics and compound semiconductor ecosystem that is needed to take this technology from concept into real world applications."

ORNL team develops fast circuit breaker for the modern grid

Medium-voltage thyristor-based circuit breaker could help reduce future electricity costs and expand capacity

RESEARCHERS at the US Department of Energy's Oak Ridge National Laboratory (ORNL) have developed medium-voltage solid state circuit breakers capable of handling increasing levels of direct current at a lower cost, an advance that can help reduce future electricity costs and expand capacity in an overburdened US grid.

"The lack of medium-voltage circuit breakers for direct current has been an obstacle to flexibility in delivering electricity," said Prasad Kandula, lead researcher. "Developing this technology helps keep the grid working safely and reliably while keeping more energy available to support our growing population and economy."

"Once you go to DC, that 'zero current' moment is gone — and without it, a mechanical switch isn't fast enough to stop a fault before heat builds up and a fire starts," said Kandula, who leads ORNL's Grid Systems Hardware group. To tackle this problem, ORNL researchers are designing and scaling up the capacity of a seminductor-based circuit breaker, which can operate a hundred times faster than mechanical switches. This enables wider use of DC in the electric grid as it becomes more attractive to energy system designers for its efficiency, flexibility and compatibility with modern energy sources and loads.

Until now, semiconductor breakers have been too expensive to either compete economically with mechanical breakers for AC, or to facilitate expanded use of DC grids. No type of commercial breaker can handle DC above 2,000 volts, and most can't achieve half that. Kandula and his team set out to find a cost-effective solution and chose a thyristor. Thyristors cannot be directly 'switched' off, so the team also had to design an external circuit

➤ Prasad Kandula and Marcio Magri Kimpara set up testing of ORNL-developed medium-voltage circuit breakers

to forcibly reduce the current. In ORNL's Grid Research Innovation and Developmentcentre, or GRID-C, engineers built and tested a circuit breaker prototype to interrupt a current at 1,400 volts in less than 50 microseconds – four to six times faster than had been demonstrated with thyristors previously.To prove the technology could be scaled up to handle higher voltages, researchers connected the breakers in a series. This approach comes with several technical challenges: First, the voltage must be shared evenly across all breakers, to prevent any single device from becoming overloaded and failing. Second, creating a series of breakers must not delay the system's rapid reaction time.

ORNL researchers designed solutions and tested them in a series of breakers operating up to an 1,800-volt testing capacity. They are already working on adding to the series for eventually scaling up to 10,000 volts, anticipating the larger energy demands of future DC grids. The project is part of a larger ORNL initiative to develop a menu of stackable medium-voltage building blocks for expanding new power applications in U.S. transportation, manufacturing and data centres.

UW-Madison opens ultra wide bandgap lab

THE University of Wisconsin-Madison has opened an Ultra-Wide Bandgap Semiconductor MOCVD Laboratory, a facility that will focus on the emerging class of ultra wide bandgap III-nitride semiconductors such as AlGaN and AlN.

At the moment, fabricating and characterising ultra-wide bandgap semiconductors is challenging because they require expensive equipment and deep expertise in MOCVD or other advanced commercialisation- friendly deposition techniques.

Shubhra Pasayat (pictured above centre), who oversees the new facility as the lab's principal investigator, set up a commercial Aixtron MOCVD reactor for research when she first joined UW-Madison in 2021.

The new facility takes this to the next level with an Agnitron Agilis 100 system that can handle higher temperatures and lower pressures.

This will allow Pasayat and her students to design and precisely synthesise high-quality two-inch diameter wafers of high-aluminium content ultra-wide bandgap materials.

The lab is described as being at the centre of UW-Madison's rising III-nitride ecosystem. The onsite faculty's broad expertise in chip design and architecture, materials characterisation, fabrication, advanced packaging, and systems integration means these ultra-wide bandgap semiconductors can go from the drawing board to the motherboard all on one campus – streamlining and improving the research process.

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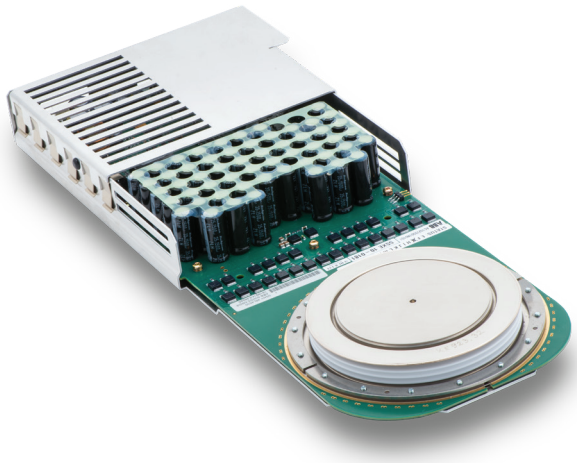

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How AI will drive growth in Power Semiconductors, from the (data) centre to the edge

The industry is facing a challenge to keep up with the ever-evolving demands of the big AI players. This is a challenge we should all embrace.

BY CALLUM MIDDLETON, PRINCIPAL ANALYST: POWER SEMICONDUCTORS AT OMDIA

THE ONE certainty that seems to come with AI is that it will change the world around us in uncertain ways. Beyond the chatbots that many now interact with daily, AI is being applied in unseen ways to improve efficiencies in processes as mundane as planning applications and as exciting as drug discovery.

Taking the former example, local councils in the United Kingdom have been using AI to scan and analyse historical planning documents which were typically handwritten and contained hand-drawn sketches.

The AI tools then produce digitised copies, which can be easily queried and cross-compared against other documents, speeding up decision making. What took two hours, now takes 3 minutes.

If all of this seems incredibly dull, that's probably because it is! When people imagine the AI future they often picture a dystopian world of miracle drugs and humanoid robots moving through neon drenched metropolises, but not necessarily how efficient the planning process must be to achieve that future. The reach of AI will go far beyond the headlines.

There is currently a very significant build out in data center capacity to allow for AI to touch as many applications as possible. Data centers are critical in the training of foundational AI models. These models form the basis of AI capability and new generations are often the result of months or even years work of development. Training foundational models is incredibly energy intensive, using the latest generations of GPUs and huge amounts of data.

Once these foundational models have been trained, secondary level models can be developed which provide the utility. They can be optimised for different applications whether that is through training on specific datasets, or for optimising efficiency. They can be specific to certain fields or certain companies and are often also trained in data centers via the cloud, although it is also possible to achieve this through servers located at the edge.

The final rung in the ladder is inference - how we all interact with AI regularly. This may be by asking questions of a chatbot, generating an image, or analysing data. This is the least computationally intensive aspect of the process and can be performed in the cloud (i.e a data center), or at a secure edge server.

Secondary models can be designed to be loaded and compute at the extreme edge, such as on a phone or laptop, allowing for no data transfer, improved security, and personalisation.
This spectrum of energy usage, from the beating heart of foundational training to the capillaries of inference at the edge will be demanding. The challenges will be different but the fundamental nature of one those challenges, how do we do this as efficiently as possible, will remain

consistent. Power semiconductors of all flavours will have a part to play.
Data centers have been constrained by what came before. Prior to the launch of ChatGPT in November 2022 very few server racks operated at above 30 kW. From 2023 onwards 50 kW became the baseline for an AI server rack operated by the likes of Meta, AWS or Oracle. Google pushed things to 100 kW, and the race to higher power continues.

To meet the need for rapid deployment these AI server racks were often upgraded versions of traditional racks and new infrastructure was based on existing standards. Two core architectures were used, one with dedicated AC-DC power supplies in each shelf of the rack, and one with a shelf housing all AC-DC power supplies and a bus taking power to neighbouring shelves containing compute functions. To increase the power in a rack it is possible to use more power supplies, but this is not desirable as it takes away precious compute space.

The alternative is to increase the power density of each power supply – an approach that brings power semiconductors to the forefront. Prior to ChatGPT, a standard form factor power supply rated at 3.3 kW was considered high performance, with 5.5 kW representing the cutting edge. As of time of writing, reference designs are available for power supplies at 8 kW and even 12 kW levels in the same form factor, representing a more than doubling of power density.

This can only be achieved through the adoption of wide bandgap semiconductors. Both silicon carbide and gallium nitride have their advantages. Silicon carbide can be used effectively in totem pole configurations in the PFC front end of the power supply. GaN is suited to resonant LLC converters in the back end. Whilst it is possible to just use one of these materials, using both in concert delivers the highest performance.

Eventually, this process of upgrading existing infrastructure and designs will reach its limit. A step change is required and this has been outlined by Nvidia who have suggested that data centers should use a high voltage (800 V, +/- 400 V) DC bus with power supplies replaced by a sidecar – an entire rack dedicated to converting voltage to an intermediate 48 V DC bus which is taken to the server racks. This provides three options for wide bandgap power semiconductors – silicon carbide in solid state transformers to achieve the 800 V DC bus, silicon carbide or gallium nitride in the sidecar to convert to the 48 V DC bus, and then gallium nitride in conversion of 48 V to 12 V or to point of load.

Wide bandgap semiconductors have gone from complementary to cornerstone. It is no coincidence that Nvidia, when naming their semiconductors partners for future data center architectures, referenced leaders and specialists in silicon carbide and gallium nitride devices. Beyond power density, wide bandgap-based data center power distribution will reduce running costs.

This positive story comes at a critical time for the power semiconductor industry. Omdia finds that revenue from discrete power components dropped by 9.9% in between 2023 and 2024. For power modules this drop was 5.0% and for power IC's it was 3.5%. The post pandemic period gave several years of growth kick started by spending on home work and entertainment during lockdown periods and was then powered forward by renewable energy and electric vehicles. Investment poured into the industry, but as these applications faltered one by one, the classic semiconductor cycle appeared. Over-capacity occurred, inventories built up, and several components faced severe ASP pressure.

There are signs that inventories are being digested, and demand is picking back up. For the most part wide bandgap semiconductors managed to withstand the headwinds in the wider market. However the emergence of a dynamic growth market is certainly welcome. Silicon carbides rise has been closely tied to the EV industry whilst gallium nitride has been not expanded beyond power adaptors as rapidly as expected.

Whilst the numbers for data center investments are eye-catching, it is worth providing perspective. The compute components within the server are absorbing an ever-greater proportion of the investment and all systems are becoming more complex. At Omdia we have estimated that demand for high voltage (600-1200 V) devices for AI data centers can hit 120-150 million shipments by 2030, made up of a mixture of silicon carbide, gallium nitride, and silicon solutions. Based on current forecasts this is expected to be an order of magnitude lower than the equivalent shipments in electric vehicle applications, which is the market that will dominate power semiconductors in the future. Data centers provide a high-quality secondary market that aids diversification and pushes innovation.

Some worry that once the next big foundational models are trained, the demand for compute will dry up and with it the demand for high performance power distribution. However as discussed earlier there is always another rung on the ladder of AI. Compute is a scarce resource and so will be quickly distributed to secondary models or inference applications, increasing the reach of AI and making it more affordable.

Away from the data center, the main target for improving efficiency in edge AI is within the models themselves. High performance power management ICs will be needed to ensure power is delivered when and where it is needed. The biggest impact will be in convincing consumers to part with their hard-earned cash. With many countries facing cost-of-living difficulties, and many consumers having upgraded their tech during the pandemic, the refresh time on items such as phones and laptops has been getting longer and longer.

Power semiconductor manufacturers should use data centers as their moonshot. Developing devices that can match the incredible demands placed here will surely mean better devices across a range of complimentary applications. EVs may provide the scale, but partnering with and suppling the likes of Nvidia will add to brand recognition and value.

Much like those hyper efficient planning decisions we are promised, power semiconductors are essential if not celebrated. The industry is facing a challenge to keep up with the ever-evolving demands of the big AI players. This is a challenge we should all embrace.

➤ Dresden cleanroom, 300 mm cleanroom at Infineon Dresden's existing site. [Infineon]

Infineon reports strong earnings as Smart Power fab advances

Rising power semiconductor revenues boost Infineon while Dresden expansion heads towards 2026 production.

BY REBECCA POOL, TECHNOLOGY EDITOR

AMID geopolitical turbulence from US tariff concerns, Germany-based chipmaker Infineon recently raised its profit outlook. In the company's Q3 earning call, CEO Jochen Hanebeck, noted that rising revenues in Green Industrial Power and Power & Sensor Systems segments, in particular, delivered strong quarterly earnings.

According to Hanebeck, key applications such as power infrastructure, renewable energy, as well as automation and drives contributed to 'sequential improvement'. Meanwhile rising demand for energy-efficient power semiconductors in AI servers for data centres also drove growth.

Hanebeck also revealed how Infineon's semiconductor modules will be used in a China-based power project combining large-scale, 400 MWh energy storage with photovoltaics to supply around 270,000 homes. And he noted Infineon's recent collaboration with Nvidia to develop 'the industry's first' 800V high-voltage, direct current power delivery architecture for AI data centres.

"In a very volatile environment, Infineon has again produced sound results," he said. "Semiconductor markets are recovering slowly from a long downturn... that affected different markets at different times, [but] there are signs of an upward trend at last." "Because of US tariffs, customers are ordering at short notice and we are seeing inventories being built up – so we're also encountering a headwind for our business development," he added.

Dresden expansion

Buoyed by the strong quarterly earnings and following final approval from the German government, Infineon is now pressing ahead with its long-term plan to construct a Smart Power Fab in Dresden. The facility,

> "The Smart Power Fab is more than just a construction project – it is a strong commitment to Dresden as a location and to the future of European microelectronics."
>
> **Infineon Dresden Site Manager, Raik Brettschneider**

designed to produce 300 mm silicon-based wafers, is intended to meet the growing demand for analog/mixed-signal technologies and power semiconductors across renewable energy, data centre, and electromobility applications – the same sectors driving Infineon's latest results. Public funds total €1 billion, coming from the European Chips Act and EU's important project of common European interest in microelectronics and communications, while Infineon is investing more than €5 billion in capital at the site.

In a recent update to Power Electronics World, Infineon confirmed shell construction is complete, with the first tools to be brought online soon. Production is set to start during 2026 and ramp according to market demand. While traditional fabs can take weeks or even months to reconfigure product lines, the company also also highlighted that innovative prediction systems in the Smart Power Fab promise to enable technology changes in mere days.

"Close and trusting cooperation with the authorities, politicians and our partners has been and remains a key factor in the impressively rapid implementation of this gigantic project," commented Infineon Dresden site manager, Raik Brettschneider.
Once up and running, the new fab is expected to create around 1000 highly-qualified jobs. It will also be closely linked to Infineon's Villach site, home to 300 mm wafer production, which the company says will give it the flexibility to very quickly supply chips to customers.

But it's not just about manufacturing chips. The Dresden expansion will undoubtedly contribute to the European Commission's objective of reaching a 20 percent share of global semiconductor by 2030, as part of the Chip Act. Indeed, Infineon itself is clear that the new fab will be critical to strengthening the European semiconductor supply chain.

Infineon has claimed that every third chip in Europe is already manufactured at its existing Dresden site, and the expanded fab will better help to secure value chains in the key European industries – with its ability to react rapidly to market segment changes helping to ensure resilient supply. "The Smart Power Fab is more than just a construction project – it is a strong commitment to Dresden as a location and to the future of European microelectronics" says Raik Brettschneider

Staying strong

So as the Smart Power Fab in Dresden readies for production, the outlook for Infineon remains strong. In his recent earnings call, Hanebeck noted that 70% of its 2024 revenue related to power discretes and modules, based on silicon, silicon carbide and gallium nitride materials, as well as analog semiconductors and sensors, including smart power switches. And continued growth is expected.

Revenues for the September quarter are predicted to reach around €3.9 billion, equating to about 5% sequential growth, which as Hanebeck said: "[makes] our fourth quarter the strongest as usual." Hanebeck also pointed out how his company is "taking advantage of opportunities in strategic growth areas" including power supply solutions for AI data centers, rapidly increasing investment in energy infrastructure, and software-defined vehicles – strengthened by the firm's upcoming acquisition of Marvell's Automotive Ethernet business.
"In these areas, semiconductor demand is increasing in the long term," he said. "Infineon, with its portfolio... is ideally positioned to play a role in shaping these markets."

➤ Dresden cleanroom, 300 mm cleanroom at Infineon Dresden's existing site. [Infineon]

➤ Construction site of Infineon's Smart Power Fab in Dresden. [Infineon]

Reshaping gate drivers for next-gen electrification

As the need for higher performance, precision, and efficiency mounts, gate driver technology is becoming more essential than ever. Advancing the technology to overcome traditional limitations will be key to truly unlocking this next generation of electrification.

BY EMMANUEL ONYEMA, AUTOMOTIVE PRODUCT LINE MANAGER AT SKYWORKS.

INDUSTRIAL ROBOTICS and renewables applications are at the leading edge of electrification and automation, yet they are only as effective as their underlying power and control circuitry.

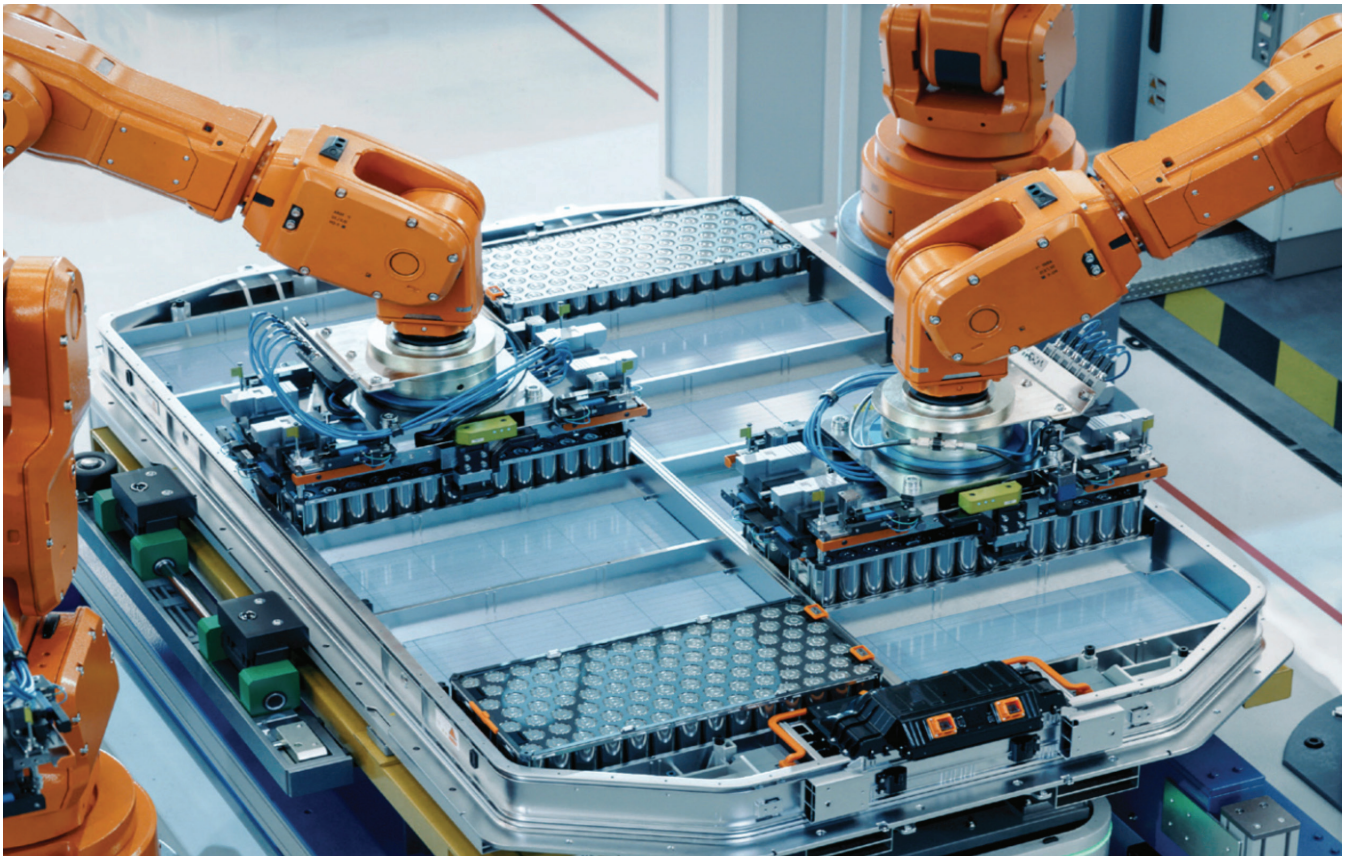
Reports suggest that the power electronics global market for EVs alone will grow at a CAGR of 17% from 2025 to 2035. Gate drivers play a pivotal role in meeting this sustainably, yet currently, traditional gate driver architectures face significant shortcomings in power loss and adaptability.

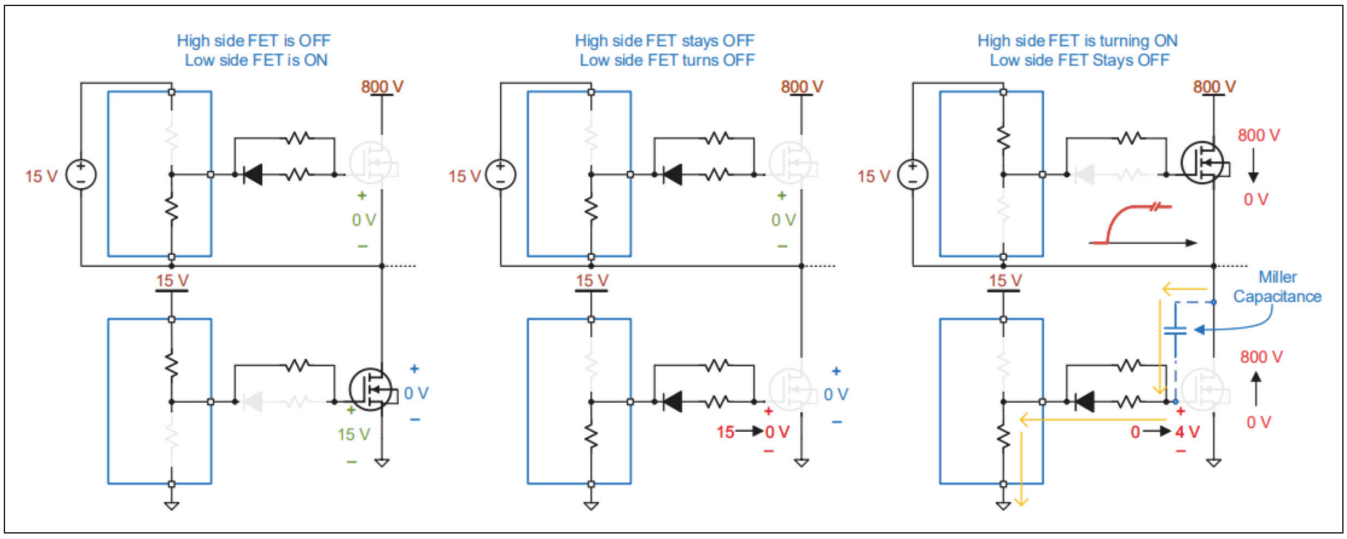
As the need for higher performance, precision, and efficiency mounts, gate driver technology is becoming more essential than ever. Advancing the technology to overcome traditional limitations will be key to truly unlocking this next generation of electrification.

What is a Gate Driver?

Taking a step back, power electronics circuits are responsible for controlling the movement of electrical current through a system, utilizing three components: power switches, called Field Effect Transistors (FETs); gate drivers and MCUs.

The FET specifically is responsible for enabling or disabling the flow of current, equipped with on/off switching





behavior. This allows it to turn on when gate voltage exceeds a certain amount and turn off when it falls below a certain amount. From there, the FET's gate acts as a sensor that builds up a charge to turn it on. The speed and strength at which the gate driver sends its control signal determines the efficiency of the FET and, in turn, the entire system. Meanwhile, the MCU is running the entire operation by providing signals to control the gate driver's movement.

Traditional Gate Drivers: Consistent but Inflexible

Traditional voltage mode drivers (TVMDs) have historically been the preferred architecture for engineers because they are simple. They function as a voltage source able to activate and turn off the FET quickly. However, the demands of modern power electronics today have revealed TVMD's limitations in performance and efficiency.

Take today's EVs, for example; onboard chargers often operate in varied conditions where the gate driver may need to adjust its behavior depending on temperature or output. With TVMDs, once the resistor values are set, they cannot be changed, hindering the ability to optimize currents for differing temperatures. This is a fundamental lack of flexibility in TVMDs that could mean significantly shorter battery range and slower charging. As demand for longer ranges and faster charging increases, automakers simply can't afford these operational shortcomings. Additionally, limits in slew rate, the maximum speed at which a voltage can change in a circuit, have become a great design consideration. Advanced gate driver designs are largely in two camps: high-current drivers that can handle more power but require careful resistor tuning, or multi-output drivers, which boost current capacity by splitting the load across multiple paths, thus improving switching speed but can be costly and complicate the design.

Each approach introduces its own unique set of benefits but also challenges: either a risk of oscillations or lower efficiency.

Outside of this, the Miller Effect, which is essentially the unintended electric charge caused by the small space between two circuit components, can trigger unintended FET turn-on and potentially result in system failure. When looking at the full picture, it's clear that power loss has become a major hurdle to overcome within the gate driver architecture. Next-generation applications require gate drivers that provide strong current, respond quickly and precisely to triggers, and are adaptable to different environmental setups. They also need to be highly resistant to electrical noise to ensure they work reliably in any environment, no matter what the strain. Leading industry players have integrated active Miller clamp functionality to suppress the unintended gate turn-on, which improves immunity against these events.

To address these challenges, the industry is tasked with creating an architectural solution that allows designers to select optimal drive profiles without external resistors, streamlines thermal and electrical tuning, and integrates active Miller clamp functionality to suppress unintended gate turn-on and improve immunity against DV/DT events.

Enter Current-Mode Controlled Gate Drive Solutions

Current-mode gate drive solutions may be the exact solution the industry is looking for. These updated architectures offer programmable gate current with a ±10% tolerance across PVT, enabling dynamic gate current control through SPD pin configuration,

Each approach introduces its own unique set of benefits but also challenges: either a risk of oscillations or lower efficiency. Outside of this, the Miller Effect, which is essentially the unintended electric charge caused by the small space between two circuit components, can trigger unintended FET turn-on and potentially result in system failure

matched to system conditions without discrete component tuning.

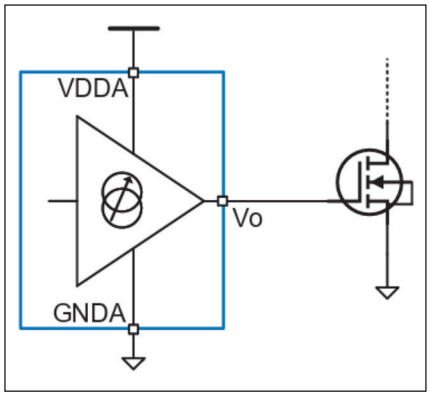
The technology offers features including programmable drive strength, which allows engineers to choose how fast or slow the switch turns. This balances the speed and efficiency necessary for different environments and tasks. Additionally, built-in protections like Miller clamps prevent accidental switching, i.e., the Miller Effect.

This is the type of flexibility needed in programming and power optimization, especially in applications like EVs, where power systems are exposed to harsh and varied conditions depending on weather, load variability, and temperature fluctuations. A current mode gate driver's ability to monitor and adjust its performance unlocks a level of system control that a TVMD would not be able to offer.

What's next?

While future integration paths are being explored, next-generation electrification technological advancements seem to be going in the direction of fully integrated gate drivers into the power switches, making systems smaller and more reliable. These drivers are set to support more automotive systems alongside industrial and renewable energy applications, with their greater adaptability to harsher temperatures and conditions.

Maintaining efficient switching performance across varying temperatures and supply voltages remains a common challenge in EV and industrial power systems. Technology like current-mode controlled gate drive addresses this by providing programmable gate current, which is configured via the SPD pin to tune drive strength per application need. This eliminates reliance on fixed external resistors and ensures consistent switching behavior across power, voltage, and temperature variations. Additionally, integrated features like active Miller clamp and



output discharge enhance robustness against noise and unintended turn-on, which streamline reliability under stress.

As power needs across the industry continue to accelerate, adaptive control will become a must-have in power electronics architecture. Having the ability to diagnose, control, and adjust your power systems will become the new normal for optimal performance, efficiency, and safety in EVs and all power electronics.

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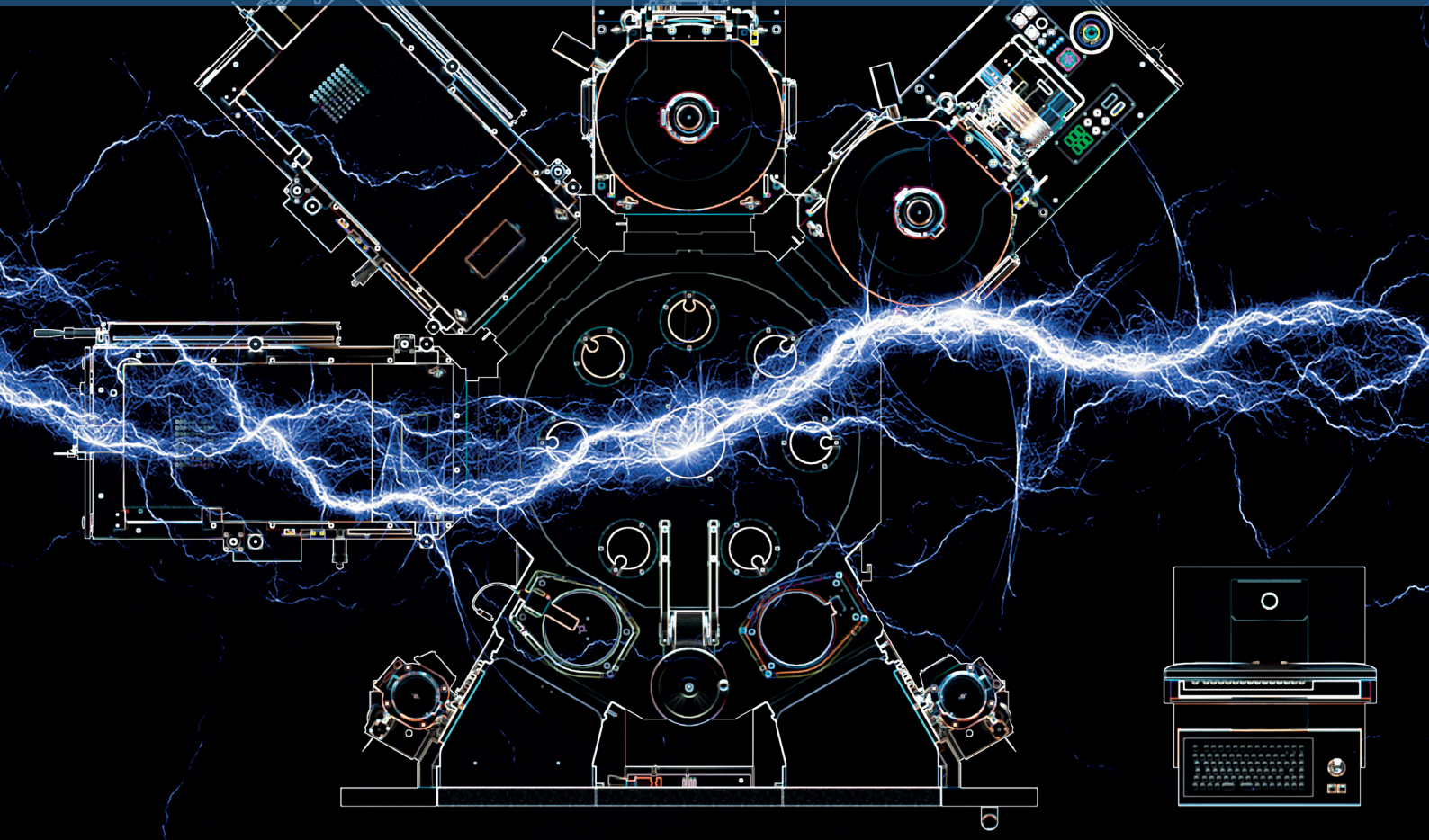

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Harnessing the sun: semiconductors in solar inverters

The shift toward GaN and SiC technologies not only improves the size, weight, and cost-effectiveness of solar inverters but also enhances their efficiency, potentially breaking through the 99% efficiency barrier.

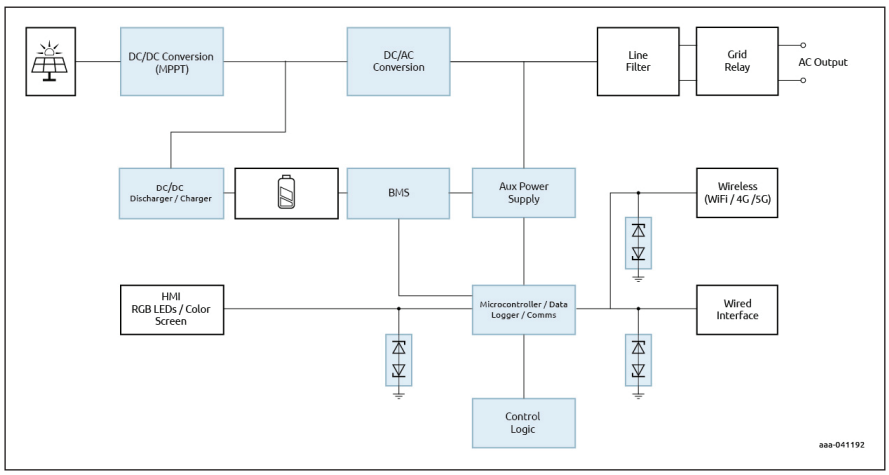
BY MATHIS FLANDRIN, GLOBAL BUSINESS DEVELOPMENT SPECIALIST, NEXPERIA.

ACCORDING to the International Energy Agency's (IEA) latest research, 77% of renewable capacity additions in 2028 will be solar energy, with an impressive 640 gigawatts (GW) of capacity added annually. As one of the most abundant and sustainable sources of power, solar energy harnesses the sun's energy and converts it into electricity using photovoltaic (PV) systems. At the heart of these systems is the solar inverter, a critical component that transforms the direct current (DC) generated by solar panels into alternating current (AC) suitable for use in homes and on the grid. Semiconductors play a pivotal role in the operation of solar inverters, and we explore their functions, benefits, and latest advancements.

Solar inverters are essential for the functioning of PV systems, acting as the bridge between solar panels and the electrical grid or home power systems. The conversion process involves two main stages:

- **DC/DC conversion stage:** where the Maximum Power Point Tracking (MPPT) algorithm optimizes the power output from the solar panels by adjusting the voltage to ensure maximum efficiency.
- **DC/AC conversion stage:** the optimized DC power is then converted into AC electricity, making it suitable for household use or feeding into the grid.

This dual-stage process ensures that the power generated by the solar panels is efficiently converted, minimizing energy losses and enhancing overall system performance.

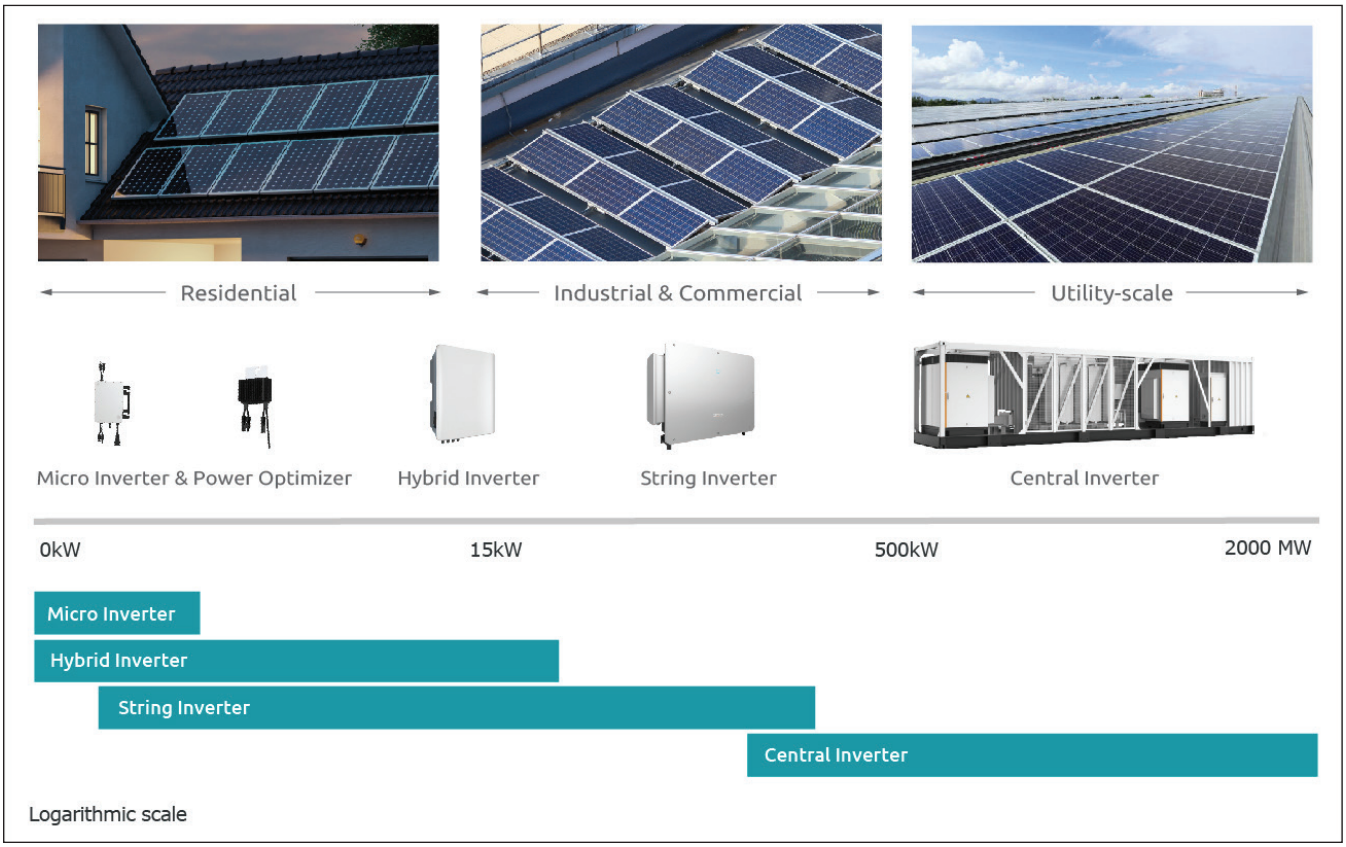


Simplified block diagram of a hybrid solar inverter.

Inverter topologies and functionality

Solar inverters utilize various topologies to achieve the best efficiencies, with two-level and three-level topologies being the most common. Two-level inverters, which are simpler and widely used in smaller systems, switch between two voltage levels to produce AC power. Three-level topologies provide a more refined output by introducing an additional voltage level, resulting in lower harmonic distortion, reduced stress on components, and improved overall efficiency. That makes them ideal for larger, more demanding solar systems. These topologies allow solar inverters to cater to a wide range of applications, from small residential setups to large-scale solar farms. To maximize the efficiency of the solar power system, inverters use Maximum Power Point Tracking (MPPT) algorithms, ensuring that the solar panels operate at their peak power output.

In grid-tied systems, inverters manage the interaction with the electrical grid, ensuring synchronization and safe operation, while also having the capability to shut down automatically during grid outages to protect utility workers. Additionally, modern inverters often come equipped with monitoring and communication features, allowing users to track their system's performance and receive alerts in case of issues, further enhancing the reliability and convenience of solar energy systems.



➤ Four main inverter types cover all installations.

Different inverters for different applications

Since photovoltaic installations come in different sizes ranging from small residential units to grid-tied solar power plants there are different types of inverters for every application case.

- The smallest inverter, mainly used for residential installations, is the micro solar inverter. Power conversion is performed at the individual PV panel level, and they can handle power from 200 W up to 3 kW. Having a microinverter on each panel allows MPPT per panel, resulting in higher efficiency and flexibility particularly in installations with shading issues.
- Another inverter commonly used in households is the hybrid solar inverter. These devices are designed to integrate solar electricity along with battery energy storage systems and EV charging infrastructure, managing all power conversion bi-directionally. To cover today's residential purposes, the current power range for hybrid inverters typically goes from 1 kW up to 50 kW.
- Often the preferred option for larger residential installations as well as commercial projects is the photovoltaic string inverter. This connects multiple panels in series (string) and converts the combined DC output into AC. These systems typically operate in a power range of a few kilowatts up to several hundred kilowatts.
- For the biggest utility and grid-tied solar projects one central inverter is at the heart of the solar power conversion process. These large box-shaped devices handle output power ranges from a few hundred to several thousand kilowatts.

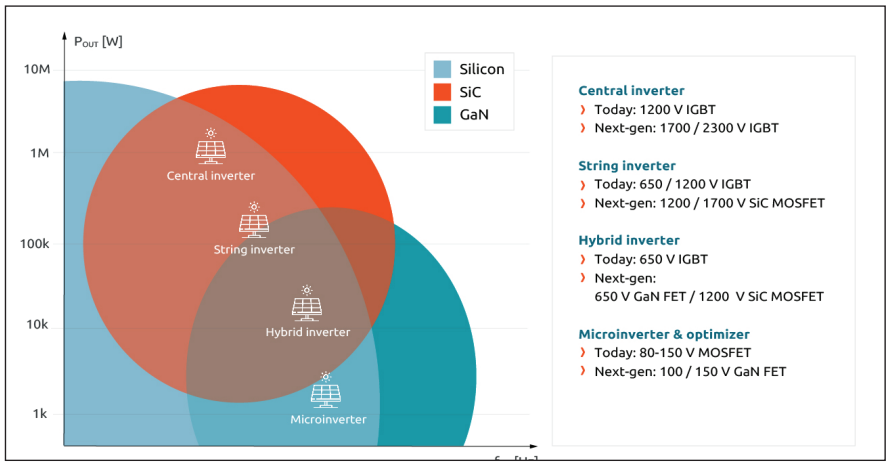
Semiconductors in solar inverters

Semiconductors are the backbone of solar inverters, playing a crucial role in the conversion and management of electrical energy within PV systems. Key semiconductor components like IGBTs, MOSFETs, diodes and bipolar transistors are integral to the inverter's operation.

- IGBTs are widely used in solar inverters for their ability to efficiently handle high voltages and currents, making them ideal for power conversion tasks. They offer the benefits of both high-speed switching and low conduction losses, which are essential for both MPPT and DC-AC conversion processes
- MOSFETs, on the other hand, are mainly employed in lower power applications within solar inverters due to their superior switching speeds and lower gate drive power requirements, which contribute to overall efficiency improvements, especially in smaller, high-frequency inverter designs.
- Bipolar Junction Transistors (BJTs) are vital in small signal control applications within solar inverters, where they ensure precise switching and amplification of signals, maintaining stable inverter operation by efficiently controlling low-level currents and voltages in various circuits
- Diodes, another critical component, facilitate the smooth flow of electricity by allowing current to flow in a single direction, preventing backfeed that could potentially damage the inverter and other connected components.

Wide bandgap a game changer

The introduction of wide bandgap (WBG) semiconductors, specifically Silicon Carbide (SiC) and Gallium Nitride



➤ Co-existence of power technologies addressing different solar inverters.

(GaN), has revolutionized solar inverter technology by offering significant advantages over traditional silicon-based semiconductors. GaN High Electron-Mobility Transistors (HEMTs) and SiC MOSFETs provide superior electrical properties, including lower on-resistance, faster switching capabilities, higher breakdown voltages, and the ability to operate at elevated temperatures.

These characteristics lead to significantly lower power losses, higher efficiency, and more compact designs due to reduced cooling and passive component requirements.

In solar inverter applications, especially in small-scale photovoltaic (PV) systems for homes and commercial buildings, GaN and SiC devices enable more efficient energy conversion and higher power densities. For instance, GaN-based designs, such as those using Nexperia's GAN041-650WSB, can achieve switching frequencies between 100 kHz and 300 kHz, which is a substantial increase compared to the 15 kHz to 30 kHz range of traditional IGBT-based solutions.

This increase in frequency allows for smaller and lighter output filters, reduced harmonic distortion, and an overall more compact and cost-effective design with power densities that have increased from 0.5 W/in^3 with IGBT modules to as much as 4 W/in^3 with the latest WBG devices.

In single-phase string inverter configurations, where PV panels are connected in series to generate a DC voltage, the higher efficiency of GaN and SiC technologies is critical. These configurations typically involve a DC/DC boost circuit controlled by a microcontroller or system-on-chip (SoC) that also manages maximum power point tracking (MPPT).

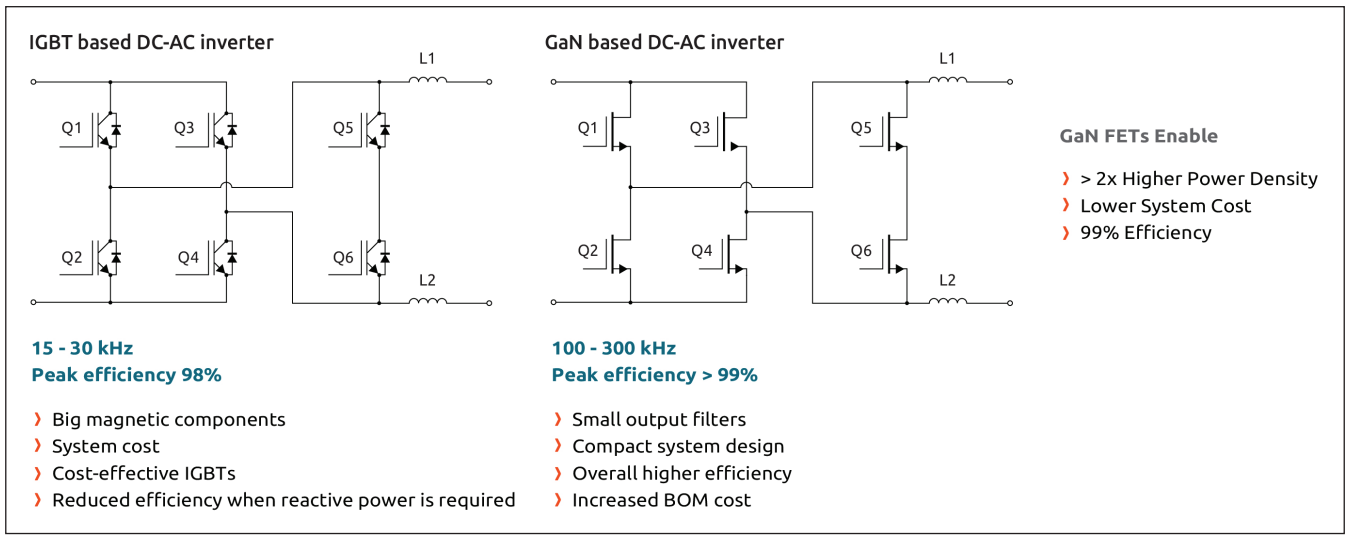
The output feeds DC link bulk capacitors, which can then supply power to an energy storage system (ESS) or a DC/AC inverter to provide single-phase AC for local use or the grid.

The future is bright for solar inverters
The shift toward GaN and SiC technologies not only improves the size, weight, and cost-effectiveness of solar inverters but also enhances their efficiency, potentially breaking through the 99% efficiency barrier.

This leap in performance makes solar energy systems more accessible and viable, ultimately lowering the total cost of ownership and paving the way for the next generation of highly efficient and resilient renewable energy solutions.

In the future, we can expect inverters to integrate even more advanced features like smart grid compatibility, enhanced monitoring, and AI-driven energy management. These advancements will enable greater energy optimization, accelerate response times, and improve integration with energy storage systems.

Further transforming the landscape for distributed energy generation and accelerating the transition to clean, efficient solar power. All enabled by advances in power semiconductor technology.



➤ Comparing IGBT-based and GaN-based DC/AC inverters.

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Wide-bandgap power semiconductor device dynamic characterisation

This article outlines the technologies and techniques required for performing dynamic characterisation of SiC and GaN power semiconductor devices.

BY RYO TAKEDA, SOLUTIONS ARCHITECT, KEYSIGHT

WIDE-BANDGAP (WBG) power semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), are rapidly replacing traditional silicon-based MOSFETs and IGBTs in a wide range of power-conversion applications, including electric vehicles, solar inverters, data center power supplies, and compact chargers. Its superior material properties (wide bandgap, high breakdown voltage, high electron mobility, and excellent thermal performance) enable higher switching frequencies, lower conduction and switching losses, and smaller passive components.

However, these benefits also come with new challenges such as extremely fast switching transitions (high di/dt and dv/dt) which intensify the effects of parasitic inductance and capacitance in test circuits, leading to waveform distortion, ringing, unintended turn-on events, and potentially damaging surge currents.

Accurate and repeatable dynamic characterisation is therefore a critical first step in designing robust power-electronic circuits using SiC or GaN devices.

Fundamentals of dynamic characterisation: The double pulse test

Both SiC and GaN devices are typically characterized dynamically using a double-pulse test (DPT). In this method, a half-bridge configuration of Field-Effect Transistors (FETs) is used, and two pulses are applied to the Device Under Test (DUT). When the first pulse is applied, the current begins to rise gradually due to the load inductor placed between the power supply and the DUT. The current increases linearly, with a rate inversely proportional to the inductance value. By adjusting the width of the first pulse, the target current for the switching event can be controlled. When the first pulse ends, the DUT turns off and can no longer conduct current. However, the current continues to circulate through the loop formed by the load inductor and the body diode (or freewheeling diode) of the high-side FET. When the second pulse is applied, the DUT turns on again, and current flows through it to the ground.

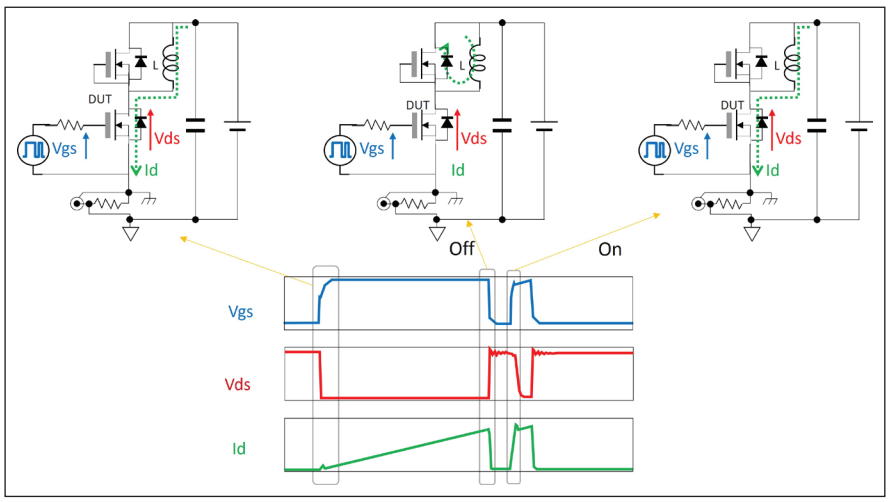


Figure 1: Double pulse test for switching characterisation.

This two-pulse sequence produces the waveform shown in Figure 1. The falling edge at the end of the first pulse corresponds to the turn-off characteristics, while the rising edge at the beginning of the second pulse represents the turn-on characteristics. In this way, both turn-on and turn-off switching behaviors can be conveniently captured in a single measurement.

Reverse recovery characteristics can also be measured using the double-pulse test. In this setup, the load inductor is connected between the neutral point of the half-bridge and ground. Two pulses are applied to the high-side device. By adjusting the width of the first pulse, the current is ramped up to the desired target value. When the first pulse ends, the high-side device turns off, and the current continues to flow through the loop formed by the load inductor and the body diode (or freewheeling diode) of the low-side FET. During this conduction phase, charge carriers accumulate in the PN or PIN junction of the diode.

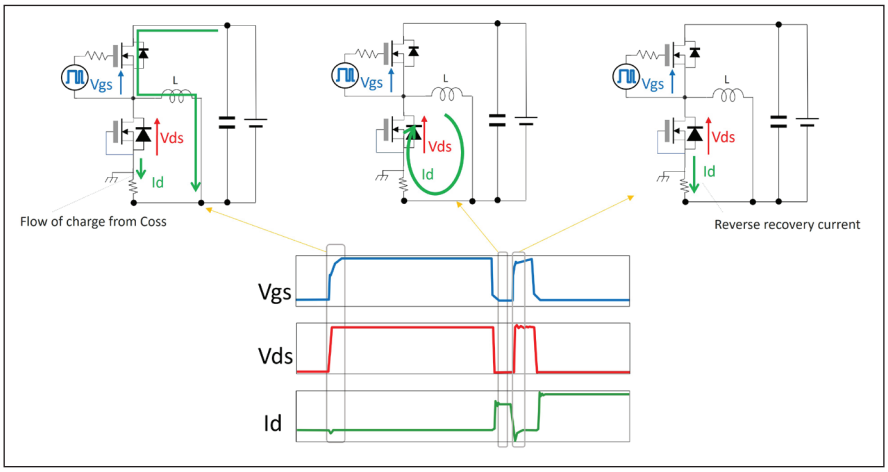
When the second pulse is applied to the high-side FET, the current commutates, abruptly turning off the diode. The stored carriers in the junction are released instantaneously and appear as a reverse-recovery

current, which is measured during this transition.

The DPT enables the capture of both turn-off and turn-on transitions in a single measurement cycle, making it a convenient method for quantifying switching losses (EOFF, EON) and reverse-recovery behavior. However, because SiC and GaN devices switch with sub-10 ns edges (or even sub-5 ns in GaN), parasitic inductance (Lpar) and capacitance (Cpar) in the test circuit, probes, and measurement equipment can introduce significant measurement errors such as:

- **Voltage Overshoot:** ΔV = Lpar·(di/dt) during turn-on or turn-off.
- **Current Spikes:** Ispike = Cpar·(dv/dt).
- **Ringing:** Fast switching edges interacting with parasitic can cause ringing.
- **Probe Skew:** Nanoseconds of timing mismatch between voltage and current probes can lead to inaccurate switching-loss calculations.

Minimizing these parasitics and ensuring sufficient bandwidth throughout the measurement is therefore essential for obtaining repeatable and reliable results.



➤ Figure 2: Double pulse test for reverse recovery characterisation.

Minimizing parasitics and ensuring measurement fidelity

PCB layout and power-loop inductance

When designing a PCB for a double-pulse test, maintaining a compact half-bridge layout is essential. Additionally, the forward and return current traces should overlap as much as possible to cancel mutual magnetic fields. A parallel-plane layout (i.e., placing the trace over a ground plane) helps reduce loop inductance (see Figure 3).

One key parameter that indicates the performance of the test system is the power loop inductance, which can be calculated using the following equation. Here, VDS,droop represents the voltage dip at the drain when the drain current (Id) ramps up. This value is easily derived from the turn-on waveform and provides a practical estimate of loop inductance—unlike source or drain stray inductances, which are more difficult to isolate individually.

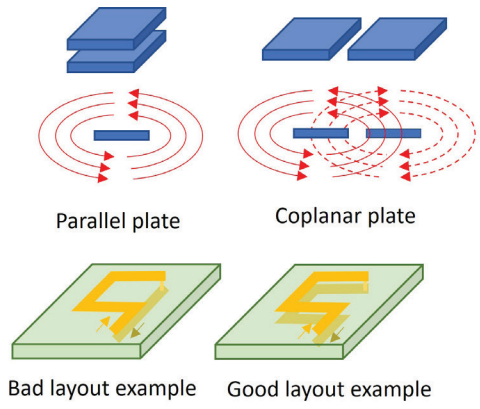
$$L_{powerloop} = \frac{V_{ds,droop}}{dI_d/dt}$$

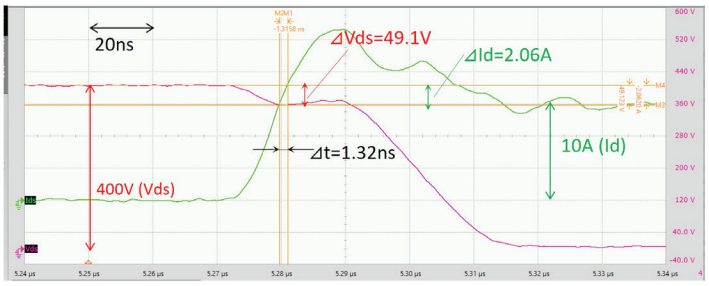
Oscilloscope and probe requirements

Because wide-bandgap (WBG) power devices have fast edge times—typically 8–15 ns for SiC and 2–5 ns for GaN—a bandwidth of 350 MHz or higher is required for the oscilloscope. In practice, a 500 MHz (or higher) oscilloscope is recommended for capturing the edges of both SiC and GaN devices. To ensure accurate waveform reconstruction, the sampling rate should be at least 5 to 10 times the highest frequency component. Therefore, an oscilloscope with a sampling rate of at least 5 GS/s is recommended. For voltage probes, it is advisable to use the same or higher bandwidth as the oscilloscope, since the overall system bandwidth is determined using the following equation:

$$system\ bandwidth = \frac{1}{\sqrt{\left(\frac{1}{BW_{probe}}\right)^2 + \left(\frac{1}{BW_{oscilloscope}}\right)^2}}$$

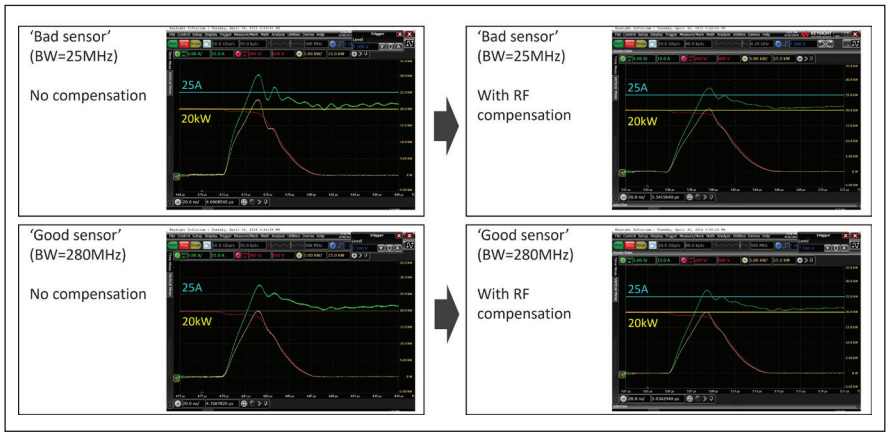
For the current sensor, since SiC devices can have edge times of approximately 8–15 ns and GaN devices as short as 2–5 ns, the sensor must capture frequency components up to at least the knee frequency (≈ 90 MHz for 8 ns edges, ≈ 350 MHz for 2 ns edges). To meet this requirement, coaxial shunt resistors are suitable for SiC, while even





$$V_{ds,droop} = L_{powerloop} \cdot \frac{di_d}{dt} \Rightarrow L_{loop} = \frac{\Delta v}{\frac{\Delta i}{\Delta t}} = \frac{49.1}{1.57 \cdot 10^9} = 31nH$$

➤ Figure 3: Layout example & power loop calculation.



➤ Figure 4: Id and power measured with different BW sensors (Left) and adjusted results with RF compensation (Right).

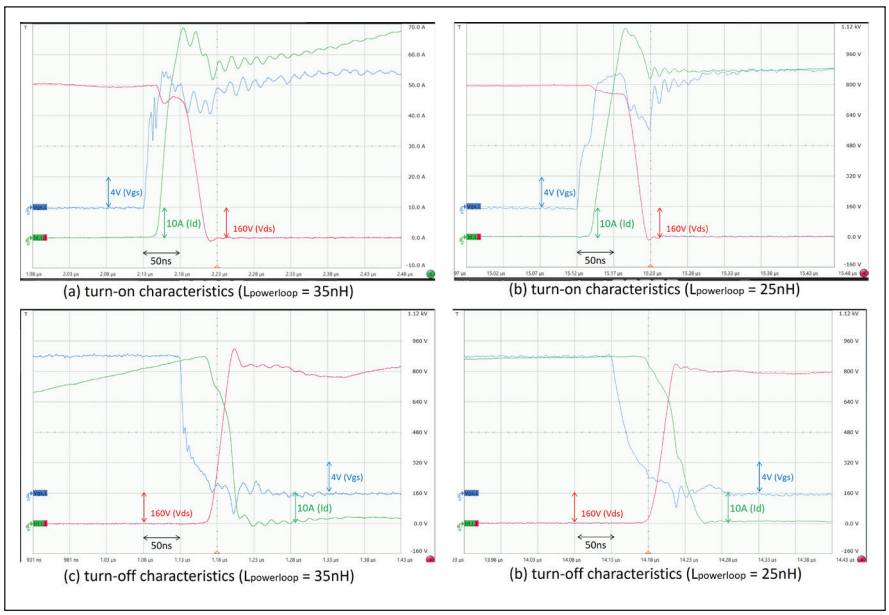
higher-bandwidth current sensors are necessary for GaN.

SiC power device dynamic characterisation

Characterising SiC devices presents a unique set of requirements compared to traditional silicon devices. Due to its high voltage and current capabilities and fast switching performance, both the test methodology and equipment need to be optimized to ensure accurate, repeatable results. The following sections outline the specific challenges and technological considerations involved in reliably testing SiC devices.

Unique challenges for SiC

- SiC MOSFETs often operate at voltages up to 1 kV and currents of several hundred amps. The test system must safely handle these levels while maintaining measurement fidelity.
- The combination of high di/dt and high dv/dt can couple through parasitic capacitance into the gate, causing unintended turn-on during turn-off. This results in large surge currents that can potentially damage the device or the test fixture.
- Although the double-pulse test injects minimal energy (due to short pulses), the device's high-power density requires careful safety mechanisms, including a robust safety enclosure and reliable discharge circuits.
- SiC power devices are available in various forms – not only in discrete packages, but also in power modules and even as bare chips from some manufacturers. A measurement approach that accommodates all these forms without compromising fidelity is essential.
- Temperature-dependent measurements are essential for power semiconductor devices because:
  - the junction temperature of these devices can reach high levels (e.g., 125 °C to 150 °C) during standard switching power supply operation, and
  - accurate device model parameter extraction requires characterisation at multiple temperatures.



➤ Figure 5: shows example measurement results for a SiC MOSFET with two different set up, DUT: Infineon IMW120R014M1H.

Heating capability during dynamic measurements is therefore critical. For power modules, often used in harsh environments, measurements at low temperatures (e.g., –40 °C) are also necessary.

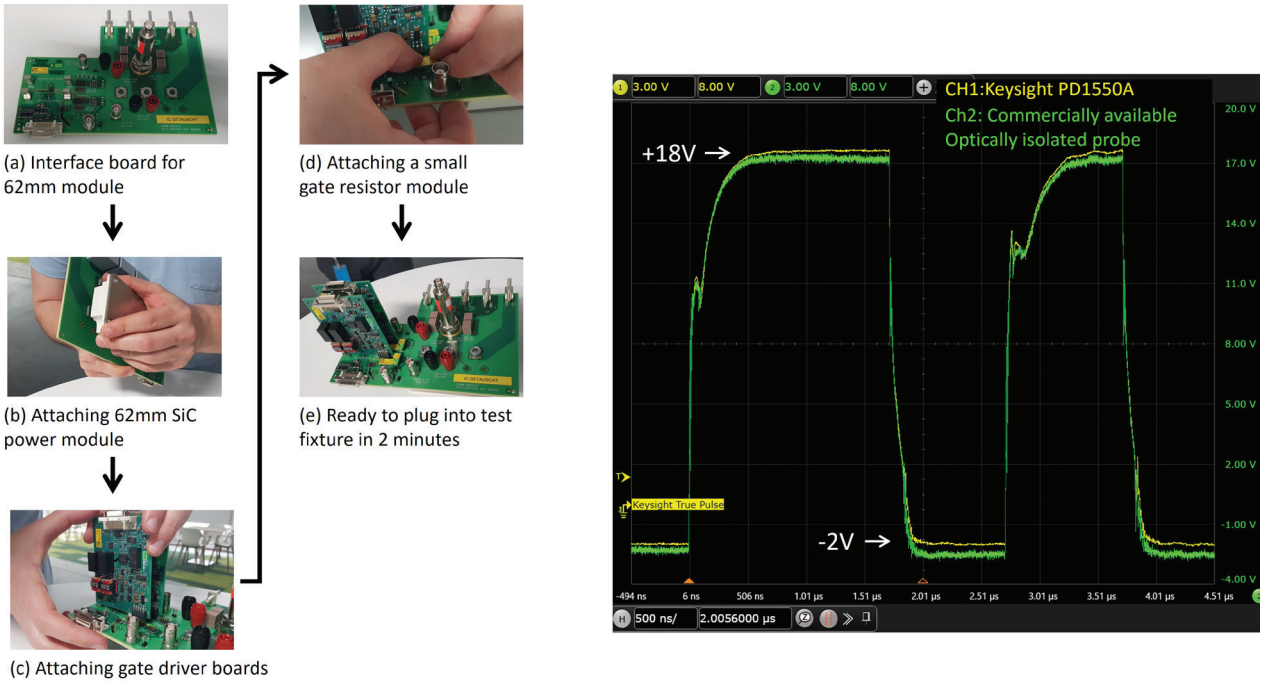
Key technologies for SiC device characterisation

The DPT system must be designed with sufficient voltage and current capacity while minimizing parasitics in the test circuit, and it must incorporate rigorous safety measures. These safety measures should include adequate redundancy to ensure both operator safety and the protection of test equipment.

Although coaxial shunt resistors with high bandwidth are suitable for SiC current measurement, commercially available coaxial shunt resistors do not always achieve the bandwidth specified in the datasheets due to production variations. In such cases, RF compensation, such as the method shown in Figure 4, can help improve measurement accuracy. This type of RF compensation requires precise S-parameter characterisation of each individual coaxial shunt resistor.

Two different DUT boards were used for the measurements. The graphs on the left were obtained using a DUT board with a power loop inductance of 35 nH, while those on the right were measured with a board having 25 nH. The measured waveforms are noticeably cleaner with the lower power loop inductance.

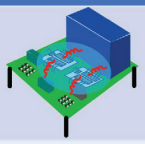
To accommodate various forms of SiC power devices, it is ideal for the DPT



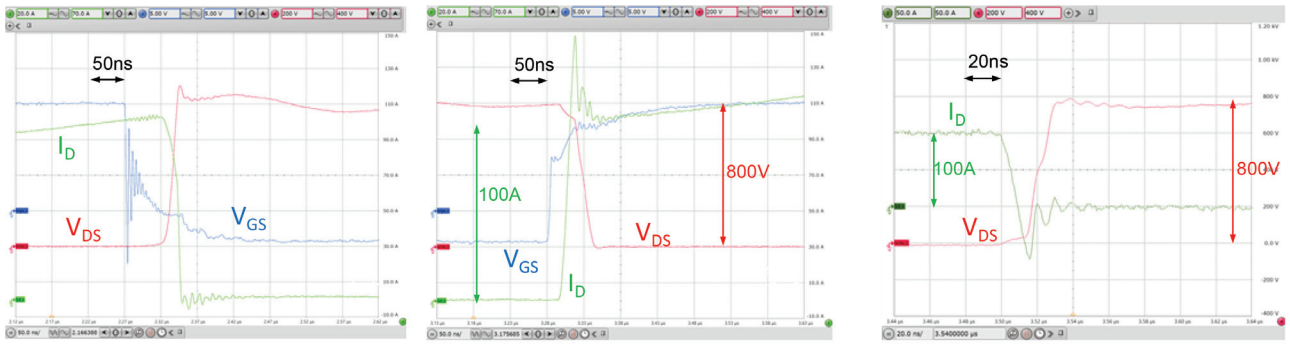
➤ Figure 6: Modular interface board and high-side V_{GS} measurement results (600V swing).

system to have a modular architecture. The DUT interface can be customized for different SiC device types and easily integrated into the modular DPT system. Such an architecture enables measurements for a wide range of package types, including 3-pin and 4-pin TO-247, surface-mount devices (SMDs), and even power modules such as 6-in-1 HybridPACKs. For power modules with half-bridge configurations, high-side gate voltage measurement is critical—but accurately capturing it is challenging due to the large voltage swing (e.g., 800 V) at the neutral point while measuring a relatively small V_{GS} voltage (e.g., 18 V). Figure 6 shows an example of a modular architecture, where a dedicated interface board is designed for the device under test while the rest of the test system remains unchanged. It also shows examples of high-side V_{GS} measurement results.

Another device form that has historically lacked a good contact solution is the bare chip. Despite various attempts to enable bare-chip dynamic testing, previous methods have been unsuccessful due to additional parasitics introduced by probe needles, the chuck used to hold the bare die,

Method	Probing with a wafer prober	Temporary Packaging	Direct mount to Test board	Keysight Solution
Image				
Vertical	NG	OK	OK	**OK**
Set up time	< 1 hour	> 1 week	> 1 month	**< 10 minutes**
Contact	Probing	Soldering/Bonding	Soldering/Bonding	**Solderless**
Parasitic inductance	Very High <1000nH	High ~ 40nH	High < 40nH	**Low < 10nH**

➤ Figure 7: Bare chip dynamic test solution comparison.



➤ Figure 8: SiC Bare chip measurement example. (800V, 100A), DUT: Wolfspeed SiC Bare chip: CPM3- 1200-0016A.

or bonding wires. The requirement for bonding itself also presents a major challenge. The only viable solution had been to create a special DPT board by soldering a bare chip, connecting it with bonding wires, and fully encapsulating the device with insulating material.

However, this method is still affected by the influence of wire bonding and supports only single-shot measurements. The board cannot be reused to test multiple SiC MOSFETs. A technology developed by Keysight is its bare-chip dynamic test method. Figure 8 shows example measurement results for a SiC MOSFET bare chip.

Another challenge in SiC dynamic characterisation is temperature-dependent measurement. Heating the DUT is relatively straightforward, ceramic heaters can be used for discrete devices, and hot plates for power modules. However, cooling a power module is more difficult. Using a thermostatic chamber is one option, but it typically requires a long time (e.g., up to 8 hours) to cool down and heat up the device.

Additionally, long cables routed into the chamber can degrade measurement quality. A viable alternative is to use a temperature forcing system, which rapidly delivers controlled hot or cold air directly to the DUT. A common issue with this approach is condensation forming on the DUT due to rapid temperature changes. A solution developed by Keysight addresses this problem, enabling reliable temperature-dependent measurements over a wide range—from –40 °C to +200 °C.

GaN power device dynamic characterisation

GaN devices are known for extremely fast switching behavior and compact packaging. While this enables significant performance benefits, it also demands careful test setup to avoid distortion and inaccuracy in measurement. The next sections describe the specific problems that arise when characterizing GaN devices and the techniques developed to overcome them.

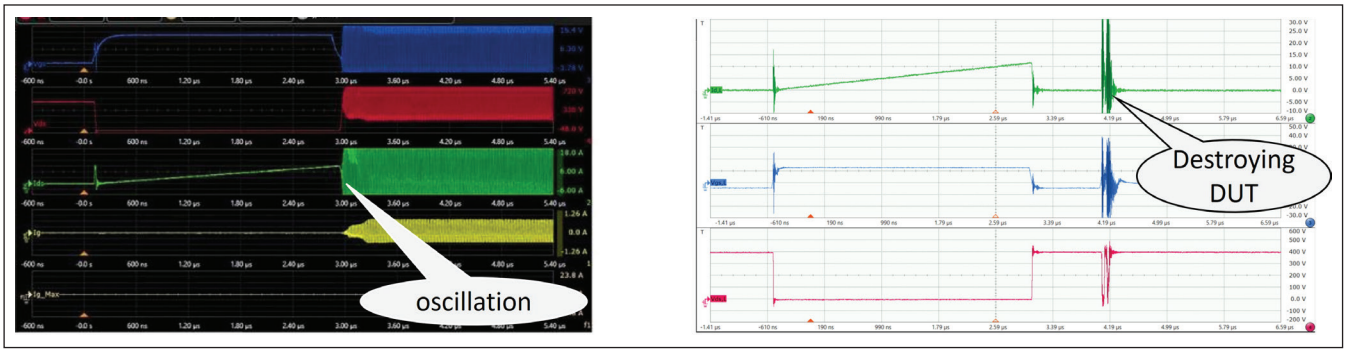
Unique challenges for GaN

- GaN HEMTs can switch in 2–5 ns, pushing parasitic-induced overshoot and ringing into the hundreds of MHz. In the case of cascode GaN HEMTs, ringing can trigger divergent oscillations, potentially leading to catastrophic device failure. It is extremely difficult to extract accurate switching parameters from waveforms distorted by such overshoot or ringing (see Figure 9).
- Many GaN devices are offered in very small surface-mount (SMD) packages (e.g., 8 mm × 8 mm, 1.5 mm × 2.5 mm) to minimize lead inductance. It is common practice to temporarily solder the DUT to the test board, as probing introduces parasitic inductance and spring contacts become more challenging with such small footprints. However, repeated soldering and rework can introduce variability, and the test boards are likely to degrade over time.

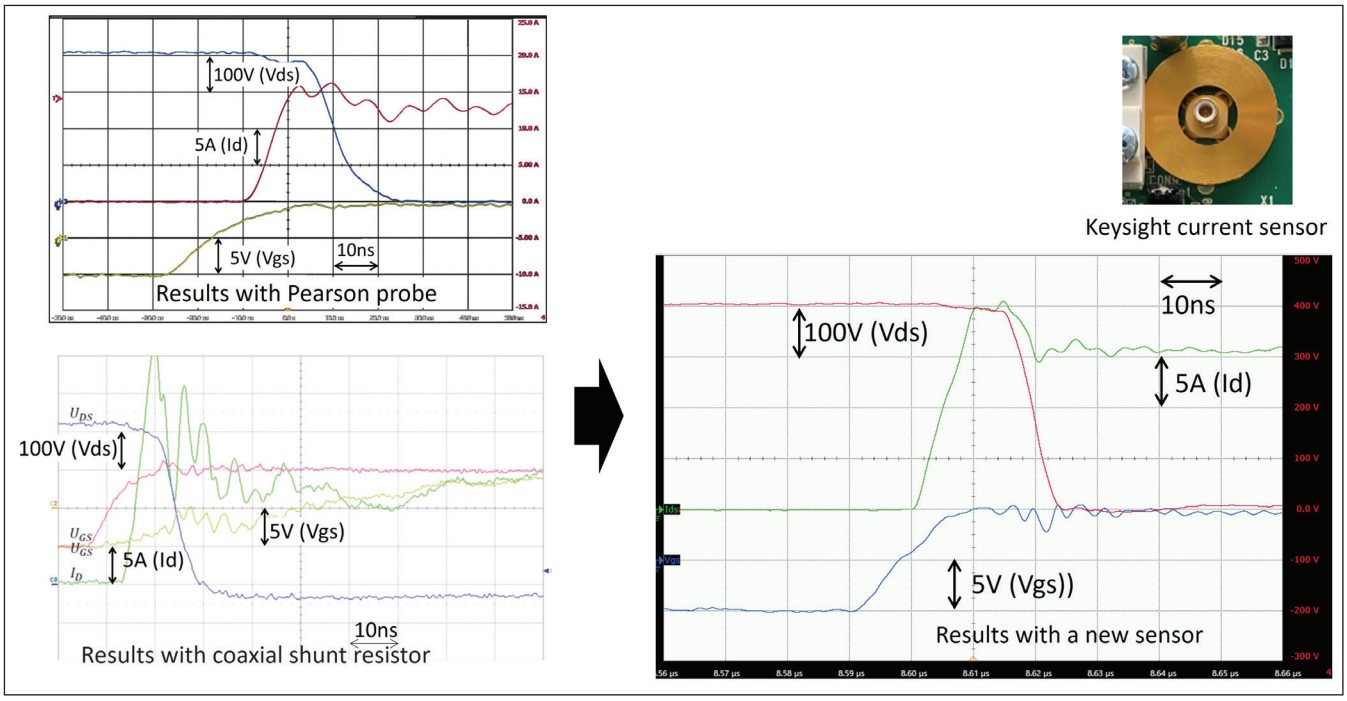
GaN devices exhibit a significant increase in on-resistance under high dv/dt conditions, a phenomenon known as dynamic RDS(on). Characterizing dynamic RDS(on) is essential, as it can lead to faulty circuit operation if left unaddressed.

Key technologies for GaN device characterisation

The test circuit board for GaN device measurement must have minimized loop inductance; otherwise,



➤ Figure 9: GaN FET switching test results with oscillation and ringing.



➤ Figure 10: Switching waveforms with different current sensors.

significant overshoot and ringing can occur, leading to severely distorted waveforms. Design techniques such as using multilayer PCBs with embedded copper planes and overlapping forward and return traces are essential.

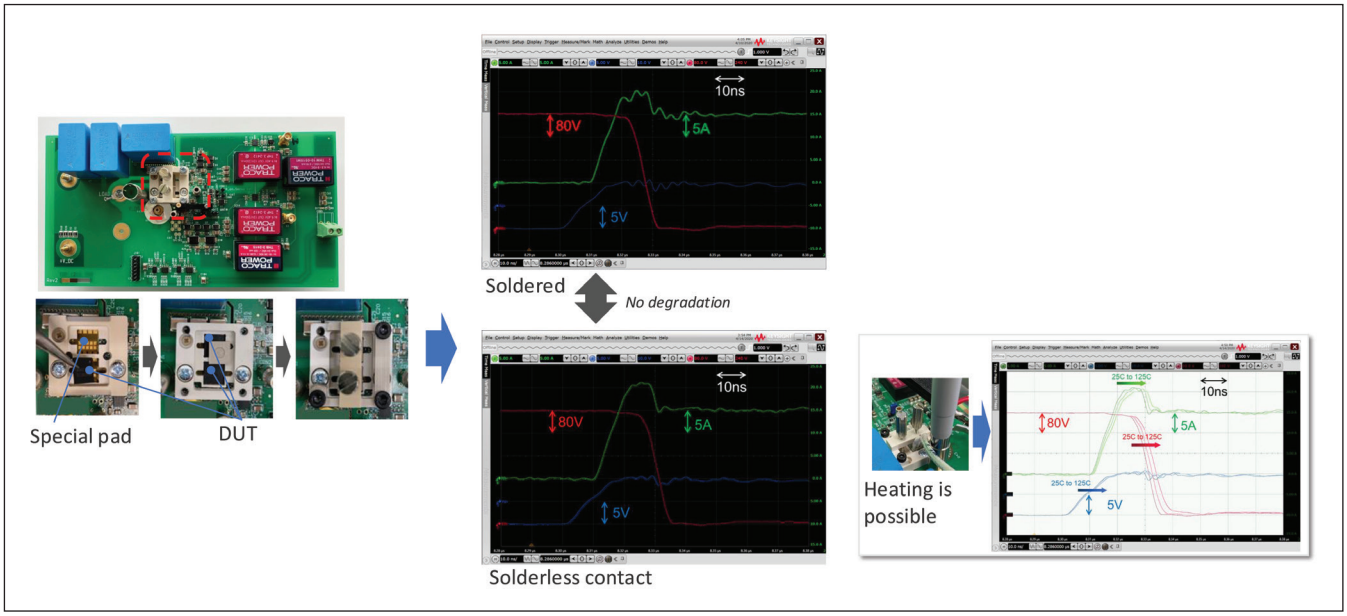
Another critical factor in minimizing power loop inductance is the current sensor. When a coaxial shunt resistor is used, it can add anywhere from a few nanohenries to around 10 nH to the power loop, significantly degrading measurement fidelity. Non-contact current sensors, such as Rogowski coils or Pearson probes, cannot capture the high-frequency components of GaN switching waveforms and are therefore unsuitable.

There is a new current sensor with less than 1 nH of insertion inductance, providing a much more accurate measurement for high-speed devices.

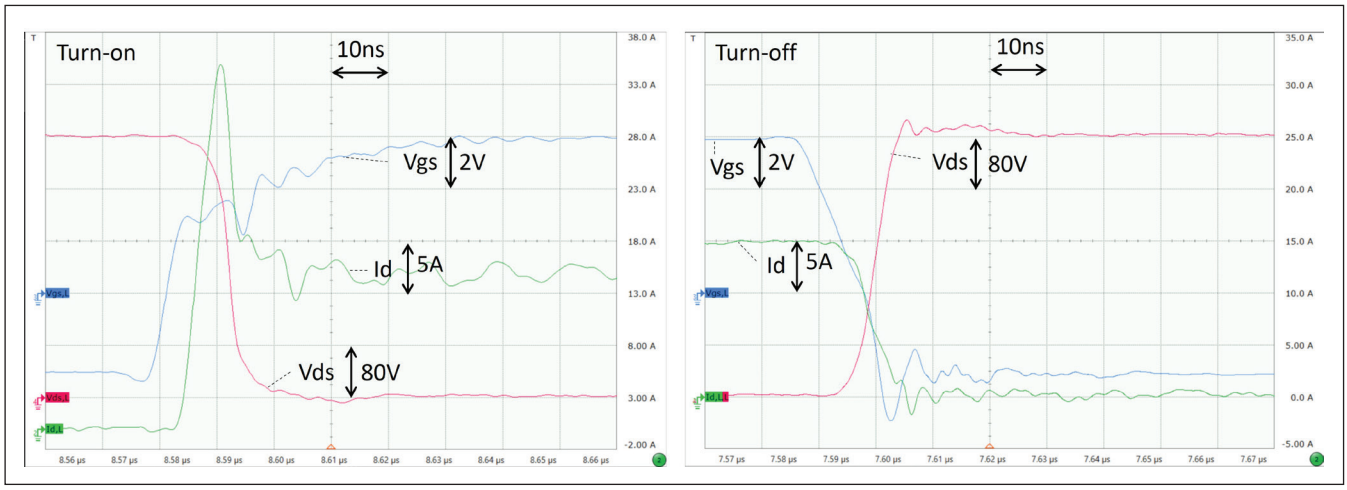
Figure 10 shows a comparison of these current sensors in GaN HEMT measurements.

Solderless contact is another strongly requested technology for GaN device measurement.

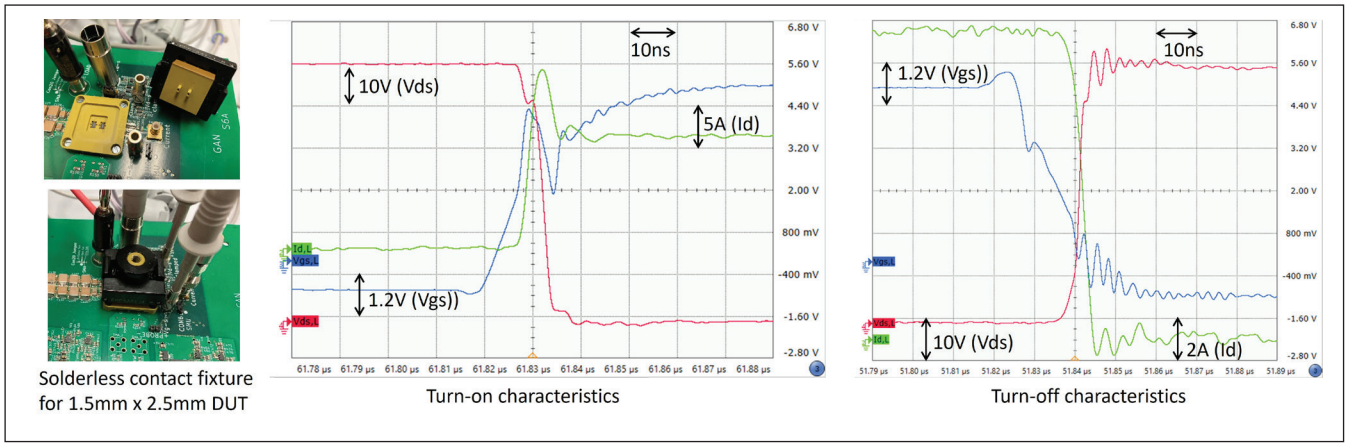
A solderless contact solution can address this problem. As an example, if the solution uses a flexible PCB with multiple raised bumps on the electrodes, which press into the terminals of the SMD device, ensuring excellent contact without introducing additional stray inductance. (See Figure 11).



➤ Figure 11: Solderless contact technology.



➤ Figure 12: Shows example measurement results for GaN HEMT (DUT: GaN Systems GS-065-030-2- L).



Solderless contact fixture for 1.5mm x 2.5mm DUT

Turn-on characteristics

Turn-off characteristics

➤ Figure 13 shows another solderless contact example, applied for very small SMD device (1.5 mm x 2.5 mm).

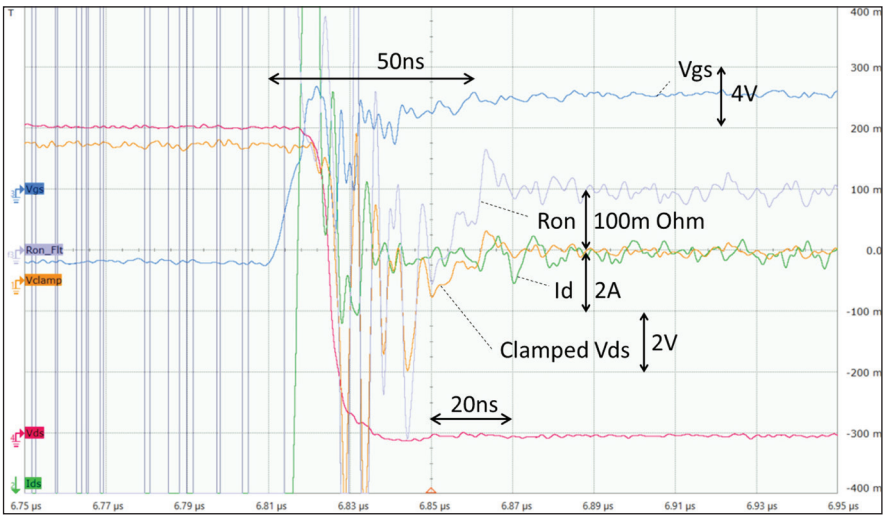
JEDEC JEP173 [1], recommends the use of a voltage-clamp sampling circuit. This circuit clamps the high OFF-state voltage, enabling a low-voltage measurement probe to accurately capture the ON- state voltage.

It should be implemented on the test board in close proximity to the DUT. Figure 14 shows an example measurement result obtained using a clamp circuit.

Summary

Building an accurate, repeatable, and reliable double-pulse tester is not a simple task, as many of the factors described in this article must be carefully considered - and in some cases, new technological developments are required.

However, there are platforms that incorporate the technologies and techniques discussed in this article which will help businesses to ease this challenge.



➤ Figure 14: RDS(ON) measurement example with clamp circuit, effective less than 50ns after the switching.

REFERENCE

➤ [1] "Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices," Version 1.0, JEP173.

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Metrology for the 2 nm era and beyond

Infinitesima bets on high-speed atomic force microscopy to keep advanced silicon on track.

BY REBECCA POOL, TECHNOLOGY EDITOR

WITH Taiwan's lead chipmaker, TSMC, set to begin full-scale production of 2 nm technology, silicon chip design is entering uncharted territory - and pulling metrology along with it.

As ever-more complex 3D architectures, complementary-FETs, hybrid bonding and advanced packaging emerge, metrology and inspection tools will be vital to robust chip fabrication. But with transistor dimensions shrinking to just a few atoms, the workhorse of defect detection - optical inspection – is hitting its limits.

Deep UV lithography at 193 nm wavelength has already given way to extreme UV (EUV) lithography at 13.5 nm. Yet the smallest etch patterns now measure as small as 9 nm. Factor in intricate buried structures with remarkably high aspect ratios and more than 100 stacked layers on a single chip, and the challenge of detecting defects becomes staggering.

One company that remains undeterred is UK-based Infinitesima, which has just joined forces with photolithography systems giant, ASML, of The Netherlands, and Belgian R&D powerhouse, IMEC, to hone its in-line metrology platform for increasingly complex device architectures.

Instead of the usual optical methods, 'Metron3D' relies on atomic force microscopy (AFM), where a probe tip oscillates above the silicon wafer surface and measures the atomic forces, to detect defects. The platform combines AFM with interferometry and other optics innovations to increase inspection throughput of structures by at least 100 times compared to standard AFM - critical for defect detection on a high volume semiconductor manufacturing line.

Together the partners now intend to optimise and drive Infinitesima's unconventional metrology tech further into the silicon semiconductor market. "Industry is operating at the atomic-scale to control transistors – for example, to store electrons in a capacitor, very complex 3D structures are being [fabricated] and that's creating a need for sub-nanometre 3D metrology," says Infinitesima CEO, Peter Jenkins. "AFM is good at this, but traditionally very slow. So solving the speed problem means customers have the metrology to move these structures from R&D and into volume manufacturing."

From lab roots to fab floors

Founded in 2001 by University of Bristol professor, Andrew Humphris, to commercialise fast scanning probe microscopy for biological samples, Infinitesima quickly switched to semiconductors – given the greater market potential. The company's rapid probe microscope (RPM) soon followed - essentially a high-speed AFM that uses optical interferometry, instead of laser beam deflection, to track the AFM probe tip's motion and enable faster sample scanning.

Come 2010, photothermal actuation had replaced mechanically or piezoelectrically-driven actuation in the RPM set-up, to reliably drive probe tips at higher frequencies.

This helped to cut surface analysis and defect detection from minutes to seconds while still delivering sub-nanometre vertical resolution - proving the technique viable for semiconductor fabs. RPM technology was later integrated to Carl Zeiss' photomask repair tools as well as the scanning electron microscope platforms of a leading US chipmaker.

"It's the optics that give RPM its speed and enable unique modes of operation, helpful for looking at small, high aspect ratio structures on semiconductors," highlights Jenkins. "We currently dither [oscillate] the probe at 600 kHz and will extend this to more than a megahertz in the future to enable even faster speeds."

Scaling to volume production

With RPM in tow, Infinitesima partnered with IMEC to integrate its technology with wafer-handling software, robotics, and a high-speed wafer stage, to provide in-line metrology for next-generation logic, DRAM and 3D NAND. Metron3D was delivered in late 2021, and backed by Asia-based investors as well as Applied Ventures, the venture arm of US semiconductor equipment heavyweight, Applied Materials, Infinitesima has been ramping production ever since.

Right now, R&D and core module manufacturing takes place in the UK, with system assembly in Taiwan. "We don't have to invest in building a factory and it's going to be much faster to scale [manufacturing]," says Jenkins.

The system has already shipped to a significant - but unnamed - Taiwan-based foundry as well as to high bandwidth memory chip maker, SK Hynix of Korea - also a supplier to AI giant Nvidia - for advanced DRAM inspection. As Young-Hyun Choi, Head of Defect Analysis, Metrology and Inspection Technology, has said: "3D process control at the nano-scale level is becoming increasingly important to ensure high yield in advanced DRAM processes. Metron3D has demonstrated excellent sub-nanometre 3D metrology with the required cost-of-ownership necessary for high volume manufacturing implementation."

Next steps

Building on this traction, Infinitesima is now working with IMEC and ASML to hone Metron3D for in-line metrology of complex devices, in volume production. ASML in particular has a vested interest in optimising the platform for high-numerical aperture EUV lithography, having shipped these first resist imaging systems in early 2024.

Meanwhile, Jenkins sees other key market opportunities in 3D logic device structures such as complementary field-effect transistors (CFETs), and in hybrid wafer bonding.

"Nearly every future device will use hybrid wafer bonding, and measuring these extremely very flat [structures] is an ideal application for AFM," he says. "AFM is one of the ground-truth metrology methods that can give you sub-nanometre, 3D information, which is why we're confident industry will need this technology as it moves forward – and we can do this so much faster with Metron3D."

As part of a three-year development project, the partners will focus on taking in-depth 3D surface detection, high-speed imaging and interferometric accuracy further.

By way of example, Jenkins notes they will refine the RPM probe tip and AFM operating modes to measure the smaller patterns and strut features formed on wafers during high-NA EUV lithography. "We won't be redesigning our system," he explains. "This is about enhancing operation within the software, codes and types of probes that we use, and the data analysis that we run."

➤ Infinitesima's Metron3D metrology system is designed to measure challenging nanoscale structures in semiconductors at high speed. [Infinitesima]

Jenkins is hopeful that come the project-end, AFM technology market growth will be well and truly on the rise. He estimates the value of today's AFM market at around $200 million, but based on a steady semiconductor industry CAGR of 8%, expects this figure could reach $1 billion come 2030. "AFM will become increasingly complementary to certain process control steps, and the number of those steps will increase as fabrication processes evolve," he says.

But will industry demand for Metron3D also rise? Jenkins thinks so, highlighting Infinitesima's two existing contracts, and also noting how the technology is under evaluation with industry's other key players – that includes Intel, Samsung and Micron. "We're pretty hopeful that we will see additional contracts with other players in the coming 12 to 24 months," he says.

"Time to market is critical and we already have some strong IP protecting our core technology," he adds. "I would imagine we'll get an [acquisition] offer from one of the lead firms down the road, which we'll evaluate at that point in time. But for now, we're happy doing our thing."

iDEAL charts a new course for silicon

Will the latest MOSFET from iDEAL Semiconductor redefine silicon chip performance?

BY REBECCA POOL, TECHNOLOGY EDITOR

IN SEPTEMBER this year, a new kind of silicon MOSFET entered mass production. Developed by iDEAL Semiconductor, the 150V and 200V devices are based on the so-called SuperQ architecture, which the US-based firm claims is the first major advance in silicon MOSFET technology in more than 25 years.

Drawing on elements of the legacy HEXFET and Superjunction topologies, the SuperQ-based MOSFET concept was first conceived more than a decade ago. While built mostly on established CMOS processes, the device is said to break through long-standing silicon barriers in switching and conduction.

“The number one question I get from applications and systems engineers is what’s the catch?” says Ryan Manack, Vice President of Marketing at iDEAL Semiconductor. “I see competitors making devices with a lower resistance and double the switching loss, but we’re providing the next level of performance without a trade-off.”

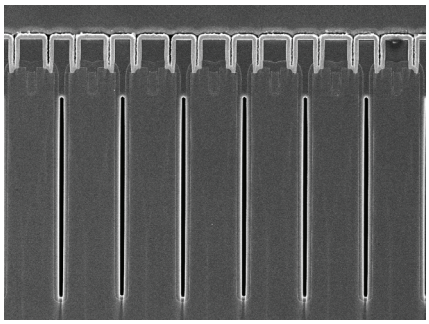
The 150V and 200V MOSFETs are just the beginning. iDEAL Semiconductor intends to soon provide a 650 V device, and has bold plans to take its SuperQ architecture up to 1200 V.

“We’ve already demonstrated that the performance of our [structures] is either equal or better than the industry-leading super-junction structures that industry has been optimising for the last twenty years,” highlights Manack’s colleague, Philip Rutter, Vice President of Development at iDEAL Semiconductor. “We’re just getting started.”

A different approach

The SuperQ architecture follows a long history of MOSFET innovation. The legacy HEXFET architecture was launched by International Rectifier back in late 1978. Its hexagonal cell geometry in a vertical MOSFET design boosted transistor density, shrank die size, and proved pivotal to the miniaturization of electronic devices. A wide *n*-type conduction region helped the device to excel at low and medium voltages, but performance became inefficient at higher levels, as blocking more voltage in this drift region drove up on-resistance.

Come 1998, Infineon Technologies (then Siemens Semiconductor) changed the game with its superjunction MOSFETs, which were based on the Reduced Surface Field - RESURF - structure and could operate at higher voltages more efficiently. The drift region of this power transistor comprised pillars of p-type and n-type layers, in contrast to purely n-type material in the HEXFET, yielding a less resistive structure that could still block higher voltages.



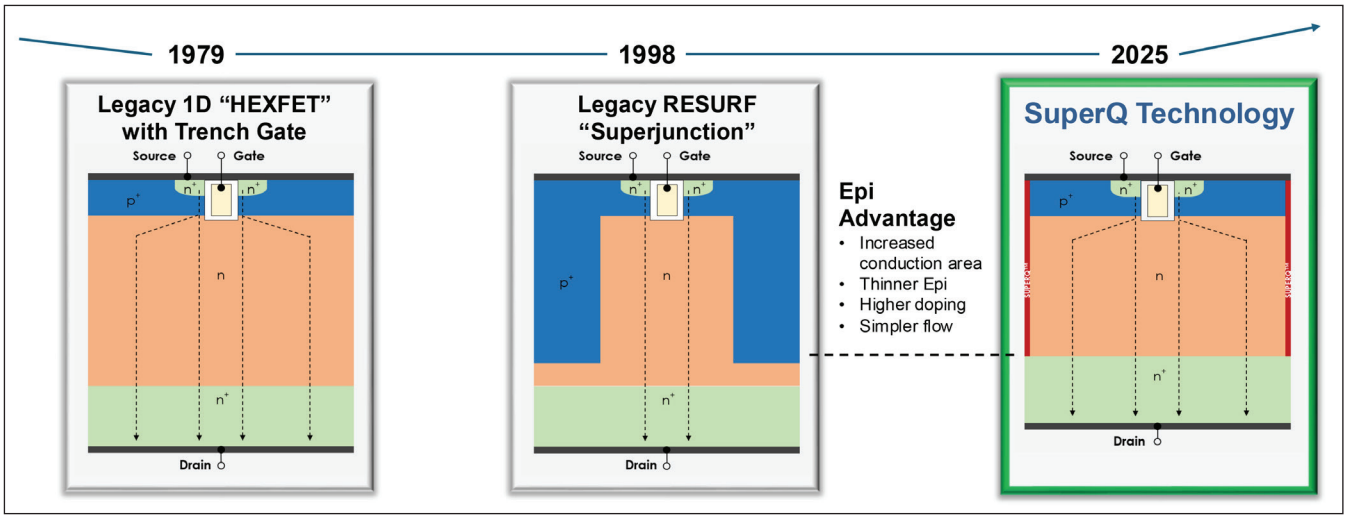
➤ SuperQ trench technology promises near-ideal charge balance, allowing thinner epitaxy. It also allows a higher doping concentration in the conduction region, helping to reduce channel resistance and lowering power loss. [iDEAL Semiconductor]

But while this superjunction approach became the gold standard for silicon MOSFETs, higher voltage operation has demanded thick, high resistance drift regions, that can stifle silicon performance and generate excess heat. Given this, Mark Granahan, now CEO of iDEAL Semiconductor, had the idea to bring back HEXFET’s wide n-type conduction region but introduce dielectric-filled deep trenches. This novel design minimized the need for p-type layers and reduced on-resistance whilst maintaining the all-important high voltage blocking capabilities.

iDEAL Semiconductor launched in 2017, with Granahan and colleagues spending some time finding the best way to etch high aspect ratio trenches and create functional structures. They settled on atomic layer deposition, a gas-phase chemical process in which thins films are deposited one atomic layer at a time. Following several investment rounds that brought in more than $75 million, including funds from Applied Ventures, the venture capital arm of Applied Materials, so-called SuperQ technology was introduced in 2023.

“We have extremely good process control that costs less [than superjunction fabrication],” highlights Rutter. “We etch our trench and then deposit a charged layer, using atomic layer deposition.”

“So as our competitors have kept on shrinking the n-type region, they’ve lost part of the benefits [of silicon] but



➤ MOSFET architectures include the 'HEXFET' and Super-junction. SuperQ is designed to maximize the n-conduction region. [iDEAL Semiconductor]

with SuperQ, we've kept the n-type region wider and have in effect just shrunk the p-region," he adds. "From an architectural point of view, there are no limits to doing this."

Delivering devices

Working with US-based independent foundry, Polar Semiconductor, iDEAL Semiconductor's first devices, both 150 V and 200 V MOSFETs entered full production within weeks of each other, this Summer, and higher voltage devices are set to follow soon.

"We've got 300 V and 400 V MOSFETs entering the fab right now, and 650 V [devices] are in the works," says Manack. "And [to deliver these], we're talking quarters not years."

Both devices are said to reduce switching losses by at least 2X compared to competing devices, and improve resistance and power losses – whilst maintaining the benefits of silicon, including its high-volume manufacturability. The company's latest lowest-resistance 200 V devices achieve a maximum RDS(on) of just 5.5 mΩ, delivering resistance that is said to be 1.2x lower than the current market leader, and 1.7x lower than its next-best competitor in silicon. Target applications include motor drives and AI servers, as well as LED lighting, battery protection, isolated DC/DC power modules and USB-PD adapters.

But there's more to SuperQ than silicon MOSFETs. The technology is also designed for IGBTs, diodes, power ICs - and even other semiconductor materials, including SiC and GaN. Manack also notes that iDEAL Semiconductor's silicon roadmap takes the technology to 1200 V.

"To reach higher voltages with the superjunction MOSFET, you grow additional epi-layers to get that thicker drift [region], which just gets more and more expensive as you get charged based on the numbers of process steps in the fab," he says. "But we're different. If you want a higher voltage, you need a deeper trench, so we look at how deep can we dig that trench - what aspect ratio can we reach? We believe that one day SuperQ will deliver a 1200 V MOSFET."

Etching ever-deeper, high-aspect-ratio trenches for higher-voltage MOSFETs is no small feat, but it's one that Rutter and colleagues believe they have mastered. With a newly acquired state-of-the-art trench etcher driving progress, they are now focused on integrating these deeper trenches into the MOSFET design - with qualification to follow. But how has the market responded to a new, high voltage MOSFET platform that is not based on wide bandgap semiconductors? High performance, energy efficient SiC and GaN devices from the likes of Wolfspeed, Infineon, EPC, Transphorm and more, have already made many in-roads into traction inverters, power supplies, fast chargers and myriad other applications. And despite recent upheavals, such as Wolfspeed's bankruptcy and TSMC pausing GaN production, market forecasts remain robust. Still, high performance and forecasts aside, these materials remain relatively expensive and can face supply bottlenecks compared with standard silicon used in most chips. Both Manack and Rutter are keen to emphasise how SuperQ MOSFETs can be cost-effectively manufactured with tools and processes commonly standard to CMOS fabs. Rutter points out that around 90% of SuperQ's production relies on established techniques used to fabricate vertical power trench devices while Manack notes that initial development took place on 300 mm CMOS.

"Having SuperQ on a silicon platform leverages a tremendous amount of existing tool-sets, and makes it very scalable," adds Manack. "We're not just increasing performance, we're also keeping costs under control." Recent partnerships with semiconductor distribution firms indicate that industry players agree. In July this year, iDEAL Semiconductor signed a global distribution agreement with Mouser Electronics, and also partnered with Richardson Electronics to gain access to its design and sales teams to expand the reach of its SuperQ MOSFETs.

"Some of the rhetoric in the industry has been that silicon is dead and you need to change materials and invent new tool-sets to improve performance," reflects Manack. "But this couldn't be further from the truth – what was dead was the new ideas and the R&D dollars."

Power semiconductors – the silent heroes in the power grid

This article explores the pivotal role of power semiconductors in the evolving landscape of the power grid, their technological advancements, application-specific challenges, and their contribution to environmental sustainability.

TOBIAS KELLER, VICE PRESIDENT, HEAD OF GLOBAL PRODUCT MANAGEMENT, PORTFOLIO & MARKETING, HITACHI ENERGY.

THE MODERN power grid stands as one of humanity's most complex and critical infrastructures. It is a vast, interconnected system that enables the generation, transmission, and distribution of electrical energy across continents. At the heart of this intricate network lies a class of components often overlooked by the public but indispensable to its operation: power semiconductors.

These devices, once considered unsuitable for high-power applications, have evolved into the silent heroes of the energy transition. This transformation is not merely technological – it is foundational to achieving a sustainable, resilient, and efficient power system.

The evolution of the power grid

Historically, the power grid was a linear and predictable system. Electrical energy flowed in a unidirectional manner – from centralized power plants to end consumers. This structure allowed for straightforward calculations of fault currents and relatively simple protection schemes. A single upstream breaker could isolate a fault, preventing its propagation through the network.

However, the contemporary grid has undergone a paradigm shift. The integration of distributed energy resources (DERs), such as solar panels, wind turbines, and battery storage systems, has introduced bidirectional energy flows. Consumers have become "prosumers," capable of both consuming and generating electricity. This dynamic environment results in constantly changing grid topologies and fault current profiles. The traditional protection mechanisms are no longer sufficient.

The modern grid demands:

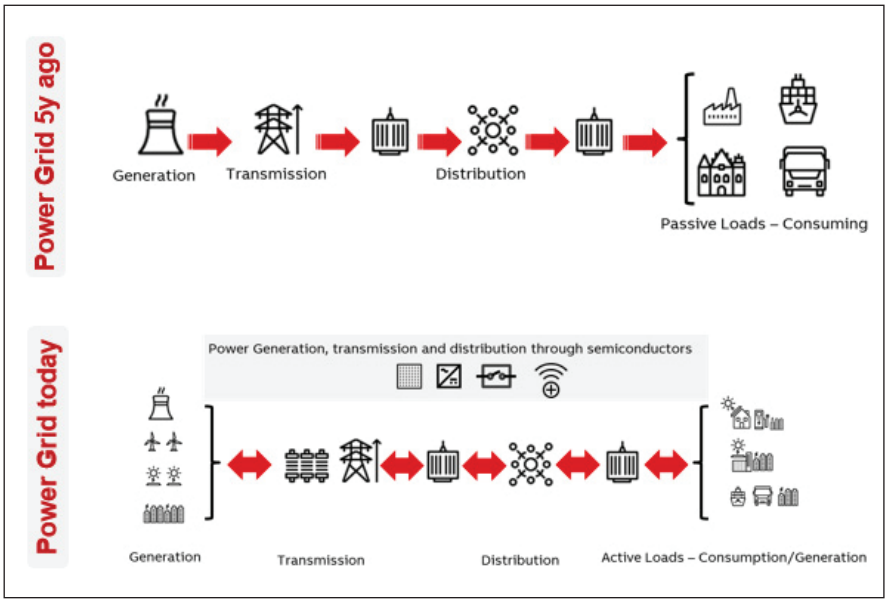
- Rapid fault detection and isolation
- Coordinated switching across multiple nodes
- Real-time adaptability to fluctuating energy flows

These requirements have elevated the importance of power semiconductors, which offer the speed, precision, and reliability needed to manage such complexity.

Power semiconductors across the energy value chain

Power semiconductors are now embedded in every stage of the electrical energy lifecycle:

- **Generation:** In power generation, semiconductors are used to convert and condition energy from various sources. Offshore wind turbines, with capacities reaching up to 17 MW, and onshore wind turbines (1–7 MW) rely on



semiconductor-based converters to interface with the grid (either alternating current (AC) or directly direct current (DC)). These devices ensure that the generated power meets grid standards for voltage, frequency, and phase.

- **Transmission:** High-voltage direct current (HVDC) systems, which transmit gigawatts of power over long distances (e.g., 700 km subsea), depend on semiconductors for efficient conversion between AC and DC. Devices such as thyristors and IGBTs (Insulated Gate-Bipolar Thyristors) are central to this process, enabling high-efficiency transmission with minimal losses.

- **Connection and Distribution:** At the grid interface, semiconductors facilitate the integration of diverse energy sources and loads. Technologies like Static Synchronous Compensators (STATCOM), Solid-State Transformers (SST), and Static Frequency Converters (SFC) use semiconductors to stabilize voltage and frequency, manage reactive power, and ensure seamless energy flow.

Semiconductor technologies and packaging

Technological improvements on the power semiconductors enabled the use of a wide variety of these devices in the power grid. Packaging plays a critical role in the performance and reliability of these devices. Key considerations include:

- **Thermal management:** Efficient heat dissipation is essential for maintaining performance and extending lifespan.
- **Mechanical robustness:** Modules must withstand vibrations, humidity, and other environmental stresses.
- **Electrical insulation and protection:** Ensures safe operation under high-voltage conditions.
- Advanced packaging techniques enable the paralleling of multiple chips to handle currents exceeding 1kA. These modules are compact, rugged, and designed for long-term reliability.

➤ Thyristor

➤ IGBT

These technological improvement led to the latest power semiconductors known as:

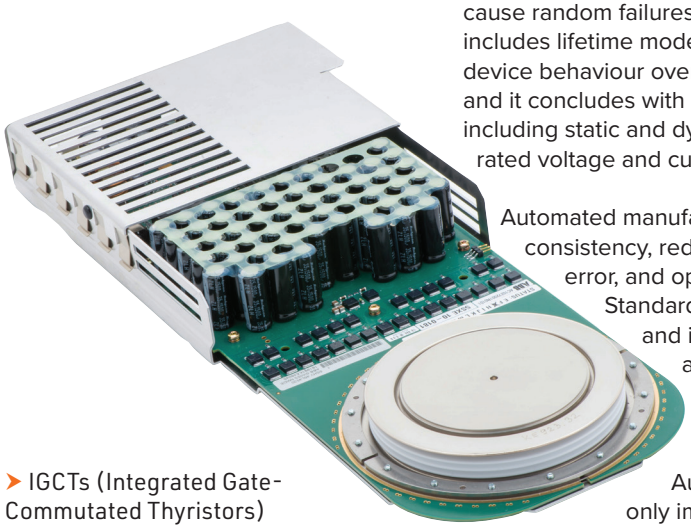
- **IGCTs (Integrated Gate-Commutated Thyristors):** Bipolar devices with integrated gate units, suitable for high-power applications.
- **Thyristors:** Capable of handling voltages up to 8kV, used in ultra-high-power systems.
- **IGBTs:** Found in various module formats such as LoPak, StakPak, and LinPak, with voltage ratings from 1.2kV to 5.2kV.

Ensuring reliability and manufacturability

Reliability is paramount in power semiconductor applications. Devices must operate flawlessly for decades under harsh conditions. To achieve this, manufacturers employ rigorous testing and quality control measures including cosmic ray testing.

This evaluates susceptibility to high-energy particles from the sun that can cause random failures. Furthermore, it includes lifetime modelling, this predicts device behaviour over extended period and it concludes with electrical testing, including static and dynamic tests at rated voltage and current.

Automated manufacturing ensures consistency, reduces human error, and optimizes cost. Standardized processes and industrialization are key to scaling production while maintaining high quality. Automation not only improves yield but also acts as a safeguard for quality assurance.



➤ IGCTs (Integrated Gate-Commutated Thyristors)

Silicon Carbide (SiC): A technological breakthrough

SiC is emerging as a transformative material in power electronics. Compared to silicon, it offers a significant higher electric field breakthrough voltage, significantly higher electron velocity, a higher thermal conductivity and last but not least a higher melting point.

These properties enables on the application side of power semiconductors various interesting improvements, e.g. higher voltages with simpler devices topologies (MOSFET instead of IGBTs), faster switching speeds (several kilohertz instead of several hundred hertz), power switching losses (towards) 200°C and above instead of towards 150°C, higher ambient operating temperatures supporting aspects on the demand of higher environment temperatures.

These improvements already let in various applications to a clear shift towards SiC. These applications include electric vehicles (xEVs) and enable a longer driving range (+7-8%) and faster

charging and furthermore electric vehicle charging infrastructure enabling smaller filters and reduced space requirements.

In terms or reliability it is proven that SiC is as reliable as Silicon (SiC devices are capable of 4 million switching cycles with no gate degradation over time).

The development of SiC technology involves mastering high-temperature processes (up to 2500°C) in the front end chip processes and continuous innovation in chip design.

These efforts are bringing SiC devices from research labs to commercial markets, enabling new levels of efficiency and performance.

Environmental impact and regionalisation

Power semiconductors also contribute to environmental sustainability. A case study summarized below uses ISO 14083:2023 CO_2 calculations to assess the carbon footprint of transporting power modules from Asia to Europe.

In 2023 Europe installed 632,400 charging stations. 12.9% thereof were DC fast chargers (81,827 units). In total in 2023 in Europe 1.54 million electric vehicles were sold.

Considering three power modules, each with a weight of 300g, per car to connect the battery and the motor the resulting CO_2 emissions just transporting the power semiconductor modules for these electric cars from Asia to Europe generated approximately 6,952 tons of CO_2 – equivalent to the annual emissions of 2,000 petrol cars (assuming 25,000 km/year).

To mitigate this impact, regional manufacturing clusters are required, they enhance supply chain resilience (e.g. during pandemics) and local production reduces logistics emissions and supports local economies.

Conclusion

Power semiconductors have transitioned from niche components to foundational elements of the modern power grid. They enable the integration of renewable energy, enhance grid stability, and support the electrification of transportation. Their evolution – from silicon to silicon carbide – has unlocked new levels of efficiency, reliability, and environmental performance.

As the energy transition accelerates, the role of these “silent heroes” will only grow. Continued investment in semiconductor technology, manufacturing, and regionalisation is essential to building a resilient, sustainable, and intelligent power infrastructure.

The future of energy depends not only on how we generate electricity, but also on how we control and deliver it. In this context, power semiconductors are not just components – they are enablers of a cleaner, smarter world.

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Bidirectional power and transient speed enable scalable active suspension

Sine Amplitude Converter™ modules offer a unique combination of bidirectionality and transient response that unlocks new possibilities for active suspension.

BY VICOR

ACTIVE SUSPENSION has long been synonymous with luxury vehicles, but today the technology is beginning to appear across a broader and more accessible range of platforms.

However, supporting this expansion requires automotive power architectures that are far more flexible and responsive than what has historically been the industry standard.

At the highest level, suspension control requires an underlying power system that can support an instantaneous bidirectional current flow direction change and high-speed transient response. A system that cannot reverse current direction or deliver power instantly may fail to stabilize the vehicle chassis during road disturbances or miss the opportunity to recover energy during rebound.

Unfortunately, traditional power electronics built around regulated DC-DC converters, buffered energy storage and 12V rails struggle to meet the fast-paced demands of suspension actuators without major weight and size increases.

Instead, Power modules based on Vicor Sine Amplitude Converter (SAC™) technology directly address both challenges by enabling symmetrical energy flow without switching overhead and delivering current with nearly zero delay regardless of dynamic load conditions.

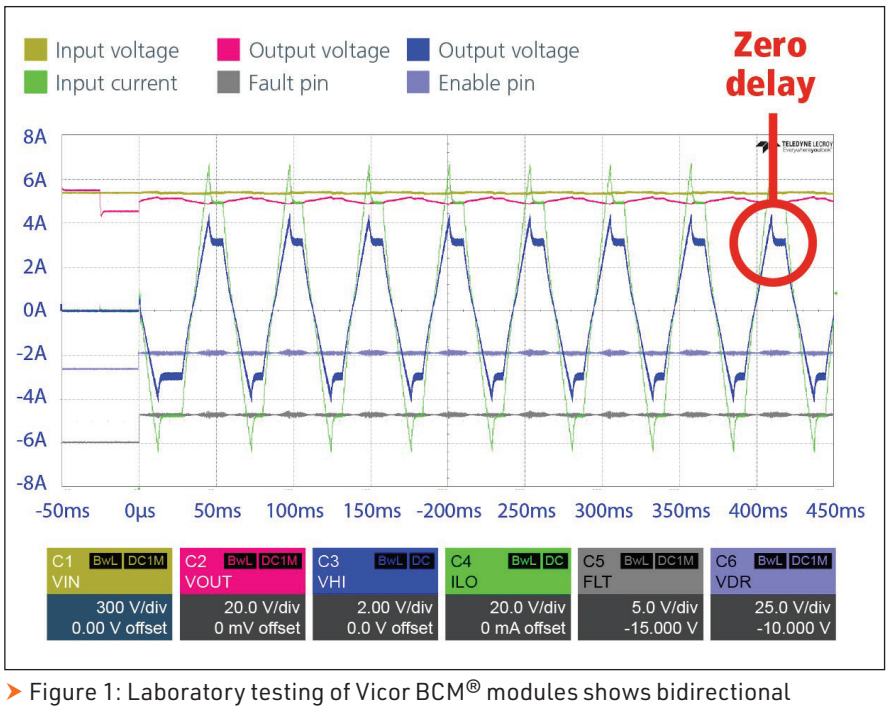
The result is a power delivery system that operates more like a direct extension of the battery than a conventional voltage regulator.

Bidirectional flow without software control or switching logic

Suspension actuators are among the few vehicle subsystems that must operate as both a load and a generator. The current flowing into a linear actuator during road compression can reverse direction milliseconds later as that same actuator rebounds and harvests kinetic energy. This is why support for bidirectionality is so important for the underlying power system. Without a converter that can accommodate fast and smooth current reversal, much of this regenerative energy would be wasted or require dissipation through resistive loads (Figure 1).

SAC-based converters are inherently symmetrical in their behavior. Because they operate with a fixed voltage transformation ratio and use soft resonant switching, current can reverse without the need for explicit control logic. There is no pin toggling, no microcontroller intervention, and no software-defined routing between source and sink paths.

This behavior is rooted in the physics of the converter itself. As the 48V low-side voltage rises (i.e., due to regeneration), the converter naturally reflects that back to the high side. In other words, when the resulting voltage exceeds the battery rail, current flows upstream. Conversely, when the suspension draws



➤ Figure 1: Laboratory testing of Vicor BCM® modules shows bidirectional operation with zero delay between input and output.

power, the converter steps down from the battery rail with no reconfiguration. In that way, a single converter can support both directions of current flow without interruption (Figure 1).

Conventional regulated converters, on the other hand, are not inherently bidirectional. To feign bidirectionality, such systems employ parallel buck-boost or regulated dual-path designs that increase the bill of materials (BOM), board area requirements and system complexity. These architectures then rely on the cumbersome process of actively detecting current transitions and responding via software or analog control loops to reestablish a stable output. During that time, regenerative energy is either lost or shunted into local buffers. This latency reduces overall system efficiency while also forcing designers to include additional components that increase size, weight and system complexity.

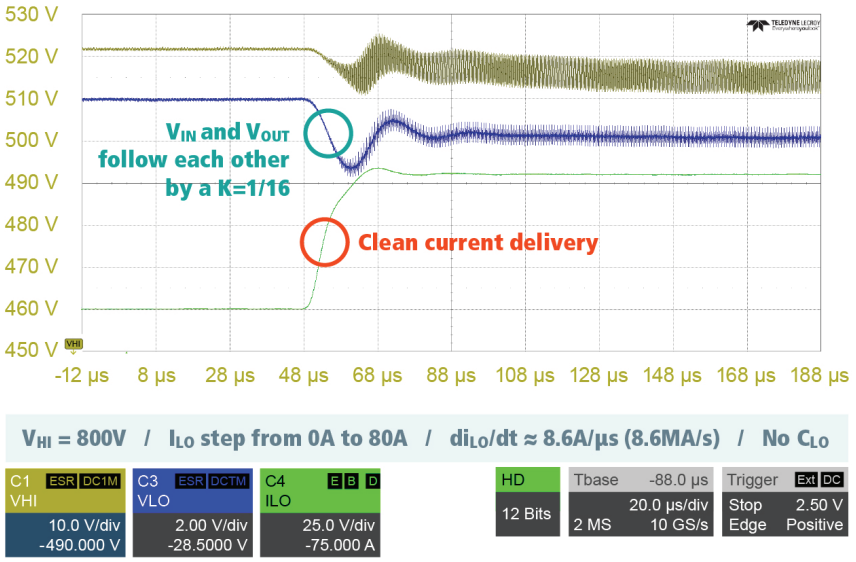
Bidirectional SAC modules avoid this entirely. Their behavior is immediate and autonomous, enabling high energy capture efficiency without complexity. In practical terms, this makes it possible to eliminate the dedicated circuitry and firmware that previously managed direction control. It also removes the need for redundant converter pathways or additional current sensing.

Ultimately, the bidirectional capability is a function of the converter's resonant, passive behavior, not an orchestrated response managed by a controller.

This performance also has implications beyond active suspension. Any subsystem with bidirectional current behavior like steering assist, regenerative braking, chassis leveling or thermal pump backflow can benefit from such a simplified flow. In this way, bidirectional SAC modules provide a means to unify power flow design across these subsystems, thereby reducing the architectural complexity of zonal power domains within the vehicle.

Transient response without output filters or buffers

Fast transient response is the second non-negotiable requirement for active suspension. The suspension system must react to rapid mechanical inputs from the road, sometimes within microseconds. During such events, the power system must be able to source or sink current without delay, droop, or overshoot.



➤ Figure 2: Laboratory testing of Vicor BCM modules shows how Sine Amplitude Converter™ modules are capable of achieving slew rates exceeding 8MA/s.

SAC modules deliver this responsiveness directly. Operating at resonant frequencies with minimal parasitic elements, SAC-based power modules exhibit current slew rates exceeding 8 million amps per second (Figure 2).

Notably, this performance is achieved without the use of output inductors, capacitors, or local energy storage. Instead of relying on energy buffering to smooth voltage and current transitions, SAC™ converters use a high-Q resonant tank to transfer energy efficiently and predictably between the primary and secondary sides.The result is a power path with extremely low output impedance and negligible phase lag, allowing the system to respond to load steps as rapidly as the control system can command them without energy lag or overshoot effects common in filtered designs.

This responsiveness is a major advantage for the control loops that govern electromechanical suspension. The closed-loop stability of such systems depends on electrical latency staying below the mechanical response time of the actuator and vehicle mass. When the electrical system can keep up, more aggressive damping algorithms can be deployed, yielding better handling, reduced body roll and faster recovery from potholes or lane changes.

Another advantage of filter-free transient performance is volume reduction. Output capacitors and inductors at the power levels used in suspension systems are physically large and difficult to cool. Their removal translates directly to smaller enclosures, fewer thermal management constraints and better placement options within the chassis.

The combination of bidirectionality and transient response also creates opportunities for new design roles. These same modules can be used to precharge the high-voltage traction bus from a 48V source, reversing their nominal direction without any firmware intervention

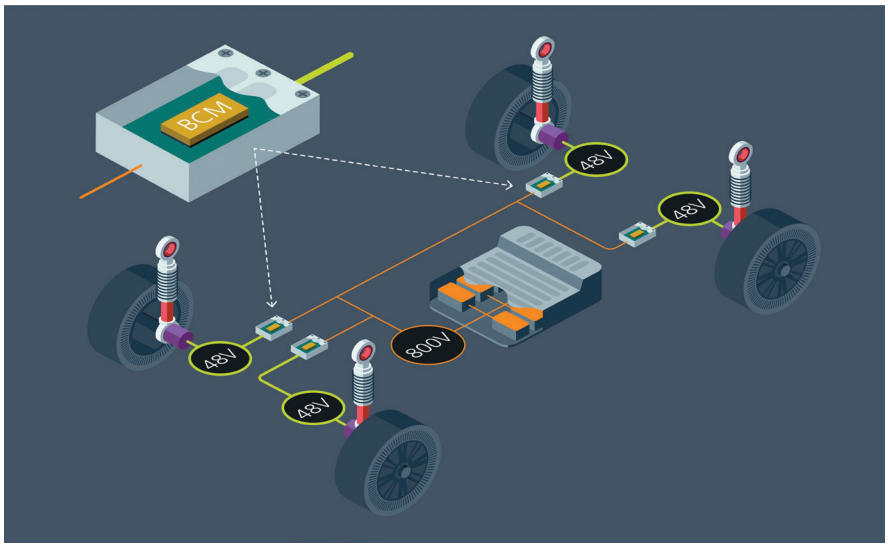
What happens when you combine bidirectionality and speed?

When bidirectional flow and fast transient response are treated as primary design constraints, the system architecture becomes significantly simpler. SAC converters eliminate the need for multiple power stages, bypass the need for intermediate batteries or super-capacitors and remove the requirement for parallel buck-boost or regulated dual-path designs.

In a conventional setup, regenerative current may follow a distinct path from actuation current, each with its own switches, protections and timing logic. In SAC-enabled designs, a single fixed-ratio converter handles both seamlessly (Figure 3). OEMs reap the benefits of simplified wiring harnesses and minimized parasitic losses.
Such an architecture also improves reliability by reducing the number of control elements and synchronization dependencies.

This improved design also enables more effective mechanical integration. SAC modules combine high power density (up to 150kW/L) with a compact, thermally optimized form factor that fits directly into existing structures, such as the battery housing or chassis. Their flat, planar surfaces provide efficient thermal contact, while the internal architecture maintains low thermal impedance despite the high component density.

As a result, these modules often match or outperform the thermal behavior of individual discrete MOSFETs, delivering kilowatts of power using only external heat sinks or airflow management.



➤ Figure 3: Sine Amplitude Converter modules can support active suspension power systems that require bidirectional current flow between the battery and suspension actuators.

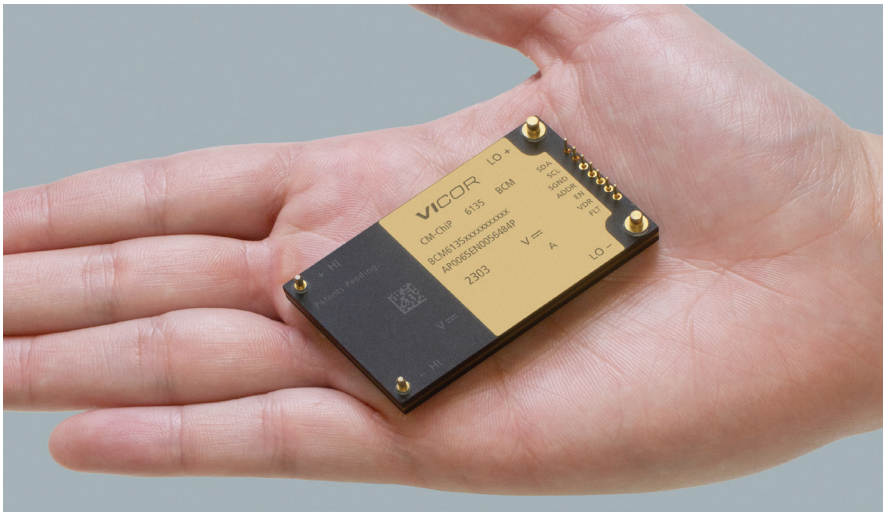
Scalability is another benefit. Because these converters operate at fixed gain and require no reconfiguration for direction changes or load types, they can be paralleled for higher output or redundancy. In that way, a single module type can be used across an OEM's entire vehicle platform. For example, the same unit can power a lightweight front suspension in a crossover or a dual-motor rear axle suspension in a commercial van, with differences in performance handled by quantity and cooling method rather than design changes.

The combination of bidirectionality and transient response also creates opportunities for new design roles. These same modules can be used to precharge the high-voltage traction bus from a 48V source, reversing their nominal direction without any firmware intervention. They can also serve as the primary conduit for 48V zonal power distribution, where they can manage other dynamic and bidirectional power profiles applications like electric pumps, compressors, and thermal systems

Bringing active suspension to the masses

Bidirectional power flow and fast transient response are both necessary to bring active suspension systems to a wider range of vehicles. And, when compared to traditional power architecture and solutions, SAC™ converters offer a clear and superior path forward.

Currently, Vicor is the only company offering SAC-based power modules at scale. Solutions like Vicor BCM® modules offer an extremely unique combination of response time, bidirectionality, efficiency, thermal robustness and power density that unlocks new possibilities for designers. By centering the design around SAC-based modules, engineers can create suspension architectures that are lighter, faster, and more energy-efficient, while also being easier to integrate and scale. Through such solutions, OEMs can introduce active suspension to a wider market in a way that is both technologically and economically viable.



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How Network-on-Chip architectures are powering the future of microcontroller design

Microcontrollers (MCUs) are no longer the humble workhorses of embedded systems. Today's MCUs rapidly evolve into compact, high-performance computing platforms, integrating artificial intelligence (AI), advanced security features, and real-time processing into power-constrained environments. As the demands on MCUs increase, one foundational component is being reimagined to keep pace: the on-chip interconnect.

BY ANDY NIGHTINGALE, VP OF PRODUCT MANAGEMENT AND MARKETING AT ARTERIS

AT THE HEART of this transformation lies the Network-on-Chip (NoC) architecture – an increasingly essential innovation that replaces outdated interconnects with a packetized, scalable communication framework.

NoCs enable MCU designers to manage performance bottlenecks, improve power efficiency, and future-proof designs against the escalating complexity of embedded applications.

The interconnect bottleneck in modern MCUs

While sufficient for basic designs, the traditional interconnect approach hits a wall when systems scale. Bus contention, increased routing complexity, and non-deterministic latency introduce inefficiencies and design headaches. NoC architectures provide an alternative that brings a packet-based, structured communication model to integrated circuits.

In the MCU world, this translates into real advantages:

- **Scalability:** NoCs support many cores and accelerators without redesigning the communication fabric.
- **Power Efficiency:** Using configurable packetised data and serialization, NoCs reduce wire counts, dynamic power, and routing complexity.
- **Latency Management:** Deterministic traffic handling and quality-of-

service features improve real-time responsiveness.

- **Modularity:** Engineers can integrate new IP blocks (e.g., AI engines, security modules) without disrupting existing traffic paths.

Power efficiency by design

The most critical advantage of NoC architectures is their ability to support fine-grained power control. NoCs naturally enable power domain partitioning, allowing different chip parts to power down independently.

With clock gating and dynamic voltage and frequency scaling (DVFS), NoCs help reduce dynamic and leakage power without sacrificing system responsiveness.

For example, in automotive MCUs used in electric vehicles or advanced driver-assistance systems (ADAS), maintaining real-time responsiveness while managing energy consumption is paramount. NoCs provide the infrastructure to prioritize critical data paths while throttling or shutting down others, ensuring optimal energy use under variable workloads.

Safety, Security, and Futureproofing
Modern MCUs often must comply with stringent functional safety and security standards, particularly in automotive, industrial automation, and healthcare applications such as ISO26262 and ISO/SAE 21434. NoC features like deadlock avoidance, fault detection, and latency-aware routing provide the determinism and reliability needed for mission-critical applications.

In security-focused designs, NoCs enable traffic isolation between trusted and untrusted zones. This built-in partitioning capability simplifies compliance with evolving regulatory and cybersecurity standards, while introducing security at a hardware level and reducing overall attack surface.

The modular, scalable nature of NoCs makes them well-suited for futureproofing MCU architectures, supporting emerging workloads and evolving interconnect standards. With the industry moving toward multi-die and chiplet-based designs, NoCs offer a natural framework for die-to-die communication, ensuring that next-generation MCUs can seamlessly scale across package boundaries while maintaining coherence, performance, and energy efficiency.

The road ahead

Network-on-chip architectures offer a scalable, efficient, power-aware solution that aligns perfectly with the next generation of microcontroller requirements. From enhancing bandwidth and lowering wire count to supporting advanced power management and safety compliance, NoCs are enabling MCUs to meet today's needs while preparing for tomorrow's demands.

Learn more about network-on-chip IP technology from Arteris, the industry leader in connectivity technologies.

Enhancing MMC VSC HVDC system performance with press-pack IGBT technology

By adopting Press-Pack IGBTs, operators can significantly reduce component-level failure risks while improving overall system efficiency and lifetime economics – a decisive advantage in today's utility-scale energy infrastructure.

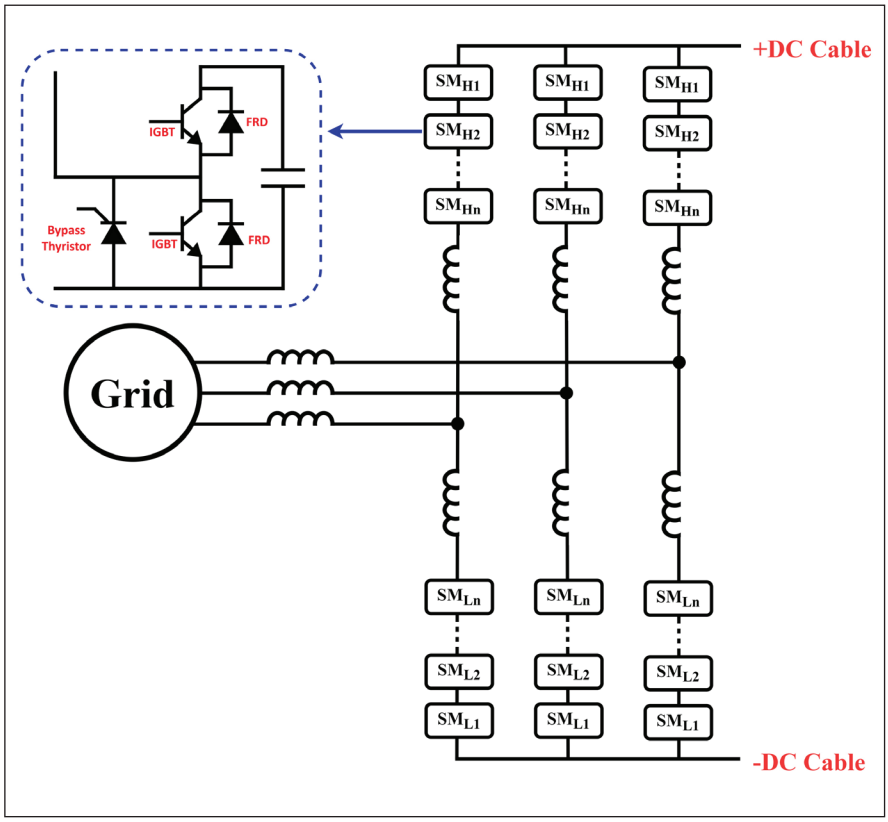
BY DR SAJAD ANSARI, SENIOR POWER ELECTRONICS APPLICATIONS ENGINEER, DYNEX SEMICONDUCTOR

HVDC TECHNOLOGY facilitates the transmission of large amounts of power over long distances using direct current. There are two primary HVDC technologies: Line-Commutated Converters (LCC) based on thyristors, and self-commutated Voltage Source Converters (VSC) based on IGBTs. LCC-based HVDC systems consume reactive power and require large AC filters, necessitating connection to a strong power grid. Reversing power flow also requires changing the DC voltage polarity, meaning all terminals must switch simultaneously, making them unsuitable for multi-terminal HVDC networks. They are therefore mainly used for high-power, long-distance, point-to-point links where power flows predominantly in one direction, such as bulk transmission from remote generation sites to major consumption centres.

MMC-based VSC-HVDC systems produce very low harmonic distortion, requiring only modest high-frequency AC filters. They can continuously generate or absorb reactive power, interconnect asynchronous grids, and maintain voltage even on very weak or "dead" networks. Unlike LCC, reversing power flow in VSC is achieved by changing the current direction while keeping the DC voltage polarity constant, which makes multi-terminal and meshed HVDC networks practical. These attributes make VSC technology the preferred choice for some renewable generation—particularly offshore wind farms – and for providing flexible grid interconnections.

MMC-based VSC-HVDC systems, as shown in Figure. 1, require various power semiconductor devices – including IGBT and FRD modules – to perform voltage switching. Bypass thyristors may also be used to reduce current stress on the modules during DC-side faults by providing a controlled bypass.

These systems demand semiconductor devices that are not only high-performing, but also robust, maintainable, and space-efficient. In this context, the Press-Pack IGBT (PPI) has emerged as the preferred solution over conventional encapsulated



➤ Figure 1. MMC VSC-HVDC Systems.

IGBTs with bond wires—particularly in high-reliability, mission-critical HVDC applications.

This article discusses the mechanical, electrical, and operational advantages of PPIs. It highlights how their integration into spring-loaded stacks, ease of maintenance, and superior thermal management and fault-tolerant behaviour contribute to enhanced system robustness, lower lifecycle costs, and improved overall efficiency.

Introduction to IGBT Packaging in HVDC

In VSC HVDC applications, where IGBT modules are subjected to extreme electrical and thermal stress, two primary packaging types are commonly used, as shown in Figure. 2:

- **Encapsulated (Plastic) IGBT Modules:**
  Fully packaged modules that rely on bond wires, PCB, and solder layers for electrical connections between the chips and terminals. They require external gate and auxiliary wiring, as well as robust mounting and thermal interface strategies.

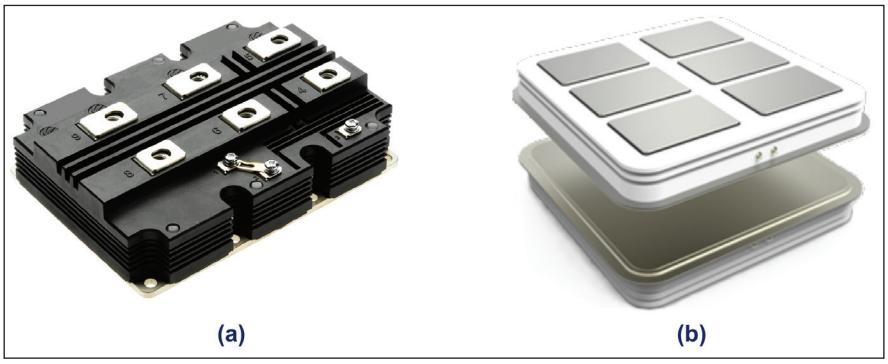
- **Press-Pack IGBT Modules (PPI):**
  Metallurgically bonded, pressure-contact devices that enable direct electrical and thermal connection under uniform clamping force and are optimised for series connection.

While both technologies are capable of handling high voltage and current demands, PPIs offer distinctive mechanical and system-level advantages — including superior thermal performance, ease of maintenance, and improved fault tolerance — which are becoming increasingly important in modern VSC HVDC topologies.

4.1 Structural and Assembly Advantages of Press-Pack IGBTs

Encapsulated IGBT modules may seem easier to mount, as they typically require only screwing down. However, each replacement still involves wiring, bolting, and applying thermal interface materials, which can be time-consuming.

PPIs are designed for direct press-contact operation, eliminating the need for thermal interface materials and extensive external wiring. PPIs



➤ Figure 2. Packaging solutions for IGBT modules in VSC HVDC applications. (a) Encapsulated IGBT module. (b) Press-Pack IGBT module.

can be assembled into spring-loaded stacks, which ensure uniform pressure distribution and consistent electrical and thermal contact across all devices. This modular and clamped approach not only enhances system integration but also supports rapid configuration and field replaceability, making PPIs particularly well-suited for high-reliability HVDC systems where downtime must be minimised.

4.2 Maintenance and System Uptime Benefits

To support maintainability in mission-critical HVDC systems, PPIs offer several practical advantages over encapsulated IGBT modules, particularly in the areas of field serviceability and condition monitoring.

These are detailed in the following subsections:

4.2.1 Field replaceability

- PPIs allow non-destructive disassembly and individual device replacement within a clamped stack, without disturbing thermal interfaces or mounting assemblies.
- In contrast, replacing an encapsulated module typically requires unbolting the unit, cleaning and reapplying thermal paste, and remaking all electrical and cooling connections — resulting in a longer maintenance time.

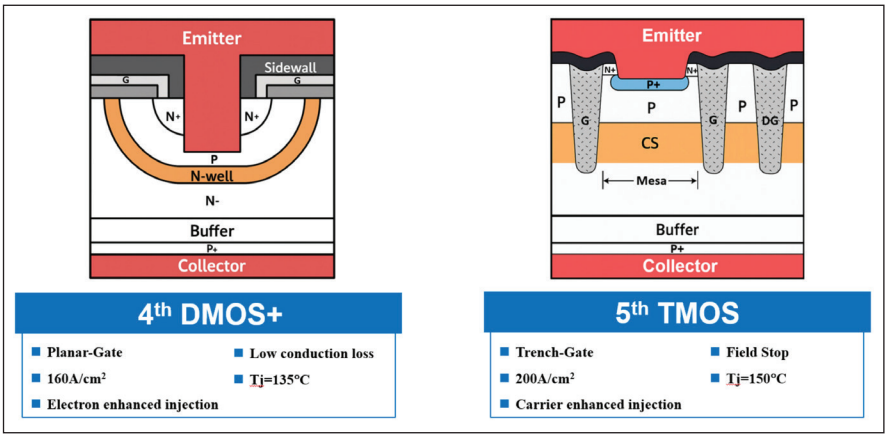
4.2.2 Visual inspection and predictive maintenance

- PPIs allow visual access to contact surfaces and support contact resistance monitoring, enabling more predictive maintenance strategies.
- PPIs integrate well with intelligent stack assemblies featuring real-time health diagnostics.

4.3 Robustness and Reliability

Beyond maintainability, the intrinsic structural advantages of PPIs also translate into superior fault tolerance and operational reliability.

The following sections outline key benefits related to short-circuit performance and endurance under demanding thermal cycling conditions:



➤ Figure 3. Trench-gate vs planar-gate for PPIs.

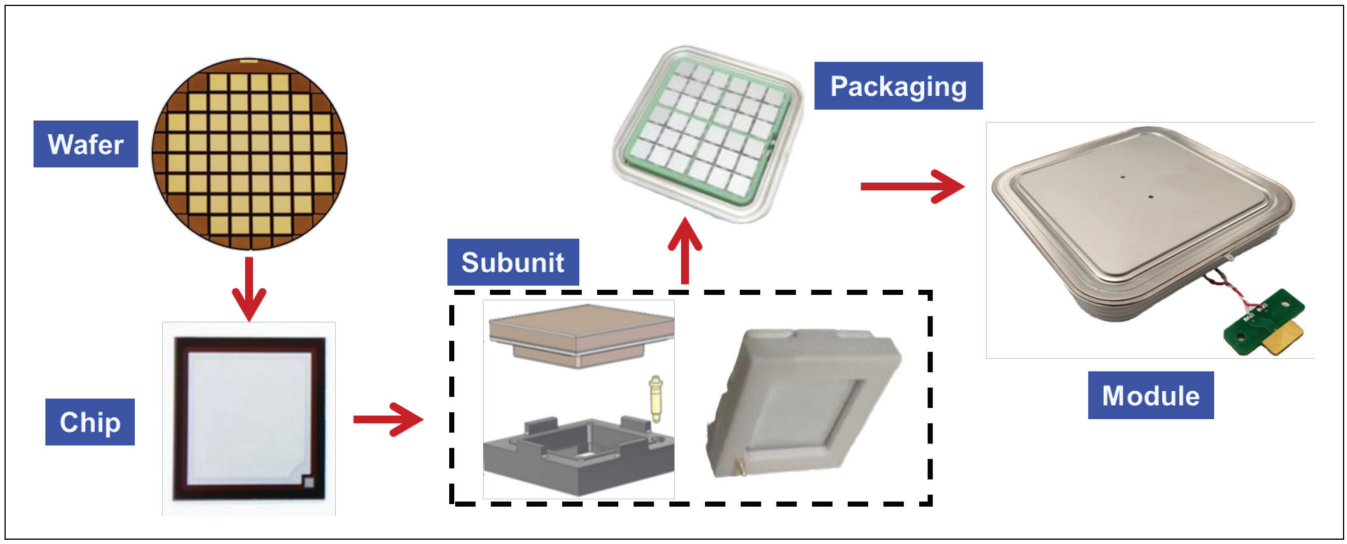


Figure 4. PPI 1.0 packaging steps.

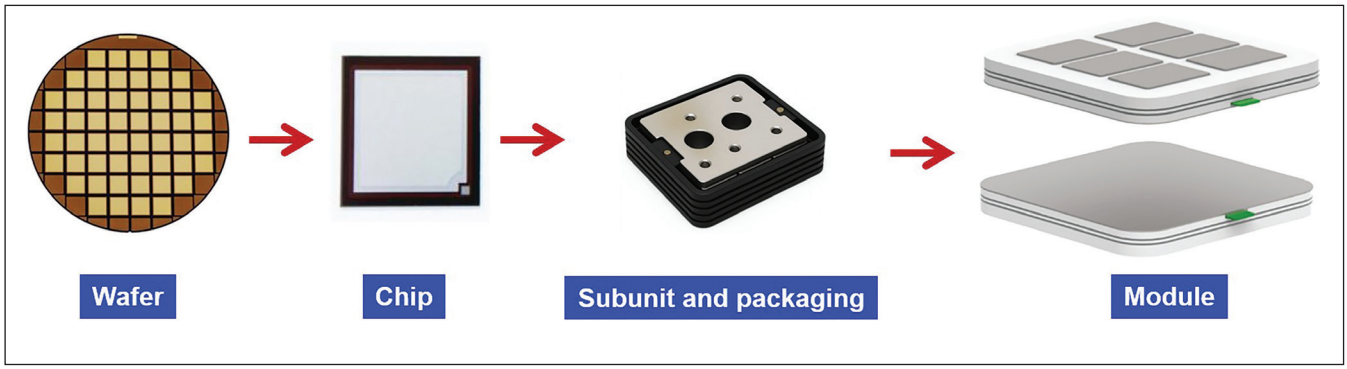


Figure 5. PPI 2.0 packaging steps.

4.3.1 Enhanced surge current capability

- Since PPIs do not use bond wires, they tend to be more robust under surge current conditions.

4.3.2 Enhanced short-circuit capability

- Press-pack devices are designed to fail short in most cases, enabling controlled bypass and system continuity.
- Encapsulated IGBTs may fail open-circuit, leading to converter-level outages or loss of redundancy.

4.3.3 Thermal cycling endurance

- Unlike encapsulated IGBT modules with bond wires, PPIs eliminate internal wire bonds – a common point of failure under cyclic loading. This design offers higher mechanical integrity and longer operational lifetimes, particularly under repetitive pulsed loads and fault conditions.
- Such reliability is critical for offshore wind power and its connection to the grid via remote HVDC systems, where frequent load variations are typical.

4.4 Efficiency and System-Level Cost Impact

Alongside reliability and maintainability, system-level efficiency and cost are critical considerations in HVDC applications. The following sections compare PPIs and encapsulated IGBTs in terms of losses and overall lifecycle economics:

4.4.1 Efficiency comparison

- PPIs benefit from slightly lower thermal impedance, which helps limit temperature rise. This in turn keeps the on-state voltage lower, directly reducing conduction losses and stress under high-load operation.
- The stack's intrinsic symmetry helps series-connected PPIs share voltage more evenly, enabling simpler active-balancing networks and reducing their power loss.

4.4.2 Cost comparison

Cost-wise, encapsulated IGBT modules are cheaper upfront due to standardised mass production and simpler mounting. However, PPIs, while more expensive initially, tend to offer lower long-term maintenance costs. Their robust, bond-wire-free design provides longer service life, superior thermal endurance, and fewer replacements.

Additionally, their lower losses can reduce operational energy costs — all contributing to a potentially lower total cost of ownership in demanding HVDC applications.

Dynex PPI Advancement for HVDC Applications

Dynex offers a comprehensive portfolio of high-voltage PPI module options specifically designed for HVDC VSC applications, with voltage ratings from 4.5 kV to 6.5 kV and current capabilities up to 5000 A.

5.1 Chip advancement

Dynex, in collaboration with CRRC, has recently released the 5th generation of Dynex IGBT chip technology for its PPI product line, marking a significant advancement in device performance and robustness. As shown in Figure. 3, this generation adopts Trench-Gate architecture, delivering superior current density of up to 200 A/cm^2 compared to the previous Planar-Gate design, which offered 160 A/cm^2.

The integration of carrier-enhanced injection and Field Stop technology enables better control of the electric field within the device, leading to lower switching and conduction losses. These advancements make the latest Dynex 5th-generation TMOS chips now available in press-pack format – ideal for demanding HVDC applications. With higher efficiency, improved thermal performance, and increased ruggedness, these new-generation chips solidify Dynex's position in delivering reliable and high-performance semiconductor solutions for next-generation power transmission systems.

5.2 Packaging advancement

Historically, Dynex—like many manufacturers – used 'Hockey Puck style' (round-shaped) Press-Pack IGBT designs, which were standard in early HVDC applications. However, as performance demands increased and packaging efficiency became more critical, the design transitioned toward a square-shaped format. This shift allowed for better utilisation of area, improved current distribution, and more efficient heat spreading, particularly beneficial for high-current, high-voltage systems.

Dynex's first-generation Press-Pack IGBT (PPI 1.0), developed with CRRC Semiconductor, laid the foundation for robust HVDC device design. As shown in Figure. 4, this generation features a sealed ceramic casing, double-sided Ag sintering, and a flexible spring-loaded contact system to ensure uniform pressure distribution across all subunits. The modular design allows for a variable number of subunits, enhancing design flexibility and enabling thermal and electrical balancing within the device. With a maximum voltage and current rating of 4500 V and 3000 A, Press-Pack 1.0 provided an exceptionally reliable

Dynex Semiconductor Ltd

DYNEX SEMICONDUCTOR LTD is a global supplier of high-power semiconductor devices, with a strong heritage in the design, manufacture, and application of power electronics—particularly in the field of power semiconductor manufacturing. Headquartered in Lincoln, UK, Dynex has been at the forefront of semiconductor innovation for over half a century, delivering solutions for critical applications.

As a wholly owned subsidiary of CRRC Corporation Limited, one of the world's largest suppliers of rail transit equipment, Dynex benefits from a unique strategic position that bridges advanced Chinese industrial capabilities with British engineering excellence. This cross-continental collaboration empowers Dynex to contribute both regionally and globally, developing and delivering robust, high-performance semiconductor solutions that meet the demanding performance, safety, and reliability requirements of today's high-power systems.

Dynex's extensive product portfolio includes a broad range of high-power semiconductor devices such as silicon IGBT and SiC MOSFET modules, Si fast recovery diode (FRD) modules, press-pack IGBTs, disc thyristors, disc diodes, disc FRDs, IGCTs, and—last but not least—bipolar modules, all engineered to support high-voltage, high-current applications with long-term operational stability.

In addition to device manufacturing, Dynex's Power Assembly division offers a wide range of integrated power assembly products and provides strong engineering capabilities for bespoke design solutions, tailored to meet customer-specific performance and environmental requirements.

Widely recognised for both its high product quality and in-depth application engineering support, Dynex stands out as a trusted partner for customised power electronics solutions. By combining its long-standing manufacturing legacy with ongoing investment in advanced R&D, Dynex continues to play a pivotal role in the electrification and digital transformation of transportation and energy infrastructure across the globe.

Application context: Versatile solutions with a strategic focus on HVDC

Dynex supplies high-power semiconductor devices to a broad spectrum of applications, including rail traction, EVs, industrial drives, renewable energy, and grid infrastructure. With a portfolio that spans nearly all standard voltage ratings, current levels, and industry-common package outlines, Dynex offers reliable, drop-in solutions that align with global application needs.

In addition to its standard product range, Dynex also offers custom and bespoke designs tailored to specific electrical, mechanical, or thermal requirements. This capability allows the company to address unique challenges in specialised systems, making it a preferred partner for projects requiring more than just standard components.

While Dynex remains active across multiple sectors, High Voltage Direct Current (HVDC) transmission has emerged as a key strategic focus. As the need for long-distance, high-capacity power transmission grows – particularly in applications such as offshore wind integration and cross-border interconnects—HVDC offers an efficient and scalable solution.

Dynex supplies a comprehensive range of power semiconductor devices suited for HVDC systems, including thyristors, FRDs, bypass thyristors, IGCTs, encapsulated IGBT modules, and press-pack IGBT modules. In particular, Dynex is advancing press-pack IGBT technology to meet the extreme voltage, thermal, and reliability demands of HVDC applications, with a strong emphasis on supporting Modular Multilevel Converter (MMC) topologies.

solution for early HVDC and flexible DC grid systems. This foundational platform directly influenced the development of the more advanced Press-Pack 2.0, incorporating many of its proven mechanical principles while introducing significant thermal and electrical enhancements.

To support the next generation of high-power and high-reliability HVDC systems, Dynex has introduced Press-Pack IGBT 2.0 (PPI 2.0) – a significant upgrade over traditional press-pack designs. As shown in Figure. 5, this new generation incorporates several advanced features, including flexible spring-loaded pressing, double-sided chip soldering, higher operating junction temperature, and a more thermally efficient layout.

The new design achieves over 20% reduction in thermal resistance, allowing for improved cooling and higher power density. Additionally, the devices have successfully passed destructive fault condition testing (at 24 mF and 4400 V), confirming robustness. Furthermore, the weight has been reduced by 25.2% compared with PPI 1.0.

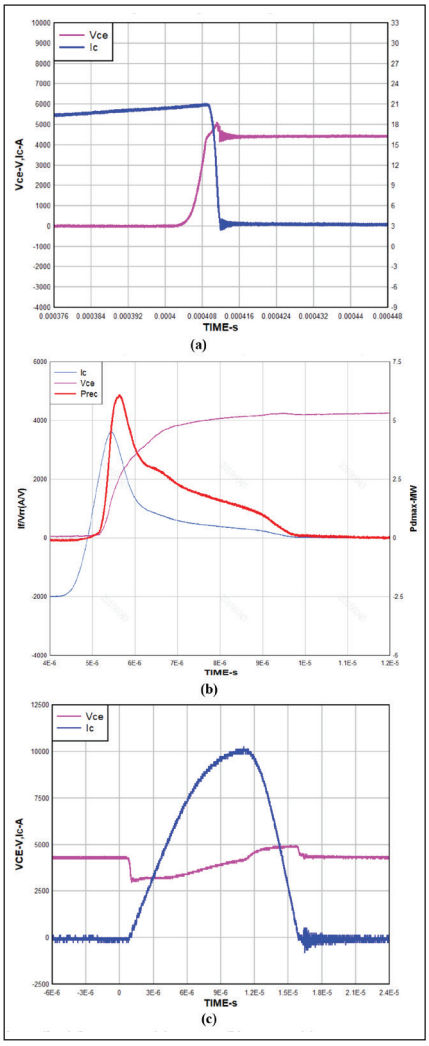
With maximum ratings of 4500 V/5000 A and 6500 V/3000 A, PPI 2.0 products are well-suited for mission-critical HVDC applications, where performance, fault tolerance, and maintainability are essential.

5.3 Validation and Standards

To ensure the reliability, consistency, and performance of its PPIs, Dynex – through its collaboration with CRRC Semiconductor – employs a comprehensive suite of validation and test procedures covering all stages of the product lifecycle. A few of these tests include:

- Chip-level defect detection and probe testing.
- High-temperature static and dynamic testing
- Safe operating area (SOA) testing Electrical insulation and integrated parameter checks
- Full thermal resistance measurements, validated using JESD51-14-2010 for junction-to-case thermal path analysis

Dynex PPIs are tested across voltage ranges from 4500 V to 6500 V, with routine tests and reliability assessments conducted at both chip and module



➤ Figure 6. Selected test results for 6.5kV/2kA PPI 2.0. (a) RBSOA. (b) RRSOA. (c) SCSOA.

levels. All testing aligns with relevant international standards, including IEC 60747-9 for IGBT devices. This rigorous approach ensures that each device meets the high reliability and safety standards demanded by HVDC systems and other mission-critical power applications.

In addition to rigorous routine testing, Dynex's PPIs have undergone comprehensive SOA validation to ensure robust performance under fault and extreme operating conditions.

As shown in Fig. 6, the 6.5kV/2kA PPI demonstrate excellent Reverse Biased SOA (RBSOA), safely turning off at 4.4 kV and 6000 A, exceeding typical test requirements.

The Reverse Recovery SOA (RRSOA) confirms that the freewheeling diode structure can withstand very high energy dissipation during reverse recovery. Furthermore, the Short-Circuit SOA (SCSOA) testing shows the device enduring 15 µs of short-circuit duration at 4.4 kV, well above the industry requirement of around 10 µs.

These results confirm that the devices possess high ruggedness, with stable operation across a wide range of stress conditions. Together with compliance to IEC 60747-9 and thermal validation via JESD51-14-2010, these SOA waveforms provide strong evidence of the devices' reliability for HVDC and other mission-critical applications.

Conclusion

In the transition toward more flexible and resilient HVDC networks, PPIs offer a compelling alternative to encapsulated IGBT modules. Their inherent modularity, superior reliability, and service-friendly design make them especially well-suited for modern VSC systems that require high performance with minimal downtime and reduced operational complexity.

By adopting Press-Pack IGBTs, operators can significantly reduce component-level failure risks while improving overall system efficiency and lifetime economics — a decisive advantage in today's utility-scale energy infrastructure.

Dynex, in collaboration with CRRC, has developed a wide range of power semiconductor devices tailored for HVDC systems. This article has discussed some of the recent advancements and features of Dynex Press-Pack IGBT technology, including:

- Hermetic packaging for enhanced reliability in harsh environments
- Both square and round housing options
- Double-sided Ag sintering for improved thermal and mechanical performance
- Flexible spring pressure design
- Excellent surge handling and short-circuit tolerance
- Short-Circuit Failure Mode (SCFM) with extended lifetime
- Optional integration with anti-parallel diodes
- Low conduction losses enabled by advanced trench IGBT chips
- High voltage and current ratings for demanding applications.

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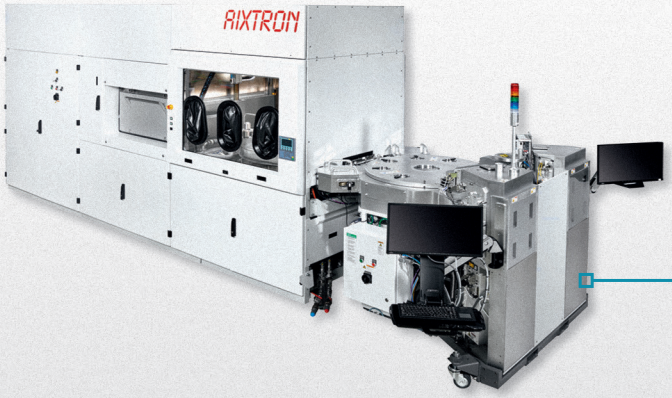

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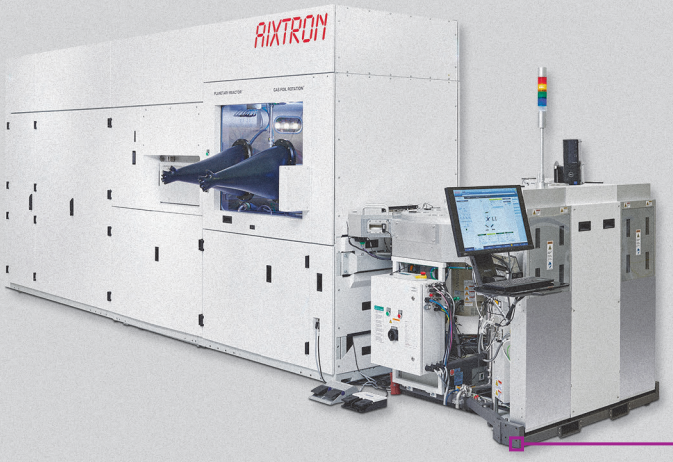

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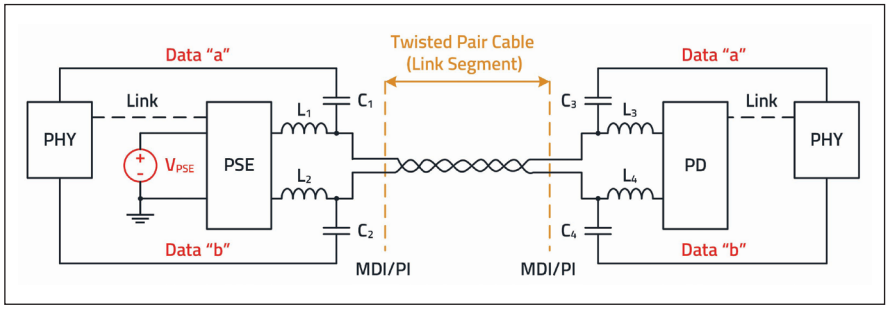
Ethernet communication

Single-pair Ethernet is becoming increasingly popular in industrial networking due to the simplified cabling with just one twisted pair of wires. When power is added to this, the SPE transmission standard with Power-over-Data-Lines is unbeatably simple. The following reference design shows how to implement SPE with PoDL.

THE REFERENCE design for single-pair Ethernet (SPE) with Power-over-Data-Lines (PoDL) from Würth Elektronik (WE) is a system that can transmit data between two points via a two-wire cable. The central device supplies the peripheral device with power via the same two-wires over which the data is simultaneously transmitted.

Single-pair Ethernet is an emerging standard for Ethernet communication that uses only one pair of wires for data transmission, as opposed to traditional Ethernet, which typically uses up to four pairs of wires. This makes SPE suitable for applications where space and weight constraints exist, such as automotive, industrial and IoT (Internet of Things) devices.

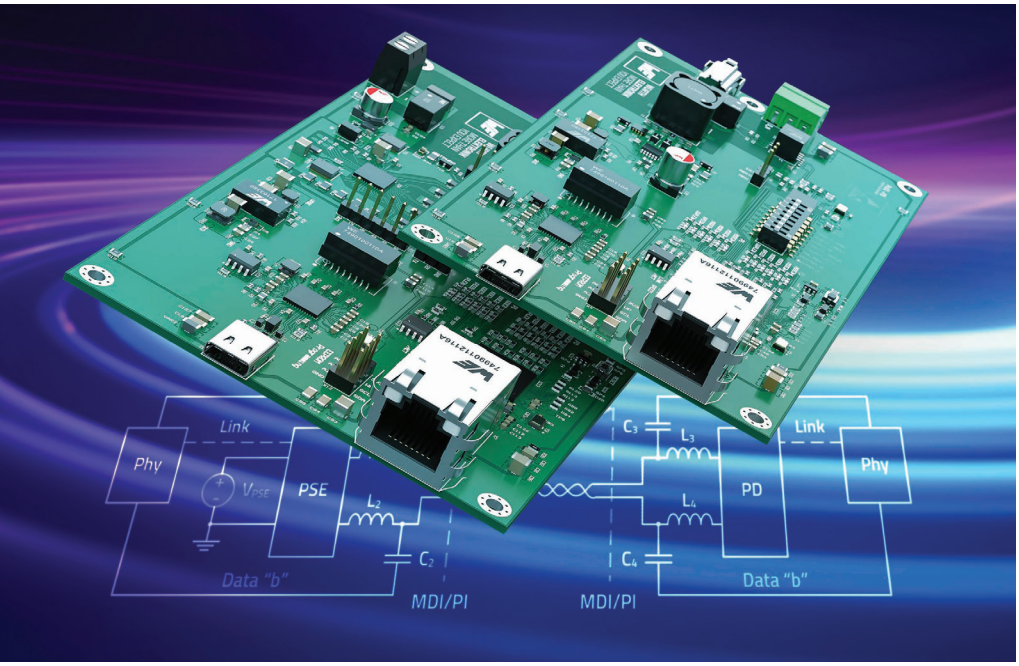
Power over Ethernet (PoE) is a technology that makes it possible to transmit electrical energy together with data via Ethernet cables [1].



➤ Figure 1: Basic circuit of an SPoE system.

This eliminates the need for separate power cables, which simplifies installation and reduces costs, especially for applications such as IP cameras, VoIP telephones and wireless access points.

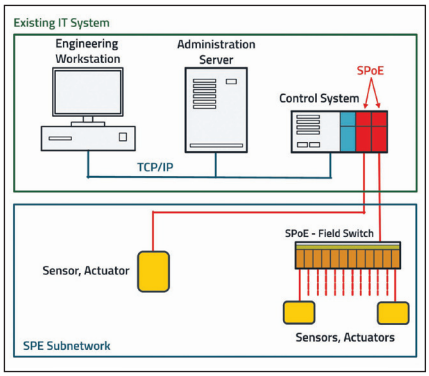
Power-over-Data-Lines (PoDL) extends the concept of PoE to Single-Pair-Ethernet (SPE) by enabling power to be supplied via the single twisted pair cable used for data transmission in SPE systems. This allows devices connected via SPE to be powered via the same cable used for data transmission. In the literature, Single Pair with PoE is often also referred to as SPoE, which is used in the following explanations.



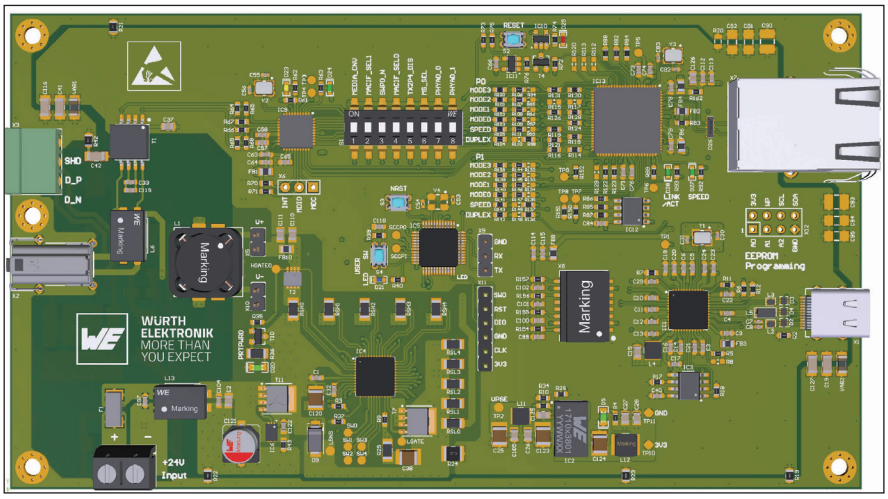
SPoE basics

SPoE differs from PoE in its definition and implementation. It includes:
a unique power coupling technique used in a 2-wire circuit. simultaneous transmission of power and data via a symmetrical, twisted pair of wires.

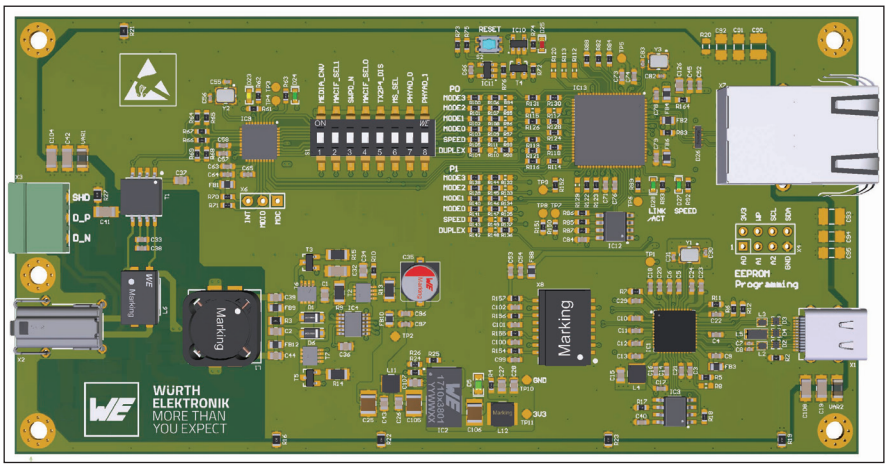
The data connections are realized via a single pair of wires, AC-coupled at each end to avoid ground loops. The PoE system transmits power simultaneously with the data. Figure 1 shows the basic circuit of the SPoE system. On the left-hand side of the circuit diagram is the Power Source Equipment (PSE) with the PHY (physical layer in the OSI model). On the right-hand side is the Powered Device (PD, load) and another PHY. The PHYs establish the data connection and the PSE supplies the PD with power. The data connection is capacitively decoupled (C1 - C4) from the power and the power supply is inductively decoupled (L1 - L4) from the data. The interface is referred to as a "Media Dependent Interface" or "Port Interface"



➤ Figure 2: Adding SPoE devices to an existing IT system.



➤ Figure 3: Top side of the PSE board, the SPE interface is located on the left, the connection can be made either via a 3-pin plug-in terminal or an SPE connector.



➤ Figure 4: Top side of the PD board, on the left is the SPE interface, the connection is made either via a 3-pin terminal or an SPE connector.

(MDI/PI).
The integration of power supply alongside data transmission requires a robust, classification-based power supply protocol to ensure compatibility between power sourcing equipment (PSE) and powered devices (PD). The protocol is defined in IEEE 802.3cg (SPoE, 2019) and explained in detail in [2].

The electrical requirements for SPoE are defined in the following IEEE standards:

- IEEE 802.3cg (10BASE-T1): Bandwidth 0.1 to 20 MHz, range up to 1000 m.
- IEEE 802.3bw (100BASE-T1): Bandwidth 0.3 to 66 MHz, range up to 40 m.
- IEEE 802.3bp, (1000BASE-T1): Bandwidth 1 to 600 MHz, range up to 40 m.

The cables used for SPoE differ from the standard cables used for Ethernet [2].

SPoE requires cables that are defined in IEC 61156, i.e. “multicore and balanced pair/quad cables for digital communication”. Standard CAT 6 or CAT 7 cables, even if they are shielded, are not suitable.

SPoE can be integrated into a mixed system with common industrial Ethernet protocols such as Ethernet/IP, Profinet and EtherCAT and can provide a simultaneous power supply for end devices. Figure 2 shows a typical setup.

SPoE hardware topology

The hardware topology of the SPoE reference design RD041 consists of two boards, the PSE circuit and the PD circuit. The interfaces with primary transient protection, common mode chokes, transformers and secondary transient protection to the PHY are the same for the PSE and the PD.
Power and data are coupled together at the interface via a power coupling network.

The SPE transmission path operates at a data rate of 10 Mbit/s with an amplitude of approx. 2.5 VPP, the operating voltage on the two-wire line is 20 to 24 VDC. The PSE and PD implementation are described in detail in the paper of the reference design RD041 [2].
Figure 3 shows the top side of the WE PSE board, Figure 4 the top side of the WE-PD board.

Further information on the implementation of the PSE and PD boards with detailed circuit information can be found at [2]. The reference design presented has not been tested in 1000 m range mode, so only operation with cable lengths of up to 100 m is currently recommended.

FURTHER READING / REFERENCE

➤ [1] Zenkner, H.: GB PoE+-Ethernet-USB-Adapter for industrial use under EMC aspects. Reference design RD022 from Würth Elektronik: www.we-online.com/RD022
➤ [2] Zenkner, H.: Design of a single-pair Ethernet system with Power-over-Data-Lines (SPoE). Reference design RD041 from Würth Elektronik: www.we-online.com/RD041

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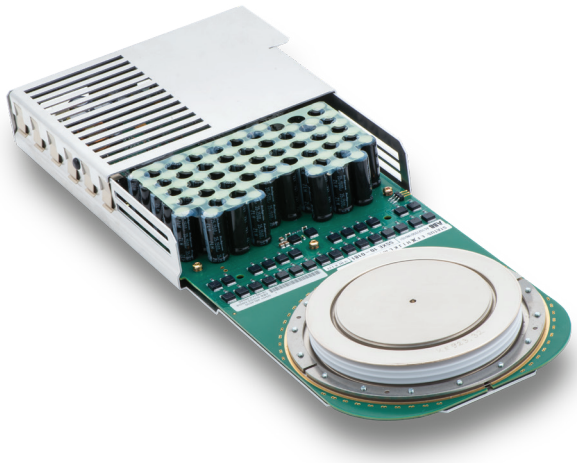

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