POWER ELECTRONICS WORLD

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Pandemic lessons have reshaped power device and IC manufacturing

ISSUE I 2022

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INSIDE

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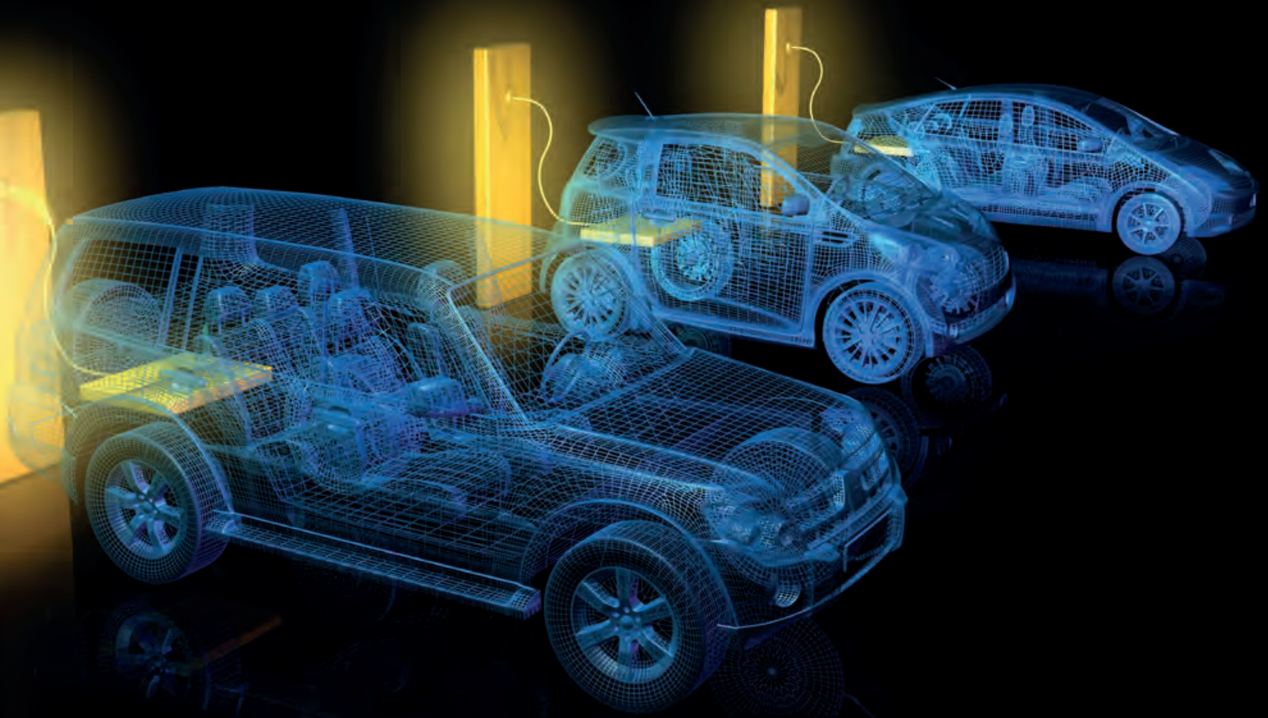
Vertical GaN p-n diodes combine excellent efficiencies with incredibly fast protection from electromagnetic pulses



Best performance for next generation SiC power electronics to address global mega trends

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VIEWPOINT

BY MARK ANDREWS TECHNICAL EDITOR

Demand for power electronics will continue driving 2022 IC sales

LOOKING BACK AT 2021 we saw a year that demonstrated the vital role semiconductors play in more end use products than ever before. Automotive power electronics and other ICs, from microcontrollers to EV inverters, took center stage when demand outstripped supply.

In a January report, IC Insights said 2021 chip sales grew 25 percent; the researchers forecast growth will likely 'fall' to 11 percent this year—a figure that would have been considered 'outstanding' just years ago.

How is 2022 progressing? The Semiconductor Industry Association (SIA) reported in March that global IC sales increased 26.8 percent year-on-year this January, which is the second highest first quarter start in history. The global supply chain is still disentangling from pandemic-induced bottlenecks; however, there are positive signs even while the war in Ukraine that began when Russia invaded may have impacts across Europe and the world that cannot be predicted at this time.

Regardless how the overall semiconductor market performs, can power IC makers build enough devices this year despite public perceptions that production shortfalls kept automakers from addressing 2021 demand? Ford Motor Company reported that the lack of 'certain' semiconductors keep it from selling up to 1.1 million vehicles in 2021, but was a lack of power devices the pain point?

According to the February update of IC Insights' Semiconductor Industry Flash Report, the common perception that chip makers were largely responsible for fewer automotive buying options last year is not the whole story. Semiconductor manufacturers in fact shipped 30 percent more ICs to automotive customers last year compared to 2020. And even in 2020, a

challenging year by any measure, more automotive ICs were shipped than in 2019. A 30 percent increase is sizeable, so why the disconnect?

Consider that the number of semiconductors going into new vehicles increases every model year and the fact that an electric vehicle uses more than twice the ICs of conventional automobiles.

In this edition of Power Electronics World we examine 2021 milestones and gauge prospects for 2022, including the story behind power ICs and their evolving role in transportation along with the latest research and new product updates.

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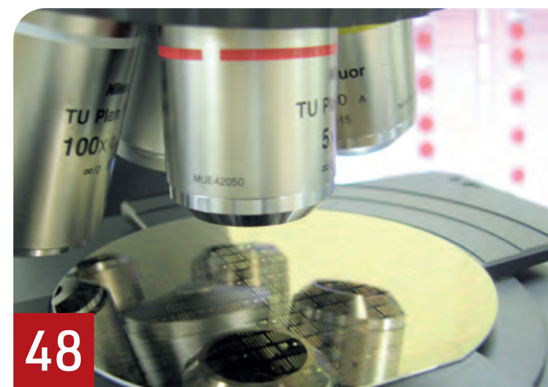

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Toshiba introduces a new size-reduced MOSFET gate driver

TOSHIBA ELECTRONICS EUROPE GmbH has introduced a new MOSFET gate driver IC TCK421G that controls the gate voltage of external N-channel MOSFETs based upon the input voltage.

The MOSFET gate driver is suitable for configuring a power multiplexer or a load switch circuit equipped with reverse-current blocking by being combined with a back-to-back connection of external N-channel MOSFETs.

The TCK421G incorporates a charge pump circuit that supports a wide range of input voltages (VIN) from 2.7 to 28.0V, providing a stable supply of 10 V to the gate-source voltage of external MOSFETs thereby facilitating the switching of large currents. The typical input quiescent current in the ON state (IQ(ON)) is as low as 140 µA while the standby current in the OFF state (IQ(OFF)) is just 0.5 µA. In addition, the

TCK421G contains an overvoltage and undervoltage lockout function. The gate drive voltage can be selected to suit the application.
Housed in the chip scale WCSP6G package, the device has a footprint of just 1.2 mm x 0.8mm and a height of 0.35 mm. This is one of the smallest packages in the industry and allows use in densely packed devices such as wearables and smartphones. The TCK421G is the first product launched in a series that will eventually comprise six devices. Due to its high efficiency and small size, the new driver can be used in a wide range of applications including battery powered, consumer and industrial equipment.

Lucid Air EV charging powered By Rohm

ROHM SEMICONDUCTOR has announced that Lucid, an advanced luxury electric vehicle company headquartered in California, is using its SiC MOSFET in the ground-breaking Lucid Air.

The Wunderbox, the main on-board charging unit in the Lucid Air, integrates a DC-DC converter and the bi-directional On-Board Charger (OBC), where an advanced power factor correction circuit is capable of operating at high switching frequencies thanks to the performance of the SiC MOSFET. The improved performance at high frequency and high temperature of Rohm's SCT3040K and SCT3080K SiC MOSFETs have helped Lucid to reduce the size of the design, and to reduce power losses, which results in high charging efficiency.

Lucid Air, is a luxury sedan with a California-inspired design underpinned by race-proven technology. Customer deliveries of Lucid Air, which is produced at Lucid's new factory in Casa Grande, Arizona, are underway. The Lucid Air was named the 2022 MotorTrend Car of the Year. Additionally, an independent article in InsideEVs confirmed the Lucid Air's charging capabilities. For example, when connected to DC fast chargers, they found it takes approximately 22 minutes to deliver a charge which will enable select Lucid Air models to cover 300 miles. The SiC MOSFET switched OBC can deliver up to 19.2 KW AC charging, adding up to 80 miles of range per hour.. "It was important for Lucid to form strategic alignments with key EV power device suppliers to ensure our future success. Rohm is one of the world's leading suppliers of SiC technology, with strong technical support.
We were impressed with Rohm's strategic investments to increase the production capacity of SiC products, and its development of next generation technologies," said Eric Bach, SVP of Product and chiefeEngineer, Lucid Group. "Lucid values the close collaborative relationship with Rohm in this work."

Keysight extends high-speed digital 800G test portfolio

KEYSIGHT TECHNOLOGIES has expanded the company's portfolio of high-speed digital 800G test solutions to enable the optical transceiver ecosystem to improve the power efficiency of components and modules used in data centre equipment.

Hyperscale data centres are adopting 800G, the latest data centre connectivity technology, to address a rise in the use of cloud-native, 5G, artificial intelligence (AI) and internet of things (IoT), as well as data-hungry applications such as video conferencing, streaming and digital entertainment.

The latest addition to Keysight's existing portfolio of 800G test solutions are new design and validation solutions that support multimode interfaces, which are critical for an energy efficient data centre infrastructure. The 800G multimode test solutions uniquely support high-speed data interconnect speeds of up to 100 gigabit per second (Gbps).

"An ever-increasing growth in data traffic, compounded with data centres' need to reduce their energy footprint, has prompted Keysight to launch the new 800G multimode test solutions," said Dr. Joachim Peerlings, vice president of Network and Data Centre solutions at Keysight Technologies. "These new solutions will help reduce power consumption in data centre equipment. Energy conservation and efficiency in data centres has a significant positive impact on the health of the planet."

In December 2020, Keysight launched industry-first 800G test solutions to help speed development of next generation data centre technologies.

The 800G multimode test solutions enable users to verify the performance of a wide range of optical transceiver modules and components, including vertical-cavity surface-emitting lasers (VCSELs), photodiodes, modulator drivers, transimpedance amplifiers (TIAs) and physical layer (PHY) chips.

Imec, KU Leuven and PragmatIC Semiconductor demonstrate fast 8-bit flexible microprocessor

AT THE 2022 International Solid-State Circuits Conference (2022 ISSCC), imec, a research and innovation hub in nanoelectronics and digital technologies, KU Leuven, and PragmatIC Semiconductor, presented the fastest 8-bit microprocessor in 0.8 µm metal-oxide flexible technology capable of running real-time complex assembly code. The microprocessor was implemented with a unique digital design flow that allowed the creation of a new standard cell library for metal-oxide thin-film technologies – relevant for designing a broad range of IoT applications. The robust thin-film technology offered by imec's foundry partner PragmatIC Semiconductor was key to integrate the approximately ~16,000 metal-oxide thin-film transistors on a 24.9mm2 flexible chip.

Flexible electronics based on thin-film transistor technology is preferred over Si CMOS-based electronics for applications requiring low-cost, thin, flexible and/or conformable devices. The technology already made inroads in, e.g., health-patch sensors and RFID labels, and as a driver for flat panel displays. The missing piece is a flexible microprocessor to perform more complex signal processing calculations – as such adding compute functionality to a broad range of IoT applications. Imec has designed a flexible 8-bit microprocessor in 0.8 µm indium-gallium-zinc-oxide (IGZO)-transistor technology, able to perform such complex computations.

To fabricate the flexible microprocessor, imec teamed up with foundry partner PragmatIC, whose unique FlexIC Foundry offers rapid prototyping and high-yield volume manufacturing of flexible integrated circuits. Brian Cobb, VP Product Development at PragmatIC: "Until recently, there was no mature and robust technology available for integrating such a large number of thin-film transistors with sufficient yield. Our pioneering FlexLogIC fab now enables the rapid turnaround of such complex new designs at an ultra-low cost, delivering ICs on thin and flexible wafers. Our FlexIC Foundry service continues to be instrumental in enabling design teams like the one at imec to expand the range of design and use cases for flexible electronics."

This research was performed in the framework of the ERC starting grant FLICs under grant agreement No 716426 under the European Union's Horizon 2020 research and innovation programme.

II-VI accelerates investment in SiC

II VI, a maker of wide-bandgap semiconductors, is accelerating its investment in 150 mm and 200 mm SiC substrate and epitaxial wafer manufacturing with large-scale factory expansions in Easton, Pennsylvania, and Kista, Sweden. This is part of the company's previously announced $1 billion investment in SiC over the next 10 years.

The global urgency to decarbonize energy consumption is accelerating the "electrification of everything" and driving a sea change in power electronics technology with the adoption of SiC, a wide-bandgap material that enables more efficient and compact power electronics subsystems than those based on silicon. To meet the accelerating global demand for SiC power electronics, II-VI will significantly build out its nearly 300,000 square foot factory in Easton, to scale up the production of its state-of-the-art 150 mm and 200 mm SiC substrates and epitaxial wafers.

Easton's 150 mm and 200 mm SiC substrate output is expected to reach the equivalent of 1 million 150 mm substrates annually by 2027, with the proportion of 200 mm substrates growing over time. The expansion of the epitaxial wafer capacity in Kista is aimed at serving the European market.

"Our customers are accelerating their plans to intersect the anticipated tidal wave of demand for SiC power electronics in electric vehicles that we expect will come right behind the current adoption cycle in industrial, renewable energy, datacenters, and more," said Sohail Khan, executive VP, New Ventures and Wide-Bandgap Electronics Technologies. "The Easton factory will increase II-VI's production of SiC substrates by at least a factor of six over the next five years, and it will also become II-VI's flagship manufacturing center for 200 mm SiC epitaxial wafers, one of the largest in the world."

II-VI will use its industry-leading epitaxial wafer technology developed in Kista. This technology is differentiated by its ability to achieve thick layer structures in single or multiple regrowth steps, which is ideally suited for power devices in applications above 1 kilovolt.

The Easton factory will be powered by an uninterruptible and scalable microgrid based on fuel-cell technology to provide high assurance of supply.

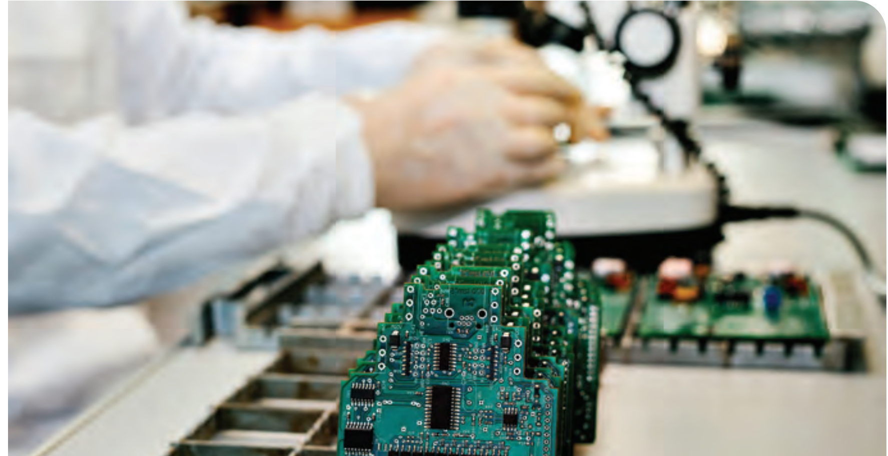
Ampleon boosts GaN-on-SiC HEMT transistor performance

AMPLEON has announced the release of two new broadband GaN-on-SiC HEMT transistors in the power classes of 30 Watts CLF3H0060(S)-30, 100 Watts CLF3H0035(S)-100. These high linearity devices are the initial products from our Generation 3 GaN-SiC HEMT process recently qualified and released to production.

The devices offer broadband high linearity features under low bias settings to raise the performance levels for broadband linearity (under -32dBc third-order intermodulation products at 5dB, and less than -42dBc at 8dB back-off from saturated power over a 2:1 bandwidth). Broadband linearity is vital for frequency-agile radios deployed in today's defense electronics for handling multi-mode communication waveforms (from FM through high-order QAM signals) with simultaneous application of countermeasure channels. These demanding applications require transistors with inherently better broadband linearity. Based on market feedback, the Ampleon Generation 3 GaN-on-SiC HEMT transistors meet these extended broadband linearity requirements.

In addition, the Generation 3 transistors are housed in a thermally enhanced package, which enables reliable operation and offers an extremely rugged VSWR withstand capability of up to 15:1 for a 30 Watt device. The ruggedness extends to Class A operation, common to instrumentation applications with saturated gate conditions while maintaining linearity over a wide dynamic range at extended frequency ranges. Ampleon's Generation- 3 GaN-on-SiC HEMT transistors set a new standard for high linearity GaN technology for broadband applications while maintaining excellent thermal and ruggedness features.

Toshiba to expand power semiconductor production capacity



TOSHIBA Electronic Devices & Storage Corporation ("Toshiba") has announced that it will construct a new 300-milimeter wafer fabrication facility for power semiconductors at its main discrete semiconductor production base, Kaga Toshiba Electronics Corporation, in Ishikawa Prefecture. Construction will take place in two phases, allowing the pace of investment to be optimized against market trends, with the production start of Phase 1 scheduled for within fiscal 2024. When Phase 1 reaches full capacity, Toshiba's power semiconductor production capacity will be 2.5 times that of fiscal 2021[1].

Power devices are essential components for managing and reducing power consumption in every kind of electronic equipment, and for achieving a carbon neutral society. Current demand is expanding on vehicle electrification and the automation of industrial equipment, with very strong demand for low-voltage MOSFETs (metal oxide semiconductor field effect transistors) and IGBTs (insulated-gate bipolar transistors) and other devices.

To date, Toshiba has met this demand growth by increasing production capacity on 200-milimeter lines, and expediting the start of production on 300-milimeter production lines from the first half of fiscal 2023[2] to the second half of fiscal 2022. Decisions on the new fab's overall capacity and equipment investment, the start of production, production capacity and production plan will reflect market trends.

The new fab will have a quake absorbing structure; enhanced BCP systems, including dual power supply lines; and the latest energy saving manufacturing equipment to reduce environmental burdens. It will also aim to achieve the "RE100" goal of 100% reliance on renewable energy. Product quality and production efficiency will be improved by introducing artificial intelligence and automated wafer transportation systems.

Going forward, Toshiba will expand its power semiconductor business and boost competitiveness by timely investments and research and development that will allow it to respond to fast growing demand, and to contribute to a low-energy society and carbon neutrality.

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Transphorm 1200V GaN Fet delivers 99% efficient switching

TRANSPHORM will demonstrate the latest R&D results from its 1200V GaN device at the IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD).

The 1200V GaN device delivers greater than 99 percent efficiency and performs well against a leading SiC MOSFET of similar on-resistance. Partially funded by the ARPA-E CIRCUITS program, Transphorm is developing the technology for electric vehicle mobility and infrastructure power systems as well as industrial and renewable energy systems.

This major milestone further strengthens Transphorm's ability to support the broadest range of power—from 45W to 10K+ kW – across the widest range of cross-industry applications when compared to any other GaN supplier today. The ISPSD presentation in May will provide detailed information of device configuration and performance analysis conducted using a hard-switched, synchronous boost half bridge topology. The initial 1200V GaN device in a TO-247 package has an RDS(on) of 70 milliohms and easily scales to lower resistance and higher power levels. Early results show notably low leakage with a breakdown voltage of greater than 1400V.

"Building on Transphorm's unique vertically integrated capability, our engineers have yet again pushed the limits of what's possible with GaN," said Umesh Mishra, CTO and Co-founder, Transphorm. "We aim to bring to market an ultra-high voltage, reliable GaN product that will give customers more choice when developing power systems.

Our 1200-volt GaN FET will enable excellent performance with greater designability and cost effectiveness than SiC solutions. We see this as an important milestone for the GaN power electronics industry."

"1200V GaN has been discussed within the industry for some time, but often perceived as rather difficult to achieve," said Isik Kizilyalli, associate director for technology at the Advanced Research Projects Agency – Energy (ARPA-E). "As part of the ARPA-E CIRCUITS program led by the Illinois Institute of Technology, the Transphorm team has demonstrated an important breakthrough, showcasing GaN performance at the 1200V device node with high efficiency 800Vswitching." Transphorm's 1200V FETs are expected to be available for sampling in 2023.

Soitec to expand manufacturing footprint

Soitec has announced today a new fabrication facility at its headquarters in Bernin, France, primarily to manufacture new SiC wafers which respond to key challenges of the electric vehicle and industrial markets. The extension will also support Soitec's 300-mm Silicon-on-Insulator (SOI) activities. The factory is to produce innovative SmartSiC engineered wafers developed by Soitec at the Substrate Innovation Center located at CEA-Leti in Grenoble, using Soitec's proprietary SmartCut technology.

Soitec says this new generation of SiC wafers adds significant value for industrial applications and electric vehicles. It allows to enlarge their driving range, shorten the charging time and diminish their cost.

With its SmartSiC products, Soitec is engaged with major SiC device makers and targets to generate first revenues in the second half of calendar year 2023.

"We expect that by 2030, around 40 percent of all new cars will be electric. Our unique, highly performant, sustainable and cost competitive SmartSiC solution addresses the industrial challenges, helps to optimise energy efficiency, and will accelerate the adoption of electric vehicles," says Paul Boudre, Soitec CEO.

"This investment is a major milestone for us as SmartSiC is set to be another growth engine for Soitec, and a driver of the transformation of the automotive and industrial markets."

EPC announces motor drive board for e-bikes

EPC has announces the availability of the EPC9167, a 3-phase BLDC motor drive inverter reference design board using the EPC2065 eGaN FET. The EPC9167 operates from an input supply voltage between 14 V and 60 V (nominal 48 V) and has two configurations – a standard unit and a high current version:

There are two versions. The EPC9167 standard reference design board is a 3-phase BLDC motor drive inverter board featuring the EPC2065 eGaN FET rated at 3.6 mΩ maximum RDS(on), 80 V maximum device voltage. This standard configuration uses single FETs for each switch position and can deliver up to 20 ARMS maximum output current.

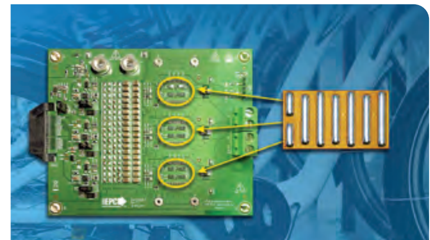
There is also a high current configuration, the EPC9167HC, which uses two paralleled FETs per switch position with the ability to deliver up to 42 Apk (30 ARMS) maximum output current.

Both versions of the EPC9167 contain all the necessary critical function circuits to support a complete motor drive inverter including gate drivers, regulated auxiliary power rails for housekeeping supplies, voltage, and temperature sense, accurate current sense, and protection functions. The boards also feature the ST Microelectronics, STDRIVEG600, smart motor drive GaN half-bridge driver.

The EPC9167 boards measure just 130 mm x 100 mm (including connector). The boards can also be configured for multiphase DC–DC conversion and support both phase and leg shunt current sensing.

Major benefits of a GaN-based motor drive are exhibited with these reference design boards, including lower distortion for lower acoustic noise, lower current ripple for reduced magnetic loss, lower torque ripple for improved precision, and lower filtering for lower cost. The EPC9167 boards' lower weight and size enable incorporation of the drive into the motor housing and supports low inductance, higher power density motors.
EPC provides full demonstration kits, which include interface boards that connect the inverter board to the controller board development tool for fast prototyping that reduce design cycle times.

The default setting for the GaN-based motor drive kit is 100 kHz switching



frequency and 14 ns deadtime. While the kit is designed to be programmed for different frequencies and deadtimes, operation at high frequency around 100 kHz allows for the elimination of electrolytic capacitors and the use of lower capacitance, and reduce the motor losses. Operating the boards with very small low deadtime of around 14 ns allows higher torque per ampere. The joint effect is to improve inverter and motor system efficiency of more than 7% vs. a silicon MOSFET solution which typically operates at 20 kHz and 500 ns deadtime.

“GaN-based inverters increase motor efficiency while reducing their cost and delivering the same performance as an expensive motor using a silicon MOSFET-based inverter”, said Alex Lidow, CEO of EPC. “This enables motor systems that are smaller, lighter, less noisy, have more torque, more range, and greater precision.”

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EPC releases lowest On-Resistance RAD hard GaN FET

EFFICIENT POWER CONVERSION (EPC) has expanded its family of radiation-hardened GaN products for power conversion solutions in critical spaceborne and other high reliability environments. The latest device is claimed to have the lowest on-resistance of any rad-hard transistor currently available on the market.

The EPC7019 radiation-hardened eGaN FET is a 40V, 1.5 mΩ, 530 APulsed, rad-hard eGaN FET in a 13.9 mm2 footprint. The EPC7019 has a total dose rating greater than 1 Mrad and SEE immunity for LET of 85 MeV/(mg/cm2). These devices are offered in a chip-scale package, the same as the commercial eGaN FET and IC family. Packaged versions will be available from EPC Space.

The device has a figure of merit (RDS(on) x QG) that is 20 times superior to alternative rad hard silicon solutions and the size is 20 times smaller. With higher breakdown strength, lower gate charge, lower switching losses, better thermal conductivity, and lower on-resistance, power devices based on GaN significantly outperform silicon-based devices and enable higher switching frequencies resulting in higher power densities, higher efficiencies, and more compact and lighter weight circuitry for critical spaceborne missions.

Finally, GaN devices support higher total radiation level and SEE LET levels than silicon solutions.

Applications benefiting from the performance and fast deployment of the EPC7019 include power supplies for satellites and mission equipment and motor drives for robotics and instrumentation.

"EPC's GaN technology enables a new generation of power conversion and motor drives in space operating at higher frequencies, higher efficiencies, and greater power densities than ever achievable before" said Alex Lidow, CEO, and co-founder of EPC. "The EPC7019 offers designers a solution with a figure of merit that is 20 times better than best-in-class silicon rad hard devices. This is the lowest on-resistance for a rad hard transistor on the market today. And, the EPC7019 is significantly smaller and lower cost".

Transphorm and TDK-Lambda expand GaN module family

HI-REL GaN maker Transphorm has confirmed that power supply manufacturer TDK-Lambda has expanded its GaN-based PFH500F AC-DC power module product line.

The PFH500F-12 and PFH500F-48 are the second and third modules in TDK's series of 500-watt AC-DC power supplies. Respectively, they offer 12V and 48V power outputs.

As with their predecessor, the GaN-based 28V PFH500F-28, these latest supplies deliver various GaN benefits to end applications including a six percent efficiency increase in a 13 percent smaller device package. Combined, these advantages yield a 38 percent power density improvement when compared to the PFE500SA-12 and PFE500SA-48, TDK-Lambda's incumbent silicon-based 12V and 48V modules.

The PFH500F series uses 72 mΩ, 8x8 PQFN GaN FETs (TP65H070LDG) from Transphorm. These power transistors' high power density enabled TDK to cool the GaN power supplies via thin baseplates. In turn, TDK was able to produce a leaner, tightly contained power module capable of supporting a wide variety of broad industrial applications operating in harsh environments. Such applications include commercial off-the-shelf (COTS) power supplies, custom fanless power supplies, 5G communication, laser, digital signage/displays, signaling, and more.

The 12V and 48V PFH500F modules were designed by the TDK-Lambda Americas Dallas, TX team and deploy a bridgeless totem pole PFC configuration. While the flagship 28V GaN power supply took about three plus years to design, TDK's engineering team was able to adapt its learning to produce these latest models in a year.

"TDK's decision to launch the PFH500F product line as a GaN line was the result of carefully considering what our customers want and need," said Jin He, Vice President of Engineering at TDK-Lambda Americas. "And, what our customers require are reliable power systems for use in rugged applications that can't afford to fail. By using Transphorm's GaN, we are able to confidently deliver that in increasingly smaller, higher performing PSUs that can also inspire end system innovation."

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SiC RoadPak – New levels of power density

No matter if high torque requirement in vehicles, efficient charging for e-busses and e-trucks or smallest footprint within train converters is needed, Hitachi Energy new generation of e-mobility SiC power semiconductor modules are the best choice.

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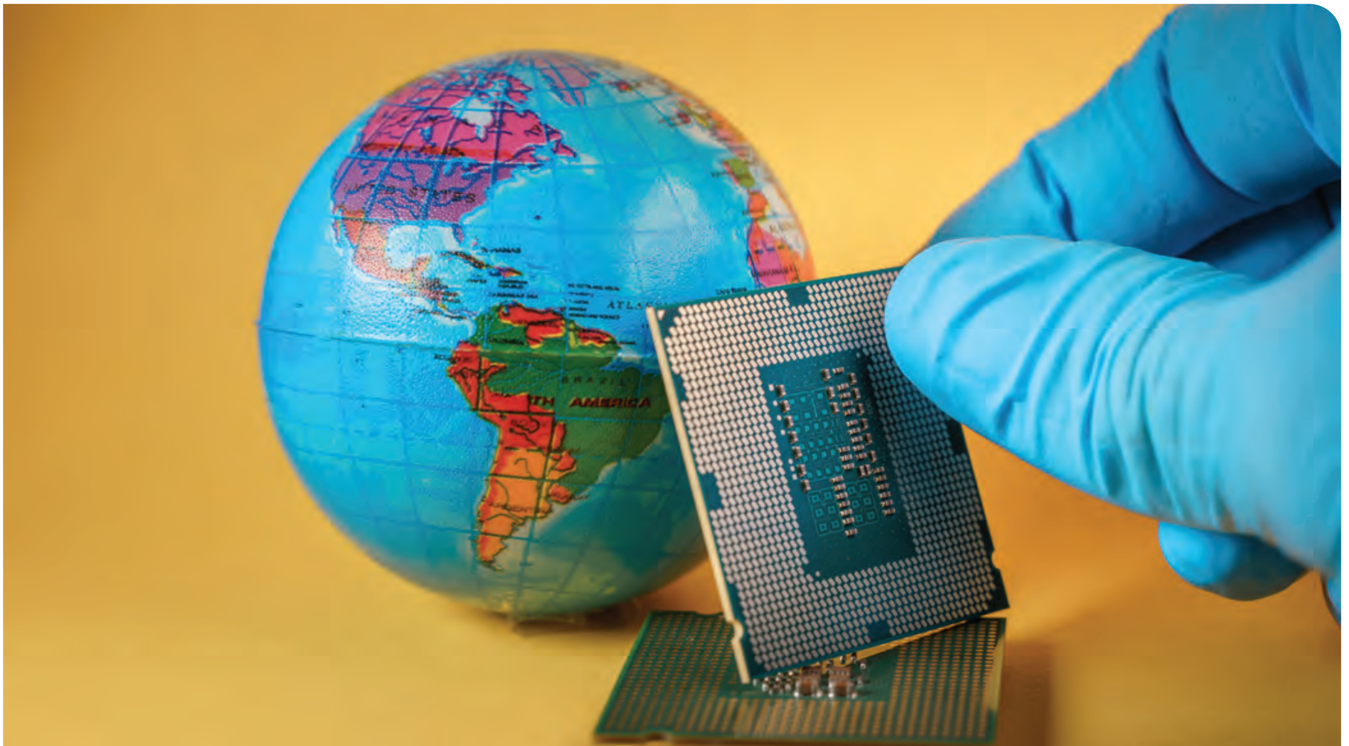


Pandemic lessons have reshaped power device and IC manufacturing

From the first days of the pandemic to the recovery now taking hold, the semiconductor industry has retained its role as both a pain point and a remedy to speed a much needed global economic recovery. One quarter into the New Year, we examine common assumptions, the facts, and strategies for achieving sustainable growth amidst challenging times.

AN ANALYSIS BY MARK ANDREWS, TECHNICAL EDITOR, POWER ELECTRONICS WORLD

BUSINESS UNUSUAL is how many have described the semiconductor industry throughout the past two years. This description persists as manufacturers work their way out and around varying pandemic-induced crises towards normalizing production processes on the road to achieving sustainable growth.

For the first time, shortages and manufacturing challenges have beset the entire range of semiconductors that manufacturers produce, from the most simple power microcontroller or switch to the most advanced SoCs and ASICs. And unlike past supply interruptions, the pandemic affected business on every continent. Power electronics have often come under intense scrutiny since, most notably, automobile and light truck manufacturers are a very visible aspect of heavy industry that finds itself millions of vehicles behind global demand.

Further complicating the recovery are a wide range of shipping, distribution and generalized supply chain issues that have kept semiconductor manufacturers – like their customers—constantly looking for new ways to keep products moving out the door even while raw materials, components, electronic materials and even substrate wafers are in short supply. In a further sign of the times, US-based General Motors announced in mid-March that it was formalizing a program in which new vehicle purchasers could take delivery, even if the auto or truck was missing 'non-essential' components that

would be installed by the company's dealer network once parts become available. Essentially: receive a drivable vehicle today with a promise its build will be completed once parts are in stock.

If the pandemic can be credited for any changes in semiconductor manufacture it is an important new understanding across different industries that a full recovery is going to require increased production of semiconductors across the board. What isn't clear is how to find the best road for meeting demand amidst continuing supply chain woes and the reality that we live in a world that continues to grow ever more dependent on advanced technology. While digitization was already well underway in 2019, the pandemic transformed evolution into revolution. And as we can appreciate now more than ever, revolution by nature forces a disruption of the status quo.

It doesn't take an in-depth market study or a survey of the world's top manufacturers and suppliers to know that power electronics and the overall IC business is booming and will stay that way for the foreseeable future. But since technology is very much 'all about the numbers,' let us take a look at some of the recent studies released that address the shortfalls and point towards recovery timeframes.

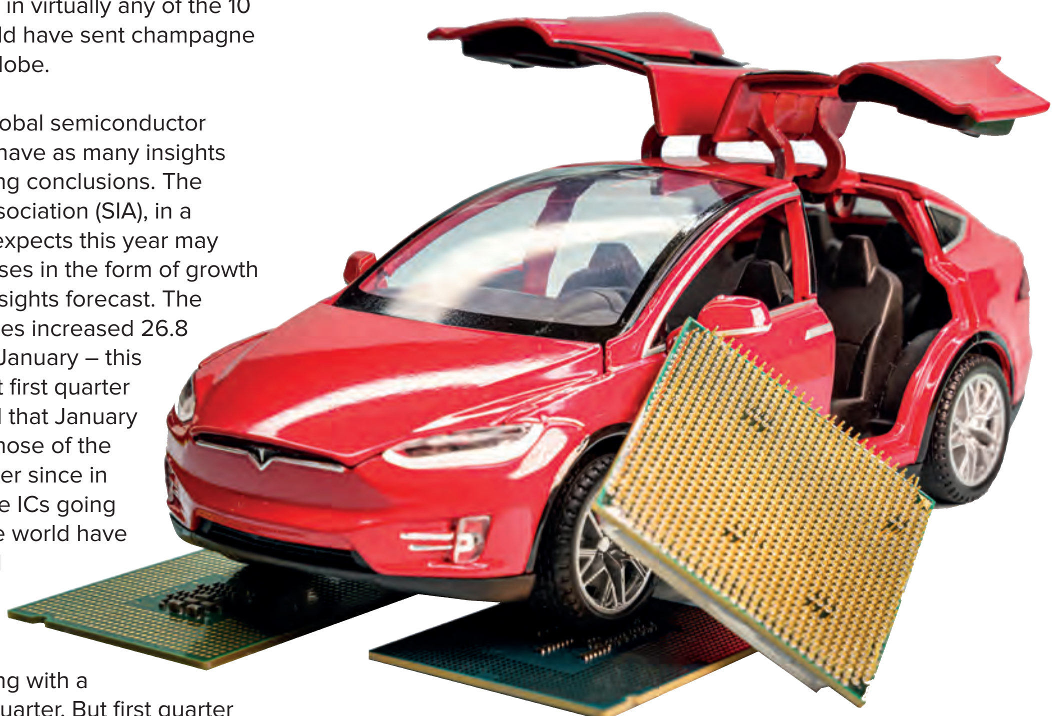
A study released in January by IC Insights showed that 2021 chip sales grew 25 percent. This came on the heels of records set in 2020 despite the challenges of manufacturing amidst the worst global pandemic in a hundred years. While 2022 is expected to be another growth year, IC Insights believes that a long anticipated return to more typical business growth will result in a comparatively 'modest' growth rate of 11 percent this year. Keep in mind that 11 percent growth in virtually any of the 10 years preceding 2020 would have sent champagne corks popping across the globe.

In an industry as large as global semiconductor manufacturing, it is best to have as many insights as is practical before drawing conclusions. The Semiconductor Industry Association (SIA), in a March 2022 report, said it expects this year may hold some additional surprises in the form of growth that could surpass the IC Insights forecast. The SIA stated that global IC sales increased 26.8 percent year-on-year as of January – this figure is the second highest first quarter start in history. Bear in mind that January sales are typically well off those of the previous year's fourth quarter since in January of a typical year, the ICs going into holiday gifts around the world have largely been built, sold, and shipped to OEMs; some seasonal peaks and valleys typically appear in the quarters that follow along with a ramp into third and fourth quarter. But first quarter is usually a time to restock, resupply and finalize planning for the ensuing months. Not so much in January 2022 – this year, January was all about filling orders, reducing backlog and working around supply chain holdups.

The lack of advanced ICs and semiconductors of all types has been widely discussed as reasons for some OEMs to report smaller than expected sales. Indeed, some were held back, like Apple that reported it 'lost' up to $6 billion in potential sales due to its inability to complete product builds. This situation could be growing worse for Apple given the fact that its key Asian manufacturing partner in Shenzhen, China (Foxconn) has had to pause operations in the area due to a resurgence of COVID-19 cases in and around the city. Apple advised that the shutdown would continue until the local government allowed resumption of normal operations. By the time stock markets closed on the day of their announcement, Apple shares closed down 2.66 percent.

Over at Nvidia Corporation, CFO Colette Kress echoed that refrain, saying her company did not realize a substantial amount of sales it believes could have been achieved had all key components been delivered as originally expected. Kress forecast supply constraints to ease by mid-year. Optimism aside, other industry observers have noted that continuing pandemic-induced issues in major manufacturing centers (like Shenzhen,) may push a resumption of normalized business operations into late 2022 or early 2023.

Furthermore, it is clear that no one can accurately predict how the conflict in Ukraine begun by Russia weeks ago may eventually affect global markets including semiconductors.



While every product that needs to move from one distant point to another has been impacted by pandemic related shipping and distribution challenges, automobile manufacturing is often cited as a heavy industry bellwether. While this is certainly true within regions dependent on a particular auto makers' profitability, understanding the true cause and effect at the national and global level isn't as simple as accounting for a single variable.

Since power electronics and especially major systems on a chip (SoC) tied to power management and in-vehicle systems have been cited frequently by auto manufacturers as being at the top of their gripes and woes, it is fair to wonder how manufacturers became entangled in the current predicament and whether the inability to meet the demand for automobiles and light trucks can be traced back to the lack of power electronics and other automotive ICs.

First, how big is the issue? According to a recent study by analysts at Auto Forecast Solutions, a lack of microelectronic chips of almost every variety collectively help reduce global vehicle production by 10 million units in 2021, with an additional 1 million at risk in 2022. That is a massive shortfall considering that in a typical year, global automobile and light truck production averages about 18 million vehicles. While semiconductors were not the sole contributor, they play an increasingly sizeable role in how a vehicle controls its engine, enables passenger safely, and achieves increasingly good mileage, not to mention the role played in communications, infotainment and navigation systems.

According to Wards Intelligence analyst Bob Gritzinger speaking in a Detroit Free Press article in February, the average modern vehicle utilizes about 1,200 ICs of various types, from very simple controllers and switches that cost pennies each, to very powerful, customized ASICs and SoCs that may cost $50 or more, each. Auto makers have not always relied so heavily on semiconductor and power ICs, but once the first automotive micro control units, MCUs, began regulating engine performance in the 1970s, manufacturers soon became more and more dependent on advanced technology to meet customer expectations, environmental regulations, and as time went by, the communications and web access that transform today's most advanced vehicles into rolling computers.

If all automotive power electronics, SoCs and ASICs were universal, there likely would be no shortage since in such an idealized world, a microcontroller that would, for example, typically be used to control an Audi's power plant could be swapped for one that might otherwise go into a pickup truck made by Ford Motor Company or Fiat. But automotive chips are almost never interchangeable. Each auto maker has its own set of goals for the devices it designs into a new vehicle. While some ICs within a company's lineup might be used in multiple cars that company makes, devices built for one company are not usable in competing automobiles.

Like most complex manufacturing processes, the success of vehicle production and sales can't be tied solely to one commodity. In fact, recent studies appear to reveal that some of the assumptions around the impact of IC shortages on new car sales may have been over stated. While contributing to empty sales lots and higher prices, was the lack of semiconductors the ultimate culprit?

In a recent IC Insights study, researchers took an in-depth look at the automotive device market as

Figure 1.

part of the organization's January Semiconductor Industry Flash Report; look to the IC Insights February quarterly update for in-depth auto IC sales numbers and forecasts.

This is the point where the 'conventional wisdom' often repeated in mainstream media these days departs from facts found in the latest industry reports. The commonly accepted rationale for what led to auto makers' woes goes a bit like this: In March of 2020, just as the first shut-downs signaled the onset of the COVID-19 pandemic, auto demand plunged worldwide. Auto makers reacted to this and began to shut down plants and halt semiconductor orders along with other commodities from their various suppliers. While auto makers were putting the brakes on their usual inventory stocking practices, there was a global surge in demand for consumer electronics from a population that was sheltering in place; what was hoped to be temporary turned into a tsunami of work-and-school-from-home paradigm shifts. As automotive orders dried up, semiconductor manufacturers switched production capacity to the commoditized components, power electronics and ASICs needed to build systems now suddenly in much higher demand.

When auto makers wanted to reopen factories in 2020, the story goes than many if not most found that semiconductor suppliers had shifted production capacity away from transportation applications to consumer electronics. A serious automotive chip shortage ensued, which drove up the price of new cars and trucks while transforming pre-owned cars into driveway goldmines.

IC Insights has said it believes that the commonly accepted scenario described above is not the complete story behind automotive industry production shortfalls. One factor not taken into consideration is the common practice known as 'just-in-time' component delivery for OEMs. Like many manufacturers, auto makers found that the relatively cheap and fast ability to move goods around the pre-pandemic world could enable a just-in-time inventory strategy that helped reduce warehouse costs by only maintaining sufficient supplies of materials for a certain number of regular production weeks. Little was held in reserve for 'just-in-case' situations, which works fine so long as the supply chain continues to flow. The strategy falls flat on its face when container ships can't load or unload, vendor factories are idled and disruptions in world trade – like a pandemic – occur unexpectedly.

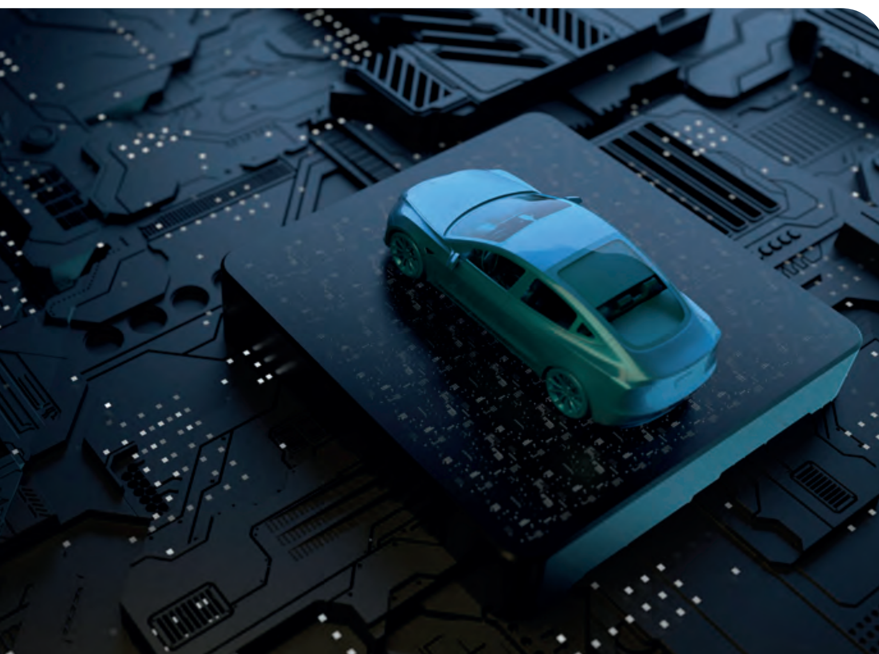
In the opinion of IC Insights' researchers, the real reasons behind the automotive IC shortage lie in a combination of factors: first, the surge in demand for automotive ICs in 2021 was to blame, not the inability of semiconductor manufacturers to increase production—they in fact increased output as we'll soon explore. Second, automotive ICs are increasingly vital in each succeeding generation of new cars and light trucks thanks to their role in advanced driver assistance and safety (ADAS) systems, greater vehicle autonomy, the shift from conventional internal combustion engine drive trains to electric vehicles, and more in-vehicle entertainment as well as internet connectivity. Essentially: supply was falling short due to a combination of pent-up demand in 2020 and 2021, plus the fact that more ICs are now needed in each new vehicle, combined with some unexpected production interruptions at a few key IC plants.

According to the researchers, IC manufacturers actually shipped 30 percent more devices to the automotive industry in 2021 as compared to 2020,

which was substantially greater than the 22 percent increase in total worldwide IC unit shipments (all semiconductors) recorded in 2020. What is especially revealing is that the growth of IC units shipped to auto makers in 2021 was substantially greater than pre-pandemic 2019. Further, the response by industry to auto manufacturers' needs represented the greatest increase in shipments since 2011. The most recent substantial jump in IC shipments to auto makers occurred between 2016 and 2017 when shipments increased 20 percent. The 2017 growth spurt was considered record-setting at the time. (See Figure 1)

So why is there a mismatch between the shipments we can see vs. the commonly held perception that semiconductor manufacturers did not 'step-up' when needed? A lot hinges on the subjective nature of perception and the complicated entanglement of influencers that affect outcomes across global markets. According to IC Insights, the pandemic's impact on global supply chains occurred at a time of continual growth in the quantity of semiconductors needed to complete a vehicle build. Essentially, demand for automotive ICs experienced what is called a 'step-function' increase in 2021. Such increases will almost always trigger a temporary mismatch between supply and demand regardless the product. So we can now see that despite a 30 percent increase in automotive device shipments, IC manufacturers could not keep up with the fact that more ICs are now needed in each new vehicle, paired with unexpectedly high demand that grew during the second half of 2020 and throughout 2021.

According to Jan-Philipp Gehrmann, head of global marketing for NXP's advanced analog business, the auto industry has indeed been affected by component sourcing issues more than any other



industrial sector. Another complicating factor was what he described as a 'major disconnect' between how long it takes to build a car, for example, and the much more lengthy time it takes to build advanced chips compared to other components going into every vehicle: auto makers were simply accustomed to getting more or less what they wanted, when they wanted it, and they at first did not comprehend why it took semiconductor makers so long to address new orders.

"What auto makers were unfamiliar with was the process of how chips are made and the complexity behind that," said Gehrmann. "While it usually only takes a single day to manufacture a vehicle from start to finish, the average chip has a front-end production cycle of 12 to 24 weeks. Additionally, it takes 4 to 8 weeks on the back-end to package and test it before finished devices are ready to be shipped. The fact that producing a single chip can take six months was hard (for them) to understand," he said.

The pandemic-driven global imbalance between semiconductor manufacturing and OEM consumption has led to a substantial reevaluation of where the most advanced chips are manufactured and how industry might work to restore balanced growth while simultaneously addressing long term needs. Major issues include the concentration of chip manufacturing in the Asia-Pacific region; impacts of More's Law-driven device architectures changing into 'More than Moore' paradigms; and the implications still being assessed of talent shortages now seen globally as today's most senior engineers, researchers and technicians retire or for other reasons decide to leave the industry.

Even before the pandemic, alarm bells were ringing when manufacturing advanced ICs had substantially moved out of North America and Europe in favor of lower labor cost locations across the Asia-Pacific region, most notably to Taiwan, Korea and China. Perhaps one of the most striking indicators is a look at the share of worldwide semiconductor manufacturing in the United States in 2020 compared to 1990. According to an analysis by Brookings Metro published earlier this year, despite its incumbency role in developing the semiconductor industry, US-based IC manufacturing has fallen steadily in the last 30 years from a 37 percent share to about 12 percent in 2020. According to experts at Employ America, this transformation has many implications, but the two most worrisome is the loss in production leadership and also what they describe as the 'learn by doing' processes that go hand-in-hand with manufacturing.

Ask any production manager or engineer how they honed their fab expertise and grew professionally. Most will reply that success is a product of continuing education plus the hands-on work experience that gives seasoned employees an edge. From a company's least experienced new hire to a company's most senior researchers and

technologists, experience counts not only in terms of production efficiency but also because of its unique ability to drive innovation. It may sound obvious, but many of the best ideas manufacturers develop are outgrowths of hands-on work with the product and the machines, processes and materials required to make said products. Essentially, building advanced devices concentrates the experience needed to build next-generation devices in the location where the manufacturing takes place. Studies by Employ America have shown that not just in the US, but in any location that hosts advanced manufacturing, it is the presence of manufacturing facilities alongside research and academia that enables constant product and process improvement, which elevates competitiveness.

In the United States and across the European Union, the importance of having advanced semiconductor manufacturing in-country is key to continuing leadership within a given field. This has led to a number of legislative initiatives in both the United States and the EU to foster 'home grown' manufacturing. The United States has its America COMPETES Act along with the CHIPS for America Fund. The EU has developed and supported its counterpart, the European Chips Act, which ambitiously calls for quadrupling Europe's production capacity by 2030 while also attempting to create systems designed to avoid future supply chain disruptions. Both US and EU initiatives are designed to counter the subsidies, government ownership and tax advantages found in other countries including China, Korea and Taiwan that underwrite the development and expansion of semiconductor manufacturing within their borders. Governmental action in North America and Europe have not gone unnoticed as evidenced by new rules and tax incentives to support and safeguard local semiconductor industry recently passed by South Korea's National Assembly. In China, 15 local semiconductor funds have been established in an effort to supply 70 percent of its own chip needs by 2025.

Not finding a sought-after consumer electronics device, new vehicle or other IC-laden product makes headlines in mainstream media. What tends to not make headlines is the titanic shift underway that is already changing how chips are designed and manufactured. While Gordon Moore's 'Law' drove the pace and essential rules for competitive semiconductor architectures until the early 2000s, it has become more and more apparent that transistor shrink can no longer meet the needs for greater performance, reduced size and lower power consumption that have enabled widespread use of semiconductors across multiple product categories. The 'More than Moore' (MTM) movement has many permutations, but to condense this into digestible bites, think of MTM innovations as design approaches that depend upon new electronic materials science, new device structures and even whole new underlying technologies as a means to

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achieve performance, cost and power consumption goals rather than conventional Dennard scaling.

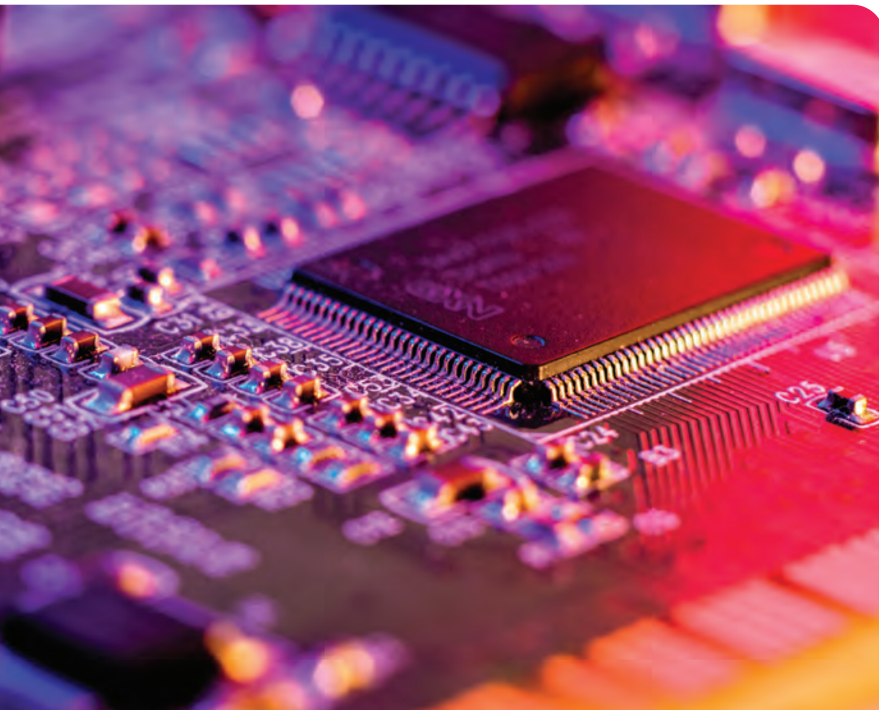
As outlined in an article in this month's edition of Silicon Semiconductor, ClassOne Technology Vice President John Ghekiere points to ways that he has seen companies outside the exclusive club of 'Uber Foundries' still pursuing transistor shrink are instead charting new courses to achieve their goals without the complexities and expense driven into Moore-style transistor shrink. These are innovative companies working to develop top-performing devices, yet they eschew the price of EUV lithography or other exorbitantly expensive technologies designed to enable transistor features to and below 3nm.

"The withering march of relentless device scaling described by Moore's Law has left a mere handful of device manufacturers in that race, with TSMC clearly in the technology lead. When the cost per transistor inflected to become more expensive with each generation, somewhere between 26 and 22 nanometer nodes, it drove even many of the larger and more powerful manufacturers to alternate paths of innovation and new means of bringing value; GlobalFoundries pivoted boldly into FD-SOI; STMicroelectronics into SiC. The broad expansion of new device types - in short, the ubiquitous adoption of microelectronic devices into almost every aspect of our daily lives - has brought about the More Than Moore era, where feature scaling is no longer the sole means of device innovation," he said.

The headlong pursuit of More Than Moore strategies at the time other manufacturers are seeking to build 3nm devices, plus the simultaneous need for more semiconductors for more applications is creating a unique combination of challenges and opportunities for the industry. This is perhaps best appreciated when one considers that third

and fourth quarter 2021 saw one of the largest employment sea changes since the Great Recession of 2008. In the United States alone, 4 million persons changed jobs, retired before age 65, or left the workforce across a multitude of professional roles for a variety of reasons. Looming on the horizon is the prospect of new fabs being built in North America, Asia and Europe will demand more talented researchers, engineers, and fab-based technicians than ever before in the history of semiconductor manufacturing.

Although chip shortages are broad-based – affecting product lines across applications – companies feeling pain acutely are concentrated amongst those trying to buy chips that are based on legacy nodes that have the longest service lifetimes, specifically the microcontrollers that are widely used in automobiles; additionally, there are sizeable



shortages of analog and power management ICs. No sudden drop in demand is expected, so almost every analyst agrees the shortage of power electronic components like microcontrollers will persist throughout the year and could linger into 2023.

Major manufacturers are warning customers and the public alike that these constraints will not be resolved for some time. GlobalFoundries, the largest US-based contract chip maker and a significant power electronics manufacturer, said that wafer capacity for its more mature nodes is sold out through 2023 even though the company plans to boost its production capacity 50 percent by the end of next year.

Varying levels of availability also mean different industries and even companies in the same industry will likely receive components at different rates in part due to efforts by manufacturers to divide supplies proportionately and to honor existing contracts ahead of new business. Glenn O'Donnell, VP of Research at the Forrester consulting group, said in a 2021 report that widespread chip shortages could soften for some sectors by later this year including PCs and consumer electronics. His firm expects continuing, significant shortfalls will effect automotive orders throughout 2022.

The SEMI trade association reported results of its latest industry survey on 28 February 2022 that points to the greatest concerns amongst its international membership. SEMI asked respondents to focus on issues affecting their abilities to manufacture semiconductors for global customers. More than 400 US member companies replied, offering insights into the importance of enhancing competitiveness through targeted public and private investments aimed at growing manufacturing capacity, infrastructure and its workforce. SEMI conducted the survey in partnership with MITRE Engenuity, the technology foundation for public good launched by MITRE two years ago.

Survey results indicate US manufacturers see needs and challenges in three primary areas:

- A need for investment across the entire semiconductor ecosystem
- Investment by private firms as well as publicly-funded entities to counter the governmental incentives provided in current centers of IC manufacturing in Asia-Pacific
- Investment in multi-generational workforce initiatives including STEM incentives, apprenticeship programmes, and similar efforts built around creating interest in careers that pay well but may be perceived as unreachable goals

While governments and major semiconductor manufacturers agree hybrid investment strategies are key to increasing competitiveness and to ensuring continual growth in the global chip supply, it was somewhat surprising to see the importance placed on growing the talent pool of engineers, technicians, researchers and scientists focused on developing and manufacturing advanced ICs.

Respondents in the SEMI survey were essentially saying that building new fabs in Europe, the United States and elsewhere are essential to expanding global semiconductor capacity while supporting the 'on-shoring' of IC manufacture, but that shiny new infrastructure will come to naught if those facilities cannot be staffed by a highly educated, well trained workforce. The combination of senior technical staff reaching retirement age and plans to dramatically increase manufacturing in North America and Europe are at odds – factors that will play an increasingly important role to correcting the supply/demand imbalance while ensuring that there is a steady supply of general purpose semiconductors, ASICs and power electronics from a diversified global manufacturing base.

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Targeting medium-voltage power electronics with vertical GaN devices

Vertical GaN *p-n* diodes combine excellent efficiencies with incredibly fast protection from unwanted electromagnetic pulses

BY ROBERT KAPLAR FROM SANDIA NATIONAL LABORATORIES, TRAVIS ANDERSON FROM THE NAVAL RESEARCH LABORATORY, SRABANTI CHOWDHURY FROM STANFORD UNIVERSITY AND OZGUR AKTAS FROM EDYNX

WE ARE LIVING in an age of increased awareness of energy efficiency. This is partly caused by concerns over global warming, rammed home by alarming images of this year's floods and heat waves. However, it also comes from increasing use of battery power, particularly in transportation, and the need to make the most out of this stored energy.

For the electric grid and various microgrids, demand is on the rise for high-efficiency solid-state power conversion in the medium-voltage range, which roughly spans 1.2 kV to 20 kV. Power converters operating in this domain could serve in solid-state transformers operating at the grid distribution-level, such as those at 13.8 kV, as well as DC microgrids, including those proposed for all-electric aircraft at 10 kV. Thanks primarily to a breakdown electric field that is far higher than that of silicon, wide-bandgap semiconductors, such as SiC and GaN, offer

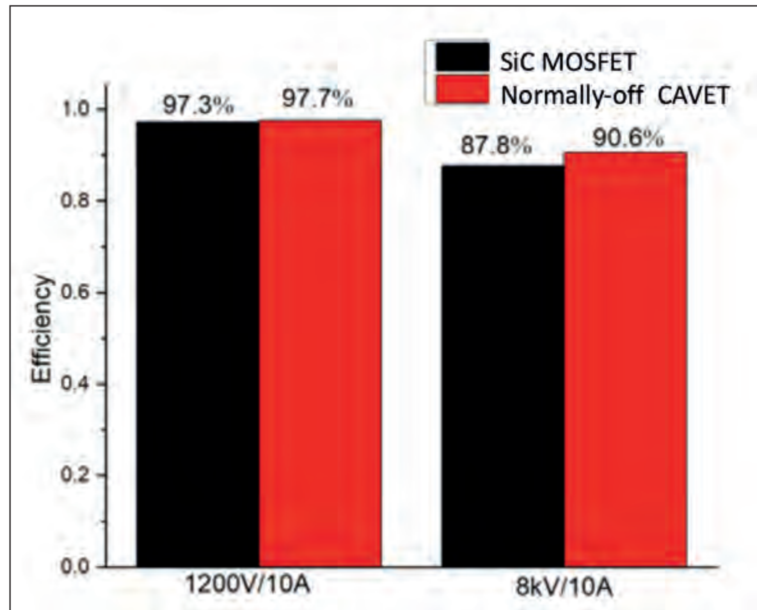
outstanding opportunities for improving medium-voltage power electronics. As well as reducing on-resistance, they can increase conversion efficiency and slash system size, due to higher switching frequencies. Of the two successors, GaN may ultimately have the upper hand at voltages of 10 kV and more, due to its higher electron mobility (see Figure 1).

The results shown in Figure 1 compare the performance of a type of GaN vertical power transistor known as a CAVET – its full name is a Current-Aperture Vertical-Electron Transistor – with a SiC MOSFET. Note, however, that the trend is applicable to other types of vertical power device. The term 'vertical' is used for device architectures that contain a thick, low-doped drift region. This layer provides the blocking voltage and governs the on-resistance of the device. As the operating voltage increases, the efficiency of the GaN converter improves relative to that of SiC (this can be seen by comparing the performance of 1.2 kV and 8 kV devices). At first glance, the increase is trivial, but this overlooks the need to consider the difference from 100 percent efficiency. Evaluated in this manner, which hones in on the loss, the difference is substantial.

One major downside of vertical GaN devices is that they are not as mature as their SiC cousins, and in this regard, in a different league from those made from silicon. To fully evaluate the feasibility of vertical GaN there needs to be ongoing improvements in the epitaxial growth of GaN on its native substrate, as well as advances in device processing, such as those that enable effective edge-termination structures.

To this end, our US collaboration, led by researchers at Sandia National Labs and involving engineers at the Naval Research Laboratory, Stanford University, Edynx, and Sonrisa Research, has established a vertical GaN foundry that is targeting 1.2 kV, 3.3 kV, and 6.5 kV devices. This holistic effort combines epitaxial growth with wafer metrology, device design, processing and characterization – the latter includes investigation of yield, reliability testing, and failure analysis. We are also undertaking a parallel effort that is focusing on higher-voltage structures, eventually up to 20 kV, and targeting specialized devices with a very fast breakdown that are capable of protecting the electric grid from electromagnetic pulses.

We have undertaken extensive mapping of bare GaN substrates and epiwafers with GaN *p-n* diode structures grown by MOCVD. Tools for this mapping include an optical profiling system, Raman spectroscopy, and typical mercury probe. The profiling system's capabilities are illustrated in Figure 2, which has maps of three 2-inch wafers featuring 8 μm, 10 μm and 12 μm-thick drift layers with a net doping density of 1.3×10^{16} cm^{-3}. For our



➤ Figure 1. Simulated switching efficiency improvement for vertical GaN CAVETs (a type of vertical transistor) compared with SiC MOSFETs at 1.2 kV and 8 kV. Mobilities of 950 cm^2 V^{-1} s^{-1} and 1200 cm^2 V^{-1} s^{-1} are used for SiC and GaN, respectively (taken from D. Ji *et al.* Int. J. High-Speed Elec. Sys. **28(01n02)** 1940010 (2019)).

foundry effort, we tend to use such structures for fabricating 1.2 kV devices. Fabrication of our devices occurs at the 2-inch wafer scale, using a foundry environment at the US Naval Research Laboratory. Here, standard processing techniques for III-N devices realize contacts, isolation, and so on.

Evaluating edge termination

When producing these GaN diodes, the most critical process step is edge termination, which is realized by ion implantation. Although etch-based processes have been shown to achieve high performance, we employ implantation for the foundry, because this enables a planar process that is compatible with true foundry manufacturing. Using ion implantation, we have processed epitaxial wafers into devices with various combinations of junction termination extensions and guard rings (see Figure 3 for photos of typical GaN foundry wafers and associated forward current-voltage characteristics). Measurements on our diodes reveal excellent turn-on behaviour and electroluminescence typical of a GaN *p-n* junction.

For diodes with areas ranging from 0.1 mm^2 to 1.0 mm^2, forward current capability is more than 5 A, corresponding to current densities spanning 500 A cm^{-2} to 5000 A cm^{-2}. The related specific on-resistance is 0.3 mΩ-cm^2 to 1.2 mΩ-cm^2.

We have also assessed the breakdown voltage of our devices. Sampling twelve of them from a single wafer shows that the breakdown voltages exceeds 1.3 kV in all cases – this is approximately 90 percent

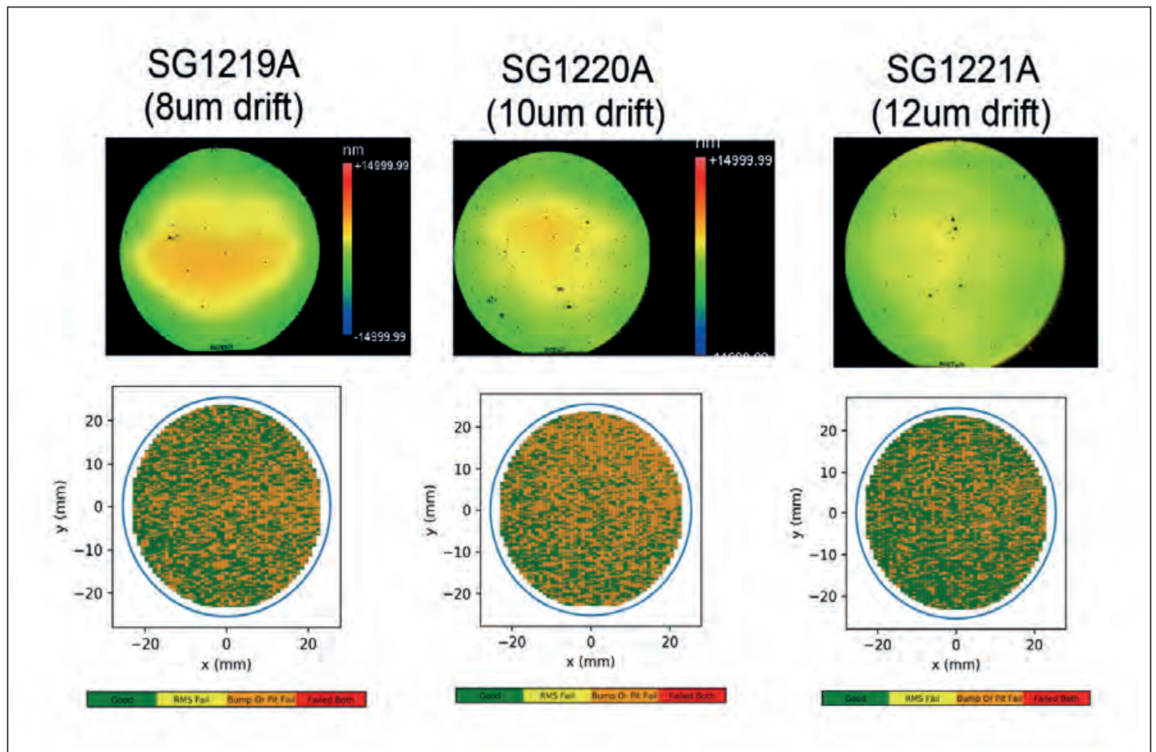


Figure 2. Optical profiles of 2-inch diameter GaN substrates with 8 µm, 10 µm, and 12 µm drift regions grown by MOCVD. The top portion of the figure shows the raw data, while the bottom portion shows yield maps: green indicates a good device; yellow a failure due to root-mean-square (RMS) roughness; orange a failure due to a bump or pit; and red a failure due to both modes.

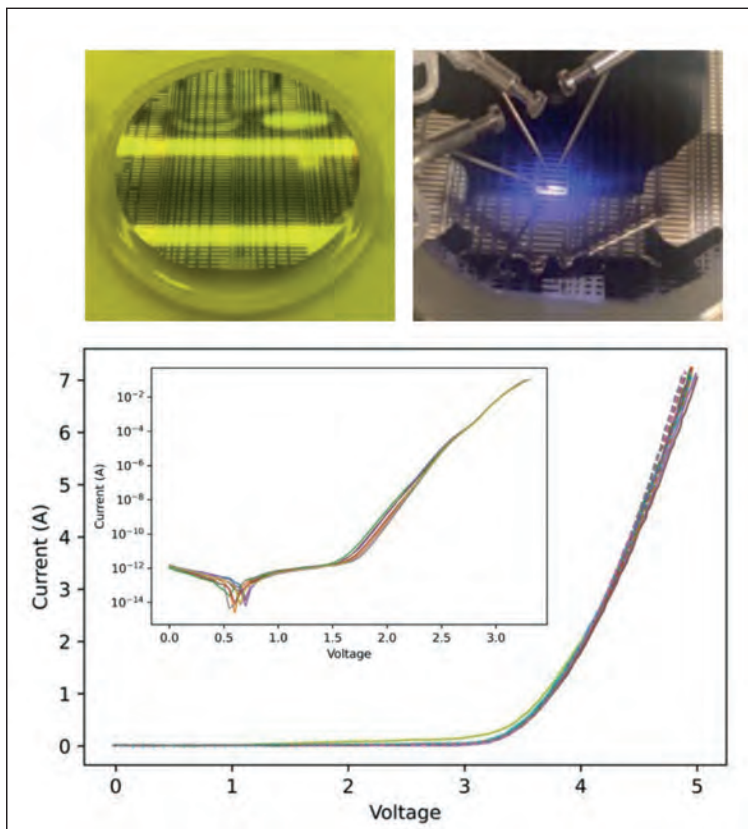


Figure 3. A photo of a typical GaN *p-n* diode foundry wafer (top left), and such a wafer under test (top right), with visible sub-bandgap light emission. The bottom portion of the figure shows representative forward current-voltage curves (main figure, linear scale; inset, log scale).

of the theoretical parallel-plane limit. Note that the precise nature of the breakdown depends on the details of the edge termination. Devices receiving a shallower termination implant profile exhibit a breakdown indicative of avalanche behaviour and characterized by an abrupt increase in current.

We are also exploring other approaches to edge termination. They include a bevel design, which we have evaluated with extensive numerical simulations (one example is shown in Figure 4, with results for a 5° bevel).

One key finding of this work is the need for very small bevel angles, employed to ensure that the electric field at the edge of the structure is maintained below the ideal parallel-plane maximum electric field (it is around 3.1 MV/cm for the case shown). We have drawn on the results of simulations to guide our fabrication of bevel-terminated diodes, using either a flowed photoresist for bevel angles of 5°, 15°, and 50°, or greyscale lithography for a bevel angle of 1°.

With vertical GaN power devices at an early stage of development, it is not surprising that reliability studies are relatively rare. Our team is adding to them, using high-temperature operating life tests to assess the diode forward-current stability, and evaluating reverse-current stability with high-temperature reverse-bias testing. In both cases, test conditions are carefully monitored to ensure that the device's temperature and its bias stay constant throughout this test. One key finding of these

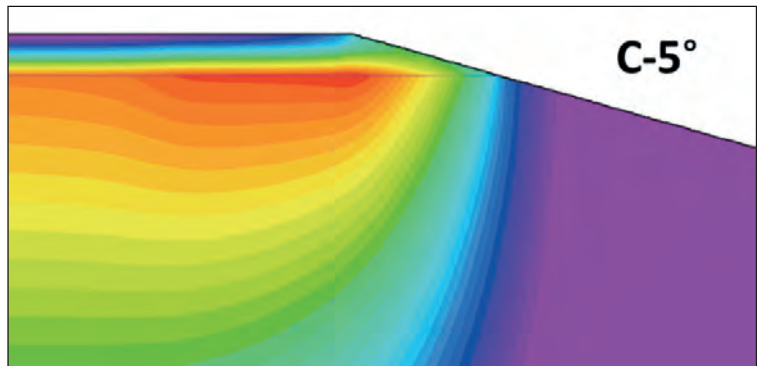
investigations is that there is a significant increase in the forward current during high-temperature operating life testing. Another important observation is that when the diode is biased in the avalanche region, there is a change in the avalanche current during high-temperature reverse-bias testing. Thermal considerations limit the DC avalanche current, which exhibits a thermal transient during the first minute at elevated temperatures.

Our team has also conducted failure analysis on selected failed devices. This includes inspecting a diode that failed high-temperature reverse-bias testing with emission microscopy (see Figure 5). Using this technique, we observed that the emission is near the edge termination of the device, indicating that this portion of the diode is responsible for its failure.

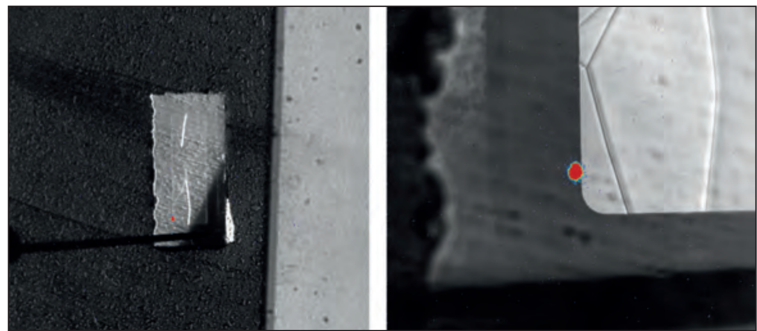
Protecting the grid

Electromagnetic pulses pose a significant threat to the electric grid, as they could potentially cause blackouts over an extremely large geographical area. For electromagnetic pulses with transients shorter than a microsecond, over-voltage conditions that ensue could cause damage to today's grid. One solution is to introduce fast breakdown GaN *p-n* diodes – they are capable of clamping the voltage across equipment on the grid when it is subjected to such pulses.

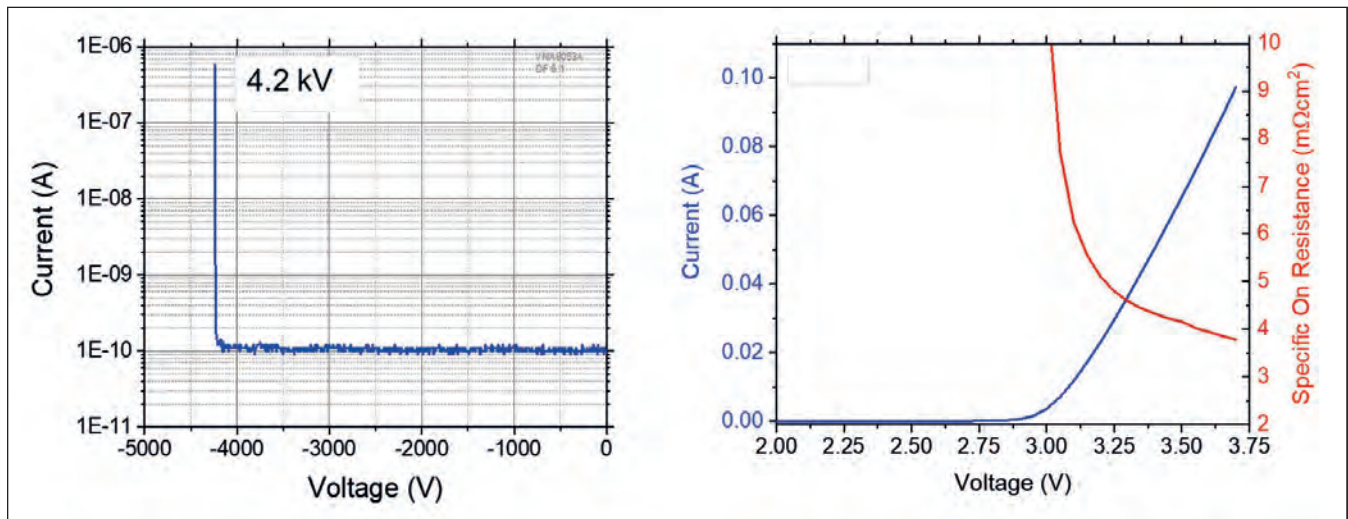
A target voltage for this specialized but critical application is 20 kV. This blocking voltage provides an adequate margin for protecting, with a single device, distribution-level equipment, when typically operating at up to 13 kV; and it provides a building-block for protecting sub-transmission equipment, as only a small number of stacked devices are needed to reach 69 kV, a typical requirement for this application. We have started on the path



➤ Figure 4. Electric field magnitude for a 5° bevel termination with an 8 μm-thick drift region with a net *n*-type doping of 1.3×10^{16} cm^{-3} and a 500 nm-thick anode layer with a magnesium concentration of 3×10^{17} cm^{-3} to achieve *p*-type doping.



➤ Figure 5. Left image shows an emission microscopy image of a GaN *p-n* diode at 1 kV and 0.5 mA under 2.5x magnification. A single emission spot is visible at the corner of the device at the termination of the junction-termination extension. Right image shows expanded view of the emission spot.



➤ Figure 6. Current-voltage characteristics of GaN *p-n* diodes with 45 μm-thick drift regions intended for an electromagnetic pulse arrestor. Left panel shows low reverse-bias leakage current and breakdown around 4.2 kV; and right panel shows forward-bias current and differential specific on-resistance, which is approximately 3.8 mΩ cm^2 at 3.75 V.

While vertical GaN power devices hold promise for medium-voltage power electronics, challenges must still be overcome related to substrates, epitaxial materials growth, and device processing. Additionally, there is a need to characterise and understand yield and reliability, to enable the fabrication process to become commercially viable

to producing 20 kV devices, with efforts to date focusing on '5 kV class' GaN *p-n* diodes. These devices have an epitaxial structure that consists of a 45 μm-thick drift region with a net *n*-type doping in the 2-5×10^{15} cm^{-3} range. Like the foundry diodes, the structure has been grown by MOCVD. The anode design contains a two-layer *p*-region with a *p*-minus layer (magnesium level of around 1×10^{18} cm^{-3}) near the junction and a higher *p*-doped layer (magnesium level of around 3×10^{19} cm^{-3}) on top. After epitaxial growth, wafers are processed using a multi-step junction-termination flow, using sequential BCl_3/Cl_2 inductively coupled plasma etches.

Electrical measurements of a representative 150 μm-diameter diode reveal that it is extremely well-behaved under reverse bias, exhibiting a low leakage current until the onset of abrupt breakdown at around 4.2 kV (see Figure 6). When operated under forward bias at 3.75 V, the diode shows good turn-on and a differential specific on-resistance of 3.8 mΩ-cm^2, calculated when defining the area as that of the *p*-contact.

To assess the capability of these diodes for electromagnetic pulse protection, we measured response times with a transmission-line system. This approach, drawing on a setup previously used to measure the reverse-recovery time of GaN *p-n* diodes, provides an upper bound of 1.3 ns for the time to breakdown. This incredibly short time demonstrates that this diode can arrest the fast component of an electromagnetic pulse.

While vertical GaN power devices hold promise for medium-voltage power electronics, challenges must still be overcome related to substrates, epitaxial materials growth, and device processing. Additionally, there is a need to characterise and understand yield and reliability, to enable the fabrication process to become commercially viable. Our team is examining these issues as we establish a foundry for fabricating vertical GaN *p-n* diodes. Additionally, we are pursuing specialized applications, such as electromagnetic pulse protection, that utilize the diodes' fast breakdown response. Further research will determine the full extent of the capabilities of vertical GaN power devices.

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A superior process for the SiC power MOSFET

Forming a gate oxide without oxidation smashes through a barrier that has held back the SiC MOSFET for 20 years

BY TSUNENOBU KIMOTO AND KEITA TACHIKI FROM KYOTO UNIVERSITY

GOVERNMENTS FROM ALL AROUND WORLD are now preparing for this year's UN Climate Change Conference, widely referred to as COP26. At this gathering, which is due to take place in early November in the UK, all nations in attendance will be asked to offer a commitment to cutting their carbon footprint.

The level of ambition they can promise will be governed by their plans for installing renewable forms of energy. But another factor that they ought to consider is how efficient they are in using the energy they generate, and whether they can make gains on this front. In almost all kinds of electric and electronic system, the efficiency of power conversion, such as AC/DC and DC/AC conversion, ranges from 85 percent and 95 percent. That implies that with current technology, about 10 percent of electric power is wasted, in the form of heat. That's a significant proportion: just imagine how many gigawatts of electric power is wasted in countless systems by power conversion, or how many coal-fired power stations could be mothballed by making gains in efficiency.

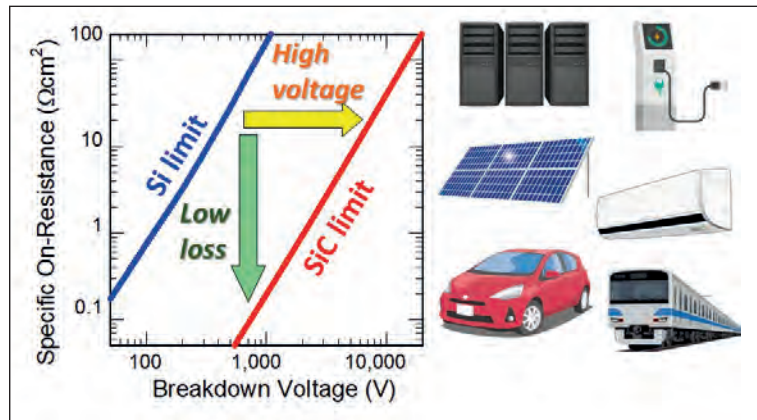
Most of this power loss is attributed to Joule heating inside power semiconductor devices, which are almost exclusively made from silicon. Power devices made from this semiconducting material have been playing key roles in electrical products and infrastructure for many decades, but this technology is now highly mature, offering little opportunity for further improvement. However, significant gains are possible by switching to wide

bandgap semiconductors, such as SiC, GaN, and Ga_2O_3. Interest in all three has been rocketing in recent years. One striking property shared by all these wide bandgap semiconductors is a very high critical electric field strength – it is more than ten times that for silicon. Differentiating the three from one from another are some unique features: SiC is renowned for its wide range of doping control, GaN is blessed with a AlGaN/GaN heterostructure that creates a high-mobility channel, and Ga_2O_3 has the merit of melt growth of bulk crystals.

Amongst this triumvirate, SiC technology is the most mature, in terms of both material growth and device fabrication. Basic research on this class of power devices can be traced back as far as 1990, when Kyoto University, North Carolina State University, Cree, and Purdue University were the main players. Now SiC wafers with a 150 mm diameter are widely available and CVD is well established for the growth of high-purity SiC layers with a low defect density. What's more, ion implantation of donors and acceptors is widely employed for forming *n*- and *p*-type regions, and thanks to the uniqueness among compound semiconductors of the native oxide SiO_2, it is relatively easy to fabricate all kinds of MOS (metal-oxide-semiconductor) device.

As chipmakers draw on all these attributes, sales of SiC power devices are on the rise. SiC Schottky barrier diodes and power MOSFETs specified at voltages from 600 V and 1700 V hit the market in 2001 and 2010, respectively, and sales have been ramping since 2015. Driving increases in shipments is the adoption of SiC power devices in servers and workstations, photovoltaic inverters, air-conditioners, fast chargers, railcars, and the electric vehicles of Tesla and Honda. In all these applications SiC provides substantial energy savings (see Figure 1). Sales of SiC devices are tipped to continue on this impressive trajectory, due to the tremendous expansion in the manufacture of electric vehicles, as well as huge investments in SiC material and devices underway in the US, Europe, Japan, and China.

Given the growing success of SiC power devices, it would be easy to assume that they are close to reaching their full potential. But the reality differs – the performance of SiC power MOSFETs is actually far from ideal. While on-state characteristics of 650 V SiC power MOSFETs are much better than their silicon equivalents, thanks to superior material properties, the on-resistance of a typical SiC product is almost ten times its ideal value.
The weaknesses of the SiC power MOSFET are highlighted by considering contributions to this device's on-resistance (see Figure 3). In any class of power MOSFET, on-resistance is a combination of several factors, including drift-layer resistance, channel resistance, substrate resistance, and contact resistance.

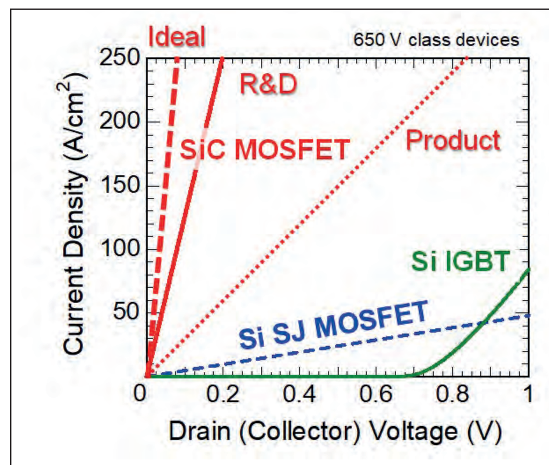


➤ Figure 1. (left) Unipolar limits of silicon and SiC power devices, showing the trade-off between the on-resistance and breakdown voltage. (right) Typical application areas for SiC power devices (MOSFETs and Schottky barrier diodes).

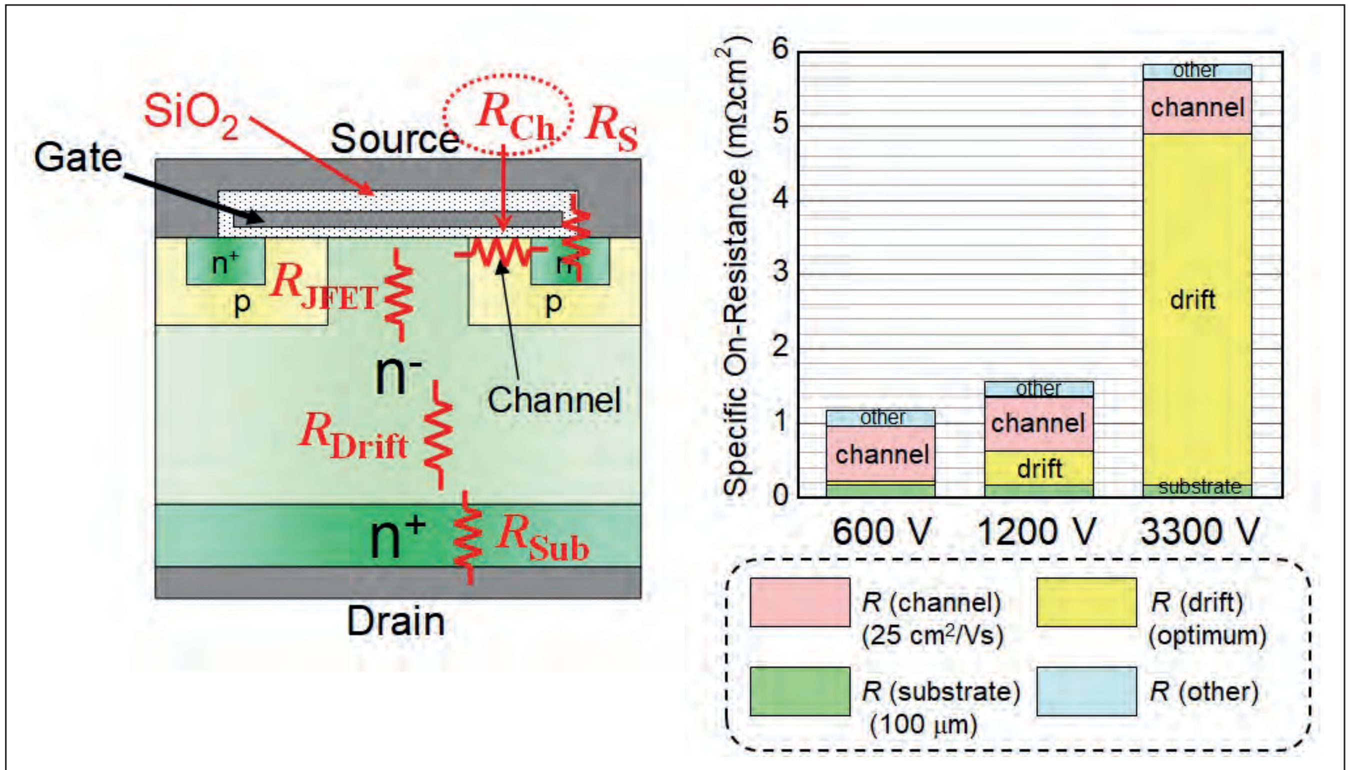
For the 600 V SiC power MOSFET, drift-layer resistance is so low that other contributions to resistance cannot be ignored. Compared to an equivalent silicon device, the drift-layer resistance of the SiC MOSFET is almost 300 times lower, while its channel resistance is about 30 times higher, due to poor channel mobility. This hike in channel resistance is incredibly detrimental, obliterating much of the benefit of a SiC power MOSFET over its silicon rival. For 600 V and 1200 V SiC MOSFETs, channel resistance accounts for about 70 percent and 50 percent of the total on-resistance, respectively.

A decades-old problem

An obvious question to ask is this: Why is the channel resistance of the SiC MOSFET so high? The reason is that at the interface between SiO_2 and



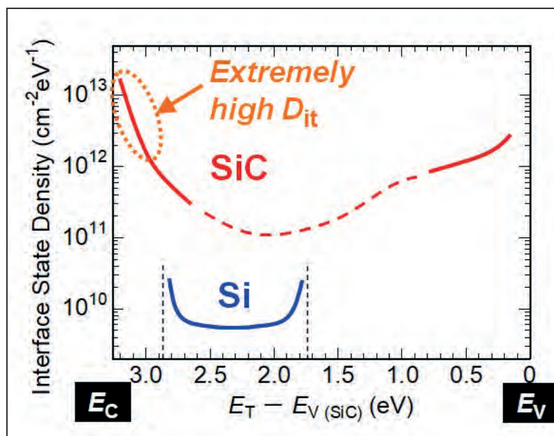
➤ Figure 2. The relationship between on-state current density and voltage for the 650 V-class SiC MOSFET, silicon super-junction (SJ) MOSFET and silicon insulated gate bipolar transistor (IGBT). For the SiC MOSFET, values are provided for the latest products, R&D device, and the ideal device.



➤ Figure 3. (left) Schematic cross-section of a vertical power MOSFET and its major resistance components. (right) Major contributors to the on-resistance of 600 V, 1200 V, and 3300 V SiC power MOSFETs. The on-resistances of 600 V and 1200 V SiC MOSFETs are severely limited by the channel resistance.

SiC there is an extremely high density of interface states, also known as traps. While silicon enjoys a density of interface states below 10^{10} cm^{-2} eV^{-1}, for SiC this exceeds 10^{12} cm^{-2} eV^{-1}. This high value has been holding back the performance of SiC devices since 1990. It is to blame for a channel mobility of no more than 40 cm^2 V^{-1} s^{-1}, despite a bulk electron mobility of around 1000 cm^2 V^{-1} s^{-1}. In fact, in SiC power MOSFETs where the *p*-body is relatively heavily doped, the channel mobility is even lower – typically, it's 15–25 cm^2 V^{-1} s^{-1}, so just a few percent of the value for bulk mobility.

Within the SiC community, a two-step oxide-formation process has been widely adopted for making power MOSFETs. This involves either the thermal oxidation of SiC; or deposition of SiO_2, followed by interface nitridation with a NO gas. Invention of the latter took place between 1997 and 2001.



➤ Figure 4. Energy distributions of the interface state density for SiC and silicon MOS structures. The extremely high defect density near the conduction band edge (E_c) in SiC is the main cause for the low mobility of *n*-channel MOSFETs.

Since the start of this century there have been numerous investigations and unique trials all over the world to try and improve the performance of the SiC MOSFET. Highlights from the last 20 years are sodium-enhanced oxidation developed at Philips, and annealing in a $POCl_3$ ambient, pioneered by engineers at NAIST. Both techniques resulted in high channel mobilities, typically 90-160 cm^2 V^{-1} s^{-1}, but the approaches are unsuitable, introducing a threshold-voltage instability and a short oxide lifetime at a high electric field.

Oxidation-free oxide formation

Our team at Kyoto University, Japan, has devoted many years to basic studies of the SiC MOS structure, and to also developing a novel technology for improving the MOSFET. Given that an interface state density over 10^{12} cm^{-2} eV^{-1} is somewhat abnormal, this suggests that something must be wrong with the SiO_2/SiC system. To uncover the cause, we have asked ourselves this simple question: What happens with carbon atoms in SiC when SiC is thermally oxidized? Almost all carbon atoms are removed during oxidation of SiC to form CO molecules. But not all – some remain near the interface, and are the main cause of defect

formation. We have some evidence to support our speculation. Between 2016 and 2018 we carried out a series of experiments involving secondary-ion mass spectrometry, which revealed that during oxidation of SiC a high density of carbon atoms accumulate near the SiO_2/SiC interface. These atoms are released by high-temperature argon annealing. Prior to this effort, between 2009 and 2014 we discovered that during oxidation of SiC, excess carbon atoms are emitted into the SiC bulk region where they can create bulk defects. So, based on the key findings of both these studies, it is clear that the behaviour of carbon atoms during SiC oxidation is not straightforward.

Offering further insight into the oxidation process are a number of first-principles calculations on the SiO_2/SiC interface. These theoretical investigations show that some C-C defects have low formation energies and can create electrically active levels near the conduction band edge of SiC.

After considering all these experimental findings and theoretical studies, we conceived the idea that it is crucial to avoid oxidation of SiC as much as possible when forming the gate oxide during MOSFET fabrication, because a high density of defects is inevitably generated by SiC oxidation. While the SiC community is happy to continue to use thermal oxidation of SiC to form SiO_2, our view is that much could be gained by taking the time to develop another approach to producing high-performance SiC MOSFETs. Our solution, which we will now detail, is to use a three-step process for forming a high-quality SiC MOS interface (this is summarised in Figures 5 and 6).

The process that we have developed begins by etching SiC in hydrogen gas to remove oxidation-induced defects near the surface. After this, we offer a choice for the second step in the process. One option of ours, which we'll refer to a process A, involves silicon deposition and conversion to SiO_2 by low-temperature oxidation; and our alternative, process B, is deposition of a SiO_2 film to exclude oxidation of SiC. Whichever option is taken, the third and final step is interface nitridation with a N_2 or NO gas to passivate some defects present at the interface between SiO_2 and SiC.

Note that at no point do we employ sacrificial oxidation of SiC, which is thermal oxidation followed by oxide removal. Those that do use sacrificial oxidation, either prior to MOSFET fabrication or

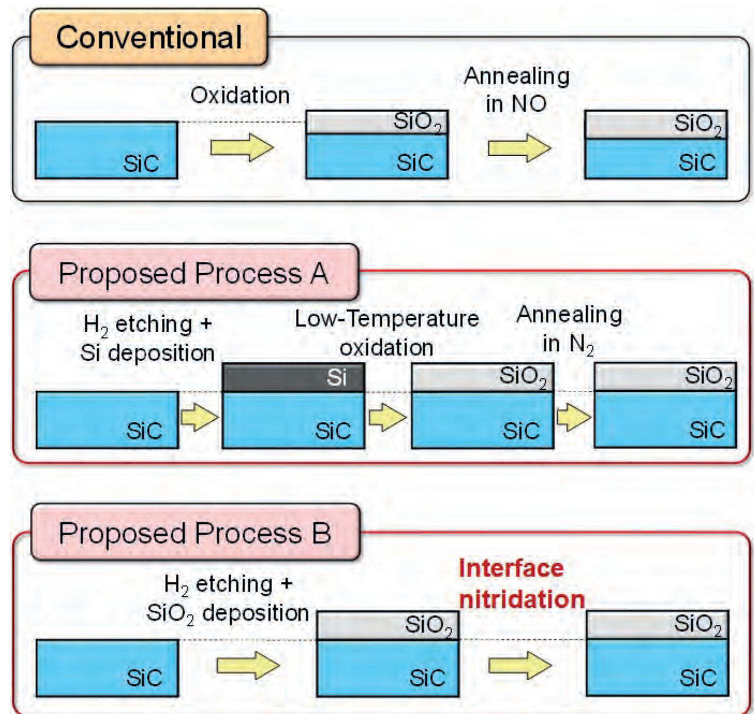


Figure 5. Flows for the conventional oxide formation process and two original processes (Process A and Process B) developed at Kyoto University. In the original processes, the oxide is formed by three steps; H_2 etching, oxide formation without SiC oxidation, and interface nitridation.

after epitaxial growth, are in danger of creating very defective regions on the surface of the SiC wafers.

Some members of our community will be surprised that we have had success with our technique. After all, there are many report of attempts to deposit a SiO_2 film when making a SiC MOSFET that have produced disappointing results. But our approach has a crucial difference, addressing defects that are generated during sacrificial oxidation and located in a sub-surface, up to a depth of 5 nm. We eradicate these imperfections with the first step of our process, the etching in hydrogen gas prior to SiO_2 deposition.

A handful of groups have also tried to deposit silicon, before converting this to SiO_2 by thermal oxidation. This is not successful: the temperature for conversion from silicon to SiO_2 is too high, and oxidation of the SiC surface results, driving the generation of a high density of defects. During our studies, we have looked in detail at the impact of all

After considering all these experimental findings and theoretical studies, we conceived the idea that it is crucial to avoid oxidation of SiC as much as possible when forming the gate oxide during MOSFET fabrication, because a high density of defects is inevitably generated by SiC oxidation

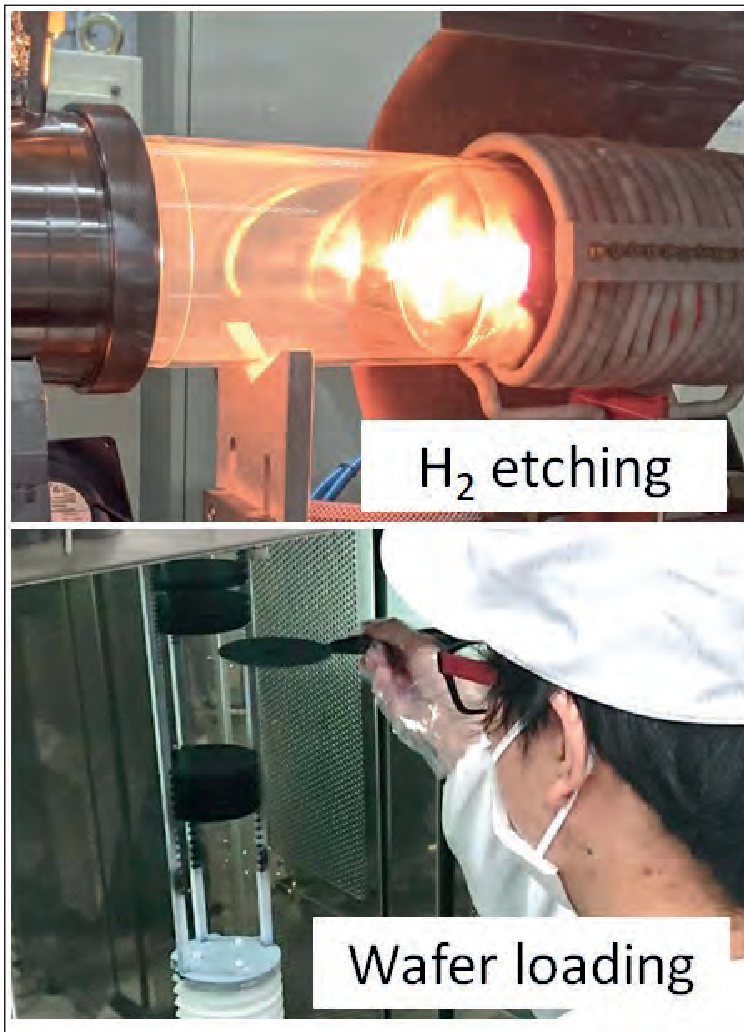


Figure 6. High-temperature hydrogen etching and wafer loading for interface nitridation to form high-quality SiO_2/SiC structures.

three steps of our process. We have found out that all of them are mandatory for realising a very low interface state density near the conduction band edge.

Depositing SiO_2

In this remainder of this article, we detail the SiO_2 deposition process (Process B), which has the merit of technological simplicity. We compare this approach with conventional thermal oxidation and nitridation annealing, in either N_2 or NO (see Table 1).

Measurements of the energy distributions of the interface state density for these four different processes underscore the promise of our original processes (see Figure 7, which demonstrates the superiority of process B, for both H_2-CVD-NO and H_2-CVD-N_2 processes). With Process B, the defect density at an energy 0.2 eV below the conduction band edge is about three-to-five times lower than it is for the conventional process used for manufacturing SiC power MOSFETs, based on oxidation and nitridation with NO. When the MOS is produced with the conventional process, the interface state density exhibits a rapid increase toward the band edge; with our original process energy distributions of the interface state density are rather flat, indicating a different nature of interface defects.

That advantage results in a superior performance for the MOSFET. For devices made with our process, channel mobilities are about twice those for equivalent transistors made with the conventional process, reaching values of between 80 $cm^2 V^{-1} s^{-1}$ and
85 $cm^2 V^{-1} s^{-1}$ (see Figure 8). We are particularly encouraged by the H_2-CVD-NO variant of our process that yields a high mobility at a high gate voltage, as well as a normally-off operation – that is, a threshold voltage greater than 0 V. Our process is the most promising technology to significantly enhance the performance of SiC power MOSFETs.

Development of the SiC power MOSFET has witnessed several false dawns. Processes showing initial promise by delivering low defect densities or high channel mobilities have fallen at the next hurdle, due to either a poor dielectric breakdown characteristic of the oxide or a large threshold voltage instability induced by the gate bias.

We have looked into both these causes of concern and are delighted to report that the devices produced by our process do not succumb to either of these pitfalls. When applying a high electric field to the oxide of our structures, we observe a beautiful Fowler-Nordheim profile above 6 MV/cm. For field strengths less than 6 MV/cm, leakage

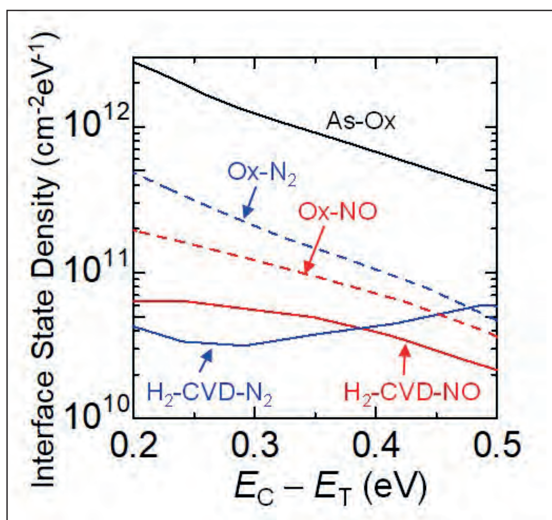
Process	H_2 etching	Oxide	Nitridation
H_2-CVD-N_2	w	PE-CVD (400°C)	N_2 (1400°C)
H_2-CVD-NO	w	PE-CVD (400°C)	NO (1250°C)
Ox-N_2	w/o	Oxidation (1300°C)	N_2 (1400°C)
Ox-NO	w/o	Oxidation (1300°C)	NO (1250°C)

Table 1. Four different processes for gate oxide formation. H_2-CVD-NO and H_2-CVD-N_2 are pioneered by Kyoto University, while Ox-NO and Ox-N_2 are conventional.

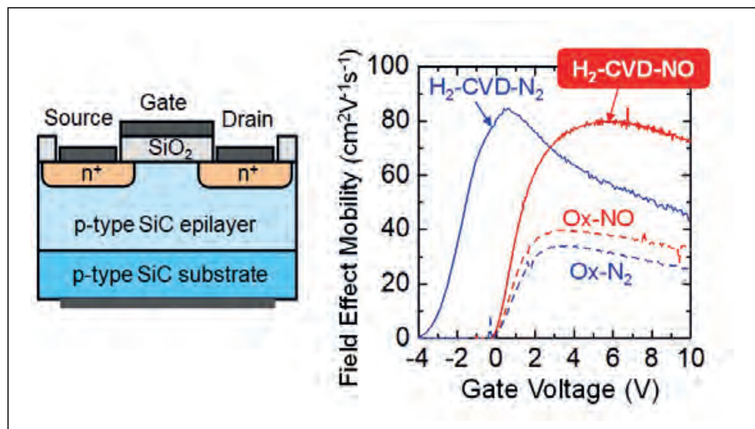
current is below our detection limit. Oxides formed with our H_2-CVD-NO process have a breakdown field in excess of
11.2 MV/cm, a value even higher than that for the conventional process. Offering further encouragement, the threshold voltage shift for SiC MOSFETs fabricated with our H_2-CVD-NO process is below 50 meV – this is smaller than that for devices made with the conventional process. Based on all these findings, we have no doubt that our process is the solution to a problem that had dogged the SiC MOSFET for 20 years.

One of our next goals is to apply our technology to non-basal planes. It is well known that SiC MOSFETs reach a higher level of performance when MOS channels are formed on non-basal planes ((1$\bar{1}$00) or (11$\bar{2}$0) face). In these devices, known as trench MOSFETs, channel mobilities of over 100 $cm^2 V^{-1} s^{-1}$ have been attained with the conventional process. Switching to our process should yield even higher values. Several SiC device manufacturers have shown much interest in this possibility, got in contact with us, and technology transfer has started.

A higher mobility is a major asset for a SiC power MOSFET. It delivers a substantial reduction in the specific on-resistance in 600 V to 1200 V devices, assuming a doubling or tripling of channel mobility. The smarter move by chipmakers, however, is to trim chip size while maintaining on-resistance. Halving the chip size would double the number of MOSFET die obtained from one wafer, and also drive production yield towards 100 percent, thanks to reductions in the probability of meeting a device-killing defect or a pattern failure. All these factors will help to reduce the cost of SiC power MOSFETs, and in turn accelerate the shipment of these devices.



➤ Figure 7. Energy distributions of the interface state density for SiC MOS structures with oxides formed by five different processes: as-oxidized (As-Ox); conventional oxidation and subsequent nitridation (Ox-NO and Ox-N_2); and the two novel technologies developed at Kyoto University (H_2-CVD-NO and H_2-CVD-N_2). The new processes yield a very low interface state density of typically just 5×10^{10} $cm^{-2}eV^{-1}$ near the conduction band edge.



➤ Figure 8. (left) Schematic cross-section of a fabricated *n*-channel SiC MOSFET. (right) Mobility versus gate voltage for SiC MOSFETs with gate oxides formed with four different processes. The H_2-CVD-NO MOSFET exhibits more than twice the mobility of the conventional MOSFET at a high gate voltage and normally-off operation.

While we have made much progress, one fundamental question remains: what is the origin of interface defects in SiC MOS structures? As we are now able to fabricate SiC MOS structures with a very low defect density, we can expect that physical and chemical analyses of the high-quality interface, as well as poor-quality samples, should provide useful insights into the cause of defects.

In addition to looking into this matter, we plan to further improve our original processes. We have realized that variations in the annealing conditions after oxide formation in the proposed processes have a striking impact on interface quality, which is not the case with conventional technology. This is further evidence that the development of the SiC MOS has just entered an exciting new era, after decades of stagnation.

➤ *The authors would like to acknowledge T. Kobayashi and M. Kaneko from Kyoto University for their contribution to this study.*

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GaN: A bridge to perfect E-mode HEMTs

Equipping a normally-off GaN HEMT with a *p*-FET bridge yields a large, stable threshold voltage

BY MENGYUAN HUA FROM SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

GaN IS STARTING to revolutionise power systems by providing higher efficiencies and miniaturization. Its wide bandgap and high saturation velocity enable it to excel in Baliga's figures-of-merit, and in turn allow power devices made from this material to block high voltages, switch at high frequencies, operate under high temperatures and provide low conduction and switching losses.

Attracted by all these attributes, interest in the deployment of GaN HEMTs is rocketing in many power applications that benefit from higher efficiencies, including electric grids, vehicle electrification, satellites, unmanned autonomous vehicles, photovoltaic systems, and power supplies for data centres.

Today's GaN HEMTs are not the finished article. One of their biggest roadblocks to fulfilling their potential concerns normally-off operation. To ensure fail-safe operation, end-users want GaN HEMTs to operate in enhancement mode, known for short as E-mode. Chipmakers have responded by launching E-mode GaN HEMTs that tend to realise normally-off operation through the adoption of a *p*-GaN gate. This design is compromised by a relatively small threshold voltage – it is less than 2 volts (this is for a current on-off ratio of 10^5). One unfortunate consequence is an increased likelihood of false turn-on during high-speed turn-off transitions, when the gate ring caused by parasitic inductance threatens to exceed the threshold voltage.

Several solutions have been proposed to boost the threshold voltage and reduce the chances of a false turn on. Options include increasing the gate metal work function and using source-connected *p*-GaN. However, the effectiveness of these methods is

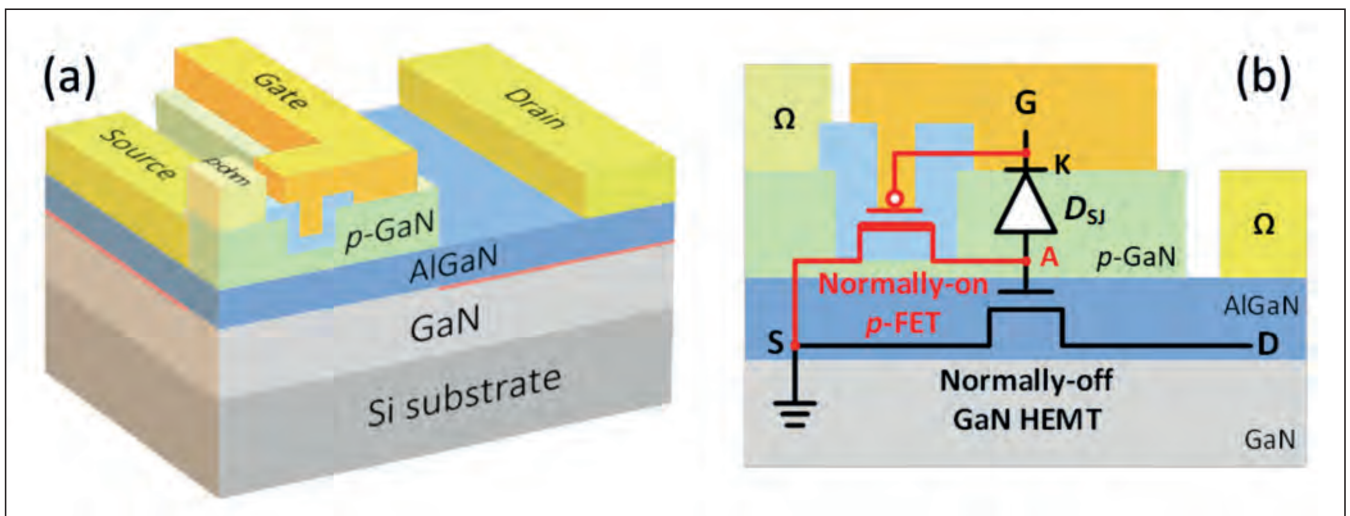
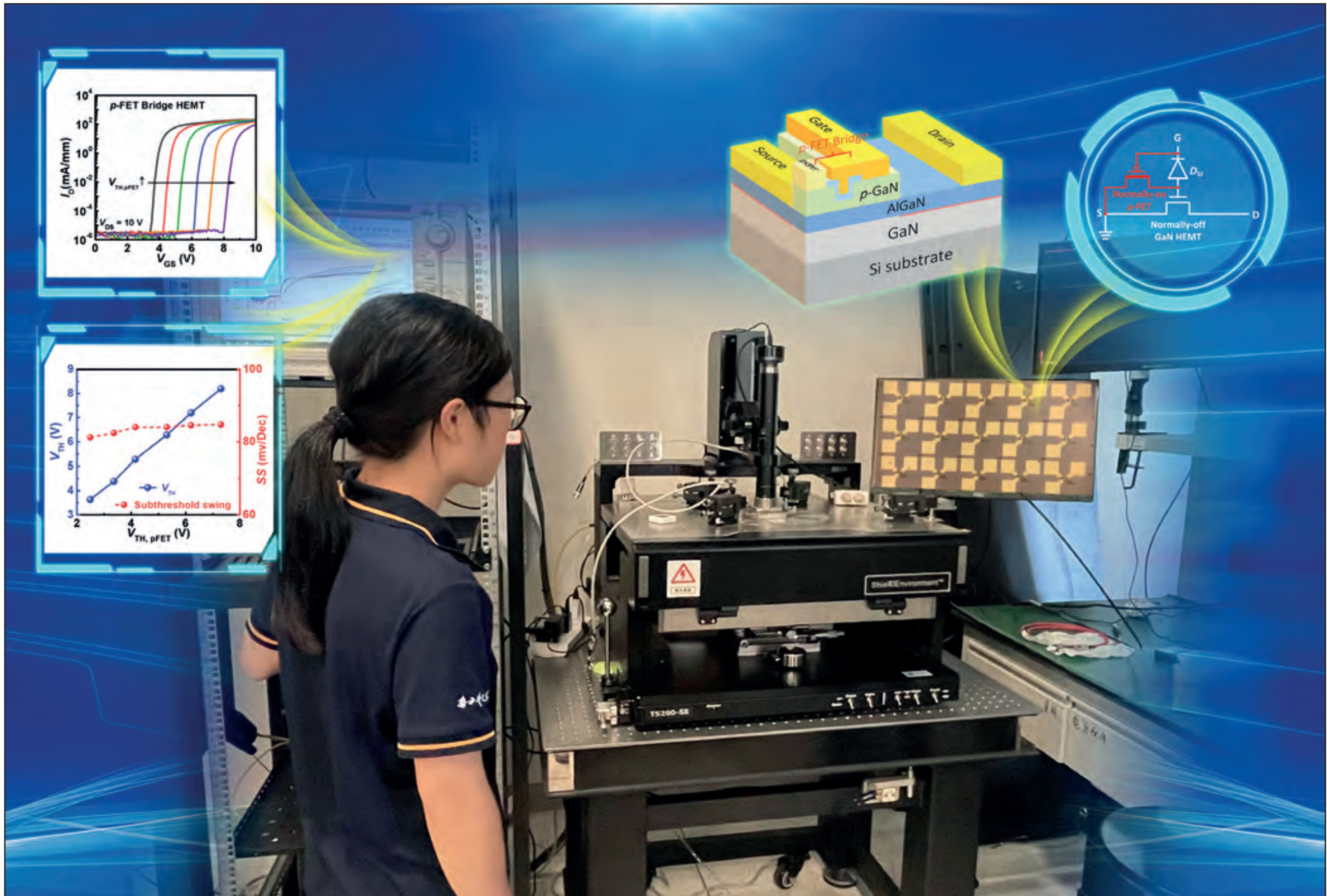


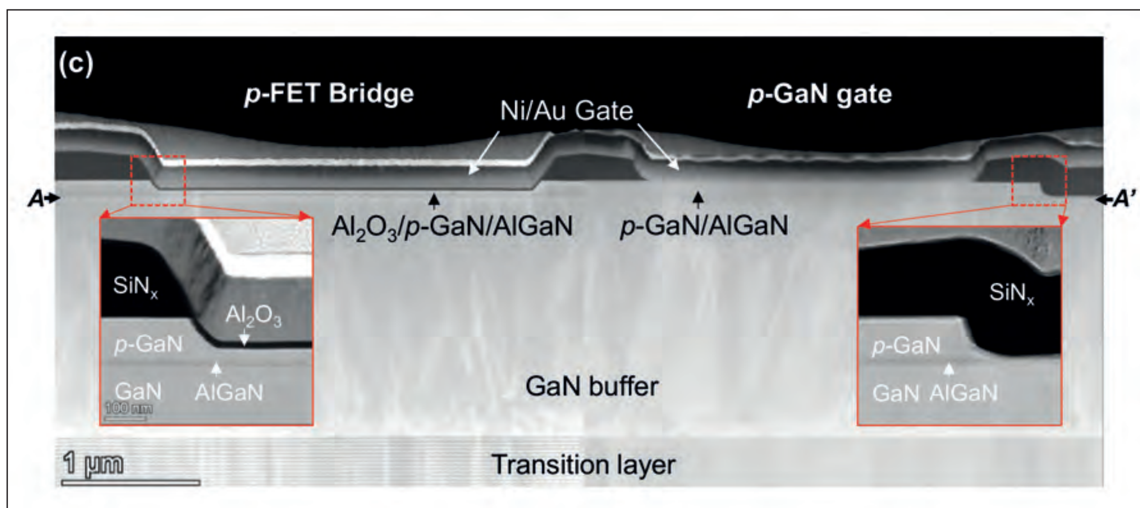
Figure 1. (a) A *p*-FET-bridge HEMT provides normally-off operation. (b) The equivalent circuit of the *p*-FET-bridge HEMT. The *p*-FET and HEMT are drawn on the same cross-section for simplicity, while in the actual device the 2DEG channel under the *p*-FET is depleted and the *p*-ohmic connects with the source are outside the *p*-FET area.



limited and they can introduce issues, such as instability in the threshold voltage and an inferior subthreshold swing.

The most common approach to overcoming the challenges associated with low threshold voltage is to use a bipolar gate-drive power supply. Providing a negative gate voltage avoids a false turn-on; but the price that is paid is complexity of gate-drive circuit design. This alternative approach is also hampered by the negative gate voltage, which threatens to accelerate device degradation by attracting the flow of holes to the gate side. The holes are generated by impact ionization in the high electric field region.

In addition to all these issues, there is another associated with a negative gate voltage: an increase in reverse-conduction loss. When GaN HEMTs handle inductive loads, during deadtime these transistors are subjected to a reverse-conduction state that provides a freewheeling current path. This condition is realized by turning on the drain-side channel with a drain-to-gate bias that exceeds the threshold voltage. An unwanted consequence is



➤ Figure 2. Cross-sectional transmission electron microscopy images of the recessed gate structure in the *p*-FET bridge and the Schottky-type *p*-GaN gate stack.

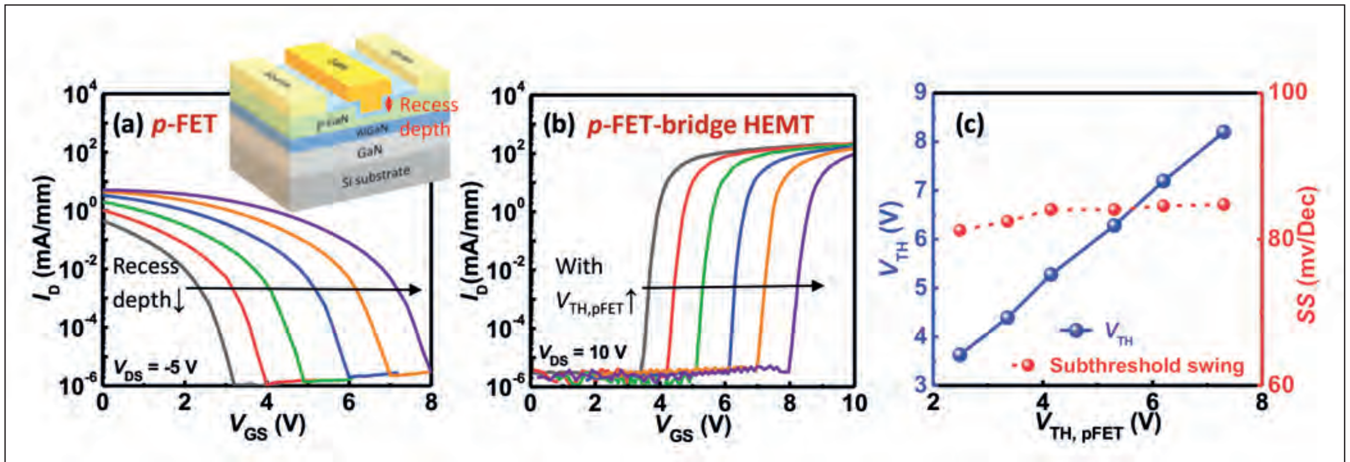


Figure 3. (a) Transfer characteristics of the gate-recessed *p*-FET with recess depths from 65 nm to 85 nm. The recess depth is estimated with atomic force microscopy after *p*-FET gate recess etching. (b) Transfer characteristics of *p*-FET-bridge HEMTs adopting *p*-FETs with a different threshold voltage ($V_{TH'pFET}$). (c) Dependence of V_{TH} and subthreshold swing (SS) of the *p*-FET-bridge HEMTs on $V_{TH'pFET}$.

that the negative gate voltage increases the reverse turn-on voltage of the GaN HEMT and exacerbates loss from reverse-conduction.

Tackling this issue head-on demands the development of an E-mode device with a large and stable threshold voltage. That's not an easy device to produce, as it requires the boosting of the threshold voltage while avoiding any increase to reverse-conduction loss. But our team at the Southern University of Science and Technology in Shenzhen, China, has succeeded on all fronts.

Our breakthrough stems from the introduction of a novel, elegant architecture for E-mode GaN HEMTs (see Figure 1). This design allows us to freely adjust the threshold voltage over a wide range without suffering from drawbacks, such as subthreshold swing degradation and threshold voltage instability. In addition to these very attractive attributes, our transistor inherently enables the decoupling of forward and reverse turn-on voltages. The pivotal enabler behind our success is the normally-on GaN *p*-FET that connects the source and the gate.

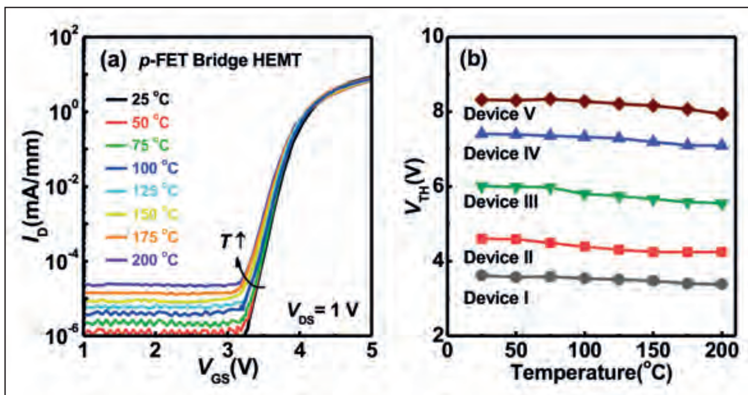


Figure 4. (a) Transfer characteristics of *p*-FET-bridge HEMTs measured at various temperatures from 25 °C to 200 °C. (b) Temperature-dependence of V_{TH} measured on *p*-FET-bridge HEMTs with different V_{TH}.

We refer to this architecture as the '*p*-FET bridge'. Outside the *p*-FET bridge area, our device has the same design as the conventional Schottky-type *p*-GaN gate HEMT – the gate metal and *p*-GaN layer form a Schottky junction diode on the top of a normally-off AlGaN/GaN HEMT. In the *p*-FET-bridge area of our HEMTs, a *p*-channel is added, connecting the anode of the Schottky junction diode with the source.

With our design, due to the normally-on *p*-channel, the anode of the Schottky junction diode is kept grounded before the *p*-channel pinch-off. Due to this arrangement, the 2DEG channel can be only turned on after the gate voltage is large enough to pinch off the *p*-channel. With these factors at play, we tune the threshold voltage of the *p*-FET-bridge HEMT so that it exceeds the threshold voltage of the *p*-FET.

An additional advantage of our architecture is its enhanced threshold voltage stability. When the device switches from a large gate or drain voltage back to a smaller one, the emitted holes from the floating *p*-GaN layer quickly flow back through the *p*-channel from the source side. This flow of charge helps ensure a stable threshold voltage.

Our technology is relatively easy to pursue, thanks to a readily available *p*-GaN layer on commercial platforms. With this approach, no complications come from the epi-structure. Another factor in our favour is that although the GaN-based *p*-FET is not mature enough to consider, that's not a show-stopper, because we only need a normally-on *p*-FET. With that particular device it is much easier to achieve a high drain current than it is with an E-mode *p*-FET. Armed with all these advantages, present epitaxy and fabrication techniques are ripe to demonstrate the *p*-FET-bridge HEMT. Note that success on this front could have wider implications, since this concept is not only suitable for lateral structures, but also vertical cousins.

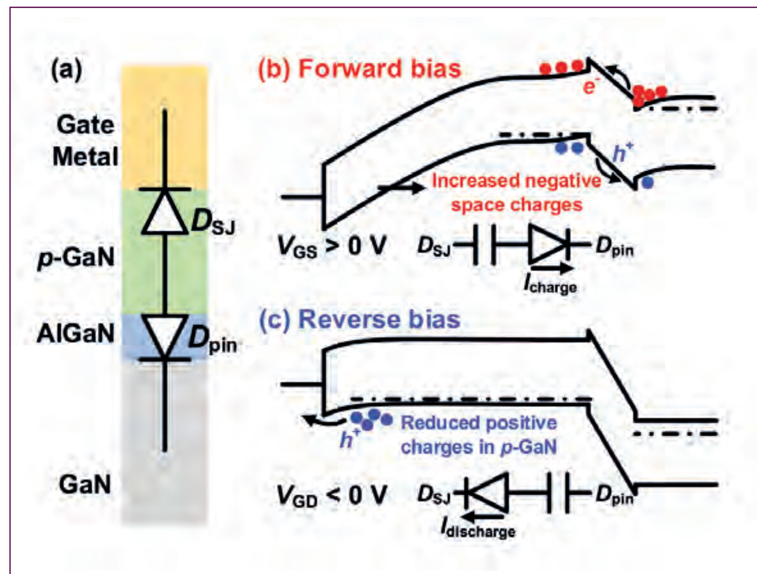
Concept demonstration

To produce our devices, we begin with 6-inch GaN-on-silicon wafers designed for E-mode *p*-GaN gate HEMTs. These epiwafers have a 4.2 µm-thick high-resistivity GaN buffer, a 420 nm GaN channel, a 15 nm-thick $Al_{0.15}Ga_{0.85}N$ barrier, and a 100 nm *p*-GaN cap that is doped with magnesium to a level of 4×10^{19} cm^{-3}. From this heterostructure we form HEMTs with a 3 µm gate length and a 15 µm gate-to-drain spacing. The later ensures a blocking voltage of more than 600 V.

Device fabrication begins by removing the *p*-GaN outside the gate region, accomplished with an inductively coupled plasma etcher that employs a combination of chlorine and boron trichloride gases. During this etch, we protect the *p*-GaN with an e-beam evaporated chromium layer. This is a better choice than a dielectric film − such as a SiN_x, SiO_2 or Al_2O_3 layer that can be deposited by PECVD or ALD − because chromium prevents plasma damage on the *p*-GaN surface and hydrogen incorporation in *p*-GaN. Ultimately, this ensures good *p*-type ohmic contacts.

Electron-beam evaporation, lift-off and annealing follow, to form source and drain electrodes. Subsequent photolithography defines the *p*-ohmic contact regions, before samples are dipped into a buffered oxide etchant for 5 minutes. We then turn to electron-beam evaporation to create a metal stack – a 20 nm layer of nickel, followed by a 20 nm layer of gold – prior to lift-off and annealing. Recessing the *p*-FET gate region follows, allowing us to adjust the HEMT's turn-on voltage. We then add about a 19 nm-thick layer of Al_2O_3 by ALD to create a *p*-FET gate dielectric.After device fabrication, we use an implanter to provide planar isolation.

Our final steps are to remove the Al_2O_3 layer outside the *p*-FET gate region and add gate electrodes and probing pads, comprised of 20 nm-thick nickel and 100 nm-thick gold (see Figure 2 for a scanning transmission electron microscope cross-sectional image of this fabricated device). To benchmark our devices, we have also fabricated individual *p*-FETs and conventional *p*-GaN gate HEMTs from the same epi-wafer.



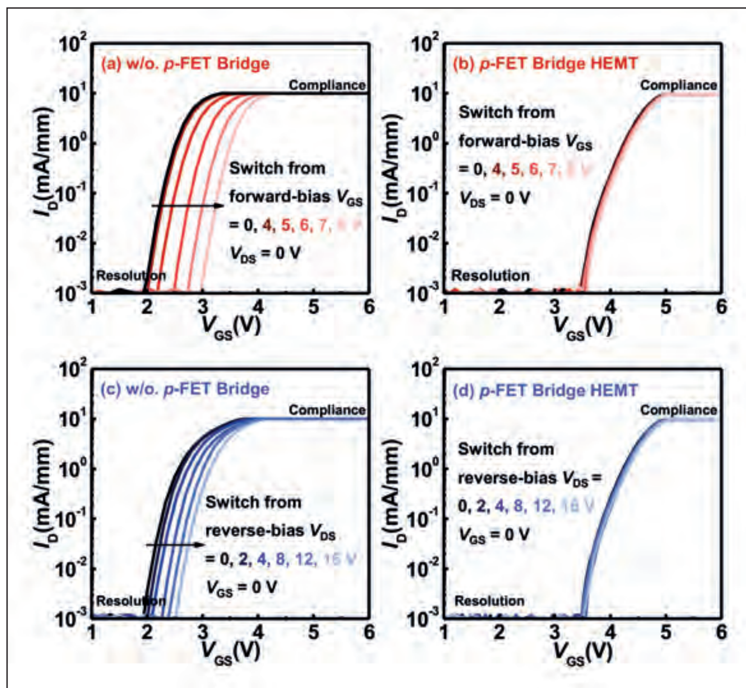
➤ Figure 5. (a) Equivalent circuit of the Schottky-type *p*-GaN gate stack. The band diagram along the gate stack under (b) forward bias and (c) reverse bias.

Freely adjustable threshold voltages...

By adjusting the turn-on voltage of our *p*-FET, we freely modulate the threshold voltage of our *p*-FET-bridge HEMTs over a wide range (see Figure 3).

Electrical measurements on a range of our devices reveal the impact of the depth of recess etch on normally-on operation (see Figure 3 (a)). Varying this depth from 65 nm to 85 nm shifts the threshold voltage from 2.4 V to 7.3 V, with a shallower recess depth providing a more positive threshold voltage. The forward saturation current for our *p*-FETs is 5.4 mA/mm, but far higher values may be possible by employing more elaborate techniques. In our

By adjusting the turn-on voltage, we can alter the threshold voltage from 3.6 V to 8.2 V in a linear manner. Encouragingly, the subthreshold swing shows negligible degradation when making large adjustments to the threshold voltage. Under the same gate over-drive bias – that is, the difference between the gate voltage and the threshold voltage – the on-resistance is similar for *p*-GaN gate HEMTs with and without a *p*-FET bridge.



➤ Figure 6. Transfer characteristics of (a) (c) the conventional Schottky-type *p*-GaN gate HEMTs, and (b) (d) *p*-FET-bridge HEMTs measured immediately after a 1 second hold under forward- (red curves) and reverse-bias (blue curves).

bridged devices, the *p*-FETs are always operated in the reverse-conduction region, with a gate bias higher than 0 V. One merit of this is that it avoids a large shift in the threshold voltage induced by a negative gate bias in the on-state. Consequently, the *p*-FET has a more stable threshold voltage in the –-FET-bridge devices.

By adjusting the turn-on voltage, we can alter the threshold voltage from 3.6 V to 8.2 V in a linear manner. Encouragingly, the subthreshold swing shows negligible degradation when making large adjustments to the threshold voltage. Under the same gate over-drive bias – that is, the difference between the gate voltage and the threshold voltage – the on-resistance is similar for *p*-GaN gate HEMTs with and without a *p*-FET bridge.

Although the 2DEG channel is depleted under the *p*-FET bridge, it may be possible to maintain a low total on-resistance thanks to the common access region outside the bridge area. We have also evaluated the thermal stability of the threshold voltage. To do this, we measured the transfer characteristics of several *p*-FET-bridge HEMTs, each with a different value for the threshold voltage. All of the tested HEMTs have a small variation in threshold voltage up to 200 °C – it is less than 0.4 V (see Figure 4).

An additional advantage of introducing the *p*-FET bridge is that this structure can maintain the same reverse turn-on voltage as the conventional *p*-GaN gate HEMT while realising a much higher threshold voltage for forward conduction.

Under reverse conduction, the *p*-GaN gate is always shorted to the source via the *p*-FET channel, ensuring that the HEMT behaves like a gate-injection transistor in this specific operation condition. Due to this, the reverse turn-on voltage is determined by the threshold voltage of the normally-off gate-injection transistor. Operation in this manner ensures that the reverse conduction capability of the 2DEG channel is fully utilized with no area sacrificed. By utilizing this property, it is possible to realise *p*-GaN gate HEMTs with lower on-resistance, higher threshold voltages, and lower reverse turn-on voltages by introducing the *p*-FET bridge.

... and enhanced stability

With conventional *p*-GaN gate HEMTs, there is the threat of a shift in threshold voltage during switching. In these devices the Schottky-type *p*-GaN gate can be regarded as one Schottky junction diode and one *p-i-n* diode, connected in series. Under forward bias with high gate bias, the *p-i-n* diode is forward biased, driving hole injection from the *p*-GaN to the channel and charging up the Schottky junction capacitor (see Figure 5 (a)). This leads to an increase in the negative space charge in the *p*-GaN layer.

When these conventional devices operate under reverse bias with a high drain bias, holes are emitted through the Schottky diode, discharging the *p-i-n* capacitor (see Figure 5 (b)). Thus, there are fewer holes in the *p*-GaN. Switching the gate and drain voltages back to a lower level results in hole deficiency, due to the Schottky barrier blocking speedy replenishment of holes into the *p*-GaN layer.

Eventually, positive threshold voltage shifts are observed (see Figure 6). A significant advantage of our design is that the floating *p*-GaN layer is shorted with the source. This ensures a stable threshold voltage, with holes immediately flowing back to *p*-GaN after switching from a high-stress voltage to a lower level.

In short, our HEMT design excels in delivering a stable threshold voltage that is adjustable over a wide range. This is an important breakthrough, taking this device a step further to providing widespread high-efficiency energy conversion.

FURTHER READING

➤ M. Hua *et al.* 'E-mode *p*-FET-bridge HEMT for Higher V_{TH} and Enhanced Stability', in 2020 IEEE International Electron Devices Meeting (IEDM), December 12-18, 2020

➤ J. Chen *et al.* "Decoupling of Forward and Reverse Turn-on Threshold Voltages in Schottky-Type *p*-GaN Gate HEMTs," in IEEE Electron Device Letters, doi: 10.1109/LED.2021.3077081

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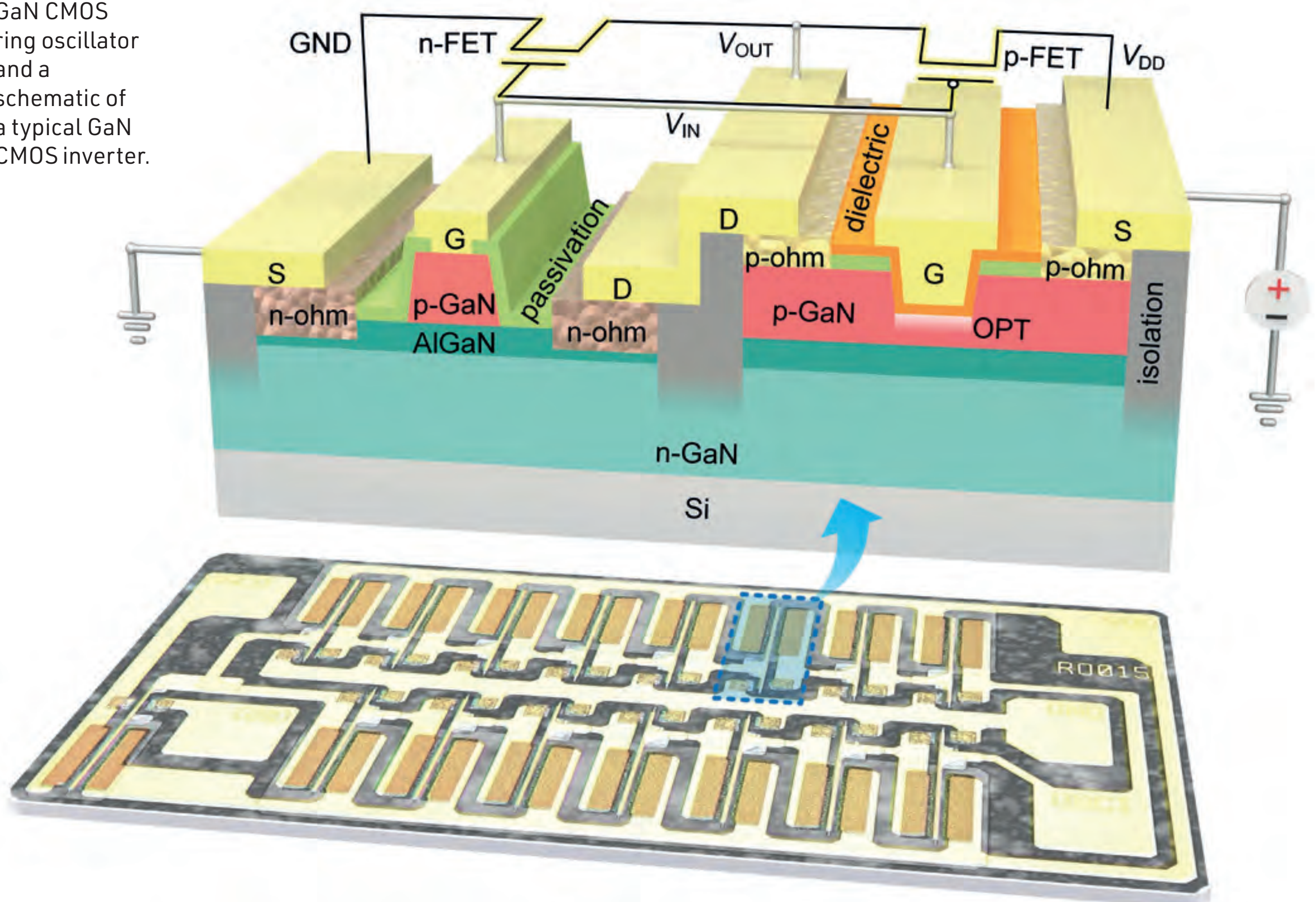
Taking GaN CMOS to the IC

Forming logic circuits with a power HEMT platform that features a *p*-GaN gate provides a significant step towards unlocking the full potential of GaN integration

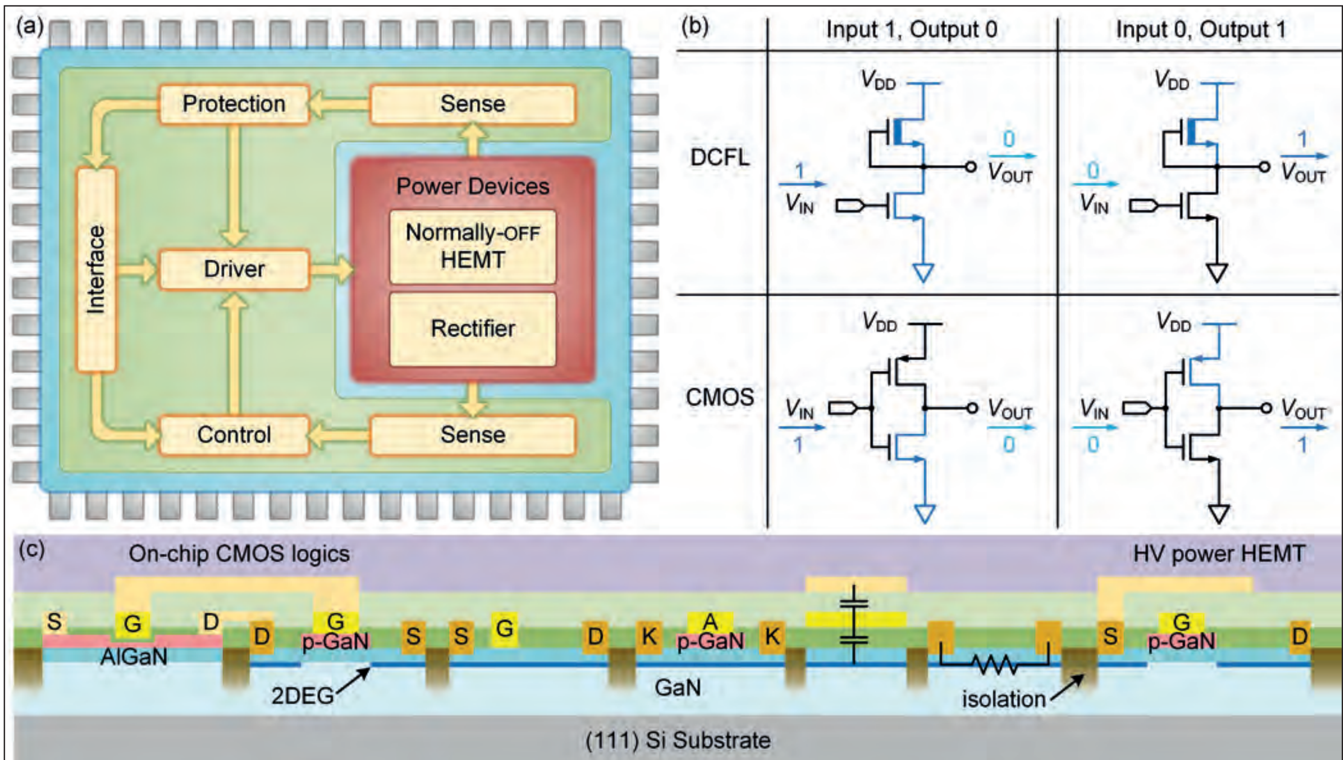
BY ZHEYANG ZHENG, LI ZHANG AND KEVIN CHEN FROM
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

CMOS TECHNOLOGY continues to prevail in very large-scale and mixed-signal ICs. In these forms of circuit, CMOS has dominated for the past four decades, thanks to topping the list of the most energy-efficient circuit topologies. Whenever new electronic devices are explored in other semiconductor materials, there is a hunt for complementary devices, to see whether this could lead to a superior successor to silicon CMOS. However, such a pursuit tends to be full of obstacles, with GaN providing a typical example.

This wide-bandgap semiconductor, blessed with an inherent capability to form a very high-mobility two-



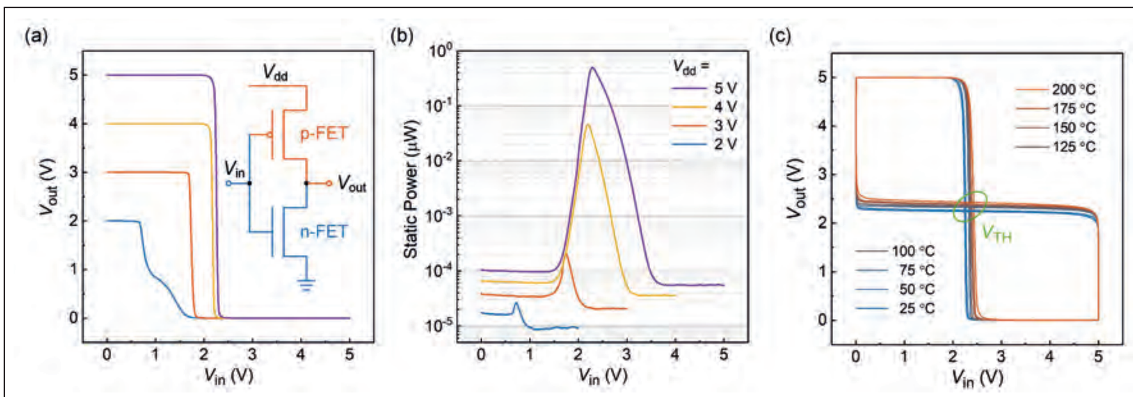
➤ A 15-stage GaN CMOS ring oscillator and a schematic of a typical GaN CMOS inverter.



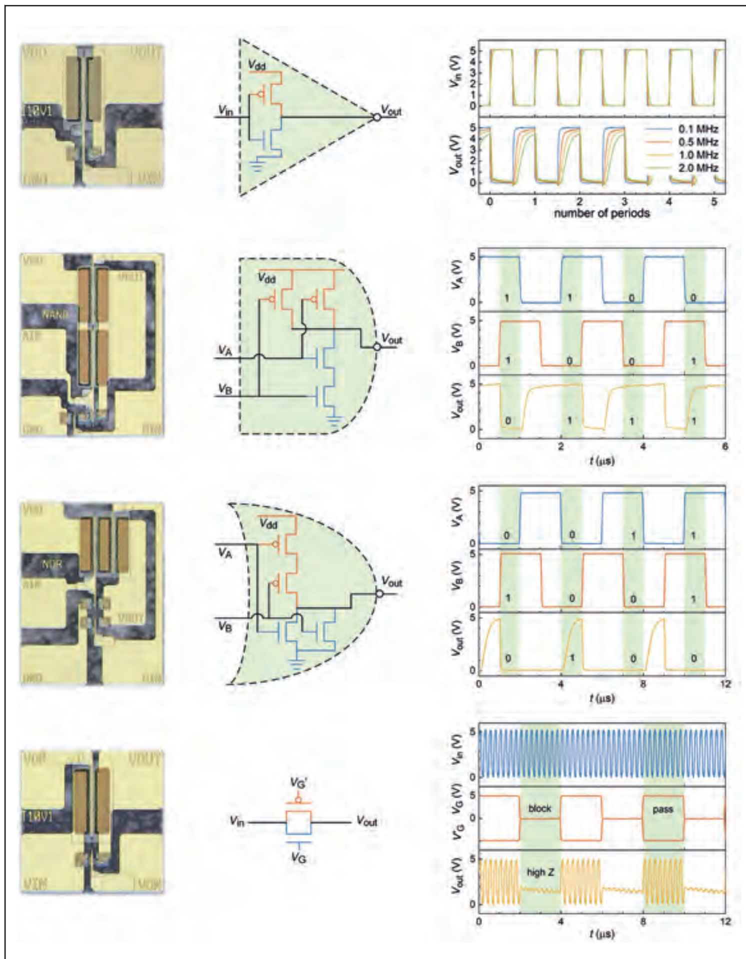
➤ Figure 1. One attractive approach to fully unlocking the potential of GaN in power electronics is the monolithic integration of the entire power conversion system. (a) depicts a GaN-based smart power platform. (b) illustrates that when a logic inverter is made of *n*-FET-based topologies, such as directly-coupled-FET-logic (DCFL), there would be one logic state when the gate has significant static power dissipation. Using the CMOS topology instead could guarantee the suppression of static power dissipation at both states; (c) is a cross-section view of available components on the *p*-GaN gate power HEMT platform. The on-chip CMOS logics would be inducted onto this platform.

dimensional electron gas (2DEG) channel, has many attractive attributes. This has driven widespread deployment of *n*-channel GaN HEMTs in 5G base stations, as well as ultra-compact power adaptors and supplies for mobile devices. In the near-term, more exciting applications are sure to emerge that are power-hungry, yet demand ultra-compactness in power supplies. This will create an appreciable market for GaN. However, much is still to be done when it comes to GaN CMOS. Efforts have been held back by undesirable material properties for implementing *p*-channel FETs and a lack of essential applications that would spur development.

Part of the problem with *p*-channel devices is the very low hole mobility in GaN. It is typically just 20 $cm^2 V^{-1} s^{-1}$, compared with around 2000 $cm^2 V^{-1} s^{-1}$ for the electron mobility in the 2DEG channel. Such a low value dampens the interest of many researchers. What's more, there doesn't appear to be a need for GaN CMOS in power amplifiers and power switches. GaN HEMTs tend to act as powerful discrete devices, usually incorporating a very large



➤ Figure 2. A GaN CMOS logic inverter shows impressive quasi-static performances, including rail-to-rail operation, V_{DD}-adaptive and well-placed transition thresholds, substantially suppressed static power dissipation, broad noise margins, and high thermal stability.



➤ Figure 3. HKUST has demonstrated a full family of elementary logic gates with GaN CMOS. This figure shows their photos, circuit diagrams, and operating waveforms with sub-megahertz frequencies.

gate width for regulating high currents and handling high powers. Consequently, despite the rapid development of GaN HEMTs, demonstrations of GaN *p*-FETs are few and far between, with efforts related to CMOS logic inverters even rarer.

Now the situation has started to change. With GaN power HEMTs intensively advanced, peripheral circuitry is starting to become a non-negligible performance-limiting factor for the entire power conversion system. Parasitic inductances are the most undesirable but inevitable issue – they are induced by interconnections between power HEMTs and other off-chip functional blocks, such as the gate driver and miscellaneous sensing modules. By hampering the continuous push towards higher operating frequencies, these inductances are compromising the superiority of the GaN HEMT. One promising solution is monolithic integration – that is, the deployment of as many peripherals as possible on the same chip as the GaN HEMTs.

Our team at The Hong Kong University of Science and Technology (HKUST) have been developing integrated GaN technology for many years. The planar structure for this class of device inherently favours high-density monolithic integration (see Figure 1).

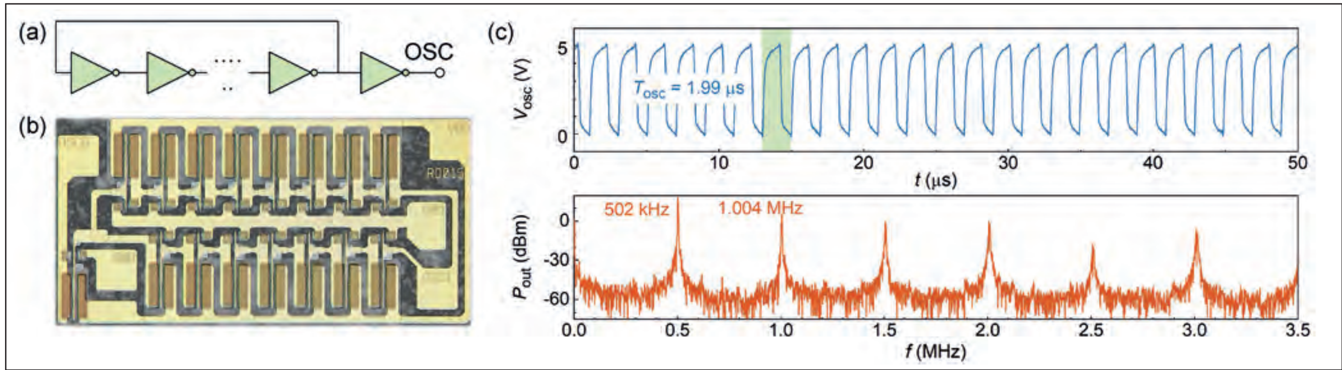
Back in 2009 we proposed the concept of 'GaN smart power systems', and since then we have kept on advancing this technique, working in partnership with colleagues in academia and industry.
As more and more functional blocks have been demonstrated, and entire systems have got more and more complicated, there has been a significant increase in the use of logic circuits. In fact, it is these logic circuits that make the power system 'smarter' and more intelligent. For GaN, logic circuits are still constructed from just *n*-channel FETs. Due to this, as the number of logic gates increases, power consumption has become a concern. It is this state-of-affairs that hampered the silicon-based ICs of the late 1970s. Back then, NMOS logic circuits consumed too much power, giving rise to CMOS.

With a potential beneficiary in mind, we wanted to develop GaN CMOS. Due to the low mobility of holes, we knew that this technology would never be deployed in cutting-edge ultra-high-speed/ low-power logic ICs. However, it could deliver on-chip logic services for specific applications, such as power electronics, thanks to its high energy efficiency. We were also intrigued in how much we could benefit from the *p*-GaN epi-layer that is readily available in the *p*-GaN gate power HEMT technology, a dominant platform for commercial GaN power electronics.

The GaN CMOS family

Three immediate benefits come from using the commercial *p*-GaN gate HEMT epi-structure to produce GaN CMOS ICs. First, this enables straightforward integration with the power HEMT. This is most welcome, given the commercial opportunity associated with the monolithic integration of high-energy-efficiency peripheral logic gates with power switches. Second, owing to the maturity of power HEMT technology on this platform, GaN *n*-FETs for CMOS ICs are naturally ready. All that's required to move from power to CMOS is to make some simple changes in the physical layout, because *n*-FETs for both applications share exactly the same device structure and fabrication steps. Third, the *p*-GaN layer is designed to deplete the 2DEG channel underneath, which could only be restored by removing the *p*-GaN layer above. This enables the *p*-channel and *n*-channel to be naturally de-coupled, suppressing crosstalk.

Drawing on the commercial *p*-GaN gate HEMT platform, our team has fabricated a large set of elementary CMOS logic gates. They include the inverter, which clearly shows almost all desired 'CMOS properties', such as: rail-to-rail output; adaptively varied transition thresholds, roughly following half of the supply voltage (V_{DD}); substantially suppressed static power; a very high voltage gain; and broad noise margins. More importantly, thanks to the use of a wide bandgap material, our CMOS logic inverter demonstrates satisfactory thermal stability (see Figure 2). When considering static characteristics, the presented GaN CMOS inverter is almost perfect for use.



➤ Figure 4. Demonstration of multistage GaN CMOS logic ICs. The team at HKUST uses a 15-stage ring oscillator composed of GaN CMOS logic inverters as an example, showing its oscillating waveform and power spectrum.

We have also demonstrated a NAND gate, a NOR gate, and a transmission gate. All three exhibit rail-to-rail outputs and deliver correct functions at megahertz-level frequencies (see Figure 3). By demonstrating this logic gate family, we have shown that, in theory, the essential building blocks of any logic function can be readily designed and implemented. From this foundation we have gone on to show that by cascading these blocks in certain ways to form more complex logic circuits, it is possible to construct multi-stage logic circuits, such as a monolithic 15-stage ring oscillator oscillating at a sub-megahertz frequency (see Figure 4).

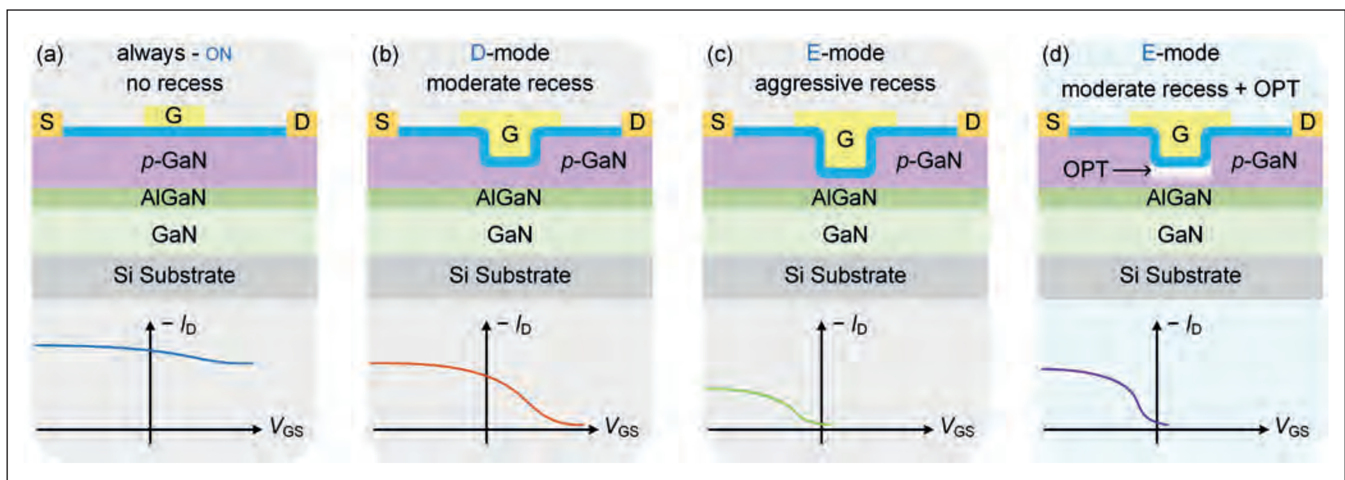
Realising E-mode *p*-FETs

The key to realising GaN CMOS ICs is to produce satisfactory GaN *p*-FETs on the selected platform. With our commercial *p*-GaN gate HEMT epi-structure, we enjoy appreciable benefits, but they come with stringent restrictions. For example, to ensure a sufficiently E-mode operation of the power HEMT, the *p*-GaN must be heavily doped and sufficiently thick to prevent punch-through at a high gate bias.

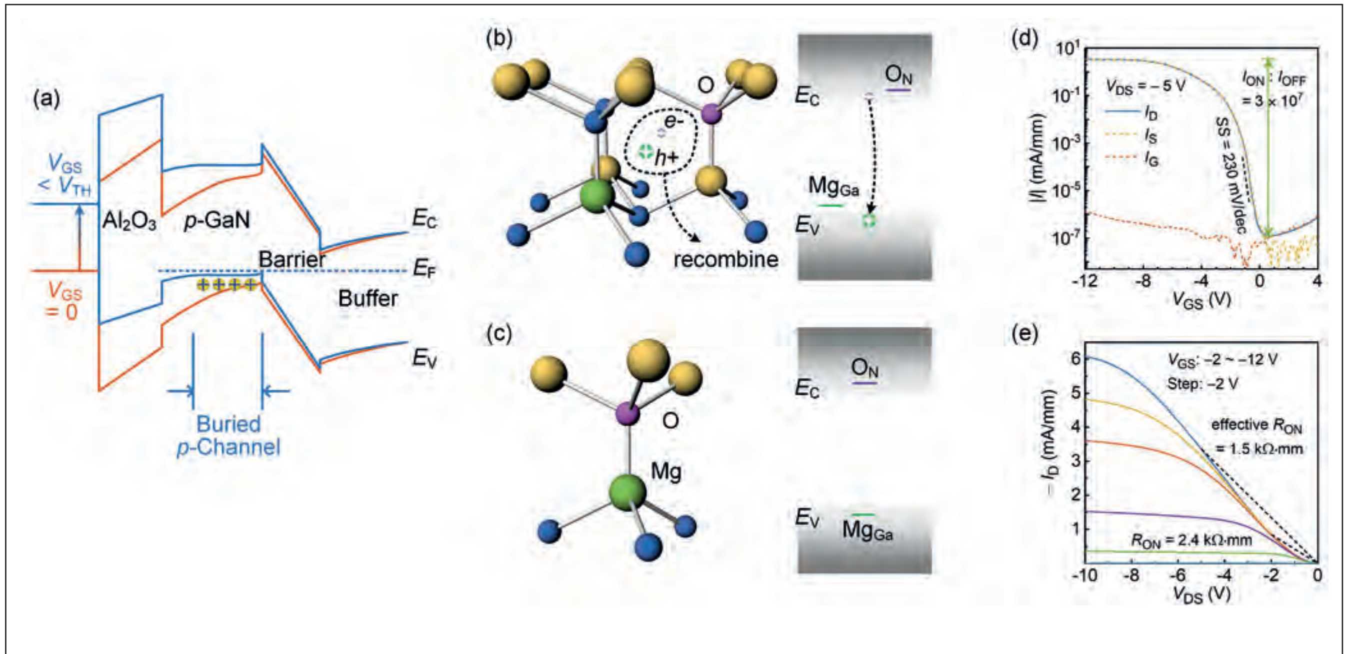
It is essential to include a recess in the design. Otherwise, the *p*-GaN, which is thick and heavily doped, could never be depleted by the gate, as the electric field would become dramatically high and induce a catastrophic breakdown. Once only a moderate portion of *p*-GaN is removed – for example, by still retaining 30 nm of *p*-GaN – the channel can be turned off with a positive gate voltage. Operating in this manner, the *p*-FET works in a depletion mode.

However, a more significant modification to the design is needed to form E-mode FETs, which are mandatory for realizing ICs with truly 'CMOS-like' behaviour (especially, completely suppressed power dissipation at static states). One option is further thinning of the channel. However, while this drives the device into E-mode, this comes at the expense of a significantly reduced on-state current, because the channel for current conduction is too thin.

Of greater concern, though, is the poor-quality of the etched *p*-GaN surface that introduces strong scattering to holes in the very thin *p*-channel.

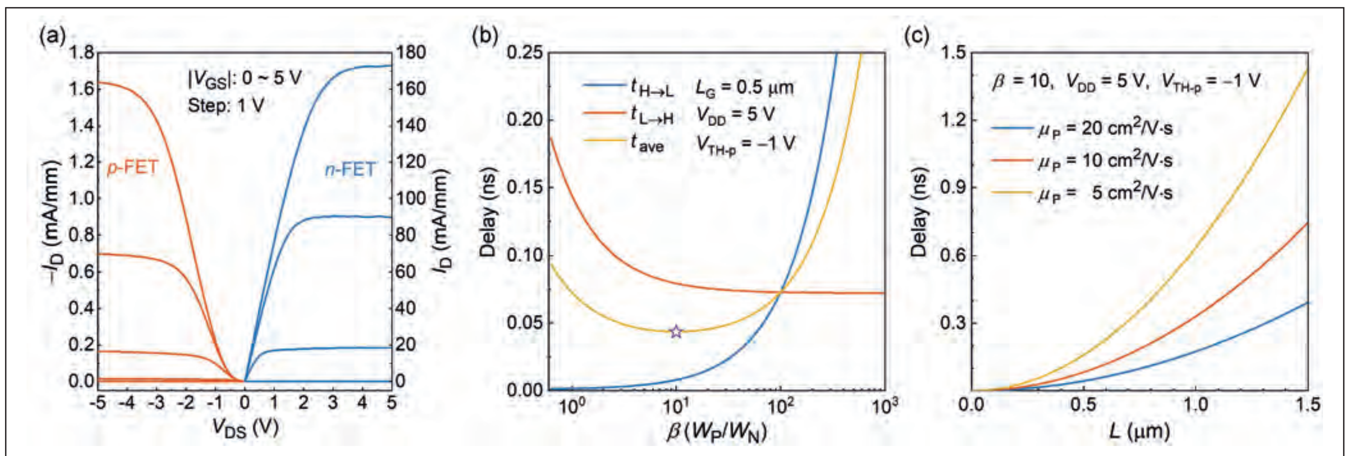


➤ Figure 5. Approaches to realising E-mode *p*-FETs on the *p*-GaN gate HEMT platform. One option is to gradually thin down the gated region to drive the device from always-on to D-mode and then E-mode. However, the aggressive etching would significantly reduce the on-state current. The team at HKUST has taken a different approach, adopting a 'moderate gate recess + oxygen plasma treatment (OPT)' to realize E-mode operation while maintaining reasonable on-current.

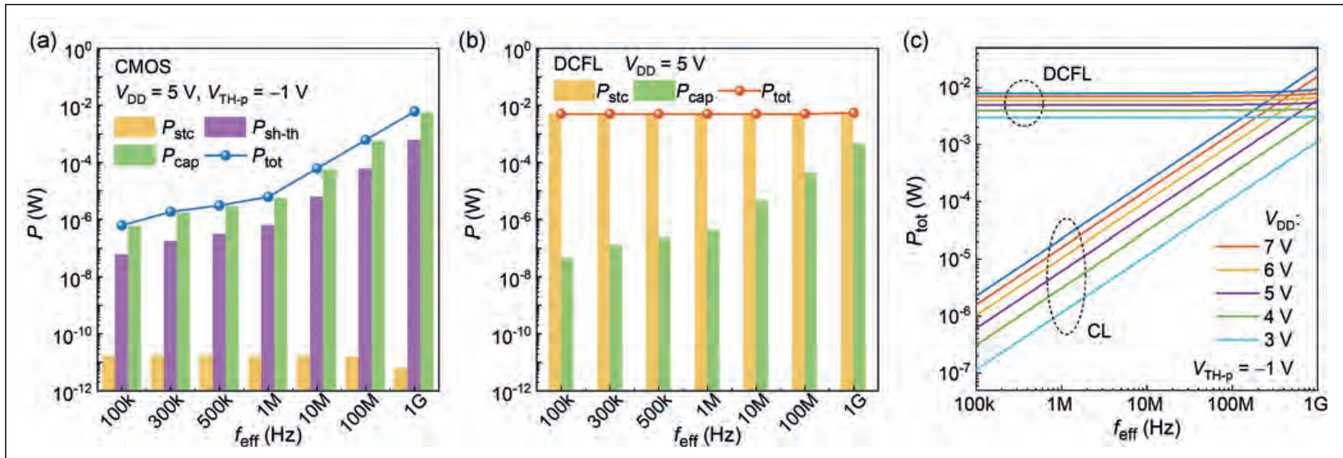


➤ Figure 6. Working principle and device performance of a buried channel GaN p-FET formed using an oxygen plasma treatment. (a) shows energy band diagrams of the off-state (with $V_{GS} = 0$ V) and the on-state (with $V_{GS} < V_{TH}$); (b) and (c) conceptually show possible mechanisms of why oxygen plasma treatment could convert the p-GaN surfaces to free-of-holes. (b) shows that oxygen acts a donor to ionize electrons to compensate holes. (c) shows that oxygen forms a Mg-O complex to directly passivate the acceptor. (d) and (e) plot transfer and output characteristics of the p-FET, respectively. The p-FET exhibits stringent E-mode operation, reasonable on-state current density, and a high on-off ratio.

By adopting a novel approach to solve this dilemma, we have maintained a reasonable on-state current density while realizing E-mode operation. This is accomplished with an architecture that combines a moderate recess with an oxygen plasma treatment to the recessed p-GaN surface. With this approach, we realise E-mode operation in a 'gentler' way (see Figure 5 for a comparison between our device and the conventional alternative). We use an oxygen plasma treatment to convert the top layer of retained p-GaN free-of-holes, thereby facilitating depletion of the p-channel buried below. It is possible that oxygen appearing in the p-GaN could act as a shallow donor, ionising electrons to recombine with holes; or it could form Mg-O complexes, passivating the magnesium acceptor directly (see Figure 6).



➤ Figure 7. The performance of the n-FET and p-FET on the p-GaN gate platform determine the optimization of the propagation delay at the circuit level. (a) Given the significant mobility mismatch between electrons and holes, the n-FET and p-FET exhibit a two-orders-of-magnitude difference in current density. (b) With device ratio, β, increasing, the average propagation delay firstly drops and then rises. Thus, there is an optimum value of β, which is around the inverse of the square root of the mobility ratio. (c) Reducing the gate length could reduce the delay in a quadratic way. Overall, it is achievable to realize a sub-nanosecond delay for GaN CMOS logic gates, which could satisfy the requirement of current GaN-based power conversion systems.



➤ Figure 8. By replacing the DCFL logic circuits with CMOS logic circuits, the power loss induced by logic blocks would be greatly reduced, because the static power dissipation (P_{stc}) in CMOS circuits is negligible. (a) shows that for a CMOS logic gate, dominating power dissipation components are contributed by the shoot-through current ($P_{sh\text{-}th}$) and the capacitance charging/discharging current (P_{cap}). Both arise at transition states and thus the total power dissipation (P_{tot}) increases with frequency. (b) shows that for a DCFL logic gate, the dominating component is P_{stc} (in this case $P_{sh\text{-}th}$ is included in P_{stc}). (c) shows that when the switching frequency is lower than 100 MHz, CMOS circuits have significantly lower power loss than DCFL circuits.

Operating with a negative gate bias, the holes in our E-mode FETs can be restored to the buried *p*-channel. This maintains a high hole mobility, because it is separated from the plasma-etched problematic interface between the oxide and *p*-GaN by the region treated by the oxygen plasma. Thanks to this, the buried-channel GaN *p*-FET exhibits decent electrical characteristics. The threshold voltage is stringently negative, and the on-state current density reasonable, exceeding 6 mA/mm. Overall, the on/off-state current ratio can reach seven orders of magnitude. We believe that the well-suppressed off-state leakage current could be attributed to a combination of: an insulating gate structure that guarantees a very low gate leakage; a stringent E-mode operation, which ensures a fully depleted channel; and a fluorine ion-based planar isolation technique that eradicates detrimental leaky sidewalls.

While there is still much room for further optimization, the performance delivered by this commercial platform-based *p*-FET is already impressive, and shows that developing CMOS ICs on exactly this platform is highly feasible. Building on this start, we had the motivation to construct CMOS ICs, and produce the first GaN CMOS IC family.

Performance projections

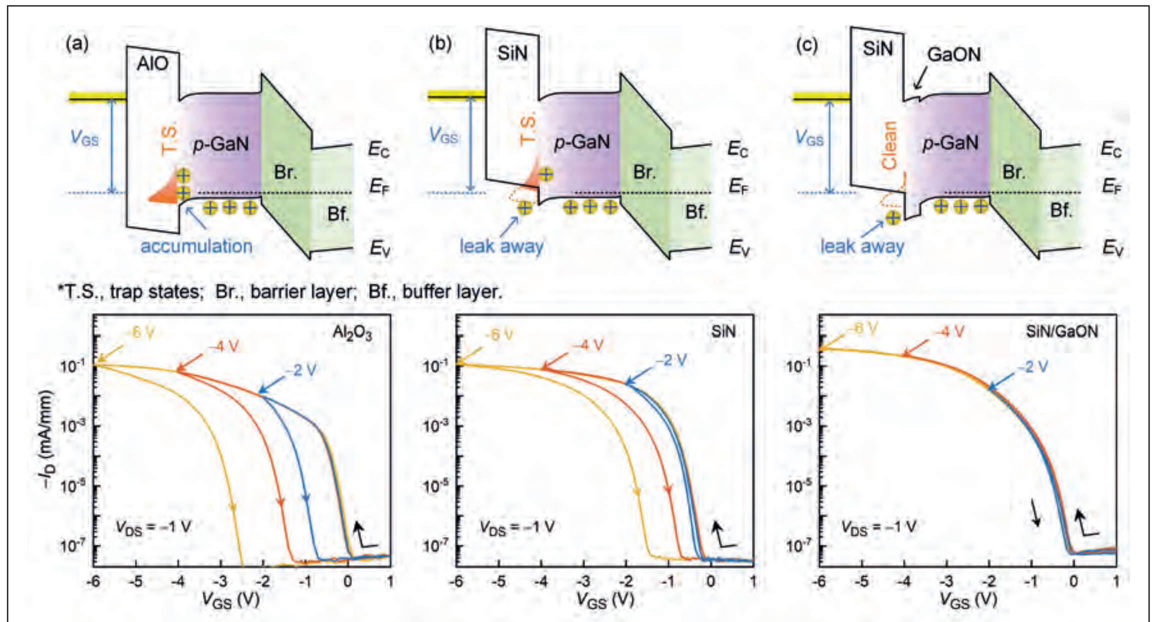
There are two aspects to evaluating the potential and the utility of GaN CMOS. One is the limit of its operating speed, given restrictions related to material properties and fabrication capabilities, and the other is the extent of energy savings associated with replacing *n*-FET-based logics with CMOS logics.

Right now it is not that practical to build circuit models for simulation-based studies, because the currently available devices have not been intensively optimized. So to gauge the potential of GaN CMOS, we have conducted an analysis using reasonable simplifications. This revealed that the operating speed of GaN CMOS will comfortably satisfy the requirement of GaN-based power systems and, as expected, that GaN CMOS is capable of significantly reducing power loss in the interested frequency regime.

A sufficient operating speed may come as a surprise, given the massive mismatch between the mobilities of electrons and holes that leads to a two-orders-of-magnitude difference in the current density of *n*-FETs and *p*-FETs (see Figure 7 (a)). Due to this, GaN CMOS logic gates inevitably exhibit asymmetric rising and falling edges. However, it is the average delay time that determines the speed of the circuit.

At the circuit level, what matters is to optimise the device ratio between the *p*-FET and the *n*-FET. When there is a hole mobility of 20 $cm^2 V^{-1} s^{-1}$, using a gate length of 0.5 μm enables an optimum delay time that's less than 50 ps (see Figure 7 (b)) – that is sufficiently fast.

When judged in terms of energy efficiency, there is no doubt that CMOS outperforms *n*-FET-based logics, such as DCFL, which is short for direct-coupled FET logic (see Figure 8). In CMOS circuits static power dissipation is negligible, with power loss mainly coming from the shoot-through current and a charging and discharging of the capacitor during transition states. But for DCFL circuits, static power dissipation dominates. Note also that as the operating frequency increases, so does the power dissipation of GaN CMOS. However, despite these concerns, in the interested frequency regime of a power system – it has a typical operating frequency ranging from 100 kHz to 10 MHz – CMOS has the potential to dramatically reduce power loss.

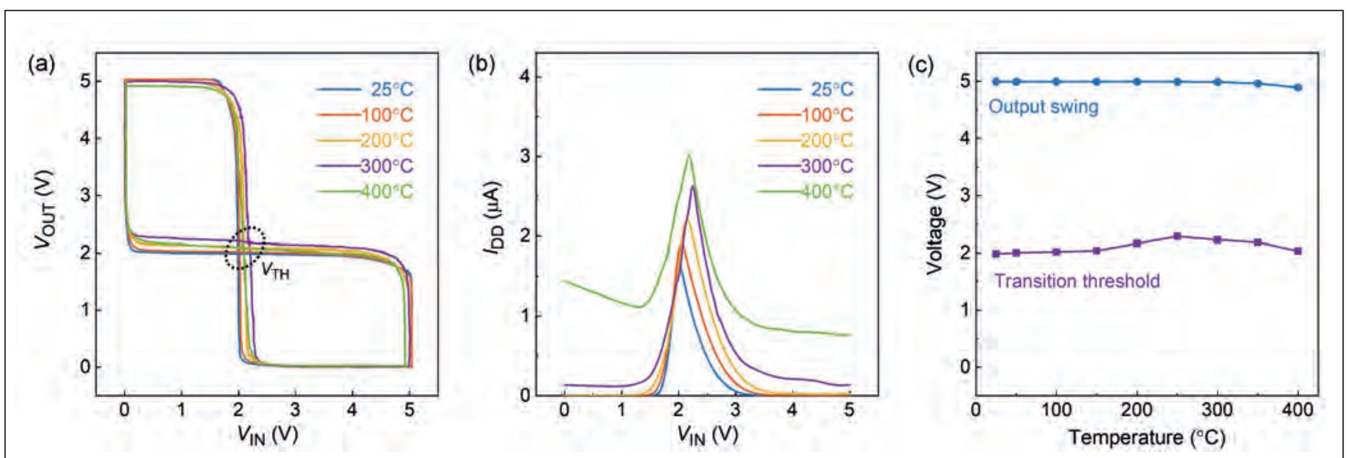


➤ Figure 9. The unoptimized gate stack results in pronounced hysteresis loops in dual-sweep transfer curves. Such an instability in the threshold voltage (V_{TH}) is very likely induced by the problematic dielectric/ *p*-GaN interface. Utilizing the buried-channel structure of this *p*-FET, the team at HKUST replaced Al_2O_3 with SiN_x, which exhibits no hole barrier to GaN, and found that the V_{TH} shift induced by highly negative V_{GS} has been effectively suppressed. The V_{TH} shift induced by a small V_{GS} is eventually suppressed by converting the OPT-treated *p*-GaN surface to GaON, which eliminates high-density interface traps.

Toward real applications

Based on constraints associated with material properties and fabrication, we believe that GaN CMOS will deliver a promising performance when used for power integration. To facilitate an actual application, in addition to the need for substantial downscaling and process optimization that would boost up the current density of *p*-FETs, there is another critical issue: examining and improving stability at the device and circuit levels. On this mature platform it will come as no surprise that the stability and reliability of the *n*-FET has been substantially studied and enhanced. So what's needed is to focus on the *p*-FET.

One option for mitigating the strong scattering within the *p*-FET is to use oxygen plasma treatment to separate the conducting channel from the troublesome etched interface. However, the downside is a sub-standard quality for the etched interface. Due to this weakness, when a large gate bias is applied, holes traversing the device get trapped at the interface, leading to a variation in the threshold voltage.



➤ Figure 10. With the stability of *p*-FETs greatly enhanced, the GaN CMOS logic inverter exhibits remarkable thermal stability up to 400 °C. The transition threshold only varies slightly, whereas the rail-to-rail output is well preserved until the temperature reaches 400 °C to induce notable leakage. These results show that GaN CMOS is very promising for use in harsh environments.

We tackle this problem with a two-step strategy. Our first move is to replace the Al_2O_3 gate dielectric with SiN_x. As the latter aligns with GaN in a type-II manner, it presents no barrier to holes in GaN. According to the disorder-induced-gap-states model, which can generally describe the interface between GaN and oxides, there is an appreciable trap density near the band edge of the former structure. Our switch to SiN_x introduces a hole evacuator, automatically nullifying the high-density hole traps near the valence band edge. The upshot is the prevention of successive shifts in threshold voltage at highly negative gate biases (see Figure 9 (a) and (b)).

However, this in itself is not a great solution, as there is still notable hysteresis, attributed to deeper trap states that align with the bandgap of SiN_x and are thus not easy to evacuate. To tackle this issue, we take a second step in gate stack engineering, converting the region that we have treated with an oxygen plasma into crystalline nano-phase, gallium oxynitride (GaON).

Previously, we used GaON to improve the gate reliability of a *p*-GaN gate HEMT. Through that effort, we learnt that GaON possesses a much better thermodynamic stability and a higher material quality than GaN subjected to an oxygen plasma treatment. Introducing GaON has had a profound effect, completely eliminating hysteresis (see Figure 9 (c)).

Our staggered gate stack differs from the conventional metal-insulator-semiconductor stack. In our case, the dielectric does not provide a barrier for blocking carriers when the device is in its on-state. Due to this, we need to include a buried-channel structure.

When operating in the on-state, the holes in the channel are confined by the built-in potential in *p*-GaN, enabling the gate leakage to remain at a very low level if the gate bias does not exceed -6 V. Yet, the SiN_x is indispensable. It effectively blocks the gate leakage at the off-state under a positive gate bias; and it serves as a voltage divider, expanding the allowed input swing to fit the *p*-GaN gate HEMT platform, where typically 5-6 V are usually used to drive *n*-FETs.

By turning to our SiN_x/GaON gate structure, we are able to extend the operating temperature of GaN CMOS ICs to 400 °C (see Figure 10). With a 5 V voltage supply, the logic transition threshold fluctuates within only 0.4 V.

At this supply voltage, the rail-to-rail output swing is well maintained, degrading only slightly at 400 °C, due to an increase in leakage that could be further suppressed with process optimization. These results underscore the superiority of GaN as a wide-bandgap semiconductor, indicating possible applications of GaN in extreme environments.

We have made major strides with GaN CMOS, demonstrating the first family of ICs and also projecting performance in power integration and substantially improving stability. Our next steps, hopefully taken in collaboration with industry partners, are to undertake device downscaling, silicon-compatible process development and yield/uniformity improvement. There is no doubt that GaN CMOS is marching toward practical applications.

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Prototype 4-inch RF GaN-on-GaN wafer)

GaN RF HEMTs:
Powering ahead with native substrates

GaN-on-GaN high-power amplifiers with through-substrate vias are delivering record-breaking power-added efficiencies and continuous-wave operation

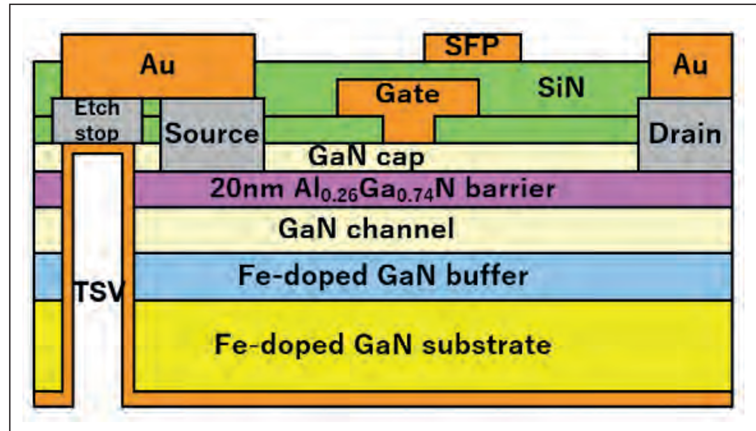
BY NAOYA OKAMOTO AND YUSUKE KUMAZAKI FROM FUJITSU LIMITED

ELECTRONIC DEVICES make our lives richer and more convenient. They are now taking us towards an advanced society, formed through the fusion of cyberspace and physical space. On entering this era, we will benefit from vast numbers of sensors in physical space collecting big data, quantitatively analysed by artificial intelligence in cyberspace. New value will be created from this, including the provision of high-quality services. Underpinning this new world order will be an increase in the use of radio waves above the microwave band to sense and collect data, alongside networks that exchange huge amounts of data, as well as sectors within industry that manufacture substances that bring new value. Supporting this introduction of a higher sensing resolution and a roll-out of a higher network capacity will be an increase in the frequency of solid-state power amplifiers deployed in radio equipment. A shift from microwaves to millimetre waves is already underway, and migration to the terahertz domain will follow.

Moving to higher frequencies is not trivial. Challenges are not limited to simply ensuring that devices can operate at higher speeds – there is also the issue of a reduction in the power conversion efficiency of solid-state power amplifiers at higher frequencies, leading to greater power consumption. This is at odds with a sustainable society, as to curb the carbon footprint of the communication sector, the power consumption of radio equipment must fall as the number of units increases. The most efficient, powerful solid-state power amplifiers are based on GaN HEMTs. These RF transistors are typically fabricated on non-native substrates, such as SiC or silicon. However, the power and the efficiency of these devices are held back by electron traps that form in the GaN epilayers – mainly the buffer layer – and lead to current collapse.

Our team from Fujitsu, Japan, is tackling this issue head-on by switching the substrate to free-standing GaN. It is a solution we have been working on for many years. About ten years ago, when characterising the metal-insulator-semiconductor interface and the Schottky junction of GaN-based epitaxial layers grown on GaN substrates, we observed excellent crystal quality in this GaN-on-GaN heterostructure. But at this time only *n*-type, rectangular GaN substrates that were small in size were available. This restricted our development to the basic research phase.

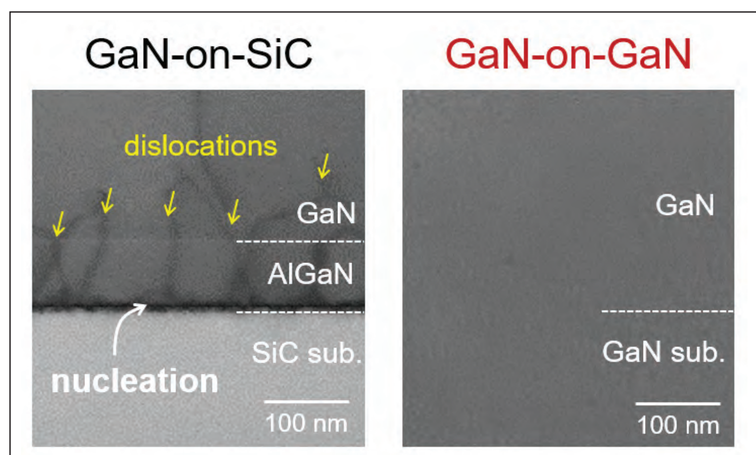
Around 2017, when the availability of semi-insulating 2-inch GaN substrates began, we embarked on full-fledged work on RF GaN-on-GaN HEMTs. Initially, we directed our efforts at developing RF GaN-on-GaN HEMT power amplifiers for microwave heating. This project, supported by the Japan Ministry of the Environment, required transistors to run under severe conditions of high-power, continuous-wave operation. Realising success on these fronts would create a device that could serve in other applications, such as radar and wireless communication. However, progress would not be easy, due to the lower thermal conductivity of the GaN substrate compared with that made from SiC. Recently, we have shown that this concern can be overcome by: increasing the power-added efficiency, through improvements to the GaN substrate/epilayer interface; and developing GaN through-substrate vias that reduce the source inductance (see Figure 1).



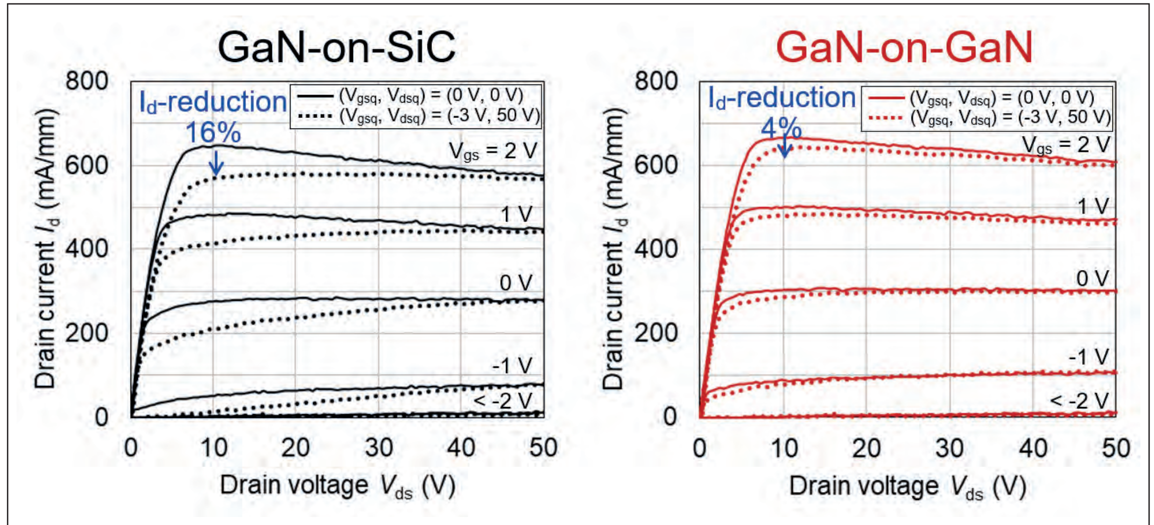
➤ Figure 1. Fujitsu is a pioneer of the RF GaN-on-GaN HEMT power amplifier.

Targeting record-breaking efficiencies

As more efficient devices minimise self-heating, we decided to aim for a record-breaking power-added efficiency. Young researchers within our team spearheaded in this effort, leading the development of front-side devices for RF GaN-on-GaN. This project kicked off by comparing the quality of GaN epitaxial crystals grown on a conventional SiC substrate and on a GaN substrate (see Figure 2). Scrutinising these materials revealed a dislocation density in the GaN grown on SiC of 2×10^8 cm^{-2}, compared with less than 10^6 cm^{-2} for GaN grown on a native substrate. In addition, HEMTs were fabricated from these epiwafers to obtain basic device characteristics. Results confirmed that GaN-on-GaN transistors have diminished current collapse compared with their GaN-on-SiC counterparts, due to superior crystal quality (see Figure 3). However,



➤ Figure 2. Transmission electron microscopy underscores the superior material quality of GaN-on-GaN compared with GaN-on-SiC.



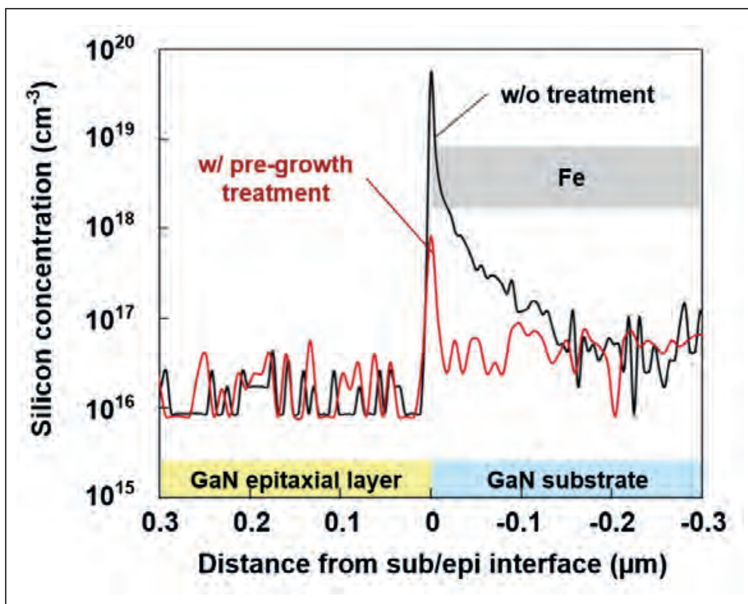
➤ Figure 3. Pulsed current-voltage characteristics show that GaN-on-GaN RF HEMTs suffer from less current collapse than those based on GaN-on-SiC.

measurements of the power output at high frequencies were disappointing, with the power-added efficiency for GaN-on-GaN HEMTs buried within conventional GaN-on-SiC data.

How can it be that despite a far better crystal quality, the power produced by this native device is no better than that for a GaN-on-SiC HEMT?

Investigations eventually revealed a conductive layer at the GaN substrate/epitaxial interface, stemming from silicon contamination. The level of silicon is not insignificant, having a concentration more than an order of magnitude higher than that of the iron concentration within the GaN substrate (see Figure 4). Note that a quarter of a century ago, a similar problem plagued GaAs substrates. Their surfaces can be riddled with the likes of silicon, carbon and oxygen, impurities activated by improvement of crystal quality through homoepitaxy. The young researchers in our team were unaware of this issue, as it had not been a problem when growing GaN epilayers, due to the use of non-native substrates. To address this issue, we turned to wet processing the substrate surface prior to epitaxial growth (see Figure 4). This approach reduced the silicon concentration to below that for iron, leading to suppression of the high-frequency leakage path. Thanks to this, we could realise a record-breaking power-added efficiency of more than 80 percent in the 2.45 GHz ISM-band (see Figure 5).

➤ Figure 4. Secondary ion mass spectrometry (SIMS) showed that pre-treatment of the GaN substrate can prevent high levels of silicon contamination.



The virtue of vias

Another important technique for improving the performance of power amplifiers based on the RF GaN-on-GaN HEMT is to add GaN through-substrate vias, as this reduces the source inductance. Taking this approach is not a novel – it is already applied to commercially available GaN-on-SiC devices. We have been working on this for some time, having started to develop through-substrate vias for GaN when we began device development.

Our efforts began by investigating GaN etching. Employing inductively coupled plasma etching, using a mix of chlorine and boron trichloride gases, we targeted an etching rate of at least 1 μm/min and an etching selection ratio of 30 or more, using a nickel metal mask. While success came relatively quickly, we still had challenges associated with the formation of pillars (see Figure 6).

Previous experience associated with SiC via hole etching had taught us that inclusions contained in the SiC substrate could impact pillar formation. To see if this issue remained with GaN, we scrutinised the bottom surface of these substrates with a scanning electron microscope. However, we failed to find any inclusions on GaN substrates grown by HVPE with void-assisted separation. Note that this might not be the case with GaN substrates grown by other methods, such as ammonothermal and sodium-flux – we simply don't know. We then focused on the wafer surface temperature during etching. Using almost identical plasma power conditions, we found that etching SiC involved a wafer surface temperature of 200 °C or more. In comparison, for GaN the temperature could be as

low as 90 °C, making the etching by-product difficult to remove. To address this concern by promoting the desorption of the etching by-product, we increased the wafer surface temperature by dialling back the cooling helium pressure. This action immediately solved the pillar problem (see Figure 6). With optimized etching conditions, we could successfully form a GaN via hole with a depth of 91 µm, using a GaN etching rate of 1.5 µm/min and a selectivity to the nickel metal mask of 35.

However, another issue emerged: etching selectivity fell to one-third of that for conventional SiC etching, falling from a value of around 100 to about 35. The reduced selectivity impacted the thickness and the process for the front-side etch stop. Compounding matters, the remaining metal mask for via etching interfered with the stealth dicing of the GaN substrate. To overcome these problems, we refined our process for forming vias in GaN (see Figure 7).

Upping the power

Thanks to this progress, we were now in a position to draw on all our development and integrate our technologies. Due to the lower thermal conductivity of GaN than SiC, we had concerns relating to heat radiation characteristics. Encouragingly, we could realise heat dissipation characteristics comparable to those for GaN-on-SiC by drawing on thermal simulation and introducing backside processing (see *Compound Semiconductor* **25** Issue 7, October, 2019, p32). But we were still to demonstrate GaN-on-GaN high-power amplifiers with output powers greater than 50 W.

Now this value has been exceeded with a GaN-on-GaN high-power amplifier featuring a through-substrate via, 36 gate fingers, a gate length of 0.5 µm, a unit gate width (W_{gu}) of 300 µm, a gate-to-gate spacing (L_{gg}) of 30 µm, and a total gate periphery of 10.8 mm. This chip has a W_{gu}/L_{gg} aspect ratio of 10, creating a very severe condition for heat dissipation. After mounting our chip on an evaluation board, we carried out large-signal measurements that produced an excellent set of results (see Figure 8). Driven in pulsed mode, using 10 µs pulses and a 1 percent duty cycle, our amplifier delivered a maximum output power of 64.3 W and a peak power-added efficiency

of 71.1 percent at 2.6 GHz. Running in continuous-wave mode produced a slight reduction in performance, due to self-heating, with values of maximum output power and power-added efficiency falling to 54.6 W and 63.3 percent. According to the simulated transient response, we think that the difference in channel temperature between continuous-wave and pulsed operation can be as high as 100 °C. However, the realisation of continuous-wave operation indicates that our GaN-on-GaN HEMT power amplifier has suitable heat dissipation characteristics, and eliminates concerns regarding this particular technology.

Looking ahead

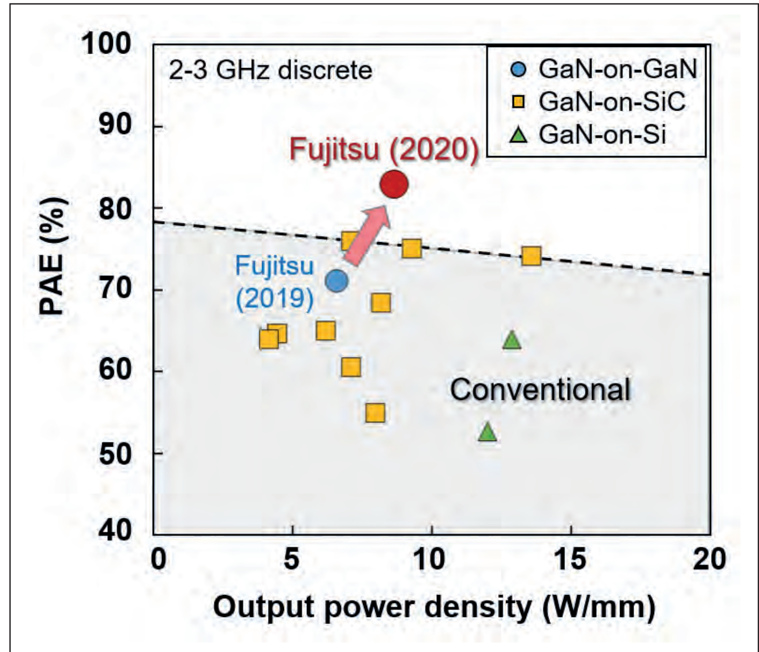


Figure 5. Supressing silicon contamination leads to a hike in the power-added efficiency of discrete GaN HEMTs operating at 2-3 GHz.

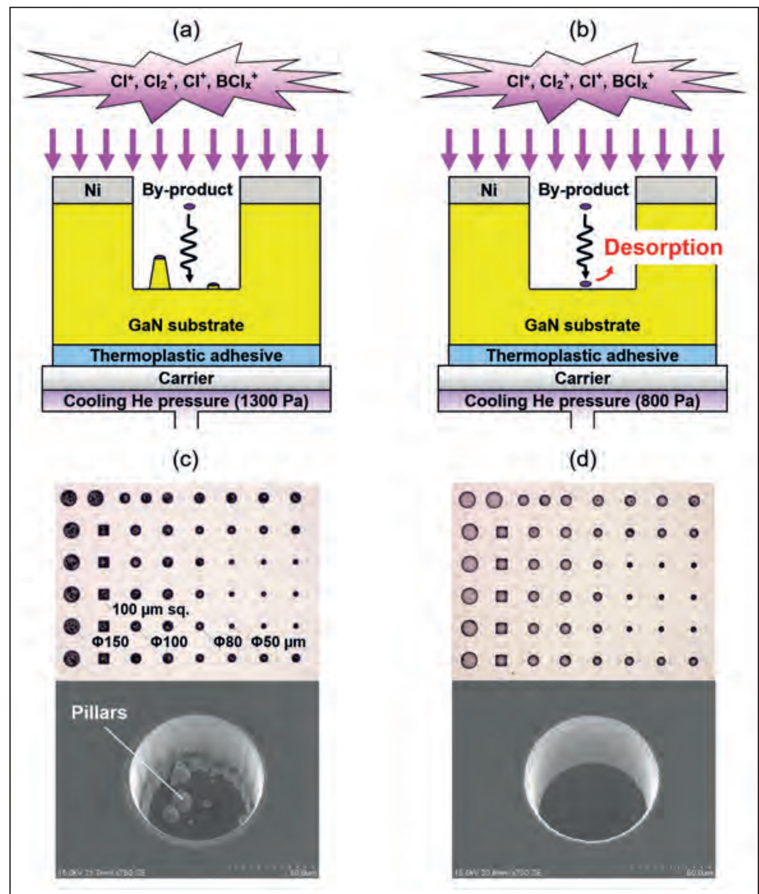


Figure 6. Optical microscopy and scanning electron microscopy images (c) and (d) show that switching from conventional conditions (a) to optimum conditions (b) improves the etching of by-products.

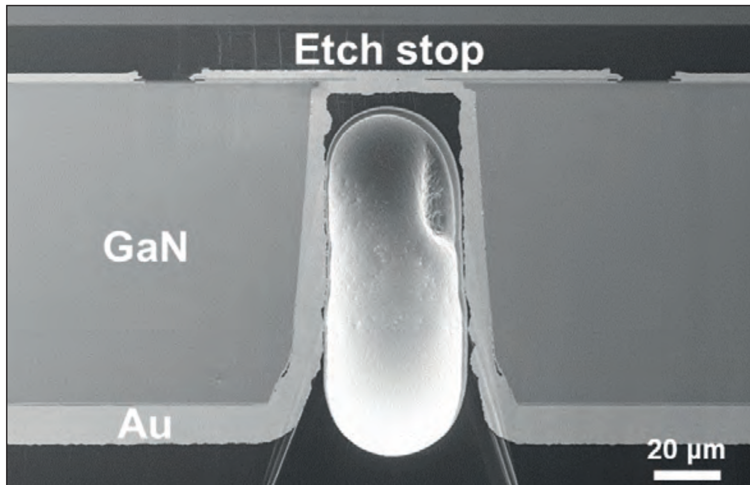


Figure 7. A cross-sectional scanning electron microscopy image of a GaN through-substrate via of a GaN-on-GaN HEMT.

Two of the biggest issues facing RF GaN-on-GaN HEMTs are the cost of these devices and the size of the substrate. Progress is being made with the latter: a 4-inch iron-doped GaN substrate has already been commercialized, and a 6-inch GaN substrate will soon be realized. Even so, prices are still quite high, and need to fall to at least the same level as SiC to enable the commercial launch of RF GaN-on-GaN HEMTs. Ensuring that this happens requires not only the efforts of substrate manufacturers, but also demand for power and optical devices, as well as RF devices.

It is also anticipated that problems will arise in device manufacturing, along with the enlargement of the diameter. Our team is playing its part in addressing these important issues by starting to fabricate 4-inch RF GaN-on-GaN epiwafers. While the efficiency of the GaN devices decreases with increasing frequency, we expect that this decline can be suppressed with high-quality crystalline material. Devices featuring such epilayers are tipped to ensure ultra-high data rates for beyond 5G and 6G, realised by using GaN-on-GaN with ultrafine gates.

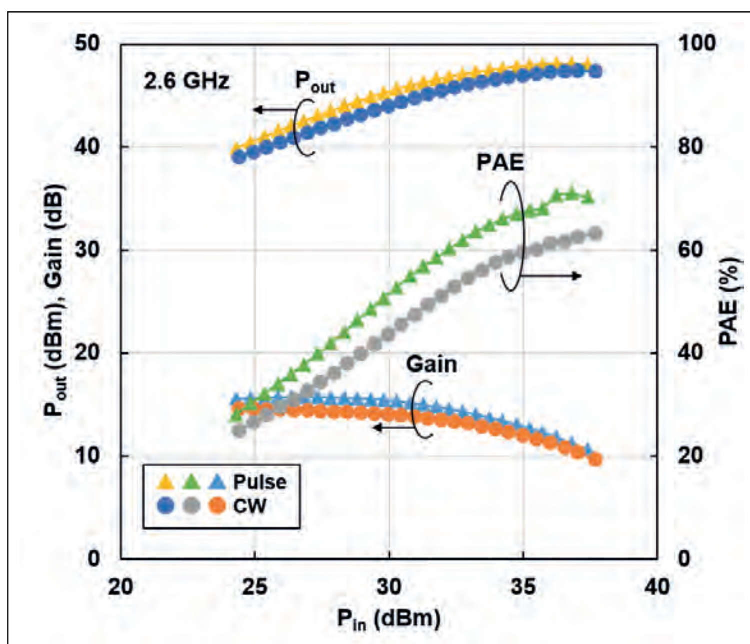


Figure 8. Power characteristics of a GaN-on-GaN HEMT power amplifier in pulsed (closed triangles) and continuous-wave (closed circles) operation.

Another opportunity for improving device performance is to introduce architectures that combine the high crystal quality of GaN-on-GaN with materials with great thermal conductivity. Options for high-performing heat spreaders include diamond. However, its addition would need to be cost-competitive, just like the introduction of GaN substrates.

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