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Virtualisation: a key enabler of the future power grid

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IT'STIME TO COMMERCIALISE THE GaN IC

Power ICs combine several power functions in a GaN chip are set to play a major role in worldwide electrification

THERE IS STILL LIFE IN THE SILICON IGBT

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THRESHOLD VOLTAGE IN SiC MOSFETS

System designers can now benefit from new test and stress procedures for SiC MOSFETs

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VIEWPOINT

By Christine Evans-Pughe, Acting Editor

There's more to power electronics than new materials

WIDE bandgap power semiconductor devices based on silicon carbide (SiC) and Gallium Nitride (GaN) are evolving fast and playing a greater role in many applications. But there is far more to power electronics than new materials.

At the device level, architecture matters. And of course, there's the wider impact of big global trends such as the growth in renewable energy generation.

In this edition of Power Electronics World, we look at the latest development in power GaN and new test procedures for SiC; we revisit the silicon IGBT; and discover how architectures can revolutionise power devices. As power grids shift from one-directional power flow to integrating renewable energy resources, we also explore the benefits of virtualisation.

In March, Tesla announced that it will use 75 percent less SiC in a new EV powertrain, sending a shockwave through an industry investing $billions in SiC fabs. But as our news analysis explains, there is plenty of life left in silicon IGBTs.

SiC is the long-term future. As well as new fabs coming on stream, other developments are continuing apace including, as Infineon outlines in its article, new test and stress procedures for SiC MOSFETs.

We have several interesting GaN articles. Innoscience looks at how bidirectional GaN switches are disrupting power management, while Wise Integration details how highly integrated GaN chips are set to play a greater role in power electronics. Jim Witham, CEO of GaN Systems, explains why surging sales EVs, data centres and industrial motors, have brought GaN devices to a key inflection point.

Back in the lab, researchers at Stanford University describe how a multi-faceted endeavour, starting

with material growth and extending all the way to circuit-level investigation, can ensure uniform, robust avalanche in GaN vertical power diodes.

Of course, new materials are only part of the story of innovation. Yuhao Zhang from Virginia Tech reminds us that architectures matter, with the likes of superjunctions, multiple channels and multiple gates offering the opportunity to revolutionise power devices.

And finally, there's the big picture. Power grids must evolve to integrate renewable energy resources. In a fascinating overview, ABB explains how virtualisation of protection and control forms a key part of this journey, offering new possibilities to optimise the supply of renewable generation and achieve flexibility and scale.

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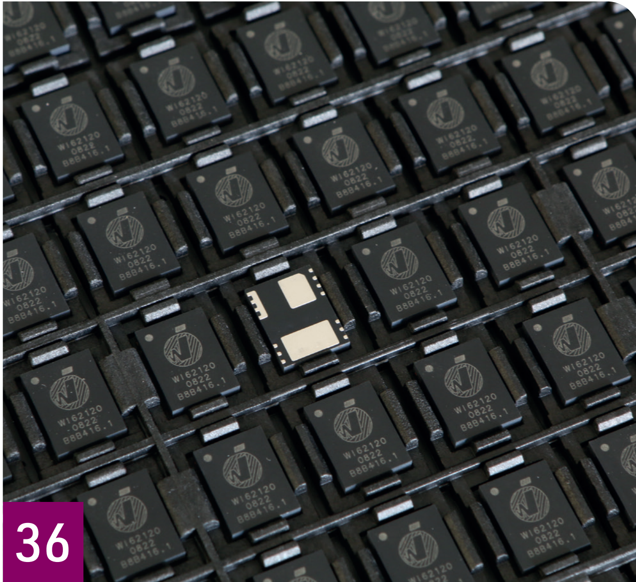
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EU PowerizeD project aims to transform power electronics

Multi million euro European research initiative will involve 39 companies and 23 research institutions

A NEW RESEARCH initiative called PowerizeD, involving 39 companies and 23 research institutions, aims to transform power electronics in Europe.

Coordinated by Infineon Technologies AG, PowerizeD aims to increase the degree of mechanical and electrical integration of control, driver and switching functionalities in components and to advance the integrated optimisation of all power switch functions, independent of the semiconductor material used.

New switching topologies and advanced control strategies involving the application of Artificial Intelligence are expected to improve efficient, robust and reliable operations even further.

The immediate project objectives include: reduction of power loss in power conversion by 25 percent; extension of the service lives of devices and systems by 30 percent;; reduction of chip size by at least 10 percent; and shortening development times by a challenging 50 percent.

The project partners are focusing on applications from the fields energy and mobility. 17 demonstrator paths are concerned among other things with improvement of drives for the rail industry, charging systems for the automotive industry, liquid batteries for the energy industry as well as drives for the manufacturing industries. The research partners will take an interdisciplinary approach with topics including modeling and Digital Twin, Federated Learning as well as reliability and sustainability.

"We have to make highly efficient use of energy if we are to achieve net-zero climate protection goals. Digitalisation can help here as a highly decisive lever for more energy efficiency," says Constanze Hufenbecher, Infineon chief digital transformation officer.

"Power electronics is key to the energy transformation and is used anywhere and everywhere that electricity is generated, transferred and used efficiently," says Dr. Rutger Wijburg, COO at Infineon. "The broad spectrum of power electronics applications makes it very important that we collaborate with partners across the boundaries of corporate entities and organisations to jointly advance Europe as innovation engine."

The European Union is funding PowerizeD with approximately €18 million as part of the joint program for digital key technologies (Key Digital Technologies Joint Undertaking, KDT JU) in its Digital Agenda. The amount will be matched by funding from the national governments of the respective countries involved.

The subsidies from Germany are being provided by the German Federal Ministry of Education and Research. A summary of all the project partners and supporting organisations is available on the project web site. The project will have a three-year duration and is expected to end in December 2025.

The broad spectrum of power electronics applications makes it very important that we collaborate with partners across the boundaries of corporate entities and organisations to jointly advance Europe as innovation engine

Gridspertise and ST extend 20-year collaboration

Companies to add features to smart-meter customers in the US and other geographies

GRIDSPERTISE and STMicroelectronics (ST) have entered a new phase in their 20 year smart-meter collaboration.

Over 65 million Gridspertise smart meters deployed in Spain, Eastern Europe, and Latin America already use ST's power-line communication (PLC) technologies. And ST's latest PLC system-on-chip has been integrated in Gridspertise smart meters for Italy to enable a near real-time cyber-secure communication channel for in-home devices; the so-called Chain 2 technology.

Now, Gridspertise and ST are working together to extend Chain 2 to new metering solutions in the Gridspertise portfolio, making it suitable for the US and other geographies.

Chain 2 technology aims to improve customer awareness of the energy consumed and self-produced. For example, it enables the smart meter to collect real-time data on home appliances' consumption, that can be used, for example, to modulate the charging power of an EV charger according to the available capacity and other demands for power in the house.

Gridspertise and ST are collaborating in other areas too. Beyond working on ANSI C communication standard for the US market, the companies are cooperating for the adoption of the latest DLMS-certified standards into Gridspertise smart meters, to further enhance interoperability and interchangeability between devices and systems.

"Working together with other key industry leaders is fundamental to accelerating grid digitalisation and to promoting an active role for end users in the energy transition," said Gianni Ceneri, CTO. "We are pleased to strengthen our strategic collaboration with STMicroelectronics leveraging shared best practices for the development of innovative solutions to serve an ever-increasing number of markets and bring benefits to new customers, starting from the US where Gridspertise is enhancing its activities through its North American platform to better support power grid operators and utilities in the region."

"As Gridspertise accelerates the growth of its business, ST continues to develop and contribute our unique system know-how, dedicated support, and ready-to-use solutions based on our advanced semiconductor integration capabilities," added Domenico Arrigo, general manager of STMicroelectronics's Industrial and Power Conversion Division in the Analog, MEMS & Sensors Group.

"We are maintaining and enhancing our connection as a key technology provider for Gridspertise solutions and services, and with them delivering smart and sustainable grids that are robust, secure, resilient, and reliable."

Beyond working on ANSI C communication standard for the US market, the companies are cooperating for the adoption of the latest DLMS-certified standards into Gridspertise smart meters, to further enhance interoperability and interchangeability between devices and systems

Infineon QDPAK and DDPAK registered as JEDEC standard

New top-side cooling packages for high-voltage MOSFETs registered as JEDEC standard for high-power applications

INFINEON TECHNOLOGIES has successfully registered its QDPAK and DDPAK top-side cooling (TSC) packages for high-voltage MOSFETs as a JEDEC standard. This registration further solidifies Infineon's goal to help establish a broad adoption of TSC in new designs with one standard package design and footprint.

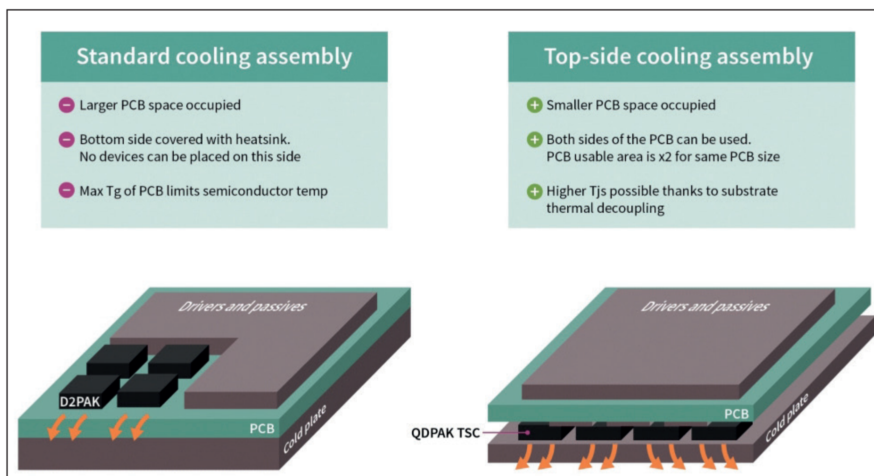
"As a solutions provider, Infineon continues to influence the semiconductor industry through innovative packaging technologies and manufacturing processes," said Ralf Otremba, lead principal engineer for High Voltage Packaging, Infineon.

"Our advanced top-side cooled packages bring significant advantages to the device and system levels to fulfill the challenging demands of cutting-edge high-power designs. Package outline standardisation will help ease one of the main design concerns of OEMs for high-voltage applications by securing pin-to-pin compatibility across vendors."

JEDEC has been widely accepting semiconductor packages such as the TO220 and TO247 through-hole devices (THD) – devices that have been prominently used over the past decades and are still an option in new onboard charger (OBC) designs, high voltage (HV) and low voltage (LV) DC-DC converters.

The registration of QDPAK and DDPAK surface-mounted (SMD) TSC package designs signals a new era for package outlines, says Infineon, ushering a wide market adoption of the TSC technology as a replacement for TO247 and TO220, respectively. With the benefits of this technology, this new JEDEC package family registration, according to the MO-354 standard, serves as a key enabler for the transition of high-voltage industrial and automotive applications to top-side cooled designs in next-generation platforms.

To facilitate design transition for customers from the TO220 and TO247 THD devices, Infineon has designed QDPAK and DDPAK SMD devices to deliver equivalent thermal capabilities with improved electrical performance. Based on a standard height of 2.3 mm for QDPAK and DDPAK SMD TSC package for HV and LV devices, developers are now able to design complete applications such as OBC and DC-DC conversion with all SMD TSC devices measuring the same height. Compared to existing solutions



Additionally, TSC packaging offers up to 35 percent lower thermal resistance than standard bottom-side cooling (BSC)

that require a 3D cooling system, this facilitates designs and reduces system cost for cooling.

Additionally, TSC packaging offers up to 35 percent lower thermal resistance than standard bottom-side cooling (BSC). By enabling the use of both PCB sides, TSC packages offer better board space utilisation and at least two times more power density.

The thermal management of the packages is also improved by thermal decoupling from the substrate since the thermal resistance of the leads is much higher compared to the exposed package top side.

Because of the improved thermal performance, stacking different boards is not necessary. Rather than combining both FR4 and IMS, a single FR4 is enough for all components and also requires fewer connectors. These features deliver an overall bill of materials (BOM), which ultimately reduces overall system cost.

TSC technology is also said to offer an optimised power loop design for increased reliability. This is possible by the placement of the drivers, which can be placed very close to the power switch. The low stray inductance of the driver switch loop, reduces the loop parasitics and leads to less ringing on the gate, higher performance and a smaller risk of failures.

US DOE announces $48 million grid project

ULTRAFAST project will advance performance limits of silicon, wide bandgap, and ultra-wide bandgap semiconductors to improve their actuation methods

THE US Department of Energy (DOE) has announced $48 million in funding to support a new program focused on developing power grid technologies that improve control and protection of the US domestic power grid.

The goal of ULTRAFAST (Unlocking Lasting Transformative Resiliency Advances by Faster Actuation of Power Semiconductor technologies) is to advance the performance limits of silicon, wide bandgap (WBG), and ultra-wide bandgap (UWBG) semiconductor devices that will enable faster switching and/or triggering at higher current and voltage levels for improved control and protection of the grid.

Unforeseen power grid outages are estimated to cost the US economy $150 billion annually. The DOE says that modernising the US grid infrastructure with improved efficiency and resilience against extreme weather events is critical to ensuring that clean energy and transportation options can reach communities across the country. Grid modernisation will also support President Biden's goals to accelerate the deployment of renewables, boost the nation's energy independence, and achieve 100 percent clean electricity by 2035.

ULTRAFAST will fund projects that aim to enable utilities to more effectively control grid power flow to avoid disturbances, and quickly isolate and route around disruptions.

Managed by DOE's Advanced Research Projects Agency-Energy (ARPA-E), the ULTRAFAST's categories include:

- Device and/or module technologies targeting protection functions at high current and voltage levels by achieving very fast by-pass, shunt, or interrupt capability at as low level of integration as possible with nanosecond-level reaction time (and corresponding slew rates).
- High switching frequency devices and/or modules which enable efficient, high-power, high-speed power electronics converters.
- Complementary technologies such as wireless sensing of voltage and current, high-density packaging with the integrated wireless actuators and device/module-level protection, power cell-level capacitors and inductors, and thermal management strategies to support (1) and (2).

ARPA-E first held a workshop on this topic last year. Workshop participants provided expert inputs on the technical aspects of ultra-fast-triggered semiconductors, and how such devices can aid US national goals to develop future high-performance resilient power systems.

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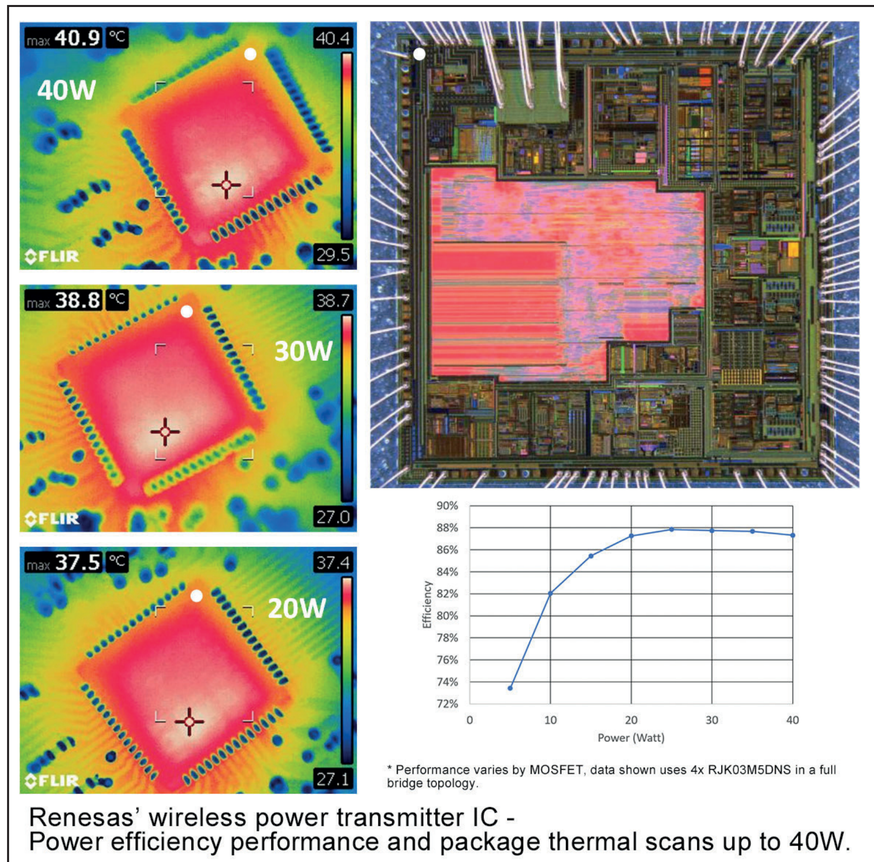
Renesas presents wireless power transmitter update

New wireless device charging technology improves efficiency, measurement accuracy and user safety

RENESAS ELECTRONICS presented advancements in its charging technology at the International Solid-State Circuits Conference (ISSCC) in San Francisco, February 19-23. During the conference, Renesas described its single-chip wireless power transmitter solution that measures AC and DC transmitter power for improved accuracy and safety.

The presentation also included details of a transmitter technology with adaptive Zero-Voltage Switching (ZVS) that achieves reduced electromagnetic interference (EMI) and higher power transmission efficiency. These technical capabilities enable wireless power transmission up to 15W with a Qi power receiver (PRx) and up to 40W with proprietary PRx solutions.



Renesas' wireless power transmitter IC - Power efficiency performance and package thermal scans up to 40W.

DC and AC Coil Current Sensing and Foreign Object Detection

Renesas is the first in the industry to develop single-chip transmitter (Tx) technology that can directly measure both DC and AC power transmission components. With this approach, transmitted power can be measured more accurately, providing a means to accurately detect a mismatch between the power transmitter (PTx) and the PRx power levels.

Furthermore, DC and AC coil current sensing can detect if a small metal foreign object, such as a paper clip, is caught between the transmitter and receiver, which otherwise could cause the object to heat up and compromise safety.

The transmitter is equipped with analogue AC coil current sensors and supports up to four transmitter coils to increase the charging area, improving the end user's charging experience.

Adaptive Zero-Voltage Switching and Low EMI

One of the key innovations to be described at the ISSCC presentation is adaptive ZVS, which ensures that the power MOSFETs switch after their drain-source voltage has dropped to 0V, reducing switching losses and increasing efficiency. Since this adaptive ZVS technology operates over wide load conditions, it is ideal for half-bridge inverters powering varying loads. Moreover, this ZVS technology reduces EMI by lowering the amount of energy that is converted into electromagnetic noise.

When compared to the conventional methods, using ZVS decreases EMI by 4 decibel (dB) and can increase the PTx efficiency by 1.7 percent or more. ZVS also helps extend the operational life of power systems in many applications such as automotive in-cabin chargers by auto-calibrating the initial threshold of the comparator.Additionally, the system has a highly programmable Pulse Width Modulation (PWM) generator, which controls the transmitter power delivery characteristics to ensure that the device being charged receives the right amount of power. This improves the accuracy and stability of the charging process and provides more control over the delivered power.

"With the integration of these innovative technologies, new wireless charging systems are expected to change the way portable devices are charged," said Filippo Neri, senior manager of Electrical Engineering for Renesas' Mobility Infrastructure and Industrial Power Division, who co-authored the paper."

Mitsubishi acquires Swedish DC circuit breaker firm

Scibreak and Mitsubishi to work together on DCCB tech for HVDC systems

MITSUBISHI ELECTRIC has entered into a share transfer agreement on February 16 to wholly acquire Scibreak AB, a Swedish-based company that develops direct current circuit breakers (DCCBs).

The two firms aim to work closely together on developing DCCB technologies for high- voltage direct current (HVDC) systems to support the increasing global deployment of renewable energy.

The introduction of renewable energy generation, such as wind power, is increasing worldwide to achieve carbon neutrality. Particularly in offshore wind power generation, HVDC is used for long-distance transmission between offshore and onshore load centres, as it offers lower power losses and cost when compared to AC transmission. In the future, multi-terminal HVDC networks are expected to develop, particularly for offshore wind power generation in Europe, allowing for efficient cross-border energy transmission. These networks will require DCCBs, which will play a critical role in protecting the power system.

HVDC breakers will require very fast operation times, in the order of a few milliseconds, and companies are stepping up technological development in response to the need for more compact, high-performance, and cost effective DCCBs.

Scibreak has market leading DCCB technology, in terms of operation time and footprint. Through the acquisition of shares, Mitsubishi Electric says it will utilise Scibreak's technology and know-how to lead the market commercialisation of DCCBs, strengthening its global HVDC system business and contributing to the realisation of carbon neutrality through the further spread of renewable energy.

Pictured are Mitsubishi Electric Executive Officer Noriyuki Takazawa (left) and Scibreak CEO Tomas Modeer)

VisIC paves way to high-power GaN traction inverters

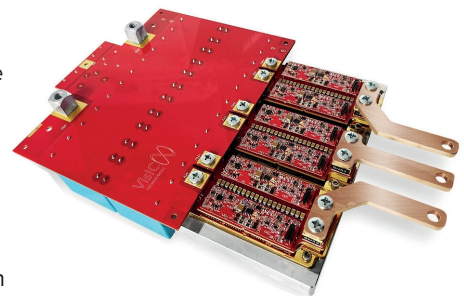
VisIC TECHNOLOGIES has successfully tested its 2.2mΩ 650V half-bridge power module, consisting of four parallel 8mΩ Power FET, in a 3-phase configuration on a dyno-test-bench using a PMSM motor at a major automotive OEM.

The company say this proves its D^3GaN (Direct Drive D-Mode GaN) technology is well-suited even for the most challenging high-power automotive applications. Concerns about parallelisation and oscillations caused by fast-switching transients have been addressed. The inverter phase current reached 350Arms (500A peak) at 400V, although test system set-up limitations prevented higher currents, which the 2.2mΩ Power Module is capable of.

Worldwide Harmonised Light Vehicles Test Procedure (WLTP) driving cycle testing was executed and achieved comparable efficiency with commercial Silicon Carbide-based modules, despite using early non-optimised module prototypes. VisIC says this means that D^3GaN will deliver its promise of the highest efficiency, improving car costs through lighter, smaller power systems and a smaller battery size, without compromising the car's driving range. In addition, the D^3GaN technology, based on GaN-on-Silicon semiconductor process, is delivering better than SiC performance at the more competitive Silicon cost level.

"With this great accomplishment, acknowledged by a leading automotive OEM, VisIC Technologies has provided overwhelming evidence for higher-efficiency at lower-cost future EV traction inverters, for the automotive world," said Tamara Baksht, CEO & co-founder of VisIC technologies. "The automotive market demands high-power, high-voltage, high-reliability GaN, and our D^3GaN die and module solutions are the answer."

VisIC Technologies 3-phase prototype inverter system will be available for testing across additional customer sites towards the end of the 2nd quarter of 2023.



Microchip invests to expand SiC capacity

Ramping production in Colorado Springs fab will enable Microchip to respond to growing semiconductor demand

Microchip Technology has announced plans to invest $880M to expand its SiC and silicon production capacity at its Colorado Springs manufacturing facility over the next several years. Microchip was also approved for state and local incentives of approximately $47M for the expansion.

One significant phase of the expansion is to develop and upgrade its 50-acre, 580,000-square-foot Colorado Springs campus for increased SiC manufacturing for use in automotive/E-Mobility, grid infrastructure, green energy, and aerospace and defence applications.

The campus currently employs more than 850 people and produces products from 6-inch wafers. The manufacturing technology that Microchip is installing will run on 8-inch wafers, which will significantly increase the number of chips produced at this location. The additional 400 jobs anticipated at the facility will range from production specialists to technical roles in equipment procurement and management, process control and test engineering.

"With over two-decades of investment in SiC, Microchip's portfolio is designed to provide our customers with innovative power solutions," said Rich Simoncic, senior vice president of Microchip's Analog businesses. "This campus is an integral part of producing our SiC technology to assure our customers with supply certainty as they transition to SiC solutions."

President and CEO of Microchip Technology Ganesh Moorthy said: "Microchip Colorado Springs has a long history of partnering with the city and state and we applaud their

continued support of our efforts to advance the semiconductor industry in the US. The CHIPS and Science Act is already making a positive impact on our business through the Investment Tax Credit and we are seeking capacity expansion grants for several of our semiconductor factories, including our Colorado Springs factory. We see a bright future in the region made possible by great partnerships, state and local incentives, and a strong local talented workforce."

Toshiba launches gate-driver for automotive DC motors

TOSHIBA has launched TB9083FTG, a gate-driver for automotive brushless DC motors used in applications such as electric power steering (EPS), electric brakes and shift-by-wire. Volume shipments start today.

The new product TB9083FTG controls and drives external N-channel power MOSFETs for driving a three-phase brushless DC motor. It is highly capable against the ISO 26262 2nd edition functional safety and supports ASIL-D for use in highly safety-critical automotive systems. This makes the new product ideal for automotive applications using brushless DC motors, such as EPS, electric brakes and shift-by-wire.

For systems requiring safety relays such as EPS, TB9083FTG has a built-in three-channel gate-driver for the safety relays that control and drive the relays for motors and power supply. This eliminates the need for external components and helps reduce the part count.

TB9083FTG is housed in a P-VQFN48-0707-0.50-005 package with a wettable flank[4] structure. This allows visual inspection of solder joints using an automatic optical inspection (AOI) system, and contributes to improved solder joint reliability.

In addition, Toshiba has verified that it can go through 3000 cycles in the mounting temperature cycling test and has obtained data that will allow customers to use this QFN package with full confidence.

By using a small package ((7.0mm x 7.0mm (typ.)), the mounting area has been reduced by approximately 66 percent against the current product. This helps to control the increase in the mounting area, as the number of electronic components on ECU boards tends to rise due to redundant designs that are effective in ensuring higher levels of safety.

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Virtualisation: a key enabler of the future power grid

Power grids are undergoing a period of radical change. This feature explores the transition to virtualised protection and control in the age of renewables.

BY HENRY NIVERI, PRODUCT MANAGER AT ABB

POWER GRIDS are shifting away from an aging infrastructure designed for one-directional power flow to one able to integrate dynamic renewable energy resources.

To address this complex challenge, operators are looking for new solutions for sustainable power generation, responding to increasing demand and supply requirements whilst maintaining grid stability.

The virtualisation of protection and control forms a key part of this journey, offering new possibilities to optimize the supply of renewable generation and achieve flexibility and scale.

The transition to virtualised protection and control is one of the enablers in the battle to stabilise the electricity grid in the age of renewables. The energy transition is certainly on. Already about 30 percent of the world's electricity comes from renewables, including hydropower, solar and wind.[1] By 2026 this figure is forecast to rise to the equivalent of today's fossil fuel and nuclear energy capacity combined.[2]

But while this emerging new energy economy may be critical to our low carbon future, integrating these new energy sources is having a fundamental impact on the electrical grid. Put simply, our aged grid infrastructure was not designed for the renewable

energy revolution. It was only designed to deal with a steady, reliable supply of energy, under the basic assumption that electricity generation is easily adjustable depending on the amount of electricity consumed. The inherent variability of wind and solar, including potential imbalances in supply and demand and changes in transmission flow patterns, make load balancing on the existing grid problematic.

This becomes even more complex when considering the current rate of added distributed energy generation. Today, we are seeing customers taking a more active role in generation, as energy production has become more accessible for all. We have also seen a rise in microgrids being powered by the growth in solar and wind. More decentralized resources enable a more resilient system and allow small and large power consumers alike to produce much of the electricity they need locally. However, distribution system operators still need to ensure stability and alignment between generation and demand.

Add to the mix a changing grid profile, as electricity needs evolve with rapid electrification driven by electric mobility, heating and ventilation, data centers and emerging industries, and it becomes clear that the world needs innovative approaches to balance the grid – and fast. Enter virtualisation which is set to become a key enabler in efficient supply and demand management, optimization and, in turn, grid stability.

Virtualisation in electrical distribution

Virtualisation – which, in simple terms, means creating a virtual, rather than actual, version of something – can help to stabilize the electrical grid in several ways.

But to understand how, we must first look at a typical modern substation. Though the size of today's substations can be variable, typically those that serve the power generation sector can be the size of a football field, and house, at the most basic, circuit breakers and switches, isolators, transformers and a busbar system to enable the smooth functioning of transmission and distribution systems.

Though, as the power grid needs continue to evolve, today's substations are increasingly integrating additional technology too. From communication components, such as routers, Ethernet and mobile phone networks, and operator terminals through to SCADA (Supervisory Control and Data Acquisition) systems to enable full monitoring and control of all connected devices, most substations today have multiple computing devices, both legacy and newer assets, running specific applications and working in isolation.

This can make maintenance a minefield for the standard operator, tasked with keeping track of an ever-growing list of varied components. In most cases too, because individual devices have vendor-specific properties, for example, communication interfaces or engineering tools. This means any modifications involve a specialist skillset to be outsourced at a cost. This requirement will continue to grow as more digital functionalities, such as increased monitoring, diagnostics and analytics, are added.

Further, more devices mean more space required in a substation, making the task of physically installing and maintaining each asset a challenge in itself. Additional considerations include the expenditure associated with power supply, cooling, heating and ventilation requirements, maintenance and whole lifecycle management. Through virtualisation, it becomes possible to address many of these challenges by consolidating multiple workloads, such as protection and control, from various pieces of equipment into one single, easy-to-use platform. In short, virtualisation separates software functionality from the physical device.

As the first major benefit, virtualisation drastically reduces the number and type of devices in substations. These devices could be handling, for example, protection, control, monitoring, diagnostics, and communication. This means that there are fewer devices to replace, test, commission and maintain. As there is only one kind of hardware running all the different tasks it effectively eliminates the need for users to learn the specifics for each device and reduces the amount of knowledge required to maintain the substation. It also enables most key activities to be performed remotely, in real-time, anywhere in the world, negating the need for a physical presence. The result is faster, less expensive operations.

But the benefits do not end there. What is equally appealing about virtualisation is the ability to aggregate all the data from various devices in the substation into one single location. For the utility provider, the wide-reaching visibility afforded by this approach can empower better decision making in power quality, renewable integration, asset management and more.

Virtualised protection and control

Inherently, the switch from a conventional approach to a virtual one will not happen overnight. As with all big innovation, it will only be achieved through incremental steps – the first of which will be the shift towards virtualised protection and control.

As many utility operators know, handling protection and control is complex, because of the involved engineering and maintenance required with interdependencies born out of the increasing amount of intelligent devices. Take, for example, the growing demand and the increasing penetration of large-scale intermittent sources, such as wind farms and solar panel systems, which place new pressures on the need to balance local supply and demand

as much as possible, maintain voltage levels within tolerances, and control power quality and reliability at connection points.

Given the typical complex setup, which can entail any number of varying protection and control, measurement and communication devices which needed to be both physically installed and integrated into the established substation, the resulting system can be complex to maintain.This is where virtualisation comes in. By virtualising protection and control functions, it becomes possible to upgrade, maintain and operate the protection and control arrangement in real-time with ease.

Working via one central software platform also makes it easier to analyse and act upon the data obtained from the assets, individually and collectively. For the busy utility operator, this level of insight will be game-changing. Through a more holistic overview, it will allow energy distributors to respond to significant changes far better and even prepare for them ahead of time. This strategic approach also affords the ability to identify and address issues before they escalate and analyze recurring trends to anticipate similar failures or performance constraints. Virtualisation also entails less material requirements and curbs the carbon footprint associated with material manufacturing. Other benefits include simplified life cycle management and flexibility to scale with ease.

A strong example of this is ABB working with UK Power Networks, as a part of the Constellation project[3], to develop a wide area protection system that uses the 5G telecoms network for communication between substations. Based on the IEC 61850 standard, the system will enable real-time monitoring and control of distributed energy resources such as wind and solar farms.

With thousands of substations across Great Britain, UK Power Networks' new approach has the potential to unlock 1.4 gigawatts (GW) of network capacity that will enable further integration of DER. This would achieve annual savings of 19 million tons of CO_2 emissions and would be a significant step in the right direction for the UK to reach Net Zero by 2050. Constituting a complete industry first, this ground-breaking system follows in ABB's ongoing investment into the virtualisation of protection and control in recent years, with new further innovations in the pipeline.

An enabler for change

The world's energy mix is evolving at pace, and the reality is that utilities will still need to redesign, if not completely overhaul, the grid infrastructure to respond to the challenges that have arisen.

In the interim, sharper focus will be placed on those solutions which can support greater renewable integration and evolving power needs in the now. The virtualisation of physical assets will prove a critical tool, empowering utility operators with the advanced capabilities and intelligence needed to streamline operations, optimise processes and prepare for changes in grid behaviour ahead of time. Not only will this inevitable shift make for a more stable grid but also have a positive impact on the environment. Clearly then, the era of virtual protection and control has arrived.

FURTHER READING

- 1. https://www.iea.org/reports/global-energy-review-2020/renewables
- 2. https://www.iea.org/news/renewable-electricity-growth-is-accelerating-faster-than-ever-worldwide-supporting-the-emergence-of-the-new-global-energy-economy
- 3. https://new.abb.com/news/detail/78658/abb-technology-enables-uk-grid-to-integrate-more-renewable-energy

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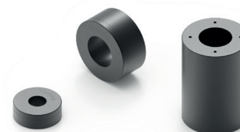

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Bidirectional GaN switches are disrupting power management

Bidirectional voltage blocking and current conduction is an important function in overvoltage protection. How can BiGaN devices help?

BY THOMAS ZHAO, DIRECTOR OF R&D; DAVID ZHOU, VP OF R&D; FELIX WANG, VP OF PRODUCT DEVELOPMENT; AND DR. JAN ŠONSKÝ, VP OF ENGINEERING AT INNOSCIENCE

BIDIRECTIONAL voltage blocking and current conduction is an important function in overvoltage protection on USB ports, switching circuits for devices that operate from multiple power sources and high side load switches. But until now, designers have been limited to using two N type MOSFETs connected back-to-back in a common source configuration.

Such a solution requires two components and suffers from limitations related to on-resistance (RDS(on)), safe operating area (SOA) and other parameters. Innoscience's Bidirectional gallium-nitride (BiGaN) switch is a disruptive solution that reduces power dissipation and offers a significantly smaller footprint. This article introduces our innovative BiGaN device structure, reviews the performance of BiGaN devices and elaborates on different driver configurations for BiGaN.

The integration limitations with MOSFETs are mostly a result of their vertical structure that makes it extremely challenging to put two FETs onto one die with optimised cost, RDS(on), and voltage ratings for devices rated for about 30 V and above. The lateral structures of GaN HEMTs and the lack of a parasitic body diode makes it relatively easy to create a monolithic bidirectional GaN switch.

In a smartphone, for example, replacing back-to-back MOSFETs with a BiGaN HEMT reduces on-state resistance by 50 percent, chip size by 70 percent, and temperature rise by 40 percent (Figure 1).

Losing the losses, shrinking the footprint

The adoption of an over-voltage protection (OVP) switch in the battery management system of a smartphone is driven by the desire to reduce total losses within the minimum possible footprint.

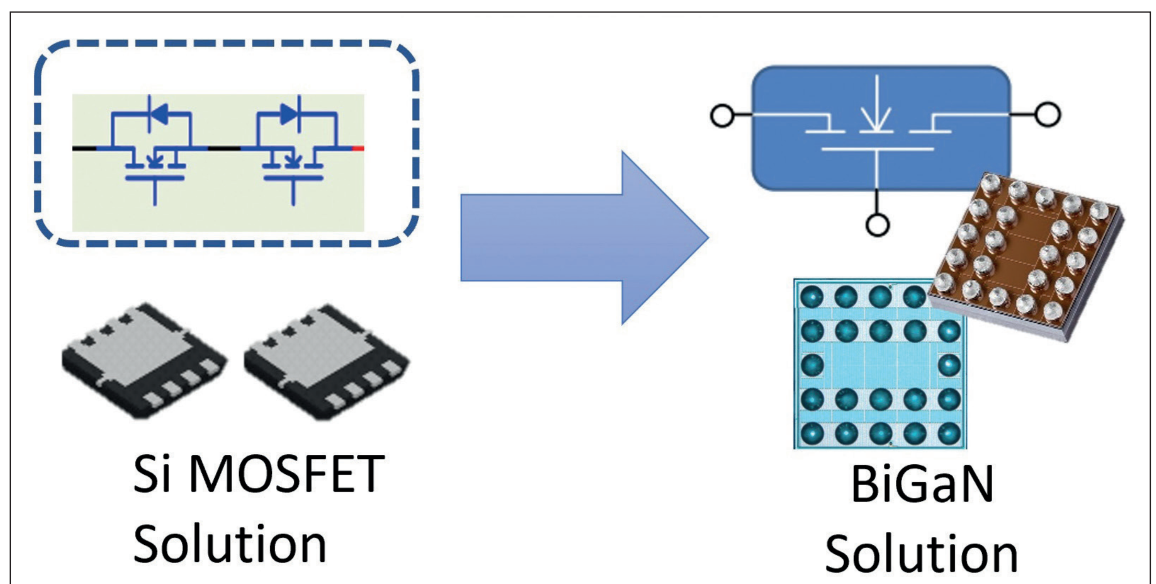


Figure 1. Two back-to-back Si MOSFETs are replaced by one BiGaN

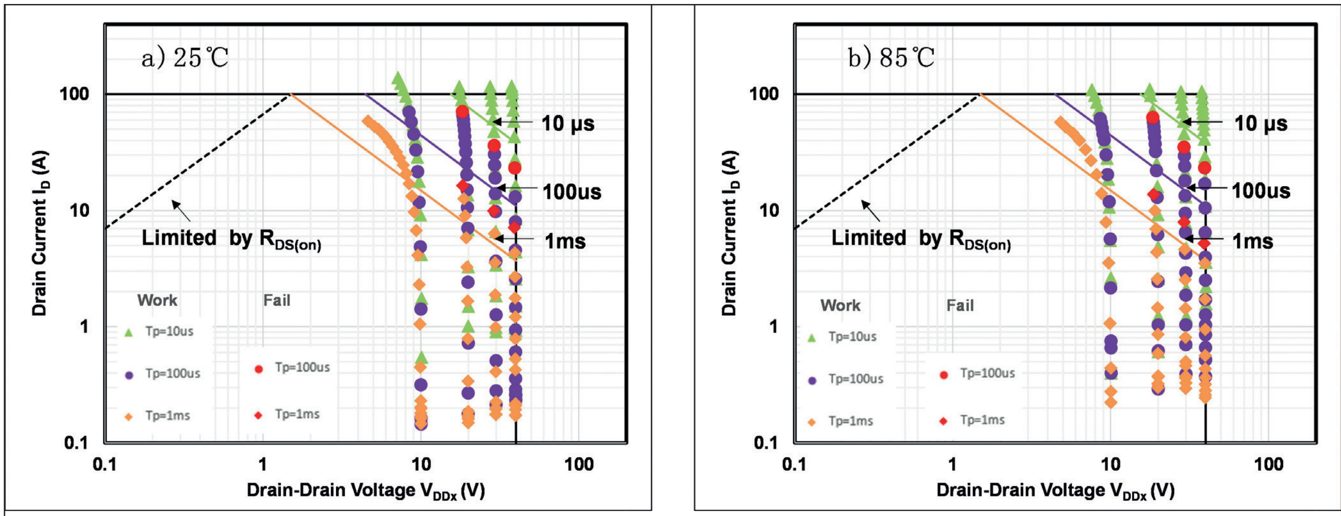


Figure 2: BiGaN INN040W048A SOA: a) 25°C; b) 85°C.

In this particular use case, the power switch is either blocking voltage or conduction current without the need for frequent switching between these two states. Hence the switching losses determined by the gate charge are not important. The total losses are determined essentially only by conduction losses, and thus device total on-resistance.

Traditionally, the OVP functionality is realised by back-to-back discrete MOSFETs. Innoscience's solution is the BiGaN device, which is only slightly larger than a typical single GaN HEMT. It has significantly lower on resistance and is a smaller solution when compared to using two discrete devices in a bidirectional switch configuration.

For a conventional MOSFET, RDS(on) is the resistance between the drain and source when the device is fully on. The equivalent value of a BiGaN device is RDD(on) the resistance between the two drains when the device is fully on. For the 40 V INN040W048A BiGaN bidirectional switch with a drain current of 20 A, the max RDD(on) is only 4.8 mΩ, resulting in a very low conduction losses.

The package can be an important contributor to on-resistance. The lateral structure of BiGaN devices enables the use of a wafer level chip scale package (WLSCP) measuring only 2.1 x 2.1 x 0.54 mm INN040W048A. This package has minimal parasitic resistance, contributing to lower conduction losses and less thermal dissipation. The small package size also results in excellent on-resistance * area performance (Ron*A), an important factor in system miniaturization. And a single BiGaN device replaces two MOSFETs, further contributing to smaller solutions and a reduction in the bill of materials.

Overall, customers can make different trade-offs with Innoscience's BiGaN devices. One option is to maintain the existing space and footprint, while significantly reducing on-resistance and consequently also limiting temperature increase during charging. Alternatively, BiGaN by Innoscience enables significant reduction in footprint for the OVP function, while keeping good on-resistance and thus efficiency.

SOA, Leakage and Robustness

SOA is an important consideration for load switching applications. It's the combinations of voltage and current over which a device can be operated without damage or degraded performance. Factors limiting SOA include Ron, package considerations and thermal considerations. Improving the SOA of a Si MOSFET is challenging due to the negative temperature coefficient of the threshold voltage (Vth). Due to a reduced temperature dependence of VTH in GaN devices, BiGaN can maintain superior SOA performance also at high temperature (Figure 2).

Gate leakage is another important specification in bidirectional voltage blocking applications. Si MOSFETs have very good gate leakage performance. These devices have gate insulated from the channel by a gate oxideresulting in a sub-μA leakage at 25 °C. Since Si MOSFET Vth

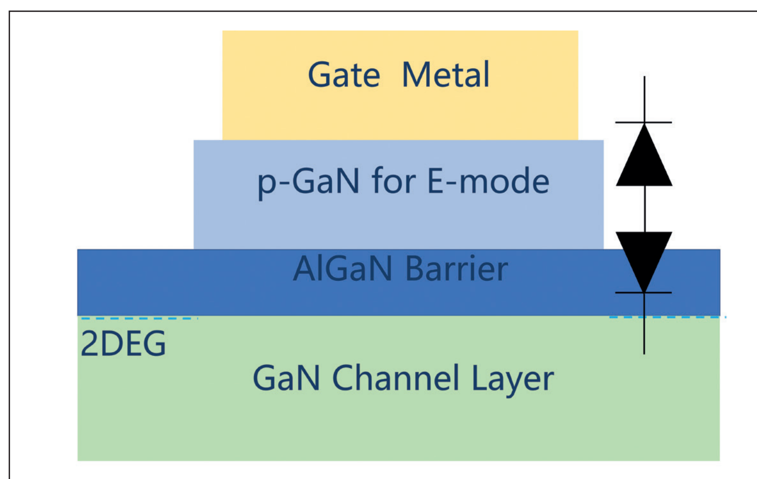
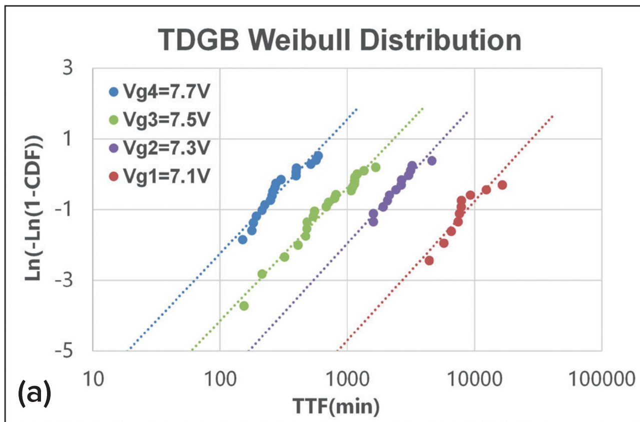


Figure 3: The inherent back-to-back diodes in the gate structure require that strict process control be implemented to achieve leakage under 3 μA at 85°C for BiGaN.



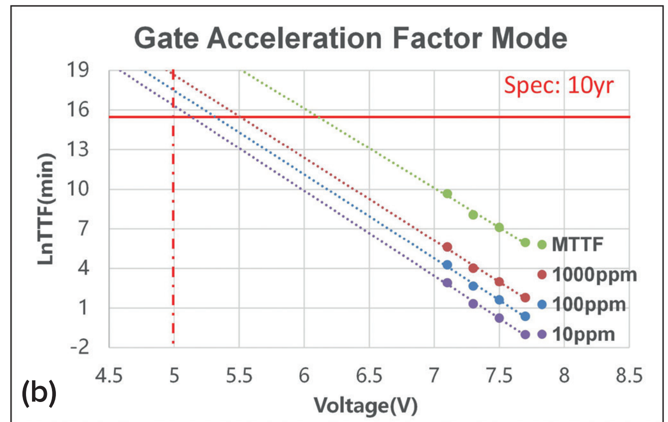


Figure 4: BiGaN Gate robustness: a) TGDB Weibull distribution; b) Gate acceleration mode.

decreases at higher temperatures, the leakage current rises at elevated temperatures.

BiGaN devices have an inherently different gate structure that can be visualised as two back-to-back diodes (Figure 3). The upper diode is a Schottky structure with the gate metal as cathode and the pGaN as the anode.

The lower diode is a junction structure with a pGaN anode and an AlGaN cathode. Without proper control, the gate leakage of a BiGaN device would be higher than that of a Si MOSFET. Innoscience's R&D team has developed differentiating process steps and process controls to ensure the gate leakage is smaller than 3 µA at 85 °C throughout the device lifetime. This was a critical requirement for its adoption in smartphone handsets.

Robust gate and drain operation are expected from all power switches. At 5.0 V (VGD) and 125 °C, the lifetime of BiGaN devices under continuous stress based on a 0.001 percent failure rate (10 ppm) exceeds 23 years. In actual applications, gate voltage spikes can be experienced from events such as short circuits.

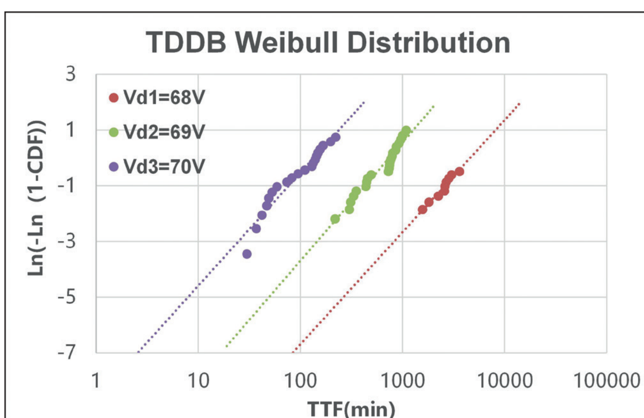
The gate pulse capability of BiGaN devices is 10 million cycles at ≤8.5 V with a 1 µs pulse width, at 25 °C and 85 °C, and 100,000 cycles at 9.5 V and 85 °C (Figure 4). To measure drain robustness, INN040W048A devices were exposed to continue stress of 68 V, 69 V and 70 V at 125 °C. The drain time dependent dielectric breakdown (TDDB) obeys the Weibull distribution and using the most conservative approach to
TDDB modelling, shows that at 32 V (VDD) and 125 °C, the lifetime based on a 0.001 percent failure rate (10 ppm) for BiGaN exceeds 10,000 years (Figure 5).

Driving BiGaN

If the drive voltage is 5 V, existing drivers used with back-to-back Si MOSFETs can be used with BiGaN. In the case of smartphones, most charger ICs are compatible with GaN HEMTs with a 5 V gate drive. Drivers like the SC8571 from Southchip, NuVolta Tech's NU2205, switch capacitor drivers from Texas Instruments and power management ICs (PMICs) from Qualcomm are suited for driving BiGaN.

The gate voltage needs to be at least Vth (~1.7 V) above either Drain1 or Drain2 to turn on a BiGaN device. To turn it off, and block current flow in both directions, both gate to drain voltages (VGD1 and VGD2) need to be below Vth.

Pulling the gate to ground will turn off a BiGaN device. In 5 V applications, a charge pump can be



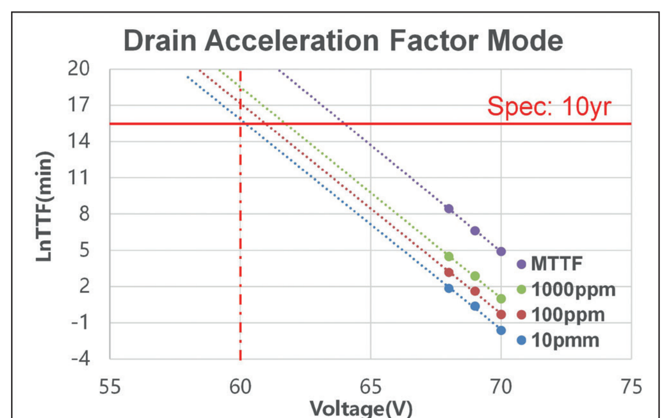


Figure 5: BiGaN Drain robustness: a) TDDB Weibull distribution; b) Drain acceleration mode.

used to drive BiGaN (Figure 6). The gate voltage will be zero when EN is low and the BiGaN will be off. When EN is high, the gate voltage will be pumped to VIN + 5 V and the BiGaN will be ON and VOUT will equal VIN.
In applications other than smartphones, 5 V gate driver ICs are not commonly used. Those applications use drivers with a drive voltage of about 10 V designed for getting the lowest RDS(on) from Si MOSFETs.

Those drivers can't be used to directly drive GaN HEMTs since the drive voltage exceeds the gate's maximum rating. In these applications, a clamping circuit can be used where Zener diodes (D1 and D2) are used to clamp VGD at under 6 V (Figure 8). Diodes D4 and D5 have breakdown voltages over 40 V to provide drain-to-gate blocking.

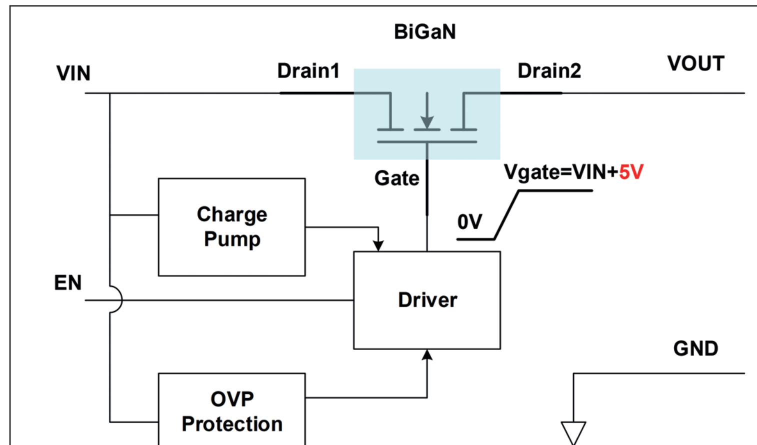


Figure 6: In 5 V applications, a charge pump can be used with a standard 5 V gate drive IC to turn BiGaN devices on and off.

Conclusion

The availability of high-performance, low-cost GaN-on-Si has enabled the development of BiGaN devices that can improve the operation of switching circuits for devices like smartphones that operate from multiple power sources, high side load switches, overvoltage protection on USB ports and similar applications.

As shown, BiGaN is reliable and easy to use. In smartphones, BiGaN can support fast charging with lower temperature rises compared with solutions using back-to-back Si MOSFETs. In addition, the small solution size when using BiGaN enables the devices to be embedded in the handset, instead of the charger, to control battery charging and discharging currents.

Taking that function out of the charger can support smaller charger designs. BiGaN is a disruptive development that is enabling new design paradigms.

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There is still life in the silicon IGBT

But silicon carbide is the long-term future for energy efficiency

Tesla's recent announcement that it will use 75 percent less silicon carbide (SiC) in a new powertrain for lower cost EVs sent a small shock-wave through the industry. With investment in SiC fabs running to billions of dollars from the likes of Wolfspeed, Infineon, STMicroelectronics, Onsemi, Microchip, and II-VI, surely SiC is the way forward for EV power electronics?

SiC MOSFETs offer faster switching and a higher temperature capability than silicon IGBTs, along with a smaller footprint for the passive components. All these factors make them ideal for EV drivetrain inverters. Except … SiC chips are expensive. And until new fabs come on-stream, they will remain so. In this context, Tesla's plans to develop lower cost inverters based largely on silicon power devices makes sense, certainly in the short term. For similar reasons, silicon IGBTs will continue to make economic sense for many other power applications including wind turbines.

18 months ago when PGC, a consultancy dedicated to SiC technology, analysed SiC die costs, the retail price of 100A SiC MOSFETs (both 650V and 1200V) was three times that of equivalent silicon IGBTs. The SiC die had the advantage, however, of taking up three to four times less space.

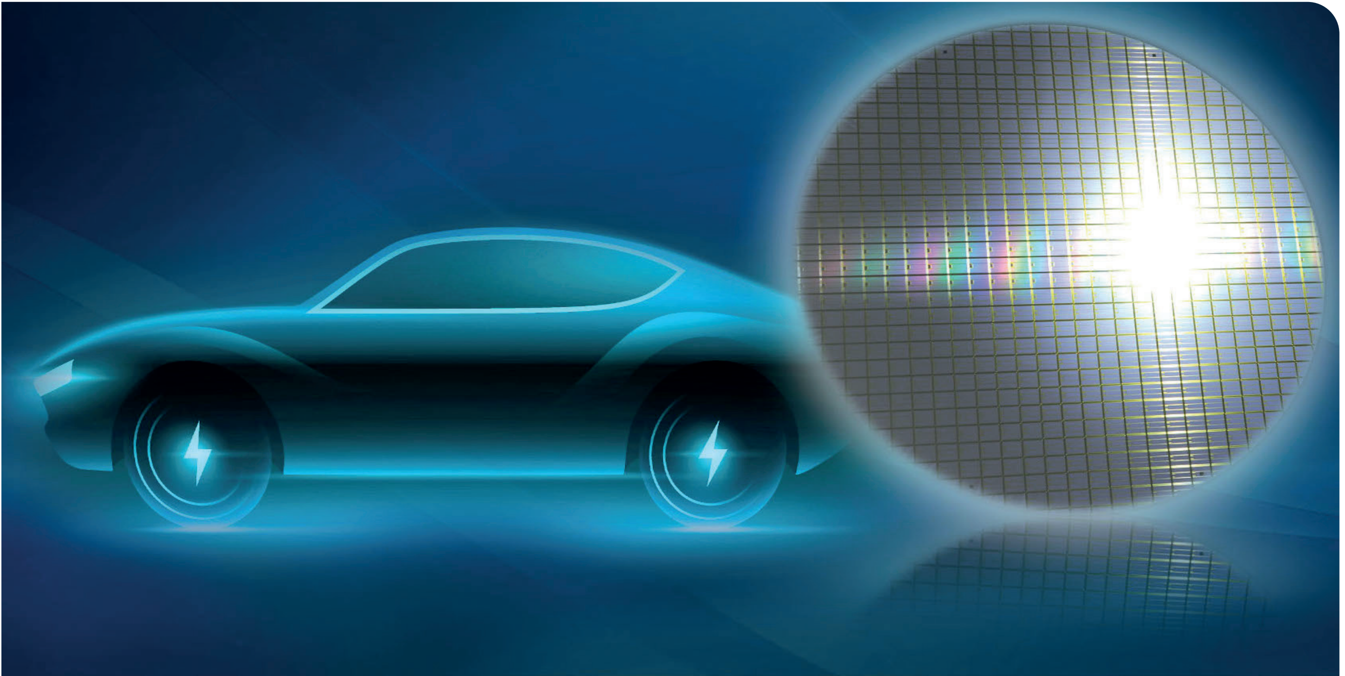
Earlier this year, Jelena Loncarski and Alberto Bellini from the University of Bologna and Hussain A. Hussain from Kuwait University, compared the efficiency, cost, and size of a SiC-based and an IGBT-based full-scale converter in a PMSG (permanent magnet synchronous generator) wind turbine. In this case, the cost of a SiC solution was twice as high as the silicon IGBT design.

The researchers' paper 'Efficiency, Cost, and Volume Comparison of SiC-Based and IGBT-Based Full-Scale Converter in PMSG Wind Turbine' in *Electronics* (2023), focused on a 2MW PMSG based wind conversion system with a bidirectional full-scale frequency converter comprised of two back-to-back inverters. Using a PLECS simulation tool, they compared wind energy systems both for the same switching frequency (low switching frequency suitable for IGBT modules) and also a SiC-MOSFET-based converter working at high switching frequencies.

They calculated that a SiC-based converter in the wind generation system would provide a similar efficiency to a silicon-based converter, but would reduce the system's size. In particular, the total volume of passive components was cut by 4.54 times (4.25 times in the case of 55 °C ambient temperature). However, as mentioned earlier, the price increase was a factor of two.

Power2Power

In 2019, 43 partners from industry and research (coordinated by Infineon in Dresden) began a three-year, EU-funded project called Power2Power to improve silicon IGBT technologies. The results suggest there's plenty of life left in IGBTs.



The project partners improved IGBT semiconductor manufacturing processes related to ion implantation, metallisation, device and yield optimisation. They also developed an advanced micro-pattern trench (MPT) IGBT that outperforms current approaches. And they enhanced pressure-less chip soldering, wire bonding, clip sintering and automated packaging.

For end applications, the project showed that IGBT-based energy conversion can reach an efficiency of over 98 percent for EV converters and drive trains. Moreover, IGBTs can cut the cost of rolling stock energy chargers by 30 percent and extend the lifetime of electric vehicle chargers by 1.5 times.

Jochen Koszescha, senior director of funding projects & coordination at Infineon, commented: “Even though new power semiconductor materials like SiC or GaN play an important role in supporting the efficient conversion to a sustainable, independent energy supply, silicon-based power semiconductors are predicted to dominate the market even beyond 2030.”

Underlining this trend, Renesas Electronics is rolling out a new generation of IGBTs, the AE5 series, targeted firmly at EVs. By reducing inverter power losses, these IGBTs are said to improve power efficiency by up to 6 percent compared to Renesas’ previous generation technology, allowing EVs to drive longer distances. The devices are initially being built on 200- and 300-mm wafers at the company’s fab in Naka, Japan. Next year Renesas will ramp mass production on a new 300-mm power semiconductor line in Kofu.

The future

Of course, as SiC-MOSFET modules prices drop, the benefits of SiC-based systems will become more marked. “In order to have overall system cost and volume savings with the SiC-MOSFET-based conversion system, the price of the SiC devices should be substantially lower, at least two times in order to have an equal cost to the Si-based system,” write Loncarski and colleagues in their paper about wind turbines.

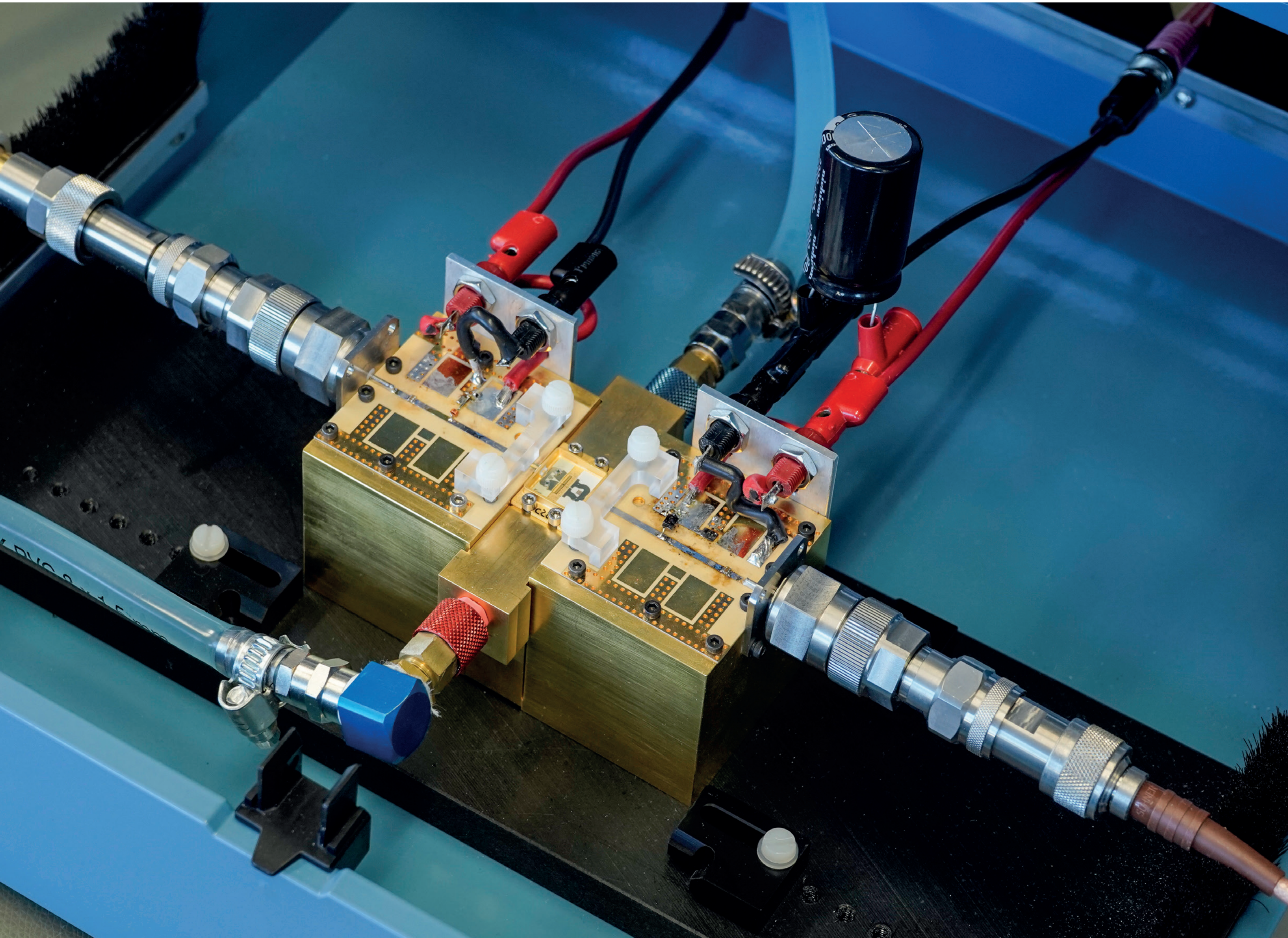
They conclude: “The cost function applied to the efficiency, volume, and cost with different weights (less for the efficiency and equal to the cost and volume) has shown that the SiC-MOSFET-based converter at 30 kHz has the best value, regardless of its higher cost, when compared to a Si-IGBT converter, as the benefits in the volume reduction were superior.”

A new IDTechEx report *‘Power Electronics for Electric Vehicles 2023-2033’* highlights SiC technology’s benefits in the context of the shift from 350-400V to 800V in EVs. 800V allows joule losses to be reduced and high voltage cabling to be downsized.

Combined with 1200V SiC MOSFETs, this typically leads to 5-10 percent efficiency gains, which can potentially downsize the expensive battery, save costs, or improve the vehicle’s range, says IDTechEx.

SiC’s electronic properties make it well suited for higher-voltage applications, where it can deliver superior performance at a more competitive cost. As high-volume SiC device manufacturers ramp up production, SiC will increasingly become cost competitive with silicon.

Nevertheless, silicon IGBTs have dominated the medium-to-high power device range for 20 years. And may well continue to for a while longer.



Targeting the C-band with ultra-high-voltage HEMTs

GaN HEMTs with a minimal output capacitance and terminated harmonics deliver record-breaking powers and efficiencies

BY SEBASTIAN KRAUSE FROM THE FRAUNHOFER INSTITUTE FOR APPLIED SOLID STATE PHYSICS IAF

DURING THE LAST DECADE, the GaN-on-SiC material system has established itself as the dominating semiconductor technology for delivering very high powers in the gigahertz range. Its more established rival, silicon-LDMOS, is more popular, and the cheaper choice for powering most systems in the VHF and lower UHF spectrum. However, this incumbent is even losing market share in that application space to GaN: this wide bandgap rival is renowned for its higher device efficiency, which trims operational expenses; and its higher power per die area that enables the design of smaller and lighter systems.

The enviable position that GaN holds in the high-power market is primarily due to its capability to maintain a high efficiency, even at high voltages and hence high-power levels. In contrast, LDMOS struggles to find a sweet spot that ensures a good efficiency, alongside a high-power density and high-frequency performance. So usually a trade-off has to be made in device design, favouring one attribute. Or, to put it another way, GaN has the stamina to go

the extra mile, in terms of its frequency range, while LDMOS is already running out of gas.

However, there's a need to understanding the underlying physical principles of these limitations, and pinpoint the critical device parameters that require careful tuning, in order to optimise GaN devices. Clearly, device scaling does not come for free.

Looking towards higher frequencies, the predominance of GaN is built on its capability to deliver very high powers and efficiencies. Yet, generally accepted scaling rules apply, implying that operation at higher frequencies must go hand-in-hand with a reduction in supply voltage. Consistent with this expectation are the product portfolios of manufacturers: they list the availability of 65 V devices up to 2 GHz, while those capable of 12 GHz and 18 GHz seem to mark the final frontier for 50 V and 40 V transistors, respectively. Beyond that, devices are rated for 28 V operation, if at all.

Last summer Integra Technologies of El Segundo, CA, launched a packaged 100 V GaN HEMT. This product pushes the boundaries for the supply voltage and ultimately the output-power-per-device. Designed for L-band avionics radar operating in the 1.030 GHz to 1.090 GHz band, this HEMT adheres to the mapped-out trend, highlighting once again that higher frequencies must be traded for supply voltage.

There are applications demanding kW-level powers higher in the spectrum, such as the C-band (4 GHz to 8 GHz) and even the X-band (8 GHz to 12 GHz). It makes much sense to try and address these opportunities with GaN, by taking on the challenge of marrying its high-frequency attributes with its outstanding high-power capabilities.

Keeping control of the charge

Unfortunately, when designers move to higher voltages, there is not much working in their favour. In fact, almost every critical performance parameter appears to get worse when raising the supply – there are problems associated with the transition frequency, greater trapping and diminished reliability to name but a few. All these issues stem from the rising electric field, which is the main factor to consider when trying to maintain performance when shifting operation to higher voltages.

Another major downside of a higher electric field is that it can lead to so-called 'short-channel effects'. When this happens the gate, which is solely responsible for controlling the electrons in the channel under ideal conditions, struggles to do its job. Short-channel effects tend to be associated with high-frequency technologies, because their occurrence usually leads to an 'under scaling' of electrical parameters – that is, electrical parameters scale less than what the scaling rules imply. Note that broadly speaking, scaling up in frequency or in voltage leads to similar field-related issues, unless appropriate countermeasures are taken.

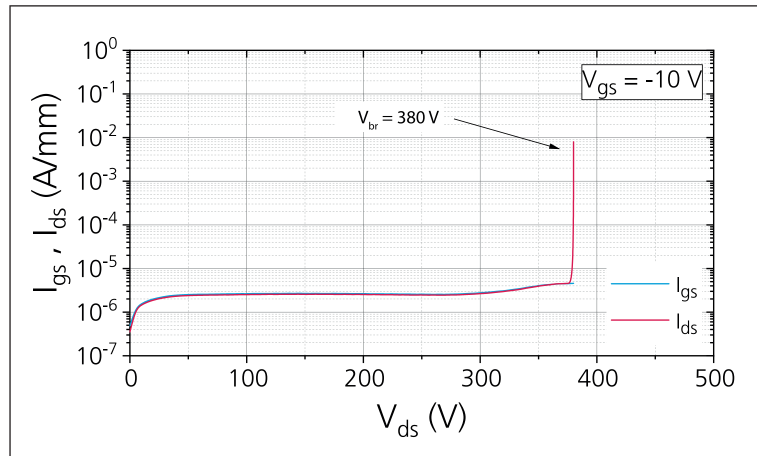


Figure 1. Drain-Source breakdown characteristics for a device with a total gate width of 1.2 mm (6 x 200 µm). For the measurement, the source of the device is grounded, whereas the gate potential is set to - 10 V. Then the drain potential is quickly raised until the recorded gate and drain current exceed the compliance value of 1 mA/mm, which is considered as breakdown.

One common countermeasure is to introduce field plates, a concept found in most GaN technologies up to Ka band. As its name suggests, the role of the field plate is to tame the electrical field by spreading this out from the gate towards the drain electrode. With its addition, there is a reduction in the maximum electric field close to the gate contact, and a quashing of short-channel effects. Another benefit is that a device can realise a higher breakdown voltage for a given on-resistance. Since a higher on-resistance translates to increased losses, it is crucial to keep this as low as possible when targeting the highest efficiency.

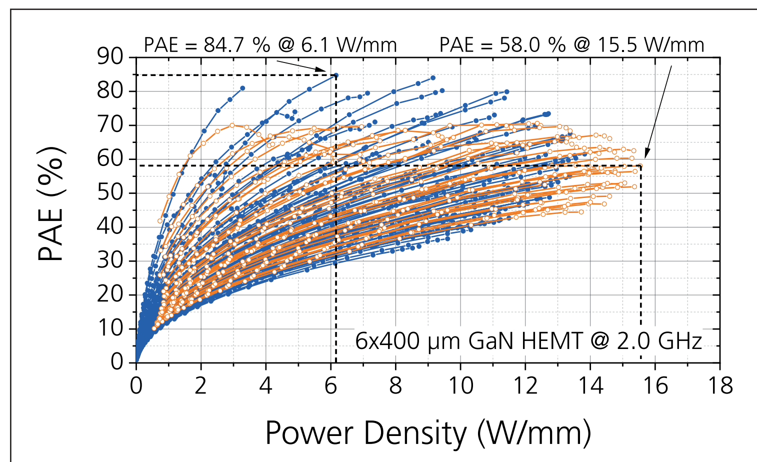


Figure 2. Pulsed load-pull measurements of a 100 V GaN HEMT with a total gate width of 2.4 mm (6 x 400 µm) at 2.0 GHz. The pulse width is 100 µs with a duty cycle of 10 percent. Two conditions are plotted here. Orange is for load pull at the fundamental frequency without termination of harmonics, while blue is for fundamental load pull with second harmonic impedances at input and output set for maximum efficiency.

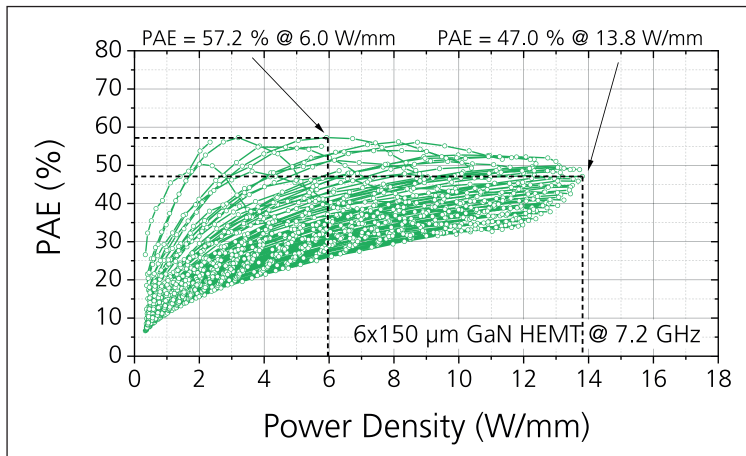


Figure 3. Pulsed load-pull measurements of a 100 V GaN HEMT with a total gate width of 0.9 mm (6x150 μm) at 7.2 GHz. The pulse width is 100 μs, with a duty cycle of 10 percent. No harmonics have been terminated during the measurement.

Working at the Fraunhofer Institute for Applied Solid State Physics IAF, our team is engineering devices to try and meet these criteria. Measurements show that the breakdown voltage for our 100 V GaN HEMTs is in excess of 350 V (see Figure 1). Meanwhile, on-resistance is just 4.2 Ω mm, a value merely one-third higher than that of established 50 V GaN processes.

Setting the stage for harmonics

At first glance, it would appear to be rather conservative to have such a high breakdown voltage for a 100 V device. However, there is good reason behind this caution – harmonic termination. When you dive a bit deeper into high-efficiency amplifier design, you are very likely to come across this technique of manipulating harmonic impedances.

Ultimately limiting the efficiency of an ideal amplifier is its class of operation. While class A and class B are probably familiar to most of us, brave designers opt for class E, class F or class F^{-1}, which is also known as inverse class F. These latter three have a theoretical efficiency of 100 percent, while class B and class A are limited to 78.5 percent and 50 percent, respectively. In practice, all these numbers are impossible to achieve, due to the lossy nature of real devices. However, efficiencies as high as 90 percent have been demonstrated for GaN HEMTs. I doubt you expected a free lunch, so you'll not be surprised that harmonic termination comes at a cost. Presenting specific impedances to the device at its harmonic frequencies – ideally a short or open circuit – alters the time domain waveform at the device output. For Class E and class F^{-1}, there can be waveforms with a voltage magnitude as high as three-and-a-half times the supply voltage. Such a high voltage arises due to the high second harmonic impedance (at or close to an open circuit) that is required for the operation modes. Due to this, a sufficiently high breakdown voltage is a pre-requisite for reaching the highest efficiency levels.

At higher frequencies the concept of harmonic termination slowly falls apart. This arises because real devices show a finite output capacitance in parallel to the intrinsic current source. Over frequency the reactance of the output capacitance decreases, forming a shunt current path to ground. If the designer now tries to force the device into class-E or class-F^{-1} operation, the open circuit at the second harmonic is bypassed by the output capacitance. At a certain frequency this results in an effective short-circuit for the second harmonic and all higher harmonics. This set of shorted harmonic impedances leads to the class-B condition, limiting the maximum theoretical efficiency from 100 percent to 78.5 percent.

In addition to this road block to realizing a high efficiency at high frequencies, there is another issue associated with high voltages. In this case it is the praised field plates that are part of the problem. Most troublesome are the so-called source-terminated field plates – they can account for a large proportion of a device's output capacitance. It's tempting to simply ban this form of field plate from the device layout, but such a move would contradict the goal of proper field control. Like many times in life, it's better to seek a good trade off.

Stepping up in efficiency

Previously, we demonstrated a power-added efficiency of more than 77 percent at 1.0 GHz, a record for 100 V GaN HEMTs at the time. However, we uncovered some weak spots when we compared this device to our baseline 50 V devices. Deficiencies included a maximum efficiency that lagged the baseline devices by around 7 percentage

> We believe that more is possible. There is no reason to think that the C-band is the ultimate limit for 100 V GaN HEMTs. Our high levels of performance at these frequencies imply that there is still room to push the technology towards the X-band.

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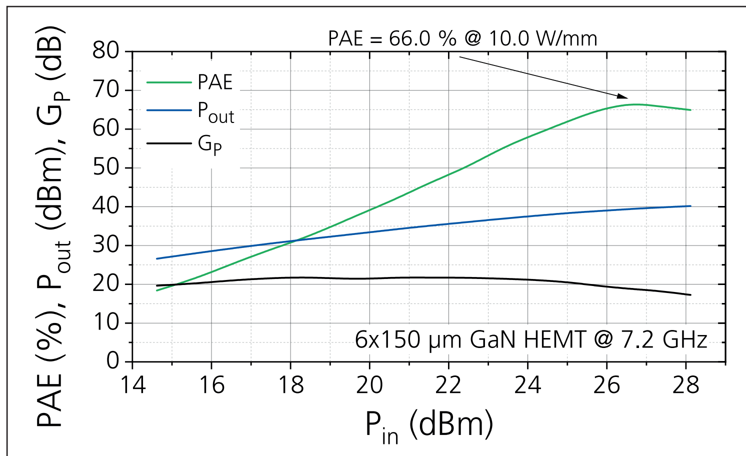

Figure 4. Pulsed load-pull measurements of a 100 V GaN HEMT with a total gate width of 0.9 mm (6 x 150 μm) at 7.2 GHz. The pulse width is 100 μs, with a duty cycle of 10 percent. For this measurement a 'trade-off' of fundamental impedance was chosen that yielded a good combination of efficiency and power density. Additionally, the second harmonic at the output of the device was set for the value that showed the highest power-added efficiency.

points. We also observed a pronounced efficiency roll off when measuring our 100 V devices at higher frequencies.

To address these weaknesses, we decided to make a fresh start. This involved redesigning the epitaxial stack and the intrinsic device features, with the goal of tightening the electrostatics. When we extracted the drain-induced barrier lowering – a measure that quantifies the parasitic control over the electrons by the drain contact, with the lower the value the better – we verified our success. This key figure of merit showed a five-fold reduction, yielding a value below 1 mV/V. In a nutshell, this result reveals that the gate has all the power over the electrons, without any interference from the drain at high voltages.

Further measurements underscored the capability of this new device. They revealed a record-breaking power-added efficiency for our 100 V GaN HEMT at 2.0 GHz of 84.7 percent – that's an increase of almost 8 percentage points, despite a doubling in frequency. The maximum power density hit 15.5 W/mm (see Figure 2).

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There's more to our second-generation device than just headline-grabbing figures. By revising the intrinsic device layout, we have shaved off as much of the output capacitance as possible without deteriorating electrostatics. This refinement should enable these transistors to operate efficiently at much higher frequencies than before. By trimming the output capacitance by 40 percent, theory would suggest that these devices are susceptible to harmonic termination at higher frequencies.

Evidence from the lab supports this view. Measurements at the upper C-band frequency of 7.2 GHz – used by the European Space Agency for Deep Space Antennas to track spacecraft throughout the complete solar system – provide very impressive results. According to fundamental load-pull measurements, the power density is only a little down from the value for 2.0 GHz, reaching an impressive 13.8 W/mm. Meanwhile, power-added efficiency tops out at 57.2 percent.

Still, the question remained on whether terminating harmonic impedances would enhance efficiency. Due to set-up limitations, we could not tune the input and output simultaneously, as we had done for the 2.0 GHz measurement. So we tuned just the output second harmonic, and selected a fundamental load that provided a judicious combination of efficiency and power density. We then optimized the second harmonic phase, until we found the setting that yielded the maximum efficiency (see Figure 4 for the results of the power sweep).

The reduction in the output capacitance has paid off. The power-added efficiency has climbed to 66.0 percent, an increase of around 9 percentage points compared with the load pull without second harmonic termination. This value also sets a new benchmark for the efficiency of 100 V GaN HEMTs in the C-band. No less impressive are the associated power density of 10 W/mm and the gain of 18.5 dB, both achieved at the maximum power-added efficiency.

Crucially, these performance numbers are realized simultaneously, rather than marking the individually best obtainable values – that sets these 100 V devices apart from commercially available GaN technologies. While the power-added efficiency of our ground-breaking HEMTs is comparable to the best 40 V and 50 V technologies, the power density and gain of our 100 V devices is a big step up from the capabilities of today's commercially available GaN HEMTs.

We believe that more is possible. There is no reason to think that the C-band is the ultimate limit for 100 V GaN HEMTs. Our high levels of performance at these frequencies imply that there is still room to push the technology towards the X-band. We don't know where exactly the frequency limitations of these high-voltage devices are, but we are prepared and willing to find out.

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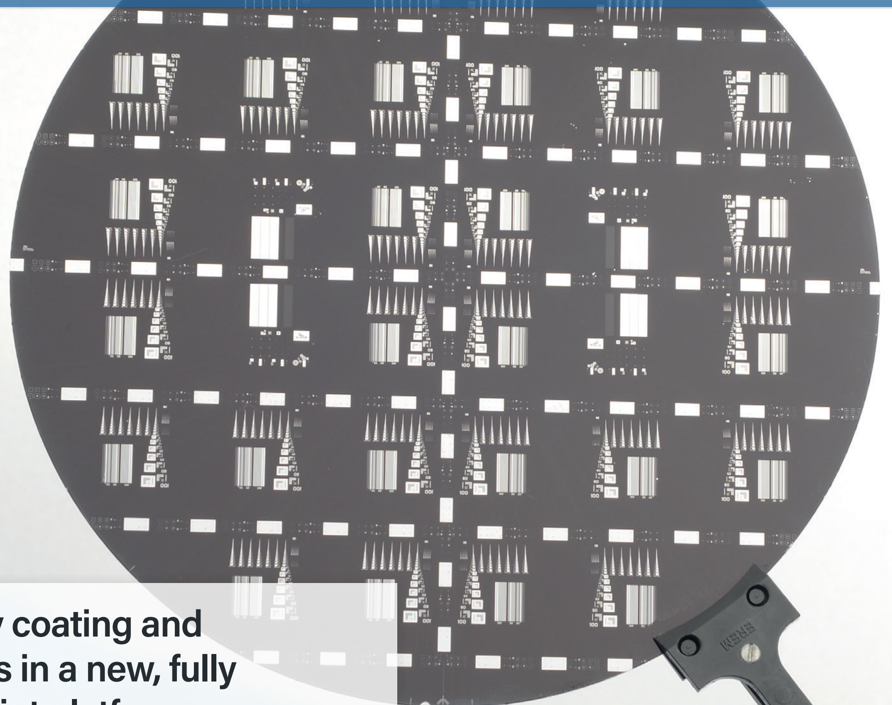

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Controlling threshold voltage instabilities in SiC MOSFETs

System designers can now benefit from new test and stress procedures for SiC MOSFETs that realistically determine their worst-case threshold voltage variations

BY THOMAS AICHINGER FROM INFINEON TECHNOLOGIES

ONE OF THE GREATEST strengths of the SiC power MOSFET over its silicon-based equivalent is its capability to operate at much higher switching frequencies and lower losses. Thanks to this, engineers can build advanced power electronic circuits that feature smaller cooling units and smaller passive components. These gains are so highly valued that as well as opening up new applications, they are enabling SiC MOSFETs to replace silicon counterparts in existing applications, where new ground is being broken for lighter, more efficient system design.

When engineers design circuits with SiC components, they expect that as well as exploiting the performance benefits, they will not be held back by any compromise in quality compared with silicon counterparts. There is an expectation from these engineers of a predictable electrical parameter stability over lifetime.

Unfortunately, until fairly recently the initial general impressions of these engineers had been that SiC technologies are not quite there. There were concerns, for instance, regarding so-far-unknown threshold voltage (V_{TH}) peculiarities, and their extraordinary electrical parameter drifts during reliability investigations. Scientific papers had shown large V_{TH} variations within short periods of stress, raising concerns that critical electrical parameters of SiC MOSFETs were highly variable, threatening to get out of control during operation in the field, sooner or later.

Until recently, the origin and the application relevance of these short-term V_{TH} instabilities in SiC MOSFETs had not been fully understood, with literature reporting a wide range of parameter variations. Various possible reasons have been proposed. One is that first-generation products had varied levels of quality; and a second is that fundamental issues hampered stable, reproducible measurements of crucial electrical parameters, such as the threshold voltage.

Recently, this second issue has been addressed by the release of new measurement guidelines for evaluating the V_{TH} in SiC MOSFETs, published by JEDEC and drawing on contributions from our team at Infineon. We have gone on to develop a deeper understanding of the trapping dynamics at the metal-oxide semiconductor (MOS) interface. Outlined in this first section of this article, this insight has helped us to adapt V_{TH} measurement routines so that they resolve the issue of undefined and non-reproducible measurements.

With a reproducible and reliable V_{TH} measurement procedure at hand, we have made further strides, finally quantifying the effect of electrical stress on

the condition of a device in a standardised way. This has been most valuable in dispelling major doubts surrounding the overall stability and controllability of SiC MOSFET technology. Our findings include the revelation that the mysterious short-term V_{TH} variations are fully reversible and recur in every single switching cycle. Note that this effect, found in all SiC MOSFETs in the market and already present in pristine devices, is not a cause for alarm: it is an inherent device characteristic, rather than a reliability-critical degradation mechanism.

Our next important step has been to discover how to stress SiC devices in the most realistic way, so that we can determine worst-case V_{TH} variations after the MOSFET has been used in an application for its intended lifetime. Historically, the approach that's been applied to silicon power MOSFETs to check for systematic V_{TH} variations is to raise these devices to an elevated temperature and perform static stress tests at a constant positive or negative gate bias. For high-temperature gate-bias tests, one would tend to select a stress temperature and bias higher than the use conditions, in order to cover the chip's entire lifetime within a 1000-hour (typical) qualification test. The result produced by this test has always been considered to be the worst-case scenario. It has been assumed that a common alternative – the more application-near, gate-switching stress test – is less critical, because it may involve some compensating drift effects and recovery phases in between. We question that assumption with work showing that these factors do not apply to SiC MOSFETs. These findings are described in the second section of this article, along with our completely new stress procedure.

Threshold voltage peculiarities

A stable and reproducible measurement of V_{TH} is important. It's needed to define the datasheet values of pristine devices and it's mandatory for assessing V_{TH} evolution in a stress experiment. In silicon MOSFETs this task is straightforward – it does not require any particular precaution. Pristine silicon power transistors always show the same V_{TH}.

That's not the case, though, in SiC MOSFETs, which have a V_{TH} that's not constant. According to our measurements, the V_{TH} shows different values when the transistor turns on, coming from a negative gate voltage; and when it turns off, coming from a positive gate voltage (see Figure 1). This indicates that there's a need to define the V_{TH} hysteresis: it is the difference between the V_{TH} during turn-on, the so-called upsweep V_{TH} (V_{TH}^{UP}); and V_{TH} during turn-off, the so-called down sweep V_{TH} (V_{TH}^{DOWN}).

Hysteresis is at its largest when sweeping the gate between deep accumulation and deep inversion, for example, between -10 V and +15 V (this is illustrated in Figure 2, which shows typical transfer characteristics of SiC MOSFETs for fast upsweeps and downsweeps of the gate voltage). Hysteresis

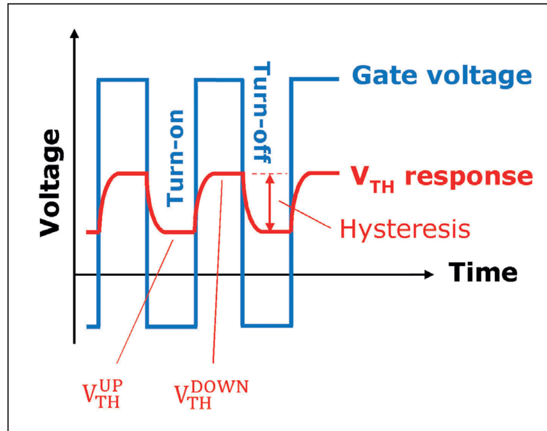


Figure 1. An illustration of threshold voltage dynamics of a SiC MOSFET when switching the gate of a pristine SiC MOSFET in bipolar mode.

reduces when the upsweep starts at voltages closer to 0 V, and when sweeping is slower.

Our investigations suggest that these effects are due to short-term charging and discharging of pre-existing traps located near to or directly at the SiC/gate-oxide interface. We have determined that the upsweep V_{TH} is always lower, because the interface is charged positively in the negative half period of the gate pulse, due to holes captured from the valance band. Meanwhile, the down sweep V_{TH} is always larger, because the interface is charged neutrally or even negatively in the positive half period of the gate pulse, due to electrons captured from the conduction band. There is actually a continuum of possible V_{TH} values within the

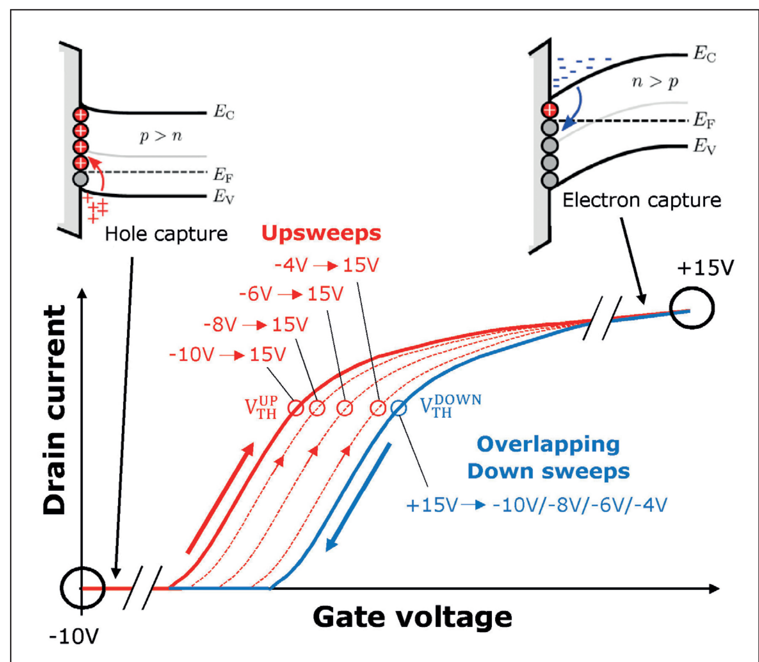


Figure 2. Transfer characteristics vary during turn-on and turn-off. V_{TH} is lower during turn-on due to holes captured at negative gate bias. During turn-off, V_{TH} is higher due to electrons captured at positive gate bias. Hysteresis reduces when the upsweep starts at gate voltage levels closer to 0 V, because fewer holes are trapped during the negative gate voltage period.

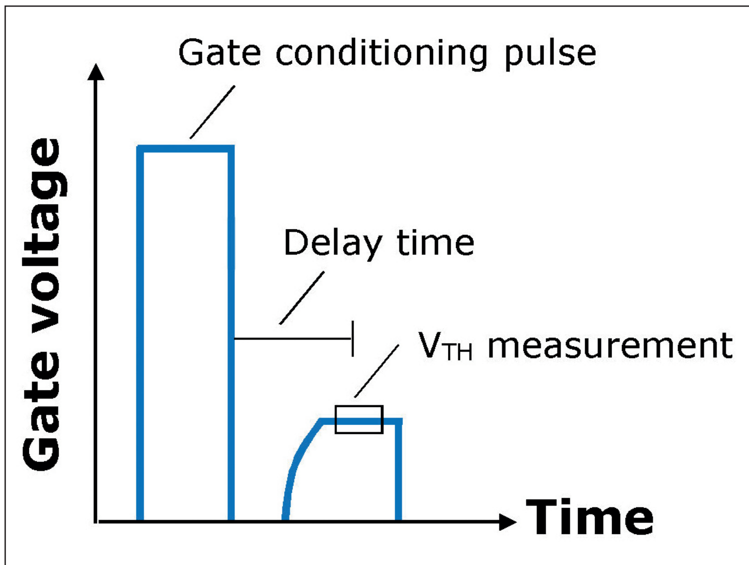


Figure 3. An example of gate conditioning. Before measuring the V_{TH}, a positive gate pulse is applied for several milliseconds to bring the MOS interface to a defined charged state. Afterwards, a V_{TH} spot measurement is performed using, for instance, a gated-diode biasing scheme. To ensure reproducible results, there must be a constant time delay between the conditioning pulse and the V_{TH} measurement.

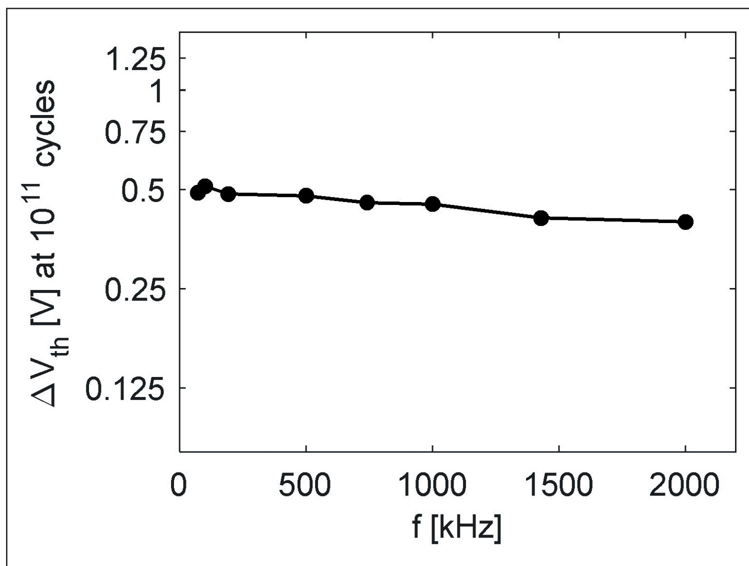


Figure 4. An exemplary threshold voltage drift after 10^{11} switching cycles, using stress frequencies between 70 kHz and 2 MHz. The resulting V_{TH} drift after the same number of switching cycles is virtually identical despite the different total stress times.

hysteresis envelope, arising from the large variety of capture and emission time constants for trapped charges in the virtually continuous defect band.

One consequence of these findings is that the 'gate biasing history' of the MOSFET can impact V_{TH} measurements for a very long time. For instance, when the device is either floating, or biased at V_{GS} = 0 V after the application of a positive or negative gate pulse, charges that are trapped near the mid-gap may be 'stored' at the interface for hours, days or even longer – this keeps the device in a state of non-equilibrium. This is a consequence of large thermal emission barriers, associated with the large bandgap of SiC. There's no similar effect in silicon MOSFETs, because they have a lower density of interface traps and a narrower band gap.

Based on these findings, we knew that the key to accomplishing a reproducible V_{TH} measurement with a SiC MOSFET was to begin by defining a 'gate biasing history'. One option is to apply a short positive gate pulse to the device, using gate voltages between the recommended use voltage and the maximum allowed voltage in the datasheet (see Figure 3). We call this technique gate conditioning. Once undertaken, V_{TH} must be measured with a constant time delay.

An easy way to accomplish fast, well-timed V_{TH} spot measurements is to use a gated-diode measurement scheme. Here, the gate and drain terminals of the device are shorted, the source terminal grounded, and a threshold current, for example 1 mA, forced. Eventually, this gate conditioning procedure creates a defined, reproducible charge state at the SiC/gate-oxide interface, and enables a defined, reproducible V_{TH} measurement. Our own research that is consistent with recent guidelines published by JEDEC has shown that more complex conditioning procedures, involving negative and positive gate conditioning pulses, also allow for reproducible measurements of hysteresis.

Having crossed the hurdle of measuring V_{TH} in an accurate and reproducible manner, we took on the next challenge: controlling and assessing V_{TH} instabilities in SiC MOSFET operations, by developing a stress procedure for determining worst-case V_{TH} drifts for different application profiles.

Worst-case threshold voltage drifts

Quality is the ability to deliver what is promised. It follows that to realise the highest quality levels and secure reliable operation of SiC MOSFETs in different applications and/or mission profiles, it is crucial to know the worst-case change in V_{TH} and other related electrical parameters over lifetime. Armed with such insight, system design engineers can consider potential variations in electrical parameters.

The most direct way to determine the variation in electrical parameters during real operation is to run full application tests and measure the condition of devices within their specified lifetimes. However, this is impractical in most cases. That's because it would be too time consuming to come to a final result, and the variety of possible applications would be far too large to be checked in individual long-lasting application tests.

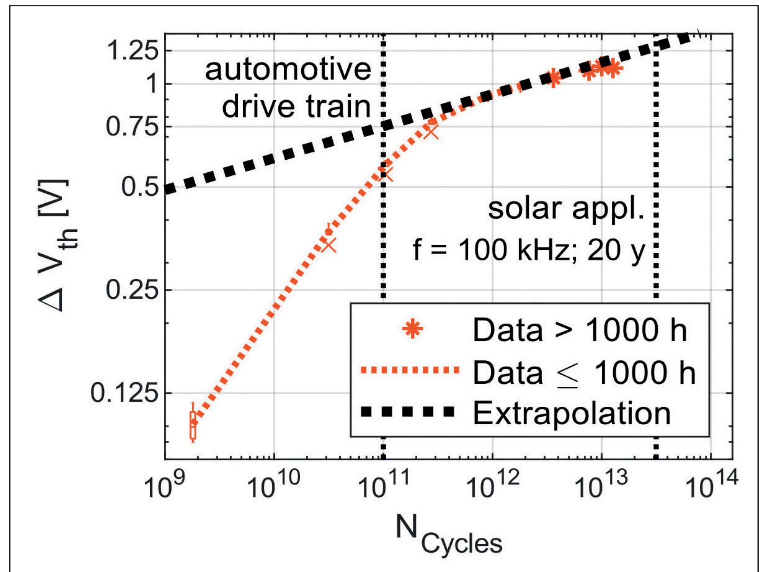
To ensure quality management while employing a practical approach, best practice is to select worst-case stress conditions and strive for stress procedures that are simplified but do not alter the degradation mechanism of interest. One of the merits of this is that all allowed application conditions are covered by one stress test. There may also be an opportunity to turn to simplified stress procedures, which might offer some potential for acceleration and parallelization.

Another way to look at this is that the ideal stress procedure should encompass all important stressors addressing a certain application-relevant degradation mechanism, but at the same time be devoid of application conditions that do not impact the final drift result, or hinder upscaling of sample size and acceleration of stress. To uncover such a unified stress procedure, we have found that it's been useful to look at common aspects of different SiC MOSFET applications and identify the main stressors.

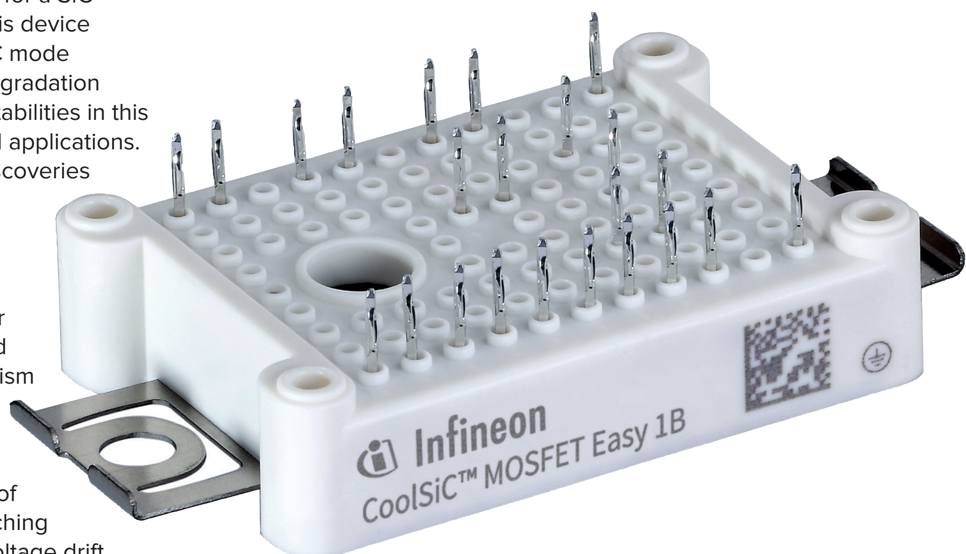
When SiC MOSFETs are used in switching applications, they are typically running at frequencies between 5 kHz and 500 kHz. As well as fast switching, there is often the need for a wide and flexible gate drive operation window, including margins for overshoots, undershoots, and negative gate turn-off voltages to allow safe turn-off. Due to this, over the lifetime of a SiC MOSFET, it is often exposed to a large number of bipolar gate switching events.

Based on the typical characteristics for a SiC MOSFET, it is expedient to stress this device in pulsed gate mode rather than DC mode when aiming to trigger the same degradation mechanisms that determine V_{TH} instabilities in this transistor, when it's deployed in real applications. Underlining this point are recent discoveries by our team, and also academic researchers working independently in China, that SiC MOSFETs show different and even enhanced parameter instabilities under bipolar gate switching conditions compared with static gate stress. This mechanism is called the gate switching instability.

Another key finding from this body of work is that for any given gate switching condition, the resultant threshold voltage drift depends predominantly on the number of gate switching events (see Figure 4). Consistent with our findings, a team in China has later independently confirmed that the total stress time and the frequency of the duty cycle is of minor or even of no importance. Drawing on this finding, it has been revealed that it is possible to determine the time evolution of V_{TH}, for a given application profile, by simply stressing devices up to their maximum number of gate switching cycles. We have shown that this can be accomplished using elevated stress frequencies of up to 2 MHz for acceleration.



➤ Figure 5. Example of worst-case V_{TH} drift evolution curve due to gate switching stress. This measurement has been made at the maximum data sheet conditions and 500 kHz. The bold dashed line (black) indicates the power law fit of data points in the saturation regime, but within 1000 hours of total stress time, corresponding to around 2 x 10^{12} cycles. Additional data points recorded up to 7000 hours of stress time (> 10^{13} cycles) confirm the validity of the power law fit.



To cover all possible applications, devices must be stressed to their worst-case conditions, using the most critical operating conditions allowed in the datasheet. This means using $V_{GS,max}$ and $V_{GS,min}$. Taking this approach also exposes overshoots and undershoots in the gate signal that may occur in the application and influence gate switching instability.

We have found that devices from different manufacturers behave differently when stressed at different temperatures. Some SiC MOSFETs drift more at lower temperatures while others drift more at higher temperatures. Due to these variations, it is far from obvious which temperature is really the worst-case for devices from different manufactures.

Through collaborative efforts, we have tested two more potentially application-relevant stressors: the drain voltage and the load current. This study revealed that neither led to altered V_{TH} instabilities. It's a negative result that is extremely beneficial, because it allows a drastic simplification of the stress procedure without neglecting any important V_{TH} stressor present in real applications.

Using a stress frequency of 500 kHz and maximum data sheet conditions for gate voltage and temperature, we have undertaken measurements that led to the plotting of an exemplary V_{TH} drift evolution curve (see Figure 5). The total stress time is 7000 hours, with stress interrupted multiple times to record the V_{TH} using the gate conditioning approach described previously. The slope of this V_{TH} drift evolution curve is higher for fewer switching cycles (< 10^{11} cycles), and tends to saturate when exceeding 10^{11} – 10^{12} switching cycles.

To assess the worst-case drift at the end of an arbitrary application profile, one must calculate the total number of gate-switching events, before either interpolating or extrapolating the V_{TH} drift evolution curve. This curve can also be used to calculate variations in other related electrical parameters, such as the on-resistance. In that case, it's worth noting that changes in V_{TH} predominantly affect the channel resistance as a component of the total on-resistance of a power device. Other components of resistance, such as those associated with the JFET, the drift zone and the substrate, are not affected by V_{TH} instabilities.

In application notes, our company has published parameter drift evolution curves that are similar to those shown in Figure 5. Drawing on this information, our customers are able to directly extract the maximum drift that can be expected for a given technology during a specific application. For instance, for automotive drive applications, the total number of switching cycles until the end-of-application profile is relatively low, typically around 10^{11} cycles. This allows the maximum V_{TH} drift to be directly read from raw data, shown in Figure 5.

However, for solar applications, which feature operation under frequencies of typically 70–100 kHz during daylight hours for 20 years or more, data must be extrapolated, because a real end-of-application profile test would lead to an unreasonably long stress time. The curve to be used for this power law extrapolation is shown in Figure 5.

In short, drawing on our efforts to increase our understanding of trapping dynamics at the SiC/gate-oxide interface, we have gone on to develop new characterisation and stress procedures that are tailored to the characteristics of the SiC MOSFET.

These new methods provide standardized, reproducible measurements, as well as realistic assessments of time-dependent parameter variations in real applications. In turn, this allows engineers to predict how device characteristics will evolve during an application, and paves the way for SiC MOSFETs to reach their next level of quality excellence.

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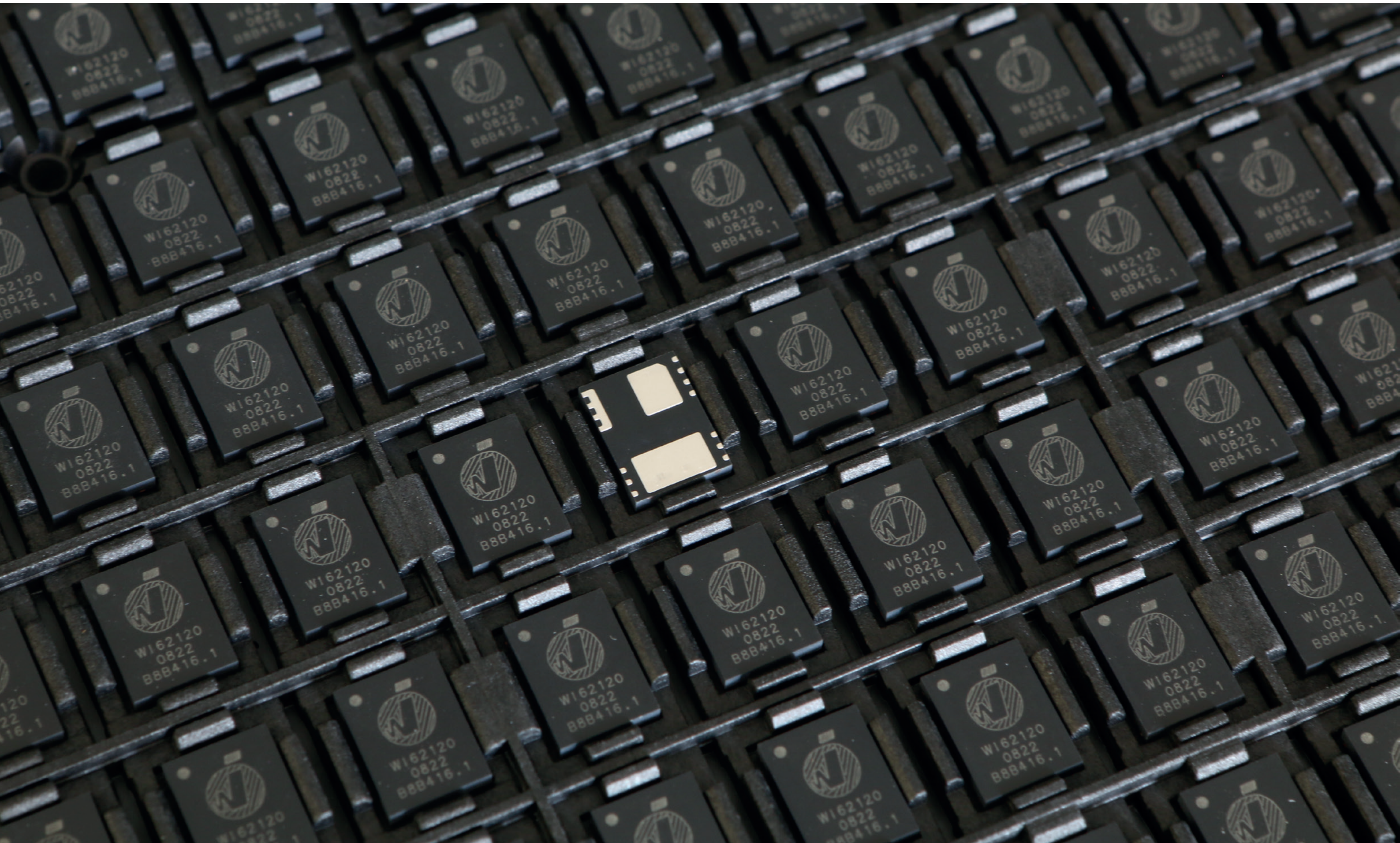


Now's the time to commercialise the GaN IC

Power ICs that combine several power electronics functions in a single GaN chip are set to play a major role in worldwide electrification.

BY GERALD AUGUSTONI, PLINIO BAU, DOMINIQUE BERGOGNE, FLORIAN COUVIN AND RYM HAMOUMOU FROM WISE INTEGRATION

POWER CONVERSION SYSTEMS are at the heart of most electronic equipment, from home appliances and laptops to data centres and electric vehicles. In some of these applications GaN technologies will soon be essential, because silicon has hit its physical limits as a power-conversion platform.

As well as increasing the efficiency of power conversion stages, GaN has other virtues. They stem from its great physical properties, such as: a bandgap of 3.2 eV, nearly three times that of silicon; and a breakdown field of 3.3 MV/cm, which is around ten times that of silicon. These strengths contribute to excellent values for both the on-resistance and the key figure of merit – the product of the on-resistance and the surface area of the chip. GaN devices can deliver high currents, a high breakdown voltage and a high switching frequency, and are competing with current MOSFETs and super junction MOSFETs in power applications operating at voltages of up to 650 V.

Traditionally, power designers build half-bridge circuits that serve in power conversion systems from discrete transistors and a number of external components, such as drivers, level shifters, sensors, bootstraps and peripherals. Improvements can be realised by combining discrete GaN devices, rather than those made from silicon, with other components. However, there is a better approach than this – one that we are pursuing at Wise Integration, which is based in France. Founded in 2020, our team is pioneering the GaN power IC, which combines several power electronics functions in a single GaN chip. Through integration, we are improving speed, efficiency, reliability and cost-effectiveness.

More agile adapters

Over the past decade, major OEMs have devoted much effort into making the most powerful smartphones, the thinnest notebooks and the largest TVs. The common factor in this trend is the growing demand for power, to enable sharing of a massive amount of data every second.

Unfortunately, OEMs have not been paying much attention to the adapters placed next to their products. This has resulted in bulky, heavy, inefficient power supplies that rely on silicon transistors. But that is starting to change.

Back in 2019, GaN technology penetrated the consumer market, initially in 30-100 W adapters. Since then this wide bandgap technology has spread widely, evolving as a next-generation power-conversion option. Today, most makers of mobile devices acknowledge that adapters are part of the equation, with mobility requiring them to be compact and lightweight, in tune with their main product strategy. Power supplies are now becoming an integral part of the product.

Power density is the main 'driver' for GaN, while efficiency is becoming increasingly important to meet new demand for AC-DC/DC-DC power supplies from 100 W to 3 kW, especially for the data-centre industry. For this specific market, higher power is required in the same form factor to reach high levels of efficiency.

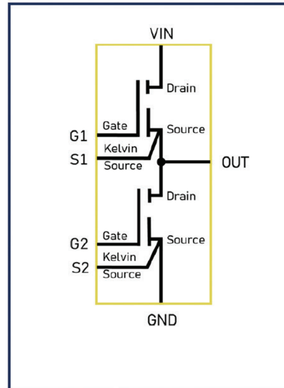
GaN had a great year in 2022. Along with its growing popularity it became cost competitive, with expanding demand prompting several global foundries to add GaN lines. At the system level, it will not be long before AC-DC analogue controllers are 'GaN compatible'. However, their GaN capabilities will not be fully utilised, because they are still switching at low frequencies.

Now is the time for the GaN industry to start overcoming this limitation and deliver the next big energy and power boost. This can come from a move from discrete GaN devices to GaN ICs that deliver a hike in efficiency at the system level, and lead to material costs that are more competitive than traditional silicon-based power supplies.

GaN IC design

To see this vision fulfilled, we have been prototyping different HEMTs, using different form-factor and metallisation strategies. Our efforts have involved the modelling and design of GaN transistors for 100 W to 1 kV applications using multi-project wafers. These investigations have drawn on expertise at CEA-Leti, the French microelectronics research institute. Through this collaboration we have obtained a solid basis for mass production.

Among all the multi-project wafers and prototypes we have built, we have undertaken R&D projects that are focused on power transistor layout topologies. From matrix metallisation to comb metallisation, we have uncovered parasitic contributions from the metal paths that affect performance parameters, leading to different values for parasitic capacitance, on-resistance and gate internal resistance. We have found that the pad positioning in the floorplan diagrams impacts the parasitic on-resistance caused by the bonding wires, as well as the distribution of current and metal resistance calculated by metal squares. Changing the bonding wires' position in the power IC floorplan impacts the final on-resistance in two ways: post-layout simulation and performance parameters change, due to variation in current distribution inside the metallisation; and the addition of bonding wires in parallel impacts the final resistance. Over the past two years we have built hundreds of prototypes, selecting the best ones. We have also performed electrostatic discharge (ESD) tests on: prototypes for different circuit strategies, circuits with diodes, digital input/output clamp and power clamp circuits.



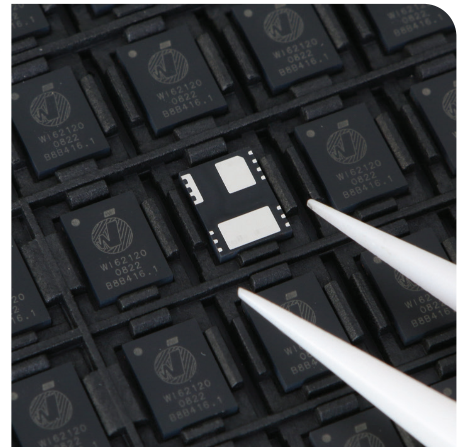


Figure 1. WiseGan half-bridge.

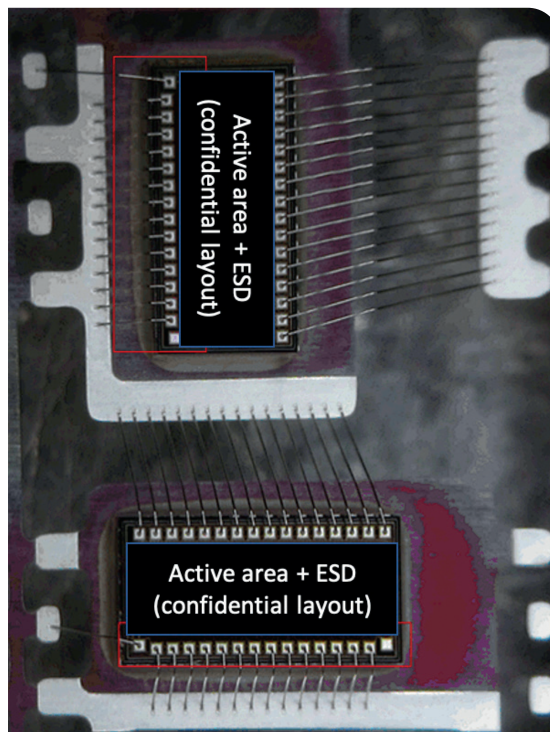


Figure 2. Integrated half-bridge transistors composed of a low-side and a high-side power switch in the same package.

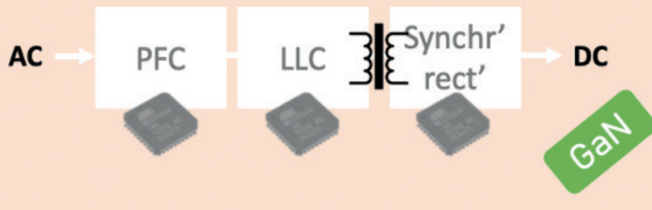


Figure 3. Typical GaN-based power supply with analogue control.

When our community gathers at international conferences, along with discussions of power transistors, there are conversations related to analogue circuits for GaN power integration. To obtain high-performance circuits, it is clear that there's a need to overcome fabrication-corner dispersion and a charge-trapping effect. Another impediment is the absence of *p*-type transistors for pull-up circuits. However, designers can overcome these challenges by adapting their circuit topologies. Many have demonstrated analogue circuit blocks, such as voltage reference, under-voltage lock-out, ESD circuits, comparators and operational amplifiers, with high switching frequencies of up to 10 MHz. These blocks are also compatible with voltages up to 650 V and powers of up to 1 kW.

System-level benefits

An entrenched factor that limits the performance of systems that employ silicon MOSFETs is the figure of merit for this transistor – it is the product of its on-resistance and the combination of its internal gate-to-source and gate-to-drain capacitance. Moving from silicon to GaN allows designers to enjoy a far better figure-of-merit. There's no longer a limit to the operating frequency, which can be ten times that of silicon.

However, it's not as simple as it first appears, as there's another obstacle to raising the system frequency. If the GaN transistor in the converter is not operating in a soft switching condition – that's the situation where the voltage at every turn-on of the transistor is close to zero, or otherwise limited – the energy stored due to the capacitance of transistor, as well as the system capacitance, has to be dissipated in GaN, causing the transistor to quickly overheat. While this may be acceptable for systems operating at 100 kHz or below, it is not for frequencies from 500 kHz to 2 MHz, the typical operating frequencies of our systems.

Our solution is to constantly operate in a soft switching condition, accomplished by specific control and topologies. To ensure that this is possible for everyone, we have launched WiseWare controllers (see Figure 4).

Driving forces

The GaN IC is destined to be the next step on the road to high power density and system integration, two of the key drivers behind the historical success of semiconductors. But power electronics, and power transistors in particular, have lagged in integration, held back by the complicated processes employed for forming vertical architectures.

We are in no doubt that the integration offered by our GaN lateral process will deliver benefits at the system level. Realising integration is a crucial step forward, as it always enables a reduction in system dimensions and an increase in complexity, which improves reliability and performance.

Our GaN ICs will bring benefits to market, because they enable: a shrinking of system dimensions, by reducing the number of components and minimising power losses, which leads to practical packaging for heat transfer; increased complexity, which can lead to optimised system performance, including better shaping of the power signal; improved reliability, thanks to fewer components on the board, and additional system protection that

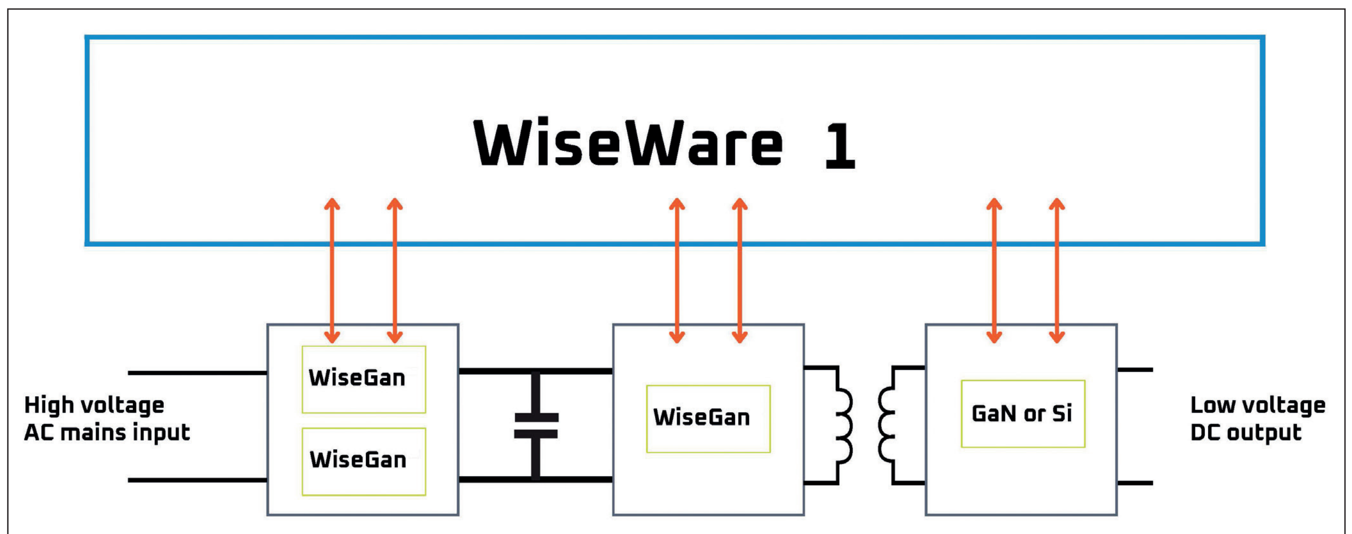


Figure 4. WiseWare 1 digital control.

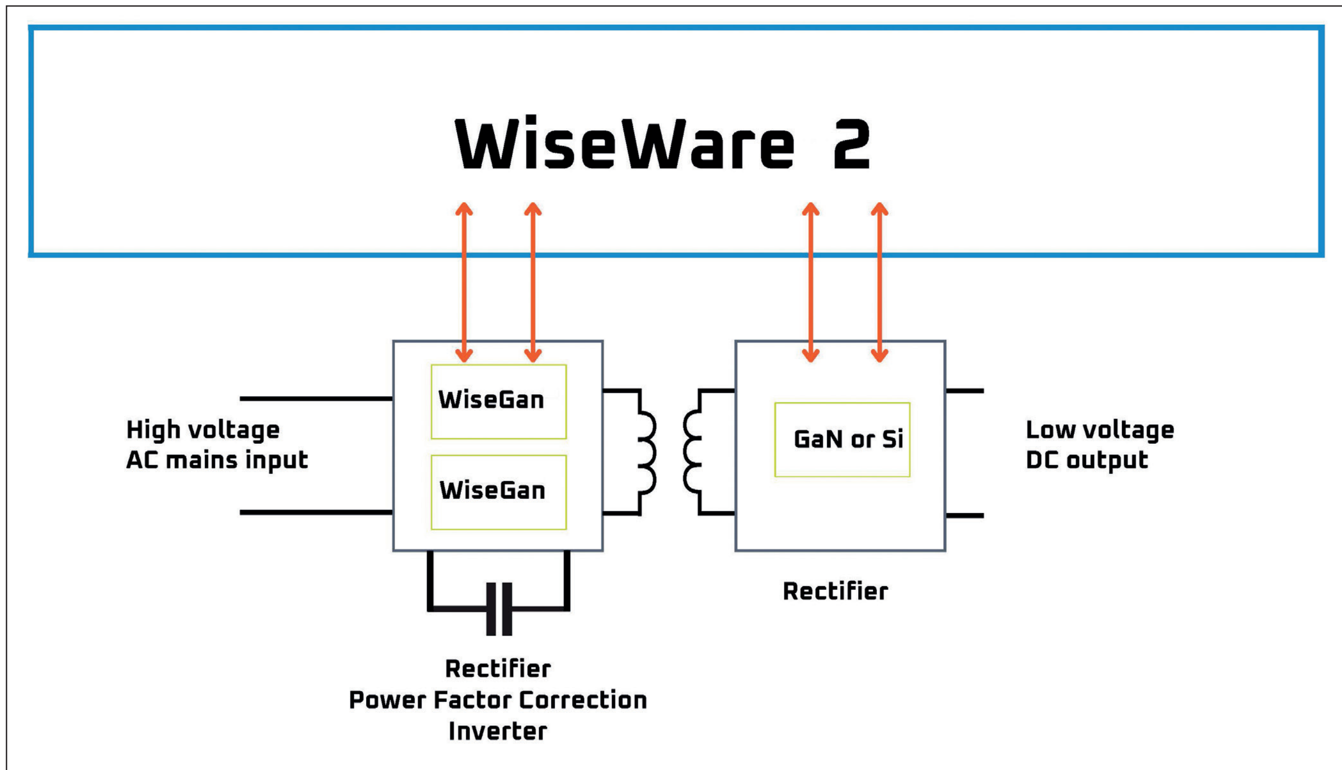


Figure 5: WiseWare 2 digital control.

includes early detection of abnormal conditions; and better performance with faster switching devices, thanks to driver integration. The latter enables a higher operating frequency, by reducing parasitic components and ensuring better switching behaviour. In addition, there is the opportunity to introduce 'in-power sensing', to feed the true status of the converter back to the controller through sensors integrated on the power transistor die.

Of course, this evolution requires several steps. However, such efforts are worthwhile, as they provide the main driving force to the future of the GaN market. While progress may span several decades, the result will be a revolution in system design, so that it delivers unmatched performance at low cost.

Digital control

Digital GaN is a promising option for realising great performance with GaN ICs. It is a disruptive approach to digital control. No longer are analogue signal blocks 'translated' into digital blocs, while the functions of the GaN IC and digital GaN controllers are partitioned in such a way that each part boosts the other part's performance. Current sensing is usually complex to achieve, but the digital GaN solution makes the analytical estimation of the current possible, thus creating a virtual current sensor. Such a sensor, which costs only lines of code, prevents losses, saves PCB area, reduces the bill of materials and eliminates analogue sensor problems (see Figure 5).

Another advantage of digital GaN is that it elevates high resolution pulse-width modulation to a level that cannot be reached with analogue controllers. By opening up the opportunity for a precise sub-nanosecond timing resolution, combined with high-performance microcontroller units (MCU), new solutions are introduced for zero-voltage switching – this is a technique that reaches extreme high switching frequencies without increasing switching losses, thanks to what is called 'soft switching'. By computing exact switching times, a digital GaN controller can perform zero-voltage switching using

Digital GaN is a promising option for realising great performance with GaN ICs. It is a disruptive approach to digital control. No longer are analogue signal blocks 'translated' into digital blocs, while the functions of the GaN IC and digital GaN controllers are partitioned in such a way that each part boosts the other part's performance

low-bandwidth hungry sensors and a model of the switching device.

Note that the high-frequency, switched-voltage waveforms are not measured or sensed. Instead, slow-changing variables are fed to the MCU analogue-to-digital conversion peripheral.

Digital GaN opens new pathways from the power stage to the cloud, helping to combat climate change by drastically reducing the amount of data exchanged. Sitting at the heart of power supply units and power converters, digital GaN can aggregate performance data from the power circuits to compute health-and-usage data. An ultralow bandwidth data flow can be generated by processing the data onboard: it requires just a few kilo-bytes per day to provide optimal information for monitoring huge installations using a massive quantity of power supply units.

By providing an intelligent link between the world of data and the world of electrical power, digital GaN enables remote-firmware updating, as well as feature activation over the internet. This possibility is common in many computing devices, such as internet boxes, TVs and computer mainboards. There is also the opportunity to deliver power and data to EVs.

For power supply systems that serve data-hungry needs that are as diverse as consumer electronics, e-mobility, data centres and industrial applications, there will be increasing pressure to deliver the vast amounts of power required to transmit that data. Helping to meet that demand are our GaN ICs that combines several power electronics functions in a single GaN chip. The payoff: improved speed, higher efficiency, greater reliability and cost-effectiveness, alongside a digital control that opens new paths from the power stage to the cloud, while respecting the environment by drastically reducing the amount of data exchanged.

FURTHER READING

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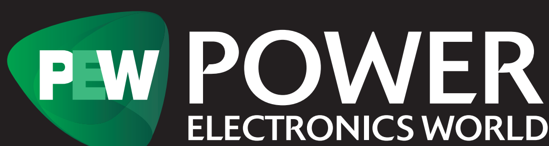

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Multi-dimensional power devices

Advancing power electronics is not all about new materials. Architectures really matter, with the likes of superjunctions, multiple channels and multiple gates offering the opportunity to revolutionise power devices

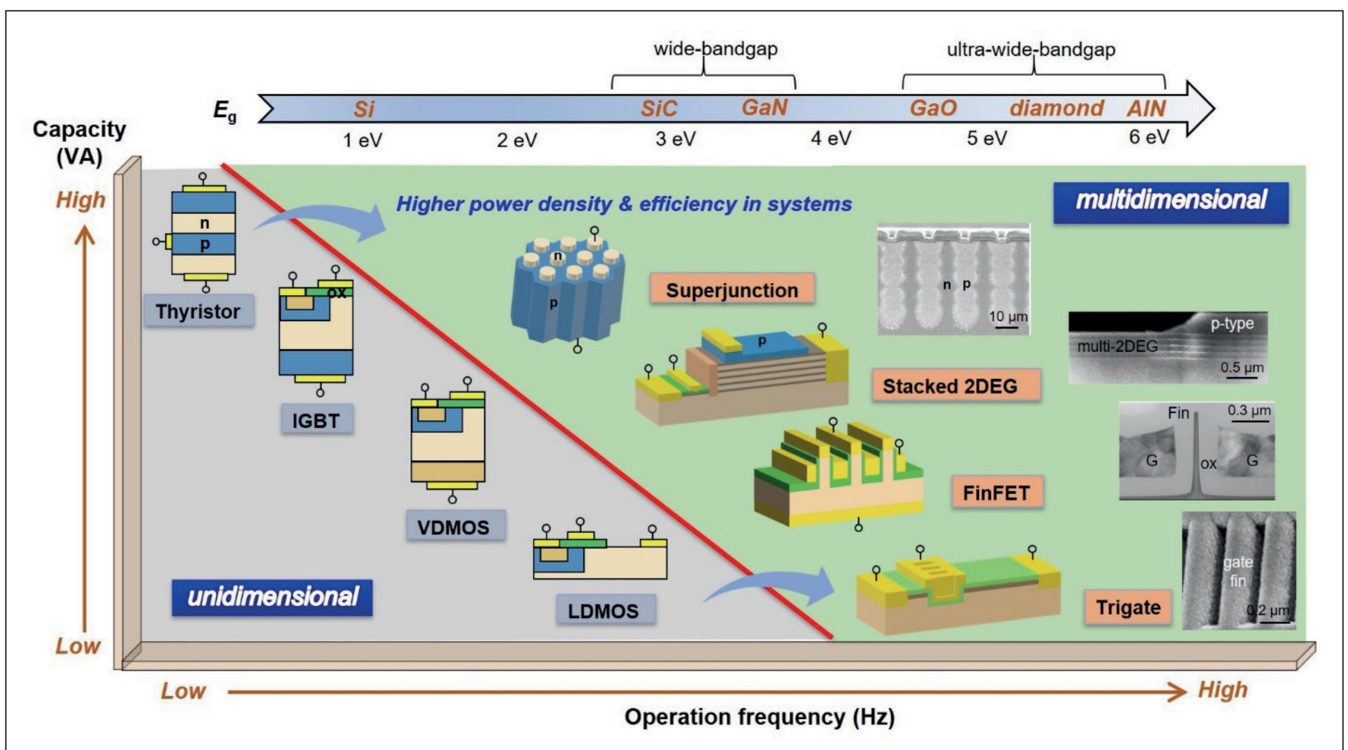
BY YUHAO ZHANG FROM VIRGINIA TECH

POWER ELECTRONICS is key to realising high-efficiency energy conversion in various applications, including data centres, electric vehicles, electric grids and renewable energy processing. The global market for power semiconductor devices and ICs is already worth $40 billion per annum, and it is rapidly increasing.

Many working in this sector hold the belief that to advance power devices there's a need to introduce new materials. Transistors made from silicon should be replaced by those made from wide-bandgap semiconductors, such as SiC and GaN, and there will come a time when it's right to move on to ultra-wide-bandgap variants, such as Ga_2O_3, AlN and diamond.

But my view, shared by colleagues including Florin Udrea of the University of Cambridge and Han Wang of the University of Southern California, is that innovation in device concept and architecture is equally important – and such innovation is material agnostic. This has led us to publish a roadmap late last year for device architecture innovation (for the details of that paper, see Further Reading).

History supports our position. Just track the evolution of silicon power devices before the advent of wide bandgap materials. During that era, innovation in device architecture drove the development of power electronics, from the commercialisation of thyristors in the 1950s to the power MOSFETs of the 1970s and the insulated gate bipolar transistors (IGBTs) of the 1980s. We believe that a new wave of power devices hinges on the introduction of multi-dimensional architectures.



➤ Figure 1. Power capacity and frequency trade-off of 1D and multi-dimensional power devices.

The role of the power device is to conduct a high current in its on-state, block a high voltage in its off-state, and be capable of continuously switching between these two states at a high frequency. For conventional power devices, such as MOSFETs and IGBTs, the main current flow and the blocking electric field are aligned in same direction, rendering them as effective uni-dimensional devices.

Recently, several innovative architectures have been developed that introduce electrostatic engineering in at least one additional geometrical dimension. Such architectures include super-junctions, multiple channels and multiple gates. Depicted in Figure 1, these multi-dimensional devices overcome the capacity-frequency trade-off that holds back the performance of their conventional cousins, enabling them to realise a lower power loss and a higher frequency. Armed with these attributes, designers can enhance the efficiency of their power electronics systems, while reducing the form factor.

Unipolar power devices are also hampered by another trade-off that fundamentally limits their performance: the relationship between the breakdown voltage and the specific on-resistance. As shown in Figure 2, when multi-dimensional devices are made in silicon, SiC and GaN, they can surpass their respective 1D material limits. What's particularly encouraging is that their performance can be continuously enhanced by scaling certain structural parameters. This has spawned a new band of device limits, beyond the 1D limit line for each material. In stark contrast, most 1D unipolar power devices gain little improvement with geometrical scaling. Hence, there's a compelling need to re-write the performance limits and the figures of merit for multi-dimensional power devices.

For superjunction devices, the electric field is modulated in a plane that's perpendicular to the direction of current conduction. This class of power device is formed by creating alternating *n*-type and *p*-type regions. Charge balancing leads to a uniform electric field and a superior blocking voltage, regardless of the doping in each region. With this architecture, the doping level can be increased by orders of magnitude, slashing on-resistance.

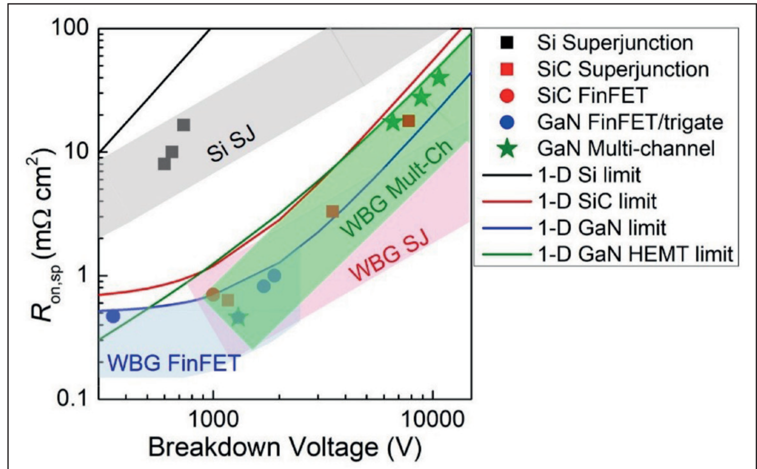


Figure 2. Specific on-resistance and breakdown voltage trade-off of 1D material limits and multi-dimensional power devices demonstrated in silicon and the wide-bandgap semiconductors SiC and GaN.

Since the introduction of CoolMOS in the late 1990s by Siemens, now Infineon, the silicon superjunction has been a spectacular commercial success. And in 2016, the superjunction family welcomed a new member, in the form of SiC, with this device exceeding its 1-D performance limit.

For GaN, breakthroughs coming from the introduction of new architectures have included the development of devices with multiple two-dimensional carrier channels aligned perpendicular to the plane of current conduction. In such devices,

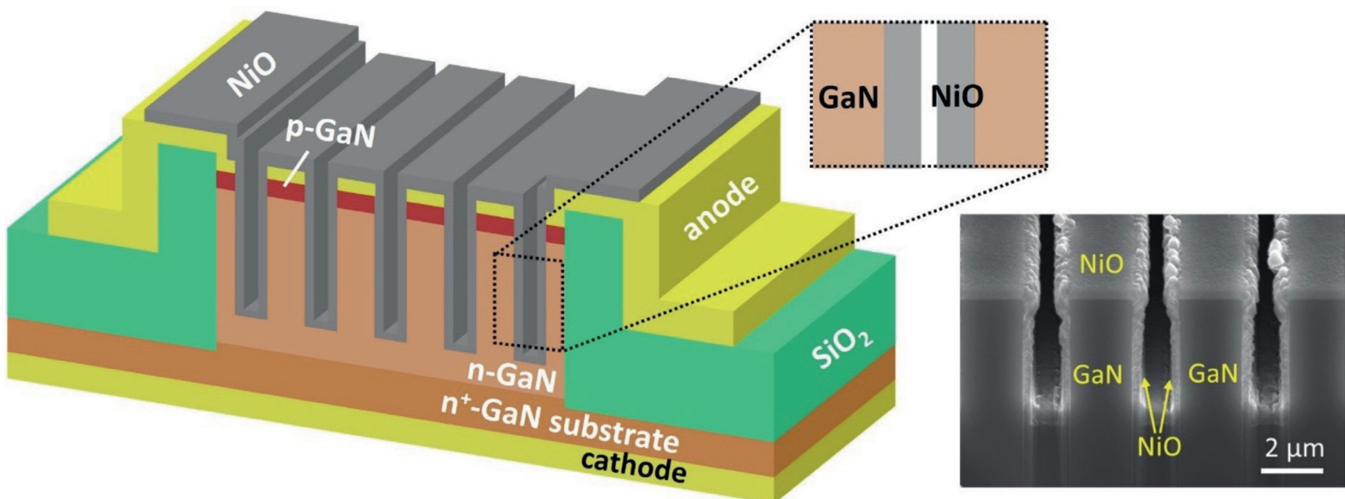


Figure 3. 3-D schematic of the vertical GaN superjunction diode and the zoom-in illustration of a NiO/GaN unit-cell (left). Cross-sectional scanning electron microscopy image of the superjunction region (right).

the polarisation charges, as well as a possible additional *p*-type cap layer, can be self-balanced in the device off-state, fulfilling a functionality similar to that of a superjunction. Using this approach, our teams at Virginia Tech, University of Southern California, and University of Cambridge, have demonstrated multi-channel AlGaN/GaN devices blocking 10 kV, a performance that exceeds the limit of 1D lateral GaN devices.

For transistors operating below a kilovolt, the channel resistance can dominate the device's on-resistance. To slash resistance, device designers can turn to multi-gate architectures and submicron fin-shaped channels. The fin is a particularly attractive option, as it shifts carrier transport away from the low-mobility surface channel, thereby increasing the overall channel mobility.

This approach is widely applicable, with trigates and FinFETs demonstrated in various power transistors, including MOSFETs and HEMTs, using multiple materials.

Late last year, working with additional collaborators, our teams broke new ground, unveiling the first vertical superjunction in GaN. This success, unveiled at the 2022 International Electron Devices Meeting, builds on the heterojunction with *p*-type NiO, which was sputtered conformally on the sidewalls of the GaN pillars (see Figure 3). Thanks to charge balancing between NiO and GaN, our superjunction provides a blocking voltage of 1100 V and a specific on-resistance of 0.15 mΩ cm^2. This level of performance exceeds the 1D limit for GaN.

While we have illustrated the benefits of multi-dimensional architectures to power devices, the gain they can deliver can also be enjoyed elsewhere. For radio-frequency devices, they can deliver improvements in power, frequency, and dynamic range.

Note that we are not disputing the benefits that can be wrought be introducing new semiconductor materials. But the next time you need to build a better device, don't just think about switching materials – also consider what might be possible with a refined architecture.

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- Y. Zhang *et al*. "Multidimensional device architectures for efficient power electronics," Nat. Electronic. **5** 723 (2022)
- M. Xiao *et al*. "First demonstration of vertical superjunction diode in GaN," 2022 International Electron Devices Meeting (IEDM), 35.6, Dec. 2022.

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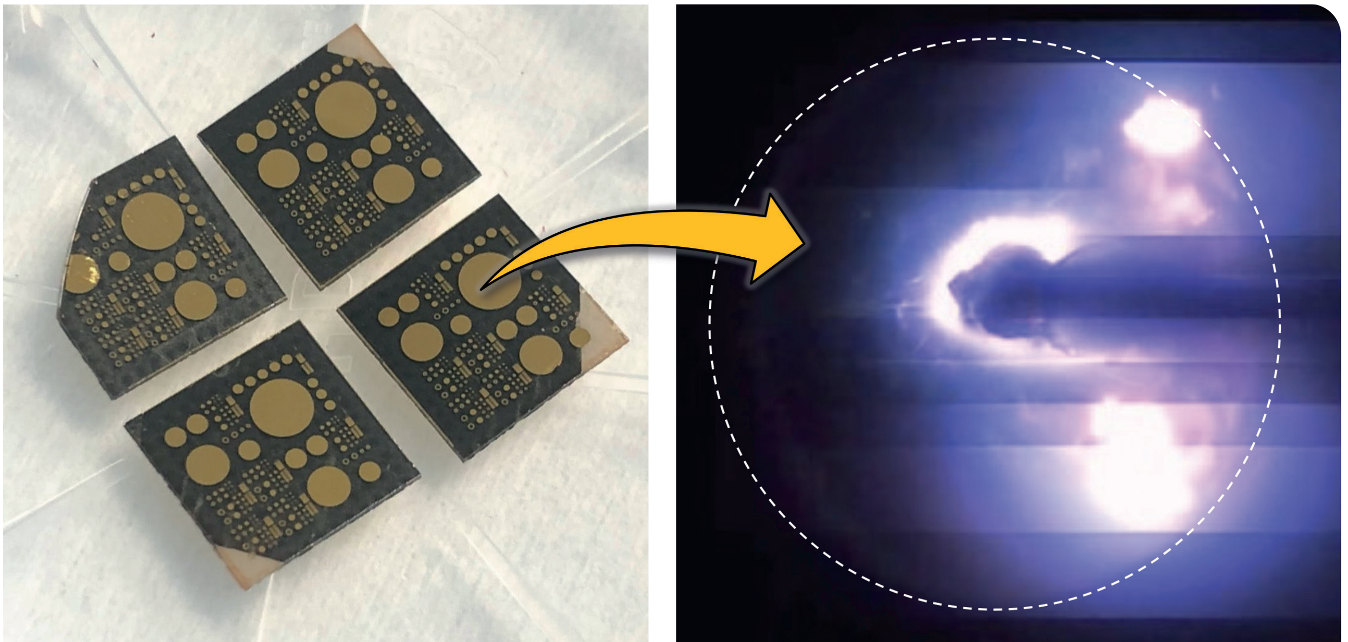


GaN diodes with uniform, robust avalanche

A multi-faceted endeavour, starting with material growth and extending all the way to circuit-level investigation, ensures uniform, robust avalanche in GaN vertical power diodes

BY BHAWANI SHANKAR AND SRABANTI CHOWDHURY FROM STANFORD UNIVERSITY

IN EVERY power electronic system, it is the power devices that provide the building blocks. When these semiconducting devices, often diodes and transistors, are used in power electronic circuits, they are often placed in series with inductive loads, such as a motor or a discrete inductor.

In this configuration, when device switching occurs, there's an interruption to current flow through the series inductor – and this generates a voltage transient, appearing across the device terminals (see Figure 1). If the voltage transient exceeds the breakdown voltage of the device, this poses a threat to damage the device.

To prevent failures from such overvoltage scenarios, device engineers tend to design power devices with extra headroom in the breakdown voltage. But there are penalties to pay: a higher on-resistance, leading to an increase in conduction losses; and a higher device manufacturing cost, stemming from a hike in semiconductor estate associated with the larger drift region volume needed to hold the higher voltage.

Combatting this concern are semiconductor devices with an avalanche capability, which have an inherent overvoltage protection. When such devices face overvoltage transients in a circuit, they undergo avalanche breakdown and generate micro-plasma or current filaments that bypasses the electrical stress and protect the device.

Fortunately, one of the most promising materials for the future of power electronics, GaN, possess avalanche capability. However, despite more than three decades of exploration of this wide bandgap semiconductor as a mainstream device material, reports of its avalanche breakdown are limited to devices that have been grown on native GaN substrates.

Achieving uniform avalanche

This limitation may raise a few eyebrows, given that any GaN-based device with an intrinsic *p-n* junction should show avalanche behaviour, so long as it has been designed correctly. But there are valid reasons why there are so few reports of experimentally realising this phenomenon, and why it took until

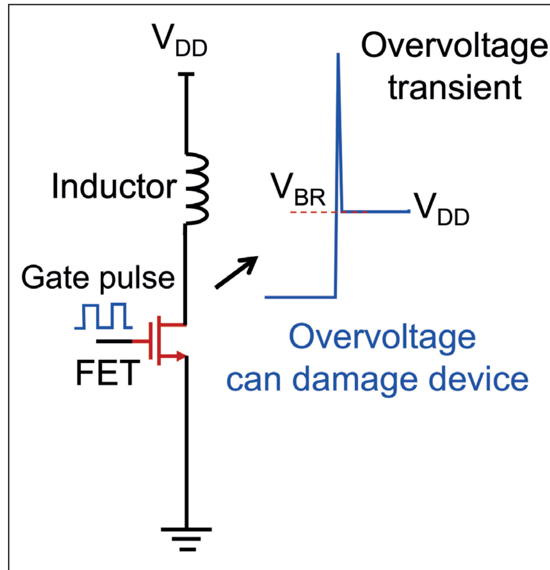
➤ Left: Dies with GaN vertical *p-n* diodes of various diameter, fabricated in the Wide-Bandgap Lab at Stanford University. Diodes of voltage class 1.2 kV and 3 kV with robust avalanche are successfully developed and tested.

2013 to first see this behaviour. The long wait occurred because effort is required on several fronts to realise avalanche breakdown – there's a need for high quality material, very precise device design and well-optimised processing. Regarding the first of these requirements, one pre-requisite for realising avalanche breakdown in GaN devices is a defect density below 10^6 cm^{-2}.

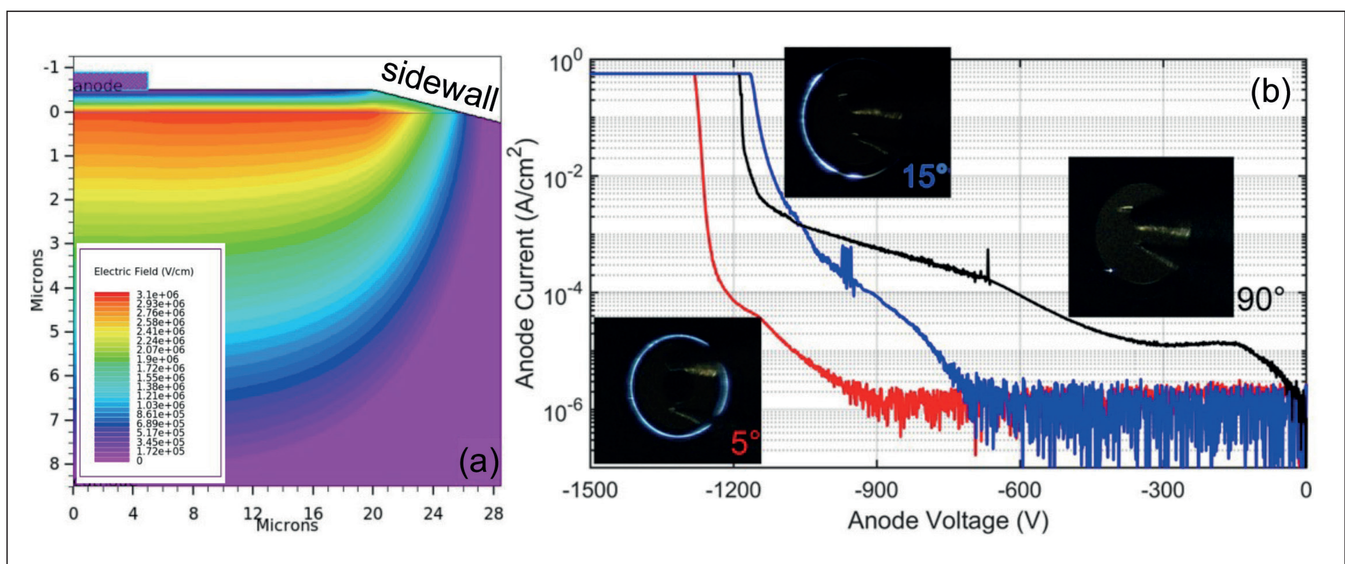
When it comes to device design, as avalanche breakdown is an electric-field-driven phenomenon, electric field management is crucial to realise this mode of operation. However, it is nearly impossible to achieve an avalanche breakdown mode in GaN-based lateral device geometries, such as HEMTs and lateral *p-n* diodes, because they tend to suffer from premature failures, either from corner effects, which cause local field enhancement, or from excessive buffer leakage at high voltages.

In marked contrast, GaN-based vertical devices offer better field management, higher current density, and a superior area efficiency than their lateral counterparts. These merits are behind the demonstration of GaN vertical *p-n* diodes with an avalanche breakdown voltage of up to 6 kV, reported in 2022.

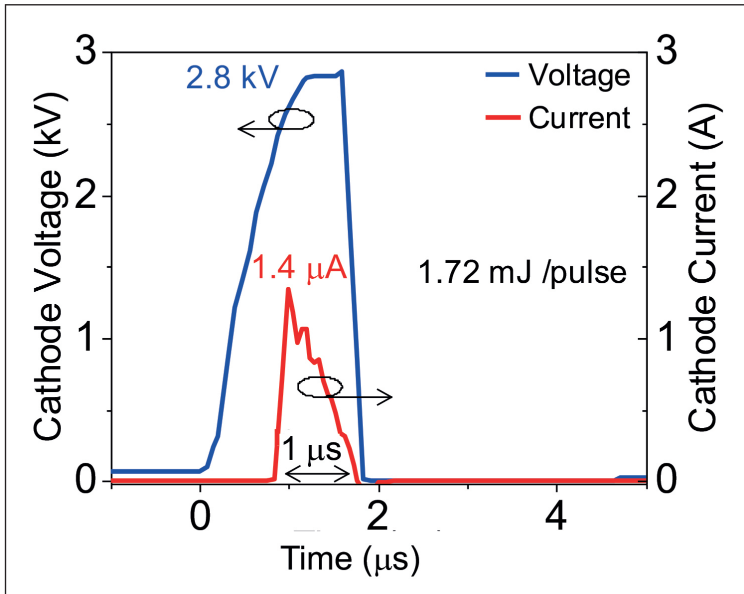
Given that the development of high-performance avalanche GaN diodes is still a work in progress, it's not surprising that there are relatively few reports of experimental investigations of this device. Most testing has been undertaken using DC conditions, with studies considering the temperature-dependent reverse characteristics of diodes to verify a positive temperature coefficient of breakdown – this provides proof of avalanche behaviour. However, observing this trait under DC test is no guarantee of reliable, repeatable avalanche operation in a real application.



➤ Figure 1. A power MOSFET in series with an inductor experiences voltage overshoot during switching. If the FET is not avalanche capable, the overvoltage can cause device failure. To avoid premature failures, typically the device is overdesigned for a breakdown voltage (V_{BR}) higher than required.



➤ Figure 2. Avalanche breakdown study for a 1.2 kV GaN vertical *p-n* diode. (a) Bevel termination redistributes the electric field, triggering avalanche mechanism in the bulk GaN. (b) Reverse characteristic of the diode studied at different bevel angles. A uniform electroluminescence (light emission) occurs at breakdown in the diode with a 5 ° angle, exhibiting 1.2 kV avalanche breakdown voltage.



➤ Figure 3. Current and voltage waveforms of a 3 kV GaN vertical *p-n* diode during avalanche breakdown. The diode voltage clamps and a high current flows from cathode to anode in avalanche mode.

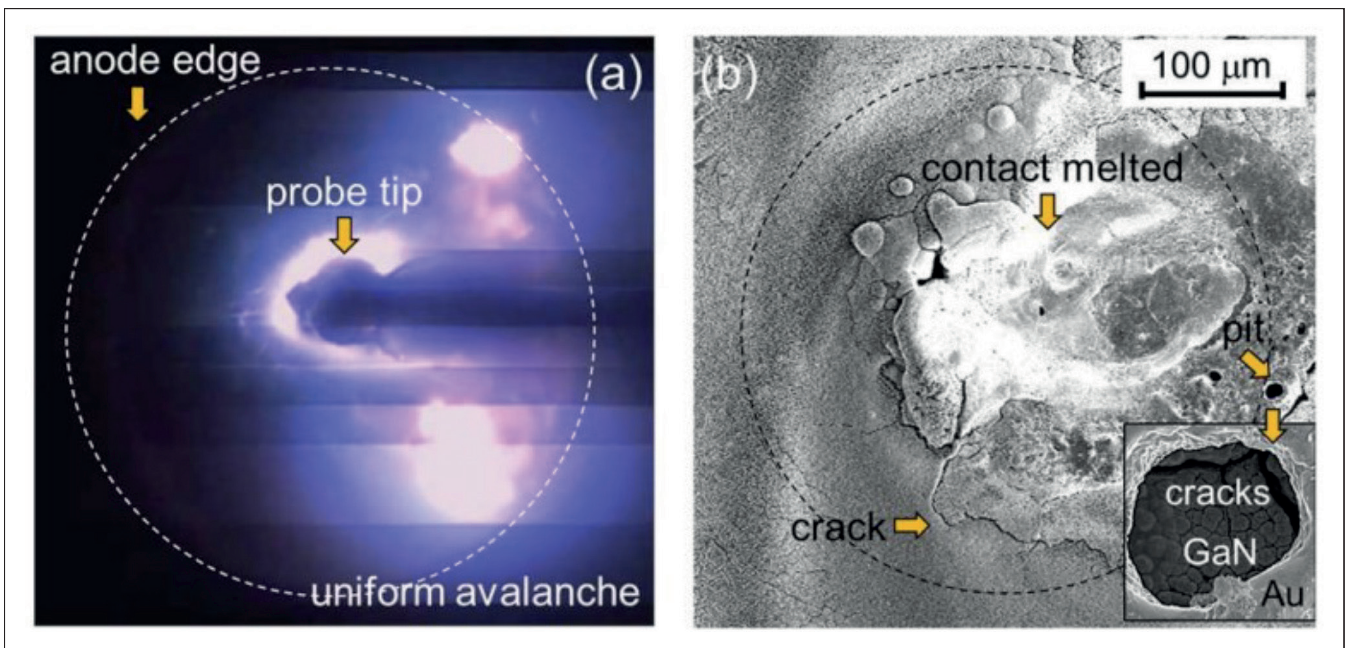
Our group, the Wide-Bandgap Lab at Stanford University, is breaking new ground by investigating the various factors that can guarantee uniform, repeatable avalanche in GaN vertical devices. We have embarked on a multi-faceted endeavour, beginning with material growth and extending all the way to circuit-level characterisation.

Fabrication of our vertical *p-n* diodes starts with the growth of an epi-structure on GaN substrates with an ultra-low defect density – it is less than 10^6 cm^{-2}. We carefully selected the doping profile and its concentration to ensure a uniform electric field distribution in devices, key to a uniform avalanche. Employing optimised *p*-type doping, with a magnesium doping concentration of 3×10^{17} cm^{-3}, resulted in an avalanche breakdown voltage of 1.2 kV.

We have devoted much effort to developing diode designs that avoid the high charge density at device corners and edges, as such features locally enhance the electric field, thereby introducing non-uniformity. To suppress local field peaks and unify the field distribution, we have employed edge-termination techniques, such as bevel and field plate.

Evaluating edge termination efficacy

For this part of our study, we considered a range of bevel angles from 0 ° to 90 °. We found that diodes produced the most uniform avalanche breakdown with a 5° bevel, for a *p*-type doping concentration of 3×10^{17} cm^{-3} (see Figure 2). Higher levels of doping required a higher bevel angle, leading to a lower breakdown voltage in the device. We have found that in general, a bevel is more effective up to 3 kV. It's worth noting that a bevel termination carries an area penalty: the smaller the bevel angle, the shallower the slope, hence the need for a greater area to realise the device. Due to this, a bevel alone cannot offer breakdown voltages higher than 1.2 kV. To overcome this limitation, a bevel should be combined with other edge terminations. Adopting this approach, we fabricated GaN diodes possessing both a bevel and a field plate at the anode and showed an avalanche breakdown voltage of up to 3 kV (see Figure 3).



➤ Figure 4. (a) Uniform electroluminescence, hence uniform avalanche breakdown, observed in a 1.2 kV GaN vertical *p-n* diode under unclamped inductive switching stress. (b) After several thousand avalanche pulses, the diode eventually encountered thermal failure.

A significant difference between the design of our 1.2 kV and 3 kV diodes is that the latter incorporates a spin-on-glass, which passivates the diode surface and acts as a field plate dielectric. For the 1.2 kV diode, it is the SiN that provides passivation at the surface and sidewalls. This form of passivation is unsuitable at voltages above 1.2 kV, as SiN on the bevel sidewalls becomes leaky.

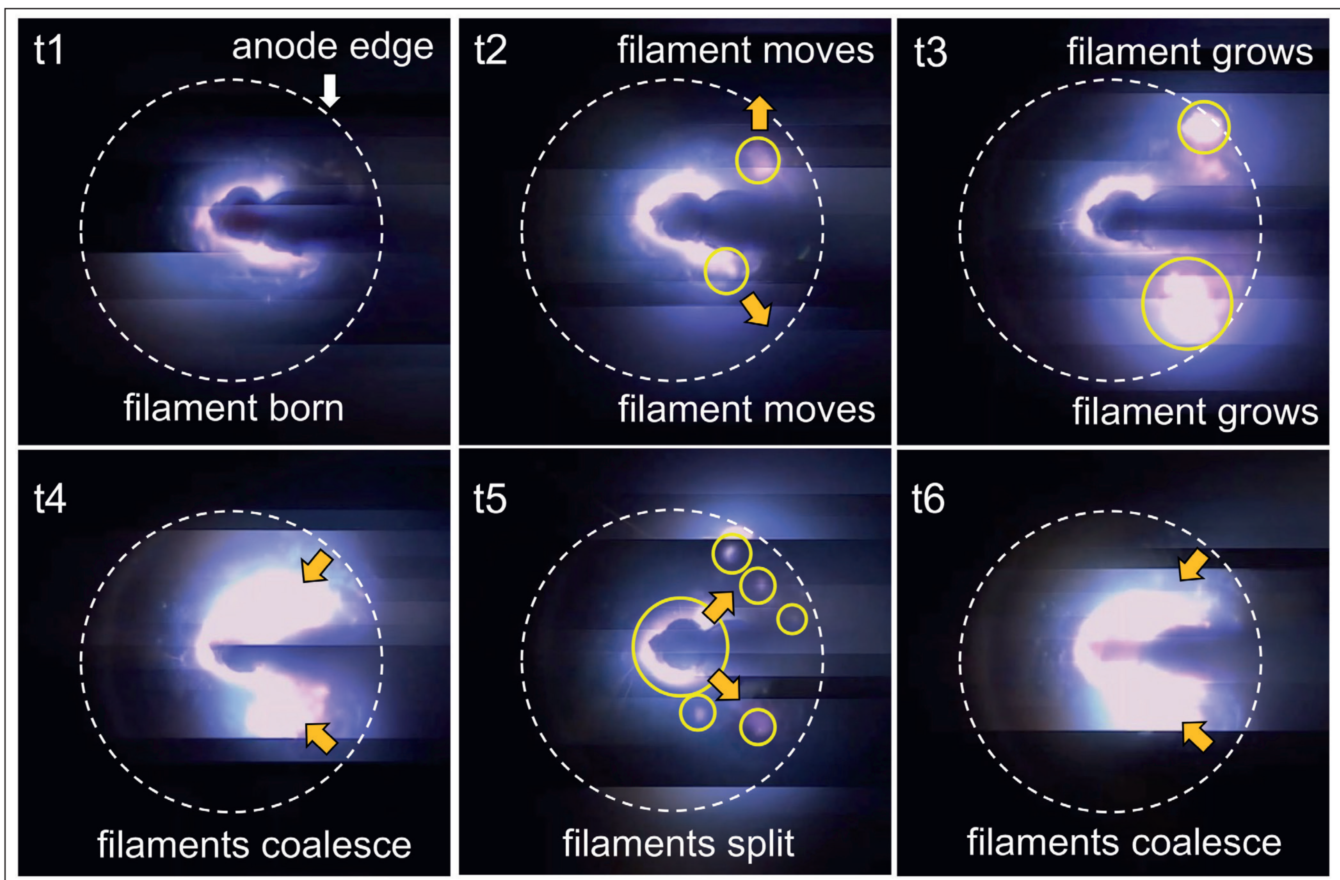
One technique offering great insight into avalanche behaviour is spatially resolved electroluminescence. When avalanche occurs, there is band-to-band and defect-mediated recombination of free electron-hole pairs at breakdown, giving rise to electroluminescence. We have turned to spatially resolved electroluminescence to investigate the efficacy of edge termination in our 3 kV GaN vertical *p-n* diode. We found that electroluminescence emission remained localised at the field plate corner and eventually the diode failed after few avalanche cycles.

Subsequent failure analysis revealed damage to a portion of the field plate under intense heating associated with the avalanche current. This investigation also found that the diode had been compromised by cracking and peeling of the field plate dielectric, due to the thermal stress. On the otherhand, the 1.2 kV diode had more robust bevel termination and the diode could attain uniform avalanche which eventually led to uniform thermal failure (see Figure 4). We have concluded from these observations that there's much need for robust edge termination, which is trustworthy during intense avalanche events involving high currents, high voltages, and tremendous self-heating within the device.

Avalanche robustness?

There is an established approach to evaluating a device's avalanche robustness, involving measurement of the energy-per-cycle that the device can carry without failure during avalanche breakdown. The common approach to determining this value is an unclamped inductive switching test, often involving packaging a device prior to its testing.

Unfortunately, it's challenging to comprehensively investigate the device's avalanche behaviour at the package-level, due to a limited physical and optical access to the die. So, to overcome this issue we have employed a modified test set-up that integrates the unclamped inductive-switching circuit with the wafer-prober. On-wafer tests on devices allow us to perform device-material co-investigations. With this configuration we can undertake on-wafer avalanche tests and electroluminescence measurements simultaneously.



➤ Figure 5. Top view optical images of a GaN vertical *p-n* diode at different instants during an avalanche breakdown. A high voltage, unclamped inductive switching pulse train applied to the diode pushes it into the avalanche breakdown mode. At breakdown, current filaments (or micro-plasma tubes) form which later dynamically move around, spreading the heat across the diode area as the avalanche progresses.

Dynamic filaments improve the diode's reliability and robustness under avalanche breakdown. Filaments may be static in poorly designed devices, causing local burnouts and failures and ultimately limiting device reliability

Such studies show that our 1.2 kV GaN vertical *p-n* diode with optimised *p*-type doping and bevel angle produces uniform electroluminescence. When the diode is operating under avalanche, its cathode voltage clamps to the avalanche voltage and there is a high current flow from the cathode to the anode terminal.

This robustness is highly sought after by circuit designers and power electronics engineers who use power semiconductor devices. What's encouraging is that the degree of avalanche robustness of the GaN *p-n* diode is significant – it exceeds that of a commercial SiC Schottky diode of similar voltage and current rating by 22 percent. Having said this, one might wonder, what contributes to high avalanche robustness in GaN diode? When avalanche occurs in GaN *p-n* diode, this is accompanied by the formation of highly conducting micro-plasma tubes or current filaments across the junction. Due to this, short-circuit paths are momentarily created between cathode and anode terminals. During avalanche, the surge energy from the inductor discharges through these filaments and is later dissipated as heat and light.

We have discovered that the avalanche current filaments in our GaN diodes are not stationary but grow and dynamically move around the diode's active area under switching conditions (see Figure 5). This movement, which is driven by the temperature gradient inside the filament's core, is beneficial, assisting uniform spreading of heat across the device area and suppressing any potential local hotspots. Consequently, these dynamic filaments improve the diode's reliability and robustness under avalanche breakdown. Filaments may be static in poorly designed devices, causing local burnouts and failures and ultimately limiting device reliability.

It is clear that GaN diodes with avalanche capability have great potential to improve the performance of power electronic circuits. There's still a long way to go to understand how to design and optimise these devices for tapping into their full potential using their intrinsic capabilities such as avalanche. But we have shown the benefits of a holistic approach to realise GaN devices with robust avalanche, and how electroluminescence can offer great insight into their avalanche behaviour.

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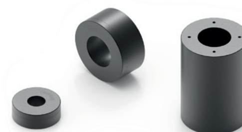
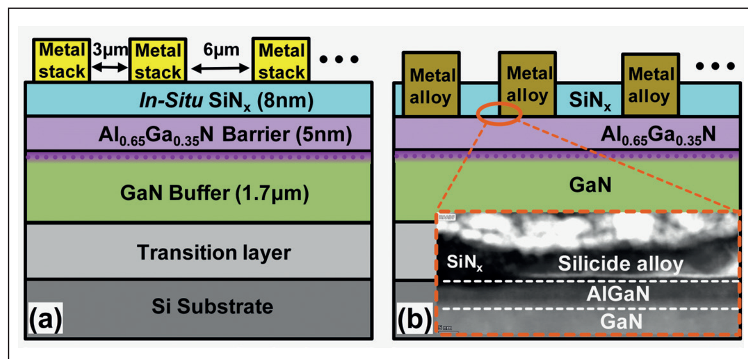


SiN trims the resistance of high-speed HEMTs

In-situ addition of SiN reduces the contact resistance of aluminium-rich HEMTs

ENGINEERS FROM Xidian University, China, have significantly cut the contact resistance of GaN-based HEMTs with an aluminium-rich AlGaN barrier layer by *in-situ* insertion of SiN.

Their triumph promises to aid the development of HEMTs operating above 40 GHz. In these devices, the aluminium-rich AlGaN barrier enhances the transistor's speed, but hampers the realisation of a low contact resistance.



➤ After adding the metal contact to the heterostructure with a SiN layer (a), the annealing step creates a metal alloy that's in contact with the $Al_{0.65}Ga_{0.3}5N$ barrier (b).

According to the team, their approach is simpler and cheaper than that of alternatives for realising high-frequency AlGaN/GaN HEMTs with a low contact resistance, such as silicon implantation and the re-growth of a heavily doped *n*-type GaN layer.

Spokesman for the researchers, Zhihong Liu, told *Compound Semiconductor* that the idea for inserting a SiN layer came from previous experimentals.

He remarked: "We knew that a thin layer of silicon, deposited in a certain way, could help the ohmic contact formation in GaN HEMTs; and at high temperatures the quality of SiN will degrade and become very leaky – so a thin layer of SiN may decompose and the remaining silicon help with the ohmic contact."

Liu and co-workers investigated this possibility with an $Al_{0.65}Ga_{0.35}N$/GaN HEMT featuring a thin layer of SiN, grown *in-situ* on the surface of the heterostructure.

This study began by taking a sapphire substrate and growing, by MOCVD, a 1.7 μm-thick unintentionally doped GaN buffer, followed by a 5 nm-thick $Al_{0.65}Ga_{0.35}N$ barrier and a 8 nm SiN layer. According to room-temperature Hall mobility measurements, this structure has a two-dimensional electron gas density of 2.2 x 10^{13} cm^{-2} and a mobility of 1190 cm^2 V^{-1} s^{-1}.

After planar isolation by argon-ion implantation, the team formed ohmic contacts through the addition of a Ti/Al/Ni/Au metal stack, annealed under nitrogen gas for 30 s at 850 °C. It is claimed that the composition of the stack and the annealing conditions is optimised. For comparison, the researchers fabricated a control, identical except for omission of the *in-situ* SiN layer.

Turning to the transfer length method, with electrode spacings from 3 μm to 18 μm, revealed that adding of SiN reduced the contact resistance from 0.320 Ω mm to 0.175 Ω mm and cut the specific contact resistivity from 2.84 x 10^{-6} Ω cm^2 to 8.45 x 10^{-7} Ω cm^2. A combination of resistance-related measurements between 300 K and 450 K and modelling of this data allowed the team to deduce the primary transport mechanism in ohmic contacts at metal-semiconductor interfaces for both types of device.

That approach revealed that thermionic field emission governs transport in the ohmic contact of the sample with the SiN layer. This behaviour is beneficial in GaN-based electronic devices, because they often operate at high junction temperatures. In the control, field emission is thought to dominate, due to the thinness of the $Al_{0.65}Ga_{0.35}N$ layer and its larger barrier height.

Inspecting the contacts with high-resolution transmission electron microscopy revealed that the 8 nm-thick SiN layer decomposed under annealing. It's suggested that the dark clumps observed at the interface are TiN. They are partially surrounded by gold – its presence is confirmed energy-dispersive X-ray spectroscopy.

Liu admitted that he is still to optimise the thickness of the SiN layer, which has a tremendous impact on the resistance.

The team also applied its technology to an AlN/GaN HEMT, grown on silicon, and recorded high values for both the cut-off frequency and the maximum oscillation frequency. "This work is submitted to another journal and is still under review," added Liu.

The next goals for the engineers are to try and improve the contacts by tuning the thickness of SiN, and using their recent breakthrough to develop millimetre-wave and terahertz HEMTs.

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Enhancing the credentials of Ga_2O_3 with a novel MOSFET

A vertical Ga_2O_3 MOSFET with a U-shaped gate trench and a current-blocking layer combines promising performance with E-mode operation

ENGINEERS FROM CHINA are claiming to have broken new ground by unveiling the first β-Ga_2O_3 MOSFET with a U-shaped gate trench.

This vertical MOSFET has key advantages over those with a lateral geometry, according to Guangwei Xu from the University of Science and Technology of China, who is the spokesman for a team that includes departmental colleagues and Yongjian Ma from the Suzhou Institute of Nano-Tech and Nano-Bionics. "For Ga_2O_3 lateral MOSFETs, channel thickness is limited to hundreds of nanometers," commented Xu, who added that in this class of device the substrate tends to just provide structural support, and does not contribute to device performance.

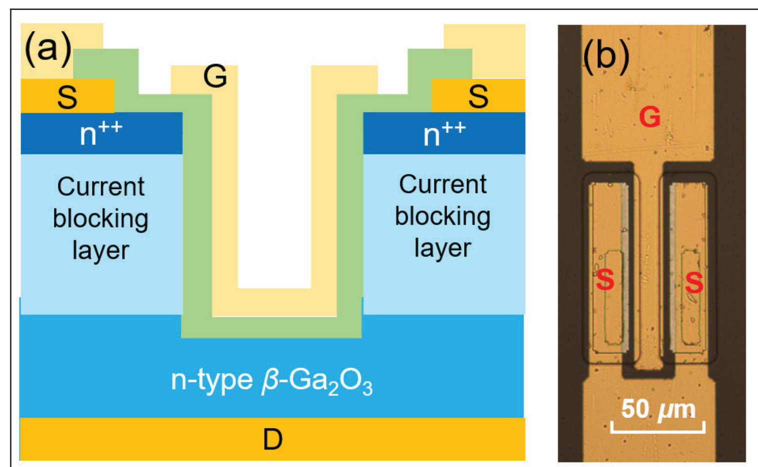
"Therefore, the drain-to-source current cross-section for a lateral MOSFET is much smaller than a vertical MOSFET, which means that a much larger current density is needed for a lateral MOSFET to achieve the same current level as a vertical MOSFET."

Another advantage of the vertical MOSFET is that its breakdown voltage can be increased without sacrificing chip area, because the breakdown voltage scales with drift-layer thickness. Vertical transistors also benefit from a more uniform heat distribution, as well as burying the peak electric field in the bulk – this prevents premature device failure caused by surface flashover, and alleviates performance instabilities induced by surface states.

Xu and co-workers are not the first to produce a vertical β-Ga_2O_3 MOSFET. There are reports of vertical fin-channel FETs, vertical diffused-barrier FETs and vertical current-aperture FETs – but all of these have their weaknesses. The fin-channel FETs, which have realised a breakdown voltage of more than a kilovolt, are produced using a complex, costly fabrication process. Meanwhile, unlike the U-shaped trench MOSFET, the vertical diffused-barrier FET and the current-aperture FET feature a JFET region, leading to a higher internal resistance.

Of all the variants, the cell pitch for the U-MOSFET can be made much smaller, enabling a higher packing density, according to Xu.

Realising a U-shaped trench β-Ga_2O_3 MOSFET is not easy, because it is a challenge to form an effective current-blocking layer. Drawing on work that shows how thermal annealing can create a high-resistivity layer, Xu and colleagues have introduced current blocking by thermal oxidation. This has led to the formation of an enhancement-mode MOSFET with an on-off ratio of 6 x 10^4.



➤ (a) U-shaped trench β-Ga_2O_3 MOSFETs feature an effective current blocking layer, formed by oxygen annealing. (b) An optical image of this device.

To produce the team's U-shaped trench β-Ga_2O_3 MOSFETs, the researchers began by taking a (201)-orientated substrate with a doping concentration of around 3 x 10^{17} cm^{-3} an annealing it under oxygen for 6 hours at 1200 °C to form a current blocking layer. Implanting oxygen with a concentration of around 3 x 10^{19} cm^{-3} introduced an n^{++} layer, activated by thermal annealing for 5 minutes at 950 °C. Mechanical grinding of the backside of the wafer removed the high-resistivity layer, before etching defined the trench and mesa. Electron-beam evaporation enabled the addition of source and drain contacts, prior to atomic layer deposition of the gate dielectric and the formation of the gate, using magnetron sputter deposition.

Electrical measurements on the devices revealed an off-current below 10^{-4} A cm^{-2} at a gate-source voltage of 0 V, suggesting normally off operation. The threshold voltage is 11.5 V, a high value that is attributed to the thick dielectric. Trimming this layer could realise a more preferable threshold voltage.

Xu revealed that one of the team's next goals is to reproduced their results via HVPE. The breakdown voltage of the latest devices is limited by the small depletion width of relatively highly doped substrates. "To improve both the on-state and the off-state performances, future work will focus on the highly doped substrate with a lightly doped epitaxy layer."

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Passivating GaN with ruthenium

Schottky diodes deliver improved performance when a ruthenium solution is used to passivate the surface of GaN

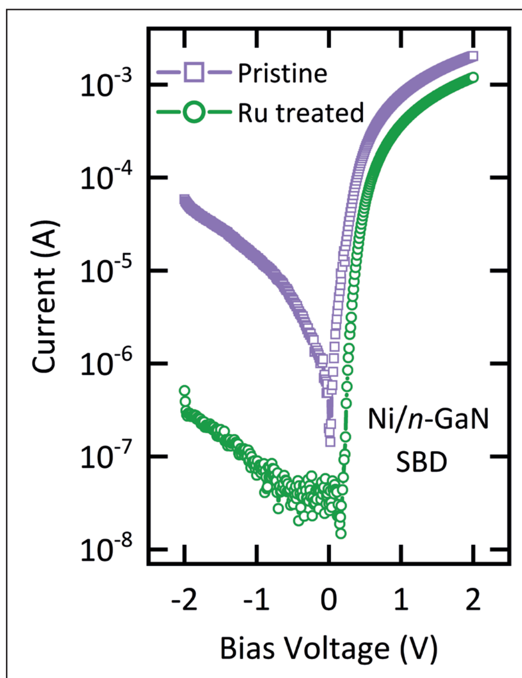
A TEAM from India is pioneering the use of a ruthenium solution to passivate the surface of GaN.

Effective passivation is crucial to optimising performance of GaN devices, as it eradicates defects such as oxygen impurities and nitrogen vacancies, causes of high gate-leakage currents.

The researchers – from Kurukshetra University, the University of Petroleum and Energy Studies and the Inter-University Accelerator Centre – have demonstrated the benefits of ruthenium treatment with GaN Schottky barrier diodes. Treated devices show considerably better performance, including a significant reduction in leakage current.

Spokesman for the team, Ashish Kumar, who is affiliated to both the University of Petroleum and Energy Studies and the Inter-University Accelerator Centre, told *Compound Semiconductor* that the team has been looking at the impact of ruthenium on GaN for many years. In 2014, they published a paper reporting the results of investigations with X-ray photoelectron spectroscopy; and now they are unveiling the findings of a study involving the use of scanning tunnelling microscopy and photoluminescence.

➤ Current-voltage plots highlight the reduction in the leakage current provided by passivation with ruthenium.



One of the benefits of using ruthenium for passivation is that it has a small atomic radius, which aids chemisorption on the GaN surface. A monolayer of ruthenium results from passivation, preventing atmospheric oxygen from forming bonds with gallium and nitrogen atoms.

"Ruthenium can have positive as well as negative oxidation states, so it can make stable bonds with both anions and cations," explains Kumar, a claim confirmed by X-ray photoelectron spectroscopy, which revealed Ga-Ru and N-Ru bonds.

The latest study involved *n*-type, single-crystalline GaN with a thickness of 500 μm and a carrier concentration of 5.6 x 10^{17} cm^{-3}, according to Hall effect measurements. Prior to passivation, samples were: ultrasonically cleaned in trichloroethylene, acetone and isopropanol, each for 10 minutes; rinsed with deionised water; dried under nitrogen gas; and etched in hydrochloric acid to remove the native oxide. Passivation resulted from dipping these pristine samples in a solution containing equal volumes of $RuCl_3$ (0.05 M) and HCl (0.1 M).

Photoluminescence measurements on passivated and pristine samples revealed a doubling in the intensity of emission after treatment in ruthenium solution for 1 minute, and a small further enhancement when extending this process to 5 minutes.

Kumar and co-workers also used scanning tunnelling microscopy to compare passivated and pristine samples of GaN. Mapping areas of 62 nm by 62 nm revealed that ruthenium treatment altered the surface features.

Plots of tunnelling spectra – the current as a function of the bias voltage of the tip – showed that after chemical treatment, a dielectric layer is induced on GaN surfaces. This layer reduced tunnelling, and shifted behaviour at negative voltages, possibly due to a neutralising of defect states and the accumulation of charge carriers in the conduction band near the surface. The implication is that the position of the Fermi level changed, turning into the conduction band at the sample surface.

To demonstrate the effectiveness of their passivation process, Kumar and co-workers fabricated Schottky diodes on pristine GaN, as well as that subjected to ruthenium treatment. Measurements showed that passivation increased the Schottky barrier height from 0.78 eV to 0.91 eV, decreased the ideality factor from 1.42 to 1.12, and reduced the leakage current at reverse bias by around two orders of magnitude.

Kumar says that the team plans to continue its studies of passivation, using deep-level transient spectroscopy and time-dependent investigations.

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