POWER ELECTRONICS WORLD

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ISSUE II 2021

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Bi-directional power flows need SiC MOSFETs

Silicon substrates for satellite comms

High-voltage GaN trumps SiC

High-voltage GaN HEMTs

How robust is the SiC MOSFET?

Overcoming bumps along the EV road

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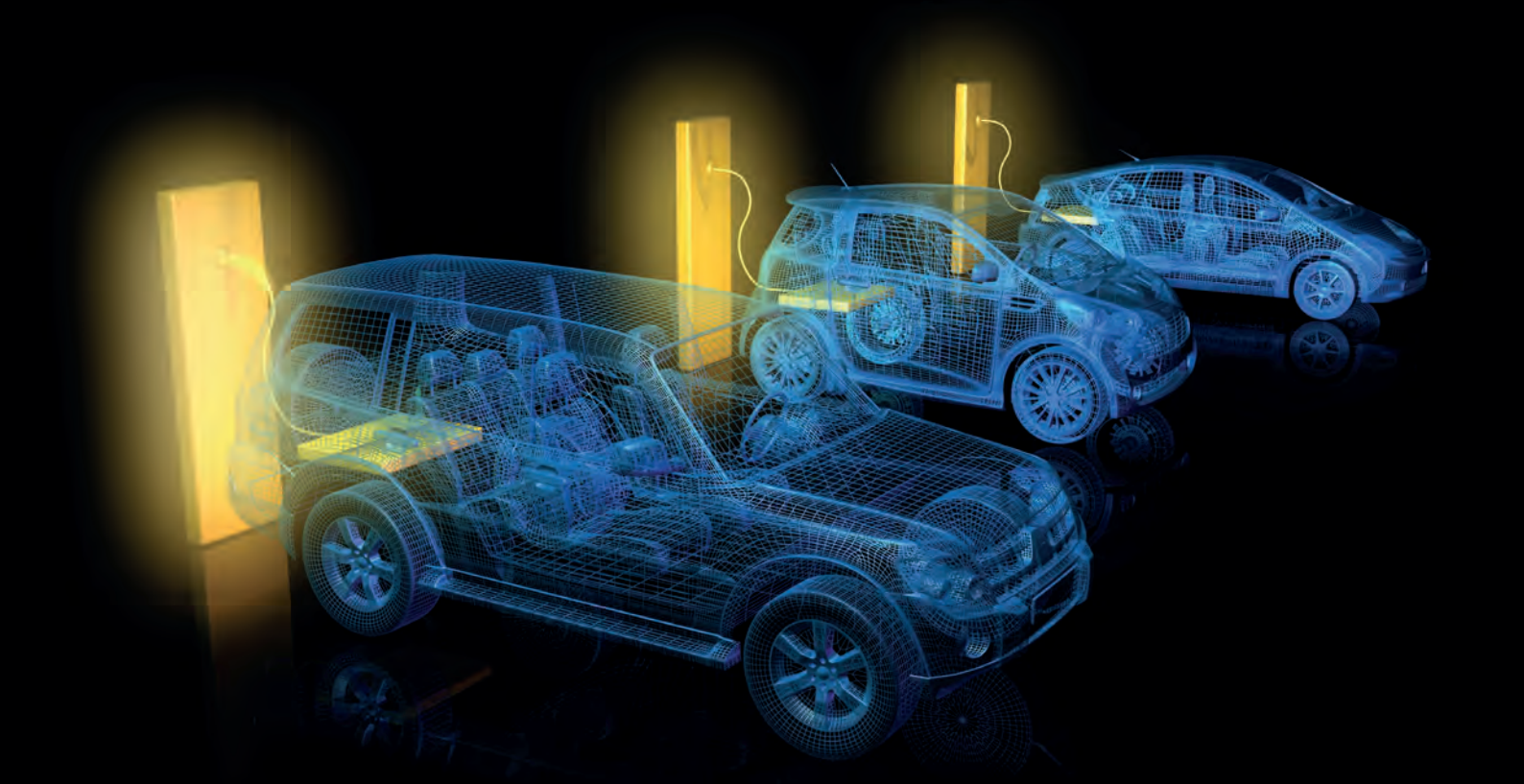

Best performance for next generation SiC power electronics to address global mega trends

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editor's view

By Mark Andrews, Technical Editor

Wafers, materials, refurb equipment surge as post-COVID market takes shape

EVEN AS THE WORLD STRUGGLES to regain its pre-pandemic footing, leading semiconductor indicators point towards a strong post-COVID economy that seeks to slake its thirst for tech-driven products and services. The demand for power controllers by vehicle manufacturers and stronger than usual demands across practically every supply chain sector is fueling concerns that soaring demand may bring inflation along for the ride.

Consumers are paying more for just about everything in these post-pandemic times. If anyone has shopped recently for food staples, consumer electronics, automobiles or even homes, the chances are that prices seen today are higher than two months ago. Answering the 'why' question is straightforward —demand continues to outstrip supply. In a world where almost everyone has been told for months to stay at home, avoid crowds, mask, and get vaccinated, factory output is lagging behind consumer ambitions to make up for lost time.

The SEMI trade group reports that as of 4th May, first quarter silicon wafer shipments easily ran past historic 1Q seasonal benchmarks. Materials makers are also enjoying robust sales as digitization (in part brought on by the pandemic,) continues to surge ever more deeply into daily life. SEMI also attributes the rise in materials sales to an outgrowth of 5G buildouts and new interest in this supply chain sector by global investors. Unsurprisingly, semiconductor equipment makers are also on track for another bonanza year, so much so that legacy gear (anything supporting wafers less than 300mm) is enjoying

a resurgence. Refurbished equipment is also a means to bring new fab capacity online quickly since there is a trained workforce ready and willing.

In this edition of Power Electronics World we look at how the demand for electric vehicles (EV) continues to grow, which presents challenges for charging station designers, battery makers and automakers already short of the ICs they need to build new vehicles. We also examine a new MOSFET technology from Infineon designed to make power conversion in renewable energy systems more efficient, how GaN may beat SiC in the power rectifier game and how GaN devices are also disrupting the traveling wave tube market.

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PEW Magazine is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication.

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news

Infineon launches 1200V CoolSiC MOSFET

INFINEON has launched a new EasyPACK 2B module in the company's 1200 V family. The module comes in 3-level Active NPC (ANPC) topology and integrates CoolSiC MOSFETs, TRENCHSTOP IGBT7 devices, and an NTC temperature sensor along with PressFIT contact technology pins.

The power module is suitable for fast-switching applications like energy storage systems (ESS). The module also increases the power rating and efficiency of solar systems and supports the growing demand for 1500 V DC-link solar applications.

Using the latest CoolSiC MOSFET and TRENCHSTOP IGBT7 technology combined with an increased diode rating, the Easy module F3L11MR12W2M1_B74 is designed to operate over the entire power factor (cos ϕ) range.

A single module per phase is capable of supplying a power level of up to 75 kW in energy storage applications. For solar applications a power level of up to 150 kW can be reached by operating two modules in parallel per phase.

With its improved pin positioning, the module also ensures short and clean commutation loops with reduced stray module inductances.

Its optimized layout enables excellent thermal conduction of the CoolSiC MOSFET chips within the EasyPACK 2B package. In addition, the power module supports easy design-in and provides a high degree of freedom for inverter design. The EasyPACK CoolSiC MOSFET module F3L11MR12W2M1_B74 is now available. The product will be showcased at Infineon's Virtual Power Conference, which complements PCIM Europe digital days.

Carbon Neutral Energy brings battery storage solution to US

CARBON NEUTRAL ENERGY (CNE) is to open in the US, two months after officially launching in the UK.

The hybrid power solutions company is fast-tracking its overseas expansion due to the huge demand for mobile energy storage systems which could prevent emergencies like the loss of power in Texas earlier this year.

CNE has developed a revolutionary energy storage solution that meets the growing challenge of storing and using electricity produced from renewable sources. Using a range of mobile, modular energy storage systems with large capacity battery storage, CNE aims to increase green electrification and reduce carbon emissions, accelerating the world's net-zero ambition. Their energy storage systems can store and deliver significant green power capacity to address inadequacy in power infrastructure.

The company, which has embarked on a £300m fund-raise and made several executive and non-executive appointments, is currently exploring locations for its first overseas base in

Texas. The US state experienced a major power crisis in February this year as a result of three severe storms sweeping across the US. Half a million Texans were without power. CNE believes its battery storage solution can prevent this happening in the future.

CNE sales director, Philip Patterson, said: "Two things happened: sources of electricity, like wind turbines, went offline and demand for the energy they produce went up. The crisis drew much attention to the state's lack of preparedness for such storms. Damages from the blackouts were estimated at $195 billion, making this the costliest disaster in Texas' history. "Battery storage is a vital in balancing the grid. Without storage, power emergencies such as those in Texas could occur again across the globe. With ongoing climate change, these events could become more frequent, so we believe the time to act is now and are getting into the US market early. Our vision is that our product range will help achieve greater efficiencies and build resilience into the Texas grid."

CNE has invested heavily in game-changing technology to meet the growing challenge of storing and using electricity produced from renewable sources. With a defined market strategy to become a significant player in the mobile green battery storage market, CNE is raising funds to ensure it has the right level of capital to exploit the opportunity and build a business capable of creating and supporting hundreds of green energy jobs.

CNE's systems offer large capacity battery storage from 1MW to 5MW in the form of a mobile unit with a suite of smaller static modules that can also be combined to create mega storage banks. These can be customised to meet any size of customer power requirements at any location, potentially creating gigawatt storage systems.

Imec and Aixtron pave the way for GaN to enter SiC high voltage domain

IMEC, a research and innovation hub in nanoelectronics and digital technologies, and Aixtron, a provider of deposition equipment for compound semiconductor materials, have demonstrated epitaxial growth of GaN buffer layers qualified for 1200V applications on 200mm QST substrates, with a hard breakdown exceeding 1800V.

The manufacturability of 1200V-qualified buffer layers opens doors to highest voltage GaN-based power applications such as electric cars, previously only with feasible SiC-based technology. The result comes after the successful qualification of Aixtron's G5+ C fully automated MOCVD reactor at Imec, Belgium, for integrating the optimised material epi-stack.

Over the years tremendous progress has been made with GaN-based technology grown on for example 200mm Si wafers. At Imec, qualified enhancement mode HEMTs and Schottky diode power devices have been demonstrated for 100V, 200V and 650V operating voltage ranges, paving the way for high-volume manufacturing applications. However, achieving operating voltages higher than 650V has been challenged by the difficulty of growing thick-enough GaN buffer layers on 200mm wafers. Therefore, SiC so far remains the semiconductor of choice for 650-1200V applications – including for example electric cars and renewable energy.

For the first time, Imec and Aixtron have demonstrated epitaxial growth of GaN buffer layers qualified for 1200V applications on 200mm QST (in SEMI standard thickness) substrates at 25degC and 150degC, with a hard breakdown exceeding 1800V.

The image above shows vertical forward buffer leakage current measured on 1200V GaN-on-QST at two different temperatures: (left) 25degC and (right) 150degC. Imec's 1200V buffer shows vertical leakage current below 1μA/mm2 at 25degC and below 10μA/mm2 at 150degC up to 1200V with a breakdown in excess of 1800V both at 25degC and 150degC, which makes it suitable for the processing of 1200V devices.

Denis Marcon, senior business development manager at Imec: "GaN can now become the technology of choice for a whole range of operating voltages from 20V to 1200V. Being processable on larger wafers in high-throughput CMOS fabs, power technology based on GaN offers a significant cost advantage compared to the intrinsically expensive SiC-based technology."

Key to achieving the high breakdown voltage is the careful engineering of the complex epitaxial material stack in combination with the use of 200mm QST substrates, executed in scope of the IIAP program The CMOS-fab friendly QST substrates from Qromis have a thermal expansion that closely matches the thermal expansion of the GaN/AlGaN epitaxial layers, paving the way for thicker buffer layers – and hence higher voltage operation.

Felix Grawert, CEO and president of Aixtron said: "The successful development of Imec's 1200V GaN-on-QST epi-technology into Aixtron's MOCVD reactor is a next step in our collaboration with Imec.

"Earlier, after having installed Aixtron G5+C at Imec's facilities, Imec's proprietary 200mm GaN-on-Si materials technology was qualified on our G5+ C high-volume manufacturing platform, targeting for example high-voltage power switching and RF applications and enabling our customer to achieve a rapid production ramp-up by pre-validated available epi-recipes. Currently, lateral e-mode devices are being processed to prove device performance at 1200V, and efforts are ongoing to extend the technology towards even higher voltage applications.

ON Semi announces new SiC diodes at PCIM Europe

ON Semiconductor introduced new SiC diodes as part of its activities during this year's PCIM Europe Digital Event (3rd to 7th May, 2021).

The automotive AECQ101 and industrial grade qualified next generation 1200 V SiC diodes are for high power applications such as EV charging stations and solar inverters, UPS, EV on board chargers (OBC), and EV DC-DC Converters.

The new design improves on the first generation SiC diodes thanks to a smaller die size and lower capacitance. The NVDSH20120C, NDSH20120C, NVDSH50120C, and NDSH50120C deliver a lower forward voltage drop and a 4x increase in rated current, with a higher rate of change (di/dt) of 3500 A/μs. The smaller die size also returns a 20 percent lower thermal resistance in an F2 package.

Ford boosts investment in Solid Power

FORD MOTOR COMPANY has announced it is growing its investment in Solid Power, an industry-leading producer of all-solid-state batteries for EVs. Initially investing in Solid Power in 2019, Ford is making an additional equity investment to help accelerate further development of solid-state vehicle battery technology, contributing to a $130 million Series B investment round in which the BMW Group becomes an equal equity owner with Ford.

Solid-state batteries are showing great promise. They don't use the liquid electrolyte found in conventional lithium-ion batteries, can be lighter, with greater energy density and provide more range and lower cost.

Solid Power, which uses sulfide-based solid-state battery cells, has demonstrated its ability to produce and scale next-generation all solid-state batteries that are designed to power longer range, lower cost and safer electric vehicles using existing lithium-ion battery manufacturing infrastructure.

Solid Power's leadership in all solid-state battery development and manufacturing has been confirmed with the delivery of hundreds of production line-produced battery cells that were validated by the BMW Group and Ford late last year, formalizing Solid Power's commercialization plans with its two long-standing automotive partners.

"By simplifying the design of solid-state versus lithium-ion batteries, we'll be able to increase vehicle range, improve interior space and cargo volume and ultimately deliver lower costs and better value for customers," said Ted Miller, Ford's manager of electrification subsystems and power supply research. "We look forward to delivering these improvements and working with Solid Power to seamlessly and quickly integrate their sulfide-based all-solid-state battery cells into existing lithium-ion cell production processes more efficiently than oxide-based solid-state battery cell makers can."

Under the new agreement, Ford will receive full-scale 100 ampere hour (Ah) cells from Solid Power for testing and integration into its future vehicles starting next year. Solid Power already is producing 20 Ah solid-state batteries on a pilot manufacturing line using lithium-ion production processes and equipment. Ford also has a separate joint development agreement with Solid Power to develop and test its specific battery cell design and help streamline Ford's integration into future vehicles.

Earlier this week, Ford announced a new global battery center of excellence – named Ford Ion Park – to accelerate research and development of its battery and battery cell technology – including future battery manufacturing.

Ford is building on nearly two decades of battery expertise by centralizing a cross-functional team of 150 experts in battery technology development, research, manufacturing, planning, purchasing, quality and finance to help Ford more quickly develop and manufacture battery cells and batteries, ultimately aiming to deliver more, even better, lower cost EVs for customers.

The Ford Ion Park team also is exploring better integration and innovation opportunities across all aspects of the value chain – from mines to recycling – working with all teams within Ford, including experts at Ford's new Battery Benchmarking and Test Laboratory, Ford Customer Service Division, plus key suppliers and partners.

The Ford Ion Park team already is underway. In addition, a $185 million collaborative learning lab in Southeast Michigan that is dedicated to developing, testing and building vehicle battery cells and cell arrays opens late next year. This world-class 200,000 sq.-ft. learning lab will include pilot-scale equipment for electrode, cell and array design and manufacturing and will use state-of-the-art technology to pilot new manufacturing techniques that will allow Ford to quickly scale breakthrough battery cell designs with novel materials once the company vertically integrates battery cells and batteries. Ford is committed to leading the electric vehicle revolution and this year has gained significant momentum on its plans.

In North America, the Ford Mustang Mach-E has found early sales success. Plus, the all-electric Ford Transit is set to go on sale late this year and the all-electric F-150 arrives by mid-2022. Ford will be the first automaker in the U.S. to offer commercial customers fully electric van and full-size pickup choices.

In Europe, Ford is moving to an all-electric lineup by 2030, with its commercial vehicle range 100 percent zero-emissions capable, all-electric or plug-in hybrid by 2024. Ford also is investing $1 billion in a new electric vehicle manufacturing center in Cologne to build a high-volume all-electric passenger vehicle for European customers starting in 2023.

In China, Ford is preparing to produce the Mustang Mach-E for local customers later this year, and recently announced it is establishing a BEV division with a direct sales model and network that will reach 20 major cities across China this year. In addition, Ford has partnered with China's State Grid and NIO to offer EV customers access to more than 300,000 public charging stations, of which 160,000 are fast-charging, in more than 340 cities across the country.

Ford has been actively involved in battery research and electric vehicles dating back to the days of Henry Ford and Thomas Edison. To date, the company has secured more than 2,500 U.S. patents in electrification technologies, with another 4,300 patents pending and has sold more than 1 million hybrids, plug-in hybrids and all-electric vehicles since 2004.

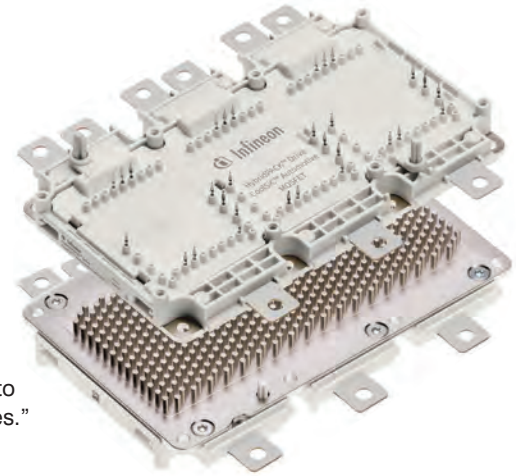
Infineon launches SiC six-pack module for EV traction inverters

INFINEON has introduced a new automotive power module with CoolSiC MOSFET technology. At this year's virtual PCIM trade show, Infineon will present the new HybridPACK Drive CoolSiC, a full-bridge module with 1200 V blocking voltage optimised for traction inverters in electric vehicles (EV).

The power module is based on the automotive CoolSiC trench MOSFET technology for high-power density and high-performance applications. This offers higher efficiency in inverters with longer ranges and lower battery costs, particularly for vehicles with 800 V battery systems and larger battery capacity.

"The 800 V system of the Electric Global Modular Platform (E-GMP) represents the technological basis for the next generation of electric vehicles with reduced charging time", said Jin-Hwan Jung, head of the electrification development team at Hyundai Motor Group. "By using traction inverters based on Infineon's CoolSiC power module, we were able to increase the range of the vehicle by more than five percent because of efficiency gains resulting from the lower losses of this SiC solution compared to Si based solution."

"The automotive e-mobility market has become highly dynamic, paving the ground for ideas and innovation", said Mark Münzer, head of Innovation and emerging technology at Infineon. "As the price of SiC devices significantly decreases, the commercialisation of SiC solutions will accelerate, resulting in more cost-efficient platforms adopting SiC technology to improve the range of electric vehicles."



The HybridPACK Drive was first introduced in 2017, using Infineon's silicon EDT2 technology, specifically optimised to deliver the best efficiency on a real-world driving cycle. It offers a scalable power range of 100 kW to 180 kW within the 750 V and 1200 V class. This product is Infineon's market-leading power module with a track record of more than one million pieces shipped for more than 20 electric vehicle platforms.

The new CoolSiC version is based on Infineon's silicon carbide trench MOSFET structure. Compared to planar structures, the trench structure enables a higher cell density, resulting in the best-in-class figure of merit. Therefore, trench MOSFETs can be operated at lower gate-oxide field strengths, resulting in increased reliability. The power module offers an easy upscale path from silicon to silicon carbide with the same footprint. This allows the inverter design to achieve higher power of up to 250 kW in the 1200 V class, greater driving range, smaller battery size and optimised system size and cost.

In order to offer an optimal cost-performance ratio for different power levels, this product is available in two versions with different chip counts, resulting in either a 400 A or 200 A DC rating version in the 1200 V class.

Fluke launches clamp meters with non-contact voltage measurement

FLUKE has announced the launch of a family of clamp meters that make electrical measurements much safer for servicing and maintenance technicians. The Fluke 377 and 378 are non-contact voltage True-rms AC/DC clamp meters that allow technicians to make rapid electrical tests without the danger of coming into contact with hazardous live parts.

The Fluke 377 and 378 use FieldSense technology to sense voltage and current through the clamp jaw, with only a connection to earth needed for reference. With no direct connection with live components, the risk of electric shock and arc flash is minimized.

The clamp meters measure up to 1000 A True-rms AC/DC and up to 2500 A (AC) with the 'iFlex' current probe. Designed for ease of use, only three steps are needed to measure in three phase systems, with each voltage and current shown simultaneously on the dual display. Both meters are available in FC (Fluke Connect3:38 PM) versions with Bluetooth interface. The 377 FC and 378 FC versions also show phase rotation, which can be displayed on a smart phone and saved to the cloud via Fluke Connect software, eliminating the need for handwritten notes. Fluke Connect allows maintenance technicians and service staff to document values and share them with their team. The data gathered can be used as a basis for designing a preventive maintenance program. The 378 FC includes a unique power quality (PQ) indicator that senses PQ issues, relating to current, voltage or power factor. This allows users to rapidly check if issues relate to the power supply or the connected electrical equipment.

Also included with the clamp meters are a TPAK magnetic hanging kit, a premium carrying case, TL224 test leads, TP175 Twist Guard Test Probes, and an AC285 black grounding clip.

5G to spur growth of GaN & SiC semiconductor market by 2027

RAMPANT development and roll out of 5G technology around the globe will offer new growth prospects to GaN and SiC power semiconductor manufacturers. These semiconductors are known for providing small form factor and high-power density, hastening their adoption whilst telecom operators augment infrastructure development.

According to a study conducted by Global Market Insights, the GaN & SiC power semiconductor market is projected to surpass USD 4.5 billion by 2027. Constant initiatives taken by governments for adopting 5G technology will drive the expansion of the industry.

Technological innovations within SiC power modules due to the incorporation of dedicated chipsets and IC could decrease device footprint and raise energy efficiency, which is likely to propel their demand in smart grid applications and smart energy meters. Additionally, the industrial motor drive segment is expected to witness high product demand given to growing trends of industrial automation robots and machinery.

The discrete GaN category accounted for around 2% industry share in 2020 and is projected to register a CAGR of around 40% over the forecast timeframe.

Discrete GaN power semiconductors provide low cost advantages and have wide band gap, hence escalating their demand in charging applications in consumer electronics devices.

GaN & SiC power semiconductor devices help in increasing power density and in minimizing the size of passive components, which is driving their usage in PV inverters. The PV inverters application segment held above 25% of the market share in 2020 and is likely to grow at a 30% CAGR over the forecast timeframe owing to surging consumer preference towards clean electricity.

Based on region, the Europe GaN & SiC power semiconductor market was valued at over USD 100 million in 2020 and is projected to grow at a 25% CAGR during the forecast period. Rising favorable initiatives taken by the government to accelerate electric vehicle adoption are expected to boost the regional growth in the estimated timeframe. In March 2021, the German government announced to offer USD 6.5 billion funding for electric vehicle charging infrastructure. Such initiatives will provide an additional opportunity to regional players operating in the industry.

The key players operating in the GaN & SiC power semiconductor market include Fuji Electric Co., Ltd, Alpha and Omega Semiconductors, Mitsubishi Electric Corp., Microsemi Corp., Infineon Technologies AG, and Diodes Inc., among others.

The major players are focusing on taking strategic initiatives like mergers, acquisitions, and partnerships for staying competitive in the market. In June 2020, ROHM announced its partnership with Vitesco Technologies to deliver SiC components to Vitesco to increase the efficiency of power electronics in electric vehicles.

This partnership is expected to aid the company in strengthening its market position of SiC power solutions in EV applications.

Dennis Ralston
Sr. Director –
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Overcoming bumps along the EV road

Efforts to decarbonize vehicle powertrains bring many challenges. Beyond addressing consumer preferences and range anxiety, all while achieving 'net-zero' carbon levels to reduce climate change, there are extensive technical and logistical challenges. TAn insights into these technology issues against the backdrop of UK efforts to transform the way people and products are transported.

BY SIMONE BRUCKNER, MANAGING DIRECTOR OF AUTOMOTIVE RESISTOR MANUFACTURER, CRESSALL

How can technology alleviate concerns around the electric vehicle (EV) rollout? The ten-year countdown is on for the UK's 2030 petrol and diesel vehicles ban. Changing the fuel source of the nation's vehicle fleet is sure to present some hurdles. So what can be done to make widespread electric vehicle rollout a reality?

When Prime Minister Boris Johnson revealed his Ten Point Plan for a Green Industrial Revolution back in November 2020, he brought the end date for the sale of new fossil-fuelled vehicles forward by a decade. This has placed extra pressure on automotive manufacturers and the government to realise the nation's EV capabilities in a much shorter timeframe

than initially planned. By 2030, it's estimated that over a third of the cars and vans on the UK's roads will be electric. The electrification of the automotive sector is a huge step towards decarbonising the UK and reaching net-zero carbon emissions by 2050, but it is undoubtedly a challenge. To achieve this goal, we must overcome several obstacles.

Battery concerns

When looking to purchase an EV, a main concern among consumers is its battery capability. Range anxiety is the fear that you may run out of charge mid-journey with no access to charging points. EV range varies depending on the model, but the distance EVs can travel on a single charge is typically less than their petrol or diesel alternatives.

Additionally, many consumers are held back by long battery charging times. Although new lithium-ion batteries were developed by Israeli company StoreDot that are capable of fully charging in just fifteen minutes, this innovative technology is likely to come with a sore price point that will limit widespread uptake.

Standard EV batteries can be fully recharged in four to seven hours using a 22-kilowatt (kW) fast charger, or in an hour using a 55-kW fast charger. These timescales are significantly longer than the time it would take to fill the tank at a petrol station.

Unsurprisingly, encouraging consumers to reconsider their expectations and change their behaviour has caused some lag in EV uptake. Traveling in an EV requires prior planning that incorporates an adequate charging timeframe to guarantee their uptake, and this is something we will all have to get used to.

Infrastructural limitations

An entirely new fuel source also requires an entirely new infrastructure to facilitate simple charging. The UK government has pledged to invest £1.3 billion in charging infrastructure, and Transport Secretary Grant Shapps has hailed the UK's EV charging network as 'world-leading'.

However, concerns around regional differences in charging infrastructure have already arisen. A report by the UK's leading think tank, Policy Exchange, revealed that currently, London has over 100 public charge points per 100,000 people — triple that of the North West, Yorkshire and Northern Ireland.

Although the densely populated capital will undoubtedly have a higher demand for EV charging stations, it's unlikely that elevated demand is fully responsible for these regional discrepancies. In addition, the number of charging points across the country will need to increase over ten-fold by 2030 to meet demand, from the current 35,000 to over 400,000.

Supply problems

The increased demand for EVs creates more load on the National Grid, which was not designed to facilitate the electrification of the entire country's fleet. As a result, EV charging could negatively impact the UK's power system, resulting in an imbalance between supply and demand.

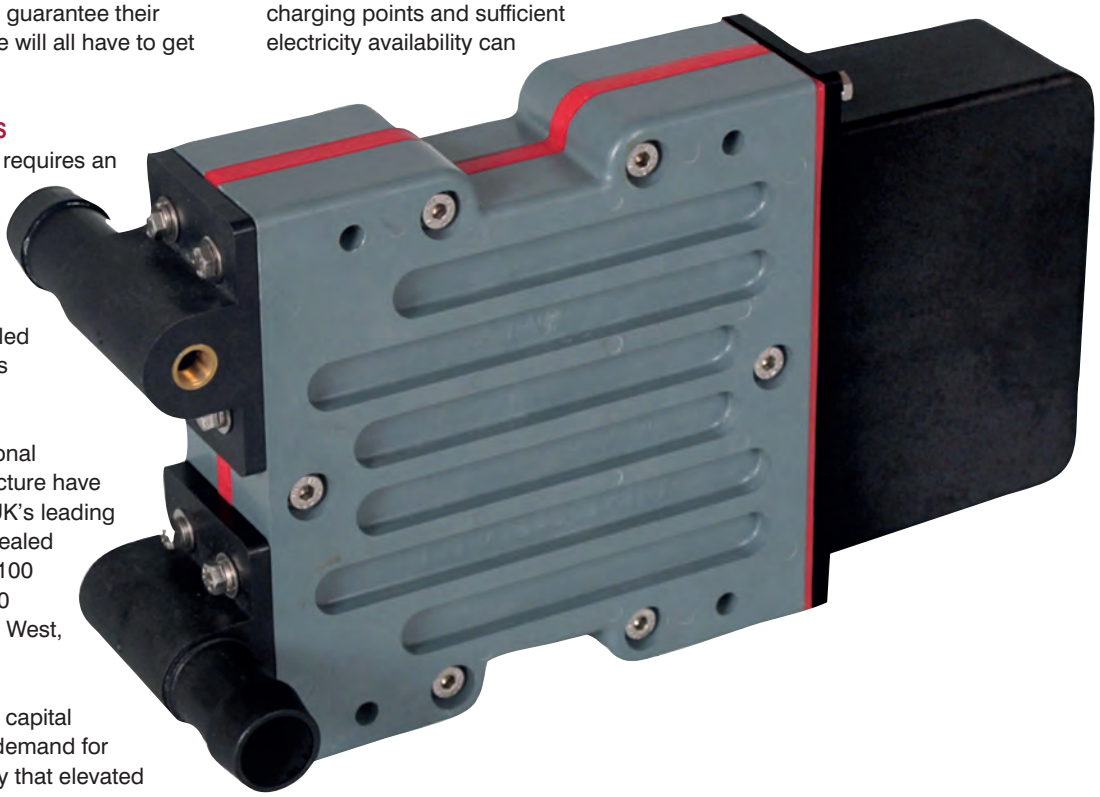
In the International Energy Agency's (IEA) Sustainable Development Scenario (SDS), by 2030 there could be 250 million EVs on the road globally. Currently, EVs account for 0.3 percent of global electricity demand — if the IEA's SDS becomes reality, this figure will increase to 4 percent.

Transmission networks are likely to need further investment as well as additional electricity generation resources to power an entire added sector of the country's infrastructure.

Overcoming hurdles through design

All of these concerns focus on infrastructural problems, which require costly, large-scale solutions. However, by designing EVs with these challenges in mind, automotive manufacturers can help to mitigate their impact on consumers and contribute to a simpler EV rollout.

Concerns around battery capabilities, access to charging points and sufficient electricity availability can



be alleviated, in part, by making energy efficient EVs that can travel the furthest possible distance on the smallest possible amount of power. One technology crucial to achieving this is regenerative braking.

In regenerative braking, as a vehicle slows down, its kinetic energy is converted into a form that can be stored and reused, rather than just dissipating it as wasted heat. On average, regenerative braking is between 60 and 70 percent efficient, which means that around two thirds of the kinetic energy lost during braking can be retained and stored in the EV battery and used later for acceleration, drastically improving the energy efficiency of the vehicle.

Reliable resistors

The principle of regenerative braking is simple, but in practice further technologies are required to ensure the vehicle operates safely. If the battery is already fully charged, or kinetic energy is being converted at a rate too fast for the battery to handle, then regenerative braking isn't viable. However, this excess energy has to go somewhere to make sure the EV stops when the driver brakes.

To manage excess energy, a dynamic braking resistor (DBR) is used to safely dissipate the energy and ensure the vehicle's braking system remains operational. Cressall's EV2 DBR is uniquely designed to separate the resistor elements from the coolant and is available in up to five-module assemblies to meet high-power requirements.

The EV2 also contributes to an EV's energy efficiency since it is water-cooled, which means that heat can be dissipated safely without the need for extra components, such as fans, as is the case with air-cooled resistors and has a total weight 15 percent less than a conventional DBR. These weight-saving properties lighten the load of the vehicle itself, meaning it can travel further on the same amount of fuel.

The UK is not alone in its goal to electrify the automotive industry, with countries around the world working towards the switch to EVs. For example, analysis by Frost & Sullivan has found that EV sales in the US are expected to increase from 1.4 million units in 2020 to 7 million units by 2025. With distributors across the globe, Cressall's EV2 DBR can be used by automotive industries worldwide to achieve efficient regenerative breaking in EVs.

EVs are the future of the UK's automotive market, but their deployment will not come without challenges. However, by anticipating these challenges and integrating technologies that can help to overcome them, car manufacturers can support the UK government in a successful, national EV rollout; an approach that both government regulators and the EV supply chain should consider world-wide.

EVs are the future of the UK's automotive market, but their deployment will not come without challenges. However, by anticipating these challenges and integrating technologies that can help to overcome them, car manufacturers can support the UK government in a successful, national EV rollout; an approach that both government regulators and the EV supply chain should consider world-wide.

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Power Rectifiers:

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BY YUHAO ZHANG AND MING XIAO FROM VIRGINIA TECH AND HAN WANG FROM THE UNIVERSITY OF SOUTHERN CALIFORNIA

RECTIFIERS providing high switching speeds and withstanding up to several kilovolts are in much demand. They are needed in power electronics systems used in the electricity grid, renewable energy processing, and industrial motors (see Figure 1).

Today, the most widely used device for rectification is the bipolar silicon *p-n* junction diode, despite its major drawback – a very slow switching speed, stemming from poor reverse recovery. A superior alternative that allows fast switching is the SiC Schottky barrier diode (SBD). However, its performance has only recently caught up with that of the silicon *p-n* diodes, and its epitaxial and fabrication costs are far higher.

Another material offering even more promise for high-voltage rectifiers is GaN: compared to silicon and SiC, it has the upper hand in several key areas, having a wider bandgap, higher mobility, and a higher critical electric field. Drawing on these strengths, several companies have launched GaN power devices with a lateral geometry, operating at up to 650 V. This geometry is challenging, limiting current and power capabilities, because current conduction takes place in a layer just a few nanometres thick – that's a consequence of the two-dimensional-electron gas (2DEG) channel. Note that this impairment does not arise in high-voltage silicon and SiC devices, because they usually have a vertical architecture, with current spreading into bulk materials.

One major drawback, resulting from the limited current capability of GaN power devices with a lateral geometry, is the need for larger die sizes when accommodating high voltages and high currents. As well as increasing chip costs, the larger die induce large capacitances and charges, compromising device switching speed.

To overcome these challenges, our team at Virginia Polytechnic Institute and State University (Virginia Tech), working in collaboration with engineers at Enkris Semiconductor, Qorvo and the University of Southern California, has developed a novel high-voltage lateral GaN technology that features multiple channel materials and innovative anode structures.

We fabricate our devices from 4-inch AlGaN/GaN-on-sapphire wafers that host five stacked 2DEG channels and are produced by Enkris. A five-fold increase in the number of 2DEG channels compared with a conventional structure increases current capability by at least that factor, and delivers a corresponding reduction in sheet resistance. Around the multi-channel fins is wrapped a new anode architecture, comprising *p-n* junctions. This structure shields the Schottky contact from a high electric field and suppresses the leakage current for the five-channel device to below that for a single-channel counterpart. The performance of the novel multi-channel GaN Schottky rectifier is impressive, boasting a power figure-of-merit that exceeds the unipolar SiC limit, and is among the highest in all high-voltage rectifiers.

Stacking 2DEG channels

When engineers design power devices, efforts centre on the concurrent realization of a high breakdown voltage and a low on-resistance – for a lateral GaN rectifier, the latter is the product of sheet resistance and anode-to-cathode distance. While this distance is usually determined by the breakdown voltage, the on-resistance hinges on the sheet resistance, which can be trimmed by increasing the mobility and density of the 2DEG. As the number of channels increases through stacking, the density of the 2DEG increases proportionally. In turn, die size for a specific current rating can be greatly reduced, leading to smaller capacitance and charges, and ultimately a higher switching speed and lower losses.

The idea of turning to multiple channels is not new. Around the start of the previous decade, researchers in the US and Japan pioneered AlGaN/GaN multi-channel epitaxy, using MBE. However, this growth technology is rarely suited to high-volume production of large-diameter wafers.

Our design, incorporating innovations in multi-channel materials and junction-fin anodes, promises to pave the way to a new generation of high-voltage GaN power devices that combine a low epitaxial cost with fast switching characteristics and high-power capabilities. Thanks to these attributes, our multi-channel lateral devices are will-equipped to extend the reach of GaN devices into high-voltage power electronics.

Very recently, the most common approach for the production of compound semiconductor devices, MOCVD, has been used to manufacture multi-channel structures on a variety of large-diameter substrates, including silicon, SiC, sapphire, and GaN. It is this growth technology that Enkris has employed to produce 4-inch, five-channel, GaN-on-sapphire wafers that feature a 2DEG with a density of 3.7×10^{13} cm^{-2} and a mobility of 1475 cm^2 V^{-1} s^{-1}. The corresponding sheet resistance is just 110 Ω/sq, a figure at least two times lower than the best value for a single-channel wafer. We estimate that the cost of this multi-channel GaN-on-sapphire wafer is no more than a third of that of a 4-inch SiC wafer.

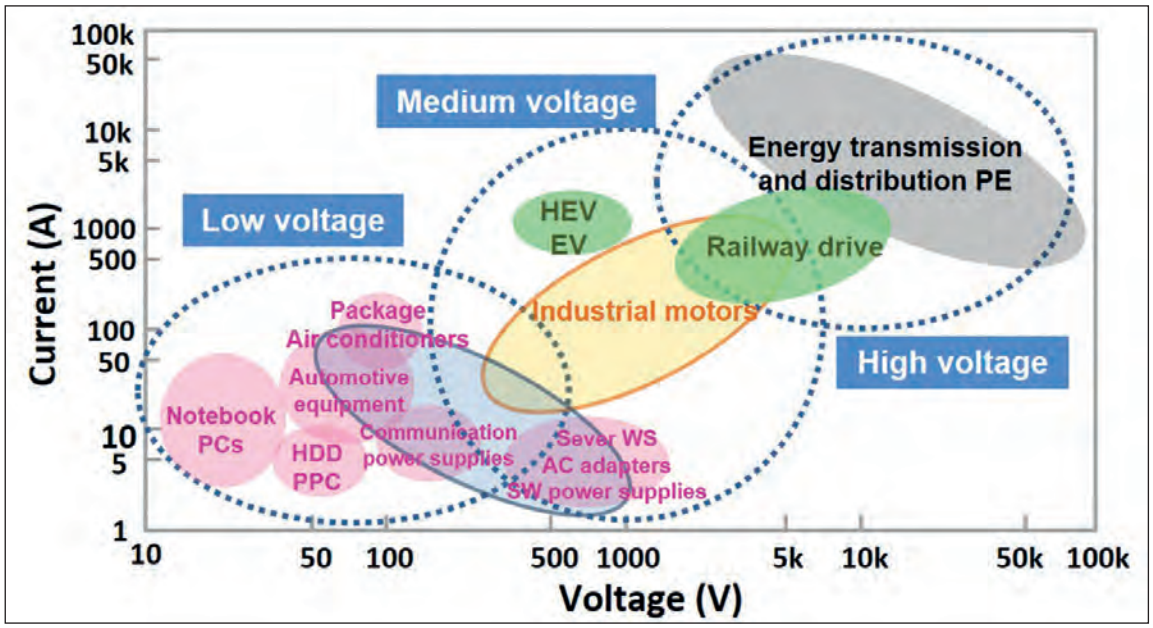

Figure 1. Application space of power rectifiers with different voltage and current ratings.

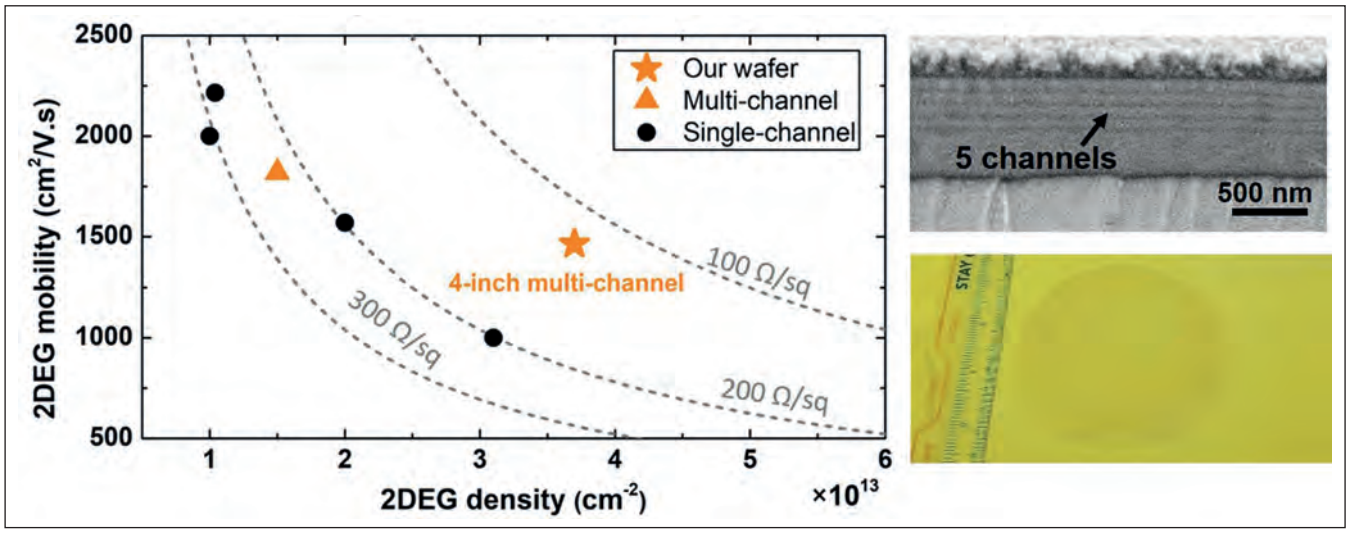

Figure 2 (left) 2DEG density versus 2DEG mobility for the single-channel and multi-channel AlGaN/GaN materials reported in the literature and measured on the wafer detailed in this article. (right) cross-sectional scanning electron microscopy image and top-view photo of the 4-inch, five-channel, GaN-on-sapphire wafer produced by Enkris Semiconductor Inc.

Cranking up the voltage

Scaling up the voltage of multi-channel devices is much more challenging than it is for their single-channel counterparts because the increased charges from multiple channels threaten to induce electric-field crowding. However, overcoming this challenge is crucial for Schottky rectifiers, because their blocking voltage tends to be limited by the peak electric field at the Schottky contact region.

Holding the key to suppressing electric-field crowding is proper edge termination, which may also shift the peak electric field away from the Schottky contact region. For lateral Schottky rectifiers, the common approach to edge termination is to add a field plate (see Figure 3(a)). However, if this is to be effective, there must be precise control over the field plate geometry, such as the thickness of the dielectric and the length of the field plate. In addition, the design and production of the device must account for complex interfaces between dielectrics and semiconductors.

Unfortunately, it is not uncommon for the device to exhibit instability when operating under high electric fields, or at high temperatures.

To tackle all these challenges, we have developed a new termination structure that uses a *p*-GaN layer grown on AlGaN/GaN (see Figure 3(b)). Thanks to vertical depletion enabled by our *p-n* junction, the electric field lines in the Schottky region spread out, and their distribution is more uniform. What's more, the peak electric field is re-directed from the Schottky contact to the edge of *p*-GaN termination, a shift that shields the Schottky contact from the high electric field. Compared with the field plate, our *p*-GaN termination possesses a wide design window, in terms of doping concentration and *p*-GaN thickness, and it produces minimal dielectric interfaces. Another key attribute is that the fabrication is fully compatible with today's foundry process for manufacturing the *p*-gate normally-off HEMT, opening up possibilities for monolithic integration of high-voltage rectifiers with GaN power ICs.

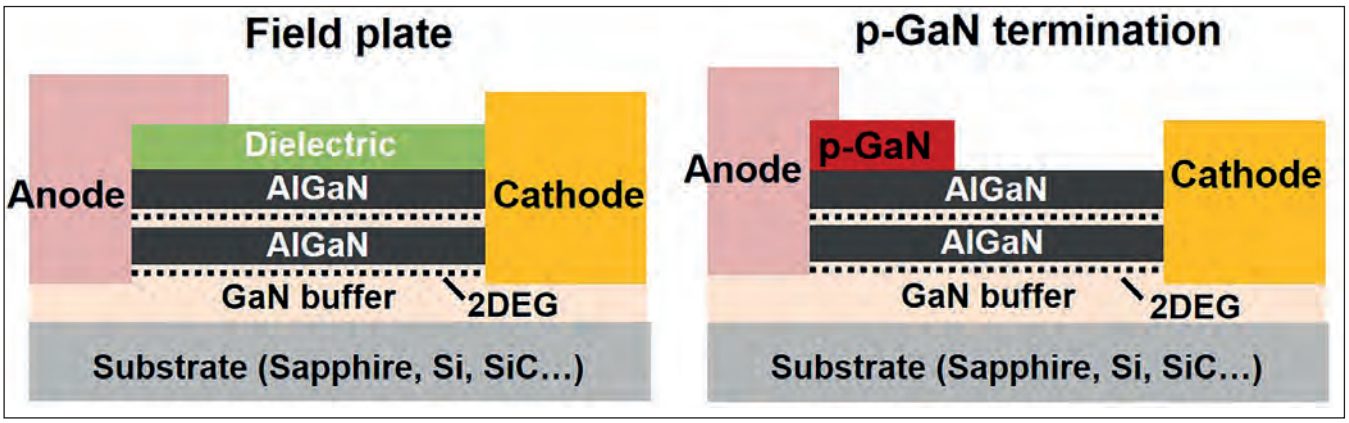

Figure 3. A conventional field plate termination (left) and Virginia Tech's novel *p*-GaN termination (right). Two channels are drawn to illustrate multi-channel structures.

Minimising device leakage

When developing our high-voltage multi-channel devices, the challenges we faced included minimising leakage current. Our solution is the junction-fin-anode. This is a three-dimensional anode structure, formed by wrapping *p-n* junctions around the multi-2DEG-fins (see Figure 4(a)). With this architecture, the *p*-type material provides strong depletion of the 2DEG channels. When the device is reverse biased, the junction-fin assists the Schottky contact for charge depletion, while shielding the Schottky contact from a high bias.

Our design can be evaluated with an equivalent circuit model of the entire rectifier (see Figure 4). This model includes an equivalent series connection for a sidewall SBD, a junction-fin-gated HEMT, and a *p*-gate HEMT. As the reverse bias increases, the sidewall SBD is pinched off, and then the two HEMTs. The voltage drop on the sidewall SBD is clamped at the threshold voltage of the junction-fin-gated HEMT, which is merely a few volts. This clamping occurs regardless of the reverse bias at the cathode, which can reach thousands of volts. Operating in this manner, the leakage current of the entire rectifier is equal to that of one of the sidewall SBDs biased at a few volts.

In our prototyped device, we realise the junction-fin structure by regrowth of *p*-GaN on top of the fin, and the addition of a *p*-type nickel oxide at the fin sidewalls. The resulting rectifier delivers a blocking voltage up to 5.2 kV, and when operating at 90 percent of this limit, the leakage current is just 1.4 μA/mm. The specific on-resistance is 13.5 mΩ cm^2. Based on all these values, we find that the power figure-of-merit for our device exceeds the SiC unipolar limit and is among the highest in all multi-kilovolt power SBDs.

We have also fabricated large-area devices. They are capable of handling a 1.5 A current, have a leakage current measured in microamps, and a total charge of 13 nC (see Figure 5). Compared with commercial SiC SBDs with similar voltage and current ratings, our multi-channel GaN SBDs exhibit a significantly lower forward voltage and charges.

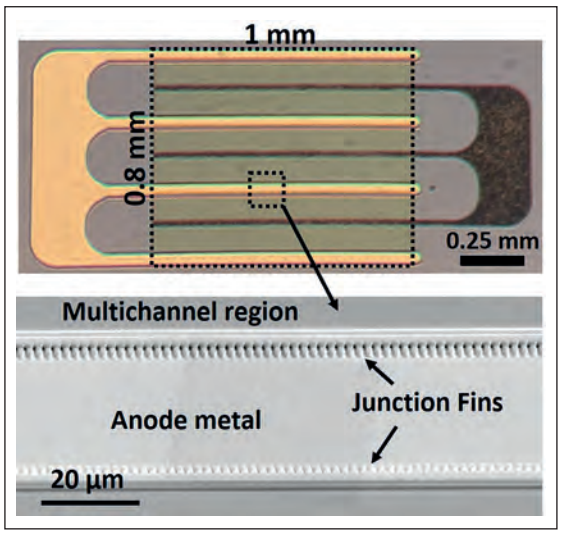

Figure 5 Top-view microscopic images of the fabricated 1.5 A, 5 kV GaN power Schottky rectifier.

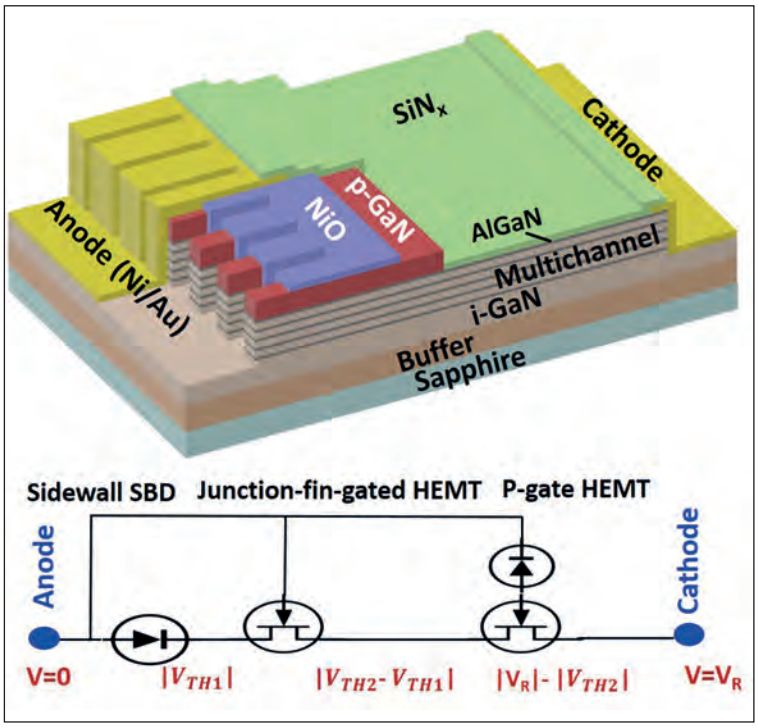

Figure 4 (top) Virginia Tech's multi-channel Schottky rectifier with a junction-fin anode. (bottom) Equivalent circuit model of the rectifier, comprising a series combination of a sidewall Schottky barrier diode, a junction-fin-gated HEMT, and a *p*-gate HEMT. The internal voltage distribution under a high reverse bias (V_R) is also illustrated, with the threshold voltages of the junction-fin-gated HEMT and *p*-gate HEMT marked as V_{TH1} and V_{TH2}, respectively. The voltage drop on the sidewall Schottky barrier diode is clamped at $|V_{TH1}|$ regardless of V_R.

These impressive characteristics show that our design, incorporating innovations in multi-channel materials and junction-fin anodes, promises to pave the way to a new generation of high-voltage GaN power devices that combine a low epitaxial cost with fast switching characteristics and high-power capabilities. Thanks to these attributes, our multi-channel lateral devices are will-equipped to extend the reach of GaN devices into high-voltage power electronics.

Further reading

M. Xiao *et al*. "5 kV Multi-Channel AlGaN/GaN Power Schottky Barrier Diodes with Junction-Fin-Anode", 2020 IEEE IEDM, 5.4.

M. Xiao *et al*. IEEE Electron Dev. Lett. **41** 1177 (2020)

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Switching to silicon substrates for satellite communication

Today's solid-state high-power power amplifiers operating in the microwave domain are based on the GaN-on-SiC HEMT. Replace the SiC with silicon and key attributes remain, while costs fall, thanks to production on larger wafers

BY ROCCO GIOFRÈ, FERDINANDO COSTANZO AND ERNESTO LIMITI FROM THE UNIVERSITY OF ROMA 'TOR VERGATA' AND ANTONINO MASSARI, FRANCESCO VITULLI AND ANDREA SURIANI FROM THALES ALENIA SPACE - ITALY

BROADBAND ACCESS SERVICES are destined for unprecedented growth this decade. As 5G is rolled out, data rates are climbing to 100 Gbit/s, while, in urban areas, simultaneous connections will total more than a million for every square kilometre. Alongside traditional services, such as video streaming, audio calls and data sharing, billions of daily used objects will be hooked up to the internet, including washing machines, fridges and ovens.

To underpin this new era in connectivity, there will need to be a new paradigm for the underlying network. This will include: a higher cell density, and thus a lower peak power; the introduction of a carrier frequency in the K-bands (18-27 GHz); an extended bandwidth; alternative channel access techniques, such as beam-division multiple access (BDMA); massive MIMO; and the use of more efficient spectrum aggregation signals. But even with all of this innovation, this network, which relies upon terrestrial infrastructures, will still fail to satisfy all of tomorrow's requirements.

One option for addressing this issue is to combine terrestrial infrastructure with satellite communication. Such a move will provide a major growth opportunity for geostationary earth orbit very-high-throughput satellites. These satellites can realise phenomenal data rates of more than 1 Tbit/s, while increasing the flexibility of the overall network, by allocating capacity where it is needed.

A key step in the deployment of very-high-throughput satellites is the development of high-performing space-borne equipment operating at high frequencies. It is envisaged that the feeder link, which is the radio channel between the satellite and a ground station, will be in the Q/V bands, so typically 40 GHz. Meanwhile the data link, providing the radio channel between the satellite and the end users, will reside in the K_a-band, at a frequency of 18.75 GHz.

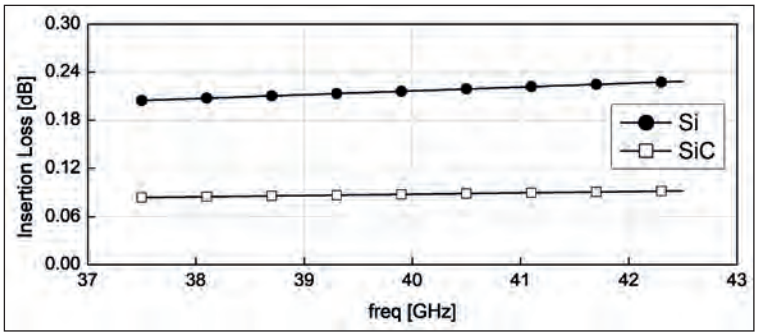

Figure 1. Simulated insertion loss of a transmission line with a $Z_0 = 50\ \Omega$ characteristic impedance and 1 mm length realized on silicon (filled symbols) and SiC (empty symbols) substrates.

Very-high-throughput satellites feature many beams. To accommodate this, satellites must house more equipment, realized ideally through miniaturization. New hardware needs to be lighter and smaller, as well as more reliable and better at thermal management.

Fulfilling all these requirements at the spacecraft level hinges on increasing the performance of the power amplifier, which sits at the last stage of the transmitting channel. This sub-unit of a payload consumes more than 75 percent of the overall DC power, so governs systems efficiency and thermal management

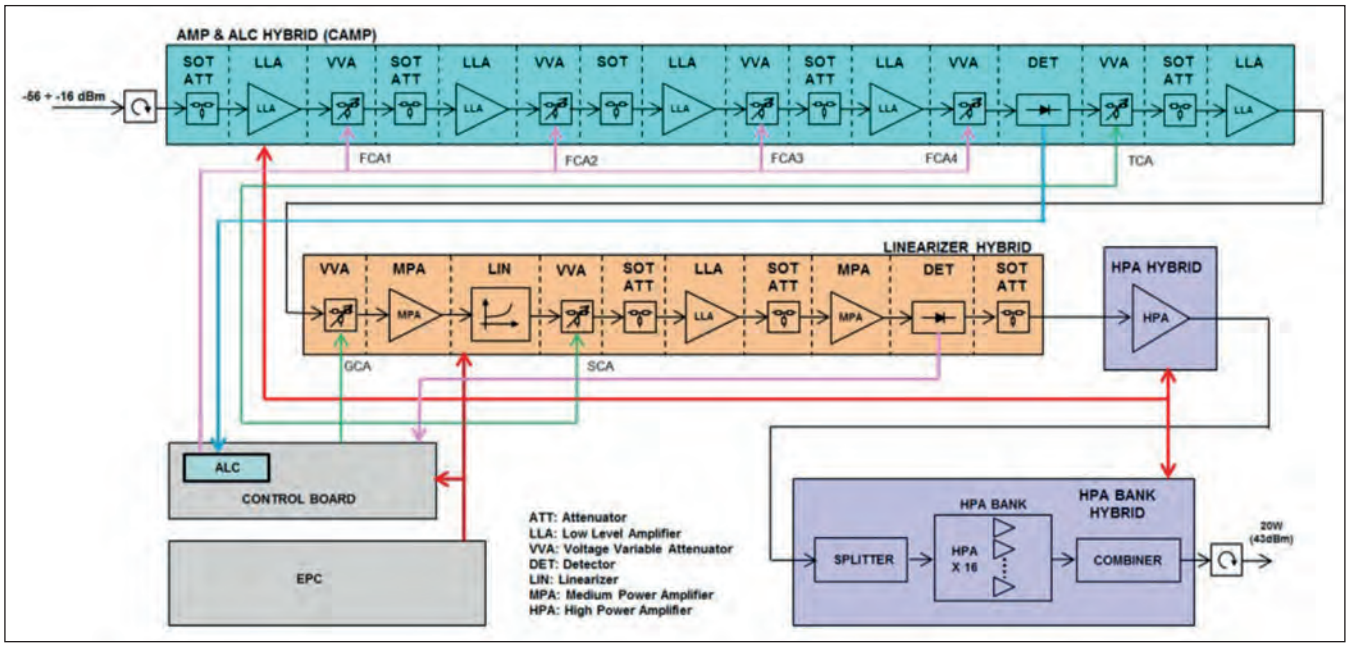

Figure 2. RF line-up of the solid-state power amplifier. It is composed by four sub-units, namely a Channel Amplifier (CAMP Hybrid), Linearizer Hybrid, HPA Hybrid and HPA Bank.

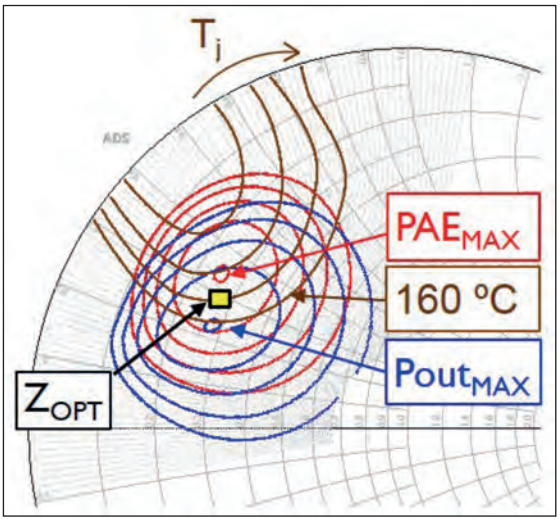

Figure 3. Simulated load-pull counters of the 4 x 75 µm device at a frequency of 40 GHz. Output power (blue), PAE (red), junction temperature (brown) and selected impedance (yellow).

requirements, while also impacting the reliability, mass and volume of the transmitter. In addition, the power amplifier determines the output power level and the spectral regrowth of the transmitted signal – these traits are determined by linearity and power characteristics.

Historically, when designers of communication satellites have needed power at high frequencies, they have turned to travelling-wave tube amplifiers. Their choice has been limited, because solid-state power amplifiers have fallen short of the performance required. But this has changed with the introduction of GaN, which has propelled solid-state technology to new levels of efficiency and power density, as well as a higher operating voltage and a higher impedance, which eases matching.

There are currently two types of process for producing GaN RF devices: one is for SiC substrates, and the other for silicon. The former has proven to be the best foundation for making high-power, efficient PAs at microwave frequencies, such as the K_u-band. However, silicon has much promise. This platform can exploit key features of most common GaN-on-SiC technologies, while drawing on additional benefits, including a reduced production cost, driven by larger wafers.

GaN-on-silicon: Concerns...

At this stage, doubts surround the suitability of GaN-on-silicon HEMTs for satellite communication. While studies have proven that GaN-on-SiC power amplifiers are a worthy replacement for tubes for several applications, the prospects for the GaN-on-silicon amplifier are held back by concerns related to thermal management and passive structure losses.

There is good reason to question the thermal management of the GaN-on-silicon HEMT, given that the thermal resistance of this material system is roughly double that of its GaN-on-SiC counterpart, due to the inferior thermal conductivity of the substrate. Regardless of the substrate type, the junction temperature of a GaN device is limited to ensure reliability in space – the European Space Agency insists that it does not exceed 160 °C. Due to this constraint, the dissipated power density for GaN-on-silicon technology can only be half of that for its SiC counterpart, and for equivalent devices, RF power density is also halved.

To illustrate this, consider two 4 x 75 µm technologies, differing only in the substrate type (they have the same bias voltages, gain, power density, efficiency and so on). The GaN-SiC device produces an RF output power of 1.5 W, equating to a power density of 5 W/mm. The associated power-added efficiency is 50 percent, and the gain 10 dB. The performance is realised at a junction temperature below 160 °C, by restricting the base plate to 80 °C, conditions that lead to a power dissipation of 4.5 W/mm.

In comparison, the equivalent silicon device, having the same power-added efficiency, gain and periphery, has to operate at half the power density and power dissipation to ensure a junction temperature below

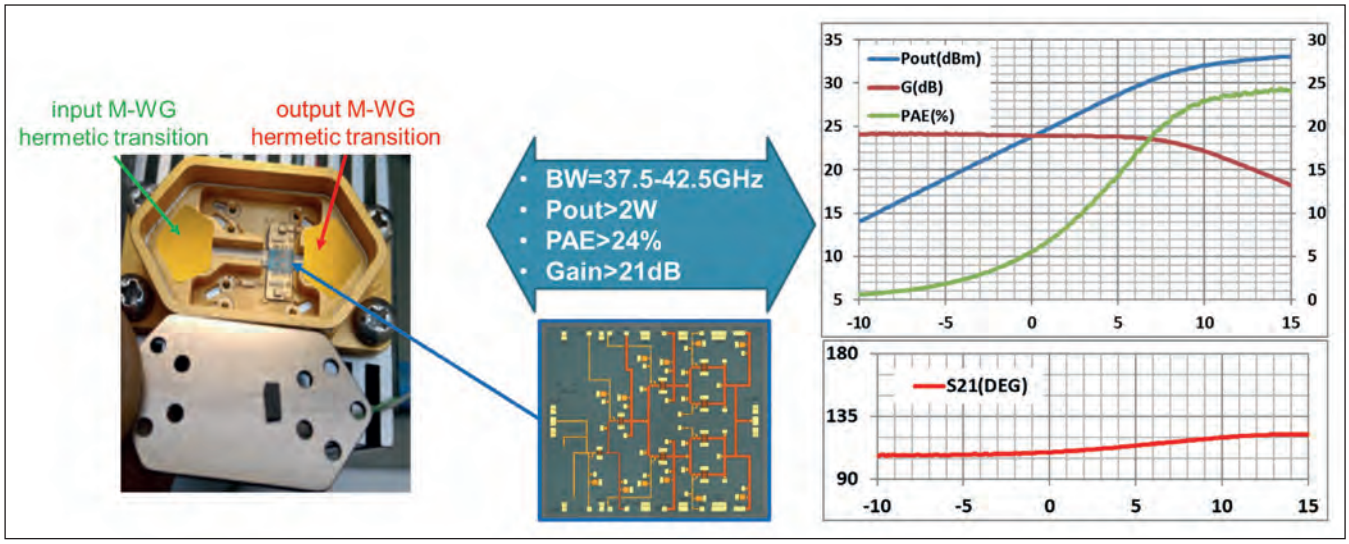

Figure 4. The assembled MMIC provides good performance at 40 GHz.

160 °C. To fulfil this requirement, the power density is limited to 2.5 W/mm, while power dissipation is around 2.25 W/mm.

Concerns related to losses in passive structures made from GaN-on-silicon are focused on the transmission lines. Simulations suggest that the insertion loss of a 1 mm length 50 Ω transmission line in the Q-band is 0.13 dB higher for GaN-on-silicon than it is for GaN-on-SiC (see Figure 1). This insight shows that when designing an amplifier with GaN-on-silicon technology, it is better to synthesize matching networks using lumped elements than distributed ones.

...and strengths

There are some remarkable advantages associated with GaN-on-silicon, including a lower material cost and access to larger wafers, which are well-suited to production volumes for 5G. By producing amplifiers from GaN-on-silicon, risks of import/export restrictions are diminished, making it easier to procure material.

And last but by no means least, GaN-on-silicon is compatible with heterogeneous integration in SiGe/CMOS technologies, so it offers many opportunities for making highly integrated, multi-functional chips. To help drive adoption of the GaN-on-silicon power amplifiers in tomorrow's communication satellites, our Italian collaboration – a partnership between researchers at the University of Rome 'Tor Vergata' and Thales – has built and characterised a Q-band GaN-on-silicon power amplifier. It features an RF tray, formed using a waveguide structure to combine sixteen MMIC power amplifiers realised with a commercial 100 nm gate length GaN-on-silicon process.

Despite the inherent drawbacks of the GaN-on-silicon HEMT, our power amplifier produces more than 20 W, has a noise-to-power ratio exceeding 18 dB, and operates at a power-added efficiency in excess of 15 percent. Shown in Figure 2 is the RF line-up of this amplifier, which delivers a level of performance that showcases the outstanding potential of GaN-on-silicon technology for space applications.

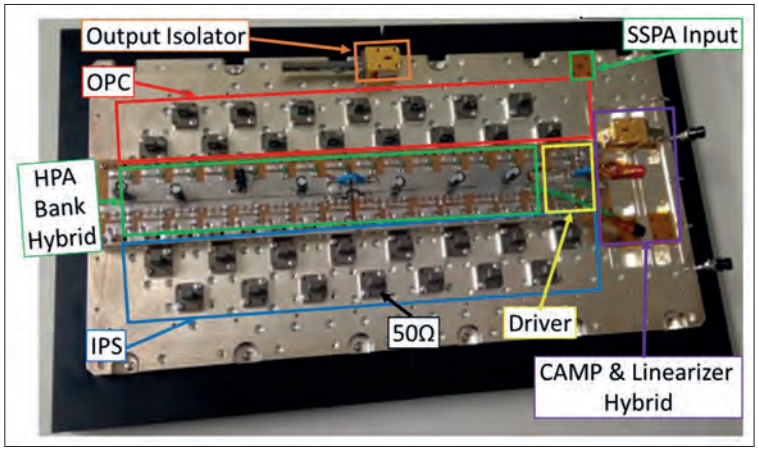

Figure 5. The splitter/combiner structures delivers an encouraging performance from 35 GHz to 45 GHz.

The first part of our power amplifier is the channel amplifier that provides an output of around -3 dBm. This sub-unit has a cascade of several low-level amplifiers and variable/fixed attenuators, carefully chosen to control the uplink flux, which can be adjusted by either ground telecommands – a fixed gain mode – or by an automatic level control loop. The latter is capable of compensating for in-orbit ageing of power amplifier gain, using a feedback signal provided by an integrated detector.

Downstream of the channel amplifier is a linearizer, primarily there to compensate for the nonlinearity of the high-power-amplifier bank that follows. The linearizer is designed to provide, as much as possible, equal but opposite amplitude-to-amplitude and amplitude-to-phase distortions with respect to those experienced by the high-power-amplifier bank.

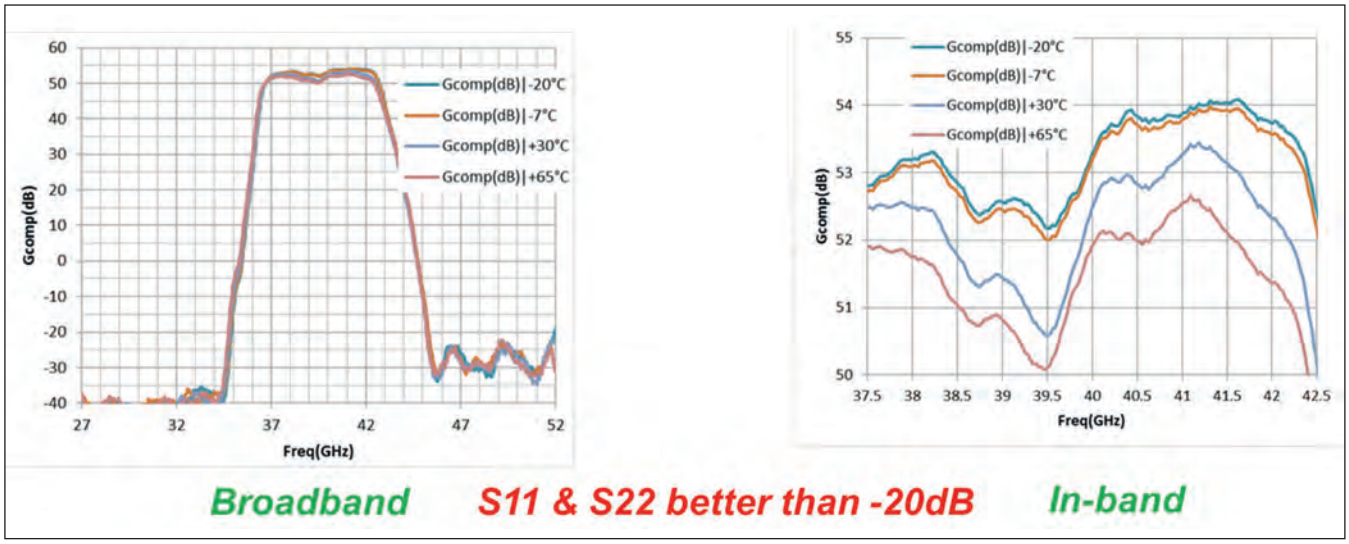

Figure 6. Measured small-signal performances of the solid-state power amplifier.

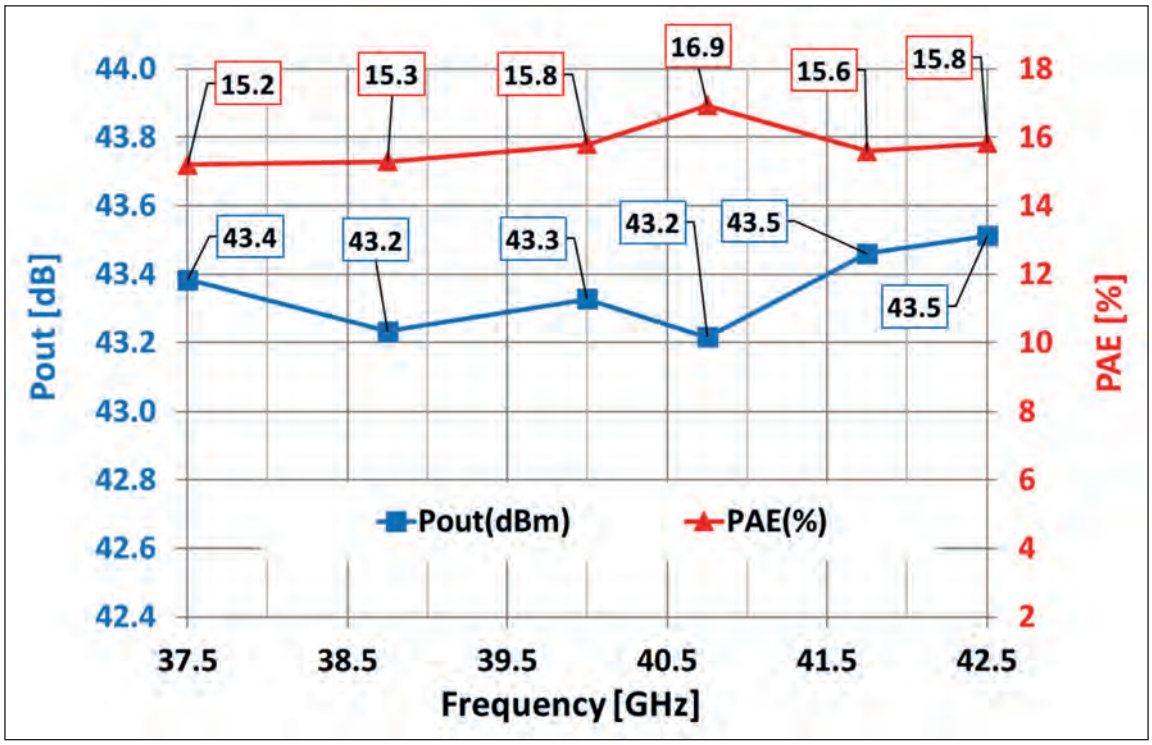

Figure 7. Measured large-signal performances of the solid-state power amplifier.

Controlling the overlap between the expansion of the linearizer and the compression of the high-power-amplifier bank is a setpoint control attenuator. In this arrangement, the linearizer compensates for up to 7 dB of gain compression and +/- 45° of phase variation, and provides a constant output power of 7 dBm.

The signal from the linearizer is fed to the high-power-amplifier hybrid, which drives, in a 1-to-16 ratio, the high-power-amplifier bank. The last two sub-units are implemented in an WR-22 waveguide, and exploit the MMIC PA developed ad-hoc on a commercial 100 nm gate length GaN-on-silicon process available at the Ommic foundry.

During the development of our MMIC, we devoted much effort to accounting for the thermal, electrical and physical constraints of GaN-on-silicon technology. This included undertaking a series of load-source pull simulations on devices with a different geometry, evaluated using the centre frequency, which is 40 GHz. For each geometry, as well as calculating the output power, power-added efficiency and gain, we considered the resulting junction temperature. For this work we assumed a base plate temperature of 80 °C, which corresponds to the maximum value expected below the MMIC.

For our load-pull simulations, we selected the optimum load impedance for the 4 x 75 µm device (the values for the output power, power-added efficiency, and junction temperature are shown in Figure 3). To ensure that we comply with the de-rating rules while maximizing the output power, we have selected a load impedance that is between those for maximum power and power-added efficiency, and we produce a junction temperature contour that is slightly lower than 160 °C. By adopting these conditions, we give ourselves a margin when implementing our actual MMIC. Although this choice sacrifices efficiency performance by about 1 percent, it guarantees fulfilment of the power level requirement at the circuit level.

Drawing on the results of our load-source pull simulations, we have undertaken a power budget analysis. Insights provided by this led us to design a MMIC based on a four-stage corporate architecture, with a final stage comprising four 4 x 75 µm devices driven by the same device in a 1:2 ratio. For the second and first stage, we used a single 8 x 50 µm and a single 2 x 50 µm device, respectively.

All of the MMICs used to form our power amplifier are equipped with an input and output microstrip-to-waveguide hermetic transition. This is visible in the picture of our MMIC, shown in Figure 4 alongside plots illustrating typical performance from 37.5 GHz to 42.5 GHz. Output exceeds 2 W, while the associated efficiency and gain are greater than 24 percent and 21 dB, respectively.

We have connected sixteen MMICs in the high-power-amplifier bank using a WR-22 waveguide splitter/combiner network. In our design there are fifteen T-magic structures, with a response that has been carefully optimised to minimize losses while ensuring a matching better than 20 dB at all ports. A waveguide isolator is added at the output side to improve the

matching of the high-power-amplifier bank. We have measured losses for both the splitter and the combiner of 0.8 dB, and 0.3 dB for the isolator, giving a loss for the network of 1.9 dB.

Our power amplifier, including the WR-22 waveguide input and output isolators, weighs 5.5 kg and has dimensions of 45 cm by 22 cm by 7.2 cm (a picture is shown in Figure 5). This unit is powered by two positive voltages – 3.5 V, provided by GaAs devices, and 11.25 V, produced by GaN devices – and has a single bias voltage of -8.0 V, conditioned for the gates. For space applications, the thermal design of the amplifier is of upmost importance.

It is critical that the junction temperature of any active device does not exceed a safe figure for that particular technology, in order to guarantee reliable operation over the satellite lifetime, typically 15 years. For our amplifier, accurate thermal and mechanical design ensures that the hottest GaN-on-silicon MMIC never exceeds 160 °C, so long as the base plate temperature is no more than 65 °C.

Measurements of small-signal performance of our amplifier for base plate temperatures ranging from -20 °C to +65 °C, when the automatic level control loop is active, show that the forward voltage exceeds 53 dB, with a ripple lower than +/- 1dB in the overall operating bandwidth of 37.5 GHz to 42.5 GHz (see Figure 6). Input and output return losses are better than 20 dB, and gain variation over temperature is limited to less than 2 dB over 85 °C.

We have also measured our amplifier's performance for a fixed gain of 65 dB at a base plate temperature of 65 °C. Saturated output power exceeds 20 W, with a power-added efficiency exceeding 15 percent, aided by a DC-DC converter efficiency of 90 percent (see Figure 7). Overall power consumption is 155 W at saturation, falling to 100 W for a 3 dB back-off, corresponding to a 10 W RF output power. Alongside efficiency, the linearity of a power amplifier is of paramount importance.

Linearity is critical in applications that include very-high-throughput satellites, which involve the use of time-varying envelope signals that feature a significant peak-to-average power ratio. We evaluate our linearity by measuring the noise-to-power ratio. This figure-of-merit, determined by driving our amplifier with hundreds of uncorrelated carriers, is 18 dBc (average) at an output power of +43 dBm (see Figure 8).

Our results compare well with other solid-state power-amplifiers, and highlight that GaN-on-silicon technology, despite its differences to GaN-on-SiC, can still yield high-performing power amplifiers in the Q-band for serving space applications.

Despite trailing travelling-wave tube amplifiers in efficiency – for the same power levels, they can hit 20 percent – our GaN-on-silicon-based design has a great deal to offer, combining a lower cost with graceful degradation and selectable form factor. The upshot is a significant benefit for satellite designers.

The authors wish to acknowledge the Italian Space Agency (ASI) for funding this work in the context of project KALOS-DEVAQ within ESA's ARTES C&G Technology Program. Particular thanks are due to Francois Deborgies from ESA/ESTEC for his expertise and technical support.

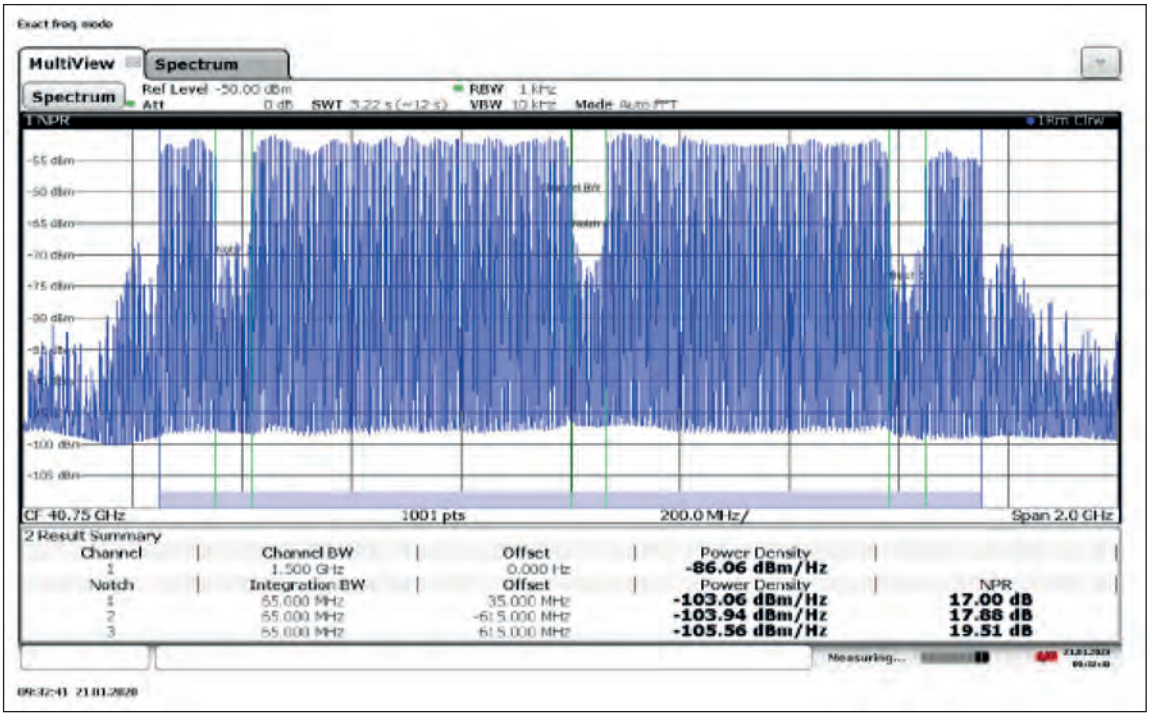

Figure 8. Measured noise-to-power (NPR) of the solid-state power amplifier (SSPA). This measurement was made by driving the SSPA with 301 uncorrelated carriers occupying a frequency band of 1.5 GHz large and applying three notches 65 MHz large.

Disrupting the tubes market with high-voltage GaN HEMTs

GaN HEMTs operating at voltages of up to 150 V outperform vacuum tubes by combining high performance with greater reliability, longer lifetime and lower operating costs

BY GABRIELE FORMICONE, JEFF BURGER, JAMES CUSTER AND JOHN WALKER FROM INTEGRA TECHNOLOGIES

INVENTED PREDOMINANTLY in the first half of the twentieth century, vacuum electron devices (VEDs) have a long history as a critical component enabling satellite communications, radar systems, high-energy particle accelerators, and other applications requiring high output power, wide operating bandwidth and high efficiency. VEDs include traveling-wave tubes and klystrons.

While VEDs are an accepted technology, they suffer from multiple weaknesses, many of which can be addressed by semiconductor-based solid-state amplifiers, which have become the mainstream technology in the lower power, lower frequency VED market. Semiconductor-based solutions deliver longer lifetime, superior ruggedness, and higher reliability, and reduce overall system size, weight, and costs. Yet despite all this success, solid-state sources have yet to penetrate the high end of the market for high power, multi-kilowatt applications.

Modernization of high-power RF communication

and data transmission systems will push the requirements of what traditional VEDs can deliver. In addition, system architects are demanding more efficient power sources to meet green requirements while driving down operating costs over the system life. Thanks to the pioneering work of our team at Integra Technologies Inc., a market leader in RF and microwave high power devices, we have achieved a breakthrough by pushing the operating voltage for this class of device to a new high, raising the bar for high efficiency GaN-on-SiC technology. These efforts draw on our long heritage of silicon bipolar and GaN/SiC RF high power expertise at 28 V and 50 V, with our latest success representing yet another milestone in our advancements in green technology, which date back to 2013. The ground-breaking progress that we have made enables high-voltage GaN/SiC-based HEMTs to offer a compelling commercial alternative to the VED.

The foundation for our advanced R&D activity is our portfolio of proprietary epitaxial structures. They are specifically developed for high-power RF applications, and benefit from decades of refinement, realised through close collaborations with our high-power customers.

Leveraging this field-proven IP, we have developed new epitaxial structures specifically designed for high-voltage operation. In addition to this advance, we have introduced and then patented innovated circuit and thermal management techniques specifically for high power operation. Benefiting from all this progress, our devices can now operate at voltages of up to 150 V, resulting in a dramatic improvement in output characteristics.

Our latest generation of high-voltage GaN/SiC devices, which produce pulsed power densities up to more than 20 W/mm, enables the production of solid-state devices with an output power of several kilowatts. Critical to the performance of the next high-power-generation green platforms, our HEMTs deliver sufficient gain, efficiency, and reliability to enable these systems to fulfil their performance targets. Our devices are manufactured in a mainstream wafer fabrication foundry, using commercially available, production-ready materials.

Increasing power and dynamic range

At last year's International Microwave Symposium, our company demonstrated the incredibly high output powers that can be produced by RF GaN/SiC transistors operating at elevated voltages of between 100 V and 150 V. We reported 2 x 50 mm gate periphery die yielding 1.2 kW when operating in CW mode at 100 V, and producing 2.3 kW when driven at 145 V using 100 µs-wide pulses and a 5 percent duty cycle. Plots of power gain and drain efficiency versus output power for these devices, which have a drain efficiency of 80 percent when operating in both modes, are shown in Figure 1. Two key features

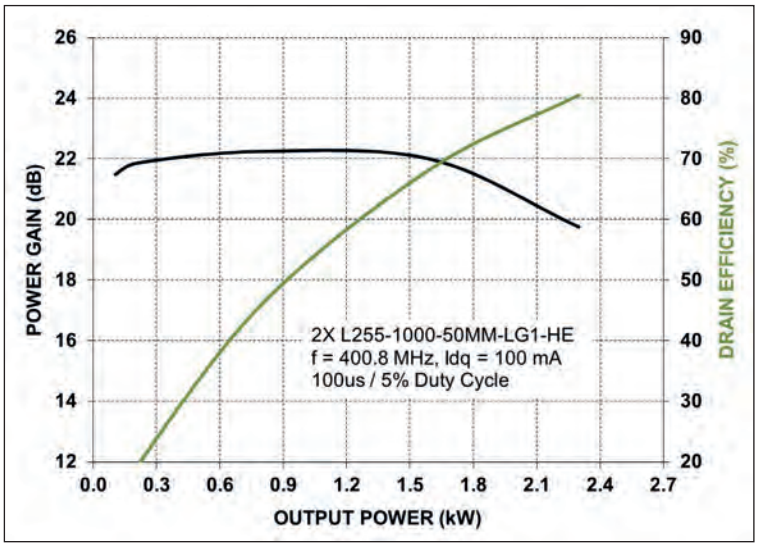

Figure 1. Measured RF power gain and drain efficiency versus output power at 145 V bias and 400.8 MHz. Quiescent current is 100 mA. 6 Ω series gate resistors help to stabilise the transistor with 20 dB gain at 2 dB compression and 2.3 kW saturated power. Drain efficiency peaks at 80 percent. In CW operation at 100 V bias, saturated power is 1.2 kW with the same 80 percent peak drain efficiency.

of this amplifier's design are harmonic tuning, used to realise high efficiency, and patented thermal enhancement techniques that help mitigate heat dissipation in such high-power density transistors. We have designed the devices and circuits to operate at 400.8 MHz. This is the frequency employed in today's largest particle accelerators, and also a frequency of interest for long-range, early-warning radar systems.

Our technology enables a single transistor to produce a CW power level of 2 kW and a pulsed output of 4 kW at an efficiency greater than 70 percent. With this level of performance, megawatt power levels can be realised with fewer combiners and lower related losses. By comparison, off-the-shelf 50 V RF technology would require massive power combiners

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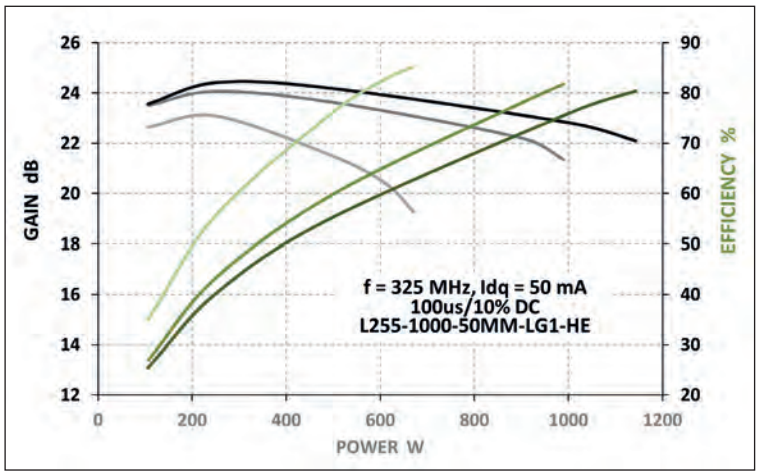

Figure 2. Measured RF power gain and drain efficiency versus output power for a 50 mm die with a signal of 100 μs pulse width and 10 percent duty cycle at 325 MHz. The device is characterized at 100 V, 125 V and 145 V DC bias demonstrating a 3 dB power dynamic range. By reducing operating bias to 50 V a 6 dB dynamic range is achieved.

to achieve similar performance, degrading system efficiency, while increasing the complexity of heat extraction. We also showcased the design flexibility of this technology by increasing the operating voltage to 150 V at the 2020 European Microwave Week. In this forum, we reported a single 50 mm gate periphery die that produced a 3 dB power dynamic range when modulating its operating bias from 100 V to 125 V and then on to 145 V (see Figure 2).

This amplifier's devices and circuits are designed to operate at 325 MHz, targeting large particle accelerators. Our single semiconductor die delivers a 1.1 kW peak power at 145 V with 80 percent peak efficiency. The peak power decreases by about 3 dB at 100 V bias.

Going to even lower voltages can offer additional benefits. When we dial back the bias to 50 V, peak power can be modulated by around 6 dB while still preserving 80 percent peak efficiency; and we can realise additional dB of dynamic range by reducing the operating bias towards 28 V or 32 V. We have obtained similar results, also announced at European Microwave Week, with a power amplifier designed to operate at 650 MHz.

Such a great dynamic range is a key enabler in high-power RF systems. It allows multi-use or functionality, and it also enables older systems to be upgraded to combine legacy performance with additional state-of-the-art capabilities. For the high-power devices we reported at the most recent International Microwave Symposium and European Microwave Week, the peak channel temperature is only around 150 °C. Such low temperatures are realised from proprietary techniques that enhance heat flow from the hottest spots of the active region.

Our R&D activities have extended to considering the bandwidth associated with the higher power densities and higher load impedances at 100 V and 150 V. Power-over-bandwidth is a 'hot button' in several applications, with requirements that may be strictly application-specific and not discussed in the public domain. What we can say, nonetheless, is that broadband high-power applications are destined to reap huge benefits from our 100 – 150 V amplifier technology.

System-level benefits

As mentioned earlier in this article, the higher voltage GaN transistors can achieve power densities of more than 20 W/mm, thus allowing for reduced circuit complexity for the same relative power level. As an example, two 1 kW transistors running at 50 V could be replaced by a single 2 kW transistor operating at 100 V. This eliminates one transistor and the combining structure required for the lower voltage solution.

Another advantage of a higher voltage is evident in a simple load-line analysis. While a 50 V device will provide a 25 W output power with just a 50 Ω load, a 100 V device will provide four times this power.

For broadband applications, higher voltage GaN HEMTs can also be an advantage, considering that the device impedances increase with higher voltage operation and the capacitance-per-Watt are reduced. Lower voltage solutions require larger impedance transformations to achieve bandwidth, while a higher voltage solution can eliminate these transformers or reduce transformation ratios and their complexity. When utilizing 100 V GaN, the matching structure size can be reduced by a factor of two or more by removing transformers over a 50 V GaN solution for the same RF output power.

There is no doubt that much is to be gained from increasing the operating voltage of the GaN HEMT. There are benefits for the device itself, including an increase in output power, plus plenty of advantages at the circuit and system level. Our company is in talks with several VED's users to commercialize our high-voltage GaN/SiC green technology.

Further reading

G. Formicone et al. "A 2.3 kW 80% Efficiency Single GaN Transistor Amplifier for 400.8 MHz Particle Accelerators and UHF Radar Systems", IEEE-MTTS International Microwave Symposium, 2020.

G. Formicone et al. "A GaN/SiC UHF PA for Particle Accelerators with 100-145V Quasi-Static Drain Modulation," European Microwave Week, 2020.

G. Formicone et al. "Targeting radar with 150 V RF GaN HEMTs" Compound Semiconductor magazine, March 2016.

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Bi-directional converters benefit from CoolSiC MOSFETs

BY DAVID MENESES HERRERA, SENIOR STAFF APPLICATION ENGINEER, AND NICO FONTANA, SENIOR STAFF PRODUCT DEFINITION ENGINEER,INFINEON TECHNOLOGIES

STORAGE OF SOLAR and wind renewable energy is increasingly important and batteries are a practical solution. They can be used at any scale from utility to domestic with costs dropping, driven by the EV market. Additionally, while carbon-based fuels are still in the mix, batteries can usefully feed back in to the grid to provide 'peak shaving' for a more reliable and cost-effective supply and a cash rebate to domestic or industrial consumers. In this case, a bi-directional power converter is required to charge the battery from AC or the renewable source and alternatively 'feed-in' energy back to the AC line when there is light or no local load. EV batteries can also be included in the arrangement.

Bi-directional converter efficiency is key

Efficiency of bi-directional converters is clearly a key issue for effectiveness and payback in solar energy systems. It is now common for individual stages in power converters to achieve 99%+ efficiency, but bi-directional converters are more difficult to optimize with their forward and reverse energy flow.

Fortunately, when MOSFETs are used for switches and synchronous rectifiers, they can normally be configured as bidirectional. Figure 1 shows an outline bi-directional battery charger/inverter and the left to right symmetry should be evident, with energy flow direction controlled by MOSFET drive arrangement The power factor correction stage shown is typically a 'bridgeless totem-pole' type which is optimum at medium power levels, or higher with interleaving. Its efficiency however is limited by the body diode of the two MOSFETs which act as a boost diode on alternate polarities of AC supply. For low conduction losses, the circuit is 'hard switched' in continuous

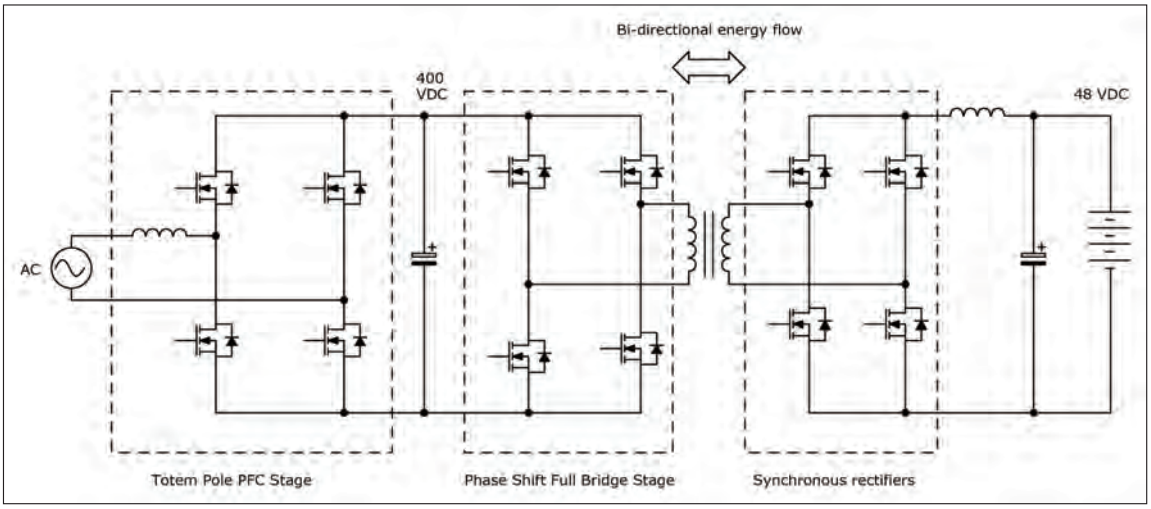

Figure 1: MOSFETs in bridge arrangements as a bi-directional power converter

conduction mode and charge is stored in the body diode in the dead time between MOSFET channel on- and off-states. Recovery of this charge each cycle leads to power loss and EMI and the effects can be severe when silicon MOSFETs are used. Excessive power loss can also occur if the MOSFET has a high output charge QOSS, which must be charged and discharged each cycle.

The DC-DC stage shown in Figure 1 as a resonant 'phase-shift full bridge' type is not affected by body diode reverse recovery except perhaps transiently at start-up, shut-down or with load steps.

However, this converter can also be affected by a high value of QOSS, making resonant operation difficult to maintain under all conditions. A high value also forces a minimum dead time, limiting high frequency operation.

SiC MOSFETs solve the problems

The problems discussed are largely solved by using silicon carbide (SiC) MOSFETs. Reverse recovery charge is about 20% of the value for a similar class si-MOSFET and QOSS is around one sixth. The CoolSiC™ SiC MOSFET 650 V (IMZA65R048M1H) from Infineon for example, has 125nC charge compared with 570nC for their silicon-based 600 V CoolMOS™ CFD7 superjunction MOSFET (IPW60R070CFD7) with its similar on-resistance.

Variation of output capacitance and resulting QOSS is much less with SiC MOSFETs. Figure 2 shows how the IMZA65R048M1H CoolSiC™ MOSFET changes by 10x between low and high drain voltage, but the figure for a superjunction si-MOSFET is closer to 8000x. The non-zero value for SiC at high voltage can be a benefit as it helps to reduce voltage overshoot on the drain, which would otherwise require a high gate resistor value, reducing controllability.

Reference design demonstrates SiC advantages

An Infineon reference design (EVAL_3K3W_TP_PFC_

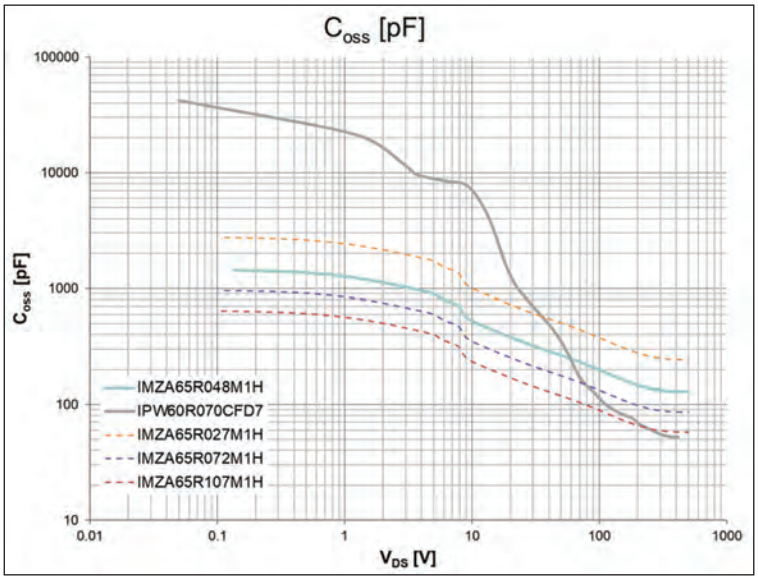

Figure 2: SiC device output capacitance varies far less with drain voltage than silicon

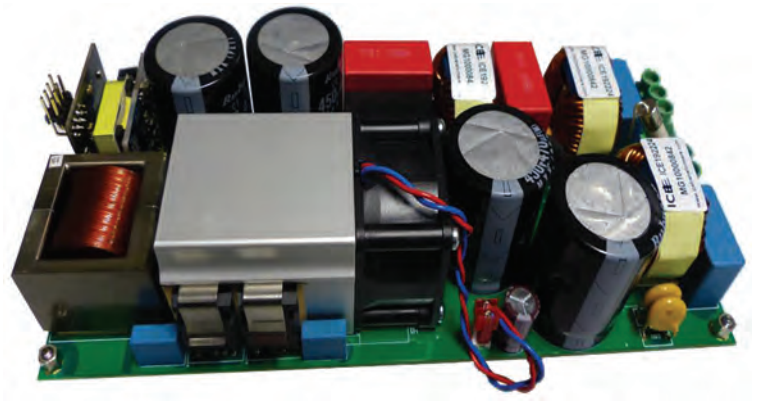

Figure 3: Infineon high efficiency, bi-directional, totem-pole PFC stage demonstrator, using SiC MOSFETs

SIC) [1], (Figure 3) demonstrates the performance of SiC MOSFETs in a bi-directional, 3.3 kW totem-pole PFC stage, achieving 73 W/in3 (4.7 W/cm3) power density with a peak efficiency of 99.1% at 230 VAC input and 400 VDC output. In inverter mode efficiency peaks at 98.8%. Control is fully digital using the Infineon XMCTM series microcontroller.

Conclusion

CoolSiCTM MOSFETs offer clear advantages in bi-directional converters and are available from Infineon in discrete and module formats, along with a complementary range of EiceDRIVERTM gate drivers. Current sensing ICs and microcontrollers for digital control are also available.

FURTHER READING

For more information on the CoolSiC™ MOSFET 650 V products and related boards, please visit www.infineon.com/coolsic-mosfet-discretes.

References

[1] 3300 W CCM bi-directional totem pole with 650 V CoolSiC™ and XMC™ Infineon application note AN_1911_PL52_1912_141352

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How robust is the SiC MOSFET?

Researchers at the International Reliability Physics Symposium report the results of investigations into the impact of defects and gate oxide quality on the performance of the SiC MOSFET

BY RICHARD STEVENSON

THE SiC MOSFET is guaranteed a great future. Thanks to its capability to efficiently control current at high voltages, sales are accelerating in a multitude of applications, including electric vehicles, solid-state circuit breakers, and various types of motors. Multi-billion dollar revenues are sure to follow.

However, exactly how much success the SiC MOSFET will have is not set in stone. Factors weighing heavily on this are price, performance, and reliability. And of these three, reliability is arguably the most critical. That's because many of the adopters of this device will really value robustness, as this allows them to foster a reputation for producing products that never fail. Efforts within the SiC community continue to take the reliability of the SiC MOSFET to a new level. At the recent *International Reliability Physics Symposium* (IRPS), a forum with a rich history in considering the long-term health of silicon devices, several presentations considered the robustness of the SiC MOSFET.

At this meeting, held on-line due to Covid-19 restrictions, the likes of Infineon, STMicroelectronics and On Semiconductor provided insights into the impact of defects on the lifetime of the device, and offered options for assessing reliability of the gate oxide.

Hidden assassins

Today, most SiC devices are produced using 150 mm SiC substrates. The quality of this foundation has improved a great deal over the last two decades. However, even state-of-the-art substrates grown by physical vapour transport are far from perfect. It is the norm for them to have around ten thousand defects per square centimetre, according to conference speaker Thomas Neyer from On Semiconductor.

Neyer's presentation considered many different forms of defect that occur in SiC MOSFETs. He explained that one common option for exposing them is to treat the material in molten potassium hydroxide, and then examine the wafer under a microscope.

But he prefers to classify defects with non-destructive approaches, such as photoluminescence techniques, X-ray topography and imaging with cross-polarised light. Using these techniques to record defects allows the performance of devices to be correlated with the type of imperfection. So powerful is this approach that it is even possible to relate device performance to the actual number of defects in a particular die.

It would be easy to blame all the defects found in epiwafers on imperfections in the boule. That's misleading, however, explained Neyer, who pointed out that they can also be introduced in the slow and costly wafering process flow, involving slicing, grinding and polishing. When substrates are formed from a boule, this creates nanoscale dislocations with open cores that hamper the quality of SiC epilayers.

Neyer and his co-workers have categorised the defects found in SiC epilayers into three groups: killer visible defects, which include triangular types of defect, strong topographic defects and carrots; non-killer visible defects, such as obtuse triangles, scratches, pits and V-type defects; and non-killer crystal defects, such as stacking faults, basal plane dislocations, grain boundaries and bar stacking faults (see Figure 1 for more details).

Investigations at On Semiconductor have uncovered the impact of non-killer defects through a study that considered around 3 million devices with a 9 mm^2 die size – they are a combination of Schottky diodes and MOSFETs. According to Neyer, this survey showed that a significant proportion of devices have five or more defects per die. This begs the question: does device performance drop off with more non-killer defects?

The answer is nuanced. For Schottky barrier diodes, an increase in non-killer defects has little impact; but for MOSFETs, the opposite is true – and when a die has more than 10 non-killer defects, this is more of concern than a killer defect. Non-killer defects are to blame for early life rejects, burn-in failures, and outliers in short circuits and avalanche tests.

Neyer and co-workers also discovered that SiC MOSFETs with double-digit numbers of stacking faults have a wider distribution in key device characteristics. Average values for the leakage current and its standard deviation both increase markedly, while values for the breakdown voltage and threshold

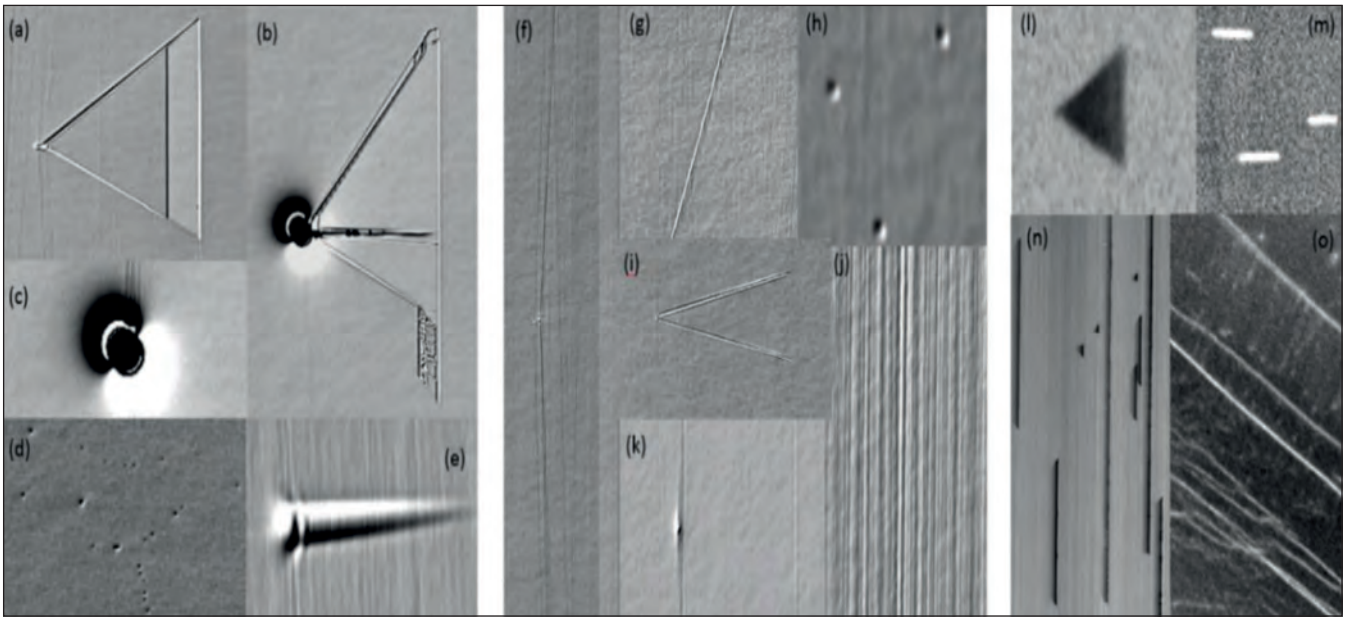

Figure 1. Researchers at On Semiconductor have categorised SiC defects into three classes: killer visible defects (left), non-killer visible defects (middle), and non-killer crystal defects (right). Examples of killer visible defects are (a) triangular defects, (b) particle triangles, (c) particles/downfalls, (d) strong topographic defects and (e) carrots. Non-killer visible defects include (f) obtuse triangles, (g) scratches, (h) pits, (i) V-type defects, (j) roughness/step bunching and (k) small topographic defects. Non-killer crystal defects include (l) stacking faults, (m) basal plane dislocations, (n) bar stacking faults, and (o) grain boundaries.

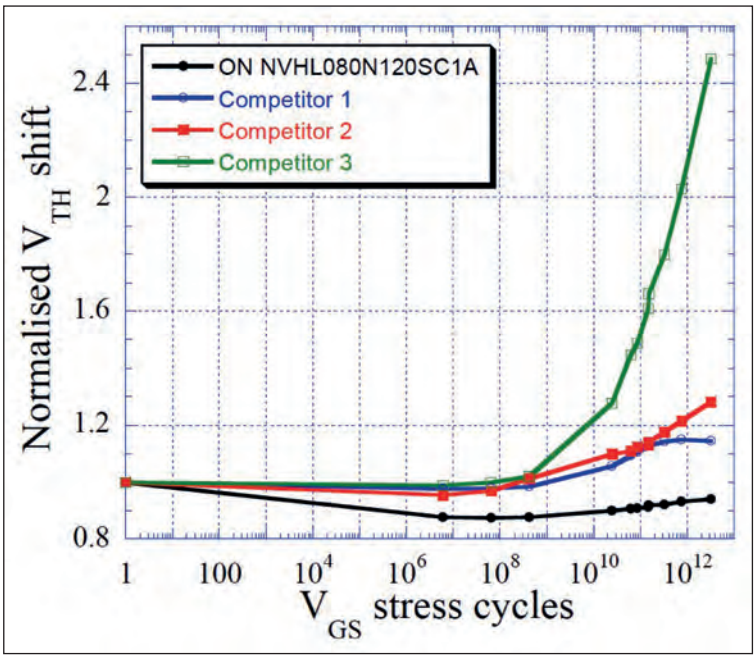

Figure 2. Engineers at On Semiconductor benchmarked their SiC MOSFET against that of three competitors using a gate-source stress at 100 kHz and a 50 percent duty cycle.

voltage – these depend on extraction currents – decrease as the number of stacking faults per die increases.

Another investigation by the team from On Semiconductor considered bipolar degradation in the SiC body diode of the MOSFET. This technique, widely employed for evaluating 3.3 kV devices, has been applied by Neyer and co-workers to MOSFETs designed to handle 1200 V and 1700 V.

After stressing these devices for between one and three days with a DC drain-source current of 60 A cm^{-2} and a gate-source voltage of -5 V, the engineers found that the greater the basal plane dislocations per die, the greater the shift in on-current.

For 1200 V devices, the team recorded an increase in on-current of almost 2 percent for a die with 35 basal plane dislocations, while for the 1700 V equivalent, 30 basal plane dislocations were behind an up-tick in on-current of almost 7 percent.

Encouraging results have come from benchmarking the threshold voltage stability of On Semiconductor's MOSFETs against rival SiC products with planar and trench architectures. Using a gate-source stress at 100 kHz and a 50 percent duty cycle, this device exhibited greater stability than its three competitors used in this study (see Figure 2).

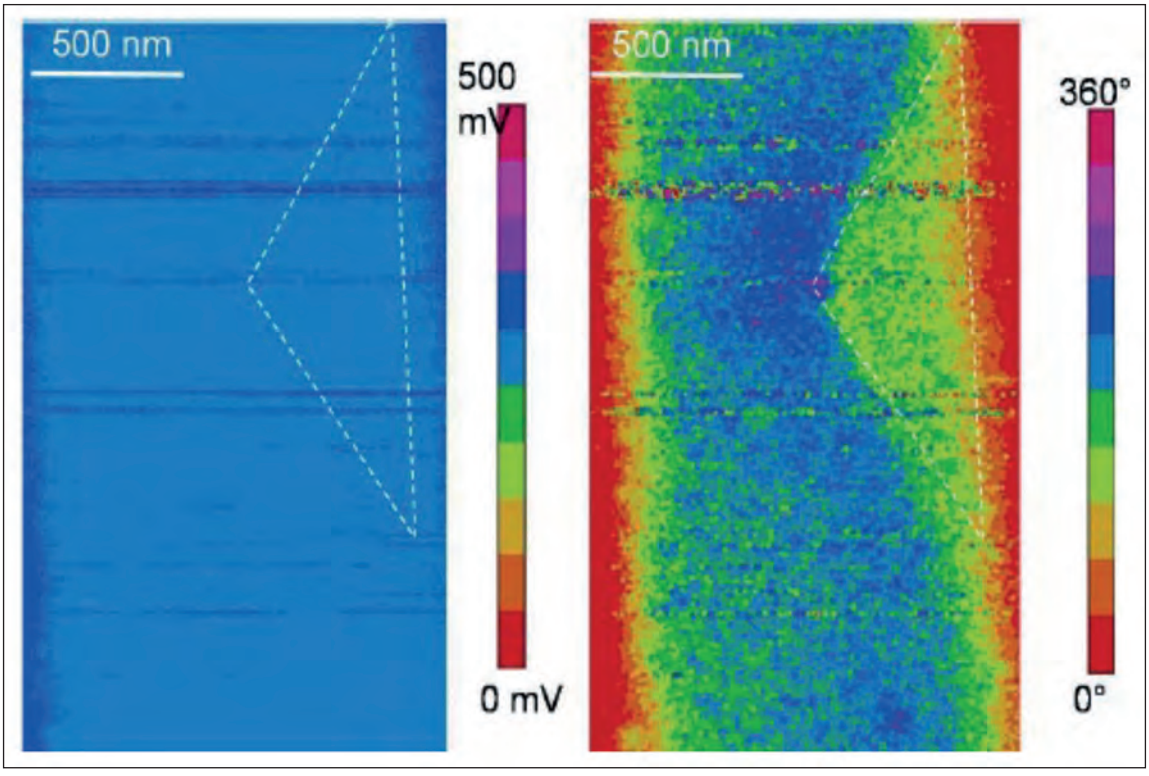

Figure 3. Investigations of threading dislocations by a partnership between CNR-IMM and STMicroelectronics have involved scanning capacitance microscopy measurements. A map of the amplitude of this signal (right) reveals a constant doping concentration; the phase of the signal (left) uncovers local variations in minority carrier concentration, and enables identification of a charge distribution associated with a triangular defect.

Troublesome triangles

Studies of the role of defects on the MOSFET's breakdown have also been conducted by a team from CNR-IMM, Italy, working in collaboration with STMicroelectronics. Speaking on behalf of this partnership, Patrick Fiorenza from CNR-IMM argued that efforts to understand infant mortality have to begin with wafer level tests involving thousands of devices. He pointed out that it is critical to differentiate between extrinsic breakdown, which happens during the early life of a device, and intrinsic breakdown.

Fiorenza provided an example of a device that had failed instantly. Imaging this device by emission microscopy and scanning electron microscopy revealed a surface pit, which has a hexagonal nature, according to differential atomic force microscopy. When the team delved more deeply into this imperfection with cross-sectional scanning electron microscopy, they found a region with a polytype within the substrate. Weighing up the implications of this finding, Fiorenza concluded: "We have to take care of the fabrication steps, in particular the epitaxial growth of the material."

He added that when working at the buffer level, it is also worthwhile to check the gate current: "This is important to understand if some extrinsic failure can be intercepted before finalisation of the fabrication." At very low electric fields – such as just 4 MV/cm, which ensures no threat of insulator damage – he and his co-workers have found that it is possible to observe gate currents that don't follow the ideal Fowler-Nordheim behaviour. Looking at devices with this attribute in more detail, the team have identified compromised devices that failed high-temperature gate bias tests, due to surface bumps that are seen in atomic force microscopy images.

Devices passing this test were packaged, before undergoing a high-temperature stress test at a 600 V reverse bias. The 2 percent of devices that failed this test, lasting 3 months and involving an elevated temperature of 140 ° C, exhibited a hike in gate current of around seven orders of magnitude. In addition, their characteristics changed dramatically, such as moving to normally-on behaviour.

Imaging the surface of the device with a focused ion beam failed to shed any light on the cause of failure of the MOSFETs. So Fiorenza and co-workers removed the poly-silicon metal gate and the gate oxide, before inspecting the structure once more. This time they discovered triangular defects in the JFET region of the MOSFET. Using a two-beam form of transmission electron microscopy, they found a mixed edge and screw dislocation.

Additional analysis of this stripped back sample, using other forms of probe-based microscopy, enhanced the team's understanding of this imperfection and its consequences. Local current measurements

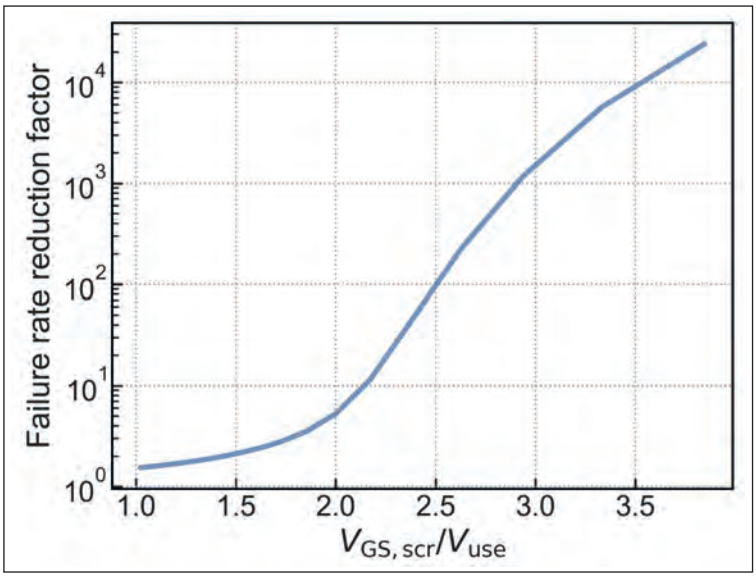

Figure 4. Engineers at Infineon have drawn on previous work (Aichinger and Schmidt, IRPS2020, 3B4_042) that relates a failure rate reduction factor to the ratio of the screening voltage ($V_{GS,scr}$) to the recommended gate use voltage provided by a datasheet (V_{use}). Combining this relationship with rapid stress tests enabled a comparison of the reliability of SiC MOSFETs produced by various vendors.

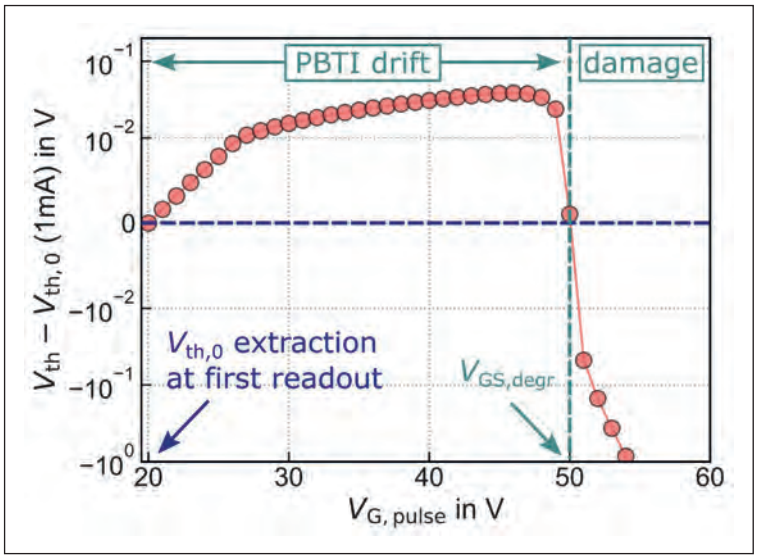

Figure 5. Infineon has developed a new form of stress test for SiC MOSFETs. A series of voltages are applied, each 1 V higher than the previous one, and the threshold voltage is recorded. As the stress voltage incrementally increases, initially the threshold voltage increases as well, due to a positive bias temperature instability. But beyond a certain value the threshold voltage plummets and the device is irreversibly damaged.

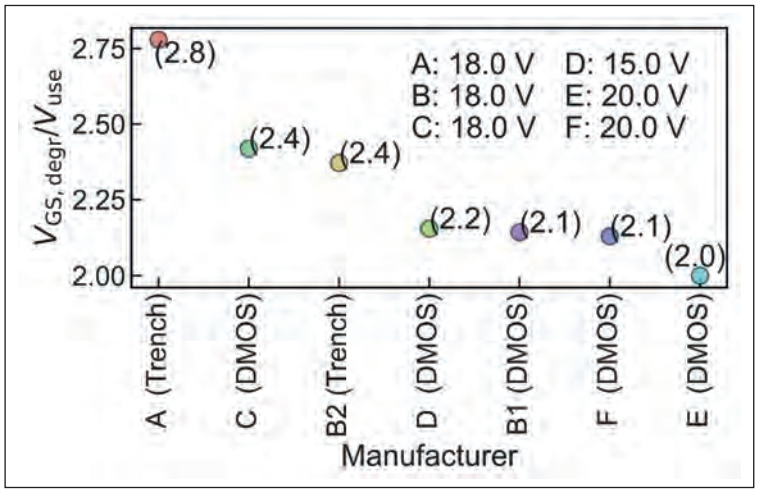

Figure 6. Research at Infineon has uncovered a difference in the failure rate reduction factor of two orders of magnitude between SiC MOSFETs made by different manufacturers. This implies that the most reliable devices have roughly one hundred times fewer failures in the field than the most unreliable devices.

revealed an increase in two orders of magnitude in the conductivity around the threading dislocation, and scanning capacitance microscopy measurements, considering the phase of the signal, revealed local variations in minority carrier concentration and identified a charge distribution associated with the triangular defect (see Figure 3).

After drawing on reports in the scientific press, Fiorenza accounted for this observation by reasoning that the threading dislocation has an increased hole concentration and a bandgap that is 0.8-1 eV lower than the surrounding SiC. Simulations supported this view and enabled the team to discover that threading dislocations act as quantum wells, increasing hole concentration by 13 orders of magnitude. Operating in reverse bias, these holes are driven through the SiO_2 layer of the MOSFET, accelerating its degradation.

Speeding screening

Those needing to assess the reliability of the SiC MOSFET will welcome the introduction of a relatively straightforward, speedy technique developed by Infineon Technologies and announced at IPRS. This approach focuses on the weakness of the gate oxide, which is the key failure mechanism.

Speaking on behalf of Infineon, Judith Berens detailed this powerful technique after laying the groundwork – the distinction between the intrinsic and extrinsic branch of gate oxide reliability. “The intrinsic branch only plays a role towards the end of the life, and is similar for SiC and silicon MOSFETs,” explained Berens. “Extrinisics, however, might lead to early failures in the field, and for this reason need to be avoided.”

Failures due to extrinsics are a significant cause for concern, given that their prevalence is higher in SiC MOSFETs than in silicon devices. One promising option for uncovering them is to measure device performance at different voltages. “By gate-voltage screening, you mainly sort out devices with extrinsics, and reduce the field failure probability,” said Berens.

The extent of failure reduction realised by screening depends on the ratio of the screening voltage to the operating voltage – Berens refers to this as the failure reduction factor. Note that this factor exceeds a thousand when the screening voltage is three times the value of the recommended operating voltage (see Figure 4).

Of course, there are limitations on how high a voltage can be used for screening. This method of evaluation must avoid permanent damage to ‘good’ chips, accomplished by avoiding degradation caused by the tunnelling of carriers and impact ionisation. Both phenomena can lead to a negative threshold voltage shift.

Berens championed a new measurement procedure that avoids using too high a stress voltage. Instead, a series of voltages are applied, each 1 V higher than the previous. After each pulse, which should be as short as possible to reduce the chances of degradation, the threshold voltage is recorded.

To illustrate the value of this approach, Berens presented an example of what one could expect when carrying out this measurement. To begin with, as the stress voltage incrementally increased, so did the threshold voltage, due to a positive bias temperature instability. But beyond a certain value the threshold voltage plummeted, reaching a point of no return and causing the device to be irreversibly damaged (see Figure 5).

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Berens explained that determining the likelihood of field-rate failure requires the value for the stress voltage for the onset of irreversible degradation, along with the intended operating voltage for the MOSFET. The ratio of these two determines the failure reduction factor and gives an insight into device reliability.

Demonstrating how this works in practice, Berens compared data for a range of commercial MOSFETs, including trench and DMOS designs. Pulsed stress tests uncovered a 20 V range in voltages required to reach the onset of irreversible damage, with values depending on the thickness of the oxide. This is understandable, as thicker oxides are subjected to a weaker electric field strength that reduces the chances of impact ionisation.

For the next step in this analysis, Berens and co-workers accounted for the operating voltage of the various devices. With this factor included, the differences between manufacturers narrowed significantly; and the new, normalised ratio allowed the failure rate reduction factor to be determined by reading this value from the graph shown in Figure 4.

Note that due to the high degree of non-linearity of this graph, small variations in the normalised ratio produce a difference in the failure rate reduction factor by two orders of magnitude (see Figure 6). This implies that the most reliable devices have roughly one hundred times fewer failures in the field than the most unreliable devices.

Berens says that one of the advantages of this method is the speed with which it determines the likelihood of failure – it takes less than a minute per test run. The technique is also straightforward, with no special test equipment required. "And last but not least, we didn't need any special knowledge, only publicly available data sheet values."

The problem of pits

SemiQ, a producer of SiC power devices based in California, has also been investigating the screening of SiC MOSFETs using the gate voltage. Speaking on behalf of the company, Yongju Zheng detailed measurements on 1200 V, 80 mΩ SiC planar depletion MOSFETs with a 50 nm-thick gate oxide. This investigation considered a variety of voltages and voltage ramp rates, with measurements taken at room temperature and 130 °C.

Zheng and co-workers have pursued a two-step process. In their study, they began by ramping from 40 V to 50 V, which screened out about 4 percent of devices from the sample size of 289. "These are defined as weak gate oxides, as the median voltage of our devices is about 53-54 volts," said Zheng. The second step involved ramping from 40 V and 70 V. The upper end ensured breakdown and enabled a failure distribution to be obtained. Failure is defined when gate leakage hits 9 mA.

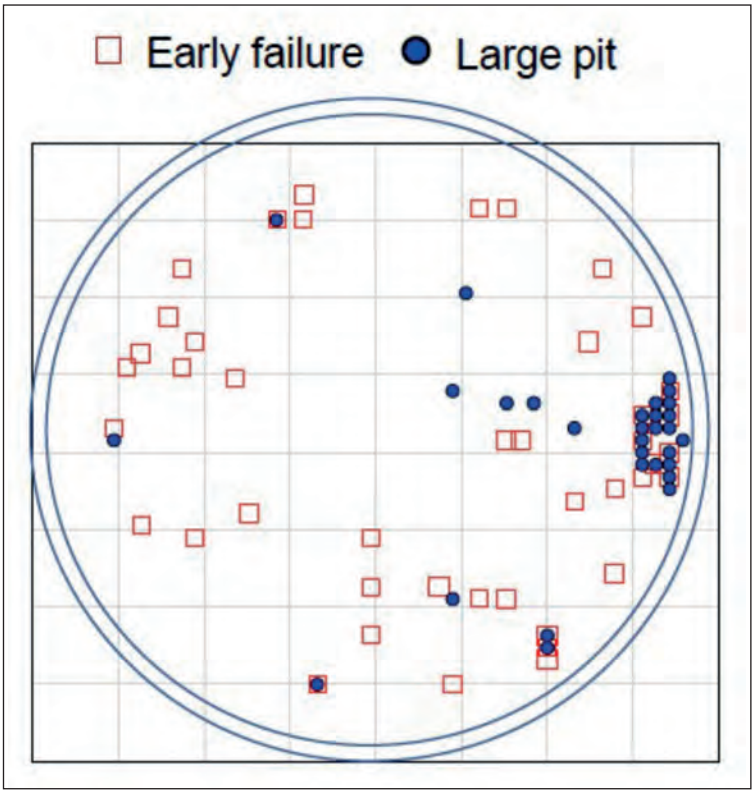

Figure 7. A study at SemiQ has shown that when pit defects are larger than 100 mm², 80 percent of them cause early failure of a SiC MOSFET.

The engineers found that the failure voltage is higher when the ramp rate is faster. "This could be due to longer stress time, leading to more charging at the interface of silicon carbide and silicon dioxide," speculated Zheng. Note that for the two temperatures used in this study, no notable difference in failure voltage is found.

Zheng and her colleagues have considered whether large epi pits could be behind the early failure of some SiC MOSFETs. "It turned out that these early failures show very strong correlation to large pit defects, that are defined as pit defects larger than 100 micron-squared." This correlation is so strong that 80 percent of these large pits caused early failure (see Figure 7). According to Zheng, the presence of these pits may alter the epitaxial growth conditions, and lead to local oxide thinning that would result in electric field crowding – both factors could account for early failures.

One of the downsides of using a high screening voltage is that it causes a negative shift in the threshold voltage, which could impair reliability, especially when operating the MOSFET at high temperatures under reverse bias. Measurements by the team from SemiQ have shown that ramping from 40 V to 50 V produces a negative shift in the threshold voltage of 0.85 V, taking this device close to normally-on behaviour.

"Based on the study in this work, the screening voltage is suggested to be below 38 volts for a 50 nanometre gate oxide in production," said Zheng,

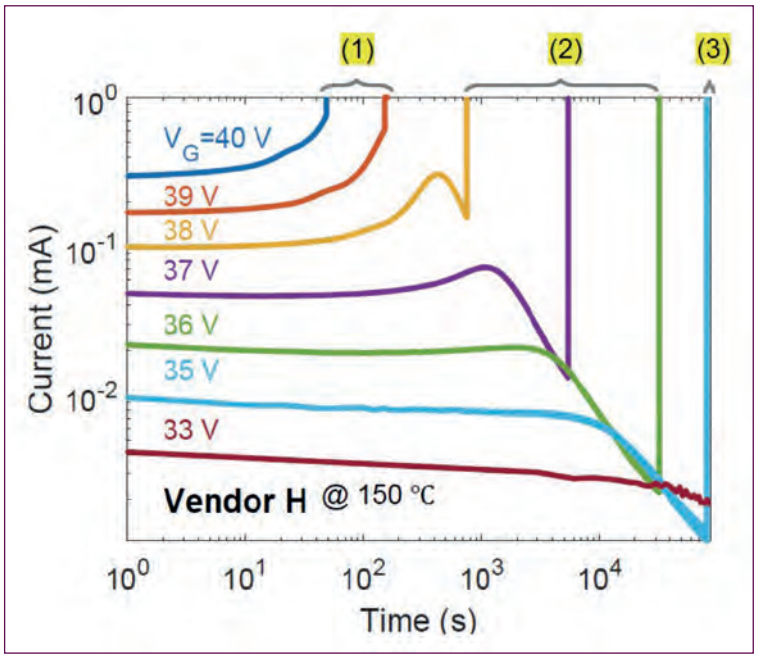

Figure 8. Researchers have identified three different regimes for SiC MOSFETs subjected to gate-stress tests. When the gate voltage is 39 V or more, the gate current accelerates; for voltages of 38 V to 35 V, initially the current varies, before a rapid hike; and for a voltages of 33 V, current falls steadily.

adding that such a value should be low enough to detect the extrinisic failure rate, while not significantly lowering the threshold voltage of the MOSFET, or shortening the lifetime of its gate oxide.

Looking into leakage

A thorough study into the leakage current of 1.2 kV commercial SiC power MOSFETs has been conducted by researchers at Ohio State University, working in partnership with engineers at Alpha and Omega Semiconductor. Highlighting the findings at IPRS, Shengnan Zhu from Ohio State University explained that one of the challenges with this type of study is that the device makers do not disclose the thickness of their gate oxides. So Zhu and her co-workers have had to estimate this from the value for the breakdown voltage, obtained by measuring the gate leakage current while ramping the gate voltage. This approach indicated that the oxide in 1.2 kV power MOSFETs varies from 39 nm to 46 nm, assuming a dielectric breakdown field in the range 10 MV/cm to 11.5 MV/cm.

The team also recorded variations in the gate current leakage over a 24 hour period for a range of gate voltages, while maintaining the device at an elevated temperature of 150 °C. Plotting the data revealed three regimes (see Figure 8). For gate voltages of 39 V or more, the gate current accelerates; for voltages of 38 V to 35 V, there are variations in the current, before a rapid hike; and for a voltages of 33 V or less, the current falls steadily.

Zhu offered a detailed explanation for this range of behaviour. She argued that for gate voltages of 39 V or more, corresponding to an oxide field of at least 9.8 MV/cm, hole trapping dominates. This takes place due to Fowler-Nordheim tunnelling of electrons into the device – these carriers trigger impact ionisation and generate electron-hole pairs, with holes driven to the semiconductor-oxide interface, where they are joined by additional holes resulting from anode hole injection. A high hole density at this boundary reduces in the width of the barrier for tunnelling of electrons and leads to an increased injection of this carrier, which generates yet more holes through impact ionisation. With positive feedback at play, there is an acceleration of the gate leakage current.

For voltages of 38 V to 35 V, the oxide field is slightly lower, at 9.5-9.0 MV/cm. In this case, there is also hole trapping that enhances the electric field near the interface. However, this time subsequent electron trapping in the oxide leads to a reduction in the strength of the local field, a widening of the tunnel barrier, and ultimately a reduction in leakage current. Dominance of hole trapping, followed by electron trapping, results in a rise and then a fall in the gate leakage current. When investigating this in more detail, the team found that their conjecture is supported by variations in threshold voltage.

When the gate voltage is 35 V or below, the field across the gate oxide is restricted to no more than 8.8 MV/cm. For devices operating in this regime, electron trapping takes place, relaxing the electric field. This increases the barrier width, and in turn reduces Fowler-Nordheim tunnelling.While this takes place, the threshold voltage increases. The insights provide by Zhu and the other speakers at IPRS showcase the progress being made to understand the reliability of the SiC power MOSFET, and differences in the devices of many manufacturers.

As insights feed in to device development and production, robustness of this transistor should increase, driving its deployment in ever more applications.

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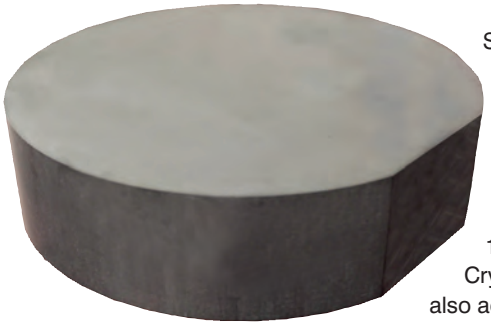

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