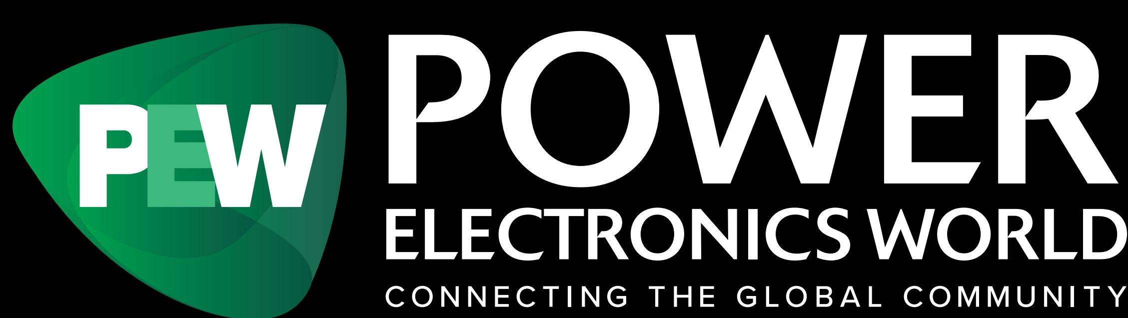

Soft-switching becomes reality for EV drivetrains

ISSUE II 2023

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VIEWPOINT

By Christine Evans-Pughe, Acting Editor

Driving change: soft switching and SiC fabs

THE INTERNAL COMBUSTION ENGINE has ruled our roads for over 100 years. EVs, by contrast, have some catching up to do. Limited range is one major concern. Charging time is another. But one former Audi EV drivetrain designer believes that the answer is soft-switching. Meanwhile, EVs are winning on semiconductor content. A battery EV contains around $950 worth of chips (double that of a combustion engine vehicle) and power semiconductors are driving much of this. By 2030, over 95 percent of passenger BEVs will use SiC MOSFETs in their powertrains, according to Exawatt, a UK market analysis firm.

In this issue, Bruce Renouard, CEO of Pre-Switch explains his company's approach to soft switching in EV drive trains using a forced-resonant topology controlled by Artificial Intelligence: it's a fascinating read. We also delve into the world of SiC fabs with analysis of Microchip's $880M investment at its Colorado Springs campus. We look too at the bigger picture of how SiC chip makers are building resilience into their supply chains and forging long-term alliances with car companies to avoid future oversupply or shortages.

Our GaN coverage this issue examines Infineon's recent acquisition of GaN Systems, and shows how GaN HEMTs can be used for high power density USB-C designs. Anthony Marini and Max Zafran from EPC Space, write about how GaN HEMTs are the ideal device for making circuits that drive motors in space.
In the lab, scientists from the National Yang Ming Chiao Tung University in China, enhance ferroelectric gate HEMTs by adding lanthanum doping and a ZrO_2 seed layer. And a team from Novel Crystal Technology in Japan is making headway with the design and performance of normally-off Ga_2O_3 transistors, using multiple sub-micron fins to ensure far greater consistency in threshold voltage.

Finally, Richard Stevenson, editor of CS Magazine, brings us two conference reports. One from the International Physics Reliability Symposium, where speakers detailed the best approaches for evaluating the long-term capability of SiC power devices. Reporting from this year's packed CS International Conference, Richard explains why Ga_2O_3 is being hailed as the most promising material ever for power devices. He describes SiC and GaN as 'middleweights', whereas Ga_2O_3 is a 'heavyweight' for its capability to handle incredibly high voltages and provide switching at even higher efficiencies.

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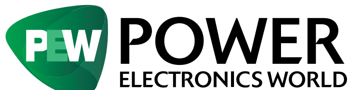

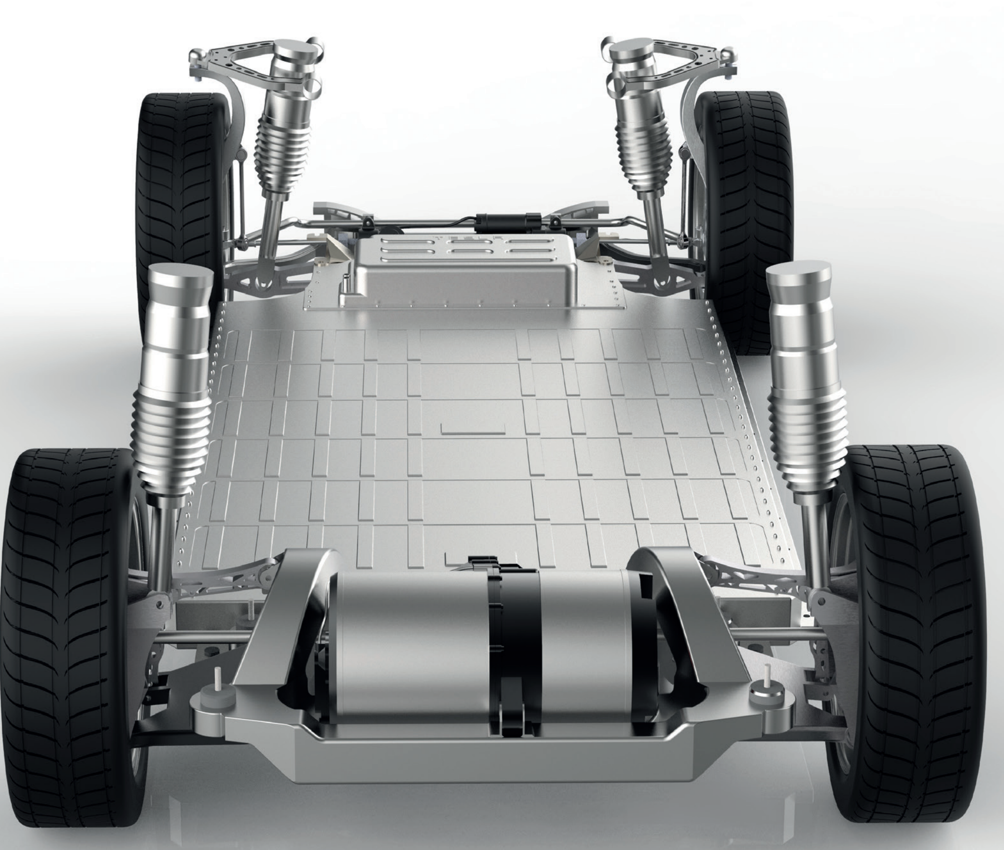

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Acting Editor
Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Contributing Technical Editor
Richard Stevenson
richard.stevenson@angelbc.com
+44 (0)1923 690215

Sales & Marketing Manager
Shehzad Munshi
shehzad.munshi@angelbc.com
+44 (0)1923 690215

Senior Event and Media Executive for Power Electronics International
James Cheriton
james.cheriton@angelbc.com
+44 (0)2476 718970

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Publisher
Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

CEO Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

CTO Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

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6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com W: angelbc.com

Nexperia introduces interactive datasheets for MOSFETs

Datasheet parameters dynamically respond to user inputs

NEXPERIA has announced the release of next-generation interactive datasheets to accompany its power MOSFETs. By manipulating interactive sliders within the datasheets, users can manually adjust the voltage, current, temperature and other conditions for their circuit application and watch how the operating point of a device dynamically responds to these changes.

These interactive datasheets offer a type of graphical user interface to a circuit simulator, using Nexperia's electrothermal models to calculate the operating point of a device. In addition, they allow engineers to visualise immediately the interaction between parameters such as gate voltage, drain current, RDS(on) and temperature. Their collective contribution to the device behaviour is then displayed dynamically in tables or graphs.

As a result, Nexperia says its interactive datasheets can significantly increase productivity by eliminating the time needed for an engineer to perform manual calculations or set up and debug a circuit simulation. Chris Boyce, senior director of Nexperia's Power MOSFET business adds: "Whether you are a design engineer looking to see how a device will perform at elevated temperature, or a component engineer trying to compare devices under different test conditions, our new interactive datasheets are designed to make your life easier."

The technology powering these datasheets is the same as that used in Nexperia's precision electrothermal MOSFET models, which demonstrate how the behaviour of discrete MOSFETs changes with hot and cold temperatures.

The new interactive datasheets are offered in addition to the traditional static datasheets and operate in any standard web browser without the requirement of additional software for device simulation.

PI introduces IGBT/SiC module gate drivers

SCALE-2 technology improves current sharing by 20 percent

POWER INTEGRATIONS has introduced the SCALE-iFlex LT NTC family of IGBT/SiC module gate drivers.

The new drivers target the popular dual, 100 mm x 140 mm style of IGBT modules, such as the Mitsubishi LV100 and the Infineon XHP 2, as well as SiC variants up to 2300 V blocking voltage.

The SCALE-iFlex LT NTC drivers provide Negative Temperature Coefficient (NTC) data – an isolated temperature measurement of the power module – which enables accurate thermal management of converter systems. According to PI, this is important for systems with multiple modules in parallel, ensuring proper current sharing and dramatically enhancing overall system reliability.

Thorsten Schmidt, product marketing manager at Power Integrations commented: “Designers of renewable energy and rail systems using SCALE-iFlex drivers already benefit from increased system performance; the SCALE-iFlex approach handles paralleling so expertly that one module in five can be eliminated without loss of performance or current de-rating. Adding an isolated NTC output reduces hardware complexity – particularly cables and connectors – and contributes to system observability and overall performance.”

Based on Power Integrations’ SCALE-2 technology, SCALE-iFlex LT gate drivers are said to improve current sharing accuracy and therefore increase the current carrying capability of multiple-paralleled modules by 20 percent, allowing users to increase the semiconductor utilisation of their converter stacks. This is possible because the localised control of each 2SMLT0220D MAG (Module Adapted Gate driver) unit ensures precise control and switching, enabling excellent current sharing. Advanced Active Clamping (AAC) is employed to deliver accurate overvoltage protection.

To further increase space saving, up to four MAG-driven power modules can be parallel-connected from a single 2SILT1200T Isolated Master Control (IMC) unit, which can also be mounted on a power module due to its compact outline. The gate drivers are qualified to IEC 61000-4-x (EMI), IEC-60068-2-x (environmental) and IEC-60068-2-x (mechanical) specifications, and undergo complete type testing – low voltage, high voltage, thermal cycling – to help shorten designer development

time. Power Integrations has also announced a new, single-channel, plug-and-play gate driver for 190 mm x 140 mm IHM and IHV IGBT modules up to 3300V.

The 1SP0635V2A0D combines Power Integrations’ SCALE-2 switching performance and protection features with a configurable isolated serial output interface, which augments driver programmability and provides comprehensive telemetry reporting for an accurate lifetime estimation.

Multiple sensing circuits including thermal and device and bus condition information are incorporated, simplifying system design and enhancing observability, control and reliability. Application areas are rail traction inverters, power grid and medium-voltage drives.

BAE Systems and Eaton collaborate on EV trucks

BAE SYSTEMS is collaborating with Eaton, a power management company, to develop electric vehicle (EV) technology.. The companies will initially offer a solution for medium-duty commercial trucks, with a Class-7 pickup and delivery demonstration vehicle in development.

As part of the collaboration, BAE Systems will incorporate its electric motor and SiC/GaN power electronics suite with Eaton’s MD 4-speed EV transmission.

“Our complementary strengths and industry knowledge in providing clean transportation solutions will address a critical need for new, clean technology options for the global truck market,” said Steve Trichka, vice president and general manager of Power & Propulsion Solutions at BAE Systems. BAE Systems has more than 16,000 propulsion systems operating in transit buses, boats, and military and industrial vehicles across the globe. Its electric

propulsion technology is developed and serviced at its facilities in Endicott, New York and Rochester, UK.

A new era for silicon power?

iDEAL Semiconductor launches its patented SuperQ technology

iDEAL Semiconductor, a fabless US company focused on delivering better power efficiency, has announced the availability of its patented silicon-based SuperQ technology. The launch comes on the heels of a Series C funding round bringing total investment to over $75 million.

Silicon power semiconductors have seen limited innovation in the past two decades with performance increases focused on new materials like SiC and GaN. But iDEAL says it has created a novel architecture that sets a new frontier of performance that debunks the idea that we've reached end of the road for silicon.

The SuperQ structure is pictured above. The company says that unlike superjunctions that restrict the N-conduction region to 50 percent of the structure, the SuperQ asymmetrical approach has almost no limit on the conduction area. At the same time, it provides the benefits of higher doping and a thinner epitaxial region. The result is a record-setting low resistance per unit area (RSP). For example, SuperQ-based 200V MOSFETs are said to deliver six times lower resistance than existing silicon and 1.6 times lower resistance than GaN. Motor drive inverters designed with SuperQ technology can save up to 50 percent of power losses, according to iDEAL .

"iDEAL Semiconductor is one of the only companies focused on both process and architecture for building power devices.

Our improvements in silicon rival the improvements offered by other materials, but with silicon's manufacturability, availability, and reliability," said Mark Granahan, CEO and co-founder of iDEAL Semiconductor. "Through collaborations in the US with Applied Materials and Polar Semiconductor, we have unlocked previously unimaginable performance gains. Material agnostic, we address the increasing demand for power devices."

The company is initially targeting voltages up to 850V, to provide higher performance power diodes, MOSFETs, IGBTs and integrated circuits. The technology is manufactured using CMOS equipment.

Denso and USJC ship first automotive IGBTs

DENSO CORPORATION and United Semiconductor Japan Company (USJC), a subsidiary of the foundry UMC, have announced the start of mass production of IGBTs at USJC's 300mm fab.

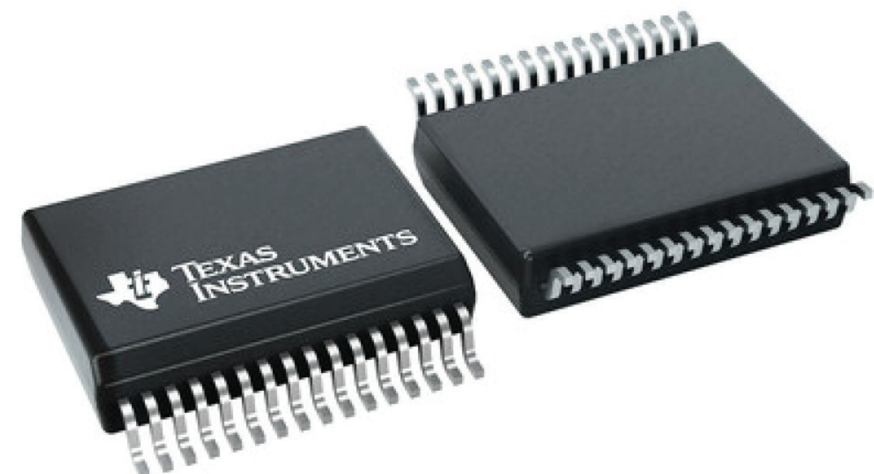
This comes one year after the companies announced a strategic partnership for IGBTs used in electric vehicles. The jointly invested line at USJC supports the production of a new generation of IGBT developed by Denso, which is said to offer 20 percent reduction in power losses compared with earlier generation devices. Production is expected to reach 10,000 wafers per month by 2025. "USJC is proud to be the first semiconductor foundry in Japan to manufacture IGBT on 300mm wafers, offering customers greater production efficiency than the standard fabrication on 200mm wafers.

➤ From left, Denso president Koji Arima, UMC co-president Jason Wang

Thanks to our dedicated teams and support from Denso, we were able to complete trial production and reliability testing without delay and honour the mass production date as agreed with the customer," said Michiari Kawano, president of USJC.

SiC gate driver maximises EV range

TI says new driver chip can improve vehicle range as much as 1,000 miles per year



TEXAS INSTRUMENTS (TI) has released a highly integrated isolated gate driver that enables engineers to design more efficient traction inverters and maximise electric vehicle (EV) driving range.

TI says that carmakers can build safer, more efficient and more reliable SiC and IGBT-based traction inverters by designing with the UCC5880-Q1, featuring real-time variable gate-drive strength, Serial Peripheral Interface (SPI), advanced SiC monitoring and protection, and diagnostics for functional safety.

"Designers of high-voltage applications like traction inverters face a unique set of challenges to optimise system efficiency and reliability in a small space," said Wenjia Liu, product line manager for high-power drivers at TI.

"Not only does this new isolated gate driver help enable engineers to maximise driving range, but it also integrates safety features to reduce external components and design complexity. And it can be easily paired with other high-voltage power-conversion products such as our UCC14141-Q1 isolated bias supply module to improve power density and help engineers reach the highest levels of traction inverter performance."

The need for higher reliability and power performance for EVs is growing, as efficiency gains have a direct impact on operating range improvement per charge. But achieving any increase in efficiency is difficult for designers, given that the majority of traction inverters already operate at 90 percent efficiency or higher. By varying the gate-drive strength in real time, in steps between 20 A and 5 A, designers can improve system efficiency with the UCC5880-Q1 gate driver as much as 2 percent by minimising SiC switching power losses, resulting in up to 7 more miles of EV driving range per battery charge. For an EV user who charges their vehicle three times per week, that could mean more than 1,000 additional miles per year.

CGD launches second ICeGaN series

650V GaN HEMTs are designed to eliminate typical e-mode GaN weaknesses

CAMBRIDGE GaN DEVICES (CGD) has launched the second series of its ICeGaN 650 V GaN HEMT family.

Called H2, the new HEMTs employ CGD's smart gate interface that is designed to eliminate typical e-mode GaN weaknesses, delivering improved overvoltage robustness, higher noise-immune threshold, dV/dt suppression and ESD protection.

H2 devices feature a NL3 (No Load and Light Load) circuit, integrated on-chip alongside the GaN switch, to lower power losses. A clamping structure with integrated Miller Clamp – also on-chip - eliminates the need for negative gate voltages, achieving zero-volt turn-off, and improving dynamic RDS(ON) performance. These e-mode (normally off) single chip GaN HEMTs also include a monolithically-integrated interface and protection circuit for gate reliability and design simplicity. Finally, a current sense function reduces power dissipation and allows direct connection to ground for optimised cooling and EMI.

Like CGD's previous generation devices, the new 650 V H2 ICeGaN transistors are driven similarly to silicon MOSFETs, using commercially available industry gate drivers.

"CGD has solved all the challenges that normally slow the adoption of a new technology. Furthermore, we are now ready to satisfy the mass market with our H2 Series ICeGaN transistors which are available through an established supply chain," said Giorgia longobardi, CEO and co-founder of CGD.

She added: "Independent research by Virginia Tech has proven ICeGaN to be industry's most rugged GaN devices, and in terms of ease-of-use, they can be driven like a standard silicon MOSFET, so the learning curve which can slow market acceptance is eliminated. The efficiency of GaN is well known, and ICeGaN is impressive across the full load range."

Onsemi and Kempower sign deal on EV chargers

UNDER A NEW agreement, Onsemi will provide the Finnish firm Kempower with EliteSiC MOSFETs and diodes for scalable electric vehicle (EV) chargers.

The ongoing collaboration between the two companies focuses on Kempower's EV charging solutions and includes a variety of power semiconductor technologies, including Onsemi's EliteSiC. These devices will be used in the Active AC-DC front-end and in the primary and secondary DC-DC converters.

Kempower will incorporate the latest EliteSiC D3 diode and M3S MOSFETs into its cloud-connected EV charging solutions. These chargers allow for dynamic load balancing, ensuring maximum power distribution.

"Onsemi EliteSiC power devices improve the efficiency and lower the size and weight of our EV charging solutions," said Petri Korhonen, chief engineer, Kempower. "In addition, Onsemi's vertically integrated supply chain and broad portfolio of intelligent power solutions give us the stability needed to continue delivering world-class EV charging solutions to the market."

"Our strength in manufacturing and resilient SiC supply chain assure Kempower that we will deliver high-quality products in the agreed-upon volumes today and in the future," said Asif Jakwani, senior vice president and general manager, Advanced Power Division, Onsemi. "Incorporating highly reliable power devices leads to the dependable and durable EVCs that Kempower and its customers expect every time."

Microchip SiC E-Fuse protects EVs

New demonstrator is available in six variants for 400–800V battery systems

TO PROVIDE BEV and HEV designers with a faster and more reliable high-voltage circuit protection solution, Microchip Technology has developed a SiC-based E-Fuse demonstrator board, available in six variants for 400–800V battery systems and with a current rating up to 30A.

The E-Fuse demonstrator can detect and interrupt fault currents in microseconds, 100–500 times faster than traditional mechanical approaches because of its high-voltage solid-state design, according to the company. The fast response time substantially reduces peak short-circuit currents from tens of kilo-amps to hundreds of amps, which can prevent a fault event from resulting in a hard failure.

"The E-Fuse demonstrator provides BEV/HEV OEM designers with a SiC-based technology solution to jumpstart their development process with a faster, more reliable method for protecting power electronics," said Clayton Pillion, vice president of Microchip's SiC business unit. "The E-Fuse solid-state design also alleviates long-term reliability concerns about electromechanical devices because there is no degradation from mechanical shock, arcing or contact bounce."

With the E-Fuse demonstrator's resettable feature, designers can package an E-Fuse in the vehicle without the burden of design-for-serviceability constraints. This is said to reduce design complexities and enable flexible vehicle packaging to improve BEV/HEV power system distribution.

A built in Local Interconnect Network (LIN) communication interface enables the configuration of the over-current trip characteristics without the need to modify hardware components, and it also reports diagnostic status.

The E-Fuse demonstrator uses Microchip's SiC MOSFET technology and PIC microcontrollers' Core Independent Peripherals (CIPs) with a LIN-based interface. The companion components are automotive-qualified and yield a lower part count and higher reliability over a discrete design. The E-Fuse board is supported by MPLAB X Integrated Development Environment (IDE).

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EPC and ADI introduce reference design

High power density for regulated DC-DCs achieved using EPC GaN FETs and Analog Devices' controller

EPC has announced the EPC9158, a dual output synchronous buck converter reference design board operating at 500 kHz switching frequency. The board combines Analog Devices' LTC7890 synchronous GaN buck controller with GaN FETs from EPC to convert an input voltage of 48 V - 54 V to a regulated 12 V output and delivers up to 25 A per phase or 50 A total continuous current. The solution is said to achieve 96.5 percent efficient at 48 V to 12 V and 50 A continuous current.

The high-power density makes this solution suitable for computing, industrial, consumer, and telecom power systems requiring small size and high efficiency.

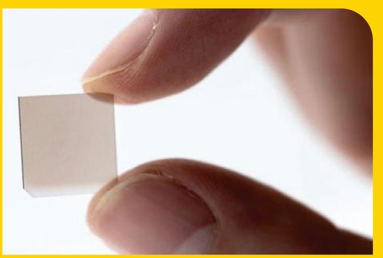
The EPC9158 reference design uses the EPC2218 100 V enhancement-mode GaN FET and the LTC7890 two-phase analogue buck controller with integrated GaN drivers. The LTC7890 100 V low Iq, dual, 2-phase synchronous step-down controller is optimised to drive EPC GaN FETs and integrates a half bridge driver and smart bootstrap diode.

It offers optimised near-zero deadtime or programmable deadtime and programmable switching frequency up to 3 MHz. The quiescent current of 5 uA (VIN = 48 V, VOUT = 5 V, CH1 only) enables very low standby power consumption and excellent light load efficiency. The EPC2218 is a 100 V GaN FET with 3.2 mOhm max RDS(on), 10.5 nC QG, 1.5 nC QGD, 46 nC QOSS and zero QRR in a super small 3.5 mm x 1.95 mm footprint and can deliver up to 60 A continuous current and 231 A peak current. The excellent dynamic parameters allow very small switching losses at 500 kHz switching frequency.

The efficiency of the EPC9158 is greater than 96.5 percent for 12 V output and 48 V input. In addition to light load operating mode and adjustable dead time, the board offers UVLO, Over-current protection, and power good output. Alex Lidow, CEO of EPC commented, "GaN FETs are required to achieve the maxim power density for DC-DC converters. We are delighted to work with Analog Devices to combine the benefits of their advanced controllers with the performance of GaN to provide customers with the highest power density and low component count solution that increases the efficiency, increases power density, and reduces system cost".

Orbray and Mirise to collaborate on diamond power chips

JAPANESE jewel-processing company Orbray and Mirise Technologies, an automative research firm established in 2020 by Denso and Toyota, have begun collaborating on vertical diamond power devices. Over the three-year period of this project, Orbray and Mirise Technologies will use their respective technologies, resources, and expertise in diamond substrates and power devices to develop the technologies needed to deploy vertical diamond power devices in a wide range of future electric vehicles.



Orbray will be responsible for developing a p-type conductive diamond substrate, while Mirise Technologies will take charge of developing a high-voltage operating device structure to demonstrate the feasibility of a vertical diamond power device. Compared with current mainstream semiconductor materials such as silicon, SiC and GaN, diamond is sometimes called the 'ultimate semiconductor material' because it has higher voltage operating capability and superior thermal conductivity (heat dissipation). The development and mass production of next-generation automotive semiconductors using diamond is expected to improve the fuel efficiency and power consumption of electric vehicles, and reduce battery costs.

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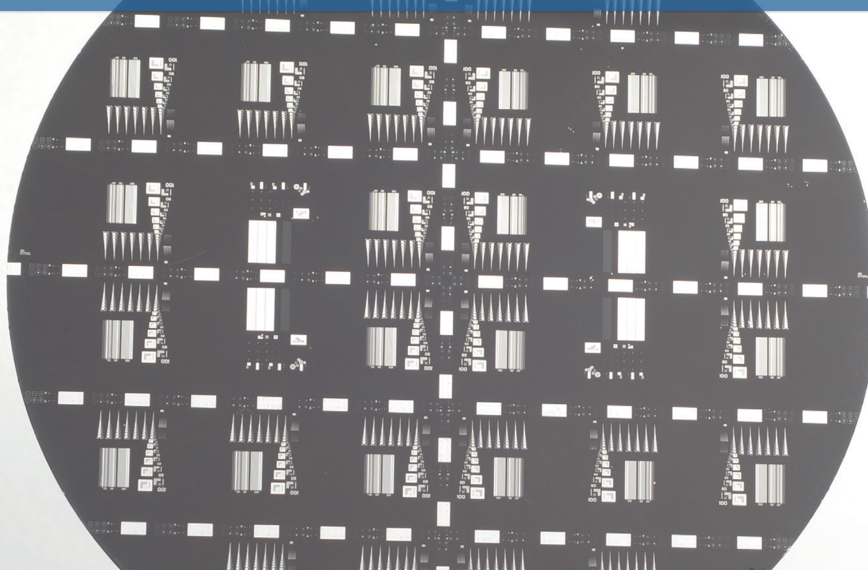

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Getting strategic with SiC

As we gradually transition from fossil fuels, the world is waking up to the critical importance of power semiconductors

EFFICIENCY, electrification and CO2-reduction are watchwords for our age, but they are only part of the story behind the recent flurry of SiC chip fab investments. From Wolfspeed's plans to build the world's largest SiC plant in Germany, to Mitsubishi's intended construction of an 8-inch SiC wafer plant in Japan, these projects are as much about simmering global tensions and safeguarding chip supplies as they are about climate change.

We see this most strikingly in the US government's $52.7B package of subsides for domestic chipmaking as part of its Chips Act, closely followed by the EU's $47B plan. The EU aims to be totally self-sufficient in semiconductors; this is onshoring on a big scale. Moreover, it wants to build market share from 10 to 20 percent by 2030.

Japan is dedicating $2.8B to chip subsidies, which includes covering up to one third of capital investments in power semiconductors.

The UK released its long-awaited National Semiconductor Strategy in May, focusing on semiconductor design, compound semiconductors, and R&D. The UK government will invest a modest £200 million over the next two years, and up to £1 billion in the next decade to support growth of the home-grown compound semiconductor sector. So far, no fab funding.

How will this pan-out? According to Yole Group's estimates last year, SiC power devices will represent 30 percent of the overall power device in the next four years, with a market potential of over $6 billion by 2027, up from around $1 billion in 2021.

Will the market be there, and is there a risk of undersupply or oversupply?

Interestingly, as part of the European Chips Act the European Commission has launched a Semiconductor Alert System, a new pilot to monitor the semiconductor supply chain, allowing stakeholders to raise awareness on any critical disruption along the semiconductor value chain. The idea is that the Commission can quickly react to any potential crisis situation.

The semiconductor industry is well known for its cycles of fab building followed by oversupply. Boom usually follows bust. But SiC chip makers are bullish. Onsemi and ST Microelectronics have both announced aims to secure $1bn in SiC business in 2023. Infineon wants 30 percent share of the global SiC market by the end of the decade.

Cars are the main focus of the SiC gold rush. Data from Infineon shows that vehicle semiconductor content is expected to rise from ~$490 per vehicle for an internal combustion engine vehicle to ~$950 for a battery electric vehicle (BEV). Power semiconductors will drive much of this content increase, especially from the high-powered inverters used to drive the electric motor.

Exawatt, a UK market analysis firm, forecasts that by 2030 over 95 percent of passenger BEVs will use SiC MOSFETs in their powertrains. It also expects BEVs will account for more than 50 percent of annual passenger vehicle sales by 2030. Exawatt also predicts that SIC-based inverters will surpass silicon-based inverters by 2024. By 2030 95 percent of battery electric vehicles will use SiC based semiconductors in their powertrains.

According to Angelique van der Burg, chief procurement officer at Infineon, her company is doubling down on its SiC investments. "In this context, we are implementing a multi-supplier and multi-country sourcing strategy to increase resilience to the benefit of our broad customer base," she said, about recently signed deals with two Chinese SiC suppliers ¬– TanKeBlue and SICC – under which they will supply Infineon with 150 mm SiC wafers and boules and support Infineon's transition to 200mm wafers. Infineon already has an agreement with the US firm Coherent (formerly II-VI) to supply 150mm substrates, and to collaborate on 200mm, signed last year.

STMicro is building a pilot line for wafers and a processing frontend in Catania, Sicily, alongside its existing SiC fab. It aims to increase the front-end capacity ten-fold and will have 40 percent of substrates internally sourced by Q4 2024, starting with 150mm and moving to 200mm.

US firm Onsemi aims to expands it SiC boule production capacity by five times year-over-year as part of its plan to gain full control of its entire SiC manufacturing supply chain, starting with the sourcing of SiC powder and graphite raw material to the delivery of fully packaged SiC devices. In-house sourcing of wafers is key to its strategy.

To boost SiC research in the US, Onsemi has also just signed an MOU with Penn State University to build an $8 million collaboration with the establishment of a SiC Crystal Center at Penn State's Materials Research Institute (MRI). Onsemi will fund the centre with $800k per year over the next ten years.

"Penn State is uniquely positioned to rapidly establish a SiC crystal growth research program," said Pavel Freundlich, chief technology officer, Power Solutions Group, Onsemi. "The university offers a wide breadth of capability based on its current materials research, wafer processing capabilities in its nanofab facility, and a comprehensive, world-class suite of metrology instrumentation."

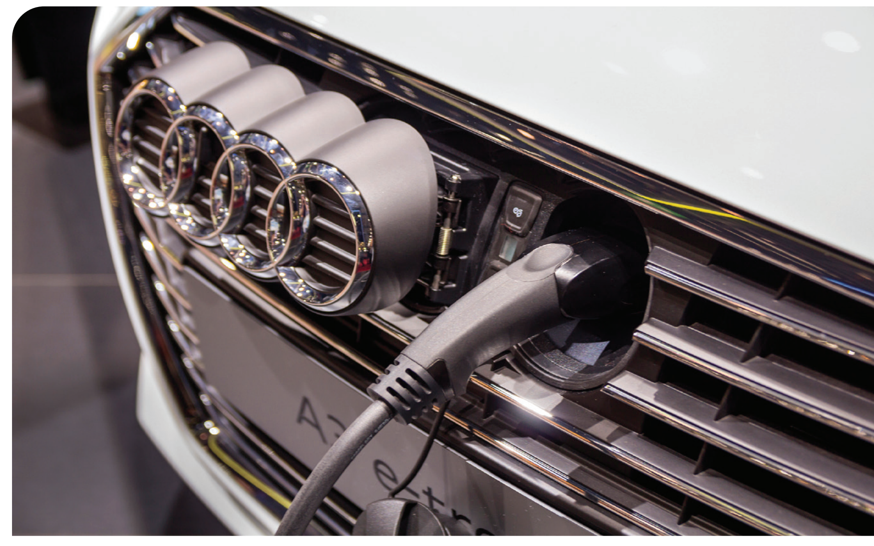
Cars, cars, cars

Alliances with automotive companies are central to the SiC story. ST has recently announced that it has 25 ongoing electric vehicle projects with eight customers. Infineon, which provides SiC semiconductors to more than 3,600 automotive and industrial customers, has just signed an agreement with Hon Hai Technology Group (Foxconn), the Taiwanese electronics manufacturing services provider, to work together on electric vehicles and establish a system application centre in Taiwan.

Wolfspeed has a strategic partnership with the huge German automotive systems company ZF Friedrichshafen AG, which supplies systems for passenger cars, commercial vehicles and industrial technology. ZF and Wolfspeed also plan to establish a joint European R&D centre for SiC power electronics in Germany in the Nuremberg area.

Onsemi will be supplying Volkswagen with SiC modules and semiconductors for an EV traction inverter solution. The company also has a long-term supply agreement with BMW, signed in March 2023, for electric drivetrains. Added to these are a collaboration with the Finnish firm EV charging company Kempower around SiC MOSFETs and diodes, and a tie-up with the Chinese electric mobility firm Zeekr, a developer of battery technologies, battery management systems, and electric motor technologies.

Rohm, meanwhile, has a joint development agreement with Mazda Motor Corporation and Imasen Electric Industrial for inverters and SiC power modules to be used in the electric drive units of electric vehicles. These are just a handful of announced SiC alliances. But "strategic'" is more than just a throw-away term. It means long-term reliable supplies for the car companies, and guaranteed customers for the output of the soon-to-be burgeoning SiC fabs.



Investment in SiC production will introduce the capability to process 200 mm wafers.

SiC production to soar at Microchip

An $880 million investment at Microchip's Colorado Springs campus will create a 200 mm line for producing SiC diodes, MOSFETs and modules

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

RIGHT NOW, barely a month or so goes by without another major maker of power electronics unveiling plans to ramp SiC capacity. Arguably the chipmaker that's been attracting the most attention in this regard is Wolfspeed, which is devoting $6.5 billion to expand production, with efforts including the construction of new fabs in the US and Switzerland and a massive expansion of its crystal growth facility in North Carolina. Others moving in a similar direction include: onsemi, which is investing $300 million to expanding capacity at its fab in Roznov, Czech Republic; and Microchip, which this February revealed that it would be spending $880 million on its Colorado Springs facility, to increase SiC and silicon capacity.
Offering an incredibly diverse product portfolio that includes SiC diodes, MOSFETs and modules, Microchip has a pedigree in SiC that dates back 20 years. Its technology comes via an acquisition of Microsemi, which got its hands on this class wide bandgap power electronics when it bought Advanced Power Technology, a company that launched SiC products in 2003.

Microchip combines internal and external capacity to ensure supply chain redundancy. In the US, Microchip's dual-fab strategy uses an internal and external fab for SiC production, with SiC epiwafers processed into a variety of devices.

At Microchip's Colorado Springs campus, scaling of production and efficiency is continuous, according to Clayton Pillion, Vice President of the company's SiC Business Unit. When asked whether SiC

production is at full capacity, Pillion responded by saying that this is a moving target. “It’s a hard concept for people to believe, because it’s either full or it’s not in most people’s minds. From our perspective, we continue to scale.”

Helping to increase this capability is an increase in external capacity, which, despite market constraints, is delivering small expansions. Microchip is not disclosing its split between SiC and silicon in its $880 million investment that will be spent on facility, equipment and hiring. However, even if this chipmaker were more forthcoming, it would still be unable to provide a definitive figure. “Some of the equipment and some of the labour that goes with that is fungible between the two technologies,” says Pillion.

Expansion of the Colorado Springs facility is supported by state and local incentives, totalling around $47 million, as well as the CHIPS and Science Act. Microchip is a valuable asset to national security – although it’s not the only maker of SiC chips in US, it has a strong track record in supplying to this country’s aerospace and defence markets. Investment at Colorado Springs will create a 200 mm line for SiC. However, Pillion says that the company will only move to this larger format when it’s prudent to do so, making manufacture with 150 mm wafers likely for foreseeable future.

To aid expansion of the facility, Microchip is planning to add 400 staff to the 850 currently employed at the Colorado Springs campus. While expertise in SiC is ideal for new hires, it’s not going to be a pre-requisite, according to Pillion. “That skill pool [for silicon carbide] is limited in size. You’re always working to balance silicon carbide experience with those that have very good engineering basics, who can grow to learn silicon carbide.”

With so many chipmakers competing for sales of SiC products, those that are to thrive need to stands out from their peers. Helping Microchip to have an edge over its rivals is the level of robustness of its products, underscored by compelling reliability data.

➤ The Colorado Springs facility has existed for many years. In 1989 Honeywell sold this to Atmel, which was acquired by today’s owners, Microchip, in 2016.

This allows designers to reduce the level of chip redundancy, and ultimately trim costs.

Another asset of Microchip is the level of support it offers its customers. “We never say ‘Here’s your product. Go away’. That’s not in our DNA,” says Pillion. Instead, Microchip supports its customers, drawing on its expertise to help develop designs at the system level. To illustrate this point, Pillion remarked: “We had a visitor to our corporate headquarters two days ago. They were asking us to sit there and work with them, to help them optimise the performance and the balance of the design – total system cost versus performance – and work through some experiments.”

One of Microchip’s goals is to expand its sales beyond the aerospace and defence markets, where it has enjoyed success for many years.

“In January I took over the group, and we are now focused on driving into a broader industrial and commercial space,” reveals Pillion, who says that the company is starting to target some automotive applications. “We prefer a more diversified market, much like we do with our core business at Microchip. Our embedded business is highly, highly diversified, and that’s the approach we’re taking for silicon carbide.”

BASED around a hot industry topic for your company, this 60-minute recorded, moderated zoom roundtable would be a platform for debate and discussion.

MODERATED by an editor, this online event would include 3 speakers, with questions prepared and shared in advance.

THIS ONLINE EVENT would be publicised for 4 weeks pre and 4 weeks post through all our mediums and become a valuable educational asset for your company

Contact: jackie.cannon@angelbc.com

Following the acquisition, Infineon will combine GaN products produced on internal lines with those of fabless GaN Systems.
Image Credit: Infineon Technologies AG

GaN's glorious marriage

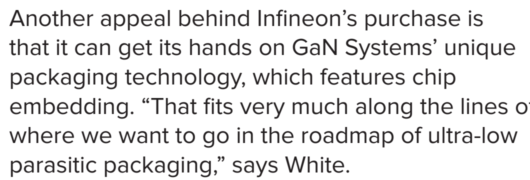
Infineon will enhance its prowess in power electronics with the acquisition of GaN Systems

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

ONE OF THE MOST significant milestones for wide bandgap power electronics arrived when silicon powerhouses decided to invest in one flavour of this technology. At that time some went for SiC, while others threw their weight behind GaN; now many of the biggest names have both. In fact, so great is the promise of these successors to silicon that one of the leading players, Infineon, is now planning to strengthen its GaN offering by combining its in-house capabilities with an $830 million acquisition of Canadian fabless firm GaN Systems.

This acquisition - following negotiations that are said to have lasted for months rather than years, and slated to close by the end of 2023 – will equip Infineon with two complementary GaN technologies, according to Adam White, Infineon's Division President, Power and Sensor Systems.

"The device concepts of the technologies are slightly different," argues White, who adds that this difference can help address different application requirements across the application space. For example, soft switching versus hard switching or the level of robustness.



Another appeal behind Infineon's purchase is that it can get its hands on GaN Systems' unique packaging technology, which features chip embedding. "That fits very much along the lines of where we want to go in the roadmap of ultra-low parasitic packaging," says White.

One area where Infineon already excels is in its capability to couple its GaN technology to silicon ICs, such as drivers and controllers. It's a synergistic approach that empowers the company to target customers with products that are designed from a whole system perspective.

Once the acquisition goes through Infineon will instantly double the number of products in its GaN portfolio. In turn, the number of design opportunities will increase by at least this factor. "That would then accelerate our applications understanding," enthuses White, "and from there, of course, ultimately bring value to the customer from a system perspective."

A key difference between Infineon and GaN Systems is that the former has chip production

lines, while the latter is fabless. "That's another benefit of the acquisition upon closing," says White, pointing out that the purchase will lead to more fruitful conversations with foundry partners. "This is definitely a pillar of our growth strategy. We recognise that gallium nitride will need capacity."

On the unveiling of its plan to buy GaN Systems, Infineon's CEO, Jochen Hanebeck, remarked that this move would create an entity with unmatched R&D resources.

Supporting this claim, White says that once GaN Systems is on board, it will give Infineon a 450-strong GaN team. "That doesn't include all the areas of go to market, all the areas of operations. This is just an application knowledge domain, product domain knowledge, and R&D product domain knowledge."

The purchase of GaN Systems is described as a synergistic growth acquisition. No-one within the entity that's due to be acquired should fear for their job, as Infineon's intent is to maintain and motivate these staff, and keep them within the company.

The acquisition will strength Infineon's already formidable patent portfolio. The German chipmaker can already boast of more than 300 patent families, and once GaN Systems is on board, this figure will top 350.

One may wonder what's behind the timing of the acquisition. According to White, one motivation for making the move at this time is that Infineon believes that GaN is now at a "very healthy tipping point", in terms of both the customer's interest in this wide bandgap material and their willingness to pursue sponsored projects.

There's also a level of maturity within the customer base. No longer are the virtues of a GaN device defined in what it can deliver when providing a drop-in replacement for a silicon equivalent. Customers are now thinking about what GaN offers when deployed in the right system with the right topology. "You can then unleash the potential of gallium nitride," says White.

While $830 million may appear a lot to spend on a fabless outfit with a couple of hundred employees, there's definitely the potential for a good return on investment for the German powerhouse

He is now starting to see the adoption of GaN in a number of applications. These devices are now being deployed in: charger and adapter markets; server markets for high power; residential solar markets; and the on-board charger, as well as the DC-to-DC converter in cars.

"This is really the reason why now [we've acquired GaN Systems], and hence why we went after this acquisition to complement our approach that we're doing standalone," adds White.

The immediate impact is not the most overriding consideration. What's more important to the German outfit is the mid-term to long-term perspective.

"The addressable market will really justify the value that we are paying for this asset," reasons White, who backs this up by quoting figures from Yole Intelligence. Forecasts from the French analyst include a compound annual growth rate for GaN for power applications of an eye-watering 56 percent from 2022 to 2027, which will propel this market to more than $6 billion by the end of this timeframe.

So, while $830 million may appear a lot to spend on a fabless outfit with a couple of hundred employees, there's definitely the potential for a good return on investment for the German powerhouse.

Using GaN HEMTs for high performance in USB-C designs

GaN HEMTs operate at the high switching frequencies need for high power density USB-C adapter and charger designs. **Luo Junyang, Technical Marketing at INFINEON TECHNOLOGIES,** discusses alternative approaches to implementing common topologies found in USB-C power delivery (PD) designs

MODERN USB-PD adapters and chargers (including those with extended power range) are required to deliver exceptional performance in the smallest possible form factors. There are a range of topologies commonly used: active clamp flyback, hybrid flyback, as well as PFC and hybrid for extended power range. But what are the pros and cons of implementing them using discrete devices versus fully integrated GaN HEMTs? And what might be the benefits from using integrated switching controllers, where appropriate to a topology?

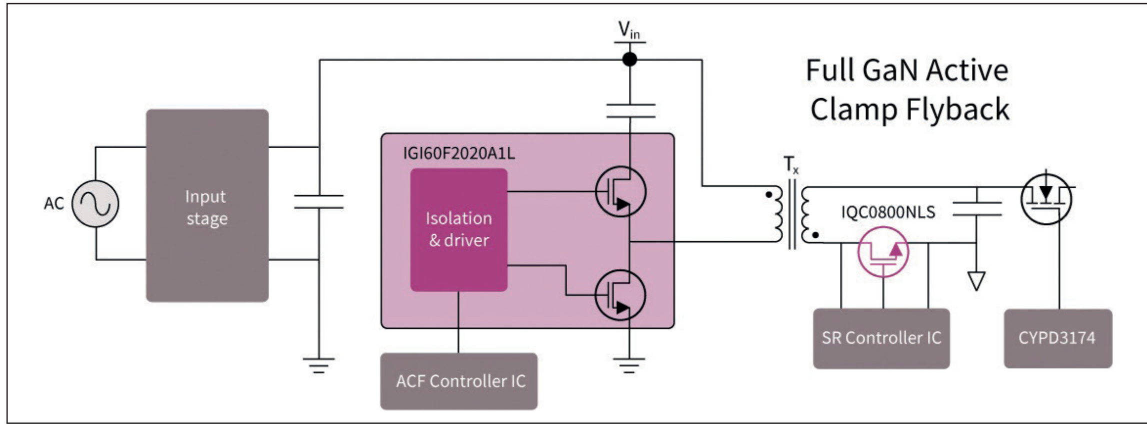
Active clamp flyback - Discrete

We'll start with one of the most popular topologies: the active clamp flyback (ACF) converter which enables zero voltage switching (ZVS) for power switches. The topology (Figure 1) is suitable for higher frequency operation than a quasi-resonant flyback due to the ZVS operation and complete recovery of the energy in transformer leakage inductance dissipated in the flyback resistor-capacitor-diode (RCD) clamp. Clamping the primary-switch voltage through the clamp capacitor (combined with ZVS) means the ACF topology provides good electromagnetic interference (EMI) performance.

Two ACF control schemes exist: complementary (CP) and non-complementary (NCP). In CP mode, the main flyback switch and clamp switch turn on and off in a complementary fashion in each switching cycle, so the transformer current waveform has an approximately sinusoidal shape. The main flyback switch and clamp switch operate under ZVS switching, with the switching frequency increasing as the load decreases. This can impact light-load and standby efficiency as well as affect EMI. Additionally, the total resonant current in the resonant tank causes conduction losses in the transformer to increase. NCP ACF can be used to overcome both of these issues. In this mode, the active clamp switch only turns on sufficient magnetic energy to maintain ZVS in the main switch. This way, the circulating clamp capacitor currents are mitigated.

Active clamp flyback - Integrated

Figure 2 shows an alternative implementation of the active clamp flyback (ACF) using a CoolGaN integrated power stage (IPS). Here the clamp switch provides a path to recover the energy stored in the transformer's leakage inductance (Llk) when the main switch turns off, and the clamp switch turns



➤ Figure 1. Discrete implementation of the Active Flyback Converter Topology

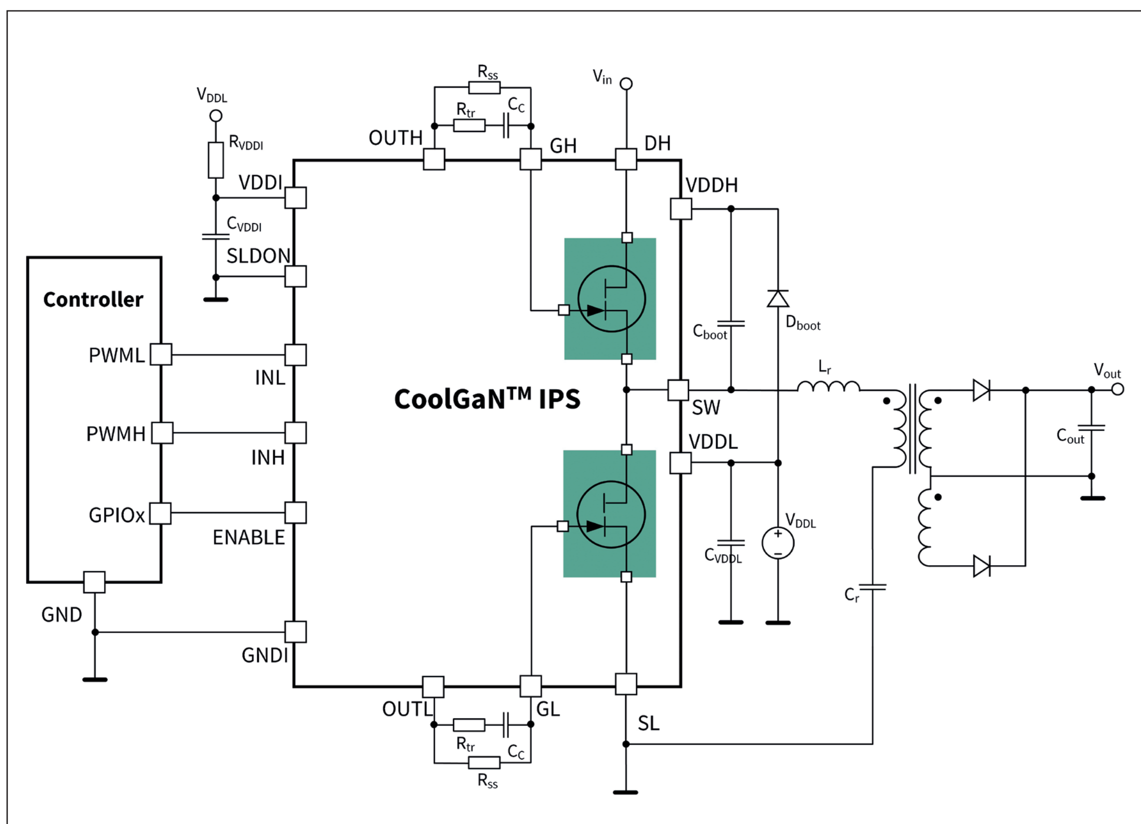


Figure 2. Active Flyback Converter Topology implemented using IPS

on. As a result, Cclmp and Llk resonate together through the clamp switch and the transformer, resulting in energy transfer to the load. This energy recovery increases the system efficiency compared to the passive clamp flyback, where the energy is stored in Llk damps in a traditional RCD clamp circuit.

Hybrid flyback – Discrete

The hybrid flyback (HFB) converter (Figure 3) is another resonant topology that not only employs ZVS but zero current switching (ZCS) too. The primary-side converter has resonant-type current waveforms, which means high-frequency, high efficiency is possible due to ZVS operation with lower RMS currents. In addition, the capacity of the resonant capacitor assists with energy storage, which means the transformer size can be smaller than for other flyback-type topologies.

Thanks to the half-bridge structure with a self-voltage clamp to Vbus on the primary side, the voltage stress on the switching device is better than for the ACF topology. HFB has an additional switch on the primary side compared to QR flyback, which requires special care for the light-load efficiency due to the circulating currents of the resonant type operation. Careful design is needed for universal input specifications, and the control complexity required for HFB is much higher than that needed for the QR flyback topology. However, Infineon's XDP digital power XDPS2201 controller uses a dedicated control algorithm, greatly simplifying this task.

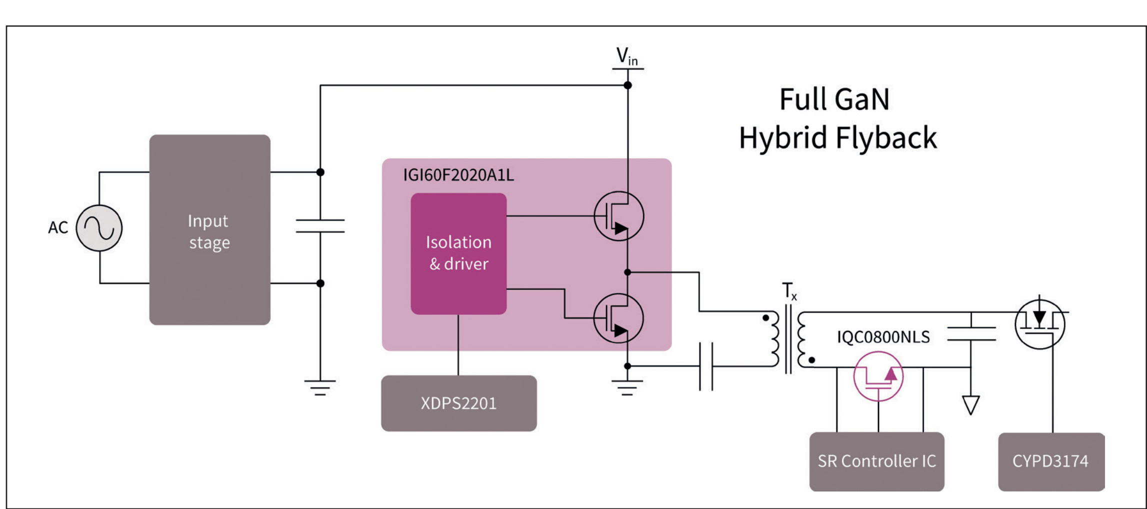


Figure 3. Discrete implementation of the Hybrid Flyback Topology with XDPS2201 controller

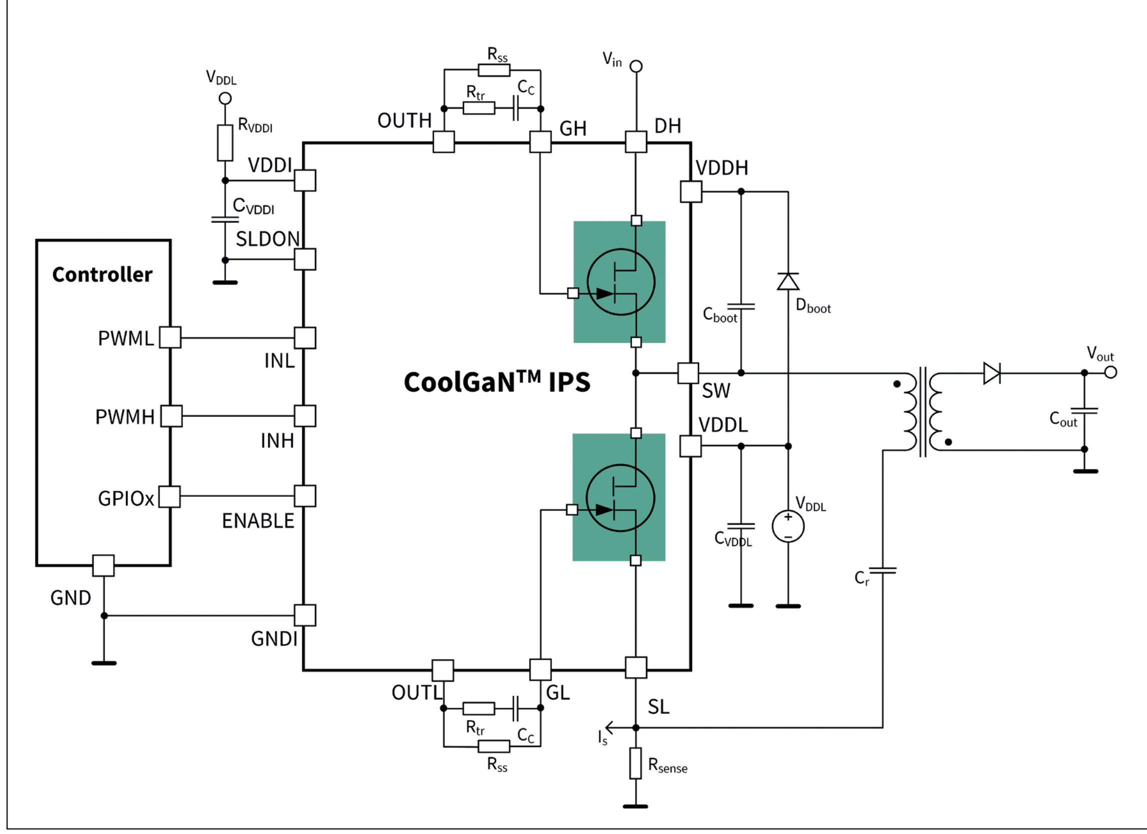


Figure 4. Implementing a Hybrid Flyback Topology using an IPS

Hybrid flyback – Integrated

Figure 4 shows a hybrid flyback converter (HFB) topology with the CoolGaN IPS. The converter consists of a high-side and a low-side switch, the transformer, the resonant tank (Llk and Cr), the output stage rectifier and capacitors. An advanced control scheme with a non-complimentary switching pattern provides a solution that supports a wide range of AC input and DC output voltages, which is necessary for universal USB-C PD operation.
When the high-side switch is turned on, the hybrid flyback converter stores energy in the primary-side inductor. The energy stored in the primary side inductor is transferred to the output when the low-side switch is turned on. With proper timing control during the switch transition of both switches, HFB runs under ZVS for both devices, ensuring high system efficiency without requiring additional components. Both devices benefit from ZVS and higher efficiency (from ZCS operation on the secondary side), making hybrid flyback a cost-competitive solution for ultra-high power density converters, like USB-PD fast chargers.

PFC and hybrid flyback

Finally, we look at the requirements for USB-PD with extended power range (EPR) standard. This provides for even higher power levels of up to 240 W, paving the way for a universal AC-DC adapters suitable for many different purposes, including charging a wide variety of end devices, from smartphones to gaming laptops, up to power tools, and even e-bikes. However, the requirements for electromagnetic compatibility, power factor correction, standby power, and average efficiency present a new challenge for the currently used converter topologies. At the same time, size and power density have become increasingly essential requirements in this application.
The wider output voltage range (from 5 V to 48 V) presents new challenges for existing converter topologies, so combining an AC-DC power factor correction (PFC) boost converter with a DC-DC hybrid flyback (HFB) stage provided the most suitable combination for USB-PD chargers and adapters with a wide input and output voltage range (Figure 5).

This architecture uses an innovative controller to provide a combination of high power density combined and efficiency (to meet international regulatory standards like EU CoC Version 5 Tier 2 and DoE Level VI). Furthermore, this architecture supports effective control of the broad output voltage in the most recent USB-PD standard. Compared to conventional versions of the flyback topology, a much smaller transformer can be used. The XPD XDPS2201 integrates an AC-DC power factor correction (PFC) controller with a DC-DC hybrid flyback controller (HFB), also known as an asymmetrical half-bridge (AHB), in one single package and enables compliance with regulatory requirements through the harmonized operation of these two stages. Integrating all gate drivers, a 600 V high voltage start-up cell for the initial IC voltage supply, and the certified active X-capacitor discharge reduce the bill of material (BOM) for external components.

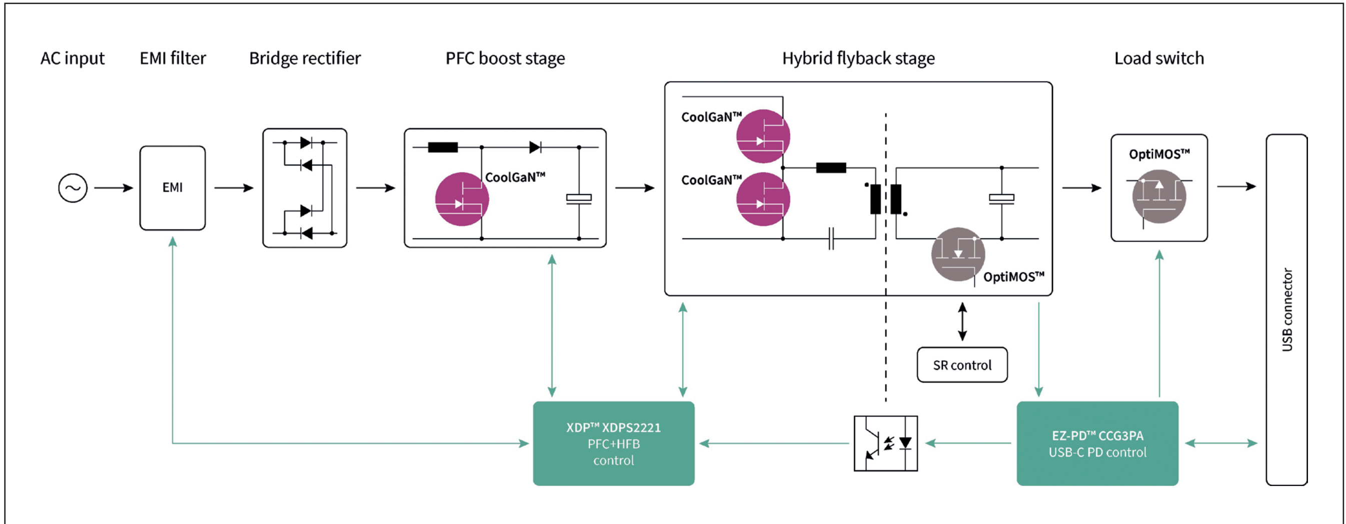
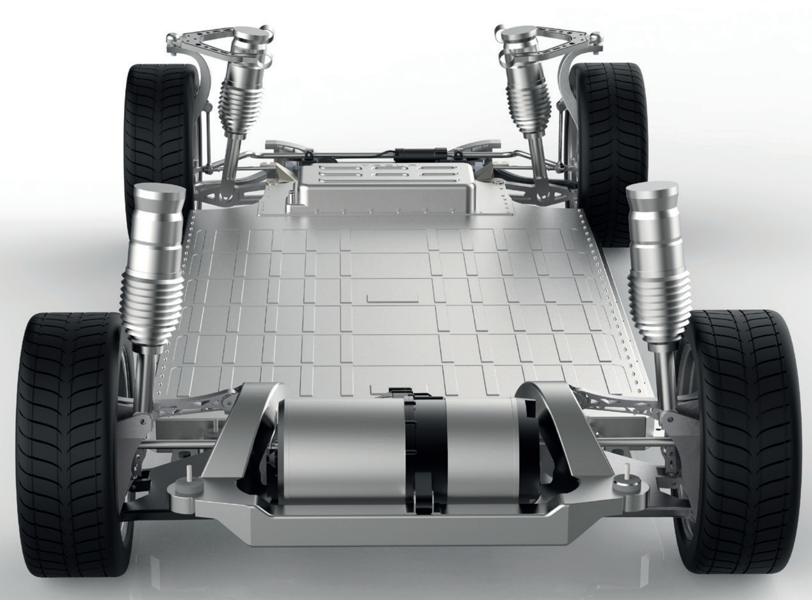


Figure 5. Power architecture for USB-PD extended power range

Based on a novel zero-voltage switching (ZVS) HFB topology (based on GaN devices), this controller enables unsurpassed efficiency across a wide range of line and load conditions.

These features, combined with inherent topology advantages (such as zero voltage switching and resonant energy transfer for transformer size reduction), mean system designs using XDP XDPS2221 can achieve exceptionally high power densities. This new combo controller IC also features a synchronous PFC and HFB burst mode operation to provide the lowest possible no-load input standby power performance. In addition, the quasi-resonant multimode PFC stage is enhanced with automatic PFC enable/disable functionality and adaptive PFC bus voltage control to maximize average and light load efficiency. Optionally, the integrated PFC function can also be disabled to support any external PFC Controller. The hybrid flyback stage uses peak current control operation for robust regulation and fast dynamic load response. For ZVS operation under all conditions, the hybrid flyback features ZVS pulse insertion, including body diode cross-conduction prevention in discontinuous conduction mode.



Soft-switching becomes a reality for EV drivetrains

Soft-switching at high frequencies used to be impractical. Now, a new approach, using a forced-resonant topology controlled by AI, is delivering inverters that are 98.5 percent efficient at 5 percent load, and 99.57 percent peak. **Bruce Renouard, CEO of** PRE-SWITCH INC, explains the benefits

TRANSPORTATION is in a period of great change as electrification asserts itself as the preferred technology for a greener, sustainable future. But the automotive internal combustion engine has enjoyed over 100 years of heavy investment, development and refinement.

EVs, by contrast, are still emerging and – in many ways – have some catching up to do. Limited range is one of the major concerns for people when they look into EVs. Charging time is another. Both these factors demand that EVs must be as efficient as possible. Which is one of the main reasons why the EV industry is so interested in soft-switching, which promises very high efficiency across the full load range.

Various soft-switching architectures have been discussed for many years, but until recently, soft-switching at high frequencies has been impractical. Now, a new approach, using a forced-resonant topology controlled by AI, is delivering inverters that are 98.5 percent efficient at 5 percent load, and 99.57 percent peak, resulting in increased EV range of up to 12 percent.

These performance figures are part of the reason why one former Audi EV drivetrain designers believes that “in future, all EV inverters will need to use soft-switching”.

What is ‘soft-switching’?

Let’s start by defining ‘soft-switching’. There are basic approaches to switching transistors on and off. These are termed: ‘hard- and soft-switching’. Hard-switching turns the target transistors on and off directly.

Although this is a very simple design, it leads to switching losses when transistors turn on and off in the presence of a voltage as shown in Figure 1.

These losses are higher in high-voltage transistors employed in EVs, and there are also other issues. Hard-switching generally requires a lower switching frequency, EMI is increased and the size and weight of components such as DC link capacitors can increase to the point where they occupy up to 60 percent of the inverter volume. These characteristics result in reduced efficiency and increased system cost.

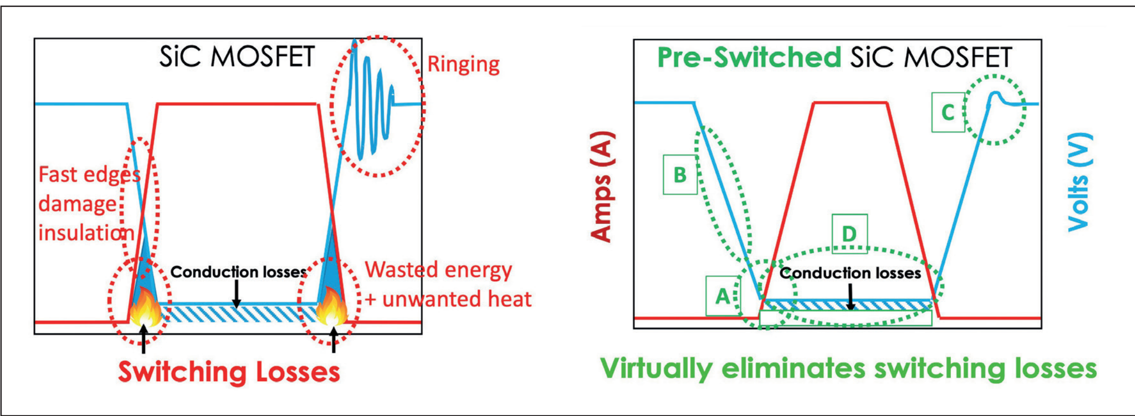


Figure 1

In contrast, soft-switching is achieved when the transistors are turned on and off when there is no voltage present (zero voltage switching) as in Figure 1b. This is achieved using a self- or forced-resonant circuit to ensure effective transistor commutation timing. The result is that switching losses are virtually eliminated, EMI is reduced and efficiency is significantly increased. However, soft-switching has never been perfected for isolated AC/DC and DC/AC power converters, so consequently this topology has been limited to non-isolated power converters with low input voltage and output load range.

The challenge has been how to ensure that the transistors always switch on and off at the precise point when voltage is zero, given many varying factors, such as input voltage, output load, device tolerances, and temperature changes. This is the essence of the Pre-Switch breakthrough: artificial intelligence (AI) is used to monitor all these variables and adjust the timing on a cycle-by-cycle basis to achieve true soft-switching.

Using AI to resolving timing calculations

The Pre-Switch topology for soft-switching is a variation of the Auxiliary Resonant Commutated Pole (ARCP) soft-switching converter topology. At its most basic, ARCP is a conventional inverter topology with an auxiliary circuit that helps soft-switch the main inverter (Figure 2).

The auxiliary switches are activated before the main power output switches, and generate a current in the auxiliary inductor that is used to induce the condition required to soft-switch the main inverter switches. The auxiliary switches are turned on and off at zero current while the main switches are switched at zero voltage.

The sophisticated, embedded AI, developed by Pre-Switch, dynamically solves all complex timing calculations demanded by changing operating conditions, and resolves the previous limitations of ARCP soft-switching. The control algorithm can drive any type of power switch and is ideally suited for all power switching technologies including silicon-based IGBTs and MOSFETs, gallium nitride (GaN) and silicon carbide (SiC). The Pre-Switch topology enables drivetrain systems based on with industry standard IGBTs and MOSFETs to equal to surpass state-of-the-art wide bandgap-based power components (SiC & GaN).

An animated sequence of 20 1µs screen captures (Figure 3) provides a simplified explanation of the Pre-Switch AI, showing the algorithm actively learning from initial start-up with unknown conditions, then subsequently optimizing and adjusting the timing necessary to ensure that a PWM input generates a current ramp to simulate the first part of a sine wave output. The GIF demonstrates how the AI is works with Pre-Switch's Cleanwave

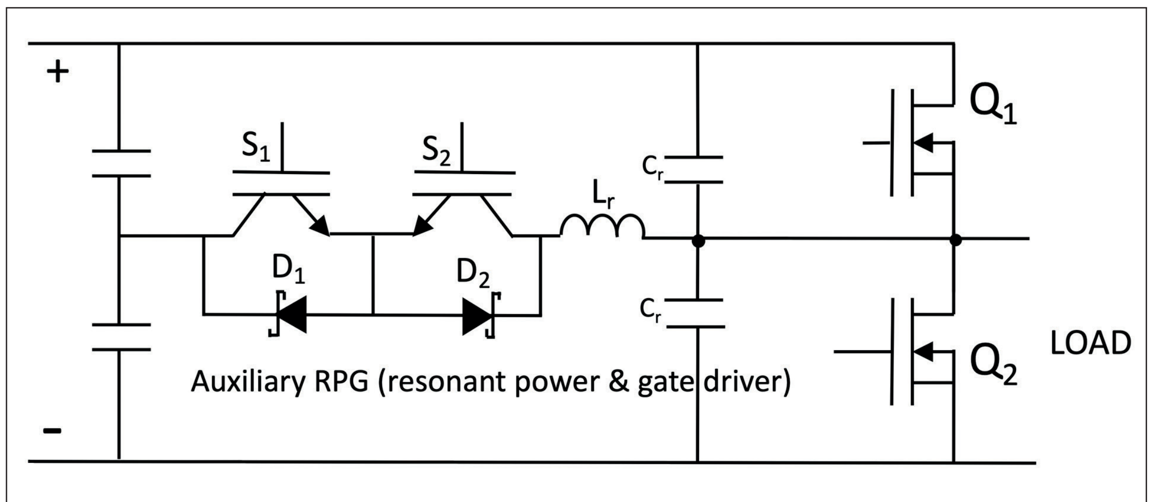


Figure 2

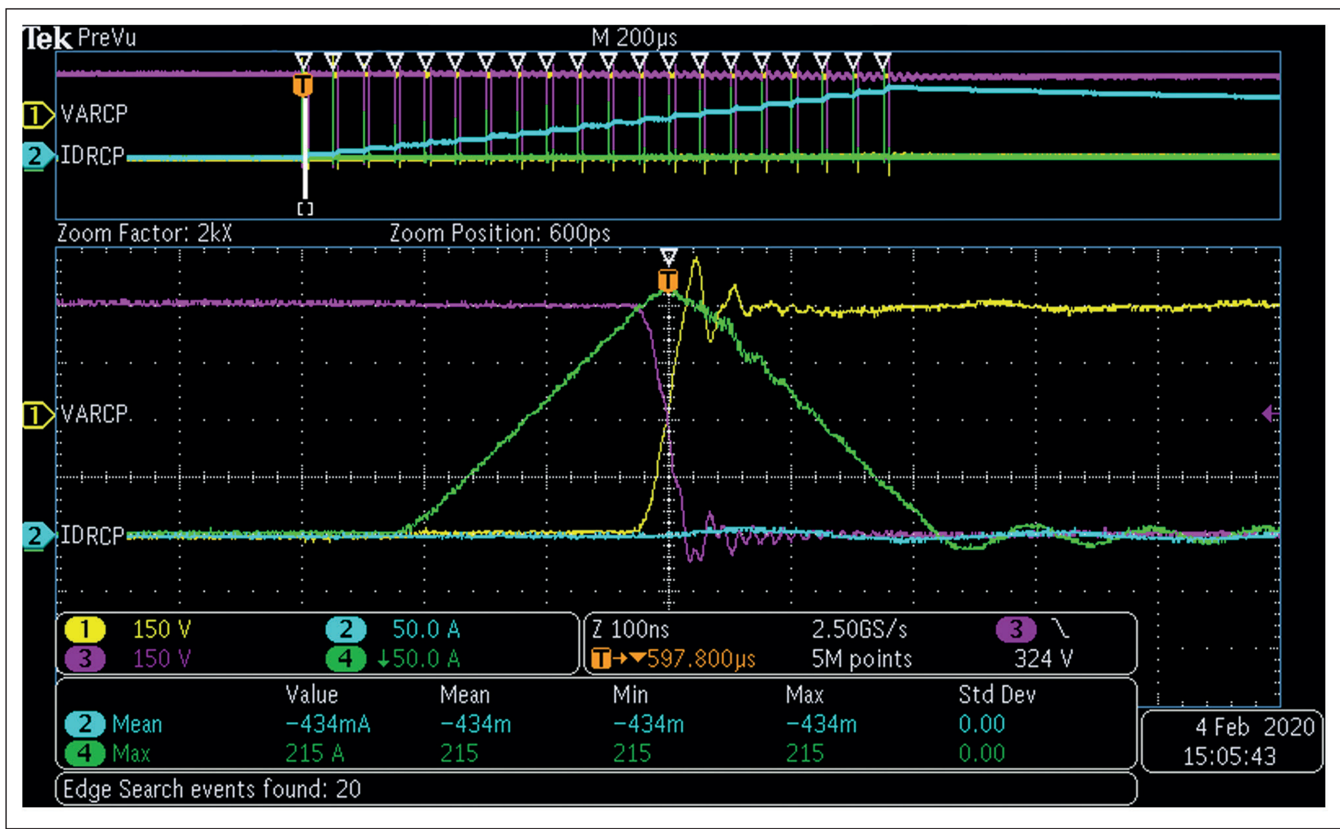


Figure 3

200kW inverter reference to bi-directionally convert 800VDC to three-phase AC at power levels of up to 200kVA with a switching frequency of 100kHz at 99 percent efficiency levels.

Double pulse test data obtained from the Cleanwave inverter demonstrates that the Pre-Switch soft-switching platform – comprising the Pre-Drive3 controller board powered by the Pre-Flex FPGA, and RPG gate driver board – reduces total system switching losses by 90 percent or more. Upon commencement of the initial switching cycle (0), the Pre-Switch AI controller assesses multiple inputs to determine what mode the system is in, and then makes a safe but non-optimal estimate of the resonant period needed for soft switching. During the next switching cycle (1), all AI inputs and resulting outputs from switching cycle 0 are precisely re-measured and analysed. A second conservative resonant timing period, similar to switching cycle 0, is issued.

In follow on switching cycle (2), the AI algorithm is now quantitatively-confident and able to predict the optimized resonant timing to ensure full soft-switching – thus minimizing losses in all aspects of the system. Then in switching cycle 3, the AI compares system inputs and results from previous switching cycles and adjusts the resonant timing to fully optimise soft-switching with the increasing load current. These inputs and outputs are stored with the previous switching cycle inputs and resulting resonant timings to improve accuracy and system optimization. In subsequent cycles, soft switching accuracy continues to be optimized, stored to and compared to desired results necessary to maintain accurate forced resonance soft switching. Changes in system temperature, input voltage, output load current, and device degradation are all accounted for and optimized within the AI algorithm, which is being continuously updated.

The dynamic, soft-switching control AI is delivered in Pre-Switch's Pre-Flex programmable ICs. By incorporating a remote boot code on the chip, Pre-Switch can update the AI at any point during the life of an EV or other product, ensuring that performance is always optimal. Pre-Flex ICs also now include an embedded digital oscilloscope, Deep View, enabling designers to diagnose exactly what is occurring remotely, and then make adjustments in-situ. Traces can be recorded and exported out to see how the system is performing. If there are any issues, Deep View enables developers to understand why, so that actions can be taken. In future, preventative maintenance programs may be able to be implemented, using the feedback from Deep View and the remote programming capability. The practical implementation of soft-switching is resulting in huge drivetrain benefits.

Soft-switching inverter benefits

Soft-switching effectively eliminates switching losses for wide bandgap (WBG silicon carbide + gallium nitride) transistors, and reduces IGBT switching losses by approximately 65-80 percent, resulting in increased efficiency. Specifically, efficiency is improved in the low operating points for inverters where switching losses dominate total losses. The result is an inverter with higher peak efficiency,

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higher average efficiency and higher low-load efficiency. The elimination of switching losses also reduces cost by allowing designers to pass more current through a transistor with the same transistor loss budget. This is possible because the transistor is no longer dissipating switching losses as well as conduction losses. There is also a second order improvement in transistor conduction losses because the transistors are operating at lower temperatures. Both factors combine to reduce cost and size of an inverter.

The elimination of switching losses also means that inverter switching speeds – which today are limited to slow (10-15 kHz) frequencies in order to maintain efficiency – can be run 5-10X faster (50-100kHz) with the same or higher efficiency. Pre-Switch's higher switching frequencies have profound inverter and motor benefits. They include: a high-quality sine wave sent to the motor which improves motor efficiency; a reduction in the DC link capacitor size and cost by up to 90 percent; the elimination of audible noise that can be heard by human ears; and reduced common mode noise in the motor between the rotor and stator which is known to ruin motor bearings.

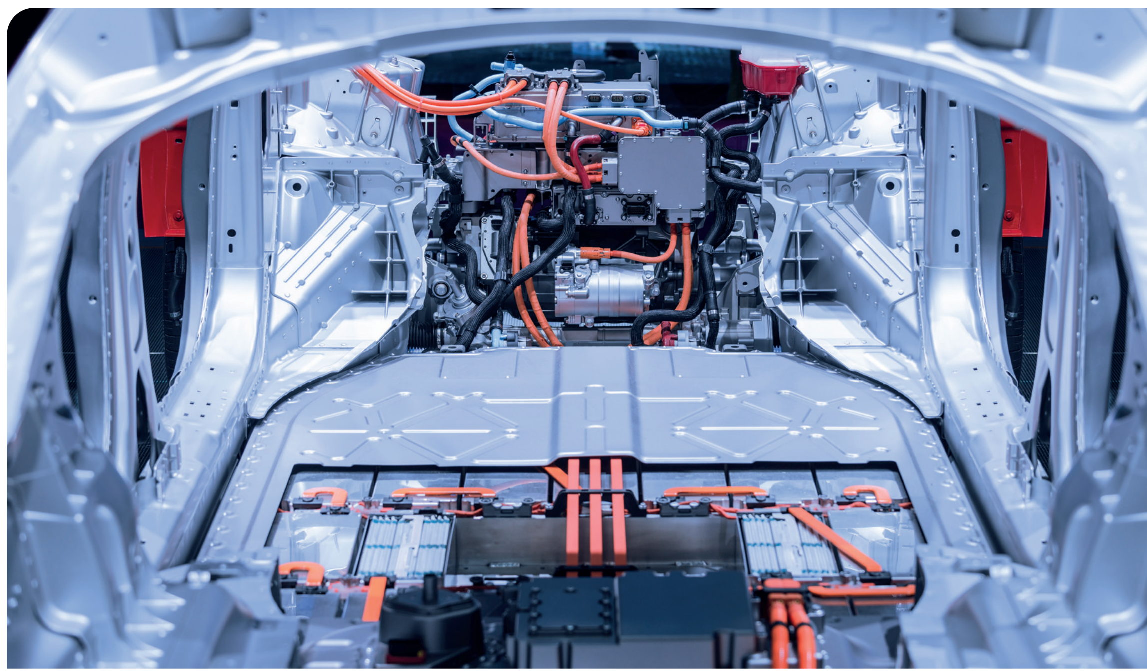
Soft-switching enables designers to build a lighter and lower cost inverter, as discrete transistors can be used instead of heavy and expensive power modules. Lastly, Pre-Switch technology virtually eliminates EMI because each transistor is turned on and off with no voltage or current present.

Soft-switching motor benefits

A soft-switching inverter reduces sine wave output distortion by 10 times, enabling motors to run more efficiently. In a conventional hard switching design, the output ripple current of the half-bridge circuit switching back and forth at 10-15 switching events per fundamental frequency causes a significant level of distortion. The distortion is effectively an induction heater in the motor coils and does no useful work. Soft-switching minimizes this ripple by switching 10 times faster. The reduced-distortion fundamental sine wave to the motor improves motor efficiency predominantly at lower RPM and lower torques which is where EV's are driven and increases EV range.

The second benefit of the Pre-Switch soft-switching architecture is that inverter dV/dt is configurable with a free lossless dV/dt filter that is part of the architecture. Reducing dV/dt improves motor reliability and reduces motor winding insulation allowing higher power density motors. Due to the fast edge speeds of WBG (SiC; GaN) transistors, high dV/dt is traded off for reduced switching losses. But high dV/dt speeds of above 10-15V/ns can cause insulation damage. Inverter designers in the past accommodate these excessive dV/dt speeds by adding extra insulation in the motor. This approach has the adverse effect of reducing motor power density and increasing motor costs. In contrast, the Pre-Switch architecture slows edge speeds but allows increased switching frequencies, eliminating the problem of high dV/dt speeds and reducing the insulation required.

Faster switching speeds mean that motors can be spun faster, so for some applications, a lower cost, lighter and higher RPM motor can be used. The final benefit for motor design is that because Pre-Switch-enabled systems switch so fast, low inductance motors can be used which have the benefit of being smaller and lighter and lower cost. This is particularly suitable for applications such as electric aircraft, where designers are trying to reduce the amount of iron in the motors to keep weight to a minimum.



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Driving motors in space

Its intrinsic radiation hardness and excellent electrical characteristics position the GaN HEMT as the ideal device for making circuits that drive motors in space

BY ANTHONY MARINI AND MAX ZAFRANI FROM EPC SPACE

THE NUMBER of satellites circling the globe in a low-Earth orbit is increasing at an astonishing rate. Back in 2019, active and defunct satellites totalled just over 3,000; today it's around 10,000; and by the end of this decade this figure will have rocketed to several hundred thousand.

This breath-taking growth in the level of activity in the outer reaches of the Earth's atmosphere has ensured that ventures and activities that at one time appeared far-fetched are now a certainty. That includes the commercial development of this sector, which is well underway, as well as manufacturing in space.

The latter, an activity that offers intriguing possibilities, will involve the use of all types of motors to perform every mundane and precision task associated with manufacturing. For those designing manufacturing systems for space, as well as having to source the most appropriate motor, efforts will need to be directed at carefully selecting the most appropriate driver, to ensure that the motor runs efficiently and reliably. Making such decisions are not easy, because the motor and its driver behave as a tandem entity, with their interplay

determining the system's mechanical and electrical attributes – both criteria are of critical importance for overall system performance. Partner a motor with an inferior driver and it will be incapable of operating efficiently and delivering its peak performance. Note that up in space efficiency really matters, alongside radiation hardness – excellence on both these fronts is needed without compromising the mechanical attributes of the motor, such as its speed and positional accuracy.

Varying requirements

When using a motor in space, there are specific challenges that depend on the physical location of the system, particularly with regards to radiation. Satellites orbiting the Earth have to handle radiation fields that are not found in stationary locations, such as the surface of the Moon or Mars.

Two classes of radiation are found in space: cosmic radiation, coming from high-energy particles that are moving at relativistic speeds; and lower energy protons and electrons from the solar wind, trapped in Van Allen radiation belts, due to the Earth's magnetic field.

When sensitive electronics is deployed in space, it is surrounded by shielding. However, there is a limit on how much shielding can be applied. Shielding adds mass to the launch – this incurs substantial costs, due to the energy required to either place objects in orbit or to escape the Earth's gravity. This cost-related limitation is particularly pressing in commercial space ventures, where financial margins really matter, and where constellations of low-cost satellites are stationed in primarily low-Earth orbits.

Due to this state-of-affairs, there's a need for electronics that has an inherent radiation 'hardness' or tolerance, and can survive high-energy insults and longer-term, lower-dose radiation exposure over the duration of the planned mission.

Another factor influencing the type of radiation, and its magnitude, that electronics will encounter in Earth's orbit is the altitude of the satellite. The radiation hardness requirement for a satellite in a low-Earth-orbit differs from that in a geosynchronous Earth orbit – and both these sets of requirements differ from those for landers and missions to the Moon and other planets, and for deep space probes. In all cases, those working on their particular ventures must consider the radiation profile over the life of the satellite or spacecraft, and carefully select every component within the motion control system to prevent its premature failure.

For motion control systems under bombardment by radiation, their weakest link is the electronics associated with their motor drives. The motors themselves are not a concern, as they provide a very robust component of the system – they are constructed from wire, and thus present an inherent radiation hardness during operation. That's not the case for the electronics that comprise the motor driver. This driver contains numerous interconnected semiconductor components, including: power switches for motor windings; associated catch diodes; and electronics that interfaces between circuity. All circuits and constituent components have to have an assured/tested level of radiation hardness to ensure that the mission will succeed long-term.

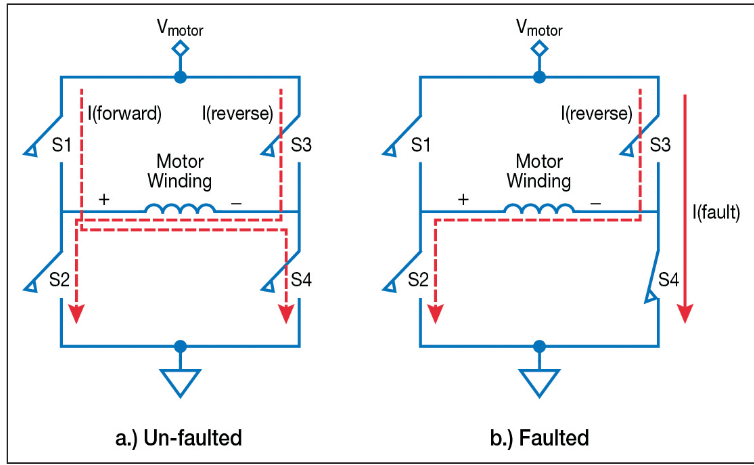


Figure 1. A single-phase motor driver with speed and direction control.

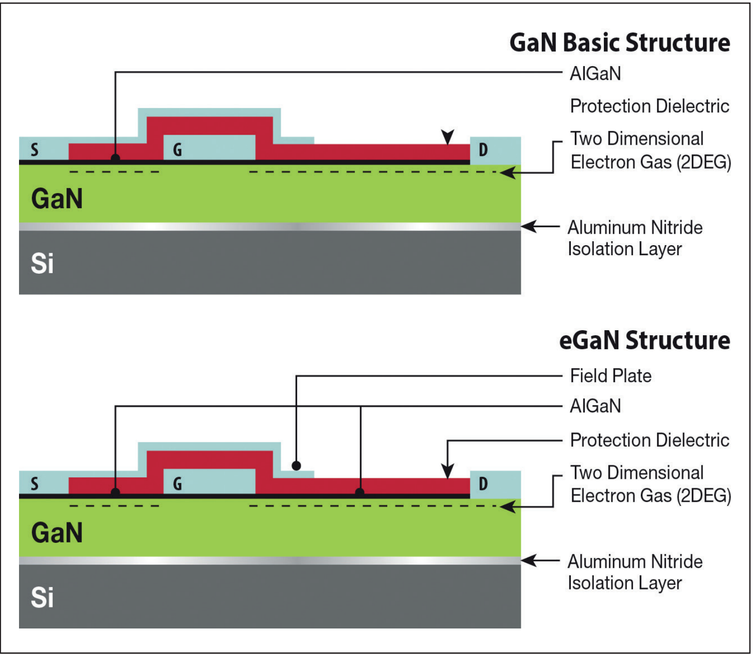
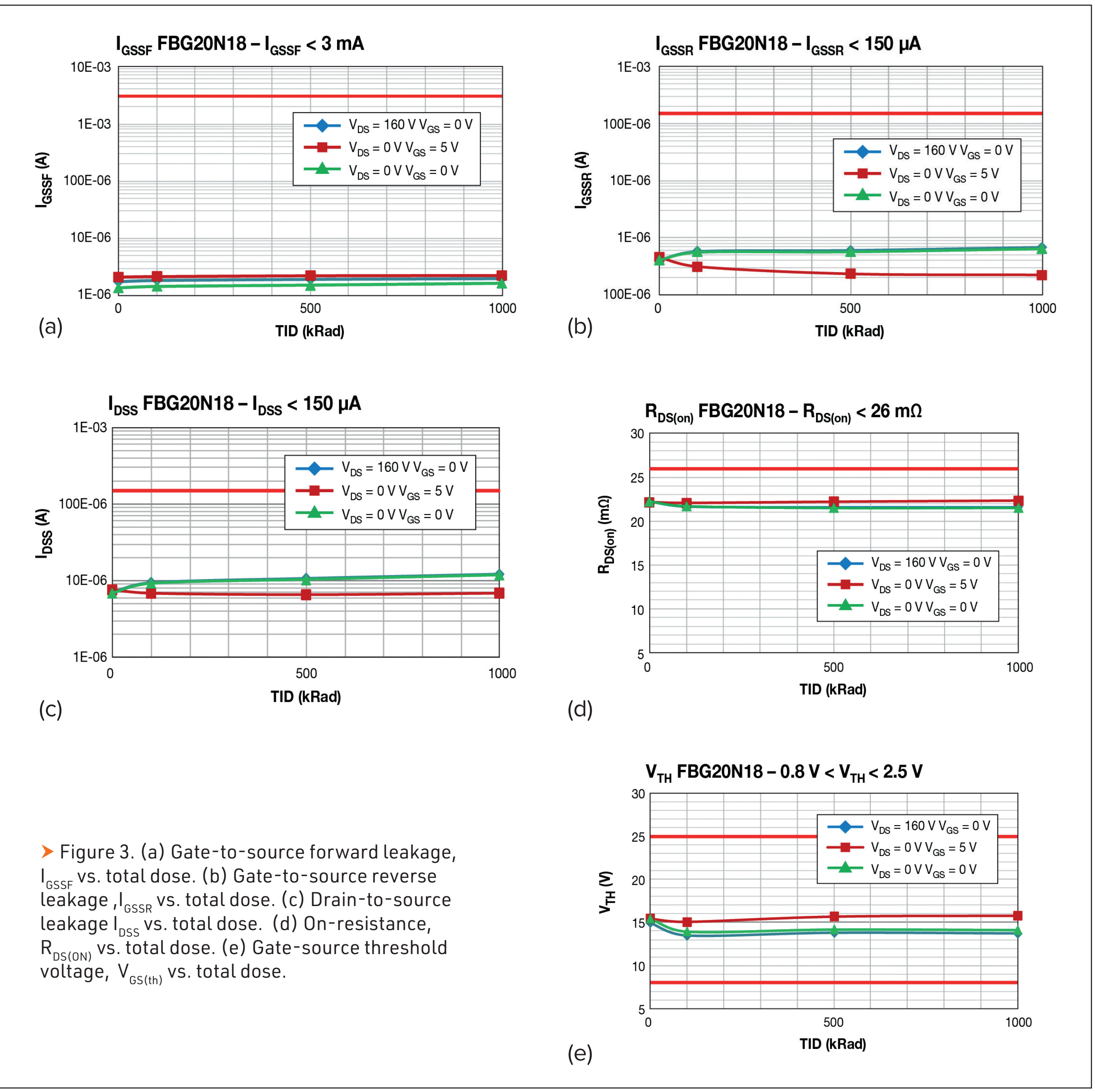


Figure 2. Depletion-mode (top) and enhancement-mode (bottom) GaN transistor structures.

There are operational implications from a radiation-induced event, ranging from erratic operation to outright system failure. Consider the case where a motor phase is being driven in an H-bridge configuration, as shown in Figure 1. In this circuit, the switches S1 through S4 represent the power switch transistors driven by the gate drivers. As depicted in Figure 1 (a), for the forward motor direction switches



➤ Figure 3. (a) Gate-to-source forward leakage, I_{GSSF} vs. total dose. (b) Gate-to-source reverse leakage ,I_{GSSR} vs. total dose. (c) Drain-to-source leakage I_{DSS} vs. total dose. (d) On-resistance, $R_{DS(ON)}$ vs. total dose. (e) Gate-source threshold voltage, $V_{GS(th)}$ vs. total dose.

S1 and S4 are closed/switched; and for the reverse direction, switches S2 and S3 are closed/switched. In both cases, it is the pulse-width modulation control of the switches that determines the speed of the motor.

If high-energy radiation disrupts the gate driver circuit or the output power switch, represented by S1-S4, this can cause S1 to S4 to either open or close momentarily. In the open switch case no damage occurs, and the only downside is a missed switching opportunity. But in the closed case, the damage can be catastrophic. For example, consider what could happen when S4 is induced closed by radiation when it isn't supposed to be, and S3 is simultaneously closed in normal reverse-direction operation. In that scenario, shown in Figure 1 (b), a cross-conduction event will occur from V_{DD}-to-ground through S3 and S4, destroying one or both switches. Clearly, this event, arising from uncontrolled current flow, must be avoided at all costs.

In the space environment, GaN transistors are ideal candidates for rad-hard transistor switches. These devices are blessed with an inherent tolerance to total ionizing dose radiation. They can be exposed to megarads of radiation without serious consequence; the only noteworthy changes are a slight rise in the gate and drain leakage currents. Thanks to their lateral structure and the absence of gate oxides and substrate-related junctions, these devices are immune to damage from interaction with single, energetic particles, so long as the transistor is well designed (see Figure 2). The robustness

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Our products offer inherent radiation hardness, a trimming of size and weight, and a reduction in losses from heat generation, allowing designers to focus on optimising the electro-mechanical performance of the motor system

that a 200 V, 18 A discrete GaN HEMT provides is illustrated by typical radiation performance data. This device is adept at handling ionising doses (see Figure 3), neutron radiation (see Figure 4) and heavy ion bombardment (see Figure 5). These results underscore the robust immunity GaN transistors provide to various forms of radiation found in space.

As well as great robustness to radiation, GaN HEMTs excel in electrical performance, due to their high electron mobility and wide bandgap. The transistors also exhibit a low on-resistance and low input capacitance, ensuring that the figure-of-merit that comes from the product of these two characteristics tends to be more than ten times lower than that of similarly rated silicon MOSFETs.

At EPC Space, a joint venture between EPC Corporation and VPT Corporation, we have been developing a product line of rad-hard discrete and modular components for space motion control, as well as other power-related applications. Drawing on EPC's proprietary Rad Hard eGaN HEMTs, our portfolio of discrete devices provides two packaging configurations: hermetically-sealed devices in thermally-efficient AlN ceramic packages; and discrete devices mounted to AlN ceramic die adapters/'inteposers', designed for hybrid applications. Modular devices in our family include single and dual low-side gate drivers; single and dual low-side power drivers, incorporating proprietary GaN-driving-GaN gate drivers, along with power HEMT switching elements and Schottky catch rectifiers; and a half-bridge driver comprised on independent low- and high-side power drivers. All devices have demonstrated radiation performance.

One of the products within this portfolio, the FBS-GAM02-P-R50 module, can be readily configured in a half-bridge configuration (see Figure 6). This module, housed in an 18 pin non-hermetic plastic

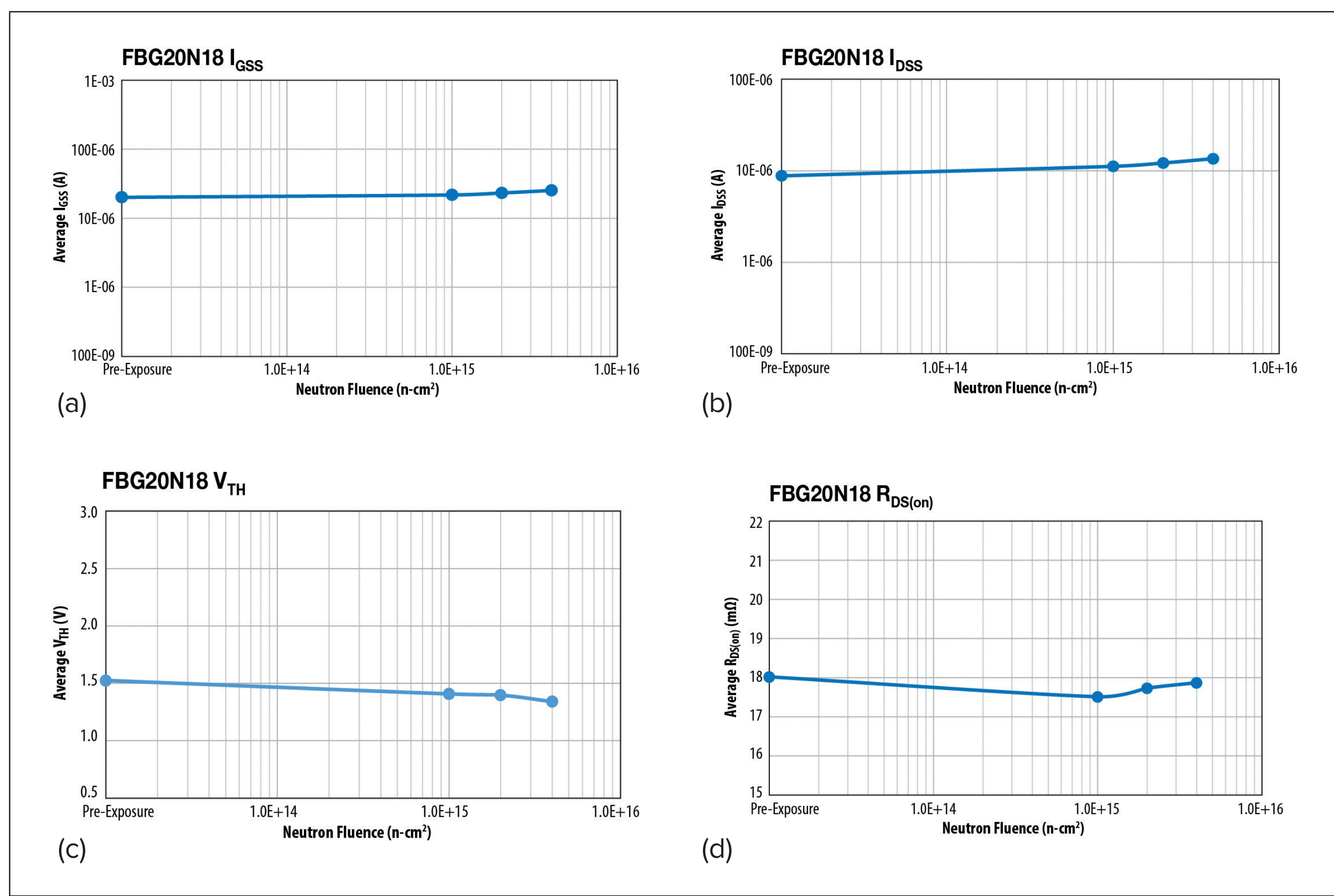


Figure 4. (a) Gate-to-source leakage, I_{GSS} vs. neutron fluence. (b) Drain-to-source leakage, I_{DSS} vs. neutron fluence. (c) Gate-source threshold voltage, $V_{GS(th)}$ vs. neutron fluence. (d) (d) On resistance, $R_{DS(ON)}$ vs. neutron fluence.

over-molded package, features low- and high-side power switches, gate drivers and Schottky catch rectifiers, a high-side bootstrap capacitor and diode, an under-voltage 'power good' function, and input shoot-through protection.

Many of the motors that are used in space drive reaction wheel assemblies. This includes the use of three-phase motors to drive spinning masses in the *x*, *y* and *z* axes, to create inertia in one or more of these axes and ultimately control the altitude and position of a spacecraft in orbit. By selectively changing the speed of rotation, and thus the inertia of the spinning mass, it is possible to control the pitch, yaw and orbital position of the spacecraft. To control the three-phase motor, three half-bridge drivers are required per motor. And as three axes require control, nine half-bridge drivers are needed for each reaction wheel assembly system.

To address this motor drive requirement, we have developed the EPC7C006, a three-phase motor demonstration board that utilises the GAM02 as the three-phase control switches (see Figure 7). This board is designed to be either stand-alone, with phases driven by external three-phase digital pulse-width modulation signals, or to interface with the EPC9147A microcontroller interface board – it features a Microchip DSP to provide a pulse-width modulation signal for each phase, based on voltage, current and optional positional feedback. This control board utilises the Microchip motorBench Development Suite, under license to EPC. Thanks to this, designers either control the motor to be driven in the end-application with an existing control system developed in-house, or with a purpose-built control system that interfaces to a computer via a USB connection and GUI interface provided by us or EPC.

There's no doubt that the commercial and industrial activities planned for space, both in orbit and extra-terrestrially, are demanding and exciting. Many motors are already spinning away in space, and it is a sure bet that far, far more will follow. Thanks to our efforts, circuit designers no long need to feel daunted by the task of implementing high-reliability motor control circuits, due to the availability of robust, rad-hard, high-performance discrete devices and modular components for motor drive/control. Our products offer inherent radiation hardness, a trimming of size and weight, and a reduction in losses from heat generation, allowing designers to focus on optimising the electro-mechanical performance of the motor system. Do this, and the biggest benefit of all is keeping the motor system in question on-orbit, or fulfilling its mission elsewhere.

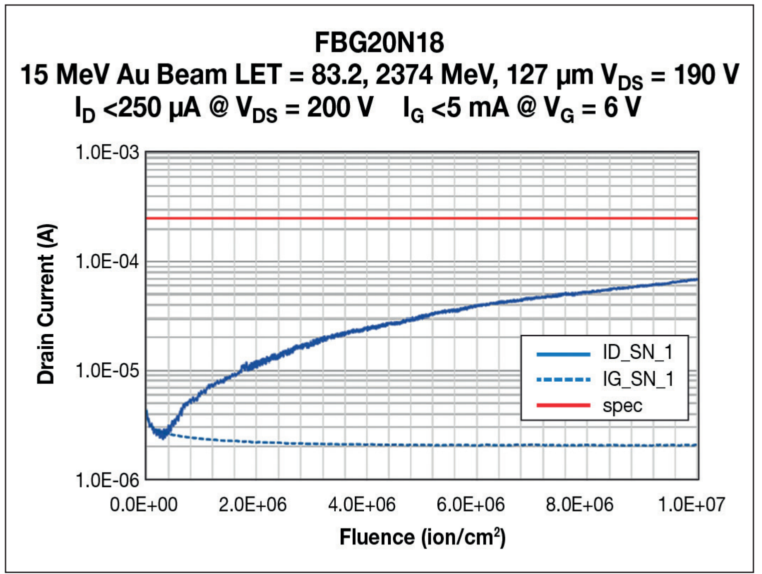


Figure 5. Gate to Source leakage and Drain to Source Leakage, I_{GSS}, I_{DSS} vs. Fluence at LET =83.

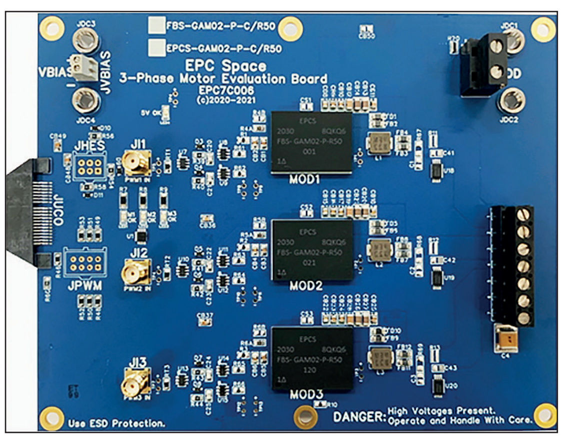


Figure 7. EPC Space EPC7C006 three-phase motor driver demo board, which measures 6.50 inch by 5.22 inch.

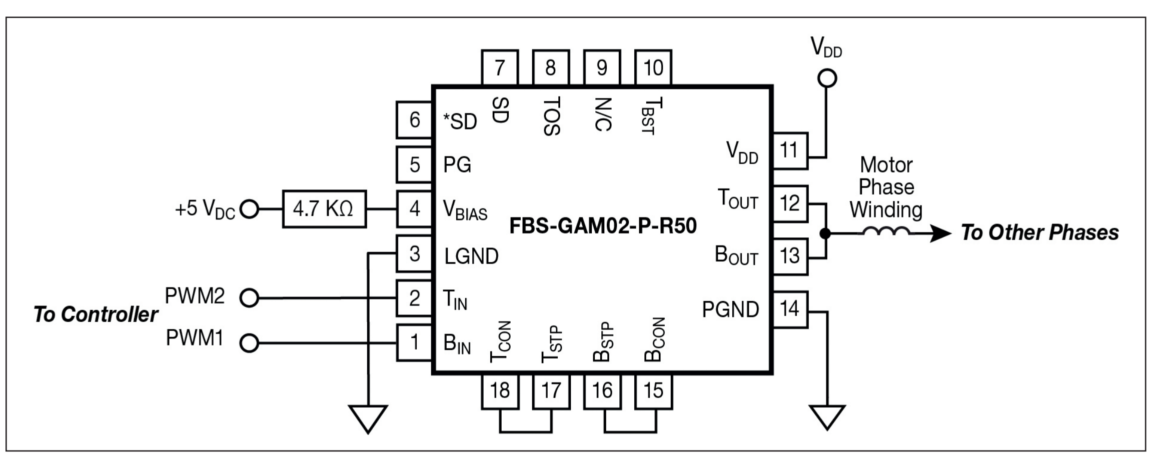


Figure 6. EPC Space FBS-GAM02-P-R50 in a half-bridge configuration.

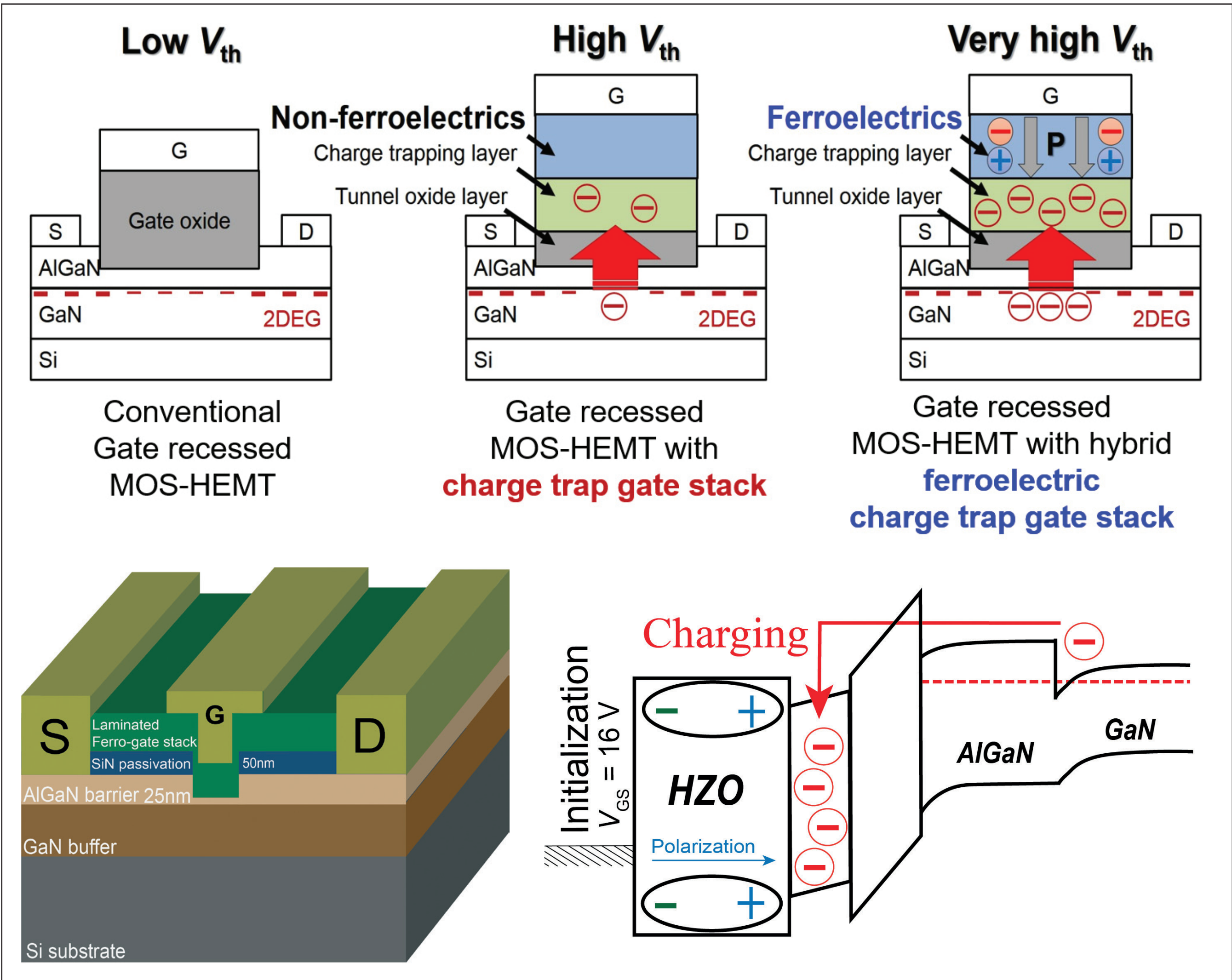
Enhancing the ferroelectric gate HEMT

Adding lanthanum doping and a ZrO_2 seed layer to a normally-off ferroelectric gate HEMT causes leakage currents to fall, threshold voltage stability to increase and lifetime to lengthen

BY EDWARD YI CHANG FROM NATIONAL YANG MING CHIAO TUNG UNIVERSITY

GaN IS AN incredible material for producing high-power and high-frequency electronic devices. In particular, when it is used to make a HEMT, it enables exceptional performance in power switching and radio-frequency applications. Drawing on the unique polarisation-induced electric field, the GaN HEMT combines a very low resistance with a high output power. However, the internal electric field within this device is both a blessing and a curse, as it creates an obstacle to enabling enhancement-mode operation, which is strongly desired for safe operation in power-switching systems.

Given the importance of realising enhancement-mode operation, also known as normally-off, it's not surprising that several technologies have been developed to meet that goal. Those approaches include the introduction of a recessed gate, *p*-GaN gate, fluorine implantation, and oxide charge engineering. For all these designs, to avoid faulty turn-on, the threshold voltage for a power device should be around +3 V. However, meeting this requirement and ensuring normally-off operation has compromised performance, with the approaches just described for realising enhancement mode leading to an inferior current



➤ Figure 1. An enhancement-mode hybrid ferroelectric GaN HEMT with a charge storage gate combines a high threshold voltage with a low on-resistance and a high output current.

density and on-resistance, compared with state-of-the-art normally-on devices. So the search has continued for a normally-off GaN technology for power devices.

Offering much hope in this regard is the work of our team at the National Yang Ming Chiao Tung University, Taiwan. Recently, we have developed ferroelectric charge trapping gate (FEG) GaN MIS-HEMTs, namely FEG-HEMTs.

These hybrid, novel, high-performance devices combine good power-electronic characteristics with those associated with flash memory. Drawing on the low crystallisation temperature for solid solutions of $Hf_{0.5}Zr_{0.5}O_2$ and the feasibility of atomic layer deposition, the hybrid ferroelectric charge-trapping gate stack that lies at the heart of our devices has gradually gained a great deal of attention, because it enables a simple way to realise enhancement-mode operation with a threshold voltage of more than 2.5 V. The combination of the charge-trapping layer and the ferroelectric leads to a positive shift in the threshold voltage beyond the safety margin of +2.5 V after a positive gate bias initialisation. This ensures enhancement-mode operation (see Figure 2).

Our FEG-HEMTs deliver extraordinary static and dynamic performance. Their strengths include a high threshold voltage, a high off-state breakdown, and a low dynamic on-resistance. These transistors are particularly attractive for enhancement-mode high-frequency power-switching applications, and especially, their capability to provide a large forward gate voltage swing – this ensures tremendous immunity to large positive-voltage overshoot spikes. However, for the *p*-GaN power transistors, a gate stress of more than 10 V could easily result in gate breakdown.

The ferroelectric charge trap gate is still in its infancy, and more intensive research and development are needed before the commercialisation of this power device. A critical

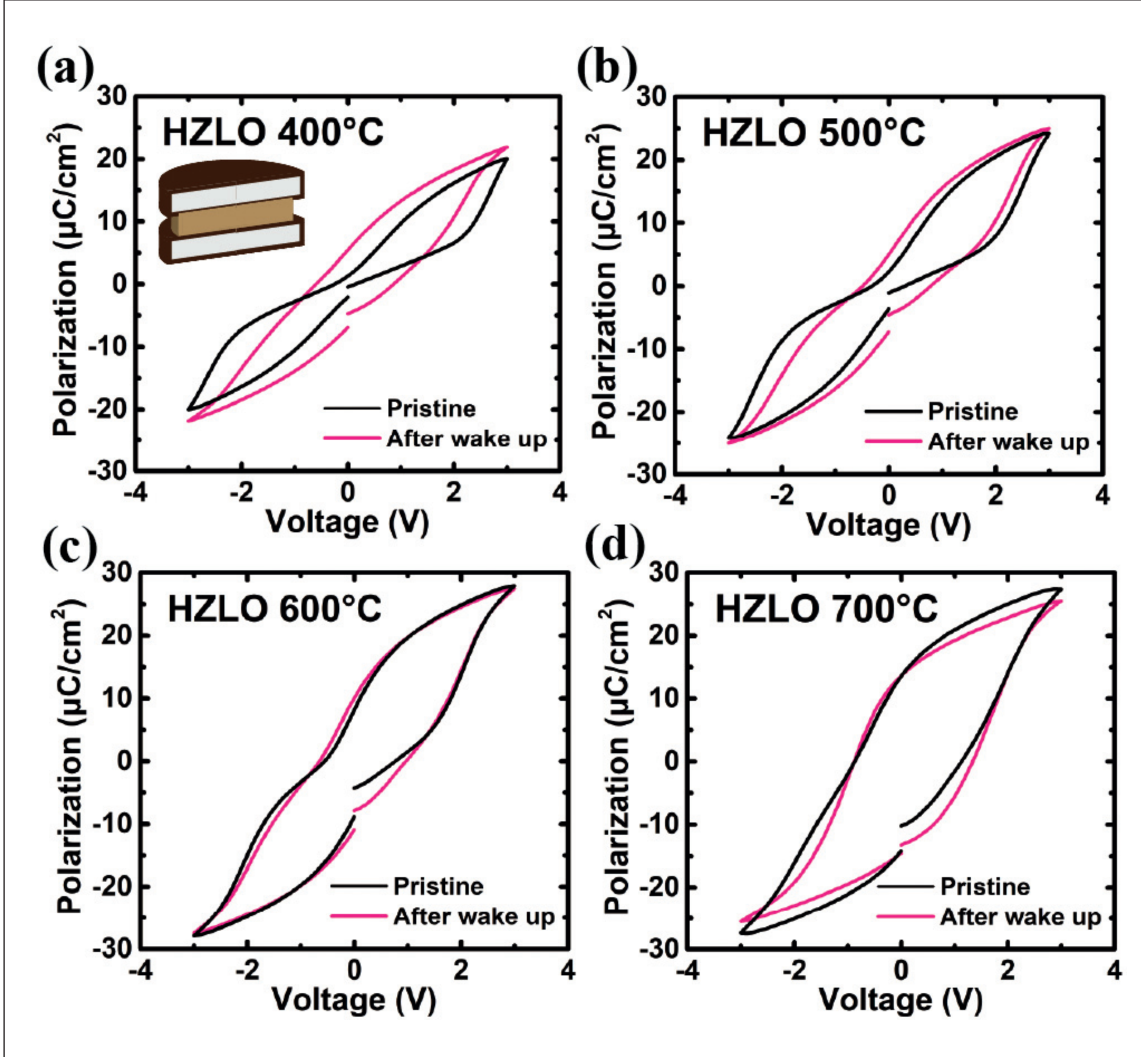


Figure 2. Polarisation as function of voltage for TiN/ lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$ (HZLO) (10 nm)/ TiN metal-ferroelectric-metal stacks.

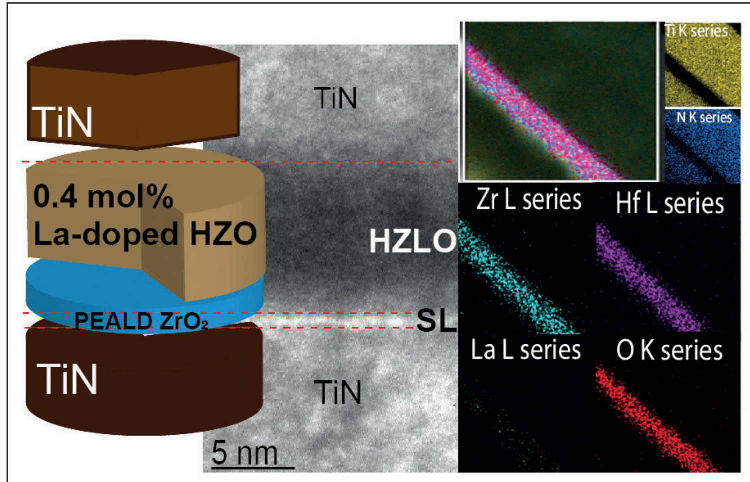


Figure 3. Schematic structure, transmission electron microscopy image, and energy-dispersive spectroscopy mapping of the TiN/ lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$/plasma-enhanced ALD ZrO_2 seed layer/ TiN metal-ferroelectric-metal stacks.

issue for every form of enhancement-mode GaN MIS-HEMT is its threshold voltage stability. This is especially important for GaN FEG-HEMTs, due to the charge-trapping nature of the charge-trapping layer, and also the stability of the ferroelectric behaviour – any changes here will have a big impact on threshold voltage behaviour, and can lead to instability in this key characteristic. It's also important to note that the reliability of the FEG-HEMT could be accelerated by electron-impact ionization and the generation of thermal defects.

To further advance our devices, we have introduced lanthanum-doping to our $Hf_{0.5}Zr_{0.5}O_2$, using a seed layer ferroelectric engineering technique. Read on to discover the effect of lanthanum doping on $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric thin films, as well as how a ferroelectric-engineered enhancement-mode FEG-HEMT can increase the charge retention time and the time-dependent dielectric breakdown lifetime for this type of device, as well as improving its gate swing. These advances are helping to bring devices with a ferro-charge-trapping gate stack closer to commercialisation.

Ferroelectric engineering

The benefit of doping with elements from the

lanthanoid series, and large trivalent dopants in general, is that they can increase the ferroelectric phase in HfO_2 films and enhance the stability of the threshold voltage, thanks to a larger remnant polarisation after initialisation. In addition, when lanthanoids are added to $Hf_{0.5}Zr_{0.5}O_2$ films with an acceptor centre, this can shift the Fermi level of the $Hf_{0.5}Zr_{0.5}O_2$ to the mid-gap position, leading to a significant reduction in leakage current.

A lower leakage current is advantageous on many fronts, enabling an increase in gate voltage swing, a lengthening of the time-dependent dielectric breakdown, and more complete charging during initialisation.

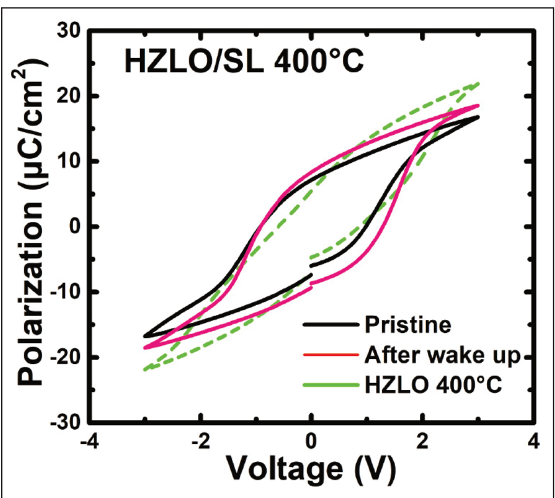
We have plotted polarisation-voltage loops of our lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$ metal-ferroelectric-metal structures for different post-metal annealing temperatures. We found that polarisation increases with annealing temperature, and only the highest annealing temperature, 700 °C, caused the sample to exhibit a wake-up-free behaviour in its pristine state.

Additional measurements showed that lanthanum doping delivers a significant reduction in the leakage current of these structures. Here, lanthanum acts as an amorphiser in hafnium oxide.

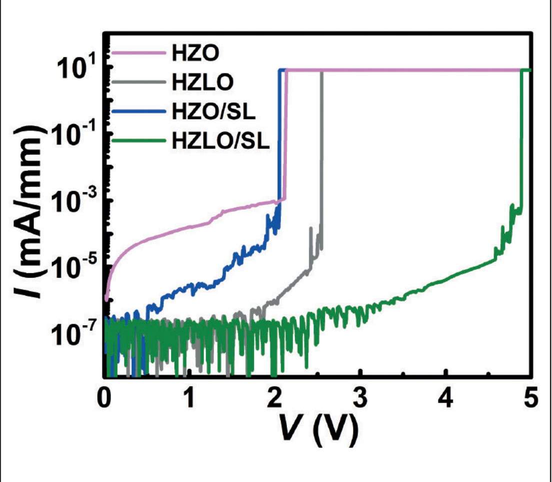
To lower the thermal budget while maintaining the benefits of lanthanum doping – including a high remnant polarisation and a reduced leakage current – we introduced a seeding layer. Inserting a seed layer of ZrO_2, grown by plasma-enhanced atomic layer deposition, beneath the lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$ enhanced its nucleation and slashed the temperature required for post-deposition annealing (see Figure 3). Our measurements revealed that the addition of the seed layer also increased the strength of the polarisation by 50 percent, and cut the annealing temperature for wake-up-free behaviour from 700 °C to 400 °C (see Figure 4).

From this, we have concluded that we have realised a more stable ferroelectric behaviour, which aids the threshold-voltage stability of FEG-HEMTs. The addition of the seed layer, as well as the introduction of lanthanum, benefits electrical characteristics, with the soft breakdown significantly muffled and the hard breakdown further delayed (see Figure 5).

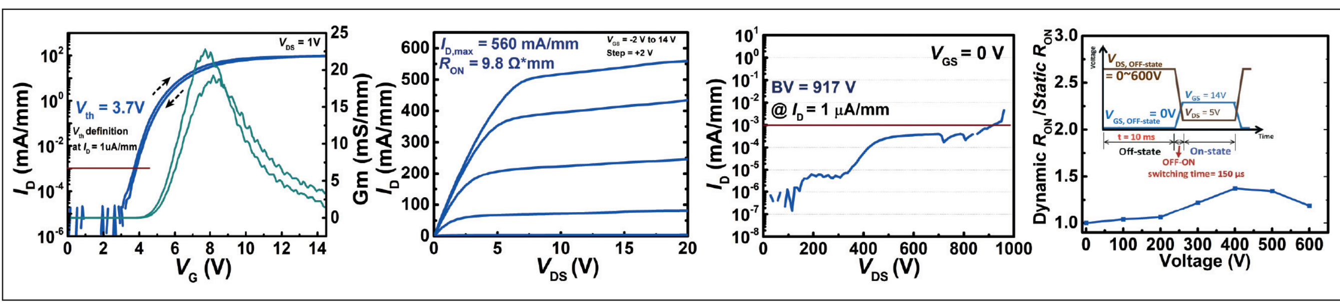
We have found that the addition of our ZrO_2 seed layer promotes the formation of the o-phase, improves crystallinity, and reduces the thermal budget. This led us to investigate whether this seed layer could decrease the annealing temperature required for the FEG-HEMT to exhibit its ideal characteristics. Initial results are very encouraging. Our enhancement-mode GaN FEG-HEMT exhibits



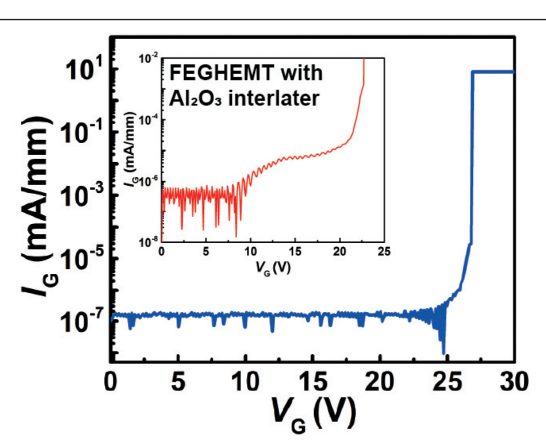
➤ Figure 4. Polarization versus voltage plots of lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$ metal-ferroelectric-metal stacks featuring a ZrO_2 seed layer.



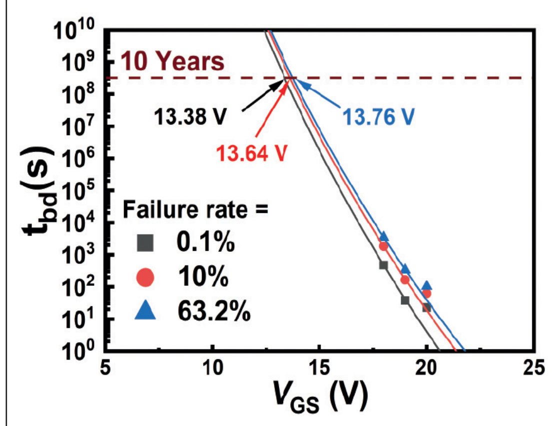
➤ Figure 5. DC leakage current characteristics.



➤ Figure 6. Static and dynamic on-resistance performance of the FEG-HEMT with a laminated ferroelectric gate stack formed with lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$, grown on a ZrO_2 seed layer.



➤ Figure 7. I_G-V_G gate leakage and gate breakdown characteristics. Inset shows data from previous works without the enhanced ferro-charge trapping gate stack.



➤ Figure 8. Lifetime prediction of the FEG-HEMT with lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$, grown on a ZrO_2 seed layer.

a positive threshold voltage of 3.7 V and threshold voltage hysteresis of just 0.12 V (see Figure 6). The output characteristics are a maximum drain current density of 560 mA/mm and an on-resistance of 9.8 Ω·mm. The off-state breakdown voltage is as high as 917 V at a gate-source voltage of 0 V, while the ratio of dynamic to static on-resistance is low, with a value of just 1.37.

Improving reliability

The combination of the lanthanum-doped $Hf_{0.5}Zr_{0.5}O_2$ and the seed layer leads to promising gate leakage and gate breakdown characteristics for the laminated ferroelectric gate stack (see Figure 7). Thanks to an enhanced nucleation seeding layer and crystallisation of La_2O_3, there is no longer a soft breakdown, and there is a high hard breakdown voltage. Improvements in gate breakdown lead to a larger off-state breakdown voltage, more complete charging of the charge trapping layer, and a higher gate swing.

We have undertaken an electric-field-accelerated time-dependent dielectric breakdown test on our laminated ferroelectric-gate stacks with lanthanum doping and seed layers (see Figure 8). Using a gate-voltage power-law model to analyse trap generation and gate leakage mechanisms, we determined, using a failure rate of 0.01 percent, that our ferroelectric charge trapping gate stack could withstand a voltage of up to 13.38 V for 10 years.

This is a very encouraging result, given that in the literature, the equivalent figure for *p*-GaN devices with a failure rate of 63.2 percent is below 6.5 V. The high time-dependent dielectric breakdown shows that in addition to exceptional electrical characteristics, our FEG-HEMTs can handle a larger gate voltage swing.

As well as improving gate leakage, our ferroelectric-engineered FEG-HEMTs with a seed layer offer improved threshold voltage stability. These enhancement-mode devices have a threshold voltage of 3.1 V after a 30,000 s threshold-voltage retention test (V_{GS} = 0 V, V_{DS} = 0 V).

What's more, the threshold voltage values after 1,000 s shows a stable trend. We estimate a threshold voltage of 2.9 V for a retention time of 10 years. Our novel hybrid ferroelectric charge trap gate stack scheme has introduced a brand new perspective to realising enhancement-mode operation in GaN MIS-HEMTs, so that they meet system-level requirements found in the likes of the electric vehicle and photovoltaic industries.

As well as the efforts described here, in recent years investigations have evaluated the possibility of improving FEG-HEMTs via nitrogen incorporation, other forms of ferroelectric engineering, and the addition of a source-connected field plate. With all this progress, there is good reason to believe that enhancement-mode GaN FEG-HEMT technology is destined to play a major role in the future of GaN power electronics.

Our novel hybrid ferroelectric charge trap gate stack scheme has introduced a brand new perspective to realising enhancement-mode operation in GaN MIS-HEMTs, so that they meet system-level requirements found in the likes of the electric vehicle and photovoltaic industries

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Making headway with normally-off Ga_2O_3 transistors

Multiple sub-micron fins ensure far greater consistency in threshold voltage

A TEAM from Novel Crystal Technology (NCT), Japan, is claiming to have made significant progress in the design and performance of β-Ga_2O_3 vertical transistors. The team's normally-off devices are said to combine a ground-breaking consistency in threshold voltage with good values for on-resistance, channel mobility and current density.

This success will help to drive the progress of power devices made from β-Ga_2O_3. Drawing on a bandgap of 4.5 eV or more and a theoretical breakdown electric field of 6-8 MV cm^{-1}, devices made from this oxide are promising candidates for power electronics, particularly for deployment in power conditioning, power distribution and switching applications.

➤ Novel Crystal Technology's multi-fin transistors have a relatively small variation in threshold voltage

The Achilles heel for Ga_2O_3 is its lack of *p*-type doping. Due to this, normally-off characteristics have been realised by turning to lateral transistors with a recessed gate and a sub-micron fin-channel. However, with this design the threshold voltage is then governed by the recess depth and the sub-micron fin width.

"Although it is technically possible to fabricate FETs with sub-micron patterns, it requires equipment dedicated to microfabrication, such as an electron-beam exposure machine," argues Daiki Wakimoto from NCT. He explains that 100 mm and 150 mm production lines use i-line stepper exposure tools, which are less accurate and would struggle to offer sufficient control over the dimensions of the sub-micron FETs.

To overcome this issue, some researchers have investigated β-Ga_2O_3 high-resistive *p*-well-like structures, which have a threshold voltage that depends on the dopant concentration of deep acceptors. But these devices are yet to fulfil their promise: in once case, the device only operated in the sub-threshold regime; while another required a positive gate-bias of 25 V.

NCT's devices, which employ several sub-micron fins with a width that has very little impact on the threshold voltage, feature a 3.3 µm-thick nitrogen-doped Ga_2O_3 well layer. This well is grown by HVPE on an n^+ β-Ga_2O_3 substrate that does not have a drift layer.

Fabrication of the transistors began with two silicon-ion implantation steps, employed to connect the MOS channel to the source region, and to enable an ohmic contact to the source. A combination of mask deposition, electron-beam lithography and dry etching defined fin channels with near-vertical sidewalls, before the addition of: a 53 nm-thick SiO_2 gate dielectric by atomic layer deposition; and source, gate and drain contacts by electron-beam evaporation.

The team's portfolio of devices features fins with widths of either 1.0 µm, 1.5 µm or 2.0 µm. Each transistor has 14 fins, but only 10 are covered with the source electrode, because those on the outside often have large errors in dimension, due to what's described as a micro-loading effect.

According to Wakimoto, the etching environment differs between the pattern's outermost periphery and its inside. "We select conditions that stabilise the inner shape, so the error in the outer dimensions becomes larger than the inner dimensions." This problem has been seen in other materials, and resolved by optimising etching conditions. "Therefore, we believe that gallium oxide can be improved in the same way," added Wakimoto

Electrical measurements on the devices revealed: a threshold voltage of around 1.9 V; a current density of 760 A cm^{-2}; an on-resistance of 2.9 mΩ cm^2; and a mobility of around 100 cm^2 V^{-1} s^{-1}, a value that is said to be attractive for making 600 V to 3 kV MOSFETs.

Wakimoto are co-workers are now planning to increase the threshold voltage of their devices, via greater nitrogen doping, to 3 V or more, a pre-requisite for practical power devices.

REFERENCE

➤ D. Wakimoto *et al*. Appl. Phys. Express **16** 036503 (2023)

HEMTs: Optimising the architecture

An AlN back barrier and a thin GaN channel equips the HEMT with better characteristics for wireless communication

A PARTNERSHIP between researchers at Xidian University and Nanjing Electronic Devices Institute is claiming to have broken new ground with the GaN HEMT by combining an ultrathin GaN channel with an AlN buffer layer.

"As a result, the power characteristics, off-state leakage characteristics, voltage endurance characteristic, linearity and high-temperature performance of the device have been greatly improved," enthuses team spokesman Kui Dang from Xidian University.

This team from China is not the first to investigate this particular architecture, which benefits from the switch from a conventionally doped high-resistance GaN buffer to an AlN buffer with a far wider bandgap and the highest thermal conductivity of any common III-N. However, previous HEMTs with this design employed GaN channels more than 200 nm thick, with reports offering little detail into the device's carrier transport properties, high-temperature performance or breakdown characteristics. The HEMT fabricated by Dang and colleagues features a GaN channel just 120 nm-thick, realised by modulating the growth mode.

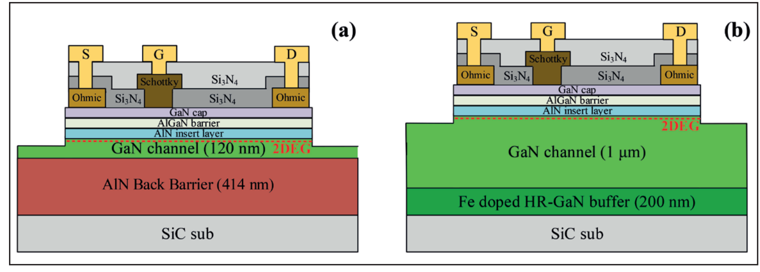
Growth of this device exploits previous work by the team, which determined that modulation during the MOCVD process alters the film-forming point of a GaN channel grown on an AlN buffer, opening the door to thinner channels. "That is why the results in previous reports all possess a thick GaN channel," explains Dang.

Key to the novel growth is an ammonia partial pressure – this slows deposition and advances the film-forming point of the GaN channel on the AlN buffer.

HEMTs were produced by loading SiC substrates into an MOCVD reactor and depositing: a nucleation layer; an AlN buffer, grown at high temperature; a GaN channel, formed by modulating the growth mode; a 1 nm-thick AlN interlayer; a 20 nm-thick $Al_{0.28}Ga_{0.72}N$ barrier; and a 2 nm-thick GaN cap.

Dang and co-workers have found that the film-forming point for GaN that's grown on AlN varies with the thickness of the AlN layer. Due to this, after deciding the thickness for the GaN channel, it's important to employ the appropriate associated thickness for the AlN buffer. For the 120 nm-thick buffer, a 414 nm-thick back barrier is employed, said to ensure excellent confinement of the two-dimensional electron gas, along with high crystalline quality and excellent transport properties.

The team have compared the performance of a device with this heterostructure with that featuring a more conventional design, including a 200 nm-thick high-resistance iron-doped buffer and a 1 μm-thick channel. HEMTs with a 50 μm gate width, a gate length of 1.5 μm, and a range of gate-to-drain spacings were fabricated from both heterostructures.



➤ Researchers from Xidian University and Nanjing Electronic Devices Institute have demonstrated that HEMTs with an AlN buffer (a) have superior characteristics to those with a GaN buffer (b).

The HEMT with the conventional design had a slightly higher mobility, attributed to less interface scattering, which reduces mobility. However, the sheet density in the novel device is higher, thanks to the back barrier effect of the AlN buffer.

Additional measurements revealed that the HEMT with the AlN back barrier has a maximum drain current density of 1170 mA/mm, realised with a gate-source voltage of 3 V and a drain-source voltage of 8.6 V. This peak current density exceeds that for the conventional device, which topped out at 1047 mA/mm.

Measurements of DC transfer characteristics determined that the device with the AlN back barrier had a transconductance of 185 mS/mm, compared with 175 mS/mm for the reference design. The novel design also provides a greater degree of transconductance flatness, a valuable asset, because it is related to the linearity of microwave power devices. Greater linearity leads to a superior signal quality for communication, and a reduced code error rate.

Further benefits of the AlN back barrier are a quashing of the leakage current, particularly at elevated temperatures, and a hike in breakdown voltage – for devices with a 4.5 μm gate-to-drain spacing, introduction of the AlN barrier increased breakdown from 129 V to 209 V.

One of the team's next goals is to switch to an ultra-wide band gap AlGaN channel, which promises to deliver significant increases in power and efficiency. "The relevant research is under way," says Dong.

REFERENCE

➤ Y. Zhang *et al.* Appl. Phys. Lett. **122** 142105 (2023)

This year's IRPS was held in Monterey, CA, bot far from the famous Bixby Bridge.

Superior testing of SiC

Speakers at the International Reliability Physics Symposium detail the most insightful approaches for evaluating the long-term capability of SiC power devices

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AT THE VERY EARLIEST STAGES of development of any power device, the focus is always on instantaneous performance characteristics, such as on-resistance, blocking voltage and peak current delivery. But it's not that long until evaluation expands to include insights into reliability. After all, if the device doesn't last long enough to serve in any practical application, it will never be commercially viable.

As the device matures and volume production begins, new questions need answering when assessing reliability. For example, there is a need to know what fraction of devices will fail at any point in time. It's also beneficial, from the perspective of the customer base, to vary the conditions of assessment to reflect different applications; and it may be crucial to pinpoint any drifts in key characteristics, even if this doesn't lead to device failure, as it could still be a compromise too far.

All these sorts of questions are now being asked of SiC transistors and diodes, power devices that are well beyond the stage of simply being promising – they are netting billions of dollars per year, with sales ramping fast.

Insights into better approaches for assessing the reliability of SiC power devices, alongside commentary considering what traditional methods may overlook, formed the heart of several presentations at the recent *International Physics Reliability Symposium*.

At this meeting on 28 to 30 March, held on-line and also in person in Monterey, CA, illuminating talks on SiC included those from: ABB's Elena Mengotti, who revealed the various tests that this company is using to assess the reliability of SiC MOSFETs from different suppliers; Kin Cheung from NIST, who explained why exceptional wafer cleaning fails to guarantee a great gate oxide; and Peter Moens from onsemi, who made a strong case for distinguishing between the lifetime of the SiC MOSFET and its useful time.

Seeking standardisation

Mengotti, a Principal Scientist at ABB's Corporate Research Centre in Switzerland, claimed that one of the issues surrounding SiC power devices is the variation in testing.

"The standardisation of silicon carbide diodes and MOSFETs has not yet converged to a set of stable

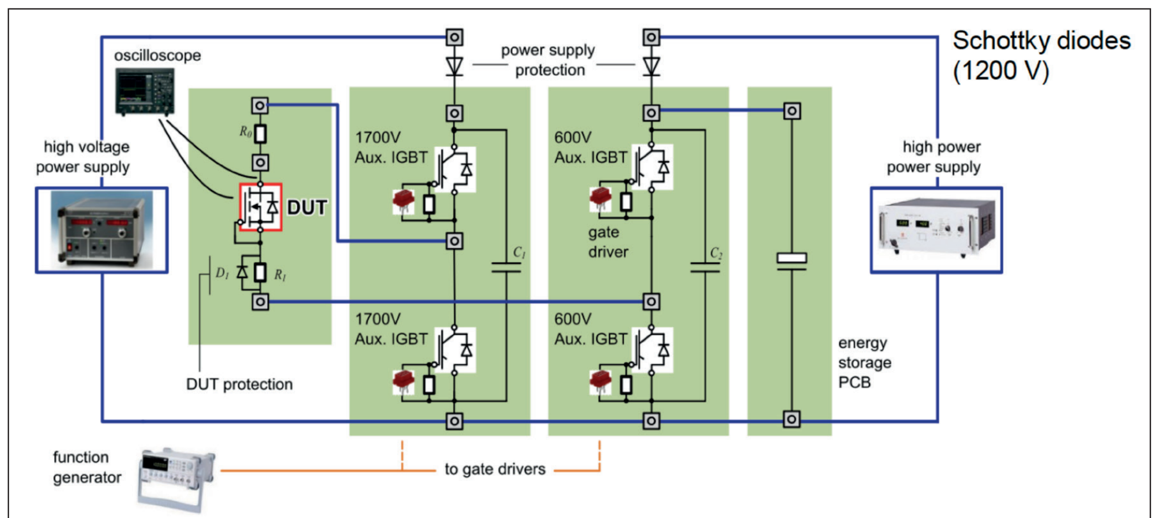


Figure 1. ABB evaluates SiC power devices with a variety of tests. Two half-bridge legs subject devices to stress, with characterisation following this procedure.

and specific tests to pass that the industry can simply request from the supplier," argued Mengotti.

While she is in no doubt that SiC outperforms silicon, she points out that any new technology introduces new failure mechanisms. Consequently, new qualification methodologies are needed to minimise the risk during initial device deployment.

Taking action on this front, ABB has developed a number of in-house tests, covering both the chip and the package.

One such test is that of avalanche ruggedness, an assessment that's suitable for applications where there is a switching of the inductive load. At ABB this test, conducted on chips in a TO-247 package, begins by charging the load inductor with a current that's low enough to avoid device self-heating.

The device is then turned off, with avalanche energy dissipated in the MOSFET. Those carrying out this test determine the destruction energy limit for five samples, before conducting further tests on eight MOSFETs, using 100 pulses with an energy that's 95 percent of that of the destruction limit.

ABB uses its avalanche ruggedness test to assess SiC MOSFETs from six different suppliers. "Pre- and post-stress curves did not show sign of ageing electrically," remarked Mengotti. "The avalanche ruggedness of state-of-the-art silicon carbide MOSFETs is sufficient to allow unclamped switching of inductive loads."

Another test at ABB, helpful for determining how SiC power devices behave during start-up and shut-down procedures in grid-connected solar and wind farms, is a study of the repetitive surge current.

"During the test we stress the silicon carbide diode or the body diode of the MOSFET, which is supposed to be a weak part of the device," said Mengotti.

The set-up involves two half-bridge 'legs' (see Figure 1). One generates rectangular high-current pulses with a 10 μs width at a frequency of 10 Hz. The other leg delivers a blocking voltage that's 80 percent of the nominal value between the surge pulses.

Using this approach, engineers at ABB evaluate devices by first increasing the surge current pulses, an approach that tests five samples to destruction. Then ten samples are aged with 1,000 pulses, using a current that's 90 percent of the value that led to device destruction. After that characterisation of the devices is undertaken. "No electrical aging sign has been observed," revealed Mengotti, who added that all of the SiC devices that have been tested show a very good level of reliability, in terms of repetitive surge current operation.

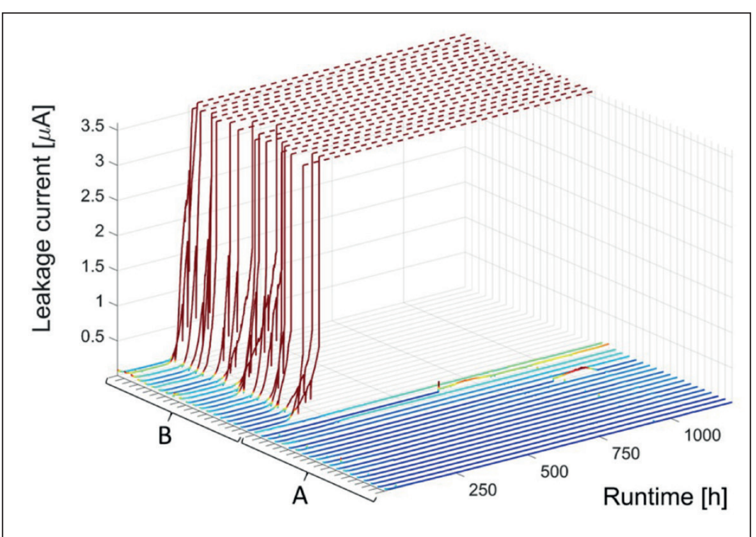
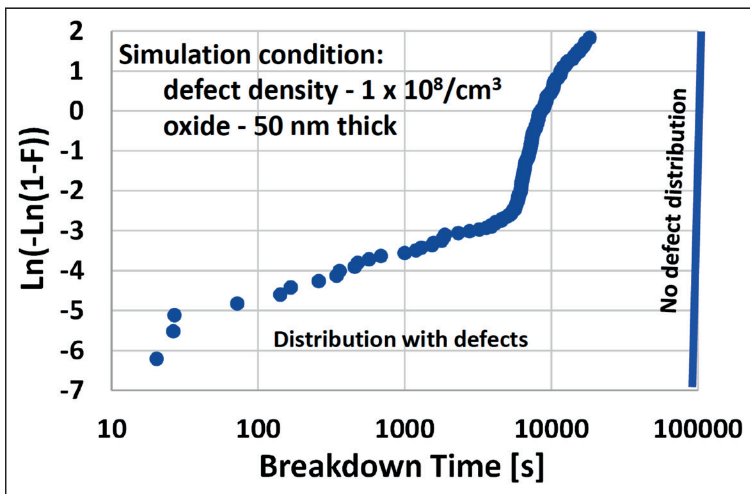


Figure 2. The H3TRB-HVDC test carried out at ABB runs for 1200 hours and involves a temperature of 85 °C, a relative humidity of 85 percent, and a drain-source voltage of 80 percent of the maximum value. The leakage current recorded throughout this test reveals substantial differences between suppliers.



➤ Figure 3. Simulations by NIST catering for variations to the energy of the defect, the width of the energy distribution, and the density of the defect, can model the extrinsic tail of failures associated with the lucky defect.

Also included in the testing suite at ABB is passive 'dV/dt' switching – this is also known as the dynamic reverse-bias test. For this evaluation, 20 devices are tested in parallel for 1000 hours, using a frequency of 60 kHz, and a dV/dt of 100 V/ns.

Using this test to monitor the drain source leakage indicated no sign of device aging. Only the very first generations of diodes showed an abrupt failure, due to an issue associated with edge termination.

"Since no failures were observed in devices from generation two onwards, and no ageing signs were seen, we currently regard this test as unnecessary," remarked Mengotti.

There have always been concerns associated with the quality of the gate oxide in SiC MOSFETs. There are imperfections at the interface of SiO_2 and SiC, and the dielectric oxide is relatively thin. To evaluate the quality of this oxide, the team at ABB elevates the temperature of the SiC MOSFETs to 175 °C, steps up the voltage every 24 hours and monitors the threshold voltage and the gate leakage current.

Using this approach, Mengotti and co-workers have aged 30 planar and 30 trench MOSFETs simultaneously. "The trench [devices] failed at a latter voltage value, indicating higher robustness than the planar. But the planar presented a lower standard deviation, indicating a more mature technology," revealed Mengotti. Another plus for the planar device over its trench cousin is a lower failure rate at the use condition, in terms of gate voltage.

The representative from ABB also discussed a number of other reliability tests for chips. They involved subjecting them to: a high reverse bias, which indicated that reliability is beyond expectation; transfer curves, to study threshold voltage hysteresis; transient measurements of drain current, which revealed that SiC MOSFETs behave differently to their silicon counterparts, but there is no cause for concern; and a test combining voltage and humidity, known as H3TRB-HVDC (see Figure 2 for details).

As well as all these chip-level tests, ABB carries out others at the package level, including power cycling, a test widely used for silicon MOSFETs. This examination involves looking at temperature differences after devices had undergone current cycling that increased their temperature to 80 °C. This test uncovered a difference between packaged devices that had wires soldered and sintered to the baseplate of a SiC MOSFET. "The failure for the solder is reached at around 50,000 cycles, with a smooth increase in the 'delta-T' junction that is proven to be a solder die attach failure mechanism, while for the same temperature condition, the number of cycles has improved to around 90,000 for the sintered junction," remarked Mengotti. In the latter case, failure is due to a wire bond lift-off.

The lucky defect model

A presentation by Kin Cheung, a Project Leader at NIST, provided a more detailed discussion relating to concerns associated with the gate oxide of SiC MOSFETs.

"A few years ago, I heard from a number of silicon carbide companies that there is a persistent, extrinsic tail in the breakdown distribution," remarked Cheung, who explained that this small proportion of problematic devices remained after exhaustive efforts to clean the wafer.

He said that at this time, this was considered a specific SiC problem, because a thermal oxide grown on SiC has more defects than a thermal oxide grown on silicon. When SiC is oxidised, as well as the addition of SiO_2, CO_2 is also added – it cannot easily escape the oxide layer, and may lead to trapped carbon.

One may expect that this extrinsic breakdown problem is unique to SiC. But that's not the case. Cheung pointed out that it has also been reported in silicon, back in 2007, for an oxide thickness of 55 nm.

Historically, there has been just one model for extrinsic failure, based on local thinning. It's been argued that local thinning, caused by particulates and contamination, leads to a lower growth rate that is to blame for a higher electric field in that region and ultimately an earlier device breakdown. But if that were the cause, there's no explanation for extrinsic failure in cleaned wafers.

A model that can do just this is the 'lucky' defect model, which Cheung championed. He argued that while debate continues over the cause of breakdown in the oxide of SiC devices, there is consensus that this failure mechanism is related to current flow across the dielectric, with higher currents leading to a shorter lifetime.

As well as local thinning, trap-assisted tunnelling can increase the current, remarked Cheung: "If you have defects at the right energy and the right spatial

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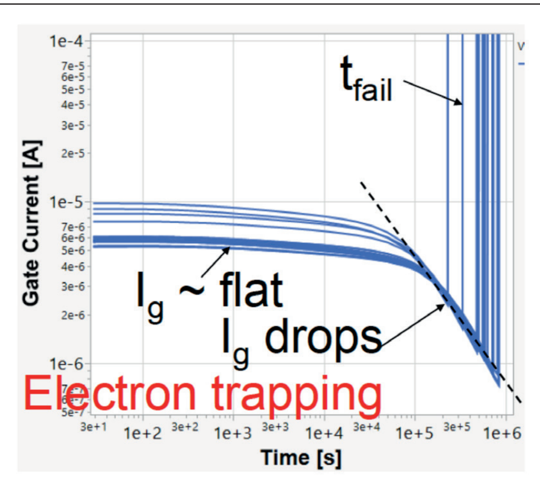

Figure 4. Investigations by onsemi reveal that gate currents of a SiC MOSFET show a similar trend, for a range of voltages and stress times. The gate current is initially flat, before it drops and then rapidly climbs, due to failure. A 'use' time, referred to as t_0, can be defined from the intercept of two lines: one for the gradient of the flat part of the curve, and a second from when it is dropping.

location, this can greatly enhance the tunnelling probability through the trap-assisted tunnelling mechanism." When this happens, there's an increase in the local current, leading to a shortening of device lifetime.

Cheung said that there is a sweet spot at which the effect is strongest. "The effect decays away rapidly as you move away from the sweet spot. That is the reason why it's called a lucky defect model."

It's important to note that with the lucky defect model, even if the oxide is grown on a perfectly clean wafer, defects will still be present. Simulations confirmed this, modelling a 50 nm-thick oxide with a defect density of 1×10^8 cm^{-3} (see Figure 3). To produce this plot, Cheung and co-workers considered variations to the defect's energy, its density, and the width of its energy distribution.

"The good news is that the lucky defect model gives you another way to further improve the extrinsic failure distribution, which is to improve the growth process," remarked Cheung. "Some companies have reported that improving the growth process did help to reduce the extrinsic failure, although exactly what they've done is proprietary information."

The lucky defects have implications for common tests that are applied to SiC MOSFETs, such as those involving the ramping of voltage (V-ramp) and high-field screening.

Cheung explained that producing SiC MOSFETs that are completely free of extrinsic failures is both hard to realise and difficult to prove. When efforts are directed at improving the growth process, a technique is needed to determine whether changes are beneficial. The standard method for assessing the gate oxide – the time-dependent dielectric breakdown method – is far from ideal for this particular task. One major drawback is that this technique requires the measurements of many thousands of devices, because only a small proportion exhibit concerning characteristics.

"Some vendors prefer a much faster alternative, which is the V-ramp test. With that you improve your growth process," explained Cheung. However, he added that to ensure product reliability in the field, it is very common for chipmakers to also use high-field screening before they ship their products.

But do these strategies actually work? "If extrinsic breakdown is due to local thinning, it likely does – at least, there is no strong evidence to say it wouldn't work," said Cheung. However, if extrinsic breakdown is due to lucky defects, it doesn't."

Determining the safe operating area

Peter Moens from onsemi also discussed concerns related to the gate dielectric in SiC MOSFETs. He pointed out that during gate stress, substantial charge trapping occurs in the dielectric. "This results in parametric shifts, limiting the use time of the device." These shifts could cause device characteristics to stray outside the values given in the accompanying data sheets. To avoid that from happening, Moens championed the introduction of a 'use time', which he agued is preferential to a 'lifetime'.

To promote this concept, Moens presented an internal study, considering 1.2 kV *n*-type SiC MOSFETs with a 30 A on current, an on-resistance of 20 mΩ and an oxide thickness of around 40 nm. Measurements were made at both the wafer level, and on chips housed in a TO-247 package. "Typically, when people look at lifetime, they look

> The good news is that the lucky defect model gives you another way to further improve the extrinsic failure distribution, which is to improve the growth process," remarked Kin Cheung from NIST. "Some companies have reported that improving the growth process did help to reduce the extrinsic failure, although exactly what they've done is proprietary information

at time to fail," remarked Moens. "But it's more instructive to look at the complete gate current versus time characteristics."

Plots of this for a device temperature of 175 °C show that initially the gate current is almost flat, before it drops significantly due to electron trapping, and then hikes when the device fails (see Figure 4). This trend is seen for different gate voltages and for stress times of up to 7 months, with plots revealing what Moens refers to as an "envelope curve" that is independent of both gate voltage and temperature. "And strangely enough, this same envelope curve is also observed on silicon technologies," added Moens, who said that this finding shows that device behaviour must be related to the characteristics of SiO_2.

Based on the plots, Meons suggested that rather than giving a lifetime for SiC MOSFETs, it is more insightful to give a use time, defining this as the intercept of the flat gate-current curve with that of the envelope curve. The use lifetime, given the moniker t_0, can also define the safe operating area – this corresponds to a timeframe when the on-resistance shifts by only around 10 percent and the shift in threshold voltage is below 1.2 V. In comparison, between t_0 and device failure, the on-resistance can change by more than 100 percent. Meons and co-workers have also considered SiC MOSFET behaviour at 0 °C, a temperature where hole trapping occurs. Due to this, during gate stress an there's initial increase in the gate current due to hole trapping, followed by a fall due to electron trapping; and over that timeframe there is also a decrease and a subsequent recovery in the threshold voltage, driven by these changes.

Further investigations, considering different stress voltages, revealed that hole trapping only takes place at gate fields in excess of 8 MV cm^{-1}. The team from onsemi also determined that there is no hole de-trapping at 0 °C, and there is some electron de-trapping at 175 °C.

Drawing these findings together, Moens concluded that for high gate voltages, corresponding to a gate field of more than 8 MV cm^{-1}, changes in threshold voltage determine the safe-operating area. But at the 'use' gate voltage, which is set by electron trapping, the change in threshold voltage is less than 1.2 V over 20 years, and t_0 should be used to define the safe operating area.

This insight into how to best to describe the working life of the SiC MOSFET, along with the findings provided by NIST and ABB, show that there's still a long way to go to refine the way we characterise and assess SiC devices. Progress is highly valued, as it will help to accelerate the shift from SiC to silicon power devices, by equipping engineers with the confidence that they understand the superior alternative, and know what to expect from it for many years.

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Championing a true heavyweight: Unleashing the promise of Ga_2O_3

Blessed with an incredibly wide bandgap, shallow donors and the capability of bulk growth from the melt, Ga_2O_3 is making a compelling case as the most promising material ever for power devices

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

Aside from a record number of delegates and a packed exhibition hall, those attending this year's CS International will remember this meeting for the phenomenal level of interest in wide bandgap power electronics. Excitement in this sector is incredibly high, because sales of SiC and GaN devices and modules are set to rocket throughout the remainder of this decade, climbing from an annual revenue that now totals below $2 billion to around $18 billion by 2030. That's great news not only for chipmakers, but also those making related materials, metrology tools and device design software.

A healthy uptake of these two new classes of power electronics with benefit humanity. There will be improvements in the efficiency with which electricity is converted between its AC and DC forms, and is stepped up and down. This leads to a reduction in the carbon footprint of numerous electrical systems. What's more, electric vehicles will travel further on a single charge, helping to sooth concerns related to range anxiety, as well as making a more compelling case for switching away from the combustion engine.

But does the revolution in power electronics end with SiC and GaN? Or is there more to come?

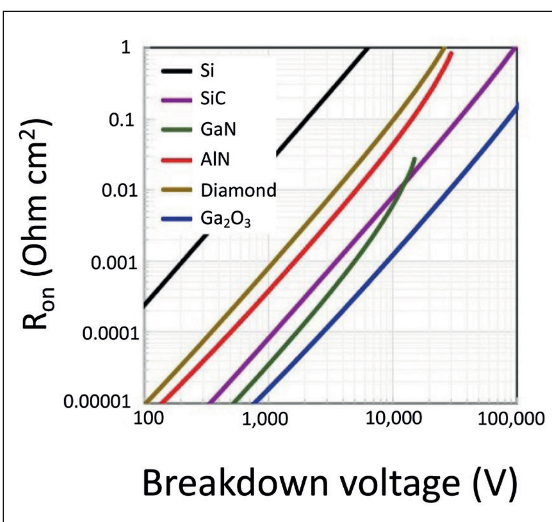
It's the latter, argued three presenters at CS International: Martin Kuball (pictured above), leader of the Centre for Device Thermography and Reliability at Bristol University; Akito Kuramata, CEO of gallium oxide substrate maker Novel Crystal Technology (NCT); and Heather Splawn, CEO of

➤ Martin Kuball, chair of the Royal Academy of Engineering in Emerging Technologies and a physics professor at the University of Bristol, UK, is expanding his research into gallium oxide, thanks to the introduction of an MOCVD growth tool in his labs.

HVPE specialist Kyma Technologies. All made the case that compared with the middleweight duo of SiC and GaN, gallium oxide is a heavyweight with the capability to handle incredibly high voltages and provide switching at even higher efficiencies. These attributes make this oxide a very promising candidate for the ultra-high-voltage market, where it could be deployed for supporting the grid, handling the power produced by wind turbines and finding application in electric trains.

In terms of its physical prowess, Ga_2O_3 is best known for its very wide bandgap of 4.9 eV and a breakdown field that can reach as high as 8 MV cm^{-1}. But how does it perform when benchmarked against the common yardstick for gauging the potential of power devices, Baliga's figure of merit? Well, that depends on what's considered. Initially, while it would appear that oxide is ahead of SiC and GaN by a considerable margin, it lags behind two other heavyweights, diamond and AlN. However, when one considers the depth of the dopants, a crucial factor in determining the capability of power devices, the β form of Ga_2O_3 comes out on top, thanks to relatively shallow dopants (see Figure 1).

Another major asset of Ga_2O_3 is the relative ease of crystal growth. Like silicon, GaAs and InP, it can be grown from the melt, ensuring relatively easy production of substrates with low dislocation densities. That's not the case for SiC, which tends to be produced by vapour phase transport; or GaN, which is yet to have a bulk growth technique suitable for producing native power electronic devices in volume.



➤ Figure 1. Once the level of activity of dopants is considered, Ga_2O_3 emerges as the most promising of the ultra-wide bandgap semiconductors, based on Baliga's figure of merit. This graph is taken from Y. Zhang et al. Semicond. Sci. Technol. **35** 125018 (2020).

Obstacles to overcome

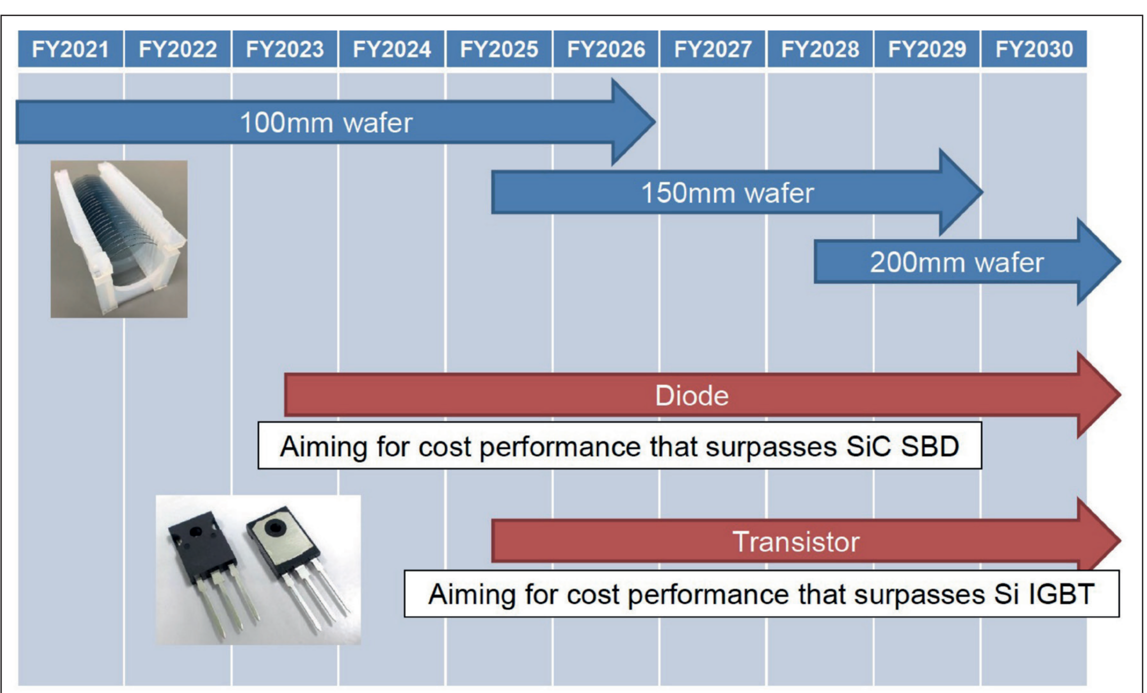
Thanks to all these merits, devices made from Ga_2O_3 are already delivering impressive results. "The performance is already exceeding silicon carbide," remarked Kuball during his presentation to delegates at CS International 2023. However, that does not imply that commercial success is assured, partly due to weaknesses associated with these devices.

➤ Akito Kuramata is CEO of Novel Crystal Technology, a provider of Ga_2O_3 substrates and epiwafers. The company plans to expand into the production of diodes and transistors based on this oxide.

Kuball did not brush aside these concerns, but discussed them head on. One weakness is a high density of defects in the material, with deep-level transient spectroscopy uncovering many different trap states in β-Ga_2O_3. More work is needed, as it is still largely unknown what the killer defects in this oxide might be.

Another concern is the low thermal conductivity of Ga_2O_3, which has led many to claim that this oxide will never be a viable material for power devices, due to overheating of the chip. But this issue can be addressed with engineering, with Kuball suggesting that the introduction of diamond beside the active region could suck heat away. It's an approach his team have already used to improve the thermal management of GaN devices.

The addition of diamond is actually capable of offering much more than simply superior heat extraction. Work by Kuball's team has shown that superjunction Schottky barrier diodes formed by filling trenches in *n*-type Ga_2O_3 with *p*-type diamond enables electrical control of the device. This is encouraging, because the lack of *p*-type doping of



➤ Figure 2. NCT intends to increase the diameter of the substrates it produces, as well as branching out into the production of Ga_2O_3 diodes and transistors. semiconductors, based on Baliga's figure of merit. This graph is taken from Y. Zhang et al. Semicond. Sci. Technol. 35 125018 (2020).

Ga_2O_3 is a major concern – and integrating other *p*-type semiconductors is a promising solution.

When any device is in its infancy, there will always be concerns over its reliability. Kuball and his co-workers have been investigating Ga_2O_3 trench FETs provided by the University of Cornell, with experiments finding failure at the dielectric, Al_2O_3. Efforts will now need to be directed at improving the interface between Ga_2O_3 and Al_2O_3.

Trench Schottky barrier diodes have also been produced by the Bristol team. Benchmarking of these devices, which do not have field plates, indicates a performance comparable to that of the other leading groups in this field.

➤ Figure 3. For high-speed growth of Ga_2O_3 material with a large diameter, edge-defined, film-fed growth delivers unparalleled results.

In May 2022 Kuball's team commissioned the first commercial Ga_2O_3 MOCVD reactor in Europe, an Agnitron Agilis tool. Since then they have been enjoying the opportunity to grow their own material, producing both Ga_2O_3 and $Al_x(Ga_2O_3)_{1-x}$ epilayers for a variety of structures, including vertical devices.

Kuball explained that to improve the thermal performance of devices, they have investigated two-step growth on diamond. Transmission electron microscopy and scanning electron microscopy images of a 245 nm-thick layer of β-Ga_2O_3 have revealed a completely coalesced surface, and different competing crystalline orientations. The physical characteristics of this film are not that different from β-Ga_2O_3 grown on sapphire, leading Kuball to describe results so far as very promising.

Options for boule growth

More insight into the growth of Ga_2O_3 boules came in the presentation from NCT's Kuramata, who discussed both of the growth technologies that his company has employed to produce commercial material: edge-defined, film-fed growth; and vertical Bridgeman growth.

While this Japanese firm, based in Sayama, is better known for its production of substrates and epiwafers, it also has plans to produce chips and packaged devices. Kuramata presented a roadmap for the company, which included the introduction of 150 mm and 200 mm wafers within the next five years, and the launch of diodes and transistors in 2023 and 2025, respectively (see Figure 2 for details). The company's diodes are intended to offer a cost performance exceeding that of the SiC Schottky barrier diode, while judged by the same yardstick, transistors are expected to have the upper hand over the silicon IGBT.

For the production of larger material, edge-defined, film-fed growth leads the way, with NCT already having reported the development of material with dimensions of 6 inches. "It's the only way to produce large *n*-type substrates at present," remarked Kuramata.

Another merit of this film-fed growth approach is that it's the fastest of all the Ga_2O_3 growth technologies – with a growth rate of 15 mm/hour, it's three times as fast as a float-zone process, and considerable faster than growth by the Czochralski and vertical Bridgeman techniques, which are capable of only 2 mm/hour and 1 mm/hour, respectively.

With edge-defined, film-fed growth, engineers draw molten gallium oxide through a slit by capillary action, leading to growth on seed material (see Figure 3). This yields crystalline material with a plate-like geometry that has a defect density of typically around 10^3 cm^{-2}.

As the Ga_2O_3 industry is still in its infancy, it's not surprising that today there are no orders for 6-inch material. However, Kuramata is confident that once such orders arrive, NCT will quickly establish production of material of this size.

The Japanese outfit is also developing Ga_2O_3 boules produced by the vertical Bridgeman process, as this yields material with a very high quality. Growth involves a crucible made from a platinum-rhodium alloy and a (010) Ga_2O_3 seed crystal. By carefully controlling the motion of the crucible through the thermal gradient produced in the furnace, molten Ga_2O_3 is cooled to yield a crystalline boule. With this approach, NCT has produced 2-inch (010) substrates – claimed to be the largest size for (010) Ga_2O_3 substrates ever reported.

For the growth of epilayers, NCT employs HVPE, a technology transferred from Tokyo University of Agriculture. Working in partnership with Saga University, NCT has produced Schottky barrier diodes on a 100 mm β-Ga_2O_3 epiwafer, with chip sizes of up to 10 mm by 10 mm. For a 10 μm-thick layer, film thickness uniformity is $\pm$ 5 percent; and donors, at a concentration of 1×10^{16} cm^{-3}, have a variation of $\pm$ 7 percent.

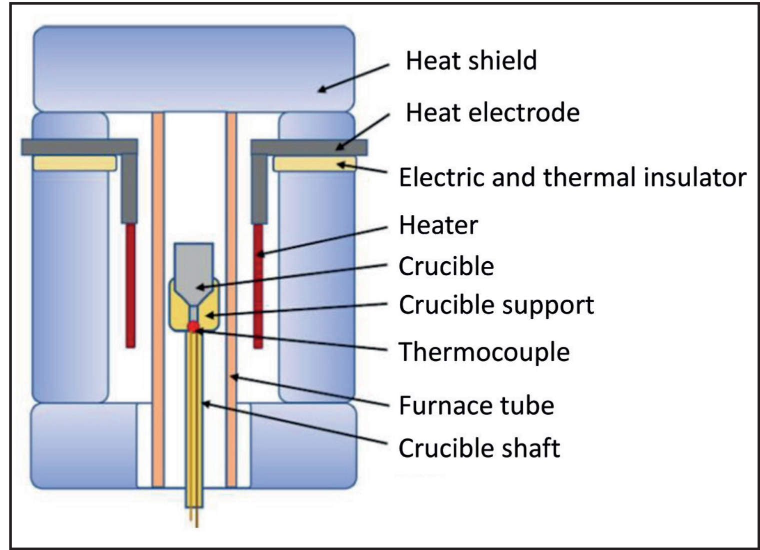
Diodes from this wafer with sides of 10 mm by 10 mm have a yield as high as 51 percent. Based on this figure, the killer defect density for the epiwafers is about 0.7 cm^{-2}.

Championing HVPE

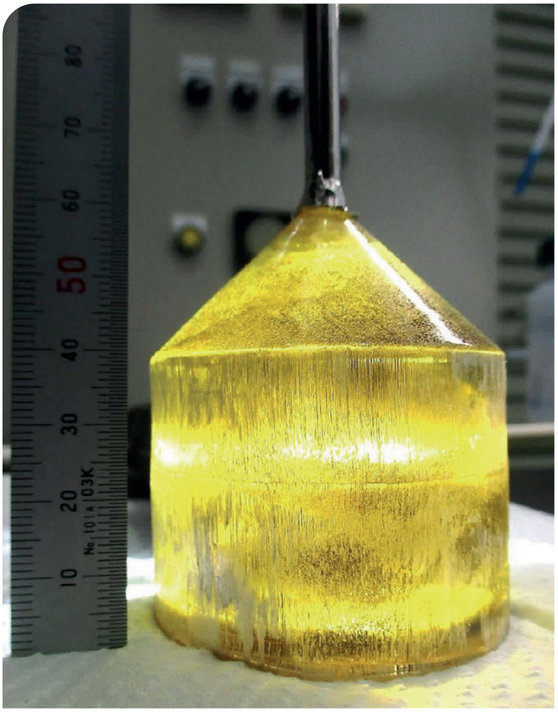
Another advocate of HVPE for gallium oxide high-voltage power electronics is the leader of Kyma Technology, Heather Splawn. She argued at this year's CS International that this form of epitaxy produces material with a low cost and high performance, using high growth rates that are ideal for device manufacture. Splawn also pointed out that HVPE is inherently cleaner than MOCVD, due to chemically pure precursors and the absence of metal-organics, which contain carbon. Thanks to these assets, HVPE is capable of high-purity growth.

Kyma has launched to market a tool called Katharo, designed for the growth of Ga_2O_3 devices for high-power switching. This reactor is capable of accommodating wafers up to 200 mm in diameter.

While growth on such large diameters is still some way off, the company has realised encouraging results on smaller substrates. In HVPE reactors with 100 mm capability, excellent doping control is realised at epilayer thicknesses that can be more than 20 μm, according to Splawn. Her team has also



➤ Figure 4. NCT uses the vertical Bridgeman process to produce Ga2O3 crystals with a very high quality.



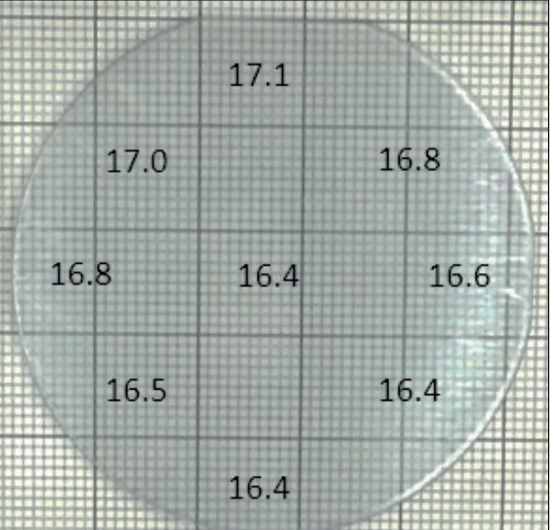
➤ Using the vertical Bridgeman technique, NCT has produced 2-inch (010) substrates.

➤ Kyma's CEO, Heather Splawn, advocates HVPE for HVPE – that's hydride vapour phase epitaxy for high-voltage power electronics

deposited Ga_2O_3 epilayers with uniform doping and thickness on 50 mm wafers, with X-ray diffraction measurements indicating a very high level of crystal quality – linewidths are just 25-30 arcsec.

Material produced by Kyma has been used to produce some very encouraging device results. Breakdown fields in these devices are as high as around 5.5 MV cm^{-1}, and Baliga's figure-of-merit is in excess of 1 GW cm^{-2}, a value very close to the theoretical limit for SiC.

Such results highlight the great promise of Ga_2O_3. With SiC and GaN seemingly assured of a bright future, it will be some time before this oxide makes a really big impact – both at CS International and within the power industry – but there's no doubting that the omens are good.



➤ Using HVPE, Kyma has grown a 16.7 µm-thick layer of Ga_2O_3 on a 2-inch native substrate that has a thickness variation of ± 3 percent. Values for the difference between the concentration of donors and acceptors within this epilayer range from 2.7×10^{16} cm^{-3} to 5.8×10^{16} cm^{-3}.

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For more information contact:

Jackie Cannon **T:** 01923 690205 **E:** jackie@angelwebinar.co.uk **W:** www.angelwebinar.co.uk
Angel Business Communications Ltd, 6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry, CV5 6SP. UK
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