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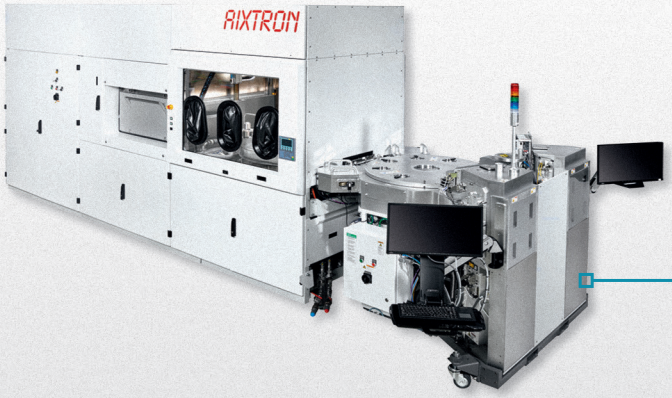

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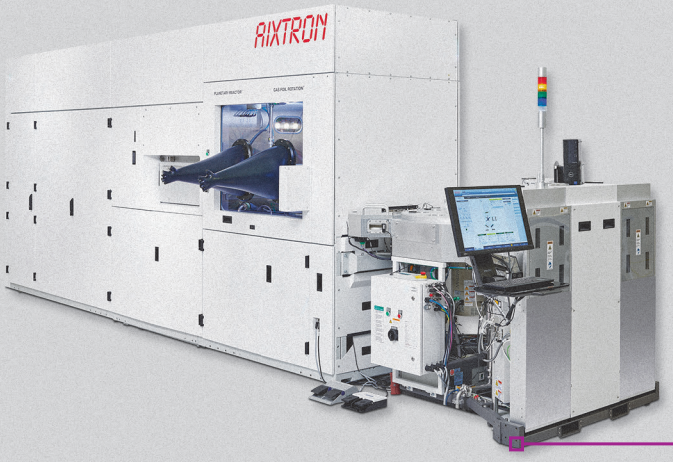

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VIEWPOINT

BY PHIL ALSOP EDITOR

Data centres – delivering a digital and sustainable future?

THE RECENT REPORT published by the Compound Semiconductor Applications (CSA) Catapult suggests that the UK can be a leader in power electronics for data centres and the critical role of compound semiconductors in managing data centre energy consumption. The report highlights the potential efficiencies which could be obtained by integrating innovative compound semiconductor devices into power distribution networks, notably: power supply units, uninterruptible power supplies and solid-state transformers.

One imagines that other countries and regions have similar thoughts/ambitions, and not just when it comes to the power distribution network. There's already much work being done across the world when it comes to addressing the power efficiency of the IT hardware housed in data centres – there's a whole host of start-ups and more seasoned semiconductor and IT organisations already working on developing AI chips, silicon photonics and quantum computing solutions which consume significantly less power than more traditional compute, networking and storage architectures, for example.

What is less clear – and I may well have simply missed the relevant report(s) – is how all of the data centre power efficiency work (both outside and inside the building) will have an impact on the many predictions which suggest that data centre power consumption is set to at least double over the next few years. In other words, is this predicted, huge data centre power consumption increase happening despite the best work of the semiconductor and IT industries to improve energy efficiency across the board, or is there a very real chance to slow down this 'power-hungry' future? And maybe there are some more DeepSeek moments out there, which could further disrupt the anticipated future power demand for data centres and their resident IT hardware solutions? A recent conversation with a data centre consultant revealed that many organisations, from the hyperscalers down, are slightly nervous as to how to truly monetise the AI opportunity. In other words, there's maybe something of a pause as the hype and the reality are better understood. Add in the longer term prospect of quantum computing and the data centre/IT landscape is far from easy to predict when it comes to (rising) power consumption levels.

The good news is that, despite any amount of uncertainty, the ongoing focus on data centre power/energy efficiency is set to continue for two main reasons.

Firstly, the data centre industry seems determined to improve its sustainability credentials over the coming years. Indeed, much good work has already been done in this area. The prospect of significant, semiconductor-inspired power savings in the distribution networks that power the IT loads hosted in data centres is highly welcome for an industry which, at times, risks falling foul of public opinion when it comes to the environment. (Never mind that the environmentalists see no contradiction in accessing and exploiting their digital, data centre-driven devices to spread the sustainability message...). As are the similar potential power savings from new generations of servers/computers, optical networks and the like.

Secondly, energy efficiency makes great business sense. If you can achieve more with the same, or even less, power, then why wouldn't you?

Whether or not data centres ever will be able to address the apparently contradictory demands of a truly digital and sustainable world equally well – we can leave that question for another day. For now, at least, let's welcome the semiconductor-led innovations which are already delivering significant power savings across the data centre industry ecosystem and look forward to the promise of much more innovation to come.

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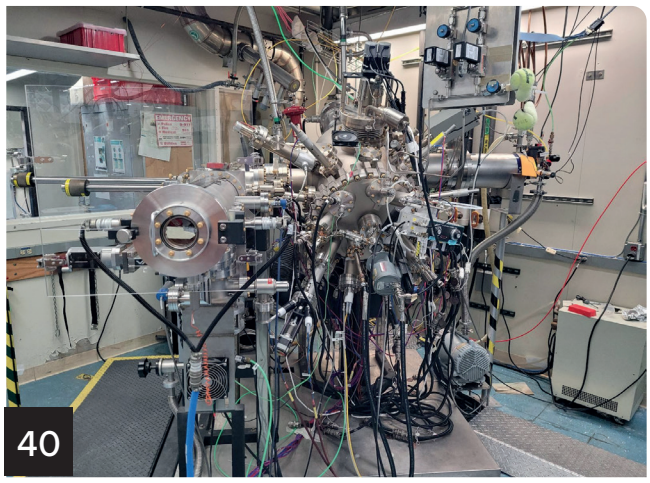

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Angel BUSINESS COMMUNICATIONS

UK could lead the world in data centre power technology

Report by CSA Catapult highlights the UK's strengths in compound semiconductors for managing data centre energy consumption

A NEW REPORT published today by the Compound Semiconductor Applications (CSA) Catapult has highlighted how the UK can be a leader in power electronics for data centres and the critical role of compound semiconductors in managing data centre energy consumption.

The report 'Advancing Data Centres: Key Trends and the Rise of Wide Bandgap Solutions' explores the exponential rise in the number of data centres worldwide to meet the growing demand of AI applications.

Energy efficiency is paramount for data centre providers, with projections showing they could account for up to 10% of global electricity by 2030.

The report highlights the possible efficiencies that can be achieved by integrating novel compound semiconductor devices into power distribution networks.

In particular, the report highlights three areas in which compound semiconductors can play a significant role: power supply units (PSUs),

uninterruptible power supplies (UPSs) and solid-state transformers (SSTs).

With over 500 data centres — the third highest amount in the world — and robust engineering and compound semiconductor expertise, the UK is well-positioned to lead in advancing wide bandgap technologies for data centres. CSA Catapult plays a pivotal role in this innovation landscape, providing world-class capabilities in advanced power electronics design, simulation, optimisation and rapid prototyping.

Nick Singh, CTO at CSA Catapult said: "This report is a timely reminder that as the UK leverages AI in unlocking growth, and consumer data demands continue to rise, compound semiconductors have a vital role to play in managing our future energy needs."

Onsemi tries to acquire Allegro MicroSystems

Chip company Onsemi, valued at around $19.8 billion, has announced its intention to acquire Allegro MicroSystems for $35.10 per share in cash, with an implied enterprise value of $6.9 billion.

Over the past six months, Onsemi has made various attempts to discuss a potential transaction with Allegro. This most recent proposal was submitted on February 12, 2025, and represents an increase over an initial $34.50 per share proposal submitted on September 2, 2024.

"We believe the combination of Onsemi and Allegro would bring two highly complementary businesses together, benefitting our respective customers and delivering immediate value to Allegro shareholders," said Hassane El-Khoury, president and CEO of Onsemi.

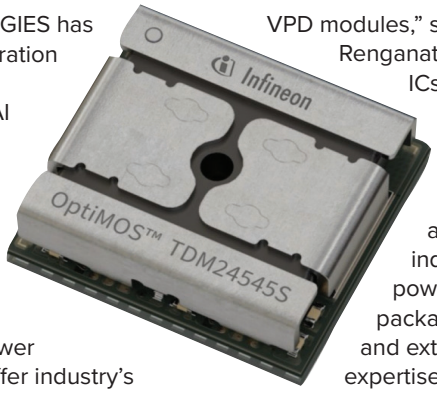
"The Allegro team has built an impressive leadership position in magnetic sensing and power ICs for the automotive and industrial end-markets. Together, Allegro's unique product portfolio and Onsemi's differentiated intelligent power and sensing technologies would create a diversified leader in automotive, industrial and AI data centre applications."

El-Khoury continued, "While we would have preferred to reach an agreement with Allegro privately, the decision to make our proposal public reflects our conviction in the merits of a combined company, which we believe is in the best interests of Allegro and Onsemi shareholders. We urge the Allegro board and management team to engage in good faith discussions with Onsemi's management team regarding the proposed transaction, which maximises value for Allegro shareholders."

Infineon unveils next-gen vertical power modules

OptiMOS TDM2454xx quad-phase power modules offer industry's best current density of 2A per mm^2

INFINEON TECHNOLOGIES has launched its next generation of high-density power modules for enabling AI and high-performance computing.



The new OptiMOS TDM2454xx quad-phase power modules are said to enable true vertical power delivery (VPD) and ri offer industry's best current density of 2 Ampere per mm^2.

In traditional horizontal power delivery systems, power needs to travel across the surface of the semiconductor wafer, which can result in higher resistance and significant power loss. Vertical power delivery minimises the distance that power needs to travel, thereby reducing resistive losses enabling increased system performance.

Data centres are currently responsible for two percent of global energy consumption according to the IEA. Fueled by AI, the power demands within data centres are expected to grow by 165 percent between 2023 and 2030. Continually improving the efficiency and power densities of power conversion from grid-to-core is vital to enable further advancements in compute performance while reducing TCO.

"We are proud to expand our high-performance AI data centre solutions with the OptiMOS TDM2454xx VPD modules," said Rakesh Renganathan, VP power ICs at Infineon Technologies. "We take a three-dimensional design approach and leverage our industry-leading power devices, packaging technologies and extensive systems expertise to provide high-performance and energy-efficient computing solutions as part of our mission to drive digitalisation and decarbonisation."

The OptiMOS TDM2454xx modules are a fusion of Infineon's robust OptiMOS 6 trench technology, chip-embedded package for superior electrical and thermal efficiencies, and innovative low-profile magnetic design that continue to push the envelope for performance and quality of VPD systems. Additionally, the OptiMOS TDM2454xx has a footprint that is designed to enable module tiling and improving current flow that enhance electrical, thermal and mechanical performance.

The OptiMOS TDM2454xx modules support up to 280A across four phases with an integrated embedded capacitor layer within a small 10x9mm^2 form factor. Combined with Infineon's XDP controllers, they offer a robust power solution with improved system power density.

Data centres are currently responsible for two percent of global energy consumption according to the IEA. Fueled by AI, the power demands within data centres are expected to grow by 165 percent between 2023 and 2030

BelGaN's production site has three bidders

THREE CANDIDATES have come forward to purchase the BelGaN chip manufacturing site in Oudenaarde, Belgium. Two of the bidders are from Asia and one is from Europe, according to an article in The Brussels Times online newspaper.

The property spans over four hectares, including two clean rooms, and is located along the N60 in Oudenaarde, East Flanders.

BelGaN planned to become a leading 6 inch and 8 inch GaN foundry, developing GaN technologies and manufacturing GaN products for the high demands of the automotive market, amongst others. But it closed last year after the company went bankrupt, resulting in 440 job losses.

More than 80 percent of the high-tech equipment has already been sold, but bidding for the large company site was open until Wednesday 12th March at 7 pm.

"They are talking about increasing the workforce to 250 employees and more within three years," curator Ali Heerman told the newspaper.

The bids meet the set conditions, including a minimum price and specific payment guarantees. The site's value was estimated at around €20 million. However, Heerman did not confirm any exact figures. "The court still needs to authorise us to proceed with a private sale, but we are confident a decision will be made soon," he is quoted as saying.

The sale is expected to be concluded in April 2025.

Magnachip launches two new Gen6 650V IGBTs three bidders

Optimised conduction and switching losses enhance system efficiency

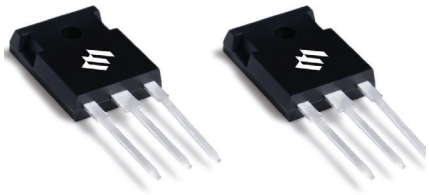
MAGNACHIP SEMICONDUCTOR has announced the launch of two new 6th-generation (Gen6) 650V IGBTs, specifically designed for solar inverters.

The newly introduced Gen6 IGBTs, incorporating polyimide insulation layers, are said to demonstrate outstanding performance by passing high-voltage, high-humidity and high-temperature reverse bias (HV-H3TRB) tests. These products offer dependable reliability in industrial equipment operating under extreme conditions, including elevated temperatures and humidity.

Additionally, integrated fast recovery anti-parallel diodes ensure swift removal of residual current, reducing switching losses in applications while supporting an operating temperature range of up to 175°C.

Of the two new products, the MBQ40T65S6FHTH features high conduction loss reduction. Compared to the previous generation, this IGBT decreases conduction loss by approximately 25 percent and boosts system efficiency by about 15 percent in 15kW solar inverters.

The MBQ40T65S6FSTH is engineered to significantly reduce switching loss. It cuts switching loss by 15 percent and conduction loss by approximately 8 percent compared to its predecessor, enhancing system efficiency by about 11 percent in 3kW solar inverters. With these performance upgrades, the new IGBTs are suitable for applications that



demand high reliability and efficiency, such as solar inverters, industrial motor drives, power supply units and uninterruptible power supplies.

“In the second half of this year, we plan to introduce a broader range of Gen6 650V IGBT products with current ratings from 5A to 75A, as part of our strategy to significantly expand our pipeline of new-generation Power products,” said YJ Kim, CEO of Magnachip.

Toshiba 600V MOSFET improves efficiency

TOSHIBA ELECTRONICS EUROPE has launched an N-channel power MOSFET to address the growing demand for improved efficiency in power supply circuits.

The new TK024N60Z1 uses the DTMOSVI 600V series process with a super junction structure to achieve low on-resistance and reduced conduction losses.

Applications include servers in data centres, switched-mode power supplies for industrial equipment, and power conditioners for photovoltaic generators.

The TK024N60Z1 has a drain-source on-resistance RDS(ON) of 0.024Ω (max), which is the lowest in the DTMOSVI 600V series. It also improves power supply efficiency, which reduces heat generation.

Combined with the TO-247 package, which delivers high heat dissipation, the TK024N60Z1 offers good heat management characteristics.Like other MOSFETS in the DTMOSVI 600V series, the TK024N60Z1 benefits from an optimised gate design and process. This reduces the value of drain-source on-resistance per unit area by approximately 13 percent. More importantly, drain-source on-resistance × gate-drain charge is reduced by approximately 52 percent, compared to Toshiba’s conventional generation DTMOSIV-H series products with the same drain-source voltage rating.

This means the DTMOSVI series, including the TK024N60Z1, offers a better trade-off between conduction loss and switching loss, which helps improve the efficiency of switched-mode power supplies.

Toshiba offers tools that support circuit design for switched-mode power supplies. These include the G0 SPICE model, which quickly verifies circuit function, and the highly accurate G2 SPICE models that reproduce transient characteristics.

GaN-IGBT combo targets EV powertrains over 100kW

CGD reveals alternative to SiC that combines smart ICeGaN HEMT ICs and IGBTs in the same module

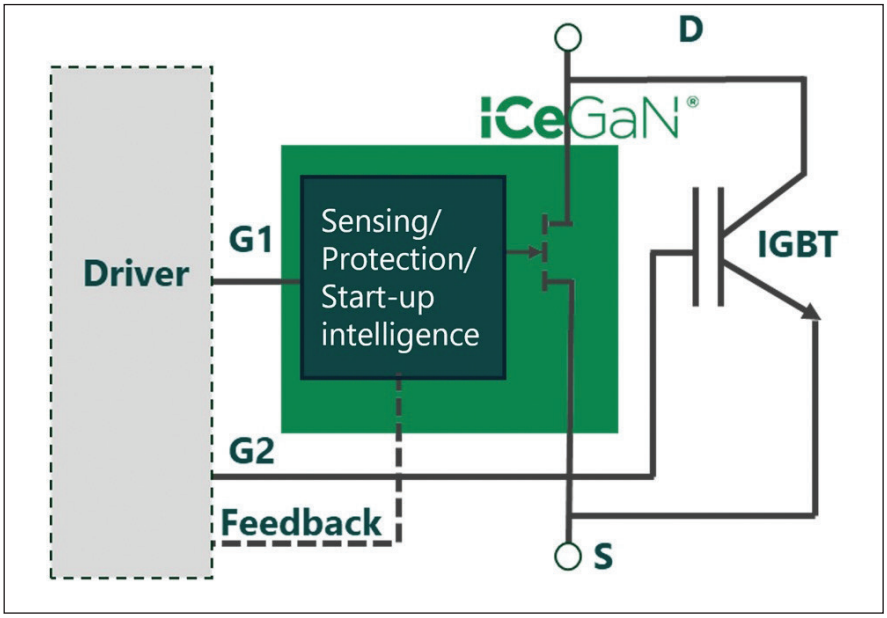
CAMBRIDGE GaN Devices (CGD) has revealed more details about a solution that will enable the company to address EV powertrain applications over 100kW – a market worth over $10B - with its ICeGaN GaN technology.

The combo combines smart ICeGaN HEMT ICs and IGBTs in the same module or IPM, maximising efficiency and offering a cost-effective alternative to expensive SiC solutions.

Giorgia Longobardi, founder and CEO of CGD said: “Today, inverters for EV powertrains either use IGBTs which are low cost but inefficient at light load conditions, or SiC devices which are very efficient but also expensive. Our new Combo ICeGaN solution will revolutionise the EV industry by intelligently combining the benefits of GaN and silicon technologies, keeping cost low and maintaining the highest levels of efficiency which, of course, means faster charging and longer range. We are already working with Tier One automotive EV manufacturers and their supply chain partners to bring this technology advancement to the market.”

The proprietary Combo ICeGaN approach uses the fact that ICeGaN and IGBT devices can be operated in a parallel architecture having similar drive voltage ranges (e.g. 0-20V) and excellent gate robustness. In operation, the ICeGaN switch is very efficient, with low conduction and low switching losses at relatively low currents (light load), while the IGBT is dominant at relatively high currents (towards full load or during surge conditions).

Combo ICeGaN also benefits from the high saturation currents and the avalanche clamping capability of IGBTs and the very efficient switching of ICeGaN.



At higher temperatures, the bipolar component of the IGBT will start to conduct at lower on-state voltages, supplementing the loss of current in the ICeGaN. Conversely, at lower temperatures, ICeGaN will take more current. Sensing and protection functions are intelligently managed to optimally drive the Combo ICeGaN and enhance the Safe Operating Area (SOA) of both ICeGaN and IGBT devices.

The company says that ICeGaN technology allows EV engineers to enjoy GaN’s benefits in DC-to-DC converters, on-board chargers and potentially traction inverters. Combo ICeGaN further extends the benefits of CGD’s GaN technology into the rich 100kW+ traction inverter market.

ICeGaN ICs have been proven to be very robust and IGBTs have a long and proven track record in traction and EV applications. Similar, proprietary parallel combinations of ICeGaN devices with SiC MOSFETs have also been proven by CGD, but Combo ICeGaN – which is now detailed in a published IEDM paper - is a far more economical solution.

CGD expects to have working demos of Combo ICeGaN at the end of this year.

Florin Udrea, founder and CTO of CGD said: “Having worked for three decades in the field of power devices, this is the first time I have encountered such a beautifully complementary technology pairing. ICeGaN is extremely fast and a star performer at light load conditions while the IGBT brings great benefits during full load, surge conditions and at high temperatures. ICeGaN provides on-chip intelligence while the IGBT provides avalanche capability. They both embrace silicon substrates which come with cost, infrastructure and manufacturability advantages.”

CGD will be exhibiting at APEC (Applied Power Electronics Conference and Exposition) at the Georgia World Congress Center in Atlanta, March 16-20, 2025.

$25 billion compound semi market by 2030

Compound semiconductors are “enablers” outpacing the broader chip market, says Yole

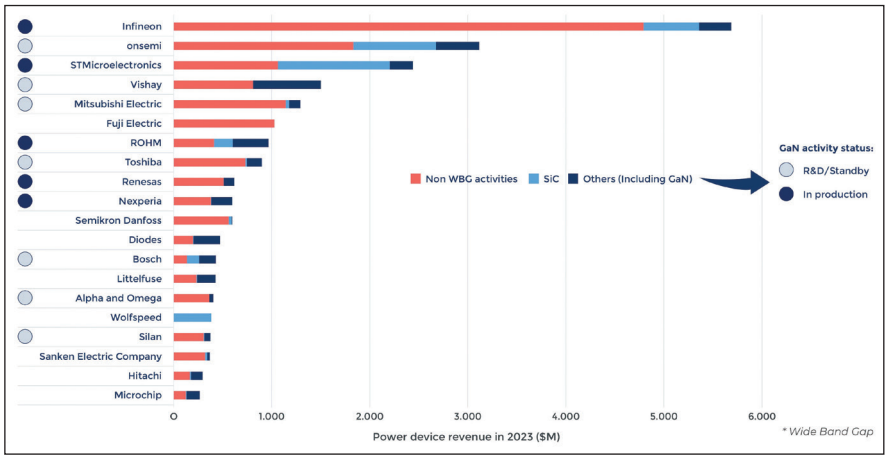
THE compound semiconductor market is set to reach $25 billion by 2030 according to market research firm Yole’s latest report, ‘Status of the Compound Semiconductor Device Industry’.

While being only a small part of the $1 trillion semiconductor device market, compound semiconductors are “enablers”, says Yole, driven by rapid growth in automotive, telecom, and mobile sectors. Ezgi Dogmus, activity manager, compound semiconductors at Yole Group said: “The compound semiconductor device industry is on a rapid growth trajectory between 2024 and 2030, surging at an impressive CAGR of nearly 13 percent—outpacing the broader semiconductor market. This acceleration is fuelled by the booming automotive and mobility sectors, with strong momentum also coming from telecom, infrastructure, and consumer electronics.”

After SiC adoption, is GaN the next to watch?

Over the past decade, a rapid push for power SiC adoption saw Wolfspeed divest its RF and LED businesses to concentrate on SiC. In parallel, STMicroelectronics, Onsemi, and Infineon Technologies expanded their SiC investments, adopting vertically integrated business models to reduce wafer supply dependencies amid geopolitical tensions.

Following the SiC boom, OEMs are showing stronger interest in GaN for power electronics applications. This interest has led to a change in the landscape. The power GaN market is projected to grow beyond $2 billion by 2029, with a strong 5-year CAGR, according to Yole Group’s analysts. As of 2025, Innoscience, Power Integrations, and Navitas lead the power GaN market. In parallel, semiconductor giants Infineon Technologies and Renesas grew by acquiring GaN Systems and Transphorm, respectively.



Poshun Chiu, senior technology and market analyst, compound semiconductors at Yole Group said: “It has also created synergies with GaN for RF applications. Companies like Infineon Technologies and GlobalFoundries, having invested in power GaN-on-Si, are exploring synergies to leverage existing equipment, such as epitaxy, for RF production.”

RF applications : a unique perspective?

RF GaAs was the first compound semiconductor to achieve success in consumer applications, with a well-established ecosystem by 2025. Skyworks leads the market, followed by Qorvo and Murata, securing design wins in consumer end systems. However, geopolitical restrictions are driving Chinese OEMs to develop a local ecosystem. Aymen Ghorbel, technology and market analyst, compound semiconductors at Yole Group said: “RF GaN was initially adopted in defence applications like radar, but over the past decade, it has expanded into telecom infrastructure, meeting 5G base station requirements. Interest in satellite communications and other use cases has also grown.”

The AI boom: driving datacom growth and powering compound semiconductors

Semiconductor lasers drive the photonics compound semiconductor industry with an expected $5 billion market by 2029. These technologies are widely used in communication, sensing, and more. With the rise of AI, the datacom sector has experienced significant growth, driving strong demand for silicon photonics.
At Yole Group, analysts have identified a growing number of collaborations between the InP photonics and silicon industries. Major semiconductor giants like TSMC are entering the photonics business. And step by step, more players, such as GlobalFoundries and Samsung, may follow in the future.

MicroLED display, a fragmented landscape

The microLED display industry is highly fragmented, with no single entity overseeing manufacturing from start to finish. Unlike traditional vertically integrated display production, microLED manufacturing requires distinct expertise. Major display makers like BOE and AUO are securing control over LED suppliers, while startups and equipment makers contribute to major technologies. Geographic alliances, particularly in China and Taiwan, are shaping industry dynamics.

Apple’s withdrawal has slowed funding, leaving most startups struggling and undermining confidence in microLED’s prospects.

Korean team develops method to evaluate SiC chips for space

Method will be applied across aerospace, medical radiation equipment, nuclear power plants, and military/defence electronics

A RESEARCH TEAM at the Korea Electrotechnology Research Institute (KERI) has developed technology to evaluate radiation resistance and reliability of SiC power semiconductor devices in Space.

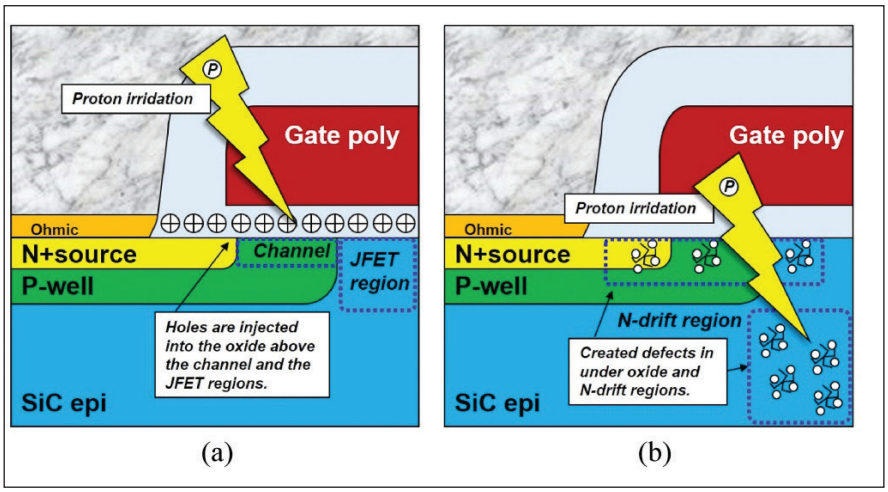
Space radiation is a major cause of degradation in the electrical characteristics of power semiconductors installed in aircraft, exploration vehicles (rovers), and satellites. While radiation effect research is actively conducted in the US and Europe, Korea's efforts have primarily focused on the quantitative analysis of radiation resistance in silicon power semiconductors, with limited research outcomes.

In Korea's first high-energy space environment simulation, KERI's team led by Jae Hwa Seo, created an extreme space radiation experimental environment, with protons making up 80–90 percent of the total composition.

To implement precise radiation exposure conditions, Seo's team used high-energy protons (100 MeV) from the accelerator facility at the Korea Atomic Energy Research Institute in collaboration with a team led by Yoon Young-jun from Andong National University.

Under these conditions, KERI analysed the effects on domestically developed SiC power semiconductors, including voltage changes, increased leakage current due to exposure, and lattice damage. The research 'Degeneration mechanism of 30 MeV and 100 MeV proton irradiation effects on 1.2 kV SiC MOSFETs' was published earlier this month in the journal Radiation Physics and Chemistry.

The results showed that drain currents were reduced at 30 MeV and proton fluences of 1 × 1014 cm^{-2} due to the displacement damage (DD) effect. Meanwhile, at 100 MeV, the protons mainly induced total ionizing dose (TID) effects, characterised by a negatively shifted threshold voltage. The on-state current at a gate voltage of 10 V and a drain voltage of 5 V of the test device with irradiation of 100 MeV and proton fluence of 1 × 1014 cm^{-2} was higher than that of the test device without irradiation because of a reduction of threshold voltage. (Pictured above are the radiation effects on SiC power MOSFETs: (a) TID effect and (b) DD effect.)



Using the accumulated data, the team have formulated design criteria to ensure the long-term reliability of SiC power semiconductors for space applications.

Jae Hwa Seo of KERI said, "Setting various radiation effect parameters and testing core components in similarly simulated environments is considered a key space industry technology worldwide," adding that "this technology will be applied across various fields including aerospace, medical radiation equipment, nuclear power plants, radiation waste treatment facilities, and military/defence electronics."

The research team plans to expand the technology's scope by pursuing reliability evaluations of SiC power semiconductors under ultra-high energy (over 200MeV) radiation conditions and developing advanced radiation-resistant power semiconductors.

Additionally, they are conducting research on future power semiconductors using diamond in collaboration with Gyeongnam Province and Japanese company 'Orbray'. Their goal is to contribute to Korea's development in high-value-added aerospace industries.

The results showed that drain currents were reduced at 30 MeV and proton fluences of 1 × 1014 cm^{-2} due to the displacement damage (DD) effect

Trend in electromobility continues

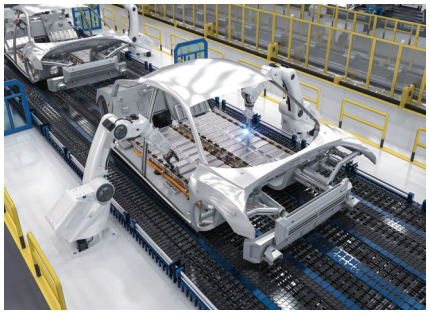
Almost 42 million EV cars worldwide according to German research organisation ZSW

14.8 million new electric vehicles were registered worldwide in 2023 (EVs running on battery power alone, plug-in hybrids and vehicles with range extenders), according to new research by ZSW's Centre for Solar Energy and Hydrogen Research Baden-Württemberg, Germany.

China is in the lead with over nine million electric cars while the USA has claimed second place ahead of Germany. The number of new registrations of electric cars in Germany last year was almost 700,000. This brings the current tally of electric cars on German roads to 2,330,400 but this is not enough to achieve the goal set by the German government of 15 million electric vehicles by 2030. The annual level of new registrations would have to double or triple in order to achieve the target.

The global count of electric cars in circulation at the end of 2023 was almost 42 million. More than half of these vehicles are registered in China, ahead of the USA in second place with 4.8 million electric cars and Germany in third place. Setting aside the Chinese figures, the highest growth rates in circulation were seen primarily in smaller markets like Belgium with 71 per cent (192,400 vehicles) or Portugal with 54 per cent (65,000 vehicles). In terms of new registrations, the EU is the second largest market in the world after China. Around 2.5 million new electric cars were registered here in 2023, with the USA following in third place with 1.5 million vehicles. Electric cars still have the highest share of the total vehicle market in Norway where four in every five new vehicles are powered by electricity.

Germany, by contrast, is seeing a significant slowdown in the momentum gathered in 2022, when the figures rose by 22 per cent on 2021, and is now reporting that new registrations actually fell by 16 per cent in the past year. One of several factors accounting for



this development, says ZSW, is that sales of plug-in hybrids have fallen sharply since the government subsidy scheme ended on 31 December 2022. It is also evident, however, that an 11 per cent growth in cars run entirely on battery power did not fully compensate for this decline.

The higher initial outlay on the purchase of an electric vehicle remains a frequently cited point of criticism. The relatively weak overall economic situation in Germany has probably also had a dampening effect on the development of electromobility, as have falling fossil fuel prices after the phase of high prices in 2022.

"There is a need for new incentives in the market in order to achieve the electromobility targets in Germany – 15 million electric vehicles in circulation by 2030 – and to encourage new momentum in climate action in the transport sector. The initiative for growth proposed by the German government in greater support of electric company cars cannot amount to anything more than an initial step," said ZSW staff member Andreas Püttner.

"In view of the strict austerity budgets choking the public finances, there can be a major impetus in abolishing privileges for conventional vehicles – aka subsidies having an adverse impact on climate targets. Examples of steps which could be taken to come much closer to a 'level playing field', with the same conditions for cars with combustion engines and electric cars, would be to abolish tax breaks for fossil diesel fuels and for company cars with conventional engines, known as the diesel concession and company car concession respectively, or to limit incentives strictly to company cars powered by electricity."

Despite the weakness of the German domestic market, German manufacturers are successful on the international stage where VW, BMW and Mercedes all rank among the top 10 manufacturers and where VW has even moved up to third place in the statistics on new registrations, having sold just over one million cars overall, according to ZSWI.

Compared to the industry leaders BYD (China) and Tesla (USA), however, there is still a large gap in terms of numbers, with Chinese company BYD reporting sales of over three million electric cars and therewith another significant increase of 68 per cent in the number of new registrations compared to last year, thereby maintaining a confident lead in the rankings over the other manufacturers, while Tesla holds on to second place with 1.8 million sales. The most successful model in the world by far last year was again the Tesla Model Y, which was sold over 1.2 million times. Tesla enjoys further success with its Model 3 in third place. The other electric cars in the top 10 worldwide all come from China, with the manufacturers BYD, GAC Group and SAIC increasingly widening their range of vehicles.

"If Germany is to achieve its climate control goals, there is an urgent need for attractive vehicles in the lower and middle segments in order to appeal to a larger customer base. If the German and European manufacturers do not fill this gap, there is a risk that other manufacturers, especially those in China, will seize this opportunity in spite of the introduction of punitive tariffs at European level in a bid to prevent this," added Andreas Püttner.

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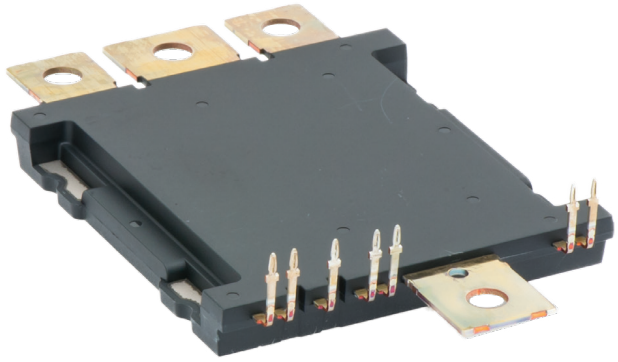


Hitachi Energy

300 mm SiC: A format for when?

Is the unveiling of a 300 mm SiC substrate by SICC going to drive a relatively rapid shift to high-volume production with this format?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THOSE in our industry will probably remember the recent *Electronica* for the unveiling of the world's first 300 mm SiC substrate. This breakthrough, showcased to the world in mid-November from Munich, Germany, is undoubtedly a great demonstration of technical prowess. But is it going to have an impact in an industry that is only just starting to make the transition from 150 mm to 200 mm SiC lines?

Some may argue that this triumph, realised by one of the world's biggest manufacturers of SiC, SICC of Jinan, China, is of little relevance in the near term, but the trailblazer sees the situation differently.

Speaking of its behalf, Chairman Yanming Zong told *Compound Semiconductor* that one of the purposes behind this demonstration is the promotion of industrialisation of 300 mm SiC. While the rate of technical progress and the level of demand for this new format will influence the precise timing of SICC's commercialisation of 300 mm *n*-type SiC substrates, the anticipation is that small production volumes will begin in 2027.

At this stage, it's unclear which chipmakers will be keen to buy this new format. However, Zong believes that some of the leading makers of SiC devices may be willing to invest in upgrading their lines to trim costs, and he points out that some start-ups may see the benefit of beginning with larger wafers.

For all those making SiC devices, weighing on production costs is the slow growth rate of the boules, which are sliced to form substrates.

"We want to continuously reduce the cost of material per unit area by expanding the substrate size," remarks Zong, who hopes that one of the consequences of introducing larger wafers will be an increase in the bang-per-buck of SiC devices.

Swift scaling

Founded in 2010, SICC, which focuses on the R&D, production and sales of SiC substrate material, used equipment designed and installed by its R&D team to produce the record-breaking substrates. This multicultural, highly qualified team took just

18 months to enlarge its *n*-type boules from 200 mm to 300 mm.

The ground-breaking enlarged boule, produced using the same axial growth rate employed for manufacturing of 200 mm material, has a thickness of around 20 mm. From this ingot, it is possible to slice around 25 to 35 wafers with a thickness of 500 μm. And as the team refines its process, it will be possible to produce thicker boules that yield more wafers.

Historically, SiC substrates have been plagued with a variety of imperfections that degrade and even kill devices. However, those issues have now been addressed by many companies, and as the process that's used to fabricate the 300 mm substrate is the same as that used to produce smaller wafers, there is no major barrier to realising state-of-the-art quality with the larger format.

Encouragingly, one of the critical defects, the micropipe, is not a significant issue in SICC's *n*-type 300 mm substrate. With further development, micropipe density is forecast to fall to below 0.2 cm^{-2}, which is a degree of prevalence found in the company's 200 mm *n*-type SiC.

Of more concern are basal plane dislocations. However, while this class of defect needs to be reduced, the company is confident it can replicate the density found on its 200 mm *n*-type substrates.

Efforts will not have to be directed at improving surface roughness. SICC's 300 mm substrate has a roughness of just 0.2 nm, a figure comparable to that for the company's 200 mm wafers.

One of the next steps on the road to commercialisation is the verification of the quality of the epilayers produced on 300 mm substrates. Today, none of the suppliers of MOCVD reactors have tools designed to accommodate this size. However, Zong argues that they will have anticipated the unveiling of this format, and he does not expect tool availability to hold back progress.

The *n*-type 300 mm format that SICC is pioneering is suitable for producing power devices that operate at high voltages and high frequencies and are deployed in inverters and electric vehicles.

As well as being the world's second biggest producer of *n*-type SiC, SICC has other SiC-related products in its portfolio, including a heat dissipation SiC bare product that is said to combine exceptional thermal stability with ultra-high thermal conductivity.

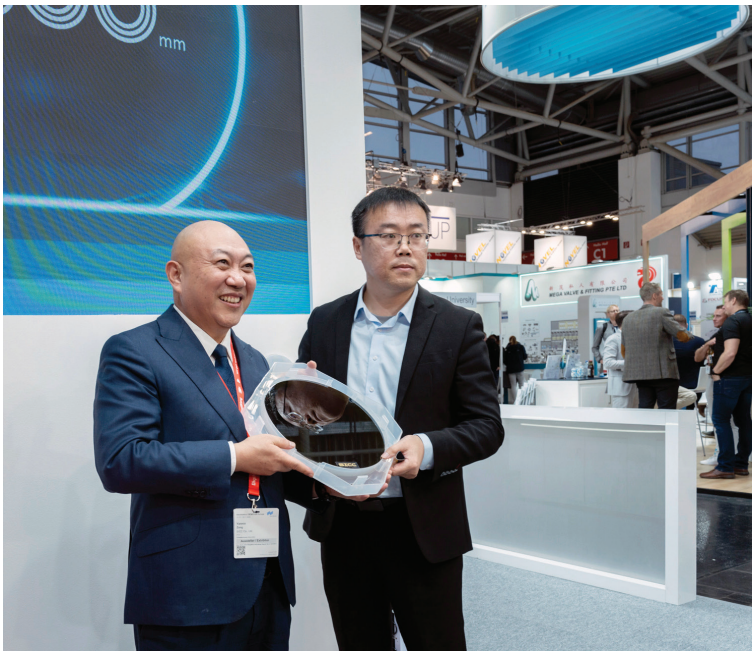
For the last five years SICC has been the third largest producer of semi-insulating SiC, a popular platform for RF products. It also offers *p*-type SiC, the ideal platform for producing bipolar SiC IGBTs, which are attractive candidates for deployment in high-power electronic systems, such as smart grids – they require devices than can handle 10 kV or more.

SICC also offers *p*-type SiC, the ideal platform for producing bipolar SiC IGBTs, which are attractive candidates for deployment in high-power electronic systems, such as smart grids – they require devices than can handle 10 kV or more

A novel growth process

To address concerns related to cost, high resistivity and defect control with *p*-type SiC, SICC has pursued and mastered an alternative growth technology to the standard approach, physical vapour transport. By turning to top-seeded solution growth, the company has been able to produced *p*-type substrates with low threading dislocations, zero stacking faults, and a uniform resistivity that's below 200 mΩ cm. These substrates have an off-cut of 4°.

To increase its capacity for producing 200 mm SiC wafers, SICC is now investing in its facility in Shanghai. This will help to satisfy the global demand for 200 mm SiC substrates. That's clearly going to be the leading format for the next few years, but beyond then there may be the introduction of 300 mm variants, thanks to the recent efforts of SICC.



➤ SICC unveiled its record-breaking 300 mm SiC *n*-type substrate at Electronica, held in Munich, Germany, in mid-November. On the left is the company's Chairman Yanming Zong, and on the right its CTO, Chao Gao.

Paving the way to piezoelectric converters without transformers

How building on its earlier breakthroughs introducing a new way of converting electrical power using piezoelectric resonators and developing a dual-bridge piezoelectric resonator converter, CEA-Leti has paved the way to isolating piezoelectric converters without transformers.

BY GHISLAIN DESPESSE, RESEARCH DIRECTOR AT CEA-LETI

PEW: *You previously worked on introducing a new way of converting electrical power using piezoelectric resonators and developing a dual-bridge piezoelectric resonator converter. If you can perhaps give us a reminder or a resume of that work before we then discuss what you have now developed?*

GD: The use of piezoelectric material for a conversion is quite new. In fact, in the past, some converters used piezoelectric material but as a transformer. Transformer means one piezoelectric primary side and one piezoelectric secondary side and a mechanical coupling between the both parts. But our idea is to use a simple piezoelectric resonator to make an inverter, replacing not the transformer, but the inductor to begin with. We started to work on it in 2016, and we developed that new way of piezoelectric converter. The piezoelectric converter is quite different compared to inductor because a piezoelectric material has a capacitive behaviour outside of its resonance. This means that it's an open circuit in DC voltage while an inductor is a short circuit in DC voltage. The way of use of the piezoelectric material compared to the inductor is slightly different. We have to operate the resonator at its resonant frequency between its resonance and anti-resonant frequency. For proper operation, its energy and load must be balanced during a cycle to avoid any amplification of vibrations and to maintain constant oscillation in steady state.

For proper operation, its energy and charge must be balanced during one cycle to avoid any amplification of the vibration and to maintain constant the oscillation in a steady-state operation. To do this, we can't use only a PWM modulation. We need to add additional voltage level in order to be able to balance the energy and charge during one cycle.

Then we developed a specific control mechanism to drive at least three different voltages to be applied cyclically to the piezoelectric material. In fact, to the piezoelectric material, we apply a first voltage, a second voltage, and a third voltage. But, as the piezoelectric material is also very capacitive, we can't use hard switching. We need to operate the

resonator in soft switching. To do this, we let the resonator move its voltage between two constant voltage phases just by using the inertial movement of the resonator. Then the voltage moves to the next voltage and we close the switch at zero voltage. We can achieve very high switching efficiency. This driving mechanism applied to a simple resonator is a quite big breakthrough in using piezoelectricity for power conversion. One big change is the use of a simple resonator and not a transformer, thus eliminating the need for mechanical coupling between a primary and a secondary, which is a source of losses and reducing the operating frequency. It can address many converters that don't need any insulation.

PEW: *Okay, that's the previous work you've carried out. And this has paved the way to where you are now able to isolate or you're isolating piezo electric converters without transformers?*

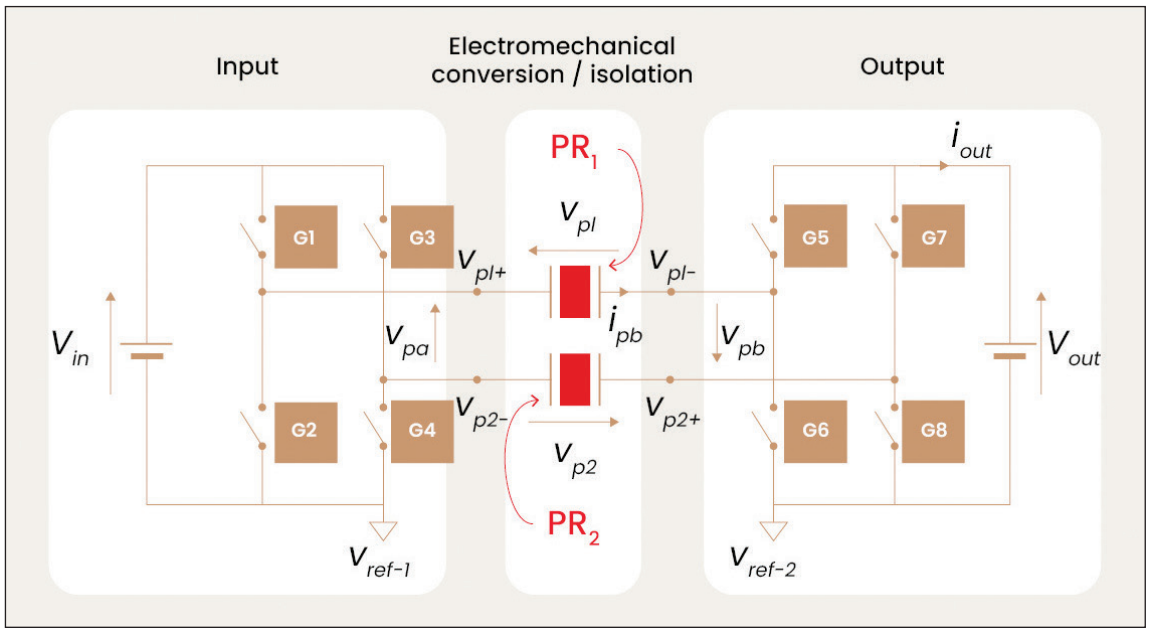
GD: Yes. I've just spoken about non-isolated, because the first idea was to take full advantage of the high quality factor and the high power density of piezoelectric material and not to use the possibility of mechanically coupling two resonant parts. Because we can store a lot of mechanical energy compared to the magnetic energy that we can store in an inductor. We want to use that advantage also for an isolated converter. In place of using a transformer, the idea is to use not only one piezoelectric, but two piezoelectric resonators, one for the direct path and one for the return path in order to ensure the isolation between the primary part and the secondary part of the converter. It's not a transformer, it's just two resonators that operate at the same frequency. The symmetry of the topology means the dual full bridge. It ensures the isolation and prevents a common mode voltage between the primary side and the secondary side. We can then benefit from the advantages of the simple resonator also in isolated converters. With that conversion principle, we reach a power of 179 watts with an efficiency of 89%. This new type of isolated converters can open up a wide range of applications for low powers.
But we saw that there is a limitation. When we increase the voltage, we need more energy to reverse the voltage on the dual full bridge. The idea that we have now developed is to introduce an assisting circuit to reverse the voltage and then to decrease the main current in the principal piezoelectric resonators. Then we can increase the efficiency between 2 and 11% depending on the power points.

PEW: *If I've understood it correctly from what you've told me and what I've read, the new topologies, we're talking dual-bridge isolated piezoelectric resonator converter, providing isolation using two independent piezoelectric resonators. In terms of that, the improved version of DC to DC converter, you talk about improving the efficiency, but also it maintains the converter isolation principle. Is that right?*

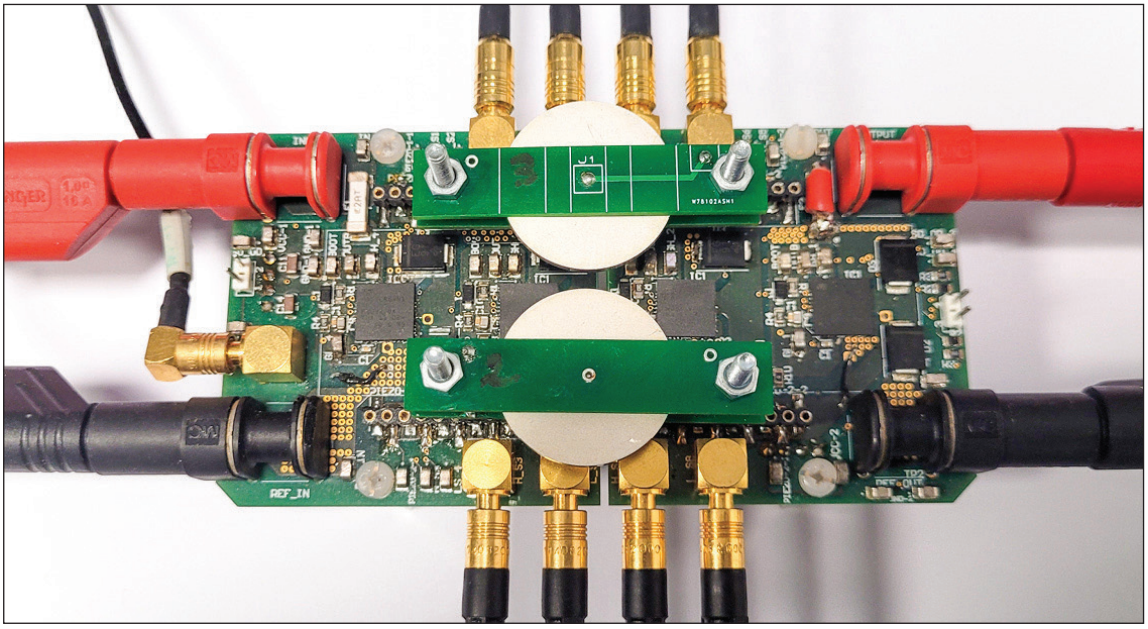
GD: Yes. In fact, the assisting circuit is added to the output and not linked between the input and output. So, there is no break in the isolation between the input and the output. Furthermore, the operation is like differential when one voltage increases while the other one decreases on the full bridge. So there is no common voltage variation at the converter output. It means that the ground of the output doesn't move compared to the ground of the input while the assisting circuit reverses the output full bridge voltage.

PEW: *You presented a paper at PCIM Europe, and that gave a nice summary of the efficiency benefits?*

GD: Indeed, we developed two assisting circuits, one inductive and one piezoelectric. We have



➤ Dual-bridge isolated piezoelectric resonator-based converter (DB-IPRC).



➤ Isolated transformerless piezoelectric DC_DC con verter

shown that the inductive one increases efficiency for any output power. But for the piezoelectric one, it must be sized for a specific output power. Here it improves the efficiency only for high output power because its impedance moves drastically between its resonance and anti-resonance frequency. The effect of the assisting circuit is about 20% to 30% current reduction in the piezoelectric material. It increases efficiency due to the decrease of the currents in the piezoelectric resonators and also in the transistors. Finally, for all the power range, we can get an average efficiency increase of 5%.

PEW: *More generally, can you talk a little bit about the benefits in terms of using electric resonators instead of inductors when it comes to power conversion? What are those benefits you're achieving?*

GD: To reduce the size of converters for years, we have been increasing the operating frequency in order to decrease the size of the passive component. It means the inductors and the capacitors. But when we increase the frequency, we found that the capacitor size reduces drastically with the frequency, but the inductor doesn't reduce as much as the frequency. It means that for very compact converters, the inductor part becomes significant compared to the global volume of the converter. It's like a limitation. Using piezoelectric type converters allows us to significantly reduce the size. This cannot be done by using an inductor because of the inductor losses which increase as we increase the frequency and beceause the saturation field which decreases with frequency. It's a way to overcome this limitation in the pursuit of increasing frequency of the converters in the last decade.

PEW: *By extending the compact conversion that you've talked about to isolated converters, what's the impact in terms of the type of applications that are now possible?*

GD: In fact, non-isolated converters are used in many applications inside the devices. For example, in a computer, the USB, the memory, the computer parts can be powered with different sub voltages. However, many applications also need to be supplied from the electrical network. In this case, we need an insulation, and then introducing the isolation for that type of converter enables us to address these applications, like powering a TV, a robot, a USB port, a battery, etc.

PEW: *In finishing, what impact do you think the development we've talked about will have over time? Also, what other things might you be looking - can you take this work a little bit further?*

GD: Today, we are just beginning to use of piezoelectric resonators for power conversion, and I think it will take a significant part in power electronic in the future. We started by using PZT as piezoelectric material, but this material shows an increase of the losses while increasing the current. It means that the losses increase exponentially with the current. It makes a limitation in term of power density. Currently, we work on lithium niobate material, which is a monocrystalline material. It enables to significantly increase the power density, several kilowatts per cubic centimeter. It's also a bigger improvement compared to the previous material to overpass the magnetic component. But that material has a low dielectric permittivity, so we need to operate it at very high frequency, higher than a few MHz. That is a constraint, but it enables us to achieve very high power density with high efficiency. Finally, the global trend is to increase the operating frequency with improved components in terms of transistors, for example, high wideband gap transistors like SiC, GaN transistors. For the driver, there are some improvements. So, the introduction of that piezoelectric material becomes possible with our current development for the other parts of the power electronics.

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How to choose the right lock-in amplifier

Lock-in amplifiers are important tools for test engineers and material researchers because of their unique ability to precisely measure signals that are otherwise too small to detect amidst noise and other interfering signals.

BY LAKE SHORE CRYOTRONICS

THIS SINGULAR CAPABILITY makes them indispensable in a wide range of low-level measurement applications, from fundamental research in material science and engineering labs to product testing and development by electronic component developers and manufacturers.

In addition, lock-in amplifiers are increasingly playing a vital role in advancing research and innovation in various rapidly evolving fields, such as in the characterization and testing of quantum computing devices, including superconducting and topological qubits, as well as analyzing signals from quantum sensors. Plus, as electronic devices continue to get smaller, lock-in amplifiers play a key part in enabling researchers to precisely measure small signals in nanoscale structures, such as nanowires, nanotubes, and nanoelectromechanical systems, as well as single-electron transistors, quantum dots, and nanoscale sensors.

Because they improve measurement quality by enhancing the signal-to-noise ratio (SNR) and enabling phase-sensitive detection, lock-in amplifiers enable you obtain more precise and therefore repeatable measurements. Advanced features, such as programmable hardware and software filters and the ability to identify and measure multiple reference frequency harmonics, enable you to use them in an even wider range of highly complex measurement applications.

When used in less-complex measurement applications, if you're new to lock-in detection technology and typical lock-in products, you may find it difficult or confusing when researching and evaluating lock-ins for purchase. This paper aims to help simplify the selection and buying process.

The benefits and standard functions of a lock-in amplifier

A lock-in amplifier is a versatile instrument designed to measure weak signals that are obscured by noise and often also DC offsets. They do this by measuring very low amplitudes of the frequency of interest in the presence of large broadband noise and large spurious signals at other frequencies. They selectively extract signals with the same frequency and phase as a known reference signal using phase-sensitive detection.

This reference signal, which is typically generated using an internal oscillator or externally using some other modulation equipment, has a specific frequency and phase compatible with the samples and signals to be measured. The lock-in process begins with the input signal containing the desired weak signal of interest combined with the reference signal being fed into the lock-in and then amplified and fed into the digital phase sensitive detector (PSD).

The PSD performs a multiplication process, which is a de-modulation process, resulting in the production of sum and difference frequencies as well as phase and amplitude information. The desired signal having the same frequency and phase as the reference signal is then reported as the measured X amplitude and Y phase results.

As for the lock-in amplifier output, it is a voltage proportional to the amplitude of the desired signal, which is now separated from the noise. The output also provides phase information relative to the reference signal, which can be useful in various measurement applications.

The different types of lock-in amplifiers available today

Evaluating lock-in amplifiers for test and measurement and material research applications involves ensuring that the equipment meets the specific requirements of your experiments or testing setup. But before you do, understand that there are different lock-in product types available. Here are the most common ones:

Single-input lock-in amplifiers

These are dedicated instruments designed specifically for lock-in voltage and in some cases, current detection. They are highly specialized and are ideal for applications requiring high precision and flexibility for low signal detection, particularly when measuring weak photonic signals, small changes in resistance, or signals from piezoelectric devices. They are also good for phase-sensitive measurements when studying material properties that depend on the phase relationship between an excitation signal and the response.

Multichannel lock-in amplifiers

These lock-in types can process signals from multiple inputs simultaneously, making them suitable for experiments that require measurements from several sources at once or need to monitor multiple harmonics of multiple signal channels. They are particularly useful for experiments or test applications where you need to measure several parameters or samples at the same time and you're looking to increase throughput and efficiency. They are also ideal for complex characterization or testing applications because they allow the measurements to be made under various conditions by measuring multiple frequencies concurrently.

Lock-in amplifiers with built-in programmable voltage and current sources

Most lock-in amplifiers come with an integrated signal source, simplifying the setup by providing both the excitation signal for the sample and the detection mechanism in one unit. These are particularly useful for impedance spectroscopy, which involves studying the frequency response of samples by applying an AC signal and measuring the resulting current or voltage. They are also useful for investigating electrochemical processes, where they can supply an AC voltage to the electrochemical cell and measure the AC response.

Multichannel systems for sourcing and measuring with built-in digital lock-in

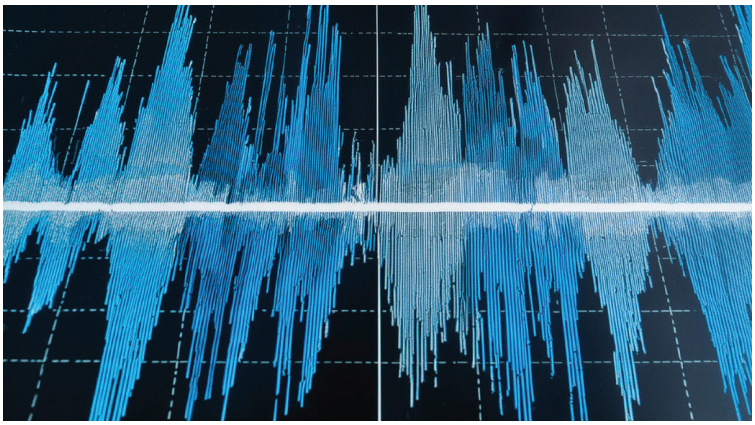
Lock-in amplifiers are primarily voltage measurement devices, and to add current and

resistance measurements for low-level material or device characterization generally requires additional source and V-to-I conversion instruments as well as gain and filter enhancement preamplifiers. But it is possible to get such capabilities built into the same measurement system itself with the lock-in capabilities implemented digitally. Such is the case with the Lake Shore M81-SSM synchronous source measurement system, a type of multichannel system that combines DC and AC sourcing with DC and AC measurement and enables continuous data sampling on every connected channel.

This high degree of synchronization between source and measurement means that the M81-SSM can be used to make lock-in measurements that can extract very weak signals from noisy backgrounds, and each channel can be set to perform AC, DC, or lock-in measurements. The higher sensitivity for lock-in detection is particularly useful for characterizing low-power or low-resistance electronic devices.

Key considerations when choosing a lock-in amplifier

Choosing a lock-in amplifier for your application involves several steps to ensure that it meets the specific requirements of your experiments or testing setup.



Here is a list of considerations when evaluating a lock-in amplifier:

The smallest and largest signals you need to measure (both current and voltage)

Determine the range of signal amplitudes and the resolution to which you need to measure the smallest and largest signals. This information is often found in product datasheets. In specifications, measurement sensitivity (given in µV/nV and µA/nA) and resolution (given in number of digits or ADC bits) should be listed in terms of absolute accuracies traceable to a specific standard and ideally include offsets, time, and temperature drift adders so you obtain a realistic understanding of lock-in instrument and total system uncertainties to ensure your application needs are satisfied.

Typical lock-in amplifiers referenced in many research papers have varying levels of accuracy, noise, and drift specifications and are typically specified around 1% absolute accurate to a given voltage or current standard. While sufficient for many applications, a best-case accuracy and repeatability specification of 1% may not provide adequately precise or repeatable/ reproducible results over time. This is why an entire system error budget should be established. Once it is, you can determine each instrument's measurement error contribution and suitability for each given test setup.

Also note the input resistance specifications of the lock-in and whether there is the potential for the lock-in affecting your measurements due to shunt loading of higher-resistance samples. For example, connecting a lock-in with 10 MΩ input impedance directly across a 100 kΩ resistance sample would alone reduce the true signal amplitude by 1%.

For a 1 MΩ sample, the loading effect would be 10%, and so on. Preamplifiers with higher input impedance or alternate input modules for certain lock-ins should be chosen based on this specification in addition to maximum voltage, noise, and other key specifications noted above. The ideal case would be to choose the highest input impedance lock-in that also meets noise and other requirements to avoid use of additional preamplifier add-on instruments.

The signal frequency range you'll be working with

Lock-in amplifiers have specific frequency ranges over which they operate. These can vary, but typically they are from mHz to hundreds of kHz with some reaching MHz and even GHz frequencies for highly specialized RF applications. Choosing a model with a sufficient minimum and maximum frequency range allows you to use it in a variety of applications, from low-frequency measurements typical in some material science experiments to higher frequencies used in other scientific and engineering fields. The maximum operating frequency must encompass the highest harmonics of the reference signal so as not to attenuate or otherwise distort those harmonics.

The lock-in, in the simplest description, is an AC voltmeter that measures at one frequency both the amplitude and phase of the input. In most cases, a DC signal cannot be measured, which is both a benefit and a limitation of the lock-in in some applications. The lock-in's inherent ability to reject DC signals, while a benefit in the case of unwanted thermal offsets, can be limiting in applications where DC biasing is required because typical lock-in's cannot measure DC signals separately from the AC signals at the reference frequency. There are also cases where high levels of DC mixed into the AC signals of interest can overload and even damage an AC lock-in input amplifier and some commonly used filters and preamplifiers as well.

Certain newer digital lock-ins have two voltage inputs, and the coupling of the input can be AC or DC. Because these lock-ins, like most modern lock-ins, operate using digital signal processor (DSP) technology and can work to very low frequencies, the DC coupled input is often required (even while the lock-in itself is measuring an AC signal).

Another thing to keep in mind: The frequency range you need can differ depending on application. For example, a 2D material characterization application may have different frequency ranges versus the frequencies required for testing fully constructed electrical devices. Graphene, transition metal dichalcogenides (TMDs), and other types of 2D materials often exhibit unique properties that are frequency dependent. Characterizing such materials might require very low to high frequencies depending on the physical phenomena under investigation. You may require low frequencies to determine charge transport, conductivity, and dielectric properties, but high frequencies might be necessary for investigating optical properties, plasmonic behavior, or fast electronic transitions.

Also, in the case of testing electronic components to ensure reliability, the required operational frequency range of the lock-in is often determined by the operational frequency range of the device itself, such as low frequencies for power electronics. And it may also be determined by the nature of the tests, which might include noise measurements,

impedance spectroscopy, or harmonic distortion analysis. These tests generally cover a broader frequency range than material characterization, as they need to simulate operational conditions the device may encounter in real-world applications.

Data acquisition and transmission speeds

The bandwidth and time constant — essentially, a measure of the response time of the lock-in amplifier's low-pass filter and how long it takes to "settle" to a steady state output after a change in the input signal — affect how quickly it can accurately respond to signal changes. If the signal changes rapidly, a shorter time constant (higher bandwidth) may be necessary to track these changes accurately. For signals that change slowly or when measuring very low-level signals where noise is a significant concern, a longer time constant (lower bandwidth) would be more appropriate.

Separate from the signal data acquisition speed, you should also consider transmit data rates to remote PC controllers, especially in streaming and applications studying time-varying signals. Lock-in technology that tightly synchronizes data collection and supports streaming can be useful in these situations. It can also be beneficial when you are measuring multiple devices and need consistent data under identical conditions across all channels. Channel-to-channel synchronization may require individual ADCs per input channel versus the more typical multiplexed single ADC-type approach to adding measurement channels.

The acceptable level of noise in your application

Assess the input and complete system noise levels of the lock-in amplifier and ensure they are low enough for your applications to achieve a high SNR. Applications requiring a high SNR can include those involving impedance, photoluminescence, or magnetic resonance spectroscopy, electrochemical measurements, and optoelectronic device characterization. In contrast, there are also characterization applications where it is less critical, such as some DC electrical characterization environments, high-power device testing setups, or high-frequency RF/microwave characterization applications. Additional preamplifiers add noise to the signal chain and must be factored into the total system noise analysis and budget versus needs.

How much phase sensitivity you require

Ensure the lock-in amplifier can accurately measure the phase difference between the reference signal and the signal being measured. Phase-sensitive measurements are particularly important for certain spectroscopy applications where you need to extract spectral features and identify spectra components. They are less relevant for DC electrical characterization or high-power device testing, where factors like dynamic range and distortion characteristics are more important. One thing to keep in mind for applications requiring highly accurate phase sensitivity: Environmental conditions such as temperature stability, electromagnetic interference, and signal attenuation can adversely affect the lock-in's ultimate usable and repeatable sensitivity and accuracy.

Steps involved in evaluating and qualifying a lock-in amplifier

Step 1: Define your requirements

- Determine the smallest and largest DC and AC signals you need to measure and the range of signal amplitudes you need for lock-in detection.
- Identify the frequency range of the signals (fundamentals and harmonics) you will be working with. Lock-in amplifiers have specific operational frequency ranges, so choose one that covers your needs.
- How fast will you need to acquire (as well as transmit) data? The time constant and bandwidth of the lock-in amplifier affect how quickly it can accurately respond to changes in the signal.
- Assess the noise levels of the lock-in amplifier and ensure they are low enough for your applications to achieve a high enough SNR, and also determine the level of hardware and software filtering required.
- Determine the types of inputs and outputs you need (e.g., voltage, current, digital, analog) for interfacing with other equipment and/or integrating into larger characterization or test setups. Along with types of inputs and outputs, think about your requirements for future expansion and the need for additional input channels later.

Step 2: Evaluate technical specifications

- Look for lock-in amplifiers with frequency ranges that cover your signals of interest. Ensure that the range covers the fundamental frequency as well as any related modulation frequencies of the signals you intend to measure.
- Assess the dynamic range and sensitivity specifications to ensure they meet your amplitude range requirements. When comparing specs between different models, dynamic range might be specified in terms of a ratio (e.g., 1:1,000,000) or in decibels (dB).

- Look at accuracy specifications, expressed as plus or minus a percentage vs. time and calibrated temperature. Even if you don't care about an absolute accuracy to a known standard, you will likely want successive measurements to be within some range of precision so you can reproduce results over time. Sufficient accuracy specifications ensure sufficient repeatability. If you require repeatability to 1%, then you should have accuracy of roughly half of that, or 0.5%, because the variation can span ± the accuracy specification, for +0.5 to −0.5% or a total of 1%. And if you have more than one instrument in your system, then you need to add each instrument's contribution to errors (which reduces total system accuracy).
- Check the phase sensitivity specifications, typically expressed in degrees or milliradians, to ensure they meet your measurement precision needs. The phase sensitivity specification will tell you if it can accurately measure the phase difference between the reference signal and the signal being measured.
- Evaluate the data acquisition rates and transfer rates supported by the lock-in amplifier to ensure they are sufficient for your application.
- Compare noise levels among different models and choose one with low input-referred noise for accurate measurements. These specifications are typically expressed in terms of voltage or current noise density (e.g., nV/√Hz or pA/√Hz). Lower input-referred noise levels result in higher SNR measurements, particularly when dealing with weak signals or low-level measurements.
- Look at which type of filtering is available (e.g., lowpass, band-pass) and their adjustable parameters to match your signal processing needs. Adjustable filtering settings enable you to optimize noise rejection while preserving the integrity of the signal of interest.
- If measuring harmonics of the fundamental frequency is necessary, check the lock-in amplifier's harmonic detection capability for detecting and measuring these signals and ensure the highest harmonics do not exceed the maximum input frequency and processing ratings.

Step 3: If possible, test it out

If the manufacturer can provide a demo unit, request it and conduct bench tests to verify performance specifications within specific conditions. In addition, test the lock-in amplifier within your research or measurement applications to ensure it meets all practical requirements. You will want to verify performance across the required frequency range within your actual setup, which can be done using an oscilloscope, frequency counter, or spectrum analyzer to monitor and verify the frequency response.

Step 4: Find out if post-sales support is available

Consider the level of technical and application support provided by the manufacturer, including availability of user documentation and if their in-house experts can be reached easily and can answer application-specific questions and help with troubleshooting. Similarly, check the warranty period and service options in case of malfunction or the need for calibration.

Step 5: Compare costs, accounting for the total system

Evaluate the cost of the lock-in amplifier in relation to your budget and the return on investment by considering the performance improvements it brings to your applications. However, be sure to look at the total cost of ownership for the entire system, too. Additional costs relating to accessories, software, or necessary upgrades may impact how much you spend in the long run.

How to overcome the learning curve when using lock-in amplifiers

To help you better grasp how a lock-in amplifier works and how it can benefit your specific application, you may want to:

Evaluate the cost of the lock-in amplifier in relation to your budget and the return on investment by considering the performance improvements it brings to your applications. However, be sure to look at the total cost of ownership for the entire system, too. Additional costs relating to accessories, software, or necessary upgrades may impact how much you spend in the long run

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- Familiarize yourself with the basics. Start by learning the fundamental concepts and principles of lock-in amplifiers, such as synchronous detection, phase-sensitive detection, and time constants.
- Carefully read the user manual provided by the manufacturer. It will contain essential information on the instrument's features, specifications, and proper operation.
- Search the web for online tutorials, application notes, and other lock-in amplifier resources. These materials can provide valuable insights and practical examples of how to use and implement lock-in amplifiers in various experimental setups.
- Get hands-on practice. Experiment with the lock-in amplifier using a simple test setup, starting with basic measurements and gradually progressing to more and more complex experiments.
- Consult with experienced users. Colleagues, professors, or others in your field who have experience using lock-in amplifiers can provide valuable advice on best practices and techniques to employ in your application.
- Attend workshops or training sessions. Some manufacturers or institutions offer workshops, webinars, or training sessions on lock-in amplifiers. Taking part in these can help you deepen your understanding of lock-in usage and learn from experienced professionals.
- Develop a process. When setting up and configuring the lock-in amplifier for your experiments, a process-based approach will help ensure all necessary steps are followed, whether it is properly connecting cables, selecting the appropriate input and output settings, configuring the reference signal, adjusting the time constants and filters as needed, etc.
- Follow a troubleshooting process. If you encounter an issue during experiments, identify potential sources of error and address them one at a time so you can quickly resolve the problem.
- Keep a record. Document what you've learned in your experiments, recording settings and observations to help you track your progress and to reference during future experiments.

Examples where a lock-in amplifier alone may not be the complete solution

A lock-in amplifier is a powerful instrument for measuring weak signals buried in noise. But, at times, they can be expensive and rather complex to use, and in some cases, you may not even need one. For applications with lower performance requirements, other measurement techniques may be more suitable and cost-effective.

For instance, lock-in amplifiers are not well-suited for measuring fast signals with rapidly changing frequency or phase components. This is because the time constants and low-pass filtering in lock-in amplifiers inherently introduce a delay in the measurement, possibly preventing them from capturing fast signal variations.

In addition, lock-in amplifiers work best with sinusoidal signals, and for non-sinusoidal or complex waveforms, they may not provide the desired measurement accuracy. If your application involves these types of waveforms, alternative techniques such as time-domain or Fourier analysis may be more appropriate.

It can also be challenging to use lock-in amplifiers in applications where the reference signal frequency is unknown or unstable.

You will require a stable and known reference frequency for synchronous detection, and if it's not present, you may require additional signal processing techniques to track the frequency.

And there's also the dynamic range to consider. If the signals being measured have a large dynamic range containing a wide range of amplitudes, the lock-in amplifier may not be able to accurately capture the full range without saturating or introducing distortion.

In such cases, you may need high-dynamic-range measurement instrumentation or additional signal conditioning.

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Rewiring the road

Harnessing the power of 48V. Part 2.

BY KIRK ULERY, BUSINESS DEVELOPMENT MANAGER, MOLEX TRANSPORTATION SOLUTIONS

AS THE modern driving experience demands more electronics, the shift toward 48V electrical system technology is rapidly gaining traction, disrupting traditional automotive power architectures. Today's increasingly electrified vehicles need more. This surge in demand is propelling innovation and investment in 48V systems as automakers seek to enhance vehicle performance and efficiency.

Are we at a tipping point?

48V technology is a key enabler for advanced automotive features such as electric turbocharging, regenerative braking and advanced infotainment systems. It provides a compelling solution for a range of vehicles, from gas-powered to electric, and is poised for widespread adoption.

But it's not that easy. For 48V systems to be successfully implemented, challenges such as standardization and cost reduction must be addressed.

How do we clear the hurdles to move forward? What will it take for 48V power to become the new normal? Let's explore these questions together.

Potential of 48V in emerging vehicle segments

The development of 48V power systems provides additional opportunities beyond passenger car in-vehicle features and accessories. It extends to promising potential gains in emerging vehicle segments. Off-road vehicles can leverage 48V power to tackle challenging terrain. Electric power assist for steering, suspension and winches can elevate off-road performance and capability. Additionally, 48V systems can bolster vehicle stability and control in demanding conditions.

Electric and hybrid powertrains benefit from 48V technology as a foundational step toward full electrification. By supplementing electric motors and components, 48V systems optimize performance and efficiency in hybrid vehicles. Also, 48V supports functions like battery management and thermal management, ensuring optimal system operation.

Specialized vehicles, such as those used in agriculture, construction and mining, can harness 48V power to increase productivity and efficiency. By powering hydraulic pumps, compressors and other auxiliary systems electrically, these vehicles can achieve improved performance, reduced operator fatigue and greater responsiveness. This shift to electric-powered components aligns with industry trends toward more efficient, reliable systems, like the development of electric steering and braking in automobiles.

Autonomous vehicles (AVs) rely on robust power systems, and 48V technology delivers. By supplying reliable power to sensors, actuators and control

units, 48V facilitates the advanced functionality needed for autonomous driving. Although full autonomous vehicle deployment is still in its early stages, 48V will certainly help AVs along their path toward more widespread deployment. By targeting these emerging vehicle segments, the 48V technology can expand its market reach and contribute to the overall electrification of the transportation industry.

The journey to full 48V adoption a strategic, phased approach for the successful transition from 12V to 48V

The automotive industry is undergoing a major transformation as it moves from traditional 12V electrical systems toward more advanced electrified powertrains. While fully electric vehicles are gaining traction in market share, mild hybrid electric vehicles (MHEVs) with 48V systems offer a viable interim solution. These vehicles combine the benefits of electrification with the familiarity of internal combustion engines. MHEVs deliver these advantages without the significant costs and infrastructure requirements associated with EVs.

Despite the promise of 48V technology, its adoption is still in the relatively early stages. While some automakers have introduced mild hybrid models, the technology is far from reaching its full potential. To accelerate the transition to a 48V future, a comprehensive roadmap is essential. The following guide outlines key strategies to answer the question: how do we get from here to there?

Develop modular 48V platforms

A modular 48V platform offers a standardized, flexible architecture that can be tailored to various vehicle sizes, types and power demands. This platform consists of interchangeable components, such as electric motors, inverters, DC-DC converters and batteries, which can be combined in different configurations to meet specific vehicle needs.

Like building blocks, this approach enables automakers to efficiently develop and produce a diverse range of vehicles while maximizing component sharing and reducing development costs. Ideally, a modular 48V platform would be utilized across a broad spectrum of vehicles within an automaker's lineup.

By developing modular 48V platforms, automakers can elevate economies of scale, shorten time to market and maintain the flexibility to adapt to changing market trends and consumer preferences. This standardized approach also simplifies the integration of advanced features, such as electric power steering, electric compressors and thermal management systems.

Foster collaboration

Strategic partnerships are key to accelerating 48V system development and expanding market penetration. Automakers and component suppliers must collaborate to overcome technical challenges and establish industry standards. This close cooperation is essential for optimizing system integration, reducing development costs and speeding up time to market.

Joint research and development should focus on upgrading components such as inverters, electric motors and energy storage systems. Equally important is establishing standardized communication and electrical architectures to ensure smooth integration across different vehicle models. By pooling expertise and resources, the industry can work together to broaden the market reach of 48V systems.

Continued technological advancements

Ongoing research and development are crucial to fine-tuning 48V system performance and reducing costs over time. And these are key to accelerating widespread adoption. Focus areas include advancing battery technology to increase energy density, power output and lifespan while finding cost-saving opportunities.

Automotive design engineers must also prioritize the development of more efficient and compact power electronics, such as inverters and DC-DC converters, to improve system capabilities and minimize losses. Advancements in electric motors and generators, particularly in power density and torque output, are also important for fine-tuning system performance.

Additionally, innovative thermal management solutions are vital to maintaining optimal operating conditions for 48V components and extending their lifespan.

By following these steps and applying knowledge gained along the way, the automotive industry can gradually transition to full 48V adoption while mitigating risks and maximizing benefits.

Caresoft Global: pioneering insights into Tesla's 48V evolution

CARESOFT GLOBAL, a leader in automotive engineering analysis, performed an in-depth teardown of Tesla's Cybertruck, the first vehicle of its kind to implement 48V technology. By carefully disassembling the vehicle and analyzing its components, Caresoft uncovered how Tesla's shift to 48V impacts system efficiency, wiring complexity and vehicle performance. Its findings highlight the transformative potential of this architecture for future electric vehicles while identifying key challenges manufacturers need to address on the road to 48V.

Key findings

Enhanced Efficiency 48V systems reduce energy losses and enable lighter wiring harnesses, resulting in significant copper reduction and scalability, ultimately lowering costs. By decreasing the vehicle's reliance on materials such as copper, manufacturers can help mitigate potential raw material shortages and future availability constraints. This also reduces the vehicle's carbon footprint by minimizing material consumption. By decreasing mass, manufacturers are able to achieve higher EV range with the same battery or similar range with a smaller battery system.

Cost reduction

The shift to 48V technology also has the potential to reduce costs for OEMs by reducing the quantity of copper within the vehicle, leading to significant raw material cost savings. By optimizing the wiring design, manufacturers can reduce the weight of harnesses, resulting in smaller battery requirements and lower manufacturing and raw material costs. The reduction in copper weight also enhances overall vehicle scalability, making it a strategic decision for automakers seeking to streamline costs.

Improved performance

The higher voltage and lower current in 48V systems enhance component functionality while reducing noise, vibration and harsh environment impacts. These improvements not only contribute to a better driving experience, — they also support manufacturers in addressing emerging consumer expectations for vehicle performance and comfort. Higher voltage with a lower current enables further feature/content implementation which was previously inhibited by capacity of the 12V/16V volt system.

Future potential

48V technology supports advanced features and wider industry adoption, making it a strategic move for automakers. The scalability of 48V enables seamless integration across a range of vehicles, from luxury to mass-market models.

Conclusion

Tesla's adoption of 48V technology highlights its potential to transform the automotive industry. By carefully evaluating its key benefits and challenges, manufacturers can make strategic decisions about integrating 48V systems into their next-generation vehicles.

CARESOFT'S EXPERTISE By meticulously disassembling vehicles and analyzing their components, Caresoft identifies opportunities for optimization, cost reduction and improved performance. This expertise is invaluable for manufacturers seeking to understand the complexities of 48V systems and develop effective strategies for their successful implementation.

The role of zonal architecture in facilitating 48V integration

Zonal architecture provides a clear advantage over traditional vehicle electrical systems when incorporating 48V technology. By segmenting the vehicle into distinct electrical zones, each with its own control unit and power supply, this approach simplifies the implementation of 48V components.

Enhanced Flexibility and Scalability

Encouraging greater design flexibility for 48V systems, zonal architecture permits automakers to customize voltage levels and component selection for each zone, maximizing performance and efficiency. Additionally, this architecture supports easier scalability across various vehicle models, accelerating time-to-market.

Better power distribution

Managing power distribution within specific zones reduces electrical losses and boosts system efficiency. With dedicated power supplies for each zone, voltage levels are fine-tuned for different components, bolstering overall vehicle performance.

Reduced wiring complexity

Zonal architecture simplifies the vehicle's electrical wiring, reducing weight, cost and manufacturing complexity. Fewer wires and connections also mean a lower risk of electrical faults.

Superior system reliability

By distributing control and incorporating multiple power supply points, zonal architecture improves redundancy and fault tolerance. In the event of a failure in one zone, the system can continue operating with minimal disruption.

As the automotive industry transitions to electrified powertrains, zonal architecture will be vital to optimizing vehicle performance and reducing development costs.

Small and scrappy or tried-and-true? A balanced mindset for accelerating 48V deployment

Established automakers, known for their engineering prowess and manufacturing capabilities, have long driven automotive innovation. However, with rapid technological advancements and shifting consumer

preferences, a more agile approach is essential. Startups innovate quickly and adapt to market changes, while traditional automakers offer resources and decades of experience. By merging these strengths, the industry can accelerate the integration of transformative technologies like 48V systems.

Key strategies for nimble progress

Traditional automotive manufacturing processes optimized for large-scale production can present challenges for rapid 48V system development. To overcome these hurdles, automakers must adopt agile methodologies tailored to the unique characteristics of 48V technology.

Integrating practices such as rapid prototyping, iterative design, and flexible manufacturing can significantly accelerate product development and enhance overall efficiency.

Cross-functional teams and flexible project management

Automakers can benefit from expanding efforts to speed up 48V deployment through cross-functional teams. By bringing together diverse expertise from engineering, design, marketing and other areas, these teams create a collaborative environment that mirrors the agile structure of startups, enabling traditional automakers to respond more effectively to customer desires.

Agile methodologies, initially rooted in software development, are now being embraced by automakers. Frameworks like Scrum and Kanban empower teams to work flexibly, prioritize tasks effectively, and deliver results efficiently.

Iterative development

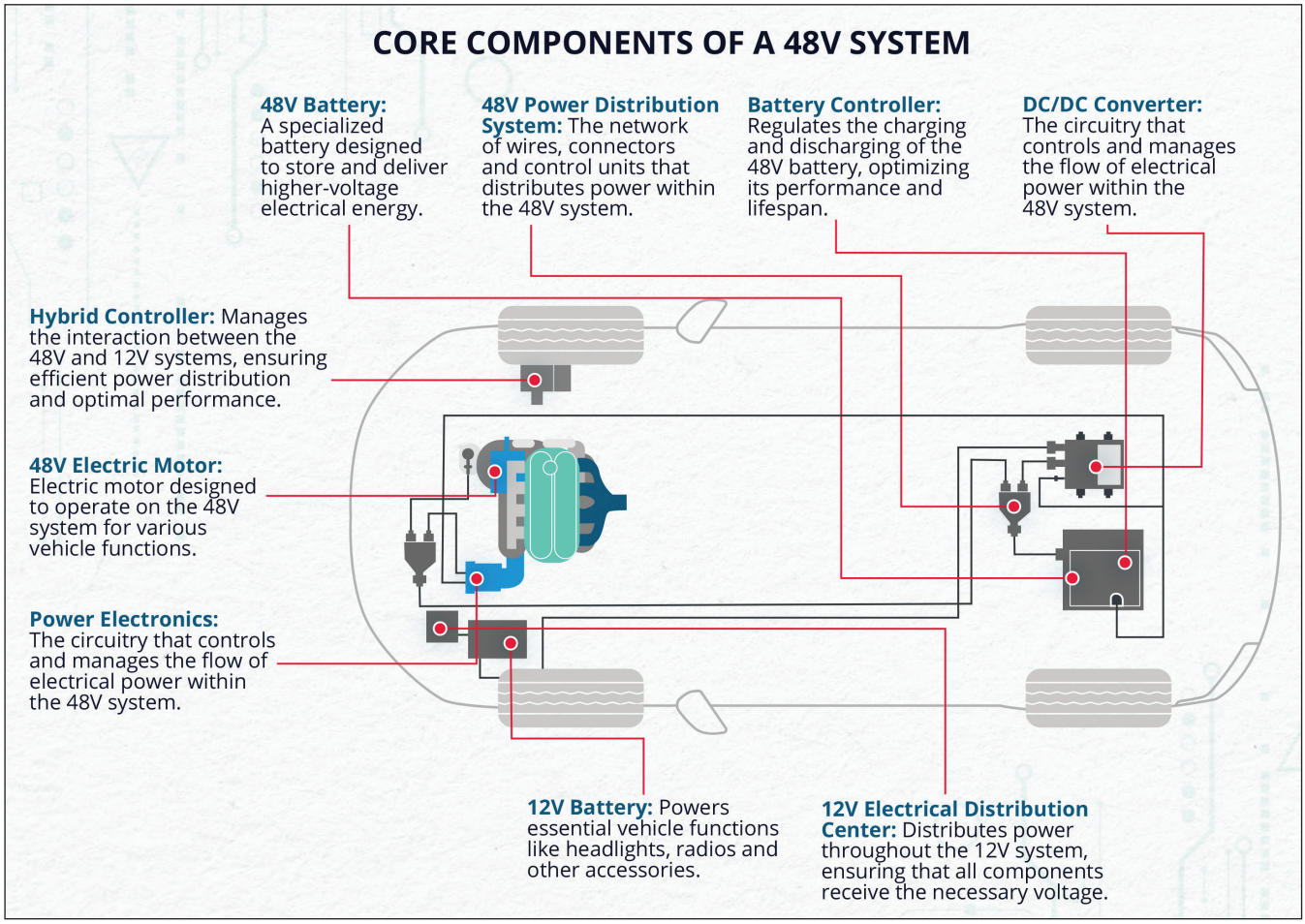
Automakers should adopt an iterative development model to shorten development timelines and enhance responsiveness. This approach allows teams to rapidly prototype, test and refine 48V systems by breaking the process into smaller, manageable cycles. It's a calculated approach that minimizes risks by focusing on incremental improvements rather than overhauling entire systems.

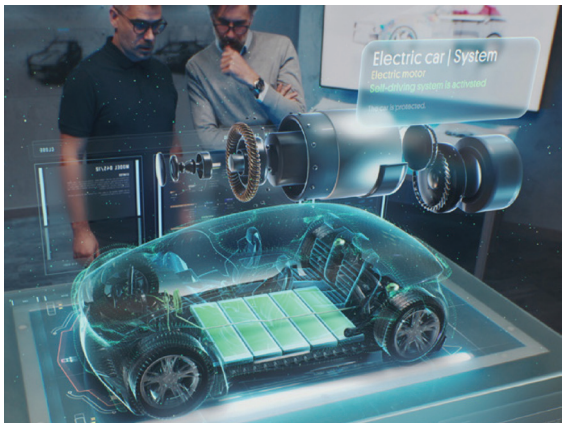
A customer-centric approach

Prioritizing customer feedback ensures that product development aligns with consumer needs. Companies that excel in this area build strong customer relationships, delivering features and experiences that address pain points and resonate with drivers. Engaged customers often become brand advocates, encouraging adoption, positive perceptions and sales.

Partnerships and collaborations

Strategic partnerships with tech startups, component suppliers and research institutions enable





automakers to leverage cutting-edge advancements in automotive technology. Collaborations focused on specific 48V components, systems integration or battery technology can yield groundbreaking results and bring new products to market faster.

Differentiated benefits

Applying startup strategies to established automakers' processes can unlock a unique set of advantages. By combining the best of both worlds – proven techniques and startup speed – automakers can set themselves apart from the rest of the field.

Accelerated market response

Automakers can cultivate a culture of rapid decision-making and iteration by empowering smaller, cross-functional teams. This nimble approach supports faster development cycles, quicker market entry and the ability to swiftly adapt to evolving trends and consumer preferences, providing a competitive edge.

Increased product innovation and enhanced product quality

Dedicated teams focused on specific 48V projects encourage experimentation and rapid problem solving. This facilitates swift prototyping and testing, potentially leading to advanced solutions that address quality issues, augment reliability and ultimately deliver superior product performance.

By integrating quality assurance into this agile framework, automakers can balance speed and innovation with proven reliability, ensuring new 48V systems meet stringent standards. Leveraging testing protocols, automakers lower risks associated with rapid development. Combining rigorous testing with agile practices, they identify and address potential issues early, differentiating them from newer companies and traditional competition. Implementing these strategies significantly boosts automakers' ability to innovate, adapt and compete in the rapidly evolving automotive market.

Molex: driving automotive advancements with every connection

As a global leader in connectivity solutions, Molex is driving support for the development of vehicles with 48V systems. The MX150 Mid-Voltage Connector system exemplifies our commitment to addressing the evolving needs of the automotive industry.

Engineered for efficient assembly and reduced package size, the MX150 delivers a robust, reliable solution for 48V wiring applications. Capable of handling up to 60V, this connector system supports using smaller wire gauges to reduce both weight and cost while maintaining high performance. Its versatility and compatibility with oil-cooled electric motors make the MX150 a top choice for automotive manufacturers.

Molex is committed to forging strong customer partnerships and developing tailored solutions that tackle industry challenges. By combining our technical expertise with customer insights and powerful automotive design and manufacturing capabilities, we are shaping the future of automotive connectivity in a 48V world.

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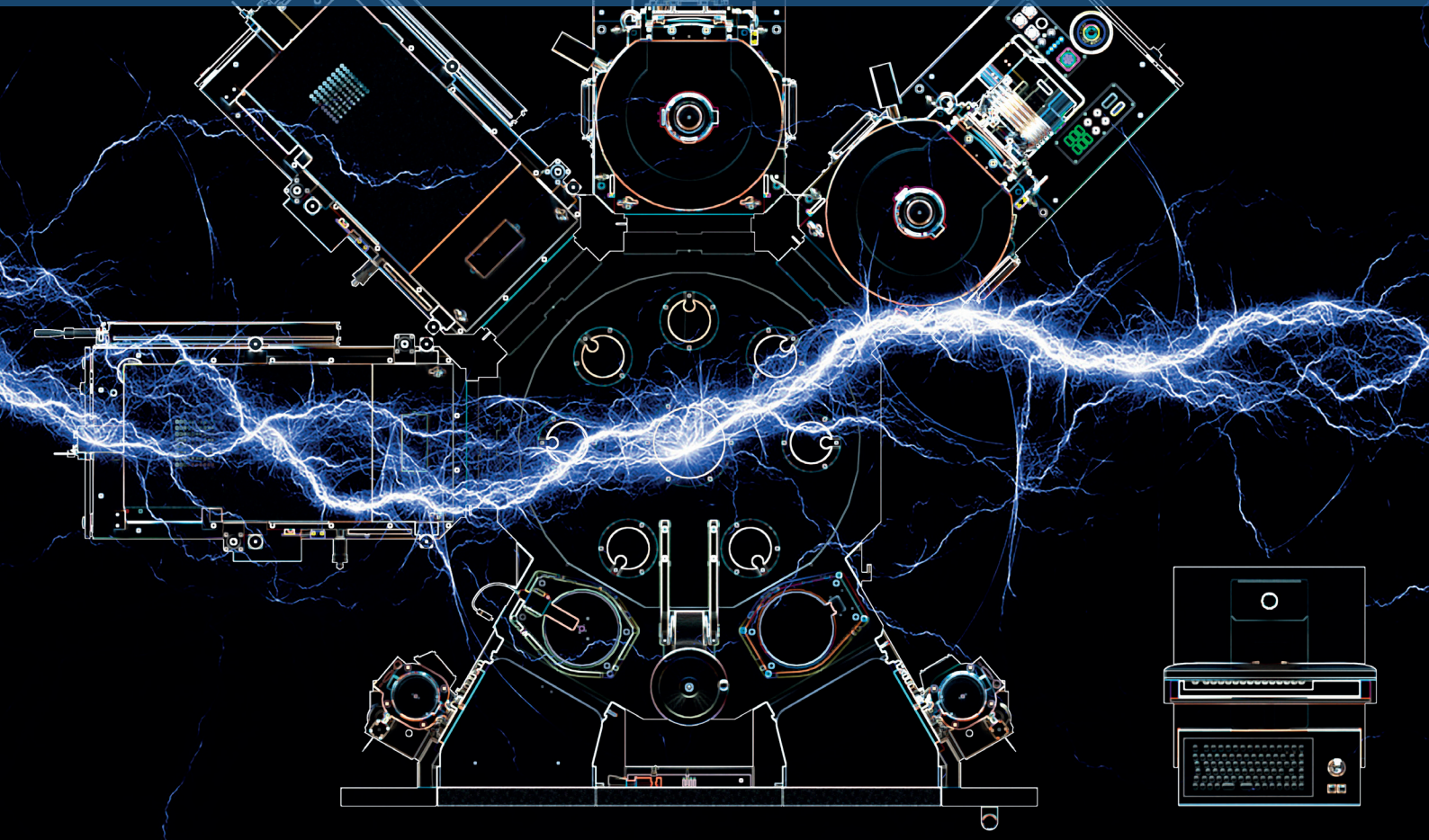

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Imec researchers lay the foundation for affordable mmWave solutions

Hetero-integration of InP chiplets on a 300mm RF silicon interposer delivers outstanding performance at 140GHz – paving the way for scalable, cost-efficient mmWave and sub-THz communications & sensing solutions.

BY SIDDHARTHA SINHA & JORIS VAN DRIESSCHE, IMEC

THE DEMAND for bandwidth, faster (wireless) data transfer, and high-resolution (radar) sensing – along with the increasing pressure on today's radio frequencies – is driving the tech industry to ever higher frequency bands.

But operating at 100GHz (and beyond) poses significant challenges. A key hurdle is the need for device and system components that can deliver higher output power than current Si-CMOS implementations – without increasing module size, cost, and energy consumption.

One promising solution lies in the heterogeneous integration of high-performance III-V materials, such as InP, with wafer-scale Si-CMOS technology. This approach has the potential to achieve high gain and power efficiency at mmWave and sub-THz frequencies in a cost-effective manner, provided that critical technical barriers can be overcome.

Breaking barriers in high-frequency communications and (radar) sensing

As the demand for data-intensive applications soars – from high-speed wireless communications to (automotive) radar – engineers are increasingly turning to mmWave and sub-THz technology.

Yet, at frequencies of 100GHz and beyond, conventional Si-CMOS based technologies face significant limitations. While they excel in wafer-scale integration, cost efficiency, and high-volume manufacturing, they fall short in delivering the power budget and gain required at these higher bands. This is where III-V materials – such as InP – step in, offering superior electronic properties that make them ideal for high-end RF applications. On the downside, however, they come with notable processing challenges – including small wafer sizes, reliance on E-beam lithography, and extensive use of passives and gold-based back-end structures.

These factors increase manufacturing complexity and cost, currently limiting InP's adoption to niche markets.

The solution? Heterogeneous integration – combining the best of both worlds.

Hetero-integration of InP chiplets on a 300mm RF silicon interposer

At the recent IEEE International Electron Devices Meeting (IEDM), imec researchers reported on the integration of InP chiplets with silicon-based wafer-scale packaging – using RF silicon interposer technology.

Silicon interposer technology is a key enabler for digital and high-performance computing applications, benefitting from innovations such as scaled micro-bumps, high-aspect ratio TSVs, and multi-layer Cu damascene routing for high-density signal routing.

Building on this, imec researchers have now adapted silicon interposer technology to also suit next-gen RF applications by adding small, high-performance InP chiplets using CMOS-like processes; an approach that overcomes several limitations of traditional III-V wafer processing techniques.

A key innovation is the addition of low-loss RF layers atop a digital interposer, optimizing signal routing for mmWave applications. Experiments using small-footprint interconnects with a 40µm flip-chip pitch showed that the passive interconnects between the InP chiplets and the RF interposer exhibit a negligible insertion loss of just 0.1dB at 140GHz, underscoring the efficiency of imec's approach. Moreover, no performance degradation was observed when assembling a two-stage InP power amplifier (PA), further validating the robustness of this integration strategy.

The advantages of a chiplet-based approach

The shift toward a chiplet-based architecture (with InP die sizes smaller than 1mm^2) is an essential enabler for scalable and cost-effective mmWave and sub-THz solutions. This approach keeps most of the circuitry in CMOS, while utilizing InP (and potentially other III-V materials) only where its superior high-frequency performance is essential.

By minimizing the use of InP, this approach not only overcomes the underlying processing challenges but also significantly reduces costs compared to full III-V solutions.

Today, however, as the industry pushes beyond 100GHz, the strengths of III-V materials – and InP in particular – are becoming increasingly clear. At these higher frequencies, InP outperforms traditional Si-CMOS solutions, making now the right time to mature the technology, develop scalable manufacturing processes, and drive down costs to enable broader adoption.

Future developments: making InP compatible with CMOS processing modules & toolsets

Building on these promising results, imec continues to actively advance its RF interposer technology – as part of a broader, and longer-term program to make InP fully compatible with CMOS processing modules and toolsets.

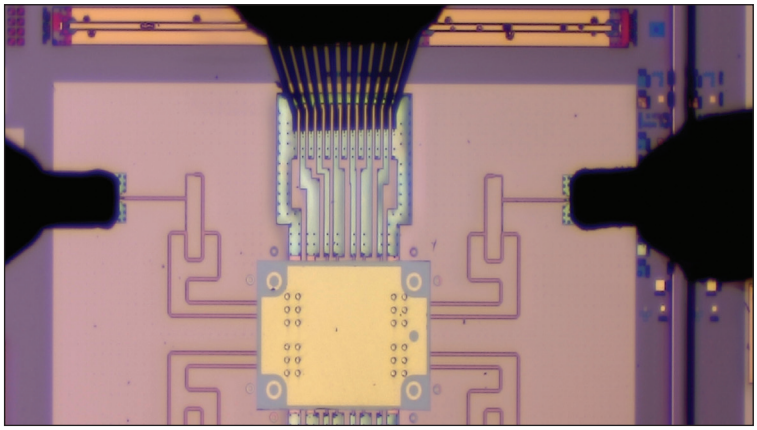
One of imec's short-term objectives is to build a demonstrator for mmWave phased-array and radar applications to further validate its technology in real-world scenarios. In addition, efforts are underway to design and develop even smaller InP chiplets while maintaining their superior RF performance.
To further enhance the functionality of its RF interposer platform, imec plans to introduce additional features, including:

- Advanced passives, such as inductors and metal-insulator-metal capacitors (MIMCAPs) – further reducing cost and footprint;
- Through-silicon via (TSV) integration for improved interconnect density;
- Wafer thinning techniques to reduce overall package thickness and enhance thermal performance.

Finally, imec invites industry partners to collaborate and prototype new designs using its RF interposer R&D platform, enabling them to explore the full potential of chiplet-based integration for mmWave and sub-THz systems.

Conclusion: commercial adoption anticipated in the early 2030s

The successful integration of InP chiplets on a 300mm RF silicon interposer marks a major step forward in the development of cost-effective, high-performance mmWave and sub-THz solutions. By combining Si-CMOS scalability with the superior high-frequency performance of InP, imec's approach overcomes key limitations in III-V material processing.



➤ Hetero-integration of InP chiplets on a 300mm RF silicon interposer delivers outstanding performance at 140GHz (source: imec)

As demand grows for high-speed wireless communication, advanced radar sensing, high-resolution imaging, and next-generation wireline applications this innovation paves the way for applications such as:

- 6G wireless networks, where ultra-high data rates and low latency are essential;
- Automotive radar systems, requiring precise sensing for enhanced safety;
- Medical imaging and security scanning;
- Assembly platform for the electronic part of wireline optical modules.

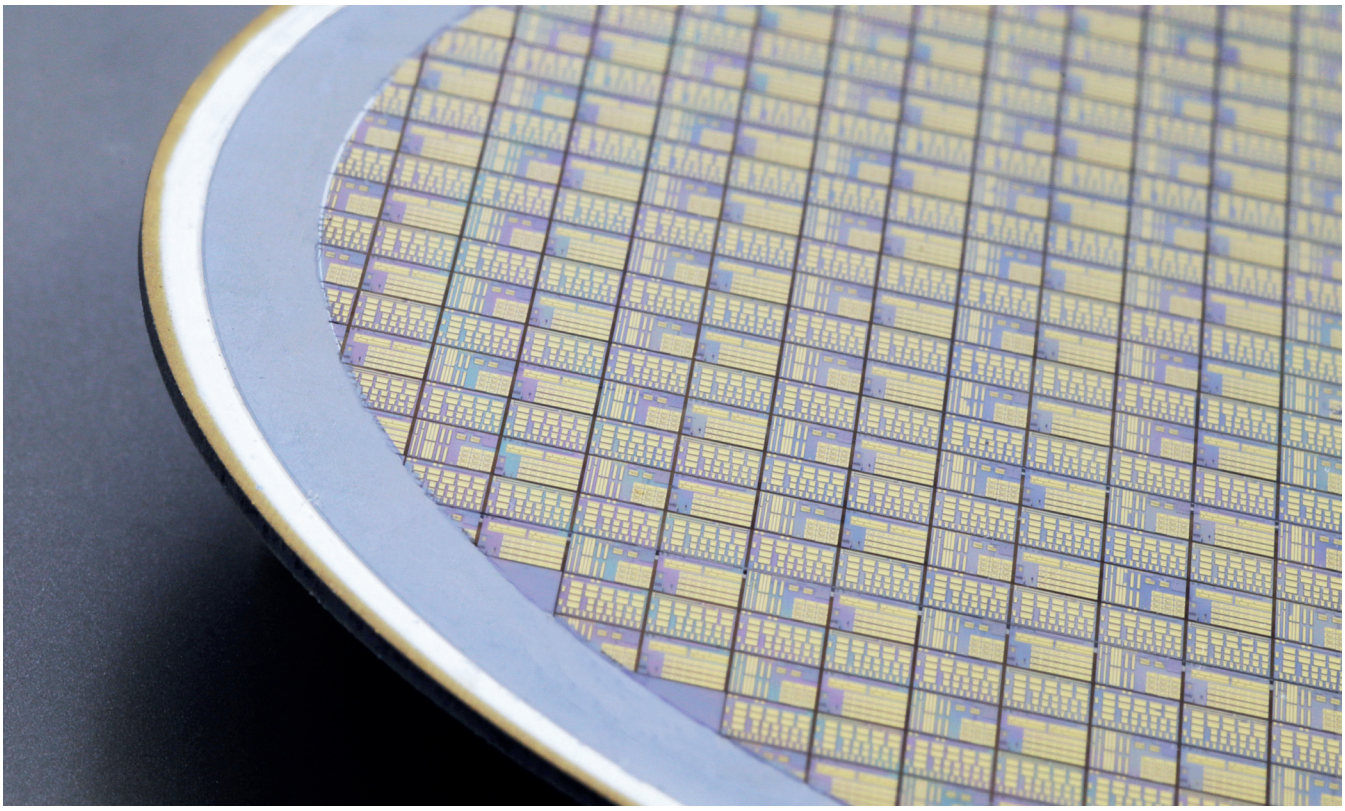
Imec's chiplet-based integration strategy significantly reduces costs compared to full III-V solutions while ensuring seamless compatibility with existing semiconductor manufacturing processes. Ongoing imec research aims to further optimize InP chiplet design, and introduce advanced passives, TSV integration, and wafer thinning techniques on its RF interposer platform.

By addressing these critical integration challenges, imec is paving the way for scalable, energy-efficient mmWave and sub-THz solutions, with commercial adoption anticipated in the early 2030s.

The key strengths of InP

The characterization of indium phosphide (InP) has been a prominent research topic for the past 20-30 years. InP is known for its exceptional material properties – in particular, its high power gain (a critical parameter for high-frequency transistors) and strong dielectric breakdown field (enabling more compact and efficient power devices).

Yet, InP's widespread adoption has been hampered by the lack of an overarching system architecture – including the necessary back-end integration and interconnect solutions. As a result, InP has remained primarily a research topic rather than a mainstream technology, a situation exacerbated by the continued scaling of CMOS to higher frequencies.



Vertical power devices with thick GaN layers on sapphire

Tuning of wafer bow by stealth laser patterning enables the growth of thick epitaxial layers of GaN on sapphire for vertical high-voltage devices

BY ELDAD BAHAT TREIDEL, ENRICO BRUSATERRA, FRANK BRUNNER, ALEXANDER KÜLBERG AND OLIVER HILT FROM FERDINAND-BRAUN-INSTITUT (FBH)

DOMINATING THE HEADLINES of our industry are the vast sums spent on building new SiC fabs and expanding the capacity in existing facilities. In general, such efforts are directed at increasing production of 1.2 kV MOSFETs, a key component in electric vehicles that is helping to maximise their range.

It is beyond question that the SiC MOSFET outperforms its silicon equivalent. But it could be outclassed by vertical GaN-based power switching devices, which promise a superior bang-per-buck.

Leveraging the potential of this class of GaN-based power devices will not be easy – it requires addressing of a number of key challenges. These include: growing a *p-n* diode on a very thick drift layer that has a well-controlled low doping concentration and supports a high blocking voltage; realising a low forward resistance; and ensuring avalanche capability and short-circuit robustness. Finally, the device heterostructure must be compatible with standard process lines.

It is not clear what the most suitable foundation for this device is. While GaN substrates are attractive from a material quality standpoint, their size is limited to between 50 mm and 100 mm, they come at a high price of around \$150 cm^{-2}, and have a relatively high resistivity, exceeding 1 mΩ cm and going up to 50 mΩ cm. Due to these limitations, foreign substrates are usually employed for such devices, with silicon and sapphire being the leading candidates. For both options, the backside drain contact can be established after either local silicon substrate removal, or the removal of the sapphire substrate by laser lift-off.

Regardless of the choice of foreign substrate, heteroepitaxy impairs material quality, with GaN

suffering from an increased dislocation density. Compounding this concern, a blocking capability larger than 1.2 kV demands GaN epitaxial layers with more than 10 μm thickness, magnifying issues associated with lattice mismatch and differences in the thermal expansion coefficients. These issues include increases in threading dislocation density, leakage current, mechanical strain, fragility and wafer bow.

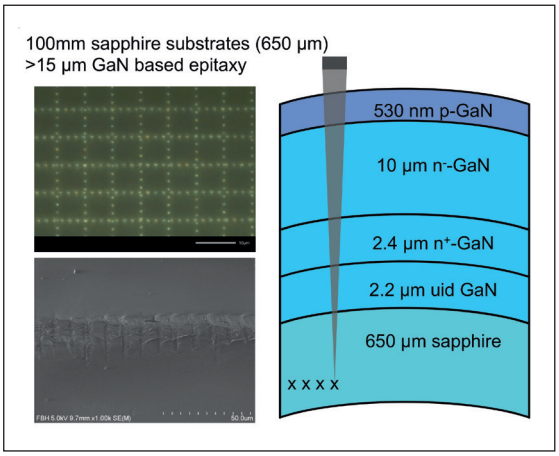
A laser focus

The team at the Ferdinand-Braun-Institut (FBH) is addressing all these issues with a novel approach that employs laser patterning. At the 2024 CS Mantech conference, a technology was unveiled allowing to grow GaN drift layers that are more than 10 μm thick on 100 mm sapphire substrates. Without further measures the resulting high wafer bow would make these wafers un-processable on commercial equipment designed for flat silicon wafers. Progress on this front allowed the demonstration of fully functional quasi-vertical electronic devices, in the form of *p-n* diodes, offering a reverse blocking capability of 1.2 kV.

Key for this success was previous work at FBH on using a focused laser beam to reduce the bow of GaN-on-sapphire-based UV LED wafers. To this end, localised damage inside the sapphire substrate, close to its backside surface was created by a tightly focused laser beam. This damage compensates the internal stress that stems from the large lattice mismatch between the epitaxially grown GaN layers and the sapphire substrate.

With this approach it was possible to reduce bow of sapphire wafers with a diameter of 50 mm and an overall thickness of less than 450 μm. However, upscaling of this technology requires extension to larger wafers with even thicker epitaxial GaN layers. Characterisation of 100 mm GaN-on-sapphire wafers with a total GaN layer thickness above 15 μm shows encouraging results.

At FBH we have an industrial process line that tolerates a wafer bow of less than 125 μm,

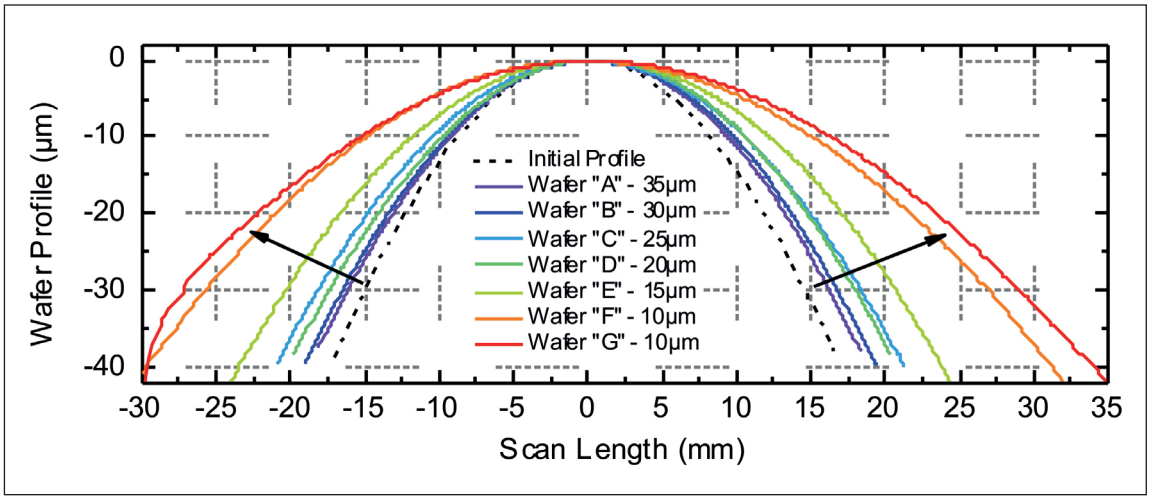


➤ Figure 1. Laser grid pattern top view with 30 μm pitch (top left) and cross-section of the laser damage along one scribe line, resulting in 10 μm of laser spacial period (bottom left). Illustration of the laser scribing process (right).

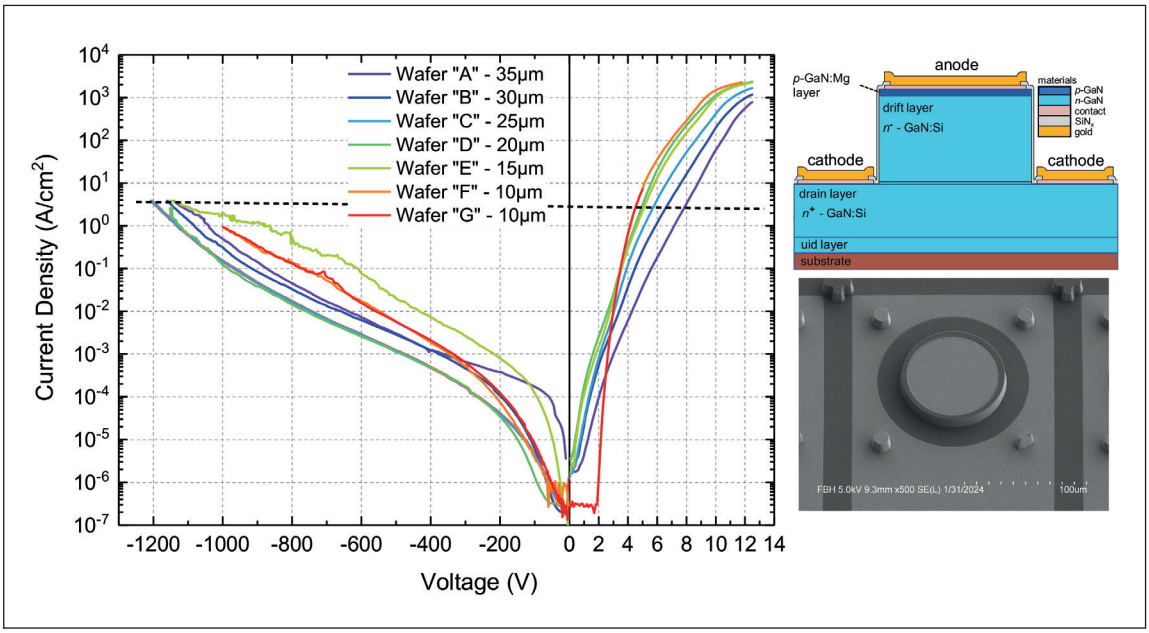
corresponding to a radius of curvature of more than 10 m. However, even with such an accommodating line, wafers with a high bow, but still within process limitations, can still present conformity issues, such as those associated with automated robotic handling, vacuum handling, and uneven temperature exposure.

Our investigations of the impact of laser scribing of GaN-on-sapphire wafers include bow measurements as well as electrical characterization of processed quasi-vertical *p-n* diodes.

The fabrication of our devices began by loading 650 μm-thick sapphire substrates with a diameter of 100 mm into an MOCVD reactor and depositing a 2.2 μm-thick unintentionally doped GaN transition layer, followed by a 2.4 μm highly conductive *n*-type GaN bottom layer, and a 10 μm n^--GaN drift layer with donor density of 1.4×10^{16} cm^{-3}. The doping concentration of the drift layer was assessed with on-wafer electrochemical capacitance-voltage measurements and post-processing capacitance-voltage measurements. After growth of the drift layer, we added a 530 nm-thick top *p*-type layer to form a *p-n* junction and an anode terminal. This structure has a total GaN epitaxial layers thickness of more than 15 μm, and produces an initial wafer bow of around 300 μm, corresponding to a wafer



➤ Figure 2. Optical interferometric bow profile for a range of wafers with different scribing pitches.

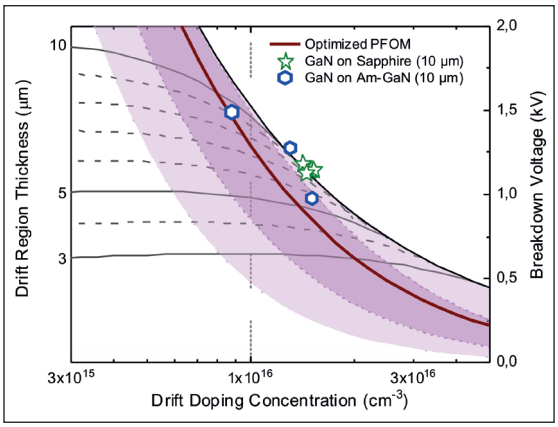


➤ Figure 3. Wafer-level median reverse and forward characteristics for quasi vertical *p-n* diodes produced on wafers with a different scribing pitch (left). An illustration of the cross-section of a quasi-vertical *p-n* diode (top right) and a scanning electron microscopy image of such diode (bottom right).

radius of curvature of about 3.8 m if no measures for bow reduction are applied.

Using a fixed focus depth and scribing pitches ranging from 10 µm to 35 µm, these wafers were patterned by focused laser irradiation from the top side through the epitaxial layer stack. The resulting damage is located around 200 µm above the bottom surface of the sapphire substrate. We employed a 532 nm laser with a repetition rate of 40 kHz, using a feed speed of 400 mm s^{-1} and a continuous laser power of 160 mW, with the focus of the laser inside the sapphire.

The scribing pattern lines are running perpendicular to the flats with the prescribed pitch. Scribing began in the *x* direction (perpendicular (or parallel) to the main flat), and then in the *y* direction, with total processing time roughly 4 hours per wafer.



➤ Figure 4. A comparison of the performance of GaN-on-sapphire quasi-vertical *p-n* diodes with the ideal breakdown voltage values.

Perfect pitch?

Optical interferometric bow profile measurements at different scribe densities revealed that wafer bow progressively is reduced with decreasing pitch. A smaller scribing pitch produces a monotonic increase in the radius of curvature, and bow reaches values as low as around 40 µm, realised with scribing pitch of 10 µm. Note that the change to the radius of curvature resulting from laser scribing is inversely proportional to the scribing pitch.

To evaluate the impact of this bow reduction on processability and device performance, we processed quasi-vertical *p-n* diodes on our line.

We compared devices from wafers with different bow values after laser patterning with different scribe pitch. The reverse-bias off-state current and blocking strength is only marginally impacted by the scribe pitch. In sharp contrast, the onset voltage of our *p-n* diodes is strongly dependent on the laser scribing pitch. This most probably is related to the strain in the layers that is not accommodated by wafer bow.

Our work shows that the laser scribing of sapphire substrates with thick GaN epitaxial drift layers is a potential route for high-volume manufacturing of 1.2 kV vertical GaN devices on low-cost foreign substrates if the carrier concentration in the drift layer can reproducibly be adjusted to about 1×10^{16} cm^{-3}.

This work has received funding from the ECSEL Joint Undertaking (JU), under grant agreement No 101007229. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Germany, France, Belgium, Austria, Sweden, Spain, Italy.

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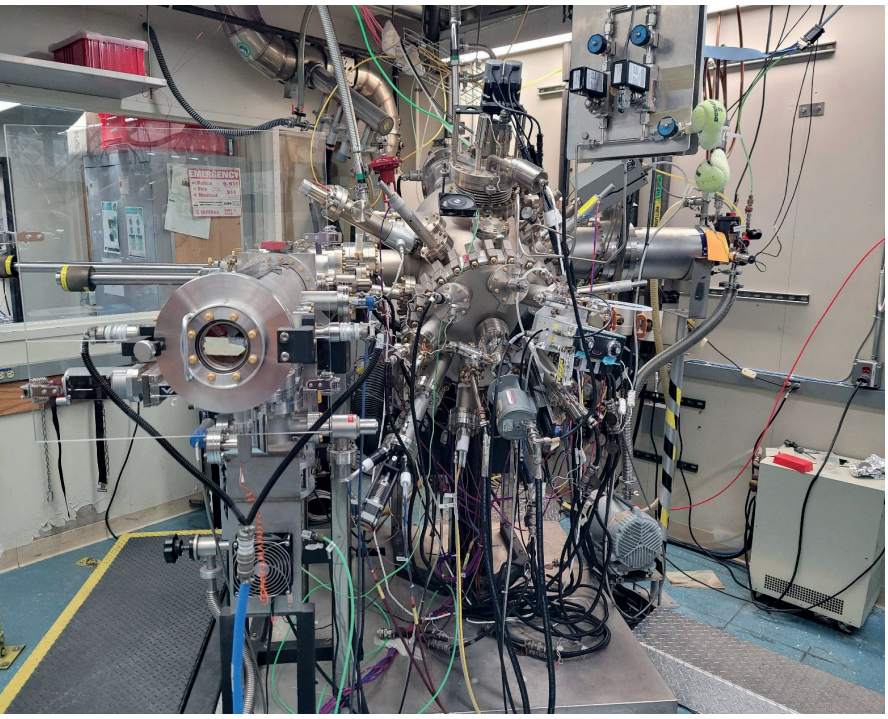
Advancing GaN power devices with **ammonia MBE**

Operating in the kilovolt regime, GaN vertical *p-n* high-power diodes produced by ammonia MBE combine a fast growth rate with an ultra-clean thick drift layer and a smooth surface morphology

BY ESMAT FARZANA,* JIANFENG WANG, KAI SHEK QWAH, ASHLEY WISSEL-GARCIA, KELSEY JORGENSEN, TAKEKI ITOH, ZACHARY BIEGLER, MORTEZA MONAVARIAN AND JAMES SPECK FROM THE UNIVERSITY OF CALIFORNIA, SANTA BARBARA

THE LAST FEW YEARS have seen a surge in demand for efficient power devices. It's a ramp that's been spurred on by the rise of a number of next-generation technologies, including fast chargers, data centres, smart grids, high-speed telecommunication, and electric transportation.

For these high-power switching applications, today's silicon-based technology is not up to the task, with concerns surrounding its poor efficiency, excessive voltage levels, bulky system volume, extensive heating, and power loss. This has driven interest in alternatives based on newer materials systems, such as wide bandgap semiconductors, which are attracting much attention thanks to their capability to enhance power-handling while shrinking system size. Amongst these promising candidates GaN has much appeal, thanks to its excellent combination of a high material breakdown field of around 3.3 MV cm^{-1}, a high mobility, good thermal conductivity, and the availability of both *p*-type and *n*-type material.



➤ The Nitride 930 MBE growth system used for ammonia MBE growth at UCSB.

With such attractive properties, it's of little surprise that GaN has already been adopted in a wide variety of commercial electronics, including RF transistors, power amplifiers, and LEDs. However, for the case of power electronics, commercial GaN devices tend to be limited to 650 V, typically employing lateral topologies.

Switching to a vertical device geometry enables an increase in the operating range beyond 650 V, thanks to a superior electric field confinement and enhanced current capability, supported by a large-area backside contact. However, to enter the multi-kilovolt range, these vertical power devices need to have thick GaN drift layers with very low and well-controlled doping alongside minimal compensation.

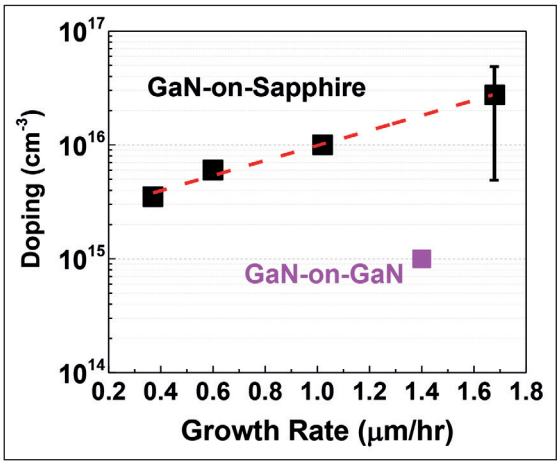
Historically, it has been difficult to address these challenges, due to a lack of freestanding high-quality native substrates. This limitation explains why much of the development of conventional GaN devices has taken place on foreign substrates, such as sapphire and silicon. One downside of these heteroepitaxial growth platforms is that they lead to a high dislocation-density in the epilayers – it is about 10^8 cm^{-2}. Such a high dislocation density may still be tolerable in lateral RF transistors, because dislocations remain perpendicular to the lateral channel. However, that's not the case in vertical devices, where the threading dislocation core directly appears along the vertical channel. For these devices, dislocations severely degrade device performance, creating a high leakage, reducing breakdown voltage, and impairing current transport.

In recent years this state-of-affairs has shifted, due to rapid advances in freestanding GaN substrates, which have significantly lower dislocation densities, ranging from 10^4 cm^{-2} to 10^6 cm^{-2}. These far lower dislocation densities are opening new doors and starting to redefine the landscape of GaN power devices. Within the GaN community, efforts are now being directed at the development of efficient strategies for growing thick epitaxial layers with low impurities that will ensure the desired high-voltage rating with vertical device structures. However, growing thick epilayers is challenging. It demands fast growth rates, comparable or more than 1 µm hr^{-1}, to ensure timely growth, a requirement that leads to increases in impurity concentration and surface roughness.

A significant research effort over many years has involved improving the quality of thick GaN epilayers on native substrates. However, these reports tend to focus on MOCVD-growth of GaN. It's an epitaxial technology that offers a fast growth rate, but due to the use of a chemical-vapour-based synthesis process involving precursors, such as trimethylgallium, it often introduces a high concentration of carbon and hydrogen impurities in the GaN epilayer. These impurities are a menace, dragging down doping efficiency in GaN, due to a combination of donor compensation effects by carbon, and magnesium acceptor passivation effects by hydrogen. Due to these issues, it is far from easy to realise controllable doping over a wide range in *n*-type and *p*-type GaN with conventional MOCVD.

Ammonia MBE for thick GaN

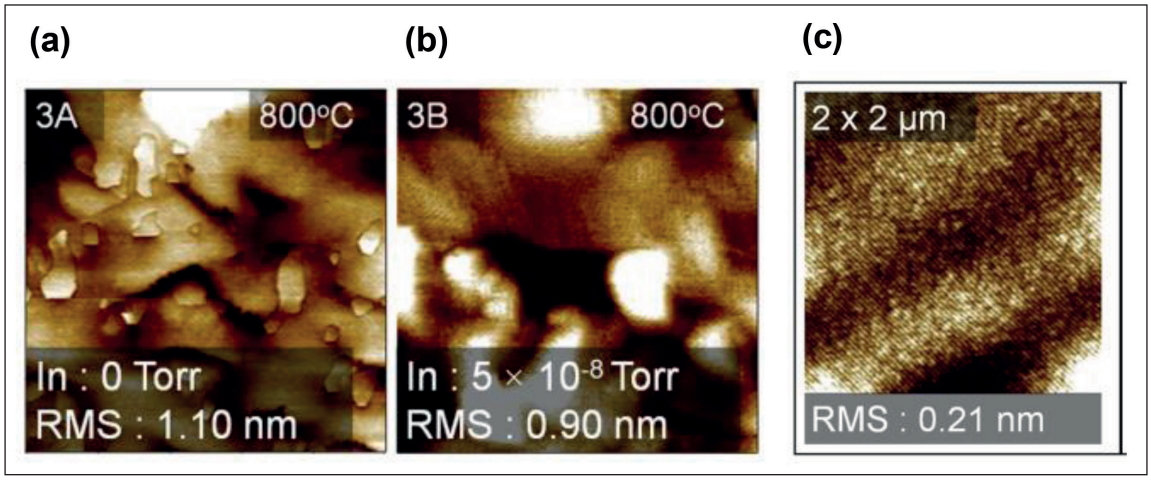
To overcome these challenges, our team that is based at the University of California, Santa Barabara (note that some of us have recently moved on, taking up academic positions elsewhere) have developed an alternative approach to growing thick GaN epilayers that employs ammonia MBE.



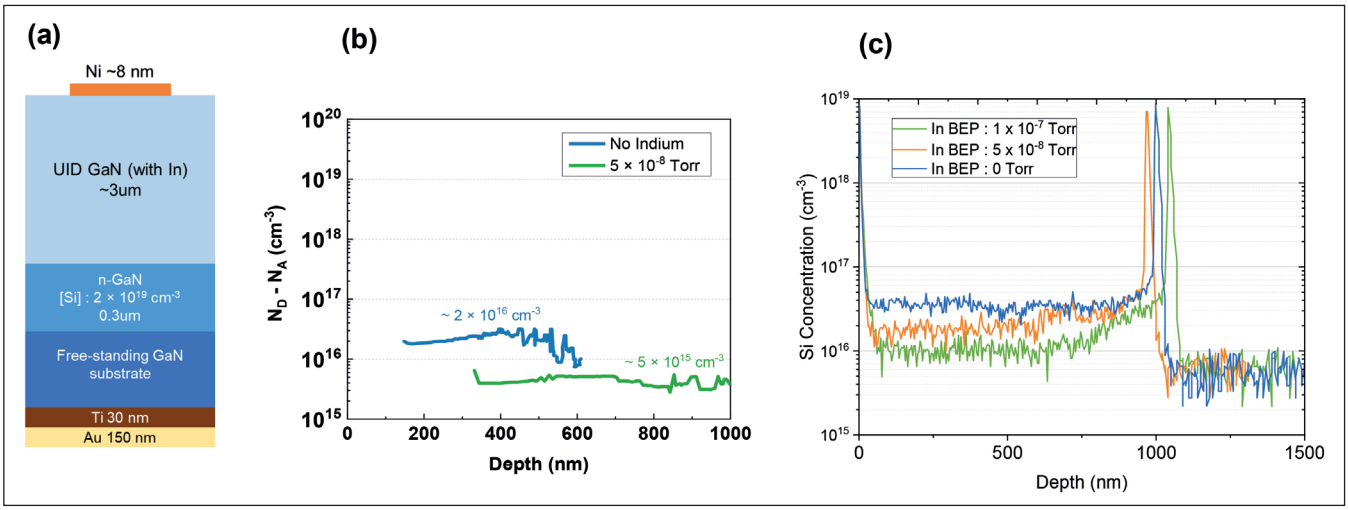
➤ Figure 1. Unintentional background doping in ammonia MBE GaN epilayers as a function of growth rate. The GaN-on-GaN epilayers provided the lowest doping compared with the GaN-on-sapphire ones. For more details, see APL Materials **9** 081118 (2021).

Compared with MOCVD, all forms of MBE offer four key advantages: a clean growth environment in an ultra-high vacuum, which allows the formation of high-purity GaN layers with a background doping as low as 10^{15} cm^{-3}, as well as minimal compensating impurities, such as carbon and hydrogen; a controlled doping profile over a wide range of concentrations, spanning the mid 10^{15} cm^{-3} to 10^{20} cm^{-3}, thanks to minimal compensating impurities; fully activated as-grown *p*-GaN, due to an absence of hydrogen passivation effects; and the opportunity to form an abrupt p^+-*n* junction, due to absence of the magnesium memory effect, a well-known challenge in MOCVD GaN growth.

Within the family of MBE, ammonia MBE offers additional advantages over its plasma-enhanced MBE counterpart. The latter utilises gallium-rich



➤ Figure 2. Atomic force microscopy scans of 2 µm by 2 µm area for unintentionally doped ammonia MBE GaN epilayers (a) on GaN-on-sapphire template using an indium flux beam-equivalent pressures of 0 Torr (b) on GaN-on-sapphire template using an indium flux 5×10^{-8} Torr (c) on a Mitsubishi Chemical Corporation free-standing GaN substrate using indium flux beam-equivalent pressures of 5×10^{-8} Torr. Homoepitaxial GaN growth on a free-standing GaN substrate shows the smoothest surface morphology with very low root-mean-square roughness of 0.21 nm. For more details, see APL Materials **10** 081107 (2022).



➤ Figure 3. (a) An ammonia MBE GaN-on-GaN vertical Schottky diode with epilayers grown with an indium surfactant using an indium flux beam-equivalent pressure of 5×10^{-8} Torr. (b) Lower background unintentional doping achieved by using indium as surfactant. (c) Lower background doping was consistent with silicon secondary ion mass spectrometry impurity profiles in the GaN epilayer with an increased indium flux beam-equivalent pressure. For more details, see APL Materials **10** 081107 (2022).

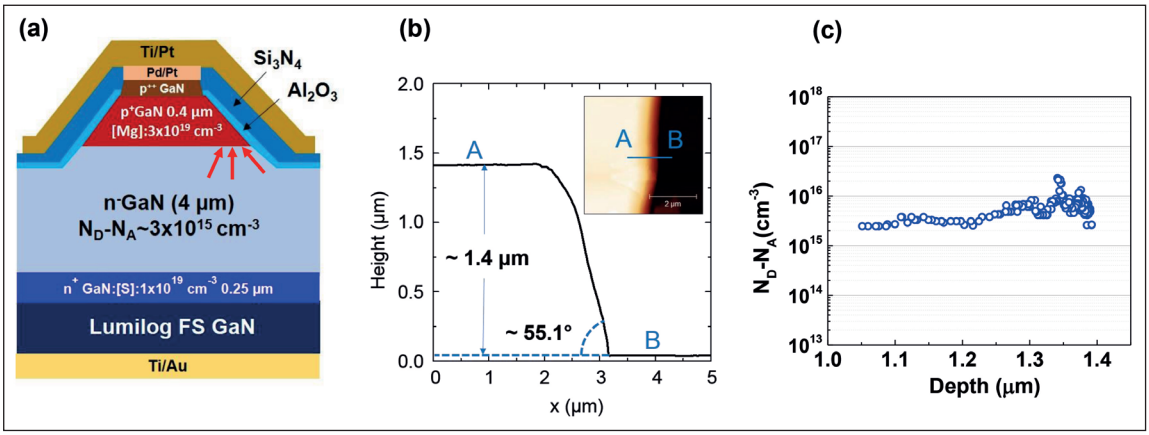
growth conditions, while ammonia MBE allows the growth of GaN deep within the nitrogen-rich region. Due to this, ammonia MBE eliminates gallium droplets, a problem that plagues plasma-enhanced MBE and causes a poor surface morphology.

In recent years, part of our focus has been directed at advancing ammonia MBE growth for the development of high-voltage vertical GaN power switches. Through our pursuit of a synergistic effort that extends from ammonia MBE growth optimisation to device development, we have been able to demonstrate kilovolt-range vertical GaN-on-GaN *p-n* diodes.

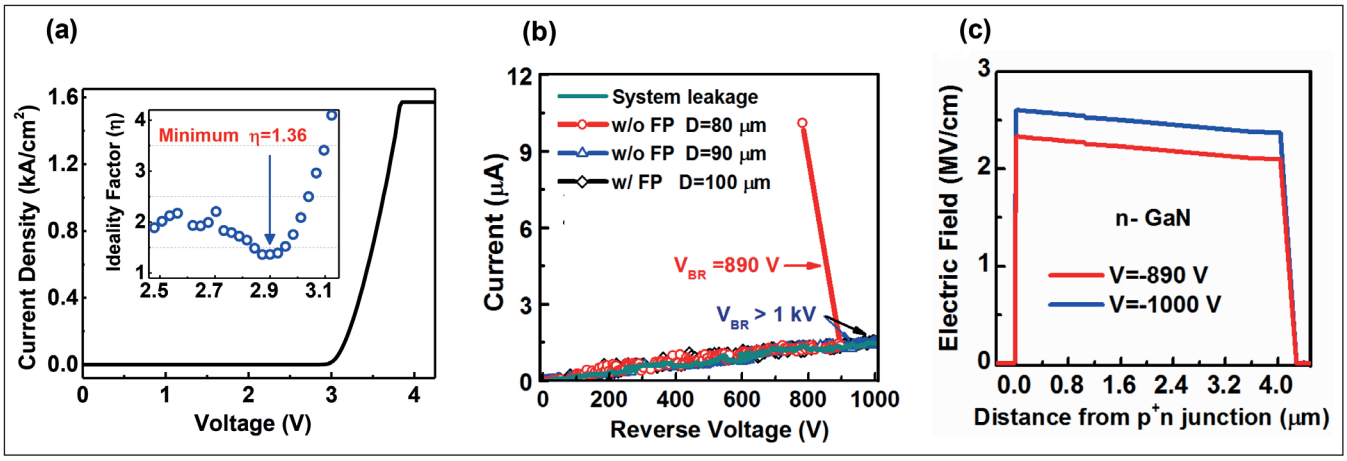
Optimising growth

These efforts began by optimising the growth conditions for ammonia MBE to enable a thick drift layer with a low level of unintentional doping, realised with a reasonably high growth rate. To uncover conditions for this, we carried out a systematic study with a Veeco 930 reactor using sapphire and free-standing GaN substrates and growth rates from 0.37 μm hr^{-1} to 1.68 μm hr^{-1}. After growing our epiwafers, we processed them into diodes to extract a net background doping, using 1 MHz capacitance-voltage measurements.

From this study, we determined a monotonic increase in background doping in the unintentional doped GaN from 3.5×10^{15} cm^{-3} to 6×10^{15} cm^{-3} and then 1×10^{16} cm^{-3}, for increases in growth rate from 0.37 μm hr^{-1} to 0.6 μm hr^{-1} and then 1 μm hr^{-1}. Switching to a free-standing GaN substrate slashed the background doping, with a value of around 10^{15} cm^{-3} recorded for a growth rate 1.4 μm hr^{-1} (see



➤ Figure 4. (a) Schematic of the fabricated ammonia MBE GaN vertical GaN-on-GaN p^+-*n* diode. (b) Atomic force microscopy image of the sidewall field plate analysis. The profile along cutline AB shows a step height of 1.4 μm and a sidewall angle of about 55°. (c) 1 MHz capacitance-voltage extracted an unintentional doping of 3×10^{15} cm^{-3} in the drift layer of the ammonia MBE GaN *p-n* diode. For more details, see IEEE Electron. Device Lett **41** 1806 (2020).



➤ Figure 5. (a) Forward current density-voltage characteristics of the ammonia MBE GaN vertical GaN-on-GaN *p-n* diode showing excellent transport behaviour with a minimum ideality factor 1.36 (inset). (b) Reverse breakdown characteristics for the ammonia MBE GaN *p-n* diodes showing that the best diodes did not show breakdown up to -1000 V (equipment limit). The leakage current of the diodes is obscured by the system leakage (c) Simulated electric field profile using TCAD that shows a punch-through electric field profile where the peak field appears at the abrupt junction interface at 0 μm with 2.6 MV cm^{-1} at 1000 V. For more details, see IEEE Electron. Device Lett **41** 1806 (2020).

Figure 1). We attribute this marked improvement to a reduced incorporation of dislocation defects, which other groups have attributed to behaving as gettering centres of donor-like oxygen impurities. Our unintentional doping level of around 10^{15} cm^{-3} is one of the lowest values reported in GaN epilayers, and about an order of magnitude lower than that for GaN grown by MOCVD.

Optimisation of the growth conditions has included improving surface smoothness. This is challenging at fast growth rates, which increase the likelihood of forming morphological and native defects, and incorporating unintentional impurities, including shallow dopants and compensating acceptors. For the growth of III-nitrides, surfactants are often used to reduce the surface roughness, with their introduction assisting adatom mobility and thus reducing native defect formation and improving morphology. It's also possible that surfactants reduce unintentional impurity incorporation.

To realise a smooth surface morphology, while adopting a fast growth rate of around 1 μm hr^{-1}, we have turned to indium as a surfactant for thick GaN epilayer growth. It's reported that the introduction of indium reduces the diffusion barrier for gallium and nitrogen adatoms to just 0.12 eV and 0.5 eV – without it, these values are 0.7 eV and 1.3 eV, respectively.

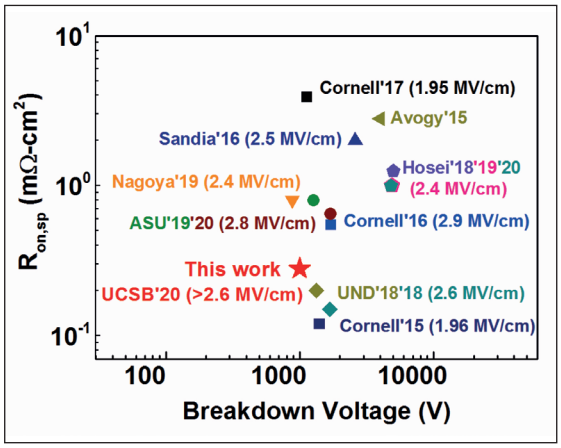
Using indium surfactants with a beam-equivalent pressure of 5×10^{-8} Torr, we have trimmed the root-mean-square surface roughness from 1.1 nm to 0.9 nm with the introduction of indium surfactants, when growing a GaN epilayer on sapphire (see Figure 2). For the same conditions, moving to a free-standing GaN substrate reduces the root-mean-square surface roughness to 0.21 nm. Another benefit of the native substrate is that it reduces the dislocation density, with that produced by Mitsubishi Chemical Corporation providing a reduction by two orders of magnitude, from around 10^8 cm^{-2} to around 10^6 cm^{-2}.

Introducing indium surfactants also improves the background doping concentration, driving it down from 2×10^{16} cm^{-3} to 5×10^{15} cm^{-3}. In addition, there is a lower silicon incorporation when using an indium surfactant, according to secondary ion mass spectrometry (SIMS) (see Figure 3). We think that the probable reason for this is indium bonding at step edges, which prevents silicon impurities from occupying dangling bonds or vacancies in the GaN surface.

Making vertical power devices

Drawing on establishing the conditions for high-quality GaN epilayer growth, we have gone on to use this expertise to produce vertical power devices. This work has taken several directions: the fabrication of vertical p^+-*n* GaN diodes with a kilovolt-range breakdown performance that use a punch-through field profile to fully utilise the low doped drift layer; the use of efficient edge termination to mitigate the high field at the p^+-*n* junction interface; deployment of high-quality contact layers to support a low contact resistance; and the use of optimal fabrication techniques to mitigate process-induced damage.

Working towards these directives, we employed ammonia MBE to grow a p^+-*n* GaN diode on a Lumilog free-standing GaN substrate. This device incorporated an unintentionally doped GaN layer grown at 0.6 μm hr^{-1}, as well as a 400 nm-thick p^+ GaN layer grown at 0.32 μm hr^{-1} and featuring a magnesium doping concentration of 3×10^{19} cm^{-3} to complete the p^+-*n* junction (see Figure 4 (a)). To minimise impurity incorporation from the substrate,



➤ Figure 6. Benchmark plot of the specific on-resistance versus breakdown voltage for the UCSB work and reported vertical homoepitaxy GaN *p-n* diodes from literature. The peak electric field is shown in parenthesis. For more details, see IEEE Electron. Device Lett **41** 1806 (2020)

we grew a buffer under our device that's about 250 nm thick, and silicon-doped at a concentration of 1×10^{19} cm^{-3}. Our epistructure also contained a 10 nm-thick, p^{++} GaN cap layer, with magnesium doping at a concentration of 3×10^{20} cm^{-3}. We produced our full epilayer structure, consisting of p^{++} cap/p^{+} layer/*n*-drift layer/n^{+} buffer, using uninterrupted ammonia MBE growth under a gallium-limited condition.

From this epiwafer we fabricated circular p^{+}-*n* GaN diodes with an 80 μm to 100 μm diameter, a Pd/Pt anode and a backside ohmic Ti/Au cathode. We realised edge termination with a side-wall angle (55°) field-plate (see Figure 4 (b)). By using an angled field plate, rather than a steep vertical field plate (90°), we gradually smoothed the crowded electric field at the p^{+}-*n* junction interface. We obtained this sidewall angle, with an etch depth of around 1.4 μm, using an optimised dry etch with an inductively coupled plasma, followed by a wet etch with potassium hydroxide. The wet etch for 25 minutes also helped minimise dry etch-induced damage. To provide additional passivation of the etched sidewall, we turned to atomic layer deposition, adding a 26 nm-thick layer of Al_2O_3 at 300°C. This oxide layer protected the device layers during subsequent deposition of a Si_3N_4 layer around 205 nm-thick, added by plasma-enhanced CVD. This layer served as the field-plate dielectric.

Electrical measurements on our diodes revealed outstanding characteristics. The extracted doping from 1 MHz capacitance-voltage profiles is 3×10^{15} cm^{-3} (see Figure 4 (c)), in line with the SIMS-detected background silicon concentration, while compensating carbon was below the SIMS detection limit of 10^{16} cm^{-3}, underscoring the purity of the ammonia MBE of GaN.

The high quality of the epilayer ensured excellent forward-transport properties. Under forward bias, our diodes exhibit a minimum ideality factor of just 1.36 – that's among the lowest reported for vertical *p-n* GaN diodes – and a specific on-resistance of only 0.28 mΩ cm^{-2} (see Figure 5 (a)).

Operating under reverse bias, the breakdown voltage exceeds our measurement limit of 1 kV, while diodes without edge termination had a breakdown voltage of 890 V (see Figure 5 (b)). According to Silvaco TCAD simulations, there is a punch-through electric field profile at a reverse bias of 1000 V with a peak electric field of more than 2.6 MV cm^{-1} located at the p^{+}-*n* junction interface (see Figure 5 (c)). It's worth noting that this kilovolt-range performance is realised with a significantly thinner drift layer of around 4 μm – that's less than half the thickness of that required for vertical homoepitaxial GaN *p-n* diodes grown by MOCVD (see Figure 6).

Future directions

By combining efficient field management and low-damage processing techniques, to the best of our knowledge we have broken new ground by demonstrating the first GaN vertical *p-n* high-power diodes grown by ammonia MBE that can operate in the kilovolt range. Key to our success is our combination of the growth of an ultra-clean thick drift layer, a fast growth rate, and a smooth surface morphology.

Building on our success, which has showcased ammonia MBE as a premier growth technique for future GaN high-power devices, we have started to investigate aluminium-rich AlGaN and AlN films on AlN template substrates. These efforts have involved single-composition AlGaN layers as well as graded-composition AlGaN all the way down to GaN. This work is laying the foundation for exploring AlGaN/GaN transistors, AlGaN power diodes, and superjunction devices. All will certainly benefit from the excellent material quality achieved by ammonia MBE.

* The current affiliation for Esmat Farzana is the Department of Electrical and Computer Engineering, Iowa State University

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Transforming the current density of AlN Schottky barrier diodes

Introducing a graded layer in AlN Schottky barrier diodes increases their maximum current density by three orders of magnitude

ENGINEERS from North Carolina State University and Adroit Materials have raised the bar for the current density of AlN Schottky barrier diodes by three orders of magnitude.

The team's diodes, capable of operating at a current density of more than 5 kA cm^{-2}, feature a highly doped $Al_{0.75}Ga_{0.25}N$ contact layer and a lightly doped AlN drift layer. It's a combination that can create an electron barrier at this interface – but is avoided by adding a compositionally graded layer, key to enabling a far higher forward current.

By delivering a dramatic increase in the current density of AlN Schottky barrier diodes, the team is helping these devices to fulfil their tremendous promise. This class of diode has the potential to serve in high-voltage, direct-current power transmission and locomotive drive systems, where it could offer a breakdown voltage of more than 10 kV. Note that thanks to a breakdown field that's greater than 16 MV cm^{-1} and a high electron mobility, AlN has a Baliga figure of merit more than 30 times that of GaN or SiC, enabling AlN devices with blocking voltages in the 10 kV range to have drift layers just a few microns thick.

Crucial to the fabrication of a high-performance device is an ohmic contact, realised with a quasi-vertical structure featuring a heavily-doped AlGaN layer as the contact layer.

To assess the impact of the AlN/AlGaN interface on the maximum forward current, the engineers carried out simulations using Silvaco TCAD software.

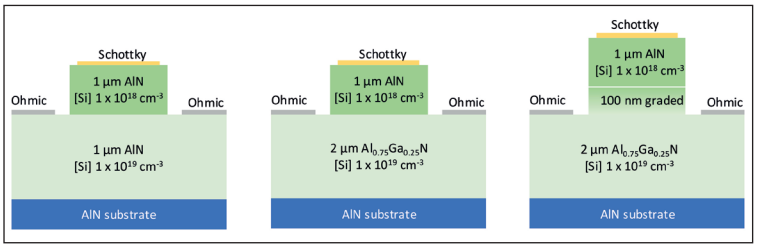
This modelling revealed that when there is an abrupt heterojunction, a sharp discontinuity is present in the band structure that introduces a barrier for electrons flowing from AlGaN to GaN. When operating under forward bias, this electron barrier is reverse biased and acts as a nonlinear series impedance. Inserting the compositionally graded layer eliminates the electron barrier.

Proof of the benefit of introducing the compositionally graded layer is provided by measurements on devices with and without this feature. Three different devices were fabricated: a control with a homoepitaxial AlN contact layer, another with an abrupt heterojunction, and a third with a graded layer heterojunction (see Figure).

All three variants were produced by loading Hexatech single-crystal AlN substrates with an average dislocation density of 10^3 cm^{-2} into an MOCVD chamber. After depositing an AlN-based stack on the substrate, the team processed the resulting epiwafers by photolithography and reactive-ion etching to form circular mesas, with electron-beam evaporation adding ohmic contacts.

Electrical measurements on these devices, which had radii ranging from 25 μm to 300 μm, revealed current scaling with the Schottky contact area for radii up to 50 μm. For radii larger than this, current density decreases with increasing device area.

Plots of room-temperature current-voltage characteristics determined an ideality factor of no more than 1.2, and an on-off ratio in excess of 10^{11}. This led the team to conclude that they had produced high-quality Ohmic contacts.



The team also found that the device with the graded-layer hetero-junction produced a current that's a factor of 10^3 higher than that with the abrupt junction, and 10^4 higher than the control.

AlN-based Schottky diodes with the abrupt and graded hetero-junctions were also investigated with impedance spectroscopy. Plots uncovered a bias-dependent feature in the diode with the abrupt junction that's attributed to the electron barrier. As this bias-dependent feature is not seen in the graded hetero-junction diode, the team concluded that this measurement offers further evidence for the hike in maximum current density stemming from either the reduction or removal of the electron barrier.

Despite the lack of edge termination to aid field management, the breakdown voltage of the diode is as high as 680 V, corresponding to a maximum electric field of 12.3 MV cm^{-1}.

➤ Introducing a graded-layer hetero-junction increases the forward current density of the diode by three or more orders of magnitude.

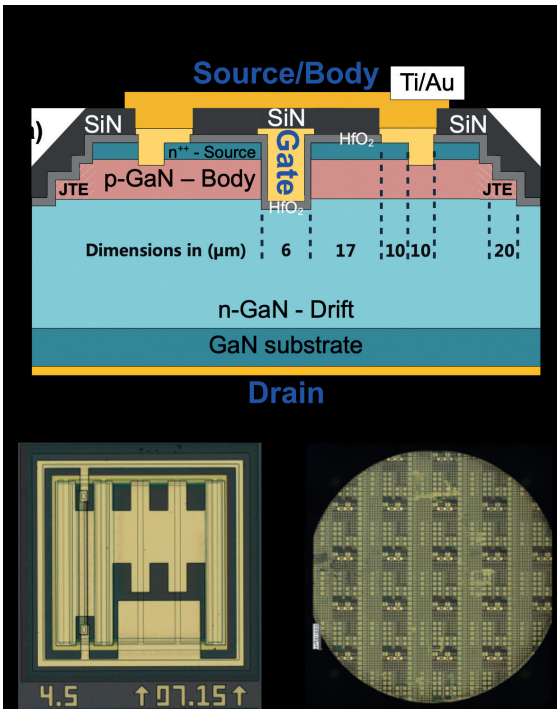
REFERENCE
➤ C. E. Quiñoes *et al.* Appl. Phys. Express **17** 101002 (2024)

Turbocharging the GaN MOSFET with a HfO_2 gate

Introducing a HfO_2 gate dielectric by atomic layer deposition trims leakage current, boosts breakdown voltage, and cranks up the output power density

RESEARCHERS from Sandia National Laboratories, Albuquerque, have delivered a dramatic improvement in the performance of vertical GaN MOSFETs through the introduction of a HfO_2 gate dielectric.

This team's 1.2 kV MOSFET delivers an output current density of 330 mA mm^{-1} – that's more than ten times that of the highest values reported for 1.2 kV-class GaN and SiC MOSFETs – alongside record-setting performance for HfO_2 on GaN demonstrating a leakage current that's just 0.5 nA at 2 MV cm^{-1}, and a breakdown strength of 5.2 MV cm^{-1}.



➤ GaN trench MOSFETs deliver a ten-fold hike in output current density with the introduction of a HfO_2 gate dielectric.

Team spokesman, Andrew Binder, told *Compound Semiconductor* that for many years it has been assumed that high-κ dielectrics, such as HfO_2, are not suited to wide bandgap semiconductors, due to the low band offset and an associated leakage current.

"This work demonstrates that given the right conditions it is possible to get low leakage and good film properties, despite the low band offset," claims Binder, adding: "This also poses an interesting question, if it can be done on GaN, could it be done on SiC?"

Binder and his co-workers believe that the biggest contributor behind the hike in current density is the higher permittivity of the dielectric, which ensures a decrease in channel resistance. "Compared to SiC MOSFETs with an SiO_2 insulator, our HfO_2-gated MOSFET has a factor of five increase in permittivity."

When the impact of a higher permittivity is considered alongside additional factors, such as a higher channel mobility and a channel length that's shorter than SiC D-MOSFETs, one can start to explain the ten-fold hike in current density. This could be a game-changer in the power electronics industry, where there is much demand for 650-1200 V SiC MOSFETs from makers of electric vehicles.

In this voltage class, channel resistance is a significant limitation to device performance, so the substantial reduction realised by the Sandia team could enable a significant competitive advantage for chipmakers that incorporate their technology.

"Another consideration is that a significant reduction in on-resistance means that for the same current rating each die becomes smaller, which means the cost-per-die decreases, as there are now more die per wafer," adds Binder.

He and his co-workers produced their devices by loading an *n*-type free-standing GaN substrate from Mitsubishi Chemical Corporation into an MOCVD reactor and depositing a 12 μm-thick drift layer, followed by a 0.5 μm-thick *p*-body and a 0.25 μm-thick source layer. Etching followed to define the trench, body and junction termination extension. Prior to addition of the gate dielectric, the team prepared the surface with ozone treatment and a piranha clean, and activated dopants via annealing.

The team turned to a Savannah S100 reactor operating at 150 °C to deposit a 100 nm-thick layer of HfO_2, using 960 atomic layer deposition cycles, before adding source, gate and drain contacts.

Electrical measurements on vertical GaN MOSFETs revealed a current density of 330 mA mm^{-1} at a drain bias of 5 V, and a positive threshold bias of 3.5 V. Specific on-resistance is 8 mΩ cm^2, but could fall to just 1.1 mΩ cm^2 by scaling the cell pitch from 70 μm to 10 μm.

Binder and co-worker are keen to explore the possibility of replicating their success with HfO_2 on a SiC transistor. "Vertical gallium nitride is still a relatively immature platform for device development," says Binder, who points to a very mature, established commercialisation path for SiC MOSFETs. "If we can demonstrate HfO_2 on SiC successfully, then we have a quicker path to market than we do with vertical GaN."

REFERENCE
➤ A.Binder *et al*. Appl. Phys. Lett. **17** 101003 (2024)

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