PEW
POWER ELECTRONICS WORLD
CONNECTING THE GLOBAL COMMUNITY

SOLiTHOR disruptive lithium solid-state battery technology

imec

ISSUE III 2022

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

POWERELECTRONICSWORLD.NET

INSIDE

SUPER DEVICES IN SILICON CARBIDE

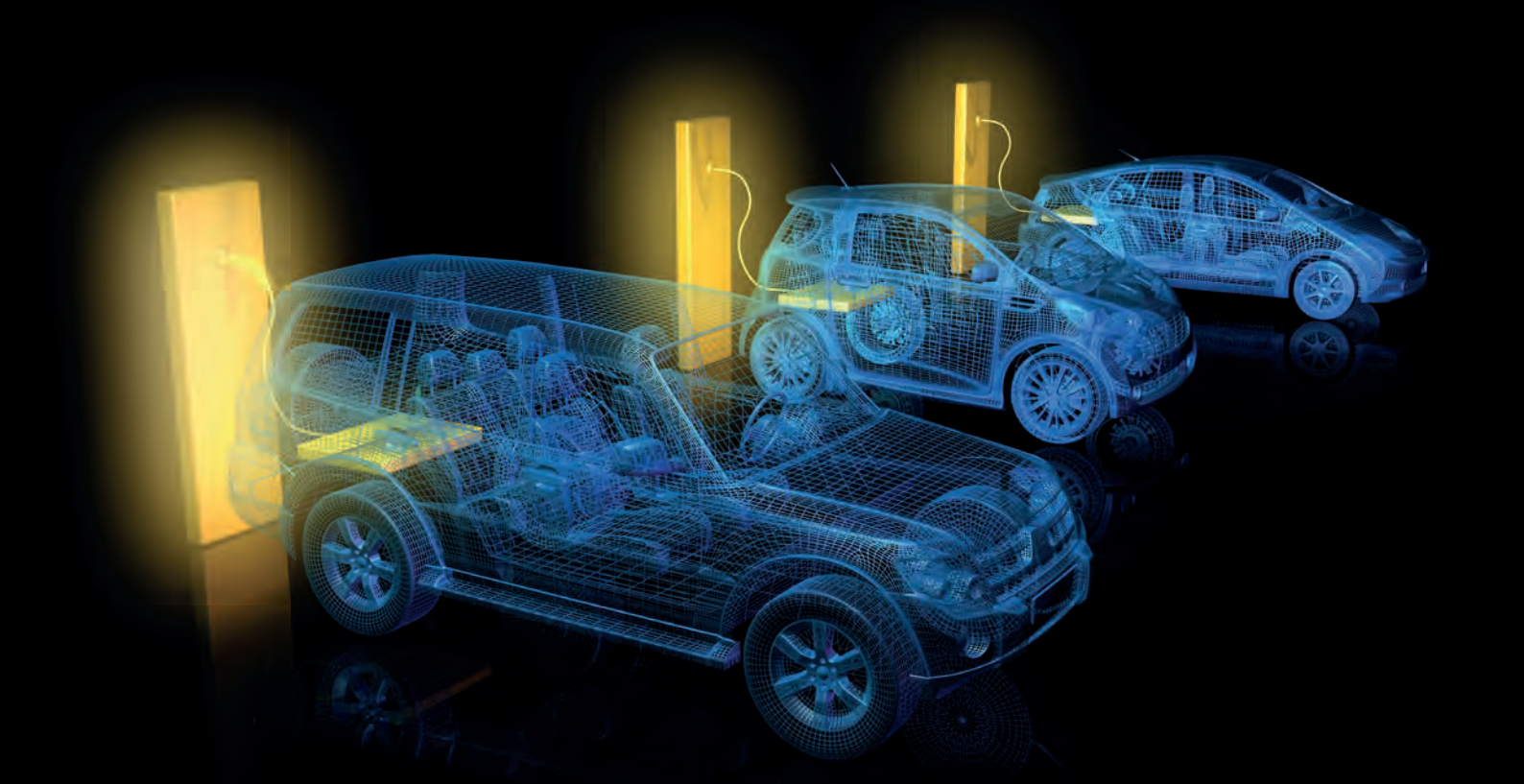
Armed with a clever charge-balance structure, SiC power devices are pushing beyond their limit

SOITEC'S SMARTSIC SUBSTRATES

SmartCut SiC is poised to revolutionise production of power electronics for electric vehicles

NEW GROUND WITH THE HYBRID TRANSISTOR

Uniting the low on-resistance of GaN HEMTs with the non-destructive breakdown of SiC diodes



Best performance for next generation SiC power electronics to address global mega trends

AIX G5 WW C

- Electric vehicles: on board chargers, power inverters
- Infrastructure: charging stations
- Renewables: solar and wind
- Industrial: motor drives, power supplies
- Power distribution: HVDC

Discover our SiC epi production *batch tool* with *single wafer* performance

Made in Germany

AIXTRON

info@aixtron.com
www.aixtron.com

VIEWPOINT

By Mark Andrews Technical Editor

New & improved technologies make waves in 2022

TRUISMS tell the tale: publish or perish; grow or go; innovate or stagnate. Business mantras abound, but consider that how we perceive any technology is based at least in part on its newness; its usefulness, cost or availability aren't always top-of-mind. Stony castles can be 'old' and still loved, but not so with tech. 'Old' tech equals 'obsolete' to many, even if not true. In this Power Electronics World we focus on new products and innovation within established technologies that boost performance, lower costs and expand market opportunities.

First up is our cover feature article on SOLiTHOR, a spin-off from the EnergyVille innovation hub backed by Belgian research giant imec. We spoke with SOLiTHOR's CTO, Dr. Fanny Bardé, after the new company received €10 million in seed money to commercialize its technology. SOLiTHOR is unique in that the company focuses on solid-state batteries that equal or exceed the performance of existing Lithium chemistries yet without the drawbacks commonly associated with today's Li-ion tech.

Easily capturing the title as most-improved is a Silicon Carbide innovation from Soitec. The company's new approach extends the 'reusability' of single crystal SiC by 10 times while also providing 10 times better conductivity. The company's SmartCut SiC is poised to revolutionise the production of power electronics for electric vehicles (EVs) and industrial applications. In another SiC focused feature, we look at a clever charge-balance structure enabling superjunction circuits to be utilized in many different SiC devices. And in a final SiC-focused article we explore the soaring market potential opportunities for Silicon Carbide. Its maturation in transport, energy and industrial applications is creating huge growth opportunities for well-positioned players.

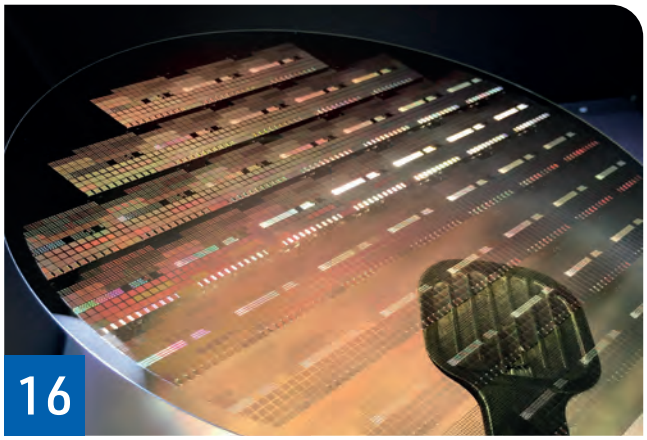
The successful and unique approach to power conservation and energy usage in sensory networks is explored in an article from Semtech detailing how the latest LoRa standards and protocols are enabling networks to push power conservation to new limits. No less exciting is the new LoRa Long Range-Frequency Hopping Spread Spectrum (LR-FHSS) protocol that extends the range of LoRa networks to realise better data collection over much greater distances, even in battery-powered wireless sensor nodes that can now efficiently collect data from satellites in low earth orbit (LEO).

PEW POWER ELECTRONICS WORLD

12

SOLITHOR DEVELOPS DISRUPTIVE LITHIUM SOLID-STATE BATTERY TECHNOLOGY

While SOLiTHOR isn't as well known as the EnergyVille innovation hub backed by Belgian research giant imec, the newly funded energy storage company is set to change the way we think about lithium-based chemistries



16

NEWS

PEW POWER ELECTRONICS WORLD

Technical Editor
Mark Andrews
mark.andrews@angelbc.com
+44 (0)1291629640

Contributing Technical Editor
Richard Stevenson
richard.stevenson@angelbc.com
+44 (0)1923 690215

Sales & Marketing Manager
Shehzad Munshi
shehzad.munshi@angelbc.com
+44 (0)1923 690215

Sales Executive
Jessica Harrison
jessica.harrison@angelbc.com
+44 (0)2476 718209

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Publisher
Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

CEO Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

CTO Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

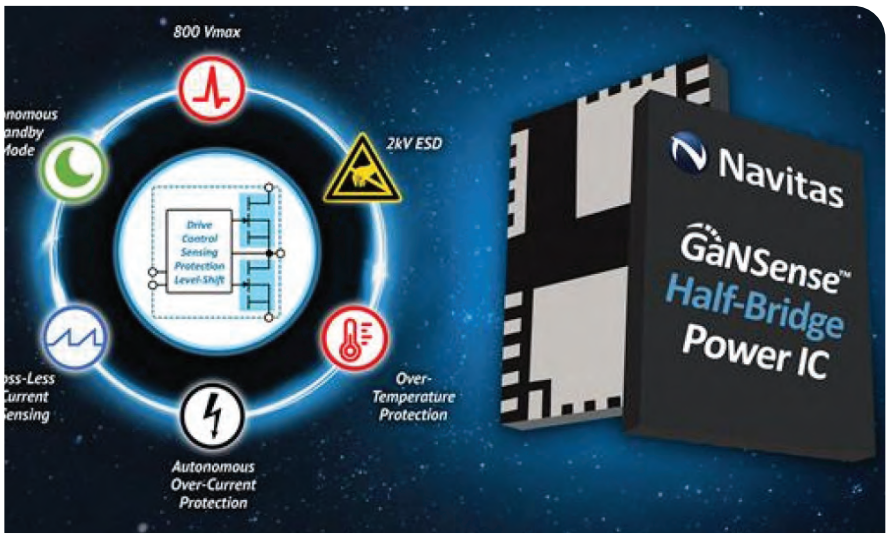
Published by
Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com

Angel BUSINESS COMMUNICATIONS

Navitas announces next gen half-bridge power ICs

Half-bridge power ICs deliver MHz performance with over 60 percent reduction in components and circuit size

GaN SPECIALIST Navitas Semiconductor has announced its first GaNSense half-bridge power ICs. According to the company, these devices enable a new level of MHz switching frequencies while dramatically reducing the system cost and complexity compared to existing discrete solutions.



GaNSense half-bridge power ICs integrate two GaN FETs with drive, control, sensing, autonomous protection, and level-shift isolation, to create a fundamental power-stage building block for power electronics. This revolutionary single-package solution reduces component count and footprint by over 60 percent compared to existing discretes, which cuts system cost, size, weight, and complexity. The integrated GaNSense technology enables high levels of autonomous protection for increased reliability and robustness, combined with loss-less current sensing for higher levels of efficiency and energy savings. Navitas says the high integration levels also eliminate circuit parasitics and delays, making MHz-frequency operation a reality for a broad range of AC-DC-power topologies including LLC resonant, asymmetric half-bridge (AHB), and active-clamp flyback (ACF). The GaNSense half-bridge ICs are also a good fit for totem-pole PFC, as well as motor-drive applications.

Gene Sheridan, CEO said. “Our initial GaNFast ICs enabled an increase from 50-60 kHz to 200-500 kHz, and now the GaNSense half-bridges elevate those benefits to the MHz range. The GaN revolution continues!”The initial family of GaNSense Half-Bridge ICs includes the NV6247 which is rated at 650 V, 160 mOhms (dual), and the NV6245C, rated at 275 mOhms (dual), both in an industry-standard, low-profile, low-inductance, 6 x 8 mm PQFN package.

The NV6247 is immediately available in production with 16-week lead times, while the NV6245C is sampling to select customers and will be broadly available in production to all customers in Q4 2022.

Magnachip unveils third-generation 200V MOSFETs

MAGNACHIP SEMICONDUCTOR has introduced its third-generation 200V Medium Voltage (MV) MOSFETs for Light Electric Vehicles (LEV) motor controllers and industrial power supplies.

To maximise energy efficiency in power devices, Magnachip’s new 200V MOSFETs incorporate it’s third-generation trench MOSFET technology. The capacitance was reduced by 50 percent compared to the previous generation 100V MV MOSFET and the enhanced design of the core cell and termination helps lower $RDS_{(on)}$ and total gate charge to achieve a high figure of merit.

In addition, these third-generation MOSFETs are available in surface mount device TO-Leadless Package (TOLL), M2PAK and TO-220 of a through-hole type respectively to reduce product size and enhance heat dissipation. Furthermore, the energy efficiency of these MOSFETs is greatly increased by fast switching and high power density. Coupled with a guaranteed operating junction temperature from -55°C up to 175°C and a high level of avalanche ruggedness, these MOSFETs are well-suited for LEV motor controllers and industrial power supplies requiring high efficiency and stable power supply.

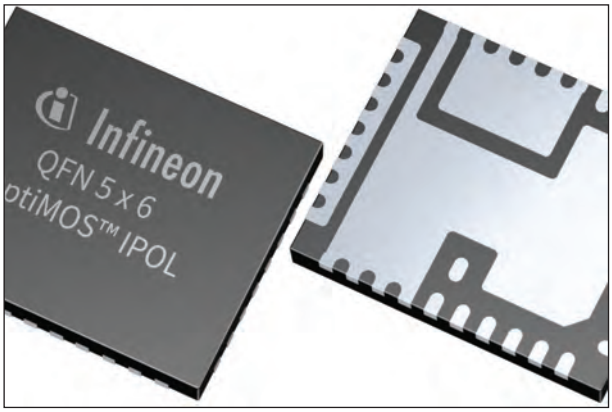
“The development of advanced applications in the automotive and industrial sectors is driving the need for high-performance MV MOSFETs,” said YJ Kim, CEO of Magnachip.

Infineon launches next-gen OptiMOS buck regulators

New integrated devices are aimed at server, storage, telecom, and datacom applications, as well as distributed power systems

INFINEON TECHNOLOGIES has introduced a new family of OptiMOS 5 IPOL buck regulators with VR14-compliant SVID standard and I²C/PMBus digital interfaces for Intel/AMD server CPUs and network ASICs/FPGAs.

Housed in a 5 x 6 mm² PQFN package, these devices are said to be an easy-to-use, fully integrated, and highly efficient solution for next-generation server, storage, telecom, and datacom applications, as well as distributed power systems.



The OptiMOS IPOL single-voltage synchronous buck regulator TDA38640 supports up to 40 A output current. The device comes with Intel SVID and I²C/PMBus digital interfaces and can be used for Intel VR12, VR12.5, VR13, VR14, IMPVP8 designs, and DDR memory without significant changes to the bill of materials (BOM).

Infineon's TDA38740 and TDA38725 digital IPOL buck regulators support up to 40 A and 25 A output current, respectively and come with a PMBus interface.

All three new devices use Infineon's proprietary fast constant on time (COT) PWM engine to deliver industry-leading transient performance while simplifying the design development. The onboard PWM controller and OptiMOS FETs with integrated bootstrap diode make these new devices a small footprint solution with highly-efficient power delivery.

In addition, they provide the required versatility by operating in a broad input and output voltage range while offering programmable switching frequencies from 400 kHz to 2 MHz. A multiple time programming (MTP) memory allows customisation during design and high-volume manufacturing, significantly reducing design cycles and time-to-market. They also offer a digitally programmable load line that can be set via configuration registers without external components, resulting in a simplified BOM.

The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the on-chip memory.

EPC introduces 100V 3.8mΩ GaN FET

Expanded family of packaged GaN FETs offers footprint-compatible solutions

Efficient Power Conversion (EPC) introduces the 100 V, 3.8 mΩ EPC2306 GaN FET, offering higher performance and smaller solution size for high power density applications including DC-DC conversion, AC/DC chargers, solar optimizers and microinverters, motor drives, and Class D Audio.

It isdesigned for 48 V DC-DC conversion used in high-density computing applications, in 48 V BLDC motor drives for e-mobility and robotics, and in solar optimisers and microinverters, and Class D Audio.

The EPC2306 GaN FET offers a super small RDS(on), of just 3.8 mOhm, together with very small QG, QGD, and QOSS parameters for low conduction and switching losses. The device features a thermally enhanced QFN package with exposed top and footprint of just 3 mm x 5 mm, offering an extremely small solution size for the highest power density applications. The EPC2306 is footprint compatible with the previously released 100 V, 1.8 mOhm EPC2302. The two footprint compatible devices allow designers to trade off RDS(on) vs. price to optimise solutions for efficiency or cost by dropping in a different part number in the same PCB footprint.

"The EPC2306 combines the advantages of 100 V GaN with an easy to assemble QFN package without sacrificing performance," said Alex Lidow, CEO and co-founder of EPC. "Designers can use our family of packaged GaN FETs to make lighter weight battery-operated BLDC motor drives for eMobility and drones, higher efficiency 48 V input DC-DC converters for data center, datacom, artificial intelligence, and other industrial and consumer applications."

Development Board

The EPC90145 development board is a 100 V maximum device voltage, 45 A maximum output current, half bridge featuring EPC2306 GaN FET. The purpose of this board is to simplify the evaluation process to speed time to market. This 2" x 2" (50.8 mm x 50.8 mm) board is designed for optimal switching performance and contains all critical components for easy evaluation.

The EPC2306 is priced at $3.08 each in 1 Ku volumes. The development board is priced at $200.00 each.

Designers interested in replacing their silicon MOSFETs with a GaN solution can use the EPC GaN Power Bench's cross-reference tool to find a suggested replacement based on their unique operating conditions.

New doping technique boosts GaN efficiency

US researchers use selectively doped GaN materials to create Junction Barrier Schottky (JBS) diodes

ENGINEERING RESEARCHERS at North Carolina State University (NCSU) have created new high-power electronic devices that are more energy efficient than previous technologies. The devices are made possible by a unique technique for doping GaN in a controlled way.

In a paper published in 2021, the researchers outlined a technique that uses ion implantation and activation to dope targeted areas in GaN materials. In other words, they engineered impurities into specific regions on GaN materials to selectively modify the electrical properties of the GaN only in those regions.

In their new paper, 'Vertical GaN Junction Barrier Schottky Diodes with Near-ideal Performance using Mg Implantation Activated by Ultra-High-Pressure Annealing' published in Applied Physics Express. the researchers have demonstrated how this technique can be used to create actual devices. Specifically, the researchers used selectively doped GaN materials to create Junction Barrier Schottky (JBS) diodes.

"Many technologies require power conversion – where power is switched from one format to another," says Dolar Khachariya, the first author of a paper on the work and a former PhD student at North Carolina State University. "For example, the technology might need to convert AC to DC, or convert electricity into work – like an electric motor. And in any power conversion system, most power loss takes place at the power switch – which is an active component of the electrical circuit that makes the power conversion system.

"Our work here not only means that we can reduce energy loss in power electronics, but we can also make the systems for power conversion more compact compared to conventional silicon and SiC electronics," says Ramón Collazo, co-author of the paper and an associate professor of materials science and engineering at NC State.

"This makes it possible to incorporate these systems into technologies where they don't currently fit due to weight or size restrictions, such as in automobiles, ships, airplanes, or technologies distributed throughout a smart grid. Power rectifiers, such as JBS diodes, are used as switches in every power system," Collazo says. "But historically they have been made of the semiconductors silicon or SiC, because the electrical properties of undoped GaN are not compatible with the architecture of JBS diodes. It just doesn't work.

"We've demonstrated that you can selectively dope GaN to create functional JBS diodes, and that these diodes are not only functional, but enable more power efficient conversion than JBS diodes that use conventional semiconductors.

For example, in technical terms, our GaN JBS diode, fabricated on a native GaN substrate, has record high breakdown voltage (915 V) and record low on-resistance.

"We're currently working with industry partners to scale up production of selectively doped GaN, and are looking for additional partnerships to work on issues related to more widespread manufacturing and adoption of power devices that make use of this material," Collazo says.

The work was supported primarily by ARPA-E as part of its PNDIODES program. The work received additional support from the US National Science Foundation, the Office of Naval Research Global's Naval International Cooperative Opportunities in Science and Technology program, and Poland's National Center for Research and Development (NCBR).

Flexible power modules simplify SiC inverter designs

ST's latest modules contain 1200V SiC MOSFETs in popular configurations

STMICROELECTRONICS has released two STPOWER modules that contain 1200V SiC MOSFETs in popular configurations. Each uses ST's ACEPACK 2 package technology to ensure high power density and simplified assembly.

The first of the new modules, the A2F12M12W2-F1, is a four-pack module that provides a convenient and compact full-bridge solution for circuits such as DC/DC converters.

Another module, the A2U12M12W2-F2, employs a three-level T-type topology to combine high conduction and switching efficiency with consistent output-voltage quality.

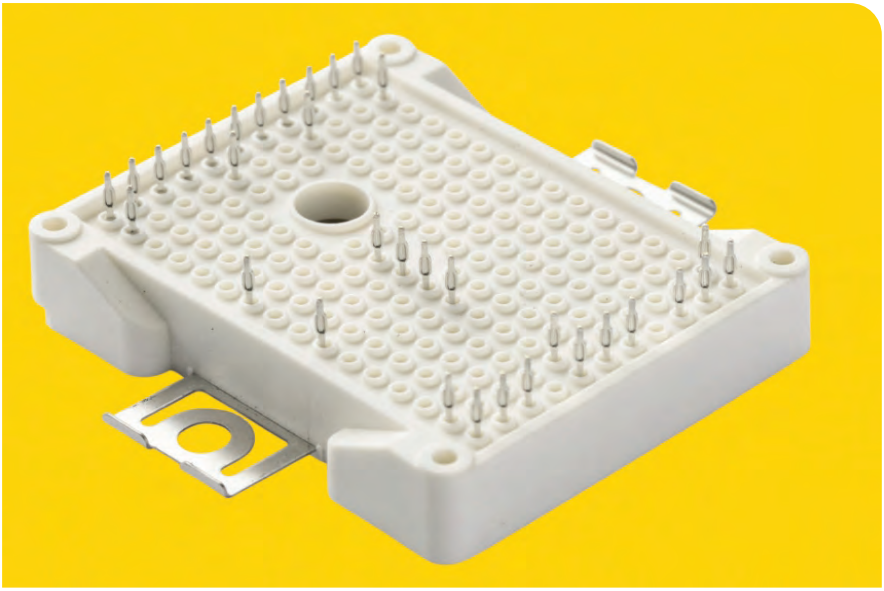
The MOSFETs in these modules leverage ST's second-generation SiC technology, which has an outstanding RDS(on) x die-area figure of merit to ensure high current-handling capability with minimal losses. With 13mΩ typical RDS(on) per die, both full-bridge and T-type topologies tackle high-power applications and ensure excellent energy efficiency with simplified thermal management due to low dissipation.

The ACEPACK 2 package has compact dimensions and ensures high power density, with an efficient alumina substrate and direct bonded copper (DBC) die attachment.

The external connections are press fit pins that simplify assembly in potentially harsh-environment equipment such as electric vehicles (EVs) and power conversion for charging stations, energy storage, and solar energy.

The package provides 2.5kVrms insulation and contains an integrated NTC temperature sensor that can be used for system protection and diagnostics.

The modules are in production now and the unit price is $235.20 for both the A2F12M12W2-F1 four-pack configuration and the A2U12M12W2-F2 three-level T-type inverter.



Allegro MicroSystems buy-out

ALLEGRO MICROSYSTEMS has announced the completion of its previously-announced acquisition of Heyday Integrated Circuits, a privately held French company specialising in compact, fully integrated isolated gate drivers that enable energy conversion in high-voltage GaN and SiC wide-bandgap (WBG) semiconductor designs.

This acquisition brings together Heyday's isolated gate drivers and Allegro's market leading isolated current sensors to enable some of the smallest high-voltage and high-efficiency power systems available on the market today.

Additionally, this acquisition is expected to increase Allegro's addressable market for electric vehicles (xEV), solar inverters, datacenter and 5G power supplies, and broad-market industrial applications.

"The demand for simplified power management is increasing across the board, and high-voltage isolated gate drivers are fundamental for enabling technology for the future of high-efficiency power system designs," said Joe Duigan, senior director, Engineering and Business Development.

"Together with Allegro's market leading current sensors and Heyday's isolated gate drivers we will be able to power the increasingly popular GaN and SiC MOSFET driven systems."

"We're thrilled to welcome Heyday to the Allegro family," said Vijay Mangtani, VP of Power ICs at Allegro. "This acquisition will greatly accelerate our efforts to deliver a market leading energy efficient technology platform for high-voltage designs in advanced mobility, clean energy, and motion control solutions.

HITACHI
Inspire the Next

SiC RoadPak – New levels of power density

No matter if high torque requirement in vehicles, efficient charging for e-busses and e-trucks or smallest footprint within train converters is needed, Hitachi Energy's new generation of e-mobility SiC power semiconductor modules are the best choice.

Hitachi Energy

Imec spin-off SOLiTHOR has developed disruptive Lithium solid-state battery technology

While SOLiTHOR isn't as well known as the EnergyVille innovation hub backed by Belgian research giant imec, the newly funded energy storage company is set to change the way we think about lithium-based chemistries. After SOLiTHOR's announcement of its €10 million seed funding in May, Power Electronics World technical editor **MARK ANDREWS SPOKE WITH SOLiTHOR CTO, DR. FANNY BARDÉ,** about what sets her company apart from others and why their new tech can change the way we store and use energy.

THE FIRST HALF of 2022 was especially important to SOLiTHOR, a new energy storage company spun-off from Energyville by the imec research consortium. SOLiTHOR raised €10 million in a seed investment round led by imec.xpand that was also supported by an investment syndicate including LRM, Nuhma and FPIM. According to SOLiTHOR, the proceeds will be used to refine and commercialize the technology required to enable further development of its revolutionary new energy storage approach that while based in part on Lithium chemistries it avoids the commonly known drawbacks of lithium-ion batteries now available.

➤ SOLiTHOR Chief Technology Officer,Dr. Fanny Bardé

One factor that sets SOLiTHOR apart from other battery developers and manufacturers is the focus on solid-state batteries. SOLiTHOR's developers intend to bring the performance of classical Lithium battery systems to the next level in terms of energy density, charging speed, weight and volume. Over the past decade, imec has invested in new technology to further enhance the performance of solid-state batteries, whilst proposing components enabling an assembly process that is more compatible with classical Li-ion battery manufacturing processes.

When the €10 million seed funding was announced in May, co-founder and SOLiTHOR CEO, Huw Hampson-Jones, remarked that, "SOLiTHOR's technology is unique and is based on breakthrough chemistry and components (including) the nano-Solid Composite Electrolyte and the nano-anode, spearheaded within the EnergyVille labs and patented by imec. This revolutionary technology will improve energy density, charging speeds and crucially, increase safety; it will be far easier to manufacture than other solid-state batteries."

Hampson-Jones also stated that in addition to continuing work with imec's research and development team, SOLiTHOR's ongoing development programme will be led by co-founder and Chief Technology Officer (CTO), Dr. Fanny Bardé, a seasoned expert in battery technology. Power Electronics World technical editor Mark Andrews spoke with Bardé following the company's announcements to discover what distinguishes SOLiTHOR's technology from that of other energy storage companies and how SOLiTHOR expects to change the storage paradigm to help increase longevity, density and cost-effectiveness.

MA: *SOLiTHOR describes its key technology as a 'nano-Solid Composite Electrolyte (nano-SCE)'. Can you elaborate on how this technology differs from*

others now available or in development?

FB: "Usually, ion diffusion in solids is much slower than in liquids. In fact, for many years, it was considered impossible to engineer solid-state materials with ionic conductivities that exceed the ones of liquid type electrolytes. However, SOLiTHOR expects to achieve this. The composite electrolyte comprises a nanoporous SiO2 matrix filled with an organic Lithium-salt which is organized along the pore walls of the oxide matrix to create 'highway' conduction paths for fast Lithium-ion transport. Consequently, the nano-SCE transports Li-ion and presents highly attractive Lithium conductivity in the range of 1-10mS/cm at room temperature - a value on a par with conventional liquid type electrolyte conductivities. However, unlike conventional liquid electrolytes used in Li-ion battery technology, the nano-Solid Composite Electrolyte is a solid electrolyte.

MA: *A major issue with present Lithium-based battery technologies is the fact that anodes and cathodes can break down over time or under other conditions and form dendrites. How is SOLiTHOR's technology safer?*

FB: "SOLiTHOR's cell technology is safer for two reasons. First, the nano-SCE is not based on flammable solvents and the nano-anode features will elude dendrites formation. Secondly, unlike some sulfide electrolytes, our nano-SCE does not react and form H2S, a dangerous gas, when it is in contact with water. Competitive technology using sulfides will need to apply extra safety features during cell manufacturing and operation to avoid possible safety issues linked to H2S formation. (SOLiTHOR) technology also has environmental advantages in that the battery cell's CO2 footprint is projected to be lower than one of a conventional liquid type Li-ion battery."

MA: *Are there other advantages that you can discuss at this point in time?*

FB: "SOLiTHOR cells will be lighter and more compact. In addition, we do not apply large external pressure on the cells to reach high performances. Other solid-state systems need to apply (especially sulfide-based or oxide-based solid-state batteries), huge pressure to assemble the cell components and/or during cell operation. SOLiTHOR cells will require moderate to low pressure, resulting in a lighter, more compact technology at the cell and module and pack levels. Employing liquid precursors that solidify 'in situ' into the composite cathode allows SOLiTHOR to re-use 100 percent of current composite cathode manufacturing lines. Further enhancing the process by impregnating the solid electrolyte into the cathode makes our technology simpler than other solid- state technology, such as Lithium-ion solid-state batteries."

➤ CTO Dr. Fanny Bardé measuring electrode thickness in one of the company's R&D labs

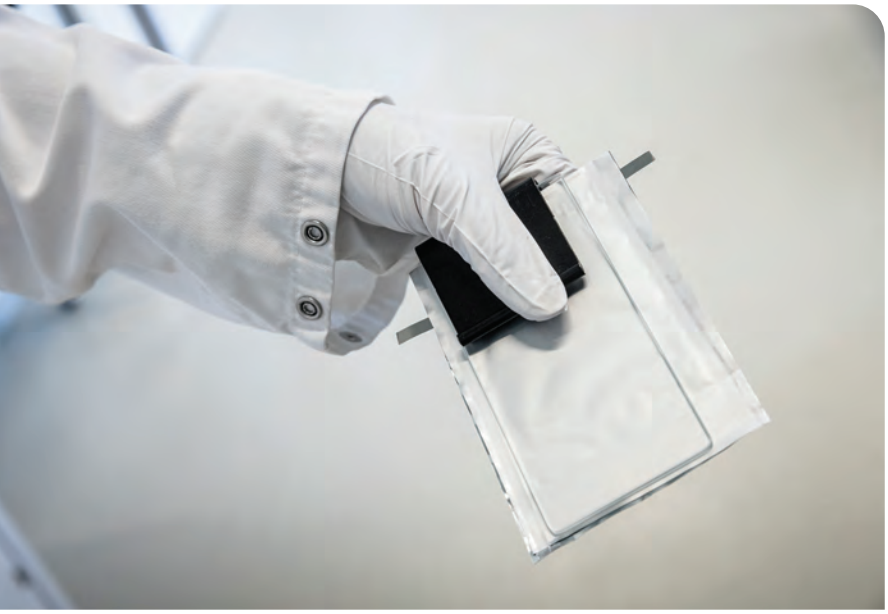
MA: *Another advantage that your company has cited in its public discussions of the technology is the fact that SOLiTHOR is 'drop-in' compatible with existing batter manufacturing technologies—could you elaborate?*

FB: "As well as its high Li-ion conductivity, our solid composite electrolyte can be applied using conventional wet processing techniques. Other solid-electrolytes with similar Li-ion conductivities are synthesized in powder-form and need high-temperature sintering and/or high-pressure techniques during cell integration, requiring an expensive rebuild of cell production lines. SOLiTHOR's cell fabrication requires no such disruption. But keep in mind that converting from one manufacturing process to another is not simple. That said, we envisage the adoption of our solid-state electrolyte technology to be simpler than the adoption of other solid-state electrolytes based on sulfides or oxides.

MA: *Today's typical Lithium-ion batteries employ a battery management system (BMS) to ensure safe charging and operation. Will SOLiTHOR's technology require the same?*

FB: "All cell formats, whether cylindrical, prismatic or pouch and all chemistries (Li-ion and post Li-ion) have proven to perform better when a Battery Management System controls the operation of the cells including those cells within a module or pack—a BMS provides better performance, in a safer way during a longer lifetime. Our technology is no different (in that regard) and will also have an appropriate BMS. Cell balancing within a module and pack is crucial for all technologies.

MA: *SOLiTHOR specifically calls out automobile applications of its technology. Can you dive into the advantages SOLiTHOR offers for transport?*



A prototype cell incorporating SOLiTHOR's unique technology designed to increase performance and eliminate the drawbacks of conventional Lithium-ion cells

FB: "Our ambition is to develop safer battery cells than the ones currently used in electric vehicles (EVs.) Our aim is to deliver cells with both higher energy density (Wh/L) and higher gravimetric energy (Wh/kg), whilst not compromising on safety. Our cells will be cathode agnostic, which means that both our nano-SCE and nano-anode will be compatible with all conventional cathode materials, including Lithium Ferro Phosphate (LFP) technology. Collaborating with our customers, SOLiTHOR will define the best cathode material for a specific application."

MA: *Another advantage of SOLiTHOR technology is that its batteries can be developed and manufactured within Europe, using component materials that come wholly or mainly from within Europe – Is SOLiTHOR trying to become independent of Asian manufactures that currently dominate the battery manufacturing sector?*

FB: "Yes, correct. SOLiTHOR is developing its technology in Europe. It will also be manufactured in Europe. That said, SOLiTHOR is an export driven company and will not exclude cross licensing its technology. We are already discussing partnerships with key industry players worldwide. SOLiTHOR's ambition is to develop a new, improved, sustainable battery technology in Europe. By freeing Europe from its dependency on battery technologies that are largely manufactured in Asia, SOLiTHOR will also decrease CO2 emissions. Cells will be produced close to where they are used. SOLiTHOR aims to play a key role within the European battery value chain, adhering to the European Commission's closed loop battery system."

MA: *Can the company please outline where it is within the overall product development lifecycle and progress towards bringing its products to market?*

FB: "The nano-SCE technology, combined with LFP cathode material has already been demonstrated into a small format pouch cell by imec, the Belgian international research and development organization. SOLiTHOR will further develop this technology by:

- Increasing the Technology Readiness Level (TRL) of the nano-anode
- Demonstrating the nano-SCE and nano-anode together in a first cell demonstrator
- Upscaling the components
- Incorporating the components into a prototype cell of relevant capacity
- Performing tests on end user vehicles to achieve expected Key Performance Indicators (KPIs)

MA: *Can you estimate when SOLiTHOR technology might appear in vehicles or other consumer applications?*

FB: "Aviation is one of our key markets and we are already developing partnerships with key players in this sector. Critical testing and validation phases will take place over several years before our cells will be available for use in commercial vehicles."

MA: *Does SOLiTHOR expect the price of its cells to be comparable to that of Lithium-ion cells?*

FB: "As a result of comprehensive upscaling and production at 'Gigafactory' level, the price of Li-ion cell technology has decreased over the last ten years. With a larger adoption of solid-state technology, and economy of scale, the price of solid-state batteries will be comparable to that of conventional Li-ion battery technology.

MA: *Are there other advantages of SOLiTHOR technology that we have not discussed so far?*

FB: "The technology will have sustainability advantages. In the long term, the technology will benefit from a fully water-based process, thereby reducing or avoiding the use of solvents during cell production. Our solid electrolyte does not rely on rare earth metals such as Germanium (Ge), which is used by some of our solid electrolyte competitors."

With a larger adoption of solid-state technology, and economy of scale, the price of solid-state batteries will be comparable to that of conventional Li-ion battery technology.

SEMI AMERICAS EVENTS

Technology Leadership Series of the Americas Events

The **Technology Leadership Series** of the Americas is a collection of eight major events representing the various technology communities in our industry. These programs connect 2,400+ member companies and over 1.3 million global professionals to advance the technology and business of electronics manufacturing and the design-supply chain.

There are numerous ways for you to participate in these events to connect with the industry and grow your business.

ATTEND | PRESENT | SPONSOR | EXHIBIT

SAVE THE DATES
FOR THESE 2022 EVENTS

Explore these upcoming programs and fill out the Interest Form on each website to get connected for the latest event updates.

www.semi.org/semi-americas

semi

Superjunction sparks super devices in silicon carbide

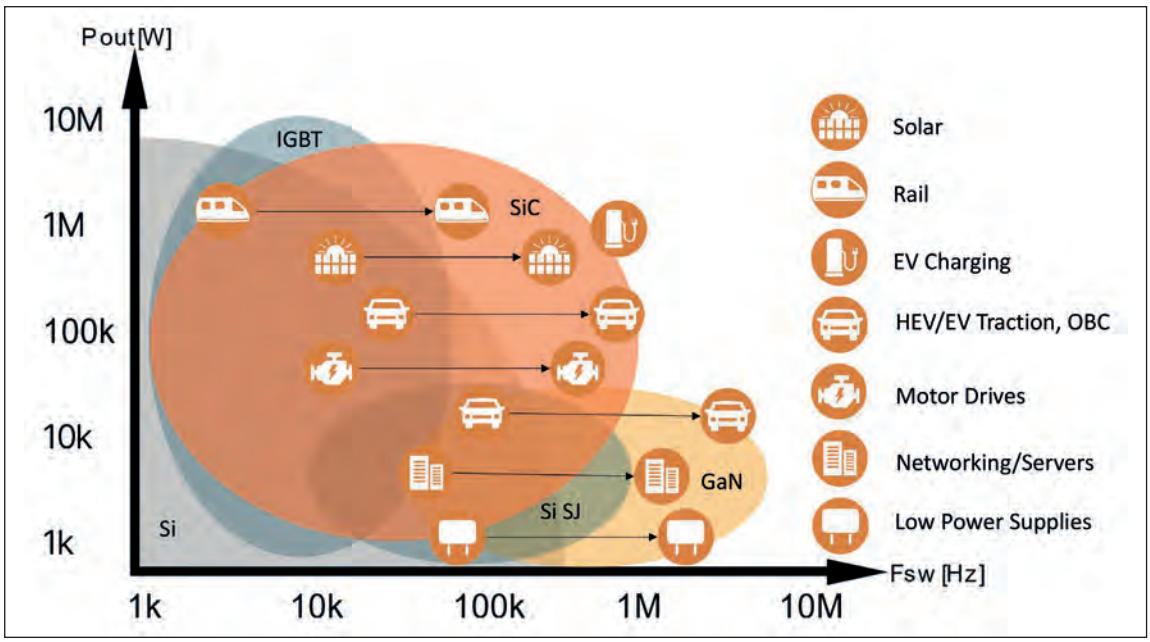
Armed with a clever charge-balance structure, SiC power devices are pushing beyond their limit

BY JAN CHOCHOL AND ROMAN MALOUSEK FROM ONSEMI

THE ENTIRE power electronics industry is buzzing with SiC activity. It's no wonder, given that SiC devices have a dielectric breakdown field strength that's ten times higher than that of silicon, as well as twice the electron saturation velocity of the incumbent, three times its bandgap, and a thermal conductivity that is better by a factor of three. All high-power applications benefit from these traits, shown in Figure 1, so it's of no surprise that vendors, fabs and OEMs are embracing the rapid adoption of SiC. All are trying to outperform, outlast and outclass their competition.

Due to all this frenetic activity, there is some turmoil in this sector, creating opportunity for all kinds of development. This has motivated our team at onsemi to explore various concepts. Against the backdrop of a maturing SiC industry, we have been able to revisit some topics that just a few years ago would be either unfeasible, too expensive or just plainly not possible with the toolset available at that time.

One such concept is the superjunction. Regardless of design, any device that is made from SiC will benefit from its unique properties. They include a large electric breakdown field that shaves tens of micrometres of epi thickness, greatly reducing the on-state resistance for a given voltage rating compared with silicon. But with the superjunction structures that we have explored, one can go a step further. Generally, this structure consists of



➤ Figure 1. Areas of application for different power electronic technologies.

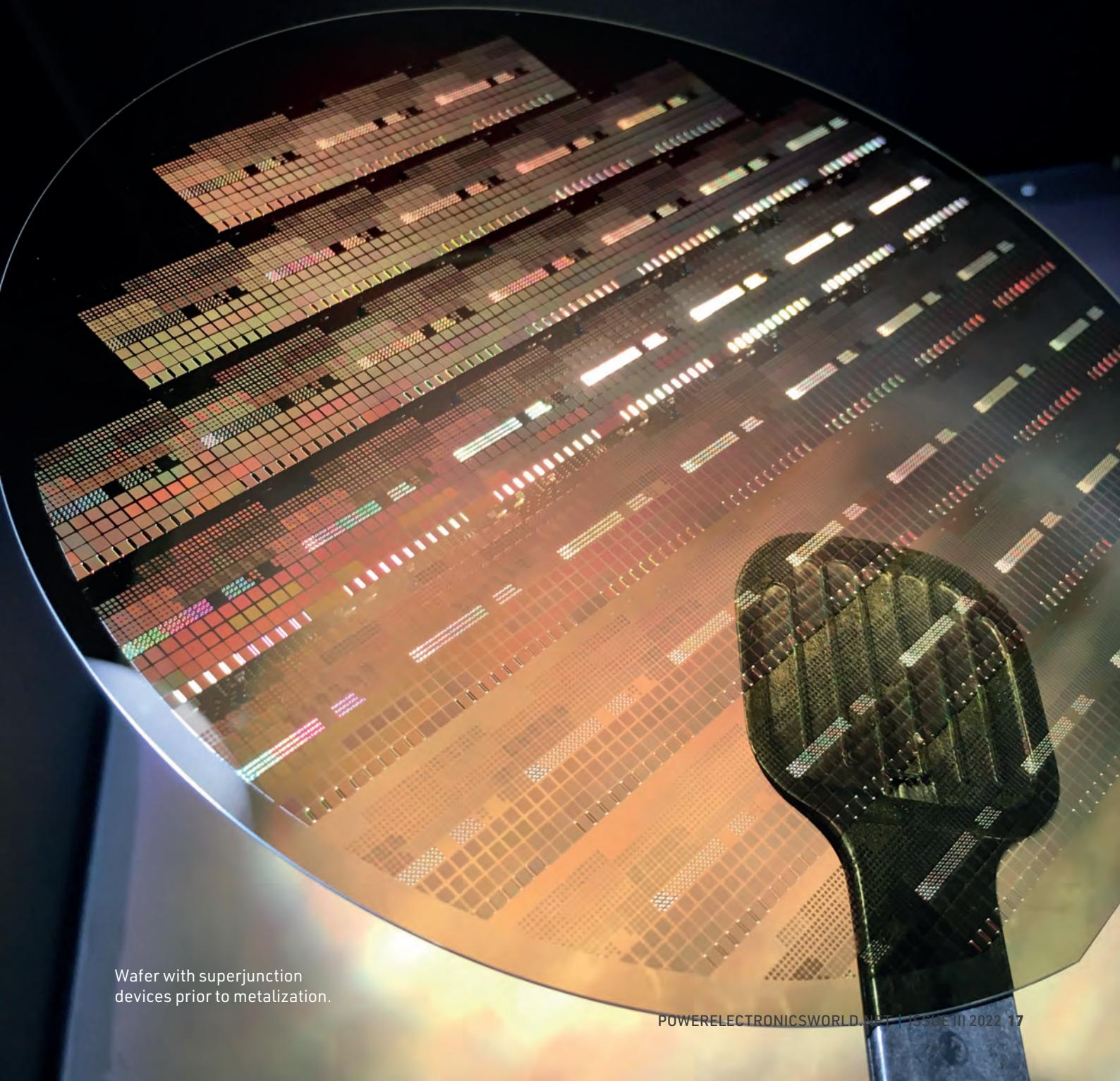
alternating regions that are highly doped, tightly spaced and with equal and opposite doping – an architecture that ensures charge balancing. With such a structure, the high doping results in superior conduction that reduces resistance. But that's not the only benefit we get – operated under reverse bias, the superjunction is fully depleted, with the electric field spread evenly in a roughly rectangular shape. Thanks to this, compared with a classical unipolar drift region, where the electric field must be trapezoidal (see Figure 2), we realise a higher breakdown field at the same drift thickness.

The real question is how can we make such a structure? We need to have defined pillars, with a controllable concentration reaching several micrometres below the surface. As each micron of superjunction depth can block about 200 V (we go on to show this), a 1200 V device needs more than 6 µm of well-controlled superjunction pillars.

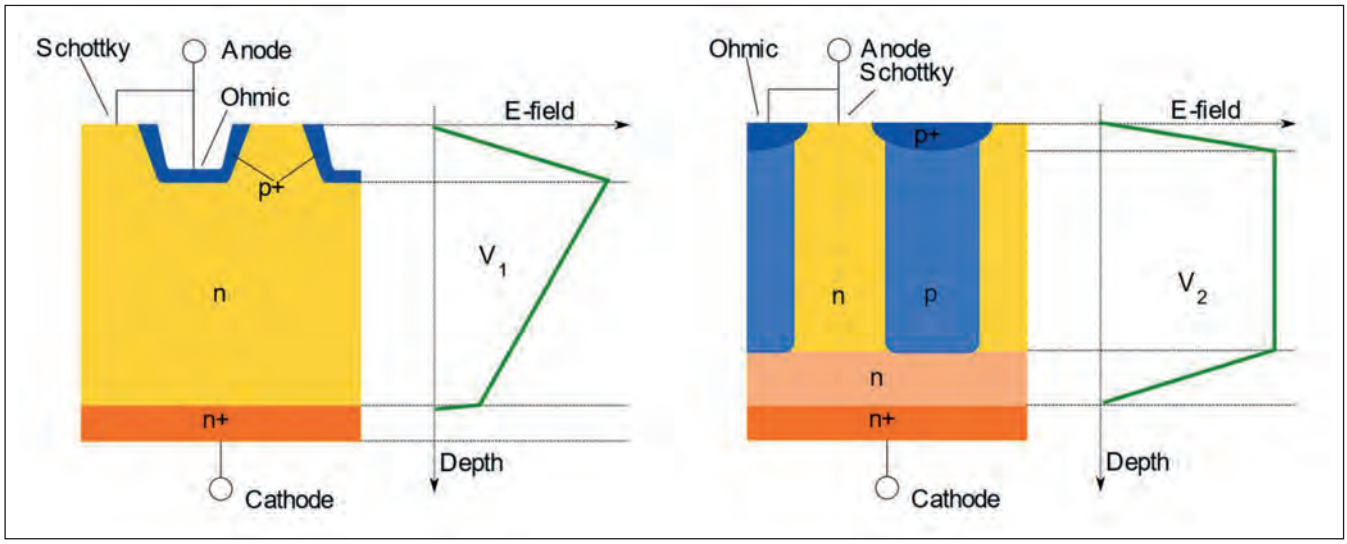
One option for forming the pillars is ion diffusion. However, those working in the SiC community don't tend to concern themselves greatly with this technique, as there is simply no way to diffuse ions in SiC. This has led some groups and companies to try other approaches, such as trench filling by CVD.

Revisiting ion implantation

But in our pilot study, we decided to take another look at ion implantation, due to the simplicity of the method and the availability of tools. We



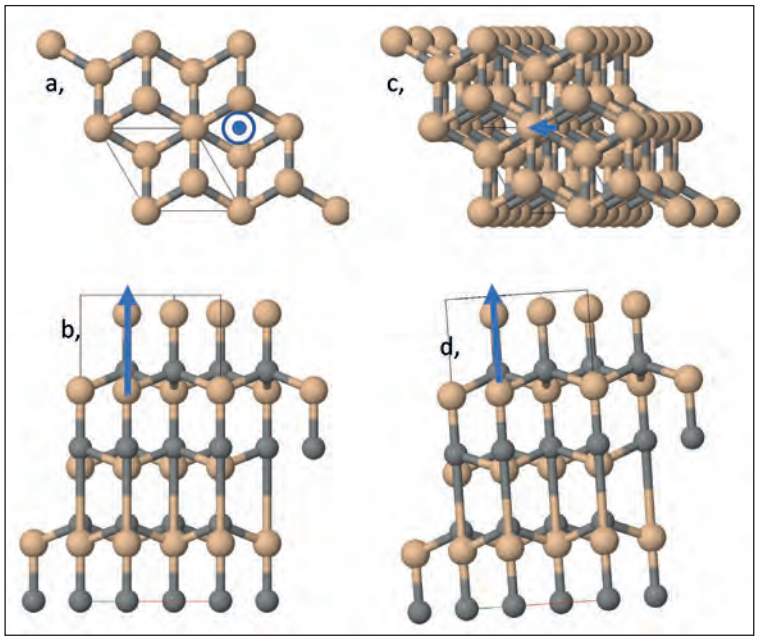
Wafer with superjunction devices prior to metalization.



➤ Figure 2. Schematic diagram of JBS diode with unipolar drift region (left) and superjunction JBS diode (right).

have investigated two different techniques. One involves using very high energy implants. Roughly speaking, this is a brute force approach; we push the implants deep into SiC, due to their high kinetic energy. Higher energy means deeper penetration. Then, using multiple implants, we can chain the concentration profile together to create a seemingly uniform distribution. The caveat of this approach is that we have to shield the other pillar from the implantation. So one implant can be blanket, while the other must be masked and have twice the dose of the other. Success is not easy, as there is only so thick a photoresist that can block the implant.

Due to this limitation, we have also explored the channelled implant. One key characteristic of the 4H polytype of SiC, used for power applications, is that it permits ion implantation along a preferential angle, where ions 'see' through the lattice and the number of ion-lattice collisions plummets. This principle, illustrated in Figure 3, leads to a concentration profile that is far deeper and flatter than that normally possible with a random implantation direction. For example, a 900 keV non-channelled implant of aluminium reaches a depth of up to 0.7 μm, while channelling with this energy extends the depth to 3 μm.



➤ Figure 3. JMOL simulation of 4H-SiC lattice. Blue arrow shows the direction of *c*-axis of the crystal. (a) view through the channelling direction; (b) sideview; (c) tilted lattice; (d) tilted lattice sideview.

With this approach we have produced pillars by combining a blanket high-energy nitrogen implantation, which does not require a mask, with a masked channelled aluminium implantation. The success of this scheme is seen in profiles obtained by secondary-ion mass spectrometry (see Figure 4).

The channelled direction is along the 0001 direction of the crystal – this is also the direction in which the crystal is grown. As most commercial SiC crystals are cut at a 4° angle, this is the channelling angle we employ. To produce well defined pillars, it's critical that the implantation tool maintains the optimal angle across the wafer and batch-to-batch. We're grateful for the support of Nissin Ion Equipment, which helped us in this endeavour during our pilot study.

Regardless of whether we employ channelling or very-high-energy implantation, an epi re-growth step is needed to get to the desired thickness. When restarting the epi process for each new pillar layer, we tuned the conditions carefully, to minimize any potential loss of implanted material (etch back) and ensure a constant concentration throughout the epi-structure. Another challenge we have faced is to tune the alignment of the masks to the alignment marks after each epi regrowth, and to renew the marks to assure a precise position of the layers that follow. For the structures formed by very high energy implantation we undertook three epilayer growth steps, each involving a deposition of a 1.2 μm-thick layer; and for the channelled run, we

used just two growths, each 2.45 µm thick. We have fabricated junction barrier Schottky diodes from both types of structure. This involved using parallel stripes as mask for the pillars. As these stripes are parallel to the wafer flat, we avoid mask shadowing when undertaking channelled implantation.

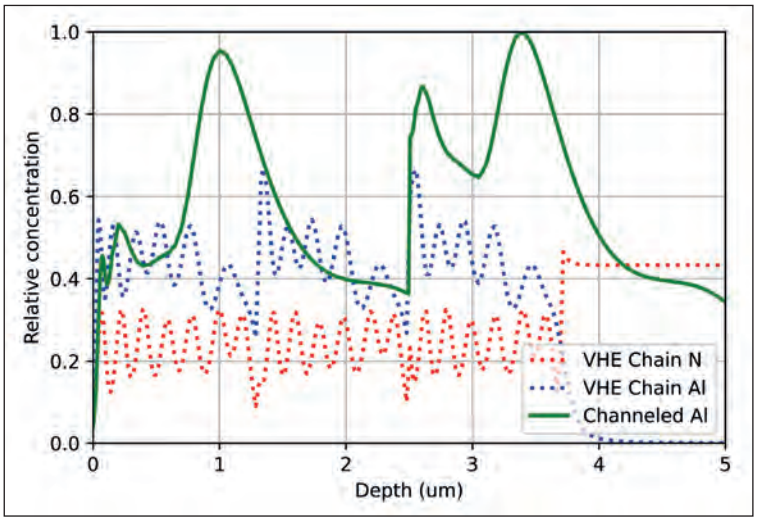
Assessing different die

To fully assess our device's behaviour, we have made both small (0.0012 cm^{-2}) and large (0.018 cm^{-2}) dies. Small dies allow us to investigate a multitude of designs, while their large siblings have properties more akin to production-line devices (the wafer with the designs can be seen in the image on p. 23).

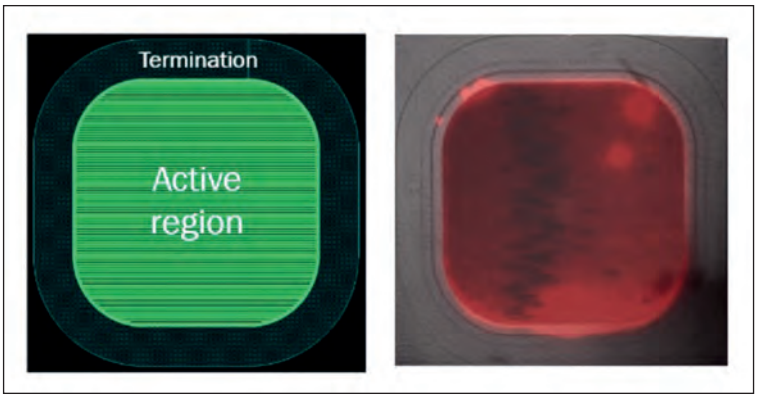
With superjunction devices, it is essential to ensure a proper charge balance. This means that both pillars have the same concentration of dopants. With any process, factors are at play that will lead to a spread in the concentration. But it is possible to address this by varying the stripe width, as this provides a mechanism to compensate and tune the design – a wider, lower-doped pillar will behave the same as a narrower, higher doped one. We implant the top of the *p*-type pillar with a shallow, high dose of aluminium to ensure a good ohmic contact.

Contacts to our devices have been made with a standard SiC process. This added a Ti/TiN Schottky/ohmic contact to the front side. We turned to a backside grind and metal deposition for the cathode contact. Our devices feature termination, used to spread the electric field and distribute the avalanche current homogeneously in an active region. We verified this had been accomplished by electroluminescence, which shows a uniform breakdown in the active structure (see Figure 5).

Before diving into the results of our superjunction study, it is worthwhile to consider our assumptions of the expected behaviour. Key characteristics are the breakdown voltage of the diode and its on-state resistance. The ideal is to have a perfect 1:1 ratio in pillar concentrations, as this ensures a maximum achievable breakdown voltage – for a given thickness of the superjunction. Meanwhile, the on-state resistance scales linearly with the *n*-type concentration, where the conduction happens (behaviour is illustrated in Figure 6).



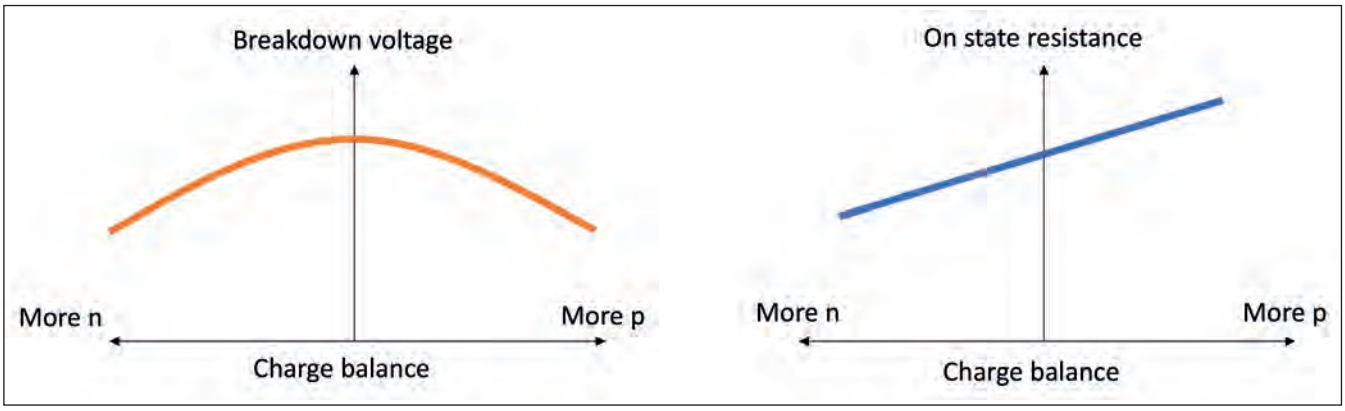
➤ Figure 4. SIMS data on implanted profiles in the superjunction experiment.



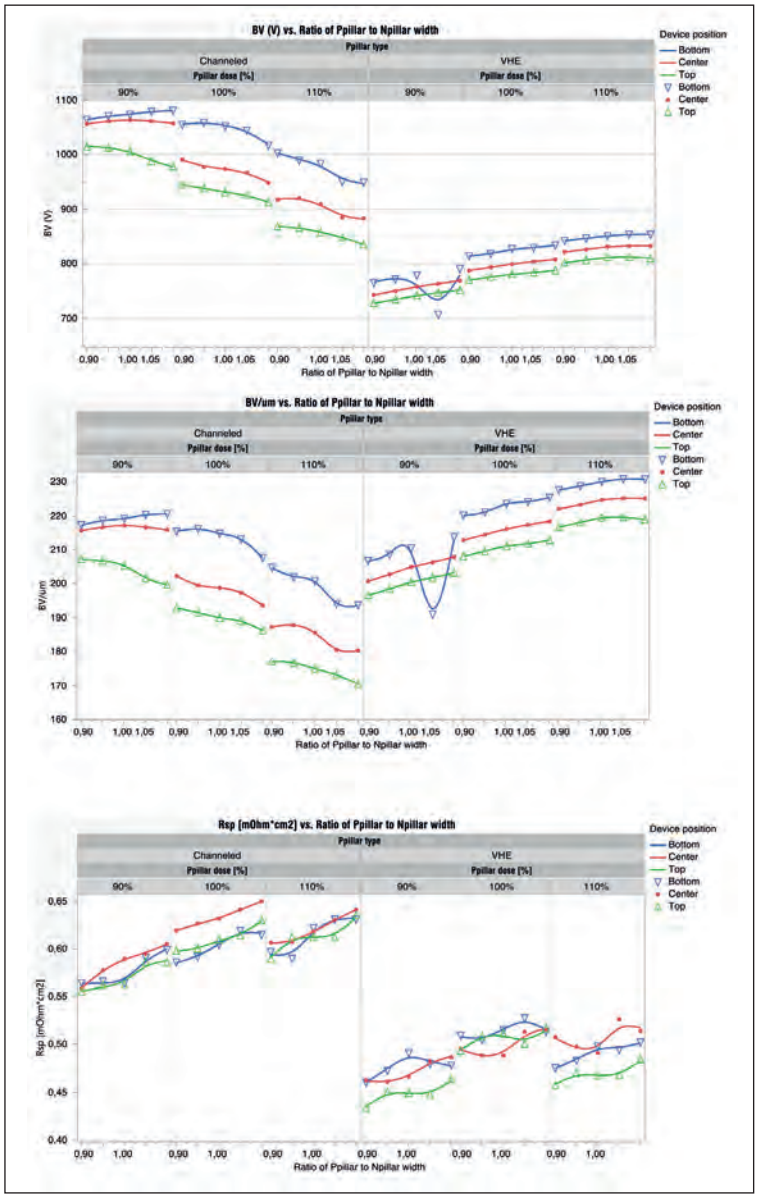
➤ Figure 5. Left: Schematic of the device design. Right: Electroluminescence of the device in the avalanche breakdown.

The actual results of our study, shown in Figure 7, confirm our assumptions. We used three wafers for each implantation scheme, each with a slightly different dose (± 10 percent), and changed pillar ratios in the device design. Our breakdown results follow a parabolic shape, with the absolute position determined by the thickness of the superjunction. Note the spread across the wafer, with a thicker epi-structure near the flat giving a higher breakdown voltage (optimizing for uniform wafer distribution

SiC devices are also sought after for their high-temperature performance, which comes in to play in almost all their applications. It is here where the superjunction puts the 'super' in devices.



➤ Figure 6. Predicted behaviour of the superjunction device.



➤ Figure 7. Electrical data from characterization of the superjunction devices characterization of the superjunction devices

was not part of the study). As expected, the on-state resistance increases with the width of the *p*-type pillar and with the epi-thickness. We have addressed the variation in the on-state resistance between the wafers to the variation of the substrate resistance.

To compare the results realised by very-high-energy implantation and channelling, we have normalized breakdown values by thickness. After omitting the epi-thickness spread, both approaches gave about 210 V/µm of breakdown. This is a crucial finding, implying that both approaches are equal, in terms of electrical performance and process stability. Where the differences lie are in the toolset needed and the number of epi steps required.

With data at hand, we can compare our devices to those with a classical architecture, including a variant with a unipolar drift region. Our evaluations, which include a plot of the one-dimensional theoretical limit of such a device, enable comparison of on-state resistance and breakdown voltage (see Figure 8). We see that with our test devices, measurements on our larger die show that we are just at the tipping point at 1000 V/0.7 mΩ cm^{-2}. Generally, the sweet spot for usage of superjunction devices is above that, in the 3 kV-5 kV region.

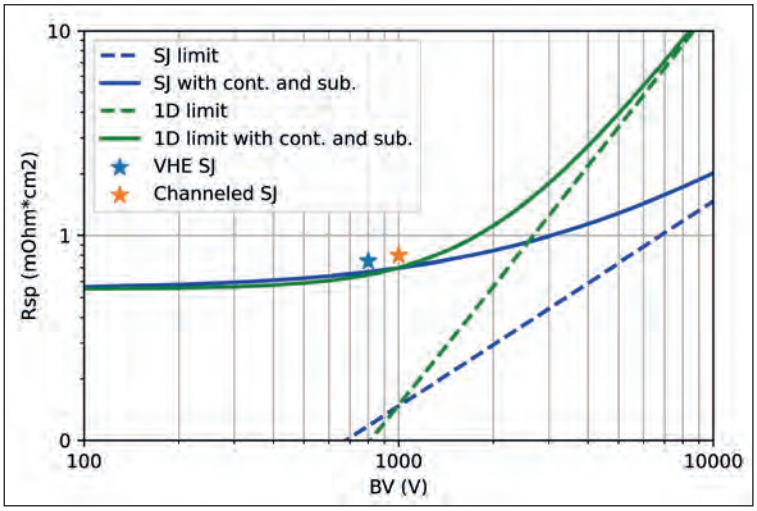
This, though, is only one side of the equation. SiC devices are also sought after for their high-temperature performance, which comes in to play in almost all their applications. It is here where the superjunction puts the 'super' in devices. The drift region, where the blocking field is spread, is the lowest doped part of the device. It is here where there is a large contributor to device resistance – but the introduction of the superjunction makes this region thinner and highly doped, changes that as we've seen pay off after 1000 V of blocking voltage. Thanks to high doping in this region, this device is less affected by a temperature-induced resistance increase. What happens is that the device maintains its low resistance even at higher temperatures. All the while the breakdown is largely unaffected. In fact, it increases, due to increased phonon scattering – more energy is needed to push electrons into avalanche. So, as we've shown, replacing the drift region with the superjunction pays

dividends, transforming an ordinary device into one that excels in highly demanding applications.

The adoption of SiC devices and their related development, including the progress reported in this study, would not be possible without scaling up the entire SiC ecosystem. Whether it is the making of substrates, involving wafering, grinding, polishing; or epitaxial growth or other front-end or backend processes; every step is a demanding operation that needs to draw on hard-earned expertise and specialized tools.

SiC initially came to us at onsemi through the acquisition of Fairchild, where device technology has ever since been developed in close cooperation between: the design center in Kista, Sweden; the device and process integration teams in Bucheon, Korea; and the engineering team at South Portland, Maine, responsible for developing SiC epi technology.

Our current role includes supporting SiC development and production in key fabs, in Bucheon, South Korea and in Rožnov pod Radhoštěm, Czechia. In Rožnov, which is a small town nestled in the Beskids mountain range, materials development is gaining much attention, recognized with an award for the most innovative company in the region.



➤ Figure 8. Trade-off curves of breakdown voltage and on-state resistance for unipolar and superjunction devices with experimental data shown

With the recent acquisition of a SiC substrate manufacturer – GT Advanced Technologies – our company has increased its level of vertical integration and solidified its SiC device portfolio. These moves have strengthened our position as a significant force in the power electronics industry and sharpened the cutting edge of SiC technology.

Gearing up for electric vehicles with Soitec's SmartSiC substrates

Offering a ten-fold reuse of single-crystal SiC and a ten times better conductivity than its conventional counterpart, SmartSiC is poised to revolutionise the production of power electronics for electric vehicles and industrial applications

BY OLIVIER BONNIN, ERIC GUIOT, WALTER SCHWARZENBACH, NOÉMIE BALLOT AND CÉLINE TRANQUILLIN FROM SOITEC

IF HUMANKIND has one task of utter urgency it is the reduction of carbon dioxide emissions. Following decades of spiralling emissions, we are now living in an age of catastrophic environmental and demographic damage, and without drastic action this situation is only going to get worse.

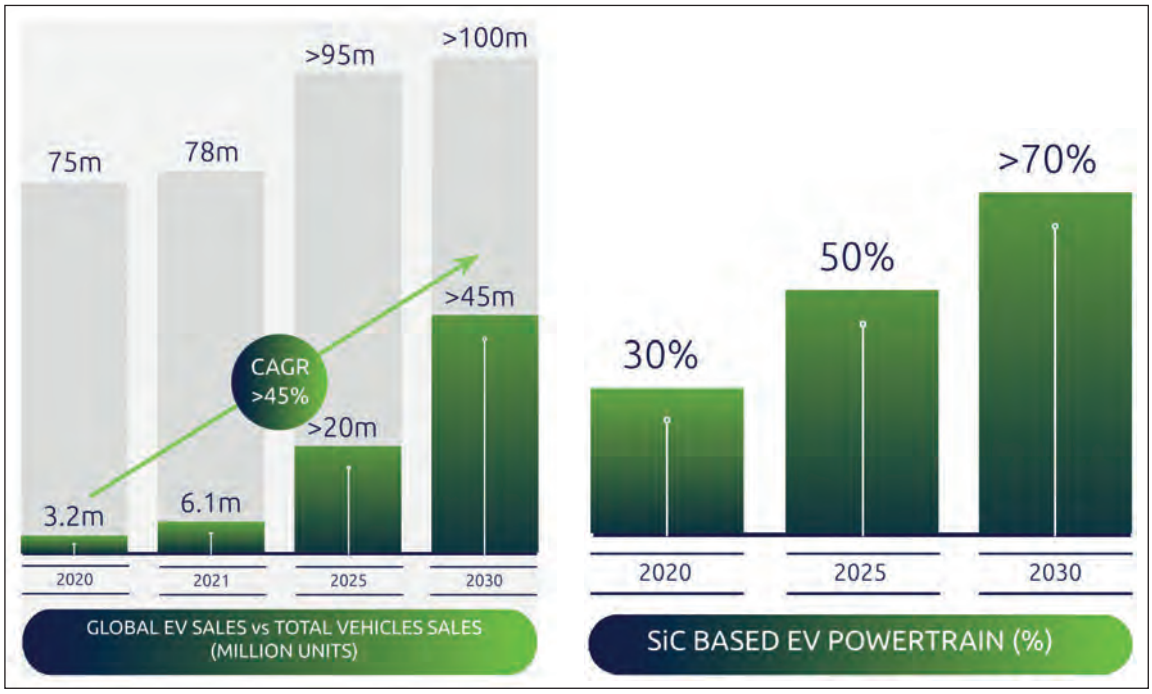
A significant share of today's greenhouse gas emissions come from transportation, traditionally a significant polluter. But this sector is embarking on a once-in-a-century transformation, driven by researchers, industries, institutions and customers – all stakeholders in the transportation ecosystem – coming together to shape a greener future. Sitting at the very heart of this industrial revolution are electric vehicles, the key driver to slashing carbon dioxide emissions associated with mobility.

Fuelling the uptake of the EV are falling prices, longer driving ranges and rapid charging times. Crucial to further advances in performance, which will spur sales to reach new heights, is the optimisation of the powertrain. It's a task attracting intense, cutting-edge R&D. In every EV the direct current from the battery is transformed into an AC form that drives the traction motors. The efficiency of the inverter that performs this function governs the efficiency of the drivetrain – increasing this is essential for improving EV performance..

Tesla, the world-famous pioneer of the EV, started introducing SiC devices into its vehicles in 2018. Since then, devices made from this wide bandgap semiconductor have been the undisputed and optimal choice for managing power conversion in drivetrains and on-board chargers. Note that the compelling case for SiC is only going to strengthen when the EV industry shifts from 400 V to 800 V systems for fast chargers. Due to this, penetration of SiC-based devices in EVs is to climb over the next decade from 30 percent to 70 percent, against a backdrop of an ever-increasing number of vehicles sold per year (see Figure 1).

With penetration of SiC-based devices and technologies climbing fast and EV sales skyrocketing in all major geographies, streamlined SiC supply chains are essential. Many power device manufacturers are fully aware of this need, and are responding with strategic moves, either investing in high-volume wafer manufacturing capabilities, or building vertical integration models and making strategic acquisitions to solidify supply chains.

While a shift to SiC may seem radical to some, the technology has in fact had an intensive maturation period with experts anticipating its arrival to the mass market for years. It's been just over 20 years since it emerged as a disruptive alternative to silicon in the power electronics industry. While chipmaking is more expensive and requires a more complex manufacturing process, this must be weighed against the increase in energy conversion efficiency. Over the last two decades, the cost of making SiC devices has fallen, partly through a migration from 25 mm wafers to ever larger diameters, with 200 mm now at the leading edge. Such gains have propelled the benefits-to-cost ratio for SiC to a level where there is no longer any discussion of whether this material is suitable for EVs. The breakthroughs have ensured that the SiC industry is an incredibly dynamic market, in terms of growth and design opportunities.



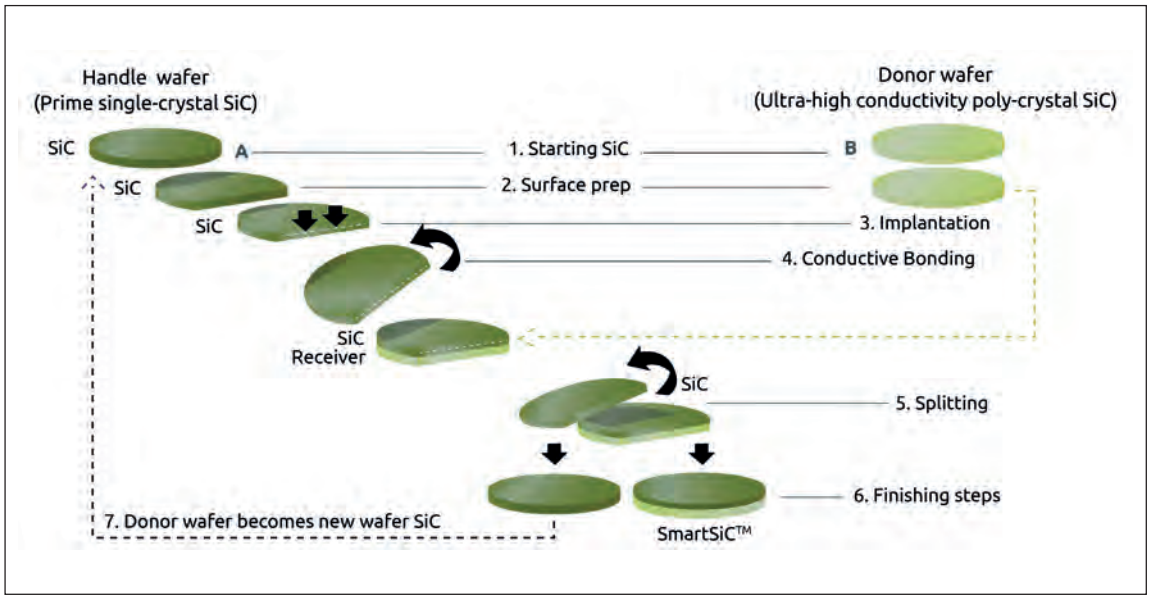
➤ Figure 1. Global EV's market trend and SiC penetration.

Yet despite all this promise and initial success, SiC has remained, until recently, a material that just serves in the high-end industrial sector, as well as other power-conversion applications. Expansion of the market has been hampered by a relatively narrow product offering from device manufacturers. There are only a few devices that have been specifically designed for EV applications, and their manufacturing yield has been compromised by the defectivity levels found in standard SiC wafers.

A physical barrier to realising a higher manufacturing yield is the range of intrinsic defects that arise during the manufacture of SiC boules using the incumbent process, physical vapour transport (PVT). These imperfections in the material prevent device manufacturers from hitting the required yield, causing chip production to be economically unviable. Yields are hampered by the large size of the chips. SiC MOSFETs with a unitary surface of at least 40mm^2 are required to ensure the handling of currents of 200 A, which are needed for the power levels of the EV traction inverter.

SmartSiC: the cutting-edge solution

Addressing this challenge is SmartSiC, the game-changing technology from Soitec. This is the latest expansion of our Smart Cut portfolio. Within this family, we ship more than 2 million wafers per year to a variety of product lines, including those for making devices for smartphones. It's a success story that has led us to be the largest pure-play supplier of engineered substrates for radio-frequency and mobile phone markets. Over the last few years we have laid the foundations to repeat that success in automotive and industrial markets with SmartSiC.



➤ Figure 2. The unique, patented Smart Cut process of Soitec, adapted to SiC material.

The strengths of SmartSiC

Christophe Maleville is CTO and SEVP Innovation, Soitec

Christophe, your SmartSiC technology is relatively young compared with SiC technology. How would you describe the maturity of SmartSiC?

CM: Soitec's SmartSiC technology is moving to the industrialization phase. We used our pilot line at CEA-Leti to develop, prototype and select a tool-of-record for high-volume manufacturing. We are now focusing on reducing variability, improving defectivity and yield, and optimizing the metrology sampling to start the high-volume manufacturing phase with an optimal process flow. We have 30 years of experience with Smart Cut in large volumes. Our advantage is that we can leverage this experience to now accelerate the maturation of our SmartSiC technology. And we are perfectly on time to get ready for manufacturing in 2023.

What level can you reach when considering product variability?

CM: Those who lead the development of SiC have done a fantastic job. They have introduced major improvements in SiC's crystal quality and diameter, and SiC devices are now already routinely powering electric vehicles that are driving on our roads. But every SiC boule and every wafer within each boule is different, bringing quite a significant variability to manufacturing. SmartSiC is lowering such variability by allowing us to use each single wafer more than ten times, thanks to our Smart Cut process. By using an epitaxy layer as a donor, I strongly believe that our next generation of SiC wafers, SmartSiC, will completely eliminate crystal-originated variability. By eliminating basal plane dislocations prior to layer transfer, every wafer sent for device manufacturing will be the same. This will be a major benefit for large-volume production and will close the gap with silicon technologies.

Can Soitec lead this revolution alone?

CM: This is indeed a revolution that will lead to major advancements in SiC device performance and metrics. But, of course, we are not doing it alone. We are collaborating with strategic partners on all fronts, from research and technology organisations to materials and equipment suppliers and leading device manufacturers. This is absolutely fundamental to accelerate the adoption of SmartSiC-based devices and the implementation of next generations. For the manufacturing of our first generation of SmartSiC wafers, which will kick off in 2023, the development cycle was extremely rapid: we went from initial development work to a volume ramp-up in only four years. This clearly demonstrates how efficient our model of close collaboration within the ecosystem is.

Drawing on 30 years of expertise with our Smart Cut process, through our SmartSiC wafers we offer a new and disruptive engineered substrate. This building block for making SiC devices introduces a new paradigm for the electrical performance of the wafer, the productivity of the supply chain, and the device power density. Merits of this engineered wafer, which creates significant value at both the device and the system level, include easing the adoption of eMobility and enabling enhancement of charging infrastructure and the renewable energy industry.

Our efforts at developing our Smart Cut technology have been driven by a team of engineers, working tirelessly at the Substrate Innovation Center of Grenoble, within CEA-Leti. Their success allows us to leverage: the exceptional physical characteristics of single-crystal SiC substrates, which are used as a donor and enable a ten times re-use capability; and an innovative, highly-electrically conductive polycrystalline substrate, acting as a handle wafer, that ensures a reduction in the device's on-resistance. We showcased our cutting-edge, high value-added engineered substrate technology last year, in issue VI of *Compound Semiconductor*. Here we go one step further, presenting the maturity of SmartSiC, the milestones towards its wide-scale adoption, and the steps we will take to drive further innovation.

Greener, faster, better

SmartSiC is a technology that is greener, faster and better in both its 150 mm and 200 mm formats. These strengths have put it on a trajectory to become one of the industry standards for the SiC market. It provides a plug-and-play solution that can seamlessly integrate into all existing power supply manufacturing lines and deliver significant commercial, environmental, and manufacturing benefits compared with traditional SiC substrates.

The greener footprint comes from the simple, energy-efficient manufacturing processes for making SmartSiC. Compared with traditional SiC, carbon dioxide emissions are reduced by up to 70 percent per wafer.

Faster deployment of these large size substrates stems from re-use of scarce, 200 mm single-crystal donors. By adopting this approach, we help to sustain market growth.

Our SmartSiC provides a better way to produce power electronics devices, by combining a superior manufacturing yield with better efficiency and a higher power density. Empowered by a higher conductivity compared with bulk SiC, SmartSiC enables an increase in current density of more than 20 percent for a range of power devices, including MOSFETs and diodes. This is the secret formula for unleashing a new generation of power devices.

We have two flavours of SmartSiC. One is SmartSiC-Performance, which is being prototyped and is moving through qualification trials with Soitec

customers. The other, SmartSiC-Advanced, provides a substrate that is free from basal plane dislocations (BPDs). This product, now in the sampling phase, is being developed by our innovation team.

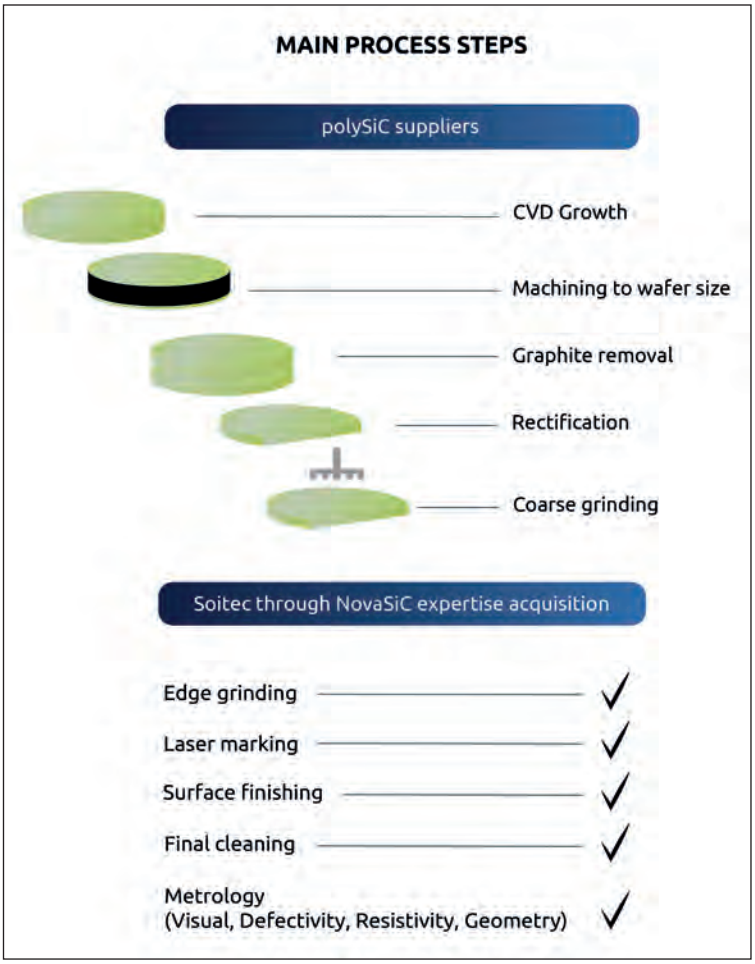
Employing an optimised design, our SmartSiC substrates feature a state-of-the-art single-crystal SiC layer that's thinner than 1 µm, on top of an ultra-high-conductivity polycrystalline SiC handle substrate. These engineered substrates, with diameters of 150 mm or 200 mm, have a total thickness of 350 µm or 500 µm, respectively. When producing a second SmartSiC wafer, we re-use the donor wafer, minus the few microns used for the first SmartSiC wafer. By repeating this process again and again, we yield a minimum of ten SmartSiC wafers per donor wafer.

The production of polycrystalline SiC, which provides a handle wafer for each SmartSiC, uses a CVD process. This is quicker and more environment-friendly than PVT, needed for high-quality single-crystal SiC wafers. Our polycrystalline SiC that we source from external suppliers has adequate doping to control the substrate's electrical conductivity while maintaining a highly competitive cost (see Figure 3). Drawing on a high level of maturity and expertise developed over many years, we are able to define and ensure the perfect geometry for our engineered SiC substrate, key for mastering the bonding of the wafers. Our acquisition of NovaSiC in November 2021 has equipped us with more than 25 years of experience in SiC wafering, strengthening our capabilities.

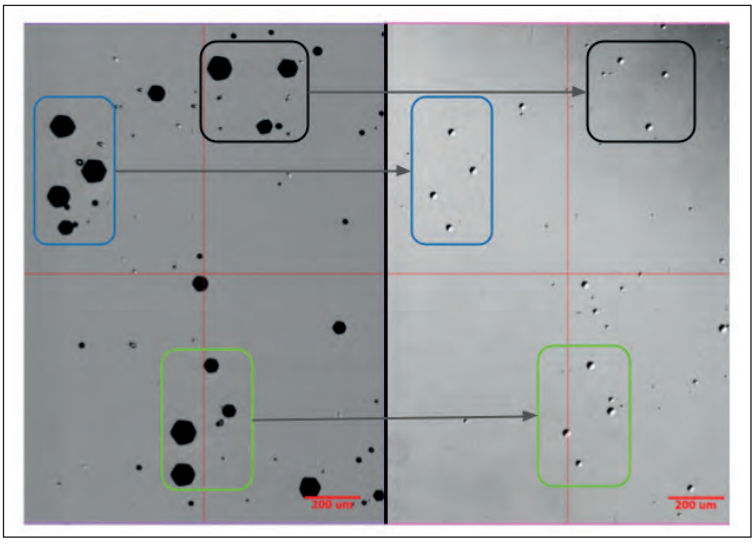
We now have a highly capable, stable process and design for our SmartSiC substrates. These wafers have been tested and prototyped intensively and at large scale; and we have confirmed the value they bring to the market, to power devices and to power systems. Measurements of MOSFETs and diodes incorporating our SmartSiC engineered substrates show significant, irrefutable performance improvements, as well as enhanced long-term reliability and high-temperature robustness. These attributes have motivated several device manufacturers to commit significant resources to adopting and implementing SmartSiC technology when qualifying their next-generation products.

Glimpsing into the R&D kitchen

A target for our R&D team is to take the manufacturing yield of SiC to the globally accepted standards applied to silicon-based power devices. This ambitious goal is within reach, thanks to the capability of the Smart Cut process to maintain the crystal quality of the incoming donor wafer. According to inspection of our engineered wafers etched with a potassium hydroxide solution, as the decorated crystal defects we observed on the donor and SmartSiC surface are at the same locations, we know that our technology does not introduce additional imperfections. To verify this and improve the defectivity level, we have performed the



➤ Figure 3. Main process steps for manufacturing polycrystalline SiC.



➤ Figure 4. Etching with potassium hydroxide enables crystal defect characterization. Decorations are easily visible with an optical microscope, allowing comparison between a single-crystal SiC donor (left) and SmartSiC (right).

Substrate	Standard 4H-mSiC	SmartSiC-Advanced
BPD density (/cm²)	~ 500	< 0.1

➤ Table 1. Basal plane dislocations and defectivity density in the donor SmartSiC-Advanced substrate.

Smart Cut process on a donor that is free from BPDs. Transferring a layer that is free from BPDs is behind our SmartSiC-Advanced substrates (see Table 1 for BPD density values for this class of engineered substrate).

One of the merits of having a BPD-free layer at the top of a SmartSiC-Advanced substrate is that it provides an excellent seed layer for drift epitaxy. This layer slashes the density of potential nucleation sites for killer defects, expands the epitaxy process window, and simplifies the epitaxial stack, which no longer needs a conversion buffer.

According to our simulations of yield and our experiments, the improvements that result from our BPD-free layer drive down the induced epi-grown killer-defect density by a factor of ten. The upshot is a hike in manufacturing yield of more than 20 percent for devices with areas of 20 mm^2 or more.

Removing BPDs also aids device reliability: it prevents dislocations from gliding and eliminates bipolar degradation. Insiders of the SiC industry expect the absence of BPDs to deliver a substantial improvement to the production process, with manufacturing yields expected to climb towards 90 percent.

Another asset of our SmartSiC, achieved through the high doping level of the polycrystalline SiC handle substrate, is the ease of forming a back-side ohmic contact for the SiC power device – either a MOSFET or a diode. Thanks to this, we recently demonstrated an annealing-free ohmic-contact process that can be easily implemented on SmartSiC substrates without compromising long-term die assembly reliability. We have started to sample our SmartSiC-Advanced 150 mm engineered substrates. Prototypes are under evaluation by our key customers, and they are available to other customers on demand. At this year's ICSCRM, to be held in Davos, Switzerland, in mid-September, we will present detailed data associated with our SmartSiC-Advanced technology, and deliver four papers.

Ramping production

Our next step is, of course, high-volume production. Paving a path towards this goal, in March 2022 we broke ground at our new factory site, Bernin 4. It will be dedicated to the large-scale manufacture of SmartSiC, with production slated to begin in mid-2023 (see Figure 5). Equipped with this state-of-the-art infrastructure, we will ramp-up SmartSiC production in 2024 and beyond, to reach a total annual capacity of 150 mm and 200 mm wafers of 1 million by 2030.

Production will be dominated by 200 mm SmartSiC. Part of the motivation for majoring on this format is that our experience, over several decades, indicates the exponential benefits of increasing wafer size. When we supply the SiC industry with 200 mm SmartSiC wafers, manufactured with ten-times re-usability, we will make a massive difference to optimising the use of resources. We will relieve pressure in supply chains and enable efficient, accelerated production and adoption of our engineered substrates in automotive and industrial markets. We have already laid the groundwork for this revolution. Multiple partners have evaluated our SmartSiC-Performance prototypes (see Figure 6), and are impressed with

➤ Figure 5. Soitec's new plant, Bernin 4, located in south-east France.

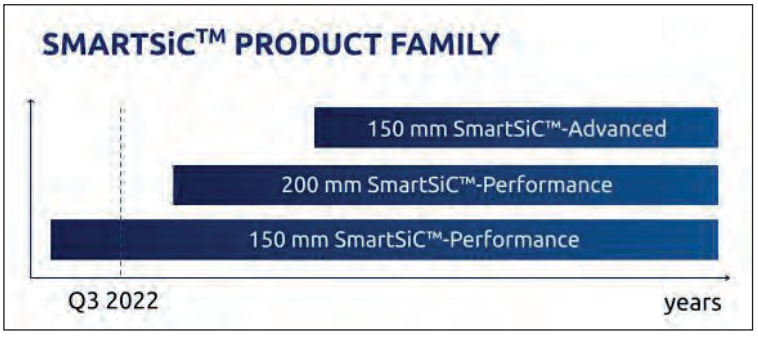
them. Throughout this year we are enlarging and accelerating this qualification phase.

SmartSiC: A new industry standard

The electrification of the automobile is a once-in-a-century transformation that is generating a deluge of innovation. During the previous revolution in transportation, dating back to the early 1900s, it took 15 years for the world to switch from the horse-driven vehicle to mechanical mobility. Let's hope that the transition from gasoline-powered vehicles to EVs will be far faster, given the urgent need to cut carbon dioxide emissions and curb global warming.

We are already underway, as following in the footsteps of Tesla, many makers of EVs are now adopting SiC. Nevertheless, there are numerous hurdles to overcome, in terms of electrical performance, productivity, cost and yield, before SiC can take centre stage in the EV sector. We have anticipated these challenges and the upcoming demand from the EV industry, responding with the development of SmartSiC, a higher value-added alternative to the single-crystal SiC substrate. As our purpose statement says: 'In our soil grows an amazing future.'

➤ Figure 6. SmartSiC wafers in 150 mm and 200 mm formats.



➤ Figure 7. The SmartSiC industrialization roadmap.

Pierre Barnabé appointed new CEO of Soitec

Pierre Barnabé took up the position of Chief Executive Officer of Soitec on 26 July, 2022, after joining Soitec in May 2022.

Between 2015 and 2021, Barnabé was Executive Vice-President of the Atos group in charge of the Big Data & Cybersecurity (BDS) division. He also managed the group's Public Services & Defense and Manufacturing activities and was interim group CEO in 2021. Before its acquisition by Atos in 2014, he was the Deputy CEO of Bull, the unique European leader in supercomputing, electronics for artificial intelligence, cybersecurity and cyberdefense from 2013 to 2015. From 2011 to 2013, he was Managing Director of the Enterprise branch of the French Telco SFR. Prior to this, he held various positions at Alcatel then Alcatel-Lucent.

Optimized LoRa sensor network power solutions can lower IoT Opex

IoT wireless sensor node network operators need thoughtfully developed power schemes to minimize operational expenditures (Opex). While various types of energy harvesting can minimize battery field service requirements, Semtech advises careful planning at the development stage to maximize performance while minimizing power and related Opex costs.

BY MARC PEGULU, SEMTECH

POWERING WIRELESS sensor nodes from batteries or energy harvesting is a key requirement for many applications in the Internet of Things (IoT). The ability to place sensors at the precise spot they are required provides access to data that helps make industrial equipment more efficient, water monitoring more effective and supply chains more efficient. No matter the application, power efficiency is always a key consideration.

Developing a wireless sensor node that can run on battery power or by harvesting the energy from the environment is not a trivial undertaking. Some wireless protocols have peak power requirements that can leave a sensor node depleted, and many of these protocols require higher power to reach an adequate range. This ends up requiring regular battery changes; in networks of hundreds or thousands of sensors spread across remote areas, battery servicing can prove a costly proposition. Using energy harvesting from local sources such as solar cells can help to recharge network batteries, lengthening the replacement cycle. But this requires more complex power management IC (PMIC) devices to handle the variable power from these sources. This can still present a challenge to deliver enough power for wireless networks that use the Internet Protocol (IP).

LoRa® devices were specifically developed for low power applications with low data rates in the IoT. The technology uses a spread-spectrum modulation technique for long-range transmission that can be many kilometres for a line-of-sight connection using the sub-Gigahertz bands of 868MHz in Europe and 915MHz in the US. The sub-Gigahertz bands provide longer range, but support lower bandwidth—alternately, LoRa supports data rates up to 50Kbit/s with battery life that can be as long as 10 years.

LoRa devices have recently been enhanced through the use of more robust technology that can be used to extend the range of sensor nodes and battery life; sensors can even connect directly to satellites orbiting the Earth.

The Long Range - Frequency Hopping Spread Spectrum (LR-FHSS) protocol significantly increases network capacity and robustness to interference, which helps to reduce power consumption for radio transmissions and increase battery life. It can also be used to reach areas that are typically hard for radio networks to access, such as basements where smart meters need a connection.

The LR-FHSS protocol has been enabled as a firmware update in the current wireless transceiver chips from Semtech used in sensor nodes and in the terrestrial gateways to which nodes connect, delivering an immediate boost to the battery life of devices that are already installed.

LR-FHSS also enables battery-powered wireless sensor nodes to efficiently connect to satellites in low earth orbit (LEO). These satellites carry a LoRa payload that can connect to the sensor nodes on the ground in the regulated 2GHz band and relay data back to a ground station. This allows new deployment opportunities across the globe including the ability to place sensor nodes in remote areas. LoRa has also been extended to the 2.4GHz band that is unregulated around the world and used by protocols such as Wi-Fi and Bluetooth. The higher reliability and ruggedness of the original LoRa technology and LR-FHSS allows low power IoT connections in this band; usage examples include smart building applications with battery-backed or even battery-free sensors that harvest energy from light or radio frequency (RF). Achieving this level of utility can be a real challenge with other protocols. LoRa was designed from the ground up for low power operation, starting in the sub-Gigahertz bands but taking those advantages into 2.4GHz and S-band frequencies as well.

Another power conserving strategy involves Chirp Spread Spectrum (CSS) modulation, which spreads narrowband signals across a wider channel, allowing greater interference resilience and low signal-to-noise ratios. This effectively reduces the power requirement. It also works with the network architecture to extend lower power functionality, meaning a typical battery life of 15 years in the sub-Gigahertz unlicensed bands is readily achievable. Part of the power efficiency seen in LoRa wireless networks also comes from limits on duty cycles in some regions. In Europe for example the duty cycle is limited to 1 percent, which translates to a device having a maximum of 36 seconds every hour for transmission. Duty cycle limits help avoid the risk of frequency bands becoming overwhelmed and ensures that the signal can operate without too much interference. Reducing interference helps reduce power consumption since the transceiver does not need to provide more power to overcome it.

Another significant advantage of the LR-FHSS protocol comes in the fact that it supports moving to the S-band for satellite links and the 2.4GHz unlicensed band with more power efficiency than other long range IoT technologies such as LTE-M, NB-IoT as well as cellular bands in 2G, 3G, 4G and now 5G networks. It is also more power efficient than short range technologies in the 2.4GHz unlicensed band such as Wi-Fi and Bluetooth.

Utilizing LTE 4G and 5G for sensor data does have its place. These bands are used for long range, high bandwidth, low latency links with high levels of security. But such use necessitates higher power consumption as they are essentially mobile phone modems with the power requirements and costs associated with mobile networks. GSM 2G and 3G provide lower cost and lower energy consumption than LTE, so these bands are options

for simple devices requiring a battery life of a few years. However, these networks are being shut down around the world to free up spectrum; they are therefore not a long-term solution for today's designs. As the 'M' in LTE-M suggests, the standard was designed for machine-to-machine communications, and as such it was created as a lower power version of LTE. But the technology has been optimised further for lower power in narrow band (NB-IoT), which operates within licensed spectrum; it is comparable to LoRa's power consumption, but since it utilizes cellular spectrum there is greater cost associated with its use.

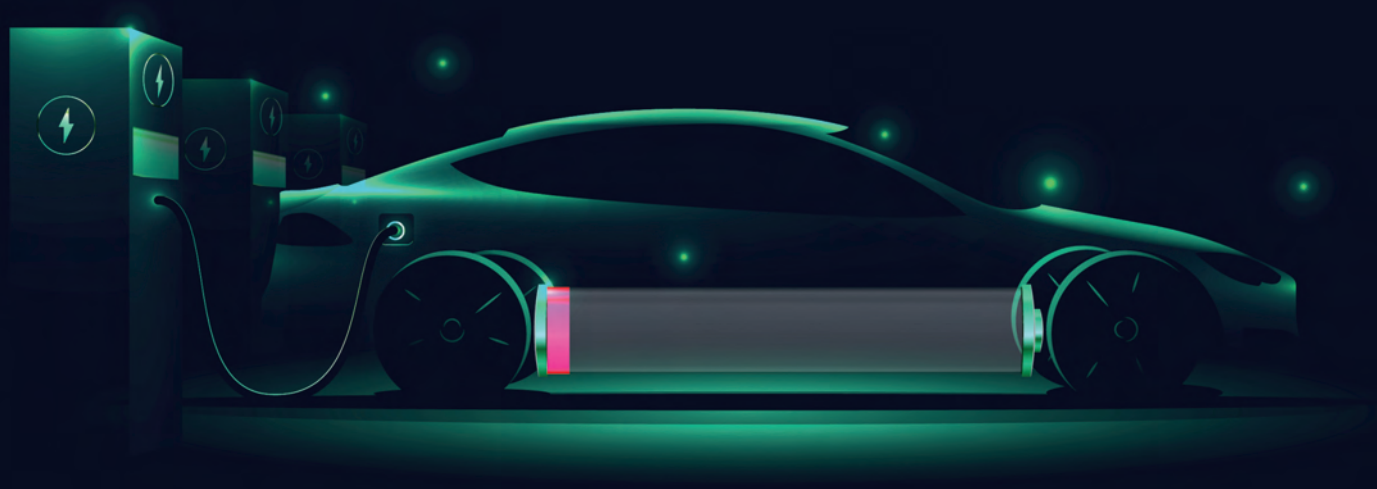
Like LTE-M, NB-IoT uses Frequency Division Multiple Access (FDMA) in the uplink, Orthogonal FDMA (OFDMA) in the downlink, and Quadrature Phase Shift Keying (QPSK) modulation. This is suited to IoT applications that require more frequent communications and low energy; it benefits high penetration use cases such as underground sensors. It has a bandwidth of 180kHz, similar to the 125kHz of LoRa with a similar data rate. Despite these advantages, it is inherently more complex than LoRa, leading to a battery life of up to 10 years.
In the 2.4GHz band, there is also Wi-Fi, Bluetooth and mesh networks such as Zigbee (now called Matter). Wi-Fi tends to have a battery life of a few days, but supports multi-megabit multimedia, while Bluetooth can last for months with data in the megabit range while Zigbee (Matter) battery life can be a couple of years with lower bit rates in the kilohertz range. None compete well with LoRa's combination of power efficiency, range and overall utility.

The choice of protocol for an IoT node has a direct impact on power consumption and battery life. Using LoRa or LR-FHSS provides a significant advantage in the lifetime of battery-backed and energy harvesting IoT node designs, reducing the cost of roll out and delivering data from nodes all around the world.

Full speed ahead for SiC

As shipments of SiC substrates and devices soar over the next few years, several companies are setting their sights on annual revenues of more than a billion dollars from this sector

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR



➤ The ramp in sales of electric vehicles is driving a tremendous hike in revenue for the SiC industry.

There's no doubt that sales of SiC devices are going to climb over the coming years, driven by efforts to expand material supply and chip production. However, even when one has taken this on-board, it's still easy to overlook just how step a trajectory is anticipated.

Those that do have a good handle on the exceptional pace of growth that's expected for the SiC industry include those that attended this year's CS International, held at the Sheraton Hotel at Brussels Airport on 28-29 June. During a session entitled *Building a Multi-billion Dollar SiC Industry*, delegates heard from market analysts, producers of chips and equipment manufacturers – all of them underscored the rapid rate of growth in the SiC sector and the drivers behind it.

Billions and billions

According to Poshun Chiu, Technology and Market Analyst at Yole Intelligence, the SiC market will grow from around $1 billion in 2021 to more than $6 billion by 2027. Over that timeframe the compound annual growth rate will be an astonishing 34 percent.

Most sales of SiC power devices are associated with the automotive industry, explained Chiu, with chips being deployed in battery-powered vehicles, such as cars made by Tesla. He claimed that in 2021 this accounted for 63 percent of all SiC revenue, and forecast that by 2027 it will be worth a 79 percent share. The majority of the rest of the revenue is attributed to a combination of: industrial markets, including charging stations; the energy sector; telecom and infrastructure; and transportation, which includes the railways.

Tipped to dominate sales over the next few years are four companies with ambitions to generate annual sales from SiC activity of at least one billion dollars. The most prominent is Wolfspeed, a vertically integrated manufacturer of SiC products with expertise in the production of wafers, epiwafers, bare die, packaged chips and modules. It is setting its sights on sales of $1.5 billion by 2024/5, driven by a ramp in the shipment of devices. The other multinationals with big plans for SiC are: STMicroelectronics, a supplier to Tesla that also manufactures bare die, packaged chips and

modules, and is expecting its SiC revenues to total $1 billion or more by 2024; Infineon, a maker of bare die, packaged chips and modules, that is targeting $1 billion of sales by the middle of this decade; and onsemi, yet another producer of bare die, packaged chips and modules, that is aiming for $1 billion of SiC revenue by 2023 – with 70 percent of sales attributed to the inverter of the electric vehicle.

These four giants of this industry, plus some of the other leading players, are all making colossal investments in infrastructure over the next few years.

These two European heavyweights ST and Infineon previously announced total capital expenditures of $2.1 billion and $1.6 billion, respectively, in 2021.

This expenditure included investment in SiC production lines. ST used funds to expand the capacity of its 150 mm facilities in Catania and Singapore. Meanwhile, Infineon, which is investing a further $2.4 billion this year, is converting of a 150/200 mm silicon line in Villach, Austria, to SiC and GaN; and funding improvements to a facility in Kulim, Malaysia, that will expand wide bandgap epitaxy and 300 mm silicon capacity.

More modest amounts are currently being invested by onsemi and Wolfspeed, which began a $1 billion investment in its 200 mm fab back in 2018. The US SiC specialist is currently expanding its material and device level capacity, having spent around $0.5 billion in 2021, with plans to invest a similar figure this year. Meanwhile, onsemi paid $415 million last year to acquire SiC crystal boule maker GTAT, and in the 15 months running up to this spring it invested around $0.6 billion in a capacity expansion supporting SiC activity.

Rohm, which Chiu describes as a “very important Japanese player”, has earmarked $3.5 billion for investment in the coming 5 years. This will fund the construction of a new 200 mm line at its Apollo facility. In addition, the company has set aside almost $440 million to secure SiC raw material.

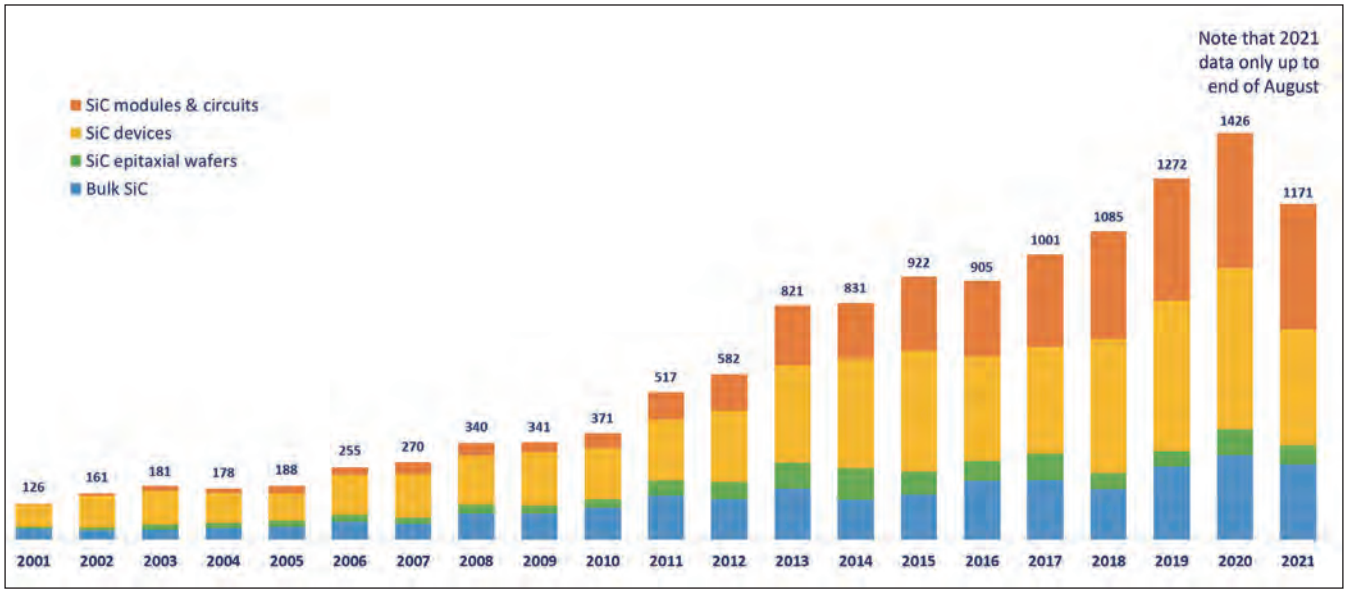
II-VI, which following an acquisition of Coherent is planning to trade under that name, also has an ambitious outlook. Over the next ten years it expects to spend $1 billion on its SiC activities, with strong interests in device business in the years to come.

It is of no surprise that the great prospects for SiC is leading to a number of mergers, acquisitions and partnerships. Chiu presented a timeline capturing this, which highlighted that there has been much activity over the last couple of years. While acquisitions tend to grab the headlines, such as Soitec’s purchase of NovaSiC and Qorvo’s buying of UnitedSiC, the sharing of IP plays a big role in the evolution of the industry. Examples include II-VI licensing technology from GE, and Vitesco Technologies, a maker of drive technologies, working with both Rohm and Infineon.

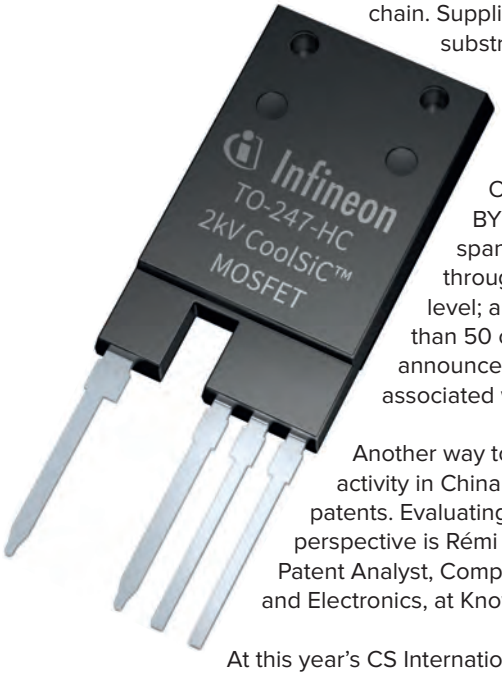
One trend that exists in every sector of the semiconductor industry is that as revenues increase, manufacturing shifts to larger wafers. That’s taking place in the SiC industry, with several companies already demonstrating a 200 mm platform. But that’s not the only important advance, according to Chiu: engineered SiC substrates are being pioneered by Soitec and Sumitomo, there is innovation in SiC growth technology at KISAB, and Infineon and Disco are breaking new ground in wafering processing.

China’s charge

So far, China is yet to make a big impact in the SiC sector. But this is sure to change, as it’s already laying the foundations for success, with companies now operating at all levels within the supply



➤ Figure 1. Patent filings reveal that China will become a major player in SiC in the coming years.



➤ Infineon is expanding its portfolio of SiC MOSFETs through the introduction of devices operating at 2 kV.

chain. Suppliers of SiC boules, substrates and epitaxy include the leading Chinese player in this sector, TankeBlue, and SICC and Sanan Optoelectronics; while BYD Semiconductor is spanning chip processing through to the system level; and there are more than 50 companies that have announced business plans associated with SiC.

Another way to monitor the growth of activity in China is through the filing of patents. Evaluating developments from this perspective is Rémi Comyn, Technology & Patent Analyst, Compound Semiconductors and Electronics, at Knowmade.

At this year's CS International, Comyn highlighted the dramatic growth in patent filing by Chinese companies over the last few years. It is his view that this country's patent activity took off in 2015, and by 2020 it started to lead the world (see Figure 1).

"While very few Chinese players are making products, we can see an ecosystem in the patent activity," remarked Comyn, who named a number of companies with IP for bulk and bare wafers, for epitaxial substrates, for devices, for modules and for circuits. He explained that the nascent SiC industry is supported by research at the country's universities, and the funding of projects that bring many partners together. Efforts are also aided by building on existing infrastructure in power electronics and in compound semiconductor technologies, such as optoelectronics.

Comyn has also considered the type of patent that's been filed, and how this has changed since the start of the millennium. He pointed out that if you go back more than a decade you will find that patents on bulk SiC and SiC devices dominated, while since 2015 there has been a shift to patents associated with SiC devices and modules. Filings associated with SiC epiwafer IP have remained relatively limited, but bulk SiC IP activity has been very active over the past decade.

➤ Aixtron's Senior Product Manager Nicolas Müsgens told delegates at CS International that the strengths of the G5WW C include very efficient consumption of metal-organics and high throughput, thanks to the opportunity to swap wafer carriers at temperatures in excess of 600 °C.

Infineon's expansion

Details from one of the big-four within the SiC industry, Infineon, were provided in a presentation by company Vice President of SiC, Peter Friedrichs.

Like many of its rivals, Infineon has a vast power portfolio, with devices made from silicon, SiC and GaN all spanning a wide range of voltages. Friedrichs explained that the company is complementing each of its silicon devices with an alternative based on a wide bandgap semiconductor: the OptiMOS silicon technology is now complemented with the GaN e-mode lateral HEMT; the silicon superjunction has both this GaN HEMT and the SiC MOSFET as alternatives; and the latter offers a second option to the silicon IGBT. Friedrichs argued that Infineon is well-positioned for success, claiming "experience is very useful". The company has been active in SiC for more than 25 years, and brought the first SiC diode to market back in 2001.

Over the years Infineon has expanded the markets it serves. Back in 2017 sales to makers of solar string inverters accounted for around 87 percent of all the company's SiC revenue. For 2021, this market still brought in more money than any other, but only accounted for 29 percent of all sales. Significant revenue has also come from sales to makers of uninterruptible power supplies, the transportation sector, the energy distribution and storage industry, and those working in transportation.

According to Friedrich's, in 2021 sales of SiC devices netted Infineon $200 million, and should climb by more than 90 percent this year. He told the delegates in Brussels that the company's target of $1 billion of annual revenue from SiC should be hit by the middle of this decade, by which time the automotive market will generate about half of these sales, with the other half attributed to the industrial sector.

Friedrich's claimed that Infineon has the broadest and best SiC portfolio. There are discrete products and modules for the industrial market spanning 600 V to 1.7 kV, and alternatives for the automotive market ranging from 650 V to 1200 V.

Supporting this portfolio is a range of other products. According to Friedrichs, controllers, drivers and switches can come together to produce systems that combine the highest lifetime and reliability with the fastest charging cycles, in a compact design that increases power density by up to 30 percent.

Friedrichs also championed the company's new die attach process, known as .XT technology. This award-winning process is said to enable a significant improvement in thermal impedance. Compared to standard technology, there is an increase in thermal dissipation capability from 145 W to 188 W.

The .XT technology is employed in Infineon's 2 kV SiC MOSFETs and diodes, released earlier this year to expand the variety of products that can serve in an ever expanding number of applications. The 2 kV power devices enable an increase in power density, leading to smaller units for energy storage, charging, and solar inverters. When replacing 1.7 kV products for applications operating at 1.5 kV DC, the MOSFETs combine additional headroom with a ten-fold fall in the cosmic-ray-induced failure rate and a lower on-resistance – for the MOSFET, it is either 12 mΩ or 24 mΩ, compared with 35 mΩ, 45 mΩ or 60 mΩ for the 1.7 kV range. The company has also released an isolated gate driver, which is claimed to provide the perfect match to its 2 kV MOSFET discrete and module.

Equipping chipmakers

The exceptional rate of growth in the SiC market is spurring the development of new tools and technologies to improve the manufacturing process. Speaking at CS International, Aixtron's Senior Product Manager Nicolas Müsgens spoke about the company's latest generation of MOCVD reactor for the growth of SiC layers, and Bernhard Botters, European Sales Manager at KLA, discussed his company's etching and metrology tools.

Aixtron's flagship for SiC epigrowth is the G5WW C, which can accommodate eight 150 mm wafers. Müsgens claimed that this tool offers very efficient consumption of metal-organics, and boosts throughput, thanks to the opportunity to swap wafer carriers at temperatures higher than 600 °C. Thickness uniformity for a 10 μm-thick layer on a 150 mm substrate is ± 2.26 percent, and doping uniformity of a layer with a doping level of 5×10^{15} cm^{-3} is ± 3.53 percent, which is a factor of two improvement.

Thanks to growth in the SiC industry, as well as the ramp in the production of VCSELs and interest in microLEDs, shipment of Aixtron's MOCVD tools is rising fast. To meet this demand, the German outfit has doubled its production capacity between 2020 and 2022, and plans for further expansion in the coming years.

With the SiC market growing so fast, it's easy to overlook the challenges associated with this material and ignore areas where improvement could lead to better devices, higher yields and reduced production costs. Helping to rid delegates of any complacency, Botters reminded them of the yield and reliability challenges facing SiC: this material has a much higher defect density than that for silicon; there is a high level of defect transfer from the substrate to the epilayer, and then to the device; there is a huge variation in the quality of SiC substrates produced by suppliers; there are heavy burn-in requirements; and the high cost of the starting material amplifies the cost of yield loss and excursions.

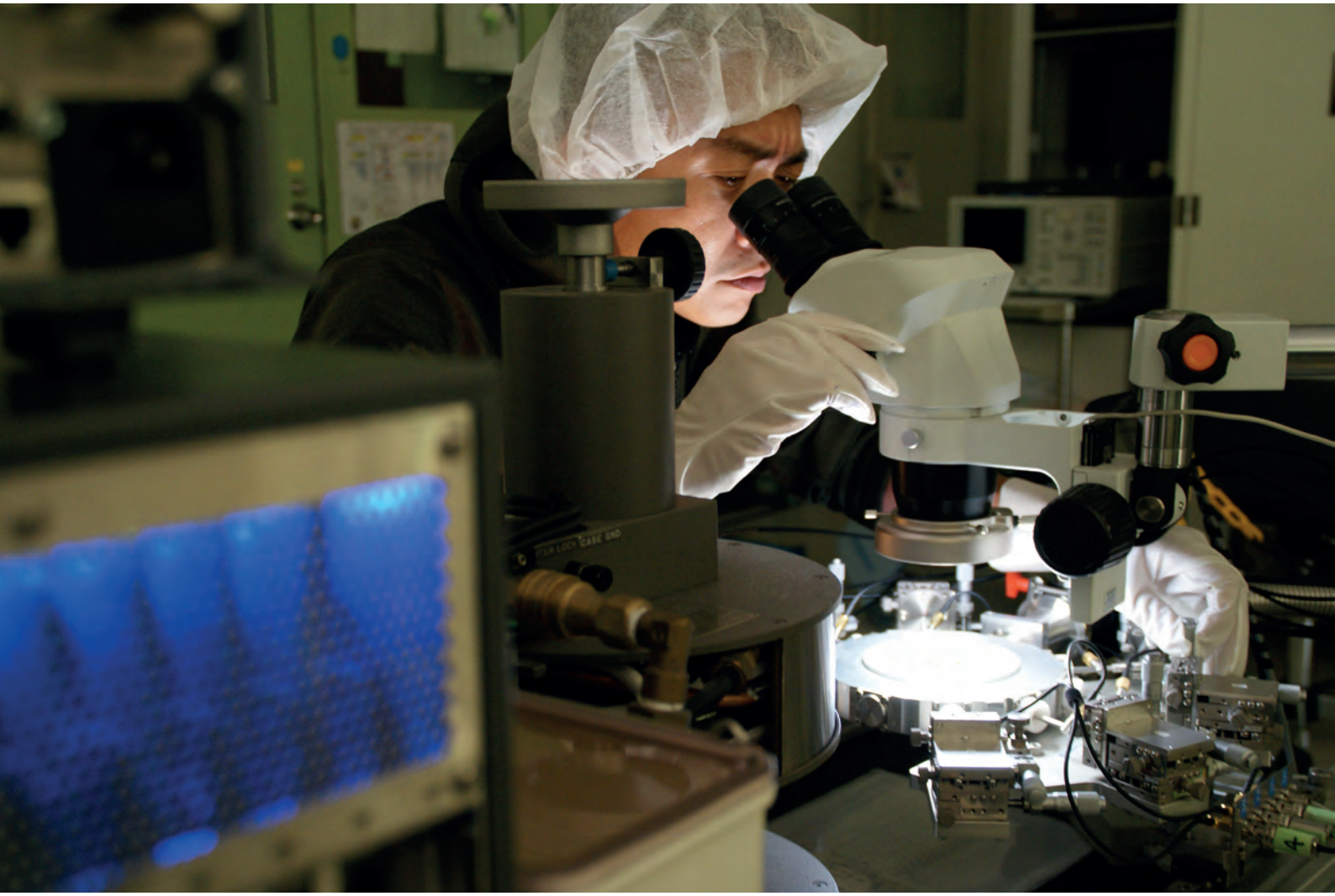
➤ Bernhard Botters, European Sales Manager at KLA, championed the company's broad portfolio of processing and metrology tools for SiC device production.

KLA has a broad portfolio of tools for processing, monitoring and measuring SiC epilayers, partly through its acquisition of the etching and dicing tool manufacturer SPTS back in 2019. According to Botters, one of the strengths of the SPTS etching process is that it enables rounded trench bases, key to the production of next-generation power devices that will not be held back by high peak electric fields, so can operate at higher voltages. He also claimed that the company's tools can provide a superior gate-oxide quality.

The SPTS tools can also be used for plasma-based wafer dicing. This approach is said to increase throughput by 75 percent, boost yield, and lower the cost-of-ownership, compared with the common alternative, blade dicing.

Within the KLA portfolio, there are also instruments for characterising defects and evaluating the mechanical properties of SiC. Using a range of technologies to detect and categorise defects, the Candela 8520 can provide incoming and outgoing quality checks, offer process control, compare the products of different vendors, and be used for tool monitoring and qualification. This instrument, which employs machine learning for multi-channel binning, draws on a large library of defects. Another tool in the portfolio is the company's Nano Indenter, which can be used to study defect propagation and optimise a process, thanks to the opportunity to measure the cracking threshold of SiC and its fracture toughness, elastic modulus, hardness and adhesion energy.

Thanks to strong support from equipment makers, the booming SiC industry is well-positioned for tremendous growth over the coming years. Stories of success are sure to feature at the next CS International, which will return to its traditional spring timeslot. Preparations are already underway for that meeting, to be held on 18 - 19 April 2023 at the Sheraton Hotel, located at Brussels airport.



Breaking new ground with the hybrid transistor

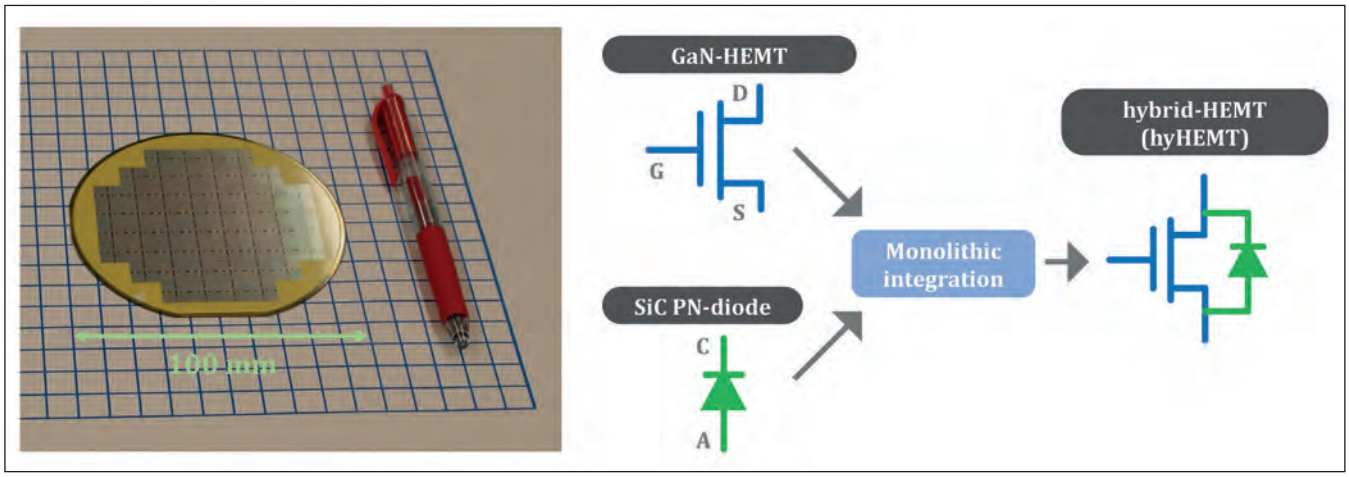
A unique integrated manufacturing process creates hybrid transistors that unite the low on-resistance of GaN HEMTs with the non-destructive breakdown of SiC diodes

BY AKIRA NAKJIMA FROM THE NATIONAL INSTITUTE OF ADVANCED INDUSTRIAL SCIENCE AND TECHNOLOGY

OUR PLANET'S TEMPERATURE is on track to rise to levels that will have horrendous consequences for humanity. Due to this, it is critical that global carbon emissions fall fast. To succeed, we must act on many fronts, including adopting new approaches to the way that energy is created, distributed and used.

If we are to move to a greener society, we will need to change the way we produce and use most of our electricity. Such efforts will have to consider the electrical power converters that step up and down the voltage and transfer it from DC to AC or vice-versa – these are the 'power bricks', extensively employed in a number of electronic applications, including the power supplies in PCs, telecommunications, electric vehicles and aerospace applications. Trim the power losses in these converters and boost their efficiency, and this will lead to energy savings at the system level.

Shifting to a low-carbon society will also require an increase in the uptake of electric vehicles, alongside the installation of far more wind turbines and solar farms. For all these green technologies, we need



power converters that are smaller, more efficient and more reliable than the incumbents. To realise this, there will have to be further technological innovation in the power transistors used in the converters.

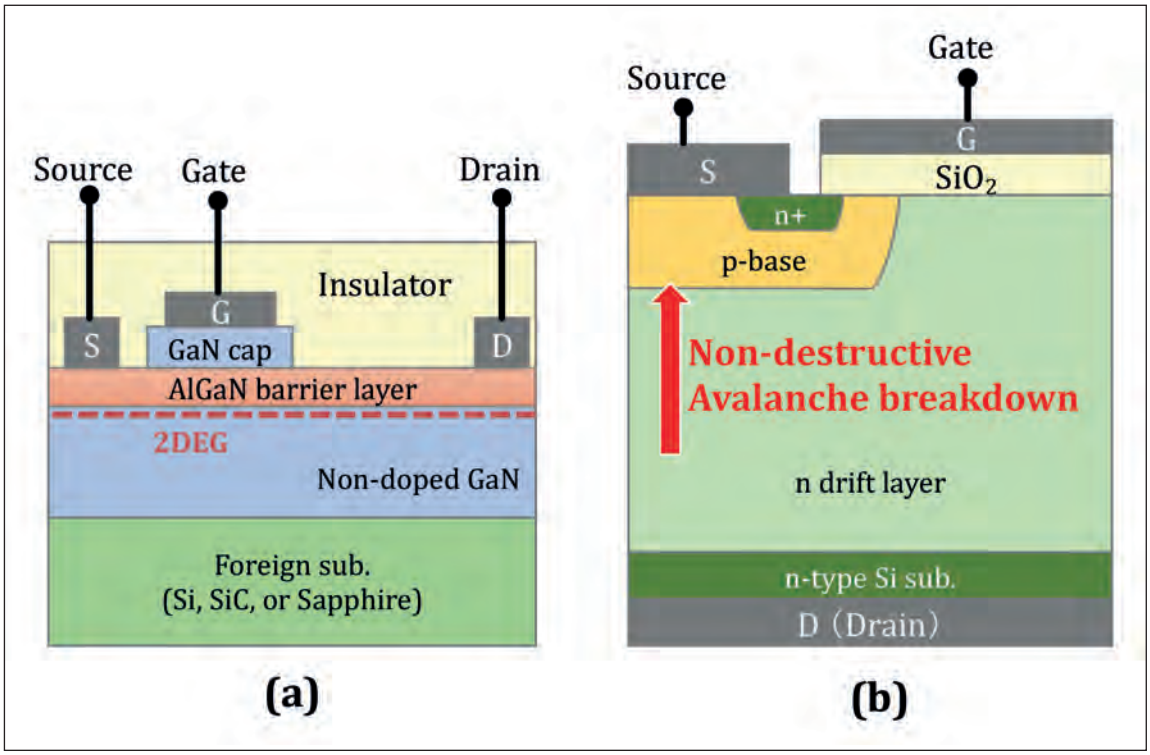
At the heart of power-conversion circuits are power transistors, performing the role of a switch. Ideally, these devices should combine a low on-resistance, to ensure a low conduction loss in the on-state, with a fast switching performance that trims switching losses.

Silicon power transistors are widely deployed in converter applications. Thanks to extensive research and development since the 1960s, their performance has improved, but now it is encroaching material limits. Thus, to deliver higher efficiencies, there's a need to turn to a different class of semiconductor.

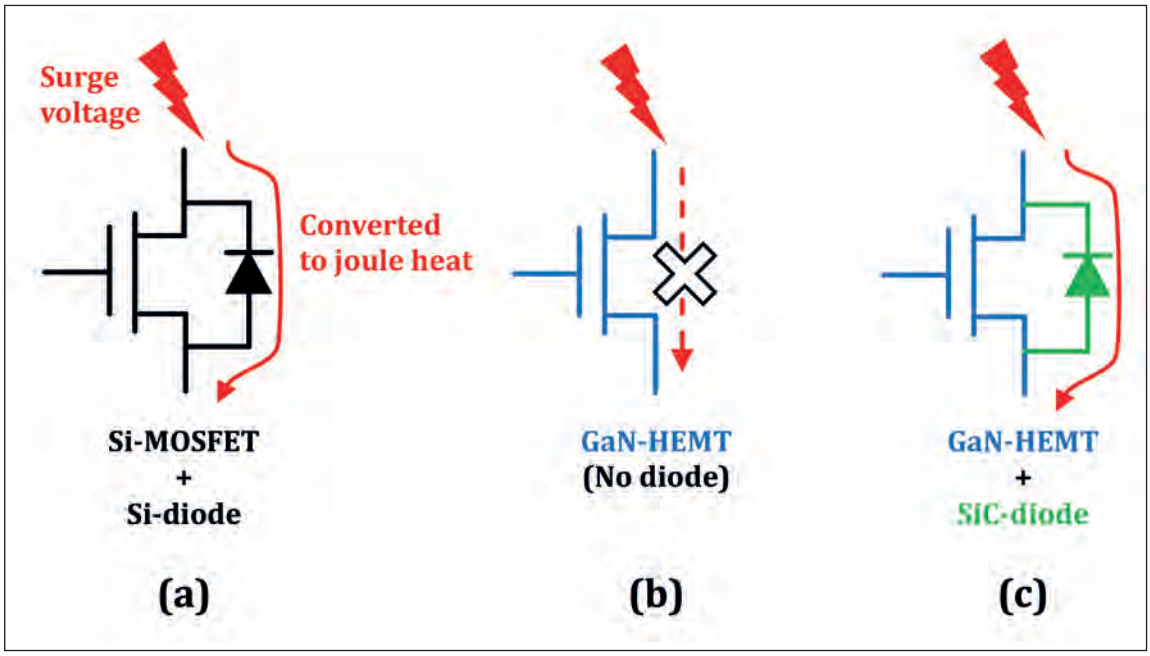
This has led to much interest in devices formed from semiconductors with a wider bandgap. One of them already enjoying commercial success is the GaN HEMT, which features a high-density, highly mobile two-dimensional electron gas (2DEG) as a channel, generated by the unique polarisation nature of the AlGaN/GaN heterointerface (see Figure 2(a)).

The mobility in this channel can exceed 1500 $cm^2 V^{-1} s^{-1}$, due to the generation of free electrons without impurity doping. Another strength of this transistor, resulting from the high electric field strength of the material, is that control of the 2DEG can be realised at a concentration as high as 10^{13} cm^{-2} – that's one order of magnitude higher than that for GaAs and silicon devices. Armed with these attributes, the GaN HEMT surpasses the silicon limit, in terms of low resistance and fast switching.

➤ Figure 1. Photograph of fabricated hybrid HEMTs on a 100 mm SiC substrate (left) and an equivalent circuit (right).



➤ Figure 2. (a) Schematic cross-section of a conventional GaN HEMT and a (b) silicon DMOSFET.



➤ Figure 3. Equivalent circuits in (a) silicon DMOSFETs, (b) GaN HEMTs and (c) hybrid HEMTs in this study.

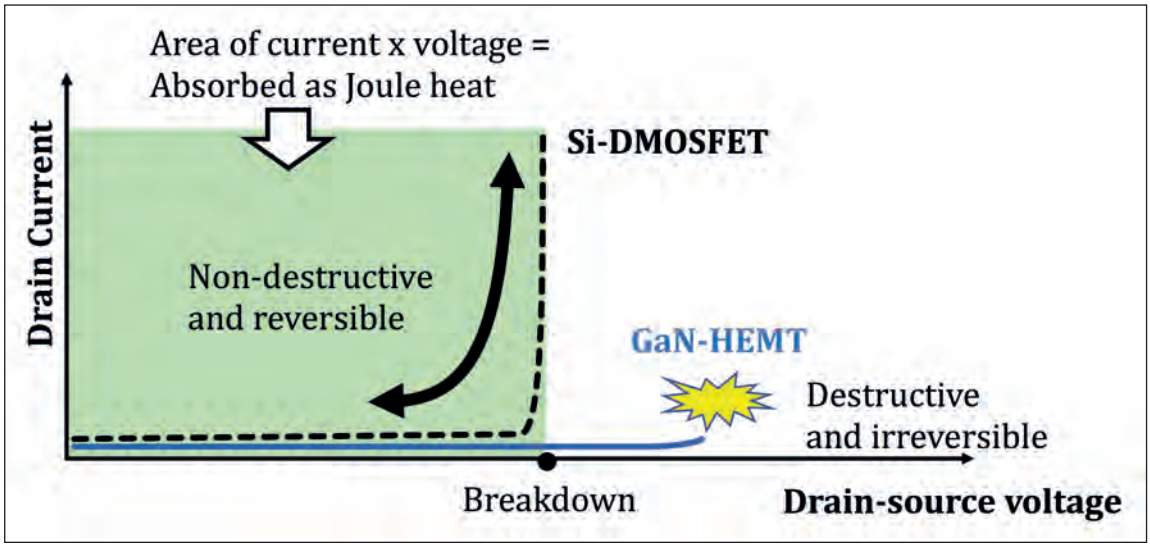
It is now many years since researchers reported the first GaN HEMTs in the 1990s. Subsequent development and commercialisation has led to their deployment in power converters of less than approximately 3 kW, such as compact AC adapters for smartphones, where they combine high efficiency with miniaturisation.

Unfortunately, GaN HEMTs suffer from reliability-related issues, hampering their deployment in high-power applications, such as electric vehicles. An impaired robustness arises from a behaviour that differs from the incumbent, the silicon double-diffusion MOSFET (see Figure 2 (b)). In this double diffusion MOSFET, there is a *p-n* junction between the *p*-type base region and *n*-type drift layer, as well as a *p-n* diode – known as the 'body diode' – that is connected in an anti-parallel configuration (the equivalent circuit is shown in Figure 3(a)). With this configuration, applying an overvoltage to the DMOSFETs under abnormal circuit operations causes the body diode to undergo a non-destructive avalanche breakdown, with the noise energy absorbed as Joule heat in the silicon chip. Due to this, when silicon power transistors are used in converter circuit topologies, they tend to prevent overvoltage during abnormal operations, thereby ensuring system reliability.

With GaN HEMTs, it's a very different state of affairs. The GaN HEMT does not have a body diode, so there is no pass for the noise energy to escape, causing this form of transistor to be destroyed by overvoltage. This weakness has limited the energy saving provided by the GaN HEMT to just low-power converters.

Uniting GaN and SiC

At the National Institute of Advanced Industrial Science and Technology our team has developed an approach to addressing this weakness, based on the introduction of a hybrid HEMT that combines



➤ Figure 4. Schematic of off-state breakdown characteristics in silicon DMOSFETs and GaN HEMTs.

EVG®

invent
innovate
implement

www.EVGroup.com

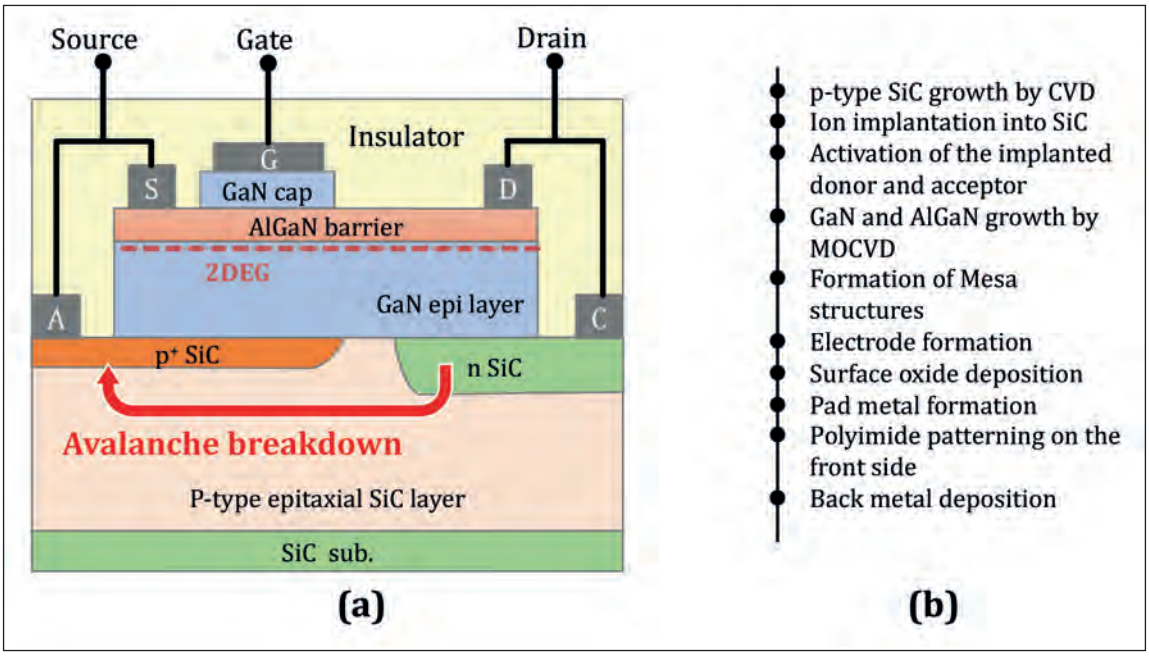
Solutions for

POWER ELECTRONICS MANUFACTURING

- **Temporary Bonding and Debonding**
  of Thinned and Fragile Substrates
- **Spray Coating**
  for Dielectrics, Thick and Thin Resist Layers and High Topography
- **Optical Lithography**
  for Device Patterning and Advanced Packaging
- **Wafer Bonding**
  for Layer Transfer and Advanced Packaging

EVG® 150

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com



➤ Figure 5. (a) Schematic of a GaN/SiC-based hybrid HEMT. Five electrodes: source (S), gate (G), and drain (D) in the HEMT; and anode (A) and cathode (C) in SiC diode. (b) Our fabrication process flow for GaN/SiC hybrid HEMTs.

GaN and SiC. This novel transistor, which solves the issue of destructive breakdown, features a SiC-based anti-parallel *p-n* diode, monolithically integrated to a GaN HEMT (see Figure 5(a)) for a diagram of this device, and Figure 3(c) for the equivalent circuit). This hybrid device has five electrodes: the source, gate and drain of the GaN HEMT structure; and the anode and cathode of the SiC diode structure.

Operated in its off-state, this hybrid can undergo non-destructive avalanche breakdown in the SiC body diode, ensuring robustness. Turn this device on and current flows through a 2DEG channel at the AlGaN/GaN interface, enabling a low on-resistance. So, thanks to these modes of operation, our hybrid HEMT combines the merits that really matter.

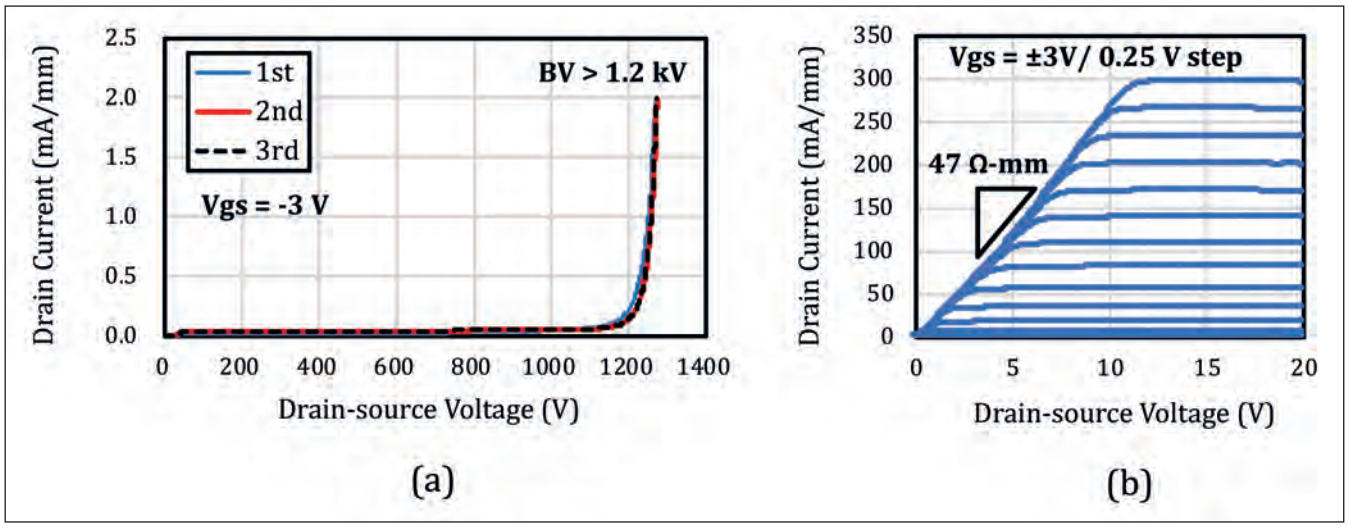
Operated in its off-state, this hybrid device can undergo non-destructive avalanche breakdown in the SiC body diode, ensuring robustness. Turn this device on and current flows through a 2DEG channel at the AlGaN/GaN interface, enabling a low on-resistance

To produce our novel devices, we expanded a 100 mm SiC-based prototyping line, located at an open innovation facility in Tsukuba, Japan. Our changes created a prototyping line for fabricating SiC, GaN and hybrid devices. With these modifications, we have been able to fabricate hybrid HEMTs that are small in size and have a gate width of 50 μm.

The steps we take to make our devices (summarised in Figure 5(b)) begin with the growth of *p*-type SiC via CVD. After this, we form *p*-type and *n*-type SiC regions by ion implantation and activation, before growing HEMT layers by MOCVD and defining the mesa structures by dry etching. Electrodes are then added, followed by deposition of a 3 μm-thick aluminium layer that provides the pad metal. Our final steps involve covering the surface with a polyimide and depositing a nickel-based alloy on the backside of the device.

Electrical measurements on our hybrid HEMT produce promising results. Unlike typical GaN HEMTs, they are not destroyed immediately after a breakdown, but undergo a non-destructive avalanche breakdown in the SiC diode – this is accomplished by designing the breakdown voltage of the SiC side to be slightly lower than that of the GaN side. The breakdown behaviour, associated with a breakdown voltage of about 1.2 kV, is shown in Figure 6(a). As the avalanche breakdown is non-destructive, our device offers a stable reversible breakdown during multiple sweeps. Operating under forward bias, our hybrid HEMT produces a drain current as high as 300 mA/mm and an on-resistance of just 47 Ω mm, thanks to current flow through a high-mobility 2DEG (see Figure 6(b)).

In addition to the low on-resistance and the non-destructive breakdown, our hybrid transistor offers excellent heat-dissipation characteristics. This



➤ Figure 6. (a) Measured off-state breakdown of the fabricated hybrid HEMT. Repetitive current-voltage (I-V) sweep curves up to 2 mA/mm show high stability against avalanche current stress. (b) On-state characteristics. Owing to current flow via the low-resistance 2DEG, a low on-resistance of 47 Ω-mm and high saturation current of 300 mA/mm were measured.

particular attribute comes from the excellent thermal conductivity of SiC, which is three times that of silicon.

Other marriages

Our hybrid HEMT has great potential, combining excellent traits under forward and reverse bias with excellent thermal management. These are very encouraging signs for a device that is still in its infancy, with much opportunity lying ahead for optimisation of the device structure and its fabrication process. Our next steps will be directed at demonstrating large-area devices, rated at 10 A or more, that can be used in actual power converters. We will also devote much effort to trying to commercialise this technology, by engaging with companies that have technical expertise in power devices. Our work forms part of a global effort at developing power devices from materials with a much wider bandgap than silicon. SiC and GaN devices are now commercialised, while those with an even larger bandgap, such as the promising trio of Ga_2O_3, AlN and diamond, are attracting much attention. Of those three, diamond has the potential to be the ultimate semiconductor, due to its extremely high field strength and its superior thermal conductivity. However, heterogeneous integration of different semiconductors may offer new, unconventional opportunities.

Our hybrid HEMT highlights how integration can deliver performances not possible with a single material. There are numerous combinations to explore, opening the door to novel device concepts. We are aiming to investigate what may be possible with this approach, and how it could unleash a new generation of power devices.

A webinar without the right audience is worthless!

Dedicated webinars for the power electronics industry:

Using our 30+ years' experience in B2B vertical technical markets, and as the publisher of Power Electronics portfolio we now offer effective webinars, webcasts and virtual events. We help you get your message, to your desired audience, by marketing to over 53,000 power electronics professionals.

We offer access to the right audience at the right time.

In addition to organising and managing your webinar, we can also market your webinar to our specialist Power Electronics database.

We deliver the audience!

In a dedicated 6 week program we will promote through our magazine, newsletters, LinkedIn group and website.

We can also provide the webinar moderator, from our team of highly respected editors and researchers.

Not sure what to say? Let our editors work with you and help you with the content.

Harness the power of a webinar

- **Brand Awareness**
  Increase global awareness by running sponsored webinars, webcasts and virtual events which also have the possibility of generating revenue
- **Lead Generation**
  Generate and mature leads through the use of online events. Then analyse, qualify, and understand their buying behaviour
- **Thought Leadership**
  Become the voice of knowledge by generating compelling content via online events

PEW POWER ELECTRONICS WORLD
CONNECTING THE GLOBAL COMMUNITY

Find out how Angel Webinar can help you organise and run a webinar within the power electronics industry, contact:

jackie.cannon@angelbc.com +44 (0)1923 690 205

angelwebinar.co.uk