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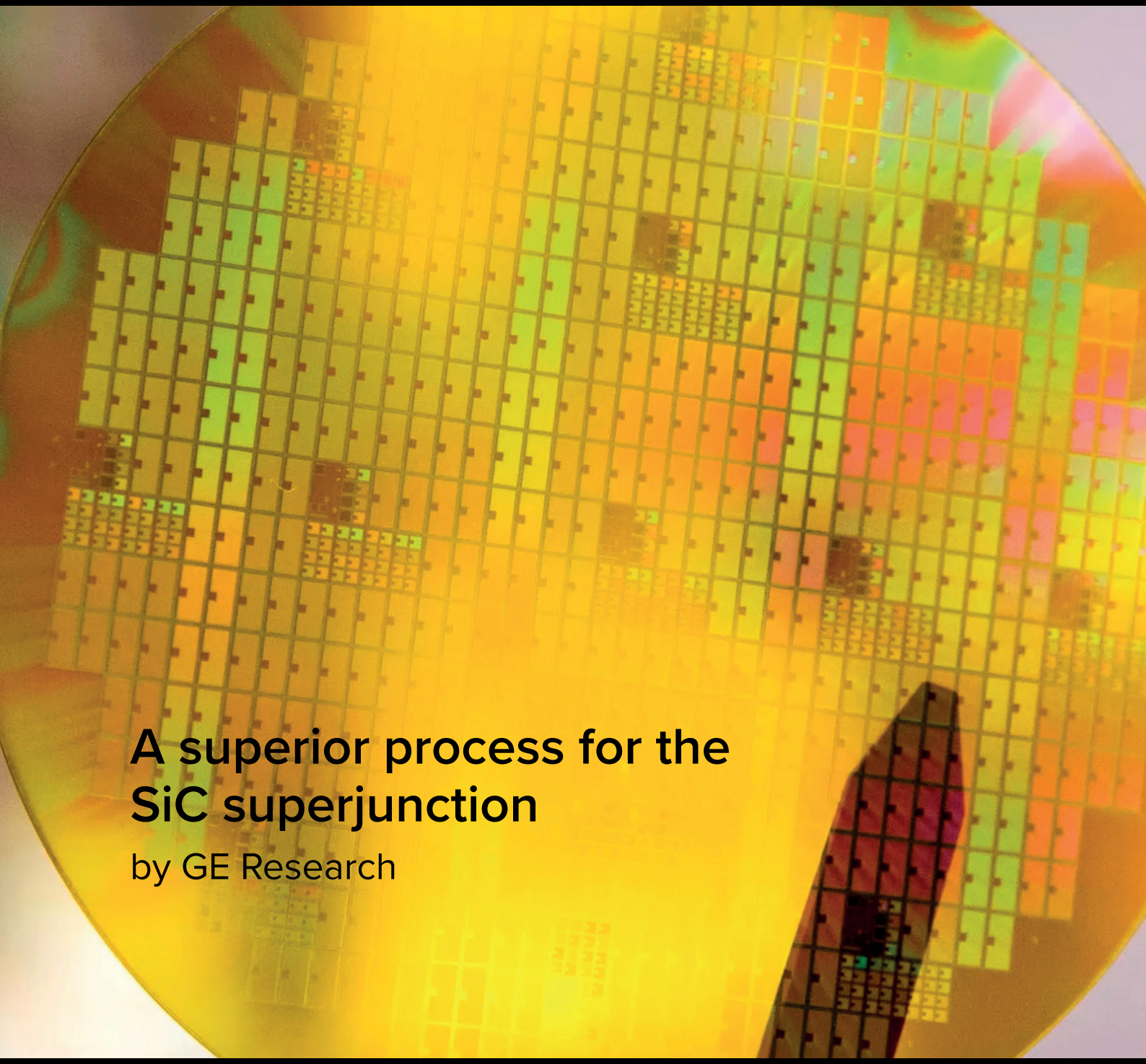

A superior process for the SiC superjunction

by GE Research

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INSIDE

News Review, Features
News Analysis, Profiles
Research Review
and much more...

Banishing barriers to GaN adoption

Performance advantages of GaN established and the challenges of driving GaN HEMTs overcome

GaN's ability in high-speed switching

GaN transistors can switch at faster speeds than silicon or SiC making them much more efficient

Physics-based tools step into the WBG space

Wide band gap (WBG) semiconductors SiC and GaN promise a dramatic increase in power performance

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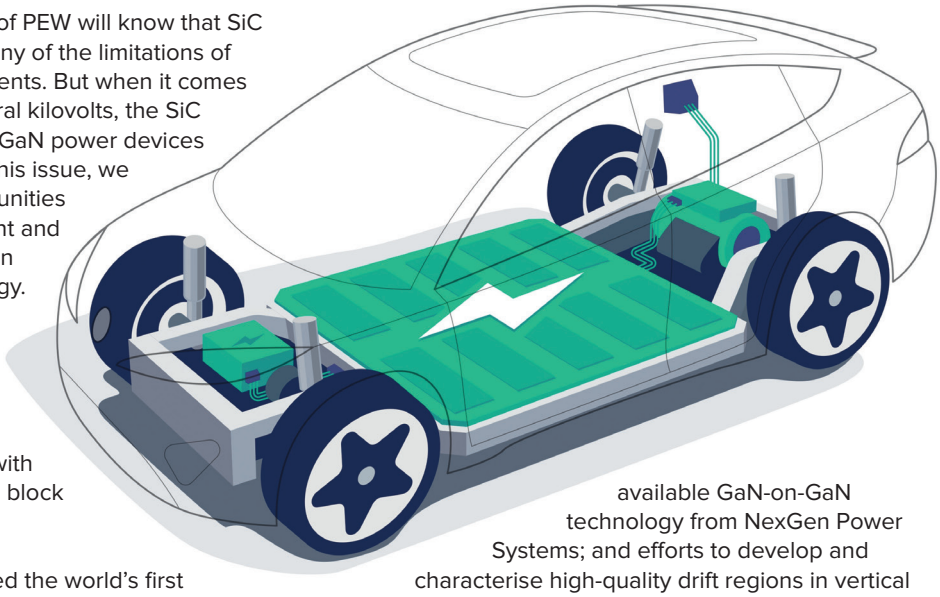
VIEWPOINT

By Christine Evans-Pughe, Acting Editor

Opportunities for GaN and SiC improvement

REGULAR READERS of PEW will know that SiC devices can solve many of the limitations of silicon-based incumbents. But when it comes to blocking voltages of several kilovolts, the SiC approach is less successful. GaN power devices are also far from perfect. In this issue, we examine some of the opportunities for performance improvement and for eradicating weaknesses in both types of WBG technology.



Reza Ghandi from GE Research reveals how rounds of ultra-high energy implantation of epitaxial growth can enable devices with a SiC super junction that can block several kilovolts.

Having recently demonstrated the world's first 3.5 kV SiC superjunction deep-implanted junction barrier Schottky (JBS) diodes, the GE team is now looking at the possibility of developing 3.3 kV SiC SJ MOSFETs.

In a fascinating piece about switching, Rob Gwynne, CEO of UK start-up QPT, explains how his company has solved some of GaN's speed limitations. GaN transistors can switch much faster than silicon or SiC but they tend to overheat if driven at more than 100 kHz, and generate unacceptable levels of EMI. QPT's technology promises to unleash GaN to work at up to 20 MHz and deliver its full potential.

Richard Stevenson, editor of *Compound Semiconductor Magazine,* looks at new approaches to GaN described by conference speakers at *CS Mantech,* held in Florida in May. His report covers the scalable manufacture of planar and vertical *p-i-n* diodes at the US Naval Research Lab; what is claimed to be the world's first commercially available GaN-on-GaN technology from NexGen Power Systems; and efforts to develop and characterise high-quality drift regions in vertical GaN devices at FBH, Berlin.

Continuing the theme of getting the best out of WBG semiconductors, Silvaco's Ahmed Nejim does a deep dive into how new physics-based design tools are helping to predict performance. Such software has been used in WBG power electronics R&D for decades. But as production ramps to serve an increasing variety of commercial applications such as electric powertrains and green energy, the search for improved device and circuit design is accelerating.

For a wider industry picture, 'Batteries on wheels' looks at recent analysis by Berkeley Lab that suggests trains could provide a cost-effective 'insurance policy' for the US grid. With other grid-related projects underway such as the German GaN4EmoBiL to develop power chips for bidirectional charging, could bold new approaches to electricity storage be around the corner?

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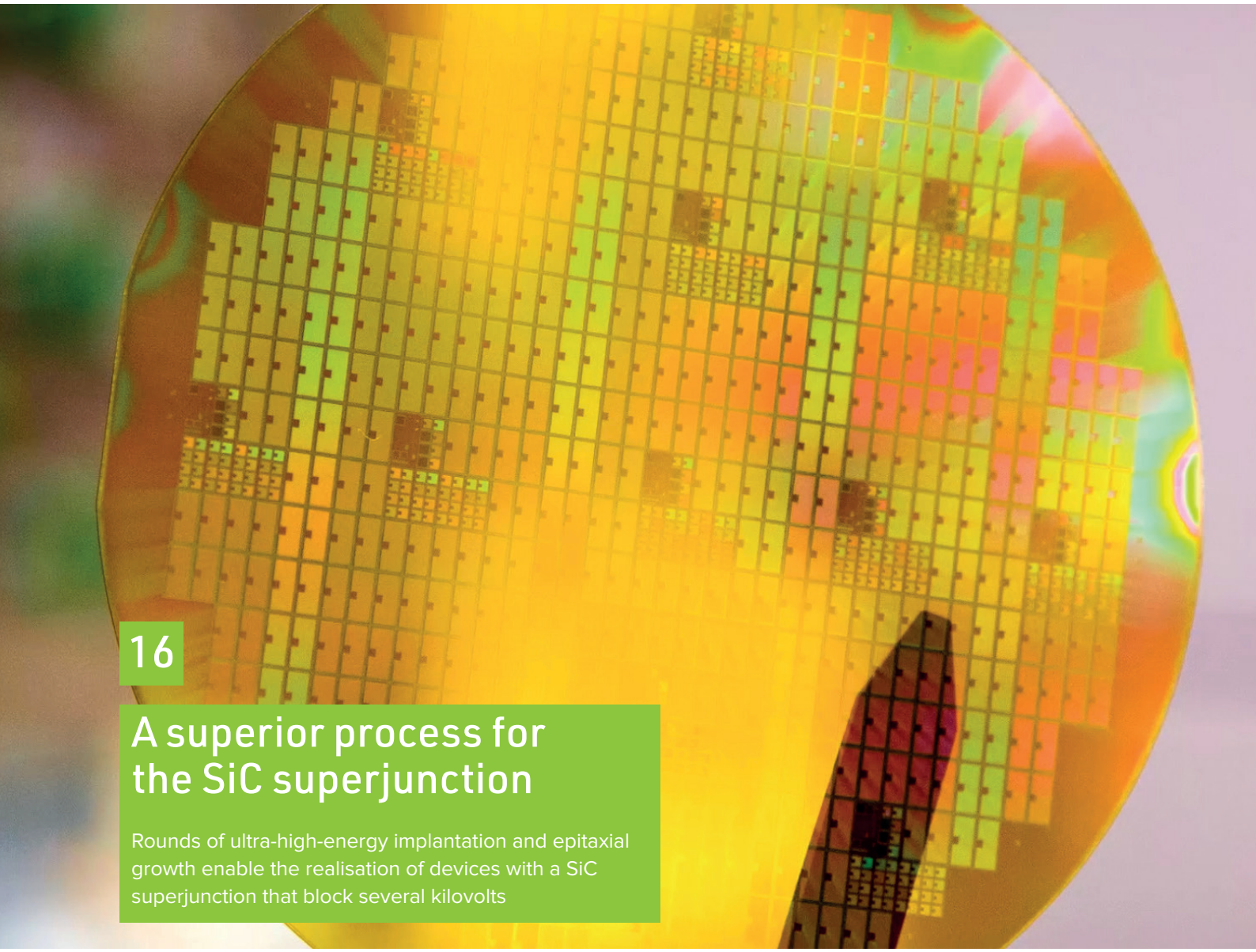

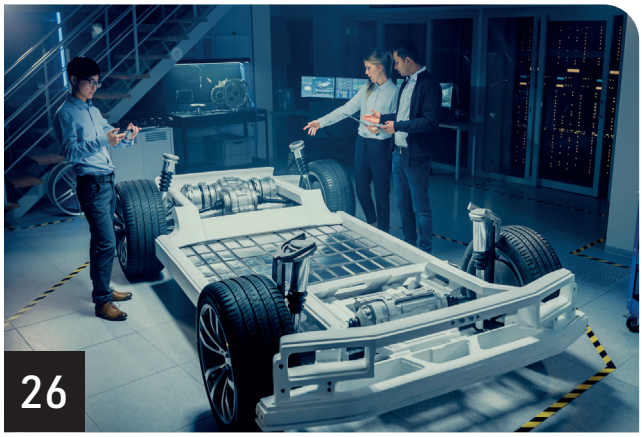

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Angel BUSINESS COMMUNICATIONS

BorgWarner uses ST SiC tech in Volvo modules

ST dice to be used in traction inverter platforms for Volvo BEVs

STMICROELECTRONICS will supply BorgWarner with the latest third generation 750V SiC power MOSFETs dice for their proprietary Viper-based power module.

This power module is used in BorgWarner's traction inverter platforms for several current and future Volvo electric vehicles.

"This collaboration will give Volvo Cars the opportunity to further increase the attractiveness of our electrical vehicles with longer range and faster charging.

"It will also support us on our journey towards being fully electric by 2030 and strengthen our increased vertical integration and our control of critical components," says Javier Varela, COO and deputy CEO, Volvo Cars.

"BorgWarner is pleased to partner with ST to supply our longstanding customer Volvo Cars with inverters for their next generation of BEV platforms," says Stefan Demmerle, VP of BorgWarner and president and general manager, PowerDrive Systems.

BorgWarner collaborated closely with ST's technical team to match their die with BorgWarner's Viper power switch to maximise inverter performance and deliver a compact and cost-effective architecture.

ST's STPOWER SiC products are manufactured in its fabs in Italy, and Singapore, with packaging and testing at its back-end facilities in Morocco and China.

In October 2022, ST announced it would expand its wide bandgap manufacturing capacity with a new integrated SiC substrate manufacturing facility in Catania, home to the company's power semiconductor expertise and the site of integrated research, development, and manufacturing of SiC.

Another step forward in the 'waves of electrification'

BRITISH ENGINEERING and technology pioneer McLaren Applied has launched an 800V SiC inverter that targets growing demand for high-performing, integrated electronic drive units (EDU).

Called the IPG5-x, the inverter is an adaptation of the company's current award-winning 800V SiC inverter, IPG5, and forms a step forward in what the automotive team at McLaren Applied describes as the 'waves of electrification'.

The first wave involved early pioneers of technology, the second wave is denoted by the breakthrough of EVs to the mainstream. The third wave is efficiency and will see inverter technology rapidly adopt SiC semiconductors, especially in 800V architectures, enabling vehicles to achieve longer range where efficient power electronics are key.

McLaren Applied is in discussions with several OEMs and Tier 1 suppliers, and is working with transmission provider TREMEC to jointly develop an integrated EDU for their first customer vehicle application.

"OEMs are increasingly looking for the option to source integrated EDUs that save space, cost and speed up development time," commented Paolo Bargiacchi, head of product, automotive at McLaren Applied. "We've developed the IPG5-x to be highly flexible, so it's ready to be integrated within any combination of motor and transmission. It carries over all of our standalone IPG5's qualities - peak efficiencies over 99 percent, continuously variable switching and fine motor control - building on the maturity of that product."

Bargiacchi added: "Models based on dedicated 800V SiC architectures are leading the way, driving a virtuous cycle: an efficient drivetrain inherently has a smaller battery, which makes the vehicle cheaper, lighter and easier to control, and offers a smaller embedded and operating carbon footprint. It also increases range and speeds up charge times, building trust in the technology."

In anticipation of a 'fourth wave', where OEMs will need to differentiate the customer experience, McLaren Applied says it has developed advanced motor control software in both IPG5 and IPG5-x that enables a variety of features ranging from improved refinement through to a more engaging drive.

Innoscience signs new design-in partner

CODICO to support designers at the 'start of their GaN journey, through to full production'

GaN company Innoscience has announced a distribution deal with CODICO GmbH, covering all European countries.

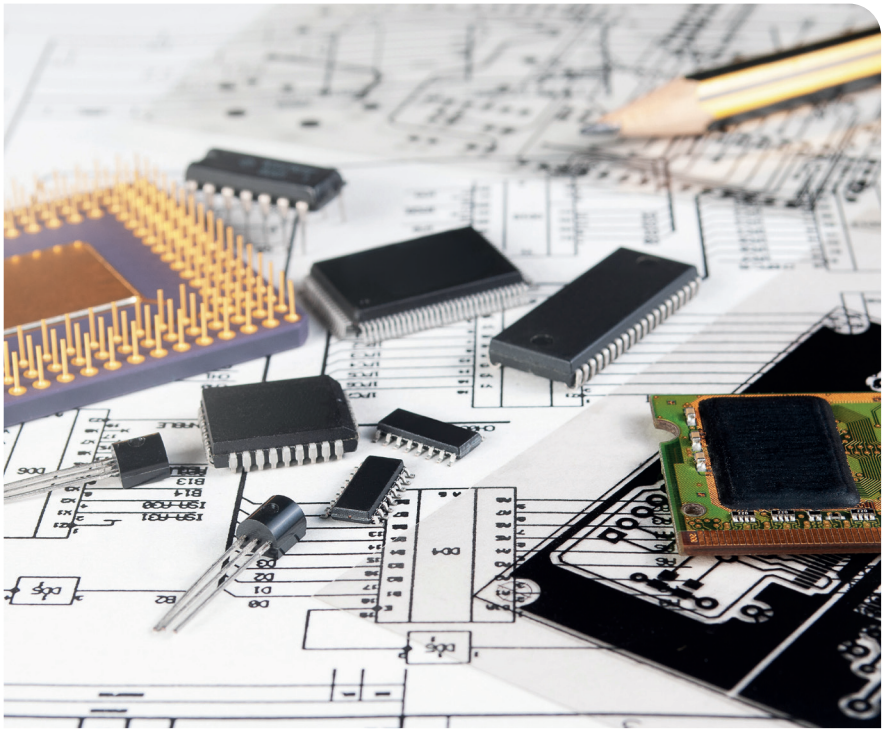
CODICO (an abbreviation of 'The COmponent Design-In COmpany') is a privately owned distributor with headquarters near Vienna in Austria, product competence centres in Munich (Germany), Treviso (Italy) and Stockholm (Sweden), and 43 offices in 12 countries.

It provides technical support from the initial development phase through to the end product, for a range of active, passive and electromechanical electronic components.

Denis Marcon, Innoscience's general manager, Europe said: "Most customers are only at the start of their journey with GaN products, therefore, even though are parts are rugged, reliable and easy to use, designers will need a lot of technical support as they transition from silicon to these WBG parts. We are confident that CODICO is able to provide the technical expertise required to enable our customers to reap the benefits GaN offers."

Thomas Berner, product management at CODICO, added: "Innoscience offers both discrete (InnoGaN) and integrated (SolidGaN) GaN power solutions and is poised to be the world's largest dedicated GaN producer with two 8-inch wafer fabs already in production."

"Therefore, having Innoscience on board supports our plans to grow in our target segments industrial, renewable energies and e-mobility. Innoscience's high-performance and reliable GaN-Fets match our strategy to deliver technical state-of-the art components to our customer-base and complements to the drivers we already offer."



Vishay's 650V MOSFET slashes on-resistance

VISHAY INTERTECHNOLOGY has introduced a new fourth-generation 650V E Series power MOSFET that delivers high efficiency and power density for telecom, industrial, and computing applications. Compared to previous-generation devices, the Vishay Siliconix n-channel SiHP054N65E slashes on-resistance by 48.2 percent while offering a 59 percent lower resistance times gate charge, a key figure of merit (FOM) for 650V MOSFETs used in power conversion applications.

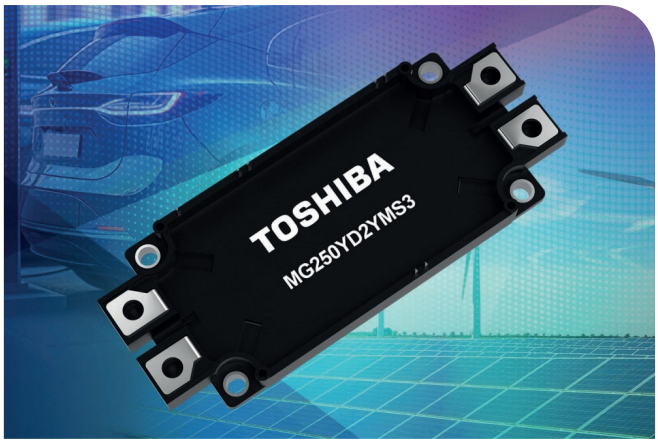
The SiHP054N65E and other devices in the fourth-generation 650V E Series address the need for efficiency and power density improvements in two of the first stages of the power system architecture — power factor correction (PFC) and subsequent DC/DC converter blocks. Typical applications will include servers, edge computing, and data storage; UPS; high intensity discharge (HID) lamps and fluorescent ballast lighting; solar inverters; welding equipment; induction heating; motor drives; and battery chargers. Built on Vishay's latest E Series superjunction technology, the SiHP054N65E's low typical on-resistance of 0.051 Ω at 10V results in a higher power rating for applications > 2 kW and allows the device to address the Open Compute Project's Open Rack V3 (ORV3) standards.

In addition, the MOSFET offers ultra low gate charge down to 72 nC. The resulting FOM of 3.67 Ω*nC is 1.1 percent lower than the closest competing MOSFET in the same class, which translates into reduced conduction and switching losses to save energy and increase efficiency. This allows the device to address the specific titanium efficiency requirements in server power supplies.

Toshiba launches 2200V dual SiC MOSFET module

Module anticipates use of DC1500V in industrial equipment in coming years

TOSHIBA has developed the industry's first 2200V dual SiC MOSFET module for applications such as photovoltaic power systems and energy storage systems that use DC1500V, anticipating widespread use of DC1500V in the future.



Conventional three-level inverters exhibit low switching losses as the off-state voltage across switching devices is half the line voltage. In comparison, two-level inverters have fewer switching modules making them simpler, smaller, and lighter. However, they require semiconductor devices with higher breakdown voltage, as the applied voltage is the line voltage.

Meeting this challenge is important as a two-level inverter based upon the new device achieved higher frequency operation and lower power loss than conventional three-level silicon (Si) IGBT inverter.

The new dual SiC MOSFET module (MG250YD2YMS3) has a VDSS rating of 2200V and is capable of supporting a continuous drain current (ID) of 250A, with 500A in pulsed operation (IDP). Isolation (Visol) is rated at 4000Vrms and the device can operate at channel temperatures (Tch) as high as 150°C.

It offers low conduction loss with a typical drain-source on-voltage (VDS(on) sense) of 0.7V. Switching losses are minimised with typical turn-on and turn-off losses of 14mJ and 11mJ respectively, meaning that the requirement for thermal management is less, resulting in smaller inverters.

Within the MG250YD2YMS3, the impurity concentration and thickness of the drift layer have been optimised to maintain the same relationship between the on-resistance (RDS(ON)) and the breakdown voltage as existing products.

This also strengthens immunity to cosmic rays, a key requirement for PV systems. Furthermore, embedding SBDs with clamped parasitic PN junctions between the p-baseregions and the n-drift layer ensures reliability in reverse conduction conditions.

Switching energy loss for the developed all-SiC module is far lower than equivalent silicon modules. In comparison, the new SiC module achieves double the frequency of a conventional Si IGBT, as well as 37 percent lower loss when comparing a two-level SiC inverter against a three-level Si inverter.

Shipments of the new device will start in September 2023.

Yole unpacks power module packaging

2023 report looks at module costs now and into the future

THE MARKET for power modules will reach $14.8B by 2028, with a 2022 - 2028 compound annual growth rate (CAGR) of 12.8 percent, according to a report by Yole Intelligence. By 2028, the power module packaging raw materials market will have a value of almost $4.1B, representing close to 28 percent of total power module cost.

In its 'Status of the Power Module Packaging Industry 2023' report, Yole has looked at the substrate, baseplate, die-attach, substrate-attach, encapsulation, interconnection, and thermal interface material (TIM) markets in terms of technology, supply chain and market forecasts.

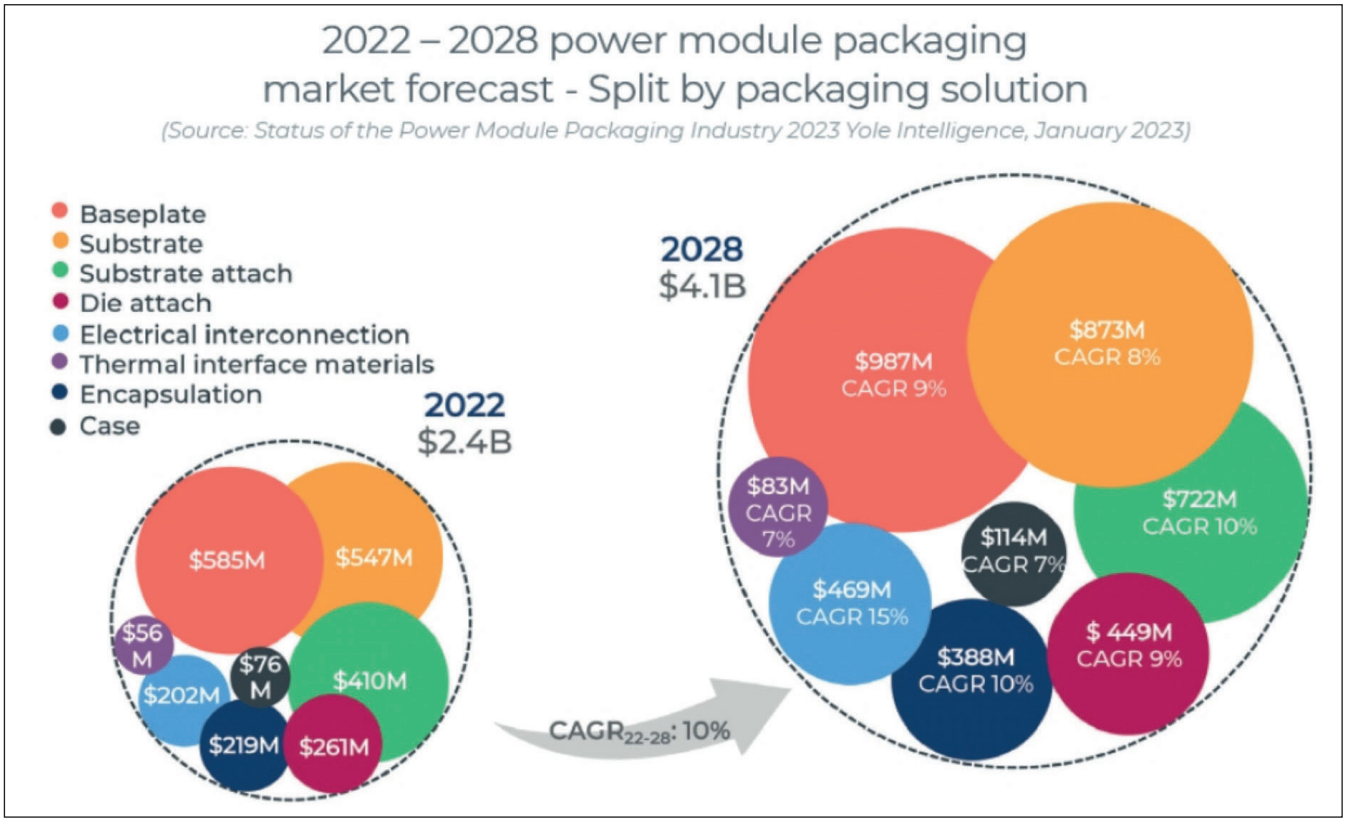
In 2022, the largest packaging material segment was for baseplates (25 percent of total market), followed by substrates (23 percent of total market). The other 28 percent of this market is represented by die-attach and substrate-attach materials. The major technological choices in these segments can rapidly impact the overall power module packaging market, says Yole. For example, the market share for silicon nitride as a substrate is increasing, driven primarily by EV/HEVs, but this technology is pricier than more conventional aluminium oxide substrates.

EV/HEV driving the market

Power packaging needs are increasingly driven by electric and hybrid electric vehicles; a market where requirements for power, frequency, efficiency, robustness, reliability, weight, and volume are more stringent than for industrial products. As a result, demand is increasing for high power density and highly reliable power module packaging materials such as silver sintering paste for die attach and substrate attach, silicon nitride-based ceramic substrate, and copper-based electrical interconnections. on-based modules are the standard power modules for EV/HEV systems. However, SiC-based power modules are gaining in popularity. The introduction of SiC technology requires new power packaging solutions, since a SiC device can work at higher junction temperatures and higher switching frequencies with smaller die sizes.

Supply chain issues?

The huge business opportunity presented by the power device market is attracting interest from different players in the power electronics and automotive supply chains. With a strong focus on power modules, changes in business models and a reshaping of the supply chain are expected. There are new partnerships and acquisitions within the supply chain, such as the acquisition of Laird by Dupont and the acquisition of Hitachi Metals by Bain Capital.



US DoE renews PowerAmerica funding

Continues investment in wide bandgap semiconductor technologies to drive electrification and reduce emissions

THE US Department of Energy (DOE)'s Advanced Materials and Manufacturing Technologies Office (AMMTO) has renewed funding for PowerAmerica, DOE's first Clean Energy Manufacturing Innovation Institute.

PowerAmerica will receive an initial $8 million, with potential funding across four more years to follow, to continue advancing manufacturing of next-generation WBG semiconductors, in particular SiC and GaN, for power electronics.

"The work PowerAmerica—and its 82 member organisations spanning industry, academia, and national labs – is doing to galvanize commercialisation of high-performance power electronics is invaluable to our clean energy future," said AMMTO director Chris Saldaña. "PowerAmerica has catalysed an innovation ecosystem that touches nearly every sector up and down each supply chain."

Raleigh-based PowerAmerica commercialised more than ten WBG technologies over five years. To date, 40 percent of PowerAmerica's 60 projects have reached, or are set to reach, commercial status.

Since launching in 2014, PowerAmerica has also trained more than; 400 masters and PhD students, 300 short course attendees, 1,800 tutorial participants, and 9,000 K-12 students in STEM programs, including 2,000 participants of hands-on trainings.

The new federal funding builds upon initial federal funding of $70 million, in addition to $81 million in cost share from its member partners, for a total of $151 million.

PowerAmerica is one of seven Clean Energy Manufacturing Innovation Institutes supported by two of DOE's Energy Efficiency and Renewable Energy program offices: the Advanced Materials and Manufacturing Technologies Office (AMMTO) and Industrial Efficiency and Decarbonisation Office (IEDO).

In addition, PowerAmerica is one of the 16 member institutes of Manufacturing USA, a national network of manufacturing innovation institutes.

FIA Formula E success for Jaguar racing car

First FIA Formula E race car with both front and rear powertrains uses Wolfspeed SiC chips

JAGUAR TCS RACING took home second place overall in the premiere electric racing league - ABB FIA Formula E Teams' World Championship. Its British-based customer team, Envision Racing, secured first place.

Both teams' powertrains were powered by Wolfspeed's SiC technology, which has been used in Jaguar's Formula E team's powertrains since 2017. This is the first season that Jaguar has supplied its powertrain technology to Envision Racing.

Jaguar TCS Racing revealed the Jaguar I-TYPE 6 car (pictured below) in November 2022. The car, described as the most advanced and efficient electric Jaguar race car ever, was designed specifically to compete in the 2023 ABB FIA Formula E World Championship. It is 74kg lighter and 100kW more powerful than Jaguar's previous electric racing cars, and capable of reaching a maximum speed of 200mph.

It is also the first FIA Formula E race car to feature both front and rear powertrains, as 250kW regen is added to the front and 350kW regen added at the rear. This doubles the regenerative capability over the Gen2 model and removing the need for conventional rear brakes.

The car is a test bed for electric powertrains for both Jaguar TCS Racing and Jaguar Land Rover.

Last year, when Jaguar TCS Racing made Wolfspeed its 'Official Power Semiconductor Partner', Jay Cameron, Wolfspeed SVP and general Manager, power Business, said: "Our SIC semiconductor technology in the Jaguar I-TYPE 6 creates an 'Innovation Lab on Wheels' to engineer improved powertrain efficiency in a high-performance electric vehicle." He added: "Our collaboration with Jaguar TCS Racing in the ABB FIA Formula E World Championship will support our shared goal of translating innovation from the race to the road and enable Wolfspeed to support Jaguar TCS Racing as the ultimate competitor on the track."

University of Arkansas starts building SiC facility

THE UNIVERSITY OF ARKANSAS in the US has began constructing the national Multi-User SiC Research and Fabrication Facility (MUSiC), enabling the government, businesses and universities to build prototypes in SiC.

The facility will offer low-volume prototyping for high-volume manufacturing, bridging the gap between traditional university research and the needs of private industry.

The aim is to accelerate both workforce development and technological advancement in semiconductors by providing a single location where chips can be go from developmental research to prototyping, testing and fabrication.

Alan Mantooth, distinguished professor of electrical engineering at the U of A, is principal investigator for MUSiC. He said that with MUSiC, the university could "begin training the next generation at a variety of degree levels to provide well-trained and educated talent for onshoring semiconductor manufacturing that domestic suppliers offshored in the late 90s and early 2000s. Our training will be equally applicable to silicon and SiC and other materials."

GaN4EmoBiL project targets two-way charging

Fraunhofer IAF and partners to develop technologies to turn EVs into 'batteries on wheels'

BIDIRECTIONAL charging could turn all EVs into 'batteries on wheels', increasing the flexibility of our wider energy ecosystem.

Now, to ensure that two-way charging can be used on a broad scale, a consortium led by Fraunhofer IAF, is researching potential new charging technologies for 800V class batteries.

Partners of the three year GaN4EmoBiL project include the University of Stuttgart, Robert Bosch GmbH and Ambibox GmbH. The consortium's goal is to demonstrate an intelligent and cost-effective bidirectional charging system using new power semiconductors, device concepts and system components.

"Our project aims to connect batteries, renewable energies and electrical consumers in an economical and flexible way. Through bidirectional charging solutions, the previously unused batteries of parking electric vehicles will make a greater contribution to increasing the flexibility of the energy system and avoiding CO2 emissions in the future," says Stefan Monch, researcher in the field of power electronics at Fraunhofer IAF and project coordinator of GaN4EmoBiL.

"In future, efficient, small-scale and intelligent charging infrastructures in electromobility will contribute to overcoming social challenges", says Etienne Tchonla, R&D director at Ambibox.

Today, bidirectional medium-power DC wallboxes for batteries up to 800V use power semiconductors that are either efficient but expensive (SiC) or low-cost but less efficient (silicon). Available 650V transistors made of GaN-on-Si are inexpensive and efficient, but require a complex circuit due to insufficient voltage rating.

To integrate as many batteries as possible bidirectionally, the cost, efficiency and compactness of charging solutions must be significantly improved. For this purpose, the project partners of GaN4EmoBiL are focusing on new semiconductor solutions as a first step. One idea is to develop GaN technology on alternative substrates (for example sapphire), which enables low-cost and efficient 1200 V transistors.

The project is funded by the German Federal Ministry of Economic Affairs and Climate Action (BMWK) as part of the Elektro-Mobil program.

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Batteries on wheels – a new energy asset

From helping with disaster-recovery to making grids more flexible, 'batteries on wheels' are set to become an increasing aspect of energy security

BY CHRISTINE EVANS-PUGHE, ACTING EDITOR, PEW MAGAZINE

WHEN TYPHOON RAI caused major power outages in the Philippines in 2021, Nissan's LEAF EVs helped communities in Cebu and Tacloban to charge over 1,000 mobile phones. This is part of its Blue Switch project1. But what if we could use the electricity stored in thousands of parked EVs during extreme events, or employ trains to transport gigawatts of power around the country?

Dramatic improvements in battery performance and cost, driven by the EV industry, mean that bold new approaches to electricity storage could soon be a reality. This summer, the GaN4EmoBiL consortium, led by the German research organisation Fraunhofer IAF, began work to develop novel GaN power chips for bidirectional charging (see later). And in a paper in *Nature Energy,* scientists from the US Berkeley Lab showed that batteries carried on trains could provide a cost-effective national 'insurance policy' for the US grid.

Cost effective grid back-up

"There's a lot of uncertainty around when extreme supply shortfalls are going to happen, where they will happen, and how extreme they may be," said Jill Moraski, a graduate student at the University of California Berkeley, a researcher at Berkeley Lab, and the Nature Energy paper's lead author. "We found that the US rail network has the capacity to bring energy where it's needed when these events happen, and that it can cost less than building new infrastructure."

The US rail network is the largest in the world, covering nearly 140,000 miles (220,000 km). The Berkeley Lab team's analysis reveals that mobile energy storage could travel between major power markets along existing rail lines within a week without disrupting freight schedules. Compared to new transmission lines and stationary battery capacity, the rail-based approach would save the power sector upwards of $300 per kW-year and $85 per kW-year, respectively.

America is building long-distance transmission lines and installing stationary banks of batteries to meet electricity demand and build capacity for backup power. But Natalie Popovich, a Berkeley Lab research scientist and co-author of the study said: "We have trains that can carry a gigawatt-hour of battery storage, but no one has thought in a cohesive way about how we can couple this resource with the electric grid."

Amol Phadke, a Berkeley Lab staff scientist and co-author of the train study, recalls watching a freight train with 100 carriages as it trundled past a railway crossing. His quick "back-of-the-envelope calculation" showed that this single train could provide power to every household in Berkeley for a few days! He was astonished.

New York State, with its robust freight capacity and current transmission constraints between upstate clean energy generation and downstate load centres, is one example of where rail-based mobile energy storage could work well, say the researchers. In other cases, it may make more ense for multiple states to share the additional capacity from a rail-based battery bank. Like an insurance policy, this approach would spread the coverage across risks for a wide geographic region.

There are regulatory and infrastructure hurdles to overcome. You'd need more interconnections to take power off the train and plug it into the grid; and a framework for approving, pricing, and regulating a mobile energy asset the way they do for conventional power plants. But solving these issues is not rocket science.

Two-way charging ahead

The GaN4EmoBiL consortium led by Fraunhofer IAF, is looking at the nitty gritty of two-way charging technologies for 800V class batteries. Partners of the three-year project include the University of Stuttgart, Robert Bosch GmbH and Ambibox GmbH.

➤ The fully electric Nissan LEAF

The project is funded by the German Federal Ministry of Economic Affairs and Climate Action (BMWK) as part of the Elektro-Mobil program.

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Next generation energy assets

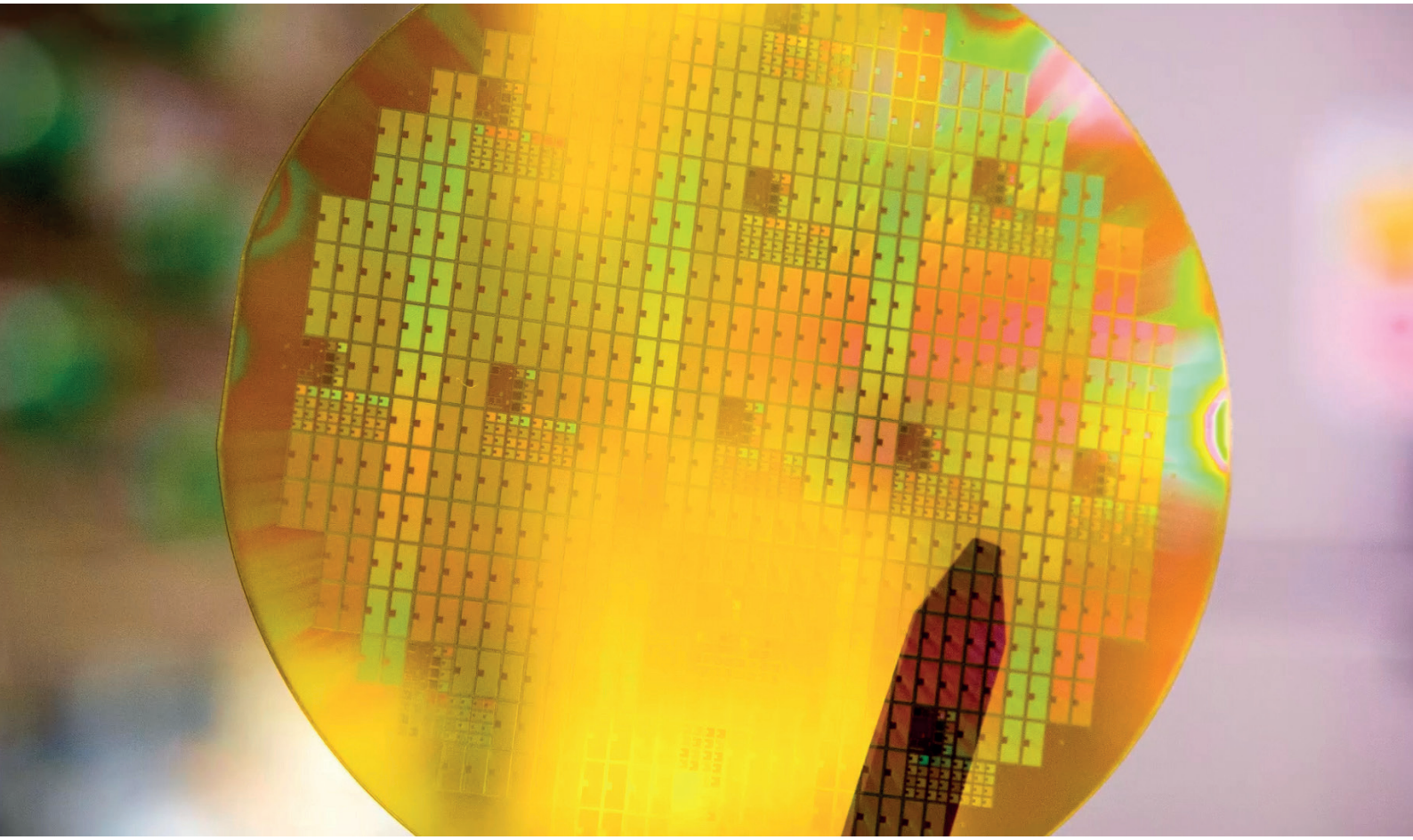
EV-style batteries look set to become a new kind energy asset, an integral part of how our world works. This is an idea that Nissan has put into practice for over a decade. In 2010, in partnership with Sumitomo, Nissan set up the 4R Energy Corp to re-use EV batteries for powering other stuff. Today, when an old Nissan EV battery reaches the 4R factory, it is graded ‘A’ if it can be reused in new high-performance battery units for a new EV; ‘B’ if powerful enough for industrial machinery like forklifts and large stationary energy storage; and ‘C’ for backup power when the electric grid fails, say at grocery stores that must have fridges and lights running during power cuts. The engineers at 4R Energy estimate that recovered batteries have a life span of about 10 to 15 years.

National grids face many pressures. Demand for power is increasing as people swap to electric cars and buildings move from gas to electricity. At the same time, climate change is driving more extreme weather. During the 2020 heat wave, there were rolling blackouts in California. This summer has seen wildfires, floods and emergency evacuations in Europe and beyond. Utilities need to be ready for such events. Re-thinking how we keep the power on by making use of new ‘mobile’ assets like EV batteries will be an important part of this bigger energy picture.

FURTHER READING

➤ Nissan Blue Switch project; https://global.nissanstories.com/en/releases/nissan-blue-switch

➤ ‘Leveraging rail-based mobile energy storage to increase grid reliability in the face of climate uncertainty’ by Jill W. Moraski et al; Nature Energy volume 8 (2023)



A superior process for the SiC superjunction

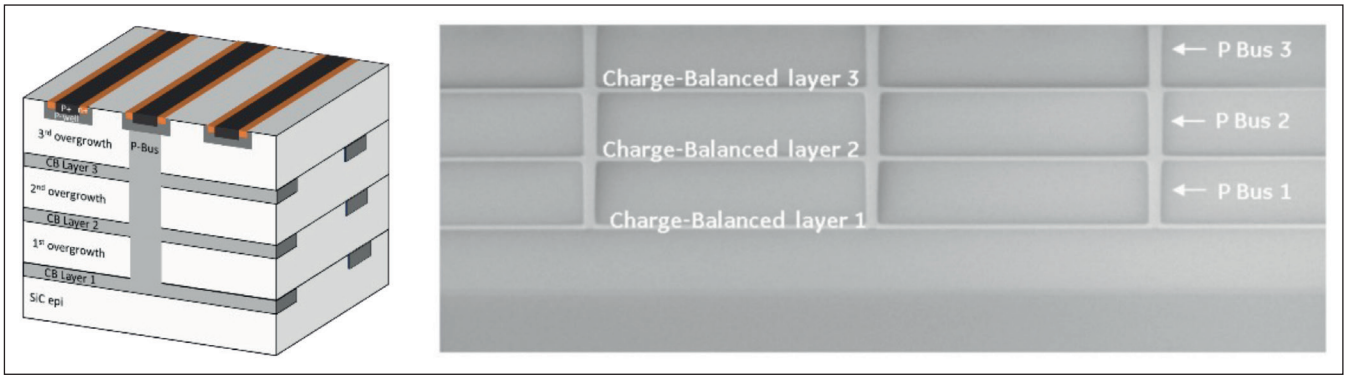
Rounds of ultra-high-energy implantation and epitaxial growth enable the realisation of devices with a SiC superjunction that block several kilovolts

BY REZA GHANDI FROM GE RESEARCH

TO TRIM the global carbon footprint much effort must be devoted at improving electrical infrastructure. As well as the most obvious priority on that front – increasing the proportion of energy that's generated from renewable sources – there needs to be an increase in the efficiency of electrical transmission, right from where power is generated to where it is used.

A key part of electrical infrastructure is the medium-voltage power-conversion system, which may be used in wind turbines, solar installations and marine converters. Operating at voltages above 3.3 kV, this class of power-conversion system is limited to switching frequencies of no more than several hundred hertz, due to losses in silicon-based solid-state switches and diodes. That's far from ideal, because at these low frequencies transformer and converter filter weights can be as high as several tons, which increases system and installation costs and limits design flexibility. What's needed is a shift to highly efficient, lightweight, multi-megawatt/multi-kilohertz power-conversion systems based on ultra-high-voltage power semiconductor devices that switch at moderate frequencies, such as 1-20 kHz.

If you are a regular reader of this publication, you will know that SiC devices can solve many of the limitations of the silicon-based incumbents. But at blocking voltages of several kilovolts, success with this approach is far from trivial. A formidable challenge arises because at blocking voltages of 3.3 kV or more, SiC unipolar switches and diodes suffer from high conduction losses at elevated temperatures, while SiC bipolar devices, such as IGBTs, exhibit a prohibitive high forward-voltage drop of 3 V. Therefore, in these systems, the advantages of SiC technology over that of the silicon IGBT are diminished.

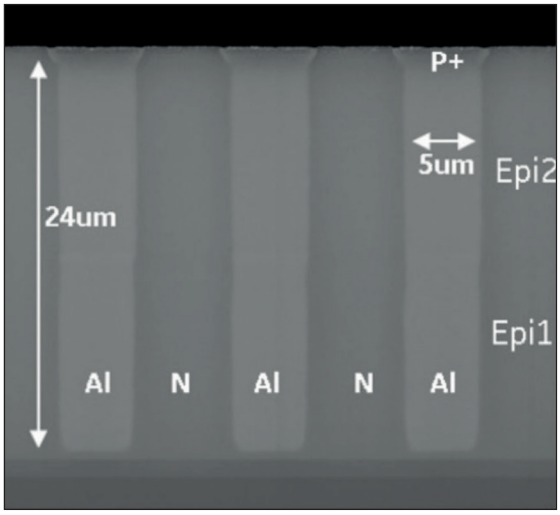


➤ Figure 1. Schematic view (left) and scanning electron microscopy, cross-sectional view (right) of GE's 4.5kV SiC charge-balanced (CB) MOSFET. These switches implement epitaxial regrowth and high-energy implantation similar to SJ devices.

One solution that's attracted interest is the SiC superjunction. This architecture breaks the unipolar conduction limit and offers an improved trade-off between the specific on-resistance and the blocking voltage in medium-voltage-class applications.

To date, there have been a few demonstrations of this device. They include multi-epitaxial SiC superjunction devices that span 1.2- 3.3 kV, and are formed with a multi-epitaxial approach. Fabricating such devices is not straightforward, as it requires several iterations of epi regrowth, due to the shallow projectile depth of implanted atoms in SiC using conventional process tools. An alternative is to make a trench-refill SiC superjunction device. However, although that device can handle 6.5 kV, it suffers from excessive leakage at high blocking voltages, due to crystallographic defects from a complex refill process.

At GE Research we are currently exploring a novel, third fabrication architecture for producing devices operating above 3.3 kV, based on ultra-high-energy implantation and epitaxial growth. This technology

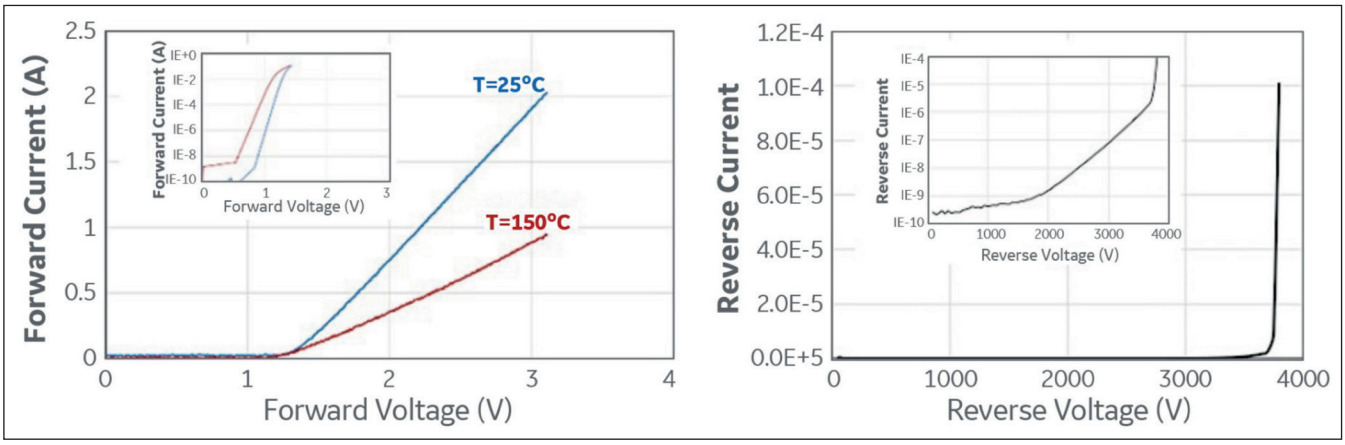


➤ Figure 2. World's first 3.5 kV deep-implanted SiC superjunction, junction barrier Schottky (JBS) diode with two rounds of epitaxial overgrowth and ultra-high-energy implantations fabricated at GE Research.

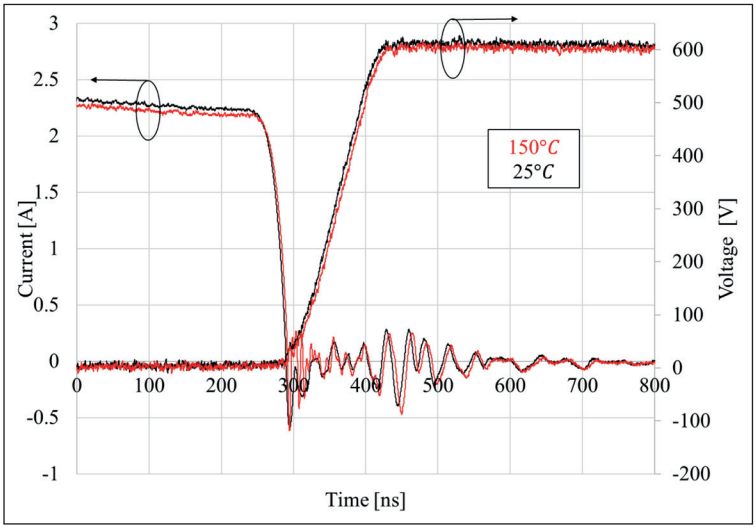
draws on our pioneering capabilities in SiC charge-balanced device fabrication, developed from a recently completed project funded by ARPA-E (the ARPA-E DE- AR0000674 "SiC charge balanced FETs for Breakthrough Power Conversion" programme). In that programme, we developed a superjunction intermediate charge-balanced technology. This involved the implementation of a novel drift layer architecture, to create buried charge-balanced *p*-type regions, which are electrically connected to the top body contact through mega-electron-volt, high-energy implanted regions (denoted P-Bus, as shown in Figure 1). As is the case with superjunction pillars, if the charge-balanced regions are designed with the optimum implanted *p*-type dose and spacing, they deplete surrounding areas during blocking and act as electric field dividers. The key implication is that for a given breakdown voltage, it is possible to use a drift layer with higher doping than that in a traditional design, that enables a lower on-resistance in forward conduction mode and obliterates the conventional, one-dimensional limits for the specific on-resistance as a function of breakdown voltage.

Using this approach, we began by producing devices that have a comparable performance to that of a 20 μm pitch SiC superjunction – and are significantly better than state-of-the art high-voltage SiC approaches. Recent highlights from that effort include the first experimental demonstration of charge-balanced MOSFETs with a differential specific on-resistance of 10 mΩ cm^2 and a blocking voltage of more than 4.5 kV. This value for the specific on-resistance is below the one-dimensional specific on-resistance as a function of blocking voltage, and is nearly 20 percent below that for conventional 4.5 kV SiC FETs reported. To our knowledge, this is the highest breakdown voltage for any SiC charge-balanced device demonstrated to date, and the lowest on-state loss for any 4.5 kV-class MOSFET reported.

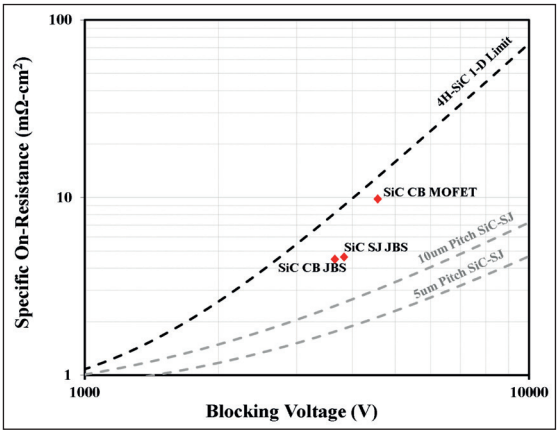
While we are encouraged by this success, we know it's just a start. One downside of this device is that due to its stacked nature for charge balancing, and the charge carrier redistribution required



➤ Figure 3. Forward and reverse current-voltage (I-V) characteristics of 3.5 kV deep-implanted SiC superjunction, junction barrier Schottky (SJ JBS) diode. The specific on-resistance, $R_{on,sp}$ is 4.5 mW cm^2 (45 percent below SiC unipolar limit).



➤ Figure 4. Reverse recovery characteristics of 3.5 kV SiC deep-implanted superjunction, junction barrier Schottky (SJ JBS) diodes at room temperature and 150°C.



➤ Figure 5. Comparison between GE's reported charge-balanced and deep-implanted superjunction devices, together with the 4H-SiC unipolar and superjunction limits.

during switching, there are switching delays, which increase with each additional layer. These delays are prohibitive when scaling SiC charge-balancing devices beyond 4.5 kV.

To build on our initial efforts, we are now extending our charge-balance architecture to full superjunction devices, supported by further funding from ARPA (ARPA-E DE-AR0001007 "Advanced Medium Voltage SiC-SJ FETs with Ultra-Low On-resistance"). Our latest work involves the fabrication of full superjunction devices based on deep implanted pillars, developed for charge-balance devices to overcome the limitations imposed by the charge-balance carrier distribution delay.

Breaking new ground, our team has demonstrated the world's first 3.5 kV SiC superjunction deep-implanted junction barrier Schottky (JBS) diodes (see Figure 2). These devices, a significant milestone for SiC, will provide a stepping stone for our development of 3.3 kV SiC SJ MOSFETs.

The deep-implanted superjunction diodes that we have produced are formed using two rounds of epitaxial overgrowth (12 μm each), leading to a total drift layer thickness of 24 μm. The *p*-doped and *n*-doped pillars were created using two rounds of high-energy implantations (MeV), enabling a maximum junction depth of 12 μm.

We have measured the forward and reverse current-voltage characteristics of our superjunction JBS diode (see Figure 3). This device turns on at 1.4 V and has a specific on-resistance of 4.5 mΩ cm^2 at room temperature and 9.6 mΩ cm^2 at 150 °C, which is about 45 percent below the SiC unipolar limit. Breakdown voltage is 3.8 kV. We have observed low leakage prior to breakdown, suggesting that there is low defectivity following high-energy implantation, epitaxial overgrowth and an activation anneal at 2,000 °C.

Using the ITC57300/57220 from AGVA Technologies (see Figure 4), we have carried

out reverse recovery measurements of SiC superjunction diodes. We did not observe any change in the turn-off current and voltage waveform when increasing the junction temperature from ambient to 150 °C. We estimate the total capacitive charge to be below 700 nC/cm^2.

Benchmarking our charge-balanced and superjunction devices against 4H-SiC unipolar devices and superjunction limits demonstrates the effectiveness of both our technologies (see Figure 5). They are an attractive alternative to the multi-epitaxial and trench-refill approaches to making superjunction devices, and they offer a scalable solution towards the realisation of medium-voltage-class, high-frequency, solid-state switches.

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DEAR0000674 and DEAR0001007 advised by Program Director Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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A new era for Finwave

Three-dimensional GaN FinFETs will ramp to production volumes under the leadership of **Pierre-Yves Lesaicherre, Finwave's new CEO**

COMPANIES THAT are spun out of universities tend to follow a similar trajectory. In their fledgling form, they recruit personnel from the accompanying research group that have specific expertise for honing the technology, and select a researcher from that background with entrepreneurial flair. But when the next phase comes, requiring the raising of substantial capital and a shift from development to production, a new leader takes over with a proven track record of delivering on these fronts.

It's an evolution that is taking place right now at Finwave, the pioneer of three-dimensional GaN FinFET technology that spun out of MIT ten years ago, initially under the name Cambridge Electronics. The company's co-founder and former CEO, Bin Lu, who helped develop the core technology while working for his PhD in Tomás Palacios' group, has now taken over the CTO role, and in his place comes industry veteran Pierre-Yves Lesaicherre.

Incredibly enthused by the tremendous potential of Finwave's technology, Lesaicherre brings with him a wealth of executive experience, having previously held a number of executive roles that include: CEO of equipment manufacturer Nanometrics, where he oversaw the merger with Rudolph Technologies; CEO of the LED manufacturer Lumileds; and several Senior Vice President and Vice President roles at NXP Semiconductors.

Lesaicherre has been appointed to scale Finwave. "The company got new investors on-board last year through Round A, and the new investors have been pretty adamant that they want to see the building of a structure that will allow the company to thrive."

Encouraging Lesaicherre to take on this challenge is what he sees as the great potential of Finwave's highly differentiated GaN technology platform, delivering an order-of-magnitude advancement in both the RF and the power domain. "I always use the analogy of a diamond. It's very difficult to find diamonds, but once you have a rough diamond, it's a lot easier to refine it and cut it and make it into a shining star than it is to develop the technology."

➤ Pierre-Yves Lesaicherre took over from Bin Lu as CEO of Finwave this June.

There's no doubt that Lesaicherre's background has equipped him with the expertise to do just that. As well as knowing how to build and structure a company, he will draw on a wide network. "I know a lot of people through the years and I think that's going to be tremendously helpful as we grow."

Early goals

To begin with, Lesaicherre will concentrate on generating sales. "We are working hard to expedite the production of our first product to meet the enthusiastic demands of our customers, as swiftly as possible."

His other goal is to secure a second round of funding to add to the Series A investment of $13.4 million, which closed in summer 2022. "That's going to come fairly quickly. We have a runway until the end of next year, so by the end of this year or early next year we're going to have to raise the Series B round."

Initially, Lesaicherre will not focus his effort on the company's strategy. That's the task for Finwave's Chief Strategy Officer, Jim Cable, who previously led Peregrine Semiconductor. Both Cable and Lu will guide Lesaicherre while he refines his understanding of the company's technology and its opportunities. However, further down the road Lesaicherre will take on the responsibility for the company's strategic direction.

Finwave has already started to target the RF market, having demonstrated its first product, an RF switch, at this year's International Microwave Symposium (IMS).

"It's a ten-watts broad-band switch that has a remarkably fast switching time and settling time," enthuses Lesaicherre. Allied to that speed – a switching time of 50 ns and a settling time of 100 ns – is a breakdown voltage of around 50 V, and a high degree of linearity and isolation.

While SOI (silicon-on-insulator) technology can match the power-handling capability of Finwave's

device, it falls short on other key metrics. SOI suffers from a slower switching speed, and with a breakdown voltage of around just 3 V, a very large number of devices must be deployed in series. Note that the other contender, GaAs, cannot offer as low a settling time as Finwave's technology, due to traps in the material.

Lesaicherre says that the unique performance of Finwave's transistors led to a very positive reception at IMS. "Now we're sampling these devices to potential customers and we are receiving very positive reactions confirming their exceptional performance."

The company is initially focusing on the 5G millimetre-wave market with a product that sets a new benchmark for power-handling capability.

"When utilised in customer premise equipment, it effectively addresses the uplink power challenge," asserts Lesaicherre. "By doing so, we can unleash the full potential of 5G millimetre-wave."

Finding a fab partner

Finwave developed its 8-inch GaN-on-silicon technology in partnership with Lincoln Labs, which has a small engineering fab in Massachusetts.

"The challenge this year and next year is to move to a high-volume eight-inch fab," says Lesaicherre. "We're in discussions with partners right now in the US and Taiwan to find a good landing spot for a high-volume, eight-inch manufacturing partner."

Negotiations are far easier than they would have been a couple of years ago, when capacity constraints were rampant.

"GaN-on-silicon will be an important factor to load these fabs," points out Lesaicherre. "So the partners we're talking to are very interested, because they see a potential long-term utiliser of their factory capacity."

Fabs with an 8-inch line, which typically have a lithographic capability that extends to 65 nm, should be capable of producing the vast majority of products that Finwave plans to manufacture. However, it's possible that if Finwave designs devices for much higher frequencies, that might require production on a 12-inch line that's capable of making devices with smaller dimensions.

Lesaicherre would like to announce an 8-inch high-volume partner within the next few months and transfer production to them. Additional aims are to expand the company's portfolio with the introduction of power amplifier products next year, and secure traction from some customers.

➤ Finwave's new switch for 5G millimetre-wave applications received a very positive reception from those attending this year's International Microwave Symposium.

"Hopefully before the end of the year we're going to be able to announce utilisation of the device in specific applications and specific customers," says Lesaicherre.

These milestones should help the company secure more funding for its Series B round, which will require winning over new investors.

"When you get to Series B you attract a different type of investor," claims Lesaicherre. "I think some of our Series A investors will be staying with us and invest in Round B, but I would expect the bulk of the money to come from new investors."

Until that money comes in, they'll not be a major change in headcount, which is currently totalling around 20, but will grow slightly as a few staff are added to support the technology development, device design and marketing activities.

"We're very conscious of our burn rate, and we want to keep operating at a fairly frugal level until we get the additional funding," says Lesaicherre.

Clearly, he knows not only what needs to be done to ensure that the FinFET excels, but the right order for those many steps to success.

Fabs with an 8-inch line, which typically have a lithographic capability that extends to 65 nm, should be capable of producing the vast majority of products that Finwave plans to manufacture

A new generation of physics-based tools steps into the WBG space

Wide band gap (WBG) semiconductors SiC and GaN promise a dramatic increase in power performance. But these emerging technologies also require new physics-based design tools to predict their performance and help get the best out of them.

BY AHMED NEJIM, R&D COLLABORATIVE PROJECTS DIRECTOR OF SILVACO EUROPE

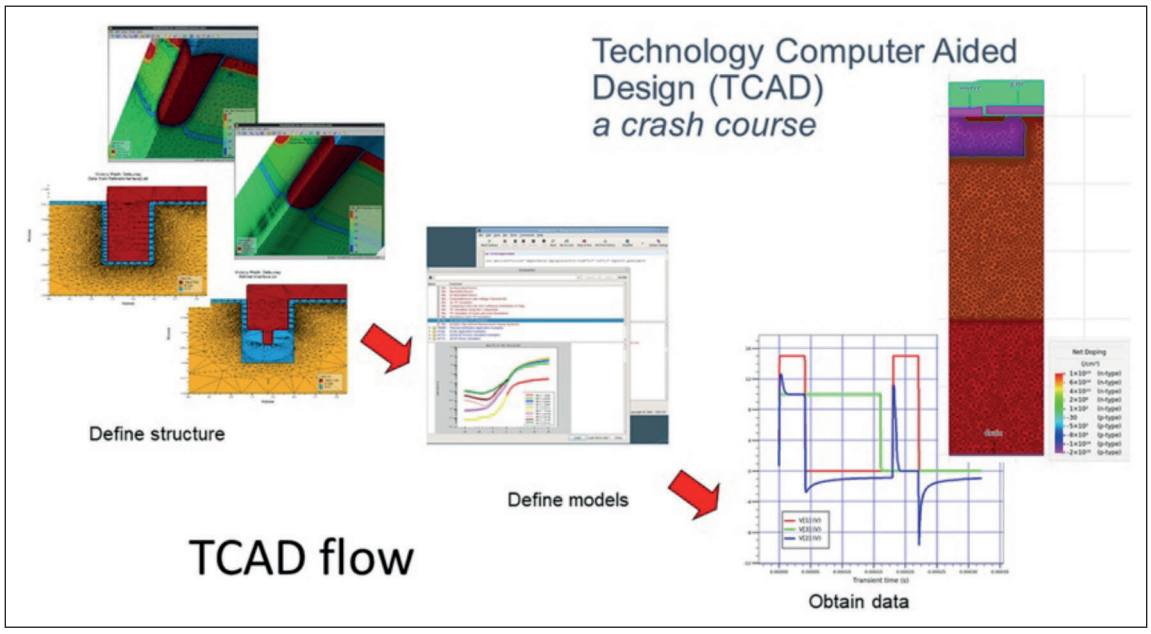
SiC and GaN CHIPS pose many novel and different design challenges compared to silicon-based power devices. Issues such as bulk and interfacial traps, crystallographic stress, and anisotropic transport in 3D structures must be captured to provide the all-important insights required to add value and enable product differentiation.

Physics-based design software has been used in WBG power electronic R&D for decades. But as production ramps up to serve an increasing variety of commercial applications such as electric power trains and green energy, the search for improved device and circuit design is accelerating.

Stepping into this space are physics based numerical Technology Computer Aided Design (TCAD) automation tools.

For decades, TCAD tools have enabled CMOS scaling and development along Moore's law by capturing the manufacturing flow (process) and technology function (device) required for constant enhancement. Look at figure 1, which encapsulates the TCAD flow.

WBG innovation starts with understanding the underlying material science and physical phenomena. This knowledge is then framed into



➤ Figure 1 shows the fundamental concept of TCAD. Users define the structure usually through process simulation, then move to select charge carrier transport models to reflect the technology deployment conditions. Finally, the simulator produces device response and contours under different bias, temperature, frequency, and stress conditions.

numerical representation (models) that capture these phenomena. This is the stuff of long-term academic research and endeavour.

While this is patently hard to achieve, the prize is the all-important insight into the technology performance beyond what can be measured in a lab. Look at figures 2a and b.

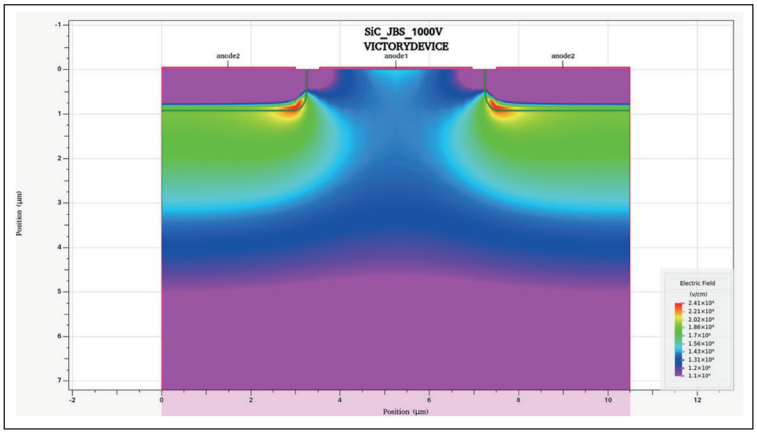
Once these models are parameterised, a multidimensional design space is created. Such space is bound by the material parameters, manufacturing capability and required performance. From this space, the most valuable and lucrative products over the last 60 years of microelectronics have emerged to revolutonise our lives and economies and will do so again in the future. Automated design tools help discover these gems.

How is this done?

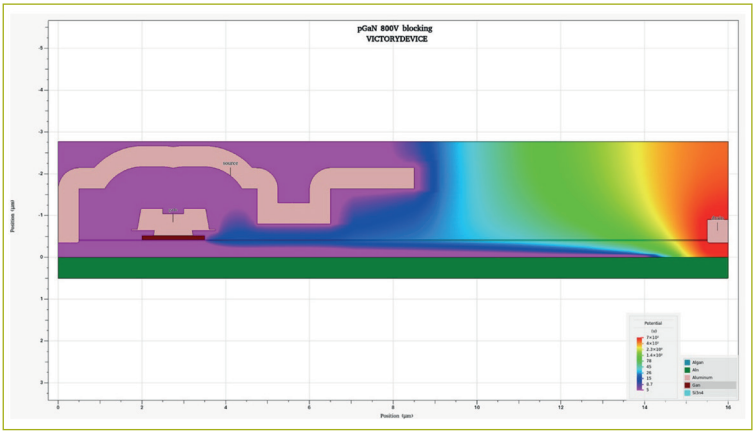
The process starts with intimate understanding of the semiconducting materials crystalline quality and its response to the manufacturing conditions (doping, oxidation, etching and thermal budget). In fact, everything that goes on in the fabrication line has to be captured here to develop a realistic representation of the technology.

Since WBG semiconductors involve grown stacks of diverse crystalline materials, the interplay between different crystalline structures must also be considered as it impacts charge transport. Although single crystals, these materials contain defects that play an active role in charge lifetime and recombination (traps). These traps reside within the bandgap and influence conduction under steady state and crucially under transient (switching) conditions. Knowing the concentration profile, energy level of these traps as well as their capture cross section will help produce realistic transient behaviours and current recovery plots. This is relevant for radio frequency (RF) applications as well as energy blocking switching performance. Furthermore, such defects might also contribute to leakage (tunnelling) currents which impacts device performance.

Since much of the transport events take place at material interfaces and heterojunctions, a clear representation of these must be captured. These include semiconductor-semiconductor interfaces which are key to WBG device stacks, dielectrics used in passivation and capping layers, and semiconductor metal contacts. The electrical contact material performance controls the leakage current and the final resistive path such as Drain Source on resistance (RDS_{on}). Dielectric material quality plays a crucial role in managing the field distribution in the device and must therefore be modelled accurately. The next arena to enter is to model the charge carrier transport as a function of bias, geometry, stress, temperature and so on, to mimic device behaviour when placed inside circuits and products. Knowing how the technology would perform under product deployment conditions is the ultimate prize designers seek.

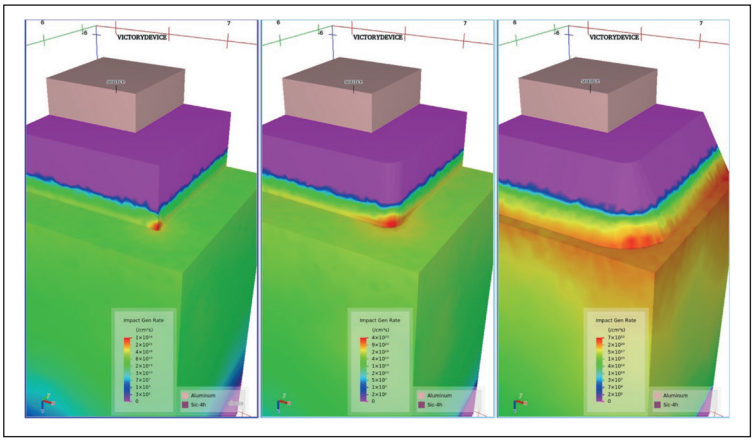


➤ Figure 2a shows electric field intensity contours in a SiC Junction barrier Schottky (JBS) diode under 1000V reverse bias. One can see the 'attack' of the field as it attempts to enter between the p-doped anode regions (shown as anode 2). Such insight and the location of the peak field helps designers optimise the distance between the regions and the doping profile to improve voltage blocking performance.

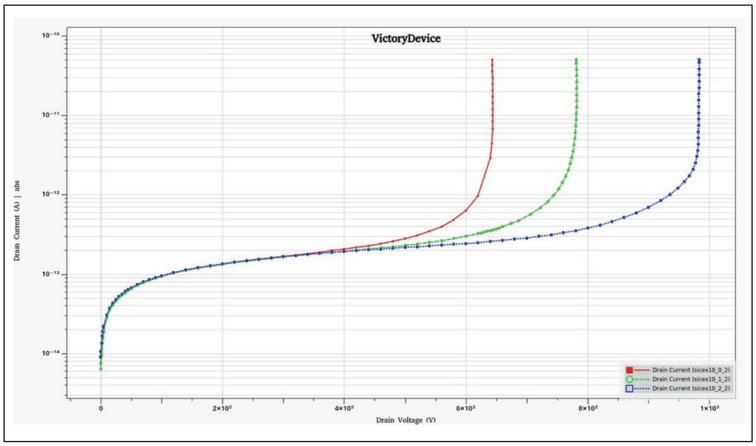


➤ Figure 2b shows the pGaN FET potential contours near breakdown. One can clearly see the role of the source shield plate in protecting the gate stack from the drain contact on the right. This helps designers in creating effective screening geometries.

The next arena to enter is to model the charge carrier transport as a function of bias, geometry, stress, temperature and so on, to mimic device behaviour when placed inside circuits and products



➤ Figure 3a shows breakdown in trench 4H-SiC power device. The impact ionisation rate distribution is shown along the wall of the trench as a function of trench slope and curvature in 3D. Vertical trench with sharp corners shows a hot spot while rounded and sloped trench shows a diffused distribution.

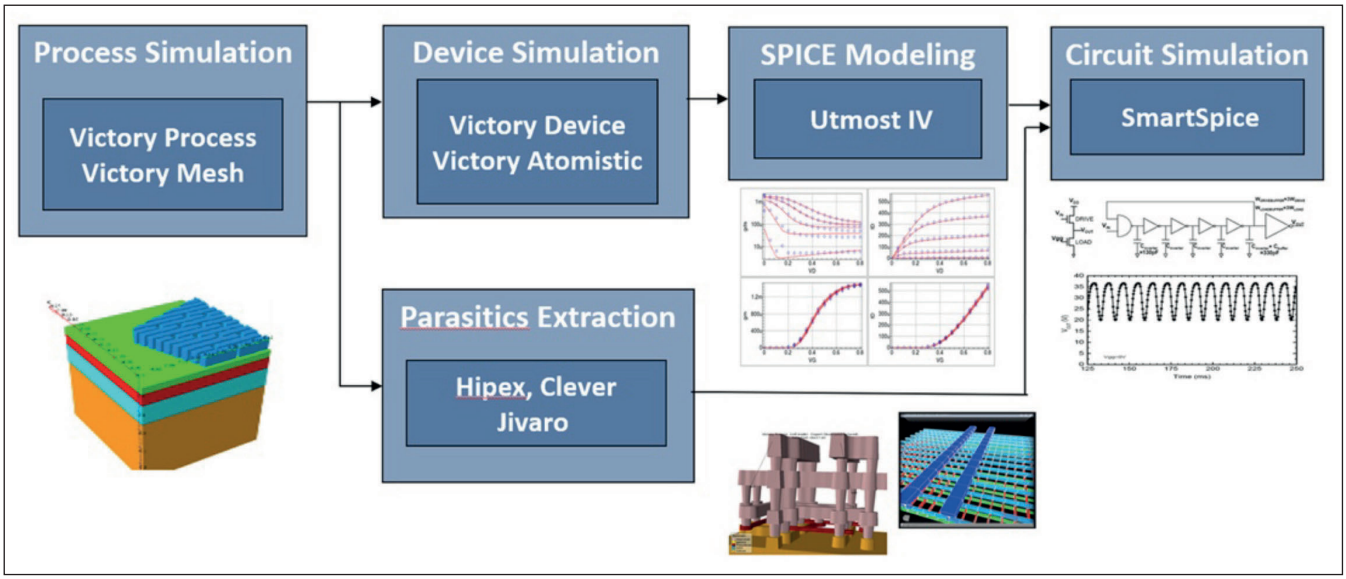


➤ Figure 3b shows the breakdown IdVd plots for the three configurations above. Red for the vertical sharp corner, green for the vertical rounded corner and blue for the sloped rounded geometry. Optimising the geometry in 3D space produces clear advantages in higher breakdown characteristics.

To give a flavour of the prominent issues facing WBG power electronics device designers contend with, here are few examples. In essence, designers need to track carriers from their generation (birth) to their recombination (death). Carrier lifetime, velocity and density is dealt with using various mobility models. These models respond to electric field strength and direction (field is a vector), temperature, carrier concentration, crystallographic orientation, and various scattering events.

Every so often carriers will encounter an energy barrier which blocks the usual drift diffusion transport while tunnelling probability through such barriers remains a possibility. This must be accounted for as key technology performance indicators are dependent on such events. Breakdown is calculated by considering carrier concentration amplification through internal impact rates under high electric field. Most of these phenomena are coupled so numerically robust tools are called for. As device geometry becomes more complex, 3D simulations become crucial. Look at figures 3a and b.

Consequently, these powerful tools have been used most effectively to develop power electronic products over the years and will play a crucial role in ramping up GaN and SiC based microelectronics. Technology issues such as voltage breakdown, leakage current and transconductance can be obtained readily from these calculations. However, since the interaction between the manufacturing conditions (fabrication flow) and device performance under steady state or switching conditions can also be quantified, and production yield can be better understood. This is especially important for mass market products such as automotive power trains and power management. To improve the usage experience and reduce entry barrier, TCAD tools come with a wealth of models and material



➤ Figure 4 shows the design tools in a design technology co-optimisation flow. The tools required to establish a seamless link between manufacturing and circuit simulation together with parasitic extraction and reduction.

libraries that are based on many years of open literature and best practice, as well as the advanced graphical user interface (GUI) and data visualisation tools. Advanced meshing engines as well as multithreading calculations accelerate calculations and enable parallel (matrix) simulations rather than sequential ones. This improves productivity.

Other features such as open architecture that enable designers to customise their material parameters and transport models add value especially for novel technologies design such as WBG based power electronics.

Model robustness and the automation of these tools enable technology designers to investigate their design space made available to them by the manufacturability limits to best respond to market demands and differentiate from competitors. Such design of experiment (DOE) tools can quickly produce optimised compromise for the highest yield. The increased technology complexity represents a profound challenge in this area. The automation of these tools is an arena of significant R&D effort in recent years. The goal here is to add value with the smallest number of iterations and computational overhead.

Since design activities acquire greater commercial value as development moves from device to circuit then to system (increased abstraction level), a seamless link between device design and circuit (SPICE) design is of particular interest. Such simulation flow (Design Technology Co-Optimisation DTCO) establishes the link between manufacturing flow and device geometry on the one hand and circuit performance on the other. (figure 4) This will base circuit design on sound technology footings framed within the available manufacturing flows.

Conclusions

TCAD tools especially when coupled with SPICE simulations within a DTCO flow propels WBG power electronics technology developments. They enable developers to discover the best available solutions for increased power efficiency, breakdown performance and high yield as well as product differentiation from competitors.

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Unleashing GaN's full ability for high-speed switching

GaN transistors can switch at much faster speeds than silicon or SiC, making them much more efficient. However, GaN transistors can overheat if driven at more than 100 kHz, and generate unacceptable levels of EMI. **Rob Gwynne, CEO of QPT Ltd,** explains how his company has solved these limitations to unleash GaN to work at up to 20 MHz and deliver its full potential.

OPERATING GaN FETs at under 100 kHz means that their performance is similar to silicon or SiC, which limits the benefits of using GaN in the first place. As GaN transistors can transition from on to off at 1-2ns instead of 20-50ns for Si and SiC transistors, there is potential for a huge improvement in efficiency.

The core of the problem is that the expertise of power engineers is in the 10 to 100 kHz region where silicon and SiC currently operate. Go above this and RF issues start to become a problem which requires solving them with a different set of skills, i.e., those of an RF engineer, with a Faraday cage to block the EMI. The second issue is the huge amount of energy within a tiny slice of GaN, which if not handled correctly means that the transistor will rapidly overheat.

This can be seen in figure 1 that shows the increasing amount of waste energy being produced as losses as the operational frequency of SiC and normal GaN increases. By contrast, the green line of GaN with QPT's technology shows hardly any increase in energy loss.

Why is there energy loss during the switching process?

A key application for GaN switching is to control an electric motor's speed using a Variable Frequency Drive (VFD). For example, a three phase, 380V supply is changed into 540V DC (typically) using a Vienna rectifier. This DC is then chopped to provide the required frequencies to drive and control the motor. The higher the frequency, the faster the motor runs. Chopping means switching the DC bus on and off, making rectangular waveforms called Pulse Width Modulation or PWM.

As the width of these rectangular waves is varied, the power delivered increases or decreases. This digital on/off signal then either has to be averaged to a sine wave in a big external filter that is expensive and bulky. Or, in cheaper systems that don't have the filter, connected directly to the motor, where these high voltage, high speed transients degrade the bearings, the insulation and heat up the motor, wasting power and reducing the life of the motor.

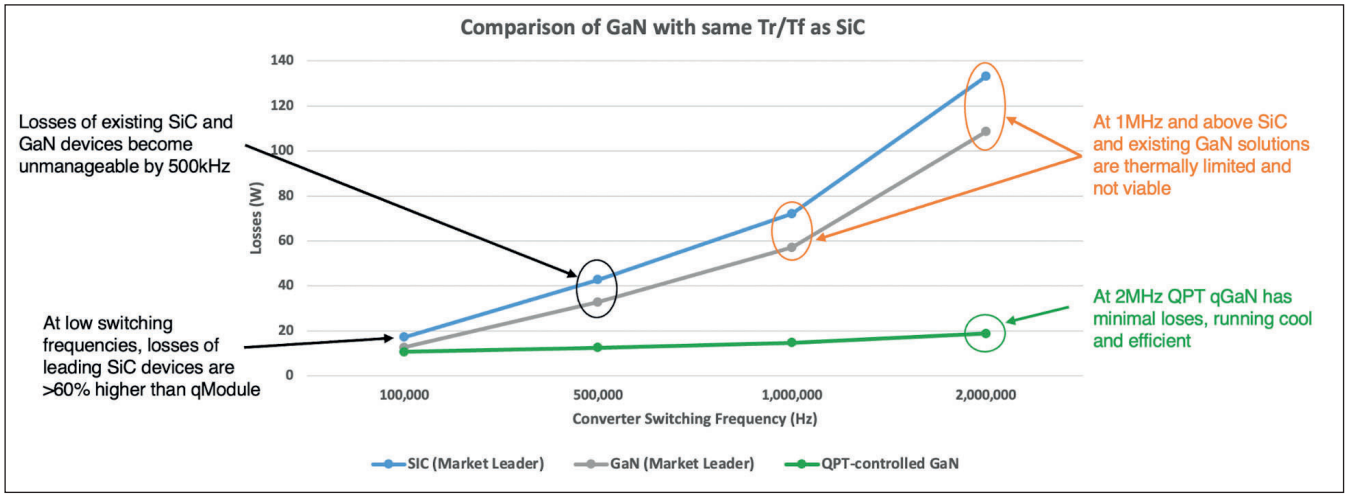


Figure 1. Showing increasing losses as switching frequency increases.

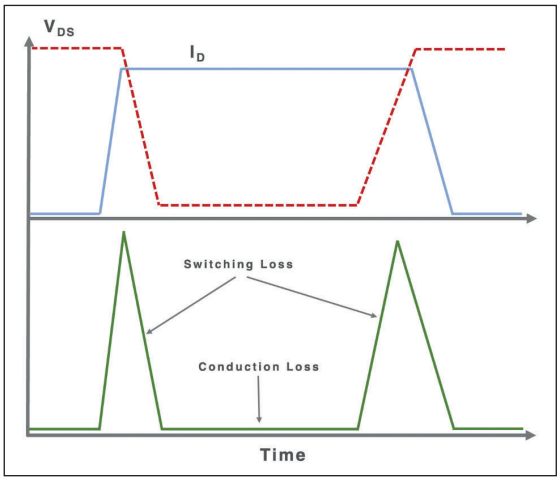
In QPT's approach, the high voltage PWM is filtered inside a VFD implemented with QPT modules using the company's proprietary WhisperGaN construction system. Only pure sinewaves leave the module. Thus, no big, expensive, external filter is needed to generate sinewaves for the motor and the connected motor's lifespan is not degraded by this VFD. Energy is lost on the rise and fall of each transition from off to on or on to off. Shorten the time that this takes and less energy is lost.

The smaller area under Vds/I_{DS} curves results in lower power being dissipated (so faster switching results in less loss). This is dependent on the frequency that the controlling transistors operate at. To be precise, the majority of energy loss occurs when the transistor is neither on nor off. This energy loss takes the form of heat so that the transistor rapidly overheats, resulting in increased on resistance and, eventually, ceases to function.

GaN transistors are capable of switching in 1-2 ns, as opposed to 20-50ns for Si and SiC transistors. Thus, GaNs are in this high energy loss region for almost no time at all and, consequently, they waste very little energy chopping the DC up into variable frequency AC to drive the motor at different speeds. This is the key to QPT being able to reduce energy wastage in a VFD by round 80 percent.

QPT's technology

QPT has integrated its technology breakthroughs into two modules so that they can be easily implemented by customers with minimal effort and changes to existing designs. The qGaN module

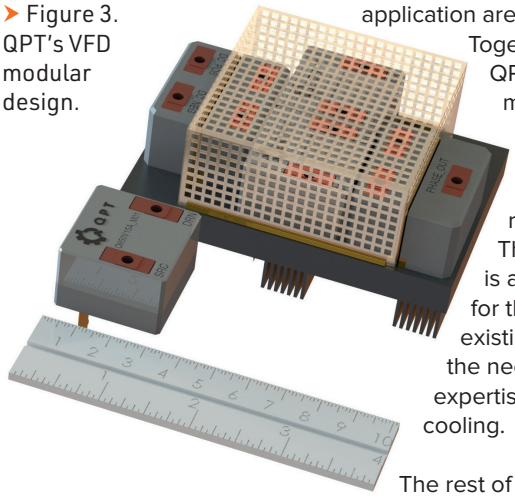


➤ Figure 2. Energy loss during switching.

contains a 650V GaN transistor with the company's qDrive that is the world's fastest, most accurate, highest resolution, low jitter Isolated GaN Transistor Gate Drive. The second module is qSensor that combines the company's ZEST and qSense technologies. It provides the sensing and control that enables the GaN to be driven at super high frequencies for the first time.

In addition, QPT has developed its WisperGaN construction system that includes a reference design for how the modules and the ancillary electronics can be assembled together in a Faraday cage so that there are no heating or RF issues.

The first qGaN module (Q650V15A-M01) will handle 15A RMS current driving 380V three phase motors. The roadmap will have qGaN modules to handle various different power loads to suit different



➤ Figure 3. QPT's VFD modular design.

application area requirements. Together with the other QPT technology modules, turnkey solutions can be easily assembled according to the reference design. The reference design is a drop-in replacement for the power stage of existing VFDs without the need for any specialist expertise in EMC or thermal cooling.

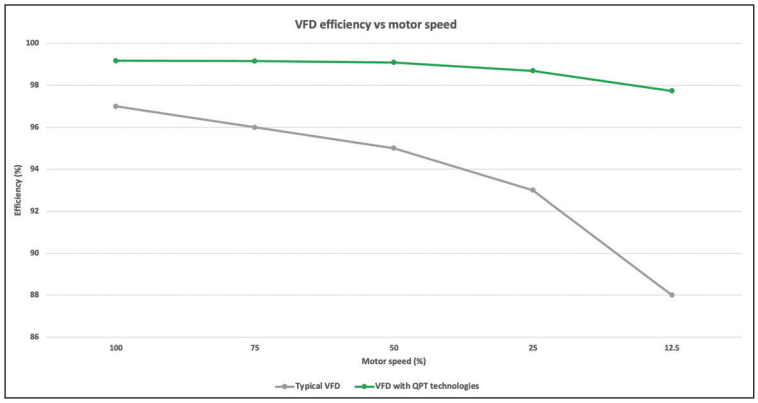
The rest of the existing system such as the microprocessor and software stack stay the same. This makes upgrading a genuine plug and play solution with the benefits of needing less power so it effectively pays for itself in weeks. In addition, there are further savings as the new BOM is less than existing solutions as it does not require external filters. Companies who want to upgrade from their current silicon solutions to be more power efficient can leapfrog over the hassle of developing a SiC solution in house and simply use QPT's new GaN solution.

Variable frequency drives are not as efficient as currently claimed

VFDs work by chopping the incoming power to create a frequency that can be changed to adjust the speed of the motor. Energy is lost every time chopping occurs and, currently, VFD manufacturers believe this to be minimal hence their quoted 97 percent efficiency figure.

However, this figure is at full speed but, in reality, the speed varies and the efficiency drops significantly as the speed drops as shown in figure 2, which is what happens in a real-world operational cycle and is quietly ignored by manufacturers.

It is similar to car manufacturers only quoting fuel usage at the optimal speed and not mentioning the real-world figures of an urban cycle. It is important to note that in most applications, the motor speed is often down at the slow speeds so that the real-world efficiency drops significantly so that there is huge energy wastage that is currently being ignored. QPT's solution unlocks the ability of GaN to now operate at ultrahigh frequencies and deliver 99.7 percent efficiency at peak loads with hardly any decrease in efficiency at lower loads. This equates to up 80 percent reduction in VFD power usage compared to existing solutions that have to operate at much lower frequencies. This is shown as the green line on figure 2.



➤ Figure 4. Shows how typical VFD efficiency drops off dramatically and wastes energy as motor speed drops unlike with QPT technology.

Combining the VFD power saving of around 80 percent with the motor usage gives around 10 percent reduction in overall power usage, which increases in applications where the motor is frequently at low speeds where the current solutions are inefficient.

Increasing the range of electric vehicles

The efficiency of the motor controllers in Electric Vehicles can make a significant difference to their operational range. As explained, using QPT technology can reduce the power usage of the motor and VFD by around 10 percent or even more at low speeds which means either the vehicle goes further or that the battery can be made smaller for the same range.

An additional boost comes from integrating and shrinking the VFD. Current VFDs are bulky, which means that it is invariably located away from the motor itself and then connected by copper cables that are big and heavy to cope with the hundreds of Amps or so going through them. QPT's next-generation GaN technology shrinks the size of a VFD to around a twentieth of the size, reducing weight, and, more importantly, the size reduction means that it can be co-located beside the motor. This integrated motor solution eliminates the need for long heavy copper cables, which can total up to a significant weight and cost reduction at around half a meter each. Additionally, the copper cables have resistance creating power loss and reducing the overall system efficiency. All these factors mean that QPT's solution without copper cables can increase the range of the car.

Reduce power wastage to help combat climate change

The company estimates that the high voltage, high power, hard switching, electric motors application markets where its new technology can be used to provide significant power savings is a Total Addressable Market of $365 billion that includes heat pumps, HVAC, EV and industrial motors. Currently electric motors account for 45 percent of global electricity usage and so by using QPT's technology, they will be more efficient by around 10 percent and that means less carbon dioxide emissions which helps combat climate changes.

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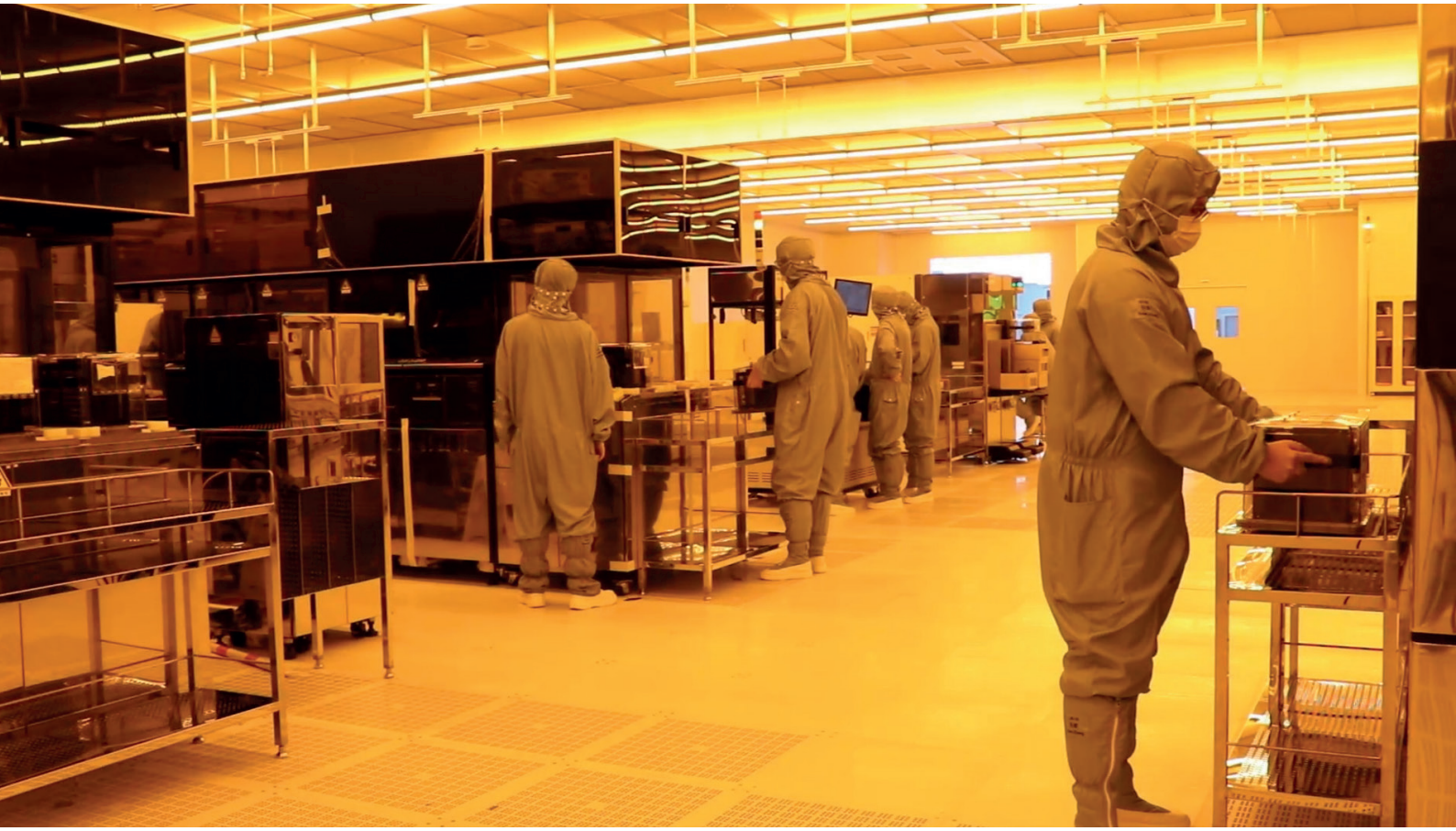


Banishing barriers to GaN adoption

With performance advantages of GaN established and the challenges of driving GaN HEMTs overcome, now is the time to address the outstanding concerns of designers, such as price, availability and reliability

BY DENIS MARCON FROM INNOSCIENCE EUROPE

IT'S NOT THAT HARD to spot the significant benefits that come from replacing silicon power devices with those made from GaN. Consider, for example, e-bike chargers, which are 75 percent smaller when they incorporate GaN, allowing them to fit in a backpack; or USB-PD laptop chargers, which are around one-third of the size of those incorporating silicon-based devices; or data centre DC/DC converters, where the introduction of GaN halves the size and delivers a substantial hike in efficiency.

There are many reasons behind the application advantages provided by GaN, which is now well known for enabling reductions in size and gains in efficiency. One significant asset of devices made from this wide bandgap semiconductor are their absence of reverse recovery current, facilitating simpler architectures. And there are additional benefits, including: GaN's ability to function at a higher frequency than silicon, thereby permitting the deployment of smaller passives; the significantly lower specific on-resistance, allowing GaN devices to be much smaller; and a 10-times-better figure of merit, based on the product of the on-resistance and the gate charge, that leads to far higher efficiencies. As a result, GaN will continue to proliferate in all application areas, including consumer, industrial, automotive and renewables, with uptake increasing the performance of all power conversion systems while trimming size, boosting efficiency and cutting costs.

GaN: the compelling case

Today, the market for GaN is buoyant, thanks to the laying to rest of previous concerns. However, that hasn't stopped some designers of power converters from harbouring doubts that are slowing the mass uptake of GaN. The reasons for this reluctance chiefly centre around price and high-volume availability, but there is also anxiety surrounding second-sourcing.

The smartphone market ably illustrates these points. Despite a slight fall in shipments, well over one billion units are still sold every year, encouraging suppliers of GaN power devices to get their products designed into phone handsets. But before this occurs, four obstacles must be overcome. First, there needs to be a clear advantage behind this move. In addition, the GaN device must replicate the very low gate leakage characteristic of silicon; sell at a competitive price; and be available in massive volumes, to sustain the billion smartphones sold per annum and to meet demand for a quick ramp, to match the 6-to-9 month cadence of new model introduction.

At Innoscience we tick all those boxes. But that's not all. We are innovating, with products such as the market's first bi-directional GaN. This technology, which we refer to as VGaN, delivers clear and compelling benefits. It enables a superior alternative to the conventional approach to blocking current in both directions, which is to use an over-voltage protection unit in a battery management system that features two back-to-back silicon MOSFETs. Thanks to our progress, this pair of transistors can be replaced with a single VGaN HEMT, delivering an alternative that's 50 percent smaller and more efficient (see Figure 1).

One of our breakthroughs has been to address concerns associated with the leakage current. Many designers are not used to having to consider this, because the oxide under the gate of a typical silicon device blocks leakage. The oxide layer is not present in GaN HEMTs, and the gate can be modelled as two back-to-back diodes (see Figure 2).

To reduce leakage, we have optimised the epitaxy, device architecture and processing. Thanks to advances on all these fronts leakage has plummeted by almost a factor of ten, falling to below 3 μA at 85 °C for the lifetime of the device. It's a level of performance that's welcomed by smartphone manufacturers, and one that ensures that VGaN HEMTs are suitable for use as the load switch within handsets.

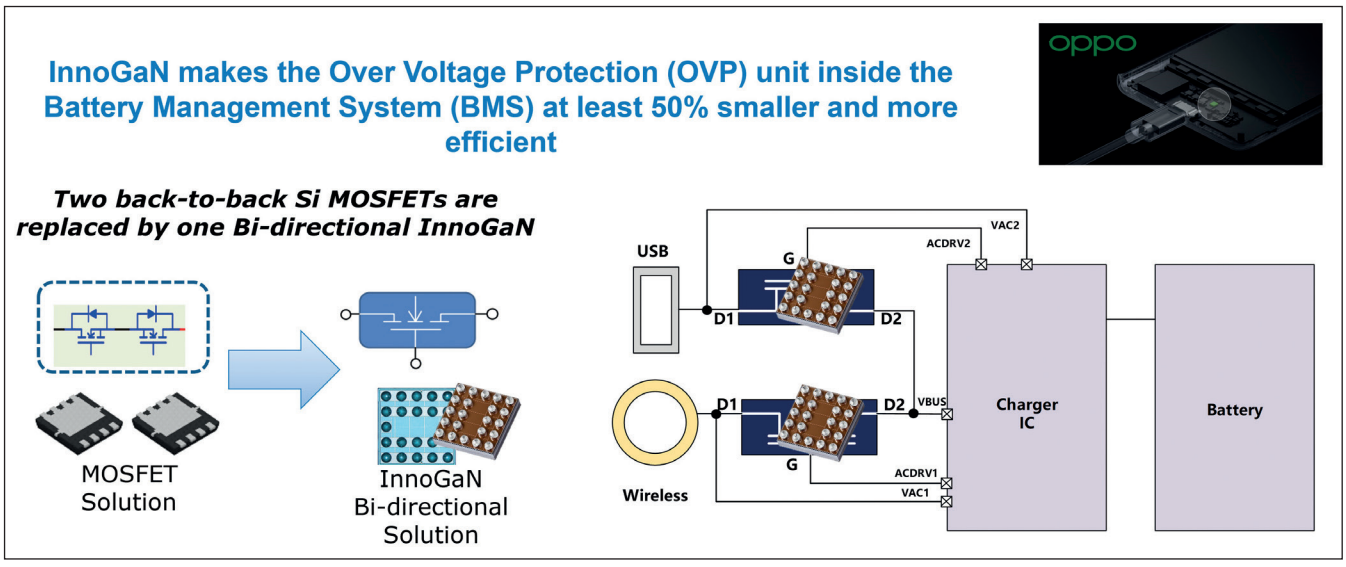
This innovation illustrates that if a company is to be a leading GaN supplier, it must be an integrated device manufacturer. Fabless companies will struggle to innovate, because they do not have the inherent ability to optimise epitaxy, architecture and processing.

If you scrutinise price and availability, you'll soon see why GaN has failed to establish its presence in the smartphone market, despite the growing desire of both customers and suppliers. For a 10 percent market penetration of the one billion phones sold in 2022, makers of GaN power devices would need to produce 100 million units a year. To manufacture this volume requires the processing of either 3,000 8-inch wafers per month, or 5,400 6-inch wafers per month. If for a moment we ignore the capabilities of Innoscience, the total global capacity of GaN is only 16,000 6-inch wafers per month, according to market analyst Yole Intelligence. Consequently, this single application would demand about a third of the world's capacity!

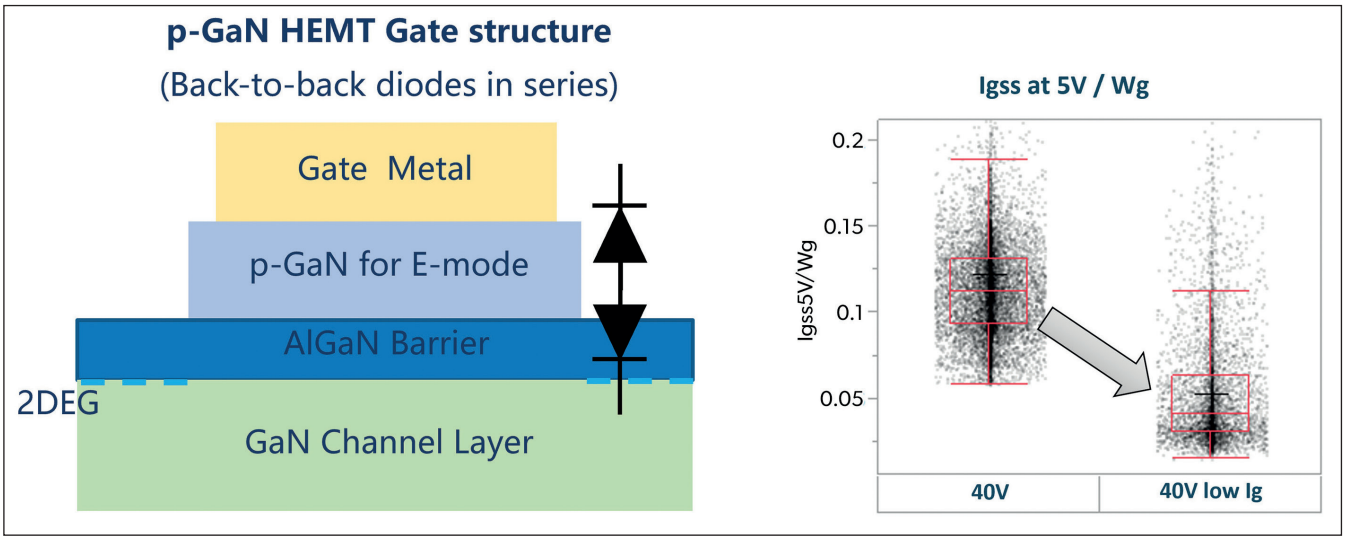
It's a markedly different state of affairs once our capacity is accounted for. We are the biggest integrated device manufacturer completely focused on GaN. By using 8-inch wafers, we can produce GaN devices cost-effectively in extremely large volumes. Our capacity continues to climb, and by 2025 we will be producing 70,000 8-inch wafers every month, dwarfing the combined production of all other manufacturers.

The reliability issue

Crucial to success is reliability. For huge companies, such as the smartphone maker Oppo, GaN could never be incorporated within the handset if reliability were in doubt.



➤ Figure 1. One VGaN can replace two back-to-back silicon MOSFETs.



➤ Figure 2. Optimisation reduces leakage to below 3 μA.

We have demonstrated that our devices are strong in this regard. According to evaluations described by JEDEC and accelerated life tests, we have 10-parts-per-million device failure rates for the gate acceleration factor mode that exceed 20 years (see Figure 3). The equivalent figure for the drain is more than 10,000 years.

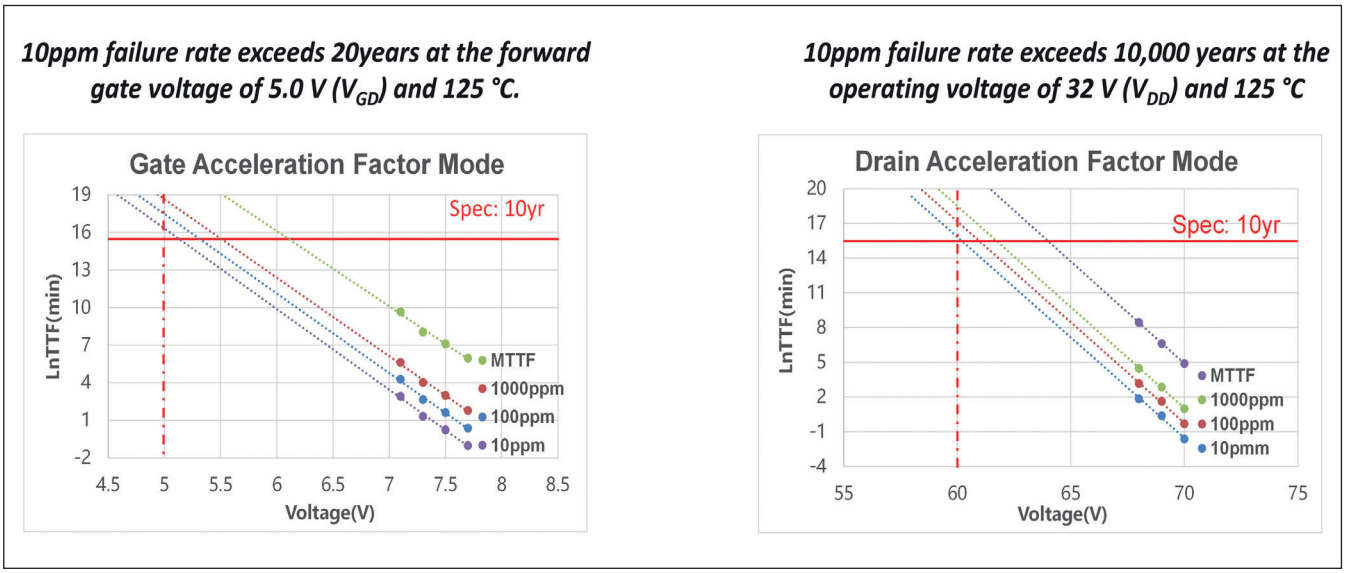
Another crucial factor is avalanche ruggedness, a vital characteristic for silicon power MOS devices. To evaluate this capability, engineers tend to perform an unclamped inductive switching test.

To carry this out, the test device is turned on, causing the inductor to charge at a linear rate. Once the drain current is high enough, the device is turned off, causing the inductor to dissipate its stored energy. This drives the device into breakdown. The avalanching capability of the test device permits the dissipation of the inductor current, therefore restricting any further increase in voltage. The test device remains in breakdown until total energy dissipation.

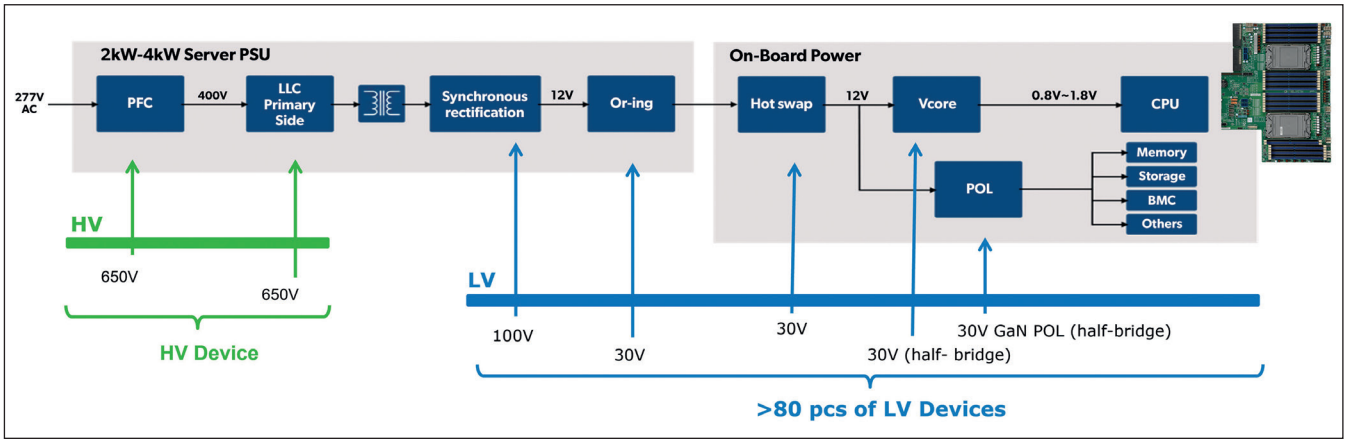
We translate the results of this test into values for the time-in-avalanche and the energy-in-avalanche that the device can support. If the power device does not have avalanche capability, it must offer a far higher breakdown voltage to allow complete energy discharge of the inductor. This is the case for our devices, where a high breakdown voltage fulfils the inductive switching rating. For our low-voltage devices, the breakdown voltage is more than double the device's rating, ensuring that these products handle voltage spikes safely and successfully pass such critical tests.

Data centres

Smart mobile devices are certainly not the only market for GaN. Of the other opportunities, data centres offer a huge and growing market that is exceptionally power-hungry. Here, efficiency is the number one priority. Even an increase in efficiency of just 0.1 percent provides considerable cost savings. The miniaturisation that GaN enables is also valued, with smaller power conversion systems freeing up more space for computing units.



➤ Figure 3. Accelerated life tests highlight the reliability of low-voltage VGaN.



➤ Figure 4. There is huge demand for GaN in power-hungry data centres.

However, to secure sales, GaN suppliers must also offer a large and available product capacity, as well as low prices.

Beginning with the transition from AC to DC, Figure 4 outlines the power conversion phases within a data centre. A normal design at the primary side, incorporating power factor correction and a pair of inductors alongside a capacitor, typically deploys 650 V devices. Meanwhile, on the low-voltage side, it's the norm to use 100 V and 30 V parts when getting down to point-of-load devices. Here, typically as many as 80 or more low-voltage power transistors are used for every implementation. All of these parts must be deliverable in volume and at the right price.

The benefits of our devices are illustrated in a 600 W full-bridge, constructed using a pair of inductors and a capacitor. When built using four of our 3.2 mΩ 100 V GaN INN100W032A HEMTs, the resulting design is just a quarter of the size of that based on a silicon solution, while delivering a 0.6 percent gain in efficiency. This equates to a reduction in energy consumption of almost 10 percent, ensuring significant costs savings and lower CO_2 emissions.

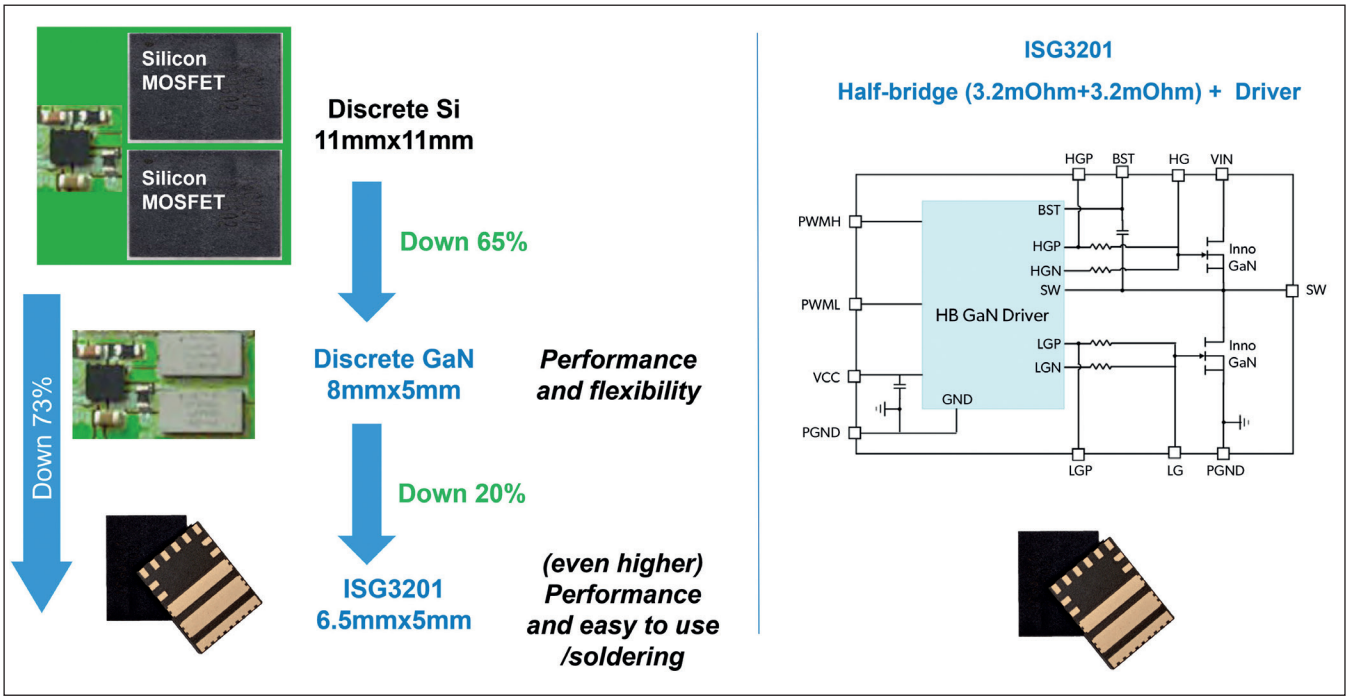
Integrated solutions

Further reductions in size are possible with integration. Consider, for example, our SolidGaN ISG3201, an entire half-bridge circuit that trims size by another 20 percent (see Figure 5). In this single-land-grid array package, measuring just 5 mm by 6.5 mm by 1.1 mm, there are two GaN HEMTs in half-bridge configuration, along with a driver and a bootstrap capacitor.

Note that the benefits of integration are not limited to scaling sizes. This approach also leads to higher performance, due to the package embedding connections between circuit elements. Consider once more the 600 W 48 V/12 V DC/DC converter for data centres. By introducing the ISG3201, designers can increase the power density and reach 1000 W in the same-size module at a heightened efficiency of 98.26 percent. This gives our customers the chance to choose between: a discrete solution, such as the INN100W032A, which offers greater flexibility; and an integrated solution, such as the ISG3201, which is easier to mount and use.

We have also directed our attention at the high-voltage sector with a portfolio of 650 V HEMTs with on-resistances ranging from 30 mΩ to 2.2 Ω. Again, we are aware that some designers will have concerns relating to avalanche failures due to high-voltage spikes. Once more, our approach to addressing this is to ensure headroom in the blocking voltage. Since GaN transistors – unlike those made from silicon – do not have an avalanche rating, the only way to avoid this form of failure is to select a device with a much larger breakdown voltage than the specified voltage rating. Our 650 V-rated devices can withstand non-repetitive pulses below 200 µs at up to 800 V, which is well above the maximum rating. When the duration of the repeat pulses shortens to below 100 ns, the maximum transient voltage our component can maintain falls to 750 V, both at room temperature

➤ Innoscience produces devices at its 8-inch fab in Suzhou, China.



➤ Figure 5. Integrated SolidGaN solutions offer size, performance and ease-of-use benefits.

and at 125 °C. This is still far beyond the 650 V rating, and adds to our collection of data that supports very reliable use.

Dual sourcing

For very good reason, some of our customers are reluctant to rely on a single supplier. But they don't have to, as multiple sources of GaN parts are emerging. For example, our 650 V/700 V devices in a DFN 8x8 or 5x6 package are pin-to-pin compatible with parts with a similar rating and specifications. What's clear is that there are no longer any barriers to GaN adoption in the mass power semiconductor market. Gone are the days when there would be concerns related to high-volume availability, price, compatibility between manufacturers, reliability at both low and high voltages, and avalanching. In short: the future is GaN.

Reducing the on-resistance with a strain layer

INNOSCIENCE'S GaN HEMTs are intrinsically enhancement-mode (E-mode) devices.

This much-preferred, fail-safe mode of operation, which is known as normally-off, is realised by growing a *p*-GaN layer on top of the AlGaN barrier, followed by the deposition and patterning of a gate metal and the selective recessing of the *p*-GaN layer over the AlGaN barrier. The gate metal layer forms a Schottky contact with the *p*-GaN layer and, as a consequence, the potential in the channel at the equilibrium is elevated to ensure normally-off operation.

By controlling all its manufacturing process stages in-house, Innoscience has been able to develop several technology improvements that have been key to optimising GaN HEMT manufacture for high performance and reliability, as well as mass production and cost reduction.

One of the critical parameters that determines transistor performance is $R_{DS(on)}$ – this is the total drain-source on-resistance per unit area. $R_{DS(on)}$ determines the maximum possible current rating of the switch and influences current loss, and thus efficiency. Consequently, by minimising the specific $R_{DS(on)}$, engineers can trim device size for a given on-resistance, and ultimately produce more parts per wafer, cutting costs.

To reduce specific $R_{DS(on)}$, Innoscience has developed a strain enhancement technology. A strain enhancement layer is deposited onto the wafer, immediately after the gate stack definition. Stress modulation created by this strain-enhancement layer induces additional piezoelectric polarisations; this causes the density of the two-dimensional electron gas to increase, leading to a fall in sheet resistance by 66 percent when compared with a device without the strain layer.

Crucially, since the strain enhancement layer is deposited after gate formation, it only affects the resistance in the access region. There is no impact to other device parameters, such as threshold and leakage. Thanks to this patented technology, Innoscience's GaN-on-silicon E-mode HEMTs exhibit a very low specific on-resistance.

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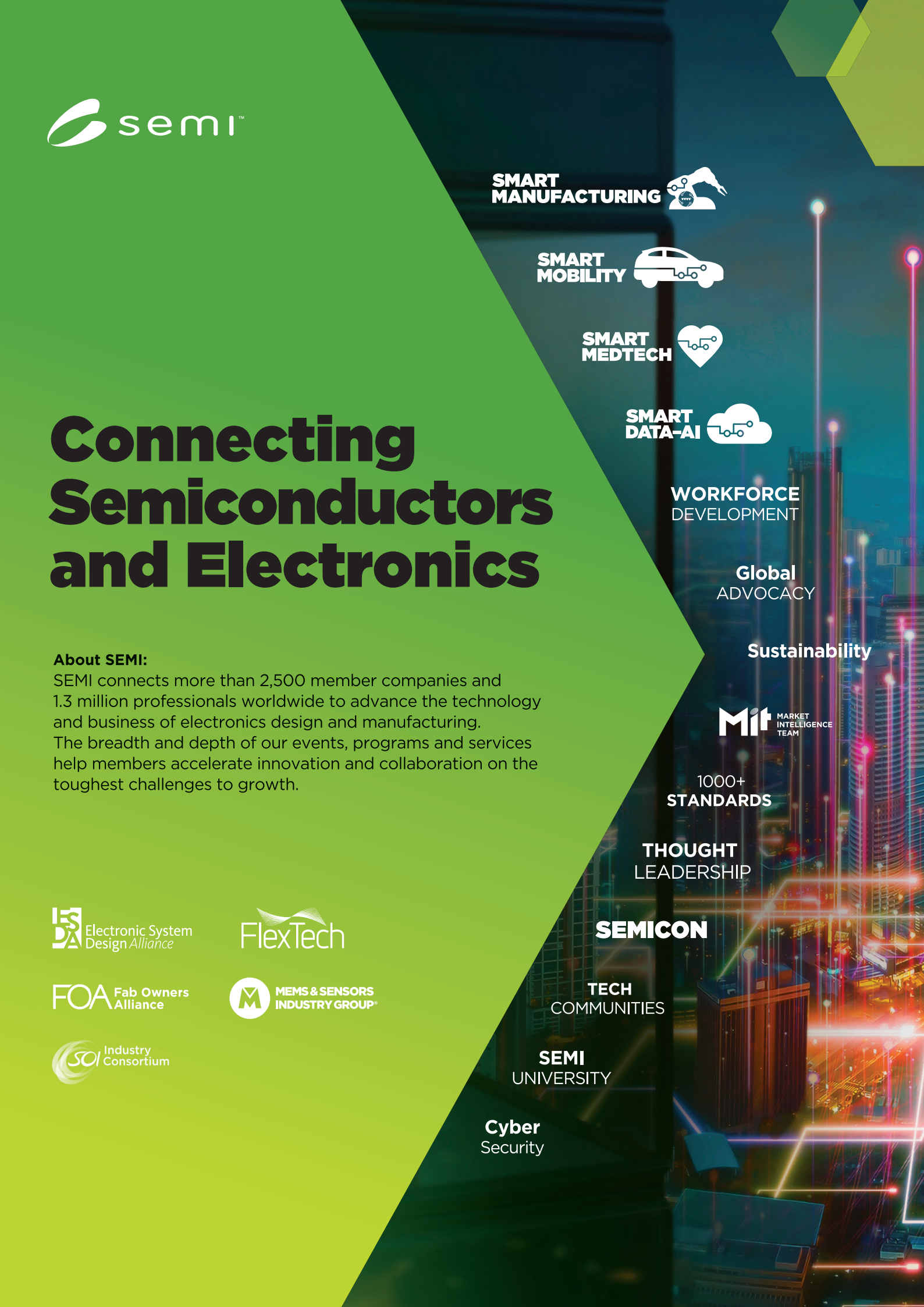


Evaluating the pros and cons of power GaN

Switching to a vertical architecture addresses concerns associated with on-resistance and capacitance, but the choice of substrate involves compromise

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THE OUTLOOK for the GaN power device is incredibly positive. Spurred on by ramping revenues for power supplies in the consumer, telecom and datacom sectors, sales are sure to rocket over the next few years. According to the French market analyst Yole Intelligence, total revenue is going to eclipse $2 billion by 2027 – that's massive growth, considering sales in 2021 were worth just £126 million.

Yet despite all this success, GaN power devices are far from perfect. The harsh reality is that there are many opportunities for improvement. And while some progress might be baked into the upbeat forecast by Yole, it is clear that the more that's done to eradicate weaknesses, the better the long-term prospects for this class of power electronics.

At this year's CS Mantech, held in Orlando, Florida, in mid-May, the most noteworthy weaknesses of the GaN power device were discussed in detail by Mariko Takayanagi, a Senior Manager from Toshiba Electronic Device and Storage Corporation. Several speakers that followed Takayanagi discussed switching to a vertical architecture, which is one option for addressing some of the weaknesses of the traditional power device. Those pursuing a vertical architecture include: Travis Anderson, from the US Naval Research Lab, who detailed the scalable manufacture of planar and vertical *p-i-n* diodes; Dinesh Ramanathan from NexGen Power Systems, who outlined what is claimed to be the world's first commercially available GaN-on-GaN technology; and Eldad Bahat Treidel from FBH, Berlin, who described efforts to develop and characterise high-quality drift regions in vertical devices.

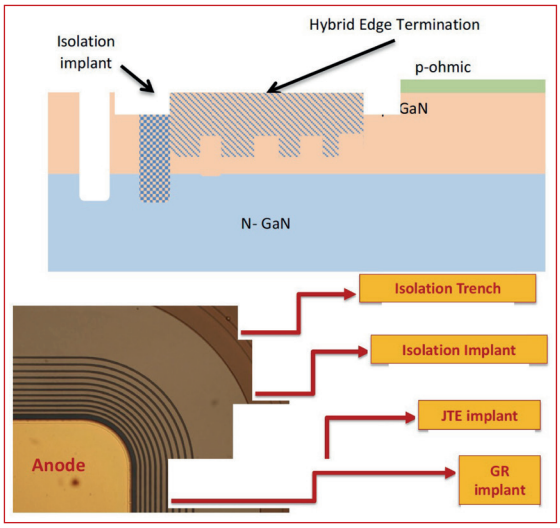
➤ Bristol University's Martin Kuball chaired this year' s CS Mantech. Taking over the reins for 2024 is Peter Ersland from MACOM.

Lateral limitations

Takayanagi, who works for one of the largest and most established makers of power devices in the world, pointed out that according to market forecasts, for the next few years sales of SiC devices will be worth far more than those for GaN, despite the latter having superior potential, based on Baliga's figure of merit. The reason for this, argues Takayanagi, is that circuit designers cannot simply swap a silicon power device for one made from GaN.

Two of the great strengths of GaN are its very high values for mobility and saturation velocity. Together, they ensure that devices made from this material switch at frequencies that are more than an order of magnitude higher than those of silicon incumbents. Switching at far higher frequencies is a very valuable asset, because it tends to enable the introduction of far smaller passive components, particularly inductors and transformers. In turn, this enables a trimming of the size of electrical units. What's more, reverse recovery losses are close to zero, thanks to the non-existence of an anti-parallel body diode. This ensures that a low switching loss is even sustained at high frequencies.

The upshot of all these merits is the possibility to produce power-conversion equipment that is relatively small, while operating at very high power densities and efficiencies. All these strengths are valued by the designers of AC adaptors, micro-invertors, server power supplies and 5G/6G base stations.



➤ Figure 1. The architecture (top) and an optical image (bottom) of the vertical *p-i-n* diodes developed at the Naval Research Laboratory, in collaboration with researchers at Vanderbilt University and Sandia National Labs.

Unfortunately, increasing the switching frequency with the introduction of GaN devices can bring its own problems. When moving to megahertz switching, electromagnetic noise may arise in regulated frequency domains. Rules are in place for good reason, as noise suppression is needed to avoid the erroneous turn-on of GaN power devices – if this were to happen, it could lead to a ground fault in power electronic equipment.

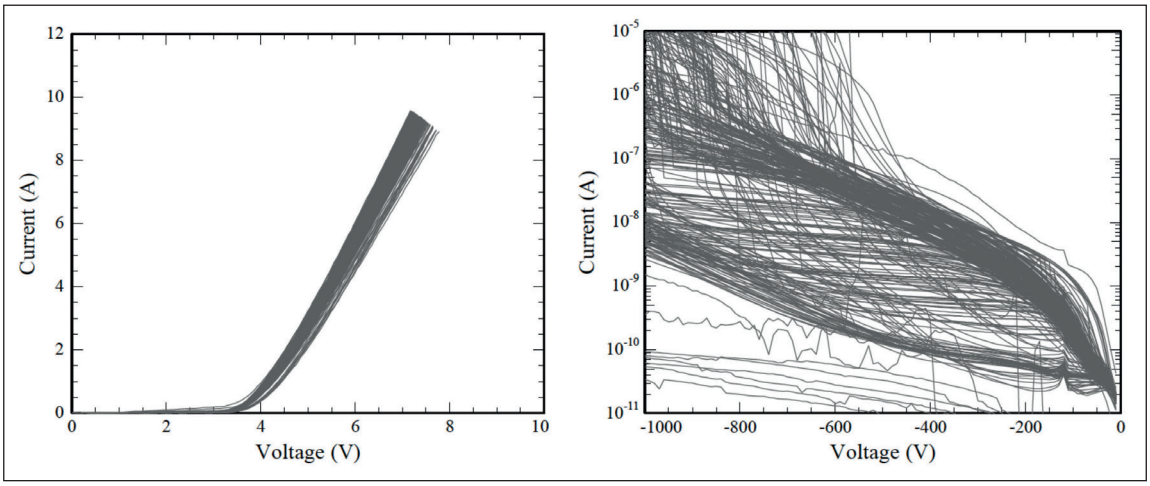
According to Takayanagi, the solution to combining a high efficiency at a high switching frequency with low noise generation is to minimise parasitic inductances and capacitances. This can be realised by placing the gate drive and the GaN power semiconductors as close to one another as possible, while minimising the parasitic inductances between the device terminals of a discrete power device.

It is a requirement that is included in what Takayanagi considers to be the three key criteria for the GaN power device, judged from an application viewpoint. These three pillars are: the need for a low on-resistance and parasitic capacitance, to ensure good switching characteristics, low energy loss and low noise; a threshold voltage that's above around 2.5 V, so that the device is immune to noise and will provide fail-safe operation; and a low overall cost.

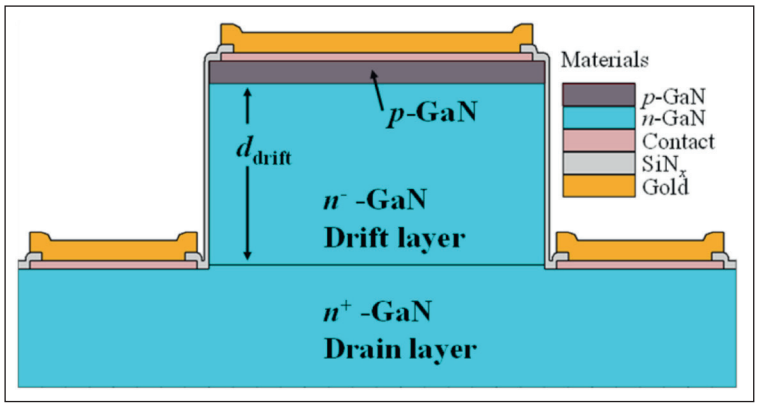
The three classes of GaN power devices on the market today are different forms of HEMT. There is the normally-on transistor, which may also be described as a depletion-mode device; the normally-off transistor, also known as an enhancement-mode device; and the cascode variant. Takayanagi has evaluated the pros and cons of these three designs of HEMT.

Merits of the normally-on transistor, which is on when the gate is biased to zero, include a very high mobility and a zero reverse recovery capacitance, traits that are preferable for high-frequency switching. However, this class of HEMT has a threshold voltage around -10 V, with less than -15 V required to ensure turn off. According to Takayanagi, having the device on at zero gate bias is fatal for power conversion applications, as it requires engineers to put great effort into designing circuitry and gate control, to ultimately ensure safety. The additional circuitry increases parasitics and costs. Due to this, normally on HEMTs are unable to provide high efficiency, high power density and low noise.

Introduced to address issues surrounding the normally-on HEMT is the variant with a cascode configuration. In this case, the normally-on HEMT is connected in series to a silicon low-voltage MOSFET – the source terminal of the MOSFET is connected to the gate terminal of the normally-on HEMT. As a commercial gate driver may be used, there are no concerns relating to cost. But there are concerns associated with the reverse recovery capacitance and the additional on-resistance of the low-voltage MOSFET. It's possible to address these weaknesses by changing the configuration of the MOSFET and HEMT, but that introduces special drivers, additional



➤ Figure 2. Vertical *p-i-n* diodes under forward and reverse bias have uniform turn-on characteristics, but a very broad distribution in breakdown behaviour.



➤ Figure 3. The reverse bias of a FBH Berlin *p-n* diode with a drift region doped to 4 x 10^{16} cm^{-3} shows avalanche behaviour.

components, a power supply and the need for sophisticated control. The third class of commercial HEMT, which is described as normally-off, promises to be the ultimate solution to all three of Takayanagi's criteria. This mode of operation may be realised with a *p*-GaN gate, which is unfortunately sensitive to over-voltage. Addressing this particular weakness is the commercially available hybrid-drain embedded gate injection transistor, which maintains zero recovery capacitance and is blessed with an on-resistance that is considerably lower than that of cascode devices. However, the threshold voltage is less than +2 V, which is just shy of what a power electronic engineer desires, according to Takayanagi. This means that there is the threat of erroneous turn-on. Additional concerns are the need for a dedicated driver to provide a current source, and some reliability issues, such as instability due to trapped charges.

➤ The winner of this year's CS Mantech 2023 Best Student Paper Award went to Yulin He for her paper *Hybrid Etching Process on Type-II GaAsSb/InP DHBT for 5G and Millimetre-Wave Power Amplification*.

To enable GaN transistors to fulfil their potential, demonstrated by their excellent value for the Baliga figure of merit, Takayanagi suggests a need to switch to a different device architecture that combines a high threshold voltage with a low on-resistance and a low capacitance.

Offering promise on all these fronts are vertical GaN transistors. Ideally they are grown on a native foundation, as they require thick drift layers, so demand lattice matching of the substrate and epistructure.

Pilot production

In the US, a collaboration that's led by the US Naval Research Laboratory and includes researchers at Vanderbilt University and Sandia National Labs, has established a pilot production line for producing vertical GaN diodes. A major motivation for this work is to address significant challenges that are holding back the mass production and widespread adoption of vertical GaN devices. According to the team, the relationship between substrate specifications and device performance is not well understood, ion implantation technology for selective-area *p*-type doping is not reliable, and there is a poor understanding of device failure mechanisms, due to a lack of large data sets from electrical stressing.

Efforts by the partnership have focused on a comprehensive study of incoming metrology and wafer mapping. The team has developed a fully planar device process for making diodes, which can be scaled to provide practical voltage and current levels – the target is 10 A and 1.2 kV.

Key accomplishments by the team include establishing pass/fail criteria for incoming epitaxial layers, and identifying the impact of substrate and epiwafer defects on device performance. To succeed in this endeavour, they are producing a large quantity of devices, with more than 500 coming from every wafer. By employing a constant process, the engineers can directly probe the effect of scaling to large-area devices and to layers designed for higher voltage operation, such as 3.3 kV.

The pilot line uses 50 mm free-standing GaN wafers. Spokesman for the team, Travis Anderson from NRL, accepts that this size is not ideal for cost-effective high-volume manufacturing. He told *Compound Semiconductor* that high volume fab infrastructure available for supporting 50 mm wafers is not really available, and yield suffers when attempting to make devices of practical size – that is, greater than 1 mm^2 – due to the limited available area.

"At 100 mm it becomes much more feasible for a

true production environment," added Anderson. "However, 50 mm is more than sufficient for a manufacturing demonstration to evaluate process stability in an R&D environment, which was the goal of our efforts."

There are concerns related to the cost, size and level of availability of GaN substrates. "I do not think the cost is prohibitive, particularly as 100 mm wafers are emerging," argues Anderson, who says that over the course of his collaboration's four-year programme, they have seen a significant shift in the economics of GaN wafers. "Even though the price has only modestly decreased, the quality and uniformity of the wafer has improved substantially, which improves our process yield." During the project, the team had no difficulty securing wafers from multiple sources. However, it should be noted that the total number of wafers they have used is not that high.

Anderson and his co-workers used their line to produce 1.2 kV diodes with an 8 µm-thick drift layer doped to 1 x 10^{16} cm^{-3}, and 3.3 kV variants with a 25 µm-thick drift layer doped to 4 x 10^{15} cm^{-3}. These devices featured an anode with dimensions varying from 300 nm to 500 nm, and a doping level from 3 x 10^{17} cm^{-3} to 2 x 10^{19} cm^{-3}.

"The *p-i-n* diode is an ideal test vehicle to understand the fundamentals of a GaN *p-n* junction," says Anderson. "Since the *p-n* junction is the building block of more complicated diodes and FETs, we chose to study the *p-i-n* diode first as a test vehicle to prove that we can reliability make high quality *p-n* junctions, evaluate edge termination processes, and study scaling to high current before moving to more complex three-terminal structures."

The metrology applied to the incoming wafers includes: C-V mapping with a mercury probe, to calculate doping and uniformity; optical profilometry; and X-ray diffraction mapping. The optical profilometry data is analysed with a machine learning algorithm that identifies bumps, pits, and regions of high roughness.

Anderson says that machine learning has been extremely helpful: "As we worked through the fabrication process, we used machine learning to correlate incoming metrology data to device performance data. By working with these data sets, we were able to develop algorithms to develop the appropriate incoming wafer and epi requirements, screen out wafers that would not yield well, and identify non-intuitive mechanisms that would impact device performance."

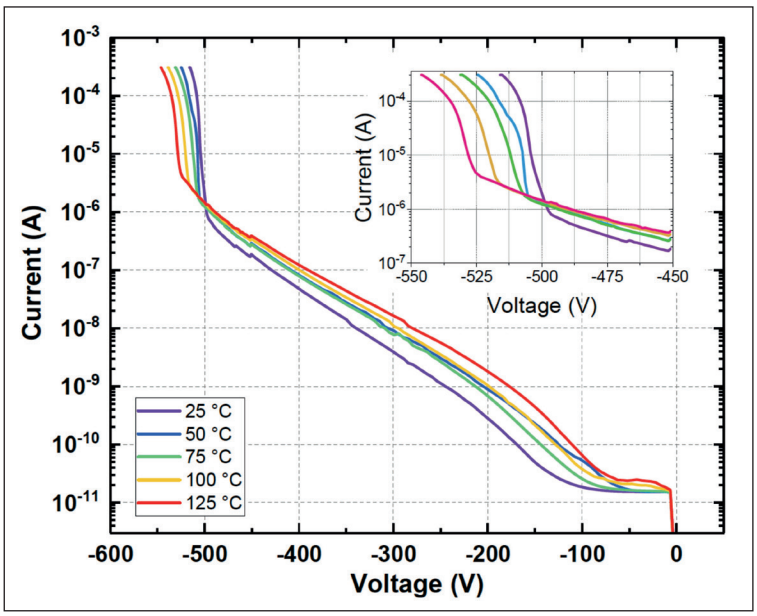
Following metrology, wafers are cleaned, before edge termination is realised using a multi-step nitrogen implant box file. This step isolates devices through the *p*-GaN layer and forms an edge termination region that utilises the hybrid structure, which consists of a junction termination extension region, with guard regions superimposed via a spacer layer (see Figure 1). After cleaning, a front side *p*-ohmic metal contact and a backside *n*-ohmic metal contact are deposited.

Electrical measurements under forward bias have produced varied results. On an exceptional wafer, diodes have a highly uniform turn on, a low leakage and high current capability (see Figure 2 (a)). This is said to be indicative of a high-quality *p-n* junction and relatively few pinholes in the film. However, on inferior wafers many devices suffer from premature turn-on, due to shorting of the anode metal to the substrate. This is caused by pinholes in the epitaxial layer, due to particles introduced in the growth process.

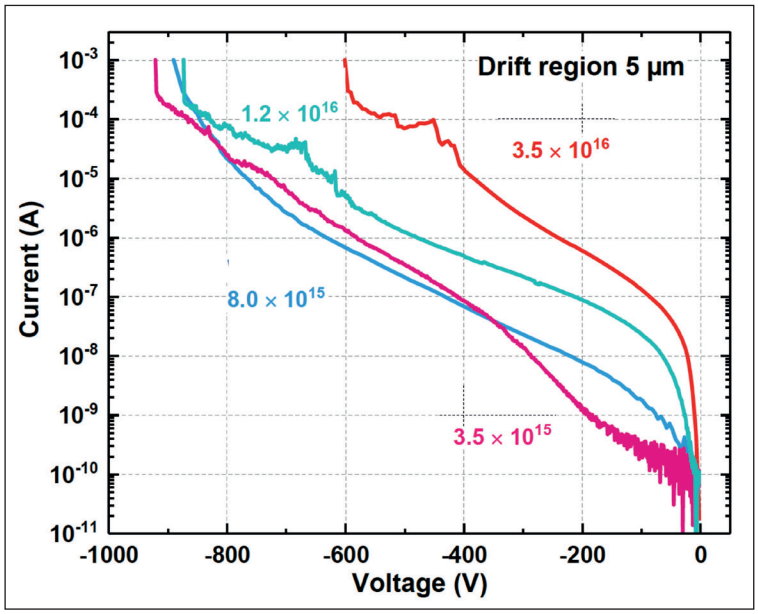
Anderson and co-workers find a very broad distribution in the breakdown behaviour of their diodes (see Figure 2 (b)). For the best discrete devices, breakdown is 1.4 kV, with a leakage below 1 nA at up to 1 kV. But there are also many devices with a high leakage at a voltage just half that of breakdown.

The team are yet to determine the mechanism behind the wide variation in breakdown behaviour. However, they speculate that it could come from localised variations in drift layer properties, arising from variations in miscut or epitaxial defects.

Efforts have been directed at optimising the edge termination design, critical to realising an abrupt avalanche breakdown. The team varied the anode thickness, which ensured a systematic variation in the thickness of the remaining *p*-GaN layer. This led them to discover that they could slash the leakage current under reverse bias by more than two orders of magnitude by thinning the underlying *p*-GaN layer to less than 10 nm.



➤ Figure 4. The reverse bias of a FBH Berlin *p-n* diode with a drift region doped to 4 x 10^{16} cm^{-3} shows avalanche behaviour.



➤ Figure 5. For *p-n* diodes with a drift region doped to 3.5 x 10^{16} cm^{-3}, plots of reverse bias reveal a hard breakdown.

Encouragingly, the team can report two observations that are consistent with avalanche breakdown. One is an increase in the breakdown voltage at elevated temperature; and the other is the moving of an electroluminescence spot from the edge of the isolation implant to the edge of the anode.

Anderson and his colleagues noted a substantial variation in diode performance from wafer-to-wafer. This is attributed to either variations in the epitaxial layers, such as drift layer doping or anode doping, or to differences in the back side of the wafer.

The team have also investigated packaged devices, developing a surface mount process using a commercially available package and outsourced mounting and wire bonding. Following packaging, devices are encapsulated with Hysol. This led to improved performance and no device degradation, benefits that are attributed to passivation.

Having completed fabrication of many devices, one of the plans for the team is to work with circuit designers to evaluate devices in practical applications.

"I am also interested in probing device reliability to understand failure mechanisms," adds Anderson. "Finally, I see large-area devices as a challenge and am interested in continuing to scale device size."

Commercialising GaN-on-GaN

Details of what is claimed to be the world's first commercial GaN-on-GaN power technology were described by co-founder of NexGen Power Systems, Dinesh Ramanathan. This Californian outfit, which is now sampling 700 V and 1200 V enhancement-mode JFETs – full production is slated for later this year – boasts that its devices have a superior breakdown voltage and current capability for a given chip area up to 4 kV, compared with any other GaN device, as well as low capacitance and switching losses. Other attributes are said to include: repeated cycle avalanche robustness, thanks in part to the *p-n* junction; a best-in-class temperature coefficient; and the smallest size, compared with other power semiconductors, for a given current rating.

Ramanathan discussed solutions to many of the challenges associated with the manufacture of GaN-on-GaN devices. To enable high-volume manufacturing, NexGen employs widely available manufacturing tools, modified to handle the transparent, fragile GaN substrates. The company is working with substrate vendors to improve substrate characteristics, such as surface finish, flatness and the level of macro-defects. In addition, efforts are directed at improving NexGen's epitaxial process, as well as etching and cleaning techniques that can aid the quality of the regrown junction, and the development of novel test structures to improve quality control.

Developing drift regions

A key element in vertical power devices is the drift layer. Evaluating its characteristics using a full device structure is a time-consuming process, so to speed this assessment a team from FBH, Berlin, have been developing approaches based on the use of process control measurement (PCM) structures.

At last year's CS Mantech FBH's Eldad Bahat Treidel outlined a PCM structure for measuring the drift region conductivity, and at this year's meeting he detailed further progress – values for the blocking strength are now possible.

Treidel told *Compound Semiconductor* that the time it takes to produce a PCM structure is just a third of what it would take to fabricate a complete transistor. What's more, it is simpler and cheaper. "For example, process and full wafer characterisation of a PCM structure would require 6 lithographic layers as compared to a full transistor process with 12 to 15 lithographic layers."

In the work described in Orlando this May, Treidel produced *p-n* diodes that target avalanche behaviour, which is a desirable attribute, as it combines the maximum blocking in the drift region with the highest conductivity.

"In addition, avalanche breakdown is controllable, repeatable, can be predicted and it's nondestructive and recoverable," adds Treidel, who points out that these strengths enable a significant reduction in the device design margin between the rated voltage and the real breakdown voltage. "Further, [avalanche] improves short-circuit robustness and ruggedness."

The team produced its *p-n* diodes on sapphire substrates. They have been developing vertical GaN-based power devices on foreign substrates, such as sapphire and silicon, through a Europen project called YESvGaN. As well as issues associated with wafer bow, substrate removal

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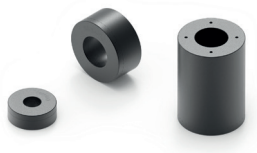

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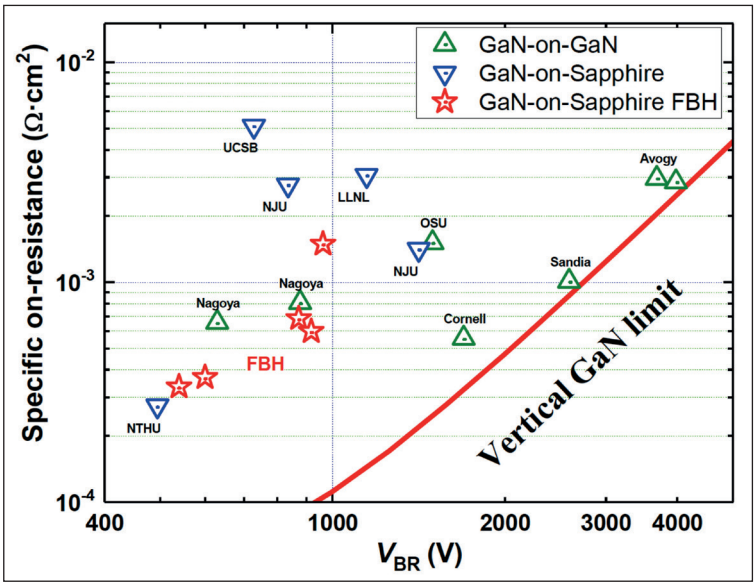
Those at FBH will be developing a number of gate module technologies, such as trench MOSFETs, finFETs and finJFETs. It is possible to integrate these technologies on native and foreign substrates

and processing of membranes, they have had to consider the high defect density in the drift layers that threatens to limit the blocking strength, reduce the conductivity of the drift layer and impact channel inversion.

None of these issues have proved showstoppers for Treidel and his colleagues. "In the frame of this project we have demonstrated high-quality epitaxial layers with avalanche capability and low resistivity for both GaN-on-sapphire and GaN-on-silicon."

The engineers at FBH fabricated diodes from five GaN epistructures with drift regions with different doping concentrations, all grown on 100 mm sapphire substrates. All these variants, grown by MOCVD, had epitaxial stacks consisting of a 2.2 μm-thick unintentionally doped GaN buffer layer, a 2.4 μm-thick highly conductive drain layer, and a 5 μm-thick drift layer. After determining the doping concentration of the drift layer by electrochemical capacitance-voltage measurements, these structure were loaded into another MOCVD reactor, where a 500 nm-thick layer of magnesium doped at a concentration of 1 x 10^{19} cm^{-3} was added, followed by a 30 nm-thick layer of GaN doped to 2 x 10^{19} cm^{-3}, prior to *in-situ* activation. Quasi-vertical *p-n* diodes were formed from these epiwafers by first applying rapid thermal annealing to remove hydrogen from the *p*-type layers, before using optical lithography and etching to define mesa structures. Ohmic *p*-type and *n*-type contacts were then formed, before the passivation of the mesa edges via plasm-enhanced CVD added 200 nm of SiN (see Figure 3).



➤ Figure 6. The *p-n* diodes fabricated at FBH, Berlin, deliver an impressive performance for variants that have a sapphire foundation.

Electrical measurements on all the devices determine that it is just the variant with the highest doing in the drift region – it's doped to 4 x 10^{16} cm^{-3} – that exhibits avalanche behaviour (see Figure 4). The other four, with doping in the drift region varying from 3.5 x 10^{16} cm^{-3} to 3.5 x 10^{15} cm^{-3}, undergo a non-avalanche hard breakdown (see Figure 5). According to the team, these findings indicate that as the concentration of doping in the drift region reduces, there is a shift from the parallel plane junction (avalanche) regime to the punch-through breakdown limit.

Triedel and co-workers have benchmarked their devices against other *p-n* diodes on GaN and sapphire substrates (see Figure 6). It is claimed that the device with a 1.2 x 10^{16} cm^{-3} level of doping in the drift region offers excellent blocking performance, with a hard breakdown of 920 V, a drift region specific resistance of 0.57 Ω cm^2, and a power figure of merit of 1.43 GW cm^{-2}.

One of the team's next targets is to develop the growth of GaN layers that are as thick as around 15 μm on sapphire substrates, because this will enable devices to block more than 1.5 kV while exhibiting a specific resistivity of around 1 mΩ cm^2. "For this we have developed a strategy to reduce the internal built-in strain in the substrate, and by that to reduce the wafer bow," says Treidel.

In parallel, those at FBH will be developing a number of gate module technologies, such as trench MOSFETs, finFETs and finJFETs. It is possible to integrate these technologies on native and foreign substrates.

"Our device processing activities for vertical GaN devices on native and foreign substrates will enable us to study the impact of GaN layer material quality on device performance and reliability," adds Treidel. The GaN-on-GaN will also enable the team to investigate the influence of different substrate manufacturing methods, such as HVPE and ammonothermal growth, and compare material supplied by different vendors.

Such efforts will help to advance the capabilities of vertical GaN devices, which offer many advantages over their lateral cousins. Progress on both these fronts may well be discussed at the next CS Mantech, which will take place in Tucson, AZ, from 20-23 May 2024.

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Better FETs with bulk AlN

A native foundation equips nitride FETs with a higher drain current and lower thermal impedance

ENGINEERS from the University of South Carolina are claiming to have raised the bar for the performance of nitride FETs with an aluminium-rich AlGaN channel.

The team's devices, grown on bulk AlN, are said to break the record for the Baliga's figure-of-merit for this class of transistor. For that metric – the square of the breakdown voltage, divided by the specific on-resistance – the researcher's FETs have a value of 460 MW cm^{-2}.

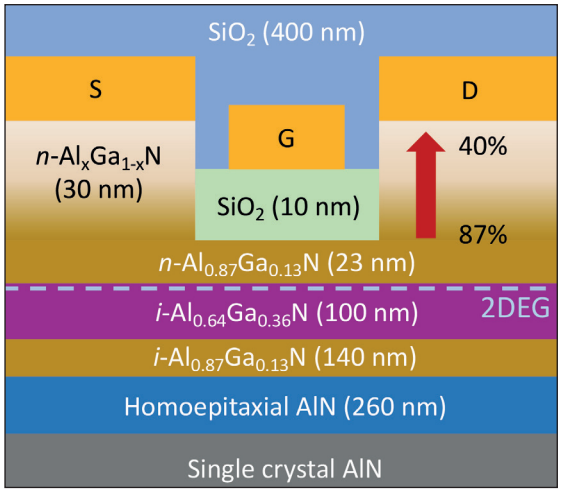
According to these engineers, their devices could improve the performance of nitride-based transistors in consumer chargers and next-generation electric vehicles. Advances have come from addressing thermal limitations with AlN substrates, which are blessed with a high thermal conductivity.

Metal-oxide-semiconductor FETs were fabricated on a 400 μm-thick single-crystal AlN substrate grown by physical vapour transport and purchased from HexaTech. Engineers loaded this substrate into a low-pressure MOCVD reactor and deposited an epitaxial stack consisting of a 260 nm-thick AlN layer, a 140 nm-thick $Al_{0.87}Ga_{0.13}N$ back-barrier, a 100 nm-thick $Al_{0.64}Ga_{0.36}N$ channel, a 23-nm thick *n*-type $Al_{0.87}Ga_{0.13}N$ barrier, and a 30 nm-thick graded AlGaN layer that's silicon-doped and designed to support the formation of ohmic contacts.

Device fabrication began by using reactive-ion etching to form a mesa. Electron-beam evaporation added source and drain contacts, which were annealed, before a second etching step removed the graded layer from the access region, prior to the introduction of a 10 nm-thick layer of SiO_2 that serves as the gate oxide. After electron-beam evaporation added gate and probe pads, devices were embedded in a 400 nm-thick SiO_2 film by plasma-enhanced CVD to relieve the surface electric field during breakdown measurements. To provide a control, identical structures were fabricated on an AlN template, formed by depositing a 3 μm-thick layer of AlN on sapphire.

Electrical measurements on FETs with a gate length of 1.8 μm, a gate-to-source distance of 1.2 μm, and a gate-to-drain distance of 2.64 μm, exhibited clear saturation and pinch-off. Peak currents of 610 mA mm^{-1} and 410 mA mm^{-1} were recorded for devices on the native substrate and template, respectively.

Thermal droop is seen in the FET with the sapphire foundation, but not in the variant built on AlN. The lack of droop is said to result from superior thermal management. Thermal impedance measurements reveal a value of 10 K mm W^{-1} for the device on AlN, and 31 K mm W^{-1} for that on sapphire.



➤ Fabricated on single-crystal AlN, the nitride FET produced at the University of South Carolina has a thermal impedance of just 10 K mm W^{-1}.

The team attributes the far lower thermal impedance, which is supported by an 8-fold higher thermal conductivity for AlN than sapphire, to the higher value for the peak current.

Due to the presence of the SiO_2 gate insulator, the team did not expect to see any difference in reverse leakage current between the two types of device. But leakage in the sapphire-based device is noticeably higher at positive gate voltages, a finding that is said to require further study.

The peak value for transconductance – the product of channel mobility and gate capacitance – hit 45 mS mm^{-1} in the FET on AlN, compared with 34 mS mm^{-1} for the variant on sapphire. As the gate capacitance is similar in both devices, the superior transconductance in the device on the native foundation is thought to be associated with an inferior mobility, which gives rise to thermal droop.

At a gate-source voltage of -30 V, device breakdown is 959 V, leading to a 'conservative' estimate for Baliga's figure-of-merit of 460 MW cm^{-2}. It is argued that because the annealed contacts are unlikely to produce an isotropic in-plane two-dimensional electron gas, a reasonable upper bound for the figure of merit is more than 750 MW cm^{-2} – that's claimed to be ten times higher than other results for FETs on AlN, and represents the state-of-the-art.

REFERENCE

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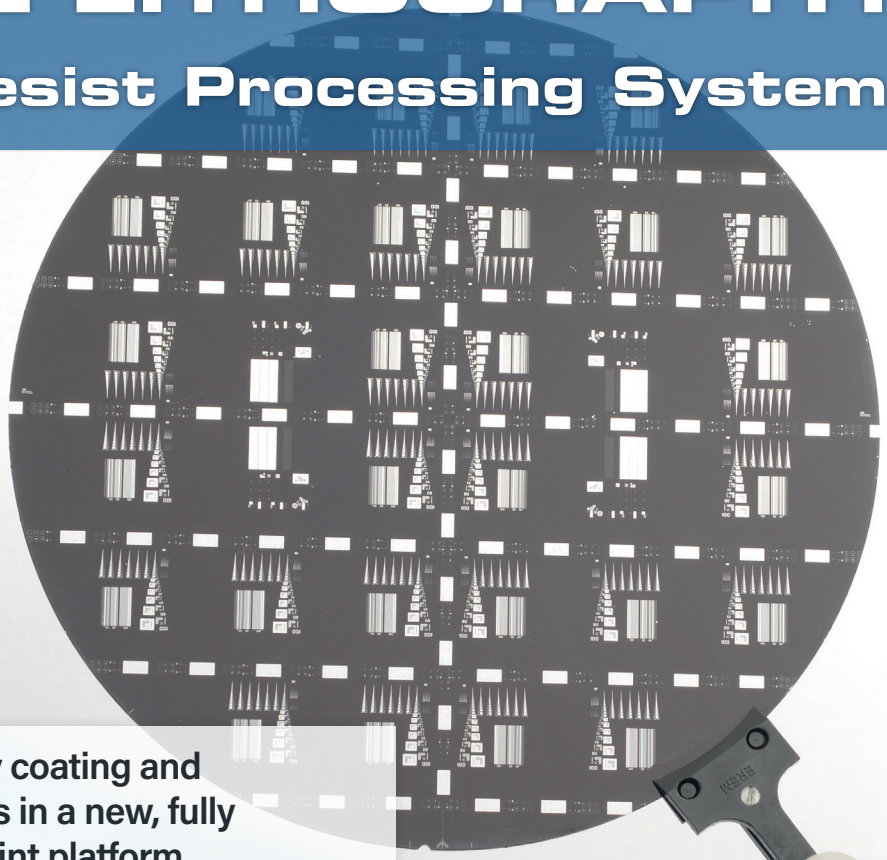

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