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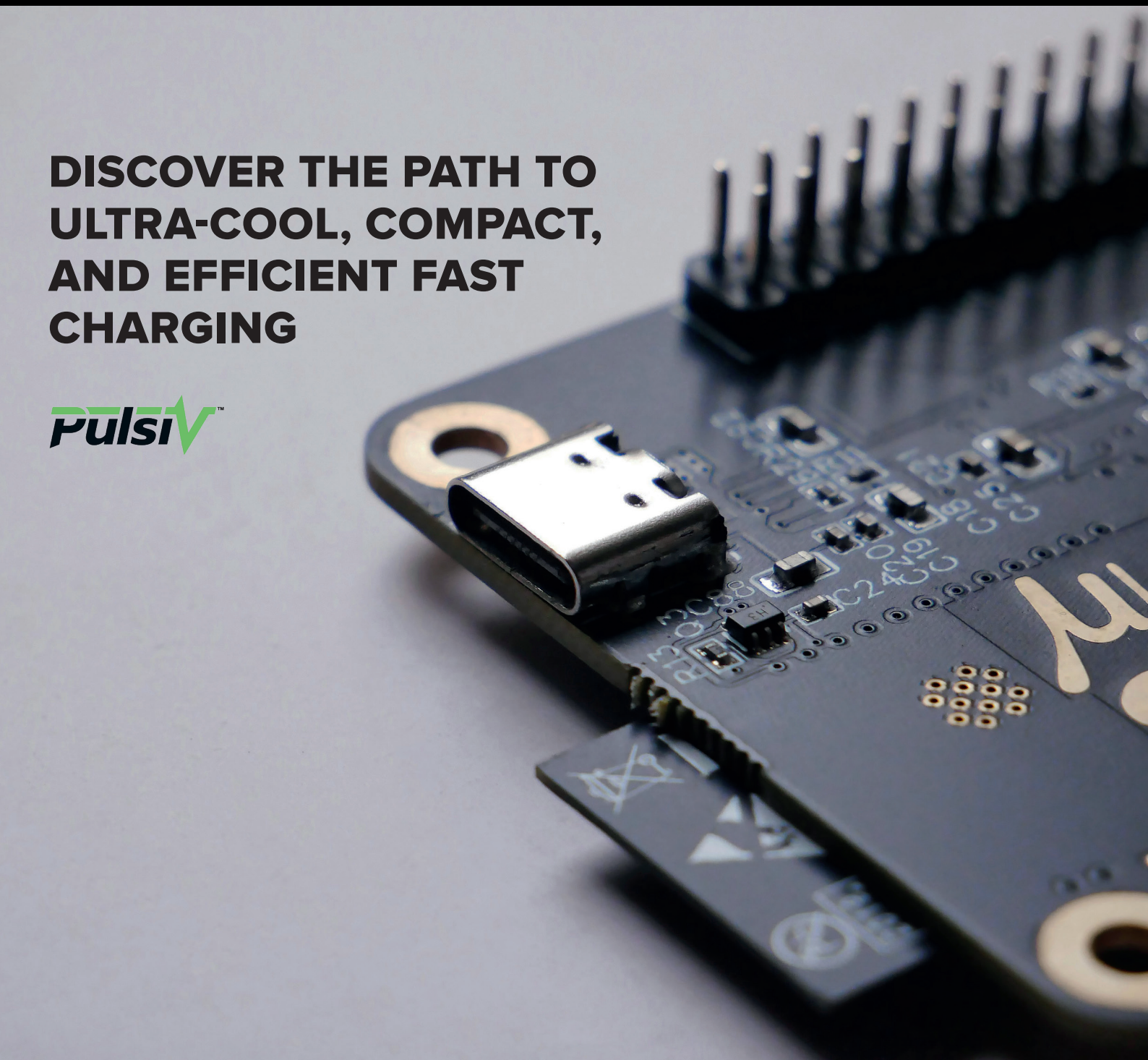

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ISSUE III 2024

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

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As reliance on renewable energy continues to increase, a three-level converter architecture built using high-voltage SiC MOSFETs

Cost-effective SiC substrate manufacturing

Silicon Carbide (SiC) power devices are seen as a game-changer in the automotive industry.

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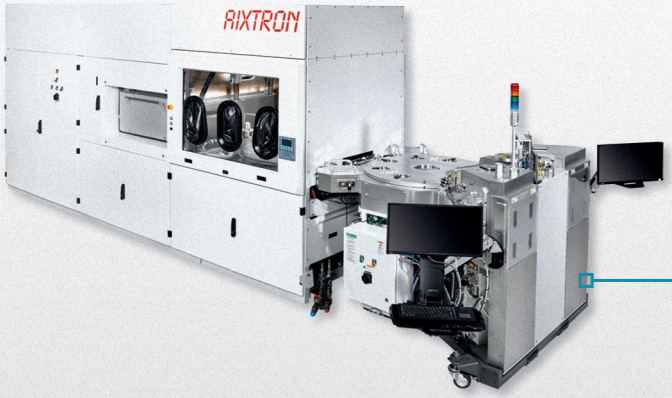

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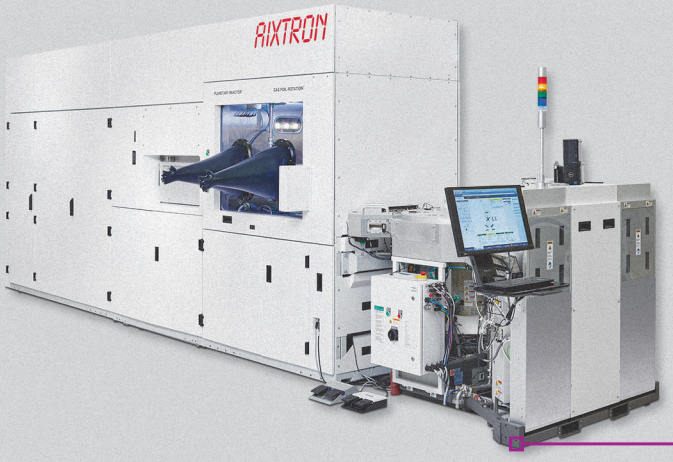

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VIEWPOINT

By Phil Alsop Editor

Power electronics can provide a sustainable, digital future

Having arrived in the semiconductor industry by way of, most recently, the data centre industry, it's fascinating to compare and contrast these two technology sectors and, not least, to understand that they are, in essence, two key parts of the same overall ICT supply chain. Asked what I do for a living, folks' eyes tend to glaze over when I tell them that I work on data centre and digital transformation publications – magazines, newsletters and websites.

Until, that is, I am given the chance to explain that, like it or not, there's almost no activity undertaken in today's digital world without some reliance on a data centre somewhere in the background. I won't say that my audience becomes engrossed with thoughts of servers, routers and storage hardware, let alone power and cooling technology, but there is certainly some recognition of this truth and maybe a grudging understanding of just how important are data centres in our digital lifestyles.

And now, of course, I can add to my party conversation, the fact that I also work in the semiconductor industry – focusing on both silicon semiconductors and power electronics. Once again, I can explain to whoever wants to listen that semiconductors and, in particular, power electronics, are an equally essential part of the digitalisation process.

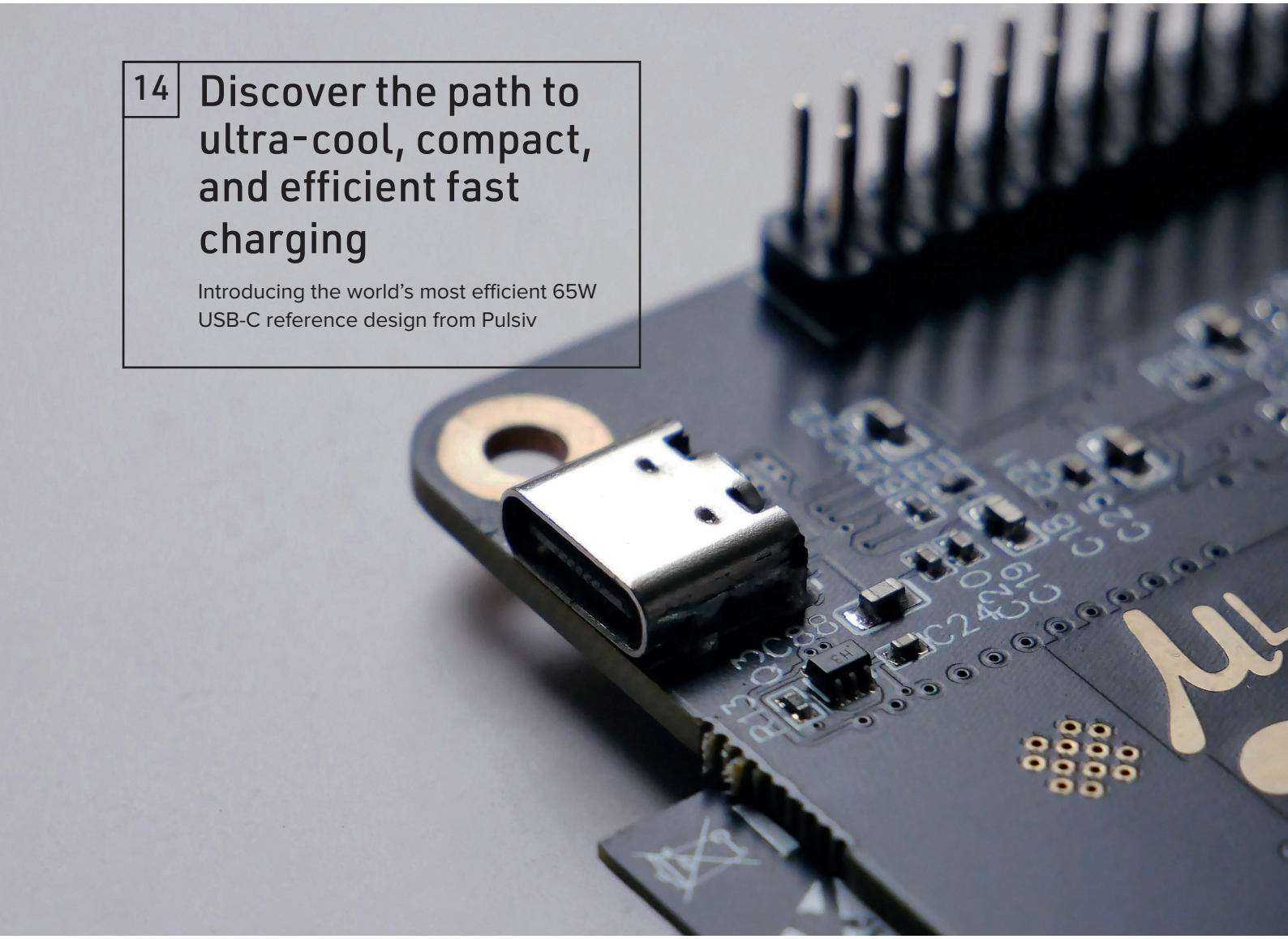
Conversations about the digital world often move on to contemplation of sustainability and the inevitable discussion as to whether a truly digital and sustainable world is actually achievable. We'll leave that debate for another day, but let us recognise the vital role that the power electronics world has to play when it comes to improving energy efficiency in so many applications and in so many ways:

- Power generation (especially when it comes to renewables and energy storage)
- Industrial automation, drives and controls
- Information and communications (ICT)
- Emobility and etransportation
- Smart/connected homes

As this issue of PEW demonstrates, there's a great deal of innovation in the power electronics sector to develop new materials and solutions with the major focus of providing significantly more sustainable power however, wherever and whenever required.

I don't have anything more complicated to add – other than to recommend that, every now and then, it's good to view the industry in which you work from an outsider's perspective. To understand the fantastic work that's often taken for granted and to maybe take the time to explain these achievements to the 'person in the street'.

PEW POWER ELECTRONICS WORLD



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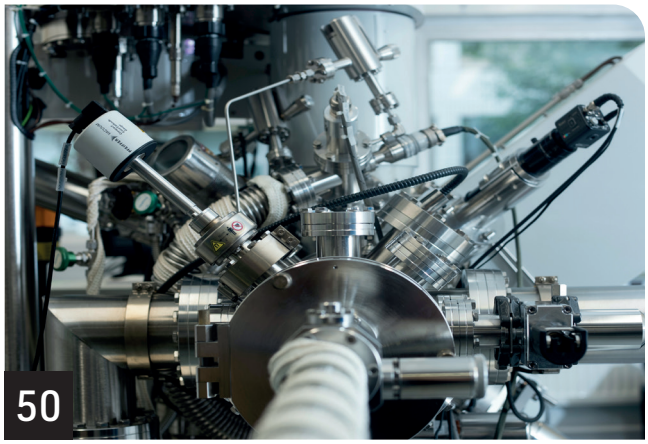

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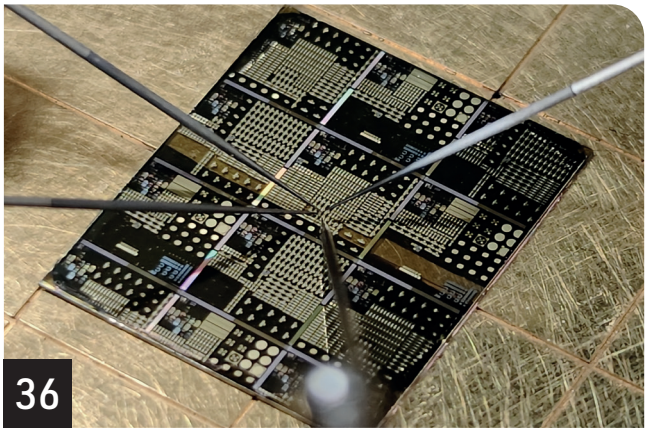

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POWER ELECTRONICS WORLD

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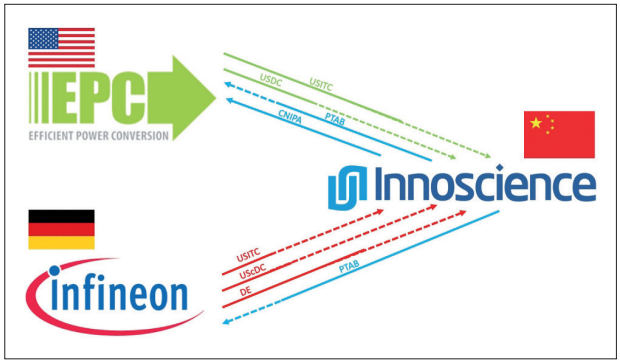
Angel BUSINESS COMMUNICATIONS

GaN transistors: An escalating patents war

The battle over intellectual property surrounding the GaN power transistor is intensifying, with EPC and Infineon attacking Innoscience over patent infringement that it vigorously denies.

WITHIN OUR INDUSTRY, last summer will be remembered as the start of a global war surrounding the intellectual property (IP) of the GaN power transistor. Back then, Efficient Power Corporation fired the first shots, accusing Innoscience of infringing four of its patents. In only a matter of days Innoscience shot back, denying any wrongdoing. More recently, another company has entered the fray, with Infineon claiming that Innoscience is also not respecting its IP. And again, Innoscience is pleading innocence.



As claims and counterclaims are launched in courtrooms around the world, there is much value in hearing from those that combine expertise in this area with a neutral standpoint. Offering all this and more is David Radulescu, head of the patent litigation boutique firm Radulescu, who has been litigating semiconductor patents in courts throughout the US for three decades. More significantly, Radulescu also holds a PhD in compound semiconductor HEMTs and has previously devoted much effort to representing global companies fighting over IP associated with GaN-based LEDs.

In late July, Radulescu spoke for a second year in a row about the escalating IP war in a highly insightful webinar covering various patents that hold the key to deciding the outcome of the many court cases.

Before delving into details, Radulescu summarised the shots that had been fired to date: a pair of actions taken by both EPC and Innoscience in their battle, plus three fired by Infineon and another by Innoscience in their more recent skirmish.

This all kicked off last summer, when EPC announced it took legal action against Innoscience for infringing four of its patents. In the intervening months, EPC dropped two patents in its International Trade Commission (ITC) case, while initial rulings have been released on the other two this July. According to the administrative law judge (ALJ) in the ITC, both of EPC's patents are not invalid, but significantly, he determined that one of them is infringed.

What's also worth noting is that in the last couple of months action taken by Innoscience in China has also led to rulings that counterpart Chinese EPC patents were not invalid.

"We have Innoscience on its own turf losing in the Chinese Patent Office," remarked Radulescu, who added that the US Patent and Trademark Office (USPTO) is still considering the validity of the patent found to be infringed by the ALJ, although the claims and prior art at issue are identical. Radulescu offered a closer look at the key patents after highlighting the recent stockpiling of US patents issued to Innoscience. In the past year-and-a-half, the Chinese chipmaker was issued 45 US patents, while EPC was issued only one, leading Innoscience to outpace EPC in the total number of US patents by 58 to 57.

Gate designs

Focusing on the shape of the gate structure is EPC's '508 patent, which the ALJ found to be not invalid but also not infringed. To put this patent in context, over the last few decades, a number of different gate structures have been used to produce GaN transistors, including: those that are self-aligned, with the gate and the insulator underneath having the same dimension (length); and those that have a T-shape or an inverted T-shape.

The '508 patent describes a multi-step process involving the use of three different photoresist patterns to produce a self-aligned gate.
For the claims brought by EPC concerning this patent, the key issue, according to Radulescu, is whether "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact," describes the Innoscience process.

"When you visually look at the [Innoscience] device, you see a gate ledge that is not co-extensive with the gate contact layer," said Radulescu, who is not surprised that the ALJ viewed this transistor as being different from that of EPC, and thus concluding that there was no infringement. The other important matter relating to the '508 patent is that Innoscience has asserted that it is invalid, an argument that was rejected by the ALJ.

Doping and compensation

Radulescu believes that those involved in ruling on the EPC-Innoscience battle will have a more difficult decision to make when it comes considering claims surrounding the '294 patent entitled 'Compensated Gate MISFET'. In his view, what's crucial is to understand what is meant by 'compensated', against the backdrop of the difficulties that have had to be overcome to realise p-type doping in GaN, key to producing LEDs with this material system.

The key claim by EPC is whether the phrase 'compensated GaN layer' describes the GaN layer in Innoscience's devices that is presumed to be p-type based on its own publications.

It's important to note, argued Radulescu, that EPC's patent does not say anything about the GaN layer's carrier type or its resistivity, characteristics that can be measured. Instead, it just uses the word 'compensated', a characteristic far harder to judge. This is because a picture or image of the device material is not determinative, but requires an understanding of semiconductor material science. The other key point that Radulescu emphasised is that the '294 patent covers simply a transistor, and makes no reference to enhancement-mode or depletion-mode devices. Many are assuming that the GaN employed by Innoscience is p-type. "They introduced magnesium, and I will be willing to bet that the hydrogen is intentionally removed after growth," remarked Radulescu, whom added that secondary ion mass spectrometry (SIMS) plots have been disclosed during the case. "Whether or not you can call it 'compensated' depends upon how you define what compensation is," added Radulescu.

Innoscience has argued that they do not employ a compensated GaN layer because they use a Schottky gate, as well as claiming that SIMS data reveals dopant activation, and testing confirms p-type conductivity. According to Radulescu, all these arguments were rejected by the ITC staff due to procedural errors of its counsel. For example, Innoscience offered evidence of the nature of the GaN through the testimony of an employee, an account viewed as problematic due to self-interest.

"Unfortunately for Innoscience, I don't think their best arguments were put forward," commented Radulescu, who explained that the full Commission will now review the ALJ's initial determination of infringement and issue a final decision on the investigation called a Final Determination, which is expected to issue in early November 2024.

Both Innoscience and EPC have tried to claim victory from the initial determination. Innoscience argues that it has won, because one of the patents was determined to not be infringed, while EPC is focusing on a finding of infringement.

The view of Radulescu is that while, in theory, EPC lost on three patents out of four, what really matters is that they have a ruling of a violation of the ITC statute against unfair competition by importing products that infringe US patents. And he believes that given how Innoscience's lawyers argued their defences, it will be far from easy to get the ALJ's determination reversed or modified, although not impossible.

Looking ahead, in March 2025, the US Patent Office will rule on the validity of the four patents asserted by EPC against Innoscience (which are also still at issue in EPC's District Court case against Innoscience in California). If the '294 patent is determined to be invalid, this decision could be appealed, dragging the case on for a couple more years. Significantly, under this scenario, the ITC's final determination will likely not matter as any potential importation ban would be expected to be stayed pending appeal. On the other hand, if the '294 patent is determined to not be invalid, and at the same time the full Commission agrees with the ALJ on infringement of the '294 patent, Innoscience's products found to infringe would presumably be subject to some form of importation ban as that is a typical remedy available to patent owners in these type of ITC investigations.

Infineon versus Innoscience

Infineon's actions against EPC began in March this year, when they brought a suit in San Francisco for a patent associated with high-voltage packages featuring so-called 'source sensing'. Innoscience response to this has been to file a petition this June with the US Patent Office, arguing for invalidation of every single claim.

Meanwhile in Germany, Infineon has also filed several cases, as well as obtaining a preliminary injunction that prevented a small fraction of Innoscience's high-voltage GaN transistors from being promoted at PCIM. Commenting on this, Radulescu remarked: "Infineon outmanoeuvred Innoscience's lawyers, because they got that injunction without Innoscience actually being heard on any of the issues. It was a surprise, but not unusual for parties to go to Germany to try to get these preliminary injunctions and mess up trade shows."

Within the last few weeks, Infineon has stepped up its action, adding three more patents to the San Francisco case, and filing its own complaint with the ITC. On the merits, the first of four Infineon patents that have been asserted involves an additional connection to the source of the power transistor, so that the parasitic elements associated with the packaging and connections have a reduced impact on overall system performance.

Infineon's accusations centre on Innoscience's use of a Kelvin source that it claims practices the patented source sensing functionality, as well as an identical pin layout. Like Infineon's products, those in question from Innoscience have 8 pins, including one that's a Kelvin source sensor.

Regarding the three other patents, one is concerned with the thickness of a titanium nitride capping layer in an electrode stack. The other two concern so-called 'merged cascode transistors', with one patent concerned with adding curvature to inter-digitated fingers to trim the electric field strength at the edge of the electrodes, and the other associated with combining a depletion-mode transistor with an enhancement-mode transistor to make a circuit. If the case is not settled beforehand, the ALJ's initial rulings on these patents are not expected until autumn 2025.

While it is impossible to predict the rulings of all the asserted claims to date in the GaN patent war, there is no doubt that substantial time and money will be spent over the next few years trying to defend IP and the products based on them. There are many different outcomes that could emerge, including licensing deals and import bans – but what is for sure is that interesting times lie ahead.

Almost 42 million EV cars worldwide

Trend in electromobility continues, according to German research organisation ZSW

14.8 MILLION new electric vehicles were registered worldwide in 2023 (EVs running on battery power alone, plug-in hybrids and vehicles with range extenders), according to new research by ZSW's Centre for Solar Energy and Hydrogen Research Baden-Württemberg, Germany.

China is in the lead with over nine million electric cars while the USA has claimed second place ahead of Germany. The number of new registrations of electric cars in Germany last year was almost 700,000. This brings the current tally of electric cars on German roads to 2,330,400 but this is not enough to achieve the goal set by the German government of 15 million electric vehicles by 2030. The annual level of new registrations would have to double or triple in order to achieve the target.

The global count of electric cars in circulation at the end of 2023 was almost 42 million. More than half of these vehicles are registered in China, ahead of the USA in second place with 4.8 million electric cars and Germany in third place. Setting aside the Chinese figures, the highest growth rates in circulation were seen primarily in smaller markets like Belgium with 71 per cent (192,400 vehicles) or Portugal with 54 per cent (65,000 vehicles).

In terms of new registrations, the EU is the second largest market in the world after China. Around 2.5 million new electric cars were registered here in 2023, with the USA following in third place with 1.5 million vehicles. Electric cars still have the highest share of the total vehicle market in Norway where four in every five new vehicles are powered by electricity.

Germany, by contrast, is seeing a significant slowdown in the momentum gathered in 2022, when the figures rose by 22 per cent on 2021, and is now reporting that new registrations actually fell by 16 per cent in the past year.

One of several factors accounting for this development, says ZSW, is that sales of plug-in hybrids have fallen sharply since the government subsidy scheme ended on 31 December 2022. It is also evident, however, that an 11 per cent growth in cars run entirely on battery power did not fully compensate for this decline.

The higher initial outlay on the purchase of an electric vehicle remains a frequently cited point of criticism. The relatively weak overall economic situation in Germany has probably also had a dampening effect on the development of electromobility, as have falling fossil fuel prices after the phase of high prices in 2022.

"There is a need for new incentives in the market in order to achieve the electromobility targets in Germany – 15 million electric vehicles in circulation by 2030 – and to encourage new momentum in climate action in the transport sector. The initiative for growth proposed by the German government in greater support of electric company cars cannot amount to anything more than an initial step," said ZSW staff member Andreas Püttner.

"In view of the strict austerity budgets choking the public finances, there can be a major impetus in abolishing privileges for conventional vehicles – aka subsidies having an adverse impact on climate targets. Examples of steps which could be taken to come much closer to a 'level playing field', with the same conditions for cars with combustion engines and electric cars, would be to abolish tax breaks for fossil diesel fuels and for company cars with conventional engines, known as the diesel concession and company car concession respectively, or to limit incentives strictly to company cars powered by electricity."

Despite the weakness of the German domestic market, German manufacturers are successful on the international stage where VW, BMW and Mercedes all rank among the top 10 manufacturers and where VW has even moved up to third place in the statistics on new registrations, having sold just over one million cars overall, according to ZSWI.

Compared to the industry leaders BYD (China) and Tesla (USA), however, there is still a large gap in terms of numbers, with Chinese company BYD reporting sales of over three million electric cars and therewith another significant increase of 68 per cent in the number of new registrations compared to last year, thereby maintaining a confident lead in the rankings over the other manufacturers, while Tesla holds on to second place with 1.8 million sales.

The most successful model in the world by far last year was again the Tesla Model Y, which was sold over 1.2 million times. Tesla enjoys further success with its Model 3 in third place. The other electric cars in the top 10 worldwide all come from China, with the manufacturers BYD, GAC Group and SAIC increasingly widening their range of vehicles.

"If Germany is to achieve its climate control goals, there is an urgent need for attractive vehicles in the lower and middle segments in order to appeal to a larger customer base. If the German and European manufacturers do not fill this gap, there is a risk that other manufacturers, especially those in China, will seize this opportunity in spite of the introduction of punitive tariffs at European level in a bid to prevent this," added Andreas Püttner.

Scientists use waste RF to power electronics

Singapore University team leads development of novel energy harvesting module

UBIQUITOUS wireless technologies like Wi-Fi, Bluetooth, and 5G rely on RF signals to send and receive data. Now a team led by scientists from the National University of Singapore (NUS) has developed a prototype energy harvesting module that can convert these ambient RF signals into DC voltage to power small electronic devices.

RF energy harvesting technologies face challenges due to low ambient RF signal power (typically less than -20 dBm), where current rectifier technology either fails to operate or exhibits a low RF-to-DC conversion efficiency. While improving antenna efficiency and impedance matching can enhance performance, this also increases on-chip size, presenting obstacles to integration and miniaturisation.

To address these challenges, a team of NUS researchers, working in collaboration with scientists from Tohoku University (TU) in Japan and University of Messina (UNIME) in Italy, has developed a compact and sensitive rectifier technology that uses nanoscale spin-rectifier (SR) to convert ambient wireless radio frequency signals at power less than -20 dBm to a DC voltage.

The team optimised SR devices and designed two configurations: 1) a single SR-based rectenna operational between -62 dBm and -20 dBm, and 2) an array of 10 SRs in series achieving 7.8 percent efficiency and zero-bias sensitivity of approximately 34,500 mV/mW. Integrating the SR-array into an energy harvesting module, they successfully powered a commercial temperature sensor at -27 dBm.

“Harvesting ambient RF electromagnetic signals is crucial for advancing energy-efficient electronic devices and sensors. However, existing energy harvesting modules face challenges operating at low ambient power due to limitations in existing rectifier technology,” explained Yang Hyunsoo from the Department of Electrical and Computer Engineering at the NUS College of Design and Engineering, who spearheaded the project.

Yang added, “For example, gigahertz Schottky diode technology has remained saturated for decades due to thermodynamic restrictions at low power, with recent efforts focused only on improving antenna efficiency and impedance-matching networks, at the expense of bigger on-chip footprints. Nanoscale spin-rectifiers, on the other hand, offer a compact technology for sensitive and efficient RF-to-DC conversion.”

Elaborating on the team’s breakthrough technology, Yang said, “We optimised the spin-rectifiers to operate at low RF power levels available in the ambient, and integrated an array of such spin-rectifiers to an energy harvesting module for powering the LED and commercial sensor at RF power less than -20 dBm. Our results demonstrate that SR-technology is easy to integrate and scalable, facilitating the development of large-scale SR-arrays for various low-powered RF and communication applications.”

The experimental research was carried out in collaboration with Shunsuke Fukami and his team from TU, while the simulation was carried out by Giovanni Finocchio from UNIME. The results were published in Nature Electronics, on 24 July 2024.

Russian venture targets SiC power

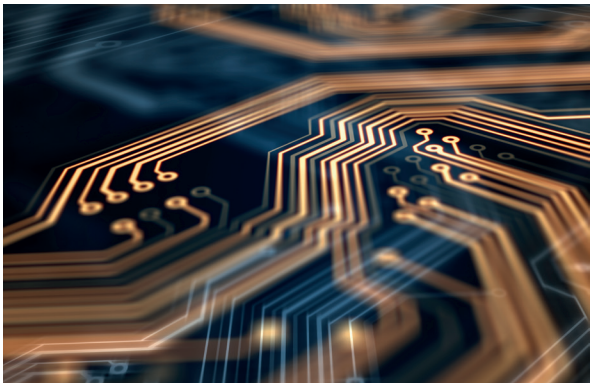
Element and St. Petersburg Electrotechnical University form joint power chip company

RUSSIAN MICROELECTRONICS company PJSC Element and St. Petersburg Electrotechnical University LETI (ETU LETI) have formed a joint venture called Letiel LLC, according to a story on Interfax, a news agency covering Russia.

"We plan to actively develop the area of high-tech power semiconductor devices and in future take leading positions among global manufacturers of SiC devices," Element president Ilya Ivantsov told Interfax.

"The objective of the joint venture with LETI will be to develop and research technologies to produce SiC devices, on the basis of which we will be able to build a modern and competitive power electronics product and technology line for various sectors of industry," Ivantsov said.

The new company will do research and development on SiC based power devices, which are used on production of modern electric vehicles, aircraft navigation systems and other sectors.



The venture, which is 51 percent owned by Element and 49 percent by LETI, also plans to study and design promising Photonic integrated circuits.

These components are used in equipment for cellular networks, satellite systems and radiolocation.

"Mass production of solutions in the area of the electronic component base for power electronics and photon integrated circuits will be rolled out at the facilities of Element Group's new plant in Zelenograd," the company said.

The partners have not specified how much they are investing in the venture, which is headed by Element technology development director Konstantin Okunev.

Element was formed in 2019 with 19 microelectronics design, development and manufacturing assets belonging to investment group Sistema PJSFC and state corporation Rostec. Element's key portfolio companies are chip factory Mikron and microchip, molecular electronics research institute NIIME and electronics research institute NIIET. The group now includes about 30 enterprises.

Project to develop EV-grade 1.2 kV SiC MOSFETs

OXFORD INSTRUMENTS will be working with Hitachi Energy Switzerland and the University of Warwick to improve SiC power MOSFET gate technology through the use of ALD oxides.

This is one of 26 new projects intended to enhance UK and Swiss collaboration on innovation and technology, supported by £7.8 million funding from Innovate UK and similar figure from Innosuisse, the Swiss innovation agency.

Hitachi Energy Switzerland (Hitachi) has a proven track record of developing automotive grade SiC power MOSFETs with a reputation for products with novel MOS interfaces. Oxford Instruments Plasma Technology (OIPT) has developed a novel oxide deposition process that uses a remote plasma source in a commercial atomic layer deposition (ALD) system. This process is suitable for the formation of gate oxides in wide bandgap semiconductors.

A research team at the University of Warwick (UoW) has recently developed an ALD SiO2 deposition process on SiC that has the potential to be commercialised.

This project will bring together the three groups and their relative expertise to demonstrate the potential of ALD oxides in the formation of EV-grade 1.2 kV SiC MOSFETs.

The aim is address one of the most pressing issues in the adaptation of this technique by fundamentally changing the way of forming a crucial part of the device, the gate oxide. Conventional dielectric and SiC interfaces are suffering from high density of defect states, hampering the further uptake of this technology.

This proof-of-concept project will demonstrate the viability and advantages of utilising ALD deposited oxides (SiO2 and high-k dielectrics such as aluminium oxide, Al2O3 in a commercial SiC MOSFET device.

The partners aim to deliver the first demonstration of a commercially relevant planar 1.2 kV SiC MOSFET that contains OIPT's remote plasma ALD-deposited SiO2 and high-k dielectric (for example Al2O3) gate oxides.

German research cluster announces AlN success

German partners demonstrate practical implementation of AlN-based value chain for power semiconductors

A NEW semiconductor technology based on AlN for power electronic transistors as well as mmWave radio-frequency circuits has the potential to significantly reduce losses in electrical energy conversion and high frequency transmission, according to German research partners.

Devices on single-crystal AlN wafers reach a higher power density and efficiency compared to GaN technology. They also show lower dynamic parasitic effects and a higher reliability.

At the same time, the high thermal conductivity of AlN enables good heat dissipation of the devices.

In order to make AlN technology accessible to industry in the medium term, the related existing activities in Germany have been combined in a strategic cluster,.

The aim is to establish a German value chain for AlN-based technology and to build up an international leadership position in this increasingly economically important field.

The Ferdinand-Braun-Institut (FBH), the Fraunhofer Institute for Integrated Systems and Device Technology IISB and the company III/V-Reclaim PT GmbH drive this initiative together.

They cover the entire value chain, starting with the growth of AlN crystals using the Physical Vapor Transport (PVT) process, to wafering and polishing of epi-ready AlN-wafers, and the epitaxy of the functional device layers, up to the fabrication of transistors for power electronics and mmWave applications.

For the first time, the consortium has now successfully demonstrated the practical implementation of a value

chain for AlN devices in Germany and Europe.

To this end, AlN crystals were grown at Fraunhofer IISB and sliced into AlN wafers with a diameter up to 1.5 inches.

The company III/V-Reclaim has developed a polishing process for epitaxial wafer production. Functional epitaxial layers were then applied to these wafers at the Ferdinand-Braun-Institut, and AlN/GaN HEMTs were successfully processed on them.

The first transistor generations produced with these wafers already show promising electrical properties, such as a breakdown voltage of up to 2200 V and a power density superior to SiC as well as GaN-based power-switching devices.

Compared to established silicon devices, AlN/GaN HEMTs, as successfully produced on AlN wafers, offer up to three thousand times less conduction losses than with silicon and are around ten times more efficient than SiC transistors.

These research breakthroughs were supported by funding from the German Federal Ministry of Education and Research (BMBF) within the ForMikro-LeitBAN and Nitrides-4-6G projects.

Samsung backs next gen GaNFast

NAVITAS GaN power ICs now fast-charge Samsung's Galaxy Series-A, Galaxy Z Fold6 and Galaxy Z Flip6 phones

Navitas Semiconductor has announced that Samsung had expanded adoption of Navitas' GaNFast ICs from the original Galaxy S22, S23 and S24 to the mainstream Galaxy A, and also the new Galaxy Z Fold6 and Galaxy Z Flip6 smartphones with Galaxy AI features.

GaN runs up to 20x faster than legacy silicon and enables chargers up to 3x more power and 3x faster charging in half size and weight. Navitas says that its GaNFast power ICs enable high-frequency, high-efficiency power conversion, achieving up to a 50 percent shrink vs. prior designs.

The new 25W charger (EP-T2510) features new energy-saving technology to reduce standby losses by 75 percent to only 5 mW, which aligns with Navitas' environmental advances, where every GaNFast IC saves 4 kg of CO2 vs. legacy silicon chips. "Since enabling the world's first production GaN charger in 2018, Navitas has pioneered and leads the adoption of GaN to replace legacy silicon chips," noted David Carroll, SVP Worldwide Sales for Navitas. "Our production partnership with Samsung dates back to the Galaxy S22 Ultra, and today's announcement reflects the dramatic expansion of GaN from niche, flagship designs to adoption in high-volume, mainstream phones."

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Energy Harvesting and Wireless Power Transfer: Enabling Autonomous Systems

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Discover the path to ultra-cool, compact, and efficient fast charging

Introducing the world's most efficient 65W USB-C reference design from Pulsiv.

BY PULSIV

THE DEMAND for USB-C is forecast to surge over the next decade, fuelled by the migration from USB-A to USB-C and a growing market of portable devices that require fast charging. As power requirements increase, the need to deliver more power in a confined space adds challenges with thermal management and heat dissipation which impact safety and reliability.

The PSV-RDAD-65USB reference design has been developed to demonstrate how Pulsiv OSMIUM technology reduces component temperatures, enabling products to consume less power and reduce overall size. It represents the first in a series of designs aimed at pushing the boundaries of power conversion to create a sustainable platform for the USB-C standard.

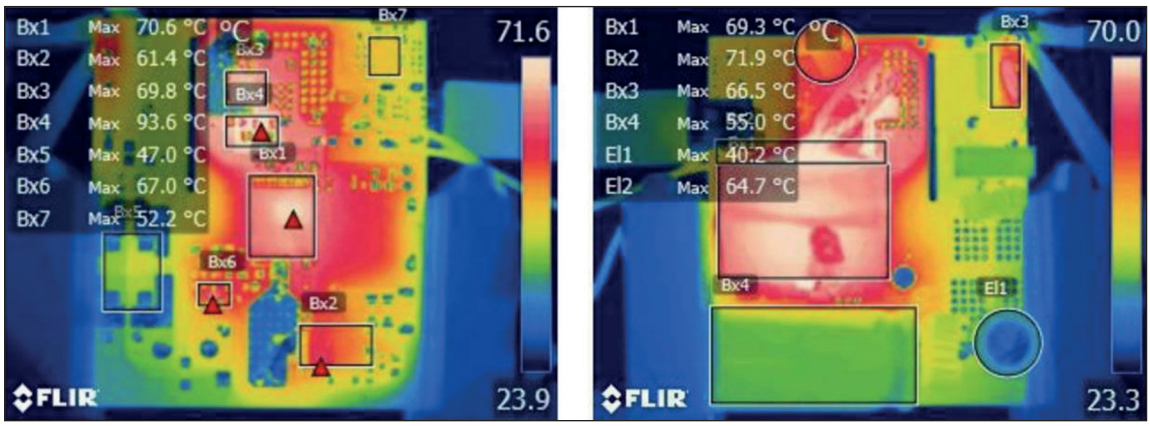
In this design, the Pulsiv OSMIUM microcontroller PSV-AD-65EG-Q24IV has been combined with OnSemi's NCP1342 Flyback controller and GaN devices from Innoscience to deliver a world leading specification:

- **Input Voltage Range** 90 – 265VAC (no input voltage derating)
- **Output Voltage:** 5 – 20VDC supporting PD3.0, QC4.0, BC1.2, & PPS (Fast Charging)
- **Output Power:** 65W max
- **Transformer Temperature:** 30.3°C above ambient
- **Operating Frequency:** 125kHz
- **Peak Efficiency:** 96%
- **Average Efficiency:** 95%
- **Half-Active Bridge:** Included
- **Line Currents:** 0.5A max
- **Inrush Current:** Eliminated
- **GaN Optimised:** Yes
- **DC-DC Converter:** Quasi-Resonant (QR) Flyback

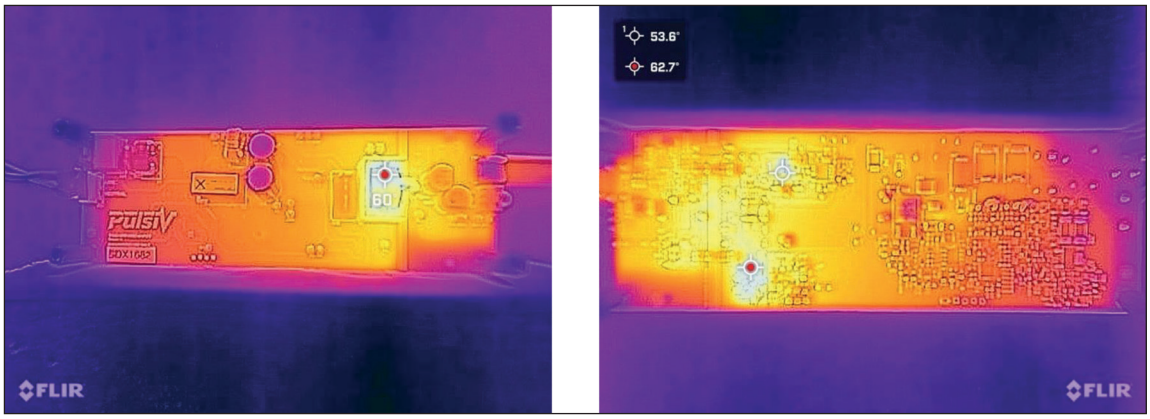
Taking ultra-cool operation & fast charging to a whole new level

Critical components in conventional designs will often reach temperatures of over 100°C, so measures must naturally be taken to dissipate heat or limit output power. This means compromising cost, performance, or physical size to mitigate impact safety and reliability issues.

The Pulsiv OSMIUM reference design demonstrates a significant improvement in thermal performance and reduces critical component temperatures by more than 30% compared to other designs. At full load, the Flyback transformer reaches an impressive 33.9°C at 230VAC and 30.3°C at 265V above an ambient temperature of 26.1°C. This incredible achievement is likely to set a new benchmark and



➤ Competitor data demonstrates a highest component temperature of 93.6°C. (A 65W USB-C reference design from a leading manufacturer of power supply solutions.



➤ Thermal measurement of the Pulsiv PSV-EBAD-65USB evaluation board demonstrates the hottest component temperature ;of 62.7°C.

enables 65W fast charging in space constrained environments and/or heat sensitive applications such as in-wall plug sockets that incorporate USBC connectivity.

Setting a new benchmark in power conversion
Pulsiv OSMIUM technology is a patented AC to DC front-end conversion method that applies intelligence to an active valley fill approach and delivers a combination of game changing benefits in power electronics designs. It significantly improves performance at low loads to increase overall average efficiency, reduce energy consumption, and deliver a totally flat efficiency profile across all load conditions.

The Pulsiv AC to DC conversion method intelligently regulates the charging current and voltage on the storage capacitor using a high-side architecture to switch Qch. This allows the use of 200V or 160V capacitors (selectable) to support a universal mains input. The valley-fill period is broadly similar to a 2C3D architecture; but the charging period of the capacitor is significantly longer and more variable.

Reducing system losses

Figure 1 shows a simplified circuit implementation to illustrate the basic operation of Pulsiv OSMIUM technology in this design. A MOSFET, Qch, is used to control the charging of Cch to generate a configurable highvoltage DC output (HVDC) and a blocking diode Db ensures that Cch does not discharge through the body diode of Qch while avoiding stray conduction through the inductor. This approach allows the use of smaller and lower cost 200V or 160V capacitors to support a universal mains input.

Losses during the charging phase are typically between 0.5% and 2%, resulting in a peak efficiency of up to 99.5%. The circuit converts just enough energy to maintain capacitor voltage and delivers consistent efficiency over the full power range.
In a traditional valley-fill design, AC to DC conversion involves a full-wave diode bridge.

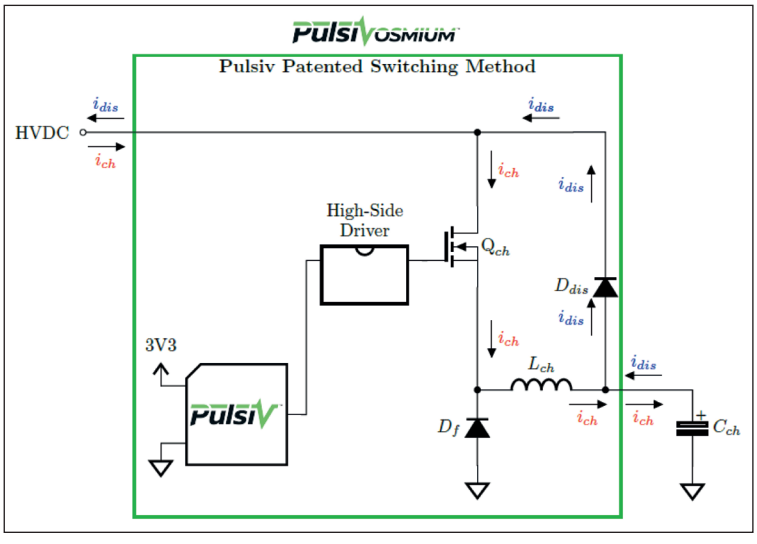
Diode losses are mainly determined by the average current, RMS current, the forward voltage drop, and the resistance during conduction. Conventional systems without power factor correction exhibit large peak currents, resulting in higher RMS currents and greater diode bridge losses. Power factor correction improves RMS current and results in a current waveform with a crest factor of √2.

Pulsiv OSMIUM designs typically have a crest factor of 1.3, which is lower than that of a sinusoid, leading to lower RMS values and reduced losses. Peak line currents are reduced by up to 90% as a direct result of the way Pulsiv OSMIUM controls capacitor charging, and inrush current is also eliminated.

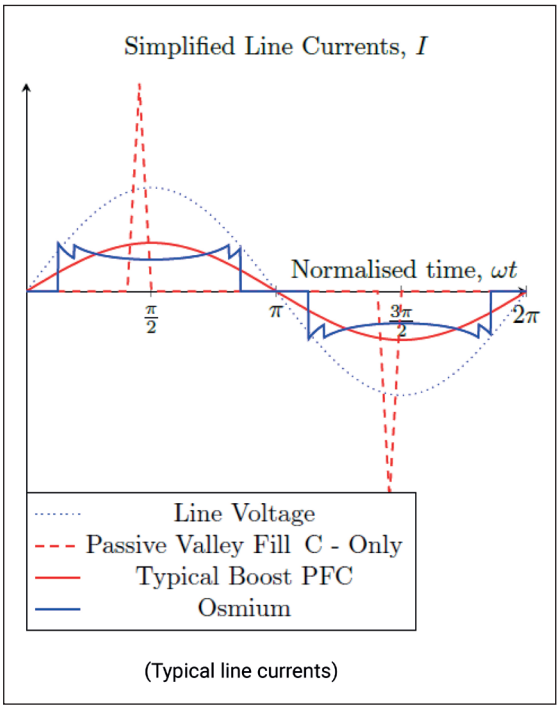
Optimize efficiency and space with a half-active bridge

Pulsiv OSMIUM technology senses AC line voltage and frequency to adjust capacitor charging time, therefore the circuit draws no line current at the AC zero voltage crossing. This enables a simple half-active bridge implementation to increase efficiency, especially at low line conditions.

MOSFETs in the lower half of the AC to DC bridge are carefully controlled, in combination with high-side diodes. The half-active bridge in this design strikes the delicate balance between efficiency, cost, and complexity and supports universal input with



➤ Figure 1: Pulsiv OSMIUM high side architecture.



(Typical line currents)

➤ Typical line currents.

efficiency gains of 0.7% at full load from a 115V AC supply.

Innovation in magnetics design reduces transformer size by 20%

Pulsiv OSMIUM technology generates a HVDC output that varies between the peak AC input and 150V (with a 230V input) to drive the QR Flyback at maximum efficiency. The wide voltage range it generates requires a significantly reduced primary side inductance which enables the use of an EQ20 transformer. This was developed in partnership with magnetics experts Frenetic where a 20% size reduction was achieved compared to the typical RM8 used in other designs.

Minimizing losses with GaN optimization

GaN transistors from Innoscience were used to lower the RDSon which reduced conduction losses, but this naturally increased parasitic capacitance. The INN700DA240B was the optimum device which provided the necessary balance between the two losses. An additional Innoscience GaN transistor INN150FQ032A was also selected to provide the most suitable match for operating with the synchronous rectifier controller and output current from the transformer.

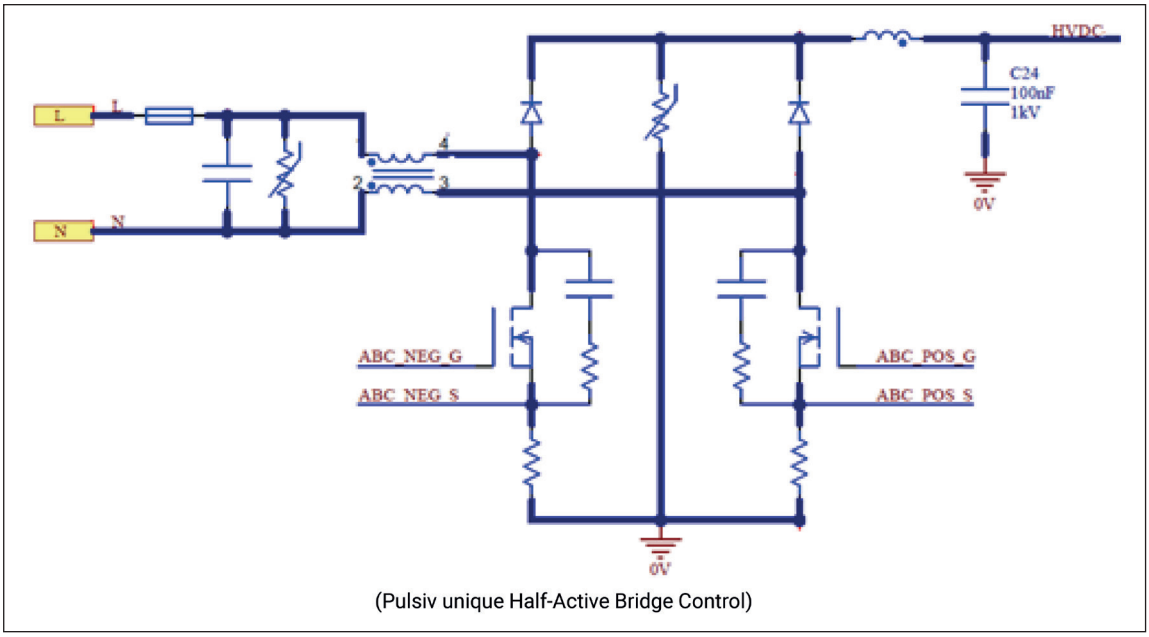
In this design, GaN lowered the overall energy consumption, reduced component size, and improved cost compared to conventional MOSFET's. Innoscience also provided outstanding support, delivering samples within 48hrs, and demonstrating the most competitive pricing.

Design package & evaluation boards

The PSV-RDAD-65USB document package is available to download free from the Pulsiv website and includes a Datasheet, Schematics, Bill of Materials, & Altium files. The PSV-EBAD-65USB evaluation board enables rapid lab testing and can be pre-ordered now for delivery in the 2nd half of August through a network of franchised distribution partners including global stockist Digikey.

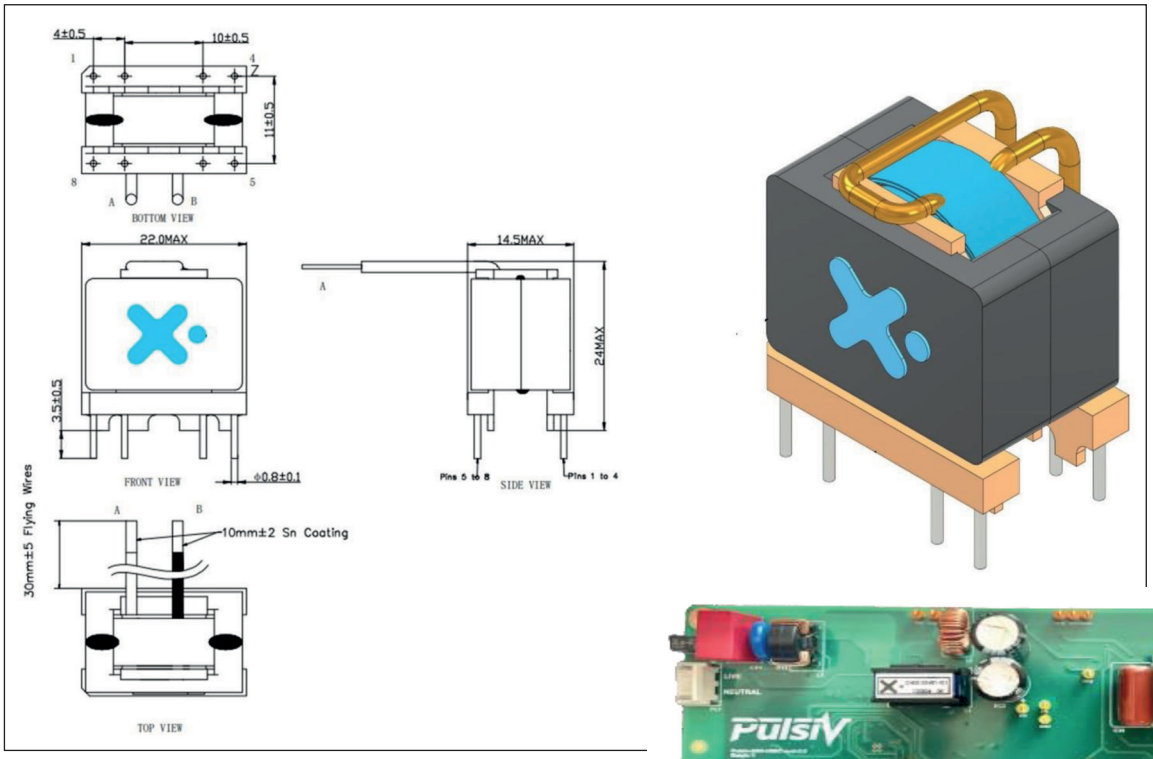
Summary

The PSV-RDAD-65USB reference design showcases a truly sustainable approach to efficient power conversion, ultra-cool thermal performance, and reduced energy consumption in USB-C applications. It demonstrates how the unique Pulsiv OSMIUM technology can influence magnetics design while supporting GaN to minimize overall losses. Its game-changing thermal measurements enable USB-C to be adopted quickly and safely while paving the way for fast charging within virtually any application.

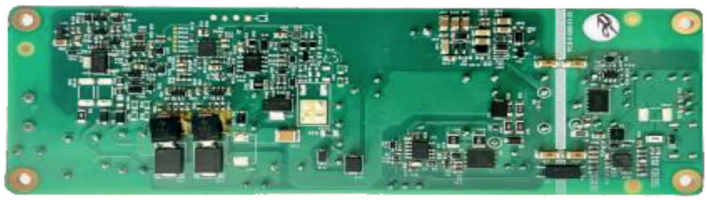


(Pulsiv unique Half-Active Bridge Control)

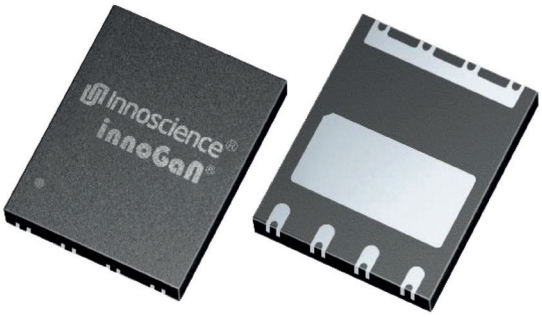
➤ Pulsiv unique Half-Active Bridge Control.

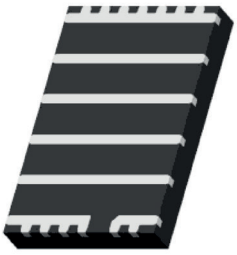


➤ Below: Pulsiv PS V-E BAD65USB Evaluation Board.

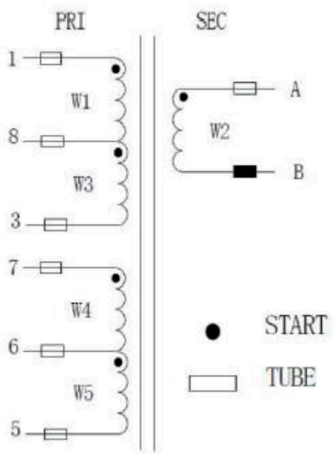


Fully assembled, size optimized, and EMC compliant "Plug & Play" modules of this reference design are currently under development which aim to accelerate adoption and simplify the design process. They will offer configurations of 1C, 1C1A, and 2C1A with other variants possible and can be pre-ordered through any of the franchised distribution partners for expected delivery in Q4 2024.

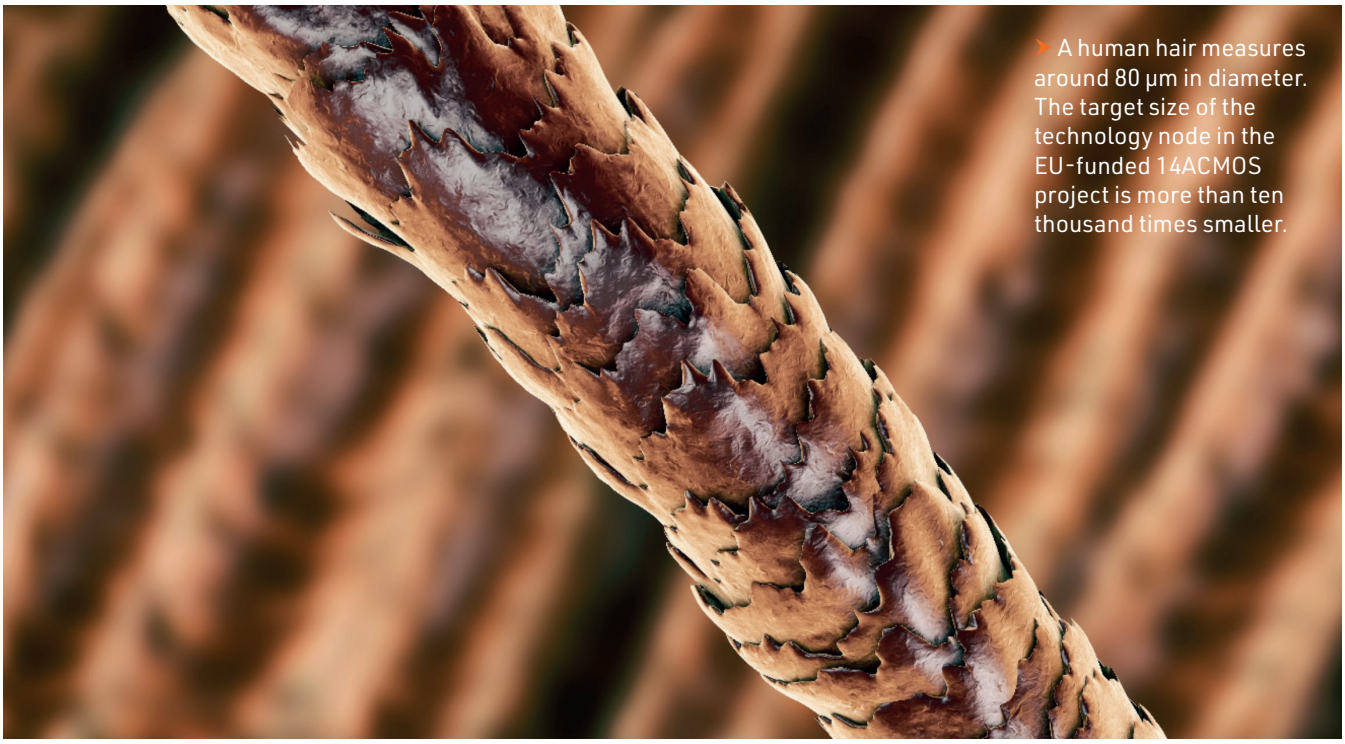




➤ Far Left Duo: Innoscience INN700DA240B and right: Innoscience INN150FQ032A.



Value	Wind	Start	End	Short	Conditions	Test	Nom	Tol(%)	Min	Max	Unit
Inductance	W1&3	1	3		25ºC, 0.1Vrms @ 100kHz	1	97.00	15.00	82.45	111.55	uH
Inductance	W2	A	B		25ºC, 0.1Vrms @ 100kHz	2	6.06	15.00	5.15	6.97	uH
Lk Inductance	W1&3	1	3	A,B	25ºC, 0.1Vrms @ 100kHz	3		15.00		3.00	uH
Inductance	W4	7	6		25ºC, 0.1Vrms @ 100kHz	4	26.62	25	19.97	33.28	uH
Inductance	W5	6	5		25ºC, 0.1Vrms @ 100kHz	5	2.50	25	1.88	3.13	uH
Inductance	W4&5	7	5		25ºC	6	44.98	15.00	38.23	51.73	uH
DC Resistance	W1&3	1	3		25ºC	7	187.50	15.00		215.63	mOhm
DC Resistance	W2	A	B		25ºC	8	12.00	15.00		13.80	mOhm
DC Resistance	W4&5	7	5		25ºC	9	360	15.00		414.00	mOhm
Hi-Pot		W1, 3,4, &5	W2		3000VAC, 60s	10				5.00	mA
Hi-Pot		W2	Core		3000VAC, 60s	11				5.00	mA



A human hair measures around 80 µm in diameter. The target size of the technology node in the EU-funded 14ACMOS project is more than ten thousand times smaller.

Splitting hairs to ten to the power of four

14ACMOS: EU project for the next technology node in semiconductor manufacturing

BY MATHIAS WINTER, HEAD OF PIEZO DRIVES & SYSTEMS TECHNOLOGY, GLOBAL RESEARCH AND MARKUS WIEDERSPAHN, CORPORATE COMMUNICATIONS, PHYSIK INSTRUMENTE L.P. (PI)

THE 14ACMOS project is part of Horizon Europe, the EU's key funding program for research and innovation for the period of 2021 to 2027 with a volume of more than € 95 billion. It tackles climate change, helps to achieve the UN's Sustainable Development Goals, and boosts the EU's competitiveness and growth.

Horizon is divided into six clusters, of which cluster 4 addresses "Digital, Industry & Space", funded with more than € 15 billion. With a total of currently 127 projects cluster 4 aims to strengthen the competitiveness of European companies in semiconductor and photonics industries.

The 14ACMOS project (14ACMOS = 14 Angstroem Complementary Metal-Oxide-Semiconductor) within Horizon aims to develop solutions for the 1.4 nm process technology node. Project activities address four key pillars: lithography, metrology, mask-infrastructure, and process technology.

Lithography solutions will be pushed to meet 1.4 nm capability, and extreme UV plasma physics will be studied to optimize optics transmission and lifetime. In the metrology pillar, advanced methods will be developed to improve measurement sensitivity and uncertainty and to assess reticle degradation induced by extreme UV light. Mask-infrastructure will cover the development of mask repair strategies based on particle removal technology and will assess durability. Process technology involves the development of patterning solutions, active device selection, and new interconnect technology, which are suitable for the 1.4 nm technology node.

The 14ACMOS project started in December 2022 and is set to end in November 2025. Total cost of the project sums up to € 94.6 million with an EU contribution of € 21.8 million. The project is coordinated by ASML. Participants are among others Carl Zeiss SMT, Trumpf, Applied Materials, KLA, Physikalisch-Technische Bundesanstalt (PTB). European players like ASML, Carl Zeiss SMT, and PI have contributed to every step of miniaturization in semiconductor manufacturing along the way from several microns down to the 1.4 nm node. To reach precision of 1.4 nm, new actuator and motor concepts, sensors and (control) algorithms for the drives must be developed, besides advancements in process technology, improved optics, and materials.

This project is co-funded by the European Union under grant agreement No 101096772 and is supported by the Chips Joint Undertaking and its members.

“Funded by the European Union. Views and opinions expressed are however those of the authors only and do not necessarily reflect those of the Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.”

PI offers 50 years of experience in piezo technology and nano positioning, a broad technological spectrum, and a high level of vertical integration in order to develop and provide components and systems that are optimally tailored to the respective process: From the very beginning, the basis for this consisted of mechanical motion systems (actuators and motors) and the appropriate bearing technology, sensors for recording the distance traveled and for determining the absolute position, algorithms for the firmware and an extensive collection of software interfaces and control technology. As a decade-long system partner of semiconductor equipment manufacturers and in particular the main participants in the 14ACMOS project, PI contributes its expertise and experience to the development of innovative motion solutions. The focus here is on very demanding motion and positioning tasks that require precision in the nanometer and sub-nanometer range. A particularly important aspect of some of the applications is the need to operate the systems under vacuum conditions. PI also offers suitable technologies and options for this.

A wide range of drive technologies

The field of semiconductor manufacturing, and the 14ACMOS project in particular, presents a unique challenge for motion systems: the combination of long travel distances (up to hundreds of millimeters) with high dynamics, speed, and precision down to the nanometer range. PI meets these challenges head-on with a comprehensive portfolio of drive technologies.

Electromagnetic drives

In the class of electric motors, PI offers rotating electric motors such as DC or stepper motors. These are used in connection with screw or worm drives. Stepper motor systems with high-resolution encoders can perform minimum incremental motions of 10 nm with high reliability and repeatability.

➤ Application examples of magnetic direct drive technology.

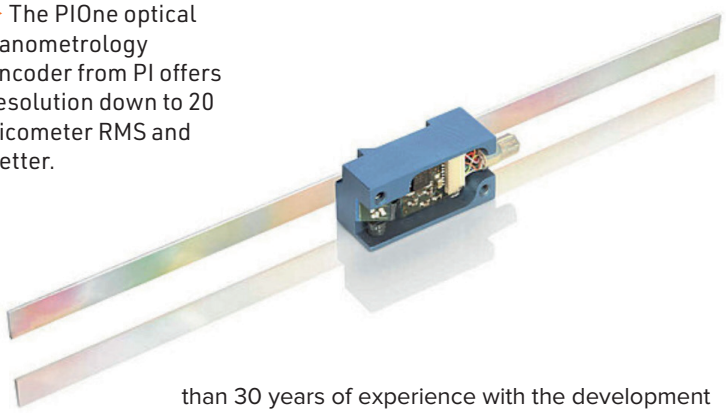
Also, in the field of magnetic direct drives, a wide range of technologies is at hand, namely voice coil motors, iron-core and ironless linear motors, and torque motors.

Piezo-based actuators and drives

The motion of piezo actuators is based on solid-state effects, giving them unlimited resolution in principle. Their stiffness is very high, enabling high force generation and dynamics. Their rapid response time in the microsecond range is a result of their high resonant frequency which can reach more than one hundred kilohertz. Actuator travel in the range of several ten micrometers can be mechanically amplified to reach more than 1 mm. The combination of extremely high resolution and small travel ranges requires the use of suitable guiding elements which are typically flexures that enable highest accuracy by avoiding friction, play and backlash.

Piezo actuators, that are preloaded against a guided runner can be utilized to build linear motors with motion resolution of far below one nanometer. PiezoWalk® piezo motors from PI offer unique capabilities which perfectly match with the needs of semiconductor manufacturing. This nonmagnetic, vacuum-compatible, and clean-room-compatible technology is based on more

➤ The new N-332 linear stage utilizes the PiezoWalk® technology.



➤ The PIOne optical nanometrology encoder from PI offers resolution down to 20 picometer RMS and better.

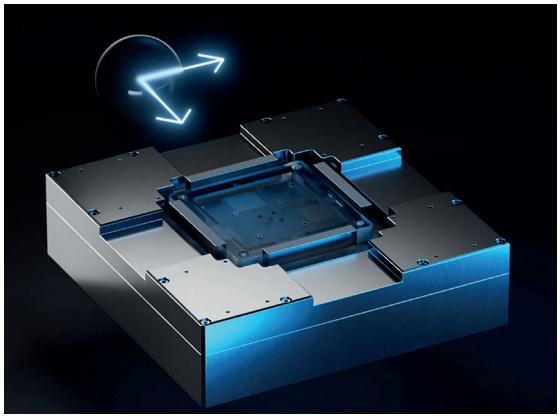
than 30 years of experience with the development and production of piezoceramic components. PI received the SEMI Technology Innovation Showcase Award for the PiezoWalk® technology in 2005. The drives are continuously developed further, and a large number of variants are now available for different areas of application.

Resolution of these drives goes down to 30 picometer, travel ranges are scalable due to scalable runner length. Feed forces are in the range of 50 N to several 100 N. These drives are self-locking when switched off thus saving energy and reducing the generation of heat.

The latest addition to this product family, the N-332 linear stage, is configurable for use in multi-axis setups involving the X, Y, Z axes, and the XY, XZ, and XYZ planes. For applications that require operation in vacuum, the N-332 stages are available in configurations suitable for pressures as low as 10-9 hPa. The PICMAWalk piezo motor inside the N-332 stage is based on PI's proprietary PICMA® piezo actuators.

A highly specialized application of piezo-based components are so-called PIRest actuators. With a load capacity of up to 4000 N per actuator and micrometer displacement with nanometer resolution, these components are ideally suited for drift compensation in machines, for alignment of optical components and static precision positioning.

Sometimes it is even necessary to combine motion systems that enable long-stroke movements, such as linear drives or piezo motors, with piezo-based actuators. Actuator and drive technologies are only one aspect considering the overall system properties. Optimal performance as required in applications targeted in the 14ACMOS project can only be achieved by implementing new and sophisticated control algorithms and the next generation of high-resolution sensor technology.



➤ Magnetic levitation is a promising technology for high-precision motion in six degrees of freedom.

The right position sensor technology

Position sensing systems are required to provide feedback to the motion controller. Linearity and repeatability of motion and positioning tasks are not possible without highest-resolution measuring devices. Accuracies in the range of a few nanometers and below require a position measurement method that can also detect motion in this range. PI can also draw on extensive experience and a comprehensive portfolio of technologies developed in-house in this discipline. Examples comprise capacitive sensors and optical nanometrology encoders. The latter achieve a resolution of 20 picometer and better due to their small signal period of 500 nm and the optimized signal processing.

New magnetic levitation stages

The PI Group is committed to meeting the demanding objectives of the 14ACMOS project through the enhancement of existing technologies and the creation of novel and transformative new solutions. PI is also engaged in the development of new technologies beyond the scope of the 14ACMOS project. One illustrative example is that of magnetic levitation (maglev) stages with six degrees of freedom. One major benefit of this technology is the avoidance of any friction in the process chamber, eliminating the risk of particle contamination.

To employ this principle for the execution of high-precision movements, the magnets in the base are designed as electrically controllable coils. In order to enable movements in all six degrees of freedom, a corresponding number of magnet pairs is required. In a multitude of practical applications, Halbach arrays are employed to reduce energy consumption, augment load capacity, and diminish heat dissipation.

The combination of magnetic guidance and dedicated high-precision drive and sensor technologies provides high dynamics and the highest resolutions down to the picometer range. Active control and definition of guiding characteristics in up to six degrees of freedom can enable additional correction tasks such as focusing in Z or adjusting tip/tilt during operation. The frictionless guiding principle, which is free of rolling elements, lubrication, and air flow, will ensure the highest precision over the entire service life and allows use in cleanroom environments.

Controller technology

As demands on the precision, dynamics, and speed of mechanical motion systems increase, so too does the complexity of the control systems. The selection

of an appropriate control technology is therefore of paramount importance. In particular, the control of piezo actuators and piezo-based positioning systems requires a high degree of specialization. PI has gained extensive experience in this field over decades. The characteristic properties of piezo actuators include the generation of large forces and fast response. In electrical terms a piezo element corresponds to a capacitance. A rapid change to the operating voltage brings about a rapid displacement of the actuator and thus a change in position.

When the control voltage suddenly increases, the piezo actuator can achieve its nominal displacement in only a few microseconds. A prerequisite for this is that the power supply provides sufficient current to charge the capacitance. For steady state operation, i.e., when holding a certain position, the stability of the power supply is crucial, as the piezoelectric actuators already respond with motion to the slightest voltage changes. Noise or drifting must therefore be avoided as far as possible.

With all these special features, PI benefits from more than 30 years of experience in the manufacture of piezo elements and the development of piezo-based positioning systems. PI is one of the few companies in the world with access to the entire value chain: from piezo development and production to the development of piezo-based motion systems and control technology.

PI can also look back on an even longer history of innovation in electric motor control technology. In addition to own cutting-edge solutions, PI leverages the expertise of ACS Motion Control, a wholly owned member of the PI Group based in Israel. Magnetic levitation stages exemplify the necessity for sophisticated control technology. In this context, the linear stage platform is not constrained by mechanical bearings, allowing for unimpeded movement within a single degree of freedom. Consequently, a robust multi-axis controller with a high bandwidth is essential to maintain control over all other degrees of freedom.

Conclusion

The 14ACMOS project presents completely new challenges and tasks for all involved. Precise positioning plays a key role in many processes. For example, in the manufacture, inspection (quality control) and repair of lithography masks. In wafer inspection, it supports the detection of structural failures, defects and particles. Precise positioning is also essential in the lithography process, and in wafer metrology, for example for measuring layer thicknesses and overlay offsets.

With a comprehensive portfolio of precision positioning technologies and complementary expertise in sensor, control, motion and force transfer technologies, PI is well positioned to support this technology node.

Cost-effective SiC substrate manufacturing for power devices enabled by oxide-free wafer bonding

Silicon Carbide (SiC) power devices are seen as a game-changer in the automotive industry.

BY BERND DIELACHER AND PETER KEREPESI, EV GROUP

THESE ADVANCED semiconductor devices offer superior device performance compared to conventional silicon-based devices. SiC as a material has a 3x wider bandgap, 10x higher breakdown voltage and a 5x higher thermal conductivity.

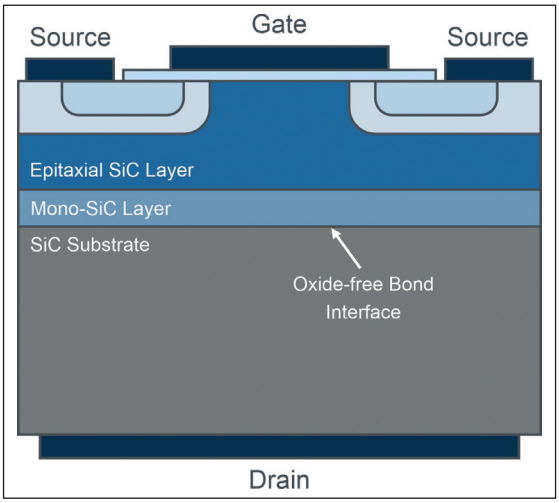
These properties ultimately translate into faster EV charging and more efficient and reliable automotive fleets. Large investments in new SiC wafer fabs underline the high interest from the automotive sector. However, SiC manufacturing processes are far from being as mature as silicon processes. Significant developments along the entire process chain are needed to pave the way for a SiC-based future of the EV industry.

Challenges include the high costs associated with substrate manufacturing, the complex processing of SiC, limited economies of scale and overall yield issues. In particular, the substrate is a major concern as it accounts for the largest share of production costs. Many routes are currently being explored to address this issue including improvements of crystal growth or novel wafer slicing technologies. The transition to 8-inch manufacturing is also expected to reduce substrate costs. This will only pay off in the long term as the processes for this scale are more complex and still need to be established and optimized. Another way of reducing substrate costs is the use of wafer bonding to utilize the expensive high quality SiC material more efficiently.

Wafer bonding is an established process in power device manufacturing, in particular temporary bonding is commonly used to support substrates during device thinning. Wafer bonding is not only used for device manufacturing, but also enables new types of substrates. In the case of SiC MOSFET power devices, the main structure is built into a thin epitaxial SiC layer, commonly grown on monocrystalline SiC wafers. SiC crystal growth defects can be minimized or eliminated during the epitaxial process and epi-layers can be efficiently electrically tuned by doping.

However, only high-quality monocrystalline SiC substrates provide the required electrical device performance but contribute significantly to the overall chip cost. Since this material is mainly required as a seed layer for the epitaxial process, using only a thin layer and substituting the bulk material with a polycrystalline or lower quality monocrystalline substrate is seen as a viable route to address this cost issue (Figure 1).

Such a process generally involves wafer bonding of the two materials as well as a method to produce a thin layer from the high-quality monocrystalline substrate and reuse the remaining substrate multiple



➤ Figure 1. SiC power MOSFET structure using a cost-effective engineered substrate (thin high quality monocrystalline SiC layer bonded on a less-expensive SiC substrate).

times. Several methods for the thin layer generation have been demonstrated, including the well-known ion-implantation and splitting process. This article focuses on the wafer bonding process and presents the latest developments for this application using EVGs high-vacuum ComBond® cluster system.

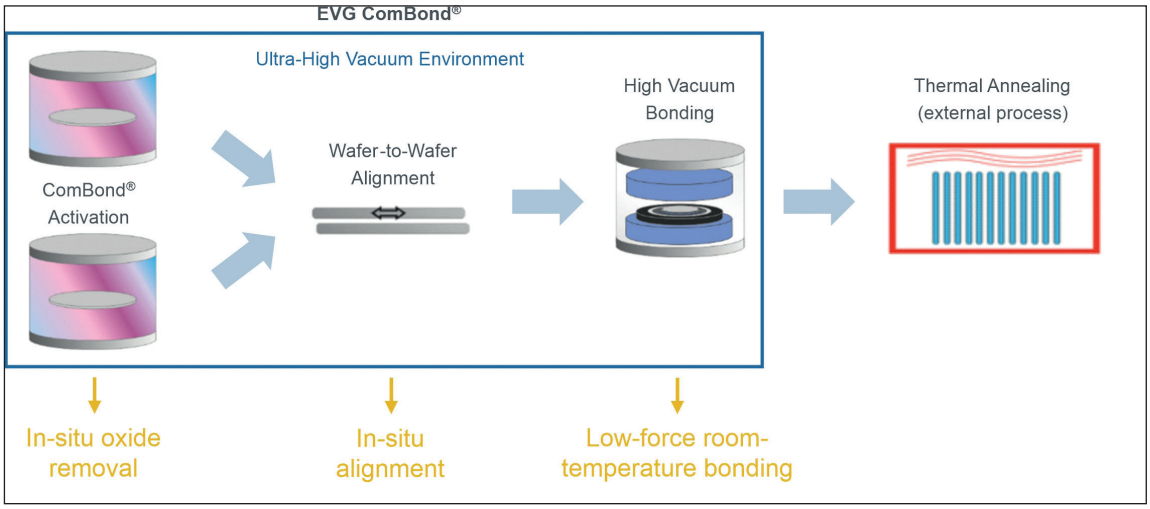
The ComBond® system (Figure 2) offers covalent fusion bonding at room temperature, enabling heterogenous integration of various materials with different lattice constants and thermal expansion coefficients. Processing at room temperature does not induce additional stress in the materials, thus initial wafer bow is not increased. While classical fusion bonding is based on oxide-oxide bonding, the ComBond® process relies on a surface activation process called ComBond Activation Process, which is based on oxide removal by ion beam sputtering. Any re-oxidation is prevented by wafer handling and bonding the wafers in an ultrahigh vacuum environment. The result is a seamless transition between the two bulk materials without any intermediate layer. Table 1 summarizes the key differences between the two technologies. Oxide-free wafer bonding enables electrically conductive interfaces, which is the most important requirement for engineered substrates with respect to the structure of vertical SiC power MOSFETs.

➤ Figure 2. EVG ComBond® - Automated High-Vacuum Wafer Bonding System

Oxide-free SiC-SiC wafer bonding optimisation and characterization

SiC bonding has been investigated using monocrystalline 4H SiC wafers, including incoming metrology, characterization of the activation process and analysis of the final bonded wafer pairs. The bonding process (Figure 3) starts with oxide removal from both wafer surfaces using an ion beam sputtering process (ComBond® Activation), followed by wafer-to-wafer alignment and transfer to the bonding chamber without breaking the ultrahigh vacuum (< $5{\cdot}10^{-8}$ mbar). Finally, the wafers are bonded at room temperature with low force. External annealing allows further optimization of the bond interface.

A general prerequisite for fusion bonding is a very low surface roughness of the incoming wafers (< 0.5 nm). The initial values of the SiC wafer were well below this requirement and it was confirmed that ion beam sputtering does not lead to a significant increase in surface roughness during the activation process, thus a good bond quality can be expected with respect to this parameter. Nevertheless, the activation process leads to numerous surface effects (see Table 1), which need to be well understood and controlled. Figure 4 illustrates different stages of surface activation and their optimization in terms of bonding energy.



➤ Figure 3. Oxide-free wafer bonding process of SiC using EVG ComBond® technology.

Parameter	Plasma Activated Fusion Bonding	ComBond® Technology
Pre-treatment	RF plasma	Ion beam sputtering
Surface effects	* Surface energy modification	* Oxide removal
	* Surface microroughness	* Dangling bonds generation
	reduction	* Chemical functionalization
	* Oxide layer growth	* Stoichiometry modification
	* Chemical Functionalization	* Amorphous layer generation
	* Contaminant removal	(few nm range)
Environment	Ambient air	Ultrahigh vacuum
Post-bond annealing	Commonly yes (<400 °C)	Commonly no
Bond type	Covalent	Covalent
Bond interface	Oxide-Oxide	Oxide-free (same as bulk material)
EVG equipment	GEMINI® FB	ComBond®

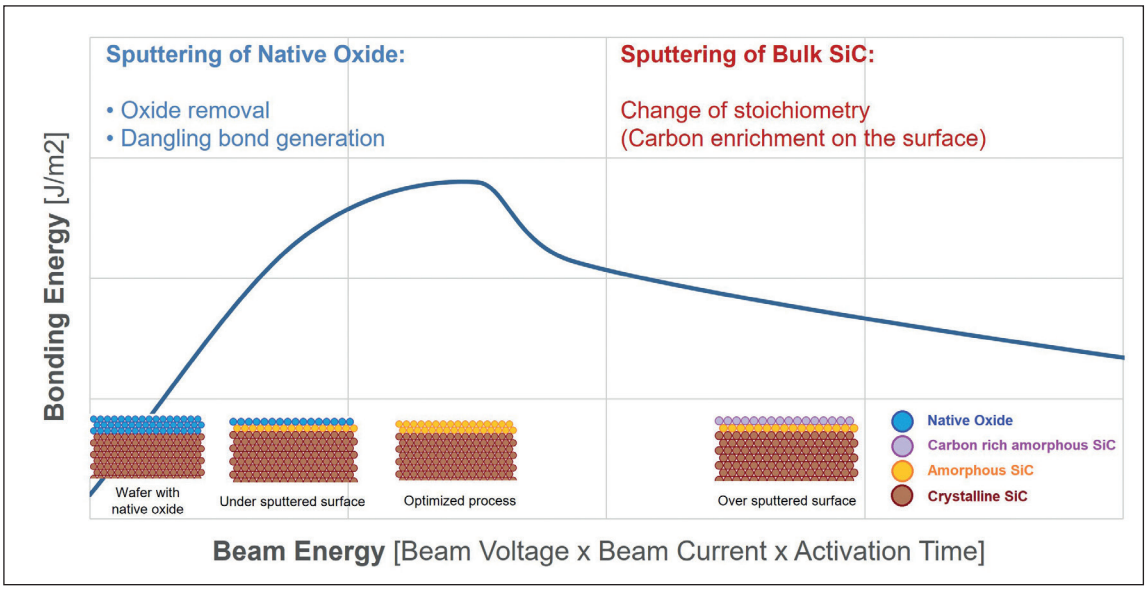
➤ Table 1. Comparison between plasma activated fusion bonding and ComBond® technology.

In the initial phase, ion beam treatment leads to a sputtering of the native oxide, which is gradually removed. At the same time, dangling bonds are formed. During this process, an increase in bonding energy is observed, reaching a maximum after complete oxide removal. The ion beam treatment also generates a thin amorphous SiC layer in the range of a few nm. Due to a preferential sputtering of carbon compared to silicon, this amorphous SiC layer becomes enriched with carbon over time, changing the stoichiometry of the material.

SiC bonding energies of 1.4 J/m^2 were observed with optimized activation parameters. This value is still below the theoretical maximum but much higher than minimum bonding energies required for further processing (0.5 J/m^2). The bonding energies were measured using the Mazara test at 4 locations on the wafer.

The bond interface across the wafer was investigated by Confocal Scanning Acoustic Microscopy (C-SAM). No scratches, delamination or particle related voids were detected, confirming a high quality bonding process (Figure 5a). Cross-sectional analysis of the interface by Transmission Electron Microscopy (TEM) shows a thin amorphous SiC layer (2.1 nm) produced by the sputtering process (Figure 5b). Amorphous layers are generally not of any concern, but they can affect the electrical or thermal conductivity across the interface.

Finally, the bonded SiC wafers were annealed in an external furnace at 1800 °C (kindly supported by centrotherm international AG). While the C-SAM images showed a similar high quality bond interface without any outgassing effects (Figure 5c), the TEM measurements revealed an interesting result. The amorphous layer disappeared completely and a



➤ Figure 4. Bonding energy optimization with respect to surface activation.

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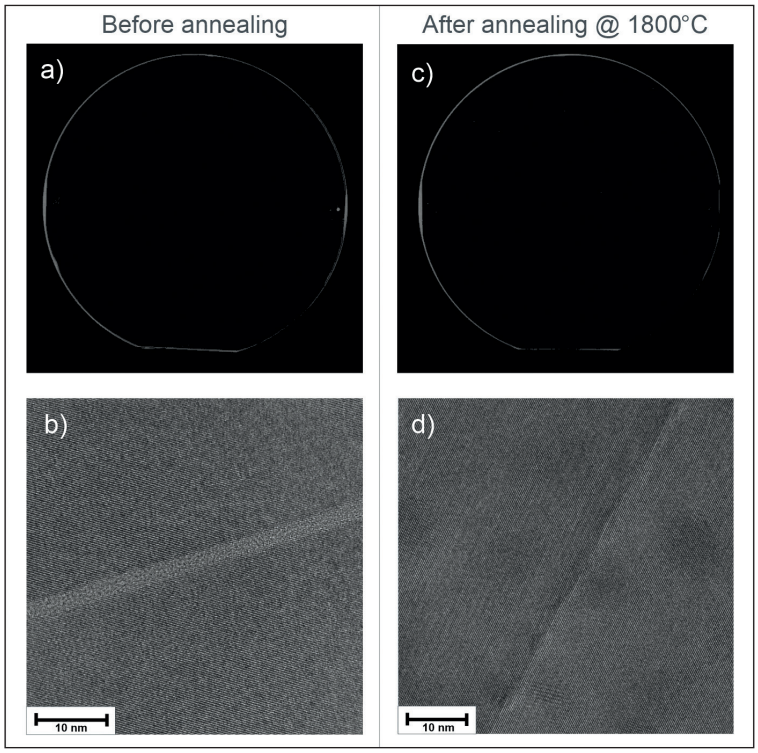

➤ Figure 5.Bonding quality and interface characterization with C-SAM (a, c) and TEM (b, d) before and after thermal annealing.

full recrystallization of the interface was observed (Figure 5d). During the annealing, the electrical characteristic is improving. In addition, the bonding energy increased significantly and reached the fracture energy of bulk SiC. Engineered SiC substrates produced by this oxide-free bonding technique are therefore ideally suited for SiC power MOSFETs.

Recrystallization begins at temperatures as high as 1400 °C. As substrates for this application are processed at high temperatures during epitaxy, no additional annealing is usually required.

Higher temperatures and full recrystallization is not necessarily needed to achieve best electrical performance.

Finally, Energy Dispersive X-ray (EDX) analysis was used to confirm an oxide-free interface (Figure 6). This measurement also shows reduced Si content at the bond interface due to the preferential sputtering of silicon over carbon.

Since characterization of carbon is challenging in the case of EDX, the enrichment of the carbon at the interface was proved by XPS measurements.

High quality SiC wafer bonding has been demonstrated using EVG ComBond® technology. The developed oxide-free bonding process can be used for the volume production of engineered SiC substrates for advanced, cost-efficient vertical power device architecture.

The extensive characterization in this work has been carried out on 4-inch monocrystalline SiC substrates. Successful bonding with similar results and quality has also been demonstrated on the ComBond® system with 6- and 8-inch wafers by now, both mono-to-mono- and mono-to-polycrystalline SiC bonding.

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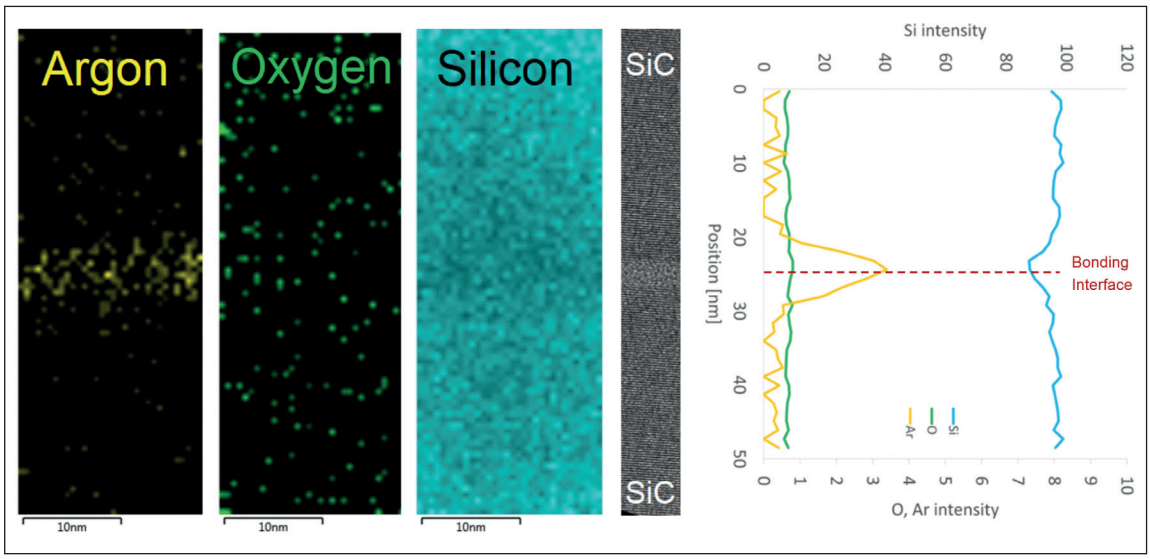

➤ Figure 6. EDX analysis of the bond interface confirms oxide-free wafer bonding.

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High-voltage SiC for storage & MV-grid conversion

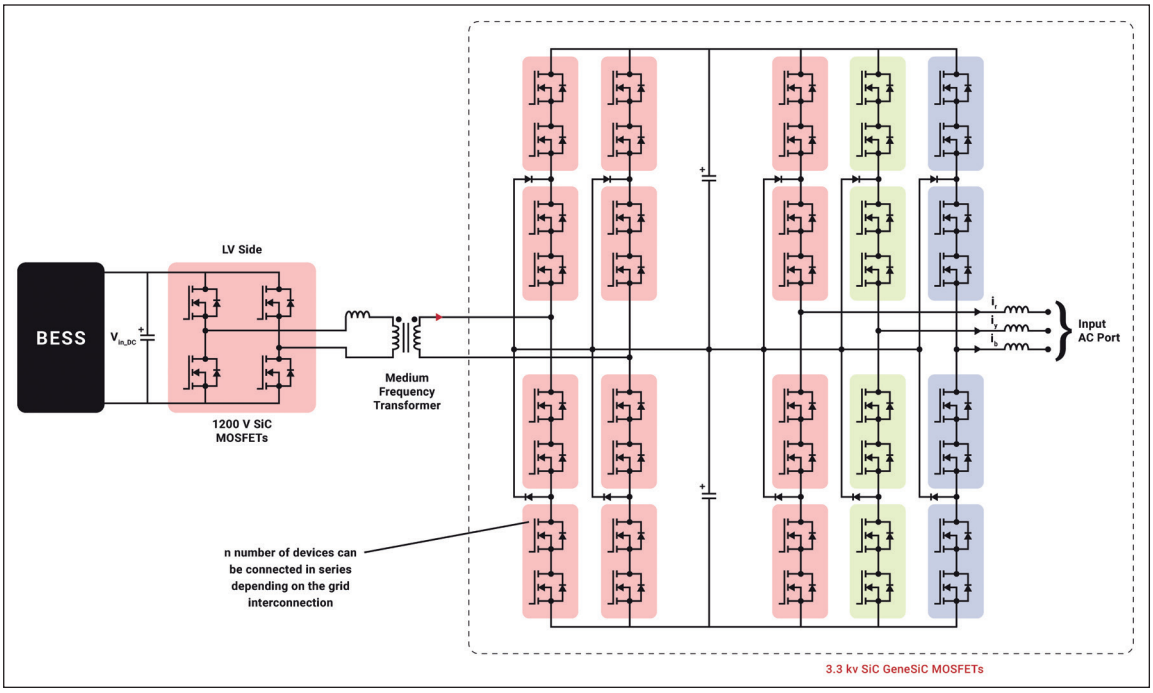
As reliance on renewable energy generation continues to increase, a three-level converter architecture built using high-voltage SiC MOSFETs enhanced with an integrated MPS diode boosts efficiency and reliability in the storage-to-grid connection.

BY RANBIR SINGH, EVP GENESIC, NAVITAS SEMICONDUCTOR AND LLEW VAUGHAN-EDMUNDS, SENIOR DIRECTOR PRODUCT MANAGEMENT AND CORPORATE MARKETING, NAVITAS SEMICONDUCTOR

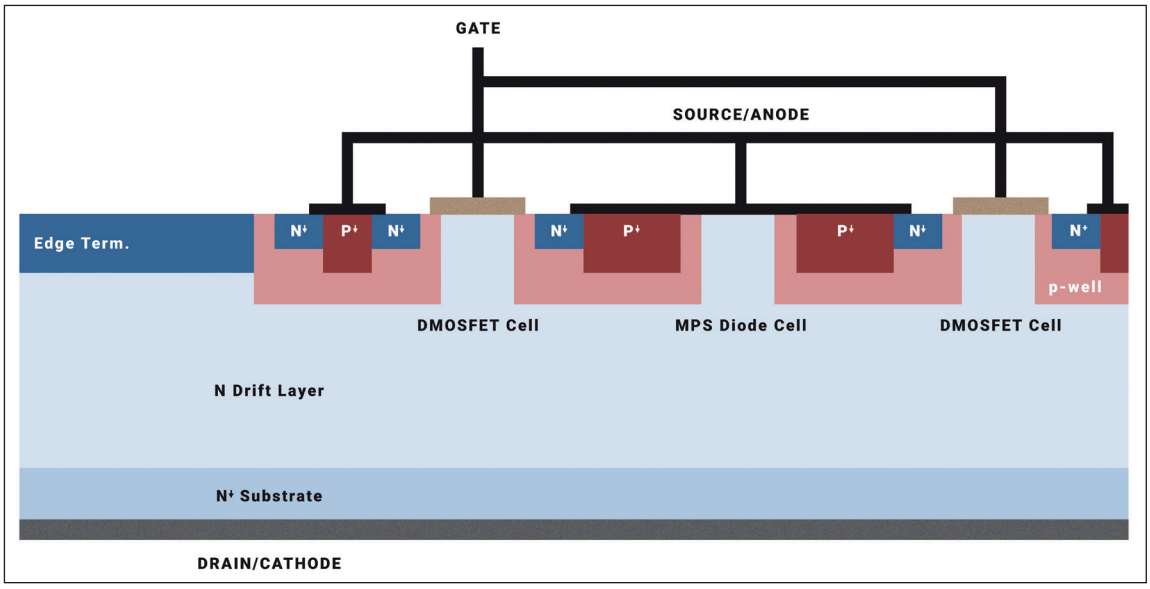
BALANCING THE FLOW of energy into and out of the grid is a perennial challenge for operators, now made tougher as an increasing proportion of energy must come from renewable sources. Historically, pumped hydro-electric has dominated, representing more than 82% of grid-connected storage capacity. It is well suited to providing a long-lasting boost at times when high demand is expected, such as in the early evening.

Wind and solar, which are intermittent and unpredictable, demand storage with different characteristics including faster response time, low/medium energy capacity, easy scalability, and compact size. Battery energy-storage systems (BESS), typically built with Li-ion batteries, can meet these demands. BESS currently represents almost 17% of storage in the US, with about 16 GW of installed capacity in 2023.

Another 15 GW is planned for 2024. In addition to helping balance energy flow, BESS can also help improve the performance of the transmission and distribution network by compensating



➤ Figure 1. Isolated BESS feed-in to MV grid with DAB and AFEC.



➤ Figure 2. 3.3kV SiC MOSFET and monolithically integrated MPS diode.

for disturbances such as voltage fluctuations, frequency variations, phase shifts, harmonics, and interruptions.

BESS to grid connection

The power-conversion network that connects the BESS to the medium-voltage (MV) grid at the utility premises must convert from DC at the battery voltage to AC at the grid voltage and frequency. The network also needs to provide isolation and must support bidirectional power flow to permit charging and discharging as the levels of power demand and generation fluctuate.

There is no standardized topology for the BESS-grid connection. A common approach is to combine a DC/DC converter at the battery with a two-level DC/AC stage, which may be a voltage-source converter for simplicity. Alternatively, this DC/AC stage can be an impedance-source converter (ZSC) to provide buck-boost flexibility. A low-pass filter removes injected harmonics and a transformer provides isolation as well as converting between the battery voltage and the grid voltage.

An alternative approach combines a dual active bridge (DAB) with an active front-end converter (AFEC), as in figure 1. The three-level, neutral-point clamped architecture allows simplified filtering, compared to the two-level topology. In addition, this arrangement reduces voltage stress across the MOSFETs, which helps enhance reliability.

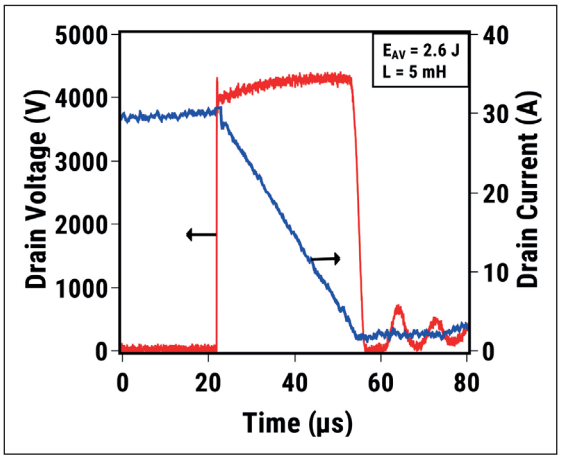
In the pursuit of maximum efficiency, silicon carbide power semiconductors have become the technology of choice in the converters used to connect the BESS to the MV grid. At the connection to the battery storage system, the DAB can be built with 1,200 V SiC MOSFETs. On the other hand, the MV-grid voltage can be as high as 13.8 kV or more. A suitable AFEC can be built using an array of silicon IGBTs or 1.7 kV SiC MOSFETs to safely handle the full MV-grid voltage. A different approach using 3.3 kV SiC MOSFETs allows a significant reduction in the component count, permitting smaller physical size, higher system efficiency, and lower operating temperature.

Enhanced SiC MOSFET structure

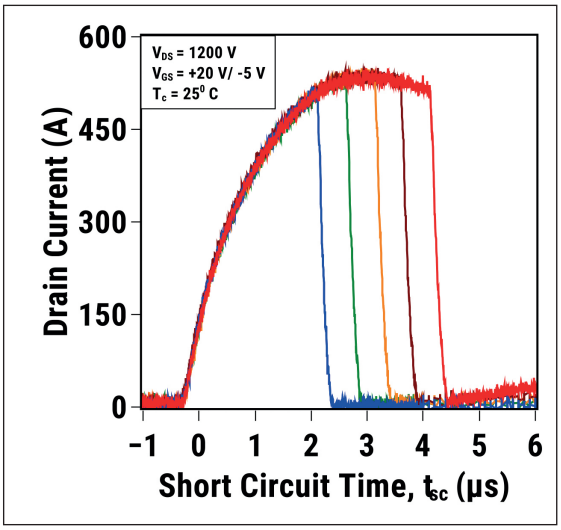
In high-voltage, high-power applications like the three-level AFEC, a Schottky diode can be connected across each MOSFET to handle freewheel currents efficiently and improve reliability. A proportion of the current also passes through the MOSFET's intrinsic body diode.

Conventional SiC MOSFETs can be vulnerable to faults at high applied voltage when the body diode is conducting. This is due to potential basal plane dislocations (BPD), which are defects present in the crystal structure from the earliest stages of SiC boule fabrication and wafer epitaxy. To overcome this, Navitas monolithically integrated a merged PiN-Schottky (MPS) diode with the 3.3 kV SiC MOSFET. In principle, MPS diodes combine the strengths of standard PN-junction (PiN) diodes, namely their high surge-current robustness and low reverse leakage, with the low forward voltage (VF) of a Schottky diode. The Schottky structure carries almost the entire current in normal operation, while the PiN diode conducts during high-current surges, which reduces dissipation and relieves thermal stress on the device.

Monolithic integration of the MPS structure in the 3.3 kV SiC MOSFET (figure 2) bypasses the built-in P-well/N-drift body-diode and so avoids the possibility of BPD faulting within the MOSFET N- drift layer. The inherently low VF of the MPS diode also effectively reduces the conduction and switching losses of the intrinsic body diode. Moreover, eliminating an externally packaged Schottky diode removes parasitic inductances associated with the physical connection and reduces the bill of materials. The integrated MPS diode also permits temperature-independent switching and simplifies device paralleling.



➤ Figure 3. Avalanche robustness of 3.3 kV SiC MOSFET with MPS.



➤ Figure 4. Short-circuit pulse testing of SiC MOSFET with MPS.

Testing the 3.3 kV SiC/MPS devices

Unclamped inductive switching (UIS) measurements have been performed to investigate avalanche robustness of the 3.3 kV SiC devices for AFEC applications. Inspecting the drain current/voltage waveforms at 30A peak drain current, as seen in figure 3, shows that the drain voltage peaks at 4,200 V during the test.

The maximum avalanche-withstand time (tAV) is 35 µs and single-pulse avalanche energy (EAS) is 2.6 Joules. In comparison, the test performed on a discrete 3.3 kV discrete SiC MOSFET with the same load-inductance showed an EAS of 4.8 Joules.

Short-circuit robustness of the GeneSiC MOSFETs was evaluated by connecting 3.3 kV discrete SiC MOSFETs, mounted on a 25°C baseplate, to a 1,200 V DC link. Devices both with and without monolithically integrated MPS diodes were tested. The devices were operated with +20 V / -5 V gate-drive. The drain current increases to a maximum of 525 A during the short-circuit pulse, as figure 4 shows. The short-circuit withstand time was measured to be 4.5µs.

Hybrid architecture – 'Trench Assisted Planar' technology

SiC MOSFETs are typically fabricated using either planar or trench architecture. Planar fabrication allows high process yield, while its relatively simple device structure enables excellent reliability. On the other hand, trench devices typically have higher RDS(ON) per die area and a figure of merit (FOM) that allows for faster switching performance. Navitas' trench-assisted planar' technology architecture combines the higher yield and reliability advantages of the planar structure with the low RDS(ON) per die area, fast switching, associated with trench technology. Building 3.3 kV MOSFETs that combine this hybrid architecture with the integrated MPS diode creates a power switch that is well suited to use in three-level AFECs at the MV-grid voltage in BESS applications.

Conclusion

Battery storage has the characteristics needed to balance supply and demand in utility grids that are becoming increasingly reliant on renewable energy sources. The battery array needs an efficient, robust, and reliable connection to the medium-voltage grid. This circuit must convert between the battery and MV-grid voltages as well as allowing bidirectional operation for charging and discharging of the battery. Silicon carbide is the power technology of choice, for its switching efficiency and its ability to withstand high applied voltage, short-circuit current, and avalanche energy.

A three-level front-end converter built with 3.3 kV SiC MOSFETs ensures high efficiency and requires minimal filtering. With the added benefit of an integrated MPS diode, these devices deliver enhanced reliability while also handling freewheeling currents efficiently and minimising component count and parasitic circuit inductances.

Navitas' trench-assisted planar' technology architecture combines the higher yield and reliability advantages of the planar structure with the low RDS(ON) per die area, fast switching, associated with trench technology. Building 3.3 kV MOSFETs that combine this hybrid architecture with the integrated MPS diode creates a power switch that is well suited to use in three-level AFECs at the MV-grid voltage in BESS applications

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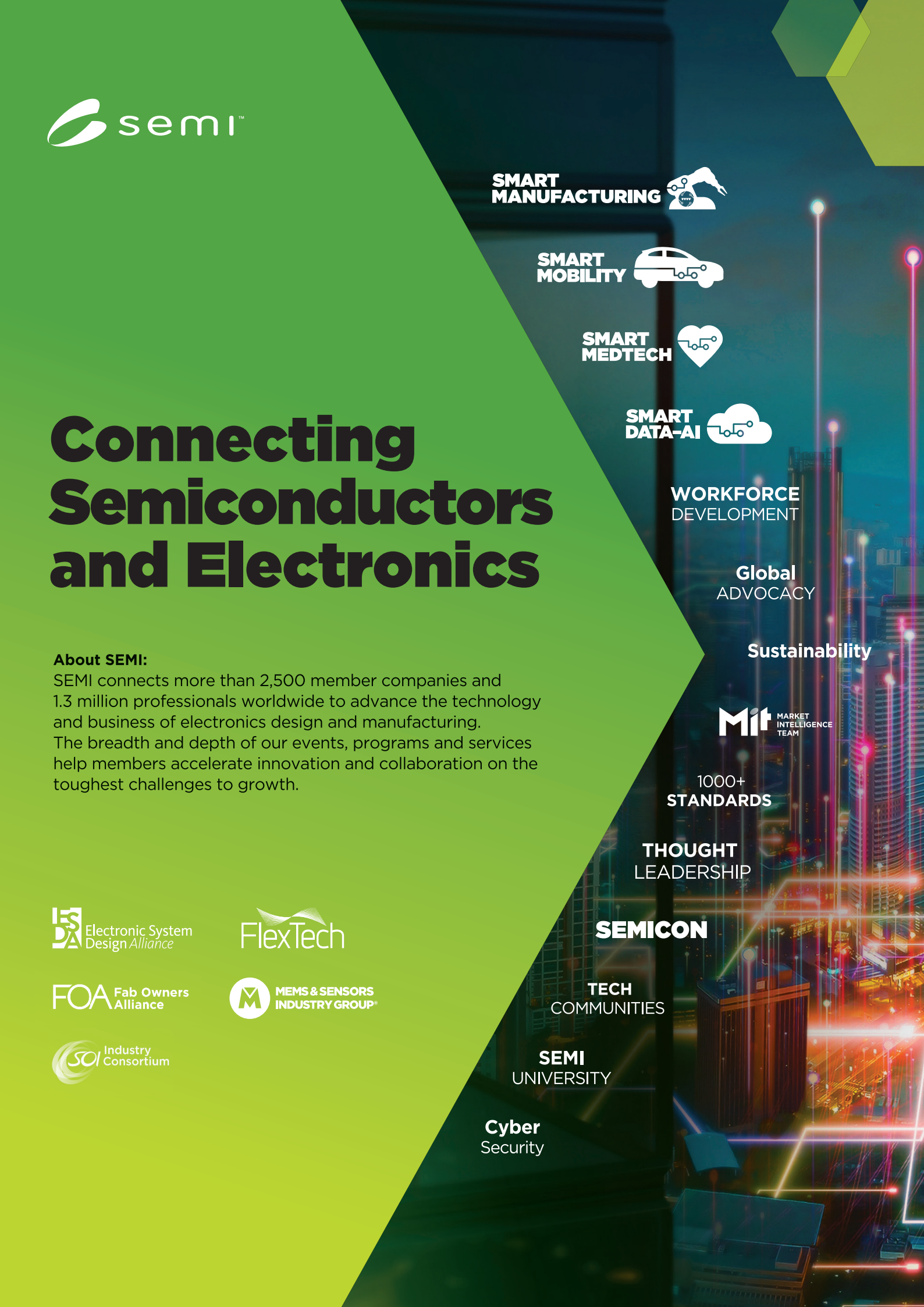
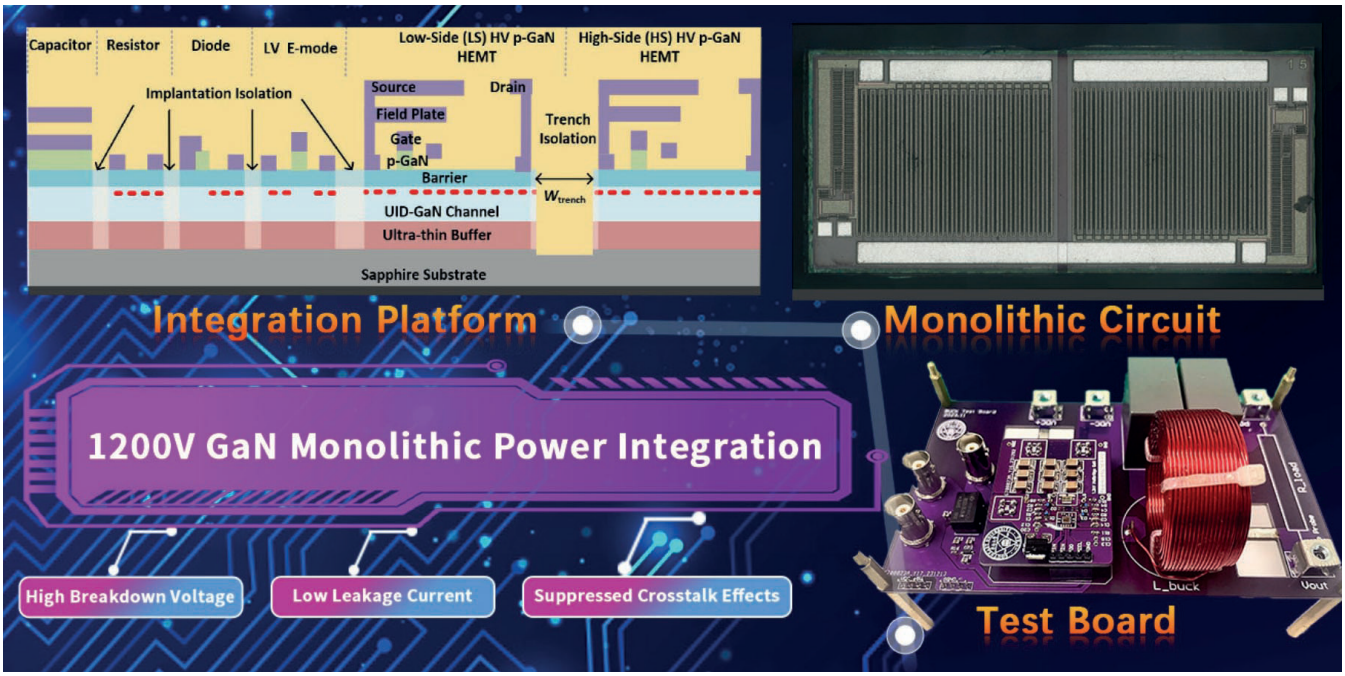




1200 V GaN monolithic power integration

Sapphire substrates with ultra-thin buffer layers provide a foundation for fabricating systems offering 1200 V GaN-based monolithic power integration while supressing crosstalk

BY SHENG LI, SIYANG LIU AND WEIFENG SUN FROM SOUTHEAST UNIVERSITY AND TINGGANG ZHU FROM CORENERGY SEMICONDUCTOR

OUR ELECTRIFIED WORLD contains countless examples of energy conversion. Within this sector the GaN-based power device attracts extensive attention, thanks to its capability to switch high voltages at high speeds. However, there are concern associated with this wide bandgap technology. In power systems featuring GaN, inductive elements generate rings and spikes during switching, ultimately leading to an increase in fault risk.

One increasingly popular way to address this concern is to eliminate the parasitic inductive elements by turning to a monolithically integrated gate driver and half-bridge configuration. However, this approach is compromised, with state-of-art GaN based monolithic integration limited to 650 V. That's far from ideal, given the rapid development of power electronic systems requiring power devices with a rated voltage above 1200 V.

The conventional foundation for GaN power devices is the silicon substrate. While it is low in cost and widely available, it is impaired by a conductivity that is to blame for the vertical breakdown and crosstalk in conventional 650 V GaN-on-silicon platforms.

These are significant limitations, hampering efforts to increase the rated voltage of monolithic integration.

Progress demands a more radical approach, such as the one we are taking at Southeast University and CorEnergy Semiconductor. Our partnership is pioneering an ultra-thin buffer technology with shallow trench isolation on a sapphire substrate. Using this approach, we have realised a 1200 V monolithic half-bridge integration platform that supresses crosstalk.

Fabrication of our platform begins by loading sapphire substrates into an MOCVD reactor and depositing a 100 nm-thick undoped ultra-thin buffer, followed by a 300 nm-thick undoped GaN channel layer and a 15 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier layer ((see Figure 1(a)). This epitaxial structure is capped with a 100 nm-thick *p*-GaN cap layer, magnesium doped at a level of 2×10^{19} cm^{-3}.

To produce devices from this epilayer, we define a trench with a dry etching process based on BCl_3/Cl_2 – this follows an implantation process (see Figure 1(b)). We suppress the influence of

sidewall traps along the trench by surrounding it with an implantation area. Our other fabrication processes are consistent with those of a normal *p*-GaN HEMT (see Figure 1(c) for an overview of our key fabrication processes).

Our ultra-thin buffer technology allows us to realise wafer-level integration of high-voltage (HV) and low-voltage (LV) enhancement-mode *p*-GaN gate HEMTs with LV passive elements, including diodes, resistors, and capacitors. Undertaking shallow trench isolation by etching the ultra-thin buffer is a relatively easy process, which supresses crosstalk between high-side and low-side HV *p*-GaN HEMTs. Following etching, we fabricate our monolithic half-bridge circuits with gate buffers (see Figure 1(d)). The formation of our integration platform is relatively quick and material costs are low, making this an attractive technology for mass production.

Ultra-thin buffers

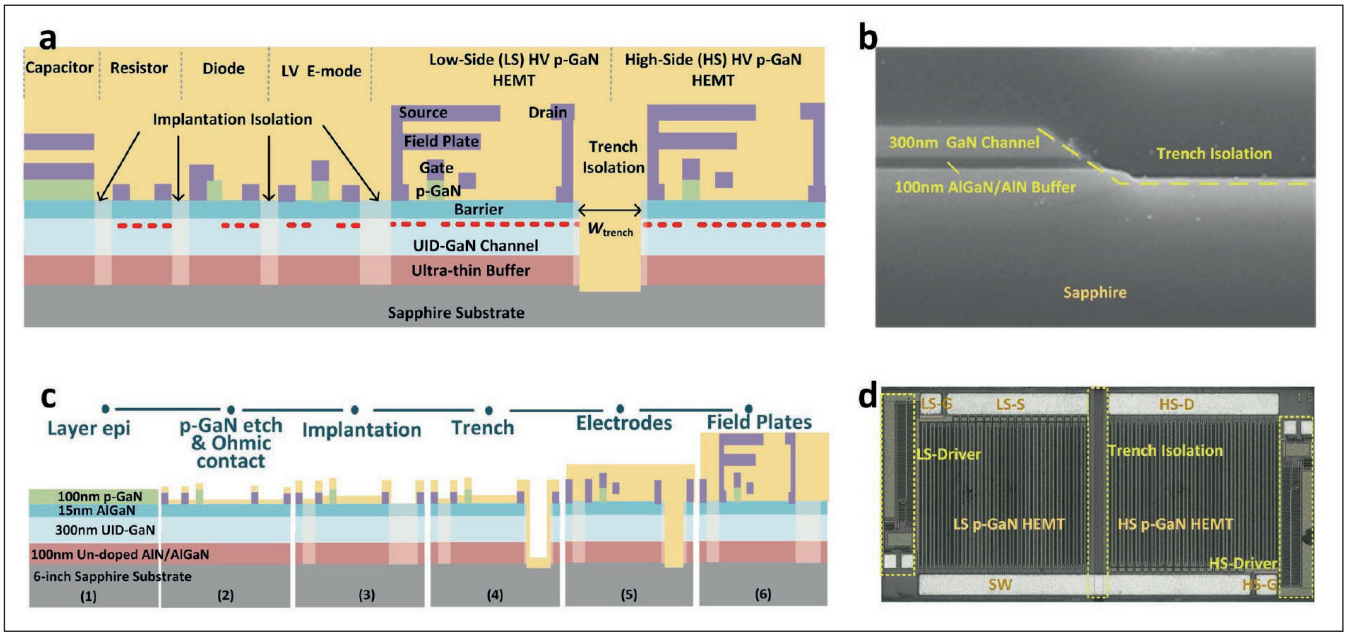
It is essential to eliminate the traps caused by heteroepitaxy, as they threaten to impair mobility in the GaN channel. With conventional GaN-on-silicon HEMTs, traps are typically suppressed by combining a nucleation layer with a thick buffer layer. Switching to a sapphire substrate reduces lattice mismatch with the GaN-based epilayers and enables a 100 nm-thick undoped ultra-thin buffer layer to suppress traps from the substrate and ensure a high-quality GaN channel.

Additional attractive features of our architecture are that it provides a low lateral leakage current and a high lateral breakdown voltage, thanks to the ease of depletion of the thin buffer and the channel under the gate region. What's more, due to the isolated sapphire substrate, the vertical blocking voltage can be increased without needing a thick buffer.

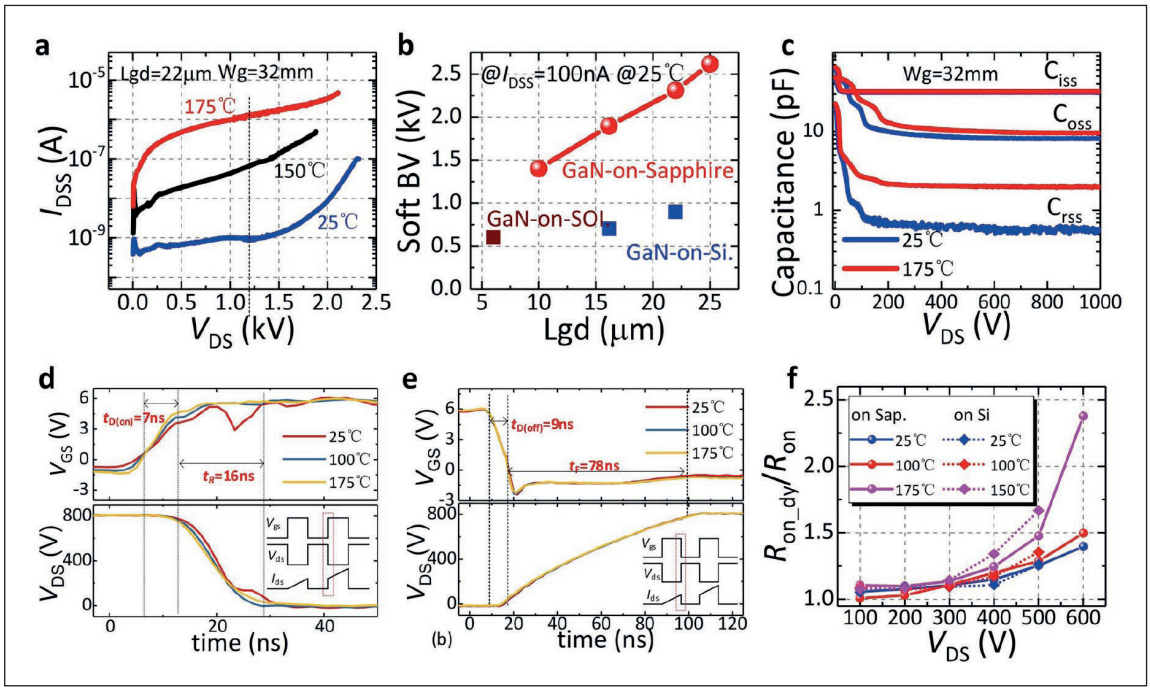
Electrical measurements underscore the superior blocking characteristics of our HV *p*-GaN HEMTs, which benefit from an ultra-thin buffer. We have realised a blocking voltage of more than 1400 V for a gate-to-drain length of just 10 μm in our *p*-GaN HEMT (see Figure 2(a) and 2(b)). This equates to 140 V/μm, which is 140 percent of that of a SOI-based *p*-GaN HEMT. To ensure a healthy safety margin, for devices rated at 1200 V we propose a gate-to-drain length of 22 μm – this geometry offers a blocking voltage of over 2300 V.

Other encouraging results from our HV *p*-GaN HEMT include its capability to withstand transient voltages higher than 1400 V for 10 ms, an attribute that helps improve reliability when an overvoltage event occurs. At a drain-source voltage of 1200 V, the drain leakage current is less than 100 pA/mm and 100 nA/mm at 25 °C and 175 °C, respectively. That's a leakage current level about two orders of magnitude smaller than that for GaN-on-silicon HEMTs. For those devices, the leakage current at high voltages rapidly increases with drain voltage, due to parasitic channels and vertical leakage caused by the conductive substrate. Our devices offer an extremely low drain leakage current, due to the isolated substrate and the undoped ultra-thin buffer, and they benefit from successful suppression of the parasitic channel at the interface between the epitaxial layers and the substrate.

We have also evaluated the dynamic electrical performance of our HV *p*-GaN HEMT (see Figure 2(c)-(e)). At high temperatures there is variation in terminal capacitances, but the influence on switching speed can be neglected, according to double pulse test results. Values for the turn-on delay time and rise time indicate fast switching



➤ Figure 1. (a) 1200 V E-mode GaN based monolithic half-bridge integration platform on sapphire. (b) Photos of trench isolation. (c) Key fabrication processes. (d) Scanning electron microscopy of 1200 V GaN-HEMT monolithic half-bridge integration.



➤ Figure 2. (a) Blocking characteristics of a HV *p*-GaN HEMT. (b) Extracted blocking voltage with different gate-to-drain lengths (L_{gd}). (c) Terminal capacitances at different temperatures. (d) Double pulse test switching characteristics of the turn-on process. (e) Double pulse test switching characteristics of the turn-off process. (f) Comparisons of the dynamic on-resistance between GaN-on-sapphire and GaN-on-silicon HEMTs.

speeds, even at 800 V. The turn-off delay and fall times are longer than they might be, due to a large external turn-off resistance of 30 Ω and a small switching current 1.5 A.

A big concern for all power GaN HEMTs is the dynamic on-state resistance, with higher values increasing conduction loss and junction temperature. We have used a test circuit to provide a highly accurate comparison of the dynamic on-state resistance of conventional GaN-on-silicon HEMTs and our HV *p*-GaN HEMTs. This investigation revealed that our devices have the upper hand in this regard, thanks to a reduction in the general trap activation energy, resulting from the undoped ultra-thin buffer technology (see Figure 2 (f)).

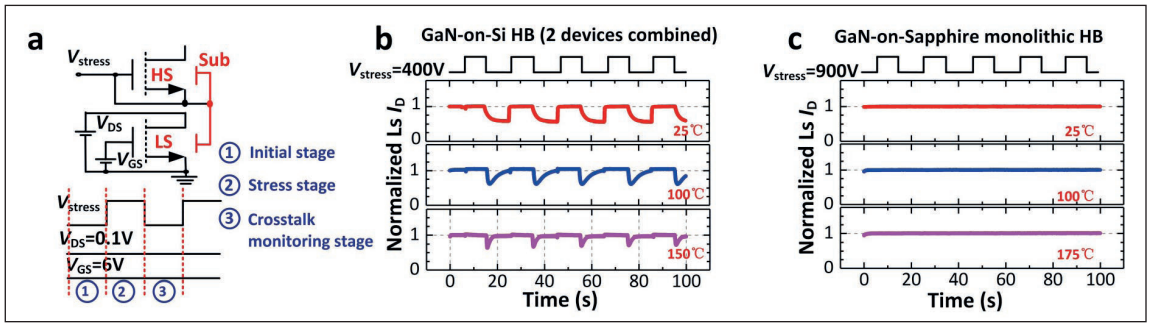
Trench isolation

The monolithic integration of GaN power systems on a single chip has much appeal. There is the promise of suppressed parasitic inductance, reduced die size and greater design flexibility.

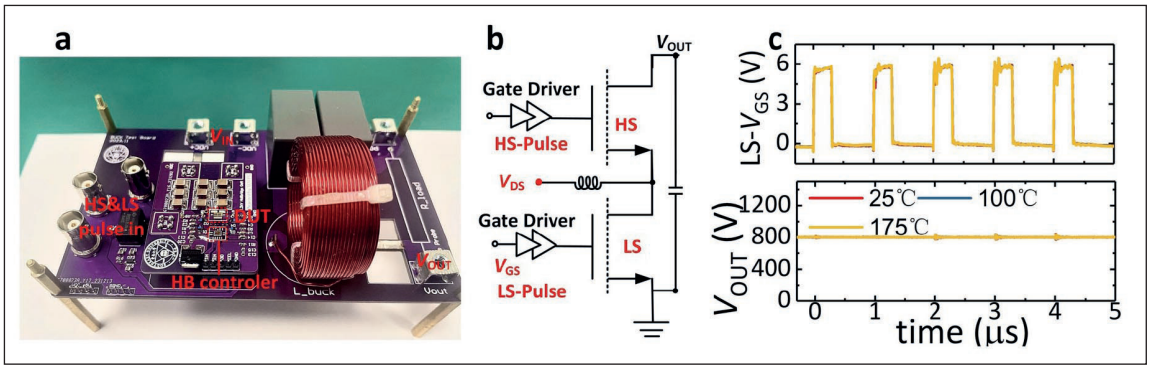
However, it's far from easy to fulfil this dream with GaN-on-silicon, due to the common conductive silicon substrate. There are reports that when the high side (HS) transistor and low side (LS) transistor are built on this conventional platform, the system suffers from back-gating and crosstalk effects, coupled through the common silicon substrate.

A number of substrate technologies have been proposed to address this issue, such as Qromis' engineered platform, as well as silicon-on-insulator substrates and engineered bulk silicon substrates. However, for all these platforms the rated voltage is restricted to no more than 650 V, due to vertical breakdown. With all these platforms, it may be tempting to try and increase the vertical breakdown voltage by introducing a thicker buffer, but this is not practical, due to wafer warpage, traps and high costs.

Offering a far better way forward is our ultra-thin buffer technology, based on insulated sapphire substrates. Crosstalk effects are avoided with



➤ Figure 3. Crosstalk evaluation: (a) test setups, (b) crosstalk of two separated GaN-on-silicon devices with the substrate connected together, (c) no crosstalk observed on GaN-on-sapphire half-bridge devices.



➤ Figure 4. Boost converter performances: (a) experimental printed circuit board, (b) circuit, (c) 800 V/1 MHz output waveforms.

shallow trench isolation, realised by etching the ultra-thin buffer layer (see Figure 1 (b)). With this architecture, the breakdown voltage of the trench isolation structure exceeds 3000 V at 175 °C, while maintaining an acceptable increase in leakage current and thus ensuring safe isolation between HS and LS devices. Another strength of this design is that it provides effective suppression of the substrate biasing effect, due to the insulated substrate withstanding the voltage drop between the electrodes and substrate.

To characterise the crosstalk between the HS and LS devices, we apply a small drain-source voltage to the LS *p*-GaN HEMT, and then apply a pulsed high-voltage stress to the HS devices and substrate (see Figure 3(a)). Due to high-voltage stress, trapping occurs in the LS *p*-GaN HEMT during the stress stage. We are then able to quickly monitor crosstalk after the stress stage.

For the conventional GaN-on-silicon platform, we observe a build-up in the dynamic positive voltage between the HS source and the LS source when the HS in 'on' and the LS is 'off'. Following this, there is a dynamic positive substrate-to-source stress voltage during the transition to HS 'off' and LS 'on' that drives electrons injection into the buffer of the LS *p*-GaN HEMT. When the half-bridge circuit switches so that it is also in this phase – that is, HS 'off' and LS 'on' – electrons trapped in the buffer region of the LS *p*-GaN HEMT cannot be emitted in time, and tend to partially deplete the 2DEG channel of the LS *p*-GaN HEMT, resulting in la ower drain current. That's not the case for our platform, however, thanks to suppression of crosstalk between HS and LS HV *p*-GaN HEMTs, due to shallow trench isolation into the sapphire substrate.

The superiority of our platform is highlighted by our measurements of the drain current of a conventional GaN-on-silicon device and our proposed half-bridge device (see Figure 3(b) and 3(c)). Our results uncover obvious crosstalk in GaN-on-silicon devices at a 400 V stress voltage at room temperature, and demonstrate effective elimination of crosstalk by shallow trench isolation with our GaN-on-sapphire platform, even at a 900 V stress voltage and a temperature of 175 °C. These results indicate that trench isolation enables high-temperature operation of a monolithic GaN half-bridge device at a high voltage – the aim is 1200 V.

Monolithic ICs

To evaluate the performance of our 1200 V monolithic half-bridge circuit, we have constructed a boost converter (see Figure 4(a) and 4(b)). The output results, shown in Figure 4(c), reveal that our converter can operate under 800 V/1 MHz conditions at 175 °C.

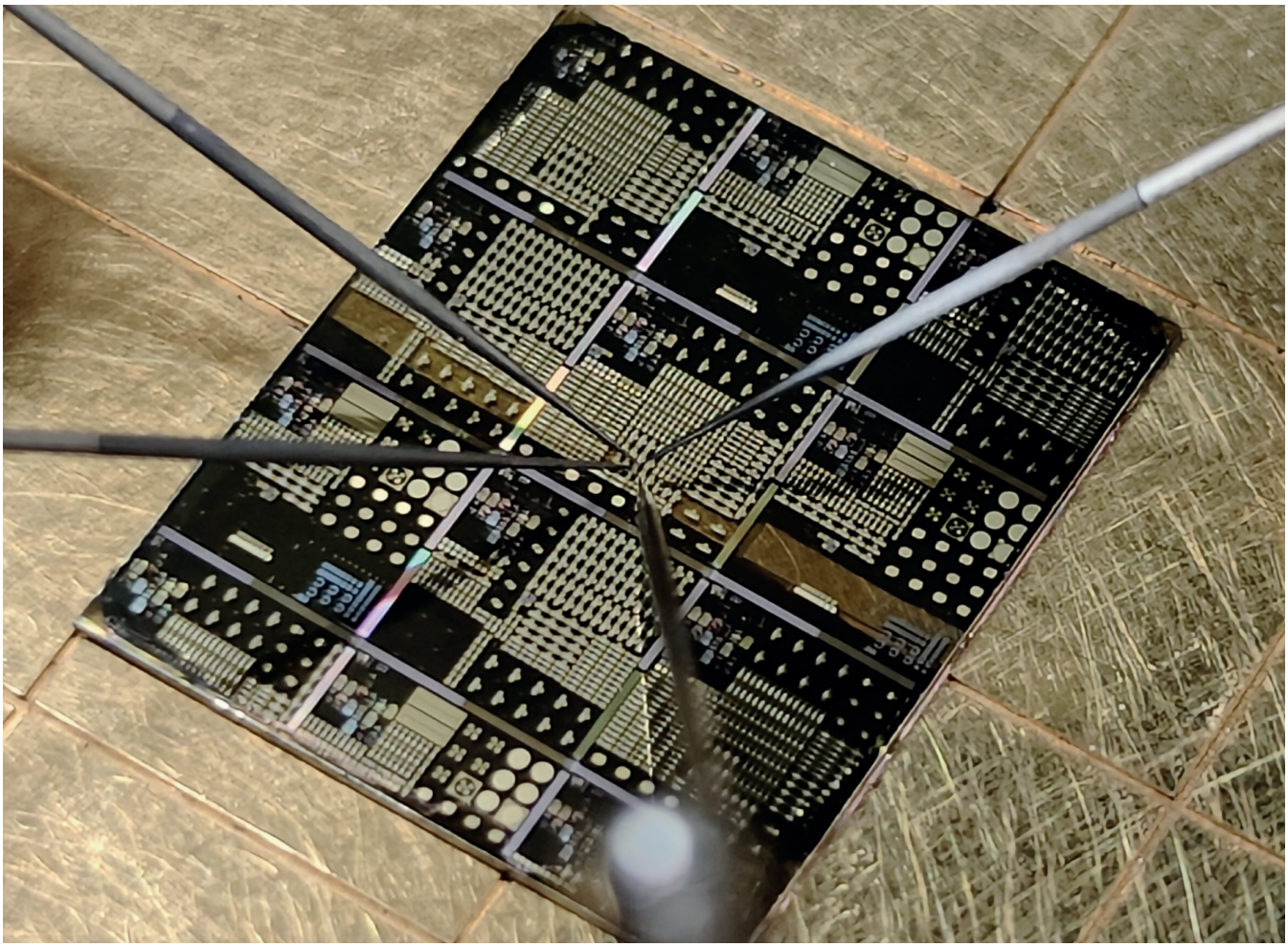
These results indicate that our proposed GaN-on-ultra-thin buffer technology is a compelling candidate for producing GaN devices for high-temperature, high-voltage power systems (see Table 1 for a comparison of our technology and that involving other foundations).

Adding to the appeal of our approach are cheap substrates and simple epitaxy, merits that slash costs and enable GaN HEMTs to target a wider range of applications. They include electric vehicles and renewable energy markets, both of which would benefit from our proposed monolithic half-bridge integration platform that combines high temperatures and high voltages with supressed cross talk.

	Maximum Rated Voltage	Normalized Device BV*	HB Isolation	HB Crosstalk	Device Leakage @25℃	Device Leakage @175℃
This work	1200V	>110V/μm	>3000V	No	<0.1nA/mm@1200V	<100nA/mm@1200V
on QST	650V	94V/μm	~1700V	No	~100nA/mm@650V	unknown
on SOI	200V	100V/μm	~1300V(trench) <1000V(box)	No	~20nA/mm@200V	unknown
on EBUS	200V	51V/μm	~1200V	No	~100nA/mm@200V	unknown
on Si	100V	--	--	--	--	--

*BV is normalized by L_{gd}.

➤ Table 1. Comparison of *p*-GaN HEMT based monolithic integration with high blocking voltages



FETs: A mighty marriage

A monolithic architecture combines the complementary merits of GaN lateral heterojunctions and SiC vertical power devices

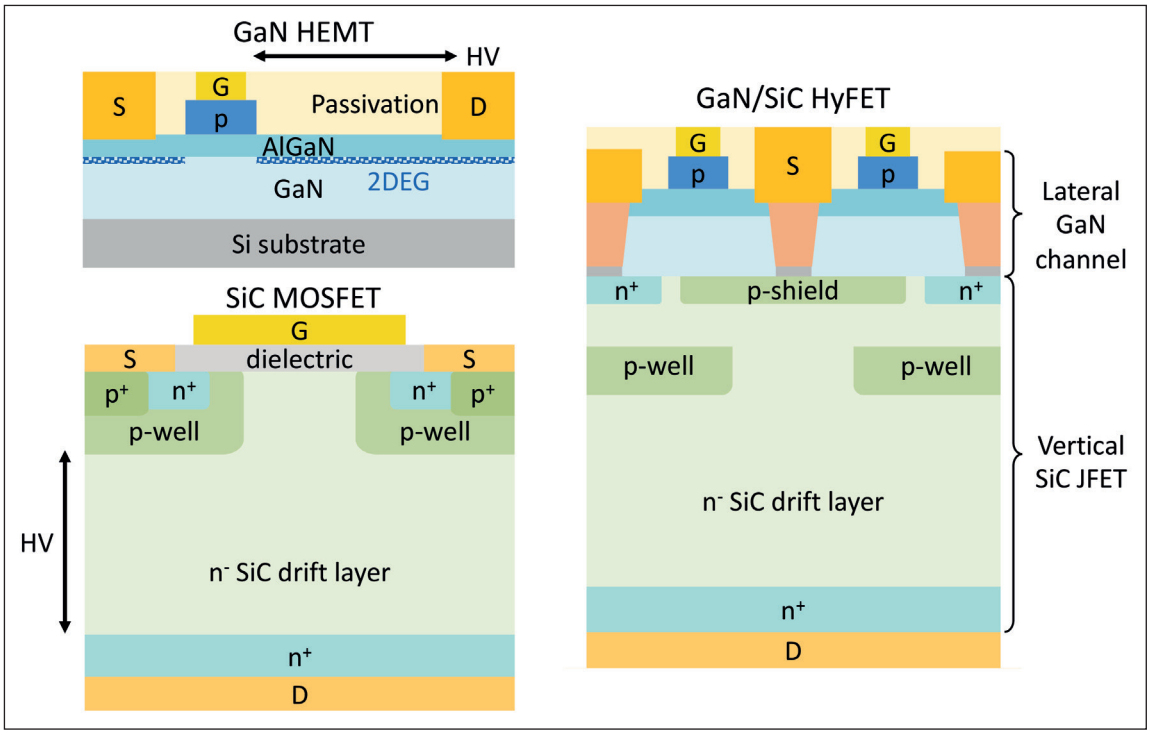
BY SIRUI FENG, ZHEYANG ZHENG AND KEVIN J CHEN FROM THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

THE REVOLUTION in power electronics is well underway. Following decades of research and development, sales of SiC and GaN devices are now soaring, and will continue to climb for many years to come. Their commercialisation is creating a pair of multi-billion-dollar markets: GaN is now extensively deployed in consumer electronics, such as fast and compact chargers for the latest smartphones and laptops; and SiC is grabbing significant market share in photovoltaic inverters, as well as motor drives for electric vehicles.

Further development of GaN and SiC power electronics technologies will inevitably lead to intense competition between these two classes of device. It's a battle that will be fought most fiercely in power range that spans 1 kW to 100 kW, due to the overlap of the power handling capabilities of GaN and SiC. While both are improving, due to efforts to increase the capability of the GaN and the SiC power transistor, is it possible that their marriage could deliver an even greater performance?

Friends or foes?

To answer this crucial question, let's begin by taking a comparative look at the prevailing structures



➤ Figure 1. The device structures of the GaN HEMT, SiC MOSFET, and GaN/SiC HyFET.

of the dominant GaN and SiC power devices, as summarised in Table 1. For this evaluation, it makes sense to consider the most popular GaN and SiC power devices, namely the GaN HEMT and the SiC power MOSFET (see Figure 1).

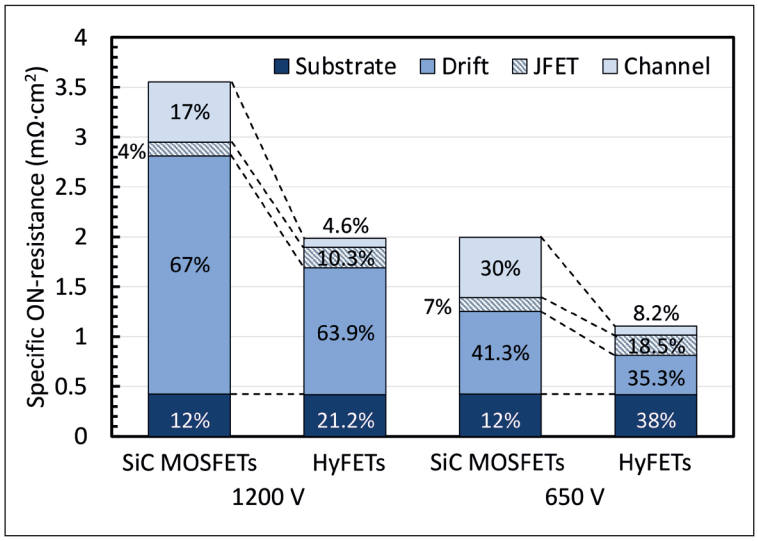
The GaN HEMT is a lateral device with small terminal capacitances. It is renowned for its high mobility, typically 2000 $cm^2 V^{-1} s^{-1}$, associated with the polarisation-induced two-dimensional electron gas (2DEG) at the AlGaN/GaN hetero-interface. The small capacitance and high mobility ensure that this device is very fast. To provide enhancement-mode operation to satisfy the fail-safe requirement, a non-negotiable in power electronics applications, this class of HEMT incorporates a *p*-type GaN gate.

As well as enjoying volume adoption in compact fast chargers, this design is under intensive development for industrial and automotive applications.

In contrast to the GaN HEMT, the SiC MOSFET has a vertical geometry, leading to a relatively large conduction volume. It is possible to manufacture a variety of *p-n* junctions under the MOS channel using mature and robust ion-implantation and epitaxy techniques. These processes produce devices with a high blocking voltage and avalanche capability, traits that have garnered widespread deployment in high-power applications, such as electric vehicles and photovoltaic inverters. However, while the GaN HEMT and the SiC

	Pros	Cons
GaN HEMT	High channel mobility (~2,000 $cm^2 V^{-1} s^{-1}$)) Excellent thermal stability in V_{TH}	Low area efficiency Small conduction volume Dynamic R_{ON} No avalanche
SiC MOSFET	High area efficiency Large conduction volume No dynamic R_{ON} Avalanche capability	Low channel mobility (20~50 $cm^2 V^{-1} s^{-1}$) Poor thermal stability in V_{TH}
GaN/SiC HyFET	High channel mobility (~2,000 $cm^2/(V \cdot s)$) Excellent thermal stability in V_{TH} High area efficiency Large conduction volume No dynamic R_{ON} Avalanche capability	High fabrication complexity

➤ Table 1. Comparison between GaN HEMT, SiC MOSFET and GaN/SiC HyFET.



➤ Figure 2. Projections of the contributions from the major resistances of state-of-the-art SiC MOSFETs and GaN/SiC HyFETs.

MOSFET have had unquestionable market success, this should not obscure their issues. For both devices, the full potential is still to be unleashed.

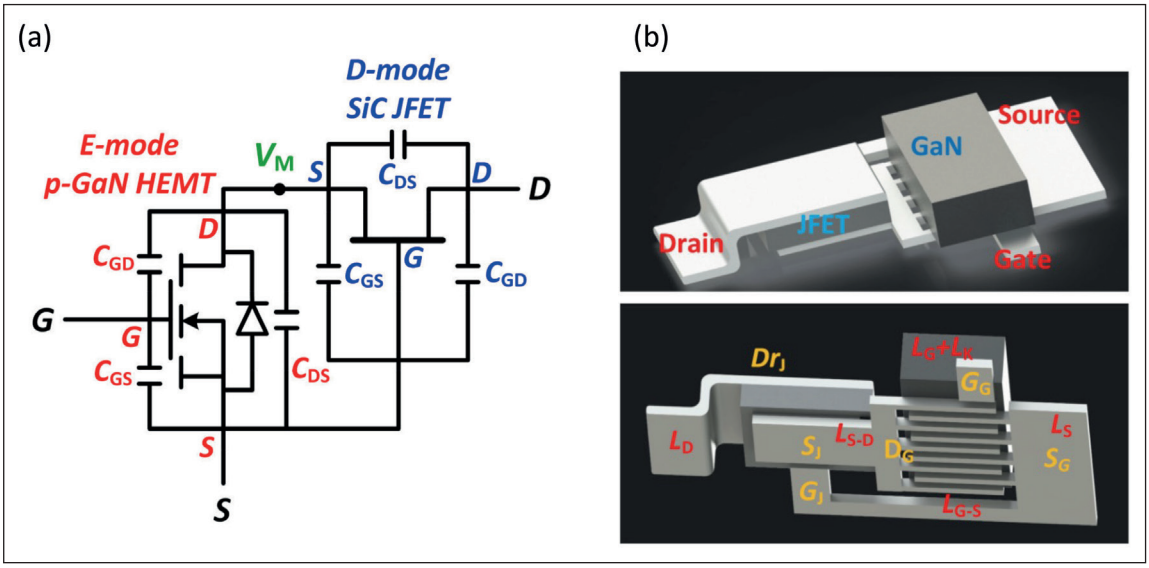
One of the significant weaknesses of the lateral GaN HEMT is that scaling of the voltage rating compromises the bang-per-buck, due to an increased terminal spacing that occupies a larger area. Another issue is that this class of transistor has a small conduction volume, with the 2DEG channel just a few nanometres thick. The small conduction volume impedes the current handling and the thermal dissipation capacity compared with a vertical structure. In addition, there is the notorious 'dynamic on-resistance' issue, induced by the trap-rich surface and buffer, that involves an unwanted increase in the on-resistance with drain bias during the switching process. The other major weakness, arising from the lack of *p-n* junctions in the high-field region, is an absence of avalanche capability, with HEMTs potentially undergoing permanent degradation or failure following risky events, such as unclamped inductive switching and short-circuit events. To prevent this from happening, engineers increase the headroom for the breakdown voltage, adding to the bill of materials.

For SiC MOSFETs, by far their biggest weakness is the low mobility in the MOS channel. Values are typically below 20 $cm^2 V^{-1} s^{-1}$ in planar channels and less than 35 $cm^2 V^{-1} s^{-1}$ in trench channels – in both cases, mobility falls far short of that for electrons in the SiC bulk drift region, where it is typically between 800 $cm^2 V^{-1} s^{-1}$ and 1,000 $cm^2 V^{-1} s^{-1}$. In the channel, mobility is pegged back by the high-density of carbon-cluster traps at the interface of the gate oxide and SiC. The low mobility is responsible for the large channel resistance, which accounts for close to 50 percent of the total on-resistance of a 650 V device, and makes a significant and unwanted contribution to the specific on-resistance of devices – especially those with 650 V and 1200 V ratings.

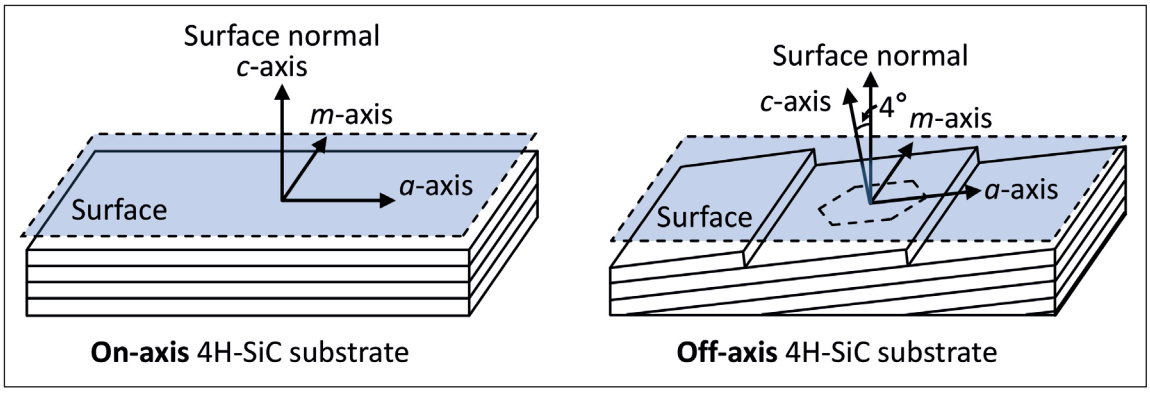
However, rather than dwelling on the negatives, one should view the GaN HEMT and the SiC MOSFET as offering complementary merits. Incorporating them together to create a heterogeneous wide bandgap power device promises to provide a compelling solution that circumvents the issues just outlined.

Initial proposal

Back in 2016, our team at The Hong Kong University of Science and Technology (HKUST) first proposed the concept of the GaN/SiC hybrid FET, based on our numerical simulations. This device consists of a GaN-heterostructure-based 2DEG channel, a SiC JFET structure, a lightly doped SiC drift layer, and through-GaN-vias that connects the GaN channel and the SiC JFET (see Figure 1(c)). This design offers E-mode operation of the 2DEG channel by incorporating a recessed gate or a *p*-GaN gate.



➤ Figure 3. A GaN/SiC cascode device. (a) Circuit diagram. (b) Co-packaged GaN/SiC cascode device with reduced parasitic inductance.



➤ Figure 4. Lattice direction of the 4H-SiC substrates for epitaxy. On-axis substrates are used for GaN heteroepitaxy, while off-axis substrates are used for SiC homoepitaxy.

When this device, which we refer to as a HyFET, is in its on-state, current flows through the *n*-SiC region in the JFET, the through-GaN-vias, and the GaN 2DEG channel. In the off-state, the high electric field from the drain is effectively blocked by the *p-n* junctions in the JFET structure, a state-of-affairs that ensures excellent protection for the high-mobility GaN 2DEG channel. Thanks to the *p-n* junctions in SiC, our HyFET should offer the same avalanche capability as the SiC power MOSFET.

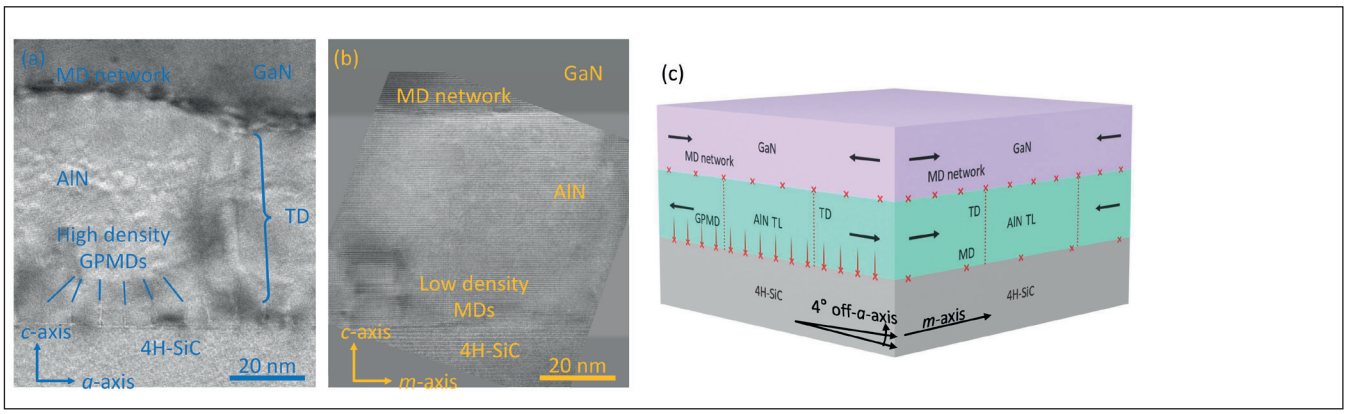
For both SiC MOSFETs and GaN/SiC HyFETs, the total specific on-resistance and its primary components (see Figure 2) has been estimated. The HyFETs offer a substantial reduction in channel resistance compared with SiC MOSFETs, thanks to far high mobility in the channel. Of even greater significance, though, is that due to an absence of the MOS channel, the HyFET is free from a problematic gate oxide, which is behind reliability concerns that have led to overdesigns in the drift region and a derating of the blocking voltage. Based on these considerations, we can reduce the drift region of the HyFET and realise a lower drift resistance.

To provide an initial demonstration of the benefits of a heterogenous wide bandgap power device, we co-packaged a discrete low-voltage GaN HEMT and a discrete high-voltage SiC JFET using a cascode topology (see Figure 3). The challenge with this particular configuration is supressing parasitic inductance, occurring in the relatively long interconnects between discrete devices. This inductance is highly detrimental, leading to serious oscillation and additional loss in the switching process. The solution is to move to a more compact co-packaging scheme that trims parasitic inductance.

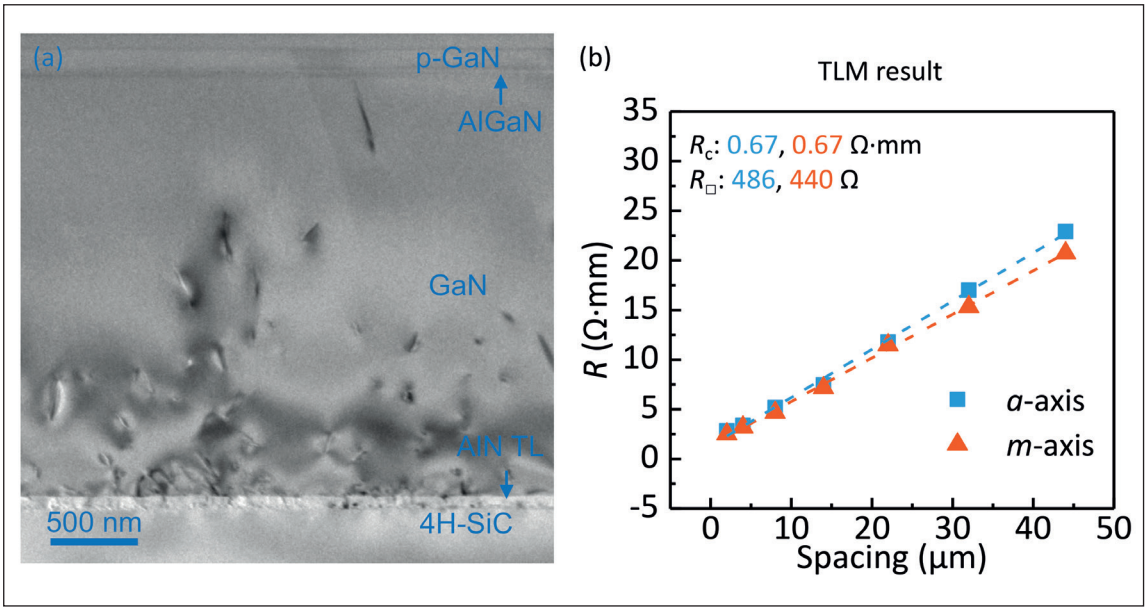
An attractive architecture that fulfils this requirement is the monolithic GaN/SiC HyFET – it has the high-mobility GaN channel and SiC JFET integrated on the sample chip. Such a design delivers incredibly low parasitics and cost competitiveness.

Material challenge

Unfortunately, it's not easy to fabricate monolithic GaN/SiC HyFETs. The biggest challenge is to grow a GaN HEMT structure on a SiC JFET. GaN-on-SiC epitaxy typically uses a 4H-SiC {0001} substrate, with the *c*-axis perpendicular to the wafer surface. However, the mainstream substrate used for the SiC JFET is a 4H-SiC wafer that is mis-cut off-axis, with the *c*-axis at an angle of 4° to the normal (see Figure 4). These mis-cut substrates have the crucial advantage of providing an atomically stepped surface that facilitates a mode of epitaxy that's referred to as step-flow growth.



➤ Figure 5. (a) *m*-plane and (b) *a*-plane view cross-sectional transmission electron microscopy near the AlN transition layer. The geometrical partial misfit dislocations (GPMDs) and misfit dislocations (MDs) at the AlN/SiC and the GaN/AlN interface are observed clearly. The empty parts of the transmission electron microscopy image have been filled with fake colour. (c) Schematics of two-step biaxial strain relaxation in the GaN/AlN transition layer (TL). The arrows show the strain induced by AlN/SiC and GaN/AlN interfaces.



➤ Figure 6. (a) Transmission electron microscopy image of the group III-nitride epilayers on off-axis SiC. Most of the threading dislocations (TDs) are annihilated at the lower part of the epilayer. (b) The transfer length method measurements results of the *a*-axis and *m*-axis GaN 2DEG channel with *p*-GaN removed. The difference in sheet resistance along *a*-axis and *m*-axis is around 10 percent.

However, while these mis-cut substrates are ideal for the single crystalline homoepitaxy of 4H-SiC, they are not well-suited to growth on overlying III-nitride layers, due to a difference in polytype. This difference is to blame for the generation of a high density of geometrical partial misfit dislocations at the III-nitride/SiC interface that tensely strain the epi along the *a*-axis. Strong anisotropic stress in the epilayer results, inducing cracks and defects, and facilitating the formation of step bunches. Concerning consequences follow, including increases in surface roughness and 2DEG sheet resistance, and severe inhomogeneity in 2DEG mobility.

The key to accommodating the anisotropic strain in the III-nitride epilayer is to simultaneously release the strain along the *a*- and *m*-axes during growth. We have devised a two-step biaxial strain release method to accomplish this task. Success comes from inserting an AlN transition layer between the GaN epistructure and the SiC substrate that separately releases the strain along the *m*- and *a*-axes at the GaN/AlN and AlN/SiC interfaces, respectively, by misfit dislocations and geometrical partial misfit dislocations (see Figure 5).

Intriguingly, in this scheme, the density of geometrical partial misfit dislocations is determined by the atomic step density, and ultimately the miscut angle at the 4H-SiC surface, while the density of misfit dislocations is predominantly governed by the lattice constant mismatch between AlN and GaN. With our novel approach, it is crucial to create sufficient misfit dislocations at the GaN/AlN interface to compromise the anisotropic strain caused by the geometrical partial misfit dislocations. However, the step-flow growth mode suppresses the formation of misfit dislocations, since the steps advance together during growth, unlike the island coalescence growth mode, where domain boundaries facilitate the formation of dislocations.

It's important to note that threading dislocations in the AlN layer are crucial for facilitating the creation of the misfit dislocation network when they terminate at the GaN/AlN interface. By adopting an AlN transition layer with an appropriate thickness that enables the threading dislocation density to be well controlled, we have been able to successfully prepare a high-quality GaN epilayer with a relatively low threading dislocation density and an isotropic electric conductivity. These beneficial characteristics are seen in transmission electron microscopy and transfer length method measurements (see Figure 6).

Monolithic HyFETs

Progress by our group, which has involved solving a variety of problems over the 8 years since we proposed the GaN/SiC HyFET, has culminated in the experimental demonstration of this novel device. During this campaign, we have collaborated with Enkris Semiconductor Inc., who prepared group III-nitride epitaxy on off-axis SiC substrates. The

It's important to note that threading dislocations in the AlN layer are crucial for facilitating the creation of the misfit dislocation network when they terminate at the GaN/AlN interface

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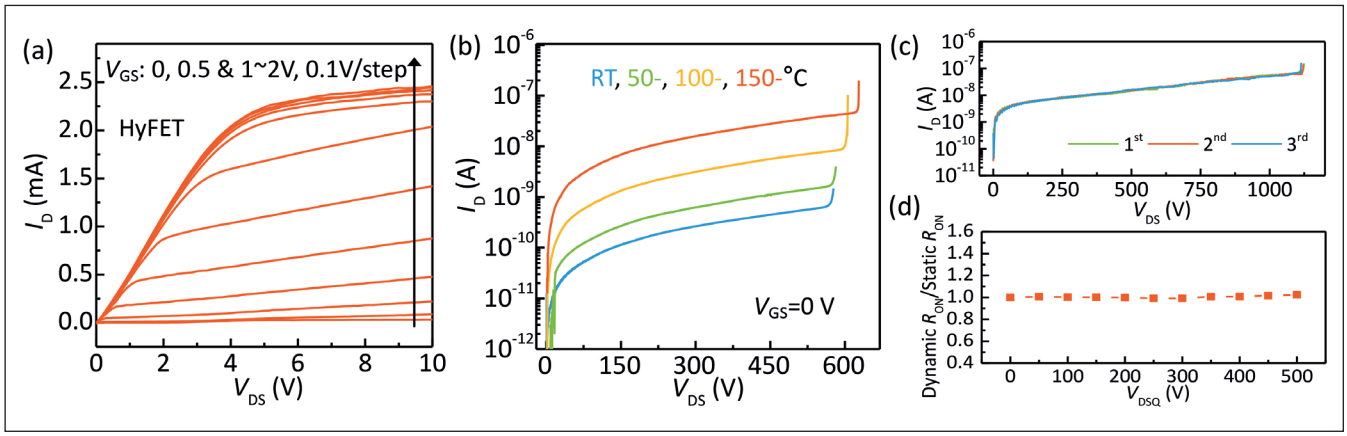

➤ Figure 7. Characteristics of GaN/SiC HyFET. (a) Output current-voltage (I-V). (b) Temperature-dependent off-state breakdown. (c) Off-state breakdown with optimised edge termination. (d) Dynamic R_{ON}. The HyFET exhibits avalanche breakdown capability and has no dynamic R_{ON}.

remaining fabrication processes were developed in the Nanosystem Fabrication Facility and the Materials Characterization and Preparation Facility at HKUST.

In order to establish a low-resistance interconnect between the GaN channel and the SiC JFET, we developed etching techniques to form through-GaN-vias in the GaN epilayer, realised without causing any damage to the SiC JFET.

Another challenge we have addressed is controlling the thermal budget. This is needed, because the GaN surface tends to degrade during SiC metallisation. Our solution has been to develop a GaON surface reinforcement protection layer at the *p*-GaN surface that provides protection during the 900°C sintering process. Following metallisation, we use a Damascene process to create an in-cell interconnect between the SiC JFET and the GaN channel. The remaining processes involve the standard procedure for forming a *p*-GaN gate HEMT.

Our GaN/SiC HyFET is capable of avalanche breakdown, evidenced by the positive temperature coefficient of the breakdown voltage. By optimising the floating-field-limiting-rings edge termination, we have achieved a soft breakdown of 1.1 kV. Another noteworthy attribute of our HyFET is that it is free from the dynamic on-resistance issue, due to distribution of the high voltage across the SiC drift region and shielding of the GaN channel (see Figure 7).

While these results are encouraging, there is still work to do. The specific on-resistance of our HyFET is around 50 mΩ cm^2, a relatively high value. In comparison, specific on-resistances for state-of-the-art SiC MOSFETs with 1.2 kV and 650 V voltage ratings are typically 3 mΩ cm^2 and 2 mΩ cm^2, respectively. We attribute this high specific on-resistance to the conservative design of our JFET, which has a large pitch size to ensure the success of this proof-of-concept in our university facility.

We anticipate a significant reduction in specific on-resistance with industry processing capability, as state-of-the-art SiC JFETs with 1.2 kV and 650 V voltage ratings have values of 1.35 mΩ cm^2 and 0.75 mΩ cm^2, respectively. Thus, we see no additional obstacles to achieving a specific on-resistance below that of the SiC MOSFET, as the channel resistance of the HyFET is far lower.

The successful demonstration of the GaN/SiC HyFET, unveiled late last year at the International Electron Devices Meeting, requires expertise in both GaN and SiC. This capability, once quite rare, is now becoming far more common. It is present in some emerging wide bandgap foundries and major power semiconductor companies.

While there is still much more research and development required to realise the optimum performance in the HyFET, monolithic integration techniques described here are helping to pave the way towards the integration of GaN and SiC at an unprecedented level and will provide the impetus to propel the proliferation of heterogeneous wide bandgap semiconductor devices.

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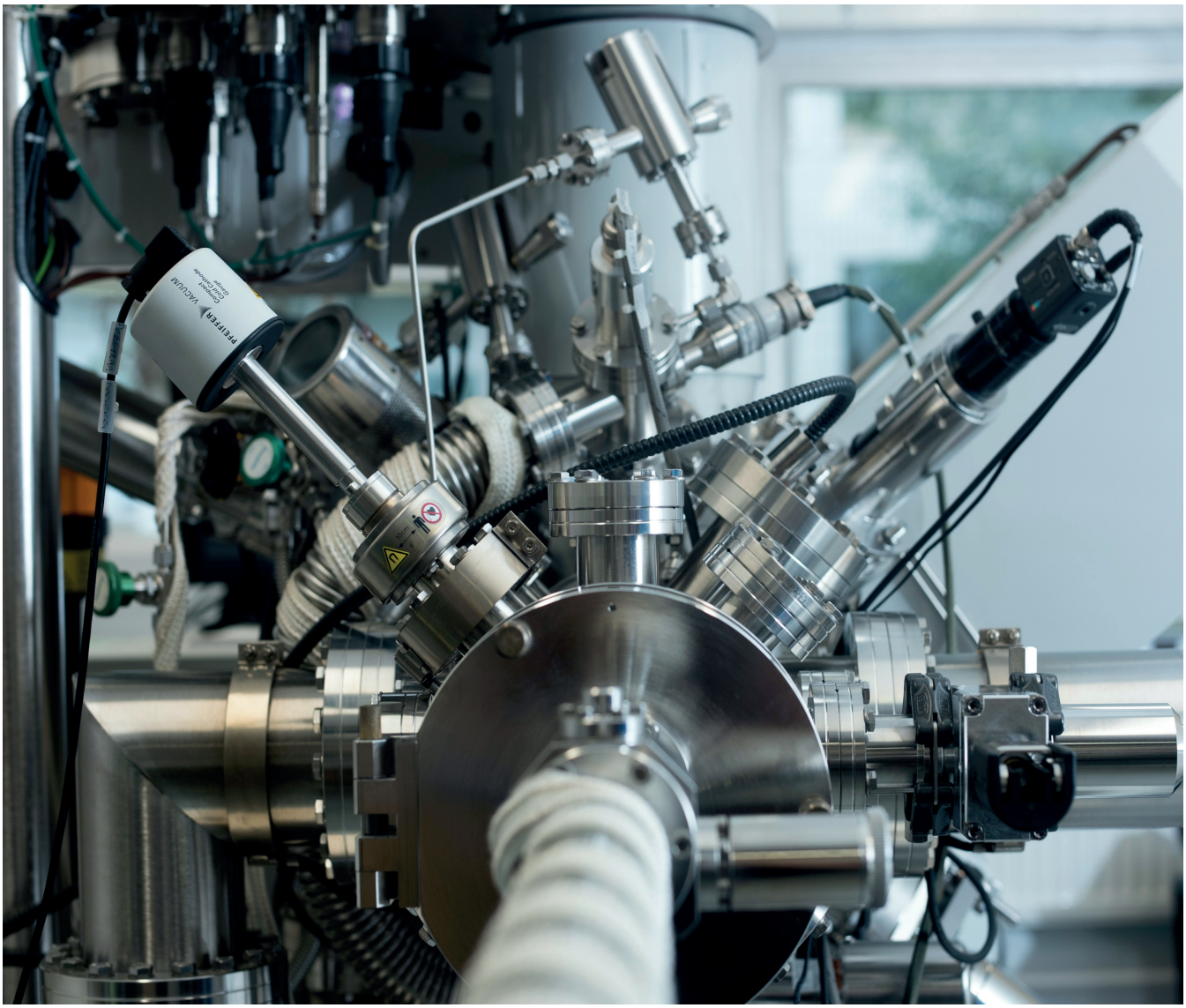


Gate to the future

Reliability benefits from deploying deposited gate oxides in SiC MOSFETs

BY ARNE BENJAMIN RENZ, PETER GAMMON, OLIVER VAVASOUR, VISHAL SHAH AND MARC WALKER FROM THE UNIVERSITY OF WARWICK, SUPPORTED BY JAMES GOTT FROM WARWICK MANUFACTURING GROUP AND ANDREW NEWTON AND MICHAEL POWELL FROM OXFORD INSTRUMENTS PLASMA TECHNOLOGY

THE POTENTIAL of wide bandgap power devices to deliver efficient, compact and light power conversion has been known since the 1980s. However, it was not until the late 2010s that the first SiC power converters from Tesla, BYD, Hyundai and others demonstrated the reliability and viability of the material for mass adoption. In the wide bandgap boom that followed, numerous press releases from OEMs and IDMs announced SiC chip supply agreements and joint ventures. In turn, multiple SiC IDMs have announced major billion-dollar expansion plans and supply agreements from SiC substrate manufacturers. The result is an industry that is predicted by Yole to reach $8.9 billion in 2028 at an average compound annual growth rate of 31 percent.

With a SiC MOSFET based inverter expected to be 5 percent more efficient than a silicon IGBT equivalent, the fact that the SiC chips can be up to three times more expensive is more than compensated for by the potential battery reduction. However, as OEMs become more familiar with the technology, and competition between SiC

IDMs mount, so the pressure for cost reductions increase. This is fuelling the development and adoption of 200 mm diameter substrates, the move to automated fabrication, and a move to reuse substrates.

However, many of the tools of cost reduction sit with the device designer, for whom every milliohm of resistance in their design contributes to the size of the finished die. By minimising the specific resistance of a die, a given product will be smaller, in turn increasing yields. As such each of the yields shown in Figure 1 need to be minimised, including the MOSFET channel, which is the subject of this work.

Challenges in gate structures

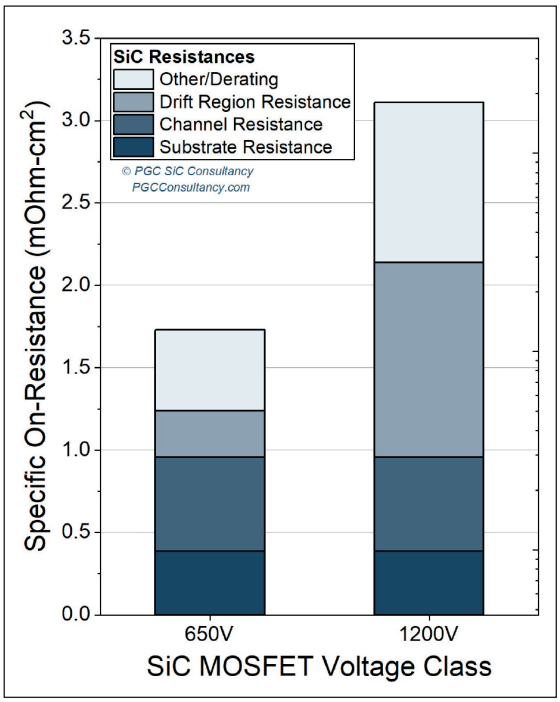
With up to one third of a SiC MOSFET's resistance originating from the channel, shown in Figure 2, this is one of the dominant resistance components in 650 V or 1200 V MOSFETs for EV systems. The main reason for this highly resistive channel is the high density of defect states at the interface between the semiconductor and dielectric. For the SiO_2/SiC interface, the density of interface defect states is typically between a hundred and a thousand times higher than it is for SiO_2/silicon. These unwanted states, and the charges trapped in them, enhance scattering at the interface. In turn, the increased scattering drags down channel mobility and significantly increases the channel resistance. The channel mobility in today's commercial MOSFET applications is just 20-40 $cm^2\ V^{-1}\ s^{-1}$, far lower than the theoretically achievable bulk mobility of SiC, which is around 1000 $cm^2\ V^{-1}\ s^{-1}$.

Ironically, the root cause of the high channel resistance in the SiC MOSFET is related to one of its biggest strengths: unlike GaN and diamond, SiC can be thermally oxidised to form SiO_2. However, the presence of carbon causes problems.

During regular oxidation, occurring at temperatures of more than 1200 °C, SiO_2 initially forms through the consumption of SiC, and carbon is dispersed as CO_2. However, as the SiO_2 get thicker, not all carbon can diffuse through it, causing carbon to accumulate at the SiC/SiO_2 interface (see Figure 3). This trapped carbon creates charge states in the channel region of the SiC MOSFET that scatter electrons and impair the channel mobility of this transistor.

One option for improving channel mobility is post-oxidation annealing in NO or N_2O. Alternatively, the oxide can be grown using NO or N_2O directly. The origin for this improvement is disputed, but a popular and widely accepted explanation is that the nitrogen attaches itself to dangling bonds and other atomic defects, rendering them passive and inactive. Of the two sources of nitrogen, NO gives the highest channel mobility. However, as it is toxic and difficult to handle safely, N_2O is often used instead.

Over the past decade, a number of processing



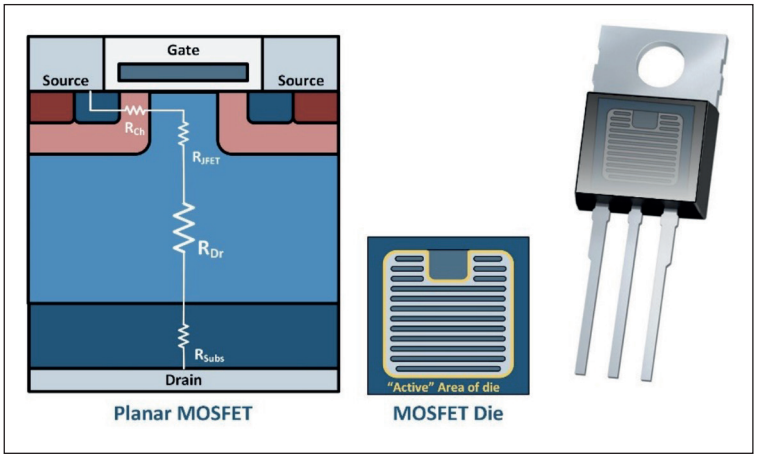
➤ Figure 1. Individual series resistance contributions to total specific on-resistance in 650 V and 1200 V planar MOSFETs.

solutions have been developed to circumvent the inherent disadvantages arising from thermal oxidation. Efforts have focused on deposition-based processes, such as atomic layer deposition (ALD) and low-pressure CVD. With these approaches, the entire oxidation process is based entirely on the chemical reaction between silicon and oxygen precursors, with no consumption of the underlying SiC or residual carbon at the interface.

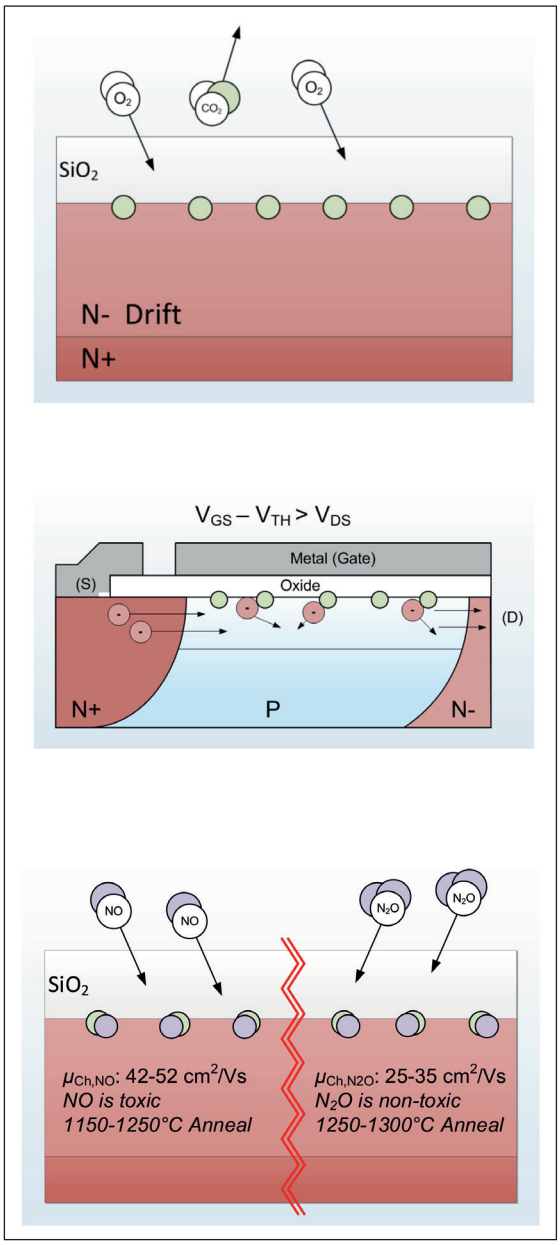
Our team, a partnership between Warwick University, Warwick Manufacturing Group and Oxford Instruments, is developing one such process. Our solution for improved gate oxide reliability focuses on ALD.

Controlling conformal depositions

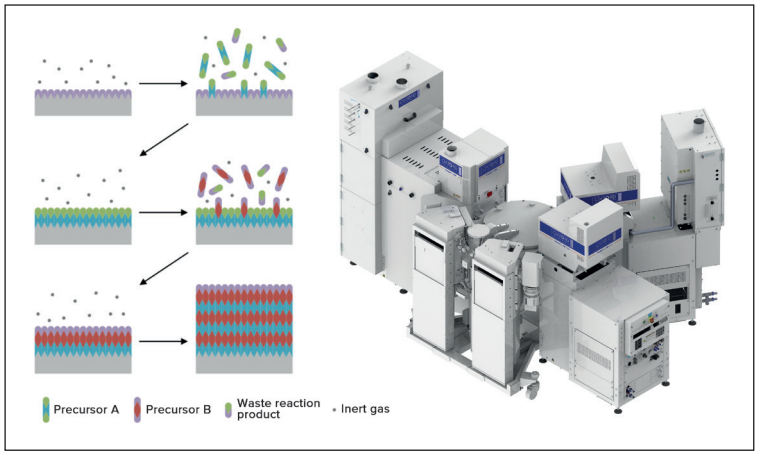
All ALD processes involve the delivery of one precursor into the chamber in a short pulse. This



➤ Figure 2. (left) Cross-sectional image emphasising the individual resistance contributions and (middle and right) an image of a packaged device.



➤ Figure 3. (Top) Interface states build-up due to incomplete carbon transfer away from the interface and (middle) interfacial charge scattering in the channel, causing a decrease in channel mobility; (bottom) common post-oxidation anneals to improve channel mobilities.



➤ Figure 4. (Left) The ALD process shown diagrammatically. Precursors adsorb and react in a layer-by-layer manner to build up films in steps of individual atomic layers; (right) example of a fully automated ALD tool, e.g., Oxford Instrument Plasma Technology's ASP Cobra tool.

precursor is adsorbed onto the samples surface, with molecules remaining on the surface after the pulse is complete. A second precursor is then pulsed into the chamber. This additional precursor reacts with the adsorbed layer, ideally to form a single atomic layer of the desired material. Unlike thermal oxidation, this approach avoids any consumption of the underlying semiconductor material. Cycling of this process stops after reaching the desired oxide thickness.

Unfortunately, as is the case with as-grown thermal layers, the quality of the as-deposited gate dielectrics is not ideal. Weaknesses include high leakage currents, large hysteresis voltages and substantial mobile charges in the oxides. To address these issues, it's the norm to anneal the dielectric in a furnace heated to between 1000 °C and 1200 °C. While an inert gas such as argon is commonly used for the post-process anneal, forming gas adds 5 percent hydrogen for reducing chemistry, in contrast to the oxidising chemistry of NO and N_2O (see Figure 4 for an illustration of the current state of the art).

Our team has spent several years developing SiC MOSFETs with low channel resistances. This can be achieved with a fully automated ALD kit produced by Oxford Instruments.

We have taken a slightly different approach from the one that most commercial entities would have pursued, deciding to shy away from using thermal oxides. We have avoided them because our view is that a deposition-based process is better suited to realising high channel mobilities – it offers greater control, as well as the opportunity to draw on the wealth of experience from very similar silicon passivation techniques that have been used to improve the interface.

Our approach begins with the deposition of a 40-50 nm-thick SiO_2 layer by ALD, followed by annealing for 1 hour in forming gas at 1,100 °C. More details of our process have been reported in the papers listed in the reading list at the end of this article (see (Figure 5 (a)) for a picture of a 200 mm wafer during the RCA 1 & 2 standard clean, and a fully patterned wafer during inspection (see Figure 5 (b)).

Measurements of the electrical characteristics of our devices have produced excellent results. In our lateral MOSFETs, the maximum field-effect mobility is 110 $cm^2\ V^{-1}\ s^{-1}$ (see Figure 7 (a), outperforming any commercially available SiC MOSFET. If industrial producers of SiC MOSFETs adopt our process, they could trim the total specific on-resistance by more than 10 percent, and have the opportunity for a die shrink while maintaining the blocking voltage and current rating.

When introducing any new processing technology, there is a need to assess whether it has any impact on device reliability. To investigate this, we began

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- ☑ Thick metal stack

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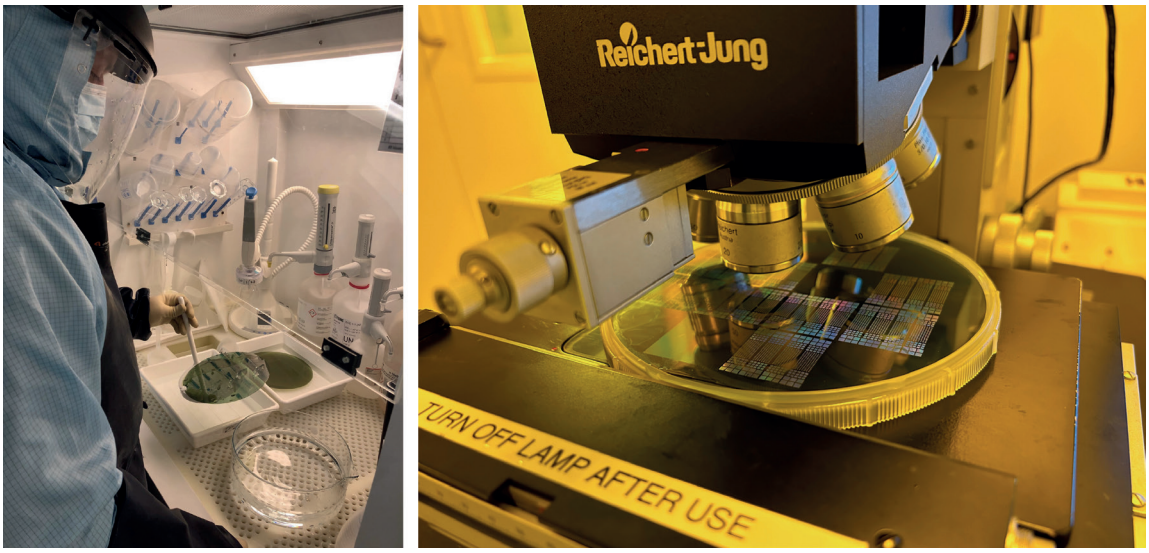


➤ Figure 5. (Left) RCA clean of an 200 mm SiC wafer prior to device fabrication and (Right) Optical microscopy inspection of a fully patterned 150 mm SiC MOSFET wafer, showing multiple test cells.

by stressing our power devices at constant voltages until we detect oxide breakdown (see Figure 6 for the test setup for static characterisation of our SiC devices).

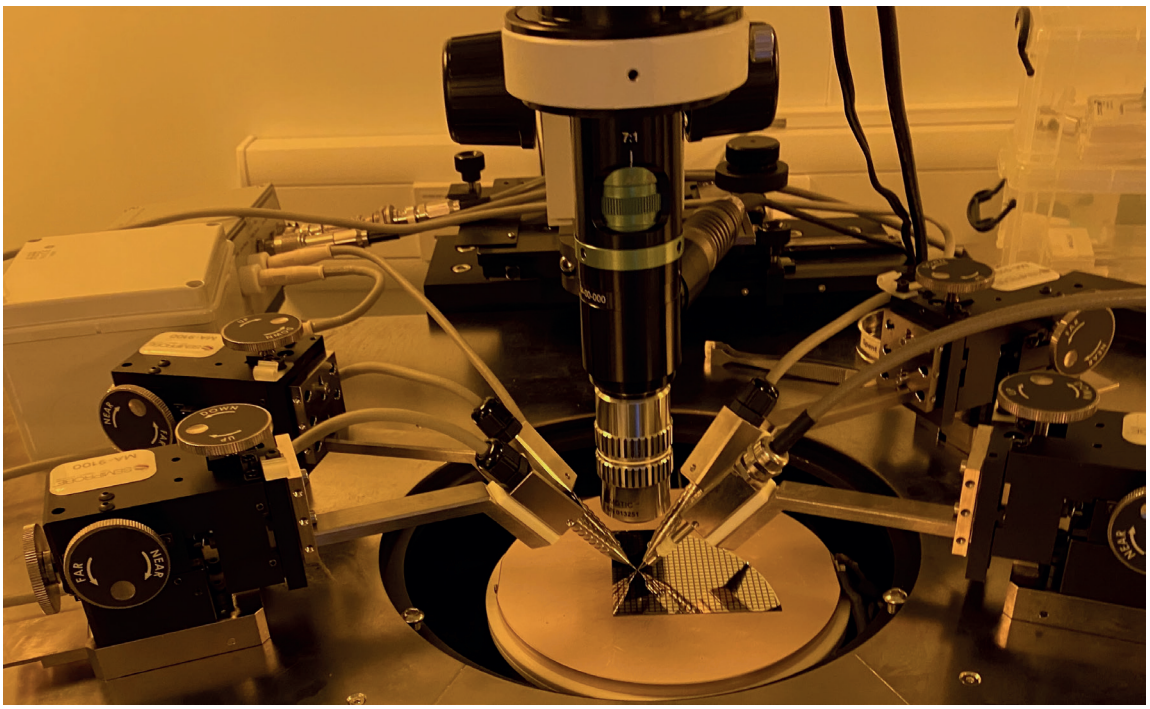
Compared with the more conventional approaches to forming an oxide, such as direct thermal growth or low-pressure CVD, gate oxides produced with our ALD process consistently show the most promising results. Our extracted channel mobilities offer a path to lower-resistance MOSFETs (see Figure 7 (a)), and we realise the best breakdown performance, allowing devices to be stressed at higher voltages before they fail (see Figure 7(b), which shows the current-voltage results of the investigated devices). What's more, our MOSFETs are more robust, evidenced by the longer time that a device can be stressed before it breaks down (see Figure 7 (c)). Extrapolations from stress tests at multiple electric fields demonstrate that our devices can operate at higher voltages while providing the same lifetime as their thermally oxidised counterparts.

To put our efforts into perspective, let's consider the planar 1.2 kV SiC MOSFET. When produced with our process, this device can operate at higher electric fields, provide a reduction in on-resistance by 30 percent, and guarantee a sufficient dielectric lifetime.

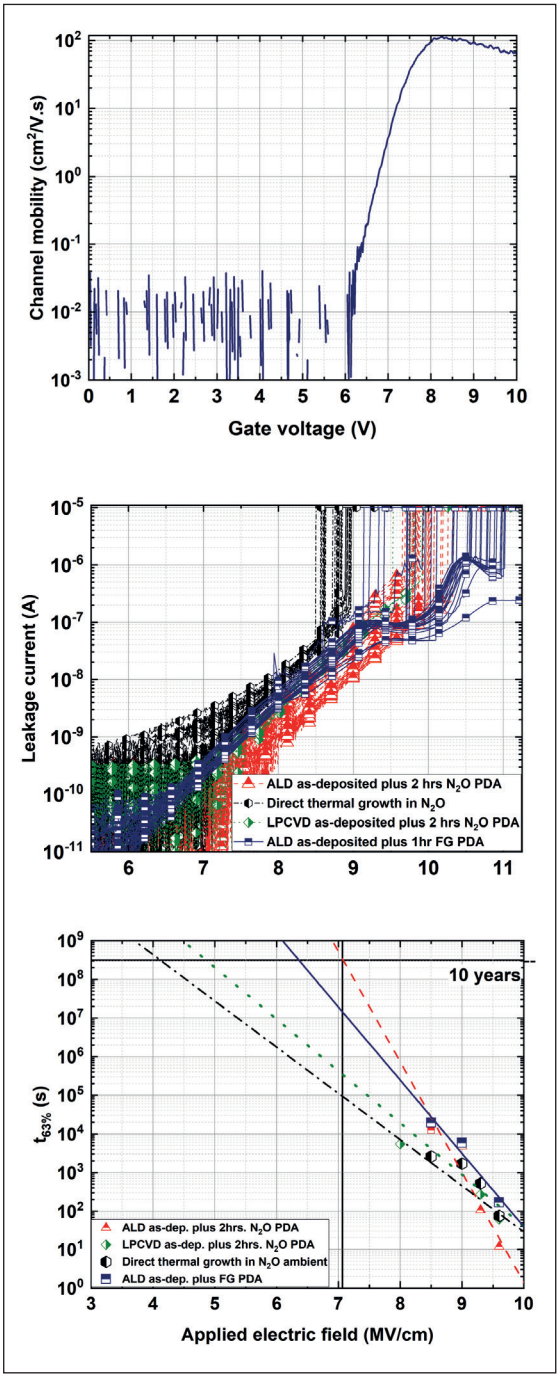
How does it work?

An immense advantage of our collaboration is that we have access to world-leading physical characterisation expertise, as well as a direct pathway to the market.

Over the last ten years there has been the development of the Warwick Photoemission



➤ Figure 6. Quarter of a 150 mm MOSFET wafer on a Semiprobe semi-automatic probe station. Measurements were carried out using a Keysight B1505A parameter analyser. Automated measurements connecting both the stage and analyser were programmed using standard LabView software.



➤ Figure 7. (Top) Extracted channel mobility of a representative lateral MOSFET structure with a channel length of 100 μm. (Middle) I-V measurements of the investigated samples at 175 °C with a device area of 3.14 x 10^{-4} cm^2. (Bottom) Time to breakdown versus applied voltage/electric field of measured devices. It is evident that the presented deposited oxides offer a path towards more reliable SiC products.

Research Technology Platform under the leadership of Marc Walker, a co-author of this feature. This suite of photoemission kit, which can be applied to semiconductor interface analysis, includes X-ray photoelectron spectroscopy specifically tailored towards the analysis of the SiC MOSFET, including the SiO_2/SiC interfaces.

One of the strengths of X-ray photoelectron spectroscopy is that it can be used to analyse the chemical bonding environment at the SiO_2/SiC interface. By comparing thermally oxidised and ALD-deposited oxides with this form of spectroscopy, we can reveal potential approaches to passivate defects.

With our Kratos Axis Ultra delay-line detector and ScientaOmicron multiprobe instruments, we are gaining additional insight into the origins of improvement brought about by the ALD process (see Figure 8 (a)). With this tool we have been able to determine whether an interface is richer in silicon or carbon by looking at the stoichiometric ratio of Si-C in the silicon 2p spectrum and C-Si in the carbon 1s spectrum.

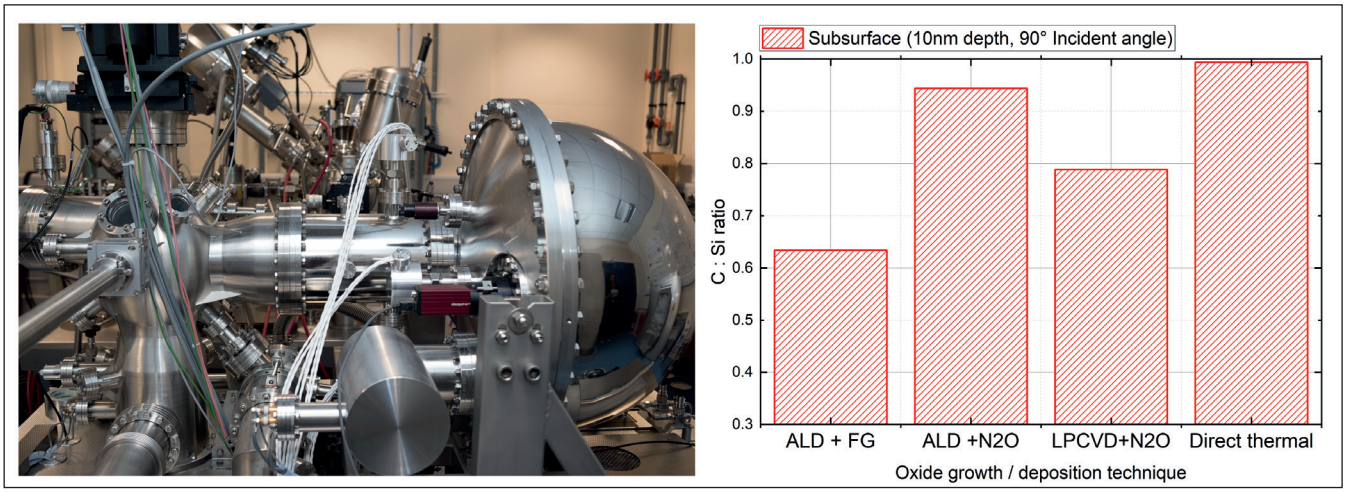
This approach has revealed a C:Si ratio below 1 for all deposited samples, indicating that the interface is silicon-rich. Our samples produced using ALD and a forming gas anneal have the most silicon-rich bonding environment (see Figure 8 (b)). Previous work from our group has established that this arises from the creation of a silicon-rich environment near the interface after ALD deposition of SiO_2, a situation that makes it easier to passivate silicon dangling bonds.

Alongside the revealing X-ray photoelectron spectroscopy analysis, our team has employed transmission electron microscopy to scrutinise the sharpness, cleanliness, chemical composition and, generally, the quality of the oxide/semiconductor interface (see Figure 9 (a) for an image of our scanning transmission electron microscope, the Thermo Scientific Talos F200X).

Using our scanning transmission electron microscope, we have undertaken structural and chemical analysis of our samples with sub-nanometre resolution. Operating at 200 kV, the F200X delivers high-resolution imaging in both transmission electron microscopy and scanning transmission electron microscope modes with a spatial resolution smaller than 0.14 nm. This instrument also provides fast, precise chemical mapping, using the Super-X quad energy dispersive X-ray spectroscopy detectors.

After preparing our samples with a focused-ion beam scanning electron microscope (see Figure 9 (b), we loaded them into the F200X to investigate the interfaces. We were keen to determine the presence of materials, the order of the semiconductor-oxide transition, and to see if

Our research has demonstrated the value and readiness of ALD gate dielectrics on SiC. Channel mobility and reliability analysis shows substantial improvements on the current state of the art.



➤ Figure 8. (Left) The Scienta r4000 ARPES analyser mounted on the ScientaOmicron multiprobe photoemission system. Samples are illuminated with Al Kα X-rays. Any spectra were analysed at take-off angles of 90° and 15°, giving a measurement depth of 10 nm and 3 nm, respectively. Photoelectrons were detected in the SPHERA hemispherical analyser mounted on the same instrument, and on the Kratos Axis Ultra DLD instrument (not shown). (Right) Extracted C:Si ratios of the investigated samples.

there were any obvious surface decorations. We are encouraged by our findings, which reveal that our annealed gate dielectric formed by ALD has excellent interface quality.

Our research has demonstrated the value and readiness of ALD gate dielectrics on SiC. Channel mobility and reliability analysis shows substantial improvements on the current state of the art. Physical characterisation has identified a chemical foundation of the performance gains and excellent physical morphology. The superb controllability of ALD processes offers further scope to improve gate oxide, on-resistance, yield and cost. Our next step is to perform a pilot of the process and verify its reliability in commercial devices, paving the way to large-scale production.

The authors wish to thank Marc Walker, Akif Yildirim, Gerard Colston, Qinze Cao, Kyrylo Melnyk, Xinkai Tian and Richard Jefferies from the University of Warwick, Geoff West from Warwick Manufacturing Group and Grant Baldwin from Oxford Instruments Plasma Technology.

➤ Figure 9. (Left) Thermo Scientific Talos F200X scanning transmission electron microscope. (Right) Sample after thinning back by means of focused-ion beam scanning electron microscope.

Celebrating a century of innovation in power electronics: Schneider Electric

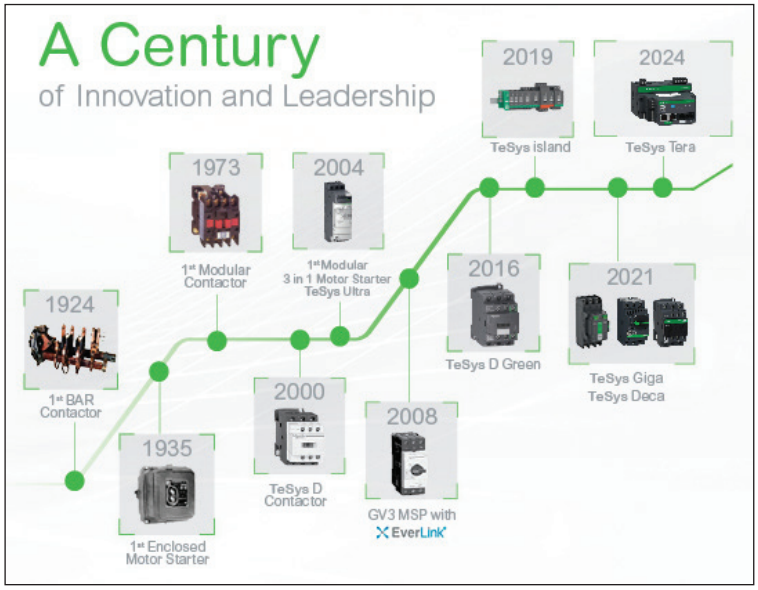
Schneider Electric, the industrial technology leader of energy management and automation, have been at the forefront of innovation for over 100 years. PEW talks to Ionut Farcas, SVP, Europe Hub, Global Power Products at Schneider Electric about how the TeSys motor control solutions, including the upcoming TeSys Tera and TeSys Deca Advance, has been able to meet modern challenges such as sustainability and efficiency.

PEW: *Schneider Electric has a rich history in motor control. How has the company's progress parallelled the evolution of electric motors over the last century?*

IF: It all started during the Industrial Revolution, where motors played a key role in ramping up production across industries like automobile manufacturing, as consumer demand for various devices and gadgets increased. These motors are essential in various industrial applications, whether they're powering belts or operating lifts, all of which require precise control.

To manage these motors, Telemecanique - a French company acquired by Schneider Electric in 1988 - introduced the first BAR contactor back in 1924. This paved the way for the creation of modular contactors, and eventually led to the TeSys solution in 2000. In 2003, Schneider Electric launched the all-in-one motor controller, offering enhanced motor control and protection for motors in industrial environments.

PEW: *With the current focus on climate change and sustainability, how is Schneider Electric adapting its motor control solutions?*



IF: These days, modern CEOs and company owners face a lot of challenges, especially when it comes to keeping plants running efficiently and avoiding costly shutdowns; even brief disruptions can lead to big financial losses. Another big concern is motor health, as unexpected breakdowns can be a big disruption to operations. And of course, with the big push toward decarbonisation, there's a growing need for companies to reduce their $C0_2$ emissions.

This is where our advanced solutions come in, like the upcoming TeSys Deca Advance. These smart modules connect with various communication protocols to give real-time data on electricity consumption and motor health, helping companies with predictive maintenance and preventive actions. Our products, like the TeSys Island, also use AI and digital technologies to predict potential issues before they happen whilst optimising performance. Plus, Eco-design is also a big priority for us; we use recycled materials where we can to cut down on single-use packaging.

PEW: *How does Schneider Electric support plant managers throughout the motor controller lifecycle, from design to maintenance?*

IF: We offer end-to-end solutions that cover everything from design to maintenance, making the process a lot easier for our customers. Our three-tiered approach includes connected products, edge monitoring, and digital software, ensuring efficient management of entire facilities. We work closely with partners like control panel builders and OEMs to deliver integrated solutions, leveraging platforms like Aveva and EcoStruxure Automation Expert for comprehensive plant management.

PEW: *What are the key benefits of the TeSys motor control range?*

IF: The TeSys range excels in control, protection, and digital capabilities. It keeps systems safe from issues like arc flash and motor overburden, ensuring everything runs smoothly and safely. Our solutions also offer precise motor control, enhancing efficiency and overall performance. Customers can

also benefit from valuable data analytics thanks to digital features, which help them optimise operations and make smarter decisions.

PEW: *In terms of other potential benefits, what about reliability, ease of installation and advanced connectivity, for example?*

IF: With over a century of industry experience, our TeSys range has earned a reputation for being reliable and efficient. We focus on providing long-lasting solutions tailored to our customers' needs, so they can enjoy some peace of mind. We also aim to simplify the installation process with design tools, clear guides, and training.

In large industrial applications, which can use thousands of product units, our partners and contractors will install motor control centres to make sure everything runs smoothly. Our role is to enhance efficiency and make everything easier to manage.

Our products support a range of connectivity protocols like RTU, Profibus, and Ethernet. And now with offerings like TeSys Tera, we're bringing advanced native connectivity for seamless integration into industrial automation systems.

PEW: *You've already outlined how the motor controls are intelligent, but as AI and other advanced technologies evolve, how is Schneider Electric enhancing its products?*

IF: Today everyone is talking about the power of AI to make predictions, generate content, or uncover new insights. AI thrives on data, and our products generate huge amounts of it. To put this to good use, we're exploring ways to use this data for predictive analytics, helping our customers anticipate and prevent issues before they happen. This predictive capability will become a gamechanger in avoiding disruptions and boosting efficiency.

PEW: *Could you share an example of how TeSys solutions are being used by your customers?*

IF: A great example is in the hoisting industry, where our TeSys Island solution is used to control cranes. These applications require precise control for things like hoisting and rotation. TeSys Island simplifies these processes by integrating multiple control modules into a single system, making everything from management to maintenance so much more efficient. This solution also supports remote diagnostics and updates, which are key to maintaining uptime and operational efficiency.

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PEW: *How would you characterize Schneider Electric's contribution to power electronics innovation?*

IF: Schneider Electric is leading the charge in Electricity 4.0 and shaping a future that's more digital and electric. We deliver high-quality products and actionable insights that help our customers achieve their sustainability goals. Our commitment to innovation shines through in our latest offerings, like the TeSys Tera and TeSys Deca Advance, which feature advanced communication protocols and eco-friendly designs.

As we celebrate 100 years of innovation, we're excited to keep pushing the boundaries with new technologies that meet our customers' evolving needs.

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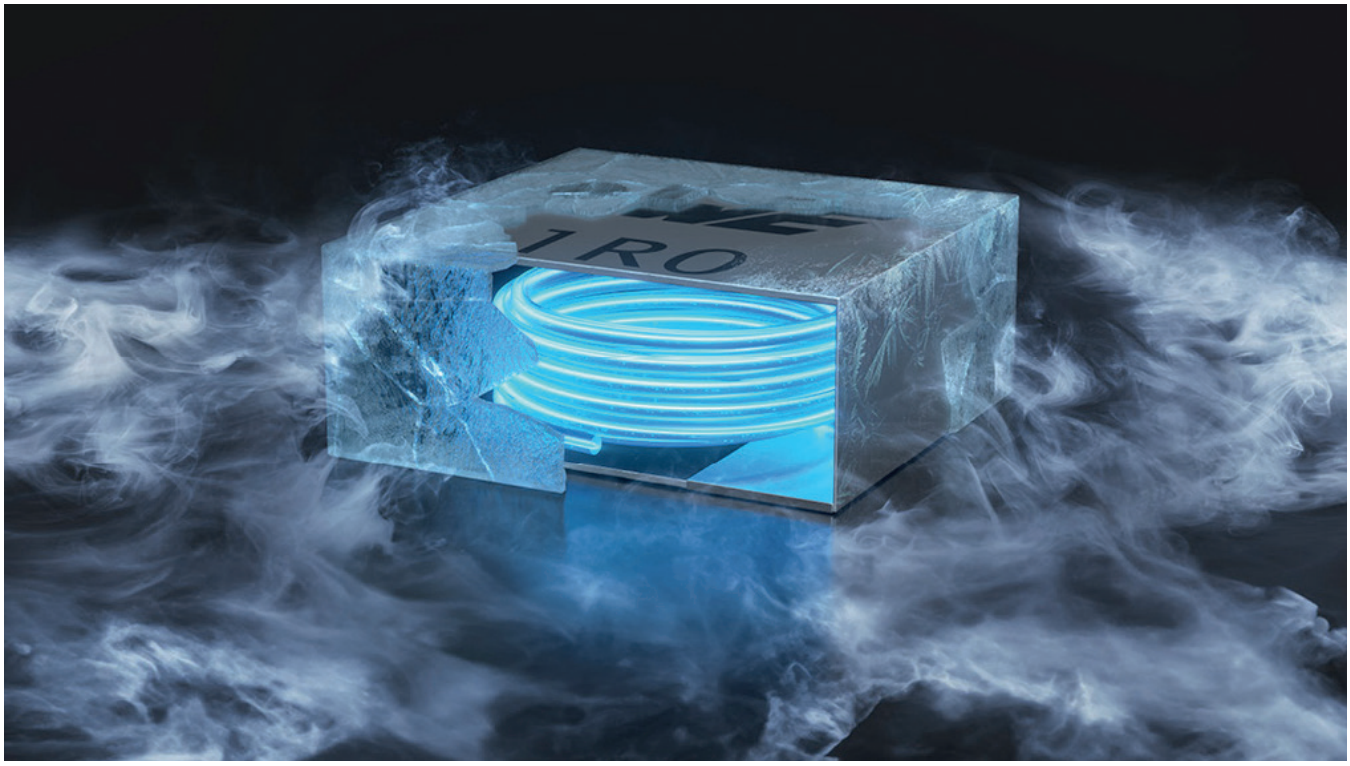

WÜRTH ELEKTRONIK offers its WE-MXGI – a power inductor with unprecedented properties. Extremely low core losses, combined with the lowest winding resistance (RDC value) of all comparable products on the market to date, give rise to maximum efficiency in DC/DC converter applications.

This was achieved by using an innovative core material and optimized winding geometry.

This makes the WE-MXGI magnetically shielded, compact SMT power inductor ideal for high-frequency DC/DC converters that utilize the latest GaN and SiC transistor technologies. The new WE-MXGI power inductor gives developers the opportunity to develop more efficient designs, to convert higher power levels, and to make their designs more compact.

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