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Key criteria for power MOSFETs in harsh linear mode applications

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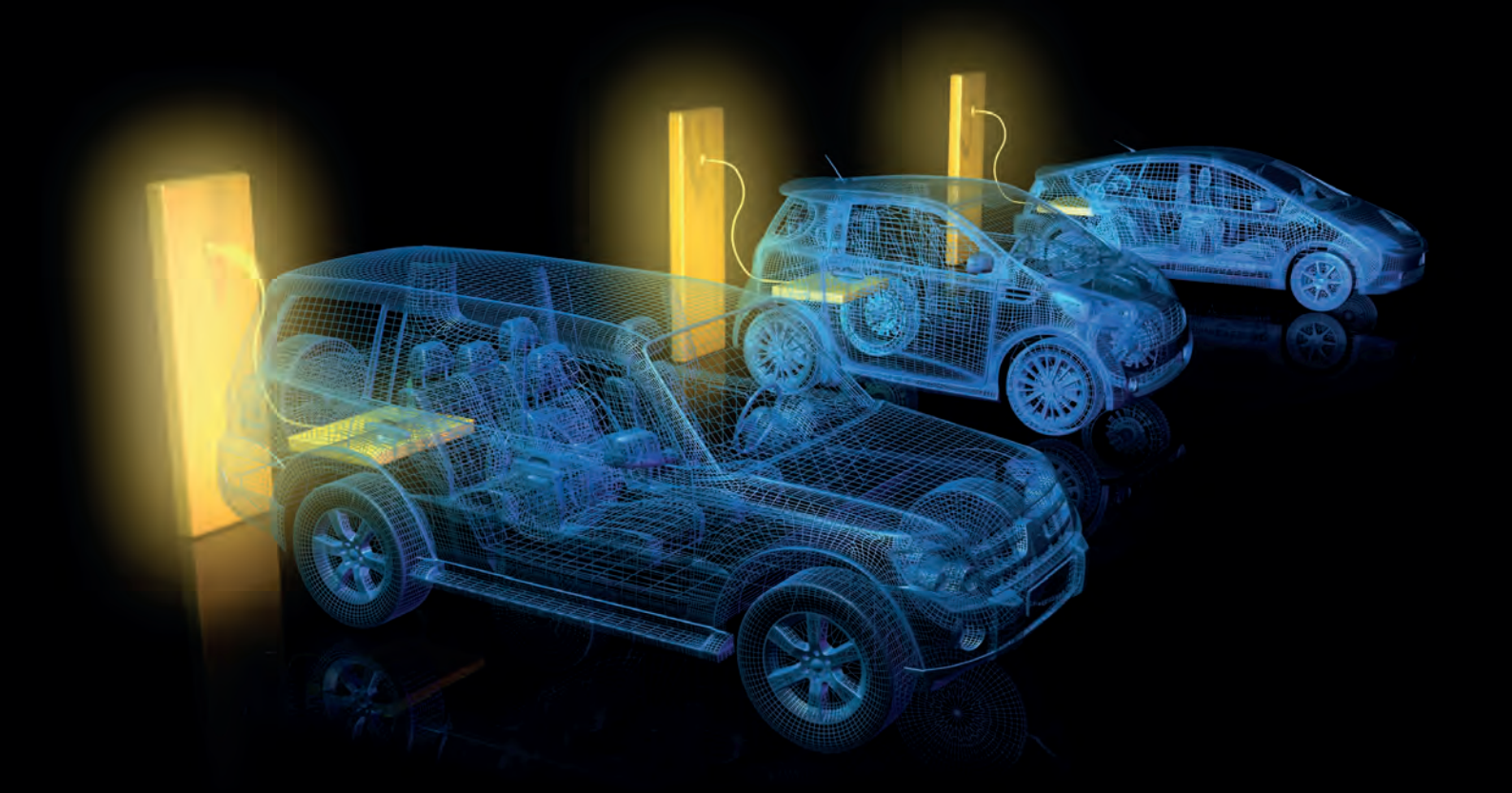

Best performance for next generation SiC power electronics to address global mega trends

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VIEWPOINT

By Mark Andrews Technical Editor

Tech evolution, new discoveries drive the future of Power Electronics

A FASCINATING aspect of semiconductor manufacture is its rapid, sometimes breakneck pace of innovation. Power electronics enjoys an ample share of new and evolving technologies that are rapidly becoming the future of high performance, high power systems.

The bulk of this Power Electronics World edition focuses on the new, the evolving and the unexpected. We'll save the 'unexpected' for last... In an article from STMicroelectronics, we look at high power MOSFET devices that are often considered system workhorses due to their wide versatility and power handling. Achieving linearity and maintaining versatility when current surges, peaks or plummets is challenging. STMicroelectronics explains how its new device family is ideal for linear power in harsh conditions.

Power electronics developers, designers and researchers have sought to bring the wide bandgap benefits of gallium nitride (GaN), silicon carbide (SiC,) and GaN on Silicon into wider applications. A Navitas news analysis explores how GaN is mainstreaming, bringing greater power density, smaller form factors, and greater power handling to more commercial and consumer applications.

We have an interesting GaN article from researchers at Virginia Tech (USA) that have stretched high performance GaN-based devices to 10 kV. Another rapidly evolving power technology – Silicon Carbide – is explored in an article from the Institute for Microelectronics (Swansea University) that focuses on the allure of 'cubic' SiC, the 3C-SiC

polytype, not today's most-manufactured technology: 4C-SiC. While some aspects of 3C-SiC are less robust than 4C-SiC, cubic SiC offers fabrication advantages including more streamlined (read 'simpler') fabrication of the device interface, be it metal or an insulator; 3C-SiC also shines reliably in the field. The authors championing 3C-SiC argue a performance trade-off is preferable if 4C-SiC remains tougher to manufacture while suffering more frequent failures.

Now the unexpected. ClassOne Technology provides a case study that explores what happens when manufacturers of new equipment find their latest and greatest is outperformed by older equipment. What engineers found was startling, including the realization that electroplating technology has not evolved nearly as far as other processing techniques like those supporting Dennard scaling. See how engineers 'broke' with established electroplating practices and techniques to achieve an astounding 4x performance increase.

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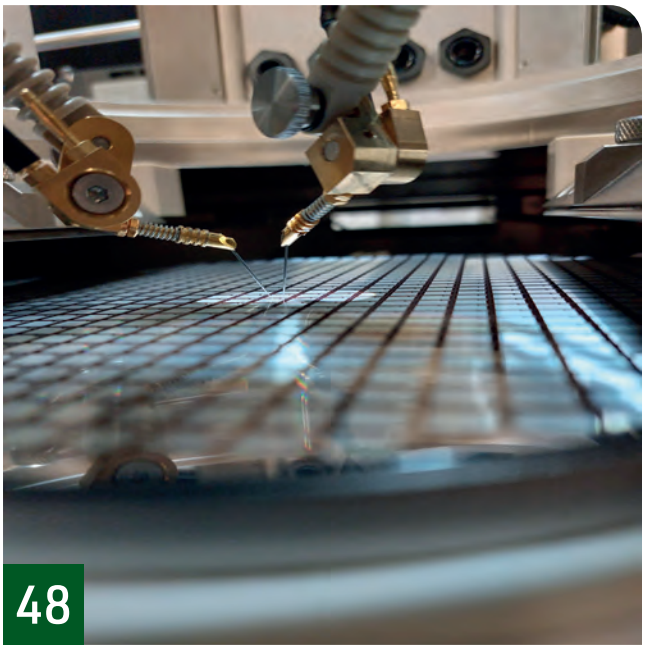

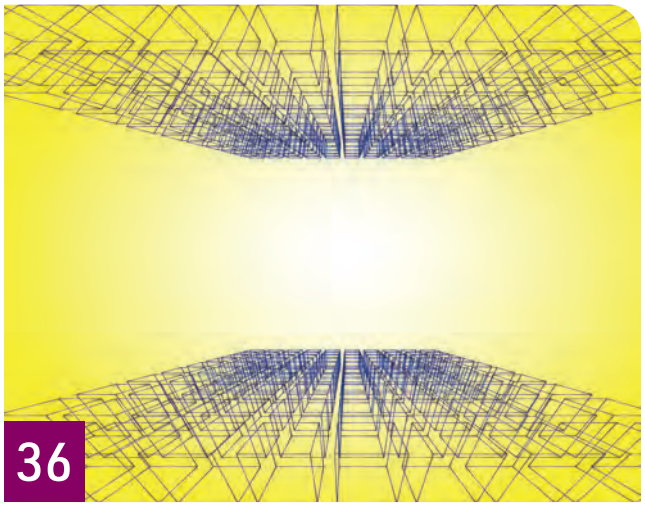

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Tech partnership with BMW Group

EAS Batteries accelerates development of cylindrical battery cells

EAS BATTERIES has supported the BMW Group's "Battery Cell Competence Centre" in the development of its first cylindrical battery cells.

The round cells have a diameter of 46 mm and will be used for the purely electric drive of future BMW models. The BMW Group officially presented the cylindrical cell format in September 2022.

The aim of the partnership between the BMW Group and EAS Batteries was to accelerate the development of the battery cells and thus give BMW a time advantage. "EAS Batteries provided us with excellent support in the early phase of round cell development, for example by supplying prototype cells, and significantly shortened the development time for the BMW cell," says Peter Lamp, head of Battery Cell Technology at the BMW Group.

EAS Batteries provided BMW with both mechanical and electrochemical support, enabling BMW to pull forward decisions on design and cell chemistry of the new cell to an earlier stage and to define the corresponding processes in a timely manner.

BMW will continue to rely on its technology partnership with EAS in the future. Michael Deutmeyer, managing xirector of EAS Batteries GmbH, emphasises the contacting: "By licensing our patented contacting technology, the 'tab-less contacting', we are making a decisive contribution to securing the high-current capability of the new BMW cell design".

EAS Batteries has positioned itself in the automotive market within a very short time. The automotive industry first turned to the highly specialised niche supplier for large format round cells in September 2020, at which time interest in co-developments with the EAS Innovation Factory skyrocketed.

The Nordhausen-based producer of innovative cell and battery solutions now supports a wide range of cell development projects for automotive companies worldwide. "EAS know-how is of great importance to the automotive industry," says Michael Deutmeyer. "The targeted charging currents require cells with high current capability. EAS has already perfected these."

Murata DC-DCs optimised for GaN gate drivers

DC-DCs target EV fast charging infrastructure, battery storage converters, smart grid implementations and renewables

USING PROPRIETARY PCB electrical and mechanical design topologies, Murata has introduced a new series of compact DC-DC converters that are aligned with the increasing prevalence of wide bandgap technology.

The new MGN1 series of 1W output DC-DC converters are designed to deliver the voltages needed by the gate drivers of GaN devices.

These units provide low-profile, small footprint, surface-mount solutions that can be easily integrated into space-limited systems. They also have the advantage of being lightweight, which opens up even greater deployment opportunities. The output voltages offered are +8V, +12V and +6/-3V.

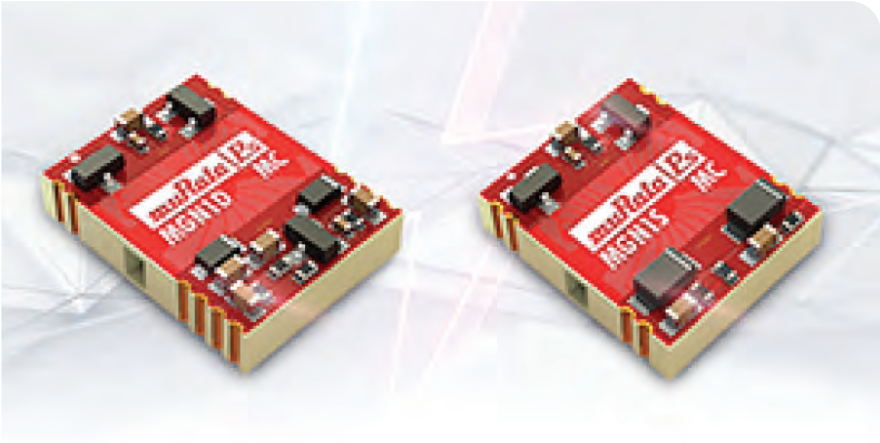
One of the key attributes of MGN1 series DC-DC converters is their ultra-low isolation capacitance of 2.5pF (typical). Through this, the coupling of transients across the isolation barrier is minimised, thereby preventing signal distortion.

In addition, it means that system EMI problems can be mitigated. The >200kV/µs common mode transient immunity (CMTI) of these units makes them well suited to the elevated switching speeds of GaN-based systems, further ensuring gate driver signal integrity. Thanks to their partial discharge performance, reliable operation is maintained in high voltage conditions.

The DC-DC converters in Murata's MGN1 series support a continuous isolation barrier withstand voltage of 1.1kV, with UL62368 conformance pending for 650VDC basic insulation and 240VAC reinforced insulation.

These converters have 6.5mm creepage and clearance figures. A -40°C to +105°C working temperature range allows them to be installed into extremely challenging environments. In addition, reverse polarity and short circuit protection mechanisms are both incorporated.

There are a wide range of GaN-based applications that the new DC-DC converters can be used for. These include EV fast charging infrastructure, battery storage converters, smart grid implementations, solar inverters, solid-state switching breakers, ICT and data centre, wind turbines and motor drives.



Toshiba MOSEFT wins AspenCore Award

TOSHIBA has won the 'Power Semiconductor/Driver of the Year' category in the World Electronics Achievement Awards (WEAA) 2022.

US-based technology media grou AspenCore gave the award for 'Power Semiconductor/Driver of the Year' to Toshiba's XPQR3004PB MOSFET.

The XPQR3004PB is an N-channel, 40V low-voltage MOSFET for automotive applications. It is suitable for battery switches in eco-friendly vehicles and driving assist motors in mild hybrids. It is Toshiba's most advanced UMOS IX die and is clipped to L-TOGL package. AspenCore noted its high current, high heat dissipation capability and high reliability.

Tsutomu Nomura, president of Toshiba Devices & Storage (Shanghai) said: "We are delighted to be recognised by the prestigious WEAA. This is the fifth year in a row one of our products has taken an award. Toshiba is determined to continue to lead the way in providing the automotive industry and other sectors with power electronics that improve the operating efficiency of equipment and advance carbon neutrality."

EasyPACK4B enables single module 352 kW PV string inverter

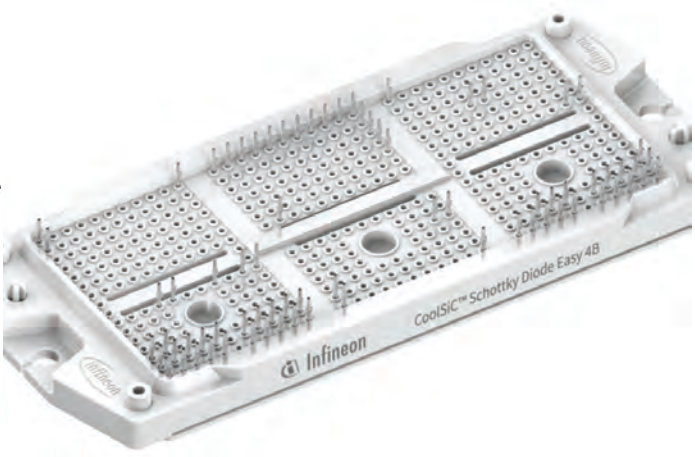
Module enables simple more powerful inverter design with higher power density and reduced system costs

INFINEON TECHNOLOGIES has recently added EasyPACK 4B to its Easy power module family. Targeting applications in photovoltaic string inverters, the module can achieve up to 352 kW.

According to Infineon, it allows a significant increase in output power of about 40 percent compared to last generation PV inverter of 250 kW using EasyPACK 3B. The module aims to enable a simpler but more powerful inverter design with higher power density and reduced system costs. The device is ideal for 1500 V DC solar string inverters.

With the introduction of the F3L600R10W4S7F_C22 lead-type, EasyPACK 4B is now the largest package in the Easy family with three DCB substrates.

Nevertheless, it still features a no-baseplate design, 12 mm height, PressFit pins and flexible pinout, and more. Like the other Easy packages, it offers flexibility in platform-based solutions. The package extends the EasyPACK 3B hold-down concept to ensure low thermal resistance (R th) and to increase robustness and quality.



Just like the existing Easy family members, the new EasyPACK 4B has optimised stray inductance for reduced design efforts.

The lead-type power module F3L600R10W4S7F_C22 features an advanced three-level NPC (ANPC) topology that combines the latest generation of 1200 V CoolSiC Schottky diode with the latest 950 V TRENCHSTOP IGBT7 chip technology for up to 600 A. ANPC is a popular topology in solar string inverters and ensures high efficiency as well as low power losses. This combination of topology and chip optimises the usefulness of the power semiconductor.

The EasyPACK 4B F3L600R10W4S7F_C22 can be ordered now. The new Easy 4B package will be available for additional typologies, current ratings and voltage classes.

Hunan Sanan secures $524M SiC order from NEV brand

HUNAN SANAN, a subsidiary of Sanan Optoelectronics, will supply SiC chips to a prominent automaker's new electric vehicle product line in the next few years.

Tony Chiang, general manager of Hunan Sanan, said: "Our agreement with this strategic partner further demonstrates the automotive industry's commitment to providing innovative electrification experience to the market and leveraging the advantages of wide bandgap semiconductors to improve overall vehicle performance. The agreement ensures a long-term supply of SiC to our customer to help them realise their promise of low-carbon, smart mobility. "

The SiC chips in the agreement will be manufactured in the Hunan Sanan's mega fab in Changsha, said to be the first vertically integrated SiC wafer manufacturing service platform in China, providing in-house supply chain from SiC crystal, substrate, epitaxy, chip manufacturing, packaging and testing, with a committed annual production capacity of 500,000 SiC 6-inch wafers. Hunan Sanan has recently obtained IATF 16949 system certification while the automotive-grade SiC MOSFETs have been verified with the cooperation of strategic partners, and are expected to be released in production in 2024.

Sike Semiconductor, a company jointly established by Hunan Sanan and Li Auto, also officially started construction this past August and is expected to start production in 2024 with a planned annual production capacity of 2.4 million half-bridge SiC power modules. Hunan Sanan's SiC technology will provide energy for the NEV power system for medium and high voltage platforms.

Rohm, Mazda, and Imasen sign SiC e-Axle deal

Through the collaboration, Rohm will develop further SiC MOSFETs and modules by working backwards from the finished vehicle

ROHM has signed a joint development agreement with Mazda Motor Corporation and Imasen Electric Industrial for inverters and SiC power modules to be used in the electric drive units of electric vehicles, including e-Axle.

As the 'heart of the EV', e-Axle integrates a motor, reduction gearbox, and inverter into a single unit that plays a large part in determining the driving performance and power conversion efficiency of electric vehicles. SiC MOSFETs in particular are expected to improve efficiency even further.

Rohm will carry out joint inverter development for e-Axle by participating in a 'cooperative framework for the electric drive units development and production' with companies such as Imasen and led by Mazda. At the same time, Rohm will contribute to the creation industry-leading compact, high efficiency electrical units by developing and supplying advanced SiC power modules that provide improved performance.

Through this collaboration, Rohm will develop even more competitive SiC MOSFETs and modules by working backwards from the finished vehicle to understand the performance and optimal drive method required of power semiconductors.

Besides creating new value through mutual understanding between car and device manufacturers, the three companies also support technical innovation in the automotive field and contribute to a sustainable society by leveraging extensive knowledge, technologies, and products garnered on a global basis.

Ichiro Hirose, director and senior managing executive officer; Oversight of R&D, Cost Innovation and Innovation, Mazda Motor Corporation said: "We are pleased to collaborate on the development and production of e-Axle with Rohm, who hopes to create a sustainable mobility society through outstanding semiconductor technologies and advanced system solution development capabilities, to co-create a new value chain that directly links semiconductor devices and vehicles in both directions as electrification brings us closer to carbon neutrality. By partnering with like-minded companies, Mazda is committed to injecting 'driving pleasure' into every product - including electric vehicles."

Katsumi Azuma, director and senior managing executive officer and COO, Rohm: "We are extremely pleased to work together on the development and production of e-Axle with Mazda, who is committed to providing 'driving pleasure' that expresses the inherent appeal of cars. Through this partnership, we hope that by reflecting the true demands and requests in our products we can develop automotive systems that contribute to decarbonization while allowing us to gain a deeper understanding of Mazda's goal of creating cars that are sustainable with the earth and society. As the role of semiconductors in the automotive market continues to grow, Rohm will strive to manufacture high quality products and contribute to the creation of a sustainable mobility society by offering a wide range of solutions."

We are extremely pleased to work together on the development and production of e-Axle with Mazda, who is committed to providing 'driving pleasure' that expresses the inherent appeal of cars

Pulsiv raises £1.5m in latest funding round

Pulsiv Limited, a UK-based cleantech company announces that it has raised £1.5m through an equity funding round supported by existing shareholders, including management and Frontier IP Group plc (a founder of the business), and new angel investors. The round remains open.

PULSIV'S unique technology aims to conserve every watt of power that needs converting when consumer devices are run from a mains supply, when batteries are being charged, when LED lights are illuminated or when electricity is generated from solar panels. Products under the Pulsiv OSMIUM brand are designed for always-efficient power supplies. Pulsiv HORIZON technology has been developed for advanced solar micro-inverters and power optimizers. The company sells a range of system controllers that intelligently manage power conversion. Our proven reference designs will enable seamless integration by OEMs and accelerate industry adoption.

The Pulsiv OSMIUM architecture can be used in a broad range of OEM products that demand high efficiency, compact design and a low-cost bill of materials. Pulsiv OSMIUM technology exceeds the highest Energy Star standards, eliminates inrush current, reduces overall component cost/count and delivers consistent performance from no-load through to full power. Our scalable solution promotes a platform approach and economies of scale – most components remain unchanged across different designs.

Pulsiv HORIZON employs patented methods for extracting more energy from solar panels than alternative solutions, and our innovative prototype uses a unique split architecture to maximize the power generated by solar micro-inverters and power optimizers under all operating conditions.

Standard reference designs will create greater competition, ensuring that future solar installations will generate maximum returns and accelerate the transition towards renewable energy. The investment raised during this round supports the commercialization of Pulsiv OSMIUM and the ongoing development of Pulsiv HORIZON:

- Pulsiv OSMIUM development systems are currently being manufactured to support customer evaluations and product integration.
- Pulsiv OSMIUM reference designs will simplify the customer journey and drive mass-market adoption.
- Pulsiv HORIZON reference designs will demonstrate our new architecture for power optimiser and microinverters with best-on-class CEC/EU efficiency and power delivery.

Pulsiv's original concept for more efficient power conversion between AC and DC was developed by Zaki Ahmed and spun-out of the University of Plymouth.

It is protected through multiple patent families and trademarks. A global energy transition is underway to phase out fossil fuels and reduce greenhouse gas emissions. IRENA (International Renewal Energy Agency) reports that 90% of the required carbon reductions can be achieved by switching to renewable energy sources and implementing a range of efficiency measures. Rising energy prices, concerns about energy security and inflationary pressures are also driving the need for Pulsiv technology.

Pulsiv CEO Darrel Kingham commented: "We are delighted to have secured this funding given the challenging fundraising environment and full credit goes to my leadership team and our strategic partners. This shows confidence in our progress over the last 18 months, with Pulsiv OSMIUM far exceeding the original design goals and the Pulsiv HORIZON prototype producing best-in-class results. The many benefits of our technology will challenge conventional thinking and give customers an opportunity to differentiate their products in a number of markets."

Nexperia launches new hotswap ASFETs

Optimised RDS(on) and SOA manage in-rush currents in 12 V hotswap and soft start applications

NEXPERIA has extended its range of Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start with the introduction of ten new 25 V and 30 V fully optimised devices.

According to the company, these combine enhanced safe operating area (SOA) performance with low RDS(on), making them suitable for use in 12 V hotswap applications including data centre servers and communications equipment.

The PSMNR67-30YLE ASFET delivers 2.2x stronger SOA (12 V @100 mS) than previous technologies while having an RDS(on) (max) as low as 0.7 mΩ.

The Spirito effect (represented by the steeper downward slope found on SOA curves at higher voltages) has been eliminated, while exceptional performance is maintained across the full voltage and temperature range (compared to unoptimised devices).

Nexperia further supports designers by removing the need to thermally de-rate designs, by fully characterising these new devices at 125 °C and providing hot SOA datasheet curves. With eight new devices (three 25 V and five 30 V) available in a choice of LFPAK56 & LFPAK56E packages with RDS(on) ranging from 0.7 mΩ to 2 mΩ, the majority of hotswap and soft

start applications are addressed. Two additional 25 V products (which will have an even lower RDS(on) of 0.5 mΩ) are planned for release over the coming months.

BorgWarner to invest $500M in Wolfspeed

Agreement ensures BorgWarner has a reliable supply of SiC devices for its inverter growth plans

SiC specialist Wolfspeed and e-mobility firm BorgWarner have announced a strategic partnership that calls for BorgWarner to invest $500 million in Wolfspeed's financing transaction in exchange for SiC device capacity.

Under the multi-year agreement between BorgWarner and Wolfspeed, BorgWarner will be entitled to purchase up to $650 million of devices annually as BorgWarner requirements increase.

"SiC-based power electronics play an increasingly important role for our customers as our electric vehicle business continues to accelerate," said Frédéric Lissalde, president and CEO of BorgWarner.

"We believe this agreement helps ensure that BorgWarner will have a reliable supply of high-quality SiC devices, which are significant to the company's inverter growth plans."

BorgWarner's Charging Forward strategy targets $4.5 billion of electric vehicle revenue for 2025, compared to less than $350 million in 2021. Based on new business awards and acquisitions announced as of the Company's third quarter earnings release, BorgWarner believes it is already on track to achieve approximately $4 billion of electric vehicle revenue by 2025.

"Today's announcement demonstrates the creative solutions two collaborative and strategic partners are pursuing to better support the growing demand for SiC devices. BorgWarner has been a strong partner with Wolfspeed for many years, and we are pleased to secure the investment from them which will be used to support our capacity expansion efforts and ensure we have a steady supply of product for their customers," said Gregg Lowe, president and CEO for Wolfspeed.

"This agreement, combined with our most recent announcement of a multi-billion-dollar materials expansion in North Carolina, confirms the industry

transition from silicon to SiC is well underway."

Last month at the company's Investor Day, Wolfspeed outlined a multi-year, $6.5 billion capacity expansion effort which included the installation of additional tools at the company's state-of-the-art, 200mm Mohawk Valley fab and the construction of a 445-acre SiC materials facility in North Carolina, which will expand the company's existing materials capacity by more than 10x. The first phase of construction is slated to be complete by the end of FY2024.

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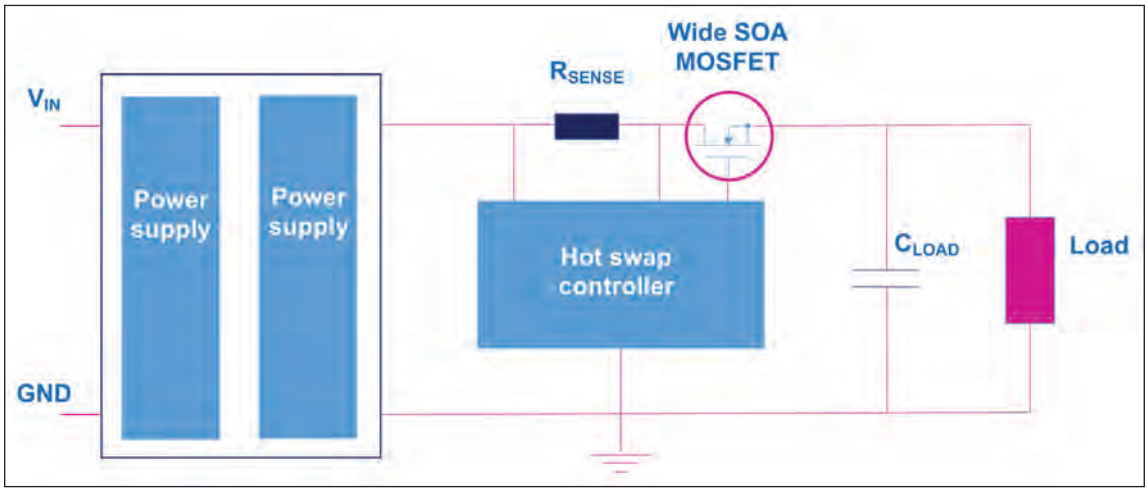
Key criteria for Power MOSFETs in harsh linear mode applications

MOSFET devices are often thought of as the ‘workhorses’ of power electronics due to their wide-ranging applications. But as the experts at STMicroelectronics advise, key criteria are essential to follow when selecting devices for harsh linear mode applications.

BY GIUSY GAMBINO, STMICROELECTRONICS, CATANIA, ITALY

NEW ADVANCED trench MOSFETs are increasingly requested with improved linear mode ruggedness to provide excellent performance in telecom, server and industrial applications. They play a key role in safety switches for battery insulation and power distribution, in-rush current limiters, electronic fuses, linear motor controllers, load switches and hot swap applications. These devices exhibit excellent performance in terms of conduction and switching figure of merit (FoM), offering an optimal efficiency and thermal behavior at high switching speed.

STMicroelectronics released new MOSFETs with a wide SOA capability able to outperform advanced planar technology in linear mode operation, being thermally stable for a wider range of operating conditions into the safe operating area (SOA). Depending on the gate-source voltage (V_{GS}) levels at which the MOSFET is driven, different areas of the device with specific gate threshold voltage (Vth) and current gain values are involved in the drain current (I_D) flow with a trade-off between linear mode and switching performance. With this improved design,



➤ Fig. 1. Hot swap system block diagram.

the new trench power MOSFETs are ideal for rugged forward biased SOA (FBSOA) applications, where high-power levels with high drain-source voltage (VDS) drops are required, ensuring both a high surge current capability in linear mode and low static on-resistance ($R_{DS(on)}$) in fully on conditions.

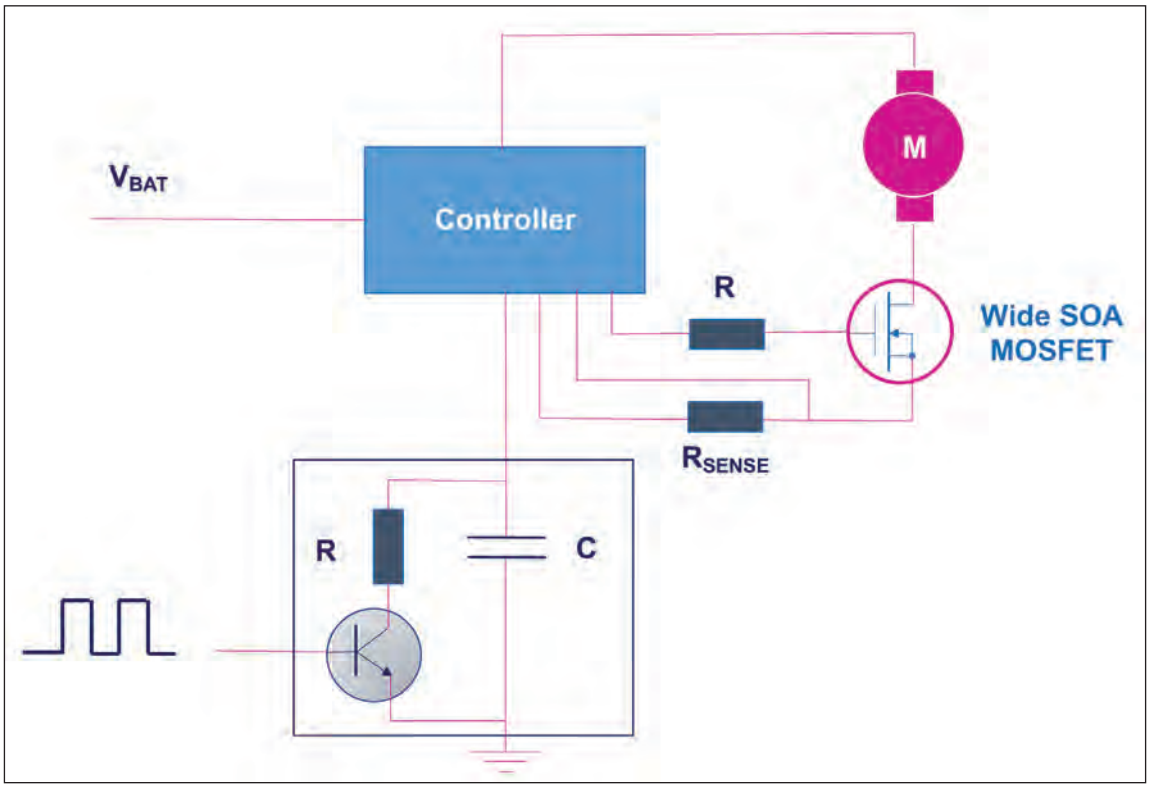
Linear Applications in Power Electronics

Linear mode operation is widely used in power electronics systems and applications that require safe and reliable devices with high ruggedness and thermal stability. High current handling for soft start under significant voltage drops, as well as limiting inrush peaks and any potential failure mechanism are all crucial for hot swap systems. In telecom applications, they are used to charge the bulk capacitor, which powers the entire loading system, such as server, rack and each load connected to the main power supply (Fig. 1).

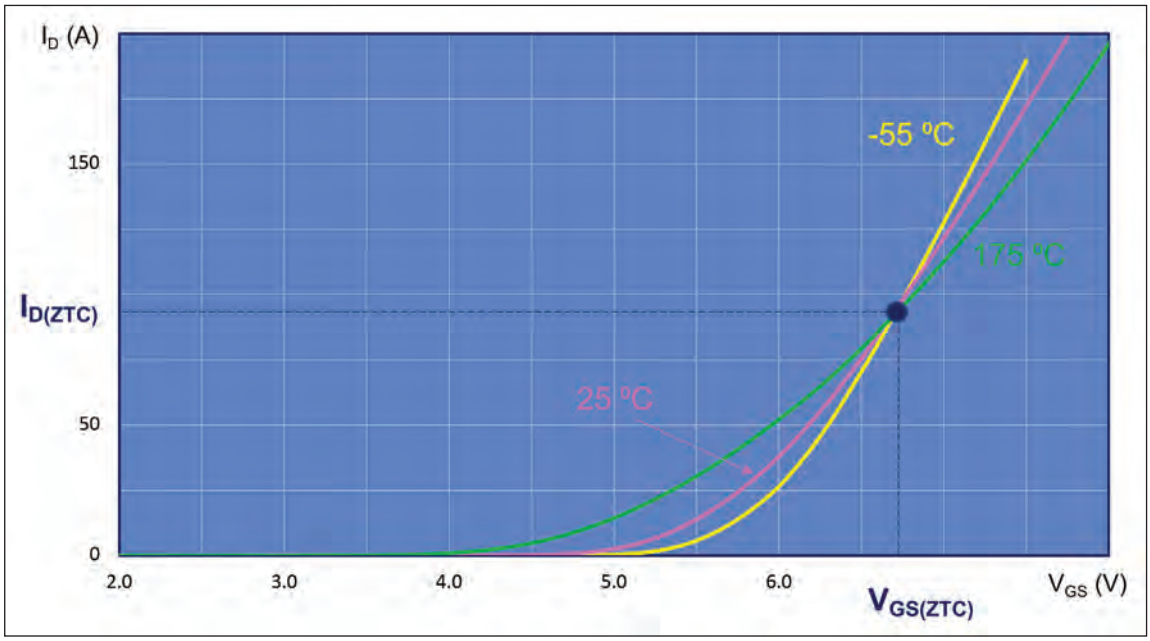
Since system maintenance is performed in most cases once it is permanently functional, by connecting the replaced parts to the rest of the live system, the capacitor may initially be completely discharged and then a huge current of up to hundreds of amperes can flow through the circuit.

Linear mode working conditions are also requested in fan motion control for heating, ventilation and air conditioning (HVAC) systems (Fig. 2).

According to the below motion control system, the VGS voltage of the MOSFET can be changed by tuning the duty cycle of the bipolar transistor driving voltage and then it is possible to control



➤ Fig. 2. HVAC system block diagram.



➤ Fig. 3. Power MOSFET transfer characteristics at different temperatures.

the current through the motor and its speed. The current is set by the equivalent resistance provided by the MOSFET when biased under FBSOA working conditions.

To meet the harsh requirements of linear mode applications, a dedicated MOSFET technology has to be considered with a special focus on the key parameters, such as the thermal coefficient, threshold voltage (V_{th}), transconductance (G_{fs}) and thermal resistance (R_{th}).

Thermal Coefficient

The key parameter to define the linear mode performance of a MOSFET is the thermal coefficient (TC) of the ID current. This coefficient represents the ability of the device to self-balance the current control at both high temperatures and voltages and can be calculated with the following equation (Eq. 1):

$$TC = \frac{\delta I_D}{\delta T} \quad (1)$$

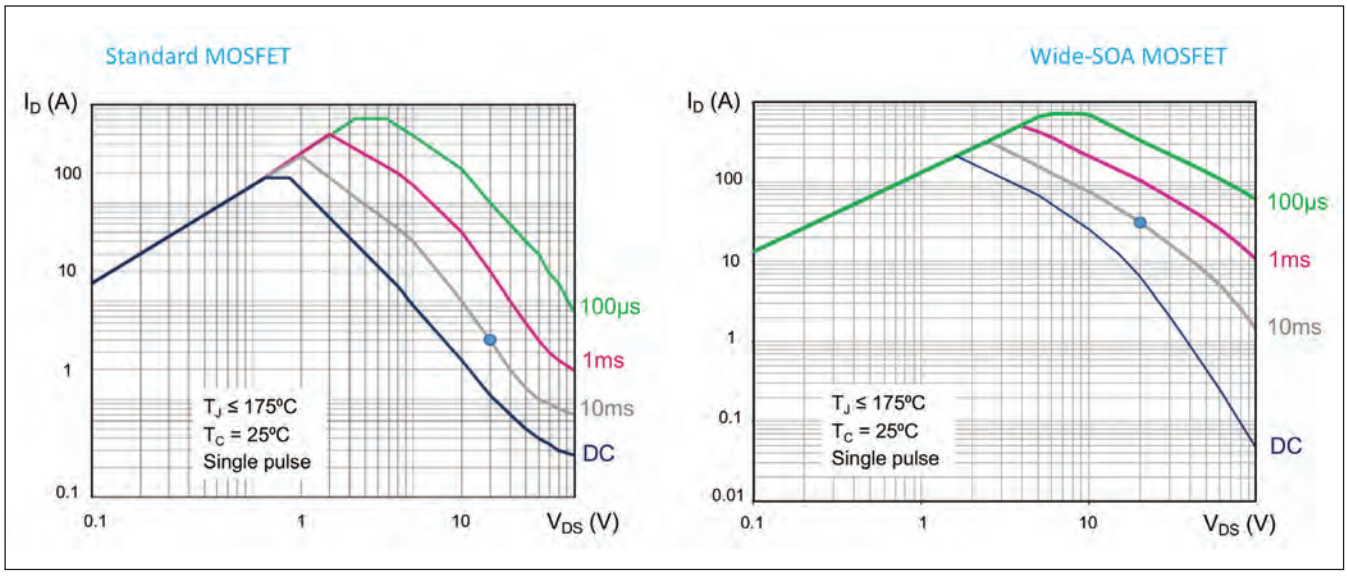
where: ID is the drain current and T the temperature of the MOSFET.

The heat developed inside the junction is due to the electrical power dissipation (PD) in linear mode (Eq. 2):

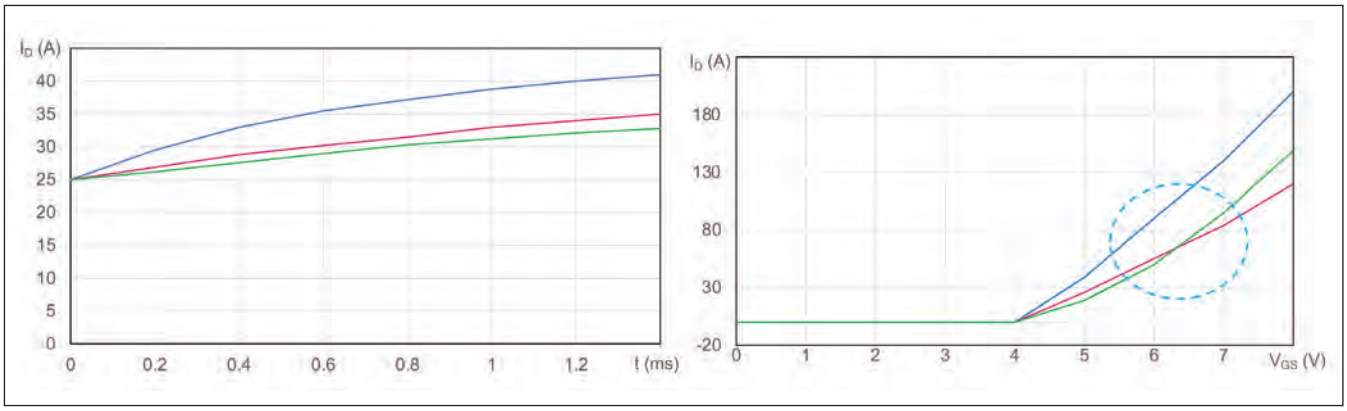
$$P_D = V_{DS} \times I_D = \frac{\Delta T}{Z_{thJA}} \quad (2)$$

where: Z_{thJA} is the junction-to-ambient thermal impedance.

When the temperature increases, the ID current changes according to the thermal coefficient and



➤ Fig. 4. SOA diagram for the standard trench MOSFET and wide-SOA device.



➤ Fig. 5. Simulated drain current stability over time (on the left) and transfer characteristics (on the right).

the device can manage the power until the failure point is reached. The maximum limit of the power is set by the following equation (Eq. 3):

$$V_{DS} \times \frac{\delta I_D}{\delta T} < \frac{\delta \Delta T}{\delta T} \times \frac{1}{Z_{thJA}} \quad (3)$$

The above equation shows that:
- when TC is zero or negative, when the temperature increases, the drain current decreases, then the device works in thermal stability conditions;
- when TC is positive, the device can work without failing if the Z_{thJA} impedance is low enough to dissipate the heat generated by the applied power.

The thermal coefficient is a technology-dependent parameter, linked to the transfer characteristics of the power MOSFET (Fig. 3).

The three transfer curves intersect at a crossing point, called zero temperature coefficient or zero tempco (ZTC):

- For $V_{GS} = V_{GS(ZTC)}$, the device current remains stable with temperature;
- For $V_{GS} > V_{GS(ZTC)}$, as the device temperature increases, the drain current tends to decrease, reaching conditions of thermal stability;
- For $V_{GS} < V_{GS(ZTC)}$ it is vice versa, as the device temperature increases. The drain current continues to increase thanks to the lower threshold voltage, which has a negative coefficient versus temperature. Consequently, when a small area of the die becomes hotter than the adjacent zone, it conducts more drain current, thus creating more heat and pushing the device to failure (thermal runaway), if the appropriate limitations are not set.

Once fixed the thermal coefficient, the device becomes potentially more unstable at high V_{DS} level. The thermal instability condition can be written also as follows (Eq. 4):

$$V_{DS} \geq \frac{1}{TC \times Z_{thJA}} \quad (4)$$

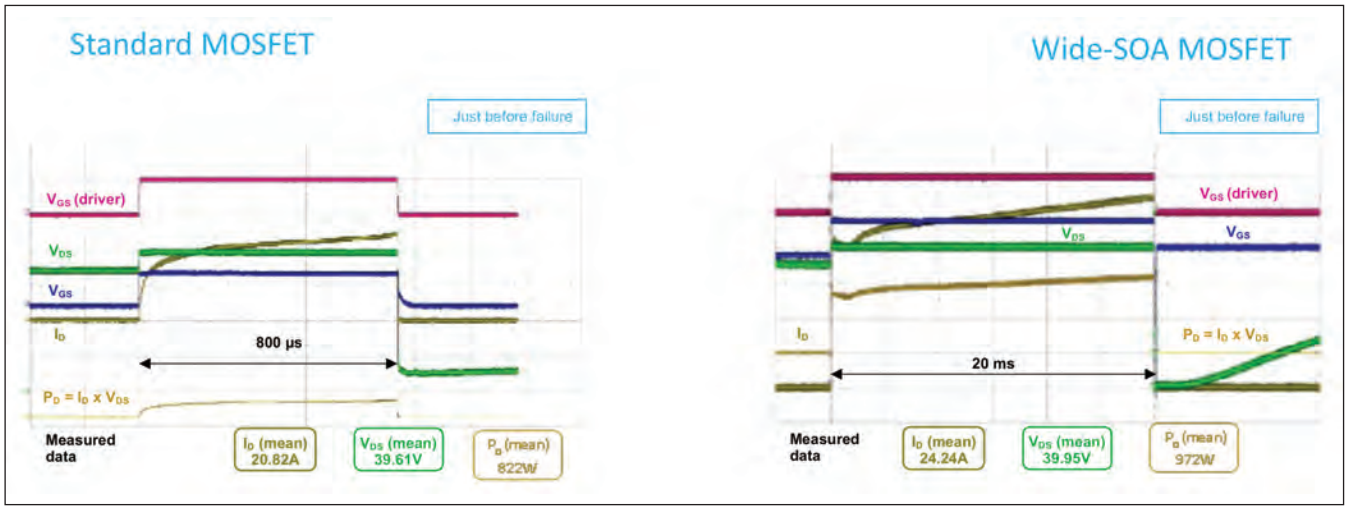
When the V_{DS} voltage increases, the temperature distribution at die level in fact becomes much less uniform, focusing in some small zones of the device. Hot spots determine a localized reduction of the V_{th} voltage and an increase of the ID current, which generates more heat further reducing the V_{th}. This condition could cause the thermal runaway and the failure of the device.

Technology Design Optimization

The wide SOA MOSFET technology is the result of a design compromise between $R_{DS(on)}$ and ZTC point. The device shows different areas, having two different gate threshold voltages (Patent proposal 19-CT-0299 registered in USA in Nov. 2020). When the gate-source voltage V_{GS} reaches the first threshold voltage and is lower than the second threshold voltage, the first device portion starts to switch on even while the second device portion is still turned off. In this condition, the overall behaviour of the device substantially coincides with the saturation mode of the first portion, showing a low current value and a good thermal stability.

When the gate-source voltage VGS exceeds the second threshold voltage, both the first and second device portions are active, therefore the total current has a second value equal to the sum of the current of the two portions. In this condition, both portions operate in the ohmic region with a low

When the V_{DS} voltage increases, the temperature distribution at die level in fact becomes much less uniform, focusing in some small zones of the device



➤ Fig. 6. Measured waveforms for standard trench MOSFET and wide-SOA device at a fixed drain current.

value of on-resistance $R_{DS(on)}$. Moreover, the high values of the V_{GS} voltage are fixed in order to be higher than the ZTC point of the power MOSFET, which therefore does not present any thermal drift issue.

As a result, the wide SOA MOSFET (Model: STH200N10WF7-2,) offers superior performance compared to an equivalent standard trench device for higher current capability under the same operating conditions, as shown in Fig. 4.

The standard trench MOSFET is able to withstand a current of 3A at 20V with a 10ms pulse time, while the new wide SOA device can handle a current of 30A at the same conditions. The improved performance is the result of a technology optimization aimed at ensuring quite flat ID current curves at high V_{DS} voltage values.

The main benefit of the technological improvement is the self-limiting current over time, which is crucial for the thermal stability of the MOSFET over a wider range of operating conditions in linear mode.

FURTHER READING

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Simulation results show the current stability and transfer characteristics of the wide SOA device compared to the standard trench MOSFET and the best competitor’s device available on the market (Fig. 5).

As a result of the design trade-off, the wide SOA MOSFET features a low current gain at lower gate-source voltage (V_{GS}), thus limiting the current increase and, consequently, the thermal runaway in linear mode operation; at higher VGS values, the current gain increases, thereby reducing the on-resistance ($R_{DS(ON)}$) under switching conditions. Thanks to this feature, after limiting the inrush current pulse in linear mode at start up, the wide SOA device can also be driven in PWM (Pulse Width Modulation) mode.

Measurement Results

The ruggedness of the wide SOA MOSFET with respect to the standard device was experimentally verified by testing the following condition:

- With a fixed ID current of 20A, the pulse duration was increased until the device failure.

The measured waveforms just before failure are shown in Fig. 6.

Experimental data highlight the high ruggedness of the wide SOA MOSFET, which survives for 20ms under the stressful linear mode conditions whereas the standard device can only work for 800µs before failing.

Conclusions

The wide SOA MOSFET exhibits good performance in linear mode working conditions thanks to high ruggedness and thermal stability that prevents thermal runaway. In addition, the new device driven in fully saturation region (linear resistive behavior) is also suitable for switching applications, particularly where the linear mode occurs during the transition phases only. The STH200N10WF7-2 is an ideal choice to design safe and reliable electronics systems.

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A case study reveals unconventional electroplating techniques can improve performance

Almost six decades ago Intel cofounder Gordon Moore postulated that processors would evolve regularly to double their transistor count, thereby enabling better performance and lower costs. While traditional Dennard scaling held true for decades, its theoretical limit is fast approaching. The electroplating experts at ClassOne Technology demonstrate a new 'More than Moore' pathway.

BY CODY CARTER, PRODUCT ENGINEER, CLASSONE TECHNOLOGY AND STAN WRIGHT, MANAGER, COMPOUND SEMICONDUCTOR-WLP, MACDERMID ALPHA

Cody Carter

Stan Wright

CLASSONE TECHNOLOGY has built its business around electroplating innovation, demonstrating that 'More than Moore' next-generation technologies do not require ever-shrinking node sizes and exceedingly complex metallization schemes. Today, the company is rethinking fundamental electroplating design to address emerging requirements. Its latest discovery reveals that industry has just scratched the surface of what electroplating can do for power ICs and many other applications.

The Past & Present of IC Tech

The dawn of Moore's Law in the 1960s recognized a trend in the semiconductor industry – namely, that MOSFET devices doubled in performance every year. Moore then predicted that they would continue to do so at least for the next decade. As semiconductors grew in use and value, manufacturers were able to exponentially improve performance through scaling ever-smaller, further increasing their use and value; this pace of advancement would continue for decades to come,

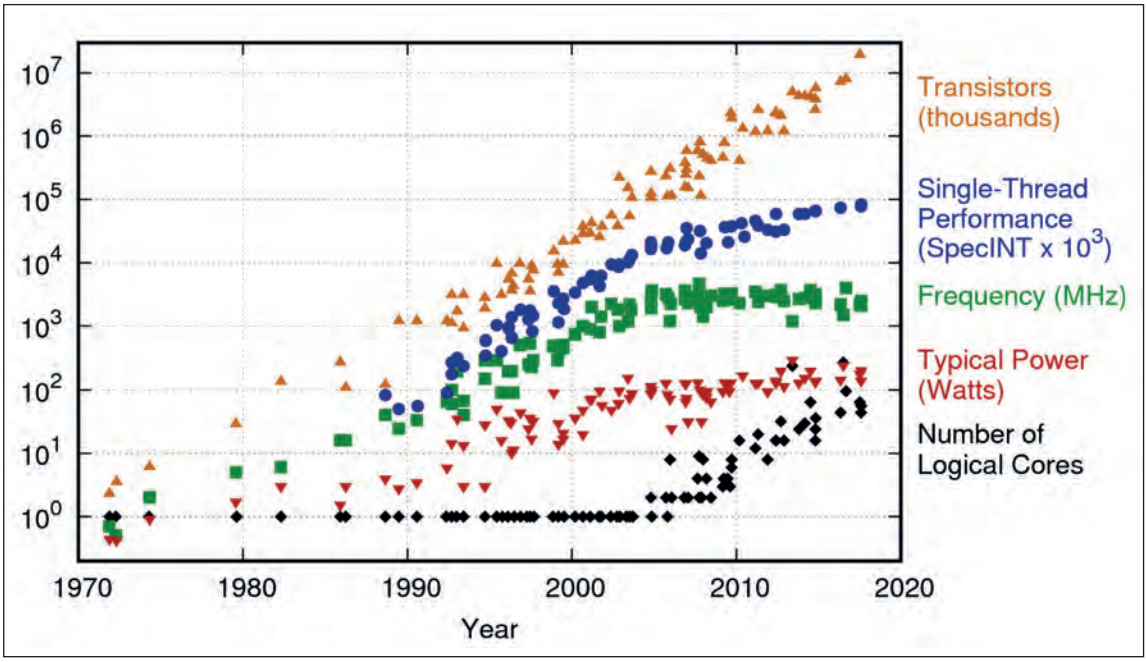
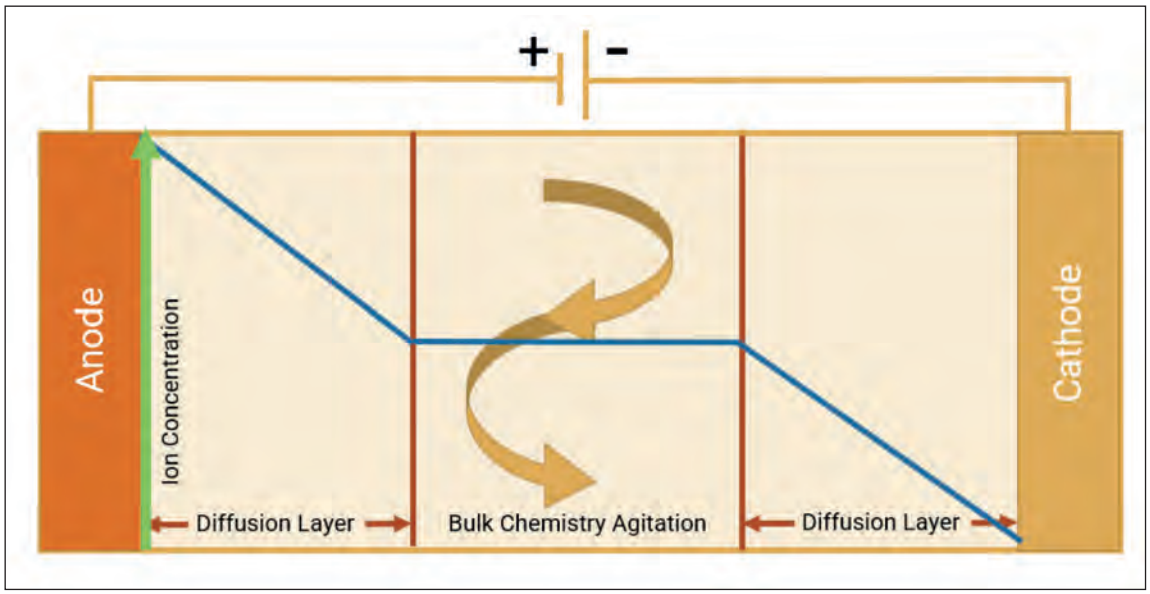
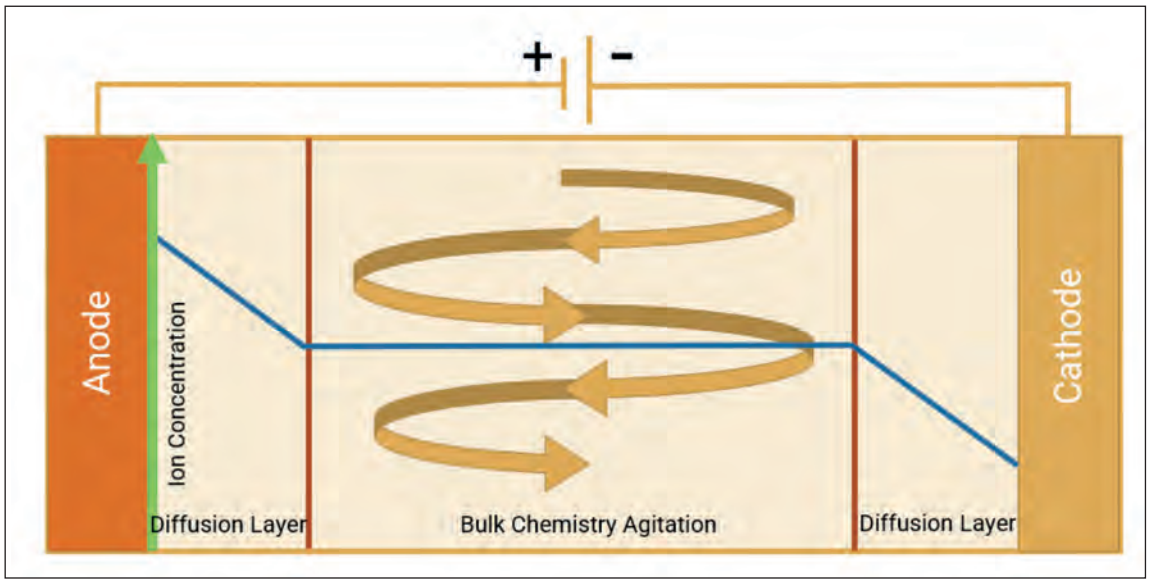


Figure 1. The rate of many device performance metrics has stagnated in recent years.



➤ Figure 2a. Ion concentration varies from the bulk chemistry within the diffusion layer during electroplating.



➤ Figure 2b. Increasing agitation at the anode or cathode shortens the diffusion layer, improving ion concentration curves.

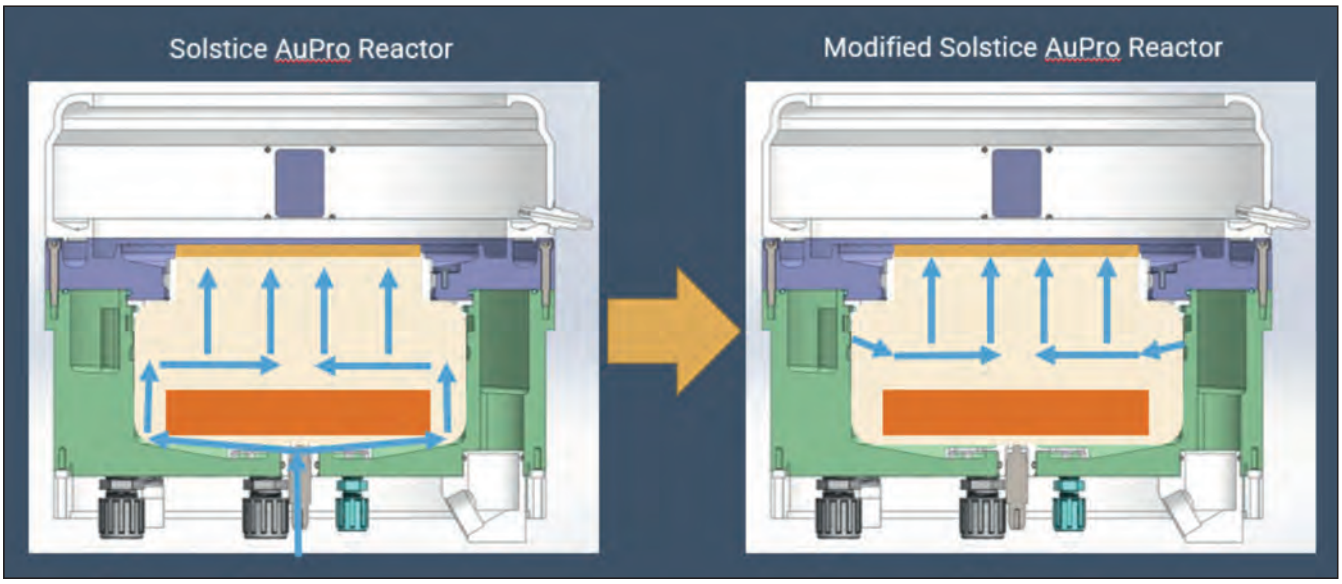
creating two key development trends that have not necessarily been as beneficial to the rest of the semiconductor industry.

The first trend is the way in which technology was driven to development. Because device manufacturers have been primarily focused on scaling logic and memory devices, technology development was dedicated to the specific bottlenecks that hindered this scaling. As a result, certain technologies, such as lithography, received intensive development; other technologies considered adequate for use in this type of manufacturing received less development; and technologies not involved in logic and memory (like gold electrochemical deposition) received significantly less development.

The second trend, specifically for equipment manufacturers, was that complexity was added to the systems to appease this particular corner of the industry. On electroplating systems, for instance, hot entry and multiple anodes were developed for damascene electroplating to counteract the effects of the high resistance of a very thin seed layer.

In the past decade, however, Moore's Law has been approaching what appears to be its practical limit in terms of making smaller nodes, as seen in Figure 1. Simultaneously, the compound semiconductor industry has exploded in diversity with the advent of high-voltage power devices based on gallium nitride (GaN) and silicon carbide (SiC) and high-frequency devices based on indium phosphide (InP). This has led equipment manufacturers, chemistry vendors, and process engineers to revisit these trends to (1) focus on underdeveloped technologies and (2) question whether the technologies they made to enable the frenzied growth of Moore's Law are best suited for this diversity.

To this end, ClassOne Technology and MacDermid Alpha have partnered with their mutual customer, a leading U.S.-based leader in RF device manufacture, to revisit the fundamental reactions occurring in



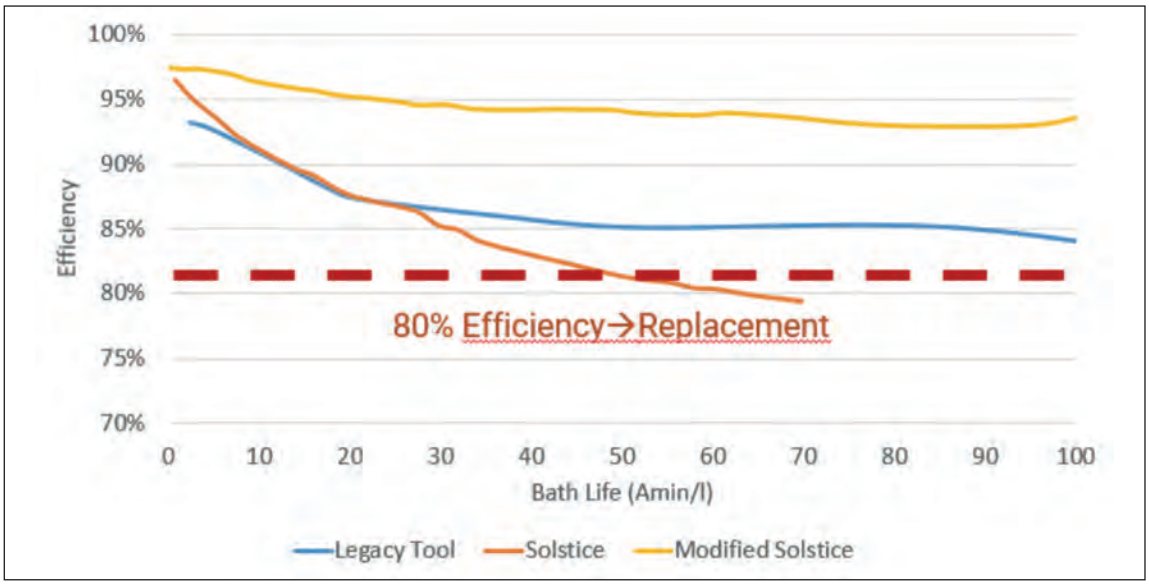
➤ Figure 3. By flowing above the anode, the boundary layer at the anode on the Solstice is increased.

an electroplating system with the goal of attaining better performance from their current process. The outcome was a simple, counterintuitive modification to an existing electroplating reactor.

Getting Moore from Less

Like equipment vendors, chemical vendors were focused on improving their chemistry performance in order to keep up with the incredible growth of the semiconductor market. For electroplating, copper has been the primary metal choice for interconnect applications, and for that reason it has historically been one of the technical bottlenecks for successive technology nodes. By plating physics alone, faster deposition will occur at areas with shorter diffusion distances. Because of this, additives were developed and refined to enable varied plating rates dependent on the topography of the wafer surface. Suppressors move through solution slowly but attach quickly to the wafer surface. Accelerators move quickly but attach slowly. When paired together, suppressors quickly adhere to the higher topography of the plating surface, preventing accelerators from doing so. However, diffusing faster, accelerators can move quickly into the lower topography of a damascene structure or a via and attach to the plated surface there. Levelers then prevent undesirable bumps from forming on the plated surface. These additives have overcome the natural physics and now allow faster plating in areas with greater diffusion distances. The result is uniform deposition on non-uniform seed.

This has been an enabling approach for copper electroplating baths, but other processes, such as gold electroplating baths, have not benefited from this development. Additionally, gold electroplating faces other disadvantages in that it is difficult to stabilize in solution and has very slow diffusion rates. Cyanide-based baths have been the historical standard for gold electroplating. The gold-cyanide complex is relatively stable but does not substantially benefit from high concentrations of gold in solution. More recently, gold sulfite baths



➤ Figure 4. Modifying the Solstice reactor to affect the anode diffusion layer greatly improved performance over that of the initial Solstice GoldPro reactor configuration, as well as the previously existing tool.

have become more popular due to safety concerns with cyanide-based baths and because they allow for higher gold concentrations (and, therefore, faster plating rates). Gold sulfite baths have their own disadvantage, as the sulfite that complexes the gold ion in solution slowly oxidizes over time, making it less stable than its cyanide predecessor.

Compared with copper plating, gold plating is very expensive. The integration of both electroplated metals depends on uniformity to increase throughput in downstream processes (such as CMP). Since gold is very expensive, not only does non-uniform deposition require longer downstream processes, but costs add up in loss of the metal itself, and metal losses are especially egregious when gold is involved. While slower deposition rates can provide better uniformity, it can also cost semiconductor manufacturers by lowering throughput of their electroplating process.

The Problem

For the customer in our case study, electroplating throughput is essential. Years ago, the company developed a process using a legacy cyanide-based soft gold chemistry from MacDermid Alpha that allowed them to meet throughput by running the bath at a current density four times higher than nominal by using semiconductor style fountain plating equipment vs. a traditional rack plating wet bench. One downside of running the bath in this manner is that the bath efficiency (that is, the amount of gold deposited per ampere) would rapidly decrease, then stabilize for a period of time before it needed to be replaced. Since the efficiency is measured by the amount of gold plated per amp, the current was increased so that the plating time for each wafer did not change as the efficiency decreased. This method, though unconventional, proved to be a stable solution. When the customer decided to replace their existing electroplating equipment with ClassOne's Solstice single-wafer platform, an issue arose in which the electroplating baths now experienced an even more rapid decline in efficiency. Instead of six months, the bath now only lasted two weeks – an unsustainable rate for production purposes.

Several potential solutions were deemed impossible from the outset. Reducing the deposition rate into a lower current density range of the chemistry would require the company to quadruple their electroplating tools to make up for the lack of throughput. Moving to a sulfite-based bath, which would allow them to maintain throughput without detriment to the chemistry, would require an extensive requalification process. The last option, then, was for the three companies to collaborate to determine the root cause of this incongruity between the two electroplating systems.

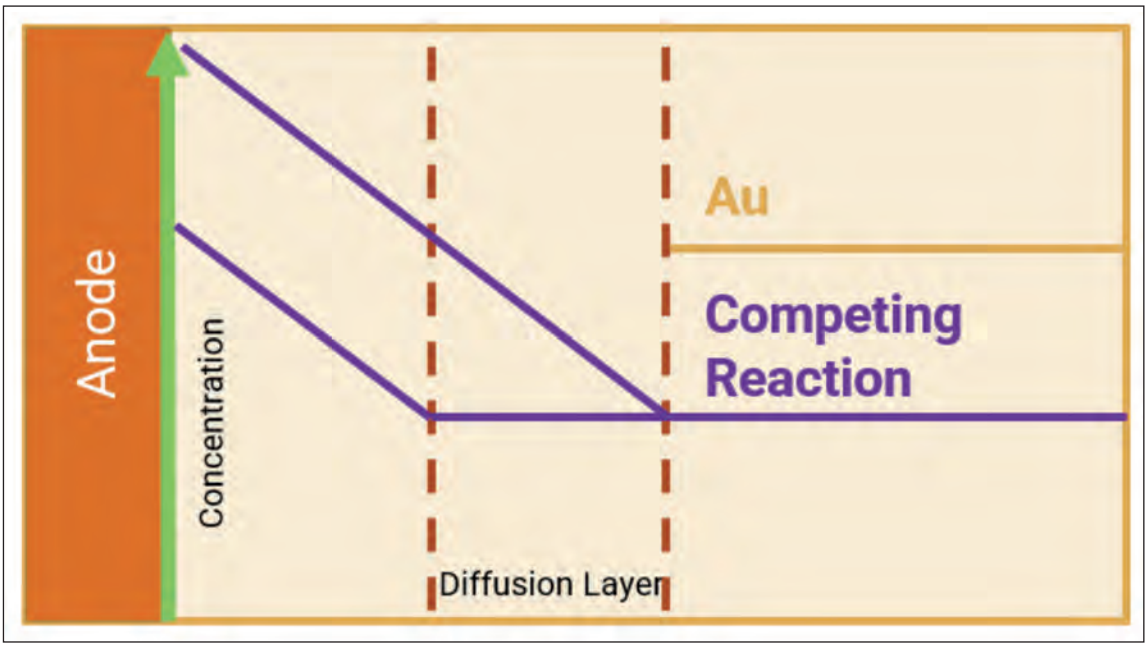
The Process

The first step was creating a model in which we could account for all differences between the two systems – not only physical differences, but even the way they were used in the fab. This included any detail that would pertain to the electroplating reaction, such as the power supply used, fluidics, possible contamination, the way the bath is managed, the product splits between each tool, and even the geometry of the reactors. Overall, 39 individual possible differences were identified, initiating months of troubleshooting to eliminate these possibilities through deliberate testing. What we found would challenge our assumptions regarding fundamental electroplating reactions. The particular electroplating fundamental in this case is that of the diffusion layer. The liquid immediately proximal to the wafer surface is stagnant relative to the wafer. As agitation of the liquid near the wafer surface is increased (by wafer spin, flow, or paddles), this diffusion layer thins, but it does not disappear. Since this liquid is stagnant, the only way for ions to cross it is by diffusion. The rate of diffusion of a particular ion is dependent on its size and the electromotive force applied by the electric field.

Since gold is very expensive, not only does non-uniform deposition require longer downstream processes, but costs add up in loss of the metal itself, and metal losses are is especially egregious when gold is involved

Figure 2a shows the impact of ion concentration at the electrode due to the diffusion layer. The closer to the anode, the higher the concentration of ions; the inverse is true for the cathode. Figure 2b shows how agitation reduces the size of the diffusion layer and therefore affects the availability of ions at the electrode surface for a given current density (depletion rate of ions).

In an electroplating reactor, both the cathode and the anode have critical diffusion layers. As electrochemical reactions occur at the surface of these two components, plating performance (in terms of rate, efficiency, deposited metal uniformity, etc.) is highly reliant on the thickness of the diffusion layer. At the wafer (cathode), a thinner boundary layer allows better access of the ions in the bulk of the fluid with the surface of the wafer, thus allowing faster deposition rate performance. The anode side



➤ Figure 5. The competing reaction becomes less efficient with the increased diffusion layer at the anode.

of the electrochemical cell has its own challenges. In electrochemical processes like traditional acid copper, the anode is soluble, meaning the ions in the bath are supplied by the oxidation reactions on the anode. As the metal atoms from the anode surface oxidize and go into solution, removing them from the anode surface more quickly is desirable as it allows more sites for the oxidation process to occur.

When comparing this example to the customer's electroplating process, we assumed that an insoluble anode used in gold electroplating processes (where the ions to be replenished are supplied as a soluble salt, not by the anode) would follow similar logic. Since ion concentration within the anode diffusion layer for an insoluble anode is not a controlled parameter (overlooking other reactions at the anode, such as evolution of hydrogen or reactions with electrolyte salts), we thus deprioritized one item that had been on our model since the beginning: the fluid path at the anode.

The Solution

The Solstice electroplating system flows chemistry into the reactor directly under the anode. It then flows around it and up to the wafer. On the legacy tool, however, flow comes into the reactor well above the anode and then up to the wafer. By traditional understanding, this was undesirable and not worth putting energy into when there were so many other possibilities.

However, having eliminated all more likely possibilities, we were left with this one difference. We stuck to our problem-solving protocol and made a simple modification to the Solstice reactor to flow the chemistry into the reactor above the anode, as shown in Figure 3. The result was not only a remediation of the short bath life on the Solstice, but a dramatic improvement over the legacy tool's performance, as shown in Figure 4. While a traditional understanding of the diffusion at the wafer remains intact, this testing has greatly challenged our understanding of its role for inert anodes. The leading theory as to why this change worked is that in the absence of gold metal oxidation at the insoluble anode, there are still other byproduct reactions at the anode.

The reduced diffusion layer at the anode does make the desired reaction more efficient, but it also makes the byproduct reaction more efficient at an even greater rate. When the diffusion layer at the anode was increased with the new flow path, the byproduct became less efficient while the desired reaction efficiency remained intact (Figure 5). What this tells us, beyond this particular instance, is that a renewed fundamental understanding of electroplating is available to inform the semiconductor industry going forward.

Looking Forward

What this documented experimentation means for semiconductor manufacturers is that the way things have been done is not the way they should be done when new and improved tool configurations are introduced. Electroplating tools have acquired immense capability over the years through complexity demanded by a particular market, while other technologies have not received adequate attention.

What if that complexity is not needed for every corner of the semiconductor field? Can we rethink the way we design equipment to provide the capability that is needed by often-neglected chip producers without added complexity? By revisiting fundamental plating principles, we believe that the era of 'More than Moore' will better serve the diverse compound semiconductor and overall power electronics market.

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Swappable batteries set to revolutionise the power industry

Paul Bramhall, Director Electrification & Rental EMEA, from Briggs & Stratton discusses the benefits of the new Vanguard Si 1.5kWh battery and what it brings to the growing power rental market.

Powering the rental market

THE BATTERY MARKET is growing swiftly with demand across multiple industries increasing. Driven by the need to reduce carbon emissions and work towards a "greener future", the push for electrification is affecting businesses of all sizes. With the cost of battery powered equipment on the rise compared to traditional combustion engines, users can face the uncomfortable situation of having to choose between meeting sustainability goals or boosting profit margins. This is when the option of rental equipment can provide a workable solution that avoids large upfront fees and reduces costs.

The global construction equipment rental market alone has grown to over $73.4 billion with a majority market share held in North America and throughout Europe.* Forward projections suggest that this market could surpass a value of over $105 billion by 2030, presenting an increasingly promising opportunity for battery manufacturers to tap into.

Rental equipment helps companies to reduce their bottom line and lower their total cost of ownership. Rather than purchasing equipment outright, which comes with high costs, maintenance fees, insurance and long-term storage needs, renters can access the best products on the market for a reduced fee without putting their own capital at risk. This is particularly beneficial for businesses new to the market, which do not yet have the capacity to take on expensive equipment and therefore need to find alternative solutions that still meets their needs. Whilst rental equipment offers great benefits for the end user, there can be difficulties when it comes to battery powered applications. Recent market trends have seen OEMs try to offer an all-in-one solution approach that leads to sub-par batteries and creates further issues for the end user. To make the rental market more inviting, more needs to be done to limit the number of batteries required to get the job done, ultimately making things easier for the end user. Rather than multiple batteries, each requiring its own power cable, charging facility and user manual, solutions that can be integrated across multiple machines will vastly improve accessibility and efficiency.

To achieve this, OEMs need to work with power suppliers to develop equipment solutions that meet these growing needs. With multiple machines in use across construction sites, manufacturing plants and landscaping grounds, renters could otherwise be forced to accommodate an untenable number of batteries, each with individual charging systems. This would put more pressure on space requirements and overheads, pushing higher costs on the renter and making the move to rental equipment an inefficient and undesirable option.

As battery power becomes the increasing norm, OEMs will need power suppliers capable of providing a power-agnostic approach whereby their power solutions can be used across a wide range of machines to better serve the growing rental market. The newly launched Vanguard 48V Si 1.5kWh Swappable Battery pack from Briggs & Stratton aims to serve this need by providing a battery that can be easily moved from application to application on active jobsites, reducing downtime for the end user and therefore boosting efficiency and productivity.

Making use of effective swappable batteries

With the ability to be used across multiple machines, rental users can easily move the Si 1.5kWh between applications. The integrated battery management system (BMS) and CANbus J1939 communicate with the application to adjust the discharge rate and ensure effective power output without damaging the battery. This helps to reduce reliance on multiple batteries and streamlines rental company service offerings. Rather than sending out numerous pieces of equipment, each with their own charger and charging recommendations, rental companies can supply one type of charger to charge one type of battery and still power multiple applications.

As different machines used by renters will each have different power requirements, it is important that they are powered by scalable batteries. These battery formats are ideal as they can be stacked in parallel to achieve the desired input required to power each of the individual applications. The Si 1.5kWh battery has been designed with this in mind, with the option for up to 10 batteries to be used in parallel to achieve an overall power of 15kWh. As not all applications will require ten batteries, those not in use can be charged to ensure that the user has access to battery power as and when it is needed.

The resulting process is far more streamlined compared to fixed solutions, which require downtime to replenish energy capacity. Batteries will always require charging, this is unavoidable, but the availability of multiple units will maximise equipment usage in the rental period, delivering the most value by providing more efficient working operations and enabling users to deliver effective results more easily. With the easy latch system on the Swappable Battery, users can swiftly replace a battery when it runs out of charge. This system also allows users to move the battery between applications to tackle a wide range of tasks.

Moving towards standardised power will reduce reliance on traditional combustion engines and enable end users to move closer to their environmental targets. It will require OEMs to work collectively with power providers and rental companies to find solutions suited to multiple machines, while ensuring power requirements are met and equipment is user-friendly for efficient and effective application.

Current factors affecting the market

Currently, there is a growing focus from OEMs to develop their own in-house batteries to power their equipment. With the intention of creating all-in-one packages, this fast-paced movement towards electrification is seeing many OEMs race to develop power solutions and failing to meet the demands of the end user. Instead, OEMs need to look outwards to power specialists who can advise on the right solution for the unique power capabilities of each application in development. Power specialists, such as Briggs & Stratton, have vast experience in developing power solutions that meet the needs of the end user. As an independent power provider, they can work with a wide range of OEMs to develop power solutions suited to the equipment in question. By working with an independent power specialist, rental companies can select from a wide range of manufacturers to meet customer needs, safe in the knowledge that they will not need to rent out multiple batteries and chargers to each user.

Instead, the renter themselves can reduce their space costs by streamlining their equipment to run off one type of battery. The rental company can offer equipment from a range of OEMs, but the power source for each machine will be the same. This helps to reduce manufacturing pressure and, in turn, reduce the need for mining new materials.

Next steps for OEMs

When it comes to developing unique applications to meet the demands of the growing electrification market, it is important to engage collaboratively with effective power providers. That way OEMs can develop unique applications that will improve efficiency and execution for your target audience. With the growing opportunities that the rental market offers, connecting with companies like Briggs & Stratton will enable OEMs to capitalise on the growing demand for electrified equipment.

As companies continue to explore ways to reduce their emissions quotas to meet growing customer demand and reduce their overall environmental impact, it is important to find power solutions that can meet demand without compromising overall performance. To achieve this, agnostic power specialists who understand your power needs and deliver a bespoke solution will provide the best way forward.

This has never been a more pressing issue for the rental hire market, where diverse ranges of equipment are available to customers. In a traditional, fossil fuel-led approach, end users can easily make use of the same petrol source in each machine. However, as manufacturers look to move to battery power, there are growing concerns over the different battery platforms that rental companies will need to deal with.

Overcoming these concerns requires an agnostic power solution that can be used across multiple brands and a wide range of machines. Breaking away from closed-off battery platforms to work collectively with other OEMs using the same battery platform will help to reduce the number of batteries in production – a vital step towards the ultimate goal of a greener future.

*study by Grand View Research: https://www.grandviewresearch.com/industry-analysis/construction-equipment-rental-market

A GaN device for all markets

GaN power device maker, Navitas, believes its latest half-bridge power IC will deliver the high powers and efficiencies that mobile phone chargers, electric vehicles, photovoltaics and data centres need, reports **REBECCA POOL**

IN EARLY September this year, California-based GaN power device manufacturer, Navitas, released 'GaNSense', a half-bridge power IC that the company reckons provides a 'new level' of megahertz switching frequencies whilst slashing system cost and complexity compared with discrete half-bridge GaN ICs.

As Llew Vaughan-Edmunds, senior director of marketing at Navitas, points out: "The difference between Navitas and other gallium nitride companies is that we integrate the gate driver monolithically with the gallium nitride power and integrate real-time sensing and autonomous protection – that's the secret of our success and why we're number one in this field."

Following industry's relentless demand for more power and higher switching frequencies, Vaughan-Edmunds is certain that GaN ICs are going to be instrumental to the power devices of the future. Looking at mobile device chargers, right now Apple and Samsung wireless fast charge power adapters are currently rated to around 45W, but this is quickly changing. "These chargers are going to 65 W and 100 W now, and ultra-fast chargers have just been released at 200 W so you can charge your phone within 10 minutes," says Vaughan-Edmunds.

At the same time, data centres are striving for higher efficiencies to reduce electrical and cooling costs, as are electric vehicles to reduce battery recharge times. "[Industry] needs half-bridge topologies to meet these higher power, higher switching frequency and higher efficiency market demands, and this is why we've released our half-bridge IC now," he adds.

Navitas' half-bridge power IC integrates two GaN FETs with drive, control, sensing, autonomous protection and level-shift isolation in a single package. GaN is notorious for its sensitive gate structure, so from word go, Navitas has set out to deliver GaN power ICs with robust GaN gate protection. Given this, autonomous protection is a key feature of the latest chips. As Vaughan-Edmunds points out, gate driver and sensing protection is now imperative given the noise generated at higher frequencies and powers. At the same time, temperature protection and over-current protection

will autonomously shut down the chip to prevent device and system failure.

The Navitas director also points out how this set-up requires 61 percent fewer components and has a 64 percent smaller footprint than a typical discrete GaN half-bridge IC. “By eliminating all the [associated] circuitry, we’re reducing circuit parasitics – this does give us nice, clean switching,” he adds. “We are the first company to release a half-bridge power IC with this level of integration and rich feature set.”

Market-driven

Importantly, these latest half-bridge power ICs are already in mass production in Europe. “Strategically, we wanted to be first to market in key growth segments,” says Vaughan-Edmunds. This sentiment is clearly in line with past product launches.

Navitas power ICs have been in production since 2018, and just last year industry analyst TrendForce indicated that this west-coast chipmaker held the greatest market share amongst GaN power device suppliers.

According to Navitas, its technology is now in well over 150 different charging products from different companies – key partnerships include Lenovo, Xiaomi, Dell, Oppo, LG and Amazon. And, in a recent *Compound Semiconductor* interview, Navitas vice president Stephen Oliver estimated that the company was working with more than 90 percent of OEMs that are supplying phones, laptops and tablets.

Beyond mobile chargers, the company is gearing up for solar, datacentre and electric vehicle applications, and anticipates these markets to start bringing in revenue within the next 3 years. “The fast mobile charging market is our bread and butter right now, but beyond charging, our strategy includes looking at solar, electric vehicle and data centre markets,” says Vaughan-Edmunds. “The electric vehicle and data centre markets take longer in design cycles and qualification, however these are key strategic markets for Navitas and where we are focusing.

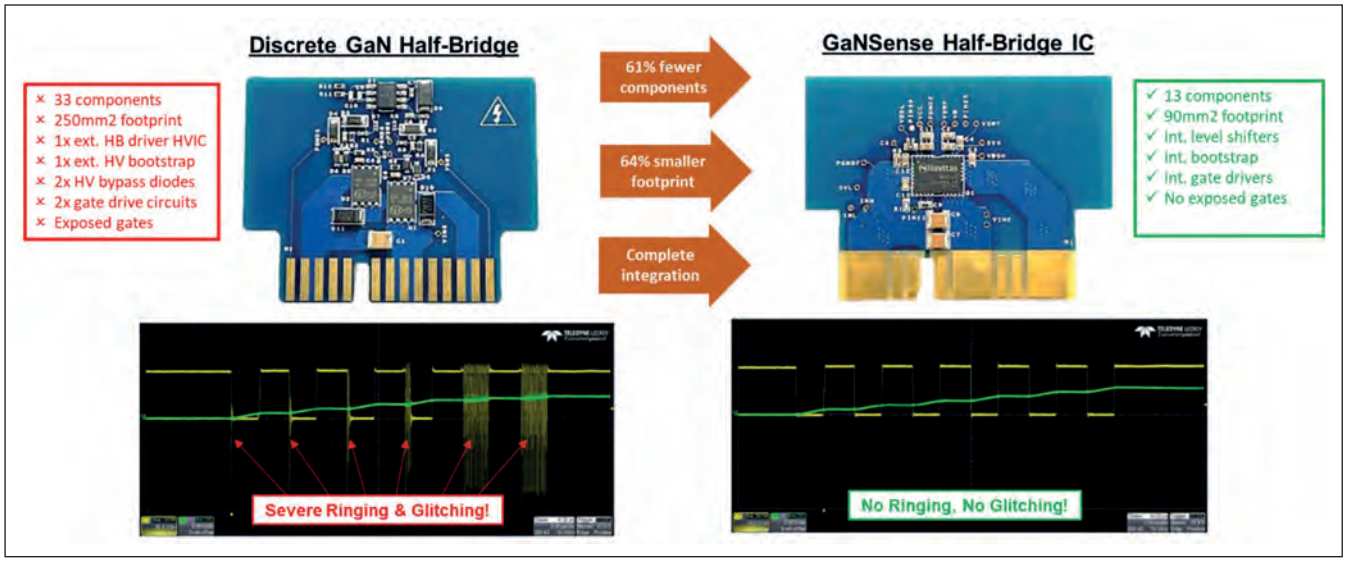
Navitas power ICs have been in production since 2018, and just last year industry analyst TrendForce indicated that this west-coast chipmaker held the greatest market share amongst GaN power device suppliers

“If we look at the mobile charging market alone – right now GaN only has a few percent of the total market so we’ve still got a lot of room to grow,” he adds.

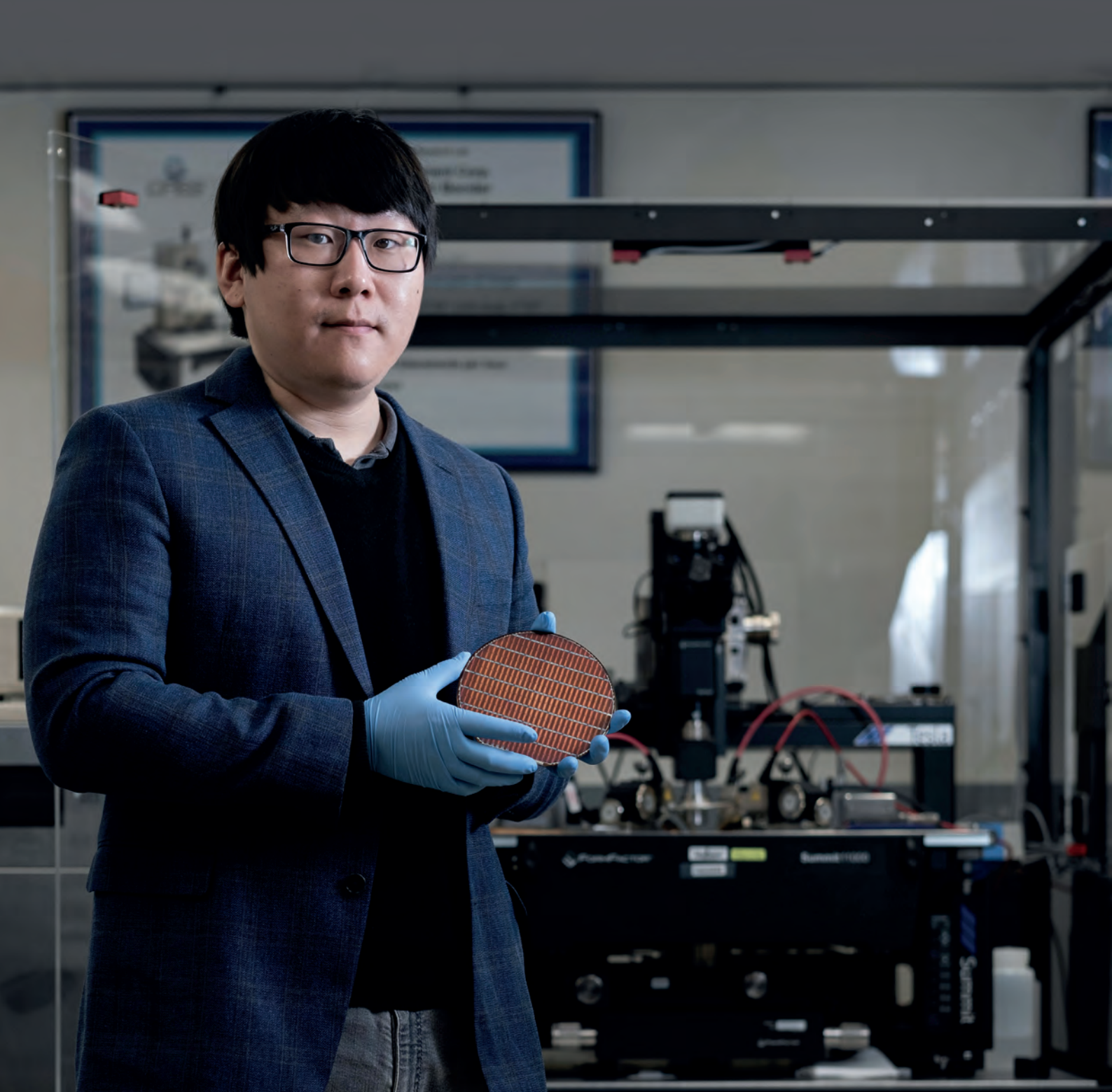
Bringing in SiC

Yet despite the company’s clear advocacy towards GaN, it acquired SiC developer GeneSiC Semiconductor for $100 million in late August. At the time, Navitas chief executive, Gene Sheridan, said GeneSiC will help his company to accelerate growth in the high-power solar, datacentre and electric vehicle markets.

For his part, Vaughan-Edmunds highlights how rugged, vertical SiC devices are better suited to traction inverters, which provide enormous amounts of torque and acceleration in electric vehicles. “We’re not a gallium nitride company trying to convince customers to use gallium nitride instead of silicon carbide. We realise that silicon carbide has its place in the market, and it’s a big market that we want to go after,” he says. “On gallium nitride alone, we’ve already shipped more than 50 million pieces, with zero field failures – and that’s only just scratching the surface.”



➤ Discrete GaN half-bridge IC versus Navitas’ latest half-bridge IC.



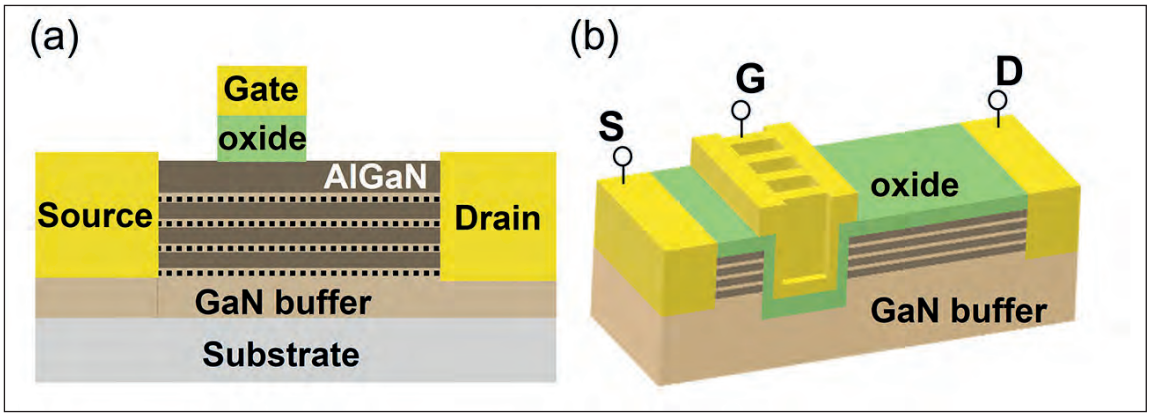
Stretching GaN power devices to 10 kV

GaN power rectifiers and transistors combine a breakdown voltage beyond 10 kV with a specific on-resistance that's below the SiC limit

BY YUHAO ZHANG FROM VIRGINIA TECH

➤ Yuhao Zhang holding a GaN power transistor wafer in front of the 10 kV probe station

ONE OF THE KEYS to getting carbon emissions to net zero is to increase the efficiency of electrical energy processing. This can be accomplished through the introduction of semiconductor-based power devices with a lower on-resistance, a faster switching speed and a high breakdown voltage. It is a roll-out that must include devices operating between 1 kV and 35 kV, a range that's often known as medium-voltage, but also referred to as high-voltage in many contexts. Devices operating in this range are ubiquitously used in electrical grids, renewable energy processing, industrial motor drives and electrified transportation. Driven by this widespread deployment, the market size for medium-voltage power devices has already topped $10 billion and is increasing at pace.



➤ Figure 1. The multi-channel AlGaN/GaN HEMT with a planar gate (a) and a trigate architecture (b).

Dominating today's medium-voltage power device market are a pair of silicon devices: the insulated-gate bipolar transistor; and the *p-n* diode, up to a voltage class of 6.5 kV. Both suffer from a slow switching speed, stemming from bipolar operation – as electrons and holes contribute to current conduction, both forms of carrier must be removed or supplied during device switching.

A superior performance can be realised by turning to the unipolar SiC MOSFET and the SiC junction barrier Schottky diode. These alternatives, which enable faster switching speeds, are covering an increasingly broad range of voltages. They have been commercialized up to 3.3 kV, and industrial R&D devices are available up to 10 kV.

But that's not the ultimate solution, as even better results are possible with SiC's wide bandgap rival, GaN. Providing a higher critical electric field and a higher electron mobility, GaN enables the fabrication of devices with a lateral or a vertical architecture. Lateral GaN HEMTs operating at up to 900 V are already on the market, and industrial vertical GaN transistors have been demonstrated at the 1.2 kV class. Progress has also been made at far higher voltages. Some groups are reporting GaN devices with blocking voltages close to 10 kV. However, specific on-resistances are much higher than those of SiC counterparts, leading many to conclude that GaN is only advantageous in the low-voltage range.

But those of us at Virginia Polytechnic Institute and State University – better known as Virginia Tech – beg to differ. Working in collaboration with engineers at the University of Southern California, the University of Cambridge, Enkris Semiconductor and Qorvo, we have developed a new generation of lateral medium-voltage devices that are based on a multi-channel GaN platform and outperform their silicon and SiC counterparts.

We produce our devices from multi-channel AlGaN/GaN wafers that consist of vertically-stacked heterostructures, which enable the fabrication of diodes and HEMTs that feature a high mobility two-dimensional electron gas (2DEG) channel. These devices offer a high-power handling capability, thanks to the stacked channels (see Figure 1(a)), and can leverage some of the benefits of vertical devices, such as a spatially distributed current. By drawing on a series of device innovations we have demonstrated 10 kV GaN Schottky barrier diodes and normally-off HEMTs that exceed the one-dimensional SiC unipolar limit, in terms of the trade-off between the specific on-resistance and the blocking voltage.

Challenges of multi-channel devices

It is easy to understand why the introduction of multiple channels reduces the on-resistance of a device. Using the 4-inch multi-channel GaN wafer grown by Enkris Semiconductor, the devices that we fabricate feature five channels, leading to a sheet resistance of just 120 Ω/sq – that's about a third-to-a-quarter of that of today's commercial GaN HEMTs formed from single-channel wafers. The upshot is that a switch to multiple channels enables a dramatic decrease in specific on-resistance.

Unfortunately, enjoying this benefit is far from trivial. There are two fundamental challenges associated with multi-channel devices.

The first arises because when the device is blocking voltage, there is a large volume of charge in the stacked channels that can lead to a fast drop in the electric field. This is a fundamental issue, expected from the simple Poisson equation. Due to this large

By drawing on a series of device innovations, we have demonstrated 10 kV GaN Schottky barrier diodes and normally-off HEMTs that exceed the one-dimensional SiC unipolar limit, in terms of the trade-off between the specific on-resistance and the blocking voltage

volume of charge, there is a low average electric field across the device length, and increasing this dimension does not ensure an upscaling of the blocking voltage. Note that with these net charges, even if there is a good edge termination that enables a large peak electric field at the device edge region (see *Compound Semiconductor* 27 **3** 44), the blocking voltage of a multi-channel device tends to be much lower than that of a single-channel counterpart with the same length.

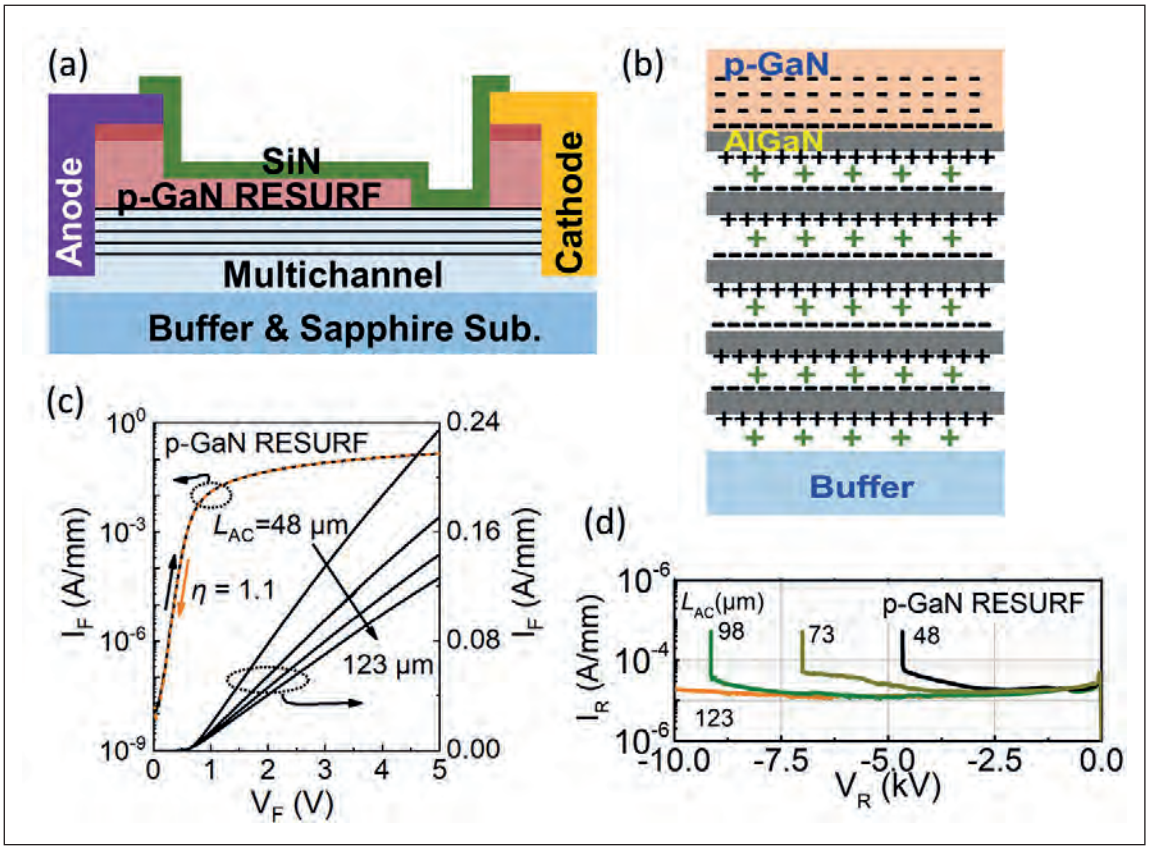
The second challenge faced with the multi-channel device is ensuring sufficient gate control. Within a conventional HEMT, a planar gate is often employed to modulate the 2DEG channel. That's not a good idea in a multi-channel device, because the top 2DEG channel will shield the gate electrostatics from reaching the buried channels. If this approach is taken, there is a very negative threshold voltage, even down to -100 V, and a very poor transconductance. In short, such a device is unsuitable for power electronics applications, which should have devices that are normally off.

A solution to this issue is to turn to either FinFET or trigate architectures, similar to those deployed in deeply-scaled silicon CMOS devices. Introducing a trigate design (see Figure 1 (b)) results in the wrapping of multi-channel fins around a gate stack. With this configuration, the sidewall gate controls the buried 2DEG channels. However, due to the high 2DEG density, the fins must be as narrow as around 10-15 nm to ensure normally-off operation in multi-channel HEMTs. Since today's power semiconductor industry mainly relies on processing at length scales of 180 nm or more, it is very difficult to manufacture trigate multi-channel HEMTs on an industrial scale.

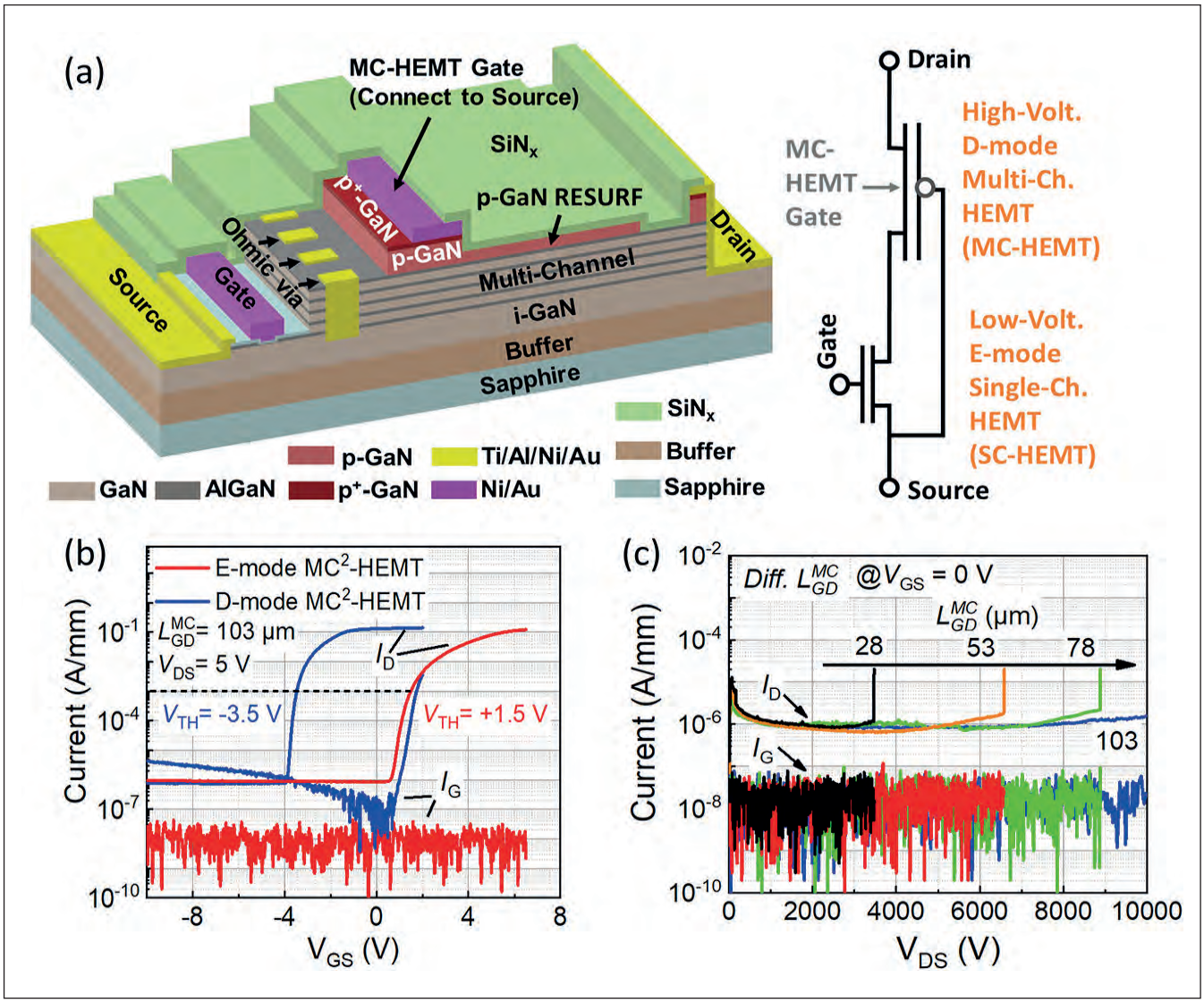
Reducing the surface field

Complicating the charge profile in a multi-channel architecture is the existence of multiple sources of polarization charge. Overall, a net donor tends to be present, which is in part the origin of the 2DEG in the multi-channel at zero bias. To balance this net donor at high blocking biases, we introduce a *p*-type GaN cap layer that provides a reduced surface field (RESURF) structure (see Figure 2 (a)). In a diode, this *p*-GaN RESURF layer extends to near the cathode, and its acceptor charges balance the net donor charges (see Figure 2 (b)). We are able to experimentally realise this charge balance by designing an appropriate *p*-type doping concentration, or by adapting the *p*-GaN thickness through a *p*-GaN etch that is monitored by a test structure.

It is worth noting that the addition of this *p*-GaN cap decreases the 2DEG density, particularly in the top channel. The wafer that we use, provided by Enkris, is produced by MOCVD, with the *p*-GaN layer grown continuously with the five-channel structure. This has a sheet resistance of 178 Ω/sq, which is still higher than the equivalent wafer without the *p*-GaN layer. However, compared to the single-channel wafer, the sheet resistance is smaller by more than a factor of two. The upshot is a slight increase in the on-resistance, but this is overshadowed by tremendous gains in blocking voltage, enabled by the RESURF layer.



➤ Figure 2. (a) The *p*-GaN reduced surface field (RESURF) architecture improves the performance of the Schottky barrier diode via charge balancing. (b) Illustration of charge balance at reverse bias. (c) Forward and (d) reverse current-voltage characteristics of devices with different anode-to-cathode distances (L_{AC}).



➤ Figure 3 (a) The multi-channel monolithic-cascode HEMT, known simply as the MC2-HEMT, combines an on-resistance and blocking voltage that comes from the multi-channel region with a gate control that is dominated by the single-channel region. The design of the MC2-HEMT is shown alongside its equivalent circuit. (b) Transfer characteristics of the MC2-HEMT with and without a gate recess in the low-voltage HEMT. (c) Off-state I-V characteristics of the MC2-HEMT with various lengths of the multi-channel region.

The introduction of RESURF technology has enabled us to fabricate a Schottky barrier diode with a turn-on voltage of just 0.6 V (see Figure 2(c)), which is lower than that of SiC junction barrier Schottky diodes. Through judicious choice of the anode-to-cathode distance, the blocking voltage of the *p*-GaN RESURF Schottky barrier diode can be about 1.5-fold higher than that of a Schottky barrier diode with merely a *p*-GaN termination (see Figure 2(d)).

For RESURF Schottky barrier diodes, the average lateral electric-field can be as high as around 1 MV/cm. This enables a Schottky barrier diode with a 123 µm anode-to-cathode distance to realise a blocking voltage of more than 10 kV and a specific on-resistance of just 39 mΩ cm^2 – that's 2.5-fold lower than the specific on-resistance of state-of-the-art 10 kV SiC junction barrier Schottky diodes.

Normally off 10 kV HEMTs

To realize normally-off operation without the need for sub-micron lithography, we are pursuing a new device concept: the multi-channel monolithic-cascode HEMT, which we refer to as the MC2-HEMT. Due to its cascode configuration, the normally off low-voltage transistor is connected to the normally on high-voltage transistor. The composite that results may be operated in a similar manner to the standalone, normally off, high-voltage transistor. Note that cascode configurations are well established, with commercial devices available in GaN and SiC, where a silicon MOSFET is co-packaged with a GaN HEMT or SiC JFET.

A key difference between these cascode devices and the MC2-HEMT is that the latter builds on a single chip. There is monolithic integration of a low-voltage,

normally off HEMT that has a single 2DEG channel and a high-voltage, normally on HEMT that is based on a stacked 2DEG multi-channel (see Figure 3(a)).

Within this design there is a plurality of Ohmic vias, which function as the effective drain for the single-channel, low-voltage HEMT, as well as the source for the multi-channel high-voltage HEMT. Additional features of this architecture are the introduction of a gate recess in the low-voltage HEMT to ensure normally off operation, and the use of a RESURF structure for the high-voltage HEMT to upscale the blocking voltage.

The MC2-HEMT delivers a strong performance on several fronts, combining an on-resistance and blocking voltage that comes from the multi-channel region with a gate control that is dominated by the single-channel region.

Thanks to these characteristics, our MC2-HEMT can exploit the low sheet resistance that stems from multiple channels while realizing a normally off gate control and enjoying complete shielding of the gate region from a high electric field. This design also obviates the need for sub-micron fin gates, significantly relaxing the lithography requirement.

Measurements of device transfer characteristics (see Figure 3(b)) shows that the introduction of a gate recess to the low-voltage HEMT enables a threshold voltage of over 1.5 V.

Meanwhile, off-state current-voltage characteristics (see Figure 3(c)) validate our claim that the blocking voltage scales with the length of the multi-channel region up to more than 10 kV.

For the 10 kV MC2-HEMT, specific on-resistance is only 40 mΩ cm^2, which is 2.5-fold smaller than that of 10 kV SiC MOSFETs, and well below the one-dimensional SiC unipolar limit. Another great result for our MC2-HEMTs is that they have the highest Baliga's figure-or-merit for any power transistors operating at 6.5 kV or more.

Our progress helps to demonstrate that medium-voltage GaN power Schottky barrier diodes and HEMTs operating up to 10 kV will allow GaN power technologies to enter a new era. These devices are breaking ground on many fronts: as well as offering higher voltages, they are setting a new benchmark for the trade-off between on-resistance and breakdown voltage that goes beyond the one-dimensional SiC unipolar limit.

Such results call into question the commonly held belief that SiC is superior to GaN in medium- and high-voltage power electronics. While SiC is now displacing silicon in this power electronic sector, the future surely belongs to GaN.

FURTHER READING

- M. Xiao *et al*. "Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV" 2021 IEEE International Electron Devices Meeting, 5.5.
- M. Xiao *et al*. "10 kV, 39 mΩ·cm^2 Multi-Channel AlGaN/GaN Schottky Barrier Diodes" IEEE Electron Device Lett. **42** 808 (2021)
- Y. Zhang *et al*. "GaN FinFETs and trigate devices for power and RF applications: review and perspective" Semicond. Sci. Technol. **36** 054001 (2021)

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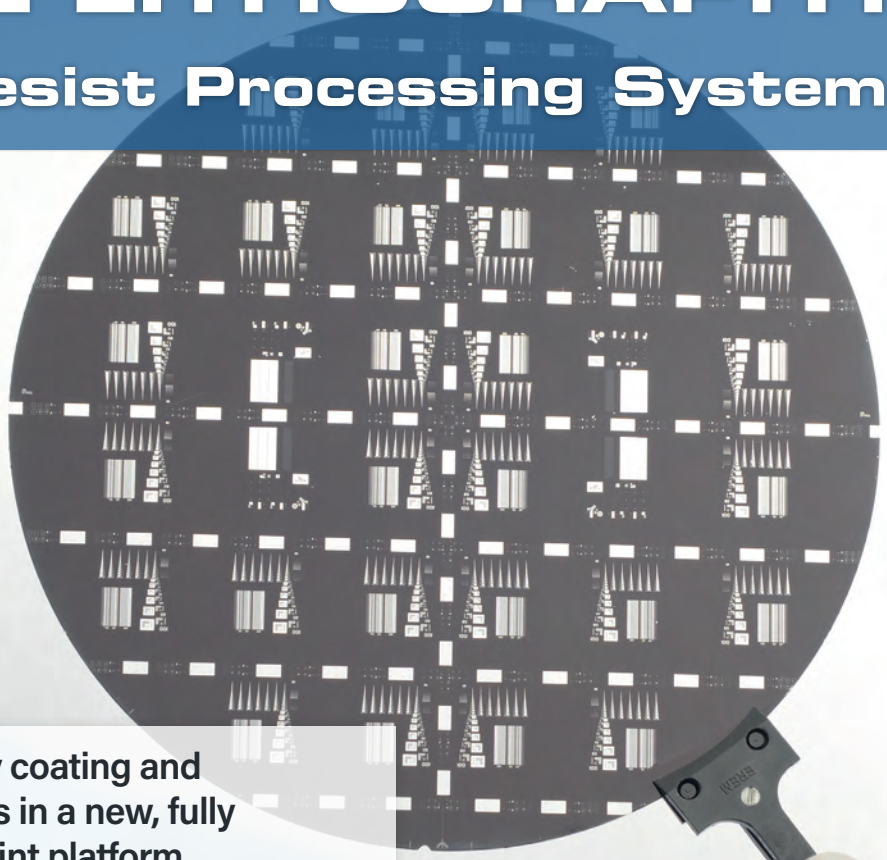

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The allure of cubic SiC

The exceptional electronic and mechanical properties of the cubic form of SiC are enabling this polytype to take rapid strides towards serving in medical devices, MEMS and power electronic applications

BY FRANCESCO LA VIA FROM THE INSTITUTE FOR MICROELECTRONICS AND MICROSYSTEMS

SiC is blessed with many attractive mechanical and electrical properties. Due to these attributes, it is a compelling candidate for making electronic devices and sensors that can be deployed in many settings. Chips made from SiC are strong contenders for deployment in sustainable energy systems, hybrid vehicles, low-power-loss inverters, implantable medical devices, optical devices, and in MEMS operating with high efficiencies at high temperatures.

One of the key considerations facing designers of SiC devices is which form of SiC is best for their target application. This wide bandgap semiconductor exists in nature in a number of crystalline structures, called polytypes, that are differentiated by the stacking sequence of the tetrahedrally bonded Si-C bilayers. Through variations in this stacking sequence, SiC adopts different atomic arrangements and symmetries, from hexagonal to cubic and rhombohedral – each has a different set of physical properties.

Today, the 4H form of SiC grabs the headlines, due to ramping volumes of diodes and MOSFETs for the electric vehicle market. Yet, despite all this success, it is not the best polytype in many important regards. This accolade could go to the cubic form of SiC, which has the highest electron mobility and saturation velocity, thanks to reduced phonon scattering that results from a higher symmetry. Known as 3C-SiC, this cubic polytype has the lowest bandgap – it is just 2.3 eV – and great thermodynamic stability, enabling growth at lower temperatures, such as less than 1500 °C. Unfortunately, thermodynamic stability at lower temperatures is actually a double-edged sword.

Its downside is that it reduces the thermal budget required for growth, thus limiting development of a reliable 3C-SiC bulk growth technology for realization of the seed for subsequent homo-epitaxial growth of device-grade 3C-SiC epilayers. Due to the lack of such a substrate, device developers are forced to grow 3C-SiC hetero-epitaxially on different substrates. Much effort has focused on optimizing the hetero-epitaxial growth of 3C-SiC on the two common hexagonal polytypes, 6H- and 4H-, but manufacturing costs are prohibitively high.

With growth on a native substrate impractical, there is a strong desire from both a technological and a scientific perspective to be able to grow high-quality 3C-SiC epilayers on a substrate with as large an area as possible. Silicon is the obvious candidate: alongside its widespread availability, large sizes and high level of affordability, it can be grown by CVD, ensuring a very high purity of the resulting product.

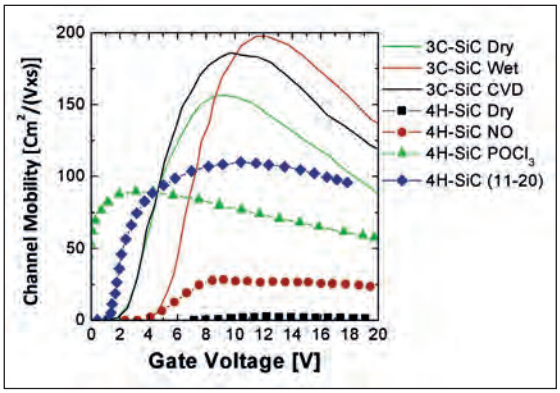
Power devices

The capability of 3C-SiC for making power devices is illustrated in Table 1, which compares the electrical properties of this polytype to those of 4H- and 6H-SiC. Silicon is also included, for the sake of comparison. The excellent characteristics of 3C-SiC have fuelled a persistent interest by the research community – and supported by the power device industry – to develop 3C-SiC devices with breakdown voltages ranging from 600 V to 1.2 kV.

Success would be most welcome. Growth on silicon would open the door to larger wafers and lower-cost production, while devices would benefit from high bulk electron mobilities, due to a higher symmetry within the crystal.

There are reports that channel mobility of 3C-SiC in structures produced with standard processing can reach ten times that of (0001) 4H-SiC (see Figure 1). Combined with the lower bandgap of 3C-SiC, the higher channel mobility should result in a lower value for on-state resistance, thereby reducing conduction losses in a forward-biased MOSFET. According to several device simulations, on-resistance should fall by about a factor of two, enabling a reduction in device area for the same on-resistance, and thus a lower-cost device.

Another attribute of 3C-SiC is its limited concentration of intrinsic carriers – they are about 11 orders of magnitude lower than that found in silicon.



➤ Figure 1. Comparison between the channel mobility in 3C-SiC and 4H-SiC.

This tiny concentration, correlated to the band-gap of 2.3 eV, contributes to a lowering of device leakage current under reverse bias, even in the low- and medium-power regimes.

In addition to these strengths, 3C-SiC has a high thermal conductivity and excellent mechanical properties. These characteristics ensure that sensors and devices based on this polytype are capable of working at temperatures above 250 °C. Operating under such conditions is required for devices that run at very high powers, or in extreme environments, such as those found in hybrid-vehicle engines and aerospace turbine engines.

While there's no doubt that 3C-SiC has much to offer, enabling this material to fulfil its promise is far from easy, due to many challenges associated with the development of high-performance devices. To facilitate marketable production of electronic devices material quality must improve, costs must fall, and there must be a substantial increase in wafer size. The hetero-epitaxy of 3C-SiC on silicon offers an ideal solution to the last two necessities, but if this growth process is to make a real difference to the chances of cubic SiC, there needs to be a fall in the density of crystallographic defects in the epilayer.

These defects stem from the substantial difference in lattice parameters – they differ by 19 percent at room temperature – and the thermal expansion coefficients. For the latter, the difference between 3C-SiC and silicon is 23 percent at the deposition temperatures, and 8 percent at room temperature.

A variety of planar and volume defects originate at the interface between 3C-SiC and silicon. These defects include micro-twins, anti-phase boundaries

Property	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.12	2.35	3.08	3.28
Intrinsic carrier concentration at 300 K (cm^{-3})	0.3	1.5	2.2	2.3
Breakdown field (MV cm^{-1})	1×10^{10}	1.5×10^{-1}	1.6×10^{-6}	5×10^{-9}
Electron mobility ($cm^2 V^{-1} s^{-1}$)	1350	900	370	300
Hole mobility ($cm^2 V^{-1} s^{-1}$)	480	40	80	120
Saturated electron velocity ($\times 10^7$ cm s^{-1})	1	2	2	2
Thermal conductivity (W $cm^{-1} K^{-1}$)	1.5	3.2	4.9	3.7
Dielectric constant	11.7	9.7	9.6	9.6

➤ Table 1. The most relevant electrical properties of silicon, 3C-SiC, 6H-SiC and 4H-SiC.

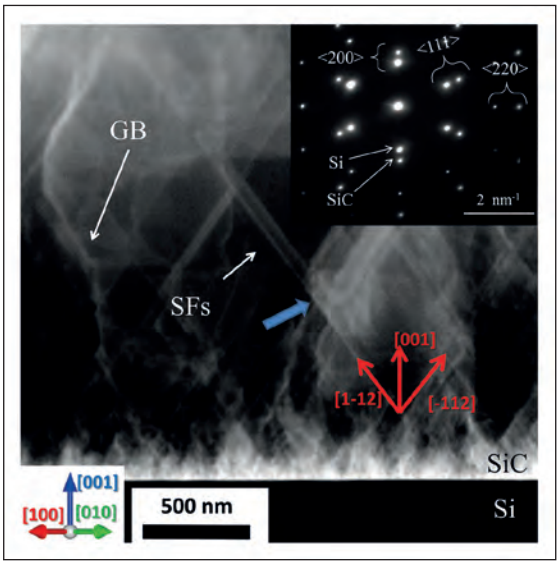


Figure 2. Transmission electron microscopy cross-section of the interface between silicon and 3C-SiC. Several extended defects can be observed.

and stacking faults in the epilayer, and voids in silicon beneath the hetero-interface (see Figure 2). These defects are device killers. However, their threat can be diminished by growing several tens of microns of 3C-SiC. This relatively thick film reduces their density, with some defects totally annihilated. Note that the defect density and the surface morphology strongly depend on the orientation of the silicon substrate.

Over the past three decades much effort has been devoted to developing a process for bulk growth of 3C-SiC. The motivation for this is that in very thick layers it's been observed that the defect density is low enough to enable the realization of power devices.

Working towards this goal is our team from the Institute of Microlectronics and Microsystems at Catania, Italy. We coordinated a four-year project entitled *Challenge*, which has driven the development of three different bulk processes that can produce a breakthrough in power technology. Through collaboration, those of us involved in this European project have developed a process for the bulk growth of 3C-SiC. Seeds of this polytype are formed on silicon (100) substrates that are loaded into a horizontal hot-wall CVD reactor, prior to the growth of epilayers with a thickness of 70 μm. A subsequent increase in temperature beyond the melting point of silicon (see Figure 3 for a temperature profile of the process) causes this substrate to fully melt inside the CVD reactor. The remaining freestanding SiC layer can then be employed as a seed layer for homoepitaxial growth, using a low-pressure regime and different temperatures (between 1600 °C and 1700 °C).

Our team increased substrate thickness with two hours of growth at a rate of 60 μm/h, with the last 10 μm low-doped for device realization. With this approach, using nitrogen and aluminium to form both *n*-type and *p*-type layers, our team produced 3C-SiC homoepitaxial samples with a thickness of about 200 μm, and wafers with diameters of 100 mm and 150 mm (see Figure 3).

Using this methodology, we have reduced the density of stacking faults with respect to thin layers by two orders of magnitude to typically just 10^2 cm^{-1}. Measurements of several *p-n* junctions formed by this approach show reasonable characteristics (see Figure 4). The leakage current of the diodes is still high, so efforts must be directed at a further decrease in the defect density, so that 3C power devices can deliver a competitive performance compared with their 4H cousins in the range of breakdown voltages between 600 V and 1200 V.

Making MEMS

The 3C form of SiC is blessed with very good mechanical properties (see Table 2). They include a high Young's modulus, a high fracture and flexural strength, and a low density. Thanks to the high ratio between Young's modulus and the density, devices made from 3C-SiC have exceptional promise for realizing very robust MEMS that can work at high

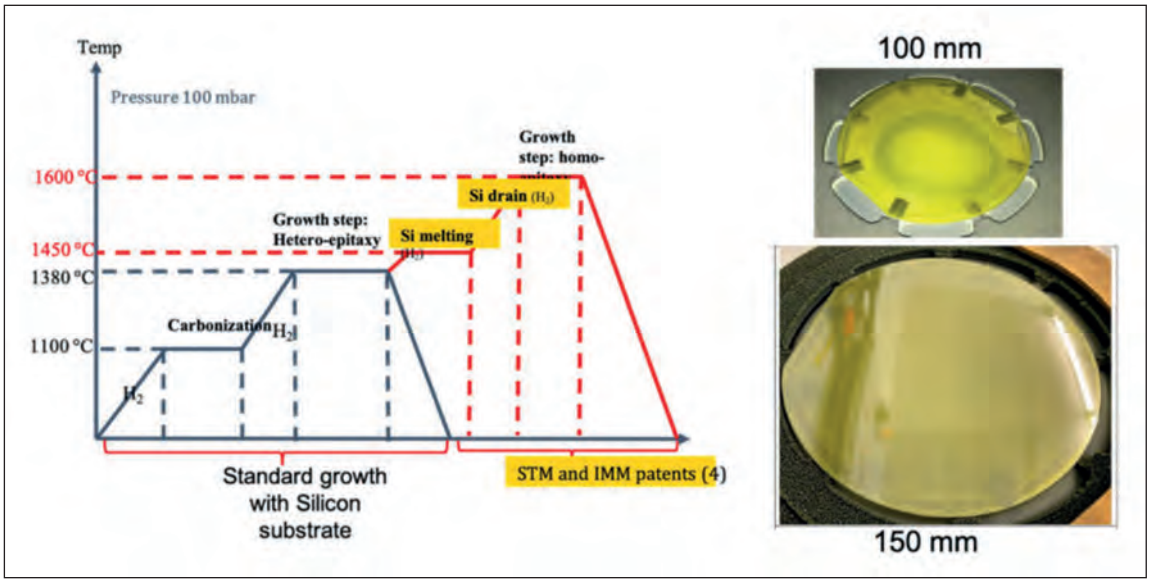


Figure 3. Temperature schematics of the CVD process for the bulk growth of 3C-SiC. 100 mm and a 150 mm wafers are reported too.

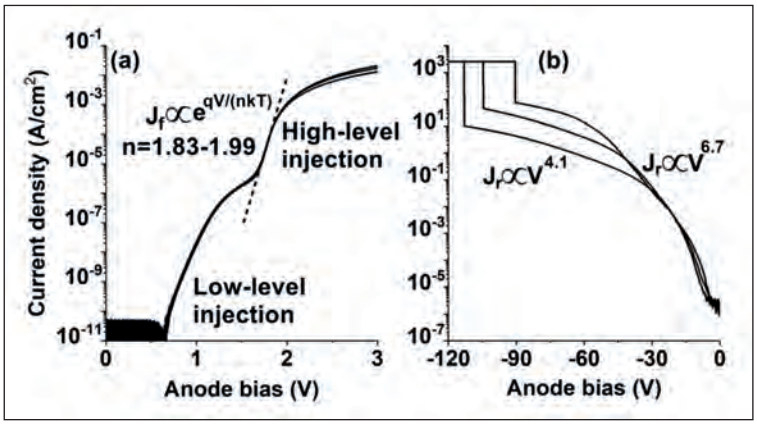
frequencies. What's more, these MEMS can operate at very high temperatures, such as 600 °C, because even in this regime there is not a large reduction in Young's modulus.

Efforts at developing micro- and nano-mechanical resonators have been motivated by the wide range of applications they can serve, both in industry and supporting fundamental science. These resonators can be used for precision sensing of mass, and to measure ultrasound, magnetic fields, inertia and strain. For many of these applications it is essential to realise a high resonator quality factor.

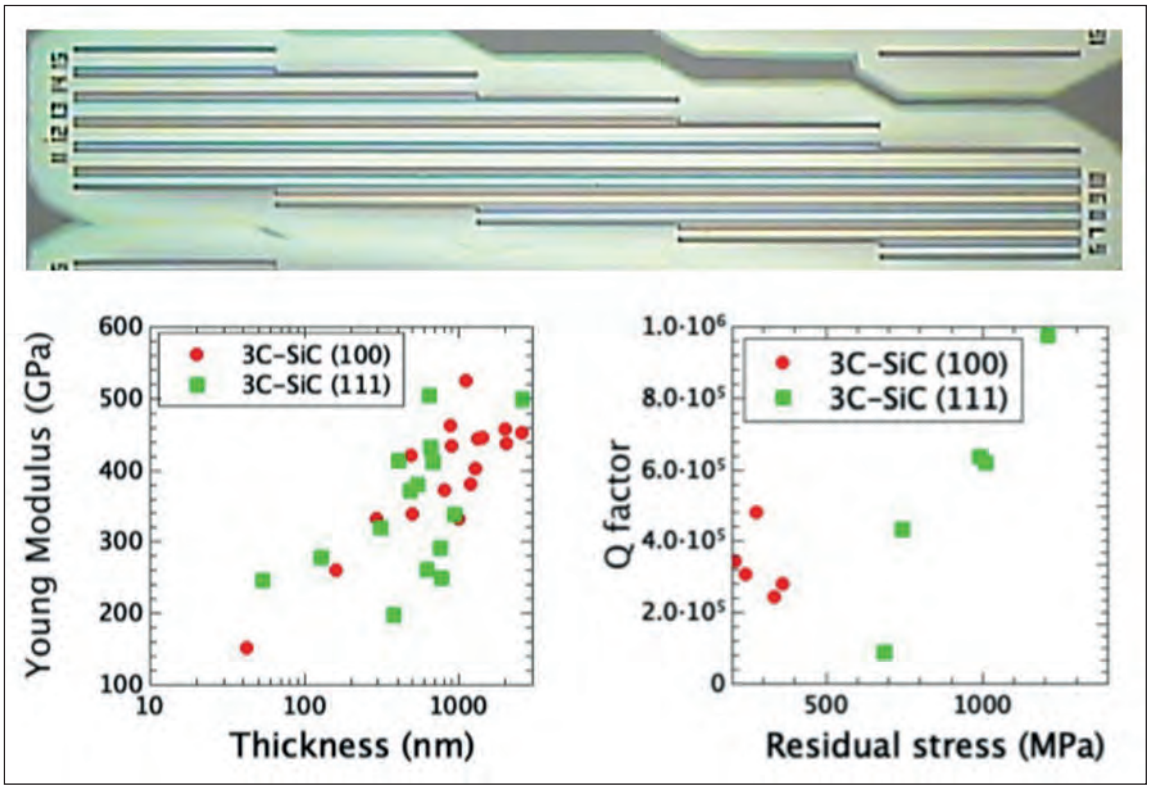
Recently, remarkable progress has been made in improving the quality factor of micro- and nano-mechanical resonators that are fabricated from highly stressed, thin amorphous films – most particularly amorphous SiN – formed on a silicon substrate. Further progress is possible by switching from these amorphous films to crystalline materials, which offer a range of advantages that could deliver a step-change in performance.

One of the merits of high-purity crystalline materials is their comparatively low defect density that allows significantly higher intrinsic quality factors. Values for this figure-of-merit of above 10^5 have been reported for highly pure diamond, CaF, and 3C-SiC – and when surface losses are eliminated, quality factors can exceed 10^6. This value far exceeds the quality factor of 25,000 for amorphous SiN and 1,000 for amorphous silicon. What's more, crystal-lattice mismatch is a benefit rather than a curse, as crystalline material with a high intrinsic stress is better suited to dissipation dilution.

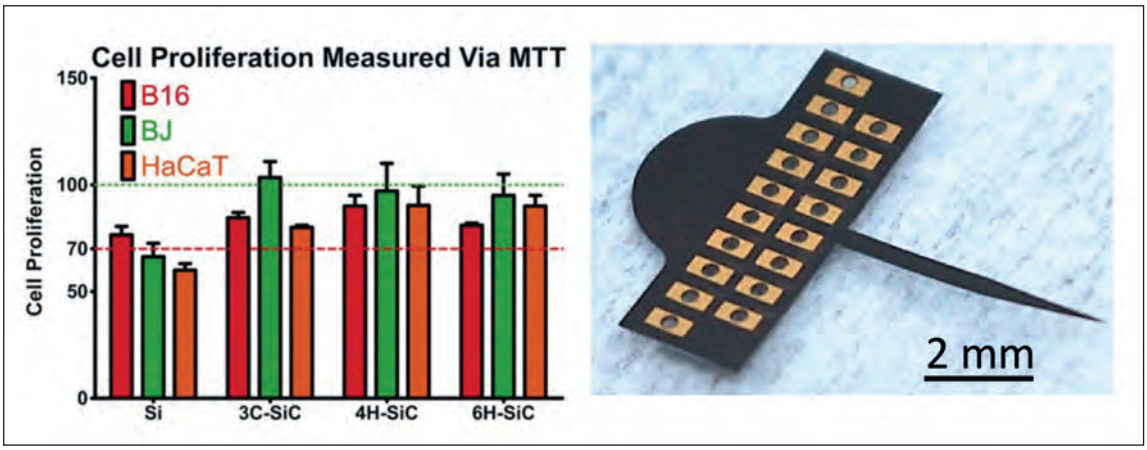
Yet despite these significant advantages, thin-film crystalline resonators are still to demonstrate the dramatic improvements in quality that have been shown in their amorphous counterparts. Progress is partly impaired by the increased complexity of fabrication, and – when grown on a silicon substrate – the dislocations and the high density of stacking faults near the interface. These imperfections degrade the mechanical quality factor and the Young's modulus.



➤ Figure 4. Forward (a) and reverse (b) characteristics of 3C-SiC p^+/n junctions on a bulk wafer grown by CVD. While the forward characteristics are almost ideal, the reverse show a high leakage current, due to the high defect density.



➤ Figure 5. (up) Double clamp beam array with different lengths and widths. (left) An increase in the Young's modulus with increasing thickness is observed in both (100) and (111) 3C-SiC. (right) The Q-factor increase at high residual stress is essentially in (111) 3C-SiC. In (100) 3C-SiC, the residual stress is lower, as is the Q-factor.



➤ Figure 6. (left) Cell proliferation for silicon and SiC. (right) A SiC neural probe.

In the last few years much progress has been made with 3C-SiC MEMS, due to developments in the growth process, in processing and in design. Several projects have reported success, including one we have coordinated called *SiC nano for picoGeo*. By addressing many of the potential pitfalls, this European effort has realised extremely good materials properties, even for films with a thickness close to 1 µm (see Figure 5, left).

Our measurements of the Q factor in structures with identical dimensions and design show that for the (111) form of 3C-SiC there is a clear linear dependence on residual stress, while this dependence is not clear for the (100) variant. Due to this characteristic, we are able to produce very efficient resonators, extremely sensitive strain meters and other high-performing MEMS devices with (111) 3C-SiC.

In the *SiC nano for picoGeo* project our team has produced a very sensitive strain meter, capable of detecting in the 10^{-12} -10^{-13} range. Such a high degree of sensitivity enables this sensor to detect very small deformations that occur a few hours before the eruption of a volcano or before an earthquake. These strain meters could also measure the deformation of a dam or a bridge.

It's worth noting that when 3C-SiC is used to make MEMS, only a thin layer of this material is needed, due to its good mechanical characteristics. Thanks to this, the fabrication process is quite easy, as it involves etching a thin layer of SiC, prior to a deeper etch of the silicon substrate, which can be accomplished using the standard process for silicon MEMS.

Implantable medical devices

Another important application where 3C-SiC can make a valuable contribution is in implantable medical devices. Silicon is highly toxic, leading researchers to pursue new classes of composite semiconductors, such as 3C-SiC, that offer a healthier solution. Experimental work by several groups suggests that SiC is extremely biocompatible, and is a good choice for this kind of device (see Figure 6, left).

Within the family of SiC poltypes, 3C-SiC appears to be a better option than its hexagonal siblings, because it enables the realization of thin implantable devices by etching the silicon substrate. This approach has enabled the fabrication of a neural probe (see Figure 6, right).

This work is in its infancy, and there are still issues to overcome. The biggest of these is the high leakage current from the junctions used to isolate the device from the substrate. Once this problem is overcome, 3C-SiC could be used to produce neural probes for the medical sector.

The cubic form of SiC clearly has much promise for power devices, MEMS and medical devices. Over the last few years much progress has been made in improving the structural quality of this material so that it can begin to fulfil its potential for delivering an outstanding performance. Thanks to these advances, it's not long before we could start to see the first commercial 3C-SiC devices on the market.

➤ Table 2. Physical properties of silicon, SiC and diamond.

Property	Si	SiC	Diamond
Lattice constant (A)	5.43	4.35	3.57
Cohesive energy (eV)	4.64	6.34	7.36
Young's modulus (GPa)	130	450	1200
Shear modulus (GPa)	80	149	577
Hardness (kg mm^{-2})	1000	3500	10000
Fracture strength (GPa)	1	5.2	5.3
Flexural strength (MPa)	127.6	670	2944
Friction coefficient	0.4-0.6	0.2-0.5	0.01-0.04
Relative wear life	1		10000

FURTHER READING

- http://h2020challenge.eu/
- http://picogeo.eu/

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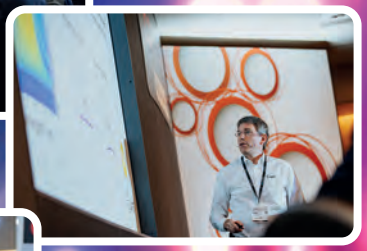


The glorious gate oxide

Should one worry about the lifetime of the gate oxide of SiC power MOSFETs under negative gate stress? Absolutely not, now that experiments show that they last as long as they do under a positive gate stress

BY SATYAKI GANGULY, BRETT HULL, DANIEL LICHTENWALNER AND JOHN PALMOUR FROM WOLFSPEED

➤ Top: The world's first 200 mm SiC wafer fabrication facility, located in Mohawk Valley, NY.

ONE OF THE GREATEST strengths of the 4H form of SiC is an electric breakdown field that is around ten times that of silicon. This means that for a given voltage rating, SiC power devices can feature a thinner drift region and higher doping than their silicon counterparts. In turn, this allows SiC power devices to have a far lower on-resistance (see Figure 1) and a simple unipolar MOSFET structure – there's no need for complex architectures, involving super-junctions or bipolar conduction. On top of this, SiC power devices have low leakage currents at relatively high temperatures, and a high thermal conductivity that supports higher current densities, enabled by the low on-resistance.

Drawing on all these attributes, SiC MOSFETs have demonstrated clear-cut advantages over other material systems, in terms of power density, efficiency, switching speed and thermal management. So significant are these gains that if every data centre on Earth used SiC instead of the incumbent, silicon, Manhattan could be powered for an entire year by the energy savings provided by this wide bandgap material.

The success story of SiC power devices dates back to just after the turn of the millennium. One of the key milestones came in 2002, when our company, Wolfspeed, released its first commercial 600 V junction-barrier Schottky diode. In 2011 we followed this up with the launch of the industry's first SiC MOSFET, rated at 1200 V; and within a further three years we had introduced the world's first 1700 V SiC half-bridge module.

More recently we have been grabbing the headlines for our efforts at increasing production capacity. This April we opened the world's first 200 mm SiC wafer fabrication facility, heralding the electrifying present and future of SiC power devices.

We are not alone in producing SiC power devices, which are finding deployment in automotive, renewable energy, power supply, and industrial applications. Setting us apart from our peers is the broadest commercial portfolio, which currently includes SiC MOSFETs and Schottky diodes in both discrete package and bare die form, as well as power modules. Our SiC MOSFETs scale from 650 V to 1700 V, with on-resistances ranging from 10-1000 mΩ; and our family of Schottky diodes span 600 V to 1700 V, with a best-in-class forward-voltage drop that trims conduction losses and boosts overall system efficiency. We continue to diversify, recently introducing 650 V Schottky diodes in a compact QFN 8 mm by 8 mm package, and 650 V MOSFETs in a TO lead-less package that have a footprint 60 percent smaller than the through-hole packages on the market today. Another breakthrough has been the introduction of our E-Series family of

power devices: they are automotive qualified, humidity robust, and optimized for on-board automotive charger, DC/DC converter and drivetrain applications, as well as PV inverters. This launch has further bolstered our reputation for SiC devices in the automotive market space.

Evaluating reliability

SiC power devices offer a level of reliability that is already excellent and on an upward trajectory, thanks to continual advancements in SiC substrate quality, epitaxial growth capabilities and device processing. However, harsh operating conditions, combined with ever demanding and evolving market requirements, are driving gate oxide reliability requirements for SiC power devices ever higher.

There are two key aspects to gate oxide reliability: threshold voltage stability and gate oxide lifetime. Nobel-prize-winning physicist Herbert Kroemer once famously remarked that the 'Interface is the device', and rightly so. Owing to differences between SiC and silicon MOS interfaces, SiC gate oxide reliability has always been carefully scrutinized, and judged against the gate oxide reliability of silicon devices.

The threshold voltage stability for the SiC MOSFET is, in general, similar to that for its silicon sibling. However, there are fundamental differences between the two material systems. They include smaller conduction band and valence band offsets between the 4H polytype of SiC and SiO_2, compared with silicon and SiO_2; the higher interface trap density for the 4H-SiC MOS device; and a difference in the interface chemistry – a nitrided gate oxide is employed for SiC, and hydrogen passivation for the SiO_2/silicon interface. Due to all these differences, it is likely that threshold voltage shift mechanisms could differ between SiC and silicon MOS devices.

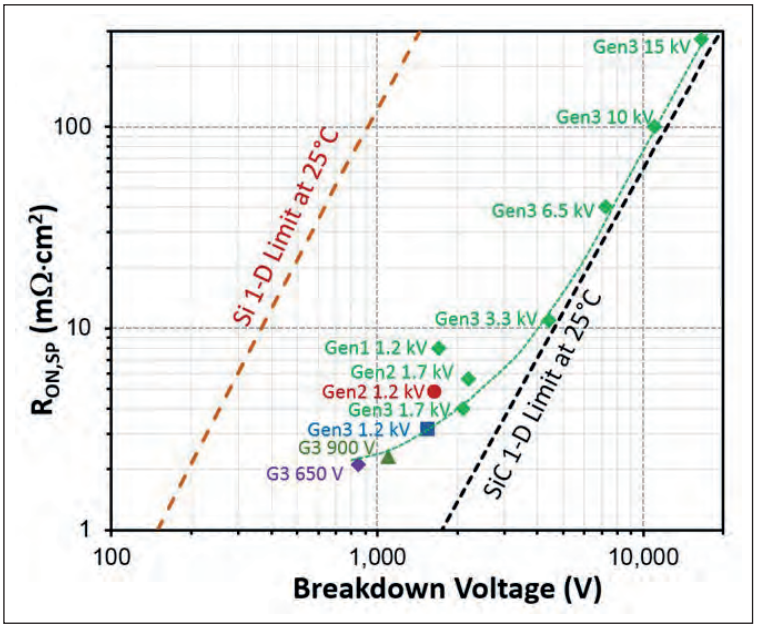
Within the wide bandgap community, much effort has been devoted to uncovering the mechanisms behind the observed shifts in the threshold voltage of SiC MOSFETs, using bias-temperature instability tests. These investigations have considered both positive and negative gate biases, and demonstrated threshold stability, alongside long-term reliability for practical applications.

The second part of gate oxide reliability, which is gate oxide lifetime, has also been carefully studied for SiC MOS devices. Our company has reported an attractive median time-to-fail gate oxide lifetime of 10,000 years at 175 °C and at a gate oxide electric field of about 4 MV/cm for *n*-channel SiC power MOSFETs through both constant and ramped positive gate bias time-dependent dielectric breakdown studies.

For silicon MOSFETs, the time-dependent dielectric breakdown is arguably one of the most well characterized and cited failure mechanisms of all time. While several models exist, for SiC the majority of researchers use the linear thermochemical electric field model to explain the time-dependent dielectric breakdown. This tends to provide the most conservative estimation. Of the two more common alternatives, the model that considers the inverse of the electric field gives extremely optimistic intrinsic lifetime extrapolations, so its validity is questionable; and the model based on a power-law governed by voltage is unsuitable, because it's been developed for ultra-thin gate oxides. Due to these issues, it's hardly surprising that the linear electric field model is widely used for SiC. This model assumes that a positive gate voltage results in the tunnelling of carriers, which create defects in the oxide film. When these defects reach a critical point, they initiate dielectric breakdown at that local weak point.

Evaluating negative bias

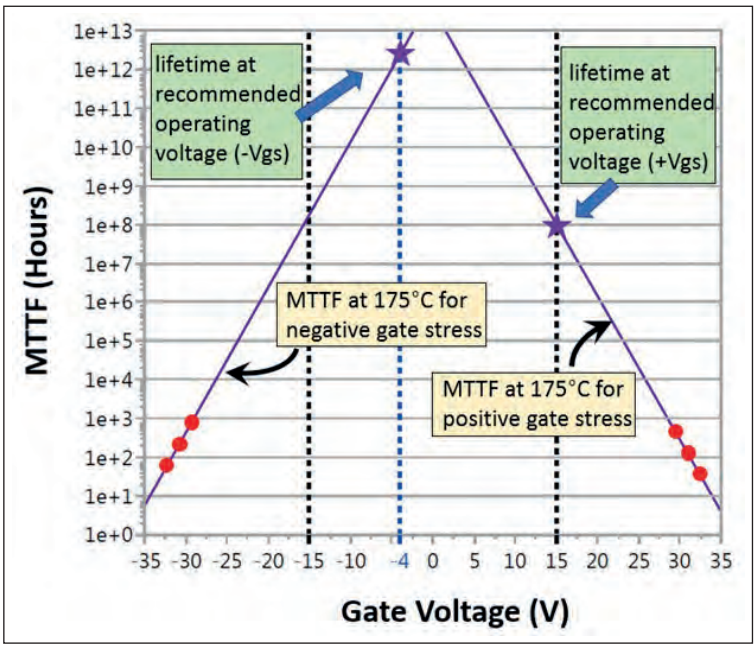
The curious reader may have noticed that while the SiC community's discussions on the threshold voltage stability encompass both positive and negative gate biases, when it comes to gate oxide lifetime, the focuses is on the positive gate bias stress for *n*-channel SiC MOSFETs. That limitation occurs because, until our recent efforts, there has been little to no work published on the gate oxide lifetime under negative gate bias for SiC MOSFETs. This is surely a significant omission, given that to turn these enhancement mode *n*-channel devices off, the channel is shut down by taking the gate bias well below the gate threshold voltage, and at



➤ Figure 1. Unipolar one-dimensional specific semiconductor drift on-resistance ($R_{ON,SP}$ in mΩ-cm²) versus breakdown voltage. Dashed orange and black lines show the theoretical limits at room temperature (RT) for silicon and SiC respectively. The RT data points represent various generations and voltage ratings of Wolfspeed SiC MOSFETs, and the green dashed line is a guide to the eye for that data. Adapted from J. W. Palmour et al., Proceedings of the 26th International Symposium on Power Semiconductor Devices & IC's, June 15-19, 2014.

least down to 0 V. From a blocking perspective, devices have no trouble realising this at 0 V gate bias. However, during turn-off, device performance improves by applying a gate bias well below 0 V. Turning MOSFETs off with a negative gate bias trims the turn-off energy loss by increasing the gate current during the turn-off transients – in turn, this forces the gate capacitance to discharge quicker than if turned off using a 0 V bias. Another point to consider is that in systems that employ multiple devices in either a parallel or a bridge configuration, devices tend to be turned off with a negative gate bias. This approach is employed because it provides further protection against parasitic turn-on, which can occur with unbalanced transients across multiple chips in a system. The importance of negative gate bias, and subsequently the necessity of gate oxide lifetime study of SiC power devices under such bias condition, certainly calls for careful investigation thus far overlooked.

To improve the understanding of the gate oxide reliability of SiC MOSFETs under a negative gate bias, we have performed constant voltage time-dependent dielectric breakdown testing on our Gen3 1200 V discrete MOSFETs at 175 °C, with applied negative gate biases much higher than the maximum recommended operating gate voltage of -4 V. Keeping source and drain at ground potential, we evaluated around 30 devices at these three gate stress voltages: -29.5 V, -31 V and -32.5 V. We monitored the gate leakage current of each device individually, which enabled us to collect the individual failure times of the stressed devices during these accelerated tests. For a true comparison, we also performed a positive gate bias time-dependent dielectric breakdown study with gate stress voltages of +29.5 V, +31 V and +32.5 V on Gen3 1200 V devices, using an identical sample size to that of the negative bias case.



➤ Figure 2. Wolfspeed Gen3 MOSFET time-dependent dielectric breakdown (TDDB) median-time-to-failure (MTTF) versus gate stress voltage at 175 °C. Red data points represent the extracted MTTF values at the gate stress voltages tested, while solid lines are the fit and extrapolation as described in the text. Stars represent fiducial points to illustrate the predicted MTTF lifetime at the recommended operating gate voltage stress condition (both positive and negative). Adapted from S. Ganguly *et al.*, IEEE International Reliability Physics Symposium (IRPS), pp. 8B.1-1-8B.1-6, 2022.

We found that the failure times for each of the stress conditions followed a well-behaved Weibull distribution. The extracted value for a characteristic that's referred to as Weibull β – it's known as the shape parameter, and it represents failure rate behaviour – is well above 2, indicating an intrinsic wear-out failure mechanism under both positive and negative gate stress. As we found similar failure time distributions and values for Weibull β, we were able to conclude that it is likely that there are similar failure mechanisms under both positive and negative gate biases.

Drawing on the Weibull failure time distribution, the linear electric field acceleration model and the maximum likelihood estimation, we extracted values for the median time to fail and extrapolated the lifetime. We found that the lifetime for the gate oxide is nearly identical for positive and negative bias, with a median time to fail of around 10,000 years (this is for conditions of 175 °C and a gate stress at -15/+15 V, which corresponds to a gate oxide electric field of about 4 MV/cm). We wish to point out that as the recommended negative gate-source voltage of -4 V for a MOSFET to turn-off the channel is generally much lower than the recommended positive gate-source value of +15 V during on-state, the oxide lifetime during the off-state should be much longer than it is during on-state operation (see Figure 2).

At this point, while you may be impressed by the stellar SiC MOSFET gate oxide lifetime under negative gate bias, you might be wondering what is the physical explanation behind this observation. Let us try to explain in a little detail. As we have already mentioned, tunnelling is to blame for the time-dependent dielectric breakdown of the gate, with breakdown occurring once defect accumulation reaches a critical point. It follows that if the levels of current flow under positive and negative gate bias are similar, so will be the extent of damage occurring in the gate oxide, and thus the resulting gate oxide lifetime. This view is credible, given that electrons under positive gate bias see an energy barrier of around 2.8 eV, and holes under negative gate bias see an energy barrier of 2.9 eV. Further support for this view comes from our TCAD simulations and electrical measurements. They show that the similar barrier heights lead to a similar level of Fowler-Nordheim tunnelling current flow under both positive and negative gate biases, thus accounting for the similarity in gate oxide lifetime in the two cases.

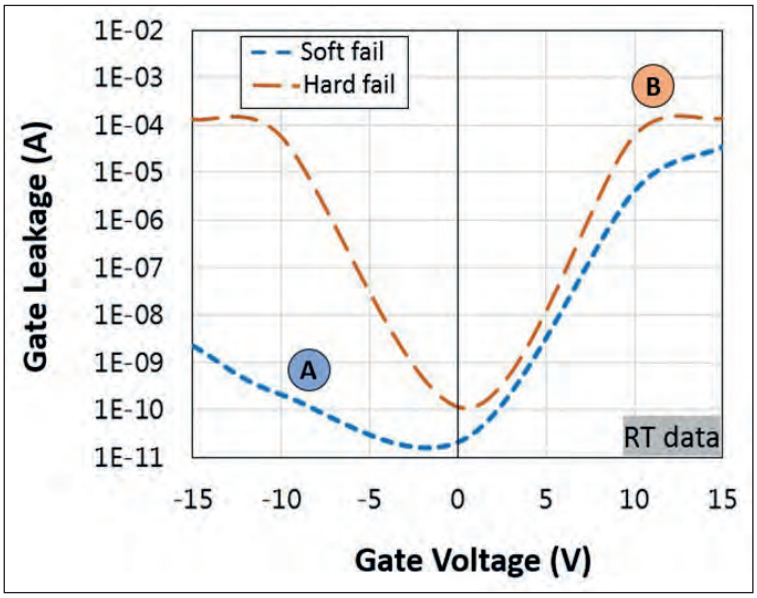
We have also established a correlation between the failure locations in a MOSFET unit cell and the failure signatures during time-dependent dielectric breakdown stress. The gate leakage profiles from the time-dependent dielectric breakdown stress under a negative bias show two distinct failure signatures – a soft fail, 'A', and a hard fail, 'B' – under all three stress voltages (-29.5 V, -31 V, and -32.5 V). We found that the post-failure leakage in type 'A' devices is orders of magnitude lower than it is in type 'B' failed devices.

As part of this study, we have measured the room-temperature gate leakage current at a range of gate voltages (see Figure 3), for failing devices with differing *in-situ* leakage signatures. When applying a positive gate voltage sweep, we found that the 'A'-type and 'B'-type devices had very similar, high current levels of more than 10 μA at gate-source voltage of 15 V. But when we swept with a range of negative gate voltages, results differed markedly. The 'soft' fail devices, which we've labelled type 'A', exhibited a current that's lower by orders of magnitude than the type-'B' devices, which encountered hard failure. This observation is consistent with *in-situ* data recorded at a higher bias and temperature during the time-dependent dielectric breakdown stress.

Our next step involved trying to determine whether the different electrical failure signatures – that is, the type 'A' and the type 'B' devices – have any degree of correlation with the failure locations in a MOSFET unit cell. To see whether this is the case, we undertook physical failure analysis, involving thermal imaging followed by focused ion-beam cross-section and scanning-electron microscopy imaging. These forms of microscopy were performed on multiple failed devices that have the two different failure types.

Inspecting these devices revealed that the subset with a soft fail ('A'-type) signature had a gate oxide rupture in the JFET gap of the MOSFET (see Figure 4(a)). On the other hand, those with the hard fail ('B'-type) signature had a gate oxide rupture in the n^+/*p*-well area of the MOSFET (see Figure 4 (b)). This is not just a mere coincidence: it is repeatable across many devices, and it can be explained by considering the energy band diagram of the poly-SiO_2-SiC interface.

Enthusiastic readers can find a detailed account of our explanation in a paper published earlier this year (for details, see 'Further Reading'). Here, we offer

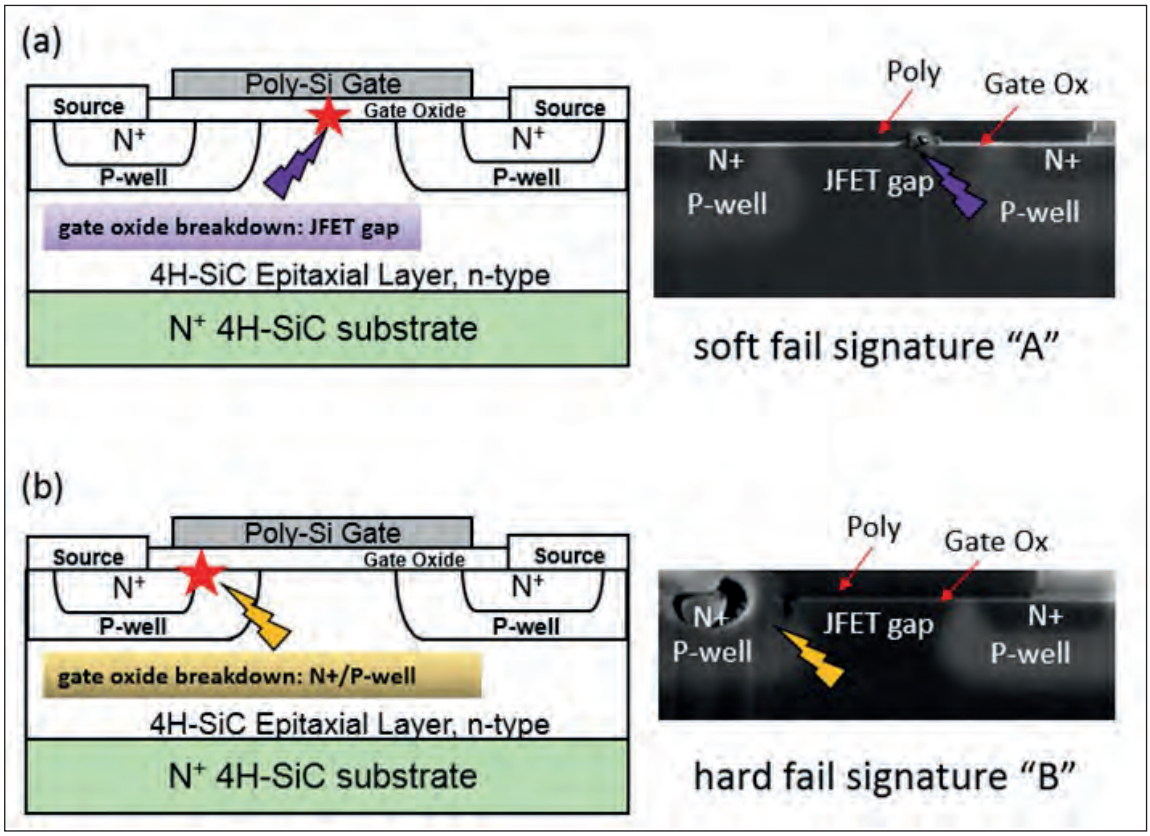


➤ Figure 3. Post time-dependent dielectric breakdown negative gate stress failure, at room-temperature. Typical gate leakage versus gate voltage current sweep data for devices with two distinct failure signatures ('A': soft fail, 'B': hard fail). During positive sweep ($V_{GS} > 0$) leakage levels are similar in 'A' and 'B', whereas during negative sweep ($V_{GS} < 0$) the leakage level of 'B' is orders of magnitude higher than 'A'. Adapted from S. Ganguly et al., IEEE International Reliability Physics Symposium (IRPS), pp. 8B.1-1-8B.1-6, 2022.

a simpler alternative. It is our view that during the time-dependent dielectric breakdown stress, if there are gate oxide ruptures in the SiO_2, the likelihood is that this will convert the poly-SiO_2-SiC interface to essentially a Schottky junction. For the poly-SiO_2-SiC that sits over the *p*-well, the majority-carrier holes will accumulate there under a large negative gate bias. Meanwhile, for the poly-SiO_2-SiC over the n^+ source, the abundance of the majority-carrier electrons will remain, even under a negative gate bias. It's a different state of affairs, though, when the rupture takes place in the low-doped *n*-type SiC JFET gap region. In this case, electrons will deplete under a similar bias condition. This is consistent with our electrical measurements – and offers an explanation of why there is a much higher current under large negative gate bias when the gate oxide breakdown occurs in the n^+ or *p*-well region, than when the rupture occurs in the depleted *n*-type SiC JFET gap.

For the ruptured areas under positive bias, current flow will always be high under positive bias,

Our work shows that the gate oxide lifetime extracted from our devices under normal operating and accelerated negative gate bias conditions is a very close match to that extracted from positive gate stresses



➤ Figure 4. Schematic cross section as well as focused ion beam, cross-sectioned scanning electron microscopy images, showing gate oxide rupture after negative gate bias time-dependent dielectric breakdown (TDDB): (a) in the JFET gap for the type 'A' soft-fail electrical signature, (b) the n^+/p-well for the type 'B' hard-fail electrical signature. Adapted from S. Ganguly et al., IEEE International Reliability Physics Symposium (IRPS), pp. 8B.1-1-8B.1-6, 2022.

because electron accumulation can take place at the n^+ source and at the *n*-type SiC JFET gap region. In the case of failures above the *p*-well, even though majority carrier holes will be depleted at the *p*-well and poly(/SiO_2) interface under a positive bias, there is still a high current due to inversion electrons in the *p*-well. So, regardless of whether the gate oxide rupture take place in the *n*-type JFET, the *p*-well or n^+ area, the resultant gate current level will remain high under positive gate bias.

Our work shows that the gate oxide lifetime extracted from our devices under normal operating and accelerated negative gate bias conditions is a very close match to that extracted from positive gate stresses. This work should help alleviate any concerns regarding the gate oxide lifetime and failure mode under hole transport, rather than conventional electron transport. While our investigation considers a planar MOSFET design, it is possible that similar observations hold for other cell designs, such as those employing a trench. However, experimental verification is required before any claims can be made. Another key finding from our investigations is that the different electrical failure signatures that exist under negative gate time-dependent dielectric breakdown stress correlate with failure locations in a MOSFET unit cell. This observation promises to aid the early phase of any new process development, as it will allow the failure location to be identified from gate leakage data, without the need for physical failure analysis. We hope this insight, as well as others provided by our study, will help the SiC world to power up even more!

FURTHER READING

➤ A.J. Lelis *et al.* "Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs," IEEE Trans. Electron Dev. **62** 316 (2015)

➤ D.J. Lichtenwalner *et al.* "Reliability Studies of SiC Vertical Power MOSFETs," IEEE International Reliability Physics Symposium (IRPS) 2B.2-1–2B.2-6 (2018)

➤ J. McPherson *et al.* "Comparison of E and 1/E TDDB models for SiO_2 under long-term/low-field test conditions," IEDM 171 (1998)

➤ S. Ganguly *et al.* 1998 "Negative Gate Bias TDDB evaluation of *n*-Channel SiC Vertical Power MOSFETs," IEEE International Reliability Physics Symposium (IRPS) 8B.1-1-8B.1-6 (2022)

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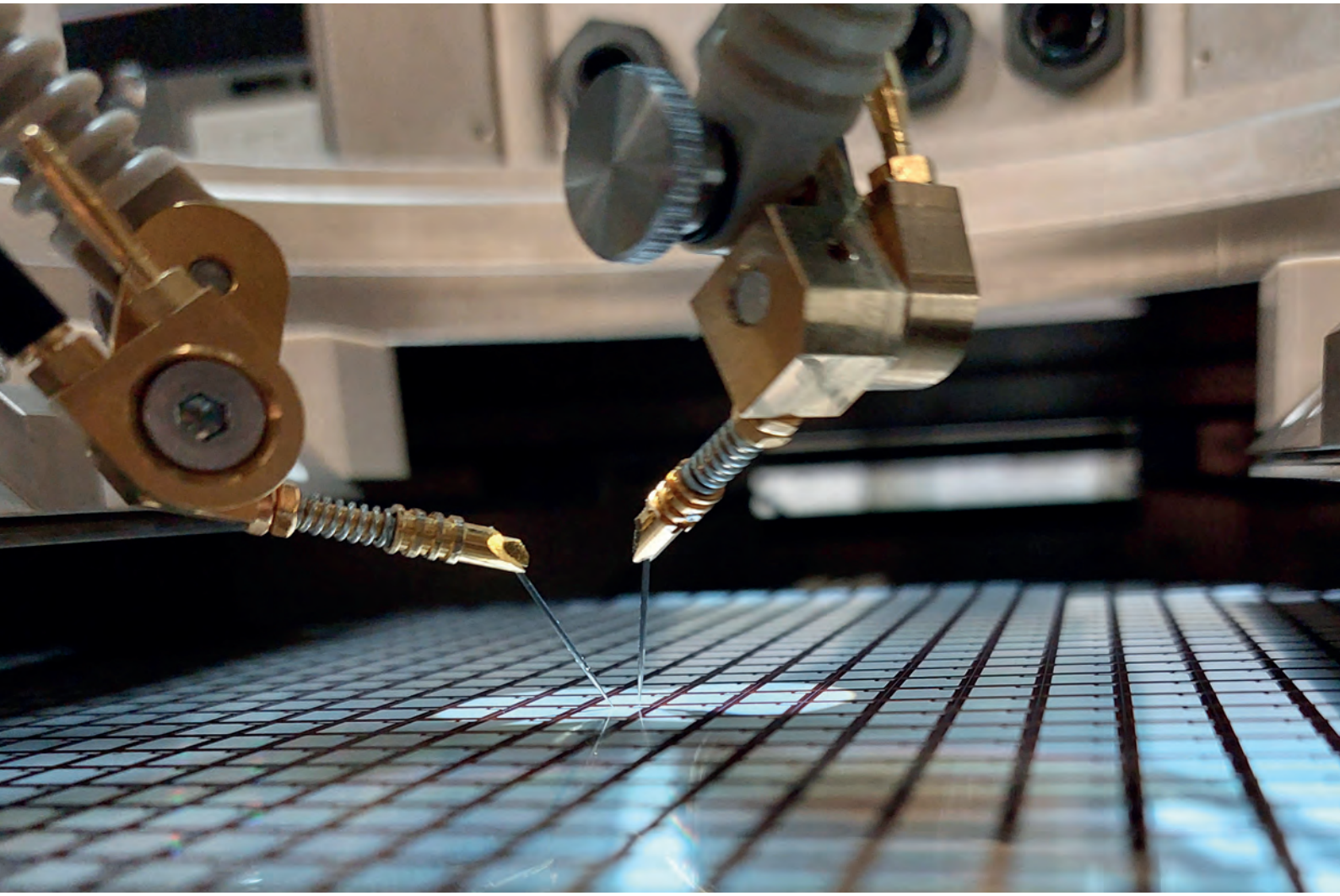


Cubic SiC: Tomorrow's champion for power electronics?

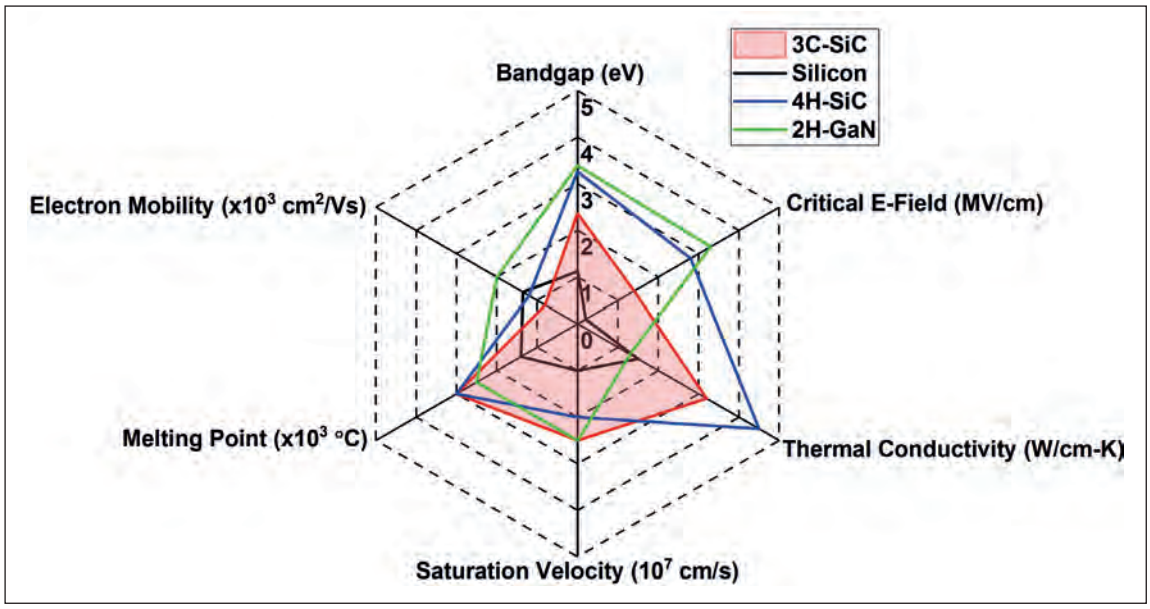
Offering the same crystal structure as silicon, alongside a wider bandgap and the potential for high reliability, what's to stop cubic SiC from playing a major role in tomorrow's power electronics industry?

BY MIKE JENNINGS FROM SWANSEA UNIVERSITY

THE UPTAKE of the Tesla is welcome on many fronts. Its lack of a combustion engine helps to trim carbon emissions; it is relatively quiet, thanks to battery power; and, much closer to home for those within the compound semiconductor industry, its early adoption of SiC power electronics is driving sales of these devices.

Where Tesla leads, other makers of electric vehicles are sure to follow. They too will employ SiC devices in their power trains, swelling sales of these wide-bandgap devices. Demand is tipped to be so strong that four of the leading makers of these chips – Wolfspeed, Infineon, STMicroelectronics and onsemi – are forecasting annual sales from this class of device to top $1 billion by the middle of this decade. Given the phenomenal success that SiC power devices are set to enjoy, one would presume that they are free from flaws. But that's not actually the case. There are, in fact, significant concerns relating to reliability, centred around the gate oxide.

The predominant role that SiC power devices have in electric vehicles is to convert the output from the battery, which is typically 800 V DC, to an AC form that drives a motor – producing up to 200



➤ Figure 1: Electrical and material properties radar chart of cubic SiC versus silicon and other commercial wide bandgap materials. This chart presents major semiconductor material parameters for power electronics applications.

kW or so of power. The voltage requirement is not particularly testing, as its well within the range of most conventional 4H-SiC devices, which span 650 V to 1.7 kV.

There are concerns surrounding the gate oxide because, like its silicon counterparts, the 4H-SiC transistor is based on a vertical MOSFET design. With this architecture failure of the gate oxide at elevated temperatures is a primary weakness. This is not that surprising, as the gate oxide used in this form of MOSFET is much thinner than its silicon equivalent, in order to maintain an acceptably low threshold voltage. Unfortunately, two unwanted consequences result from this thinner oxide: increased importance of the oxide-semiconductor interface, and an electric field inherent within the oxide that is typically two-and-a-half times that at the SiC surface.

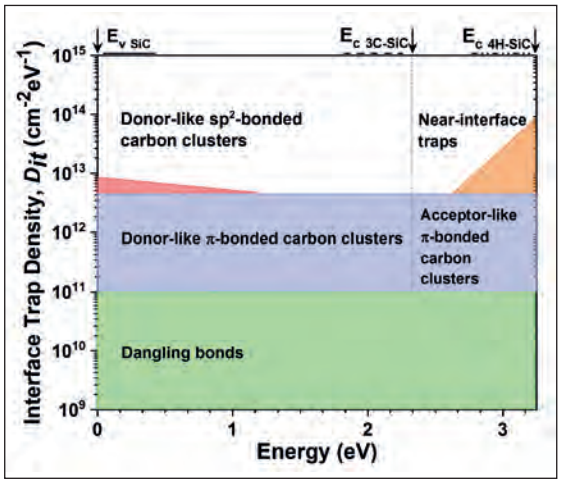
Both these issues are particularly troublesome in trench MOSFET architectures, because they are exacerbated by the trench corner. To counter this, those designing the latest trench MOSFET devices derate their blocking voltage capability to protect the fragile gate oxide.

Another option for addressing concerns related to reliability is to mirror the approach that's taken with GaN devices. Taking this tact has led some designers to advocate cascode co-packaged devices, such as the pairing of a 4H-SiC JFET with a silicon MOSFET. But this combination constrains performance, particularly at high temperatures.

Cubic SiC: a bastion for longevity

Enter cubic SiC, also known as 3C-SiC – an exciting material that promises to be 'Mr Reliable'! There's still much work to do with this polytype, as wafers and epitaxial layers are at a very early stage and hence, defective. However, massive strides in bulk material and the growth of 3C-SiC on silicon have been recently accomplished – they are detailed in the previous edition of this magazine by Francesco La Via from the Institute of Microelectronics and Microsystems at Catania, Italy.

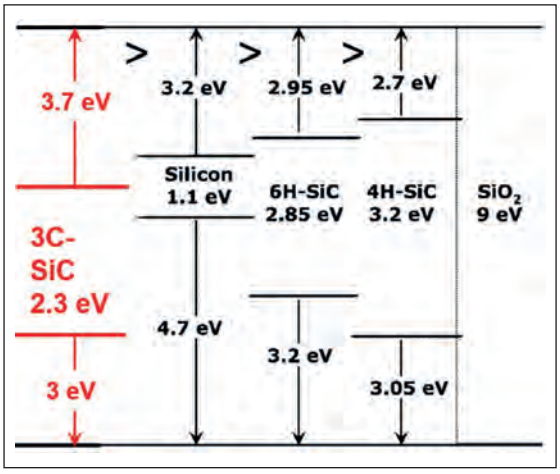
You may be wondering why so much excitement surrounds 3C-SiC. After all, compared with GaN and 4H-SiC it has a lower bandgap, a smaller critical electric field, a modest electron mobility and a low thermal conductivity (see Figure 1). Surely, this shows that 3C-SiC is inferior to those two wide bandgap titans, GaN and 4H-SiC.



➤ Figure 2: Interface trap density plot comparing cubic (3C-) SiC to commercial (4H-) SiC. 3C-SiC shows a favourable (or much reduced) trap density due to the absence of near-interface traps prevalent within the 4H- system. This is a plot is modified from R. Esteve, "Fabrication and Characterization of 3C- and 4H-SiC MOSFETs," Doctoral thesis, KTH Royal Institute of Technology, Stockholm, 2011.

While all of these pointers are valid, they overlook two crucial factors that are not covered within tables listing the properties of semiconducting materials: processing, including the quality of the interface, which may involve a metal or insulator; and reliability in the field. These are considerations that clearly matter. After all, what good is a wide bandgap material if it cannot be used to make a device, or one that only lasts for a single switching cycle.

Of course, these concerns don't apply to commercial 4H-SiC and GaN – but processing of these materials, particularly GaN, is radically different and more challenging than it is for traditional silicon. In comparison, 3C-SiC, with its cubic nature and a humble energy bandgap of 2.36 eV, is closer to silicon than the other members of the wide bandgap family. These traits offer many benefits when it comes to processing 3C-SiC into devices.



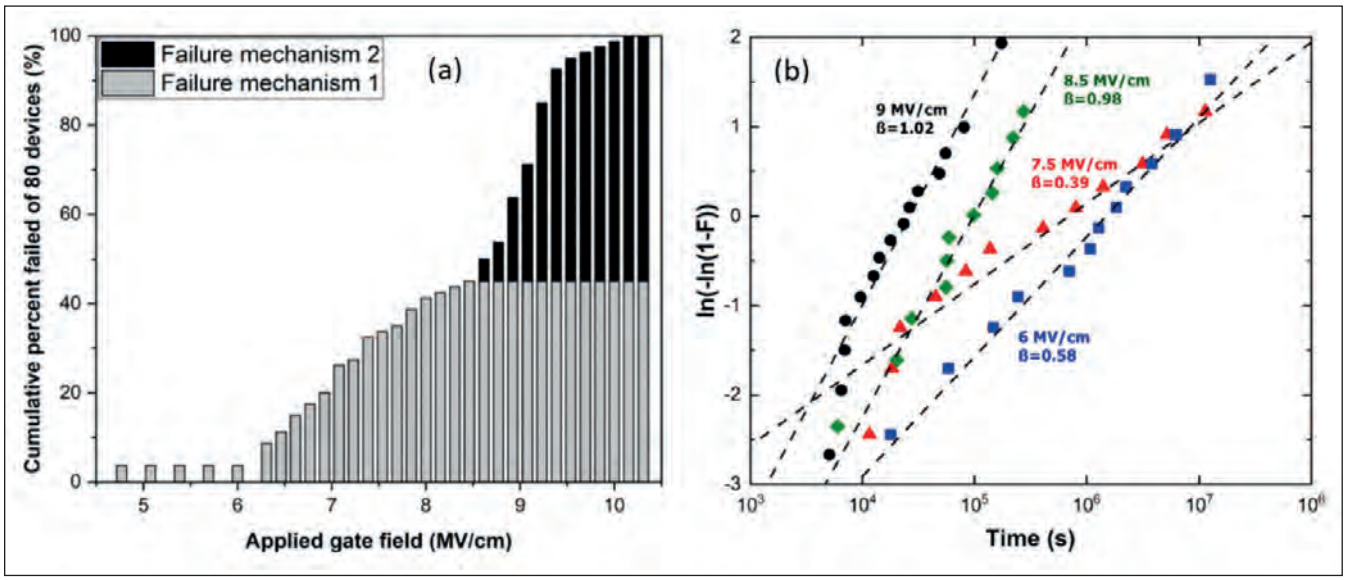
➤ Figure 3: Semiconductor-SiO_2 band offsets of other wide bandgap materials compared to cubic (3C) SiC, taken from F. Li *et al*. Materials **14** (2021)

Let's first consider the MOS interface. Power electronics applications engineers tend to want a high impedance gate, such as a MOS gate. That's proved elusive to the developers of 4H-SiC devices, who have been grappling with a poor MOS interface for the best part of 30 years – even today, it is still its Achilles heel. In the early days of the 4H-SiC MOSFET, inversion mobility was so poor – typically just 5 $cm^2\ V^{-1}\ s^{-1}$ – that the channel resistance constituted more than 90 percent of total device resistance. This is unacceptably high and untenable, in terms of utilisation within a power electronics converter. While poor mobility in 4H-SiC is now managed, as alluded to earlier, there are still problems associated with the move to trench architectures, centred around high-temperature reliability issues.

There are three main types of trap adversely affecting the MOS interface: near-interface traps; acceptor-like carbon clusters; and dangling bonds, which occur at the interface (see Figure 2 for an illustration of trap types, and a comparison of the 4H-SiC and 3C-SiC MOS interface). With 4H-SiC, the conduction band edge is swamped by all types of trapping mechanisms, including near-interface traps, which are the most dominant. In stark contrast, 3C-SiC is not affected by these near-interface traps. Of course, it is still hampered by acceptor-like carbon clusters, which have a far greater impact than dangling bonds. One key consequence of these three forms of trap is that alternative approaches to hydrogen annealing are typically required to passivate the SiC MOS interface.

What is the important takeaway from all these considerations? It's that far less effort should be required to realise higher channel mobilities, and thus lower on-state resistances, when it comes to 3C-SiC MOSFETs. In fact, efforts at developing 3C-SiC MOSFETs are already bearing fruit, with mobilities of more than 100 $cm^2\ V^{-1}\ s^{-1}$ demonstrated. It is worth noting that in addition to these results for 3C-SiC-on-silicon, there is work with bulk 3C-SiC that indicates improved performance and commercial viability for *p-n* diodes. Potential merits of bulk 3C-SiC, as opposed to the heteroepitaxy of 3C-SiC on silicon, include ease of processing technology with respect to ion implantation and metallisation. There is also the promise of scaling the voltage through adjustments to layer thickness, an attractive attribute from a commercial standpoint. This feature is especially welcome at voltages beyond 650 V, where there is competition from silicon MOSFETs, superjunction devices, insulated gate bipolar transistors, 4H-SiC MOSFETs and GaN HEMT topologies.

At Swansea University, our team is working to prove these new materials for automotive applications. The automotive and aerospace industries are notorious for insisting upon the highest reliability standards whilst keeping the cost to a minimum. That means testing gate oxides to high temperatures and



➤ Figure 4: Distribution of failures of 3C-SiC MOS capacitors for varying electric fields (a) and corresponding Weibull distributions (b), taken from F. Li *et al*. Materials **14** (2021). The time dependent dielectric breakdown analysis is conducted at electric field values of 6 - 9 MV cm^{-1}. The failure percentage increases steadily up to an electric field strength of 8.5 MV cm^{-1}, above which, the failure number rapidly increases to 100 percent.

performing accelerated lifetime analysis at the chip-level. Physical considerations suggest that 3C-SiC could offer excellent reliability. Its band offset to the SiO_2 gate oxide is 3.7 eV, a value much larger than that for silicon and 4H-SiC (see Figure 3). This is a major asset, as for a given critical electric field for the dielectric, the tunnelling current through this oxide is exponentially dependant on the band offset, which is sometimes referred to as the barrier height. One consequence of this advantage is that the electric field within a 3C-SiC MOS system can be two-to-three times higher than that for 4H-SiC, for the same leakage current into the gate driver circuitry. Due to this, de-rating requirements for a 3C-SiC trench power MOSFET can be far less stringent than those for a 4H-SiC sibling.

The 3C-SiC MOS interface also promises a high level of gate oxide reliability and a long lifetime. Measurements by Swansea University in collaboration with Warwick University on a structure with an interface formed with a gate oxidation process based on N_2O show a stabilised leakage current and a critical electric field strength at around 8 MV/cm, which is the highest value observed for a 3C-SiC MOS structure. Even preliminary 3C-SiC MOS capacitors, formed on epitaxial material with an inherent high defect density, offer a breakdown field strength of 8 MV/cm, approaching values for 4H-SiC of typically 9 - 11 MV/cm.

Our team has recently carried out a time-dependent dielectric breakdown analysis of 3C-SiC MOS capacitors (see Figure 4). We attribute their low failures to crystal deficiencies in the 3C-SiC substrate that have an impact on the localised material properties. For high field failures – that's a field strength of more than 8.5 MV/cm – failures result from an increased leakage current, or impact ionisation, due to high critical electric fields.

The primary conclusion from this work is that even at high electric fields, exceeding 8.5 MV/cm, acceleration slopes remain low for 3C-SiC. These slopes are an order of magnitude lower than 4H-SiC, suggesting extrinsic defects are still the dominant failure mechanism overall.

FURTHER READING

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➤ "Automotive Council UK and Advanced Propulsion Centre UK Roadmap 2020 Power Electronics," https://www.apcuk.co.uk/app/uploads/2021/09/https___www.apcuk_.co_.uk_app_uploads_2020_11_Technology-Roadmap-Power-Electronics.pdf.

➤ F. Iannuzzo. "Reliability Challenges of Automotive-grade Silicon Carbide Power MOSFETs," https://eepower.com/technical-articles/reliability-challenges-of-automotive-grade-silicon-carbide-power-mosfets/#.

➤ J. O. Gonzalez *et al*. "Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," IEEE Trans. Ind. Electron. **67** 7375 (2020)

➤ F. Li *et al*. "Status and Prospects of Cubic Silicon Carbide Power Electronics Device Technology," Materials **14** (2021)