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INSIDE

GaN: Natural playing field for innovation

GaN companies are re-purposing developments made in silicon over the past 70 years, while exploring new avenues

B-TRAN: Silicon-based bidirectional switching

Bidirectional Bipolar Junction Transistor (B-TRAN) is a new kind of device that offers a significant performance over power switches

GaN radio frequency transistors 2.0 ?

Switching to an N-polar architecture gives GaN transistors greater powers and efficiencies at high frequencies

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VIEWPOINT

By Christine Evans-Pughe, Acting Editor

Powering ahead with GaN

GaN found its first killer application in fast charging mobile devices. But as is often the case with mass market adoption, phenomenal success has led to lower margins and ultimately commoditisation. Now GaN chip developers are directing their efforts at products for new applications including data centres and electric vehicles.

In this issue, Florian Udrea, CTO of the start-up Cambridge GaN Devices, gives his personal view on the extraordinary potential of GaN, and how his company is optimising the use of GaN integration with intelligence, sensing, protection and more.

Richard Stevenson, editor of *CS Magazine,* looks at how Navitas is moving into higher power applications with technology such as its latest 650/800V GaNSafe range which addresses applications from 1,000 to 22,000W.

Navitas' success was helped by PowerAmerica, an organisation established in 2014 to swell domestic US production of SiC and GaN power devices. As PowerAmerica goes into its second wave of five-year funding, GaN is being given equal weight to SiC. We look at what's been achieved so far and what the next phase of investment will involve, including efforts to upskill the workforce.

While GaN is getting a second wind in terms of applications, SiC manufacturing continues to hit the headlines. Richard Stevenson explains how recent investment in Coherent from Denso and Mitsubishi (two of the biggest names in power electronics) will set the company on a new track towards improving the quality and quantity of its SiC portfolio.

Meanwhile, Nick Keller from Onto Innovation details how manufacturers of SiC power devices can produce

better transistors when they turn to metrology techniques involving Fourier transform infrared spectroscopy, optical critical dimension and picosecond ultrasonics.

Of course, let's not forget silicon. Our coverage this issue includes a fascinating piece by Ideal Power, exploring the performance and operation of the Bidirectional Bipolar Junction Transistor (B-TRAN). This new kind of device offers a significant performance improvement over conventional power switches.

All of which reminds us that nothing ever stands still in the power electronics world. In the lab, new technologies continue to take shape. Researchers from the University of California, Santa Barbara, show how switching to an N-polar architecture gives GaN transistors greater powers and efficiencies at high frequencies. And finally, a collaboration between Virginia Tech and Nanjing University is pairing gallium oxide with NiO to produce robust power electronics for harsh environments.

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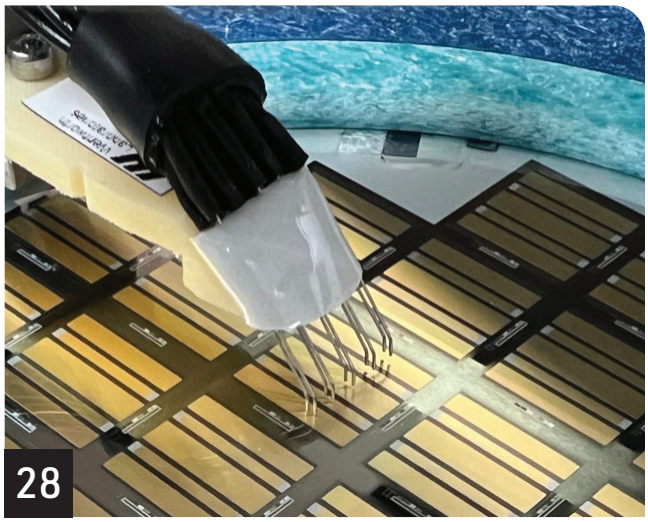

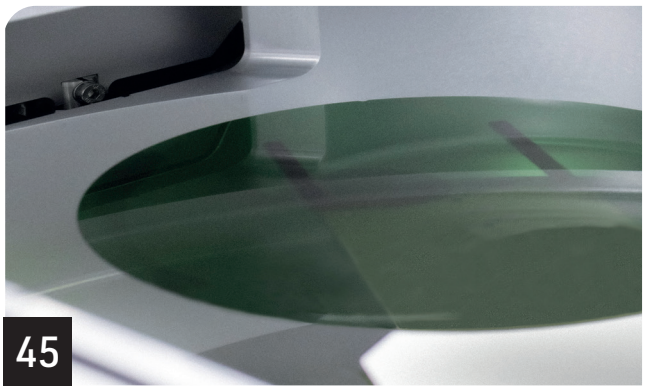

NEWS

PEW POWER ELECTRONICS WORLD

Acting Editor
Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Contributing Technical Editor
Richard Stevenson
richard.stevenson@angelbc.com
+44 (0)1923 690215

Sales & Marketing Manager
Shehzad Munshi
shehzad.munshi@angelbc.com
+44 (0)1923 690215

Senior Event and Media Executive for Power Electronics International
James Cheriton
james.cheriton@angelbc.com
+44 (0)2476 718970

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Publisher
Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

CEO Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

CTO Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

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Published by Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com W: angelbc.com

Angel BUSINESS COMMUNICATIONS

Transphorm and Allegro partner on GaN driver solution

Purpose-built isolated gate drivers to enable rapid adoption of GaN chips

TRANSPHORM and Allegro MicroSystems will collaborate on Transphorm's SuperGaN FETs and Allegro's AHV85110 Isolated gate driver to enable the expansion of GaN system design for high power applications.

Transphorm's SuperGaN FETs are designed to work in various topologies and are available in several different packages to support a wide power range while also satisfying diverse end application requirements. SuperGaN FETs are used in multiple commercial products, including higher power systems where they are proven to notably increase reliability, power density, and efficiency.

Allegro's self-powered, single-channel isolated gate driver IC is optimised for driving GaN FETs in multiple applications and circuits. The AHV85110 is said to enhance driver efficiency by as much as 50 percent compared to competitive gate drivers. This solution is also designed to simplify the system design, reducing noise by 10x and common mode capacitance by 15 times compared to other solutions in the market, according to the company.

"Allegro's AHV85110 High Voltage Gate Driver provides a highly compact and efficient power stage implementation that helps to achieve an approximate 30 percent footprint reduction with the least number of external components and bias supply requirements around Transphorm's power devices," said Tushar Dhayagude, VP of Worldwide Sales and FAE, Transphorm.

"Combined with SuperGaN's highest reliability and superior dynamic switching performance over competing technologies, the end result is a more efficient, more robust solution with increased power density in critical applications such as server, data centres, renewables and electric vehicles."

Vijay Mangtani, VP and general manager of High Voltage Power, Allegro MicroSystems, added; "we are

looking forward to the opportunity to combine our high voltage isolated gate driver AHV85110 with Transphorm's SuperGaN FET to enable higher power density, higher efficiency, and higher power output in smaller form factors and provide value to both our and Transphorm's customers."

The solution can be tested using Allegro's APEK85110KNH-06-T evaluation board. The board incorporates both the AHV85110 designed to work in various applications along with Transphorm's recently announced TOLL package available in three devices with on-resistances of 35, 50, and 72 milliohms.

QPT shortlisted for ABB power density challenge

CAMBRIDGE start-up QPT has been chosen as one of four finalists to participate in the ABB Power Density Start-up Challenge 2023 for Motor Drive Products.

ABB is seeking innovative start-ups to push the boundaries of drives and motors in terms of power density, thermal management, simplicity and cost. "Today, motors and drives are largely viewed as two independent devices. The winner will collaborate with us to develop an integrated solution that optimises resources and combines motors and drives into a single, seamless solution," according to ABB.

Rob Gwynne, founder and CEO of QPT, commented: "Our technology enables drives controls or Variable Frequency Drives (VFDs) to be made much smaller as we achieve the best power densities and efficiencies of any current technology by now enabling GaN to be hard-switched at 1 to 2ns.

"Current VFDs are bulky which means that they are invariably located away from the motor itself and then connected by copper cables that are big and heavy to cope with the hundreds of Amps or so going through them and also waste energy in the process. QPT's next generation GaN technology shrinks the size of a VFD to around a twentieth of the size so that it can be integrated beside the motor."

"The need for big, costly filters that Si, SiC or slow existing GaN alternatives require and preclude easy integration is also eliminated further reducing the overall size which further helps integration."

The final decision of which company wins the challenge is scheduled to be announced on the 7th of December 2023. Tn the meantime, there is a detailed evaluation process which means the technology will be examined in depth over ten days by key people in ABB.

UCLA researchers develop thermal transistor

Solid-state device uses electric field to control a semiconductor device's heat movement

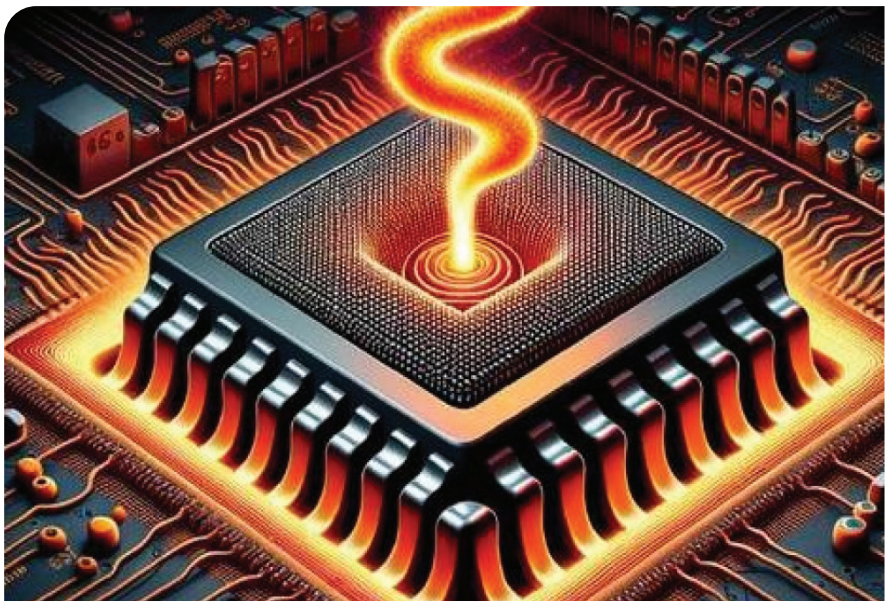
A TEAM of researchers from University of California Los Angeles (UCLA) has unveiled a solid-state thermal transistor that uses an electric field to regulate the heat generated by semiconductor devices. The group's study was published in the journal *Science*.

Precisely controlling heat flow through materials has been a long-held challenge for applications ranging from thermal management in electronics to energy systems, industrial processing, and more.

"This new design principle takes a big leap toward that, as it manages the heat movement with the on-off switching of an electric field, just like how it has been done with electrical transistors for decades," said the study's co-author Yongjie Hu, a professor of mechanical and aerospace engineering at the UCLA Samueli School of Engineering.

The UCLA team has demonstrated electrically gated thermal transistors that achieved performance with switching speed of more than 1MHz.

The transistors offer a 1,300 percent tuneability in thermal conductance and reliable performance for more than 1 million switching cycles.



"This work is the result of a terrific collaboration in which we are able to leverage our detailed understanding of molecules and interfaces to make a major step forward in the control of important materials properties with the potential for real-world impact," said co-author Paul Weiss, a professor of chemistry and biochemistry."

"We have been able to improve both the speed and size of the thermal switching effect by orders of magnitude over what was previously possible."

In the team's proof-of-concept design, a self-assembled molecular interface acts as a conduit for heat movement.

Switching an electrical field on and off through a third-terminal gate controls the thermal resistance across the atomic interfaces and thereby allowing heat to move through the material with precision.

Reference

'Electrically gated molecular thermal switch' by Man Li *et al;* Science (2023)

Nexperia and Mitsubishi announce SiC partnership

NEXPERIA has entered into a strategic partnership with Mitsubishi Electric to jointly develop SiC MOSFETs.

"This mutually beneficial strategic partnership with Mitsubishi Electric represents a significant stride in Nexperia's SiC journey," said Mark Roeloffzen, SVP and general manager of Bipolar Discretes at Nexperia.

Mitsubishi Electric has a track record as a supplier of SiC devices and modules. These devices are employed in Japan's acclaimed high-speed Shinkansen trains. Nexperia has silicon and wide bandgap devices. It also has expertise in discrete device products and packaging.

According to Roeloffzen, the collaboration will "generate positive synergies between both companies - ultimately enabling our customers to deliver highly energy efficient products in the industrial, automotive or consumer markets they serve."

Masayoshi Takemi, executive officer and group president for semiconductors and devices at Mitsubishi, said: "Nexperia is a leading company in the industry with proven technology in high quality discrete semiconductors. We are delighted to have reached an agreement on a partnership for joint development that leverages the semiconductor technologies of both companies."

Vishay to acquire Nexperia's Newport wafer fab

$177 million cash deal will accelerate Vishay's SiC production plans and secure the future of UK's largest wafer fab

US-BASED Vishay Intertechnology will acquire Nexperia's Newport wafer fabrication facility, a 200mm fab in South Wales, UK that mainly supplies automotive markets.

The $177 million cash acquisition of UK's largest semiconductor manufacturing site, brings together Vishay's capacity expansion plans for automotive and industrial customers, and meets the UK's strategic goal of improved supply chain resilience.

In addition to expanding capacity, Vishay says it intends to collaborate with the Compound Semiconductor Cluster in South Wales to develop the semiconductor industry in the UK including university and community partners in the UK and particularly South Wales.

"Under new leadership in early 2023, Vishay set an ambitious goal of investing approximately $1.2 billion in capacity over a three-year period in order to position the company to seize the opportunities created by the megatrends of e-mobility and sustainability needed for a Net Zero economy, " said Joel Smejkal, president and CEO of Vishay.

"While this transaction is supplemental to our capex investment strategy, adding Newport Wafer Fab to our manufacturing footprint will be instrumental to achieving our goal of expanding capacity for our customers and to accelerating our SiC strategy," said Joel Smejkal, president and CEO of Vishay."

By agreeing to acquire Newport Wafer Fab, Vishay says its aim is to safeguard the positions of the skilled and dedicated employees and to invest the necessary capital to set up production for SiC Trench MOSFETs and diodes. "With its solid balance sheet and ample liquidity, Vishay will

immediately bring stability and its reliable cash flow generation to ensure the facility becomes a fully operational and profitable fab" added Smejkal.

Marc Zandman, executive chairman of the board, Vishay said, "Vishay's Board made a critical decision last year to pivot the company toward profitable growth under new leadership, leveraging the company's solid cash flow generation, sound operational capabilities and broad product portfolio. A key element of this strategic shift is the investment in technologies and incremental capacity to position Vishay to capitalize on the megatrends in e-mobility and sustainability. Acquiring Newport Wafer Fab demonstrates Vishay's commitment to executing this strategic shift, and to realizing improved returns for our stockholders."

Toni Versluijs, country manager, Nexperia UK, stated: "Nexperia would have preferred to continue the long-term strategy it implemented when it acquired the investment-starved fab in 2021 and provided for massive investments in equipment and personnel. However, these investment plans have been cut short by the unexpected and wrongful divestment order made by the UK Government in November 2022.

"The UK Government's order, in combination with a weakness in the global semiconductor market, recently led us to announce the intention to reduce the number of employees at the site by at least 100. The site needs clarity about its future to avoid further losses, and today's announcement provides this. Of all options, this agreement with Vishay is the most viable one to secure the future of the site as Vishay – like Nexperia – has a solid customer base for the fab's capabilities.

"For the site, Vishay's commitment to further make the Newport Wafer Fab a success story is encouraging. Nexperia's position with regards to the UK Government's order remains unchanged."

The closing of Newport wafer fab transaction is subject to UK government review, the purchase rights of a third party, and customary closing conditions, and is expected to occur in the first quarter of 2024.

Nordic Semi and AmberSemi announce power partnership

Companies to explore opportunities to combine expertise with a focus on AC to DC power conversion

NORDIC SEMICONDUCTOR and Amber Semiconductor have entered a partnership to explore sales, marketing, and development initiatives to bring new solutions to market, such as smart electrical products, and other wirelessly integrated applications.

“We are pleased to partner with AmberSemi on exploring productisation and market opportunities around its breakthrough AC to DC conversion products and our semiconductor solutions,” said Geir Kjosavik, director for power management ICs with Nordic Semiconductor.

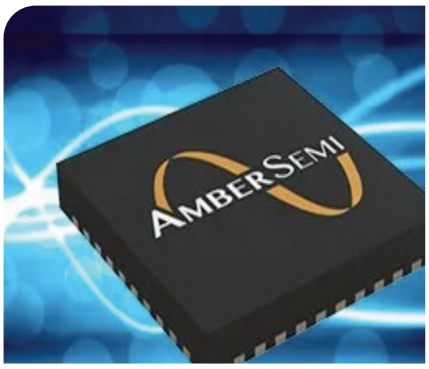
“As Nordic is expanding into wireless IoT markets that require AC power, we find AmberSemi’s compact power solutions an ideal complement to our own power management solutions for battery powered products.’

“We feel that together, with AmberSemi, we can bring new transformative and very competitive semiconductor solutions to our current and new customers,” he concluded.

“We are very excited by our partnership with such a great, forward-leaning partner as Nordic,” said Thar Casey, CEO at AmberSemi. “As we enter the commercialisation phase for our silicon products, this partnership with Nordic represents a significant inflection point and accelerator towards adoption of truly compelling and unique semiconductor solutions in the market.”

AmberSemi’s mission is to transform electrical product power management architecture from “outdated, 1950’s-era electro-mechanical power technologies, standard today in every electrical product, to smaller, safer, and smarter silicon chips”.

“Building & home control and video surveillance together constitute a $3 billion market for power semiconductors, said Paul Pickering, Semiconductors Practice Lead, Omdia. “The smart building market, in particular, includes numerous applications that require AC/DC conversion in a space-constrained environment. Examples include building safety (smoke and gas



detectors) security (video surveillance, building access control), climate control and smart lighting. Omdia forecasts growth in low-power AC/DC regulators will outpace the overall market by 31 percent from 2022 to 2027,” he said.

Casey continued: ”Our products enable dramatically smaller power solutions, creating space for a significant expansion of features in wirelessly integrated smart products, without a change in product formfactors. This dynamic is relevant and disruptive to the crowded product structures of today’s IOT products.”

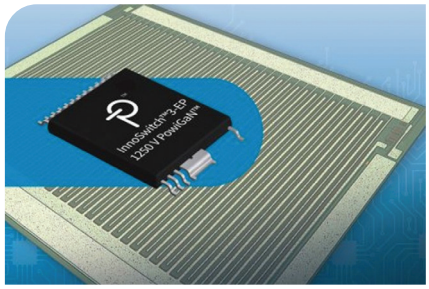
PI releases HV single-switch power supply IC

Company adds 1250V GaN power supply chip to InnoSwitch family

POWER INTEGRATIONS has released a high-voltage, single-switch GaN power supply IC, featuring a 1250V PowiGaN switch.

InnoSwitch3-EP 1250 V ICs are the newest members of Power Integrations' InnoSwitch family of off-line CV/CC QR flyback switcher ICs, which feature synchronous rectification, FluxLink safety-isolated feedback and an array of switch options: 725 V silicon, 1700V SiC, and PowiGaN in 750V, 900V and now 1250V varieties.

The switching losses for Power Integrations' proprietary 1250 V PowiGaN technology are said be than a third of that seen in equivalent silicon devices at the same voltage. This results in power conversion efficiency as high as 93 percent – enabling highly compact flyback power supplies that can deliver up to 85 W without a heatsink. The company says designers using the new InnoSwitch3-EP 1250 V ICs can specify an operating peak voltage of 1000V, which allows for industry-standard 80 percent de-rating



from the 1250 V absolute maximum. This provides significant headroom for industrial applications and is particularly valuable in challenging power grid environments where robustness is an essential defense against grid instability, surge and other power perturbations.

Samples are available now; volume-shipment lead time for 1250 V InnoSwitch3-EP ICs is 16 weeks. Pricing for InnoSwitch3-EP 1250 V devices in the INSOP-24D package starts at $3.00 for 10,000-unit quantities. A reference design, DER-1025, describing a 12 V, 6 A flyback converter is available for free download.

Diamond Foundry shrinks EV inverters

DIAMOND FOUNDRY has created a 250W EV inverter based on its diamond wafer technology, with a power electronics unit six times smaller than that of a Tesla 3.

The company, which has its HQ in California, says the solution also delivers power more efficiently, thanks to a smart design enabled by diamond wafers in composition with established SiC dies. Overall, the new 250W DF Perseus inverter use 18 SiC chips, occupies a volume of 0.46 litres and has a power density of 500KW/L In comparison, a Tesla 3 inverter has 96 SiC chips, occupies 28 litres, and has a power density of 9KW/L. Power semiconductor design is driven by thermal conductivity (the path to cool them dow) and electrical conductivity (the path to carry high currents). The thermal path has always been a challenge. To add to the problem, power semiconductors need to be isolated because of the high voltages – and voltage isolation barriers have poor thermal conductivity.

The company says that advent of cost efficient diamond wafers overcomes these issues by enabling extreme thermal performance plus extreme electrical insulation.

Toshiba 600V IPDs target BLDC motor drives

TOSHIBA has extended its range of intelligent power devices (IPD) for brushless DC (BLDC) motor drives. The new devices are suited to use in pumps, air conditioning, ventilation, fans and other similar applications.

Complementing the TPD4163F and TPD4164F, the new products (TPD4163K and TPD4164K) use a HDIP30 through hole package measuring 32.8mm x 13.5mm x 3.525mm. This new package is said to reduce the PCB mounting area by over 20 percent, when compared to Toshiba's DIP26 products such as TPD4123x, TPD4144x, and TPD4135x. This contributes significantly to reducing the space required for motor drive circuit boards.

In common with the earlier releases, the new IPDs are based upon 600V-rated IGBTs and include a matched gate driver to deliver an integrated solution in a compact package. The TPD4163K has a maximum DC current (IOUT(max)) rating of 1A and the more capable TPD4164K is rated at 2A. IGBT saturation voltage (VCEsat) of the devices is 2.6V and 3.0V respectively and the diode forward voltage (VF) is 2.0V and 2.5V.

The maximum supply voltage rating (VBB(max)) of both devices is now 600V which increases the design margin. This enhancement is useful in locations where mains power is variable or subject to fluctuations.

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Hitachi Energy

GaN: Going beyond fast charging

Navitas has introduced a range of GaNSafe ICs to expand its sales into electric vehicle, solar and data-centre markets

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

IN THE FAST CHARGING of mobile devices GaN found its first killer application. But as is often the case with mass market adoption, phenomenal success has led to lower margins and ultimately commoditisation. So, for the makers of this class of device, efforts must now be directed at developing new products for new applications.

That's the latest strategy of the US-based wide bandgap specialist Navitas Semiconductors, which unveiled its GaNSafe portfolio this September.

Strictly speaking, this fabless firm has also had success in a handful of other consumer applications, with its established range of GaN devices deployed to drive motors in washing machines, hairdryers and vacuum cleaners. "But there has been a glass ceiling into data centre, into solar and into electric vehicles," says Stephen Oliver, Navitas' VP of Corporate Marketing & Investor Relations. He told *Compound Semiconductor* that while the company's previous products excel in efficiency, reliability and quality, they don't meet all the needs for lengthy operation at high powers. "The GaNsafe range breaks through, smashes that glass ceiling, and can now be taken seriously by customers in the high-power areas."

There is a rich heritage behind the GaNSafe portfolio, which today has four parts, each designed to operate at 650 V and handle up to 800 V. Together spanning the delivery of electrical power between 1 kW and 22 kW, these packaged ICs that are based on Navitas' fourth generation of GaN benefit from three rounds of about one-fifth die shrink compared with the debut range that came out in 2018. Over the intervening years the company has equipped the GaN IC with more features, such as lossless current sensing and 2 kV electrostatic discharge protection. The launch of GaNSafe includes the addition of short-circuit protection and a higher operating temperature.

To enable higher power operation, GaNsafe features refinements to both the IC and its packaging. The three key advances at the chip level are: the introduction of a Miller clamp; a more intelligent approach to handling short-circuits, as well as ensuring overcurrent protection; and an absence of overshoot and undershoot during switching. Note that even a well-designed device, operating in an efficient manner, can run into problems by generating electromagnetic interference (EMI). But with GaNSafe it is possible to reduce any spikes in EMI via external programming.

"That means that the design team doesn't have to do another spin and cross their fingers and hope they found the thing that's making the spike," enthuses Oliver. "You can tune it in in real time."

Perfecting the package

Innovation is also seen in the 10 mm by 10 mm package, referred to as TOLL – Transistor Outline Lead-Less. Despite the tremendous functionality of the GaNSafe IC, just four external connections are used, allowing leads to be fused together. This creates what is essentially a solid lump of copper, aiding thermal performance, a particular valuable

To help succeed in new markets, Navitas has set up design centres for a data centre power team and an electric vehicle team. Both are staffed with a mix of talent, including experts in devices and those with real-world system knowledge, gained in previous roles outside Navitas

asset in solar systems that undergo wide variations in temperature every day.

Navitas has also 'keyed' some of the pins in its GaNSafe design, creating a ridge metal surrounded by plastic. It's a design that ensures a tough joint, aiding the mechanical integrity of the product. Another strength of GaNSafe is that it is better at handling humidity and preventing liquid ingress. "It's a longer path for any humidity to get into the package and destroy it," explains Oliver.

Since the start of this year, about 40 of Navitas' customers have been working with products from the GaNSafe portfolio. These firms include: Enphase, a producer of power inverters for the Solar Industry; and Geely, a maker of power systems for the electric vehicle (EV) market that supplies its products to Volvo's EV off-shoot Polestar, as well as Proton and Lotus.

To help succeed in new markets, Navitas has set up design centres for a data centre power team and an electric vehicle team. Both are staffed with a mix of talent, including experts in devices and those with real-world system knowledge, gained in previous roles outside Navitas. These design teams offer tremendous support to customers, including details for the full bill of materials, circuit diagrams, a PCB layout, and results of tests of EMI, thermal characteristics and efficiency.

One reason why these design teams are needed is that some of the companies that they work with are only just starting to move away from silicon power devices.

"With GaN, we are asking people to go from 50 kilohertz switching for the system to 500 kilohertz-to-a-megahertz, which means that they can't use the same control chip from their favourite provider that they've used for the last 20 years," says Oliver. Navitas can help in this instance, by advising customers about suitable replacement components.

Minimising manufacturing costs

To produce its GaN devices, Navitas partners with an undisclosed packaging partner and the world's biggest foundry, TSMC. Some may question this approach, claiming that it's hard to develop breakthrough technologies with external fabs, while warning that it is risky to depend on partners when there's a need to ramp volume. But Oliver questions both these views, seeing the situation very differently.

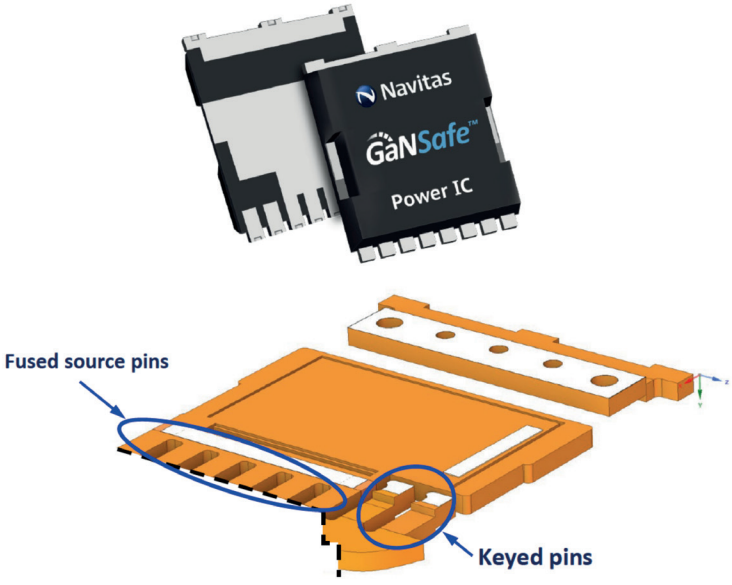
"Circuit development has nothing to do with the fab," counters Oliver "It's all about good engineers sitting around the table, having good ideas and making it happen."

And while he agrees that it's vital to have capacity, he argues that the crucial question is whether it is economical to have that capacity. He sees no sense in spending billions on new fabs – as Wolfspeed and Infineon are doing – and points out that there is no need to buy new equipment to make state-of-the-art GaN devices. At TSMC, Navitas' latest ICs are produced on 500 nm equipment around 30 years old.

Fabs with this level of capability are very common, with plenty in the US running silicon products on 6-inch and 8-inch lines at low margins. Retrofitted with a handful of tools, they can produce GaN ICs within a year, a move that is welcome, thanks to the higher margins.

With access to capacity clearly not an issue, and GaN ICs gaining traction in new markets, Navitas looks assured of a successful future.

➤ Through sourcing and 'keying', GaNSafe ICs deliver a superior thermal performance to their predecessors.



PowerAmerica powers on

Five years of additional funding will swell domestic production of SiC and GaN power devices

LATE THIS SUMMER, the US renewed its commitment to accelerating the development and deployment of more efficient power electronics by funding five more years of PowerAmerica, the Department of Energy's first Clean Energy Manufacturing Innovation Institute.

In the first year of this second phase of funding, which will see a shift in a focus from SiC to roughly equal backing of both this class of device and that based on GaN, PowerAmerica is contributing another $8 million. A call for proposals will soon follow, with projects maintaining the existing formula for funding – that's private funding supporting federal funding, with both contributing 50 percent of costs.

The latest $8 million builds on $70 million of initial federal funding in the first phase, alongside combined contributions of $81 million from member partners, which total 90 and include those from industry, academia and national labs.

Drawing on that total investment of $151 million, the 196 projects supported by PowerAmerica have been a great success. The 73 projects led by industry, along with 112 led by academia and another 11 fronted by National Energy Labs, have spawned more than ten wide bandgap technologies.

Chris Saldaña, director of the US Department of Energy Advanced Materials and Manufacturing Technologies Office, which is responsible for renewing funding for PowerAmerica, argues that another impressive aspect of PowerAmerica is the relatively high proportion of projects that have reached commercial status. Note that these projects aren't necessarily directly linked to product commercialisation:

"They are pre-competitive in nature, so commercialisation isn't the immediate goal. You have a group of companies, universities, government organisations that come together to work on problems of importance for us, the clean energy sector."

Highlights of successes so far from PowerAmerica include the creation of a SiC chip pilot line in the US, owned by X-FAB.

"The purchase and process development for that line was done through Power America, and has had a major impact in terms of meeting growing demand for those devices," says Saldaña.

PowerAmerica also supported Wolfspeed's development of 3.3 kV, 6.5 kV and 10 kV MOSFETs. "The 3.3 kilovolt MOSFETs are in production," enthuses Saldaña.

While the first phase focused on SiC, GaN was not neglected. Funding supported the growth of Navitas, which has mushroomed from a start-up to a billion-dollar company listed on the NASDAQ exchange. Growth has come from rocketing sales of GaN ICs for laptop and cell phone power supplies.

Funding from PowerAmerica is also driving the uptake of SiC in heavy vehicles. John Deere has developed a 200 kW, 1050 V DC bus inverter based

on SiC that enables 25 percent fuel savings. Cynics might argue that all of these initiatives could have happened without the support of PowerAmerica. But that misses the point.

"The goal of the Manufacturing USA institutes is to supercharge innovation in these technology spaces that we invest in," says Saldaña. And he points out that while individual advances at companies are to be celebrated, it is important to not overlook the collective impact, which is more than the sum of its parts. "We're trying to move the whole sector forward, not necessarily individual companies, individual commercial products."

Growth in domestic production of wide bandgap power electronics is also helping to trim US greenhouse gas emissions. As well as supporting the proliferation of electric vehicles, increased production of SiC power electronics is underpinning the rejuvenation of an electric grid, making it more reliable, more responsive and better at working with renewable energy technologies.

Upskilling the workforce

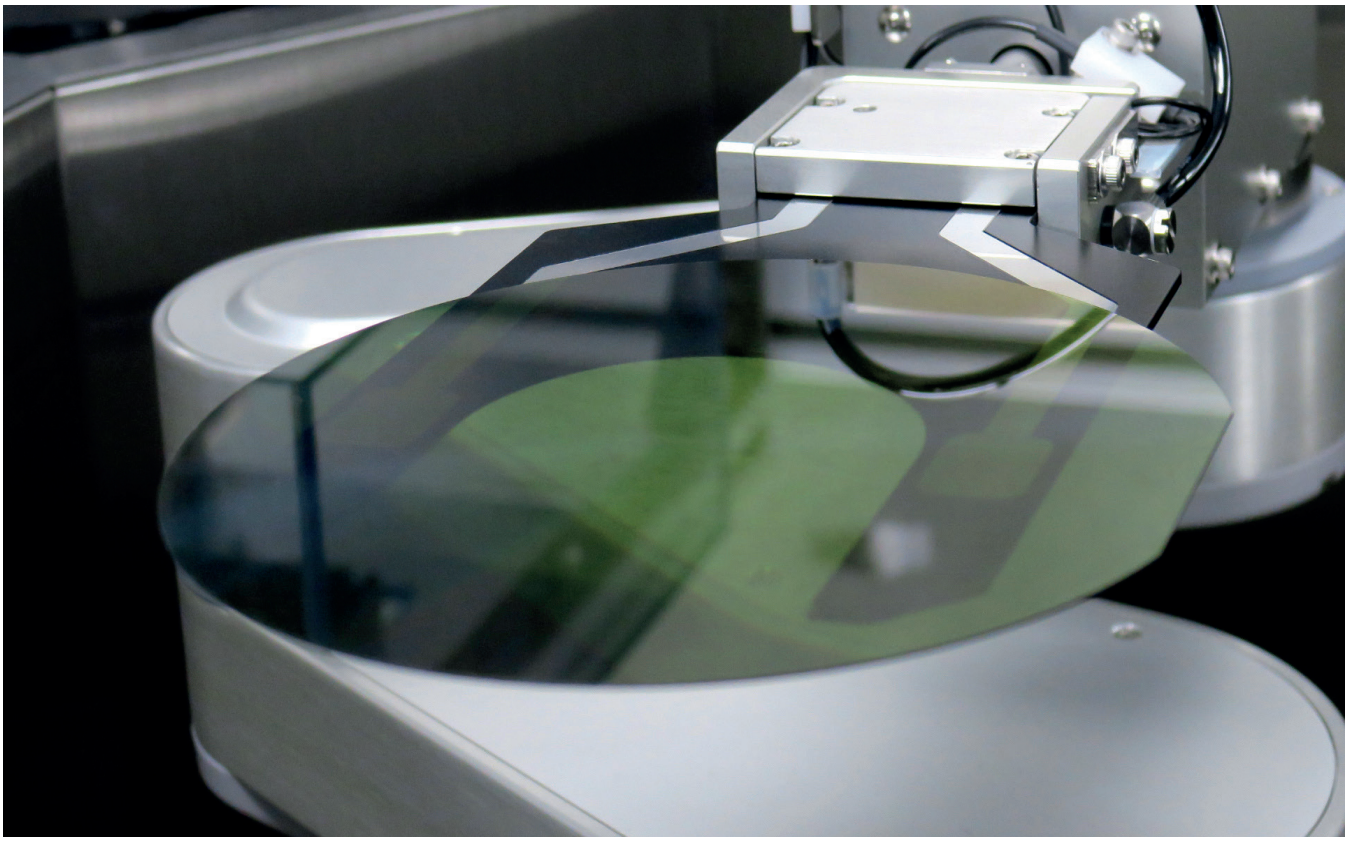
Another major contribution by PowerAmerica is the creation of a highly skilled workforce for producing and deploying wide bandgap power electronics. Efforts have already included STEM programmes for 9,000 students in their last year of school, and the training of more than 400 masters and PhD students.

Having tracked the destinations of these graduates, it is clear that training is providing a great return on investment, with the majority entering and remaining within the wide bandgap power electronics industry.

"When you create this critical mass of activity in an area, they're going to be part of the same community moving forward, and will help to push the mission that they were trained under through the Institute," says Saldaña. Motivated by this success, PowerAmerica is developing training materials, training programmes and certification to support those wanting to further their careers within this sector.

Efforts are also being directed at attracting everyone to this industry. "There's a strong emphasis on diversity, equity, inclusion and accessibility through the Institute," says Saldaña.

Another appeal of working in the US semiconductor industry is its long-term support. That extends beyond PowerAmerica, which will certainly run for the next five years and quite possibly more, to an initiative called Energy Efficiency Scaling for Two Decades. It's a national programme that aims to double the energy efficiency of microelectronics every two years. Success will drive disruptive innovation, giving yet more impetus to America's burgeoning semiconductor industry.



A Coherent plan for SiC

Backed by substantial investment from two of the biggest names in power electronics, Coherent has a well-devised plan for expanding the quality and quantity of its SiC portfolio

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

DRIVEN ON by lucrative opportunities in the burgeoning electric vehicles market, many makers of SiC materials and devices are establishing substantial expansion plans. Just this year Wolfspeed announced its intention to build the world's largest SiC fab in Germany, only to be eclipsed this summer, when Infineon boasted a similar claim for its new SiC facility, to be constructed in Malaysia. And this October Coherent has been grabbing the headlines by creating a subsidiary devoted to SiC.

Supported by investment from Denso and Mitsubishi Electric that totals $1 billion – a transaction scheduled for completion in the first quarter of 2024 – efforts to create this subsidiary are already underway. In exchange for these two substantial cash injections, each $500 million, the Japanese firms will each receive a 12.5 percent non-controlling ownership interest, as well as long-term supply agreements that support their SiC activity. Coherent will ship SiC substrates, both 150 mm and 200 mm, to Mitsubishi Electric and Denso.

Heading up the new subsidiary is Sohail Khan, Coherent's executive VP, Wide-Bandgap Electronics Technologies. Khan is definitely delighted with this modus operandi.

"You always want to have the leading system companies as your lead customers," remarks Khan, who points out that Denso is a leading tier-one supplier to the automotive industry and Mitsubishi Electric is a leading provider of industrial and automotive power systems.

Coherent, which has its II-VI heritage to thank for its SiC prowess, could have turned to a number of different options for funding the growth of its new subsidiary.

Some may see investment from other firms as questionable – but not Khan, who argues that it's an asset. "Our view was that when you have ownership, you have the right interest and motivation. I would go as far as saying not all money is the same."

➤ Top: 150 mm substrates on a robotic arm.

Note, though, that Khan is not advocating that any partner will be beneficial. “It is important to have the partners who have validated your technology, have used your technology, and have the confidence in your technology and capability.”
He adds that for the relationship to blossom, a partner also needs assurance that they will be supplied with high-quality products, in volume, at a competitive price.

Confident of meeting all these requirements, the Coherent subsidiary will benefit from getting “maximum learning”. The leadership at II-VI always considered this as a vital pillar to market success, and this philosophy still lies at the centre of Coherent and its subsidiary.

Another benefit of working with Mitsubishi Electric and Denso is that it allows Khan and his team to get much closer to the end suppliers to the market. “That’s absolutely critical,” argues Khan.

The insights gained from the new venture will help to continually refine the production processes of this vertically integrated Coherent subsidiary, which as well as making substrates and epiwafers is expanding into devices and modules.

Open to all

Khan is very keen to point out that the subsidiary is not just there to serve Mitsubishi and Denso. “I want to emphasise that we are not going to be a captive supplier. It is just an investment from these companies into the silicon carbide business.”

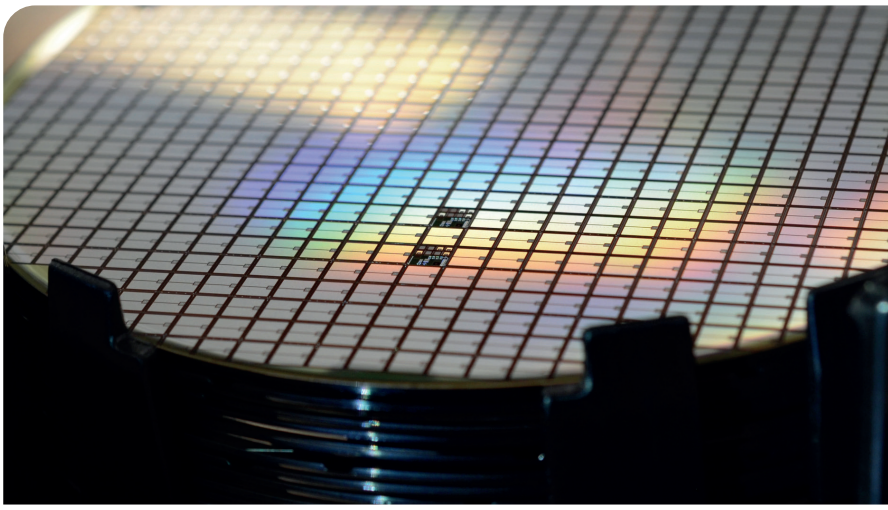
He adds: “The idea is to be a merchant player, learning from other customers and providing our products at every level.” The Coherent subsidiary will engage with some companies at the substrate and epiwafer level, and others at the device or module level.

Khan is responsible for around 650 staff in the US, spread over a number of facilities. In addition, there is a site in Fuzhou, China, that provides contract manufacturing.

Investment in the Coherent subsidiary will increase capacity and support growth. Capital and operational expenditure will follow, ranging from the installation of additional furnaces and epi-reactors to improved R&D capabilities that support the development of devices and module designs.

Substrates produced by the subsidiary are already available in 150 mm and 200 mm diameters. According to Khan, lines for processing the larger size are now being brought up, with tools undergoing qualification. However, this will take time – and Khan expects it will be 2025 before 200 mm is the dominant diameter for substrate shipments.

Through the licensing of General Electric’s SiC MOSFET technology, Coherent has been qualifying 1200 V and 1700 V devices that meet the Automotive Electronics Council AEC-Q101 standard.



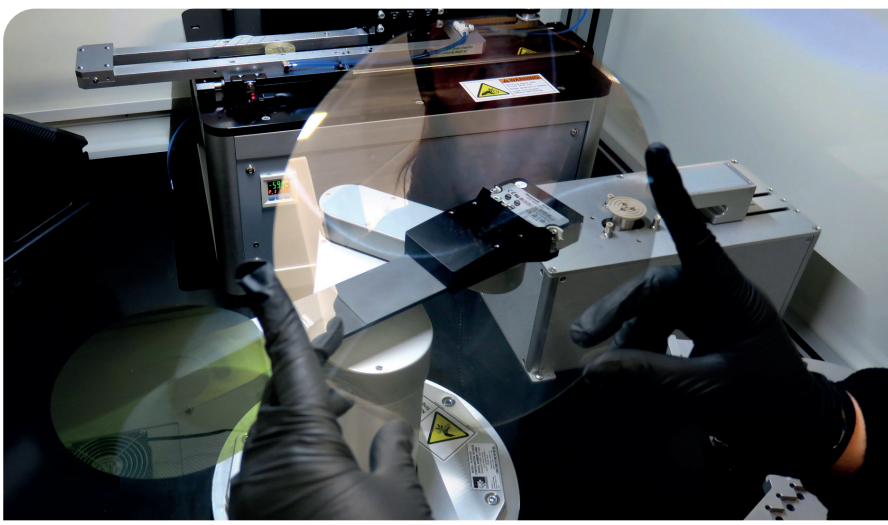
➤ 150 mm wafer populated with SiC devices.

“If you look at the power market, they guarantee 175 degrees C,” says Khan. “We guarantee 200 degrees C operation. Our devices are very rugged and go through extensive tests on reliability.” These MOSFETs are now being sampled at pre-production levels.

The degree of success that will come from Coherent’s SiC subsidiary will be disclosed in quarterly results. Khan is confident of rising sales in a global market now worth around $3 billion, and forecast to generate revenue of more than $20 billion by the end of the decade.

It is possible that sales may even outstrip this figure, suggests Khan, arguing that once newer technologies prove themselves, they always replace the incumbents. “No one has a crystal ball, but we have seen predictions anywhere from 30 percent to 80 percent penetration of [silicon carbide] in EVs.”

Should deployment veers towards the upper end, the Coherent subsidiary will enjoy tremendous success, along with its two Japanese investors.



➤ 200 mm substrate.

The road to SiC process control

Manufacturers of SiC power devices produce better transistors when they turn to metrology techniques involving Fourier transform infrared spectroscopy, optical critical dimension and picosecond ultrasonics

BY NICK KELLER FROM ONTO INNOVATION

EFFORTS at curbing carbon dioxide emissions are stepping up, with more electric vehicles on our roads and the installation of renewable energy sources on the rise. Alongside these advances, the makers of these green technologies are increasing the electrical efficiency of their offerings, with silicon-based power devices being ditched in favour of superior alternatives based on the likes of SiC.

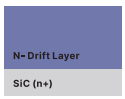
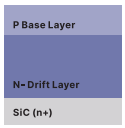
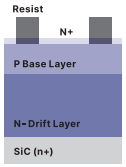
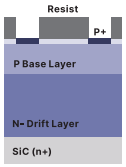
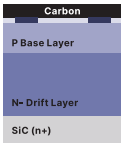
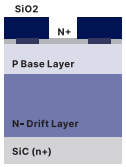
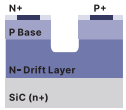
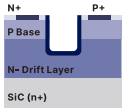
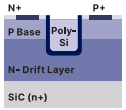
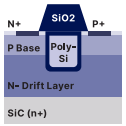
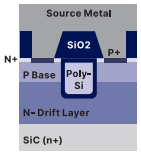
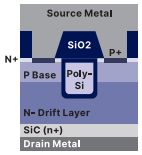
Supporting this move are the superior physical properties of these compounds. Compared with silicon, semiconductors such as SiC have wider-bandgaps, a higher electron saturation velocity, a higher critical electric field and a larger thermal conductivity. Drawing on all these strengths, power transistors offer higher operating frequencies, higher power ratings, elevated operating temperatures, better cooling capability and lower energy loss – just the traits that the market wants.

Today's manufacturers of SiC power devices are tending to focus on trench-based devices, a design that reduces on-resistance and increases carrier mobility. But there is a trade-off, with these strengths coming at the expense of increased fabrication complexity.

To address this issue, high-volume manufacturers of SiC power devices must adopt inline process control at several key steps, including optical metrology methods like Fourier transform infrared (FTIR) spectroscopy, optical critical dimension (OCD) and picosecond ultrasonics. When armed with these techniques, chipmakers are far better informed when undertaking critical processing steps, including epilayer growth, trench etch, gate poly-silicon etch back, and frontside/backside contact metallisation.

All of these three process control techniques that have just been mentioned can play a major role in streamlining SiC production. When FTIR is adopted alongside advanced algorithms, SiC manufacturers can extract epilayer thickness and carrier concentrations for two- and three-layer stacks. What's more, FTIR can non-destructively characterise the depth and the dopants in the implant layer directly on SiC substrates before and after the anneal process step. That's a significant benefit, as it removes the need for monitoring silicon wafers and secondary ion mass spectrometry when undertaking implant characterisation. Meanwhile, the introduction of a multi-channel OCD

METROLOGY SOLUTIONS FOR SiC TRENCH MOSFET PROCESS

						
LAYER	**Drift Layer Epi**	**P Base Implant**	**N+ Implant**	**P+ Implant**	**Carbon Layer Dep & Anneal**	**Hard Mask Etch**
KEY PARAMETER(S)	Thickness Dopant Conc.	Implant Depth Carrier Conc.	Implant Depth Carrier Conc.	Implant Depth Carrier Conc.	Thickness Carrier Conc. + Depth	HM Height HM CD
DEVICE IMPACT	R_{on} Breakdown Voltage	Channel Mobility(μ_{FE}) V_T	Contact Resistance	I_{DSAT} C_{GD}	Surface Roughness Si Desorption Block	R_{on} Gate SWA (Mobility)
TECHNOLOGY	FTIR	FTIR	FTIR	FTIR	OCD and FTIR	OCD
						
LAYER	**Gate Trench Etch**	**Gate Oxide Growth**	**Poly Si Etch Back**	**Passivation Oxide Etch**	**Source Metal Dep**	**Drain Metal Dep**
KEY PARAMETER(S)	Depth and TCD/ BCD/SWA/Rounding	Sidewall Thickness Bottom Thickness	Recess Depth	Height CD	Thickness (Ti/Al) Roughness	Thickness (Ti/Al) Roughness
DEVICE IMPACT	R_{on} & I_{DSAT} Parasitic JFET R	Channel Mobility(μ_{FE}) V_T & Q_{GD}	V_{GS}	Leakage Current C_{GS}	S/D Contact Resistance	S/D Contact Resistance
TECHNOLOGY	OCD	OCD	OCD	OCD	PULSE	PULSE

➤ Figure 1. SiC trench MOSFET process flow.

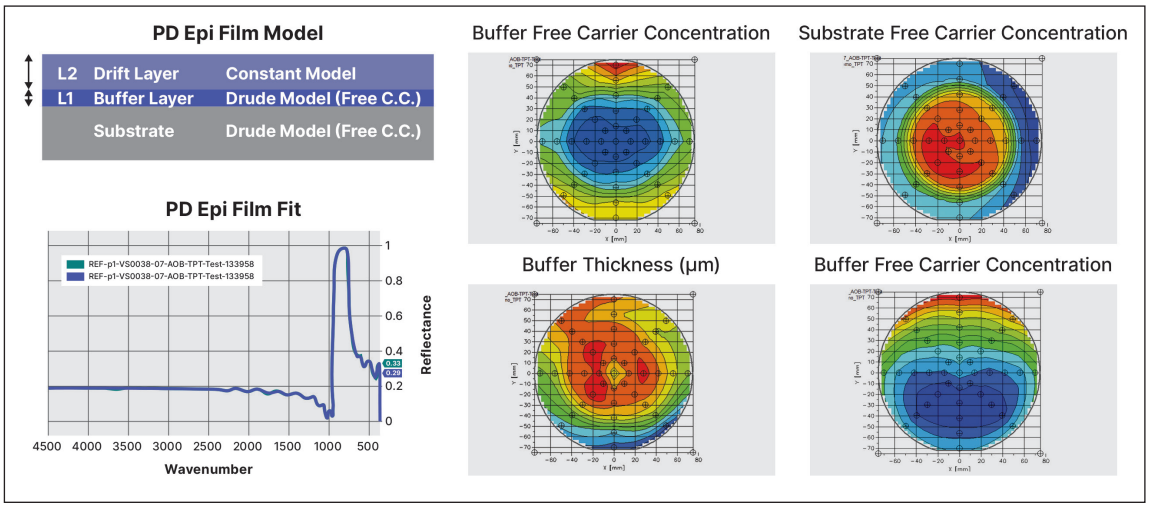
tool in a SiC fab can accurately and non-destructively determine trench depth, bottom and top widths, and bottom rounding at the trench etch step, when this technique draws on electromagnetic solvers that utilise advanced rigorous coupled wave analysis. Note that bottom rounding of the trench is critical to preventing a high electric field density, and ultimately premature device failure. Lastly, picosecond ultrasonics can improve efficiency in a SiC fab by measuring frontside and backside metal contact thickness. Together, these non-destructive, in-line process control methods empower chipmakers to solve many of the challenges posed by the increased fabrication complexity of SiC power devices.

Soon we will take a closer look at all three techniques. But before we do, let's take a minute to review the process steps for making a simplified SiC trench MOSFET and a SiC trench insulated-gate bipolar transistor (IGBT). This is outlined in Figure 1, which illustrates the process flow for the SiC trench MOSFET, and shows the key process steps, key parameters, device performance impact and the proposed process control solution. This figure also illustrates the process flow for a SiC trench IGBT device. While the steps are very similar, there are differences. The most significant is that a SiC trench IGBT has a p^+ substrate and a n^+ buffer layer before the drift layer.

Scrutinising layers with FTIR

Incorporating a Michaelson interferometer, a broadband light source and a fast Fourier transform (FFT) algorithm, FTIR spectrometers are well suited to studying the layers of SiC devices. This technique, requiring acquisition of infrared spectra extending from the near-IR to the far-IR, is quick, non-destructive and highly sensitive to molecular and free-carrier absorption. By measuring both transmission and reflectance spectra, a single tool can measure the elemental composition of epilayers and their thickness. A well-designed system is capable of obtaining the characteristics of five epitaxial layers from a single scan.

Spectroscopy in the IR offers much insight, including values for the carrier concentration of doped semiconductors. This is possible due to free carrier absorption, a process described by the Drude model, which accounts for the frequency-dependent conductivity of metals. The Drude model can be used to calculate the plasma frequency, which depends on the concentration of free carriers and their effective mass. For wavelengths above the plasma frequency, the electric field of the incident light oscillates so fast that the material acts like a dielectric. That's not the case for wavelengths below the plasma frequency, which absorb light. Note that



➤ Figure 2. PD Epi model fitted to the experimental spectra from the FTIR system and the wafer maps for all parameters of interest.

the absorption coefficient is directly proportional to the free carrier concentration.

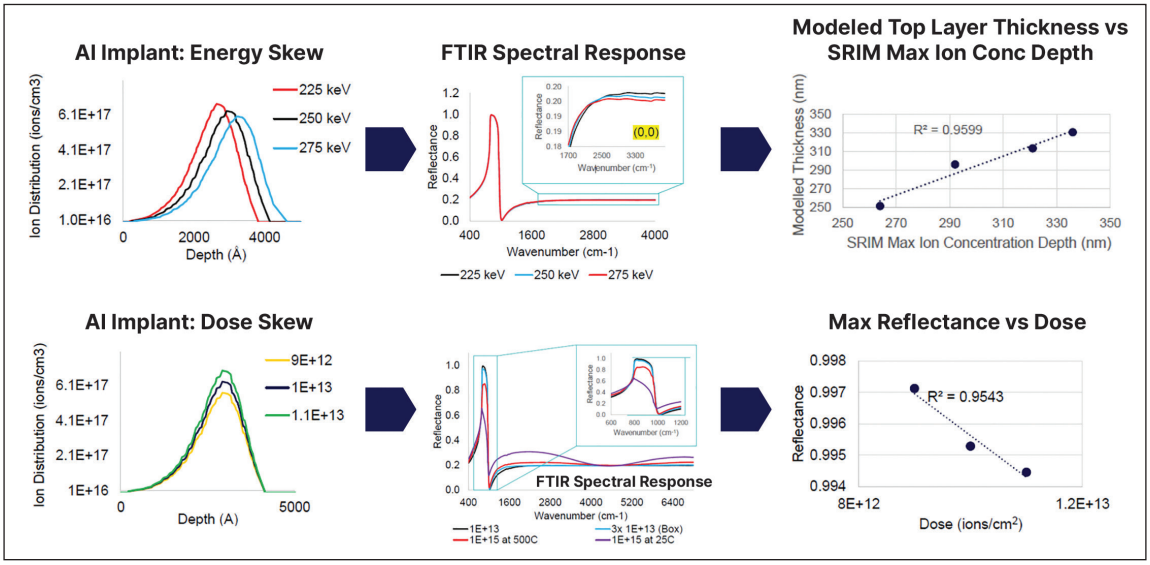
The information garnered by FTIR spectroscopy is incredibly valuable to makers of SiC trench MOSFETs and IGBTs. For the SiC MOSFETs, the thickness and the carrier concentration of the drift layer directly determines the breakdown voltage of the transistor. Meanwhile, for the IGBT, the buffer layer thickness and the free carrier concentration determine a number of key characteristics, including switching speed and conduction losses.

FTIR spectroscopy also offers great insight into the ion implantation process. Measuring the depth and free-carrier concentration of the p, p^+ and n^+ regions is critical, because all these features influence the channel mobility, contact resistance, threshold voltage and saturation current.

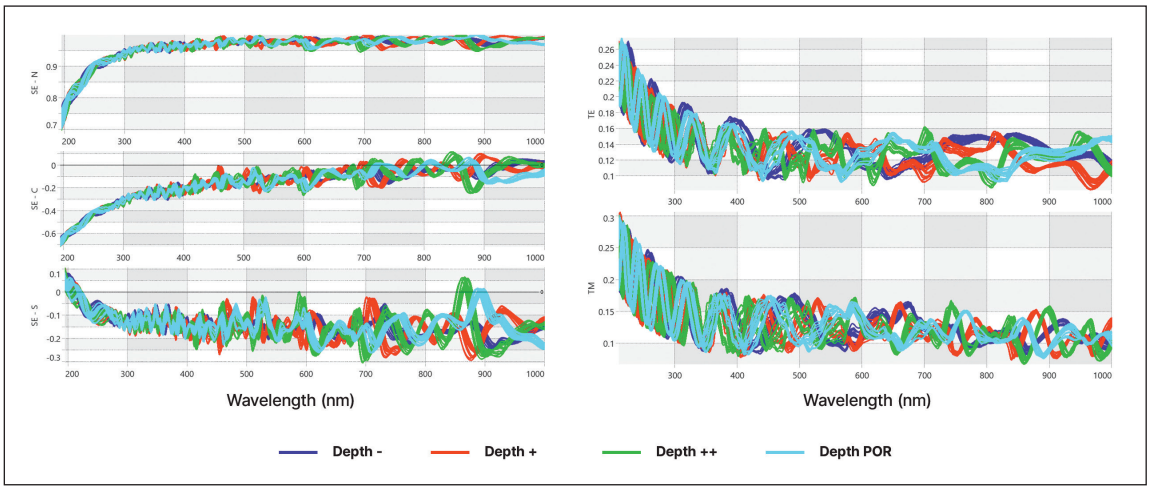
At Onto Innovation we are supporting this task, having developed a new analysis engine called PD Epi, which enables the modelling of complex epitaxial film stacks in compound semiconductors. Our analysis engine provides direct modelling of carrier concentrations and film thicknesses of multiple layers, including the substrate. Utilising Drude oscillator models and gradient layers, our engines determine the carrier concentration profile through the structure during the diffusion and implantation process.

To illustrate the power of our PD Epi model, we have used it to characterise an IGBT epiwafer. Using our model we have determined the buffer and drift layer thickness, and the carrier concentration for the buffer layer and the substrate. This study involved a Design Of Experiment (DOE) methodology, with the drift layer thickness varied from 5 µm to 30 µm. while all other parameters of interest were kept constant.

An example of results on these IGBT epiwafers, obtained with our PD Epi model and fitted to the experimental spectra from the FTIR, is shown in Figure 2, which has wafer maps for all parameters of interest. We have correlated the measured drift layer thickness to the expected thickness. This gave a coefficient of determination (R^2) exceeding 0.99, demonstrating that the predictive capabilities



➤ Figure 3. SRIM simulations for energy and dose skews, then raw FTIR spectral response to those skews and finally correlation of FTIR measurements to SRIM.



➤ Figure 4. The spectral variation of the spectroscopic ellipsometry and normal incidence reflectometry OCD channels.

of the PD Epi model are accurate. The measured precision levels – that is, the standard deviation of repeat measurements – averaged 0.2 percent for the drift layer thickness, and 8.5 percent and 2.5 percent for the buffer free-carrier concentration and substrate free-carrier concentration, respectively.

Additional capabilities of FTIR spectroscopy are measuring the implant depth of aluminium ions, and detecting dose variations of this species after the ion implantation process and prior to annealing. Normally, dopants must be activated, so that FTIR can detect the effects. However, with our PD Epi model, manufacturers can conduct their measurements prior to dopant activation.

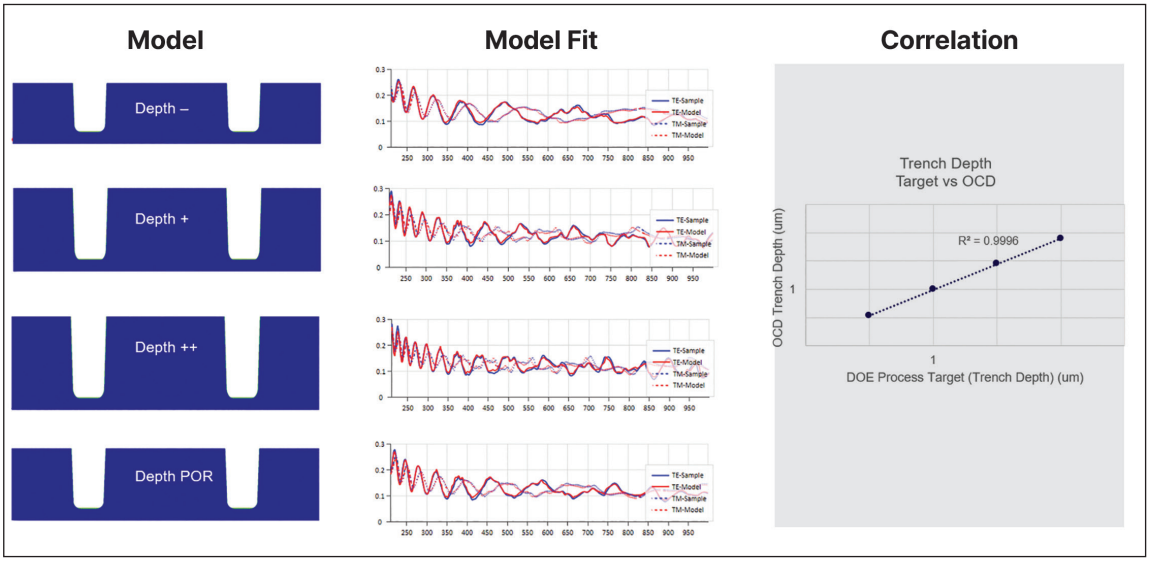
To demonstrate this, we have used FTIR spectroscopy to measure dose and energy skews. This involved simulating the stopping range of ions in matter – allowing us to then model implant depth and carrier concentrations. Using this model as a reference for our FTIR measurements, we then simulated the energy and dose skews (see Figure 3, which also shows the FTIR measurement response to the skews, and the correlation of the measurements to the SRIM simulations).

As part of this particular effort, we used a simple Drude oscillator model to determine the free-carrier concentration, while floating the thickness. The thickness results coming from this model were used to correlate peak implant depth; that correlation is roughly 0.96. Following this, we used the maximum reflectance to correlate to the dose. Again, we obtained excellent correlation.

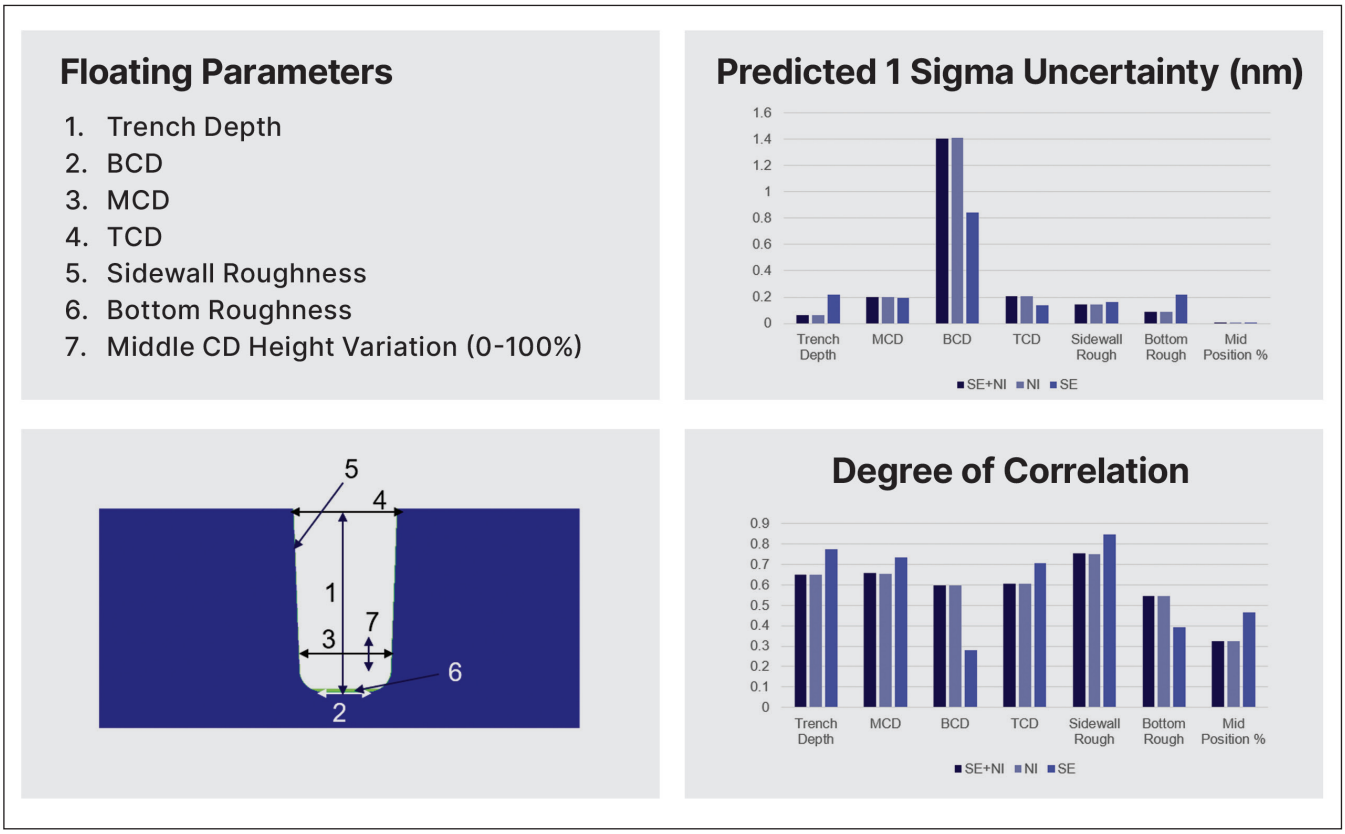
Determining dimensions with OCD

OCD has been used in semiconductor manufacturing for over 20 years. During that time its application has shifted from top-down approaches, like critical dimension scanning electron microscopy (CD-SEM) and image-based microscopy, to OCD for dimensional metrology. Driving this move has been the need to measure re-entrant and vertically recessed structures, which are invisible to top-down metrologies. Today, OCD metrology is an indispensable part of the process control loop in high-volume manufacturing.

In contemporary thin-film and OCD systems designed for the specialty market, spectroscopic

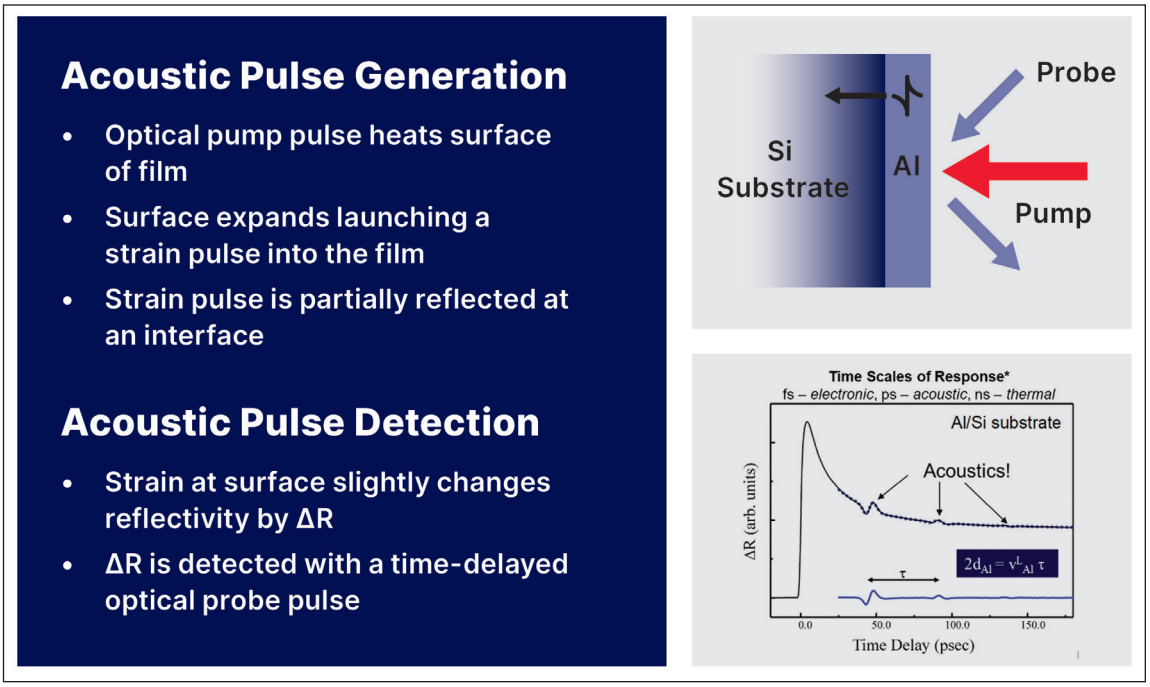


➤ Figure 5. The physical model and the model fit to the experimental structure on the four DOE wafers.



➤ Figure 6. A comparison of simulations using spectral ellipsometry (SE), normal incidence (NI), and combined SE and NI.

ellipsometry provides the gold standard for thin-film measurements. This is employed alongside polarised spectroscopic reflectometry, which collects specular scattering spanning the deep ultraviolet to the near-infrared from periodic structures, both 2D and 3D, at oblique and normal incidence, respectively. Analysing this data with our proprietary Ai Diffract software, which is an electromagnetic solver based on advanced rigorous coupled wave analysis, allows us to extract detailed structural information. Process engineers can draw on this when running advanced process control. There are several advantages of OCD over other approaches, such as atomic force microscopy,



➤ Figure7. Picoseco nd ultrasonics measurement principles. The decaying thermal component is subtracted from the signal to get the blue curve.

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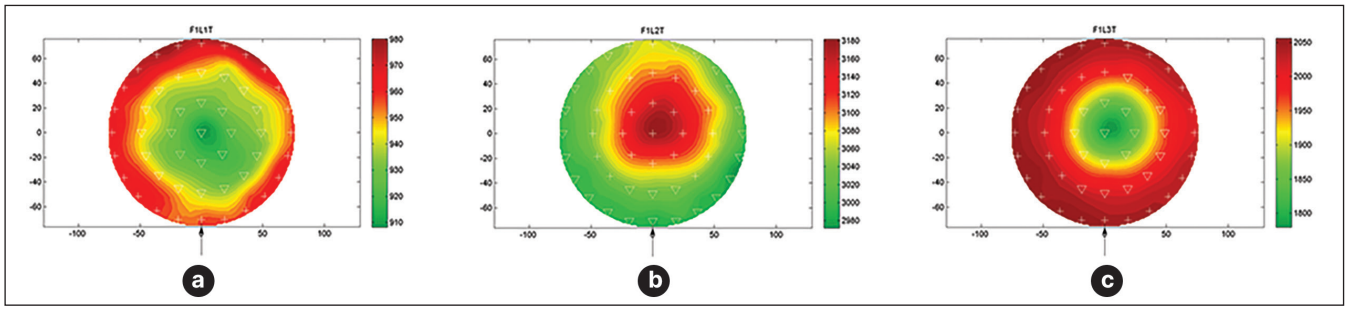


➤ Figure 8. Forty-nine point maps of (a) Ti 1000 Å, (b) NiV 3000 Å, and (c) Ag 1500 Å.

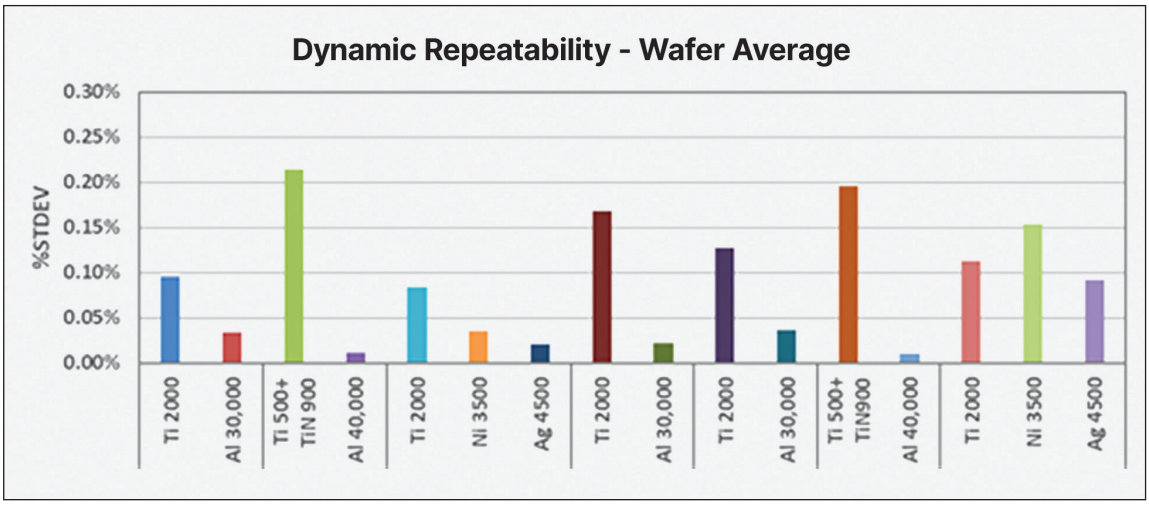
CD-SEM, and transmission electron microscopy. Merits of OCD are that it's: non-destructive; measurements may take less than a second; it is highly precise, offering angstrom level repeatability; and it is data rich, with the capability to measure tens of parameters simultaneously in complex 3D structures. However, OCD also has a significant disadvantage: being an indirect method, it requires a model to interpret complex spectroscopic data. Due to this, OCD metrology is seen by some as inaccurate and subject to long setup times. But both these drawbacks can be avoided with a model-guided machine learning algorithm that synergizes physical modelling with machine learning.

During production of SiC trench MOSFETs, OCD can be used at the key process steps shown in Figure 1. Of particular interest are the post-trench etch measurements. The trench etch is a key step because trench parameters, like bottom width, bottom rounding, sidewall angle, depth and roughness, contribute to key performance attributes, such as breakdown voltage, on-resistance, channel mobility, and time-dependent gate oxide breakdown. Evaluating the quality of the etch is paramount, because this step is challenging, due to SiC being extremely hard, chemically stable, and having a low selectivity to SiO_2 hard masks.

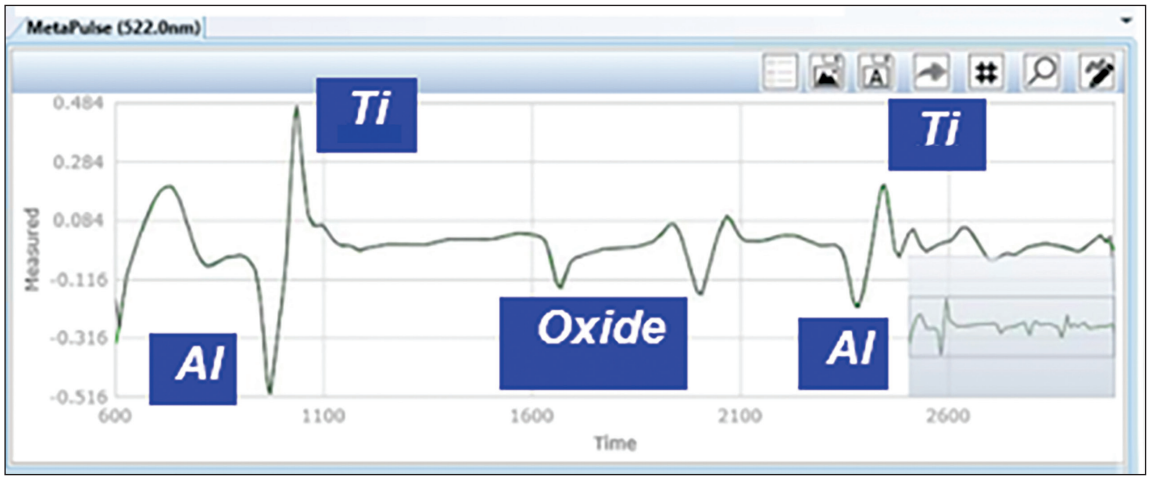
To demonstrate the benefits that analysis with our Ai Diffract software brings to OCD of SiC MOSFETs, we have undertaken a DOE, processing the trench etch step on four wafers. We began by varying the etch time to skew the trench depth, and then carrying out spectroscopic ellipsometry and normal incidence reflectometry measurements (see Figure 4). Using a physical model, we fitted the data, finding an excellent correlation between the average trench depth measured with the Ai Diffract model, and the expected depth based on DOE conditions (see Figure 5).

Building on this investigation, we considered other key parameters in the model, such as the trench bottom width. It's possible to also measure these parameters. However, how do we know whether OCD has sufficient sensitivity and discrimination? To answer this, we used uncertainty and sensitivity analysis to predict specific parameter measurements (see "Uncertainty and sensitivity analysis" for details).

Following that, we used a model with Process Of Record (POR) conditions and defined seven floating parameters: trench depth, trench bottom width, trench middle width (at variable depth), trench top width, sidewall roughness, bottom roughness, and a parameter to vary the depth location of the middle width. We simulated individual OCD channels, spectral ellipsometry and spectral reflectometry measurements, and both channels together (see Figure 6). Based on results of these simulations, we concluded that combining both channels together gives the benefits that normal-incidence channel has for trench depth and that the spectral ellipsometry channel has in sensitivity to bottom CD and top



➤ Figure 9. Repeatability performance.



➤ Figure 10. Multi-layer metallization stack measurement.

CD. It is clear that one can measure all the key parameters impacting device yield and performance at the trench etch step using OCD metrology, due to the low predicted parameter of uncertainty and the degree of correlation.

Pursuing picosecond ultrasonics

The third of the three process control techniques that we are recommending for producers of SiC power electronic devices is picosecond ultrasonics, a pump-probe technique using ultrafast laser pulses, typically with a duration of 200 fs. This is a very well understood and documented technique that involves focusing a pump pulse to a tight spot on the device surface, leading to the generation of a sharp acoustic wave. The resulting traveling acoustic wave reflects off various interfaces, and when it returns to the surface it changes surface reflectivity, which is measured by the time-delayed probe (see Figure 7, which provides a plot of surface reflectivity as a function of the optical probe-pulse time delay).

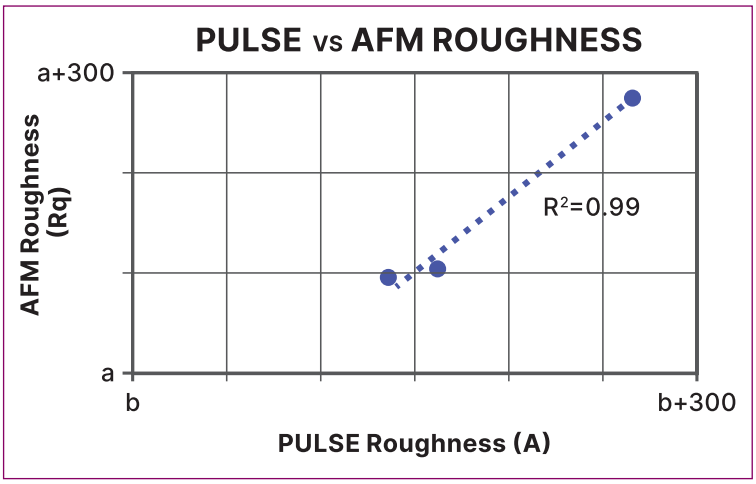
Picosecond ultrasonics reveals a lot of information about the material, with raw data including contributions from electronic, thermal and acoustic components. The thickness of the material may be extracted from this acoustic signature using the arrival time of the echo, and the longitudinal speed of sound in the material. Other properties such as roughness, density and elastic modulus can be characterised, depending on the application.

To provide a more thorough materials characterisation, the set-up can be used for time-domain thermos-reflectance measurements. Thanks to recent improvements in hardware, the thickness and the thermomechanical properties of a material can be characterised with a single configuration. With this non-destructive technique, chipmakers can measure multi-layer metal films simultaneously, and discriminate individual layers of repeating metal. As mechanical and thermal properties can be obtained quickly on micrometre-scale regions, spatially mapping is possible.

Showcasing the power of this technique for SiC power device manufacturers, we have used it to obtain the ohmic contact and conduction metal layer thicknesses of source and drain contacts of a SiC trench MOSFET. These measurements are highly valued, because they have a direct impact on contact resistance. In addition, the metal thickness uniformity impacts device reliability, and the metal roughness contributes to its contact resistance, due to the presence of crystallographic defects, such as micropipes, stacking faults and basal plane dislocations, as well as damage from etching and polishing steps.

Thanks to the advantages of picosecond ultrasonics, it is rapidly replacing more traditional methods such as four-point probe methodology, a destructive technique that only offers indirect thickness information and cannot detect missing layers or misprocessed wafers. Using picosecond ultrasonics, makers of SiC power devices can have far greater metallisation process control, with monitoring that includes the contact barrier (Ti/TiN), trench metallisation (W-based contacts), and both frontside and backside metallisation (Ti/NiV/Ag) stacks.

To illustrate such capability, we have produced wafer uniformity maps of a multi-layer metal stack (Ti/NiV/Ag), shown in Figure 8. Using a spot size



➤ Figure 11. The correlation of PULSE measurement to transmission electron microscopy (TEM) and atomic force microscopy (AFM).

There is no doubt that power devices based on wide bandgap materials, such as SiC, are the future of the power electronics industry. Thanks to their superior properties, enabling performance enhancements over silicon-based devices, sales are climbing fast

of just 8 μm by 10 μm and a rapid measurement time – it is less than 4 s per site – it is possible to characterise full wafer uniformity. Selected metal layer stacks are highlighted in Figure 9.

We also offer an example of measurements of repeating metals in a multi-layer stack, in this case Ti/Al/Ox/Ti/Al (see Figure 10). The raw data shows an excellent signal-to-noise ratio, with echoes from every layer clearly resolved. Note that competing techniques, such as X-ray metrology, cannot provide details of individual layers in such a stack, while measurements on blanket films are not representative of product performance. To assist those running SiC fabs, recipes can be set up to flag missing layers or detect misprocessing.

As mentioned previously, in addition to thickness, picosecond ultrasonics can monitor roughness, especially for thick films (hundreds of nanometres to the micron range). Roughness provides a qualitative indicator for monitoring a well-established process. Illustrating this capability are measurements from an aluminium film (see Figure 11).

The road ahead

There is no doubt that power devices based on wide bandgap materials, such as SiC, are the future of the power electronics industry. Thanks to their superior properties, enabling performance enhancements over silicon-based devices, sales are climbing fast. According to Yole Group, global revenue will reach $6 billion by 2027. Much of that will come from the automotive industry, with Yole forecasting SiC will represent approximate 80 percent of that market.

High yield, high-volume production of SiC power devices is far from trivial. There are challenges associated with process control, which is needed in many of the key steps in the fabrication process. Offering tremendous assistance are FTIR, OCD and picosecond ultrasonics metrology – all provide SiC power device manufacturers with options to address these obstacles. And once these obstacles are removed, the highway is largely clear for high-volume manufacturing of SiC power devices.

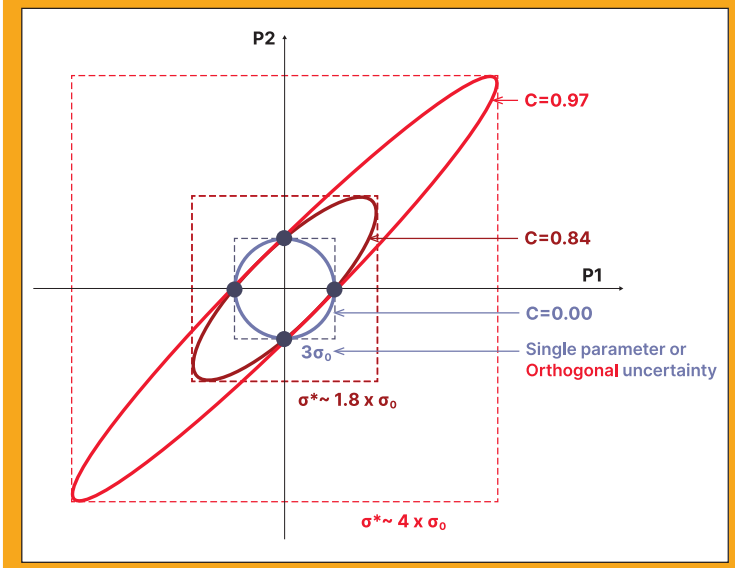
The author of this feature would like to thank the following members of the Onto Innovation team for their contributions to this article: Priya Mukundhan, Aseem Srivastava, Zhuan Liu, Andy Antonelli, and Robert Fiordalice.

Uncertainty and sensitivity analysis

IF OCD is to be employed for process control, it is critical to apply uncertainty and sensitivity analysis. This is the primary method for model optimisation and feasibility simulations, and is based on Bayesian analysis.

One input is spectral noise, which is derived from real measurements and is representative of all sources of system noise, including light source variability, detector shot noise and positional uncertainty. Another input is spectral parameter sensitivity. This is given by the partial derivative, or Jacobian, of each spectrum, with respect to each floating parameter and any weighting used in the fitting function. The output of the analysis comes in the form of a probability density function of the parameter uncertainty, given as a standard deviation.

In addition, the analysis provides an orthogonal uncertainty, or O-sigma, which is essentially parameter uncertainty from noise alone, and a degree of correlation. The latter is defined as the coefficient of multiple correlation, where the correlation between the given parameter and all other floating parameters are considered for each parameter. The figure below illustrates the impact of parameter correlation on parameter uncertainty. This plot reveals the change in the probability density function of two parameters as correlation is increased.



➤ The impact of parameter correlation on parameter uncertainty.

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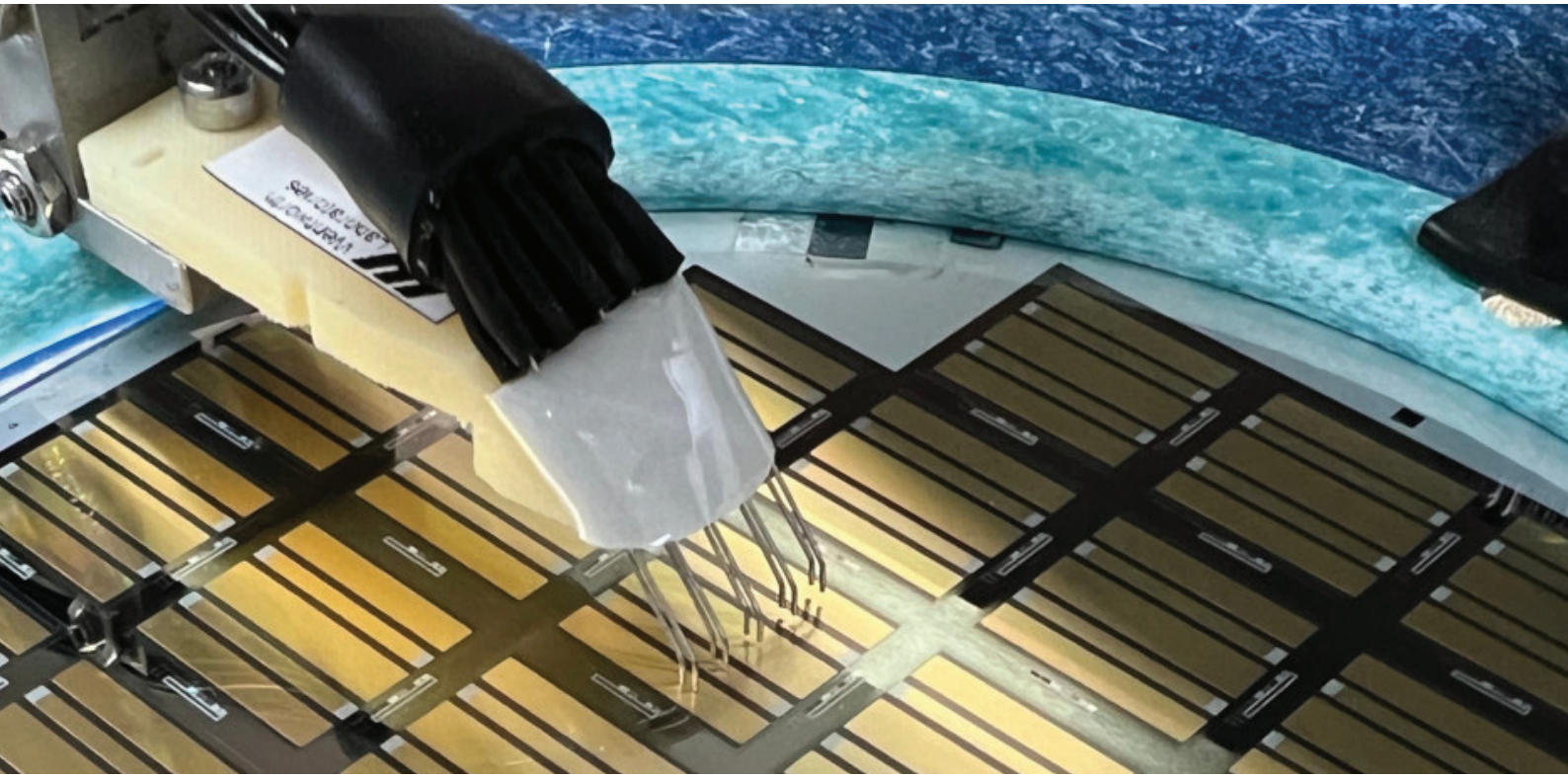


B-TRAN: a first for silicon-based high voltage bidirectional switching

The Bidirectional Bipolar Junction Transistor (B-TRAN) is a new kind of device that offers a significant performance improvement over conventional power switches. **IDEAL POWER** explores the performance and operation of this novel technology.

WITH ADVANCES in electric vehicles and renewable energy technologies, bidirectional switches have become important to solve four quadrant operation applications. For example, the performance of certain topologies employing bidirectional switches, such as Vienna Rectifiers, T-Type Inverters and Matrix Converters, would benefit considerably from a more efficient bidirectional switch.

B-TRAN is a novel four-quadrant power switch with ultra-low forward voltage and low switching losses that can be used in both unidirectional and bidirectional switching applications. Crucially, it offers a significant performance improvement over power switches such as SCRs, IGBTs and MOSFETs, as implemented in silicon or wide-band-gap materials such as SIC. The total power loss is also much lower than that of IGBTs, particularly in bidirectional applications. Ideal Power has already received over 75 patents worldwide for B-TRAN topology and its method of operation.

B-TRAN device construction and operation

B-TRAN is strictly symmetrical and bidirectional in nature and has a positive temperature coefficient. The unique process innovation allows for dual-sided device fabrication for a monolithic vertical device. B-TRAN architecture in silicon with symmetrical structure is demonstrated in Figure 1.

First-generation B-TRAN devices produced in a commercial foundry, achieved performance of 6mΩ on-state resistance, which is state-of-the-art for a bidirectional switch in silicon.

They also demonstrated excellent low die-to-die variability, laying a solid foundation for current sharing control in power modules called SymCool which have four B-TRAN single die in parallel.

SymCool packaging impedance is as low as 0.4 mΩ and 10 nH at 35 kHz for a 1200V/160A rated power module, with a unique Kelvin Source designed to reduce gate-source loop inductance.

Finally, the SymCool bidirectional power module's performance demonstrated 4mΩ resistance @ 160A thanks to the B-TRAN die's ultra-low VCE(ON) and careful design of the interconnections and module

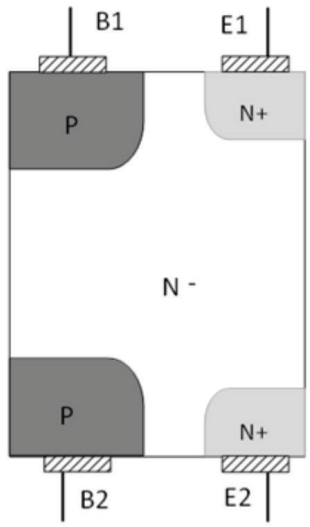


Figure 1. B-TRAN architecture in silicon with symmetrical structure

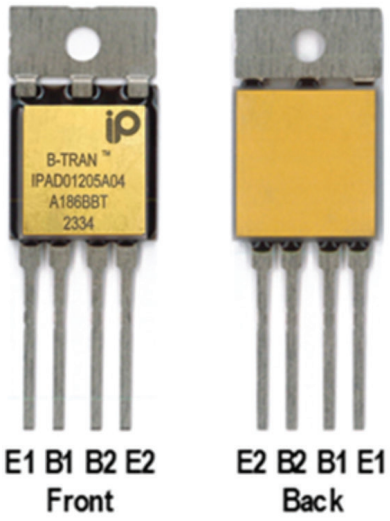


Figure 2. B-TRAN Discrete TO-264 Package

Figure 3. SymCool B-TRAN Power Module

material. Figure 2 shows a B-TRAN discrete TO-264 package. Figure 3 illustrates the SymCool B-TRAN power module.

B-TRAN is a normally-on device with the load current flowing between E1 and E2 terminals. To operate the B-TRAN die as a normally-off device, a low voltage (<60V) cascode MOSFET is connected below E1 and E2. The B-TRAN operation states are shown in Figure 4.

- To turn off the device with the top E1 connected to high voltage (1200V), cascode FET Q2 is opened and B2 is connected to ground. The depletion region from E1 to B2 blocks the high voltage.
- To turn on the device, the top B1-E1 terminal is driven with a voltage of ~1.5V to drive current into the base terminal B1. By adding the positive bias, the minority carriers are injected into the drift region, increasing the carrier density in the N- drift region, so the resistance between the top E1 and bottom E2 is significantly reduced. Q1 and Q2 are turned on to allow the current flow.

B-TRAN Performance

The single-die conduction loss characteristic is illustrated in Figure 5. With a 50A-load current at a junction temperature of 25°C, $V_{CE(ON)}$ is only 0.36V. The conduction loss for the single die is only 18W. Typical device I_c-V_c curves for different load currents and associated driving currents at 25°C and 175°C are shown in Figure 5 and Figure 6, respectively. As the junction temperature increases to 175°C, $V_{CE(ON)}$ increases, and the driving current needs to exceed 10A to get the load current of 50A.

Characterisation demonstrates a positive temperature coefficient in Figure 7. The higher the temperature, the lower the I_C, which is preferred for multiple die-in-parallel power module design. Typical switching energy including Eon, Eoff and Esw at different junction temperatures at 800V/ 100A is displayed in Figure 8. The higher the temperature, the higher Eon and Eoff. Esw does not change significantly with junction temperature. The single die was also successfully operated at much higher voltage and current up to 600V/200A.

B-TRAN applications and future developments

In addition to excellent bidirectional conduction and blocking capabilities, B-TRAN can also be used for a wide range of unidirectional switch applications, such as replacing IGBT+reverse diode and MOSFETs in switching applications. The B-TRAN die can also be optimised for high-speed switching applications (HS variant). Initial simulations and experiments of a high-speed variant (HSx) have shown a much-improved turn-on and turn-off time with only a slight increase in on resistance.

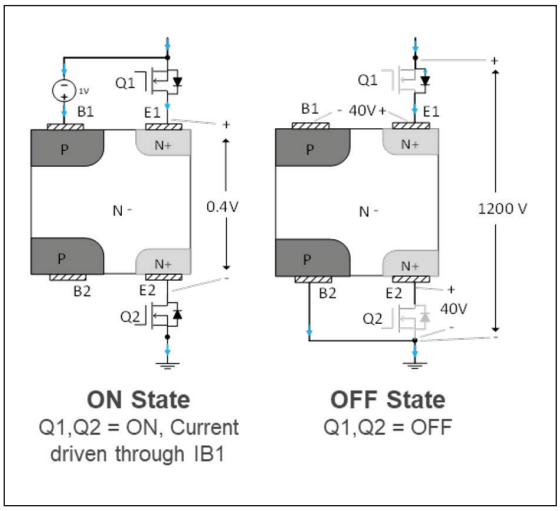
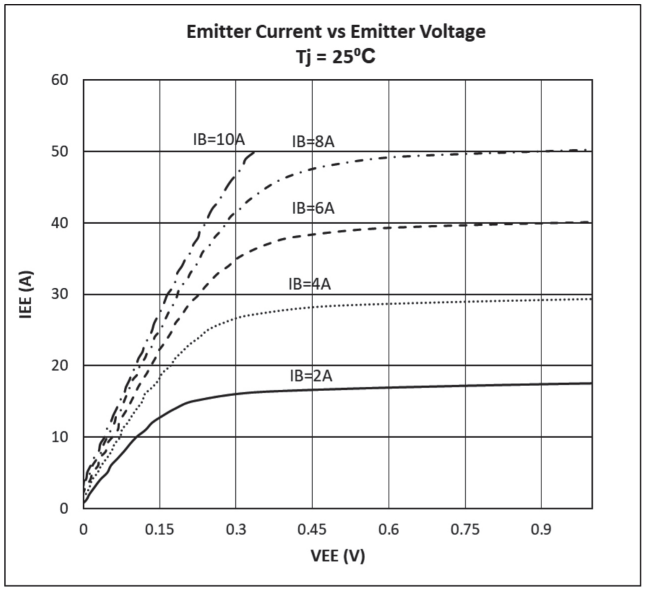
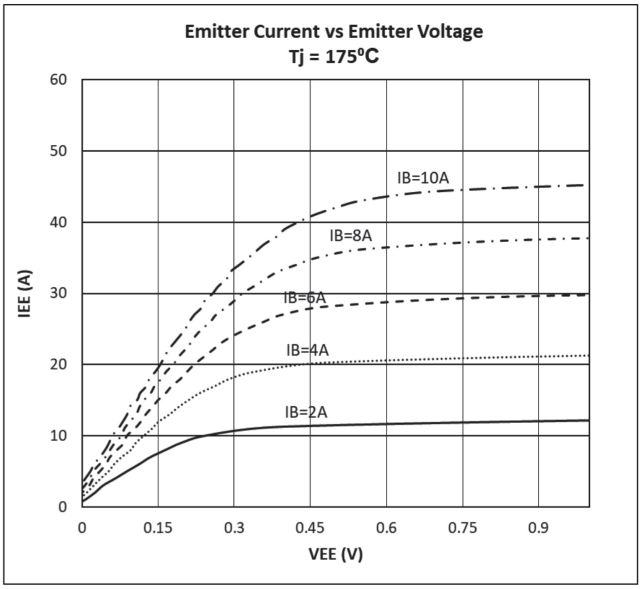


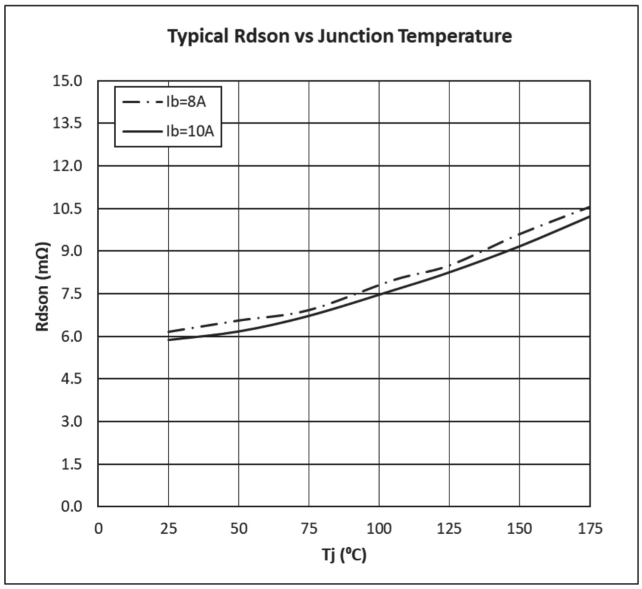
Figure 4. B-TRAN operation states



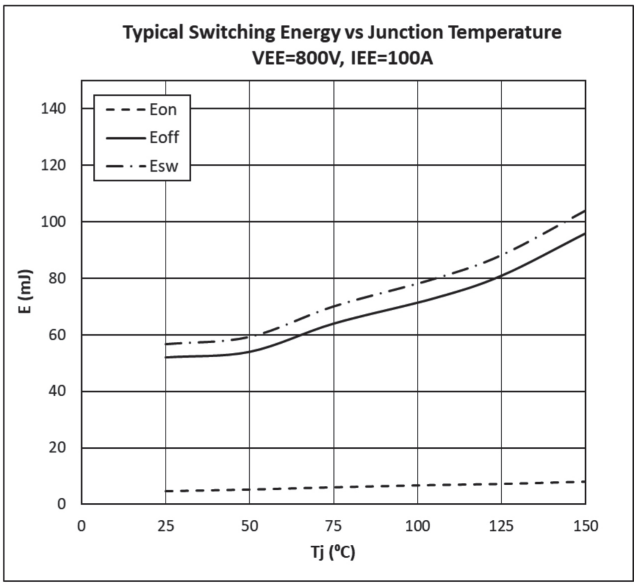
➤ Figure 5. Single die I-V curves for different load currents and associated driving currents at junction temperature 25°C



➤ Figure 6. Single die I-V curves for different load currents and associated driving currents at junction temperature 175°C



➤ Figure 7. B-TRAN positive temperature coefficient



➤ Figure 8. Typical switching energy including E_{on}, E_{off} and E_{sw} in different junction temperature at 800V/100A

The SymCool bidirectional power module has significant advantages and can serve as direct replacement in solid-state circuit breakers, T-Type inverters, and other similar applications using Common-Emitter/Collector devices.

SymCool can also be designed with high-speed die (HSx) for switching applications. With its ultra-low losses and double-sided cooling package, the design and volume requirements of the heat sink for the SymCool power module are eased. Forced air cooling or natural convection with heat sinks on both sides is sufficient for most applications. This results in substantial system volume and cost savings.

The B-TRAN device performance and tight process control in a commercial foundry has laid a solid foundation for the bidirectional multi-die power module design. SymCool, the first power module designed with B-TRAN, offers a bidirectional 4mΩ switch @ 160A, which is one of the lowest in the industry.

Ultra-low losses along with the natural ability to design a double-sided cooled package due to symmetrical die design offers many advantages compared to other solutions. With die optimisations to increase the switching speed, the range of applications of B-TRAN will increase.

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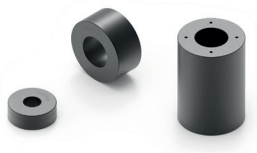

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GaN: A natural playing field for innovation

GaN companies are re-purposing developments made in silicon over the past 70 years, while exploring new avenues for innovation and integration.

PROFESSOR FLORIN UDREA, CTO OF CAMBRIDGE GAN DEVICES, gives his personal view on the extraordinary potential of GaN.

THERE ARE MANY WAYS to define innovation but the Greeks are always a good place to start. Philosopher Socrates advised: “The secret of change is to focus all of your energy, not on fighting the old, but building on the new.” Addressing the same theme from a different angle, Albert Einstein is alleged to have said: “The definition of insanity is doing the same thing over and over again but expecting different results.”

I personally believe in creating a culture of innovation — one of the founding principles of our company. If an organisation encourages creative thinking from all its employees, new ideas will emerge, challenging the old, traditional ways. Creativity sparks further creativity and great strides can be made.

All my experience - and my instinct - tells me that innovation results from a deep knowledge base. Before Cambridge GaN Devices, I ran a team at Cambridge University for more than 30 years researching different materials and technologies. Many ideas - different configurations, contexts and geometries - that were developed for silicon are now being applied to GaN. For example, superjunction technology and membrane technology are re-emerging as possibilities for GaN.

Of course, there are brand new concepts that have been developed purely for GaN too. It is this thorough and detailed understanding and appreciation of materials and device physics that is enabling new power applications based on GaN.

With our background, GaN was a natural playing ground. It is a very interesting material, but of all the materials I have studied - silicon, SiC, diamond, GaN - by far the most difficult is GaN.

GaN is not only a wide bandgap material but its incorporation in a heterojunction is what makes it special. Indeed, the use of a GaN/AlGaN structure, enables an interface quantum layer (2DEG) with concomitantly high electron charge (~ 1e13cm^{-2}) and high mobility (~1700 cm^2/(Vs)).

So, on one hand, GaN companies re-purpose all the developments that have been made in silicon over the past 70 years, and on the other hand GaN offers new avenues for innovation.

Furthermore, as opposed to SiC, GaN enables integration. So, for example, intelligence, protection and sensing can be produced in GaN and delivered on the same chip as the HEMT. Of course, this is also possible in silicon, but only at low power. GaN permits integration at much higher power levels and much higher frequencies.

Will GaN replace silicon in other markets? Well, for applications where high power and high frequency are required, GaN is the best material. But digital electronics will remain based on silicon, because

silicon has both n-channel and p-channel transistors and can be scaled down to nm levels.

GaN has the 2DEG structure which is fantastic for making an n-channel transistor, but today there is no reliable equivalent hole gas structure that would enable the creation of a p-channel transistor in GaN. And because recombination times are very small, bipolar devices are also not possible in GaN, Therefore, for the time being at least, GaN's best prospect is as HEMT device only. But for this purpose, GaN is a fantastic, marvellous material. It will be used for power applications from maybe 40V to about 1.2kV and is going to dominate in high-frequency applications. GaN is also interesting for RF and there are opportunities in optical applications such as LEDs.

A novel and innovative approach to the GaN market

Cambridge Gan Devices (CGD) has taken a completely novel – innovative – approach to the GaN market: we optimise the use of GaN integration. CGD adds intelligence, sensing and protection, making the gate extremely reliable, but at the same time keeping the simplicity of a highly efficient transistor.

This approach supports the two claims we make about our ICeGaN GaN technology: that is easy to use, because our transistors can be driven in the same way as a silicon or silicon carbide device; and that it matches or even surpasses the reliability of silicon and silicon carbide.

Let's break that down a little.

Unlike other companies that try to integrate the actual HEMT driver with the HEMT itself in one IC, CGD integrates the Miller Clamp and HEMT and an auxiliary device to regulate the voltage from a control pin (external gate) to the actual gate of the HEMT.

The Miller Clamp regulates dv/dt which is the most critical and complex issue to handle when driving a GaN HEMT. This also allows more relaxed design rules regarding how far the driver can be placed from our ICeGaN device.

Given the above, it is perfectly possible to take a standard silicon MOSFET driver IC and use it to drive CGD's ICeGaN HEMTs without any extra circuitry. To get the best performance from an ICeGaN HEMT however, especially at high frequency, an optimised driver will be required, but all the complex slew rate design issues have been solved.

The reason that CGD chooses not to integrate the full driver circuit is because to optimize performance, a power electronics designer must match the driver to work with their preferred controller. Also, the driver may also be used for three phase or multiple devices.

An ICeGaN H2 HEMT

Instead of making a very complex, and perhaps sub-par, power IC that cannot be made to function optimally because of the lack of GaN p-channel transistors (meaning, for example, that it is not easily possible to integrate a totem pole type driver) CGD has chosen to perfectly integrate the essential elements that are required to make the transistor easy to use, and very reliable. Finally, if the driver and HEMT were to be fully integrated, they would also be connected thermally, leading to performance and reliability issues.

The reliability challenge is complex. Intrinsically, GaN is at least as reliable as silicon, perhaps even more so, because the intrinsic carrier concentration of GaN is very small, therefore lower leakage currents are possible. But silicon has one huge advantage: the presence of the silicon oxide. The silicon/silicon oxide interface is close-to-perfect (described by my teacher as 'God-given') when used to make an insulated gate. With GaN, the interface is not so good, so a p-type magnesium dopant is used to create the the so called 'p-GaN gate'. Unfortunately, this limits the threshold of most GaN gates to around 1.3-1.6V, unless accompanied by an undesirable and significant increase in the specific on-resistance.

Another innovation that CGD has introduced in ICeGaN roughly doubles this gate threshold voltage to 3V. An auxiliary HEMT, integrated alongside the main switch and the Miller Clamp, is connected in a pass configuration between the external gate and the internal gate. The Miller Clamp addresses the fast dv/dt challenge, while the auxiliary HEMT

The reliability challenge is complex. Intrinsically, GaN is at least as reliable as silicon, perhaps even more so, because the intrinsic carrier concentration of GaN is very small, therefore lower leakage currents are possible. But silicon has one huge advantage: the presence of the silicon oxide

➤ The CGD team with CEO Giorgia Longobardi holding the trophy that was awarded to the company for "Best Demo" at the Innovation Zone of TSMC's 2023 Europe Technology Symposium.

delivers a higher threshold voltage and extends the gate voltage both in static and dynamic conditions. This means that there is no need to use a negative rail that makers of other GaN devices recommend employing when turning the transistor off to avoid retriggering the transistor. By negating the need for negative voltage rails – which have been shown to cause degradation over time – ICeGaN devices can be driven from 0-10V, 0-15V or 0-20V as preferred by the user, in the same way as silicon and SiC devices.

Robustness

Independent research by Virginia Tech University has also demonstrated that CGD's technology is more robust than other GaN platforms. Experimental evidence presented in a paper at APEC 2023, titled 'A GaN HEMT with Exceptional Gate Over-Voltage Robustness', shows that ICeGaN HEMTs exhibit an exceptionally high over-voltage margin of over 70V, which is comparable to state-of-the-art traditional silicon devices.

Accidental high drive voltage is a critical concern for the gate reliability and driver design of GaN HEMT devices. Previously, other GaN HEMTs survived to around only 25V, which can be well within gate voltage overshoots in applications such as converters, resulting in device failure. Moreover, under repetitive gate voltage spikes, a discrete GaN device may see degradation well below the 25 V, as demonstrated by Virgina Tech. Until ICeGaN, higher dynamic breakdown voltage values of 70V and more, were only possible with state-of-the-art SiC and superjunction devices. ICeGaN's hugely elevated dynamic gate breakdown capability is enabled by the integration of protection circuitry as discussed earlier.

Concluding the discussion on reliability, CGD has addressed the issue of very low temperatures, where GaN can fail. Even if a steady voltage is maintained on the outside gate, the inner terminal of the transistor will vary with temperature. So at lower temperatures, ICeGaN's 'Smart Robustness ' integrated protection circuitry clamps the device harder, to make it more reliable. No other GaN company offers this solution.

Innovation is one of the core pillars that Cambridge GaN Devices is based upon, and it runs through every aspect of our business, not just technology. This approach, I believe, often works better in small companies that are more dynamic and do not have the burden of previous business history and expectations.

For example, we have no fear of killing a profitable superjunction business with new GaN products because we don't have those legacy devices. We have one mission, which is to deploy GaN. To achieve this, all ideas are considered...and hence we are extremely open to innovation.

> Even if a steady voltage is maintained on the outside gate, the inner terminal of the transistor will vary with temperature

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Giving gallium oxide avalanche capability

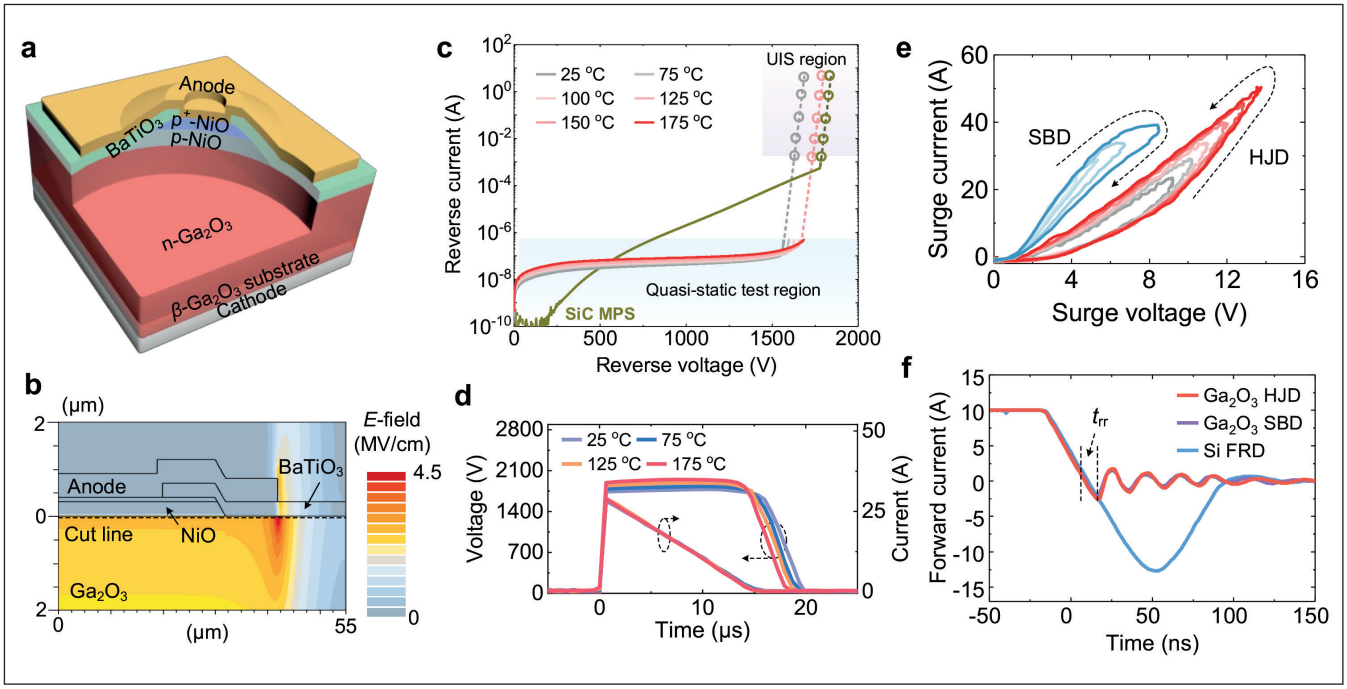
Pairing Ga_2O_3 with NiO produces robust power electronics for harsh environments

BY FENGZHOU AND JIANDONG YE FROM NANJING UNIVERSITY AND YUHAO ZHANG FROM VIRGINIA TECH

ADVANCED POWER DEVICES are essential building blocks for high-efficiency energy conversion in a number of applications, including electric vehicles, data centers, electric grids and renewable energy processing. To reach higher levels of performance with these devices, the ultimate driving force is the selection of the semiconductor material. The last decade has witnessed the success of wide bandgap semiconductors, such as GaN and SiC. Compared to silicon, these alternatives have raised the bar. But even more impressive devices are now on the horizon, drawing on the superior strengths of ultrawide bandgap semiconductors, such as Ga_2O_3, diamond and AlN.

Regardless of the material used, the primary function of the power device is to operate as a switch between a high blocking voltage and a high conduction current. Due to this requirement, the ability to handle overvoltage and overcurrent events is indispensable for any power device. Armed with that attribute, power devices can temporarily survive common faults in power systems – they could be short circuits, excessive loads, or arc/ground faults – before protection circuitry intervenes.

Traditionally, avalanche and surge current capabilities have been realised with homogenous *p-n* junctions. However, this architecture has proven



➤ Figure 1. (a) Three-dimensional illustration of a fabricated NiO/Ga_2O_3 hetero-junction diode. (b) Simulated in-plane electric-field contour of devices with the $BaTiO_3$ dielectric layer. (c) Temperature-dependent reverse current-voltage characteristics of the hetero-junction diode. (d) Typical temperature-dependent unclamped inductive switching voltage and current waveforms for Ga_2O_3 hetero-junction diodes at an inductance of 1mH. (e) Surge current-voltage locus of the hetero-junction diode and the reference Ga_2O_3 Sckottky barrier diode. (f) Reverse recovery characteristics of the Ga_2O_3 hetero-junction diode, the reference Ga_2O_3 Sckottky barrier diode, and a commercial silicon fast-recovery diode.

elusive in power devices based on ultrawide bandgap semiconductors, because it is incredibly challenging to realise bipolar doping, a requirement for making homogenous junctions.

One way to tackle this challenge is turn to the hetero-integration of foreign *p*-type oxides, such as NiO, which can be paired with *n*-type Ga_2O_3. It's an approach that has been adopted by those of us at Nanjing University. Back in 2020, we broke new ground with the first double-layered *p*-NiO/*n*-Ga_2O_3 heterojunction power rectifier. It's an innovation that enhanced the reverse blocking capability up to 1.86 kV and ensured stable operation at temperatures as high as 440 K. We then built on that success, producing β-Ga_2O_3-based bipolar power devices that combine a high current output with a fast reverse recovery and nanosecond switching. It's a foundation that has put us in a great position to address the most critical avalanche and surge robustness challenges in Ga_2O_3 devices.

For that most recent challenge, we have joined forces with Yuhao Zhang's team at Virginia Tech. It's a collaboration that has borne much fruit, realising an exceptional level of avalanche and surge current robustness in NiO/Ga_2O_3 *p-n* heterojunctions through innovative device design and circuit evaluations.

Architectures for avalanche

For power devices, it is crucial to manage electric field crowding and prevent premature breakdown. Working together, our partnership has addressed this matter by developing an etching-free edge termination technology, featuring a small-angle bevelled double-layered NiO junction termination extension (see Figure 1 (a)). We use an amorphous $BaTiO_3$ layer with an ultra-high dielectric to conformally cover the NiO junction termination extension structure in a consistent manner. Introducing this ultra-high dielectric ensures a nearly uniform electric field at the NiO/Ga_2O_3 junction, and ultimately enables a uniform and robust avalanche (see Figure 1 (b)). For circuit tests, we house a large-area (3 mm by 3 mm) NiO/Ga_2O_3 *p-n* heterojunction device in a TO-220 package.

Power devices with avalanche capability can withstand overvoltage stresses. Such devices are able to accommodate high avalanche current at the avalanche breakdown voltage, and dissipate excessive energy in circuits. The proven capability of our NiO/Ga_2O_3 heterojunction devices comes from rigorous testing, using both quasi-static current-voltage sweeps and dynamic unclamped inductive-switching circuit tests. These investigations reveal that the avalanche breakdown voltage increases with temperature (see Figure 1 (c)), with a positive temperature coefficient of 1 V/ °C – that's a typical manifestation of device avalanche. According to unclamped inductive-switching circuit testing, our device produces textbook-like avalanche waveforms (see Figure 1 (d)). What's more, the temperature coefficient of the avalanche breakdown voltage

extracted from unclamped inductive-switching waveforms is identical to that extracted from current-voltage characteristics.

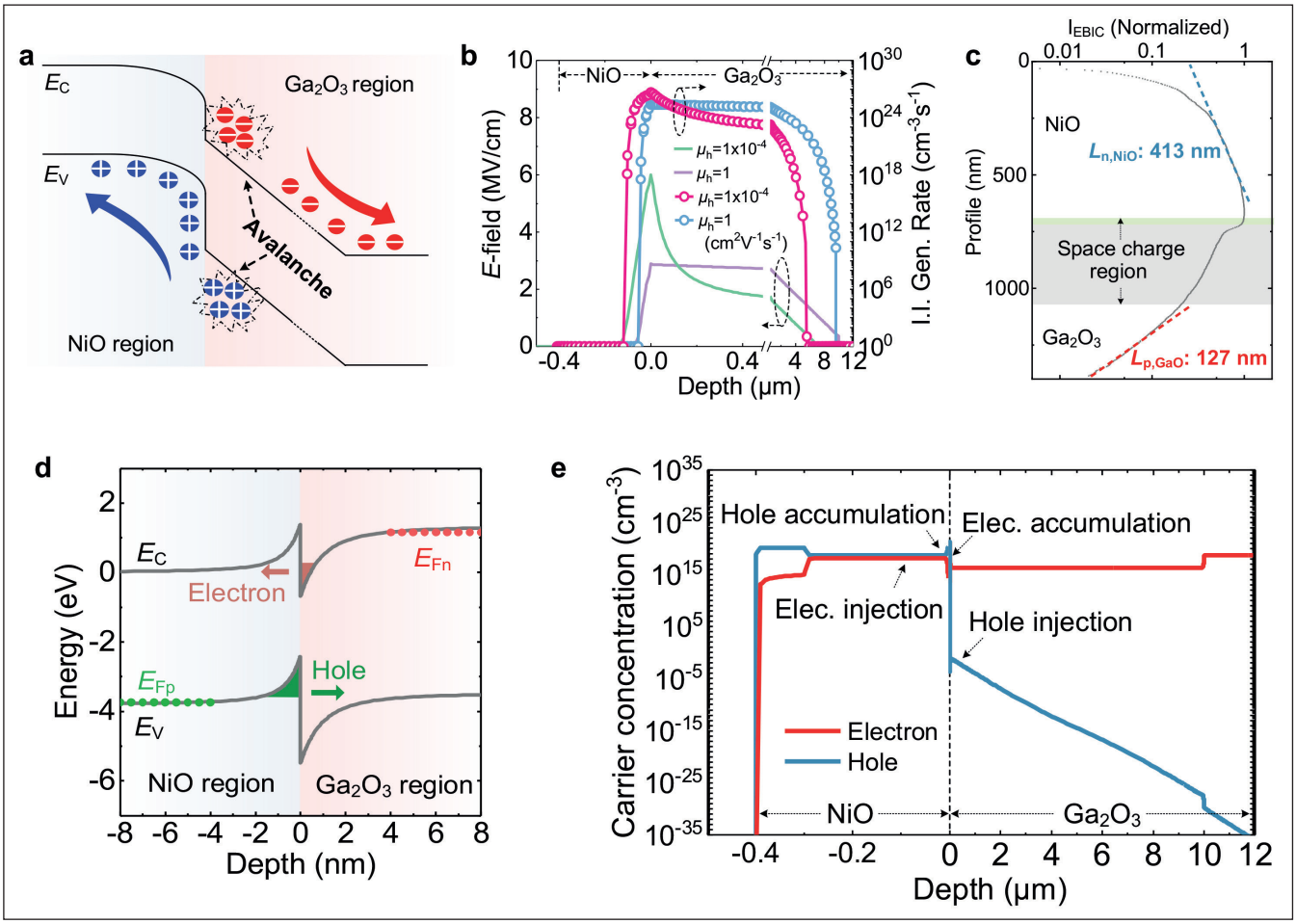
We have provided additional validation of our device's robust avalanche capacity with 1 million cycles of repetitive avalanche tests. This confirms that compared with traditional homogenous *p-n* junctions, our ultra-wide bandgap heterojunctions offer superior performance and robustness for power applications.

In addition to this avalanche capability, our NiO/Ga_2O_3 heterojunction demonstrates exceptional surge current capability, withstanding over 50 A of surge current. In stark contrast to the Schottky barrier diode, the surge current waveforms of our heterojunction device exhibit an anticlockwise locus signature, which signifies negative temperature coefficients for the differential on-resistance (see Figure 1 (e)). Surprisingly, the 1200 V reverse recovery time of our heterojunction device is at the nanosecond level (Figure 1 (f)) – that's similar to the unipolar Ga_2O_3 Schottky barrier diode, and far faster than the bipolar silicon fast-recovery diode. Based on these results, it appears that our NiO/Ga_2O_3 heterojunction can deliver a simultaneous reduction in conduction loss and switching loss, compared with conventional bipolar devices.

Operating under extreme conditions

Thanks to our breakthroughs in avalanche and surge operation, we have been able to delve into the details of fundamental carrier dynamics in these ultra-wide bandgap semiconductor heterojunctions under extreme conditions. This includes high electric fields, high current densities, high temperatures, and non-equilibrium dynamic conditions.

The realisation of avalanche behaviour hinges on impact ionisation and multiplication occurring at the junction, as well as the efficient removal of non-equilibrium carriers that result from impact ionisation. As illustrated in Figure 2 (a), once impact ionisation is initiated in the *n*-type Ga_2O_3 drift layer, the strong electric field sweeps electrons and holes produced by this interaction to the cathode and heterojunction, respectively. Due to the staggered



➤ Figure 2. (a) Illustration of the band diagram and carrier transport dynamics under the avalanche condition. (b) Simulated profiles of the electron and hole concentration, electric field and generation rate in the hetero-junction diode under two different hole mobilities, at an avalanche current of 30 A. (c) Electron-beam-induced current profile of a NiO/Ga_2O_3 heterojunction to determine the minority carrier diffusion lengths. (d) Illustration of the carrier transport dynamics under the high forward current. (e) Simulated distribution of minority carriers on both sides of the hetero-junction diode at a forward voltage of 6 V.

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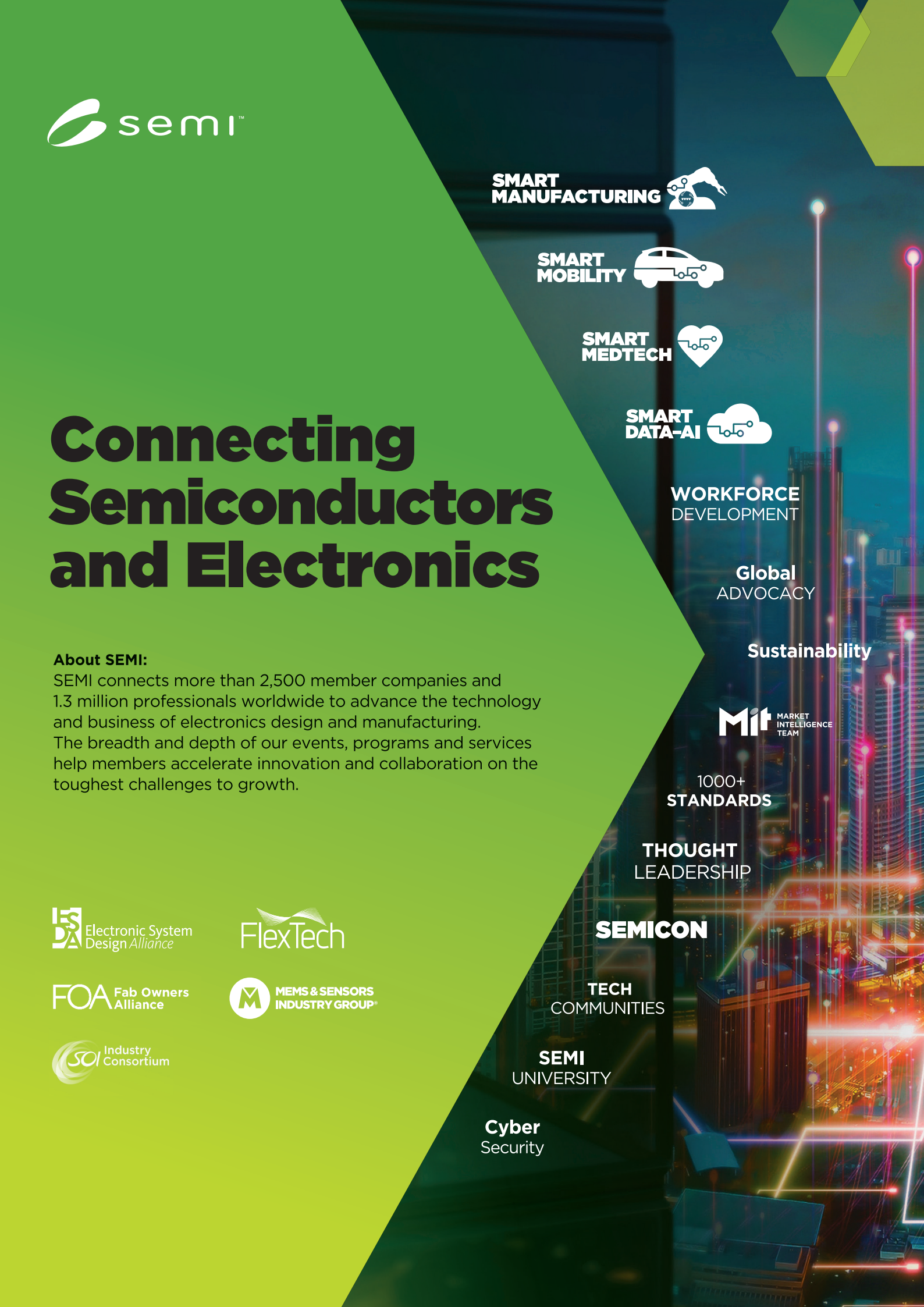

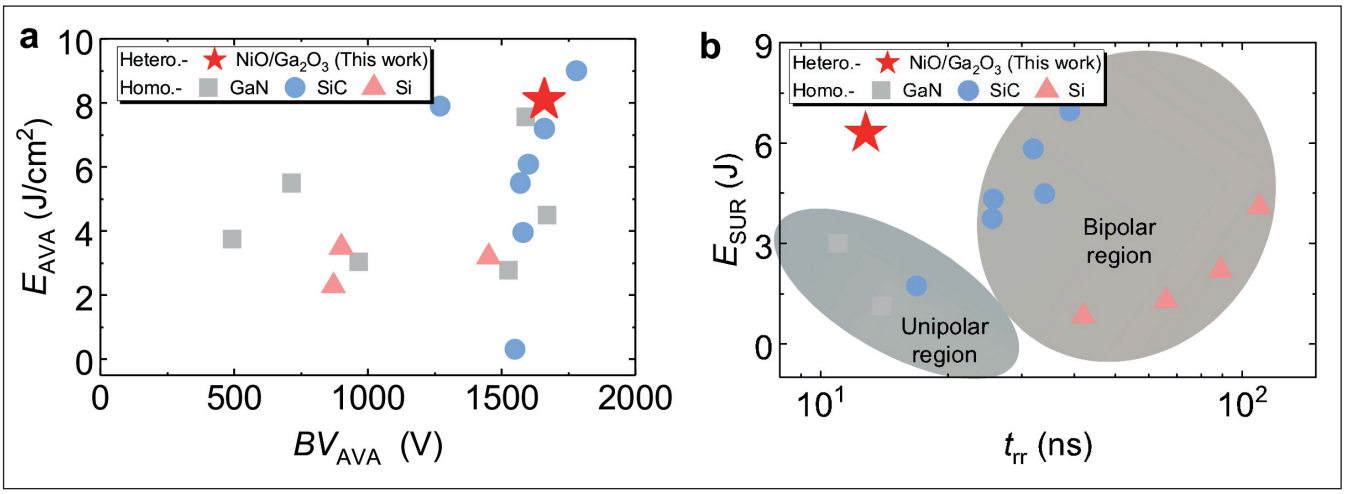

➤ Figure 3. (a) Electric field at avalanche versus avalance blocking voltage benchmark and (b) surge energy versus reverse recovery time (t_{rr}) benchmark, all for reported Ga_2O_3, GaN, SiC, and silicon power diodes.

band structure, the NiO/Ga_2O_3 heterojunction produces no barriers to hole transport.

We have simulated the behaviour of our devices. These calculations suggest that holes produced by impact ionisation in Ga_2O_3 are exempt from controversial self-trapping, and drift with considerable mobility – it is this that enables a high avalanche current. The dynamic avalanche characteristics also allow us to extract a full set of electron and hole impact ionisation coefficients in Ga2O3, which is important for developing solar-blind avalanche photodetectors that could serve in numerous applications.

Yet another advantage of the robust surge capability of the NiO/Ga_2O_3 heterojunction is that it sheds new light on minority carrier (hole) transport in Ga_2O_3, which remains controversial and largely unexplored.

FURTHER READING

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Our efforts on this front, in partnership with researchers at the Australian National University, have involved imaging the minority carrier dynamics in NiO/Ga_2O_3 heterojunction diodes with a microscopic electron-beam-induced current (see Figure 2 (c)). This technique unveiled asymmetric minority carrier lifetimes for electrons in *p*-NiO and holes in Ga_2O_3 of 124.0 ns and 6.2ns, respectively. Based on these values, we expect bipolar conductivity modulation to occur predominantly in NiO at high forward bias, primarily through electron tunnelling injection (this is illustrated in Figure 2 (d) and 2 (e)). When this device is being switched off, depletion mainly occurs in the lightly-doped Ga_2O_3. As minimal minority carriers need to be recombined in *p*-NiO for switching to occur, this has an insignificant impact on device reverse recovery.

Benchmarking

Our NiO/Ga_2O_3 heterojunction sets new performance benchmarks by combining low on-resistance with high current capacity and a high blocking voltage. As summarised in Figure 3 (a), surge current and surge energy capacities surpass those of silicon devices, and are comparable to the best reported performances for SiC and GaN devices. It's important to note that our heterojunction overcomes the fundamental trade-off between robustness and switching speed in conventional homojunctions (see Figure 3 (b)), clearing a path to advancing ultra-wide bandgap devices in power applications.

As well as the opportunities in power electronics, our innovative ultra-wide bandgap heterojunction architecture that features avalanche ruggedness has great potential for realising ultra-low noise avalanche photodetectors in the deep-ultraviolet spectral range. Such devices are expected to break through the fundamental trade-off between responsivity and response speed, a triumph that promises to have far-reaching implications in the fields of optoelectronics and photonics.

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Strengthening the case for Plasma Polish

Three pioneering metrology techniques confirm that the Plasma Polish production process eradicates subsurface damage in SiC substrates while improving crystal quality

BY GRANT BALDWIN AND JAMES SAGAR, OXFORD INSTRUMENTS PLC

BACK IN SEPTEMBER 2022 at the International Conference for Silicon Carbide and Related Materials (ICSCRM), held in Davos, Oxford Instruments, launched Plasma Polish. Originally conceived as either a replacement or a complimentary process to a chemical mechanical polish (CMP), this alternative plasma-based process has been attracting significant interest from leading substrate manufacturers and vertically integrated device manufacturers. Wafers that have undergone Plasma Polish during processing into diodes and MOSFETs have a performance that's in line with industry standard CMP, according to full wafer electrical measurements and yield results (see Figure 1).

The non-contact, dry Plasma Polish process has several key benefits including lower cost, a reduced environmental impact and the ability to remove subsurface damage.

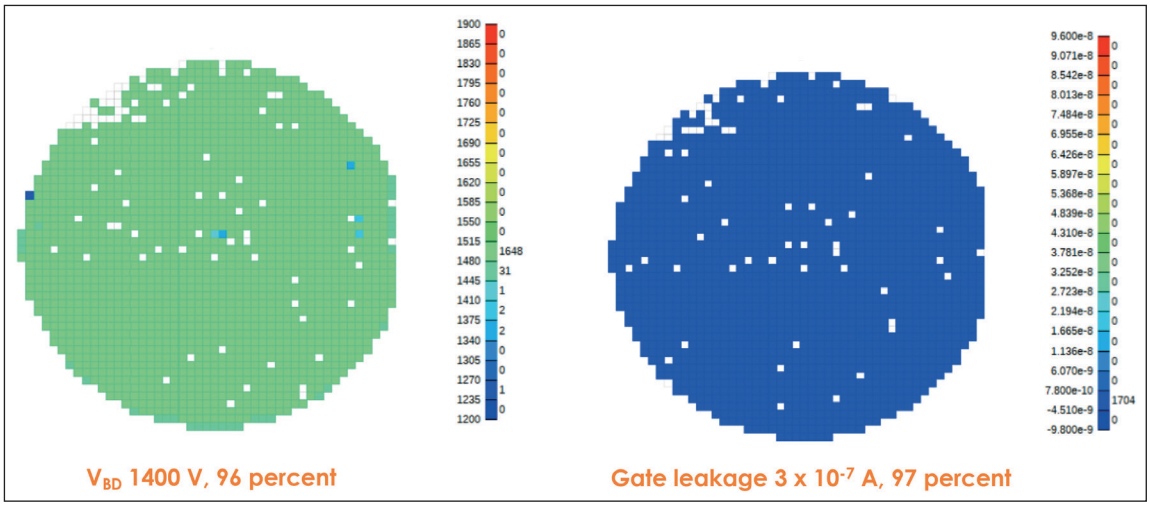
Plasma Polish requires low levels of consumables and creates no toxic slurry, leading to an operating cost reduction of up to 85 percent, resulting from the removal of these process requirements and their associated costs. The absence of the slurry also means that there are no disposal issues and removes the significant water use typically associated with CMP, making Plasma Polish better for the environment. Plasma Polish uses industry standard non-toxic process gasses, making it unproblematic to install in production facilities.

The third benefit, subsurface damage removal, is unique to Plasma Polish. This great strength, discussed in more detail ion pages XX to YY, comes without having to make any changes to either upstream or subsequent processes.

Assessing crystal quality

We originally conceived of Plasma Polish as a technique for preparing SiC substrates for the subsequent growth of epitaxial layers. However, following significant market engagement, including demonstrations on customer material, more and more opportunities are emerging where Plasma Polish provides a solution to surface and subsurface damage.

At this year's ICSRM, held in Sorrento, Italy, we presented data that confirms that Plasma Polish



➤ Figure 1. Plasma Polish achieves a high yield on full-wafer device tests.

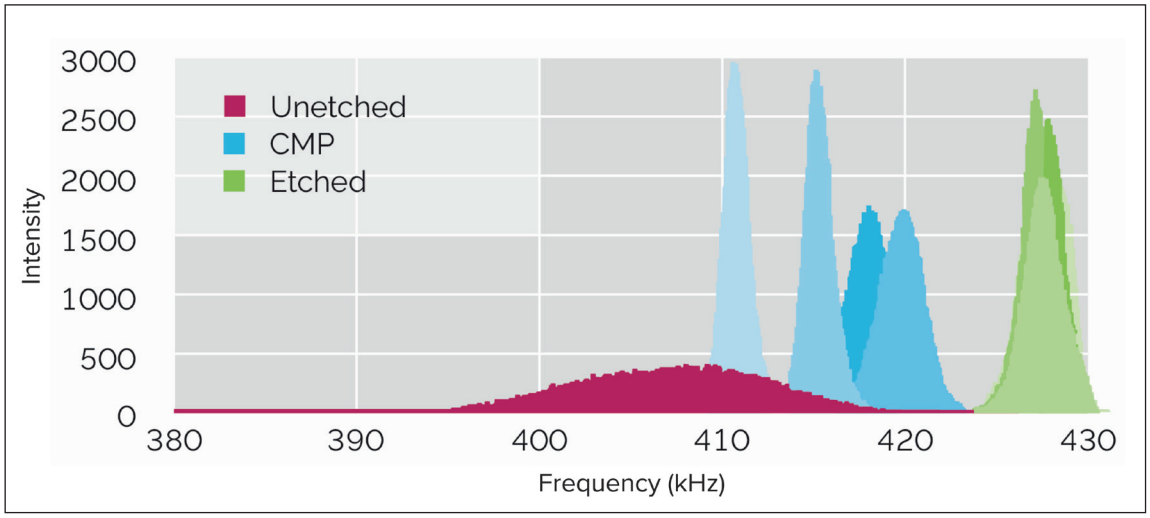
removes subsurface damage. To prove this is the case, we developed breakthrough characterisation techniques by harnessing expertise from many parts of our business. Our validation of the subsurface damage removal capabilities of Plasma Polish comes from three metrology and crystal analysis techniques: contact-resonance atomic force microscopy; electron back-scatter diffraction, which is an electron microscopy-based analytical tool; and Raman microscopy.

Before setting out into the insights provided by these techniques, we'll briefly explain how and why Plasma Polish works. It's a technique that employs physical and chemical mechanisms to access and remove subsurface damage, with the extent of this activity dependent on the chamber design, its configuration and the process recipe. Wafers are processed in a reactor chamber on a radio-frequency-biased wafer stage at a low pressure – this enables the acceleration of the chemically reactive plasma gas onto the wafer surface. As any damaged or defective crystal is inherently weakly bonded, this unique form of plasma etch removes poor-quality material far faster than good-quality, strongly bonded crystal. Consequently, all that remains after a Plasma Polish is higher quality material exhibiting excellent crystallography. In stark contrast, while CMP provides planarisation (flattening), it fails to remove damaged material at a higher rate than good-quality crystal.

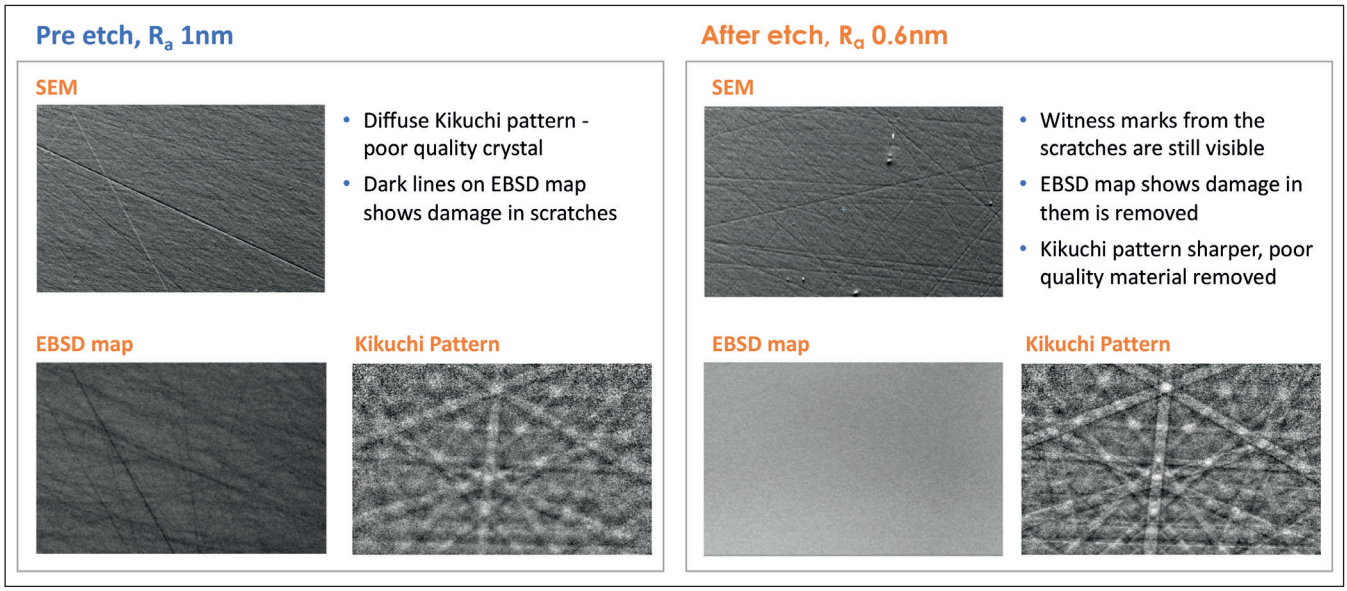
To assess the crystal quality of SiC processed by Plasma Polish, we have turned to a variant of atomic force microscopy known as contact resonance. With this technique, we have mapped the sample surface with a cantilevered stylus that spot-measures the resonant frequency. From this it is possible to obtain a measure of crystal quality as a function of material stiffness, with sharper peaks at higher frequencies equating to higher quality.

We have used contact-resonance atomic force microscopy to compare the crystal quality of incoming unprocessed material and that processed by Plasma Polish. Incoming unprocessed material has a very broad peak at the lowest average frequency, indicating neither good crystal quality nor homogeneity (see the red curve in Figure 2).

To compare SiC processed by CMP and Plasma Polish, we performed four measurements on each wafer: one treated with CMP (Blue), and one treated with Plasma Polish (green). As the blue peaks are



➤ Figure 2. Contact-resonance atomic force microscopy of four unprocessed points of a CMP substrate (blue) and four points of a Plasma Polished substrate (green).



➤ Figure 3. Electron back scatter diffraction (EBSD) images of pre-Plasma Polish and post-Plasma Polish Etch.

narrower than the red, we have concluded that CMP produces an improvement in quality compared with the incoming substrate. However, the four blue peaks are at markedly different frequencies, indicating variation. Meanwhile, the four narrow green peaks have significant overlap, indicating that Plasma Polish improves crystal quality and homogeneity.

The second technique that we have employed, electron back-scatter diffraction, characterises crystallinity and type at a depth of up to a few tens of nanometres. With this form of diffraction, we have produced two images of interest: a Kikuchi pattern at each imaged pixel; and a pattern quality map, revealing the quality of the pattern at each pixel.

For Kikuchi patterns, quality is defined by the sharpness of the diffraction pattern. If it is sharp, this indicates high crystal structure conformality; and if it is diffuse or blurry, it is evidence of either poor structure conformality or more than one SiC polytype. When electron back-scatter diffraction is used, a featureless pattern quality map with a bright colour indicates a high-quality, uniform surface.

When using a scanning electron microscope to scrutinise pre-etch samples and those having undergone Plasma Polish, we obtained images that are actually very comparable, mostly showing topography. This indicates that metrology techniques with more structural specificity are needed to offer greater insight into what is happening at the subsurface. Electron back-scatter diffraction meets this requirement, providing a true assessment of subsurface crystal conformality and polytype purity. Using this technique to study a pre-etched sample yields a pattern quality map with dark lines associated with damaged or amorphous crystal. Once Plasma Polish is applied, electron back-scatter diffraction creates a featureless pattern quality map, indicating improved crystal conformality and purity. The Kikuchi pattern is sharper and of higher quality, thanks to removal of damaged material by Plasma Polish.

Raman microscopy is the third and final SiC substrate characterisation technique we have utilised to assess crystal quality. This form of microscopy, which is incredibly sensitive to local chemical bonds, can penetrate

➤ Oxford Instruments multi-chamber production cluster

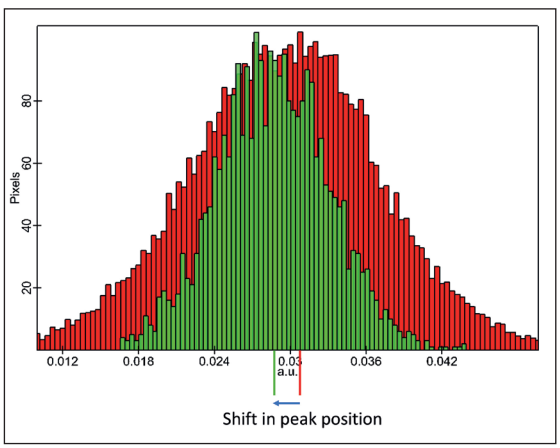
to around 2 μm, thereby enabling the gathering of information from deeper in the crystal. By comparing specific Raman peaks in a spectrum, we are able to assess types of order and disorder. This is accomplished by determining an intensity ratio for two peaks: one peak corresponding to the 4H polytype of SiC, and the other corresponding to disordered Si-C.

We have produced histograms of measured peak ratios after acquiring Raman spectra across a whole SiC wafer (see Figure 4, which has red and green bars for measurements of unetched and Plasma Polish wafers, respectively). The green peak is narrower than its red counterpart and it is closer to the ideal ratio of zero. Based on these observations, we can conclude that Plasma Polish results in a superior crystal uniformity and a higher concentration of 4H SiC, the critical polytype for device production.

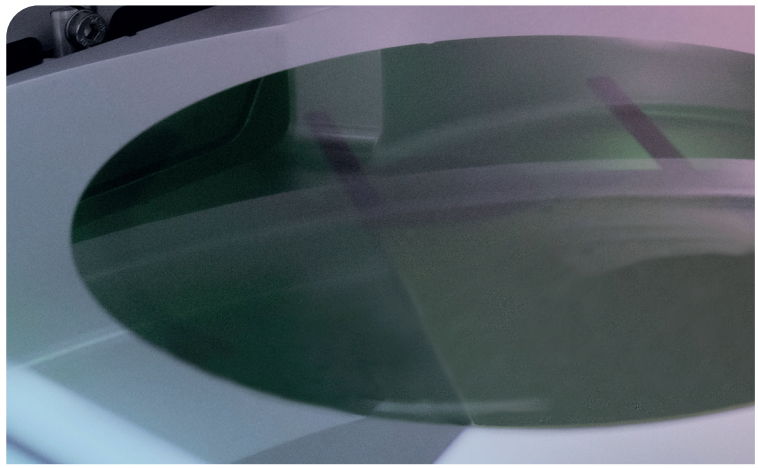
Additional opportunities

As well as replacing CMP, Plasma Polish can work alongside while offering a drastically lower operating cost, no toxic consumable usage or disposal, and a proven capability to remove subsurface damage and increase crystal quality. So, given all these great attributes, how can this advanced solution to preparing SiC substrates for epitaxial growth move forward? Well, there are limitless applications for dry Plasma Polish, where a traditional wet polish process is either not possible, or at least suboptimal. For example, Plasma Polish can rectify substrate bow/warp, optimise device process integration by swapping out wet cleans for dry polishes, reclaim substrates, maintain crystal quality on thicker epilayers for high-voltage devices, improve repeatability with integrated automatic endpoint process control and enable thinner substrates – note that all these opportunities apply equally for 150 mm and 200 mm material, thanks to the innate scalability of our process.

Our Plasma Polish technology forms part of a strong offering to producers of wide bandgap power devices. For the makers of high-end GaN devices, we have an established market-leading atomic layer etch capability to address shallow etch, surface smoothing, and defect reduction challenges. Now there is significant interest to apply this technology to the addressing of issues specific to SiC power device manufacture. For GaN MISHEMTs, we offer atomic layer etch with our Etchpoint technology, in collaboration with LayTec AG. This technology, installed at key Japanese GaN device manufacturers, enables partial AlGaN recess etches with a critical target depth to an unparelled accuracy of ±0.5 nm, for next generation E-mode device functionality. Our other production solution is for GaN HEMT manufacture. The production qualified technology offers high etch rate with repeatable Etchpoint automated switchover to atomic layer etch soft-landing to protect the device-critical underlying layers. In addition, we offer a high-quality GaN atomic layer deposition process with interface optimisation pre-treatment to reduce and remove native oxides and infill nitrogen vacancies. This is qualified and in high-volume production at leading device manufacturers in Japan and the US.

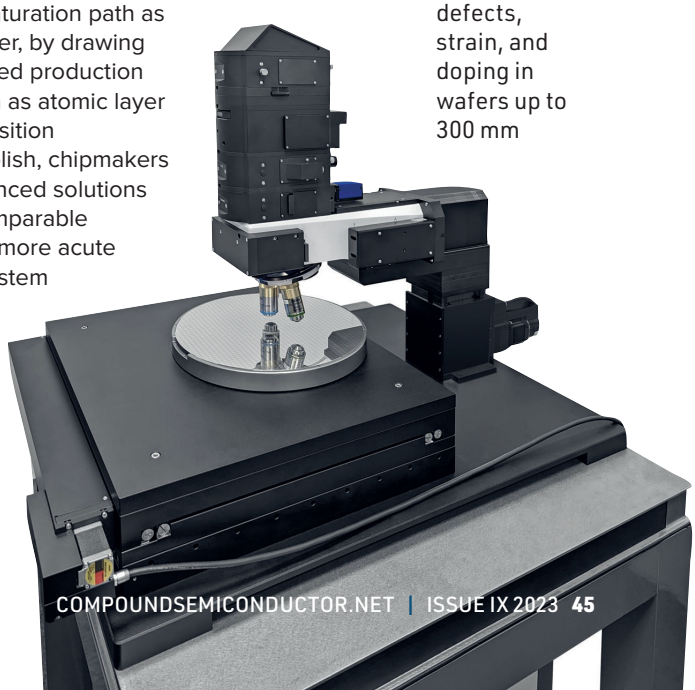


➤ Figure 4. Histogram of SiC peak positions from 2,000 Raman spectra of pre-Plasma Polish (red) and post-Plasma Polish (green).



➤ Successful transfer of 150 mm process to 200 mm wafers

There's no doubt that SiC substrate and device production will follow the same lengthy technology maturation path as silicon. However, by drawing on our advanced production solutions, such as atomic layer etch and deposition and Plasma Polish, chipmakers will have advanced solutions to address comparable but inherently more acute problems that stem from the significant differences in the cost and the properties of these two materials.



➤ alpha300 Raman microscope for characterising chemical composition, crystallinity, defects, strain, and doping in wafers up to 300 mm

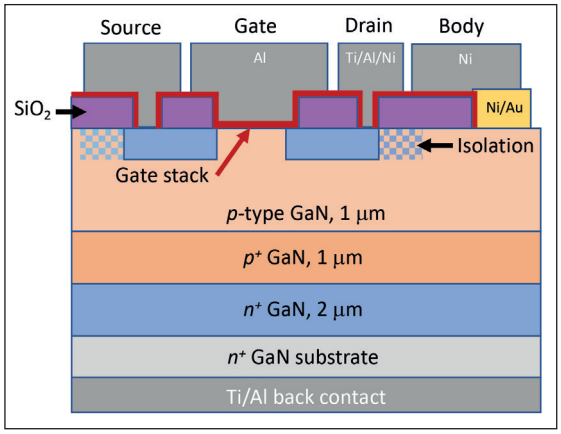
Trimming the on-resistance of GaN MOSFETs

Nitrogen radical treatment, followed by insertion of an AlN interlayer, increases channel mobility in GaN MOSFETs

A TEAM from Japan has reduced the on-resistance of its GaN MOSFETs by a factor of four through the introduction of a nitrided interface.

This advance by engineers from Toyoda Central Labs and the Institute of Materials Systems for Sustainability will help the development of devices that handle high voltages and currents at high efficiencies, a necessity for high-efficiency power conversion systems.

Potential candidates for such systems are a number of vertical device structures, including several forms of JFET. But these devices are held back by a limited gate overdrive, says team spokesman Kenji Ito, who points out that when the gate voltage exceeds 3 V the gate leakage current climbs, due to the forward current of the gate *p-n* diode. To suppress this leakage, there's a need to limit the applied gate voltage – and thus prohibit the use of gate overdrive.



➤ An AlN interlayer and nitrogen-radical pre-treatment increase the mobility of the GaN MOSFET

In stark contrast, MOSFETs have an extremely low gate-leakage current, thanks to the oxide/semiconductor junction that forms the gate structure.

One issue with GaN MOSFETs is that for a channel mobility of 100 $cm^2\ V^{-1}\ s^{-1}$, channel resistance is 0.5 $m\Omega\ cm^2$, a concern at 1 kV or more. Another weakness is insufficient reliability of the gate oxide.

Ito and co-workers are tackling both these issues. Back in 2020 they revealed that the introduction of an AlSiO gate oxide enabled a lifetime of 20 years under 5 MV cm^{-1} at 150 °C. However, the channel mobility was no better than 40 $cm^2\ V^{-1}\ s^{-1}$. Now, thanks to nitridation, they have overcome that limitation, with mobility reaching 200 $cm^2\ V^{-1}\ s^{-1}$.

Fabrication of these transistors began by loading *n*-type GaN substrates into an MOCVD chamber and depositing a stack of epilayers. Post-growth annealing at 850 °C activated the magnesium acceptors. Silicon-ion implantation and annealing created source and drain regions, before nitrogen-ion implantation provided isolation, suppressing leakage between source and drain electrodes. A HF solution then cleaned the GaN surface, removing GaO_x, before plasma-enhanced CVD added a 300 nm-thick layer of SiO_2. Removal of SiO_2 from above the channel followed, prior to plasma-enhanced ALD of a 40 nm-thick layer of AlSiO, acting as the gate oxide, and a 3 nm-thick SiO_2 cap.

In addition to this variant, formed by direct deposition of AlSiO on GaN, Ito and co-workers produced two variants: one with an AlN interlayer between AlSiO on GaN; and a second with that structure, but involving nitrogen-radical pre-treatment prior to deposition of the interlayer.

Devices were completed with 10 minutes of annealing at 950 °C under nitrogen gas and evaporation of metals to form body, source and drain electrodes.

Material profiles obtained with secondary ion mass spectrometry revealed that inserting the AlN interlayer supressed gallium diffusion. It's speculated that this suppression stems from the insertion of the interlayer, which prevents oxidation of the GaN surface during deposition and post-deposition annealing.

Measurements show that the interlayer also benefits effective mobility, which increases from 46 $cm^2\ V^{-1}\ s^{-1}$ to 130 $cm^2\ V^{-1}\ s^{-1}$. An additional hike to 229 $cm^2\ V^{-1}\ s^{-1}$ results from nitrogen-radical pre-treatment.

While the team have used a native substrate for their work, this is not essential, says Ito, because the focus is the oxide-GaN interface. However, as the team is developing vertical GaN MOSFETs, they still have to consider the source-drain leakage through the *p-n* junction under bias stress. "Since the current GaN-on-silicon wafer involves high-density threading dislocations, reverse leakage is a critical problem," points out Ito, who argues that high-quality GaN substrates have an advantage in terms of reliability.

The team is now planning to investigate how to control the threshold voltage of their devices, without compromising mobility. One downside of the interface control technique is a negative shift in threshold voltage, which hampers fabrication of normally-off devices – they are required for fail-safe switching circuits.

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➤ K. Ito *et al*. Appl. Phys Express **16** 074002 (2023)

TiO_2 enhances Ga_2O_3 diodes

Thanks to a high dielectric constant and a favourable band alignment, TiO_2 enables β-Ga_2O_3 diodes to realise a higher breakdown and a lower turn-on voltage

A KEY CHALLENGE facing designers of any power device is to ensure low losses under both forward and reverse bias. While success on these two fronts has proved particularly challenging with β-Ga_2O_3 diodes, progress may be realised by introducing a high-κ TiO_2 interlayer, according to a US team led by engineers at the Air Force Research Laboratory (AFRL). This partnership, which includes researchers at University of California, Santa Barbara, and APEX Microdevices, has recently reported that inserting a TiO_2 interlayer trims the turn-on voltage and leakage current of the Ga_2O_3 diode, and increases its breakdown voltage.

"Time will tell whether this is the most promising topology," says team spokesman Nolan Hendricks from ARFL. "But, at the very least, this topology with TiO_2 can be combined with other diode designs like junction-barrier-Schottky or trench-MOS Schottky diodes to unlock the full potential of Ga_2O_3."

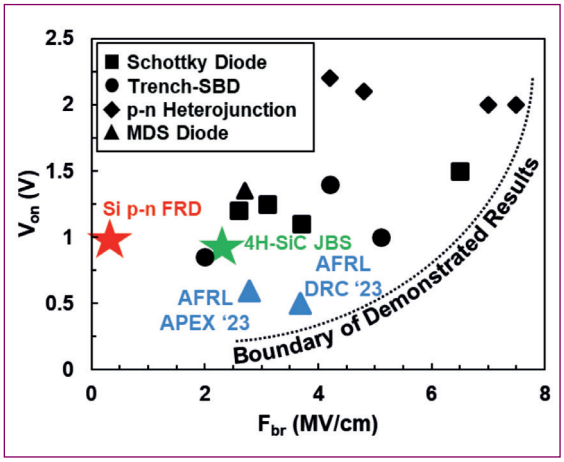
Hendricks and his co-workers are by no means the first team to investigate new device architectures for improving the performance of Ga_2O_3 power diodes.

A number of designs have already been reported that succeed in reducing the off-state current density. They include: trench-based structures, which are hampered by an increase in the specific on-resistance; devices with high Schottky barrier contacts, which cut leakage but increase the turn-on voltage; and diodes with *p-n* junctions that increase the barrier height, leading to higher on-state losses.

Offering more promise, argues Hendricks, is the metal/$BaTiO_3$/Ga_2O_3 structure pioneered by the team at Ohio State University, led by Zhanbo Xia and Siddharth Rajan.

"The metal/$BaTiO_3$/Ga_2O_3 structure gave a very large turn-on voltage due to a slightly positive conduction band offset, but the fundamental concept they conceived of was quite promising," says Hendricks. "When we saw that TiO_2 was also high κ but should theoretically have a negative band offset to Ga_2O_3, we got to work on implementing it in the metal-dielectric-semiconductor structure. The results have been great."

TiO_2 has a dielectric constant of 30-160 and a conduction band edge that is around 0.3 eV lower than β-Ga_2O_3. These characteristics promise a reduced leakage at reverse bias, due to improved blocking of tunnelling electrons, and no impairment to forward conduction, thanks to the band profile.



Results presented in the journal *Applied Physics Express* and at this year's Device Research Conference showcase the potential of Pt/TiO_2/Ga_2O_3 diodes

To determine whether TiO_2 could fulfil its promise, Hendricks and co-workers fabricated a conventional β-Ga_2O_3 Schottky barrier diode and a Pt/TiO_2/Ga_2O_3 diode in parallel. These devices were formed from adjacent die on a wafer containing a 13 μm-thick, silicon-doped β-Ga_2O_3 layer grown by HVPE on a tin-doped native substrate. Plasma-enhanced atomic layer deposition added a 4.3 nm layer of TiO_2.

Measurements on both types of diode, featuring edge passivation through the deposition of SiO_2, revealed that inserting TiO_2 lowered the turn-on voltage from 0.88 V to 0.59 V and increased the breakdown voltage from 548 V to 1380 V, corresponding to an increase in the breakdown field from 1.8 MV cm^{-1} to 2.8 MV cm^{-1}.

Hendricks regards these results as "very exciting", arguing that the breakdown field for the team's Pt/TiO_2/Ga_2O_3 diodes exceeds the limit of 4H-SiC in a planar topology, which also has a higher turn-on voltage.

Note that these results were realised without edge termination. This is now being introduced, with the team considering a range of field management structures that allow low resistive losses and a low turn-on loss. "We have already demonstrated an early advance in that area, pushing the breakdown field up to 3.7 MV/cm through *p*-NiO guard rings, which we shared at Device Research Conference 2023," says Hendricks, who is now hoping to make additional progress in increasing the breakdown field while realising a low forward voltage.

REFERENCE

N. Hendricks *et. al.* Appl. Phys Express **16** 071002 (2023)

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