PEW
POWER ELECTRONICS WORLD
CONNECTING THE GLOBAL COMMUNITY

NEW SILICON CARBIDE MOSFETS AND DIODES ENABLE HIGHER EFFICIENCY IN HIGH-VOLTAGE APPLICATIONS

ISSUE IV 2024
AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION
POWERELECTRONICSWORLD.NET

INSIDE

Large-Area Sintering for High Power Modules

Examining the benefits of large-area sintering, including thermal resistance and reliability improvements

Innovative Approaches to IGBT Production

Manufacturers of power semiconductor devices often grapple with high breakage rates and significant financial losses

Overcoming DC Bias and Size Challenges in Quantum

Quantum computing, with its promise of efficient calculations in challenging applications, is rapidly advancing in R&D

AIXTRON

THE NEW G10 SERIES

Your Productivity Solution for All Advanced Epitaxy Materials

G10-SiC

- 9x150 mm (6") or 6x200 mm (8")
- New hardware & process surpassing Single Wafer Reactor uniformities
- +50 % productivity per fab area with large batch technology & small footprint

End Markets/Products:
EV inverters & charging infrastructure

G10-GaN

- 8x150 mm (6") or 5x200 mm (8")
- 1st fully automated compact GaN MOCVD cluster designed 100 % for Si Power fabs
- Novel hardware solution for unmatched barrier uniformities and device yields

End Markets/Products:
Power Electronics & Wireless communication

G10-AsP

- 8x150 mm (6") or 5x200 mm (8")
- 1st fully automated AsP MOCVD system enabling 10x lower defect density
- Unmatched wavelength uniformity on all wafer sizes

End Markets/Products:
Micro LED, Optical Data communication, 3D-sensing & LiDAR

AIXTRON SE · Dornkaulstr. 2 · 52134 Herzogenrath · Germany · Phone: +49 2407 9030 0 · **www.aixtron.com**

VIEWPOINT

By Phil Alsop Editor

EV market running out of revs?

WHICH COMES FIRST – the EV or the charging station? In simple terms, that's the dilemma facing the EV industry right now. Should there be a massive roll out of charging infrastructure (and just think what's required to replicate the re-fuelling capacity of every single service station across the globe, before local infrastructure is even considered), which will then encourage more and more people to purchase an EV – build it and they will come? Or, do you keep trying to sell EVs until some kind of unstoppable momentum is achieved, and there's then the rush to build out the necessary supporting charging infrastructure? Either way, I think it's all but impossible to achieve success without major intervention from governments. And we're not just talking about the launch of policies and the encouragement of sustainability in general. No, we need billions and billions of state investment to kick start the EV success story. Which is maybe why China would seem to be a shining light in an otherwise slightly dimming market?

If we're being brutally honest, the global automotive industry is in danger of losing its way. Governmental pressure is telling them what is expected, but there's no clear roadmap – companies are being asked to drive forwards in the dark. And then being castigated for not moving forwards quickly enough. And consumers are picking up on this uncertainty, even if they have not been put off by the hefty price tag of going electric. And, as I've mentioned before, there are plenty of smart folks who genuinely believe that (green) hydrogen may well be the automotive industry's final destination fuel of choice.

Where some times one looks at an industry or individual companies who have simply mis-read their market, and

suffered as a result, in the case of the automotive sector, they really are being handed so many mixed messages by individual governments, and very little concrete help or advice, that there's plenty of sympathy for them. And there's no sign of this disruption clearing any time soon.

The good news, such as it is, is that there's still a massive market when it comes to adding intelligence to vehicles, whatever their fuel source, so the semiconductor market has plenty of room for growth here. Whether or not this will end up with the 'nirvana' of autonomous vehicles is anyone's guess.

However, the quest for intelligence, whatever the market size, will not disguise the EV 'chaos'. Sorry if that sounds like a gloomy message on which to end the year. On the bright side, the speed at which technology is developing almost certainly means that there will be other major opportunities ahead. And the AI market shows no signs of slowing down any time soon. And maybe renewables opportunities will outpace expected demand?

A happy festive season to you all.

PEW POWER ELECTRONICS WORLD

POWER ELECTRONICS WORLD

Editor
Phil Alsop
phil.alsop@angelbc.com
+44(0)7786084559

News Editor
Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Contributing Technical Editor
Richard Stevenson
richard.stevenson@angelbc.com
+44 (0)1923 690215

Sales & Marketing Manager
Shehzad Munshi
shehzad.munshi@angelbc.com
+44 (0)1923 690215

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Senior Event and Media Executive for Power Electronics International
James Cheriton
james.cheriton@angelbc.com
+44 (0)2476 718970

Publisher
Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

CEO Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

CTO Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

PEW Magazine is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher.

Published by Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com W: angelbc.com

Angel BUSINESS COMMUNICATIONS

Atomera/Sandia project to address GaN/Si challenges

Collaboration aims to create first GaN transistors from wafers using Atomera's Mears Silicon Technology (MST)

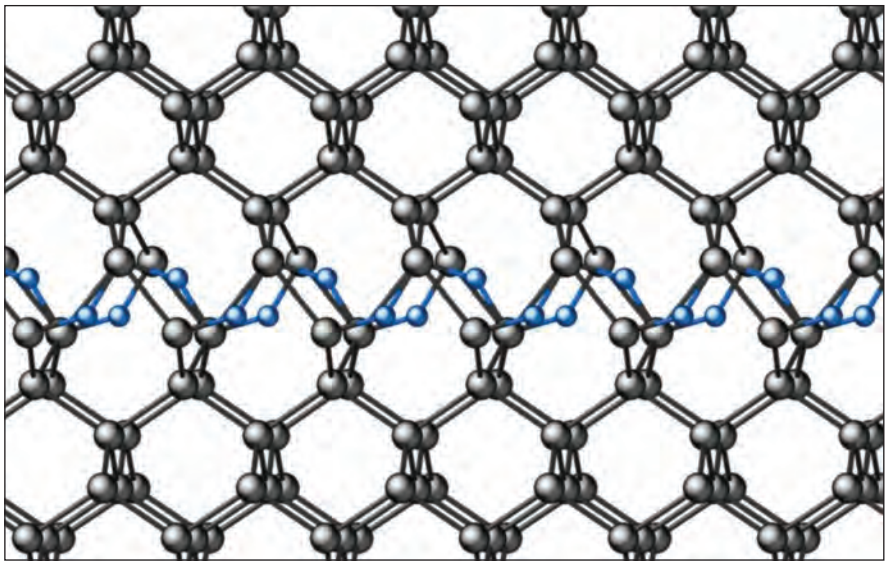
ATOMERA, a US semiconductor materials and technology licensing company, has announced a project at Sandia National Laboratories (a US Department of Energy, research centre), to address the challenges of growing GaN films on silicon.

The project, which is a collaboration with the Centre for Integrated Nanotechnologies (CINT) at Sandia, aims to create the world's first GaN transistors and test data from wafers employing Atomera's Mears Silicon Technology (MST). The effort will build upon improvements already observed at the materials level in GaN/MST on silicon wafers.

MST consists of layers of a non-semiconductor, such as oxygen inserted into a semiconductor material, such as silicon so that epitaxial growth is preserved. These layers can be used to modify or enhance the basic semiconductor properties and device attributes in a number of ways, including: diffusion blocking, variability, mobility, gate leakage, and reliability, among others.

"Atomera's MST represents a tremendous opportunity to improve GaN on Si manufacturing and provide speed, efficiency and cost-saving benefits to a wide range of industries including electronics, RF/microwave electronics and even MicroLEDs. This user project will test the effectiveness of the MST solution quickly using CINT's highly specialized tools and technology and give Atomera access to our team of scientists and researchers," said Jeffrey Nelson, director of CINT.

Due to the limited availability and size of native substrates, most GaN devices have been grown heteroepitaxially on sapphire, SiC or Si substrates.



Although impressive performance has been achieved with each of these, Si substrates offer a clear pathway to large wafer size, low cost and compatibility with well-established CMOS wafer fabrication lines.

However, there are significant challenges, including wafer warping or cracking, associated with the growth of thick GaN films on Si (GaN/Si), particularly at large wafer sizes. "Over the past approximately 25 years, GaN has transformed multiple industries, including lighting, RF/microwave and power electronics, but manufacturing limitations have hindered the widespread adoption of GaN for modern power electronics," said Shawn Thomas, vice president of Marketing & Business Development at Atomera. "This user project with Sandia Labs will allow Atomera to fabricate devices and collect data to validate the mechanical and electrical benefits of MST-enhanced GaN on Si."

Atomera's MST represents a tremendous opportunity to improve GaN on Si manufacturing and provide speed, efficiency and cost-saving benefits to a wide range of industries including electronics, RF/microwave electronics and even MicroLEDs

Managing stress is the most important aspect of growing thick GaN epi on Si. Commercially available GaN on Si power electronics (PE) devices are currently limited to a ~650V rating due to the maximum epi thickness (and thus breakdown voltage) that can be grown on Si without excessive wafer curvature, micro-cracking or poor yield. MST can improve the growth of GaN epitaxy on Si substrates by relieving biaxial tensile stress.

UK announces sustainable electronics centre

Four year project involves universities of Glasgow, Edinburgh, and Heriot-Watt with the Compound Semiconductor Catapult in Scotland

A NEW £5.5 million initiative aims to establish Scotland's Central Belt as a leader in sustainable electronics manufacturing and design.

The University of Glasgow will lead and coordinate the four-year project in collaboration with the University of Edinburgh, Heriot-Watt University, and The Compound Semiconductor Catapult in Scotland.

The Responsible Electronics and Circular Technologies Centre (REACT) is one of five new centres announced across the UK which will share in £25M from UKRI's Accelerating the Green Economy programme.

It will drive the transition to net-zero electronics, addressing both the environmental and economic challenges faced by the industry, while promoting the adoption of green technologies through collaboration between academia, industry, and policymakers.

The Compound Semiconductor Catapult in Scotland will providi access to cutting-edge equipment and world-class expertise to support start-ups, SMEs, large organisations, and academia in advancing compound semiconductor technology integration. The electronics industry is primarily driven by technical and economic considerations, often neglecting sustainability principles.

This has led to significant challenges, including large amounts of Waste Electrical and Electronic Equipment (WEEE), high emissions across the supply chain, and widespread use of Critical Raw Materials (CRMs) such as gold, palladium, and indium—materials with limited reserves.

In Scotland, the electronics industry is vital to the regional economy, with over 130 companies and 10,300 employees contributing to an annual turnover of more than £2.8bn. However, as more prominent manufacturers and buyers increasingly demand that suppliers commit to decarbonising their products, alongside growing legislative pressure, it is clear that the industry must adapt. Jeff Kettle from the University of Glasgow, who will lead and coordinate the REACT Hub, said:

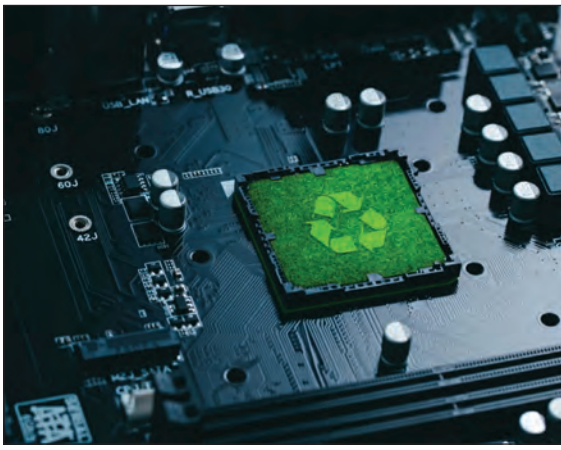
"The Centre will unite leading researchers to drive the industry's transition toward a net-zero economy. Its primary focus will be developing solutions to reduce electronic waste, minimise reliance on critical raw materials (CRMs), and reduce carbon footprints."

The REACT team brings extensive expertise across various areas, including electronic materials, design, manufacturing, and assembly, environmental impact, supply chain management, and business modelling. Bing Xu of Heriot-Watt University said: "REACT will leverage its partnerships to translate research into practical applications, boosting both the region's and the UK's global competitiveness in the sector."

REACT will collaborate with SMEs in the region to develop demonstrators and market-led solutions and provide skills training.

Jason Love of the University of Edinburgh said: "REACT will bring together industrial partners as well as the supply chain of companies and proactively communicate to the wider public, driving change at a governmental level."

REACT's work will offer key benefits, including reductions in e-waste, improved energy efficiency, and cost savings by adopting greener manufacturing processes. Additionally, REACT will play a crucial role in



fostering public-private partnerships to drive these innovations, focusing on co-creation, outreach, and advocacy.

Through conferences, workshops, and applied research projects, the centre aims to reshape the electronics industry in Scotland's Central Belt, transforming it into a sustainability model for the global market.

The University of Glasgow is also playing a key role in the Centre for Net-Zero High Density Buildings, another centre supported by the Accelerating the Green Economy funding.

Gioia Falcone of the University's James Watt School of Engineering will lead the University's contribution to the centre, which is setting out to investigate how densely-populated urban areas can be made more energy-efficient. The University of Glasgow-led centre has received £4.5m from UKRI, with a further £1.1m in support from industry, education, the public sector and the community.

The programme is part of UKRI's Building a Green Future strategic theme, which aims to accelerate the green economy by supporting research and innovation that unlocks solutions essential to achieving net zero in the UK by 2050.

‘All-GO-HEMT’ to develop β-gallium oxide heterostructures

€2 million German-funded project aims to increase in efficiency in power electronics

A €2 MILLION German-funded project called All-GO-HEMT aims to increase in efficiency in power electronics and make a significant contribution to sustainable energy generation.
Led by Andreas Fiedler (pictured above) of the Leibniz-Institut für Kristallzüchtung (IKZ), the project aims to develop modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures that exhibit high electron mobility.

Compared to established materials such as silicon, GaN and SiC, Ga_2O_3 offers potential for increasing efficiency that has not yet been fully exploited. “We believe that the development of more efficient materials can make a significant contribution to the energy transition and enable the industry to successfully master the challenges of the future,” explains Fiedler.

Even though power electronics based on Ga_2O_3 promise to be more efficient, the material is inferior to established materials in terms of charge carrier mobility. “Gallium oxide behaves to the established materials in the same way as ten metres of dirt road to one

kilometre of freeway.

Due to the shorter distance, your car consumes less, and despite the lower speed, you reach your destination faster - all thanks to a more compact design,” explains Fiedler.
The central aim of the project is to overcome the material limitation of Ga_2O_3 in terms of charge carrier mobility with the help of the innovative design of an aluminium-alloyed heterostructure and thus eliminate this disadvantage.

Fiedler emphasises: “We are convinced that the efficiency of power electronics can be significantly increased through a combination of a more compact design and higher charge carrier mobility in our newly developed materials.”

Another goal of All-GO-HEMT is to create a reliable material basis of Ga_2O_3 and the newly developed alloy with aluminum of the highest crystalline quality for research and industry.

This basis is necessary because the development of high-performance devices with compact design and optimised manufacturing processes is currently limited by the insufficient availability of high-quality material.

The project partner Ferdinand-Braun Institut (FBH) will use this material basis to develop new prototypes for power electronic devices. These prototypes will then be tested by ZF Friedrichshafen AG, the industrial mentor, for their suitability for industrial application.

In addition, the entire value chain, from crystal growth to the finished device, will be analysed by the industrial mentors Aixtron SE and Siltronic AG in order to quantify and evaluate the economic and ecological benefits of this technology at an early stage.

Infineon unveils world's thinnest silicon power wafer

Company first to master handling and processing of ultra-thin 20µm power semiconductor wafers

INFINEON has announced a breakthrough in handling and processing the thinnest silicon power wafers, with a thickness of only 20µms and a diameter of 300mm, in a high-scale semiconductor fab.

According to the company, this innovation will significantly help increase energy efficiency, power density and reliability in power conversion solutions for applications in AI data centres as well as consumer, motor control and computing applications. Halving the thickness of a wafer reduces the wafer's substrate resistance by 50 percent, reducing power loss by more than 15 percent in power systems, compared to solutions based on conventional silicon wafers.

For high-end AI server applications, where growing energy demand is driven by higher current levels, this is particularly important in power conversion: Here voltages have to be reduced from 230 V to a processor voltage below 1.8 V. The ultra-thin wafer technology boosts the vertical power delivery design, which is based on vertical Trench MOSFET technology and allows a very close connection to the AI chip processor, thus reducing power loss and enhancing overall efficiency.

"The new ultra-thin wafer technology drives our ambition to power different AI server configurations from grid to core in the most energy efficient way," said Adam White, division president Power & Sensor Systems at Infineon. "As energy demand for AI data centres is rising significantly, energy efficiency gains more and more importance. For Infineon, this is a fast-growing business opportunity. With mid-double-digit growth rates, we expect our AI business to reach one billion euros within the next two years."

To overcome the technical hurdles in reducing wafer thickness to the order of 20µm, Infineon engineers had to establish an innovative and unique wafer grinding approach, since the metal stack that holds the chip on the wafer is thicker than 20µm. This significantly influences handling and processing the backside of the thin wafer. Additionally, technical and production-related challenges like wafer bow and wafer separation have a major impact on the backend assembly processes ensuring the stability and first-class robustness of the wafers. The technology has been qualified and applied in Infineon's Integrated Smart Power Stages (DC-DC converter) which have already been delivered to first customers.

With the current ramp up of the ultra-thin wafer technology Infineon expects a replacement of the existing conventional wafer technology for low voltage power converters within the next three to four years.

Mitsubishi to invest $64m in new power module plant

MITSUBISHI ELECTRIC will invest approximately $64m (10 billion yen) to construct a new facility for the assembly and inspection of power semiconductor modules at its Power Device Works in Fukuoka Prefecture, Japan.

The plant, which was originally announced on March 14, 2023, is scheduled to begin operations in October 2026.

As the primary facility for assembling and inspecting power semiconductor modules, the plant will consolidate previously dispersed assembly and inspection production lines within the site to streamline production, from the incoming of components through manufacturing and final shipment.

New systems will be implemented to automate the management of manufacturing processes and the transportation of products for improved productivity. In addition, the company's integrated system covering everything from design, development and production technology verification to manufacturing will be strengthened to enhance product development.

Mitsubishi Electric says it expects the new plant to support its rapid and stable supply of products to meet market needs in response to the anticipated increases in demand for power semiconductors.

US DOE announces $481.5m loan to SK Siltron CCS

Company to use funds to expand manufacturing of SiC wafers for EVs

AS PART of the Biden-Harris Administration's Investing in America agenda, the Department of Energy (DOE) has announced a $544 million loan to SK Siltron CCS, LLC to expand American manufacturing of high-quality SiC wafers for electric vehicle (EV) power electronics.

The project — located at SK Siltron CSS facility in Bay City, Michigan — is expected to be among the top-five manufacturers of SiC wafers globally, boosting America's manufacturing competitiveness.

This project is forecast to create up to 200 construction jobs in the build-out phase and up to 200 skilled, good-paying operations jobs at full production.

SK Siltron CSS sells directly to device manufacturers which make power electronics used across many industries, not just EVs and high-speed EV charging. Market demand is currently being driven by transportation, next generation cellular (i.e., 5G), artificial intelligence and cloud computing end uses. SiC is also becoming increasingly common in other mid to high voltage applications such as solar photovoltaic, inverters and DC converters, and industrial chargers and adapters. The loan is offered through LPO's Advanced Technology Vehicles Manufacturing (ATVM) Loan Program, which supports domestic manufacturing of advanced technology vehicles, qualifying components, and materials that improve fuel economy.

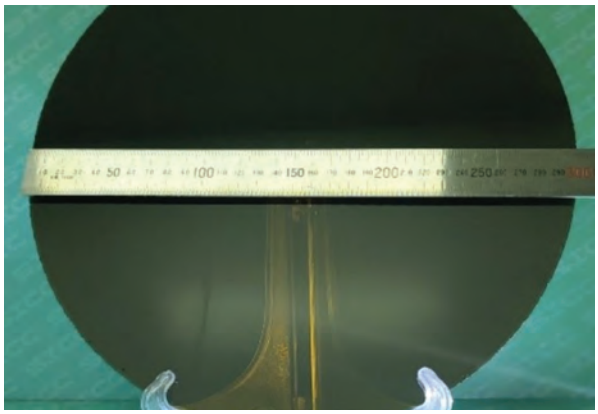
SICC shows first 300mm SiC wafer

AT ELECTRONICA 2024, Chinese SiC wafer company SICC exhibited what is thought be the first 300mm N-type SiC substrate.

SICC already makes 150mm and 200mm N-type conductive SiC, and high-purity semi-insulating substrates. The company has also developed large-size P-type SiC substrates.

But the 300mm N-type substrate, it says, is an industry breakthrough that highlights SICC's ability to push the boundaries of semiconductor technology.

For example, in its 200mm conductive 4H-SiC single crystal substrates, SICC says it has achieved near-zero threading screw dislocation (TSD) and extremely low basal plane dislocation (BPD) densities, which significantly enhances yields.



For its high-purity semi-insulating SiC substrates, SICC claims zero micro pipe density. (Micro pipes are SiC crystal defects that can cause electronic devices to short circuit and fail).

The company puts this success down to the ability to precisely control the crystal growth process, ensuring consistent wafer quality.. The company, which has headquarters in Jinan, is currently further expanding its 200mm SiC wafer manufacturing capacity at its Shanghai plant.Semiconductor value per car to reach $1k by 2029

evatec
process systems

Si, SiC & GaN

'Power ahead' in Power Devices

Frontside processes

- ☑ Ohmic contacts
- ☑ Surface protection for SiC
- ☑ Trench filling including high aspect ratio
- ☑ Sputtered AlN seed layer for MOCVD GaN growth
- ☑ Solderable top metal stack

Backside processes

- ☑ Etching / surface cleaning
- ☑ Ohmic contacts
- ☑ Thick metal stack

Choosing Evatec's CLUSTERLINE® family of 200 or 300mm tools is a sure way to "power ahead" of the competition. Our thin film process know-how on Silicon and WBG materials ensures the best device performance while our wafer handling and stress management for thin wafers delivers the best production yields.

Visit **evatecnet.com/markets/power-devices** to find out how you can power ahead in your own production or contact your local Evatec Office at **evatecnet.com/about-us/sales-service**

CLUSTERLINE® FAMILY

SEMICONDUCTOR & ADVANCED PACKAGING • COMPOUND & PHOTONICS • THE THIN FILM POWERHOUSE

www.evatecnet.com

A happy coexistence: silicon IGBTs and SiC MOSFETs

Opportunities in electric vehicles, automation, data centres and renewables will underpin the growth of the SiC MOSFET, as well as its lower performance, but cheaper alternative, the silicon IGBT

BY CALLUM MIDDLETON AND PAUL PICKERING FROM OMDIA

THOSE OF YOU owning vehicles powered by a battery will know that, in many ways, the driving experience is no different from that provided by a car consuming petrol or diesel. But there are some notable differences.

One of the first of these you'll encounter is that rather than having a traditional fuel gauge, you'll get a figure for the estimated range. And unfortunately, it will not take you long to discover that what this figure lacks in accuracy, it makes up for in optimism.

Driving range often tops the list of considerations of those looking to purchase an electric vehicle in an ever more competitive marketplace. Helping to maximise this range is the SiC MOSFET, which draws on its superior efficiency over the silicon IGBT. Having the upper hand on this front is the primary justification for OEMs to opt for the SiC solution.

While the efficiency of the SiC MOSFET is a major selling point, that's not the only benefit it offers over the silicon IGBT. Additional merits are a doubling of thermal conductivity and a far higher switching frequency, which allows the use of smaller passives and cheaper systems. It's also worth noting that many of the advantages of SiC are greater at higher voltages, allowing the wider bandgap transistor to shine in higher-voltage systems, such as 800 V electric vehicles and 1500 V photovoltaic inverters. The only significant downside of the SiC MOSFET is that it's pricey, but that concern is diminishing, as wafer sizes expand and material prices fall. So, is there much of a future for the silicon IGBT?

Well, one should not dismiss the importance of its lower price. The best engineering solution is not always the best solution, and there is no reason to expect the SiC MOSFET to ever reach price parity with the silicon IGBT, due to its higher inherent costs that are associated with the manufacturing process. While turning to SiC can drive down system costs, offsetting some of the difference in die cost, this can be a challenging proposition to make, and it is likely that users will always face a choice between performance and cost.

In the traction inverter market, after weighing up the pros and cons, many automotive OEMs and tier ones are deciding to deploy SiC. Tesla introduced SiC to this sector to distinguish its vehicles from its competitors, and in the process became the leading BEV manufacturer in the world. Now many automotive

companies are following suit in an attempt to close the gap. This is driving a ramp in SiC device sales, which climbed by 75 percent in 2023. However, today's BEVs are primarily in the 'luxury' and 'mid-range' categories, where consumers are willing to pay a little more for improved performance. As the BEV market expands, makers of these vehicles will have to penetrate the economy end of the market, where price matters much more. For customers who tend to use their vehicles for short journeys in urban settings, cars fitted with IGBTs will appeal.

It's quite feasible that even the more expensive vehicles will not solely use SiC. The Tesla model that pioneered SiC featured 48 MOSFETs. But in March 2023, that trailblazer of the BEV surprised many when it announced it would be trimming usage of these wide bandgap chips by 75 percent. Arguably, this decision should not have raised that many eyebrows, as one should expect that innovations in device design and inverter design would lead to a reduction from 48 MOSFETs, alongside a possible move to a blend of SiC MOSFETs and silicon IGBTs.

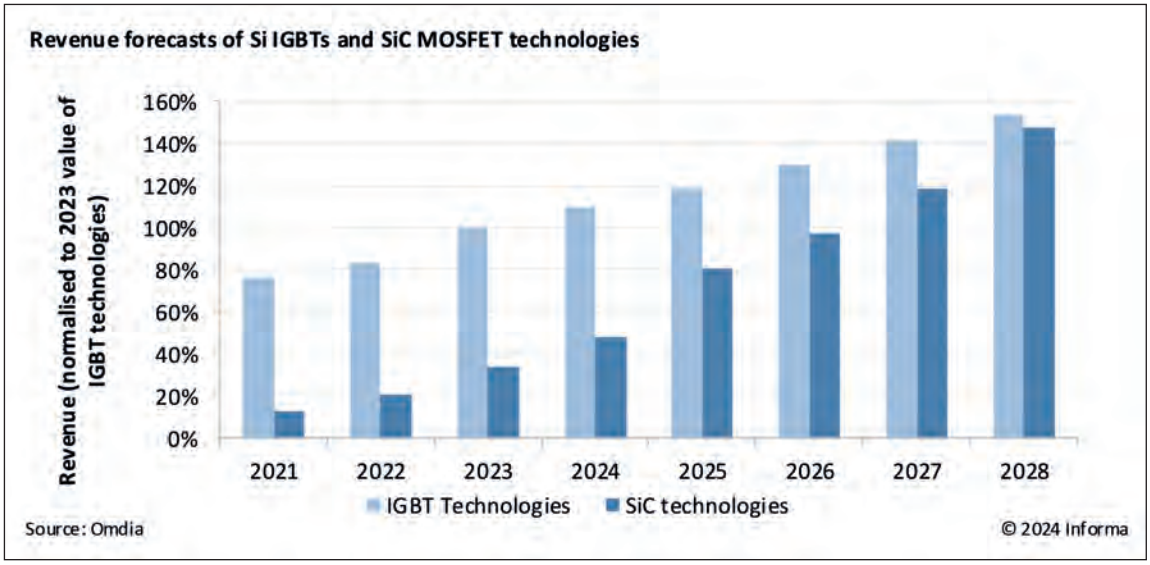
As already mentioned, BEVs are renowned for their optimistic range. This is partly due to difficulties in estimating this critical distance, which is influenced by numerous factors, including driving style and ambient temperature. The mission profile of the traction inverter within a BEV can vary greatly depending on where it is located, who the owner is, and even the day of the week. Due to these considerations, what's needed is a varied internal solution that allows the system to operate in the most efficient manner, irrespective of what is asked of it, without over-engineering. It remains to be seen whether this blended solution comes from vehicle designers deploying multiple inverters within a vehicle, or the use of power modules containing both SiC MOSFETs and silicon IGBTs.

When considering these factors, it is clear that the rise of the electric vehicle provides a great opportunity for both SiC MOSFETs and silicon IGBTs.

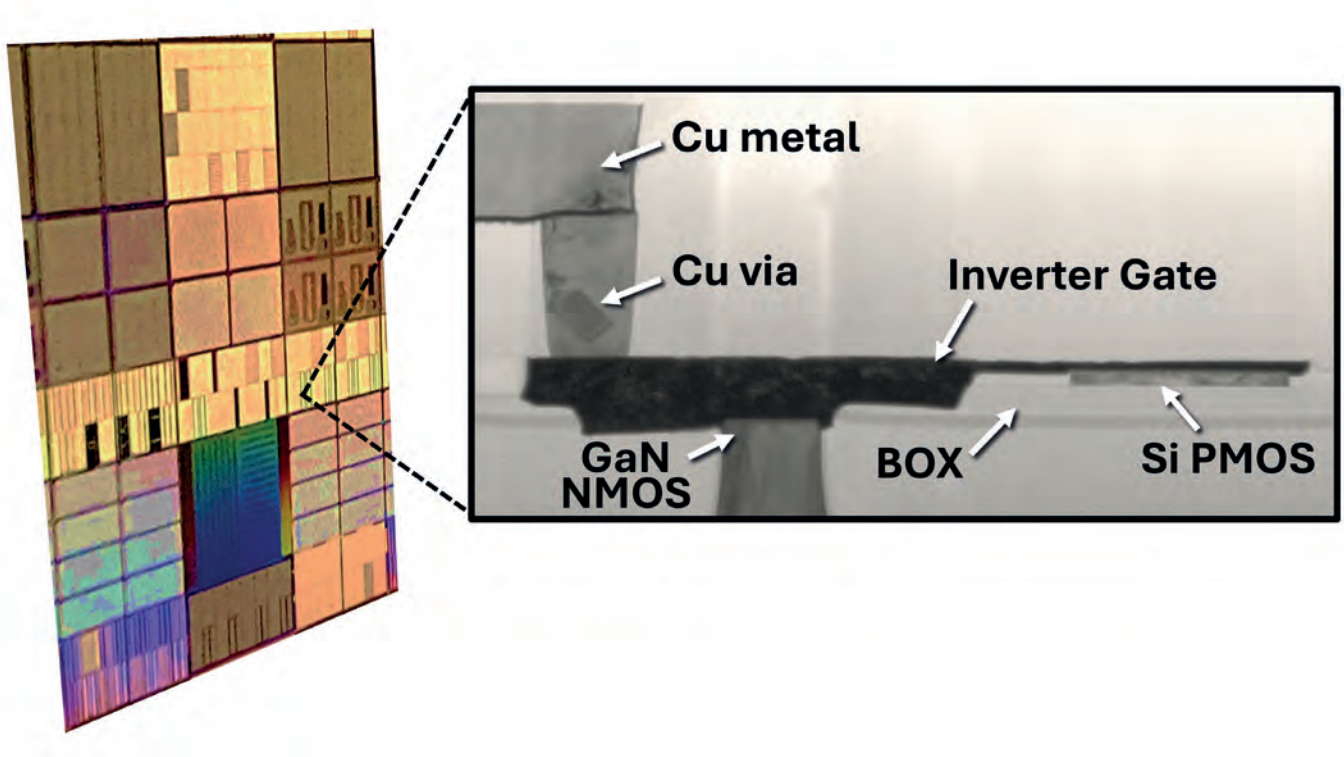
At Omdia, we are forecasting a compound annual growth rate of 32.6 percent for SiC device revenue between 2023 and 2028, and over that time frame an equivalent figure of 10.8 percent for power modules based on the silicon IGBT. Our forecast growth in SiC is eye-catching, justifying the level of investment in this technology, while the growth in the silicon IGBT offers a compelling reason to continue investing in device research and development to help companies claim more of this growing pie.

Outside the automotive sector, many of the same trade-offs apply. However, the absence of a key performance metric, such as range, makes it harder to justify a transition to SiC. We are living in a time of high energy costs and increased automation, factors that encourage investment in motor drives and grid infrastructure – and present opportunities for both SiC MOSFETs and silicon IGBTs. As SiC capacity expands, this should trim costs, but capacity is closely tied to the automotive sector. This tie-in may encourage equipment manufacturers in other sectors to stick with silicon until there's greater maturity in the SiC industry. Whilst improved efficiency is a big benefit at a time of increased energy costs, it still may not be enough to offset the extra chip cost. Therefore, it is most likely that the greatest penetration will come in applications where space savings are highly desirable, such as microinverters for photovoltaic systems, or power supplies for data centres.

There's no question that SiC growth is a huge opportunity for the power semiconductor industry, but it's not easy to see MOSFETs getting to the price of silicon IGBTs. Instead, they offer another option for the power electronics engineer, who has the opportunity to use the SiC MOSFET and the silicon IGBT concurrently. Thanks to overarching growth trends of electrification, electric vehicles, and renewable energy, there is the potential for a significant growth in sales of both device types; and industry should continue to develop IGBT technologies to aid the green transition.



➤ The historical and forecast revenue for the silicon IGBT and the SiC MOSFET. Data has been normalised to the 2023 revenue of IGBT technologies.



Combining a CMOS driver and a GaN power switch on 300 mm silicon

Intel's DrGaN technology, involving the monolithic integration of GaN and silicon CMOS on 300 mm wafers, will support power delivery in tomorrow's data infrastructure and communication networks

BY HAN WUI THEN FROM INTEL CORPORATION

THE NUMBER of power-hungry applications involving massive computation is on the rise, due to growth in datacenters, AI, wafer-scale compute, supercomputers and 5G/6G networks. Due to this, there is a need for the ICs that power these applications to combine a superior level of performance with greater energy efficiency and higher densities.

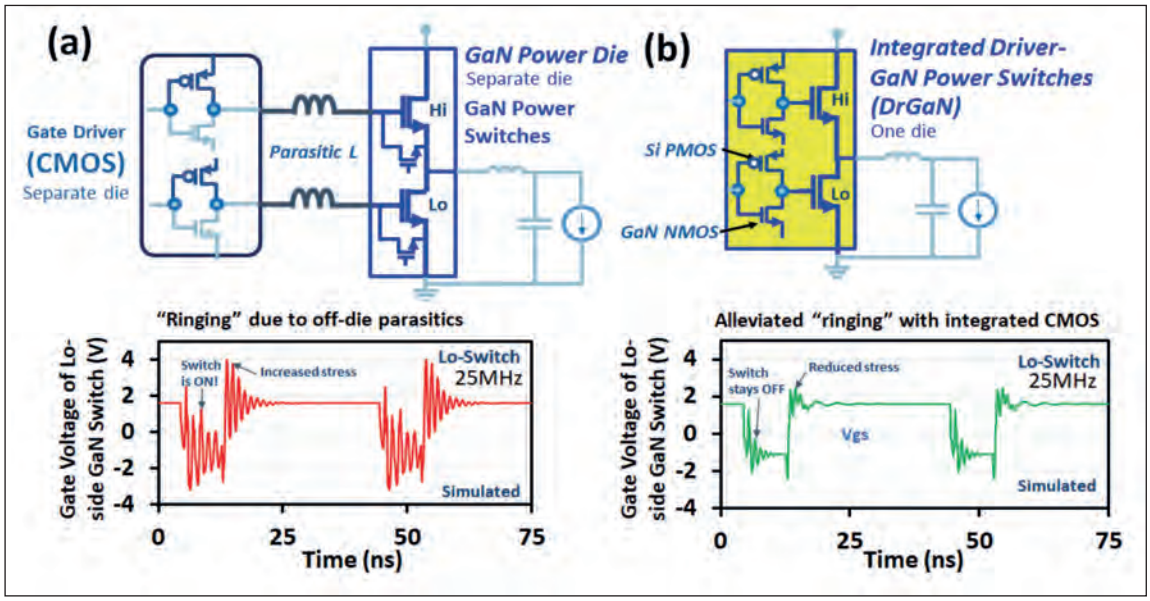
Our team at Intel Technology Research has anticipated these trends and has already devoted many years to addressing them. Back in 2019 we developed the industry's first enhancement-mode (E-mode) GaN transistor, enabled by high-κ dielectric metal gate technology; and we pioneered monolithic three-dimensional stacking integration of GaN and silicon transistor technology, all using 300 mm silicon wafers. During these efforts, we pursued the use of GaN because this high-mobility wide-bandgap semiconductor can operate at high frequencies and high power densities. These assets make this particular technology the best-in-class for power delivery and RF applications. We have focused on combining the advantages of GaN and silicon CMOS on a single chip to realise best-in-class performance, high efficiency and high density (small form-factor), as well as to integrate functionalities beyond what is possible with an *n*-channel only GaN technology.

Recently, we have taken our research a step further, employing an improved version of this process. At the most recent *International Electron Devices Meeting*, held last December in San Francisco, we unveiled what we refer to as 'DrGaN': it is a large-scale integrated CMOS driver-GaN power switch technology, realised on a 300 mm GaN-on-silicon wafer.

A single die solution

Our DrGaN technology breaks new ground. It is the first time that a GaN power transistor technology has been enhanced with an integrated CMOS driver on the same die. In comparison, other state-of-the-art GaN technologies of today employ a separate CMOS driver die that accompanies a GaN die, with the driver signal from the CMOS die routed through the package to the GaN die. This routing through the package incurs parasitic inductance

➤ Above. Intel's CMOS DrGaN Technology



➤ Figure 1. (a) A typical state-of-the-art solution involves a co-packaged two-die implementation: a separate CMOS driver die and power GaN die, where the driver signal from the CMOS die is routed through the package (represented by parasitic inductance, L) to the power GaN die. One downside of this approach is that it causes extreme ringing, visible in the simulation (inset). (b) A new approach facilitated by DrGaN, with a fully integrated CMOS driver on the power GaN die, enables a low-inductance path from the CMOS driver output to the GaN power switches. This technology suppresses the large ringing in (a).

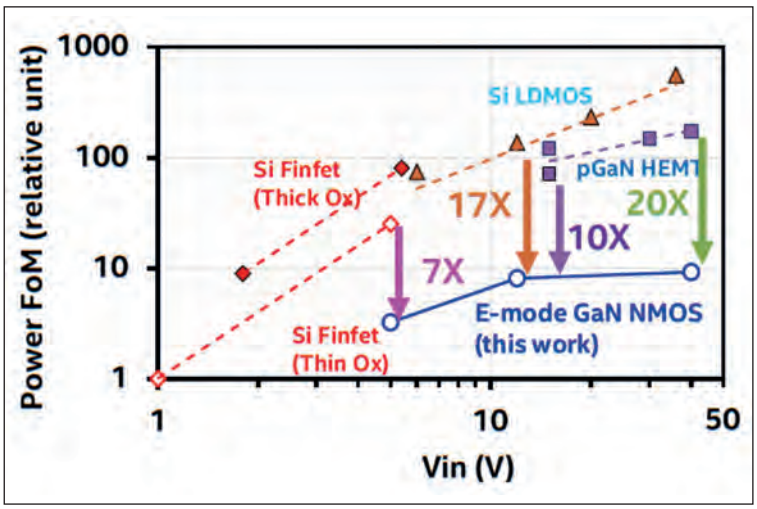
(see Figure 1(a)), which limits performance, with extreme 'ringing' at high switching speeds (this is visible in the simulation trace, shown in the inset of Figure 1(a)).

This ringing is detrimental, limiting the switching speed and the performance, in terms of the conversion efficiency. Due to this ringing, it's not possible to exploit a key advantage of the GaN transistor, which can switch far faster than its silicon sibling, evidenced by a figure-of-merit around 10-20 times higher (see Figure 2).

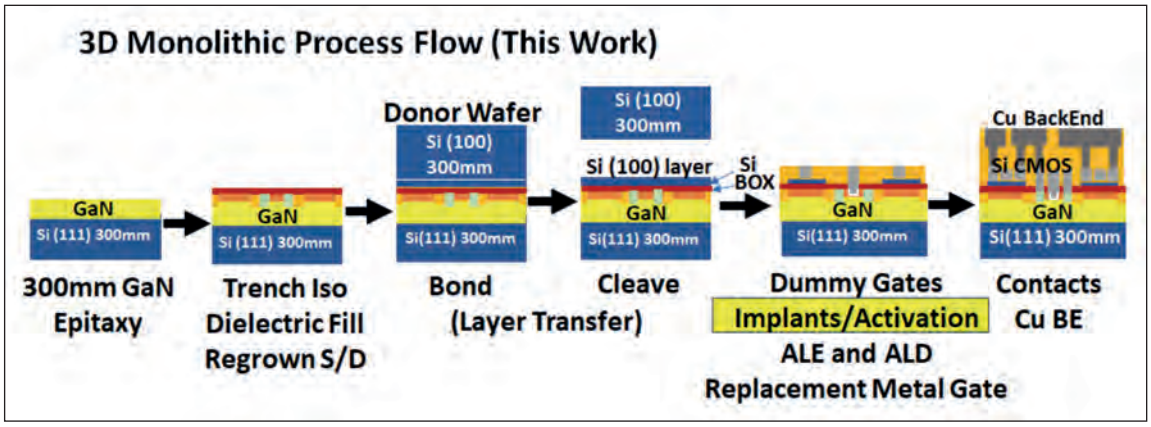
In addition, pairing a GaN die with a CMOS die leads to voltage 'overshoot'. Two issues result from this: an increase in the stress subjected to both the CMOS and GaN transistors; and inadvertent activation of the GaN power switch during the off-interval.

There is no doubt that a two-die solution fails to realise the full potential of the figure-of-merit gains offered by GaN. Overcoming this limitation is our DrGaN technology. By offering a fully integrated CMOS driver on the GaN die, our approach enables the realisation of a low-inductance path from the driver output to the GaN power gate, thereby suppressing the substantial ringing. The upshot is higher frequency operation, alongside a higher efficiency and improved reliability. The higher switching frequencies are cherished, as they open the door to smaller passives, such as smaller inductors. Shrinking the size of the power delivery unit follows, enabling higher power densities – that is, power delivery occupies less space-per-unit-power delivered, while maintaining high performance. Note that what we have just described is an instance of Moore's law in action for the power delivery solutions provided by DrGaN technology.

Our company has a long and strong track record in driver and MOSFET integration. Back in 2004 we introduced 'DrMOS' – driver and MOSFET integration for the silicon MOSFET. Our motivation for this breakthrough came from the need to keep pace with increasing microprocessor power density



➤ Figure 2. Benchmarking the power figure-of-merit ($R_{ON}xQ_{GG}$) of the GaN transistor of this work shows: a performance that's around a 20-fold better than the *p*GaN HEMT and around a 30-fold better than silicon LDMOS at 40 V; a 10-17-fold better performance than silicon LDMOS and a *p*GaN HEMT at 12-15 V, and 7-fold better performance than a silicon finFET at 5 V.



➤ Figure 3. The process flow used for DrGaN technology, which involves three-dimensional monolithic integration of GaN and silicon CMOS by layer transfer on 300 mm silicon wafers.

and efficiency demands associated with the leading PCs and laptops of that era. Since then, DrMOS has become the gold standard for point-of-load power delivery solutions for CPUs and GPUs.

One of the trailblazers for GaN is Navitas Semiconductor, which introduced integrated enhancement-depletion (E-D) mode *n*-channel drivers for high-voltage GaN power ICs. This particular architecture has been adopted because standard GaN processes cannot produce *p*-channel or CMOS devices.

The E-D mode driver is suitable for high-voltage scenarios. However, this form of driver is far too leaky – and thus not efficient enough – for lower voltage, point-of-load applications, such as those below 48 V. Turning to CMOS addresses this, while enabling efficient, high-density integration of other functionalities, including control logic and telemetry circuitries, such as current and temperature sensors. It is a broad range of features, challenging to realise with a standard GaN *n*-channel only process.

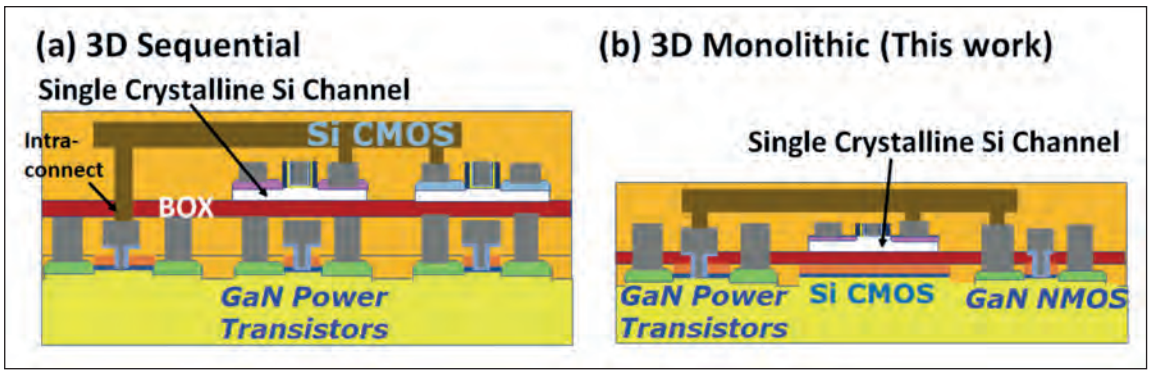
With our DrGaN technology, we accomplish the monolithic integration of GaN and silicon CMOS with a new process flow (see Figure 3), using a technique called layer transfer. We begin by bonding a donor silicon wafer to a GaN wafer. Upon separation, the silicon donor wafer cleaves along a weakened crystal plane throughout the wafer, to leave a thin layer of silicon channel material bonded onto the GaN wafer.

Our latest approach involves introducing implants and high-temperature activation steps, for the fabrication of the silicon CMOS transistors, prior to formation of the high-κ gate dielectric of the GaN transistors. From there onwards, we only perform low-temperature steps. That's critical, because high temperatures threaten to degrade the quality and reliability of the high-κ gate dielectric used for GaN transistors. By arranging our process flow in such a manner, this truly gate-last process overcomes a major hurdle in three-dimensional monolithic integration of GaN NMOS and silicon CMOS transistors.

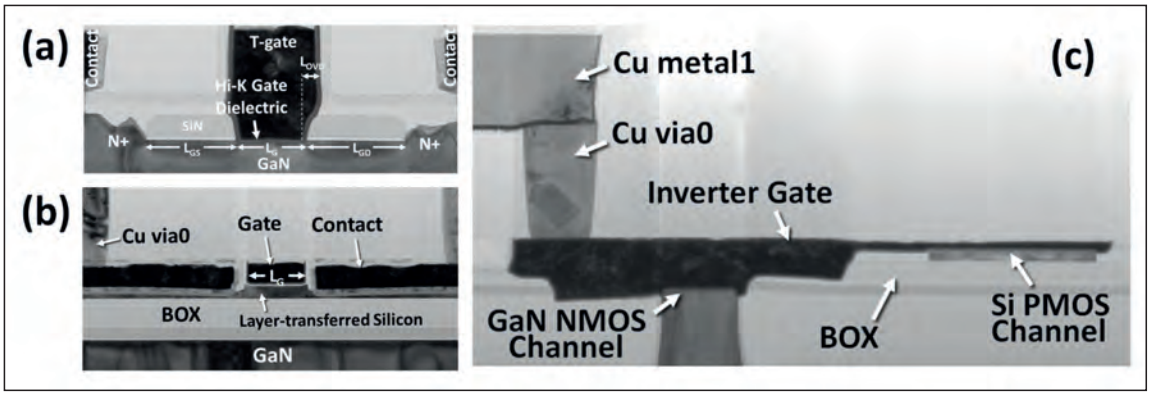
Proven superiority

The benefits of our latest process are seen in the measurements of silicon PMOS transistors fabricated by both approaches (see Figure 4). Previously, PMOS transistors were fabricated sequential, only after the GaN transistors were completed. This sequence exposed the gate dielectric of the GaN transistor to the high-temperature steps of silicon transistor processing.

Another downside of our previous approach is that this sequential process flow employed intra-connects to establish electrical connectivity between the silicon and GaN transistors. As well



➤ Figure 4. (a) Intel's prior work involved the three-dimensional sequential monolithic integration of GaN and silicon CMOS by a layer transfer process, with silicon PMOS/NMOS transistors fabricated after completing fabrication of the GaN transistors. (b) For Intel's latest work, DrGaN technology, GaN and silicon PMOS/NMOS transistors are fabricated in such a way that the high-temperature activation steps are completed before the deposition of the gate dielectric of the GaN transistors.



➤ Figure 5. Transmission electron microscopy of the completed (a) GaN transistor, (b) silicon PMOS transistor and (c) CMOS inverter, fabricated in this process on a 300 mm wafer.

as necessitating additional fabrication steps and masks, these intra-connects added path resistance when accessing the underlying GaN transistors. In contrast, our latest process for producing GaN and silicon CMOS transistors leads to a shared backend copper interconnect stack, eliminating the need for additional intra-connects and masks.

To inspect our completed devices – the GaN transistor, silicon PMOS transistor and hybrid GaN/silicon CMOS inverter – we have used a transmission electron microscope (see Figure 5). These devices, fabricated with our latest process on a 300 mm wafer, are used to construct the DrGaN.

We have undertaken a number of electrical measurements on our devices. Transfer current-voltage (I-V) characteristics for a typical GaN transistor with a channel length of 90 nm are shown in Figure 6 (a). Strengths of this device include an excellent on-off ratio of around 10^{10}, a low on-resistance of 422 Ω μm, a high drain-current drive of 1.2 mA μm^{-1}, and gate leakage below 1 pA μm^{-1}. Equally impressive are the I-V characteristics of our silicon PMOS transistor, which has a channel length of 180 nm (see Figure 6(b)). In this case the on-off ratio is around 10^6, the on-resistance 1780 Ω μm, the drain current drive 0.43 mA μm^{-1}, and the gate leakage around 1 pA μm^{-1}. Note that these are some of the best numbers ever reported for GaN and silicon PMOS transistors at comparable channel lengths. In particular, the GaN transistors show a best-in-class figure-of-merit for the reciprocal of the product of on-resistance and gate charge of 0.59 $m\Omega^{-1}$ nC^{-1}, measured from the shortest channel length of 30 nm (see Figure 7).

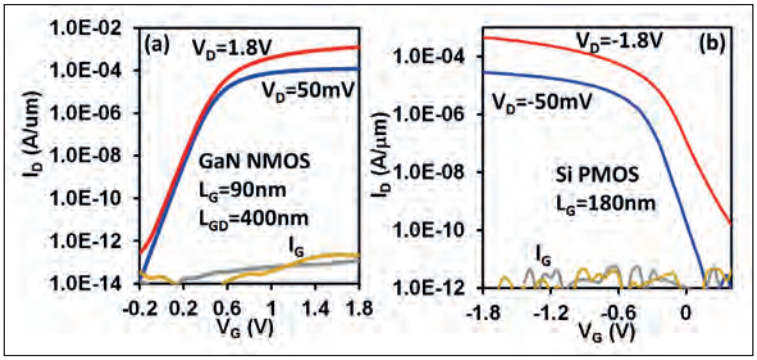
Through judicious selection of gate-to-drain separation, which can be varied from 200 nm to 1000 nm, we can obtain a breakdown voltage of up to around 60 V for our GaN transistor (see Figure 7). This enables us to target a range of use cases and application voltages.

Our DrGaN technology enables the construction of a large-scale IC from a massive array of repeated unit cells. Each of these cells, 40 μm by 10 μm in size, consists of four blocks: a silicon PMOS driver block, a GaN NMOS driver block, and two symmetrical GaN power switch blocks. The layout for these cells is outlined in Figure 8, along with a circuit schematic that illustrates the electrical connections between the silicon PMOS, GaN NMOS and GaN power switch transistors.

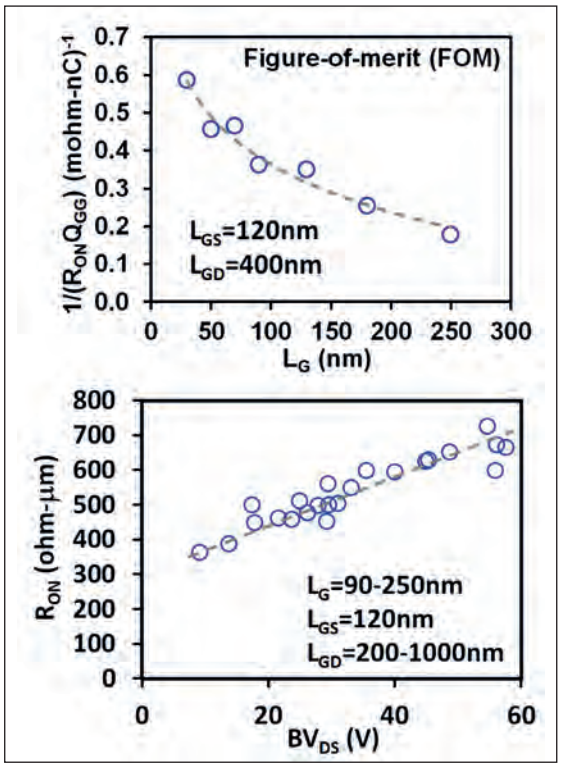
The DrGaN unit cell is arrayed over an area of 0.8 mm^2 to realise a desired total width of 421.1 mm for the GaN power switch, 49.54 mm for the GaN NMOS (driver) and 27.19 mm for the silicon PMOS (driver). The aggregate total width of all the transistors is 497.83 mm.

To demonstrate the full functionality of this 497.83 mm wide DrGaN, we have measured its steady-state electrical characteristics. To record the transfer characteristics of the GaN power switch S, which has a total width of 421.1 mm, in DrGaN, we use a probe to apply a bias voltage to the gate node of this switch (see Figure 9(a)). For this GaN power switch we have measured an on-resistance of 1 mΩ and determined leakage characteristics, with the switch turned off by applying a bias voltage of either (c) 0 V directly at the gate node of S; or (d) 1.8 V at the gate driver node of P and Q. Drain and gate leakage currents are well below 0.1 mA for the 421.1 mm-wide power switch. Also shown in Figure 9 are the transfer characteristics of silicon PMOS, P (width of 27.19 mm) (e) and the leakage characteristics of GaN NMOS, Q (width of 49.54 mm), in the gate driver (f).

We have also assessed the inverting characteristics of the combined GaN-silicon CMOS driver



➤ Figure 6. The current-voltage (I-V) characteristics of (a) GaN transistor, and a (b) silicon PMOS transistor produced by the DrGaN process.



➤ Figure 7. (a) The figure-of-merit $1/(R_{ON}Q_{GG})$ for the GaN transistors produced by the DrGaN process, for channel lengths, L_G, ranging from 30 nm to 250 nm. (b) The on-resistance, R_{ON}, and breakdown voltage, BV_{DS}, for GaN transistors produced by this process. Gate-to-drain lengths, L_{GD}, are between 200 nm and 1000 nm.

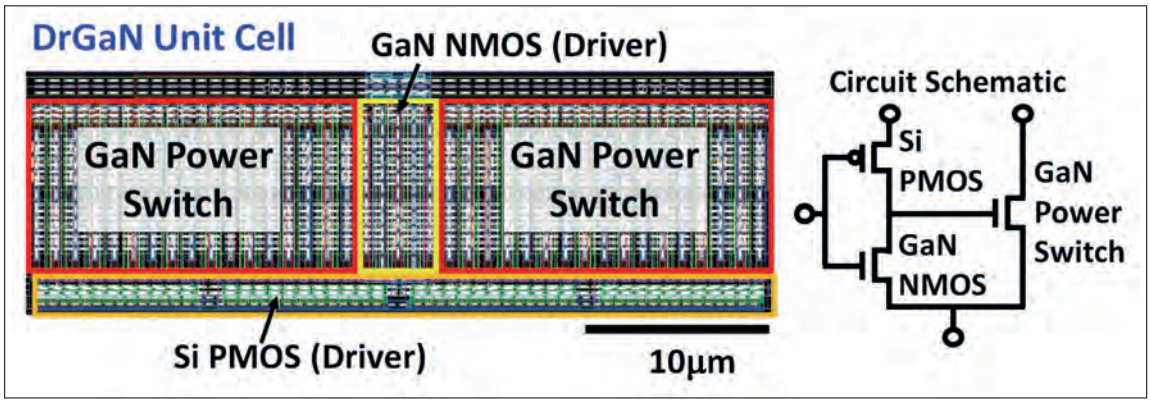
(P and Q). Figure 10 shows the steady-state transfer characteristics with DrGaN. Modulation of the GaN power switch, S, is driven by the integrated GaN-silicon CMOS driver (P and Q).

This final measurement completes full functionality testing of our DrGaN technology, which has multiple merits. We view our realisation of a large-scale, 497.83 mm-wide DrGaN is an important milestone towards demonstrating the viability of our 300 mm GaN-on-silicon process with three-dimensional monolithically integrated GaN and silicon CMOS, brought together by layer transfer. Our efforts break new ground, showing for the first time that this process can produce large-scale integrated circuits comprising GaN and silicon CMOS transistors on the same chip.

Our development of DrGaN demonstrates that the monolithic three-dimensional integration of GaN NMOS and silicon PMOS transistors is a powerful way to integrate two dissimilar best-in-class semiconductor technologies on the same silicon and deliver optimal performance, improved density, and more functionalities. Our accomplishments include the industry's first CMOS DrGaN technology fabricated in 300 mm GaN-on-silicon technology. Through the use of enhancement-mode high-κ dielectric GaN MOSHEMT technology for the GaN transistor, our DrGaN ICs set new benchmarks for performance and leakage. Another significant advance is the new improved truly gate-last process flow, resolving a major hurdle in three-dimensional monolithic integration of GaN NMOS and silicon CMOS transistors.

Thanks to our efforts, there has been a significant advance in 300 mm GaN-on-silicon technology. But that's far from all that the demonstration of DrGaN has accomplished. This technology holds the key to tomorrow's efficient, highly integrated, high-density point-of-load power delivery solutions for future high-performance compute in datacenters, AI and 5G/6G networks. DrGaN is clearly destined to deliver many great things.

The author, Han Wui Then, would like to thank team members and contributors: M. Radosavljevic, S. Bader, A. Zubair, H. Vora, N. Nair, P. Koirala, M. Beumer, P. Nordeen, A. Vyatskikh, T. Hoff, J. Peck, R. Nahm, T. Michaelos, E. Khora, R. Jordan, C. Hoffman, N. Franco, A. Oni, S. Beach, D. Garg, D. Frolov, A. Latorre-rey, A. Mitaenko, J. Rangaswamy, S. Sarkar, S. Ahmed, V. Rayappa, H. Chiu, A. Hubert, S. Brophy, N. Arefin, N. Desai, H. Krishnamurthy, J. Yu, K. Ravichandran, and P. Fischer.



➤ Figure 8. The layout of a 40 μm by 10 μm DrGaN unit cell consisting of silicon PMOS and GaN NMOS driver blocks, and two GaN power switch transistor blocks. The inset shows the circuit schematic of the electrical connections between the silicon PMOS, GaN NMOS and GaN power switch transistors. In the driver block, the silicon PMOS has a channel length, L_G, of 180 nm, and a total width per unit cell of 19.76 μm, while the GaN NMOS has the same channel length of 180 nm and total width-per-unit-cell of 36 μm. The GaN power switch transistors have a similar channel length of 180 nm, but a larger total width-per-unit-cell of 306 μm, and a longer gate-to-drain length, L_{GD}, of 400 nm, in order to withstand a higher operating voltage.

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

ULTRA LOW LOSSES

WE-MXGI

WE are here for you!

Join our free webinars on:
www.we-online.com/webinars

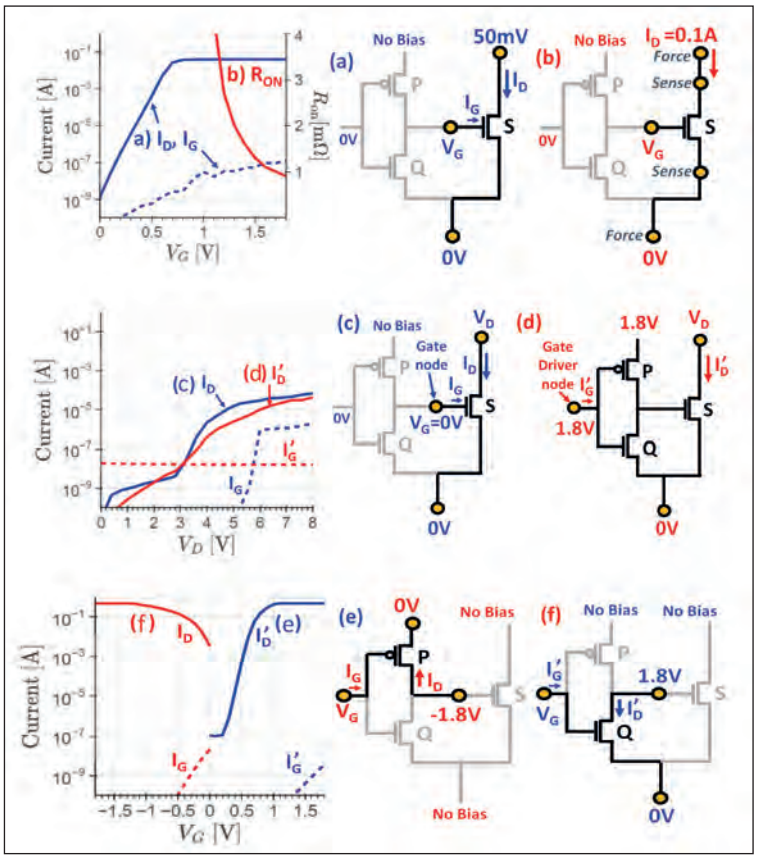
With the WE-MXGI Würth Elektronik offers the newest molded power inductor series. It combines an innovative iron alloy material that provides high permability for lowest R_{DC} values combined with an optimized wire geometry.

Ready to Design-In? Take advantage of personal technical support and free samples ex-stock.
www.we-online.com/WE-MXGI

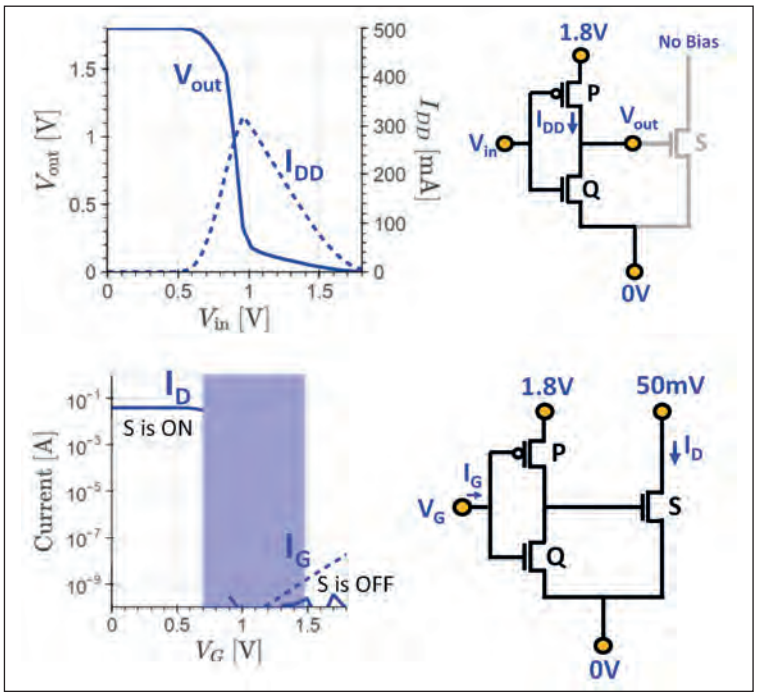
Highlights

- Extremely high power density
- Ultra low R_{DC} values and AC losses
- Magnetically shielded
- Optimized for high switching frequencies beyond 1 MHz

#UltraLowLosses



➤ Figure 9. (Top) the transfer characteristics of the GaN power switch S with a total width of 421.1 mm in DrGaN, demonstrating transistor operation. The normalized R_{DSON} is 0.8 mΩ mm^2. (Middle) The leakage characteristics, I_D-I_G-V_D and I_D'-I_G'-V_D of the GaN power switch S in DrGaN, in the off-state accomplished by either applying a bias voltage, V_G, of (c) 0 V directly at the gate node of S; or (d) 1.8 V at the gate driver node of P and Q. (Bottom) The I-V transfer characteristics of the (e) silicon PMOS, P, and (f) GaN NMOS, Q, in the gate driver of DrGaN.



➤ Figure 10. (Top) Transfer characteristics, V_{out}-V_{in}, of the GaN-silicon CMOS driver, P and Q, in DrGaN technology. (Bottom) The steady-state transfer characteristics of DrGaN. The switching of the GaN power switch, S, is driven by the integrated GaN-silicon CMOS driver (P and Q). Turning on involves a driver pull-up to a V_G rail of 1.8 V, and turning off involves a driver pull-down to a V_G rail of 0 V.

FURTHER READING / REFERENCE

- H.W. Then *et al*. "DrGaN: an Integrated CMOS Driver-GaN Power Switch Technology on 300mm GaN-on-Si with E-mode GaN MOSHEMT and 3D Monolithic `Si PMOS," IEDM 9.7.1-9.7.4. (2023)
- H.W. Then, "Stacking GaN and Silicon Transistors on 300 mm Silicon", Compound Semiconductor, May 2020.
- H.W. Then *et al*. "3D heterogeneous integration of high performance high-K metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications," IEDM 17.3.1-17.3.4 (2019)
- N. Desai *et al*. "A 32A 5V-Input, 94.2% Peak Efficiency High-Frequency Power Converter Module Featuring Package-Integrated Low-Voltage GaN NMOS Power Transistors," 2021 Symposium on VLSI Circuits pp. 1-2 (2021)
- H. W. Then et al., "Scaled Submicron Field-Plated Enhancement Mode High-K Gallium Nitride Transistors on 300mm Si(111) Wafer with Power FoM (R_{ON} xQ_{GG}) of 3.1 mohm-nC at 40V and f_T/f_{MAX} of 130/680GHz," IEDM 35.1.1-35.1.4 (2022)
- G.Moore, "Cramming more components onto integrated circuits", Electronics **38** 114 (1965) Intel, DrMOS Technical Specifications Rev.1.0, Nov 2004.
- N. Fichtenbaum, "GaN Integrated Circuits for Power Electronics," 2019 Device Research Conference pp. 1-26 (2019)
- H. W. Then et al. "Gallium Nitride and Silicon Transistors on 300 mm Silicon Wafers Enabled by 3-D Monolithic Heterogeneous Integration," IEEE Trans. Electron Devices 67 5306 (2020)

Bipolar *p*-FETs enable all-GaN power integration

Bipolar transport overcomes the inherent barriers of GaN *p*-FETs to pave the way to higher current densities

BY MENGYUAN HUA FROM SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

GaN POWER DEVICES have many attributes. They are renowned for their exceptional switching efficiency and high power density, strengths that are driving the development of miniaturised, energy-saving power systems. Thanks to a wide bandgap and stable material properties, GaN-based power devices are also capable of maintaining a good performance in challenging environments, such as extreme temperatures and irradiation conditions. And in addition to these capabilities, GaN power devices are revolutionising power systems towards higher levels of integration and intelligence. Given all this, it's of no surprise that GaN-based HEMTs have rapidly surpassed traditional silicon devices to play an indispensable role in a number of fields, ranging from consumer electronics to industrial power supplies.

However, while much progress has been made to date, there is still much more to do. In this regard, one important area for improvement is the GaN power IC – today there is a significant challenge in realising the seamless integration of power devices with low-voltage peripheral circuits. In the latest approaches to hybrid integration, the silicon-based circuits that are used for driving, sensing and protecting functions, are integrated with GaN power devices through packaging. This results in non-negligible parasitic inductance, which can lead to gate ringing, particularly during high-power fast-switching transients. Two downsides of this are a limited switching speed and a compromised system reliability. What's more, the silicon devices in these hybrid designs fail to handle extreme environments as well as GaN devices, narrowing the

application scope. Consequently, moving to an all-GaN integration strategy has much appeal, including liberation from parasitic issues and the constraints of silicon-based devices, as well as the opportunity to unleash the full potential of GaN power ICs.

There are several straightforward approaches for all-GaN integration, such as leveraging established *n*-channel device technology, resistor-transistor logic and direct-coupled FET logic. However, all these methods are impaired by excessive power consumption, due to a significant static current that diminishes the efficiency of the power IC and necessitates enhanced heat dissipation strategies.

A promising solution to effectively blocking the static current is the GaN-based complementary logic IC, incorporating both the *p*-FET and the *n*-FET. In this design, the existing *p*-GaN layer on the E-mode GaN HEMT platform is used to fabricate the *p*-FET.

The simplicity of this approach has attracted much attention, leading to efforts directed at boosting *p*-FET performance via strategies that include reducing interface trap states, downscaling the device, and engineering the gate dielectric. But even with these refinements, the current density of the *p*-FET falls far short of that of the GaN HEMT. This gap in current density between the GaN *p*-FET and its *n*-FET sibling poses a significant hurdle for progressing GaN CMOS technology.

Limiting the current density of the GaN *p*-FET is the low conductivity of the *p*-GaN layer. Due to a considerable effective mass and strong scattering, the mobility of holes is nearly two orders of magnitude lower than it is for electrons. Compounding this issue, magnesium is the only effective dopant available for *p*-type GaN. Unfortunately, it's far from an ideal dopant, being held back by a low activation ratio and a deep energy level that restricts the hole concentration in the *p*-GaN layer to 10^{18} cm^{-3}. While innovative epi-structure designs involving N-polar GaN, AlN and GaN heterostructures, superlattices, and InGaN insert layers are able to enhance hole mobility or density, these approaches are incompatible with the existing commercial *p*-GaN gate HEMT platform.

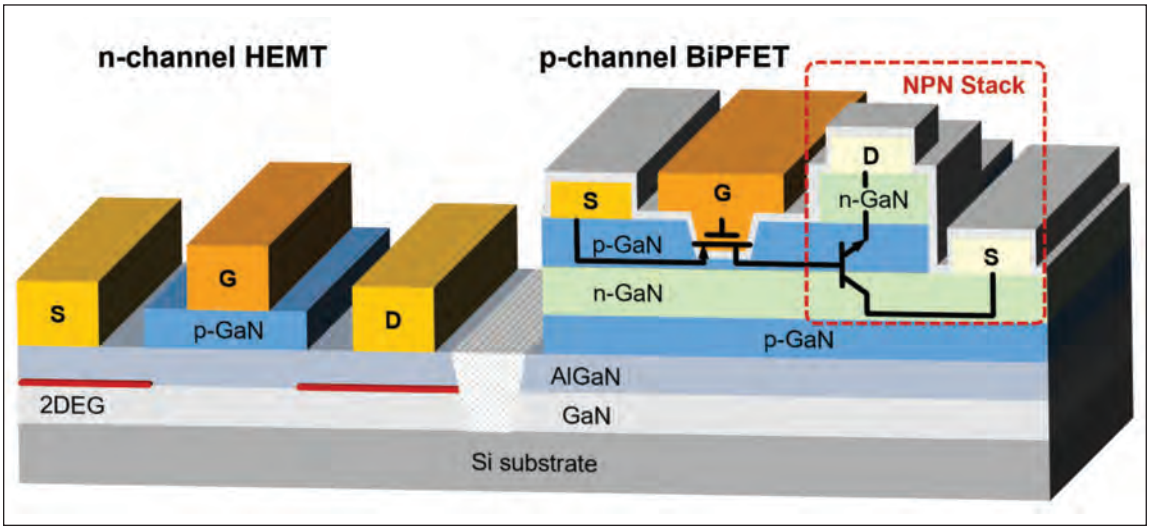
To overcome this challenge, our team at the Southern University of Science and Technology is pursuing an innovative GaN *p*-FET architecture endowed with a bipolar transportation capability (see Figure 1). This bipolar *p*-FET (BiPFET) features a conventional *p*-FET gate for maintaining *p*-type control logic, as well as an additional *n*-*p*-*n* GaN stack, which functions as a bipolar junction transistor that amplifies the current density. Operating in the on state, the *p*-channel turns on with a gate voltage below the threshold voltage. In this state, a minor hole current flows through the *p*-channel, and is injected into the base region of the *n*-*p*-*n* stack, initiating a substantial electron current. With electrons serving as majority carriers, the current density of the BiPFET is no longer confined by holes.

In addition to its remarkable conduction capability, the BiPFET inherently ensures a more stable threshold voltage and a higher drain-to-source breakdown voltage. When in the off-state, the bottom *n*-GaN region acts as a back-side field plate, extending the depletion region from the *p*-FET gate to the drain side. Thanks to this there is a more uniform electric field distribution, alleviating stress on the *p*-FET gate and improving the off-state breakdown voltage.

Another advantage of the BiPFET technology is that it is ready for integration with GaN HEMTs, thereby demonstrating outstanding compatibility and feasibility. The *n*-*p*-*n* stack can be realised through MOCVD growth, and the process flow of the BiPFET aligns well with that of the standard *p*-GaN gate HEMT. These strengths underscore the promising potential of the BiFET for the development of all-GaN ICs.

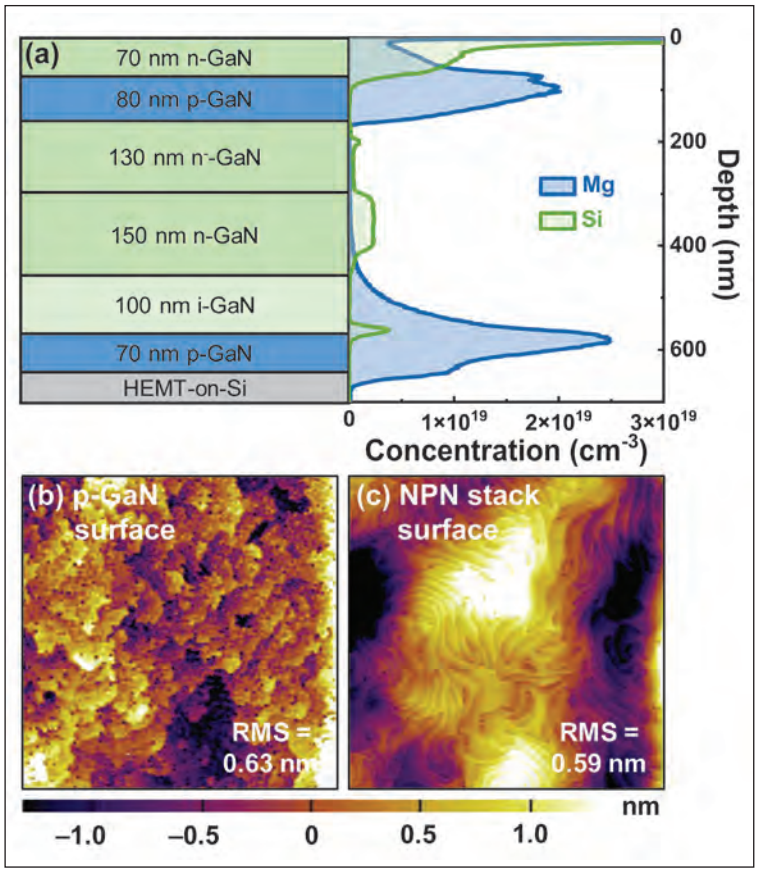
Demonstrating the concept

We have investigated the capability of our BiPFETs by producing these devices from a commercial



➤ Figure 1. A promising option for GaN integration is the combination of the *p*-GaN gate HEMT and the bipolar *p*-FET.

p-GaN HEMT platform featuring a 4.2 μm-thick GaN buffer layer, a 420 nm-thick undoped GaN channel layer, a 15 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 75 nm-thick *p*-GaN layer with magnesium doping at a concentration of 2.5×10^{19} cm^{-3}. Using this platform, our partners at Suzhou Institute of Nano-tech and Nano-bionics, Chinese Academy of Sciences, led by Qian Sun, selectively grew the *n*-*p*-*n* stack by MOCVD. This stack comprises a 150 nm-thick bottom *n*-GaN collector layer with a silicon doping concentration of 3×10^{18} cm^{-3}, a 130 nm-thick *n*-GaN layer with a silicon doping concentration of 5×10^{17} cm^{-3} to enhance voltage blocking capability, an 80 nm-thick *p*-GaN base layer with a magnesium doping concentration of 2×10^{19} cm^{-3}, and a 70 nm top *n*-GaN emitter layer with a silicon doping concentration of 10^{19} cm^{-3} (see Figure 2(a)).



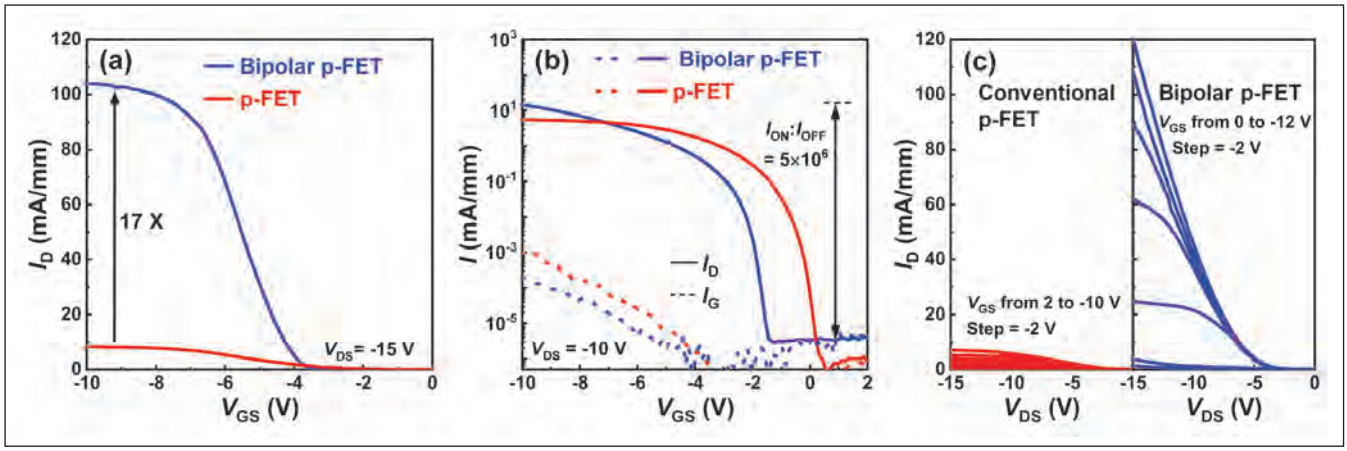
➤ Figure 2. (a) An *n*-*p*-*n* epi-structure on the conventional *p*-GaN HEMT platform and a secondary ion mass spectrometry depth profile of magnesium and silicon dopants. Atomic force microscopy images of the (b) initial *p*-GaN surface and (c) GaN surface after *n*-*p*-*n* stack growth on the E-mode GaN HEMT platform.

Note that we insert a 100-nm undoped GaN layer between the bottom *n*-GaN and *p*-GaN layers to mitigate the impact of the magnesium memory effect. Encouragingly, this *n*-*p*-*n* epi-stack preserves the favourable surface morphology of the original *p*-GaN, with clear atomic steps (see Figure 2(b) and (c)).

The fabrication of our BiPFETs starts with two-step etching, using a chlorine-based inductively coupled plasma recipe. The first step involves etching the collector region to remove the *n*-GaN layer, part of the *p*-GaN base layer, and then the hard mask SiO_2 in the *p*-FET region. During the second step, we simultaneously etch the top *n*-GaN in the *p*-FET region and the remaining *p*-GaN in the collector region until we reach the target depth. After removing the hard mask, we activate dopants in the *p*-GaN layer by annealing our samples under nitrogen gas at 750 °C for 30 minutes.

Following dopant activation, we add *p*- and *n*-ohmic contacts. To ensure an excellent *p*-ohmic contact on the etched *p*-GaN surface, we sputter a 50 nm-thick layer of magnesium on the contact region, prior to annealing at 600 °C, to diffuse this metal into the GaN layer. After removing the annealed magnesium layer, we form *p*-ohmic contacts with conventional evaporation and annealing processes.

According to electrical measurements, the contact and sheet resistance for our *p*-ohmic contacts are 57 Ω mm and 65 kΩ/sq, respectively. These values are comparable to those for a fresh bare *p*-GaN layer without any etching.



➤ Figure 3. (a) Linear-scale transfer, (b) log-scale transfer and gate leakage current, and (c) output characteristics of BiPFETs compared with conventional *p*-FETs.

Our next step is to form *n*-ohmic contacts on upper and lower *n*-GaN layers through photolithography, evaporation, lift-off, and annealing.

Following contact formation, we undertake slow inductively coupled plasma etching to gradually recess the gate trench. By going slow, we minimise plasma-induced damage. Then, using atomic layer deposition, we add a layer of Al_2O_3 that is approximately 22 nm-thick and serves as the *p*-FET gate dielectric. Evaporation of the gate electrodes follows, before we finalise the fabrication by defining contact vias and probing pads.

Improved current density ...

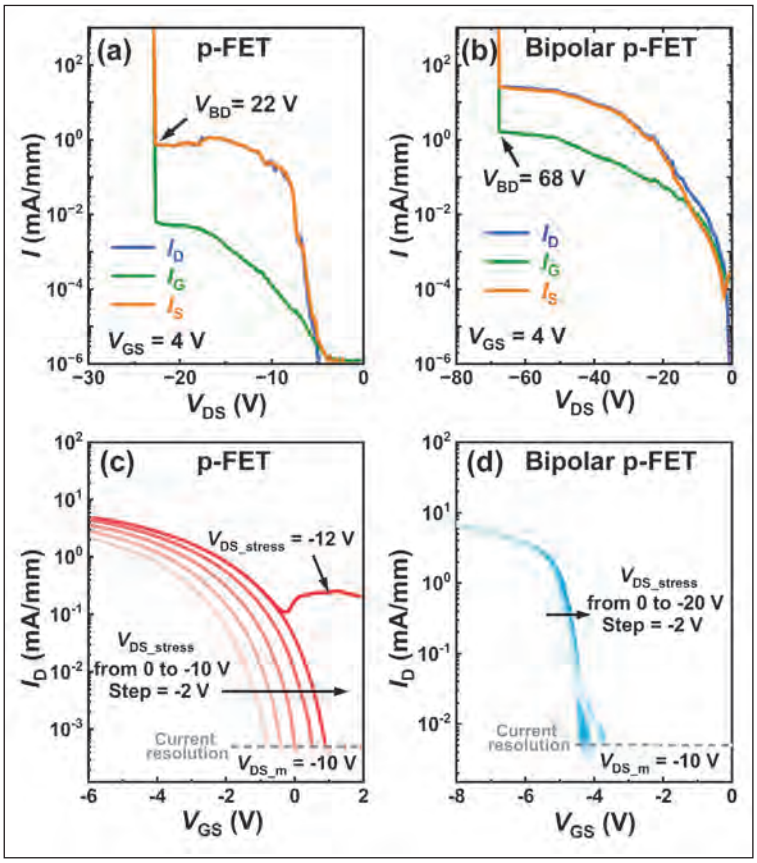
By integrating the *n*-*p*-*n* stack into the *p*-FET, we realise a substantial increase in the current density of the GaN *p*-FET. With identical MIS-gate dimensions as the *p*-FET, our BiPFET delivers a 17-fold hike in current density to more than 100 mA mm^{-1} (see Figure 3). This enhancement in current density is particularly pronounced when comparing output characteristics.

It's worth noting that this substantial increase in current density is realised without compromising the performance of the MIS-gate. Our BiPFET maintains a high current on-off ratio and exhibits a low gate-leakage current, signifying the well-preserved performance of the MIS gate (see Figure 3(b)). With moderate device scaling, we anticipate an increase in current density.

... and enhanced stability

As well as significantly enhancing the current density, the incorporation of the *n*-*p*-*n* stack offers the additional advantage of mitigating the voltage drop on the *p*-channel MIS-gate. When operating in the off-state, a depletion region forms in the reversely biased *p*-GaN/bottom *n*-GaN junction, creating a depletion region that homogenises the electric field distribution and alleviates stress on the MIS gate. The introduction of the *n*-*p*-*n* stack elevates the off-state breakdown voltage from 22 V to 68 V (see Figure 4(a) and (b)).

The strengths of our BiPFET extend to exhibiting a more stable threshold voltage under pulsed drain-bias stress, a merit that's attributed to a reduced voltage stress on the *p*-channel MIS gate. Pulsed tests, conducted on both the *p*-FET and BiPFET, show that the latter has a significantly lower drain-induced threshold voltage shift (see Figure 4(c) and (d)). In the BiPFET, the *n*-*p*-*n* stack shares the drain stress and safeguards the gate region. Even under a high drain stress of up to 20 V, we do not uncover any degradation in our pulsed transfer curves.



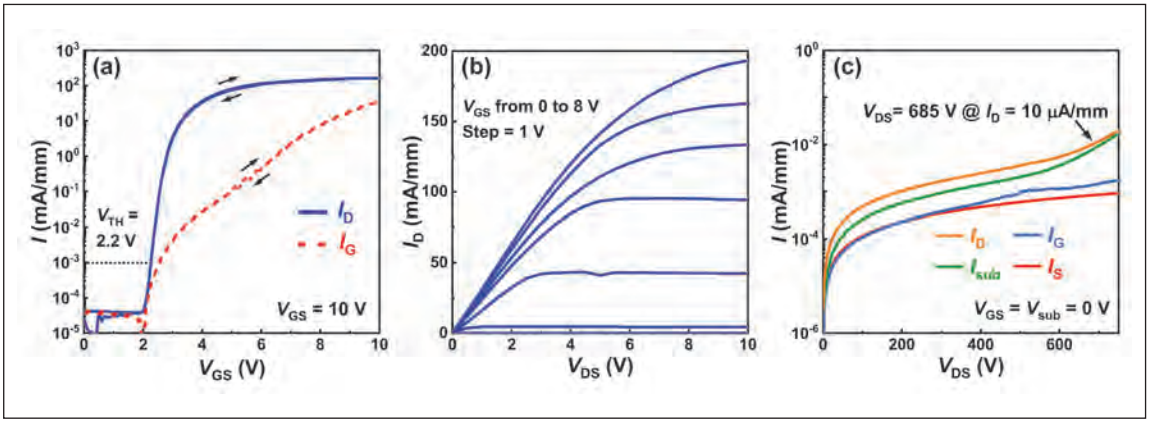
➤ Figure 4. (a) Off-state leakage current and breakdown characteristics of (a) the conventional *p*-FET and (b) bipolar *p*-FET. Plots of pulsed drain current as a function of gate-source voltage (I_D-V_{GS}) of (c) the *p*-FET and (d) the BiPFET measured with various drain-source stress voltages (V_{DS_stress}).

Integration capability

To assess the integration capability of our BiPFET, we concurrently fabricated a *p*-GaN gate HEMT on the same epitaxial wafer. This *p*-GaN gate HEMT demonstrates E-mode operation and a high on-off ratio, confirming the continued activation of the *p*-GaN layer after regrowth of the *n*-*p*-*n* stack (see Figure 5(a)).

We measure a saturation drain current density for our fabricated *p*-GaN gate HEMT of 200 mA mm^{-1},

The strengths of our BiPFET extend to exhibiting a more stable threshold voltage under pulsed drain-bias stress, a merit that's attributed to a reduced voltage stress on the *p*-channel MIS gate. Pulsed tests, conducted on both the *p*-FET and BiPFET, show that the latter has a significantly lower drain-induced threshold voltage shift



➤ Figure 5. (a) Transfer and gate leakage, (b) output and (c) off-state leakage characteristics of the E-mode *p*-GaN gate HEMT on the same platform with the BiPFET.

a value comparable to that of conventional *p*-GaN gate HEMTs (see Figure 5(a) and (b)). This robust conduction capability indicates that the 2DEG channel is not significantly impacted by regrowth of the *n*-*p*-*n* stack.

Another encouraging finding is that after regrowth, the buffer and channel layers still exhibit excellent blocking capability (see Figure 5(c)). The off-state breakdown voltage of the fabricated *p*-GaN gate HEMT achieves 685 V, validating the feasibility of integrating *n*-channel devices with BiPFETs for the realisation of GaN CMOS and power ICs.

The key strengths of our BiPFET are its exceptionally high current density and its enhanced stability, attributes that enable this class of transistor to be a very promising candidate for seamless integration with GaN HEMTs. This breakthrough paves the way for the design and fabrication of GaN CMOS and power ICs, laying the foundation for tomorrow's advanced power systems.

FURTHER READING / REFERENCE

➤ J. Tang, et al., 'Bipolar *p*-FET with Enhanced Conduction Capability on E-mode GaN-on-Si HEMT Platform', in 2023 IEEE International Electron Devices Meeting

evatec
process systems

Si, SiC & GaN

'Power ahead' in Power Devices

Frontside processes

- ☑ Ohmic contacts
- ☑ Surface protection for SiC
- ☑ Trench filling including high aspect ratio
- ☑ Sputtered AlN seed layer for MOCVD GaN growth
- ☑ Solderable top metal stack

Backside processes

- ☑ Etching / surface cleaning
- ☑ Ohmic contacts
- ☑ Thick metal stack

Choosing Evatec's CLUSTERLINE® family of 200 or 300mm tools is a sure way to "power ahead" of the competition. Our thin film process know-how on Silicon and WBG materials ensures the best device performance while our wafer handling and stress management for thin wafers delivers the best production yields.

Visit **evatecnet.com/markets/power-devices** to find out how you can power ahead in your own production or contact your local Evatec Office at **evatecnet.com/about-us/sales-service**

CLUSTERLINE® FAMILY

SEMICONDUCTOR & ADVANCED PACKAGING • COMPOUND & PHOTONICS • THE THIN FILM POWERHOUSE

www.evatecnet.com

Crushing MOSFETs one tipping point at a time

The growth of GaN is inevitable as it displaces the MOSFET in one application after another

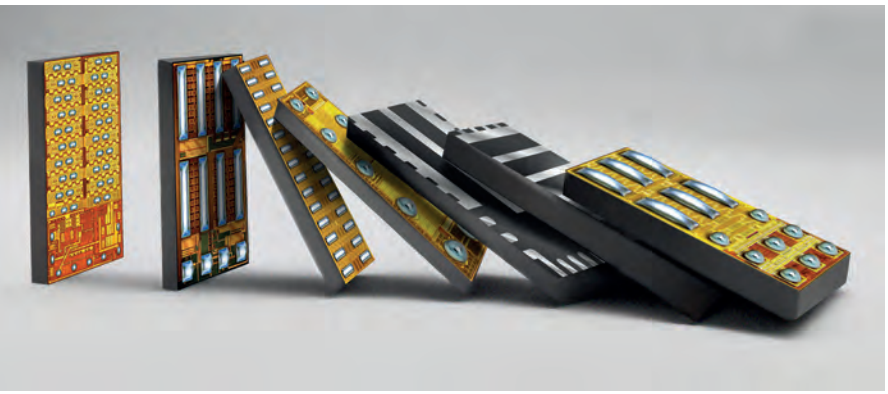
BY ALEX LIDOW FROM EFFICIENT POWER CONVERSION

GaN POWER TRANSISTORS are at a tipping point. It's a juncture where any small change or action leads to significant and often irreversible effects, and the future of these devices has reached a point of no return, where the dynamics of the situation shift dramatically.

This tipping point is following more than a decade of volume production of the GaN transistor. Since our company, Efficient Power Conversion (EPC), starting producing them in March 2010, they have repeatedly been touted as the replacement for the aging power MOSFET. Fourteen years on, the promise that GaN will crush silicon is now being realised.

To understand the changing rate of adoption of GaN, one can draw lessons from the 45-year-old power MOSFET. It's a device I know intimately, having been one of its first developers, as well as an instrumental player in the launch of the first product in November 1978. Back then the bipolar transistor was the incumbent power transistor. Despite being ten times slower, it was much cheaper than the MOSFET.

MOSFETs eventually crushed bipolar transistors. This did not occur overnight, but one application at a time. The first tipping point came from desktop computers, with Apple and IBM turning to the MOSFET for their AC-DC power supplies.



By adopting the superior transistor of the day, these tech giants could shrink their power supplies enough to fit inside desktop housings, a breakthrough that played a crucial role in widespread adoption of these computers.

Following this breakthrough, our MOSFETs continued to increase their deployment in high-performance applications while we focused on reducing costs and accelerating the learning curve as quickly as possible. Initially adoption took time, but jumps occurred whenever a new application ramped successfully. With each new tipping point for an application, the benefits to the business would extend beyond this individual triumph to trim the time and increase the likelihood of subsequent successes. Motor drives for high-speed plotters ramped in 1982. Anti-lock brakes ramped in 1985.

By 1988, thanks to higher volumes and significant capital investments, the manufacturing cost for the MOSFET had plummeted to below that of the bipolar transistor. Since then, the world never looked back. At that point in time the MOSFET had officially reached its tipping point. And that's exactly where GaN stands today.

GaN has already been adopted in several disruptive technologies, to the point where MOSFETs are no longer even considered for new designs. Each novel application for GaN can be thought of as having crossed an individual tipping point. This roadmap for ever-expanding adoption includes lidar, fast chargers, satellite electronics, AI, DC-DC power supplies, and humanoid robots.

With nearly fifty years of experience to guide us, we can identify four key factors that have played a crucial role in ensuring that GaN reaches its tipping point and finally surpass the MOSFET. These four factors, which exist in addition to all the cost, performance, and reliability requirements, are as follows: the design community now clearly

understands the large value derived from GaN; the targeted application is facing a changing landscape that leads to many open design windows; the adoption of GaN is being pursued by user community leaders, who are enjoying subsequent business success; and the existence of well-trained technical talent has emerged, which is capable of working with GaN and efficiently extracting its benefits.

For GaN technology, lidar provided the first application for crossing the tipping point. The simple reason behind this success is that GaN is capable of operating at far faster speeds than the MOSFET. Dave Hall, the visionary founder of Velodyne and the father of modern lidar, fully appreciated this benefit, realising that GaN technology enables a car sensor to see farther and with higher resolution than radar. Hall developed a spinning lidar system using EPC's first-generation GaN transistors, sparking the birth of the autonomous car.

Considering lidar from the perspective of tipping point elements, one can conclude that: Hall had a clear understanding of the substantial value derived from GaN; lidar opened many new design windows as it became an essential sensor for autonomous vehicles; Velodyne had huge success, attracting lots of customers and competitors; and Hall, with some assistance from EPC's engineers, knew how to extract the maximum performance from of these transistors.

The second application to reach a tipping point is the satellite power supply. As well as outperforming the MOSFETs, GaN is virtually immune from degradation caused by radiation in space. The key champion in helping to reach this particular tipping point is Dan Sable, CEO and founder of VPT. Today, just four years after initial deployment in this application, GaN transistors account for 30 percent of the satellite market for MOSFETs, and are on track to take the final 70 percent as legacy designs become obsolete or uneconomical.

Providing the third tipping point for GaN is the fast charger. Here the standout is Gene Sheridan, CEO and co-founder of Navitas Semiconductor. Today, virtually all fast chargers use GaN, thanks to its capability to deliver high powers and recharge power-hungry cell phones, tablets and laptops in a fraction of the time that silicon-based chargers would take.

Following all this success, we are now standing on the precipice of one of the most significant tipping points in recent history: AI. Servers for AI, such as those made by Nvidia, have crossed a crucial threshold, with virtually all of them utilising GaN in the on-board 48 V – 12 V (or in some cases 5 V) DC-DC converters.

While the full impact of the AI revolution is only beginning to be fathomed, one inevitable outcome is related to the tipping point of humanoid robots. These robots, equipped with 40 or more high-performance motors, rely heavily on GaN technology for higher torque density, higher power efficiency, less noise, and a more compact design. It is a set of requirements that is making silicon obsolete and GaN indispensable.

Taking a step back from specific successes, one can see that the tipping points for GaN are occurring with greater speed and a higher frequency. As has been the case for the MOSFET, every new development is educating the user community on GaN's unique value and accelerating its inevitable adoption in additional applications. And with each new positive experience and business success resulting from GaN, global implementation is rising, creating more and more design-window opportunities. Additional gains are the emergence of new GaN advocates within the user community, and new sources of capital. Over the last few years, thousands of trained design and manufacturing engineers have gone up the learning curve, and now know how to extract the additional efficiencies of GaN. Adding to these factors, GaN is proven to be more reliable than silicon, across a wide range of power levels, with a price that is comparable to the MOSFET. Due to all these compelling factors, it is inevitable that GaN's adoption will only accelerate, consuming the $12 billion MOSFET market while creating new markets of its own. In sum, GaN's tipping point is here.

PE INTERNATIONAL CONFERENCE

ANGELTECH

7 - 9 APRIL 2025
BRUSSELS
BELGIUM

CONNECTING, EDUCATING & INSPIRING THE POWER ELECTRONICS INDUSTRY

THEMES AND SPEAKERS ANNOUNCED

With soaring sales of silicon devices and explosive growth in SiC and GaN technologies, the industry is filled with optimism. Attendees will enjoy two days of insightful talks and panel discussions, where we will delve into the factors driving this industry boom and address emerging challenges.

In addition to enlightening conference sessions, Power Electronics International offered ample networking opportunities to connect with industry leaders. In our exhibition hall, providers of process equipment, materials, and metrology tools showcased cutting-edge innovations.

Power Electronics International is part of AngelTech, a renowned event hosting chip-level conferences. With three conferences, 800+ delegates, 80+ exhibitors, 120+ presentations, and extensive networking possibilities, AngelTech is the premier global event for compound semiconductor, photonic integrated circuit, and power electronic technologies.

Benefit from the synergy between these conferences, expanding your customer and supplier networks across comprehensive supply chains.

Key Themes for 2025

Next-Generation Semiconductor Materials: Beyond SiC and GaN

Explore the latest advancements in semiconductor materials beyond silicon carbide (SiC) and gallium nitride (GaN), including emerging options like gallium oxide (Ga2O3) and diamond semiconductors. Understand their potential applications and performance enhancements, shaping the future of power electronics.

Sustainable Power Conversion Technologies: Eco-Friendly Solutions

Delve into sustainable power conversion technologies, focusing on eco-friendly solutions for reducing environmental impact. Discuss innovations in energy-efficient designs, materials recycling, and renewable energy integration, addressing the growing demand for environmentally conscious power electronics solutions.?

Smart Grid Integration: Enhancing Resilience and Flexibility

Examine strategies for enhancing the integration of power electronics in smart grids, emphasizing resilience and flexibility. Discuss advanced grid control algorithms, distributed energy resource management, and cybersecurity measures to ensure reliable and secure operation in dynamic grid environments.

Power Electronics for Electric Mobility: Accelerating Electrification

Explore the role of power electronics in accelerating the electrification of transportation, including electric vehicles (EVs), hybrid electric vehicles (HEVs), and charging infrastructure. Highlight advancements in powertrain technologies, battery management systems, and fast-charging solutions to meet the evolving needs of the automotive industry.

Artificial Intelligence in Power Electronics: Optimizing Performance

Investigate the integration of artificial intelligence (AI) and machine learning techniques in power electronics systems for optimizing performance and efficiency. Explore AI-driven control algorithms, predictive maintenance strategies, and adaptive power conversion architectures, enabling intelligent and autonomous operation in diverse applications.

Energy Harvesting and Wireless Power Transfer: Enabling Autonomous Systems

Examine the latest developments in energy harvesting and wireless power transfer technologies, enabling autonomous and self-powered systems. Discuss advancements in harvesting energy from ambient sources, wireless charging techniques, and their applications in IoT devices, wearable electronics, and remote sensing platforms.

To find out more about our sponsor and speaker opportunities, contact us today on:

+44 (0) 2476 718970
info@peinternational.net
peinternational.net

Angel BUSINESS COMMUNICATIONS
ANGEL EVENTS

ANGELTECH

ESS EXECUTIVE STRATEGY SUMMIT | CS INTERNATIONAL CONFERENCE | PIC INTERNATIONAL CONFERENCE | PE INTERNATIONAL CONFERENCE

Sponsorship / Exhibition / Speaker OPPORTUNITIES AVAILABLE!

Sponsorship, exhibition, and speaker opportunities at PE International, enable and empower you to educate and penetrate the global power electronics industry using multiple marketing tools.

Demand is high, with sponsorship, exhibition and speaking slots already being secured for 2025, so to avoid disappointment, please get in touch today.

Delegate Earlybird Discount:

Register before 31 December and get 10% OFF!

Registration to AngelTech allows you to access both days of **PE International** and the co-located **CS International** and **PIC International.**

10% OFF

PLATINUM SPONSORS

boschman advanced packaging technology | Panasonic CONNECT | PiNK | SIGLENT 鼎阳 | YOLE Group

GOLD SPONSOR

POWERTRIM module packaging technologies

MEDIA PARTNERS

Bodo's Power Systems | CS COMPOUND SEMICONDUCTOR | 化合物半导体 CS COMPOUND SEMICONDUCTOR CHINA | everythingPE Keep up to date with Power Electronics | Go Photonics

PIC PHOTONIC INTEGRATED CIRCUITS | PEW POWER ELECTRONICS WORLD | PSW | SS SILICON SEMICONDUCTOR | 半导体芯科技 SILICON SEMICONDUCTOR CHINA

2025 SPEAKERS INCLUDE

AALBORG UNIVERSITET | boschman advanced packaging technology | EVG | Fraunhofer IISB | Hitachi Energy | infineon | Innoscience | KU LEUVEN | MINDCET | Navitas | OMDIA | Panasonic CONNECT | PiNK | POWERTRIM | ST life.augmented | universität freiburg | University of BRISTOL | YOLE Group

INVITED SPEAKER

RI.SE

ORGANISERS

Angel BUSINESS COMMUNICATIONS | ANGEL EVENTS

Unlocking the Internet of Everything with flexible chips

An Internet of Everything has long been promised, but progress has been hindered by semiconductor availability, cost, and concerns around sustainability. Could a new approach help to achieve a smarter, more connected future?

BY SHANE GEARY, SVP MANUFACTURING & OPERATIONS, PRAGMATIC SEMICONDUCTOR

FROM SMART MANUFACTURING to predictive maintenance, digital transformation is already impacting every facet of business and industry. But the hyperconnected Internet of Everything (IoE) – and the promised efficiency and insight – has remained elusive, despite the market potential being huge. McKinsey estimates the global value of the IoT alone to be up to $12.5 trillion by 2030; amplifying the level of connectivity to encompass billions of smart items could see that figure soar.

So why hasn't the IoE materialised?

In part, it's a matter of supply: ubiquitous connectivity is reliant on abundant supply of semiconductors – yet existing methods of semiconductor fabrication would struggle to satisfy the demand for billions of smart items. IoE devices typically don't use the latest, cutting-edge chips, but instead tend to rely on so-called 'legacy' chips. Despite the name, legacy chips are not old technology. They're constantly being adapted for new requirements and applications and play a central role in a manufacturing economy.

Their importance was underlined during the recent pandemic, when demand outstripped supply. The world watched in disbelief as entire production lines ground to a halt and everything from cars to TVs went unshipped, hampering an already beleaguered economy.

So, if supply is what's holding back the IoE, why don't we just make more chips?

The fact is that expanding the production of legacy chips isn't easy. They're often produced

in fabrication plants (fabs) using older equipment, and this equipment is less readily available. Furthermore, building a new fab is costly and time-consuming, requiring tens of billions of dollars and maybe two years or more to get up and running.

Sustainability is also an issue. Many of these legacy fabs were built when carbon emissions were less of a consideration. Newer fabs tend to be highly efficient, with carefully considered wastewater programmes and an emphasis on energy reduction. The long lead times and costs associated with chip manufacture are also a factor; ubiquitous connectivity requires a low-cost solution that can be swiftly proliferated, at scale.

Existing modes of chip production are ill-suited to realising an IoE. To sustainably achieve pervasive connectivity, we need to look to new methods and materials.

Unlocking the Internet of Everything

Instead of relying on traditional, outdated modes of semiconductor fabrication, new methods of manufacturing combined with advanced materials are signalling a radical shift in the semiconductor industry. Flexible integrated chips remove the need for the complex, high temperature processes required for silicon chip fabrication, and instead rely on simple spin-coating of polyimide onto a glass carrier.

This process takes place at lower temperatures, requiring significantly less energy, water and chemicals. This has a dramatic impact on the carbon footprint, as well as set-up costs and production timescales. In fact, flexible chips can be delivered in as little as four weeks. The implications for innovation are multiple: rather than adhering to 'right-first-time' workflows, designers can take advantage of rapid cycle times to amend and refine designs on the fly, iterating to achieve optimal performance. Low non-recurring engineering costs also lower the barrier to entry, making it cheaper and easier than ever before to bring designs to life.

Connecting everything, everywhere

So what does this mean for IoE?

The flexibility, low cost and low carbon footprint of flexible chips mean they can be easily integrated into everyday objects. This makes them ideal for the IoE and the generation of data to feed AI models, enabling efficiency and insights at scale.

For FMCG, that connectivity might deliver better product authentication, or one-tap consumer engagement to create personalised experiences. In healthcare, their flexibility makes them ideal for wearable patches, which could provide a quick and easy way to monitor wounds or even detect heartbeat irregularities. They could also play an important role in a circular economy, providing a scalable way to track reusable packaging or ensure accurate recycling at end of life.

We're at the cusp of an IoE revolution, but we can only truly capture the value if intelligence can be deployed at scale. Flexible chips are the key to unlock that potential and finally make the IoE a reality.

Unleashing the performance of 1200V SiC devices: driving the future of electrification

As the world accelerates toward electrification, driven by the electrification of transport, the global transition to renewable energy, and the growing demand for energy-efficient industrial systems, the role of advanced power semiconductor devices has become more critical than ever. In particular, the 1200V Silicon Carbide (SiC) MOSFET is emerging as an enabler technology, especially in Battery Electric Vehicles (BEVs) transitioning to 800V systems.

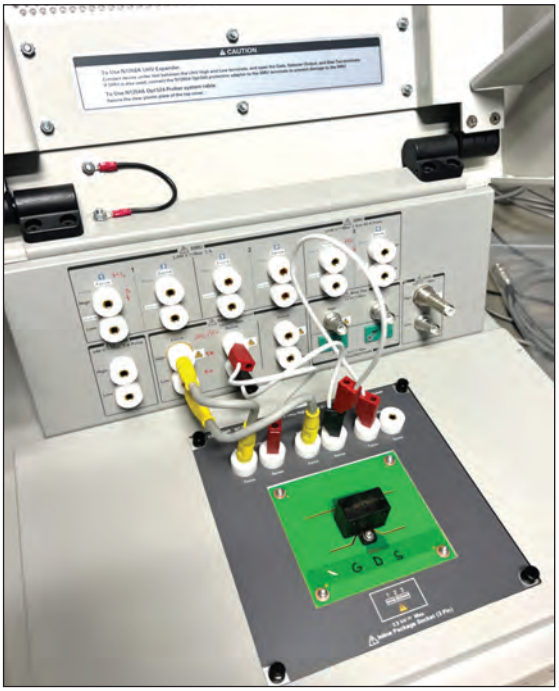
BY AMINE ALLOUCHE IS SENIOR ANALYST, COMPOUND SEMICONDUCTORS AND POWER ELECTRONICS AND POSHUN CHIU IS SENIOR TECHNOLOGY & MARKET ANALYST, COMPOUND SEMICONDUCTORS, BOTH AT YOLE GROUP

RECOGNIZING the immense potential and complexity of these devices, Yole Group and SERMA Technologies have joined forces to present two groundbreaking reports on the performance analysis of SiC MOSFETs. The first report, “SiC MOSFET Discretes Performance Comparison Analysis 2024 Vol 1,” delves into discrete 1200V SiC MOSFETs. The second report, “SiC Modules Performance Analysis 2024 Vol 1,” focuses on the performance of SiC power modules. Together, these reports offer an exhaustive comparison and in-depth analysis of SiC devices, providing essential insights for engineers, designers, and decision-makers in the semiconductor and power electronics industries.

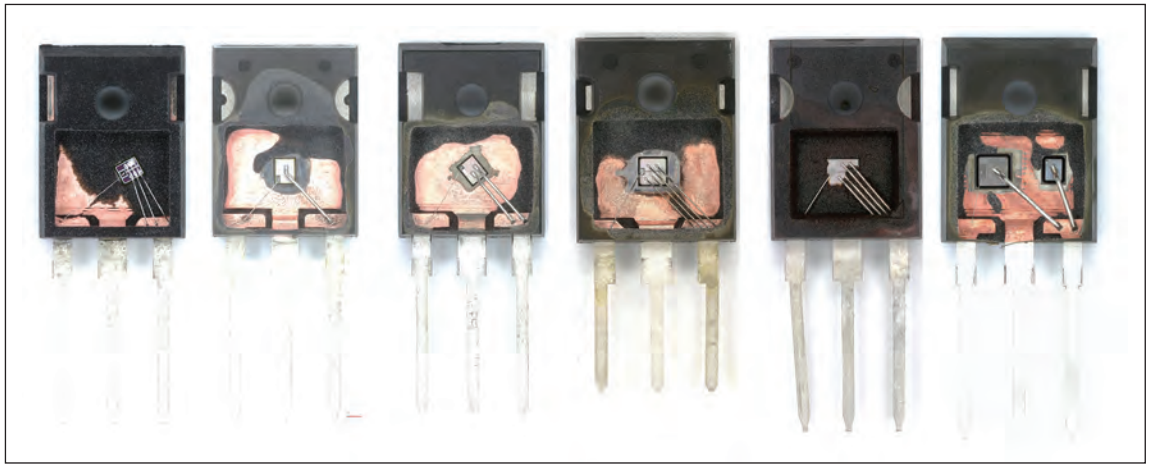
One of the interesting conclusions is that some SiC devices may compete in performance if used in their optimal mode or under specific conditions over various temperature ranges...

The SiC MOSFET Revolution: A game-changer in power electronics

SiC MOSFETs have gained immense traction in power electronics due to their superior properties, which enable them to operate at higher voltages, temperatures, and switching frequencies than traditional silicon-based devices. This makes SiC MOSFETs ideal for applications requiring high efficiency, reliability, and system compactness. In the automotive industry, for instance, the shift from 400V to 800V systems in BEVs is being enabled by 1200V SiC MOSFETs. These devices not only support higher voltage levels but also reduce system losses, enabling faster charging time, improved vehicle range, and enhanced overall efficiency. As a result, SiC MOSFETs are



➤ Test setup for the SiC discrete MOSFETs.



➤ Discrete SiC MOSFETs and Si IGBT: Package opening optical images.

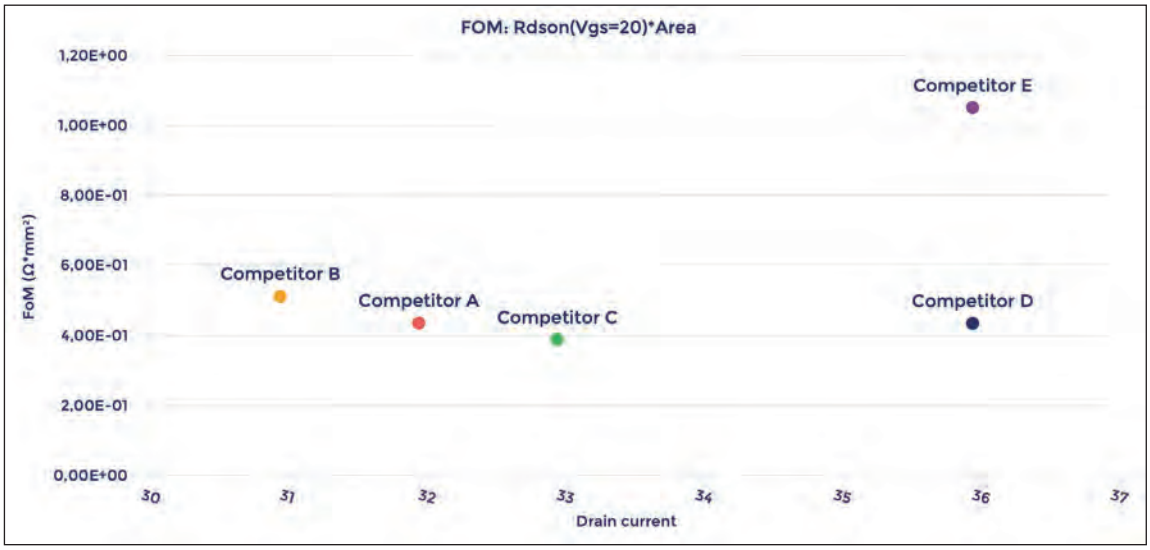
pivotal in the ongoing transformation of powertrain architectures and are becoming increasingly essential in achieving the performance targets set by modern electric vehicles. Among the automotive-qualified discrete SiC MOSFETs covered by both analyses are those using trench technologies from ROHM Semiconductor and Infineon and planar technology from STMicroelectronics. Depending on the test temperature, it was shown that these technologies compete in the performance of some parameters, such as their leakage current or threshold voltage.

The advantages of SiC MOSFETs extend beyond the automotive sector. In renewable energy applications, these devices are crucial in enhancing the efficiency and reliability of power converters in solar inverters and wind turbines. The ability to operate at higher temperatures and switching frequencies allows for more compact and efficient designs, which are essential in the space-constrained environments often found in renewable energy installations.

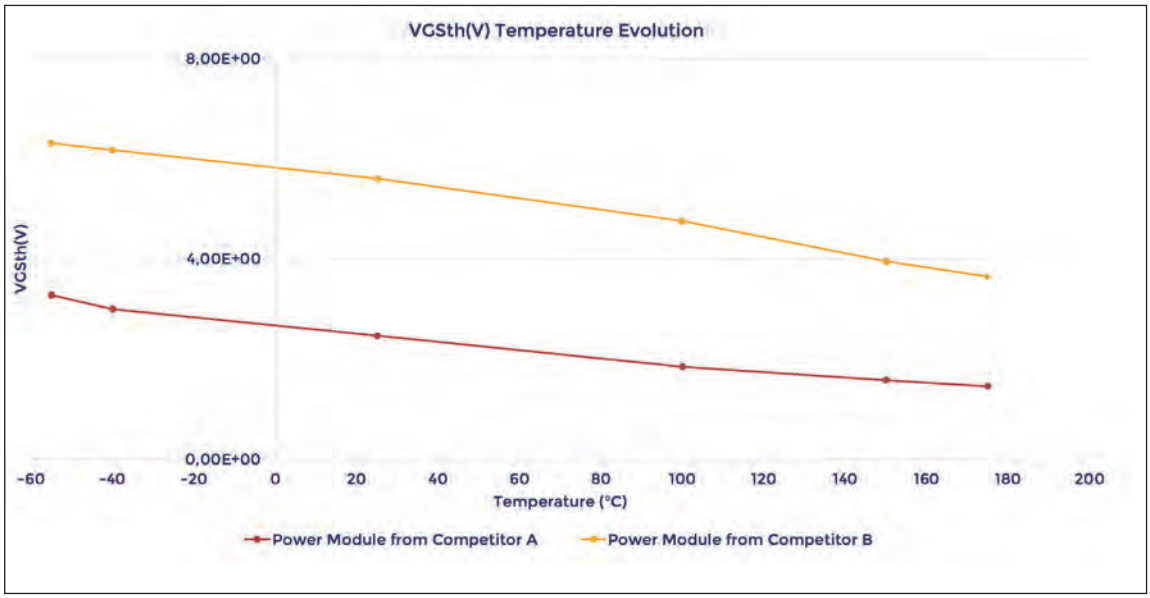
In industrial automation, moreover, SiC MOSFETs are facilitating the development of more energy-efficient motor drives and power supplies. These applications demand high reliability and efficiency, especially in environments where downtime can lead to significant financial losses. The superior thermal and electrical characteristics of SiC MOSFETs ensure that they can meet these stringent requirements, making them the preferred choice for next-generation industrial systems. Among the SiC MOSFETs dedicated to industrial applications and covered by the analyses are a device from Wolfspeed and another from the Chinese player Anbonsemi. Both reports highlight the competitive performances of the Wolfspeed device when tested at specific temperature ranges. Covering players worldwide in these analyses, and specifically including a player from China such as Anbonsemi, allowed us to open a window to an exhaustive Performance Roadmap with a “Worldwide View” and highlight the specific merits of a new wave of devices manufactured in Asian front-end foundries.

SiC device market: an expanding frontier

The market for SiC devices is growing rapidly, with Yole Group forecasting that it will exceed a staggering US$10 billion by the end of this decade. This growth is fueled by the rising demand for more efficient power electronics in BEVs, renewable



➤ Performance comparison of discrete SiC MOSFETs figure of merit.



➤ Power modules performance comparison: Gate-source threshold voltage evolution in terms of temperature.

energy systems, and industrial automation. However, with this expansion comes the need for rigorous performance analysis to ensure that these devices meet the high standards required for their applications.

Power SiC devices have been increasing penetration across various sectors due to the promising potential to improve performance at the end-system level. In the automotive industry, major OEMs have announced 1200V SiC-based designs for powertrains, recognizing the benefits of higher efficiency and faster charging capabilities. This trend is expected to continue, with the ramp-up of 800V BEV systems to meet the growing demand for longer-range electric vehicles and shorter charging times.

In the renewable energy sector, the push towards grid parity and the need for more efficient energy conversion systems are driving the adoption of SiC devices. The higher efficiency of SiC-based power electronics helps reduce energy losses in solar and wind energy systems, making them more competitive with traditional energy sources. As the cost of SiC devices continues to decrease, their adoption in renewable energy applications is expected to accelerate further.

Besides the automotive and energy segments, multiple industrial applications are interested in adopting Power SiC, such as power supplies, motor drives, and heat pumps. SiC devices are positioned as the technology that provides higher power conversion efficiency and a more compact and lightweight system.

Understanding the critical role of performance benchmarking, Yole Group and SERMA Technologies have developed a comprehensive analysis framework for SiC MOSFETs. Their collaborative efforts culminated in two key reports that provide an objective and thorough performance comparison of discrete SiC MOSFETs and SiC modules under identical test conditions. These analyses go beyond what is typically available in datasheets, offering valuable insights into the real-world performance of these devices.

A Comprehensive analysis of SiC MOSFETs and modules

Yole Group and SERMA Technologies focused initially on the static performance of selected 1200V SiC MOSFETs, providing a detailed examination of their characteristics and performance under various operating conditions and in accordance with JEDEC norms and standards, such as JESD 24 and JEP 183. The analysis includes five discrete SiC MOSFETs from leading global players, including Wolfspeed, ROHM, Infineon, STMicroelectronics, and Anbonsemi, as well as a reference Si IGBT device from Infineon.

The critical metrics evaluated in this report include on-state resistance (RDS(on)), drain-to-source voltage (VDS), threshold voltage (VGS(th)), breakdown voltage (VBR), and leakage currents (IDSS, IGSS) under various temperatures ranging from -55°C to 175°C. Additionally, the report presents data and graphs illustrating the devices' behavior concerning parameters such as RDS(on)(VGS), RDS(on)(IDS), VDS, VGS(th), VBR(DSS), IDSS, IGSS, QG, IDS(VDS), and ISD(VSD).

The physical analysis includes optical and Scanning Electron Microscope (SEM) images, along with detailed measurements of package openings and die cross-sections. These measurements are crucial for understanding how physical attributes impact device performance.

Several Figures of Merit (FoM) on the SiC Devices are also assessed and evaluated in this report: FoM (Qg*RDS(on)) and FoM (RDS(on)*Area). A

technology roadmap of these Figures of Merit is presented based on the test results as well as other performance parameters, such as current density.

The parameters derived from the physical analyses are compiled to facilitate a comprehensive analysis of their impact on the performance of the devices.

For instance, the impact of the transistor cell pitch and other gate physical parameters on the performance metrics are assessed in both analyses. Besides technology and performance, a final component manufacturing cost comparison is also detailed. This is a vital parameter for system makers when choosing devices based on their "performance versus cost" tradeoff.

One of the interesting conclusions of this report is that some SiC devices may compete in performance over various temperature ranges if used in their optimal mode or under specific conditions as identified by Yole Group's and SERMA Technologies' performance test.

By providing such an in-depth comparison of these discrete SiC MOSFETs, the report enables a comprehensive understanding of their performance benefits and limitations, helping engineers and designers make informed decisions when selecting devices for their applications.

The extensive data and analyses presented in this report from three perspectives (Technology, Performance, and Cost) make it an indispensable resource for those involved in designing and selecting SiC MOSFETs. The detailed examination of each device's performance under various conditions ensures that engineers have the information they need to choose the most suitable component for their specific application. This level of insight is particularly valuable in high-stakes industries like automotive and renewable energy, where the choice of semiconductor device can significantly impact the overall system's performance and reliability.

The second collection of reports shifts focus to SiC power modules, which are integral to high-power applications where discrete devices alone cannot meet the power requirements. In the first volume of this collection, the report analyzes the performance of the Semikron-Danfoss eMPack® 1200V SiC Module, a leading-edge choice in high-performance automotive applications. The report also includes a reference IGBT module from Infineon's HybridPACK™ Drive platform for comparison.

The analyses are particularly valuable for understanding the performance of SiC modules in real-world conditions. The performance testing covers key parameters such as on-state resistance, breakdown voltage, threshold voltage, leakage currents, gate charge...

Additionally, the report provides insights into the physical and structural aspects of the modules through detailed teardown analysis, offering a holistic view of how these modules are constructed and how their design influences performance.

For those interested in a more detailed teardown analysis as well as the manufacturing process and cost analysis of the Semikron-Danfoss eMPack® 1200V SiC Module, Yole Group has announced a complementary report, "Automotive Power Modules Comparison 2024," which provides further details on the physical analysis of the packaging and die as well as the production processes and cost of the Semikron-Danfoss eMPack® 1200V SiC Module, along with other leading-edge automotive power modules recently found in electric vehicles.

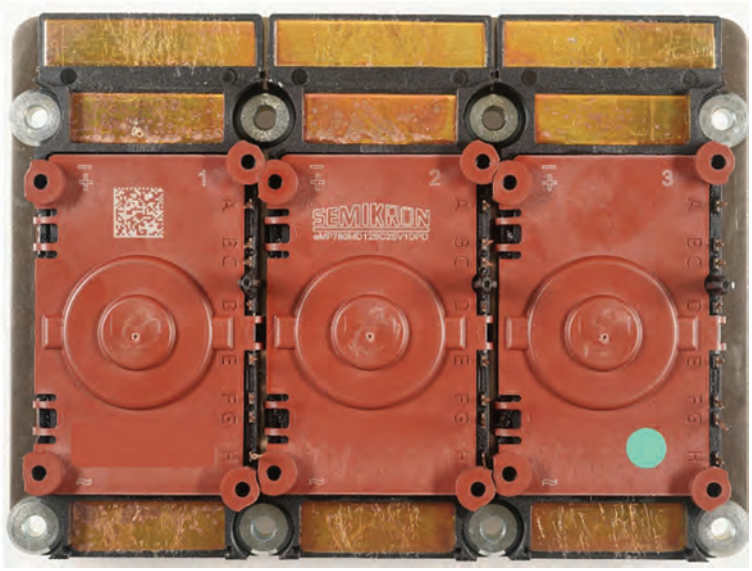
The following volumes of the SiC Module Performance Analysis Collection will cover other leading players in the 1200V SiC Power Module market, analyzing their automotive power modules. The insights gained from these reports are essential for engineers and designers who need to understand the nuances of SiC module performance in high-power applications.

The detailed analysis of the Semikron-Danfoss eMPack® 1200V SiC Module, for example, provides valuable information on how this module performs under different operating conditions, which is crucial for its application in electric vehicles and other high-power systems.

The value of a third-party & objective performance analysis

One of the standout features of these reports is the objective and unbiased nature of the analysis. By conducting tests under identical conditions, Yole Group and SERMA Technologies ensure that the comparisons are fair and accurate. This level of objectivity is often missing in manufacturer-provided datasheets, where conditions may vary, and results may be presented in the most favorable light.

The objectivity of these reports is one of their most significant strengths. In a field where performance claims can vary widely depending on the conditions under which they are tested, having a third-party evaluation that provides consistent and reliable data is crucial. This ensures that the decisions based on these reports are grounded in reality, leading to more reliable and efficient system designs



➤ Analized Semikron - Danfoss Empack 1200V SiC module optical view from above.

For engineers and designers, this third-party analysis is invaluable. It offers a reliable benchmark against which different devices can be evaluated, ensuring the selected devices perform as expected in their intended applications. This is particularly crucial in safety-critical applications like automotive and industrial systems, where device failure can have severe consequences.

The objectivity of these reports is one of their most significant strengths. In a field where performance claims can vary widely depending on the conditions under which they are tested, having a third-party evaluation that provides consistent and reliable data is crucial. This ensures that the decisions based on these reports are grounded in reality, leading to more reliable and efficient system designs.

Pioneering the future of power electronics

As the power electronics landscape continues to evolve, the importance of SiC MOSFETs in enabling next-generation systems cannot be overstated. Whether in BEVs, renewable energy installations, or industrial automation, the superior performance of SiC devices is driving advancements previously unimaginable with silicon-based technologies.

The ongoing shift towards electrification is creating new opportunities and challenges in the power electronics industry. SiC MOSFETs are at the forefront of this transformation, enabling the development of more efficient, reliable, and compact systems than ever before. As more industries adopt SiC technology, the demand for high-quality, reliable performance analysis will only increase, making the reports presented by Yole Group and SERMA Technologies even more valuable.

The reports presented by Yole Group and SERMA Technologies are not just tools for performance analysis; they are essential resources for anyone involved in designing, selecting, and applying SiC MOSFETs and modules. By providing a detailed and comprehensive analysis of these devices, these reports empower engineers to make informed decisions that will shape the future of power electronics.

Conclusion

In conclusion, the transition to 800V systems in BEVs, the growing adoption of renewable energy, and the increasing demand for efficient industrial systems are all driving the need for advanced power semiconductor devices. SiC MOSFETs, with their exceptional performance characteristics, are at the forefront of this transformation.

The comprehensive analysis provided in the reports “SiC MOSFET Discretes Performance Comparison Analysis 2024 Vol 1” and “SiC Module Performance Analysis 2024 Vol 1”” offers a critical resource for understanding and leveraging the full potential of these groundbreaking devices.

As the Power SiC device market continues to expand, with Yole Group forecasts predicting a market size exceeding US$10 billion by the end of this decade, the insights offered in these reports will be instrumental in navigating the complexities of this rapidly evolving field. Whether designing the next generation of electric vehicles, developing renewable energy systems, or working on cutting-edge industrial automation, these reports provide the knowledge and analysis you need to succeed in the era of SiC power electronics.

The future of power electronics is undoubtedly bright, with SiC MOSFETs leading the way toward more efficient, reliable, and compact systems. As industries continue to push the boundaries of what is possible, the insights provided by these reports will be essential in ensuring that the full potential of SiC technology is realized.

FURTHER READING / REFERENCE

- Automotive Power Modules Comparison 2024, Yole SystemPlus, 2024
- SiC MOSFET Discretes Performance Comparison Analysis 2024 Vol 1, Yole SystemPlus, SERMA Technologies, 2024
- SiC Modules Performance Analysis 2024 Vol 1”, Yole SystemPlus, SERMA Technologies, 2024

Pulsiv

DISCOVER

THE FUTURE OF POWER CONVERSION

Achieve breathtaking efficiency, performance, and sustainability with Pulsiv technology

DESIGNED & DEVELOPED IN GREAT BRITAIN

www.pulsiv.com

Large-area sintering for high-performance power module packaging

Examining the benefits of large-area sintering, including thermal resistance and reliability improvements.

BY DR. ANDRÉ SCHWÖBEL, HERAEUS ELECTRONICS GMBH & CO. KG, HANAU, GERMANY AND FRANCESCO UGOLINI, FEDERICO BELPONER, AND DR. ALESSIO GRECI, AMX AUTOMATRIX S.R.L., GAVARDO, ITALY

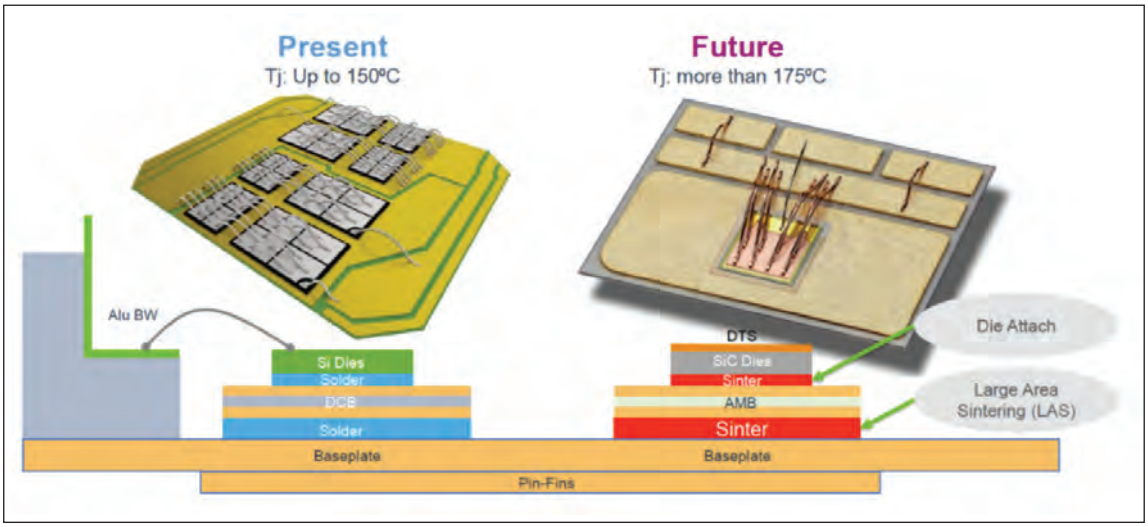
TRADITIONALLY, Si power devices such as IGBTs or MOSFETs were soldered onto the metal ceramic substrate, Aluminum wire bonds were used as interconnection technology and solder paste or thermal grease was used to connect the power module to the baseplate or cooler. Such a structure is shown in Figure 1 on the left side.

The power module package technology needs to undergo drastic changes due to the fast market introduction of Silicon-carbide (SiC) wide band gap (WBG) devices for automotive, new energy and industrial applications. SiC devices like diodes or MOSFETs can operate at higher temperatures, increased power densities and thereby impose larger thermos-mechanical stress on packaging materials.

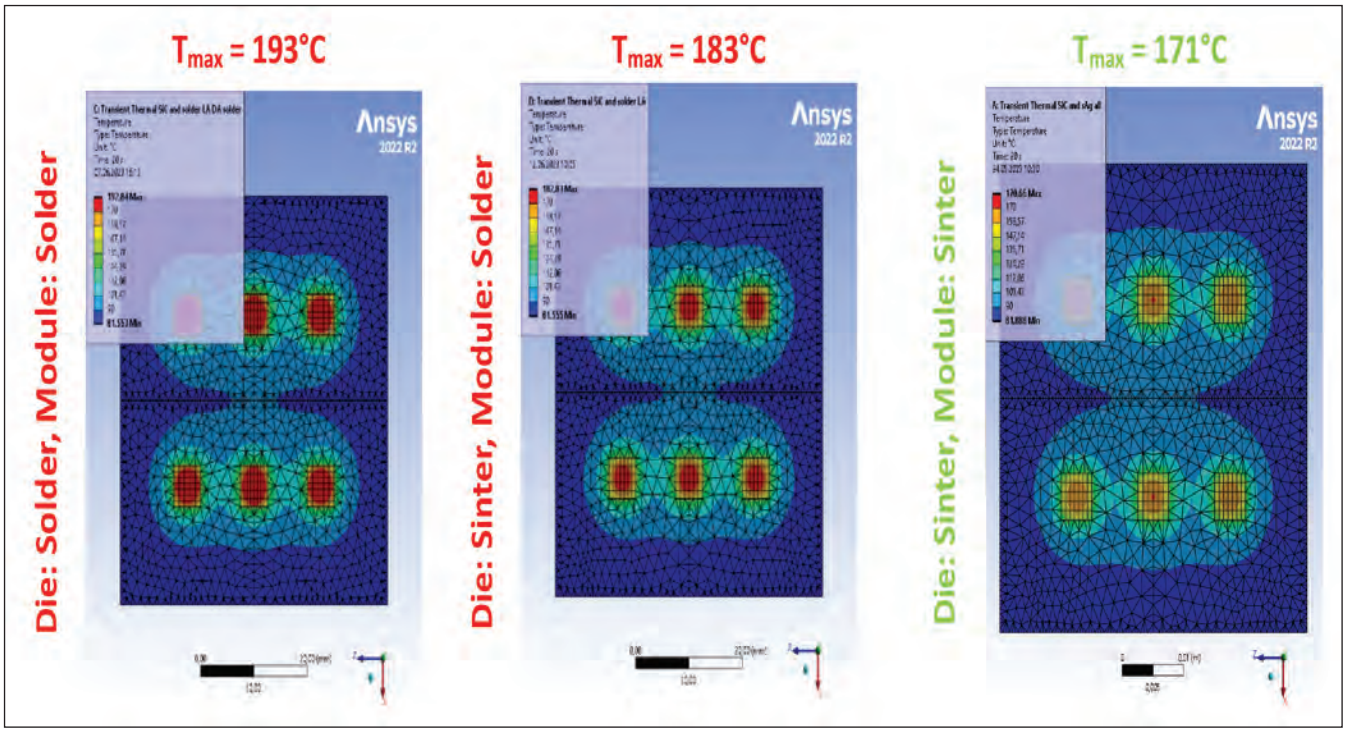
Figure 1 (right side) shows an advanced packaging concept optimized to achieve highest reliability and maximum efficiency in combination with WBG semiconductors. The future module is equipped with Heraeus Die Top System (DTS®) to enable Cu wire bonding on top of the die, combined with Ag-sinter technology to connect the chip to the substrate.

The Al_2O_3 based metal ceramic substrates from the traditional package needs to be substituted by high thermal conductive Si_3N_4 based active metal brazed (AMB) substrates to increase reliability and performance (Figure 1, right side). Finally, the solder material which attaches the module to the baseplate is replaced by a highly reliable and high thermal conductive Ag-sinter material. This process is termed large-area sintering (LAS) as complete modules are sintered onto a cooler.

The improvement in thermal performance by using LAS instead of soldering is shown in Figure 2, where a decrease in die temperature of 22°C was



➤ Figure 1: Traditional package for Si devices (left). Future high reliability package for SiC devices (right).



➤ Figure 2: ANSYS simulation results of the steady-state temperature distribution of various packaging concepts. From left to right: Module and die soldered, module soldered and die sintered, fully sintered module. Simulation details: PLoss = 202 W per chip, SiC die size 5x5x0.15mm^3.

simulated when changing from a fully soldered packaging concepts (left side, Tmax = 193°C) to a fully sintered packaging concept (right side, Tmax=171°C). The improvement in thermal resistance allows either to use smaller and therefore more cost-efficient chips to achieve the same output power of a device or run more current through the same semiconductors at the same overall cost.

Additionally, the question of reliability of the joint regarding thermal cycling is one of the key aspects which must be considered for LAS.

LAS for sintering areas beyond 300 mm^2 is still a rather young technology and few modules using this technology are in the field. However, increased demand is foreseen due to the rapid electrification of passenger cars and car manufacturers striving for highest reliability.

This trend sets new requirements to sinter paste manufacturers such as Heraeus and new requirements to sinter press suppliers such as AMX. Whereas die attach is limited by the chip size, the areas for a LAS are significantly larger and be in the range of >2500 mm^2 depending on the module size.

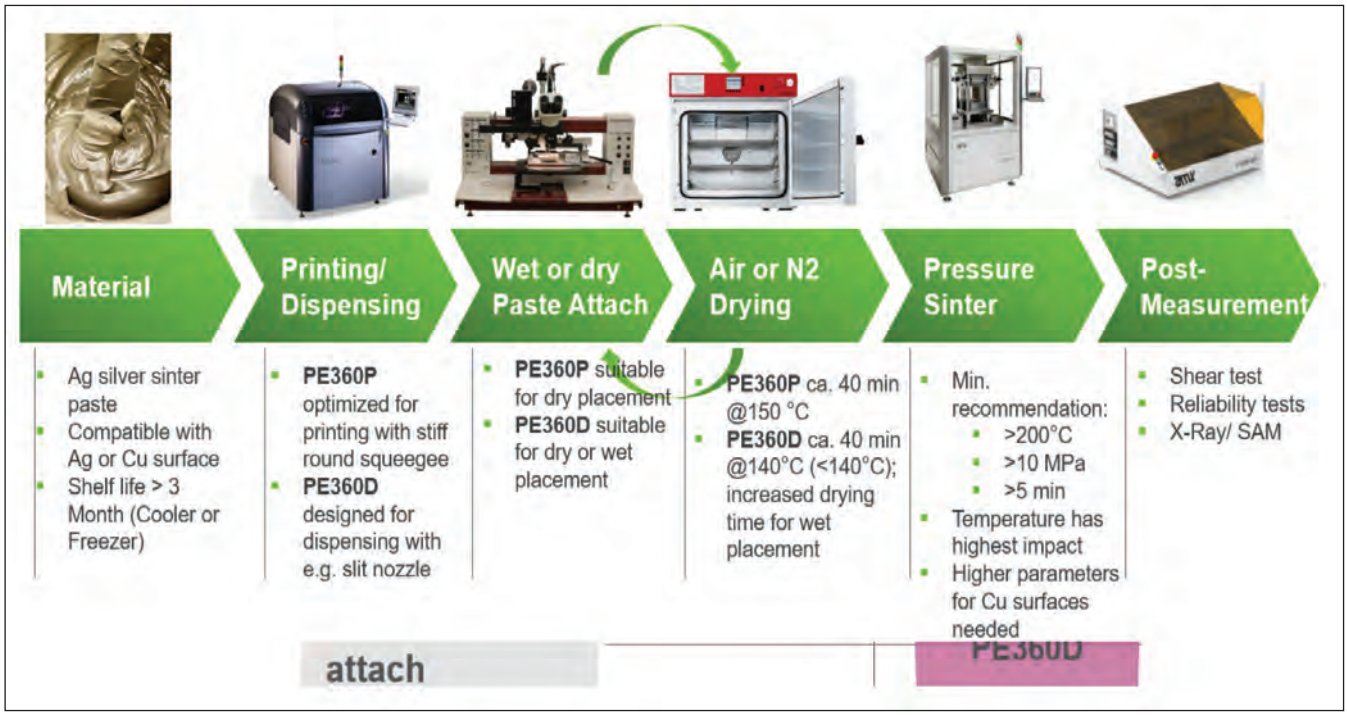
Several concepts such as wet and dry placement of the module into the paste and several application methods of paste such as stencil printing or dispensing have emerged, all with their specific advantages and disadvantages.

Therefore, a careful selection of the suitable paste, application method and sintering technology must be made for each specific package.

Heraeus mAgic paste variants for large-area sintering – PE360P and PE360D

Heraeus Electronics reacted on the trend towards large-area sintering by developing two new Ag pressure sinter pastes, PE360P and PE360D, as depicted in Figure 3. This report is focused on joint properties of PE360P, results obtained by dispensing properties are expected to be the same and will be discussed elsewhere.

➤ Figure 3: PE360 paste variants of Heraeus Electronics suitable for large area sintering applications.



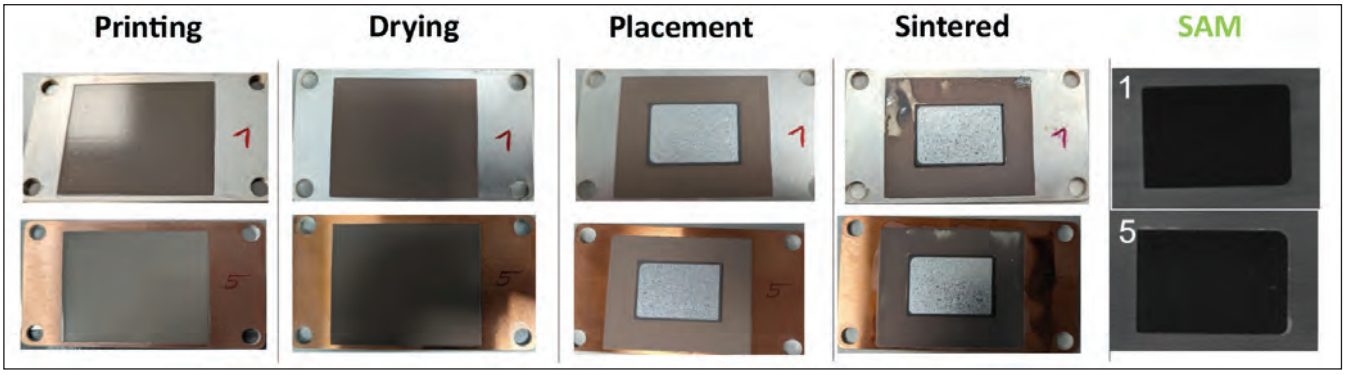
➤ Figure 4: Process flow for both PE360 variants, including wet or dry placement.

PE360P is designed for printing applications such as stencil or screen printing and ensures a processability of more than 8h on the printing machine. PE360P was designed for placement of molded packages or bare substrates in the range of 40x40 mm² up to 100x100 mm² onto the pre-dried paste.

For this kind of size, a dry placement process is favorable as the drying process of the paste is done without covering the paste by the module or baseplate, which ensures an efficient evaporation of solvents and additives before the actual sintering process. However, the influence of the warpage of the module and baseplate is a drawback for the dry placemen process, which needs to be addressed. The process flow for dry placement and wet placement is shown in the scheme of Figure 4. An example of the performance of the PE360P paste is shown in Figure 5. AMB substrates with Ag surface were sintered onto flat baseplates made from Cu.

The baseplates were used for sintering either with bare Cu surface or with an Ag plating. The sintering was done on the AMX P101 equipment with 20MPa and 250°C in Nitrogen for 5min. The paste was fully dried prior sintering. The corresponding ultrasonic scans show excellent connection and almost no visible voiding on Copper and Silver-plated baseplates indicating optimal thermal and mechanical connection between substrate and cooler. Furthermore, the reliability of the sinter joint was tested by thermal cycling (TCT).For this purpose, Ag plated AMB substrates with 0.3mm Cu thickness were sintered onto Ag-plated Cu-core baseplates (P360P paste, 230°C sinter temperature, 5min sinter time, 12MPa pressure). The delaminated area was inspected by ultrasonic scanning after 1000 cycles and 2000 cycles of thermal shock. The resulting pictures are presented in Figure 6.

After 1000 cycles of thermal cycling almost no delamination can be seen when using large-area



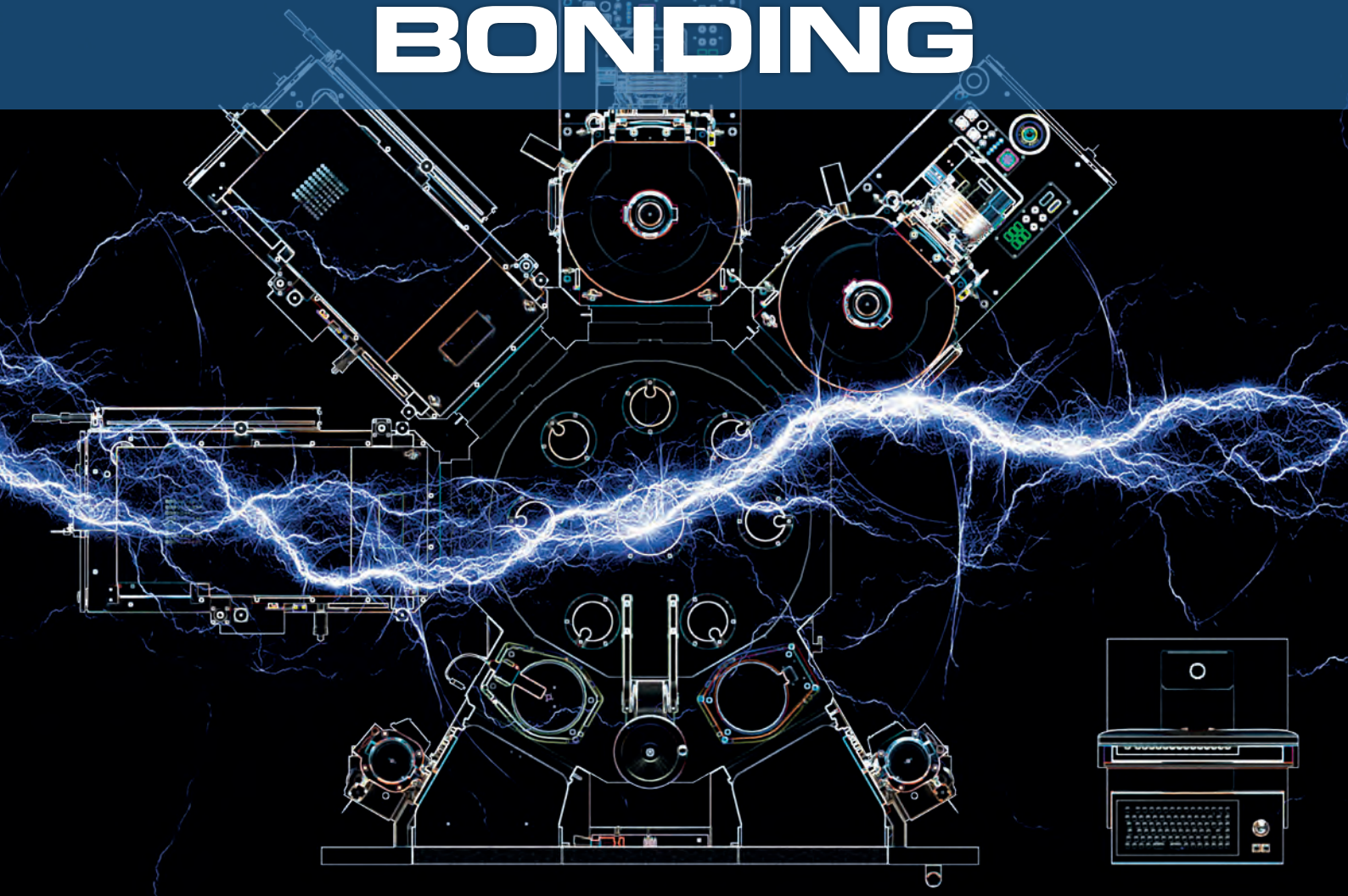
➤ Figure 5: Process flow and scanning acoustic microscopy (SAM) images of PE360P sintered AMBs substrates on Ag plated and bare Cu baseplates.

EVG®

invent
innovate
implement

www.EVGroup.com

HIGH-VACUUM BONDING



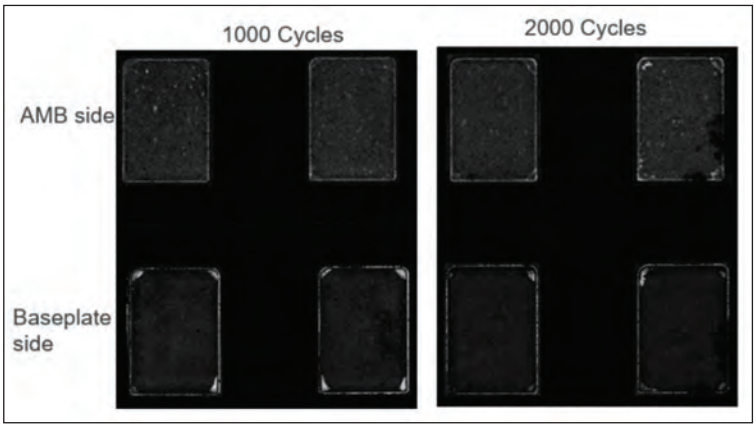
EVG® ComBond®

Oxide-free, covalent wafer bonding

High-vacuum process environment

Room-temperature process

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com



➤ Figure 6: SAM images of the AMB side and the baseplate side after thermal cycling. The area of each of the substrates is approximately 1000 mm². TCT condition: -55°C/+150°C (20min dwell time).

sintering. Only minor defects can be detected at the corners of the test samples, which can be addressed to highest stress levels occurring at these positions. The delamination is mainly located at the baseplate side of the connection. Only minor changes are seen upon 2000 cycles of TCT, which proves the excellent reliability of the sinter joint.

In response to the discernible demand emanating from the automotive industries and tier one suppliers, AMX has undertaken an expansion of its existing equipment portfolio specifically directed towards the incorporation of specialized machinery tailored to meet the exigencies of large-area sintering applications.

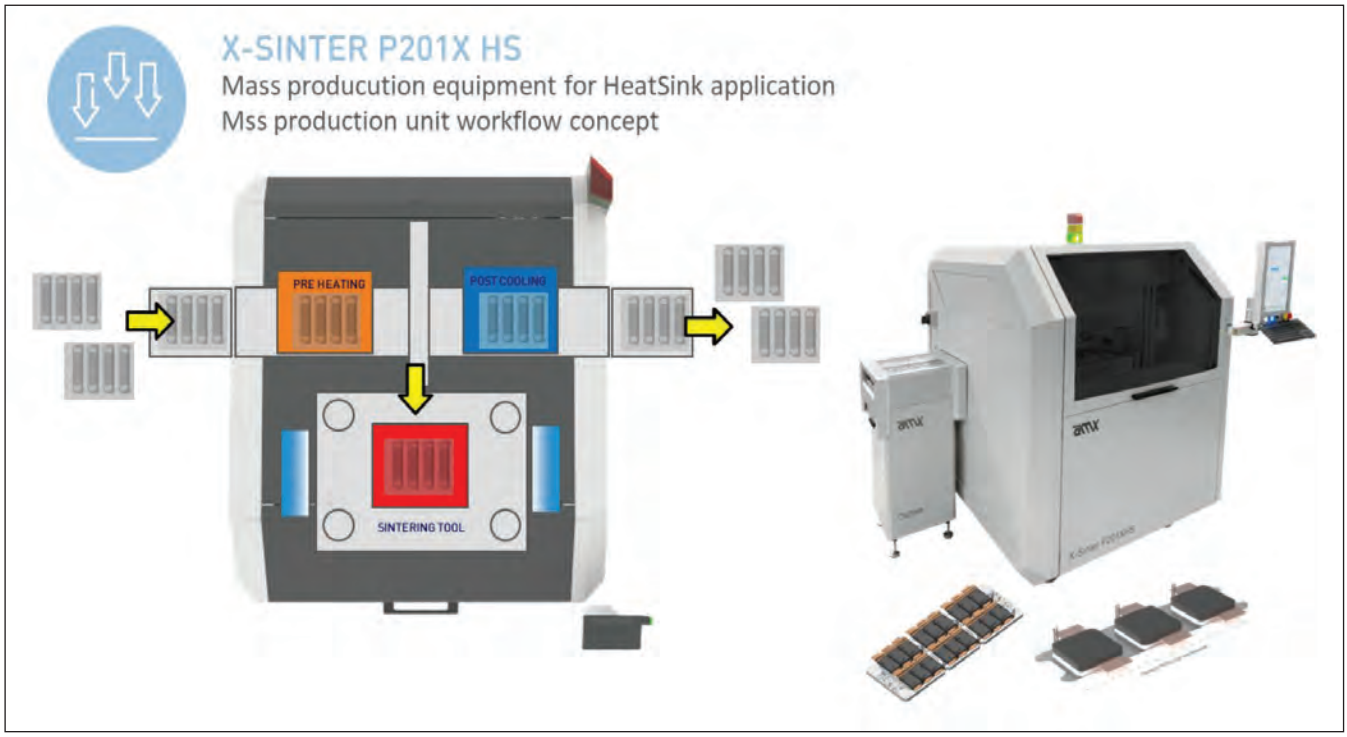
Within this initiative, the sintering area has been significantly augmented, reaching dimensions of 300mm x 300mm for the Research and Development unit (X-Sinter P55). Simultaneously, the mass production equipment (X-Sinter P201X) has undergone enhancements to accommodate the demands of heatsink pressure sintering applications, culminating in the introduction of the X-Sinter P201XHS model.

The primary objective of these modifications has been to optimize production batch processes while sustaining a high production rate, as evidenced by Technical Availability VDI3423 exceeding 99%. The design of the units is crafted to seamlessly integrate within a fully automated workflow scenario. On the software front, these units are adaptable to Industry 4.0 networks through compatibility with communication systems such as SecsGem, OPCUA, OPCON, or other advanced MES platforms.

Furthermore, the process cycle time has been enhanced through the integration of a pre-heating system, ensuring the maintenance of elevated temperatures in the cooler, complemented by a post-cooling plate after the sintering. Additionally, an optional full nitrogen cabinet is available, serving as a preventive measure against Busbar oxidation. This comprehensive approach underscores AMX's commitment to advancing technological capabilities in compliance with industry demands.

Summary

Within this study the benefits of large-area sintering, such as improvements of thermal resistance and the improvement of reliability were presented using Heraeus' new PE360 large-area sintering paste and AMX equipment. Both companies offer leading edge solutions for the future demands in terms of sinter applications.



semi

Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium

Controlling the qubits — overcoming DC bias and size challenges in quantum

Quantum computing, with its promise of efficient calculations in challenging applications, is rapidly advancing in research and development. The pivotal technology for quantum computing lies in the control and evaluation of qubits. This article explores the challenges and solutions associated with the size of quantum computers as well as the DC voltage bias sources crucial for controlling and evaluating flux-tunable superconducting qubits and silicon spin qubits.

BY GOBINATH TAMIL VANAN, PRODUCT MANAGER, KEYSIGHT TECHNOLOGIES

QUANTUM COMPUTING is gaining attention for its ability to solve complex problems that prove difficult for regular computers. In this journey, instruments like the DC bias source play a crucial role, especially for flux-tunable superconducting and silicon spin qubits. The DC bias source helps to adjust the flux to decide the resonance frequency of the superconducting qubit and to apply DC bias voltage to each gate terminal of silicon spin qubits.

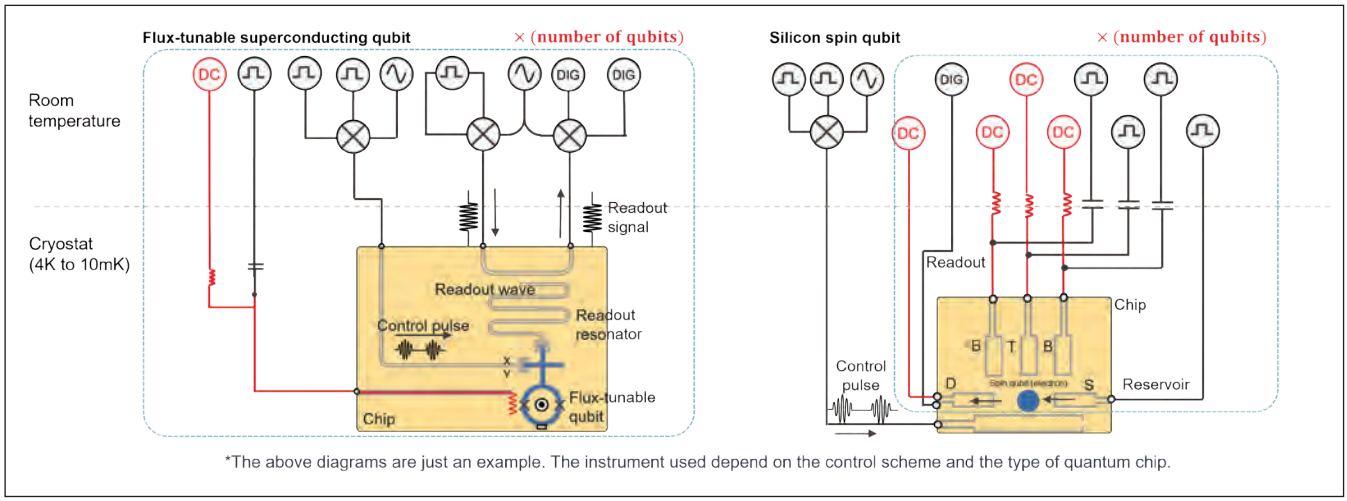
In addition, the number of qubits employed in a quantum computer increases the physical size of the machine based on the number of DC bias sources needed to control the qubits.

An engineer can initialise, control, and read the qubit states by using control evaluation systems, as depicted in Figure 1. This control evaluation system enables the characterisation of qubit properties like coherence time and fidelity and the execution of benchmark tests, thereby advancing the research and development of quantum computers.

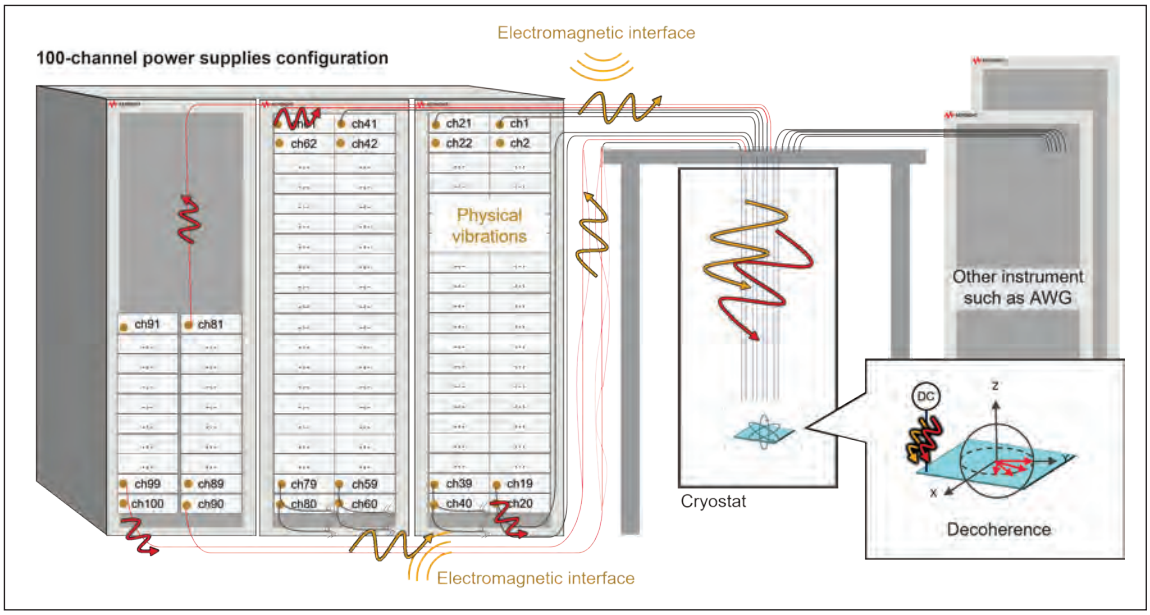
Challenges in DC biasing of qubits

There are two significant challenges when using DC power supplies:

- Voltage fluctuations due to DC power supply noise and environmental interference through long cables induce qubit decoherence.



➤ Figure 1. Single qubit control and evaluation system for flux-tunable superconducting and silicon spin qubits. The instruments and lines indicated in red represent the DC voltage bias source and wiring. For the flux-tunable superconducting qubit, the DC voltage bias source helps tune the resonance frequency using the magnetic flux generated in the coil. For the silicon spin qubit, the DC voltage bias source works by tuning the electric potential of gate terminals.



➤ Figure 2. Fluctuation in DC voltage bias propagated to qubits

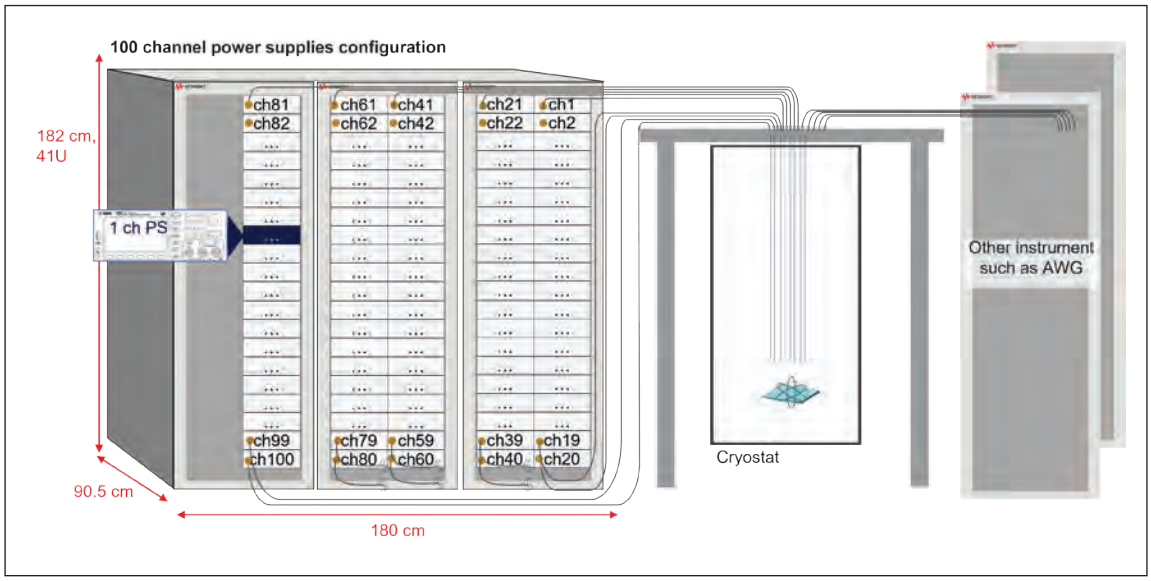
- DC power supplies that may number several hundred require substantial storage space and can introduce significant qubit decoherence.

Qubits are highly susceptible to noise and even minor voltage fluctuations. DC bias voltage can quickly induce unintended changes in the quantum state. These changes can lead to the loss of information stored in the qubit, a phenomenon known as decoherence. This results in a decline in the precision of qubit control and evaluation. Moreover, quantum computers have now reached a stage where they can exceed 100 qubits. It is essential to supply an independent DC bias to each qubit by securing substantial space to house several hundred general power supplies.

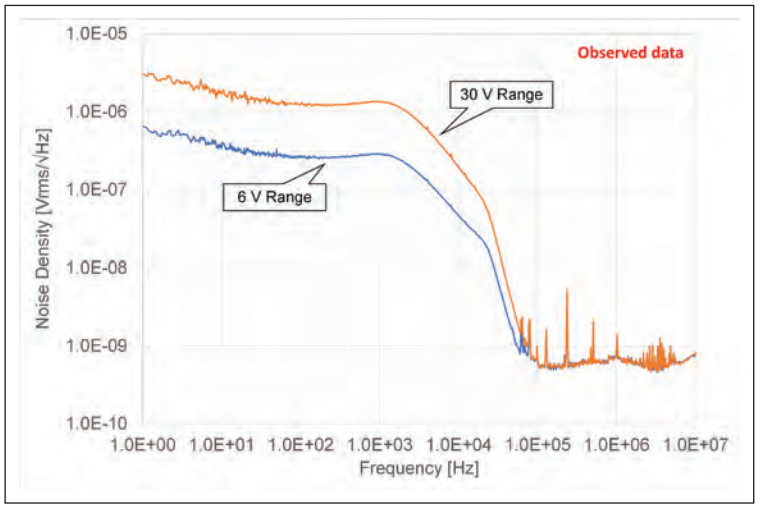
Voltage fluctuations induce qubit decoherence
In the quantum world, qubits exist in a superposition of states, representing both 0 and 1 simultaneously. This unique property makes them exceptionally powerful for certain computations. However, it also makes them incredibly sensitive to external influences. The challenge arises when DC power supply noise and environmental interference introduce voltage fluctuations that disturb the delicate balance of the qubit's superposition.

Even the slightest variation in voltage can cause the qubit's quantum state to waver, leading to decoherence making them less reliable for computations. This is a significant challenge in quantum computing because maintaining the integrity of qubit states is crucial for accurate and reliable quantum information processing.

Fluctuations in DC bias voltage primarily contribute to the DC power supply's output voltage noise. Furthermore, environmental interference, such as electromagnetic interference and physical vibrations of the cables, can contribute to voltage instability.



➤ Figure 3. Configuration of 100-channel conventional precision power sources with a large footprint.



➤ Figure 4. Voltage source noise density with the combination of a source metre and a low-noise filer adapter.

The qubit's sensitivity to noise necessitates continual monitoring of the potential noise source. Figure 2 illustrates how this effect becomes more pronounced when extending the cables because the DC power supply rack is at a distance from the entrance of the cryostat or if the power supply is in the lower sections of the rack.

The occurrence of voltage fluctuations disrupting qubit coherence is rooted in the fundamental nature of quantum systems. The challenge is not just about preventing external disturbances but also about developing tools and technologies that can shield qubits from these disturbances, ensuring stable and coherent quantum states for reliable computational processes.

Larger quantum computers can introduce more qubit decoherence

One important direction in the practical application of quantum computers is the increase in the number of qubits to run more complex quantum algorithms. For example, the current noisy intermediate-scale quantum (NISQ) machines under development require the implementation of tens to hundreds of qubits. This means the need for significant numbers of DC power supplies that both need to be physically stored and can introduce a lot of noise into the system.

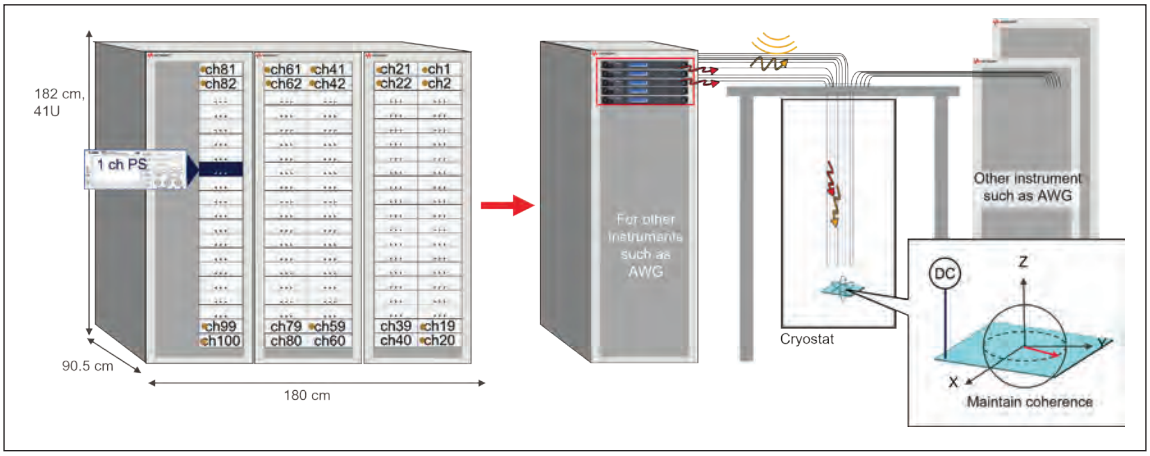
This proliferation of DC bias sources introduces additional sources of noise into the system. The noise from DC bias sources can stem from several factors:

- **Power Supply Imperfections:** Not all power supplies were made for precision, and even small fluctuations or imperfections in the DC bias source can translate to noise in the qubit's operation.
- **Crosstalk:** In a setup with numerous DC bias sources in close proximity, crosstalk can occur. This means that the adjustments made to one qubit's bias source can affect neighbouring qubits, leading to unwanted noise.
- **Electromagnetic Interference (EMI):** The operation of multiple DC bias sources in a confined space can generate electromagnetic fields that interfere with each other. This interference can manifest as noise that disrupts the qubits' quantum states.

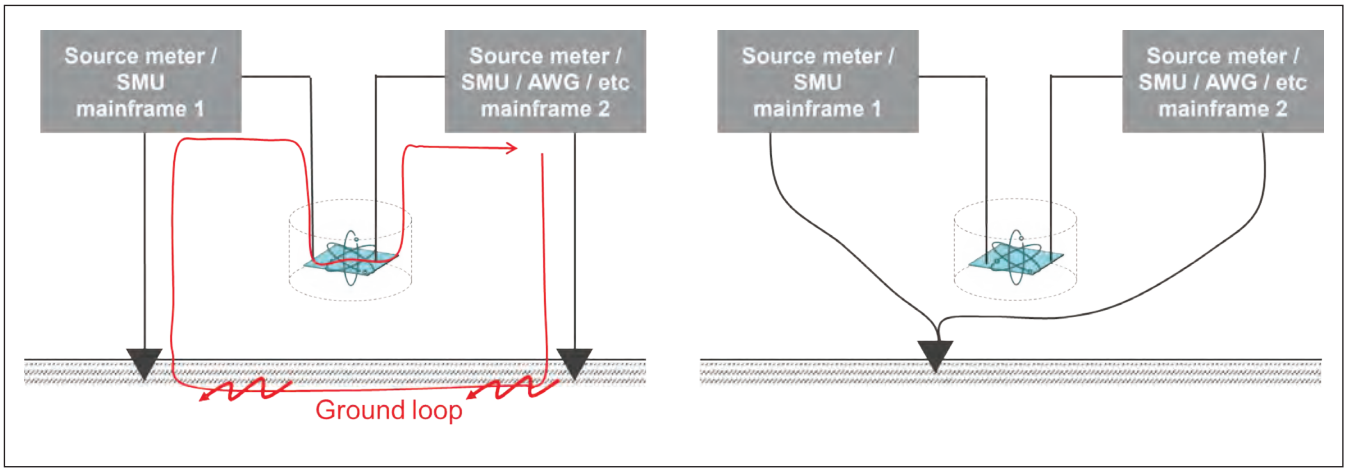
As the number of DC bias sources increases to accommodate a larger number of qubits, the overall size of the system increases, and the cumulative effect of these noise sources becomes more pronounced. Each additional DC bias source adds another layer of potential noise, making it challenging to maintain the precision and coherence of the qubits' states.

Taking an example of a quantum computer that uses 100 qubits, providing DC bias voltage to each qubit presents an additional challenge. Figure 3 illustrates that each qubit requires at least one DC power supply. The test rack must fit in a minimum of 100 power supply channels to bias all qubits. Even with power supplies of a typical size 2U half-rack housed in a maximum-sized rack, a single rack can only store 40 channels.

Consequently, securing an ample space measuring 180 cm in width, 90.5 cm in depth, and 182 cm in height for three racks becomes necessary in a laboratory filled with various other instruments, such as arbitrary waveform generators (AWG). This necessity creates a logistical challenge regarding physical space within quantum computing



➤ Figure 5. A 100-channel configuration with high-density source metres set close to the cryostat, providing clean DC bias voltage.



➤ Figure 6. Examples of wiring that creates a ground loop (left) and avoids a ground loop (right).

laboratories. This spatial challenge not only impacts the physical layout of the lab but also raises practical concerns about efficient management, accessibility, and equipment maintenance.

There is a growing emphasis on developing compact and efficient power supply solutions that can cater to the individual requirements of each qubit while minimising the overall footprint to address this challenge. Streamlining the power supply infrastructure is crucial for the scalability of quantum computing projects, enabling researchers to expand their quantum systems without space constraints.

Enabling an effective and efficient quantum computing development

Solving spatial constraints helps scale quantum computing efforts, enabling researchers to explore larger quantum systems. Managing voltage fluctuations and spatial limitations in DC bias sources for quantum computing is crucial for progress.

It is essential to use low-noise power supplies or source metres / source measure units (SMUs) to provide clean bias voltage positioned as close as possible to the cryostat to achieve this. This approach can significantly help with unnecessary environmental interference caused by exposed cable lengths.

You can attach optional accessories, such as a low-noise filter adapter (LNF), to the precision source metres to further push the stability of the bias voltage. In some cases, reducing the noise level to 25 µV rms (10 Hz to 20 MHz, 6 V range) is illustrated in Figure 4.

Figure 5 shows, from a rack setup perspective, that using source metres that are as compact in channel density allows for placements directly at the entrance of the cryostat, even at elevated positions. This approach will significantly help to minimise the DC voltage bias fluctuation, enabling ideal quantum control and precise qubit characterisation through long coherence time.

Tips to minimise the fluctuations in the bias voltage
Given the significant impact of the surrounding environment and experimental setup on DC bias fluctuations, achieving a clean bias voltage requires proper setup and usage. When constructing your DC bias line, you can minimise voltage noise and effectively utilise a high-precision source measure unit and a low-noise filter by paying attention to certain aspects.

Avoid ground loops

Using different grounds for each instrument can create a circuit known as a ground loop. Ground loops can be a source of noise. Figure 6 illustrates the steps to stabilise the DC bias voltage. Avoiding ground loops using techniques such as single-point grounding is necessary.

Choose the right LF terminal potential

You can either short the LF terminal to the frame ground or leave it floating. This choice could impact the noise level of the DC bias voltage. If your system design does not have specific requirements for the LF terminal's potential, you can experiment with both configurations and choose the one that yields better results.
Wire to minimise electromagnetic interference impact
According to Faraday's law, electromagnetic induction can contribute to the noise if the HF and LF cables become spatially separated. To prevent this outcome, keep the HF and LF cables as close as possible or use a twisted pair configuration.

Conclusion

To solve these challenges, use a combination of source metre options that helps to provide a high channel density, low noise, and precision voltage supply to provide a stable and clean bias voltage to more than 100 qubits. Ensure the source metres are as close as possible to the cryostat to minimise electromagnetic interference from long cables.

Always take note of the potential configurations of the LF terminal, avoid ground loops, and implement twisted pair configurations to reduce the impact of Faraday's Law further.

Breaking the cycle of breakage:

Innovative approaches to IGBT production

Manufacturers of power semiconductor devices often grapple with high breakage rates and significant financial losses due to stress-related damages during production. These issues not only hinder efficiency but also challenge chipmakers' ability to meet stringent industry standards, particularly within the automotive sector.

BY MECHATRONIC SYSTEMTECHNIK

THE INTRODUCTION of disruptive laser-cutting and wafer handling technologies heralds a new era of possibilities. By meticulously addressing the underlying causes of stress-related failures, manufacturers are empowered to elevate their yield, dramatically reduce defect levels, and ensure unwavering compliance with the most exacting industry benchmarks.

Resolving Stress-Induced Failures

One such prominent Shanghai-based manufacturer successfully overcame several challenges with a high-performance laser system that seamlessly integrated precise power control and high-precision positioning, effectively preventing cracks and chipping. Through the adoption of mechatronic systemtechnik's advanced mLC & mRR laser cutting and ring removing system, the manufacturer effectively resolved these challenges. This innovative solution not only ensured compliance with stringent automotive industry standards but also led to a significant reduction in defect levels.

Founded 25 years ago, mechatronic systemtechnik GmbH has established itself as a high-tech industry leader specialising in automated handling systems for non-standard substrates and non-standard handling requirements. With over 500 systems installed worldwide, the company's expertise spans mechanical, electrical, and control systems engineering.

The problem

The customer, a leading manufacturer of power semiconductor devices, encountered significant difficulties during the Insulated Gate Bipolar Transistors (IGBT) production process. The primary challenge lay in the removal of the TAIKO ring prior to the die separation step. The traditional method employed circular blades for cutting, which

➤ The mLC & mRR laser cutting and ring removing system provides precise and clean cutting of wafers, enabling customization of wafer sizes and shapes with exceptional precision.

often resulted in micro-cracks and required excessive force to remove the ring.

This caused stress-related damage to the dies and also led to substantial financial losses and difficulties in meeting the stringent yield requirements of the automotive industry.

Among the key challenges faced were notably high breakage rates stemming from stress-related damages, which proved to be a significant hurdle. This was compounded by financial losses resulting from an alarming increase in defect levels. Additionally, the inability to meet the stringent yield requirements of the automotive industry added another layer of complexity to an already daunting situation.

The solution

To address these issues, mechatronic systemtechnik implemented their state-of-the-art mLC & mRR laser cutting and ring removing system. This solution leveraged advanced mechatronic and laser technologies to provide maximum control and precision during the cutting and removal processes, significantly reducing stress on the fragile wafers.

Key features of the solution

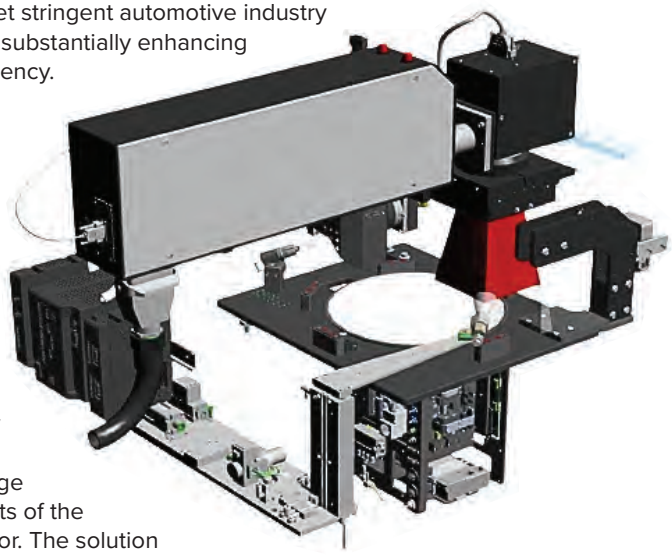
mLC Laser Cutting Unit:
The system features a high-performance laser that allows for precise control of laser power. It also includes a mechatronic high-precision positioning system designed to prevent cracks and chipping. Additionally, there is integrated measurement for assessing cutting and removal performance. A camera system is employed to recognize and align the wafer within the film frame, even when using non-transparent tape. Furthermore, an exhaust system effectively eliminates silicon condensation during the laser cutting process.

mRR Ring Removing Unit:
The mechatronic chuck system features advanced lip seal technology designed for face-down processing. It includes an integrated LED-based UV treatment system that utilizes a rotating wafer and shielding rings to ensure maximum control over the UV dose. Additionally, the system employs a circular movement that effectively minimizes stress within the gap between the tape and the ring.

Handling Sequence:
Continuous monitoring and sensing of wafers is conducted during each handling step, accompanied by unique handshake procedures designed to ensure that no wafer is lost or damaged.

Results

The implementation of the advanced mLC & mRR system delivered remarkable results, enabling the customer to meet stringent automotive industry standards while substantially enhancing production efficiency.

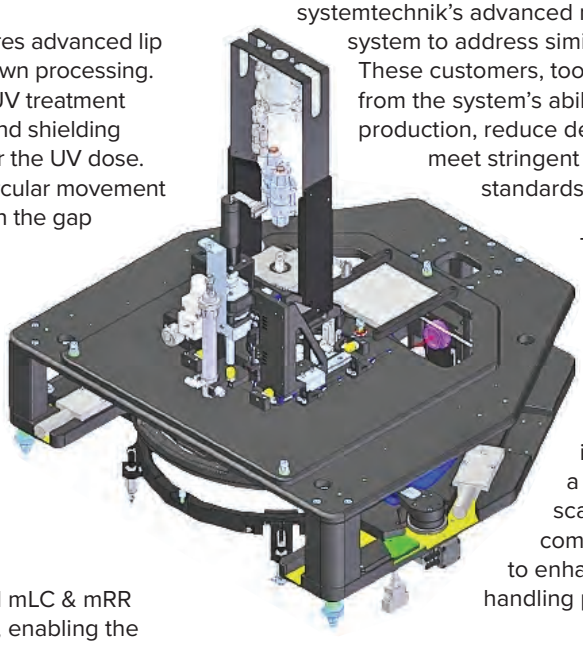


➤ mLC Laser Cutting Unit

Key outcomes included achieving a throughput of up to 60 wafers (12-inch) per hour, tailored to wafer thickness, and consistently meeting the rigorous breakage rate requirements of the automotive sector. The solution effectively eliminated micro-cracks and chipping, resulting in smooth edge surfaces and significantly reduced defect levels at the wafer edges.
Additionally, it provided a more cost-effective solution with lower capital expenditure and a reduced footprint compared to competing technologies.

By leveraging cutting-edge technologies and innovative solutions, the customer achieved notable improvements in production efficiency, yield, and financial performance. The ongoing partnership between mechatronic systemtechnik and the customer promises further advancements in wafer handling and production processes, and plans are underway to explore additional solutions from mechatronic to continue enhancing the manufacturer's capabilities and maintain their competitive edge in the semiconductor industry.

Beyond this individual case, many other manufacturers have also turned to mechatronic systemtechnik's advanced mLC & mRR system to address similar challenges. These customers, too, have benefited from the system's ability to streamline production, reduce defects, and meet stringent industry standards.



➤ mRR Ring Removing Unit

The solution's versatility and proven performance across a range of applications demonstrate its value as a reliable and scalable option for companies looking to enhance their wafer handling processes.

New semiconductor material:

AlYN promises more energy-efficient and powerful electronics

Researchers at Fraunhofer IAF have achieved a breakthrough in the field of semiconductor materials: With aluminum yttrium nitride (AlYN), they have succeeded in producing and characterizing a new and promising semiconductor material using the MOCVD process. Due to its excellent material properties and its adaptability to gallium nitride (GaN), AlYN has enormous potential for use in energy-efficient high-frequency and high-performance electronics for information and communication technologies.

DUE TO ITS excellent material properties, aluminum yttrium nitride (AlYN) has attracted the interest of various research groups worldwide. However, the growth of the material has so far been a major challenge. So far, it has only been possible to deposit AlYN using the magnetron sputtering process.

Now researchers at the Fraunhofer Institute for Applied Solid State Physics IAF have succeeded in producing the new material using MOCVD technology (metal-organic chemical vapor deposition), thus enabling the development of new, diverse applications.

➤ The different color nuances of the AlYN/GaN wafers result from different yttrium concentrations and growth conditions.

"Our research marks a milestone in the development of new semiconductor structures. AlYN is a material that enables increased performance while minimizing energy consumption and can thus pave the way for innovations in electronics that our digitally networked society and the ever-increasing demands on technologies urgently need," says Dr. Stefano Leone, scientist at Fraunhofer IAF in the field of epitaxy.

Due to its promising material properties, AlYN can become a key material for future technological innovations.

Recent research had already demonstrated the material properties of AlYN, such as ferroelectricity. When developing the new compound semiconductor, researchers at Fraunhofer IAF focused primarily on its adaptability to gallium nitride (GaN): The lattice structure of AlYN can be optimally adapted to GaN and the AlYN/GaN heterostructure promises significant advantages for the development of future-oriented electronics.

From layer to heterostructure

In 2023, the research group at Fraunhofer IAF already achieved groundbreaking results when they succeeded for the first time in depositing a 600 nm thick AlYN layer. The layer with a wurtzite structure contained a previously unattained

yttrium concentration of over 30 percent. Now the researchers have achieved another breakthrough: They have produced AlYN/GaN heterostructures with precisely adjustable yttrium concentration, which are characterized by excellent structural quality and electrical properties. The novel heterostructures have an yttrium concentration of up to 16 percent. Under the leadership of Dr. Lutz Kirste, the structural analysis group is conducting further detailed analyses to deepen the understanding of the structural and chemical properties of AlYN.

The Fraunhofer researchers have already been able to measure extremely promising electrical properties of AlYN that are interesting for use in electronic components. “We were able to observe impressive values for the sheet resistance, the electron density and the electron mobility. These results have shown us the potential of AlYN for high-frequency and high-performance electronics,” reports Leone. AlYN/GaN heterostructures for high frequency applications

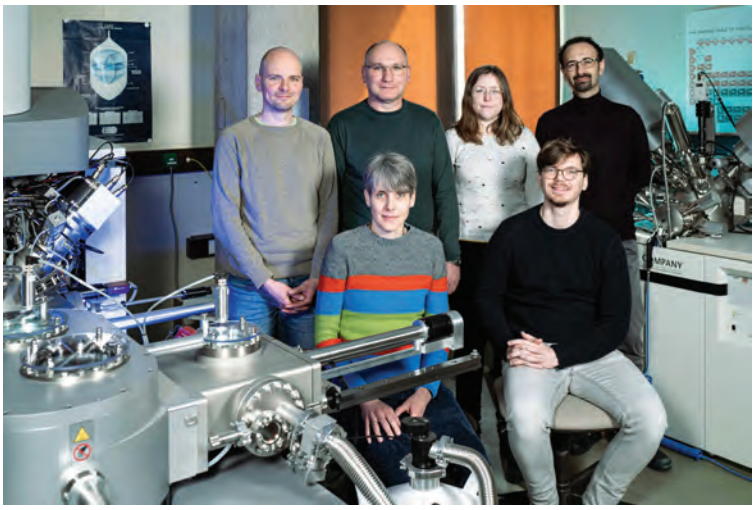
Thanks to its wurtzite crystal structure, AlYN can be adapted very well to the wurtzite structure of gallium nitride with a suitable composition. An AlYN/GaN heterostructure promises the development of semiconductor devices with improved performance and reliability. In addition, AlYN has the ability to induce a two-dimensional electron gas (2DEG) in heterostructures. The latest research results from Fraunhofer IAF show optimal 2DEG properties in AlYN/GaN heterostructures with an yttrium concentration of around 8 percent.

The material characterization results also show that AlYN can be used in high electron mobility transistors (HEMTs). The researchers observed a significant increase in electron mobility at low temperatures (more than 3000 cm 2 /Vs at 7 K). The team has already made significant progress in demonstrating the epitaxial heterostructure required for its fabrication and is continuing to explore the new semiconductor with a view to fabricating HEMTs.

The researchers can also make a positive prediction for industrial use: In AlYN/GaN heterostructures grown on 4-inch SiC substrates, they were able to demonstrate scalability and structural uniformity of the heterostructures. The successful production of AlYN layers in a commercial MOCVD reactor enables scaling to larger substrates in larger MOCVD reactors. This method is considered the most productive for the production of large-area semiconductor structures and underlines the potential of AlYN for the large-scale production of semiconductor devices.

Development of non-volatile memories

Due to its ferroelectric properties, AlYN is highly suitable for the development of non-volatile memory applications. Another important advantage is that the material has no limitation in layer thickness.



➤ With their work on epitaxy and characterization of AlYN/GaN heterostructures, the research team at Fraunhofer IAF achieved a breakthrough in the field of semiconductor materials

Therefore, the research team at Fraunhofer IAF encourages further research into the properties of AlYN layers for non-volatile memories, as AlYN-based memories can drive sustainable and energy-efficient data storage solutions. This is particularly relevant for data centers, which are used to cope with the exponential increase in computing capacity for artificial intelligence and have significantly higher energy consumption.

Oxidation as a challenge

A major hurdle for the industrial use of AlYN is its susceptibility to oxidation, which affects the suitability of the material for certain electronic applications. “In the future, it will be important to explore strategies to reduce or overcome oxidation.

This could be achieved by developing high-purity precursors, applying protective coatings or using innovative manufacturing techniques. The susceptibility to oxidation of AlYN represents a major challenge for research to ensure that research efforts are focused on the areas with the greatest prospects for success,” concludes Leone.

FURTHER READING / REFERENCE

- Scientific publications
  S. Leone et al. “Metal-Organic Chemical Vapor Deposition of Aluminum Yttrium Nitride”, Phys. Status Solidi RRL 17 2300091 (2023)
  https://doi.org/10.1002/pssr.202300091

- I. Streicher et al. “Two-dimensional electron gases in AlYN/GaN heterostructures grown by metal–organic chemical vapor deposition,” APL Materials 12 051109 (2024)
  https://doi.org/10.1063/5.0203156

New silicon carbide MOSFETs and diodes enable higher efficiency in high-voltage applications

Sanan Semiconductor, an emerging leader in wide bandgap power semiconductor materials, components, and foundry services has expanded its SiC power product portfolio with the introduction of 1700V and 2000V devices

THESE CUTTING-EDGE components are set to revolutionize power efficiency in applications ranging from renewable energy to electric vehicle charging infrastructure.

Key highlights of the new product lineup include:

- 1700V SiC MOSFETs with 1000mΩ on-resistance
- 1700V SiC diodes available in 25A and 50A variants
- 2000V 40A SiC diodes, with a 20A version planned for release by the end of 2024
- Development of a 2000V 35mΩ SiC MOSFET (release date in 2025)

“Our new high-voltage SiC devices represent a significant leap forward in power electronics,” said Leo Liao, Project Manager. “By enabling higher DC voltages, these components allow for increased power output at the same current levels, or maintaining system power ratings while reducing current and energy losses dramatically.”

The 1700V SiC MOSFETs and diodes are particularly well-suited for applications requiring extra voltage margins beyond traditional 1200V devices. Meanwhile, the 2000V SiC diodes can be utilized in high DC link voltage systems up to 1500V DC, addressing the needs of industrial and power transmission applications.

These advanced SiC devices offer superior efficiency compared to traditional silicon-based alternatives across a wide range of applications, including:

- Solar string inverters and power optimizers
- Electric vehicle fast charging stations
- Energy storage systems
- High-voltage power grids and energy transmission networks

“As the world transitions to cleaner energy sources and more efficient power systems, the demand for high-performance power semiconductors continues to grow,” added Z.R. Zhang, VP of Sales and Marketing. “Our expanded SiC portfolio demonstrates our commitment to driving innovation in this critical sector.”

The new 1700V and 2000V SiC devices are now available for sampling.

For more information, including detailed specifications and availability, please visit: **www.sanan-semiconductor.com/en** or email:

North America contact: **sanan-semi@luminus.com**
Europe contact: **sales.europe@sanan-ic.com**
China contact: **sales@sanan-ic.com**

To promote your products and services contact:
Shehzad Munshi
T: +44 (0)1923 69015
E: shehzad.munshi@angelbc.com

AIXTRON
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

evatec process systems
Tel: + 41 81 403 8000
Fax: + 41 81 403 8001
www.evatecnet.com

Greene Tweed
SEALS | CONNECTORS | COMPONENTS
gtweed.com

HITACHI Inspire the Next
Hitachi Energy
www.hitachienergy.com

WINSOURCE ELECTRONICS
Tel: + 86-755-83957316
Email: service@win-source.net
www.win-source.net

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT
Tel: +49 7942 945-0
Email: eiSos@we-online.com
www.we-online.com/en/components/products

Showcase your presence to the global Power Electronics industry for 12 months

Promoting your products or your brand through a Corporate Partnership Program in is an economical way to generate interest and drive prospects. Your message will reach over 53,000 professionals worldwide through 3 different mediums of magazine, website and newsletter which creates maximum visibility.

With the largest and most diverse global audience of qualified buyers served by Power Electronics focused magazine, secure a corporate partnership and buyers guide entry and receive 12 months of promotion and exposure to the electronic industry across the magazine portfolio including:

- **Newsletter:** One sponsored newsletter : A sponsor's message (up to 100 words) A 728 x 90 banner displayed at the centre of the alert
- **Magazine:** Listing in 4 issues: A position on the Corporate Partners page for company logo, contact details and web address 300 x 150 pixels.
- **Website:** A button banner 160 x 54 pixels for 12 months plus sponsor logo: 24/7 and 365 days (jpg or .gif; max. **File size:** 15k click-thru URL). https://powerelectronicsworld.net/home
- All Corporate Partners are included in online buyers guide https://powerelectronicsworld.net/buyers-guide/companies

WEBINARS

Specialists with 30 year+ pedigree and in-depth knowledge in overlapping sectors

CS COMPOUND SEMICONDUCTOR · SS SILICON SEMICONDUCTOR · P:W POWER ELECTRONICS WORLD · PIC PHOTONIC INTEGRATED CIRCUITS · SS SENSOR SOLUTIONS

Expertise: Moderators, Markets, 30 Years + Pedigree

Reach: Specialist vertical databases

Branding: Message delivery to high level influencers via various in house established magazines, websites, events and social media

For more information contact:
Jackie Cannon **T:** 01923 690205 **E:** jackie@angelwebinar.co.uk **W:** www.angelwebinar.co.uk
T: +44 (0)2476 718 970 **E:** info@angelbc.com **W:** www.angelbc.com

Angel BUSINESS COMMUNICATIONS

ANGELTECH

ESS EXECUTIVE STRATEGY SUMMIT

CS INTERNATIONAL CONFERENCE

PIC INTERNATIONAL CONFERENCE

PE INTERNATIONAL CONFERENCE

SAVE THE DATE

07-09 APRIL 2025

Sheraton Brussels Airport Hotel

To find out more about our sponsor and speaker opportunities, contact us today on:
+44 (0) 2476 718970

or email:

info@csinternational.net

info@picinternational.net

info@peinternational.net