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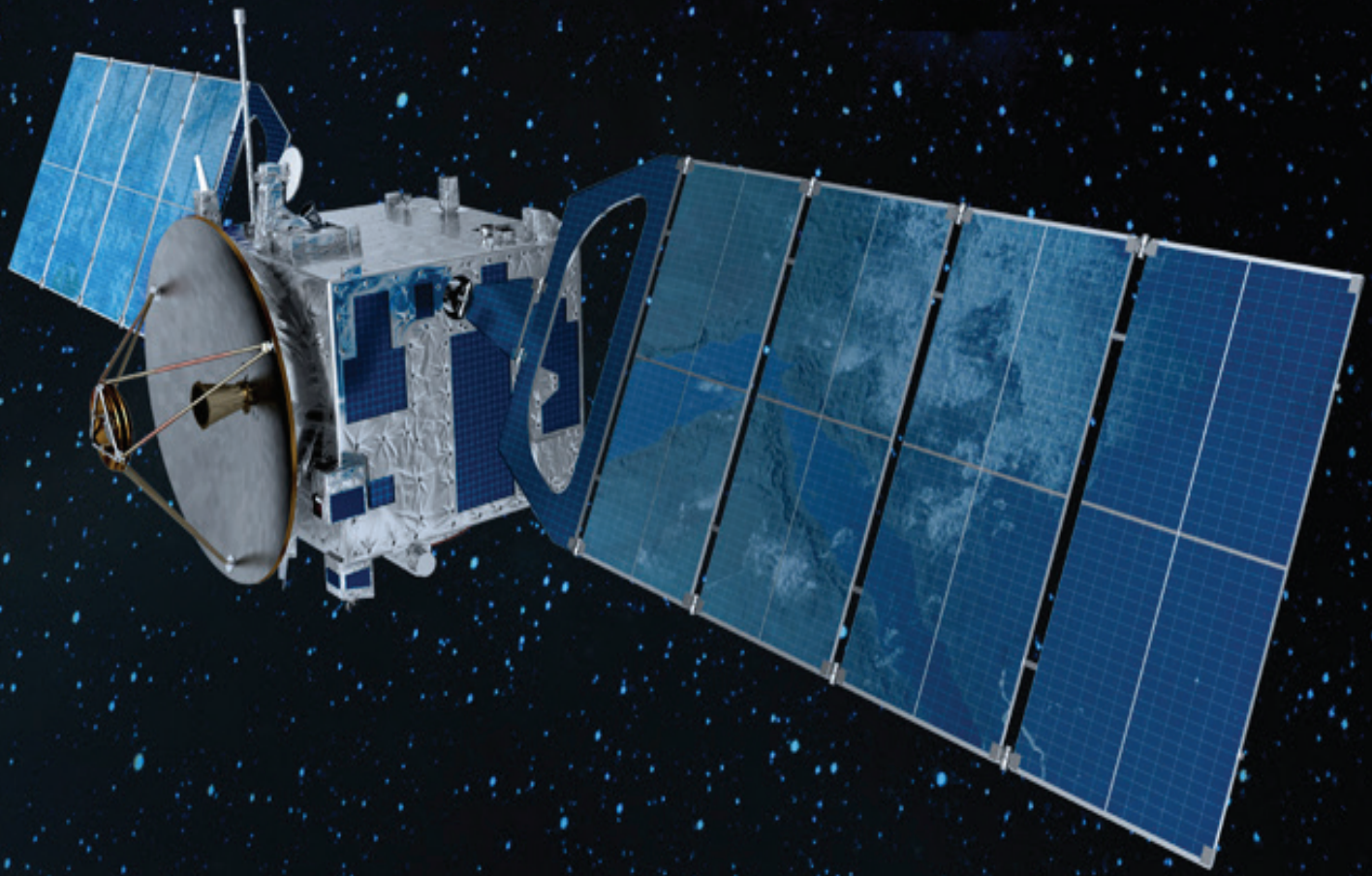

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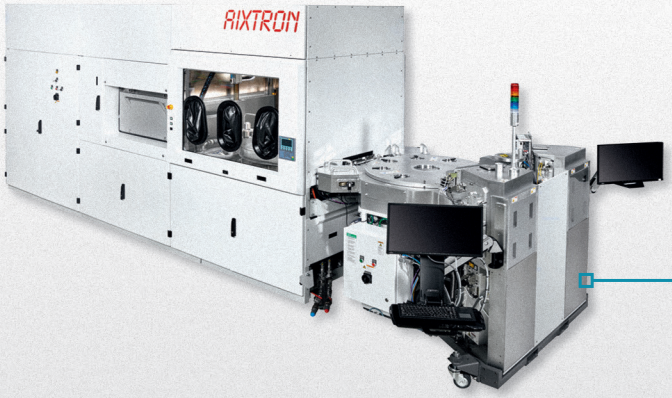

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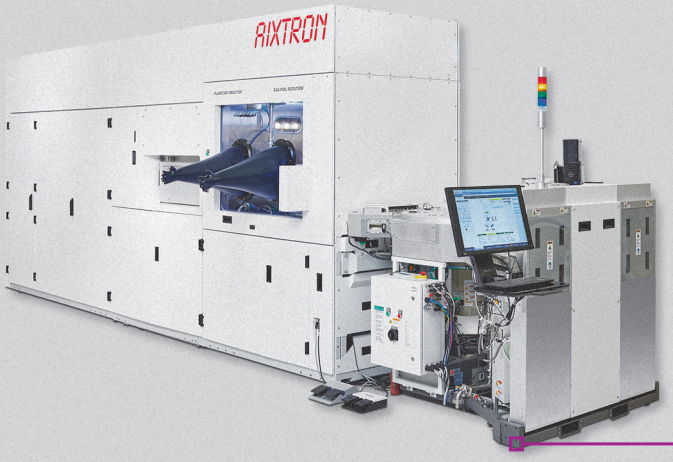

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VIEWPOINT

BY PHIL ALSOP
EDITOR

A busy time for the power electronics industry

IF BEING BUSY is a sign of a thriving business or overall industry sector, then it seems safe to report that the power electronics world is a picture of health right now.

In the news pages, you can read that Infineon's Smart Power Fab has received final funding approval, alongside news of the EU's new ENLIGHTEN project that 'aims to produce a new 1200V DC electric powertrain that offers higher performance, optimised costs and a more sustainable system architecture than today's 800V systems, while ensuring compatibility with existing charging infrastructures'.

There's also a cluster of news announcements from the UK, with the CSA Catapult talking about the importance of compound semiconductors in relation to AI, a partnership between the CSA Catapult and Cadence Design Systems to address long-term skills needs within the semiconductor design sector and to support the industry's growth by providing critical design services to SMEs and scale-up companies across the UK, and Vishay Intertechnology making an investment focused on electric vehicles.

Talk of which brings us to Yole Group's overview of the Silicon Carbide market, which reveals a battery electric vehicle slowdown, seen as only temporary, and not impacting the predicted $10 billion power SiC market to be reached in 2029. Yole has also released the first volume of automotive white papers, which looks at China's pivotal role in automotive semiconductor innovation and outlines the plan to onshore/reshore more and more of the supply chain.

With GlobalFoundries recently announcing a $16 billion US investment (not covered in this issue), it seems that the industry's well-established, global supply chains are being impacted by the plans of individual countries and regions to 'take back control'.

Article-wise in this issue, we have our cover story contribution from Texas Instruments focusing on using gallium nitride (GaN) field-effect transistors (FETs) in a power supply to help boost efficiency and enable operation at higher switching frequencies, helping designers meet the strict power requirements in space-grade radiation-tolerant and radiation-hardened applications. On the same subject, we have an article from the European Space Agency, confirming that, for future space missions, makers of electrical systems need better power devices, a requirement that's met by SiC

Soitec outline Power-SOI 300mm substrates for advanced gate driver ICs to drive power conversion wide-bandgap devices at high switching frequency; Nanopower talks about how the nPZero power-saving IC enables sensor system operation at the nanoamp level; and Keysight outlines the approach to dynamic characterisation of a power semiconductor bare chip.

As if that's not enough content to be getting on with, there's some great news analysis articles, opinion pieces and, importantly, research news: boosting the blocking voltage of birectional HEMTs; building better multi-channel Schottky barrier diodes; UK scientists to tackle AI's surging energy costs with atom-thin semiconductors; bringing quantum communications to existing national-scale telecommunication infrastructure.

I hope you enjoy reading this issue as much as I did in compiling the content.

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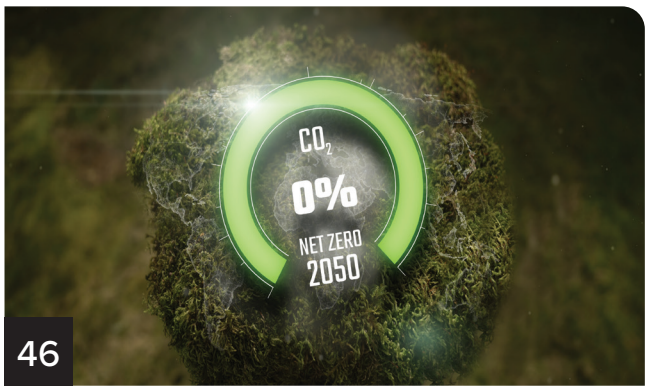

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German government approves Infineon Dresden fab funding

Construction of the new factory proceeding as planned, building shell almost complete

INFINEON TECHNOLOGIES has received final approval for the funding of its new plant in Dresden (Smart Power Fab) from the German Federal Ministry for Economic Affairs. This follows the EC's approval of funding under the European Chips Act on 20 February 2025.

The fab, which will be focused on silicon-based power electronics using 300-mm technology, is planned to be opened in 2026.

Infineon, which is expanding the site to meet customer demand for example for renewable energies, efficient data centres and electromobility, will invest €5b of its own money, creating as many as 1,000 new jobs. This figure does not include additional jobs which will be generated in the investment's ecosystem: Experts expect a positive job effect of 1:6.

In addition, Infineon is also investing in Dresden through its participation in the joint venture European Semiconductor Manufacturing Company (ESMC) GmbH.

"The final funding approval for our Smart Power Fab is an important milestone for us as a company and is a clear signal to the European semiconductor ecosystem," says Infineon CEO Jochen Hanebeck.

"We are grateful to the German federal government, the Free State of Saxony and to the European Union for their support. The semiconductors we manufacture in Dresden are our contribution to making the future value chains of key European ¬industries even more robust."
Construction of the Smart Power Fab, currently one of Germany's largest building projects, is proceeding as planned, with the building shell currently nearing completion.

Infineon held a topping-out ceremony together with all those involved in construction activities in early April this year.

EU project to develop 1200V DC powertrain

THE EU-funded project 'nExt geNeration 1200V eLectric hIGH volTage powErtraiN' (ENLIGHTEN), which runs until 2028, will be built around GaN chips.

The aim is to produce a new 1200V DC electric powertrain that offers higher performance, optimised costs and a more sustainable system architecture than today's 800V systems, while ensuring compatibility with existing charging infrastructures.

The system will incorporate a dual-voltage battery system that can be dynamically adjusted while driving; fast and efficient GaN-based DC/DC converters; an integrated motor-inverter powertrain to achieve superior power density and efficiency including an E-drive inverter using a multilevel GaN converter topology; and finally an AC/DC capable on-board charger for compatibility with existing charging infrastructure.

The project has nine project partners and two associate partners, including the Austrian Institute of Technology, which is leading the project, Cambridge GaN Devices, the Manifattura Automobili Torino, Lead Tech, and Eaton. The consortium also includes

the research institutions IFP Energies Nouvelles, Aarhus University, Ingolstadt University, Politecnico di Torino alongside associate partners FPT Motorenforschung and ETH Zurich.

Compound semis essential to UK, says report

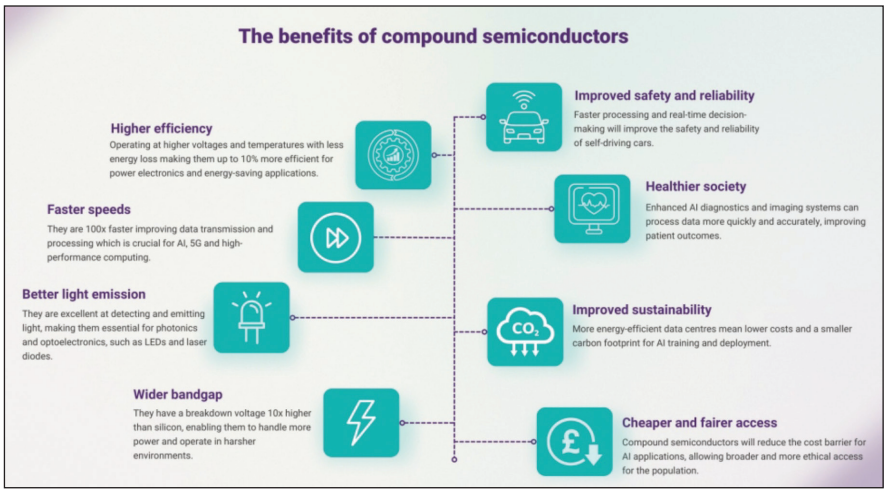
Report by CSA Catapult says compound semis are central to AI plan, for driving economic growth and offer significant benefits for society

REPORT BY CSA Catapult says compound semis are central to AI plan, for driving economic growth and offer significant benefits for society Compound semiconductors will be critical to helping the UK achieve its AI action plan, driving economic growth and significant benefits for society. This is according to a new report published by the UK's Compound Semiconductor Applications (CSA) Catapult.

With the global market for AI set to grow to over $1.5 trillion by 2030, the report outlines the significant upgrade in hardware capability needed to cope with the increased computational and energy demands of AI technology.

The report states that the UK is well positioned to lead the AI transformation through its recently published AI Opportunities Action Plan. But to realise this vision, it states that the UK must capitalise on its expertise in compound semiconductors.

Compound semiconductors offer greater energy efficiency, faster data processing, and better reliability. They are superior to traditional silicon semiconductors in areas such as power electronics, photonics and radio frequency (RF) communications – vital for infrastructure such as data centres that will underpin the AI revolution. As AI models grow and get more sophisticated, their power consumption also significantly increases. The data centres that power AI are already using 1 percent of global electricity — a figure that is expected to grow to 8 percent by 2030.



The need for a shift to faster and more efficient hardware is therefore clear. Compound semiconductor-based photonic devices will also dramatically increase the speed at which computers process and transmit data, significantly reducing latency in AI applications. Meanwhile, RF technologies leveraging compound semiconductors will improve the speed and efficiency of data transfer in AI applications, edge computing, and the Internet of Things (IoT), which is expected to connect over 32 billion devices worldwide by 2030.

Nick Singh, chief technology officer at CSA Catapult said: "Silicon-based technologies are reaching their limits in terms of energy efficiency and performance.

Compound semiconductors enable faster data processing, greater energy efficiency, and enhanced performance, making them essential for next-generation AI applications.

SiC slowdown is only short term, says Yole

BEV slowdown is delaying short-term expansion, but the $10 billion future remains on track

DESPITE a temporary slowdown in BEV shipments, the SiC market remains on a long-term growth trajectory, according to the Yole Group.

Its analysts forecast the power SiC market will exceed $10 billion by 2029, driven by a strong rebound in 2026 with CAGR between 2024 and 2023 close to 20 percent.

“SiC adoption has accelerated since 2018–2019, primarily led by Tesla, the early disruptor in automotive electrification. In 2024, Tesla continued to dominate the SiC-based BEV segment with nearly two million units shipped, although that figure is down 5 percent from 2023, “ said Poshun Chiu, senior technology and market analyst at Yole Group.

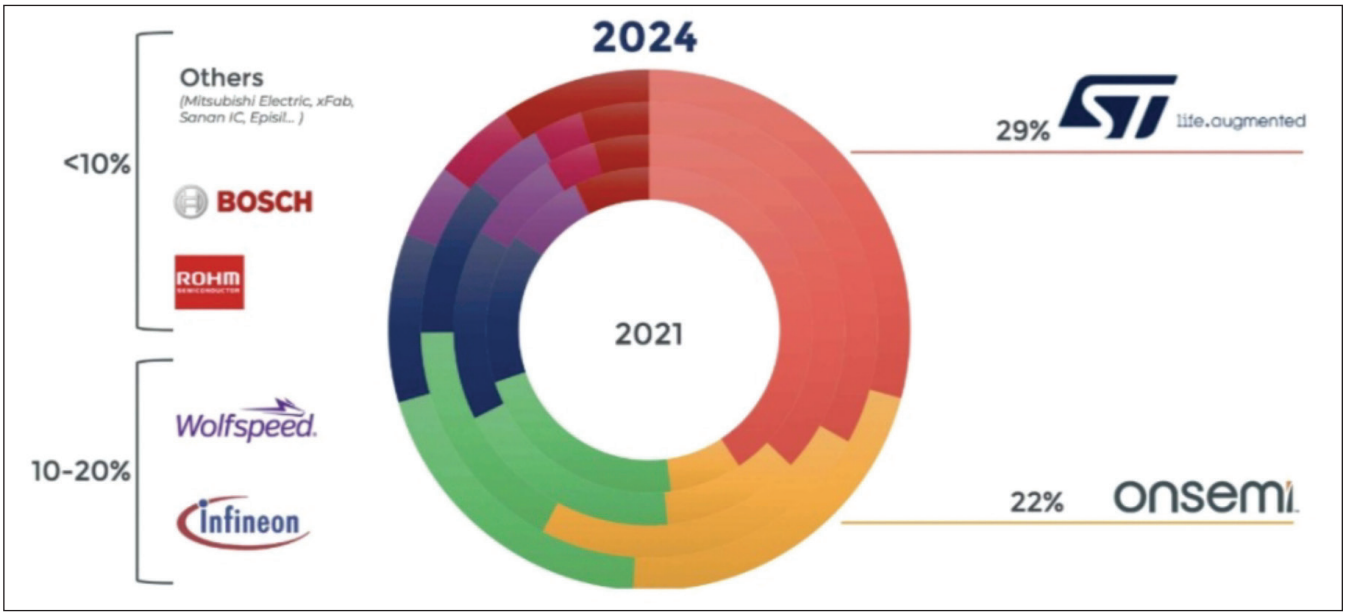
Meanwhile, other OEMs, especially from China, are gaining ground. BYD, Nio, Geely, and Xiaomi are expanding their SiC-based BEV portfolios. Despite these positive trends, the overall market deceleration has impacted the revenue growth of key SiC suppliers such as STMicroelectronics and onsemi, though Infineon Technologies continues to grow, supported by its diversified applications across both automotive and industrial sectors.

While many players are expanding capacity, especially in transitioning from 6-inch to 8-inch wafers, current end-system demand may not yet justify this scale. Ezgi Dogmus, activity manager, Compound Semiconductors at Yole Group says: “Industry feedback suggests that total announced capacity could outpace short-term SiC device consumption. Suppliers are now adjusting production volumes on a per-order basis and slowing down some expansion plans to match market realities for 2024 and 2025.”

Key factors to monitor include wafer quality, yield, and supply chain efficiency. As competition intensifies, vertical integration becomes more critical. Leading companies, including STMicroelectronics, onsemi, Wolfspeed, and Infineon Technologies, are doubling down on internal wafer manufacturing and module production to meet their billion-dollar revenue targets. Yole Group identifies STMicroelectronics’ approach as one of the most ambitious moves among non-Chinese semiconductor players. Faced with rising competition and China’s push for local sourcing, the leading semiconductor company has adopted a unique “become Chinese in China” strategy.

Yole Group’s analysts spotlight three key partnerships underpinning this approach: a $3.2 billion joint venture with Sanan Optoelectronics for SiC devices, a manufacturing collaboration with Hua Hong Semiconductor for 40nm automotive MCUs, and a strategic investment in GaN leader Innoscience. These moves are designed to localise production, support Chinese OEMs, and secure long-term market share in China’s EV and industrial sectors.

This detailed analysis, based on the Power SiC/GaN Compound Semiconductor Market Monitor, Q1 2025, suggests that these bold moves could significantly boost STMicroelectronics’ growth from 2026 while also shaping the competitive landscape in SiC markets. Yole says although the short-term outlook has cooled, analysts remain confident in SiC’s long-term momentum, especially as BEV demand recovers and industrial applications continue to expand.



£250m to turbocharge Welsh compound semi cluster

Vishay's investment in UK's largest semiconductor fab will be vital to EV production and support hundreds of highly-skilled jobs

WALES is set to benefit from a £250million investment from the semiconductor company Vishay Intertechnology, that will be vital to the production of electric vehicles, supporting the UK government's Plan for Change in delivering more skilled jobs, and turbocharging the economy.

The Chancellor Rachel Reeves will welcome Vishay Intertechnology's intention to invest on a visit to the Newport plant - the UK's largest semiconductor facility - as part of plans to develop large-scale compound semiconductor manufacturing in the country.

The investment will boost production at the factory where it will make advanced SiC semiconductors. Vishay's investment is expected to directly support over 500 high value, high skilled jobs in the region and indirectly support hundreds more in the wider supply chain.

It comes after the Chancellor Rachel Reeves' Spring Statement where she vowed to bring about "new era of security and national renewal" to kickstart economic growth, protect working people and keep Britain safe.

Supported by the government's Automotive Transformation Fund (ATF), the investment will help secure domestic supplies of semiconductors critical to the UK automotive industry, and other key industries including renewable energy and defence. It also strengthens the UK's position in a competitive, global semiconductor landscape, supporting long-term growth for our economy.

Through the ATF, delivered in partnership with the Advanced Propulsion Centre (APC), the government continues to unlock private investment in UK automotive design,

development, and manufacturing as the sector transitions to zero emission technology. To date, the ATF and APC funding programmes have leveraged over £6bn of investment from the private sector.

The Autumn Budget confirmed over £2 billion for capital and R&D funding over five years for zero emission vehicle manufacturing and their supply chains. Mike Hawes, SMMT (Society of Motor Manufacturers and Traders) CEO, said: "This significant investment in compound semiconductors is a huge contribution to the innovation and advanced technology necessary to drive the future of UK Automotive.

British-made next-generation semiconductors will create jobs, support supply chains and enhance the UK's strategic capabilities. "

Secretary of State for Wales Jo Stevens said: "This massive investment by Vishay and the UK Government is a huge boost for Wales's world-leading semiconductor industry. Earlier this month I was at Vishay to see the work they do on advanced manufacturing, renewable energy and defence industries – all key sectors in the Welsh economy." Wyn Meredith, chair of CSconnected, the Welsh Semiconductor Cluster said: "Since the launching the Welsh Semiconductor Cluster in 2015, our partners have invested heavily in creating a world-leading research and innovation ecosystem, with a highly skilled talent pipeline to address a semiconductor market opportunity which is set to surpass $1Trillion per annum by 2030. Global semiconductor players like KLA, Microchip, IQE, Vishay, and recently announced Cadence, have recognised the value of our proposition and have committed in excess of £600m investment to fuel the continued growth of semiconductor manufacturing in South Wales."

Roy Shoshani, COO Semiconductors and CTO for Vishay, said: "This is an exciting moment, and the start of our plans for growth in the UK. We can see through the development of the Industrial Strategy and the skilled workforce in Newport that there is a real opportunity to play to the UK's strength in advanced semiconductors, delivering greater economic security and supporting Net Zero."

UK establishes semiconductor design centre

Cardiff-based centre to become a leading provider of semiconductor design services, creating over 100 jobs

A NEW joint venture between Welsh Government, Compound Semiconductor Applications (CSA) Catapult, and Cadence Design Systems, Inc. will address long-term skills needs within the semiconductor design sector and support the industry's growth by providing critical design services to SMEs and scale-up companies across the UK.

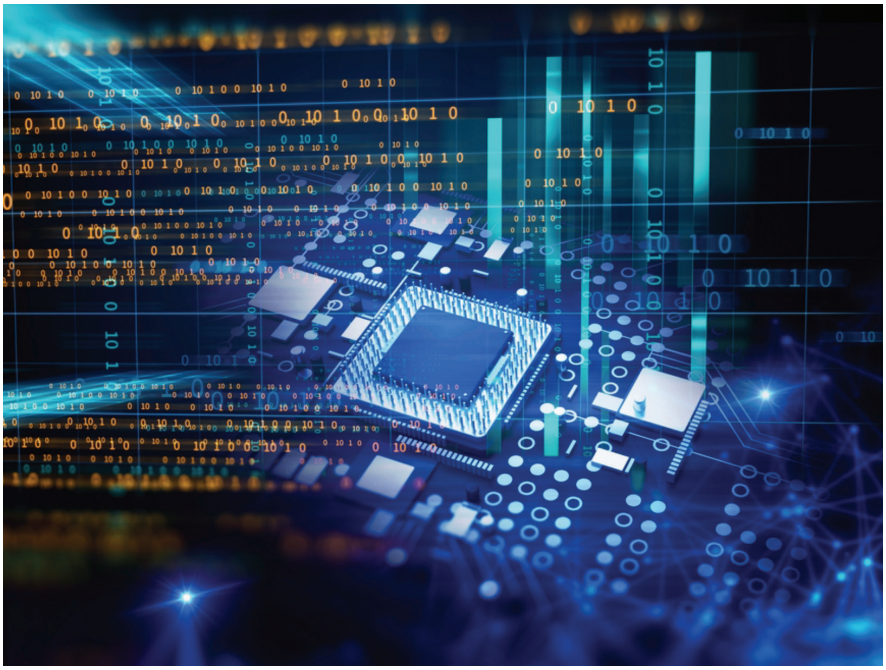
The dedicated semiconductor design centre, which has received £2.5m in Welsh Government investment, funding from Cadence, and support from CSA Catapult, will create over 100 new jobs for graduate students in the next five years, contribute an estimated £34m to the UK economy and help deliver the UK government's industrial strategy.

Martin McHugh, CEO at CSA Catapult said: "Through the joint venture, we can address the semiconductor skills gap and strengthen the UK's leadership position in chip design.

It builds on the success of the compound semiconductor cluster in Wales and will create new opportunities for the entire UK semiconductor ecosystem. There will be new career paths for graduates of electrical engineering, computer science, and physics. With the support of Cadence and Welsh Government, the new centre will create international partnerships and further investment to the UK."

The new company aims to become a leading provider of semiconductor design services, supporting key industries such as automotive, aerospace, space, telecoms, defence, and AI.

The new venture will leverage Cadence's expertise and AI-driven IC design solutions, CSA Catapult's advanced facilities and testing capabilities, and Welsh Government's financial support to create a sustainable, high-growth business. This partnership will drive innovation, create skilled jobs, and enhance the UK's semiconductor ecosystem while addressing critical industry needs.



This strategic joint venture will strengthen the existing design community, working with universities, start-ups, and small businesses on new semiconductor projects. It will build new international partnerships and further investment, helping to deliver opportunities for semiconductor companies across the UK to collaborate with European and US chip initiatives.

Over the next five years, the semiconductor design centre will provide training and a career path for graduates, apprentices, and career changers to enter the semiconductor industry.

From its base in Centre 7 in Cardiff Gate, there will be opportunities for graduates in electronic and electrical engineering, computer science, and physics, helping to bridge the gap between university education and real-world job opportunities.

Speaking about the Cadence investment, Rebecca Evans, Cabinet Secretary for Economy, Energy and Planning, said: "Cadence's exciting partnership with Welsh Government and CSA Catapult not only reinforces the international confidence in Wales' world-class semiconductor sector but also demonstrates our commitment to working with businesses to create the right conditions and opportunity for growth, investment and job creation here in Wales."

"Cadence is committed to promoting economic development in Wales," said Rebecca Dobson, corporate vice president for EMEA at Cadence. "We're investing to support the high-tech industry in Wales by creating jobs and committing to recruiting and developing top talent, which is crucial for continued semiconductor industry growth and innovation. It's a win-win for Cadence, the industry, and Wales."

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Understanding China's pivotal role in automotive semiconductor innovation

Yole Group launches its first automotive White Paper, Vol. 1 - Part of the 2025 White Paper Collection.

THE AUTOMOTIVE industry is undergoing a profound transformation. At the heart of it all? Semiconductors.

With this first automotive White Paper, Yole Group examines the current state of the industry, highlighting key innovations, challenges, and breakthroughs while exploring future developments. Leveraging their deep expertise in market trends and technology, analysts provide insights into the evolving automotive landscape and the next generation of vehicles.

The automotive industry is experiencing its most transformative era since its inception. From electric cars to autonomous shuttles, high-speed trains to aircraft, mobility is being redefined — and semiconductors are at its core.

Pierrick BoulayPrincipal Analyst, Automotive Semiconductors at Yole Group, comments: "At Yole Group, we closely monitor these shifts, focusing on how semiconductor technologies enable new mobility functions. ADAS and electrification are becoming standard, laying the groundwork for fully autonomous & electric vehicles."

Yu YangPrincipal Analyst, Automotive Semiconductors at Yole Group, adds: "In the ongoing revolution, China plays a pivotal role. As a hub of innovation and manufacturing, the Chinese ecosystem is fueling both technological breakthroughs and market acceleration on a global scale, while also fostering the rise of its own automotive giants at all stages of the supply chain."

In the face of this abrupt change, how are European and North American OEMs positioning themselves to remain competitive? What will the ripple effects

be on the global semiconductor supply chain? How will standards be (re-)defined? And as vehicles become ever more connected and autonomous, how can the industry ensure data security and privacy across such a complex, international landscape?

A key strategic question is related to semiconductor device makers: the Chinese car OEMs have a supply strategy to increase, car model by car model, Chinese sourcing of semiconductor devices. So, they are replacing their existing global suppliers, including Infineon Technologies, NXP, STMicroelectronics, TI, Renesas, and onsemi... to name just the largest ones, with Chinese companies.

This is a dramatic shift for the non-Chinese IDMs. Some, like STMicroelectronics, are building a dedicated strategy to become Chinese in China. However, a similar strategy is clearly needed for each of these companies.

Yole Group is pleased to introduce its first Automotive White Paper, marking the launch of a Yole Group 2025 Collection, with more content to follow, including a second automotive volume, dedicated to the automotive semiconductor companies and their strategy.

TU Graz and Silicon Austria Labs launch power lab

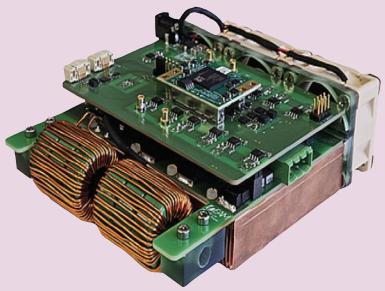
GRAZ UNIVERSITY of Technology (TU Graz) and Silicon Austria Labs (SAL) have launched a joint power electronics research laboratory 'PERL' dedicated to advancing fundamental research in high frequency switched power converters.

The research work aims to use the superior properties of wide bandgap (WBG) semiconductors, SIC and GaN, by proposing and studying new power conversion topologies (with a strong focus on soft switching ones), optimal usage and design of passive components, novel gate driving solutions, and smart packaging and integration techniques.

The main objective is to push the operating frequency of the converters and to explore and understand the associated limitations, also considering the electromagnetic interference in the analysis.

Targeted applications span various industrial fields where low size and weight, as well as very high efficiency are beneficial, including automotive, data centers, telecom, portable devices, and avionics/ space.

Researchers from both TU Graz and SAL will work together, including four dedicated PhD students. The joint laboratory is initially planned to run for three years.



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Highlights
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- Design platform REDEXPERT
- Application notes and reference designs
- Reference guide DC/DC converter handbook
- Ready-to-use simulation models

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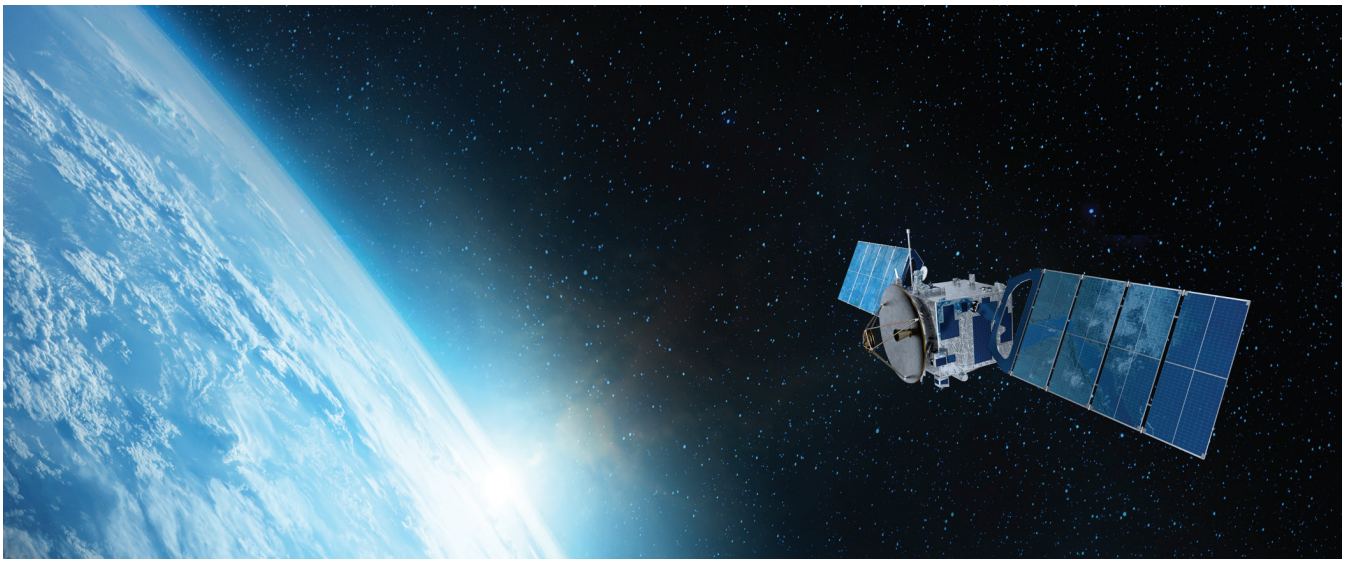
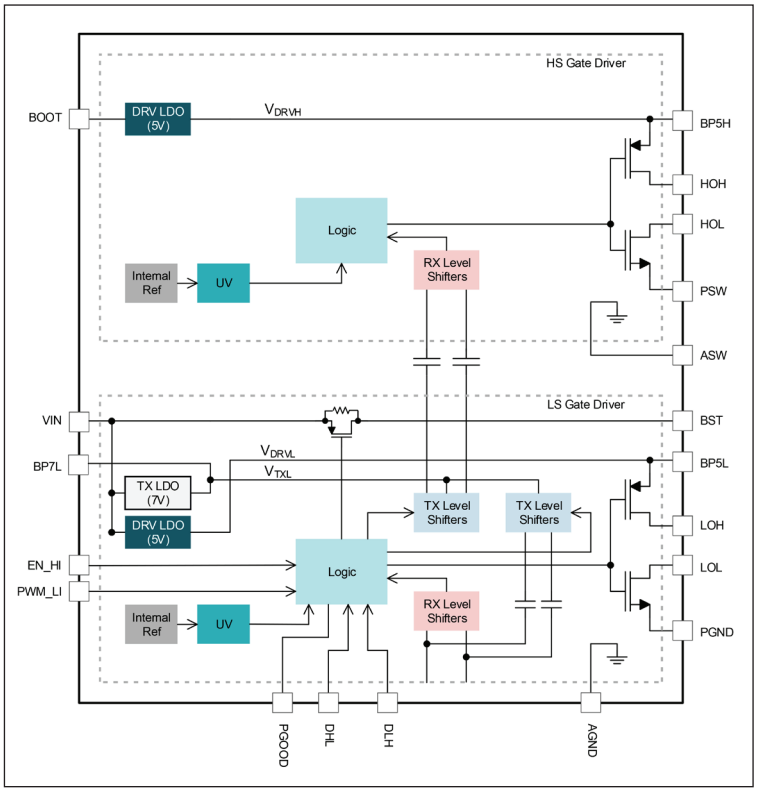


Using gate drivers to improve GaN performance in space-grade power converters

Using gallium nitride (GaN) field-effect transistors (FETs) in a power supply can help boost efficiency and enable operation at higher switching frequencies, helping designers meet the strict power requirements in space-grade radiation-tolerant and radiation-hardened applications.

BY JOHN DOROSA, SYSTEMS ENGINEER, POWER DESIGN SERVICES, TEXAS INSTRUMENTS



SINCE every kilogram of weight impacts the ability and cost to launch a satellite, it's important to optimize its size, weight and power capabilities. Increased power conversion efficiency of GaN FETs reduces the amount of heat dissipation in a system, and higher switching frequencies allow for smaller magnetic components.

While the functionality as a switching element is common between silicon and GaN FETs, their gate drive characteristics differ enough to require specific driver components. The internal low-dropout regulators (LDOs), split-gate outputs and adjustable dead-time control in the Texas Instruments (TI) half-bridge GaN FET gate drivers like the TPS7H60003-SP and TPS7H6015-SEP enable power converters to extract more performance out of GaN FETs in a power supply. In this article, I'll describe the parameters for using the gate drivers in GaN-based applications and highlight design recommendations at the system, schematic and printed circuit board (PCB) level.

➤ Figure 1. The TPS7H60xx-SP and TPS7H60xxSEP contain two die connected by a pair of communication capacitors.

Half-bridge GaN FET gate driver

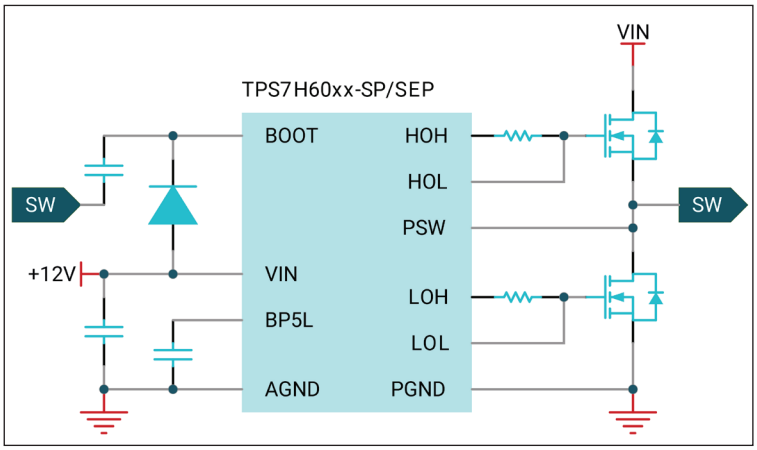
Devices in the TPS7H60xx-SP and TPS7H60xxSEP family have compelling total ionizing dose (TID) and single-event effect (SEE) performance, including validation of no cross-conduction events under single-event transient (SET) radiation. The half-bridge gate driver is constructed with two dies: a low-side gate driver and a high-side gate driver.

The low-side die contains blocks for logic, local biasing through an LDO, and a gate driver referenced to the PGND pins, while the high-side die has a local bias and gate driver referenced to the PSW pins (see Figure 1). The only connection between the two die are a pair of AC capacitors used to level-shift timing information from the low-side die to the high-side die. The 22V, 60V and 200V versions of the gate driver device correlate with the maximum stress that can be placed on the AC capacitors used for communication between the low- and high-side die [1].

Topology selection

Having two independent gate-driver die enables you to use the device in a variety of power-converter topologies. The first option is a half-bridge configuration, where the low- and high-side gate drivers drive a stacked pair of metal-oxide semiconductor field-effect transistors (see Figure 2). In this configuration, the PSW pins connect to the switch node of the FET pair.

To ensure safe operation, the bus voltage must be lower than the voltage rating of the device chosen. An external supply is needed to bias the low-side gate driver. A bootstrap diode can bias the high-side gate driver; see Section 8.3.3 [1]. Common use cases include a synchronous buck converter for non-isolated topologies and primary FETs in a full-bridge converter for isolated topologies (see Figure 3). Another option is to tie both the PSW and PGND pins to system ground and use the drivers as two low-side gate drivers (see Figure 4). In this case, the same external supply can bias the low- and high-side gate driver. You can use any voltage rating for driving dual low-side FETs with a shared ground



➤ Figure 2. Connecting the high-side gate driver to the switch node for a half-bridge configuration.

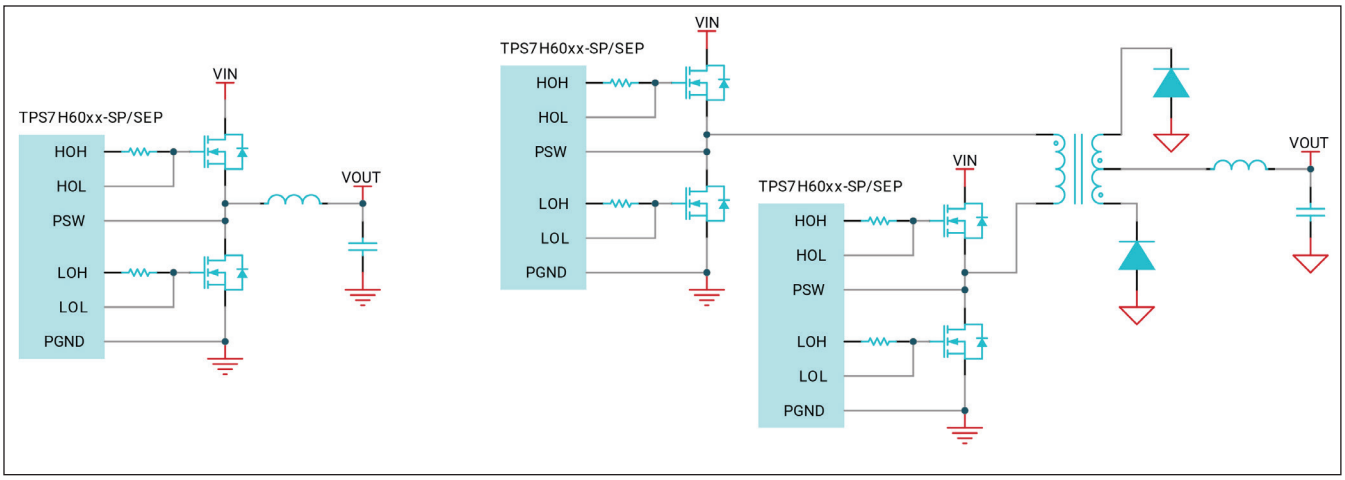
because there is no potential between the PSW and PGND pins.
It is possible to use this approach to drive two phases of an interleaved boost converter for non-isolated applications. For isolated designs, this method is popular for driving the primary FETs of a push-pull converter and can also drive the synchronous rectifiers in any forward-derived topology (see Figure 5 a and b).

The last implementation is to use the high-side gate driver as a pseudo-isolated gate driver that can handle as much as 200V isolation between the two die within the device. For these applications, bootstrapping is not possible; instead, biasing the high-side gate driver will require an isolated external supply (see Figure 6).

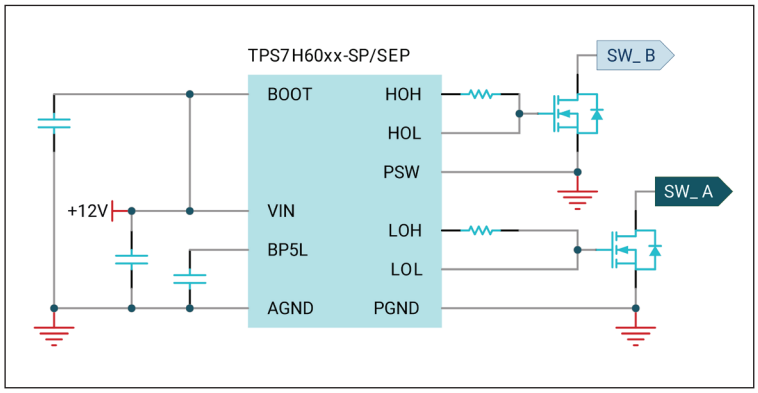
You can use a functionally isolated high-side driver on the primary side of a two-switch flyback topology. Another use case is to drive a synchronous rectifier in a single-switch isolated topology, such as a synchronous flyback converter (see Figure 7). In this configuration, the isolation voltage is limited to the voltage rating of the device; however, in many space applications that is enough to meet isolation requirements.

Internal LDOs

Each die of half-bridge driver uses an integrated LDO regulator to bias the pullup voltage for its gate



➤ Figure 3. The half-bridge driver in non-isolated (a) and isolated topologies (b).



➤ Figure 4. Using the half-bridge device as a dual low-side gate driver simplifies connections.

driver. Since the gate-to-source threshold voltages tend to be more sensitive for GaN (more than silicon) this feature ensures a clean 5V to drive the FETs for a given power stage.

I recommended using an external supply between 10V and 14V for the low-side die. The high-side die can handle a slightly wider 8V and 14V input. The recommended value will provide enough dropout voltage for the gate-driver stages. Additionally, the low-side die needs a slightly higher voltage because the logic portion runs off a separate LDO that creates a 7V bias.

Using LDOs will filter out noise from an external bias. The external bias comes from a flyback converter with a measured 8.72V peak-to-peak ripple voltage (see Figure 8). Regardless of the noise present, the LDO generates a bias with a 560mV peak-to-peak voltage, resulting in a notably cleaned up gate-drive signal to ensure proper driving of the GaN FET.

Adjustable dead-time control

In a half-bridge configuration, the time duration between one gate driver's falling edge and the other gate driver's rising edge has a major impact on total conversion efficiency. While operating in independent input mode, the controller determines this timing. In this use case, I recommended using interlock prevention while in independent input mode to prevent driving both FETs at the same time, which would result in a shoot-through event.

Another option is to use pulse-width modulation mode, where a single input signal controls the timing of both drive signals. Section 8.3.6 of the device data sheet [1] has instructions for tuning the dead time between the falling and rising edges.

Having too much dead time leads to increased power losses. For example, in a synchronous buck converter, the freewheeling current will conduct through the low-side FET before the gate-drive signal is applied. This issue is amplified with GaN FETs which do not have a body diode, leading to this portion of time being very lossy [2]. When optimizing a design, you should reduce the dead time to minimize losses.

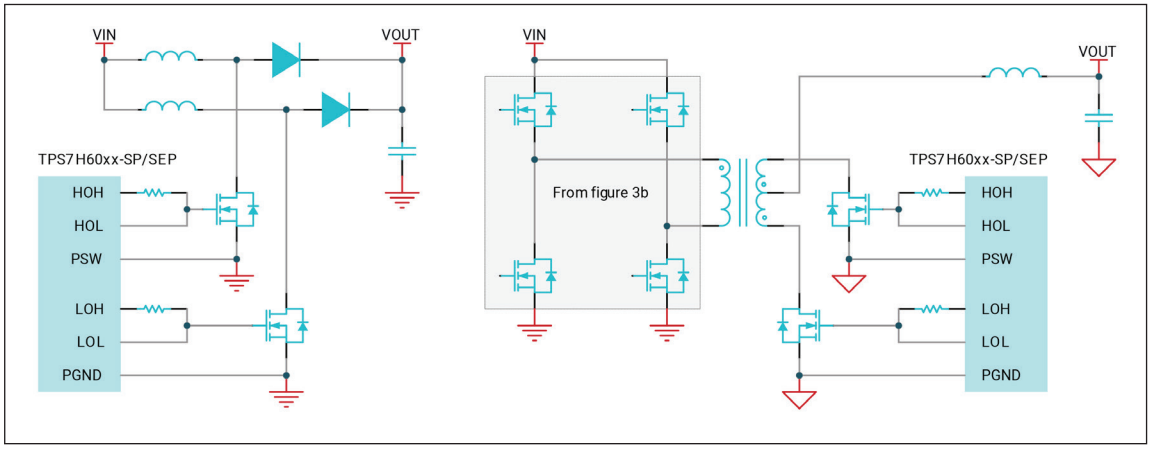
A dead time that is too short risks a shoot-through event. Even with the half-bridge gate driver preventing such effects, it is possible for one of the FETs to accidentally turn back on if the gate voltage is high enough (see Figure 9). This is especially important with GaN FETs, since their low gate-to-source voltage thresholds are susceptible to noise.

Extending the dead time will ensure that the gate signal from one gate driver is completely low before the other starts its rise time (see Figure 10). I recommended testing the actual timing by operating the controller in open loop before applying the input voltage.

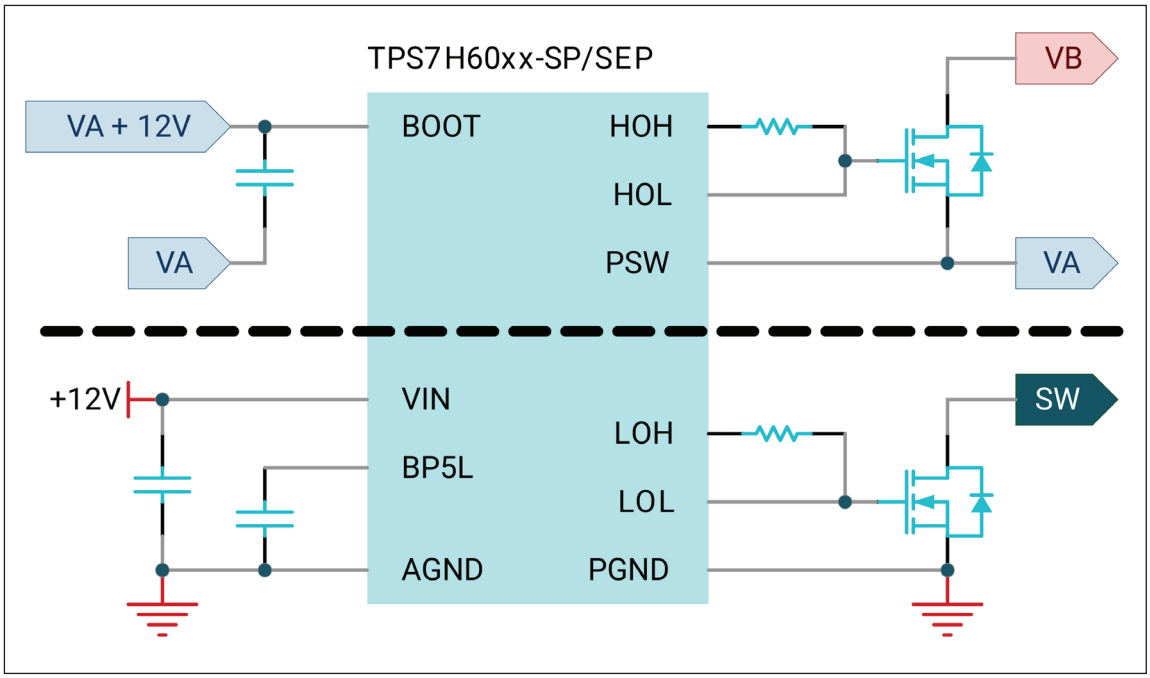
Split-gate outputs

Each die of the half-bridge driver uses split-gate outputs to drive the FET high or low. This enables individual tuning of the rise and fall times with the series gate resistors, providing a simpler solution compared to a conventional totem-pole output driver, which requires an additional diode to achieve the same functionality (see Figure 11) [3]. Faster transition times are necessary for power converters to operate at high switching frequencies. The transition period during rise and fall times is inefficient for power conversion; therefore, it's important to minimize the amount of time in this mode as much as possible.

The total power losses in a GaN FET comprise conduction, output capacitance, third-quadrant and switching losses. Conduction and output



➤ Figure 5. There are many uses for dual low-side gate drivers.



➤ Figure 6. The high-side gate driver in functionally isolated applications.

capacitance losses depend heavily on the parameters for the FET chosen, and as I mentioned earlier, adjusting the dead time can optimize third-quadrant losses. The performance of the gate driver will have the most impact on the switching-loss portion of a FET's total power losses [4]. See figure 12 for nominal voltage and current stress waveforms on a high-side FET in a buck Converter. Equation 1 calculates the switching losses [5]:

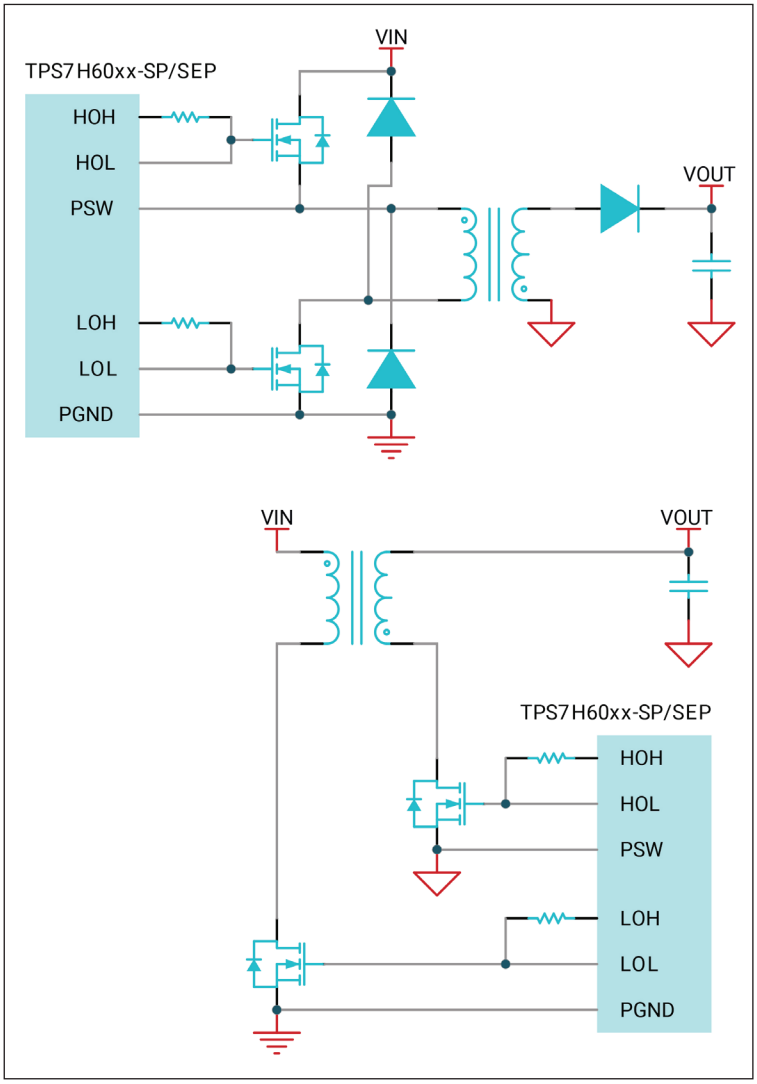
Pswitching = VDS × fswitch / 2 × (trise × IFET, min + tfall × IFET, max) (1) where trise is the rise time of the FET and tfall is the fall time of the FET.

Speeding up the transition time will minimize switching losses; however, faster transitions can cause increased ringing on the switch node at the transition times. This is especially the case with GaN FETs, which tend to have lower gate capacitance compared to silicon FETs. Having control over both the rise and fall times enables you to optimize efficiency while keeping ringing at an acceptable amount for a given design.

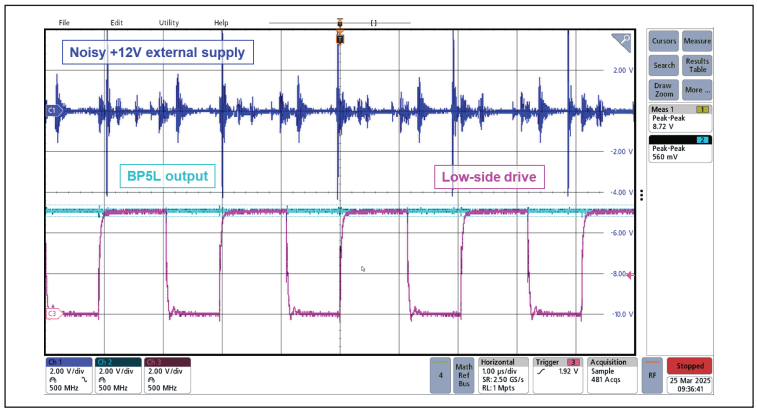
PCB design considerations

The performance of any power supply that uses GaN FETs depends heavily on the quality of its PCB design. This is because of the very fast switching times, which make even small parasitic inductances significant. Section 9.4 of the datasheet [1] includes a full list of PCB recommendations and layout examples, but in this article, I will show the direct impact of minimizing parasitic inductance.

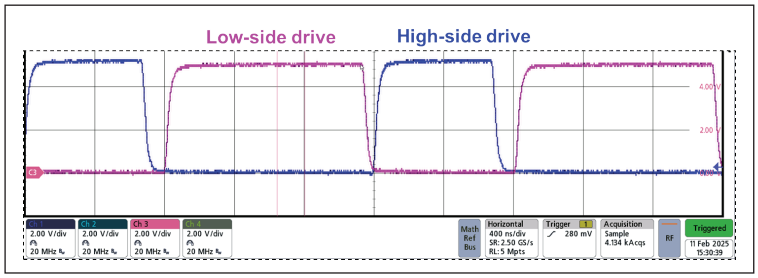
A short path from the gate-driver output to the gate of the FET, returning through the source, is the first loop to consider. Additional inductance in this path may result in slower rise and fall times, leading to increased switching losses. In extreme cases, parasitic inductance may weaken the drive signal



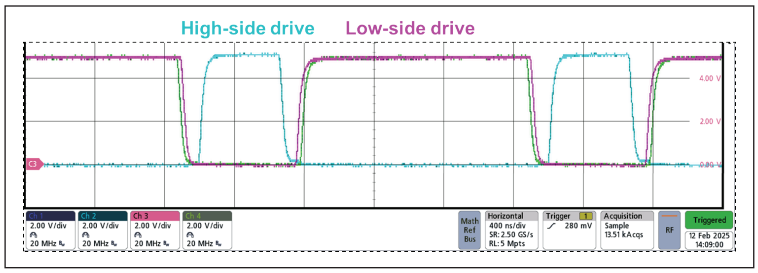
➤ Figure 7. Isolating the high-side gate driver can enable the use of higher-efficiency topologies.



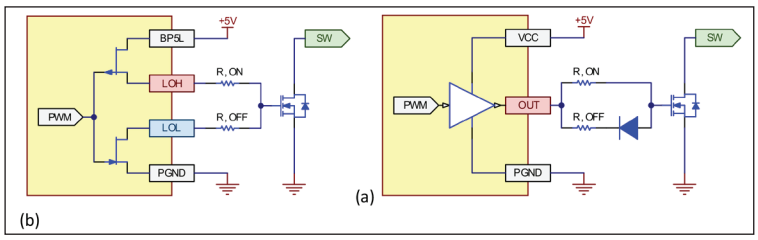
➤ Figure 8. An LDO cleaning up the ripple voltage from the external supply.



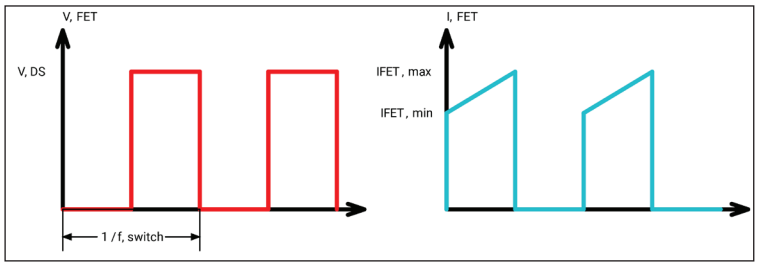
➤ Figure 9. Too short of a dead-time delay may lead to a shoot-through event.



➤ Figure 10: Extending the dead time ensures that the opposite gate drive has reached 0V.



➤ Figure 11. A split-gate output gate driver (a) does not require an additional diode compared to totem-pole (b) output.



➤ Figure 12. High-side voltage and current stresses in a synchronous buck converter.

to the point that it cannot completely switch the FETs on and off. An initial revision of a synchronous buck converter included specific intent to keep the gate loop small (see Figure 13). While the gate-drive signals were clean for the high- and low-side FETs, there is noticeable ring on the switch node (see Figure 14).

The second path to consider is the return path from the source of the low-side FET to the drain of the high-side FET through the input capacitor. In the initial PCB design, the input capacitors were placed far from the source of the low-side FET, which created enough inductance in the power stage to generate large amounts of switch-node ringing.

Using the same bill of materials, another PCB minimizes the return path of the power stage (see Figure 15). Note that in this revision, the smallest ceramic capacitors are toward the middle of the capacitor banks instead of being lined up from largest to smallest. This layout technique, along with using the second layer for a return path, minimizes parasitic inductance, greatly improving switch-node performance (see Figure 16).

Parasitic inductance is inevitable when creating a PCB design; however, the placement of components dictates where the inductance is in the circuit. Adding inductance to a gate-drive path runs the risk of not driving the FETs effectively, which could have implications on total conversion efficiency.

In this case, adding some gate inductance enabled a reduction in the power-path loop, greatly improving the switch-node ringing without having to change the selected components. With GaN-based power supplies, it's important to design the PCB carefully to weigh the impact of parasitic inductance.

FURTHER READING / REFERENCE

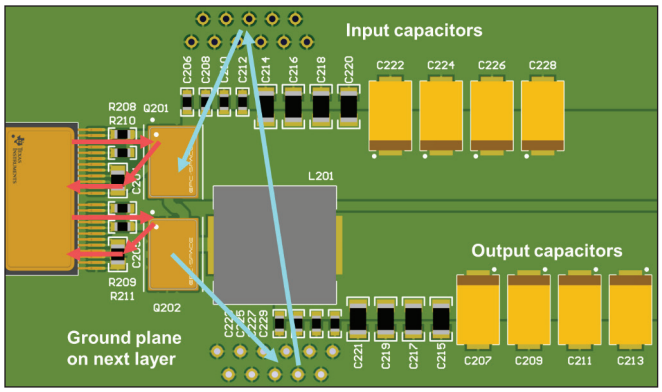
➤ [1] TPS7H60x3-SP Radiation-Hardness-Assured 1.3A, 2.5A, Half Bridge GaN FET Gate Drivers https://www.ti.com/lit/ds/symlink/tps7h6003-sp.pdf

➤ [2] Bingyao Sun "Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN" (2019) https://www.ti.com/lit/an/snoaa36/snoaa36.pdf

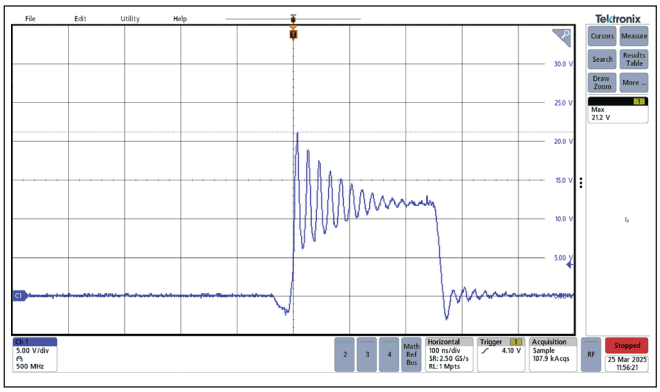
➤ [3] Laszlo Balogh "Fundamentals of MOSFET and IGBT Gate Driver Circuits" (2018) https://www.ti.com/lit/ml/slua618a/slua618a.pdf

➤ [4] George Lakkas "MOSFET power losses and how they affect power-supply efficiency" (2016) https://www.ti.com/lit/an/slyt664/slyt664.pdf

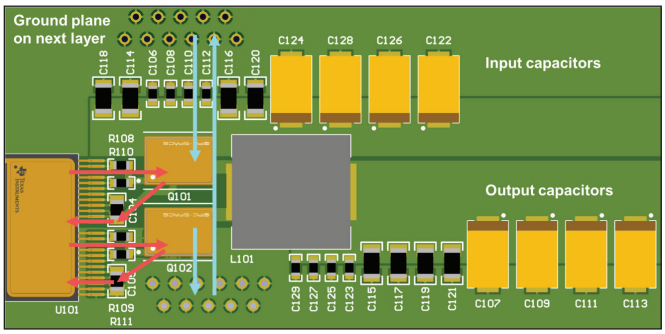
➤ [5] Markus Zehendner "Power Stage Designer User's Guide" https://www.ti.com/lit/ug/slvubb4b/slvubb4b.pdf



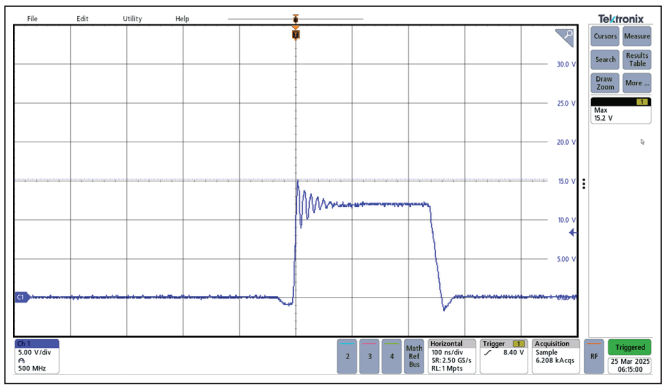
➤ Figure 13. A buck converter PCB design with a minimized gate path.



➤ Figure 14. Large switch-node ringing on a synchronous buck-converter design.



➤ Figure 15. Increasing the gate-drive path to enable better input-capacitor placement.



➤ Figure 16. Reduced ringing time and total voltage stress on the switch node.

Conclusion

Using GaN FETs for power converters provides many benefits in space applications. Switching at higher frequencies becomes possible while also maintaining high conversion efficiency.

These attributes reduce overall solution size, weight and cost which helps a satellite meet the strict requirements for space missions. Higher switching frequencies are possible when partnering GaN FETs with the right gate driver.

TI optimized the feature set in the TPS7H60xx-SP and TPS7H60xxSEP family of half-bridge gate drivers for GaN FETs to help you get the most out of your next power-converter design.

Innocent Innoscience?

The latest ruling from the US Patent Office draws jubilation from Innoscience, while EPC claims to have strengthened its key patent. But aside from the lawyers, will there ever be a winner in this long-running dispute?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THE GaN IP war raging between EPC and Innoscience is now entering a new phase, following rulings from the US Patent and Trademark Office (USPTO) this past month.

As is often the case in complex matters that involve IP, both sides are talking up the positives, while glossing over the negatives.

Innoscience, on its back foot since the imposition of a ban on importation into the US, is now incredibly upbeat. It is claiming it achieved an 'ultimate victory' in what it describes as EPC's meritless two-year-long patent war, and says that the USPTO ruling shows that EPC's allegations relating to enhancement-mode GaN transistors are 'completely unfounded'.

Unsurprisingly, US firm EPC has a different take on these matters. As well as emphasising a strengthening of its key patent, it is planning to appeal the USPTO's cancellation of its claims.

From four patents to only one

When EPC initiated its legal action against Innoscience back in May 2023, it claimed infringement of four patents, all associated with enhancement-mode GaN HEMT technology. The fabless chipmaker subsequently decided to drop two patents in the case directed to HEMTs with a self-aligned gate having 'ledges'. This left two patents being asserted against Innoscience: US Patent No. 8,350,294 (directed to a FET made with a 'compensated' GaN layer); and US Patent No. 8,404,508 (directed to a multi-step process for fabricating a self-aligned gate E-mode HEMT).

Relating to the '508 patent: EPC went to trial at the International Trade Commission (ITC) in July 2024, with the Administrative Law Judge (ALJ) deciding that the '508 patent was not infringed by Innoscience.

While Innoscience did not enjoy a full victory, having failed to convince the ALJ that the '508 patent was invalid, there is no doubt that it was pleased with the result, according to patent attorney David Radulescu, who is an expert in GaN IP. Radulescu, who is the head of the patent litigation boutique firm Radulescu LLP and has been litigating semiconductor patents in courts throughout the US for three decades, points out that EPC is now suffering from an undeniable loss on the '508 patent: "EPC has no right to an injunction (or any compensation) with its lawyers being unsuccessful in establishing use of its patented fabrication process."

However, EPC may draw some comfort from Innoscience's unsuccessful invalidity challenge before the patent office, where a final determination recently went in its favour. "For Innoscience, it was a complete loss at the USPTO, because all five claims were found to not be invalid," remarks Radulescu.

Relating to the '294 patent: In contrast to the ITC finding of no infringement on the '508 patent, EPC was successful in obtaining an infringement ruling on the '294 patent, which resulted in the ITC issuing an importation ban. The impact of the adverse ruling, however, was blunted when Innoscience claimed to have changed the design of its products to sidestep the ban. "Even so, the redesign had to be painful, particularly when lawyers are involved in device design decisions based on a patent landscape that is so fraught with traps," says Radulescu.

The 'compensation' conundrum

The on-going dispute is now focused on the '294 patent, related to the use of a 'compensated' GaN layer in a FET. Innoscience has widely reported that its devices use *p*-type GaN, but it is not disclosing whether transistor production includes an extra step to expel hydrogen, an approach widely used in the manufacture of GaN LEDs. During the

intentional doping of any semiconductor material with impurities, there will always be some degree of compensation, because no semiconductor is 'perfectly' doped with one type of impurity without other defects/impurities in the crystal lattice. With GaN grown by MOCVD, a number of factors are at play following the addition of magnesium, the common *p*-type dopant. One is that magnesium may be complexed with hydrogen, leading to compensation, because this impurity fails to create a hole.

A second factor is that lattice defects and vacancies, of which there are many in GaN grown by MOCVD on lattice-mismatched substrates, could lead to compensation. Lastly, unintentional impurities, such as carbon and oxygen, could also lead to compensation. Due to all these possibilities, characterising magenesium-doped GaN as 'compensated' or 'not compensated' is complicated to apply when that concept is written into a patent claim, says Radulescu. "It's not so simple as focusing on if hydrogen is present while ignoring other impurities or defects."

This complication hampered the efforts of EPC's lawyers, who needed to demonstrate that the patent is both infringed and not invalid.

"If you represent the patentee, the job of the lawyers is to walk the line between infringement and invalidity," explains Radulescu. "If you want to argue your claims are broad to show infringement, then you could be stepping over into invalidity territory and you could have the patent invalidated."

Although Innoscience was successful in having the all asserted claims of the '294 patent recently invalidated, EPC was successful in having two new 'substitute' claims added to its patent that escaped Innoscience's invalidity challenge.

Both claims are directed to GaN-based enhancement-mode transistors with more specificity to distinguish from the prior art. In particular, these new claims require that 'no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate voltage' and refer to a 'semi-insulating III-N layer', which includes a 'compensated GaN layer containing acceptor-type dopant atoms passivated with hydrogen'. These claims continue to not only refer to the hotly contested phrase 'compensated', but add a further complication by referring to a 'semi-insulating' layer (without any quantification of how insulating/conducting). "With all this added language, the claim scope is rich with opportunity to allow a lawyer with GaN experience to argue on either side of the dispute," Radulescu believes.

What happens next?

How both parties proceed from here will depend on a number of factors, some unknown. For EPC, if it wants to continue its battle with Innoscience, it will have to focus on appeals, attempting to overturn unfavourable decisions – which is always an uphill battle. In addition, it could file a new infringement action using other patents or the '294 patent with the new claims that have been litigation-hardened.

Meanwhile, Innoscience may decide to direct its efforts at removing the import ban, given that the infringed '294 patent claims were recently ruled as invalid. So far, there has been silence on this matter, but it's possible private negotiations are underway.

What the future holds is anyone's guess. Even those with tremendous expertise in these matters, such as Radulescu, can only speculate – and they will only do so after reeling off a string of caveats. Radulescu surmises that among a number of possible scenarios, one that would not surprise him is a sudden truce in this battle between EPC and Innoscience, with cross-licencing following. And if that were to happen, he would expect all the details to be confidential, with both companies just issuing a press release stating that they have cross-licensed their technology. Motivation for such a move would include avoiding paying more in legal fees, which may already total $15-20 million for each side.

➤ The European Large Logistic Lander enables a series of ESA missions, such as the delivery of supplies, rovers, and the return of sample packages from the Moon to Gateway.

Picture Credit: ESA Gallery.

Launching SiC into space

For future space missions, makers of electrical systems need better power devices, a requirement that's met by SiC

BY ANTXON ARRIZABALAGA FROM THE EUROPEAN SPACE AGENCY (ESA)

WE ARE GOING back to the moon, and this time we are going to stay there. Ensuring success is the Artemis programme, a collaboration between the European Space Agency (ESA), NASA, and other international and commercial partners. Together we will establish the first long-term human presence on this celestial body.

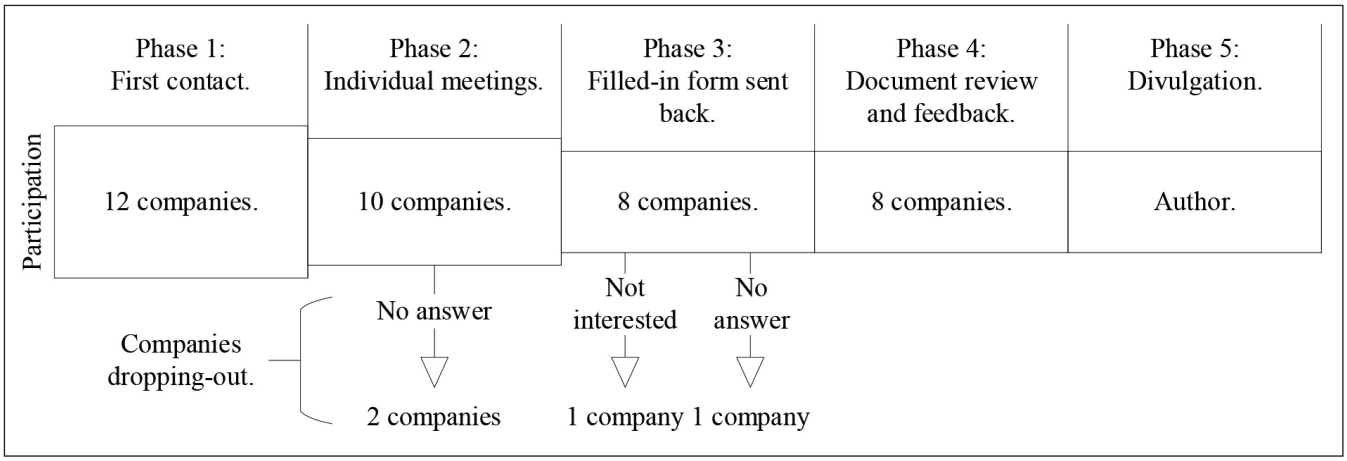
Critical to this success is a number of breathtaking technologies. They include: Gateway, the first space station orbiting the moon; lunar landers, such as Argonaut, able to ship cargo, infrastructure, heavy machinery, rovers, and power stations; and lunar habitable modules, already under development. While all these missions have differing objectives, they share a significant strand: the need for high-power.

Detailing the problem

Needing high power is a major issue, because space-qualified silicon power devices are unable to provide the technical requirements demanded by these high-power missions. Due to this inadequacy, the space power industry is searching for superior alternatives to replace them.

At the ESA, like many other organisations in the space power industry, we have noted an exceptional rise in interest and deployment of SiC power devices, and we have been investigating whether this could meet our needs. Unfortunately, there are no space-qualified SiC power devices on the market today, because producers of wide bandgap transistors and diodes are directing nearly all their attention at the huge automotive industry. Up until now, the general feeling has been that the space market for SiC is too small to generate a business case. But with the recent demand for high power, this is about to change.

To simplify the job of the SiC manufacturers and ensure fast adoption of these devices by the space power industry, we have been talking to the leading space power companies in Europe. During these discussions, we have focused on establishing



➤ Figure 1. The organised phases of the project, together with the number of companies participating in each one. Two companies did not answer the first contact email, while two other companies dropped out after the first meeting with them. One of the companies told us they mainly focus on low-power applications, and they are satisfied with the current available power device technology. The other company participated actively in the meeting, giving positive feedback, proposing ideas and even providing further information in the following months after the meeting. However, they failed to send back the filled-in form with the requested specific information. We sent a reminder, but they still did not send the form, so even if we included their feedback in the documentation, we considered them as dropping out. We were contacted by this company again after the technical talk in ICSCRM 2024, asking for follow-up information, which we gladly provided.

a clear idea of their needs, identifying potential applications, classifying the main technical drivers, and opening a new market for SiC manufacturers. Drawing on all that we have learned will enable the design of optimised devices for specific applications, making the technological transition seamless for the space industry and their adoption of these devices faster. In addition, this chain of events will create a clear business case for SiC manufacturers.

We organised our project in five phases. Efforts began by making an initial contact with the most important European companies. We then continued with individual meetings, the filling-in of specially designed forms, and gathering, classifying and documenting all the information. The final phase, divulgation, has involved reporting our findings to the SiC community using various platforms, including this publication. As part of this effort, we delivered an extended talk in a technical session at the most recent International Conference on Silicon Carbide and Related Materials, held in Raleigh, North Carolina, last autumn.

What does industry need?

After gathering and collating information from various companies, we had to classify it to ensure public access to this huge resource. We based our first classification according to industry needs.

One of our key findings is that the space industry needs to increase the power level of its systems, without losing performance. This can only be accomplished by increasing either the voltage of the system, its current, or both. Mainly due to limitations in the blocking-voltage capability of space-qualified devices, together with other technologies, increasing the current is the most common approach. Unfortunately, it's not possible to succeed on this front with state-of-the-art space power device technology without impacting performance.

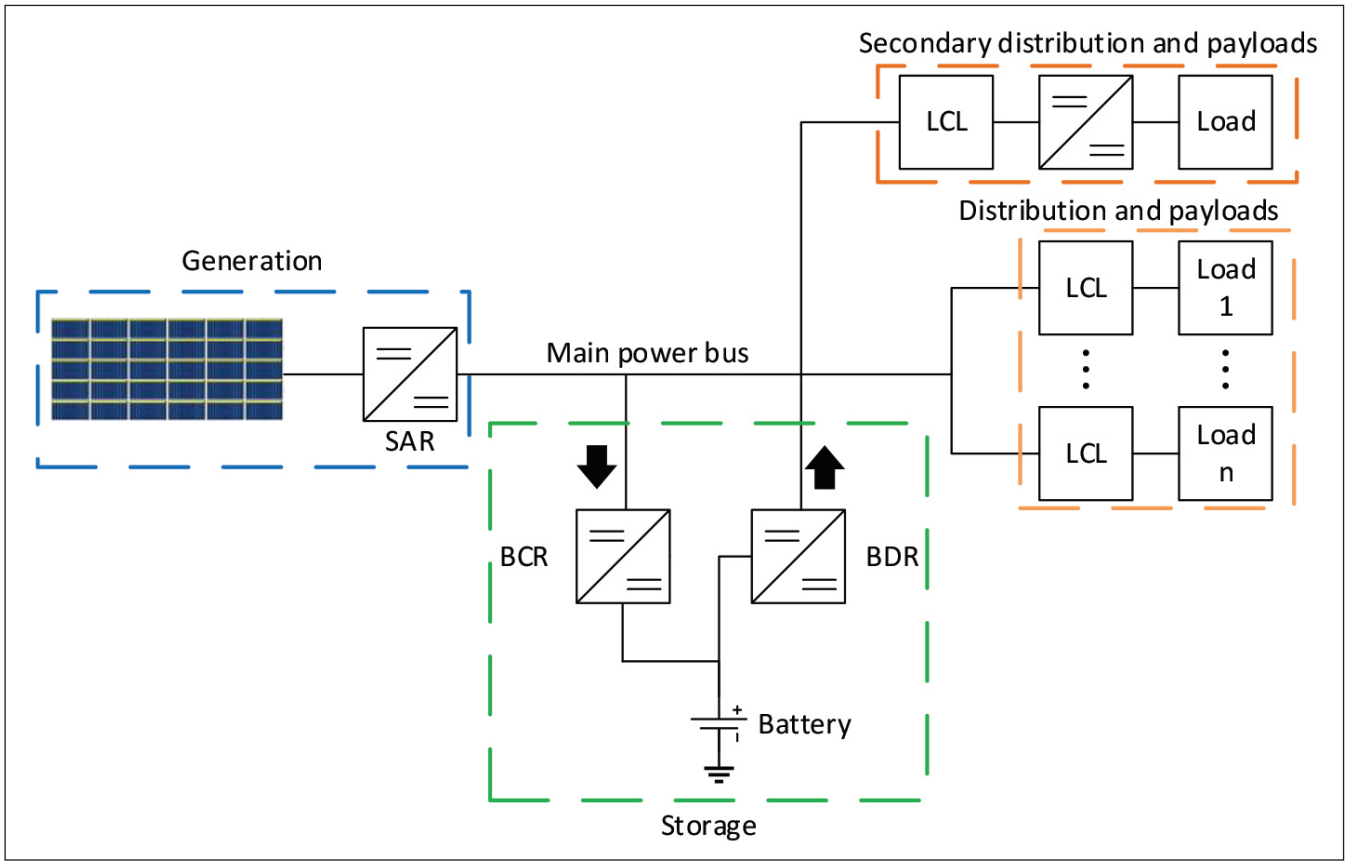
What the space industry needs is 'bigger' devices, with a higher blocking-voltage capability and a higher rated current, strengths that will allow the handling of more power in a single device while maintaining the performance figures provided by low-power systems.

Note that the space industry already has high-power solutions. How do they do it? It's through unwanted compromises, such as slow high-current devices or paralleling several lower-current ones. These approaches lead to complex layouts, high volume and lossy systems. Due to these weaknesses, the space industry is keen to improve the performance of already existing high-power systems. What this means is 'better' devices, operating at a high voltage with a lower conduction resistance, and at high current with improved switching characteristics.

Which applications?

Space systems are nothing more and nothing less than systems that provide autonomous energy generation, storage, distribution and consumption. They can be thought of as a microgrid, working in island mode, in either orbit or in space.

As is the case with any autonomous energetic system, the generated electrical power must be transformed, distributed, and transformed again, before it is either stored or consumed by the payloads – those are the end users of the satellites or space systems. DC is used for power generation from solar arrays, storage with batteries, and consumption by most payloads.



➤ Figure 2. The power architectures of satellites include several power conversion and distribution stages. Each regulator is a converter, usually based on several devices. Specific loads might require secondary distribution lines, with their own DC-DC converter to regulate the voltage to the required level by the payload. Each one of these electronic systems requires an increase in power for the future missions, providing the space industry with the opportunity to introduce SiC devices in their designs.

Generation with solar arrays, storage with batteries and consumption by most of the payloads is done in DC. To carry out the various tasks required in space, there is the need for power conversion, predominantly involving DC-DC converters based on the power devices we study. If the power of the payload increases, so does power generation, and in turn the power of the converters providing power conversion and distribution.

The space industry is considering SiC for the main DC-DC converters in satellites, the solar array regulator, the battery charge and discharge regulators, and the converters supplying the payloads. All of these DC-DC converters will have to be high-power and high-voltage. In addition, these DC-DC topologies will tend to need to include a rectifying stage. Regardless of whether this rectification is realised by diodes or synchronous active switches, these devices will need to match the high-voltage and high-power levels of the application. SiC will also play a vital part in the rectification.

Latching current limiters, traditionally based on silicon *p*-type MOSFETs for control simplicity, are used to manage the distribution and payload current limitation. However, the performance of these devices degrades drastically under high voltages, and they are very limited in current, so high voltages and high powers are not feasible with this technology. Alternatives that have warranted attention include *n*-type MOSFETs, even involving switched configurations based on GaN devices. However, as voltage and power requirements in the distribution increase, the appeal of SiC enhances. The space industry is interested in using SiC for high-voltage and high-power latching current limiters in the near future, to enable high-power distribution.

There is also a growing demand for high-power electric motor drives, mostly related to lunar landers and heavy machinery. These specific converters are not common in satellites, but they operate with similar concepts, having a dedicated battery. Due to voltage limits, these motor drives have to be very high-current systems. Even if they only operate for short periods of time, they have performance requirements that are very hard to meet with today's silicon devices.

It would be remiss of us to not mention very high-voltage applications. These are rare, involving the use of several hundred volts to supply power to scientific equipment or propulsion units. If very high-voltage distribution is needed, this requires

specific very high-voltage systems, such as current breakers. For all of these applications, specific main drivers should be optimised, improving determined technical requirements.

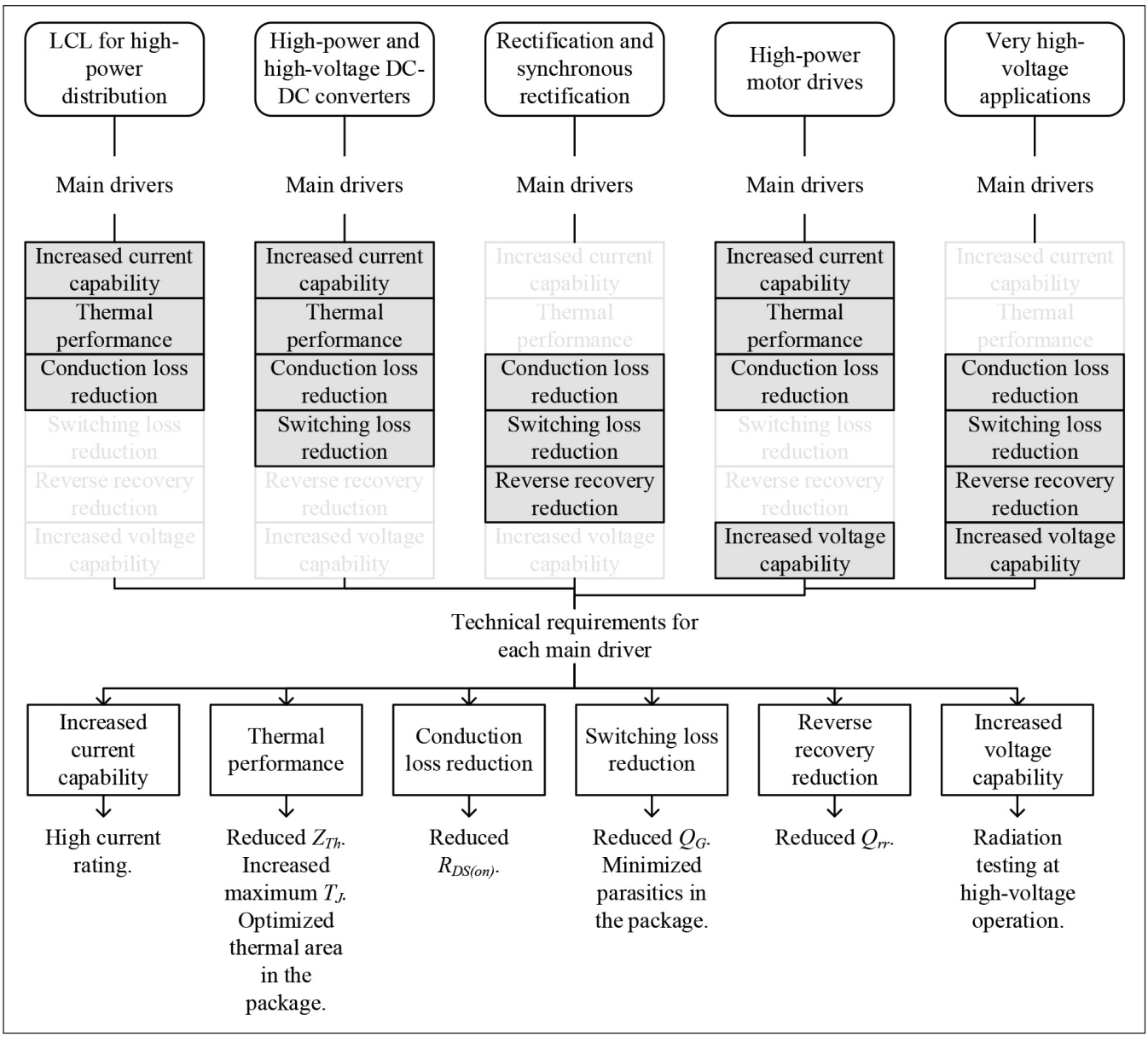
What about packaging?

Every package should be an enabler, and never a limiting factor on the operation of power devices. To ensure that this is the case, the package must be considered from the very beginning of the design process, to ensure that it provides all the functions required in a particular application.

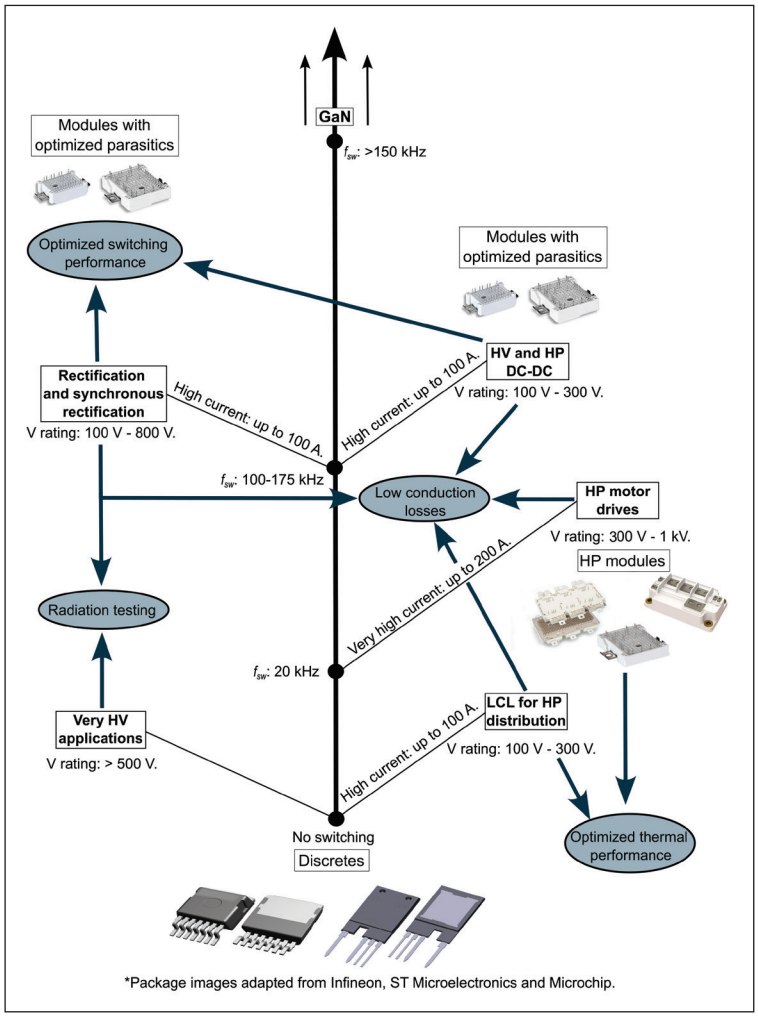
Once the target application of a new product is defined, its manufacturer must identify the main drivers and start working on the package, to ensure it is designed accordingly. This approach can be a game-changer for the adoption of a new product by industry.

It is in the low switching frequencies where we tend to find the highest power applications, such as high-power motor drives. Here, several tens of watts may be generated in the form of heat – and this needs to be removed from the die. The space industry is looking for a specific high-power package with an optimised thermal plate, directly connected to a cooling system, to ensure a low thermal impedance path.

Meanwhile, in applications requiring a high switching frequency, the devices that are deployed have the lowest gate charge and thus the fastest switching dynamics. As this leads to rapid changes in current and voltage in the converter, the package cannot



➤ Figure 3. The most mentioned applications among all the responses and feedback to the ESA from industry. During this information-gathering exercise the ESA ensured that industry made it clear what were the main drivers they wanted to be optimised in each application. The ESA has also detailed the technical requirements that the new devices need to fulfil to make a positive impact in each main driver.



➤ Figure 4. Packaging should be an enabler in a power device. As each application has its own main drivers, the devices used in them should also adapt to provide the required performance figures, together with the packaging. Moving from discrete components, where the cooling of die is done individually, industry sees the opportunity to introduce popular power modules, integrating more than one device. For very high-power applications, cooling of the die is optimised through a thermal plate, which conducts heat directly to the cooling system. For high-frequency applications, where parasitic components gain importance, the burden of creating good layouts is taken off the power engineers if the power modules already optimise the connections between the switches.

have long bonding wires and connections, because that would create current loops that insert several nano-Henries into the switching loops. In this case the package must be designed to ensure the best layout and trim inductance in the switching loop, as this will prevent undesired ringing and overshoots during fast switching.

Will industry adopt SiC?

The key to answering the question of whether the space industry will adopt SiC is to first understand how it operates. Understandably, this industry is heavily reliability driven. Due to this, there is openness to applying minor changes, if they offer demonstratable performance gains; but there is great reluctance to applying big changes to systems. The space industry loves to keep using its well-tested, reliable systems with a wide flight heritage.

Knowing this, it is clear that a new device has a much better chance of early adoption if it can be deployed in a conventional system. In the case of our power devices, this means operating SiC devices with space-qualified, well-known drivers and peripheral technology, such as the PCB, capacitors and connectors. Taking this approach reduces the development effort, time and cost for the space power electronics makers, while increasing the confidence level in their new product.

The approach to introducing SiC should be based on offering performance-enhancing innovations, as this addresses the two primary needs of the industry, which we have already discussed (to recap, they are increasing the power level of the system without diminishing its performance, and improving the performance of already existing high-power systems). It is critical that these performance enhancements impact the main drivers of the target application, without changing any peripheral technology.

However, while this approach is the best way to ensure a fast and seamless adoption of SiC technology by the space industry, it is detrimental

Radiation requirements

WHEN SiC power devices are flying in space, they will be exposed to hard radiation environments. This could lead to single-event (SE) effects that degrade the voltage-blocking capability of SiC devices in space. These effects are related to the impact of an energetic particle, leading the device to suffer from SE leakage (degradation), SE burnout (complete destruction), or SE gate rupture (if hit in the gate region). For now, the consensus among radiation experts is that the best way to prevent any SE-related issue is to derate the blocking voltage of the SiC devices. By using 1.2 kV SiC power devices, designers can derate SiC considerably while still being able to operate at over 100 V in space. However, performance comparisons need to use the operating voltage, rather than the terrestrial rating. This is the approach taken by the ESA, when using its testing platforms to compare the performance of space-qualified silicon and industrial SiC, even though it demands a case-by-case radiation analysis for every design. This need for thoroughness highlights why qualifying new SiC devices is a must for the space industry. Having qualified parts will allow aeronautical engineers to create designs without having to analyse the radiation performance case to case, ensuring repetitive behaviour and safe operation under defined radiation limits.

to the performance of these wide bandgap power devices. That's because using space-qualified drivers for SiC, rather than those that are specially optimised, impacts the performance of the power device, limiting the benefits that can be enjoyed. It is crucial to test the performance of this setup that's not been optimised for SiC, and compare it to the state-of-the-art system. The degree of success in these tests will define the adoption of SiC by the space industry.

What is ESA doing?

At the ESA, we are advancing the technology readiness level of SiC devices in space applications, and testing their performance in space operation conditions. We have developed two testing platforms for these tasks: one is designed for discrete components, and the other is intended to test high-power half-bridge SiC modules.
Both these platforms have the same objective, which is to show the space industry that it is possible to obtain performance gains with SiC without having to make major changes to the system. By only using space-qualified, well-known drivers and peripheral technology in our two platforms, we are following the approach that the space industry wants for early technology adoption.

In the discrete component platform, the power device is replaceable. It is possible to solder both space-qualified silicon and industrial SiC in the same system. With this platform, engineers can compare conduction and switching performance under the same operating conditions for both technologies. With the high-power platform, we are able to replicate the high current operation condition of the high-power motor drives. Successful testing could lead to one high-power half-bridge SiC module replacing up to eight space-qualified silicon MOSFETs, a move that can introduce substantial gains in the system. Again, all the peripheral technology is space-qualified for a fair comparison, and to ensure a seamless adoption by industry.

Failure modes

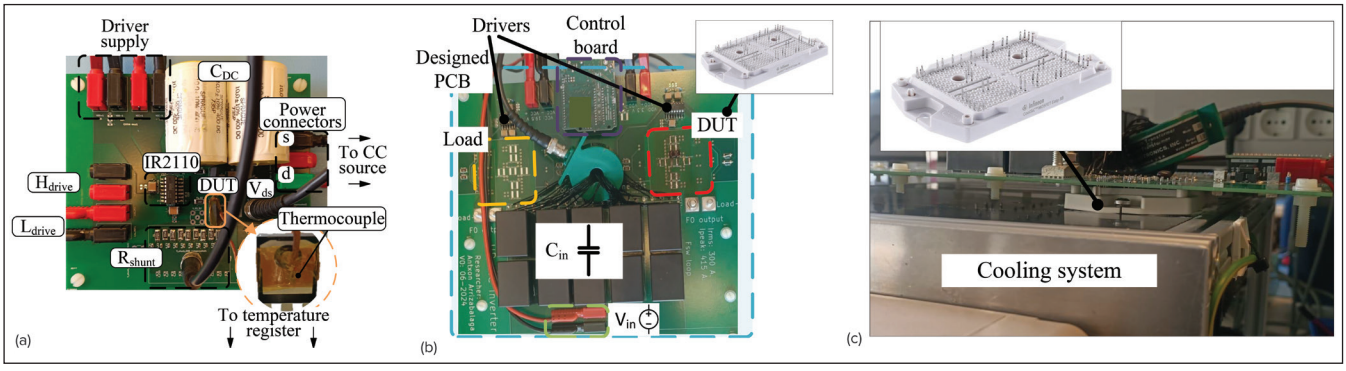
SPACE is a reliability driven industry. Every electronic design and unit accepted by ESA should be free from single-point failure. Hot and cold redundancies are common techniques to avoid single-failure modes in electronics designs, both at the component and the unit level. Every company is obliged to perform failure modes, effects, and criticality analysis before a unit is approved to fly.

This analysis is tiring and extremely time consuming. Extended knowledge on failure modes of SiC, its propagation principles and statistical data will provide invaluable information to the space power industry. In fact, this data is so important that it is hard to imagine any space power company adopting a new device for its major products without detailed communication and collaboration from the device manufacturer. This is a clear message from the space industry to SiC manufacturers: data and knowledge on failure modes and device degradation is as valuable as nominal operation data. Having a good understanding of these phenomenon, alongside maintaining a transparent and collaborative approach with the space industry, will massively help to increase the acceptance of the technology and ease its adoption.

As mentioned before, our activities extend to actively presenting our results, and sharing them in written and spoken forms. We are also offering assistance to interested companies, as well as guidance to the SiC manufacturers.

In addition, the ESA is funding space-qualified SiC development projects. They include EPOSiC, which is targeting the development, manufacture and full space qualification of a 300 V 50 A half-bridge SiC module that's manufactured completely in Europe. This ambitious project shows our agency's commitment to developing technology that will take us back to the moon and allow us to stay there.

In the meantime, we will focus on launching SiC into space. As W. Clement Stone said: "Aim for the moon. If you miss, you might hit a star."



➤ Figure 5. The ESA has developed two testing platforms. One is for discrete components and the other is for high-power modules. In both platforms, all peripheral technology is space-qualified, including the drivers. Proving performance gains with SiC power devices, while still using well known space-qualified peripheral technology, will increase the acceptance of the new technology, accelerating its adoption. This is being tested in space operation conditions in ESA labs, with satisfactory results, increasing knowledge and the device's technology readiness level.

Unleashing the potential of the JFET

The acquisition of Qorvo's SiC JFET portfolio provides onsemi with a great opportunity to accelerate the adoption of this class of transistor in circuit breakers, EV battery-disconnect units and AI infrastructure

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

BACK IN the days of the global credit crunch, many pioneers of SiC transistors were striving to be the first to market with their own particular flavour of this technology.

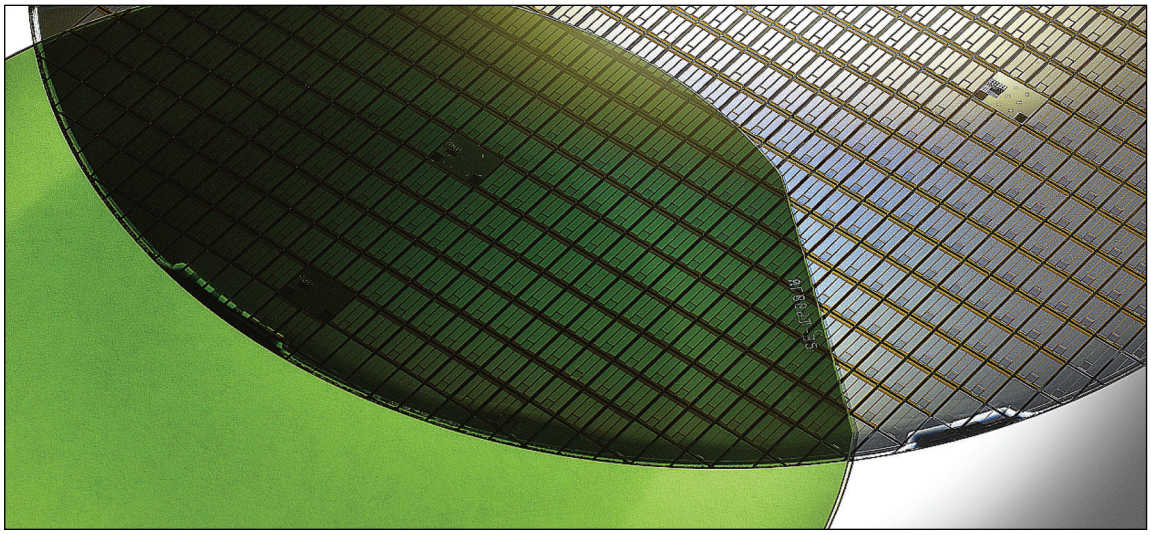
Initially grabbing the headlines were the likes of Semisouth and SiCED, trailblazers of the JFET, and BJT pioneer TranSiC. But their products struggled to make an impression, and when Cree and Rohm introduced the SiC MOSFET, this duo laid the foundations for a market that's now netting over a $1 billion per year and continuing to climb.

Based on this chain of events, it is easy to fall into the trap of concluding that the SiC MOSFET is superior to other forms of SiC transistor, which will never have a role to play. But one can also argue, for good reason, that some of the alternatives were ahead of their time, with circuit designers failing to appreciate their virtues and exploit them.

In a nut shell, that's the view of Sergio Fissore, who holds the position of Vice President and General Manager, Multi-market Power Division, at the electronic components manufacturer onsemi, which has just completed a $115 million acquisition of Qorvo's SiC JFET portfolio. Fissore believes that with this acquisition, onsemi will accelerate deployment of the JFET in EV battery-disconnect units, in AI infrastructure and in industrial solid-state circuit breakers, with total sales from this class of transistor netting several hundred million dollars per annum in the coming years.

Fissore argues that the SiC JFET, a device that's today only available from onsemi, failed to make an impact when initially introduced in the late noughties, due to concerns related to practicality and the long-term reliability of wide bandgap devices. If more designers had taken a closer look at that device back then, they would have been impressed by its performance, as well as that of the BJT, a transistor Fissore worked on during his time at Fairchild. He believes that a reluctance of customers to take a risk with new device technologies impeded sales of the SiC BJT, which were also held back by a lack of expertise in how to drive this device – rather than applying a particular voltage, it's the current that must be considered.

Tesla transformed the *status quo* with the adoption of SiC MOSFETs in its EVs, a move motivated by the opportunity to extend the driving range through an increase in power conversion efficiency, and a willingness to brush off the reliability risks and design complexities and resolve any issues that arose.



➤ An onsemi SiC wafer (left), and a final version (right), created by epitaxial growth, doping, device fabrication and etching.

"Many of our customer realised that if an automotive company takes that risk, those risks were worth taking, given the benefits you get from a wide bandgap," says Fissore.

He believes that today's designers are more adventurous, with a willingness to design gate drives and controllers for many different device requirements. Now, wide bandgap devices are seen as just another type of transistor, and designers are focusing on value, selecting the transistor by considering cost at the system level.

One of the attractions of the JFET is its bang-per-buck. For a given on-resistance, this chip can be smaller than other forms of SiC transistor, and the cost of production is relatively low, with fewer mask layers required for its manufacture compared with that of the SiC MOSFET.

The downside of the JFET is that it's normally-on. So, to provide a normally-off product with good switching and an acceptable level of ringing, the SiC JFET is paired with a low-voltage silicon MOSFET in a cascode configuration.

To optimise this combination, the JFET and the silicon MOSFET must be designed together and matched, a task that plays into the hands of companies such as onsemi, which have expertise in both forms of transistor.

Market opportunities

onsemi sees a significant opportunity for its SiC JFET in solid-state circuit breakers. This device could replace electromechanical relays, which suffer from arcing that reduces their reliable lifespan when they are switched on and off. As well as an attractive candidate for this application, the SiC JFET could find deployment in EV battery disconnects, thanks to its small size, high reliability and very low on-resistance.

Another opportunity for the JFET is in AI, a technology that has led to a dramatic increase in the power within each rack in the datacentres. The high-voltage AC supply from the mains has to be converted down to a 0.8 volt DC form as efficiently as possible. Inevitable losses occur that lead to heating, with air cooling already replaced by liquid cooling to ensure adequate thermal management. "Our customers are saving twice, by using high-efficiency high-performance transistors. You need cheaper apparatus to cool, and you have less electrical energy wasted in heat, so you reduce the challenge of reliability," enthuses Fissore.

In addition, designs with the SiC JFET can accommodate high frequencies, minimising the size of the inductors. This allows onsemi to compete with companies producing GaN transistors for this application.

An alternative to the superjunction

onsemi's interest in the JFET started around five years ago, after realising that it would struggle to make an impression in the silicon superjunction market. The company identified the SiC JFET as a promising technology that would complement its SiC MOSFET portfolio, while offering the opportunity to go to higher frequencies.

Initially, onsemi invested internally, before changing direction and deciding to get to market more quickly through an acquisition.

Buying Qorvo's SiC JFET business – which it had acquired in late 2021 through the acquisition of United Silicon Carbide – has given onsemi a broad SiC JFET portfolio, with over 80 products, spanning 650 volts to 1.7 kV. onsemi could have also developed a comparable family of SiC JFETs through internal development, but Fissore estimates that it would have taken three-to-four years to do so.

For $115 million, onsemi has obtained Qorvo's SiC JFET business, its customers, a talented workforce, and IP related to planar and trench forms of this transistor. Little equipment came with the sale, as Qorvo outsourced JFET production, but onsemi is able to continue working with the established foundries and sub-contractors.

Separating Qorvo's JFET business from its other activities has been relatively easy for both sides, as the team working on the JFET were not heavily integrated with other activities. These new staff at onsemi are bringing much valuable experience, and they include those that invented JFET technology and have been working on this class of device for a couple of decades.

Substrate supply is not a concern for onsemi. As well as its own vertically integrated SiC supply chain, the company is able to work with the three suppliers that Qorvo has qualified – and it is looking to add to this list.

Another of onsemi's goals is to refine its JFET portfolio by lowering the on-resistance, measured in milli-ohms, to what is described as "very low single digits".

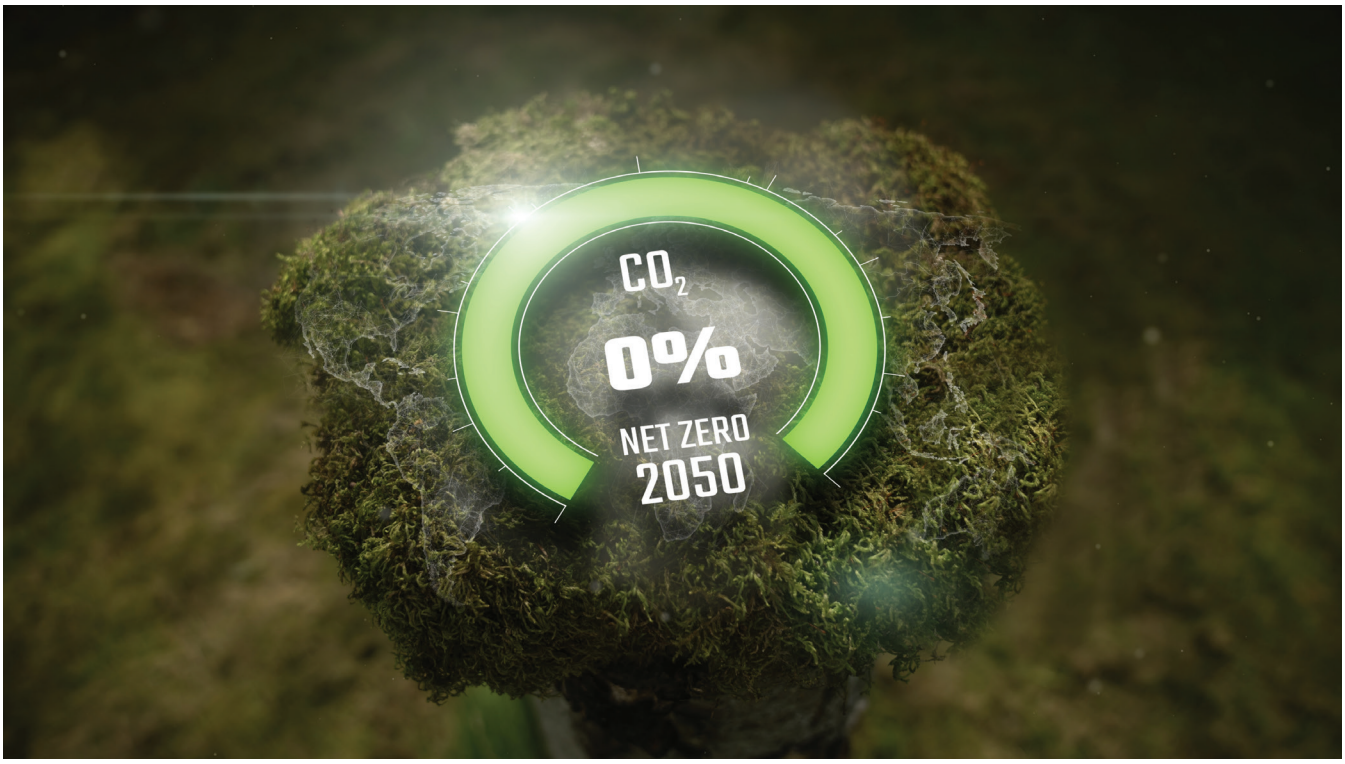
Efforts will also be directed at improving packaging, and introducing power modules capable of handling thousands of amps.

Given the market opportunities for the JFET, Fissore forecasts that competition will emerge for sales within a few years.

Potential rivals are not a concern, and the focus is on ramping sales of the JFET to generate revenues worth hundreds of millions of dollars.

"I'm sure we'll get there and stay as number-one market share as long as possible, meaning for decades," claims Fissore.

➤ Sergio Fissore holds the position of onsemi Vice President and General Manager, Multi-market Power Division. Fissore has previously worked at Infineon and the Fairchild, acquired by onsemi in 2016.



Power semiconductors for carbon neutrality

Advances in semiconductor and power electronics technologies, led by increasing deployment of wide-bandgap power devices, are essential for reducing greenhouse gas emissions and developing a carbon-neutral energy system by 2050

BY YUHAO ZHANG FROM THE UNIVERSITY OF HONG KONG

THE LAST decade has witnessed an increase in the adoption of wide-bandgap power devices, led by those based on GaN and SiC. Both these materials have enabled improvements to the performance of power electronics systems in numerous applications. But beyond performance, what impacts are these advanced semiconductors having? Are they set to play a major role in driving down greenhouse gas emissions? And are they critical to reaching carbon neutrality?

Recently, I have been digging into these important questions, working with departmental colleagues at the University of Hong Kong, and collaborators from Virginia Tech and the University of Cambridge. Together, we published our findings earlier this year in *Nature Reviews Electrical Engineering*. Our paper traverses the full material-device-circuit-application spectrum, to scrutinise the combined impacts of wide-bandgap semiconductors and power electronics on greenhouse gas emissions. This thorough investigation has led us to conclude that wide-bandgap power semiconductors are critical enablers to carbon neutrality.

Since 2015, 195 countries have joined the Paris Agreement, signing up to mitigate their greenhouse gas emissions and strive towards the goal of carbon neutrality by 2050. Currently, energy generation and energy use accounts for around three-quarters of greenhouse gas emissions, mainly associated with four sectors: electricity generation, transportation, industrial processes, and the cooling and heating of buildings. Power electronics are utilised ubiquitously in all these sectors for electrical energy conversion, such as stepping up and down the current and voltage, as well as converting between AC and DC forms.

Crucial to determining the efficiency, power density and form factor of power electronics systems are the power semiconductors, in conjunction with the circuit topology and control. While it is well known that the adoption of GaN and SiC devices can bring significant performance advances, their environmental impact on carbon emissions is less researched. Filling the gap between semiconductor technology and carbon footprint demands a multi-disciplinary approach, covering the full spectrum of material, device, circuit and application.

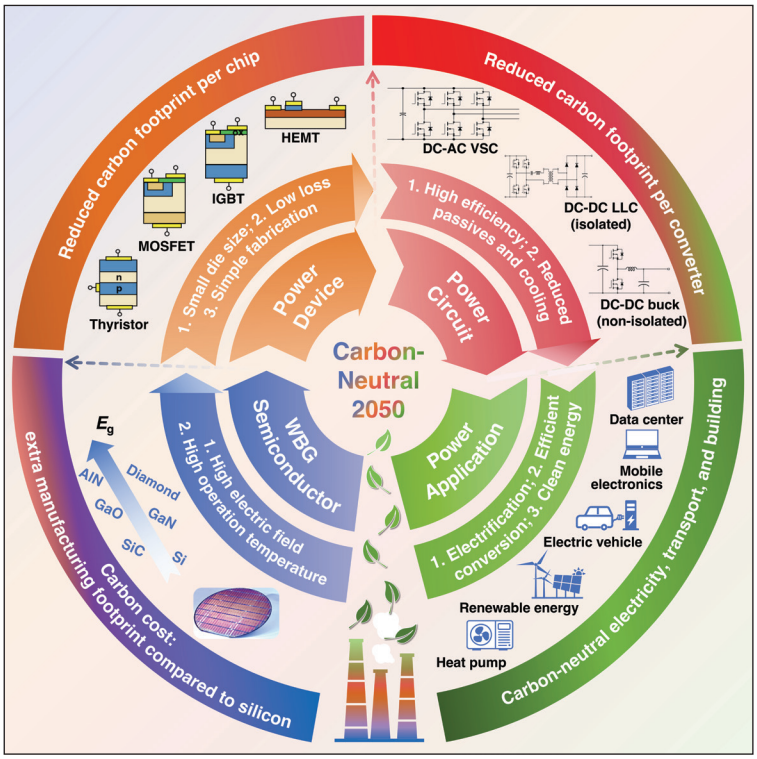
The uptake of GaN and SiC power devices cuts carbon footprints on many fronts. At the device and circuit level, these wide bandgap diodes and transistors can potentially have smaller carbon footprints than their silicon cousins, due to their smaller die size and superior performance. These strengths enable: a lower per-chip carbon footprint for the same energy and chemicals used in manufacturing a wafer; reduced energy loss, associated with an increased converter efficiency; and dematerialisation, that is, a reduction in the volume of materials used for passive and cooling components.

At the application level, wide bandgap semiconductors cut carbon emissions on three key fronts. First, they reduce energy loss in power conversion and trim the energy consumed by cooling systems; for example, these devices and co-optimised circuits increase the efficiency of electrical conversion from grid edge to the processors in data centres from below 80 percent to over 90 percent. Second, power devices and circuits aid the use of renewable energy in electricity generation, for example, through the use of solar photovoltaics, wind power generation, electric vehicles and heat pumps. Third, power electronics with a fast dynamic response, high switching frequencies and a high-power density promotes the electrification of transportation and buildings, for example, by boosting an electric vehicle's driving range, its charging time and its energy efficiency.

We have analysed and quantified the potential reduction of carbon emission across four pivotal sectors – renewable energy systems, electric vehicles, data centres, and heat pumps – from the perspectives of electrification and energy conversion efficiency. This led to a number of interesting findings, such as the replacing of 80 percent of fossil-fuel electricity generation with GaN/SiC-based photovoltaic systems could lead to an annual reduction in US greenhouse gas emissions of at least 1,236 million tonnes – that's equivalent to the annual emissions of 245 million gasoline passenger vehicles.

According to our study, substantial savings in US greenhouse gas emissions can also be realised with other significant initiatives, such as a reduction by 390 million tonnes by replacing 80 percent of gasoline cars with GaN/SiC-based electric vehicles. Meanwhile, in data centres, if silicon devices were replaced with those made from GaN and SiC, this could reduce US greenhouse gas emissions by at least 1.7 million tonnes per year; and if US homes currently heated by natural gas switched to heat pumps powered by photovoltaic systems, this could slash greenhouse gas emissions by around 260 million tonnes per year.

To ensure rigour in our findings, we considered the extra carbon emissions associated with GaN and SiC production, compared with those for legacy silicon manufacturing. Despite the smaller size of wide bandgap devices, the raw materials, chemicals and energy used in their production could be very different from those for silicon.



➤ Figure 1. The role of wide-bandgap power semiconductors in achieving carbon neutrality.

For this part of our analysis, we surveyed the normalised carbon emission by corporate revenue for GaN, SiC and silicon manufacturing, based on data disclosed from third-party-verified sustainability reports from major power semiconductor companies. From the survey, we estimated the extra carbon footprint for GaN/SiC manufacturing. We found this to be marginally small compared with the system-level carbon saving.

We hope that our recent paper, offering the first quantitatively analysis of the impact that wide-bandgap power semiconductors could have in realising carbon neutrality, will become a useful reference for researchers, engineers, and policymakers. Despite their potential to deliver significant change, the consequences of increasing the deployment of SiC and GaN devices have not been considered in detail, such as their impact on sustainability. But what we do know is that further innovation across materials, devices, circuits and systems, as well as a shift to designing power electronics based on the principles of reuse, remanufacturing and recycling, is essential to fulfil the potential of wide-bandgap power electronics for carbon neutrality.

FURTHER READING / REFERENCE

➤ Y. Zhang *et al.* "Wide-bandgap semiconductors and power electronics as pathways to carbon neutrality" nature reviews electrical engineering **2** 155 (2025)

Power-SOI technology and its potential to shape the future of power electronics

Soitec's Power-SOI 300mm substrates for advanced gate driver ICs to drive power conversion wide-bandgap devices at high switching frequency.

BY ALEX LIM AND RAINER LUTZ, SOITEC

THE POWER CONVERSION industry is shifting from silicon-based IGBTs to wide-bandgap (WBG) MOSFETs and JFETs to achieve higher voltages and better performance in applications such as electric vehicles, renewable energy systems, and data centers. WBG materials, such as SiC, GaN, and diamond, are known for their superior high-frequency switching capabilities.

Power-SOI is a robust silicon-on-insulator (SOI) technology that enables advanced designs for gate drivers and power management ICs. By supporting high-frequency switching, it is particularly well suited to next-generation power conversion devices based on WBG materials.

This white paper examines Power-SOI technology and its potential to shape the future of power electronics, paving the way for more efficient, compact systems across automotive, industrial, and renewable energy sectors.

Introduction

The power electronics industry continues to pursue higher efficiency, greater power density, and better thermal management. With silicon-based IGBTs reaching their limits, WBG semiconductors like SiC and GaN are emerging as leading options for next-generation applications.

Although WBG materials offer superior properties, fully leveraging them requires specialized driving and control solutions. This white paper introduces Power-SOI technology, designed to unlock the full potential of WBG devices in power conversion and motor control systems.

Now available in 200 mm and 300 mm, Power-SOI is a robust SOI technology that enables state-of-the-art gate drivers and power management ICs (PMICs). These Power-SOI based ICs simplify the design of SiC and GaN device platforms, improve reliability, and boost system performance in applications such as electric vehicles, industrial automation, renewable energy systems, and data center power supplies.

The following sections delve into the design considerations, operating principles, and performance benefits of Power-SOI technology, underscoring its pivotal role in the widespread adoption of next-generation WBG devices across various industries.

Gate Driver and PMIC's trends and challenges

The adoption of WBG semiconductors in power conversion and motor control drives critical advancements in gate driver and power management IC (PMIC) technology. Evolving trends

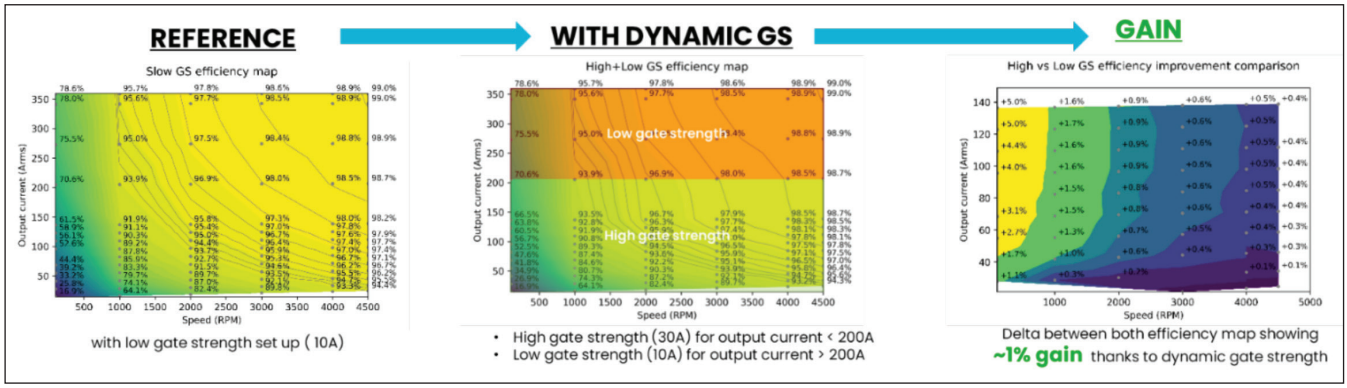
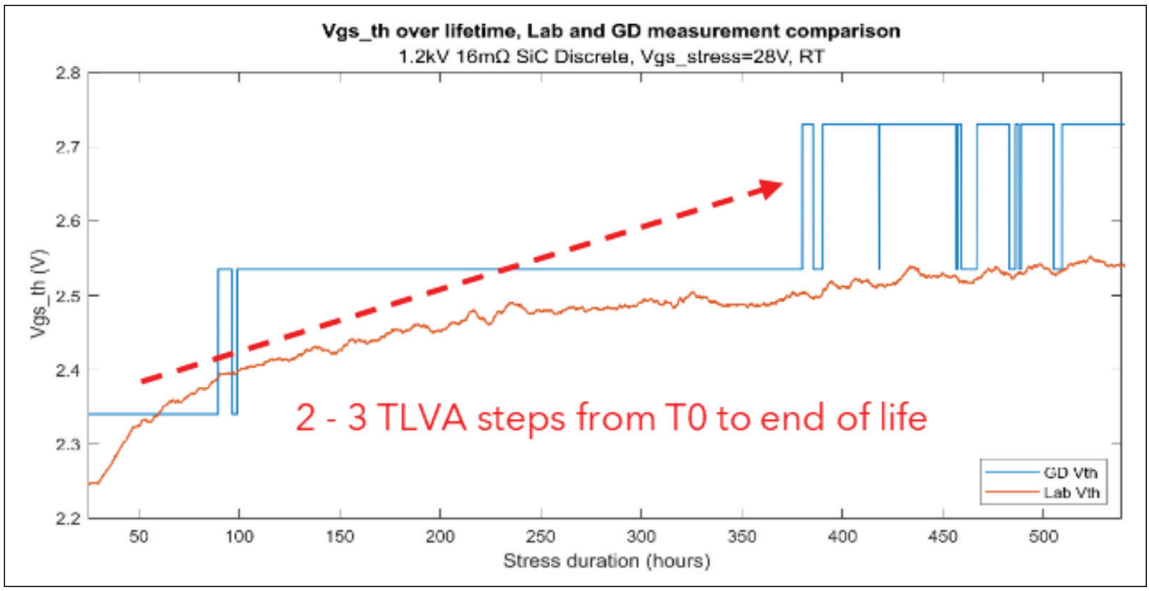


Figure. 1 GD3162 Efficiency Gain with Dynamics GS (Courtesy to NXP Semiconductors)



➤ Figure 2. Vth Drift Over Time As Measured by GD3162 (Courtesy to NXP Semiconductors)

and challenges are now guiding the development of next-generation PMIC solutions, particularly on 300 mm wafers.

Higher Switching Frequency: WBG devices are switching at significantly higher frequencies compared to silicon-based devices, enabling higher power densities and improved system efficiency.

This performance represents challenges for gate driver ICs with:

- Managing higher dV/dt and dI/dt transients during switching transitions caused by parasitics in the circuit
- Minimizing propagation delays and ensuring precise timing control
- Providing adequate and well controlled drive strength to charge and discharge gate capacitances quickly as the gate drive strength of WBG devices is significantly lower than silicon devices

Higher Voltages and Operating Temperatures: WBG devices operate at higher voltages (> 1200V) with higher junction temperatures (Tj) (> 175°C) compared to silicon. Gate driver ICs must withstand these extreme conditions while ensuring reliable operation, requiring:

- High voltage isolation and robust circuit protection
- Stable operation across a wide temperature range
- Careful layout and packaging considerations for harsh environments

Much More Dense Integration Of Intelligent Features: To simplify system design and improve reliability, gate driver ICs are evolving towards higher integration of intelligent features:

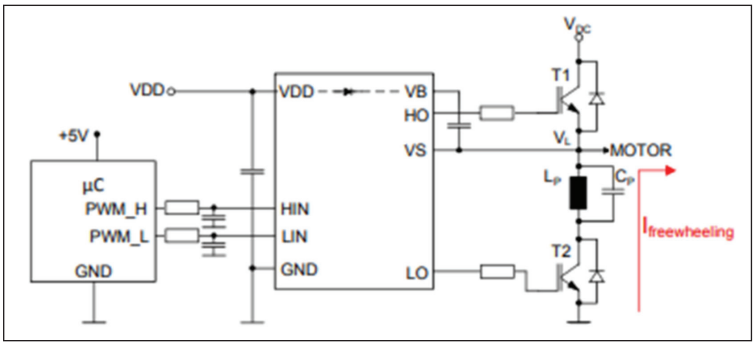
- Integrated power stages and low-side/high-side drivers
- Advanced monitoring and protection (desaturation, overcurrent, undervoltage lockout) with increasing digital blocks (e.g. non-volatile memory (NVM) etc.)
- Adaptive driving techniques (active Miller clamping, di/dt control etc.) and programmability

Automotive and Industrial Qualification: As WBG devices find applications in automotive and industrial sectors, gate driver ICs must meet stringent quality and reliability standards :

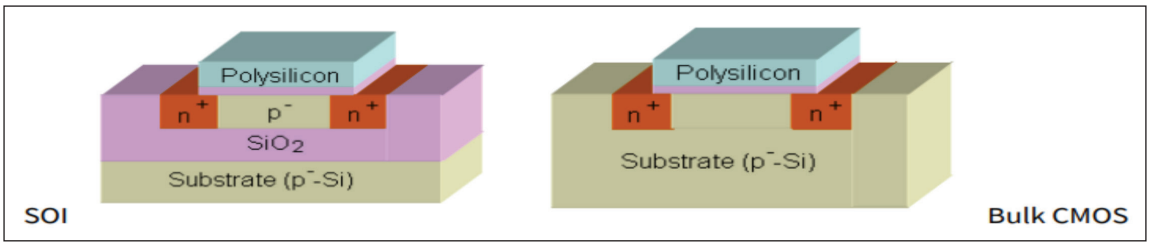
- Automotive qualifications (AEC-Q100, ISO 26262) and industrial qualification (IEC61508)
- Robust electromagnetic compatibility (EMC) and electromagnetic interference (EMI) performance
- High manufacturing quality and traceability

Innovative gate driver solutions specifically designed for wide-bandgap power devices are crucial for realizing high-efficiency, high-density power conversion and motor control systems. The functionally safe NXP GD3162, for example, offers dynamic gate strength control, power device aging detection, and integrated fast (<1 µs) short-circuit detection, thereby improving efficiency and enhancing system safety.

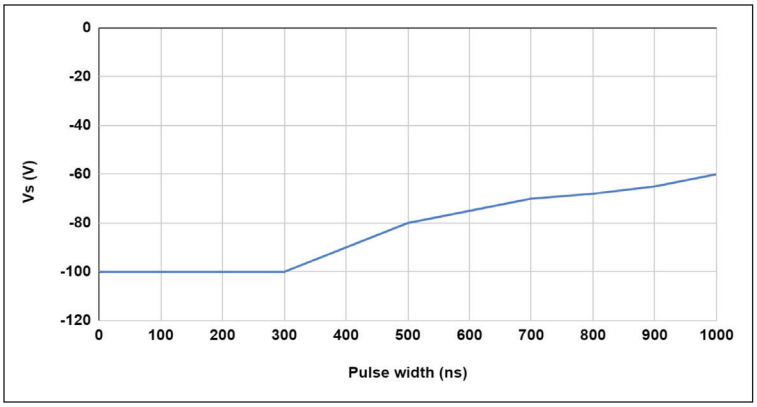
With adjustable dynamic gate strength, the GD3162 optimizes gate current based on load requirements, reducing switching losses. Figure 1 shows efficiency gain test results using NXP's power inverter reference design.



➤ Figure 3. Typical half bridge (HB) topology [1]



➤ Figure 4. Basic silicon-on-insulator (SOI) as compared to bulk CMOS structure [2]



➤ Figure 5. Example of NTSOA of an Auto Power-SOI based gate driver IC [2]

During a SiC power device's lifetime, its threshold voltage (Vth) may shift, serving as a key reliability indicator. By tracking these shifts, the GD3162 supports power switch diagnostics and predictive reliability. Figure 2 shows the Vth drift over time as measured by the GD3162.

Power-SOI Technology: A Game-Changer in 300mm

Power-SOI is a key enabling technology that addresses evolving gate driver IC requirements and challenges for advanced WBG-based power devices.

Power-SOI is a key technology for high-speed switching

Power-SOI provides superior negative transient voltage robustness. In contrast, standard bulk-based integrated circuits tolerate only limited negative voltages – typically around –1 V – before generating uncontrolled substrate currents that disrupt gate driver IC operation. Because bulk-based gate driver circuits lack isolation, fast switching and circuit parasitics can induce oscillations and voltage swings, exposing IC pins to negative voltages. Figure 3 illustrates an example of negative voltage during gate driver operation.

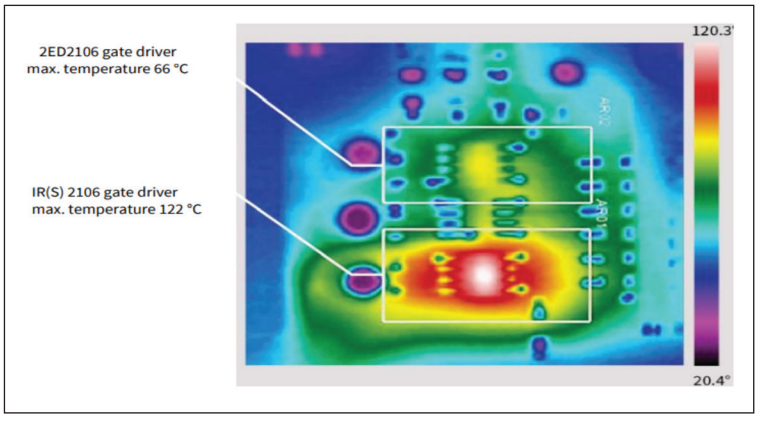
When IGBT T1 is off, the motor's inductive load generates a negative voltage at T2's collector as the freewheeling current (Ifreewheeling) flows through T2's freewheeling diode. Circuit parasitics (Cp and Lp) can exacerbate this effect, causing the half-bridge output voltage (VL) to swing to -20 V to -100 V for short durations.

Because VL is tied to the gate driver IC's VS pin, these transients can disrupt operation or even damage the device. Hence, it is critical to ensure the gate driver IC pins can withstand such negative voltages and incorporate robust internal protection.

Power-SOI, developed using Soitec's Smart Cut™ process, is an advanced SOI technology, widely adopted by smart gate driver ICs. Its buried oxide (BOX) layer isolates the active region from the silicon substrate, significantly reducing parasitic capacitance and preventing leakage or latch-up between adjacent devices. Figure 4 compares Power-SOI and bulk CMOS substrates. By insulating the active area from the substrate, the BOX inherently improves immunity to negative voltages, enhancing the negative transient safe operating area (NTSOA) of gate driver ICs. Figure 5 shows an example of the NTSOA for a Power-SOI-based gate driver IC [2].

The superior NTSOA enabled by PowerSOI allows the gate driver IC to support higher switching frequencies with good performance and no unexpected disturbances.

Power-SOI supports smaller PN junctions by leveraging its BOX layer to reduce parasitic capacitances. A lateral high-voltage, low on-resistance device can be implemented using double RESURF (reduced surface field) technology, combined with a simple local oxidation (LOCOS) process, the BOX layer, and thin drift regions in the top SOI film. This design lowers on-resistance per area and reduces gate capacitance, enabling gate driver ICs to achieve higher switching frequencies. It also minimizes propagation delays, ensuring precise timing control and sufficient drive strength for rapid gate charging and discharging of external MOS devices.



➤ Figure 6. Example of the comparison of Auto Power-SOI based gate driver IC and bulk based gate driver IC [2]

Power-SOI further reduces power dissipation at high switching frequencies by lowering device gate capacitance, resulting in lower switching losses than comparable bulk-based gate driver ICs. As shown in Figure 6, this improvement enables higher operating frequencies and confirms Power-SOI's superior efficiency and performance [2].

Power-SOI technology supports higher voltages and temperatures, enabling greater monolithic integration of high- and low-voltage blocks on the same die. By combining Power-SOI substrates with deep trench isolation (DTI), Power-SOI reduces the overall die footprint while providing robust dielectric isolation via its BOX layer. This isolation mitigates latch-up and parasitic coupling, while DTI structures form vertical barriers that allow high- and low-voltage devices to coexist in close proximity. Figure 7 compares the device-to-device isolation spacing among current technologies [3].

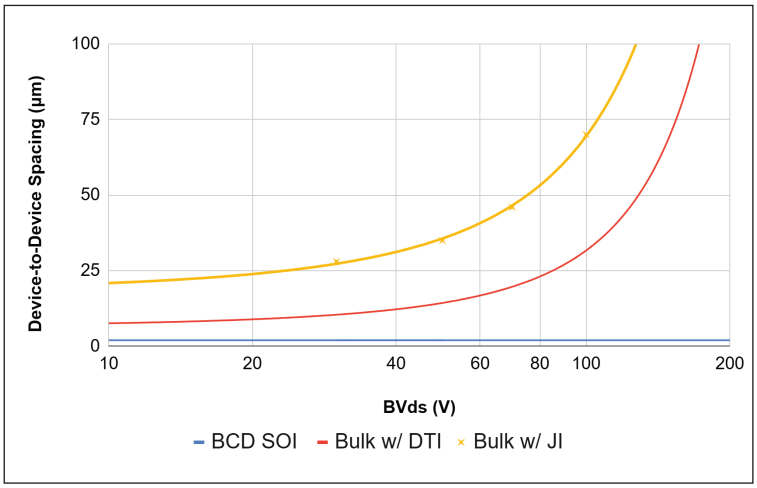
Power-SOI exhibits low leakage currents at high temperatures, making it well-suited for high-frequency power devices. Its BOX layer isolates the active region from the substrate, suppressing leakage paths that typically increase exponentially with temperature in bulk devices. Figure 8 compares leakage currents for both Power-SOI with DTI and bulk substrates with junction isolation [4].

Power-SOI's exceptionally low leakage current above 125 °C simplifies high-precision analog circuit design by eliminating the need for extensive temperature compensation, enabling reference circuits with reduced voltage and gain drift. This improves gate driver performance and reliability in high-temperature applications.

Power-SOI enables greater integration of intelligent features

As highlighted in the previous session, Power-SOI technology enables monolithic integration of high- and low-voltage blocks on a single die, reducing the overall footprint. This allows incorporation of power stages, low- and high-side drivers, and advanced monitoring and protection features within a single smart gate driver IC. Meanwhile, its BOX and DTI structures minimize noise coupling and crosstalk, streamlining the integration of next-generation gate driver ICs with intelligent features.

Power-SOI enables monolithic integration of a bootstrap diode and resistor on the gate driver die, eliminating external components and reducing system costs as well as total cost of ownership (TCO). It also allows on-chip monitoring features, such as switch node voltage and high-side switch status, lowering both BOM and PCB area, particularly in three-phase motor drives. Furthermore, Power-SOI simplifies co-packaging of gate driver chips and WBG transistors, increasing integration, boosting power density, and placing protection circuits closer to the power switches.



➤ Fig 7. Device-to-device isolation spacing based on BCD with Power-SOI and DTI, BCD with bulk and DTI and BCD with bulk and junction isolation [3]

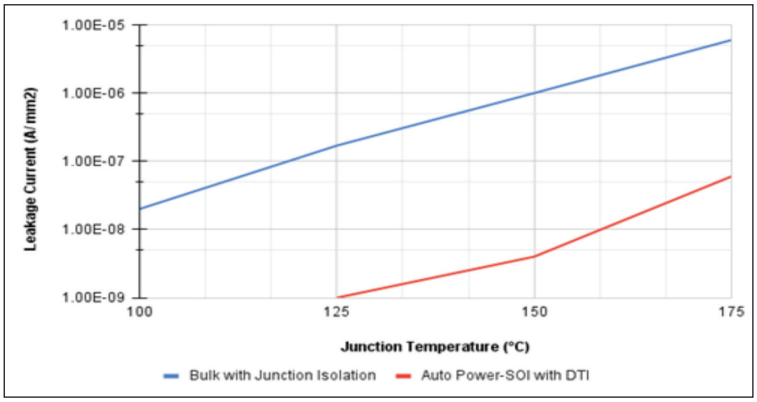
Power-SOI is fully qualified for automotive and industrial applications

The demand for higher functional safety (FuSa) requirements such as automotive ISO26262 and industrial IEC61508 is getting higher with the rising of higher autonomous driving level and factory automations (e.g. industry 4.0 & 5.0, digital twins factory etc.).

Power-SOI eases the design of higher functional safety (Fusa) level ICs. Power-SOI enables higher monolithic integration, reducing the chip count per system. Fewer components decrease the overall system failure-in-time (FIT) rate by minimizing interconnect and other failure points. This chip-level integration enhances system reliability, a critical requirement for achieving automotive and industrial functional safety targets. The monolithic integration facilitated by Power-SOI's DTI & BOX isolations directly improves the mean time between failures (MTBF) for safety-critical applications.

Power-SOI's high robustness and high reliability ease the qualifications

Power-SOI enhances electromagnetic compatibility



➤ Fig 8. Comparison of leakage currents for Power-SOI with DTI and bulk substrate with junction isolation [4]

(EMC) and reduces electromagnetic interference (EMI) through symmetric output stages and device isolation. Its BOX layer ensures complete isolation and prevents substrate noise propagation, while DTI and BOX minimize crosstalk.

Power-SOI's isolation enables high-voltage ESD protection by cascading low-voltage protection devices without introducing parasitic elements, optimizing the ESD-protection window in high-voltage designs. Additionally, replacing deep N-well junction isolation with DTI reduces the ESD layout area.

With intrinsic robustness against latch-up, ESD, EMC, and EMI, Power-SOI minimizes systematic faults from manufacturing. Its BOX and DTI layers enhance reliability, reducing the need for complex design techniques to manage process-induced faults. This simplifies the development of high-functional safety (FuSa) systems compliant with stringent automotive and industrial standards like ISO 26262 and IEC 61508.

With Power-SOI's superior low leakage current at high junction temperature as explained in previous session., it is easy to develop next generation gate driver IC passing AEC-Q100C gate 0 requirements.

And now, Power-SOI is available in 300mm

Power-SOI has been produced by SOITEC for decades in 200mm and smaller wafer sizes, with typical SOI top layer thickness in the micrometer range. Leveraging its Smart Cut™ technology, SOITEC has delivered millions of SOI wafers.

A transition from 200mm to 300mm is now underway among key Power-SOI players, driven by the need for better integration with advanced semiconductor manufacturing tools. To support this shift, SOITEC now offers thicker SOI wafers, combining Smart Cut™ technology with monocrystalline epitaxy. This process enables the growth of high-quality thick SOI layers with excellent crystallinity, precise control over resistivity and thickness uniformity, and minimal defectivity.

Conclusion

Power-SOI technology is a key enabler for advanced gate drivers and power management ICs, optimizing power conversion for WBG devices in fast-growing markets. Its monolithic integration, utilizing DTI and BOX layers, produces more compact, reliable ICs with inherent resistance to latch-up, ESD, and EMC/EMI issues, enhancing overall system reliability.

By reducing chip count, PowerSOI lowers system FIT rates and improves functional safety, meeting stringent automotive standards like ISO 26262 ASIL-D and IEC 61508 SIL-4. With 300mm availability, its adoption is expanding in EVs, renewable energy, and data center power systems.

PowerSOI continues to drive innovation, meeting the industry's evolving demands for performance, safety and efficiency.

FURTHER READING / REFERENCE

- 1. Jinsheng Song & Wolfgang Frank, Infineon, 2015, Robustness of level shifter gate driver ICs concerning negative voltages
- 2. Infineon, 2019, Advantages of Infineon's high-voltage gate driver ICs (HVICs) based on its silicon-on-insulator (SOI) technology
- 3. Alex LIM JAN PANG, Soitec, PCIM Europe 2024, 2024, Auto Power-SOI: Shaping the Future of Battery Monitoring Technology
- 4. Keiichi Fujii, 2017, "Automotive battery monitoring IC with functional safety using SOI technology",IC", https://holdings.panasonic/jp/corporate/technology/technology-journal/pdf/v6302/p0111.pdf

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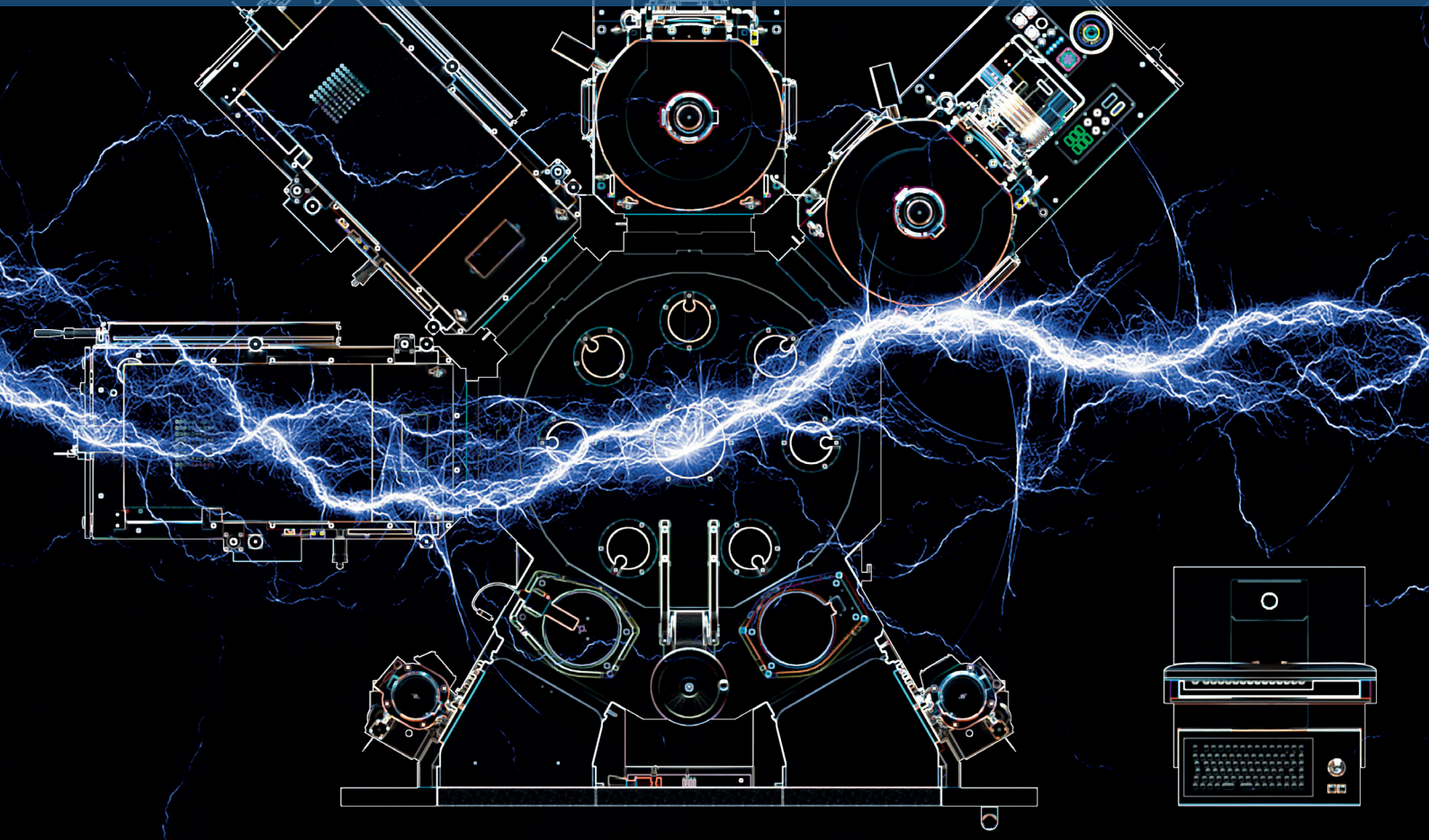

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A step change in low-power circuit design

How the nPZero power-saving IC enables sensor system operation at the nanoamp level.

BY JAN FRODE BERGSØ, BUSINESS DEVELOPMENT MANAGER, NANOPOWER SEMICONDUCTOR

A MAJORITY of IoT devices are powered by primary battery cells, also known as non-rechargeable batteries, but limited battery life and the need to replace discharged batteries create numerous problems:

- The cost to maintain a battery power supply, and to replace a discharged battery. This is particularly problematic in commercial and industrial environments, in which a large number of sensors might need regular battery replacement.
- The risk of suspension of system operation in the interval between the failure of a discharged battery, and its replacement with a fresh battery.
- The cost and environmental damage attributable to disposal of a battery at the end of its life.

In battery-powered IoT systems, which typically include a wireless connection to the internet, a smartphone, or to a central control system, the device's RF system-on-chip (SoC) or microcontroller (MCU) is responsible for most of the energy consumption. Peripherals such as sensors also drain energy from the battery, but typically at a lower rate than the SoC does.

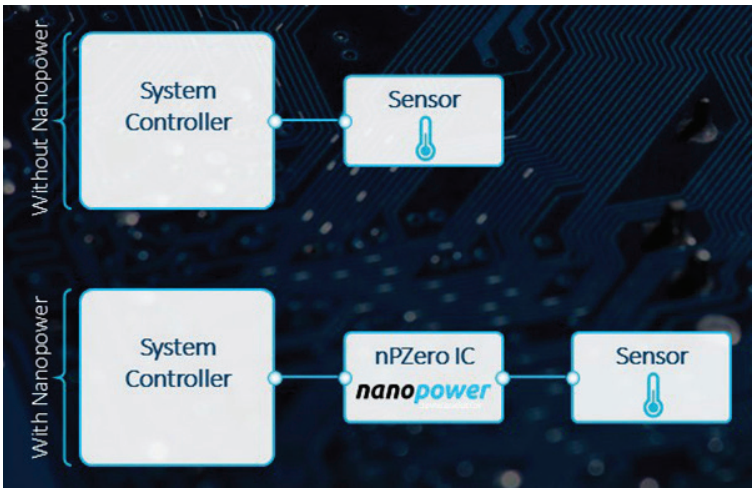


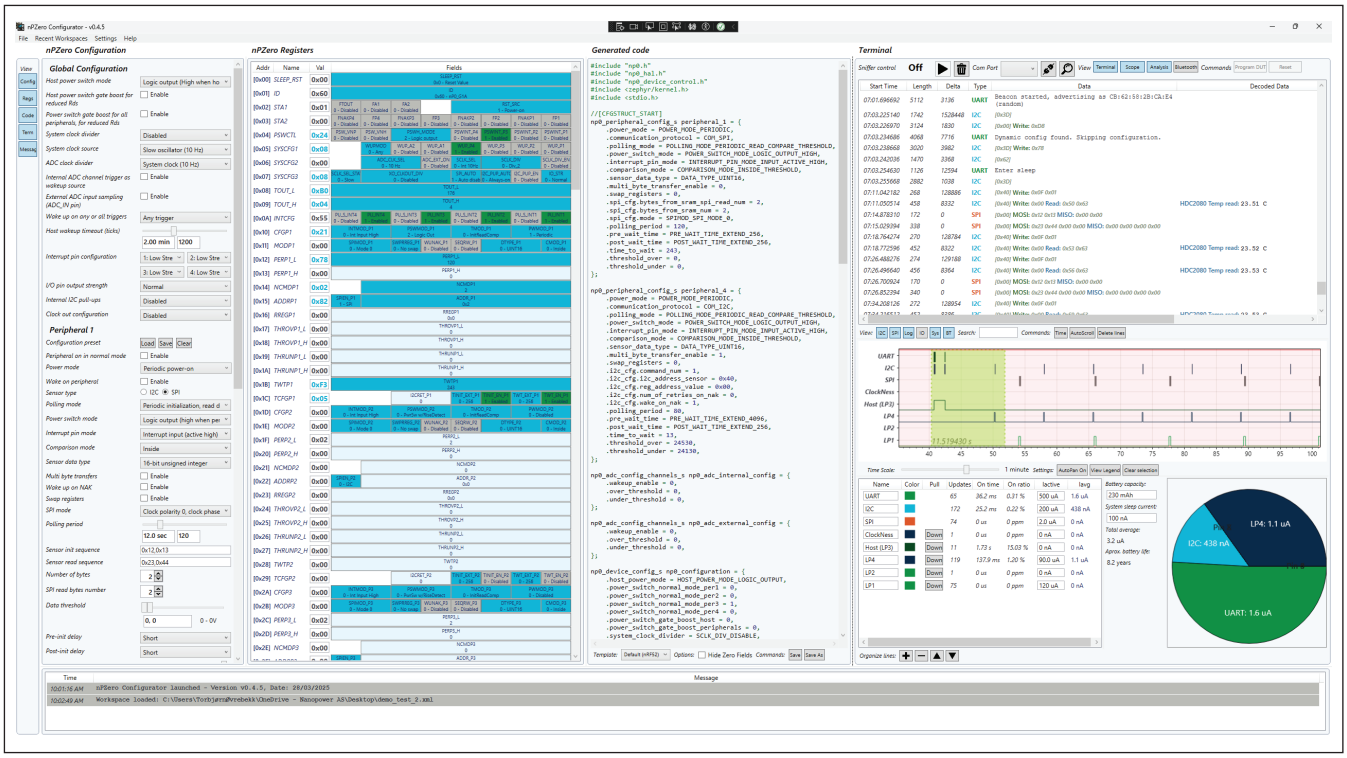
Figure 1. The nPZero IC operates as a companion chip to the SoC.

The power problem is inherent to a wireless SoC: the device needs a relatively high-performance, high-power compute system to handle the complex operation of a Bluetooth® Low Energy or similar radio protocol, as well as to perform control logic operations in response to significant sensor or user inputs. Yet in many applications, the full capability of this compute and communications circuitry is only deployed for a tiny fraction of the time. For more than, in some cases, 99% of the system's operating time, the host device is greatly over-specified for the quiescent-state operations it performs.

MCU manufacturers have put a lot of research and development effort into trying to reduce their products' power consumption in sleep mode, when the device is not performing communications or control operations. But there is a floor below which the power consumption of these big, sophisticated chips will not fall. And so embedded device manufacturers have previously had no choice but to build their power budget and to size their battery to cope with an SoC's high power consumption even when their application is doing nothing apart from periodically monitoring sensor values.

Now Nanopower Semiconductor has developed a dedicated power-saving chip, a companion to the SoC, which reduces average system power consumption in typical endpoint wireless IoT devices by up to 90%.

Finding a way to turn off the SoC



If the problem is the power consumed by the SoC when it is running, even in sleep mode, a solution might be found in switching off the SoC entirely. This is the theory behind the introduction of a new type of power-saving IC, a device which can perform the functions that the SoC performs when it is not active, but at a small fraction of the SoC's power consumption.

This concept of this power-saving IC has been developed by European start-up company Nanopower Semiconductor, and has been implemented in its first-generation nPZero product.

The nPZero is compatible with most SoCs and sensors on the market (see Figure 1). In an IoT endpoint device comprised of one or more sensors and other peripherals, the nPZero takes over sensor monitoring and system control functions between radio transmissions or trigger events, enabling the SoC to shut down completely until a threshold event occurs that requires the nPZero to wake up the SoC and hand over control to it.

Thanks to the implementation of innovative sub-threshold mixed-signal technology developed by Nanopower, the nPZero draws less than 100nA when actively monitoring and controlling sensors. Nanopower has proved the potential of the nPZero to make system power savings in typical IoT device designs of between 50% and 90%. This results in:

- Greatly extended battery life, reducing replacement frequency and cost
- The option to reduce battery size, allowing for more compact device designs
- The potential for battery-free operation. The Nanopower power-saving technology can enable the addition of a harvested energy source, eliminating the risk of battery power failure, or even enable a system to run on harvested energy alone.

How the nPZero minimizes power consumption in the quiescent state

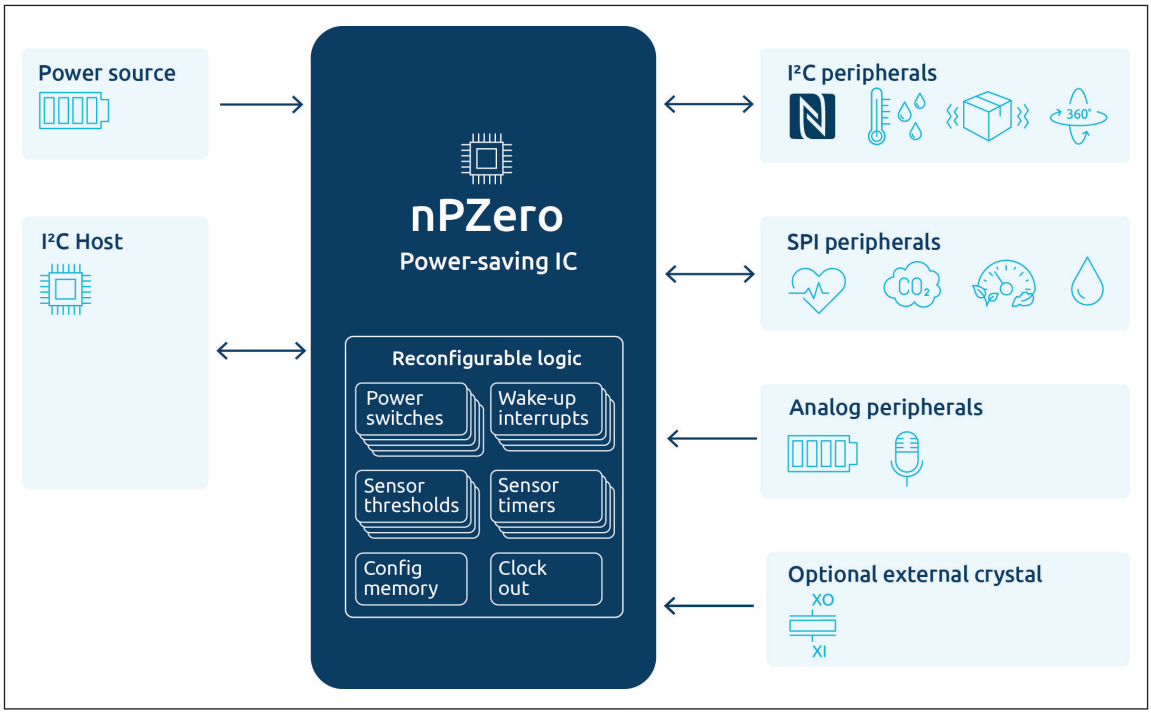
The typical use case for the nPZero is in IoT endpoints which monitor system parameters, such as temperature or motion, and which only communicate when a notifiable event occurs (such as the temperature crossing a pre-set threshold value, or excessive vibration). The nPZero performs system monitoring with the host SoC switched off, and wakes up the SoC only when a notifiable sensor value has to be transmitted. The nPZero might typically also wake up the SoC at a regular interval to send a system update.

In system monitoring mode, the nPZero can operate on an interrupt basis: here, the sensor is always on, and its state machine interrupts the nPZero when an event needs to be triggered.

Alternatively, the nPZero can operate in I2C or SPI mode: here, the nPZero polls sensors on a pre-set schedule. This means that the sensors can be switched off between polling events, saving even more power.

Nanopower provides a zero-code nPZ Configurator tool for configuring sensors in the system, applying polling schedules, and setting the parameters for triggering events (see Figure 2). The nPZ Configurator tool automatically generates the firmware code needed for the host MCU to configure the nPZero. The code can be inspected

➤ Figure 2. The zero-code tool for configuring the nPZero's operation features an intuitive GUI



➤ Figure 3. In the nPZero EVB, the nPZero manages sensors' operation with the SoC host switched off, and only wakes up the SoC when a sensor's threshold value is crossed, or for scheduled data uploads.

and manually edited in the tool if needed. Additionally, the tool can analyse the state of power switches and serial interfaces in a running system, allowing the user to evaluate the efficiency of a given implementation, and tune the configuration of the nPZero device to their requirements. Hardware implementation is also straightforward: the nPZero requires only a few external passive components, and an optional crystal for more accurate time keeping.

Test system demonstrates power-saving potential of nPZero

The potential for power-saving in endpoint IoT devices can be seen in a comparison between a conventional design implementation and a demonstration system based on the nPZero IC. The test system is based on the nPZero Evaluation Board (EVB). This is a modular system which makes it easy to add sensors to the nPZero baseboard via PMOD headers, and to add an SoC daughtercard via an Arduino Uno-compatible interface.

The demonstration design uses the ams OSRAM AS6212 temperature sensor and STMicroelectronics LIS2DW12 accelerometer boards that are shipped by Nanopower with the EVB. The SoC is an nRF52840 Bluetooth Low Energy microcontroller from Nordic Semiconductor (see Figure 3).

Designers of endpoint IoT devices can evaluate this performance themselves with the nPZero EVB and their choice of PMOD sensor boards and SoC daughtercards

Such a system might typically be used in applications such as monitoring the condition of goods in transit, or for cold-chain data logging. The test system is set up to provide frequent measurements. The temperature sensor is read every 4s and the accelerometer every 0.625s. The nPZero IC is set to wake the host if a movement is detected or the temperature is outside the range 18°C to 28°C. Regardless of sensor measurements, the host also wakes up every 5 minutes to send the most recent sensor readings via Bluetooth link. The test compared total energy consumption of the EVB system first without the nPZero – that is, with the nRF52840 SoC controlling the sensors' operation directly – and then with the nPZero, allowing the SoC to be switched off between radio transmissions.

With the nRF52840 controlling the sensors via I2C interfaces, and the nPZero disabled, average current over an hour's operation was 395.4µA. After enabling the nPZero to control the system via I2C, allowing the nRF52840 to be switched off between transmissions and the sensors to be duty-cycled, average current falls to 49.6µA – a reduction of 87%, while providing exactly the same functionality and performance.

How to evaluate the nPZero's operation

Designers of endpoint IoT devices can evaluate this performance themselves with the nPZero EVB and their choice of PMOD sensor boards and SoC daughtercards (see Figure 4). The nPZero Configurator tool is available free for users of the EVB.

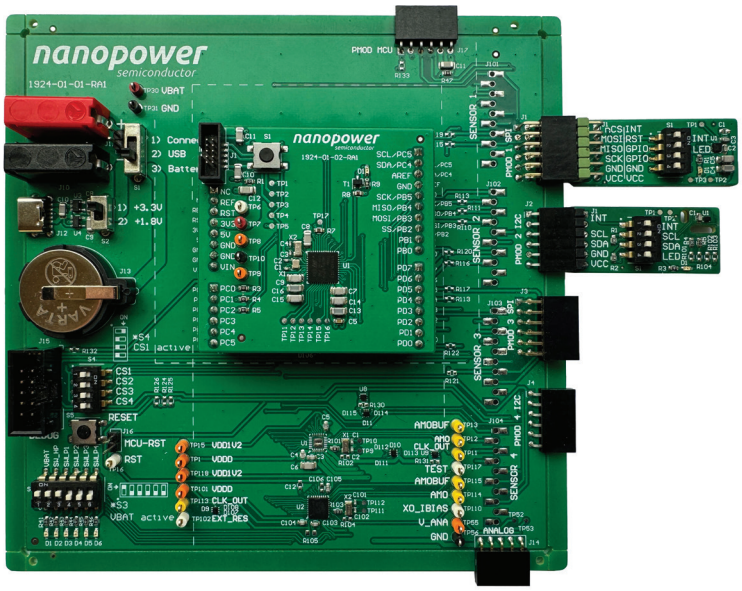
OEMs can also emulate a demonstration design developed by Nanopower which shows how the

nPZero can be used to substitute harvested energy for a battery power supply. Developed jointly with TDK, this system features the nPZero power saving IC continuously controlling environmental sensors including the TDK CH201 time-of-flight sensor. The battery-free system is powered by TDK CeraCharge solid-state batteries energized by Epishine indoor photovoltaic cells.

Naturally, power is not the only aspect of a system design that an OEM cares about: decisions about the use of the nPZero IC are also affected by the question of system cost and size. Here as well, the nPZero has a powerful case to make: as Figure 3 shows, the nPZero includes an internal low-power oscillator and power switches, enabling external components implementing these functions to be eliminated from the bill-of-materials.

In addition, the power savings produced by the nPZero can enable the OEM to reduce the size of the battery and the system enclosure.

So the nPZero offers considerable advantages to designers of wireless endpoint IoT devices, and thanks to the availability of the nPZero EVB, these advantages can readily be evaluated in the user's application.



➤ Figure 4. The nPZero EVB enables users to add their choice of PMOD sensor board and SoC daughtercard.

Dynamic characterisation of a power semiconductor bare chip

Power semiconductor devices are used in a variety of forms, such as being packaged in Surface Mount Devices (SMDs) or power modules, and they find broad applications.

BY KEYSIGHT

POWER SEMICONDUCTOR bare chips are loaded into these packages. It is desirable to characterize the bare chip before placing it in a package or a power module to expedite development. However, the small size, fragile structure, and parasitic effects caused by probing create multiple challenges for dynamically characterizing these power semiconductor bare chips. This article reviews the challenges of performing dynamic characterization on a bare chip, as well as some new technologies that help address these challenges.

Do you have a desire to measure power semiconductor devices as soon as they are fabricated? Power semiconductor devices are initially fabricated on a wafer, followed by dicing and packaging before they can be used in actual power electronics circuits. Characterization in the early phases of the manufacturing process helps expedite device development. For power module development engineers, understanding the behavior of power semiconductor bare chips is beneficial for accelerating development and aiding in troubleshooting.

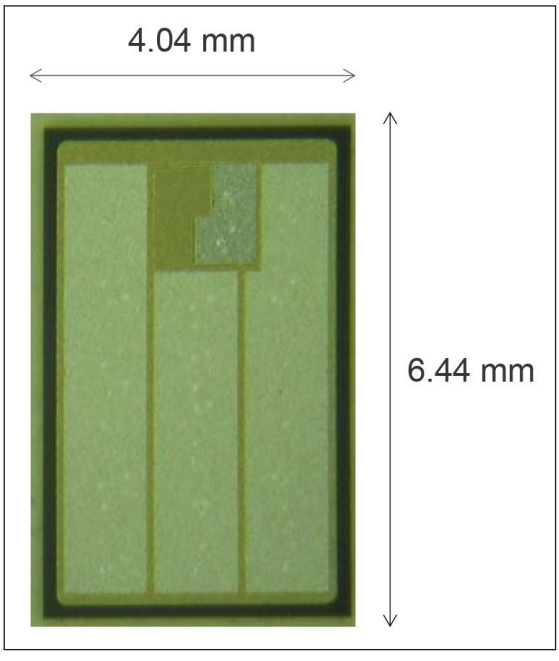
Challenges for dynamic characterization on power semiconductor bare chips

Static characterization of power semiconductor bare chips is not too difficult. The chip is physically fixed tightly on an electrically conductive stage for drain contact, and the source and gate are probed using needles from the top side of the chip. Parasitics associated with the fixturing do not significantly deteriorate measurement performance. Instruments such as curve tracers or impedance analyzers can be used for static characterization.

On the other hand, dynamic characterization of power semiconductor bare chips is extremely difficult. First, parasitics in the test circuit significantly deteriorate dynamic characterization, especially for Wide Band Gap (WBG) power semiconductors due to their fast speed. For instance, probe needles introduce additional parasitics, causing oscillation, ringing, and resulting in distorted measurement waveforms. These probe needles can also pose a risk of arcing due to the high voltage signals used in testing.

Second, SiC MOSFETs, vertical GaN devices, Si MOSFETs, and IGBTs have a vertical device structure where the current flows from the top of the chip to the bottom. Probing a chip from both the top and bottom is extremely challenging. Therefore, one side of the chip must be soldered. However, soldering and unsoldering the chip to a PCA (Printed Circuit Assembly) is inconvenient and accelerates board wear, making it less than ideal for testing.

Third, bare chips are physically fragile. Unbalanced forces during fixturing can easily cause cracks or chipping. Additionally, the small size of the chip — often less than 5mm on one side — makes handling even more difficult.



➤ Figure 1. Example bare chip (courtesy of Wolfspeed)

Fourth, bare chips can break due to voltage surges caused by the fast di/dt (rate of change of current) of the test signal, coupled with surrounding parasitic inductance.

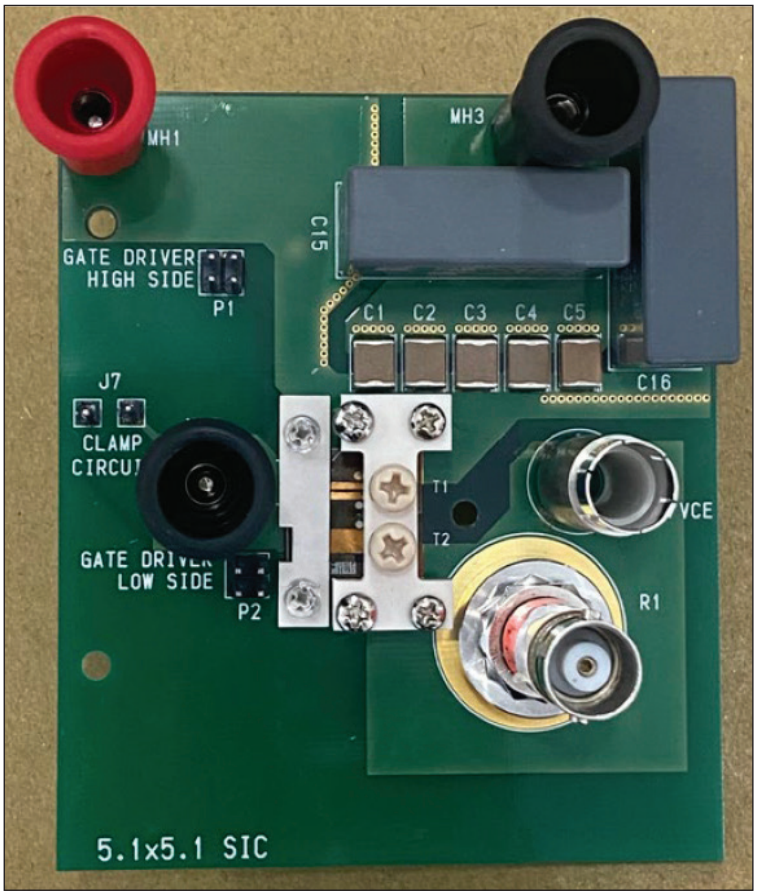
The only method currently used to characterize a bare chip is to create a complete Double Pulse Test (DPT) board for the chip. This board includes an integrated PCA with gate drivers, bank capacitors, isolation components, and other necessary elements. The chip is soldered to the PCA on the drain side, and wire bonding is used to establish connections to the source and gate. Often, the chip is coated with insulating material. However, this setup is employed only once for chip characterization because the PCB cannot be reused. The associated costs, time, effort, and lack of reusability discourage engineers from using it frequently.

Technologies enabling dynamic characterization of a bare chip

There are a few key technologies and know-how that are necessary to enable dynamic characterization of a bare chip. The creation of a special fixture for a bare die is the most important aspect of the solution. This special fixture must meet the following requirements:

- No probing needle should be used to avoid extra parasitic effects and the risk of arcing.
- The fixture must make contact with the vertical structure of the bare chip.
- Contact with the bare chip must be tight enough to ensure electrical conductivity but not too tight to avoid physical cracks or chipping.
- Solderless contact is desirable.
- A mechanism is needed to align a small bare chip with the electrodes on the test fixture.
- Parasitic effects in the test fixture should be minimized (e.g. < a few nH)
- The fixture should have high voltage and high current capabilities (e.g., 600 V and 40 A)

Additionally, there are several know-how techniques to accomplish this difficult task. For example, handling a bare chip gently is essential to avoid physical damage.



➤ Figure 2. Example PD1500A DUT board for dynamic characterization of a bare chip.

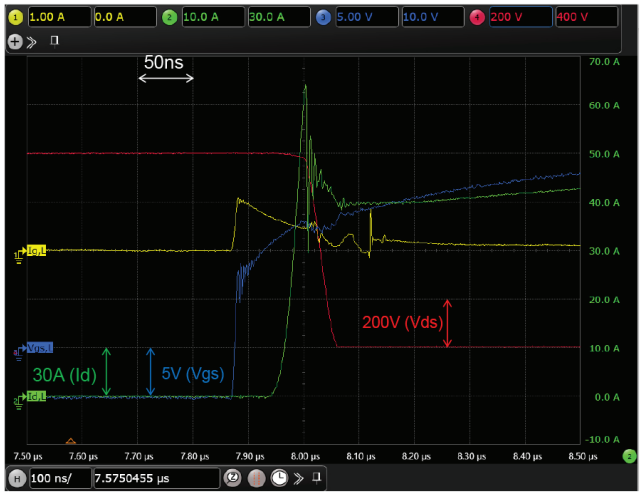
A solution for dynamic characterization of a bare chip

Keysight has two double pulse test systems: one is the PD1500A for discrete power devices, and the other is the PD1550A for both discrete power devices and power modules. The solution described below utilizes newly developed technologies

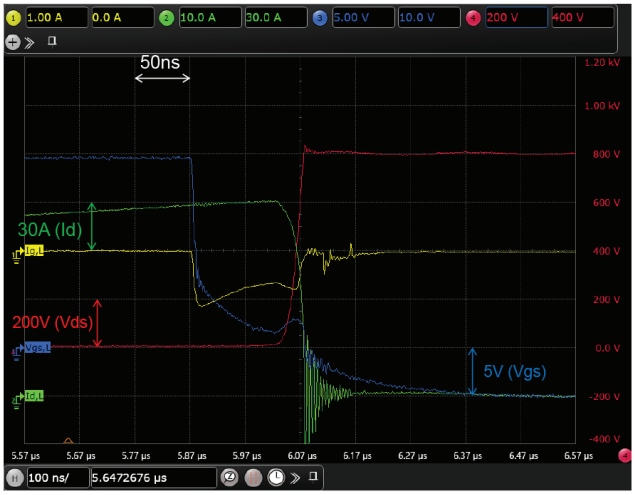
➤ Figure 3. Tailored bare chip DUT fixture for PD1500A/PD1550A.

Total Switching Energy	2.368E-03	J			
Turn On			**Turn Off**		
Turn On Delay, $t_{d(on)}$	137.3E-09	s	Turn Off Delay, $t_{d(off)}$	169.8E-09	s
Turn On Rise Time, t_r	39.86E-09	s	Turn Off Fall Time, t_f	29.22E-09	s
Turn On Time, t_{on}	177.2E-09	s	Turn Off Time, t_{off}	199.1E-09	s
Turn On Energy, e(on)	2.057E-03	J	Turn Off Energy e(off)	310.8E-06	J
di/dt (on)	1.541E09	A/s	di/dt (off)	3.127E09	A/s
dv/dt (on)	17.23E09	V/s	dv/dt (off)	32.24E09	V/s
Output Current Peak	64.24	A	Output Voltage Peak	832.6	V

Turn ON



Turn Off



Rg: Low 10ohm, High 0ohm

➤ Figure 4. Test results (turn-on & turn-off) for a SiC MOSFET.

for chip dynamic testing and is realized for the PD1500A. The DUT board is rather simple, as shown in Figure 2. The same technology can be leveraged for the PD1550A, allowing power module engineers to use it for characterizing bare chips and power modules with this new solution.

In the DUT board, special treatments are applied to the electrodes on the PCB to allow solderless contact. A flexible PCB with a similar electrode treatment is also used for top-side connections. By placing a chip between the main PCB and the flexible PCB, it becomes possible to flow current from the top of the chip to the bottom, enabling current measurements for vertical structure devices.

The PCB design aims to minimize parasitic inductance in both the power loop and gate loop. The fixture features carefully designed multiple pins protruding from the PCA, which align a bare chip precisely for optimal contact with the electrodes. The absence of probe needles further reduces parasitic inductance in the test circuit.

For Si and SiC devices, a coaxial shunt resistor can be used, even with its several nanohenry (nH) range of extra insertion inductance. In the case of GaN (Gallium Nitride) bare chips, Keysight's patented current sensor 1 provides an additional means to minimize parasitic inductance.

Power semiconductor bare chips typically exhibit different form factors. Therefore, our strategy involves creating a customized DUT board for both the PD1500A and PD1550A, as illustrated in Figure 3.

Figure 4 shows example measurement results taken for a 1.2 kV-rated SiC MOSFET bare chip. The test is performed at 800 V and 40 A, demonstrating that the fixture provides sufficient voltage and current capability for the 1.2 kV-rated SiC MOSFET. The waveforms are very clean, with a small Vds overshoot at turn-off. The calculated power loop inductance from the turn-on waveform is only 8.3 nH.

The fixture for bare chips can also be easily used with curve tracers such as the Keysight B1505A/B1506A. It eliminates the need to use a wafer prober for bare chip static measurements, greatly improving productivity.

Summary

Bare chip dynamic characterization, once regarded as very challenging and almost impossible to do, is now available through newly developed solution for Keysight PD1500 series double pulse testers. It is provided as tailor-made solution for a bare chip. There are many know-hows associated with the solution to perform the test safely and with minimized risks. For more information, contact your local Keysight representative.

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UK scientists to tackle AI's surging energy costs with atom-thin semiconductors

Queen Mary University of London will lead £6m initiative aimed at curbing data centre power use and reviving UK tech manufacturing

A team of UK scientists at Queen Mary University of London, University of Nottingham and University of Glasgow has received a £6 million EPSRC programme grant, "Enabling Net Zero and the AI Revolution with Ultra-Low Energy 2D Materials and Devices (NEED2D)." This will develop energy efficient, atomically-thin semiconductors to dramatically reduce the electricity demand from AI data centres and high-performance computing.

Led by Queen Mary University of London, the team will work in partnership with many manufacturers and several research institutions (> 20 partners contributing over £2million to the project) to develop new materials and prototype revolutionary low-energy-consumption electronic devices such as transistors. This will enable the UK to build a new electronics industry beyond traditional materials with innovative two-dimensional semiconductors.

Sir Colin Humphreys, Professor of Materials Science at Queen Mary University of London, who leads the project, said: "Governments around the world are spending billions building wind, solar, nuclear and gas power stations to meet the huge energy demands of AI data centres. Our approach is to tackle the problem at the source: by reducing the power these centres consume in the first place. To do this we will use the latest new materials, called two-dimensional materials, which are atomically thin. This will save over 90% of the energy required by data centres and computers, reduce the cost of electricity, and help to enable Net Zero."

AI's energy demands are growing at breakneck speed. The National Grid predicts that the electricity demand from UK data centres will increase sixfold by 2034, to 30% of total electricity used. This would cost £ billions and threaten climate goals. 2D semiconductors have emerged as a front-runner technology for building a more sustainable AI industry while also boosting the UK economy.

Colin Humphreys said: "Leading semiconductor industries including TSMC, Intel and Samsung have already recognised 2D materials as the future, placing them on their technology roadmaps for 2040. Our vision is to make the UK the world leader in ultra-low energy 2D devices well before 2040."

Beyond AI data centres, the 2D materials could be used to dramatically reduce the energy costs of other devices, including smartphones. "You will need to charge your mobile phone weekly instead of daily!" Colin Humphreys said. The new 2D materials being developed, including graphene and related compounds, carry electrical charge with far greater efficiency than silicon when scaled down to 2 dimensions; a future requirement for this technology. Electrons in these new materials can move much faster than in silicon, enabling ultra-low power computing and reducing heat waste. They are also ideal for miniaturisation, 3D stacking and new computing architectures like quantum and neuromorphic systems.

Amalia Patanè, Professor of Physics at the University of Nottingham and deputy project lead, said: "We are excited about the potential impact of our research and the project's comprehensive approach, spanning from computational modelling and materials synthesis to device fabrication and industrial engagement. 2D semiconductors behave in a fundamentally different way from their bulk (3D) counterparts and their unique electronic properties can support entirely new effects at the atomic scale. We will advance the precise engineering of 2D semiconductors, pushing the limits of what we can create, probe and exploit."

David Moran, Professor of Advanced Semiconductors at the University of Glasgow comments: "This is a truly exciting project that will utilise the extensive state of the art semiconductor fabrication and prototyping capabilities of the James Watt Nanofabrication Centre at University of Glasgow and complementary capabilities at Queen Mary and University of Nottingham to develop truly next generational low-power electronic devices and systems."

Queen Mary University of London, the University of Nottingham and the University of Glasgow are recognised globally as leaders in 2D materials and semiconductor research, with a world-class team pioneering breakthroughs in synthesis, characterisation and device integration. Colin Humphreys has also demonstrated the potential of graphene at industrial scale through his company Paragraf. This new project builds on those successes, going from basic science through to prototype devices, to enable the manufacture of complex semiconductor devices, such as transistors, made from new 2D materials.

The UK already has Europe's largest data centre market, with London as its central hub. Replacing energy-wasting silicon chips with low-power 2D transistors will help ensure the UK remains an attractive location for technology investment while proving the economic potential of the energy transition.

Bringing quantum communications to existing national-scale telecommunication infrastructure

Simple semiconductor technology replaces complex cryogenic components allowing quantum communications to be deployed to standard telecoms infrastructure - Technology deployed to colocation data centres and production fibre network in Germany.

TOSHIBA EUROPE has detailed the success of a world-first trial of its new coherent quantum communication technology, redefining the limits of secure communication while seamlessly integrated into standard telecom infrastructure. By using simple semiconductor technology instead of complex cryogenic components, this breakthrough unlocks new possibilities for sharing quantum-safe information across both national and international distances and paving the way for new quantum-enhanced applications. Advancements in quantum physics are promising unparalleled performance across a range of technologies, including computing power, secure communications and precision sensing.

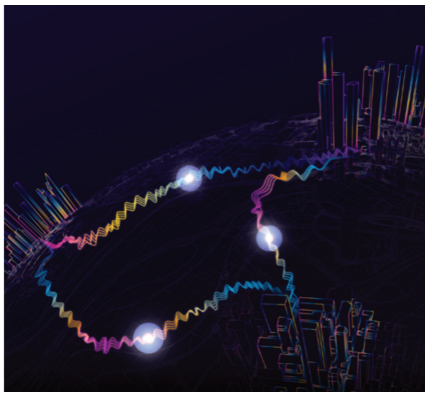
However, practical applications of quantum have remained challenging. Coherent quantum communications (quantum information encoded in the phase of light) can be scrambled by just a few metres of propagation along optical fibres, usually requiring a laboratory-grade cryogenically cooled detection system to provide stability. The cost and complexity of this cryogenic cooling technology means that organisations haven't been able to benefit from the rapid advancements in quantum physics in real-world applications.

Now, with this world-first trial by Toshiba, published in leading journal Nature, coherent quantum communications can be deployed on standard telecommunications infrastructure. The key breakthrough is a new system architecture that replaces unwieldy, complex cryogenic components with simple semiconductor-based devices. For the first time in a real-life deployment, quantum information encoded in the phase of a quantum light signal was shown to be perfectly stable, despite propagating over 250 km of deployed telecom fibre, using only off-the-shelf components and operating in a typical colocation data centre at room temperature.

A depiction of the network structure used during the world-first trial
Mirko Pittaluga, Lead Author of the study said, "Through this trial, we completely re-engineered the way that quantum information is measured and stabilised, with a unique optical configuration that completely eliminates the need for cryogenic lab-grade equipment". Robert Woodward, Team Leader at Toshiba Europe added "The key breakthrough was using semiconductor avalanche photodiodes. This hugely simplifies deployment and enables it to go from the lab to national and international networks."

Toshiba used this trial to demonstrate provably-secure communication over national-scale distances through its twin field quantum key distribution (QKD) protocol. QKD allows users to securely exchange confidential information (such as bank statements and health records) over an untrusted communication channel. Unlike other existing security solutions, the security of QKD derives directly from the laws of physics, meaning that it is secure against any future advancements in mathematics and computing (including the advent of quantum computers).

Toshiba invented the twin-field QKD protocol in 2018, a new technique that helps to extend the viable range of QKD, which is limited by fibre loss. Until now, however, twin-field QKD, as a form of coherent quantum communications, had remained limited to lab-based tests. This world-first breakthrough means that twin-field QKD, along with



other forms of coherent quantum communications, can start moving to real-life deployments across national and international networks, paving the way for widespread adoption of QKD for protecting operation-critical communications for businesses and governments.

Toshiba has led the way in quantum-safe technologies such as QKD since 1999, achieving a series of research world-firsts alongside commercialising the technology, such as through the opening of a quantum-safe communication network in London in partnership with BT, working with customers including leading banks like HSBC to deploy QKD, and partnering with companies like AWS and Equinix to further develop networking applications for QKD.

Andrew Shields, Vice President and Head of Quantum Technology at Toshiba Europe, said, "We are proud of the world-firsts we've achieved in QKD development and commercialisation at Toshiba. This trial represents another significant milestone in scaling QKD even further towards our end-goal of building a quantum internet that connects major cities and countries together, with quantum-safe protection at its core."

Boosting the blocking voltage of birectional HEMTs

3 kV monolithic bidirectional GaN HEMTs are promising candidates for 1200 V class and 1700 V class power converters

ENGINEERS from the University of Wisconsin-Madison are claiming to have raised the bar for the breakdown voltage of monolithic bidirectional GaN HEMTs to 3 kV.

This class of device, providing bidirectional current and bidirectional blocking capability, is a promising candidate for a number of novel power converters – including matrix converters, multi-level T-type inverters, current source inverters and solid-state circuit breakers – that could increase the efficiency of renewable energy infrastructure.

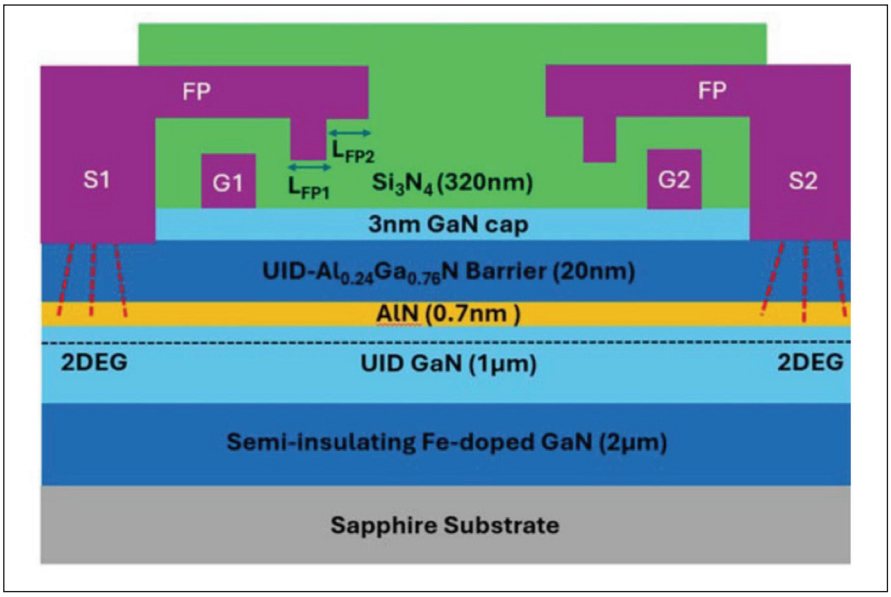
Spokesman for the team from Wisconsin-Madison, Md Tahmidul Alam, told *Compound Semiconductor* that the conventional approach to realising bidirectional functionality involves two transistors and two diodes.

One downside of this approach is a high resistance, caused by contributions to overall resistance from multiple components.

Additional issues stemming from the high device count include increased complexity and a compromised reliability. "If any of the four components fails, the entire system does not work," says Alam, adding: "Implementing the directional functionality with a single device reduces these complications."

The team from Wisconsin-Madison claims to be the first to break the 2 kV barrier for monolithic bidirectional GaN HEMTs, with 3 kV devices with an on-resistance of around just 20 Ω mm. By breaking through the 2 kV barrier, the team's devices are suitable for the construction of 1200 V class and 1700 V class power converters.

For power converters, normally-off transistors are preferred, as they can withstand accidental damage to the gate driving circuitry. While the team has used normally-on transistors in its latest work, these engineers argue that it is possible to apply similar concepts or designs to normally-off transistors when fabricating high-voltage devices.



Production of monolithic bidirectional GaN HEMTs began by loading a sapphire substrate into an MOCVD reactor and depositing a 2 µm-thick semi-insulating layer of GaN, followed by a 1 µm-thick unintentionally doped layer of GaN, a 0.7 nm-thick layer of AlN, a 20 nm-thick $Al_{0.24}Ga_{0.76}N$ barrier, and a 3 nm-thick GaN cap. The team selected sapphire over silicon for the substrate, so that they could reach blocking voltages beyond 2 kV.

Processing of the epiwafer into devices began by using lithography and metal deposition to form ohmic contacts. The next steps involved: a 750 nm deep mesa etch to isolate the devices; the addition of 200 nm-thick nickel gates; and surface passivation, realised by plasma-enhanced CVD of a 320 nm-thick layer of Si_3N_4.

The team produced a range of devices, differing in the lengths of the first and second field plates. The length of both of plates were varied from 1 µm to 3 µm.

Electrical measurements on the monolithic bidirectional HEMTs determined a stable threshold voltage of -3.25 V, a sub-threshold swing of 92 mV dec^{-1}, and an on-off ratio of more than 10^5. According to the team, the stable threshold voltage, low sub-threshold swing and high on-off ratio makes their device suitable for high-frequency operation with low conduction and switching losses.

For most devices with a first field plate length no longer than 2 µm, the team recorded a breakdown voltage of 3 kV, the tool limit. But longer first field plates led to a lower breakdown voltage, possibly resulting from an increase in the electric field strength under the field plates that causes a high impact ionisation rate.

Pulsed current-voltage measurements up to a 40 V off-state switching voltage, using a 100 µs pulse width, have determined that current collapse is less than 10 percent.

One of the next goals is to increase the breakdown voltage and/or decrease on-resistance. Another aim is to measure the switching performance of the transistors at high-voltages, such as 600 V.

REFERENCE
➤ M. T. Alam *et al*. Appl. Phys. Express **18** 016501 (2025)

Building better multi-channel Schottky barrier diodes

Stable ohmic contacts are enabling multi-channel AlN/GaN Schottky barrier diodes to start fulfilling their potential

RESEARCHERS from Singapore's Nanyang Technological University and its Agency for Science, Technology and Research are claiming to have provided the first successful demonstration of functional devices using multi-channel AlN/GaN heterostructures.

"While other groups have reported impressive results for epiwafers, the critical challenge has been transitioning from material to working devices," explains team spokesman, Hanchao Li, from Nanyang Technological University.

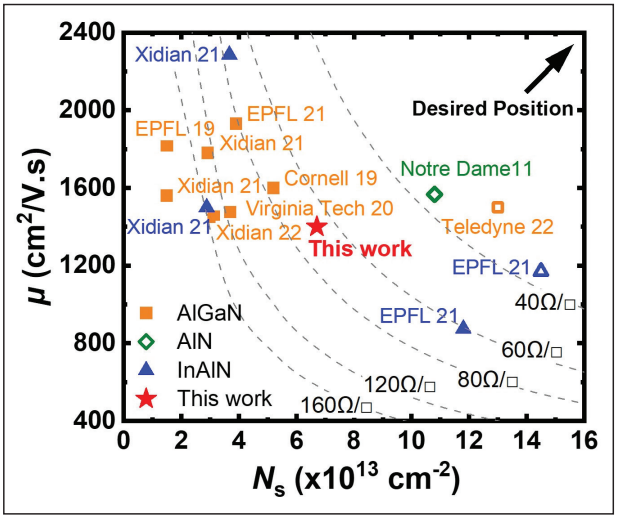
According to Li, a major breakthrough by their team has been the formation of stable ohmic contacts that avoid compromising the channel current in the Schottky barrier diodes. "This achievement is significant because the high aluminium composition and wide bandgap of aluminium nitride make ohmic contact formation particularly challenging in these heterostructures," added Li.

Over the last few years, there has been much interest in multi-channel GaN devices. Their appeal is overcoming the limited current conduction of devices with a single channel, and ultimately circumventing the trade-off between sheet charge density and mobility.

A number of research groups have produced multi-channel devices by pairing GaN with either AlGaN or InAlN. However, the team from Singapore prefers the combination of AlN and GaN. This duo provides a higher polarisation-induced charge density, allows for excellent electrostatic control of the channel in the vertical direction when a thin AlN barrier is employed, and enables excellent c
arrier confinement within the channels.

Fabrication of the team's diodes has involved outsourcing epiwafer growth to a commercial MOCVD facility. The reasoning behind this decision is to ensure stability and reproducibility in epitaxial growth.

"Given that device performance is highly sensitive to material quality, consistent and reliable epitaxial layers are crucial for our device development and optimisation process," argues Li.



Characterisation of the team's epiwafer, featuring five pairs of 4.9 nm-thick AlN barriers and 46.7 nm-thick GaN channels, reveals high-quality material growth. Scanning transmission electron uncovers sharp interfaces between the layers, and reciprocal space mapping produces well-defined, distinct peaks, indicating high-quality crystal growth.

To form diodes, Li and co-workers began by adding a cathode. To form this contact they applied an ohmic recess process, before adding Ti/Al/Ni/Au in this exposed region.

The next step involved adding an anode, with this Schottky contact formed by plasma etching that enabled a direct sidewall contact between the two-dimensional electron gas and the anode. Post-anode annealing under nitrogen gas recovered nitrogen vacancies caused by the etching process.

Using the transmission line method, the team determined an optimal ohmic etching depth of 180 nm, corresponding to the mid-point of the fourth channel. Etching deeper, through all five channels, led to an increase in resistance, rising from the optimal value of 0.38 Ω mm to 0.64 Ω mm. The team attributes the higher value to the limited effectiveness of sidewall contacts.

Electrical measurements determined a turn-on voltage of just 0.5 V. For a diode with a lateral anode-to-cathode distance of 3 μm, 1.1 V produces a forward current of 100 mA mm^{-1}, and current delivery can be as high as 1050 mA mm^{-1}.

Operating under reverse bias, the breakdown voltage – defined as the voltage where the current exceeds a 1 mA mm^{-1} threshold – is 104 V, 268 V and 422 V for anode-to-cathode distances of 3 μm, 5 μm and 20 μm, respectively.

These relatively low values are attributed to a combination of: an absence of electric field management structures, such as field plates and guard rinds, leading to a non-uniform electric field distribution and premature breakdown; and multiple cycles of AlN/GaN growth, which may introduce material quality issues that lead to increases in dislocation densities and interface states.

The team are now developing an approach for forming the ohmic contact that is based on the sputtering of GaN, and starting to investigate finFETs that are based on this epitaxial process. "We believe this could lead to enhanced device performance," remarks Li.

REFERENCE

➤ H. Li *et al*. Appl. Phys. Express **18** 016502 (2025)

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