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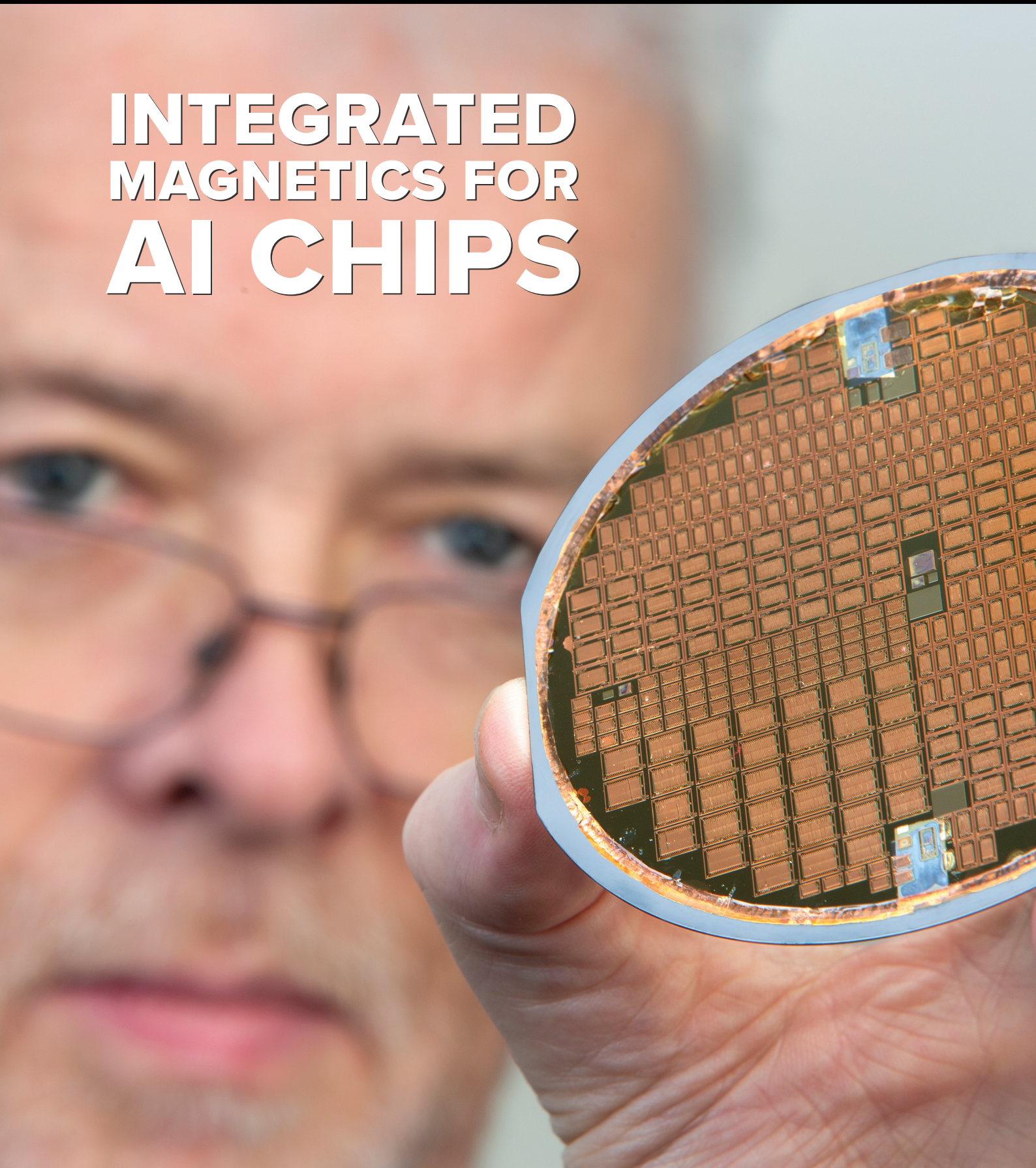

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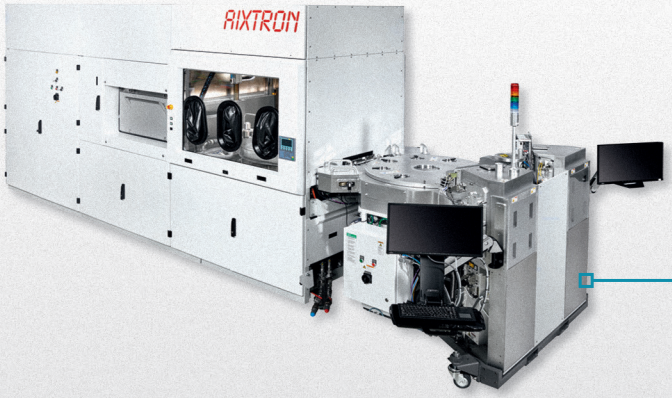

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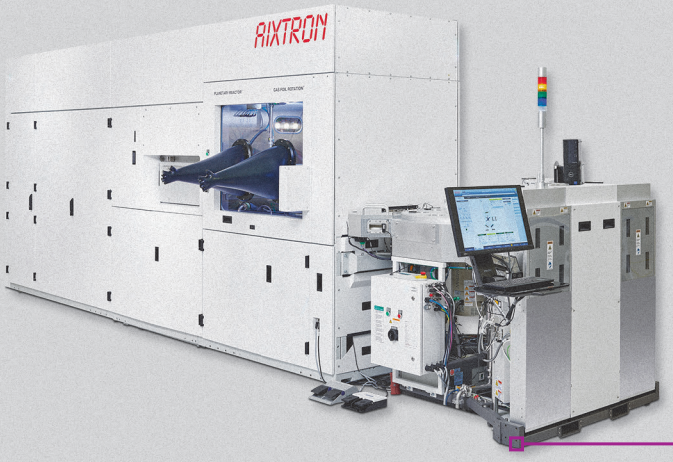

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VIEWPOINT

BY PHIL ALSOP
EDITOR

GaN's ascent, SiC's stumble?

The global semiconductor landscape seems to be undergoing a significant shift, with Gallium Nitride (GaN) emerging as a strategic front-runner while there appears to be a corresponding slowing in the momentum of Silicon Carbide (SiC).

Add in recent US reshoring investments and regional innovation hubs, and 2025 is proving to be a significant year for the industry's future.

GaN technology, once niche, has now solidified its status as a critical enabler for the next generation of power and RF applications. KnowMade's Q1 patent report reflects this momentum, documenting over 500 new GaN patent families. These filings, spanning gate design to advanced packaging, signal not just technical innovation but geopolitical positioning. Chinese players like Xidian University and Innoscience lead in filings, but the U.S. is responding with manufacturing muscle.

GlobalFoundries, for instance, just committed an additional $3 billion to GaN and photonics R&D, as part of a $16 billion initiative to onshore chip manufacturing with partners like Apple and SpaceX. Similarly, Texas Instruments is putting more than $60 billion into expanding US production, setting the record for the largest domestic semiconductor investment ever. These moves are as much about technological leadership as they are about national security and supply chain resilience.

Meanwhile, Singapore has launched its National GaN Innovation Centre, its first foundry capable of both GaN-on-Si and GaN-on-SiC wafer production. This gives the city-state a firm foothold in the future of semiconductors, especially as the industry veers toward higher frequencies and more power-dense applications like AI datacentres and satellite communications.

But while GaN surges, SiC is maybe facing some growing pains. Renesas seems to have abandoned its SiC chip production plans amid collapsing prices and an oversupply driven by aggressive Chinese competition (in fairness, something not too dissimilar is happening when it comes to GaN, as it seems that TSMC is planning to leave this space – seemingly reluctant to compete with Chinese competition). This follows signs of instability from Wolfspeed, once considered a SiC pioneer, now reportedly heading for bankruptcy. Although companies like Rohm are pushing ahead - its 4th-gen SiC MOSFETs are now in Toyota's new bZ5 EV – it seems fair to say that market volatility is forcing a rethink on how and where SiC fits in.

Radiation damage studies by ETH Zürich and ANSTO further underscore the technical limitations of SiC, particularly for space-based applications. Issues like single-event leakage currents threaten long-term reliability in extreme environments, complicating its value proposition against more robust GaN alternatives.

Strategic partnerships are now playing a crucial role in accelerating GaN's climb. Navitas has partnered with Taiwan's Powerchip to transition to high-volume 200mm GaN production, targeting fast-growing markets like AI infrastructure and EVs. Europe, too, is stepping up: Silvaco's collaboration with Fraunhofer ISIT aims to push the frontiers of GaN chip design through advanced simulation and co-optimization tools.

In this fast-evolving semiconductor race, GaN is no longer just the future - it's the present. Its rapid ascent, backed by patents, partnerships, and political capital, contrasts with SiC's progress, at least for now. As national governments, corporate giants, and research institutes converge on GaN innovation, the message is clear: the material war is far from over, but the momentum is unmistakably shifting.

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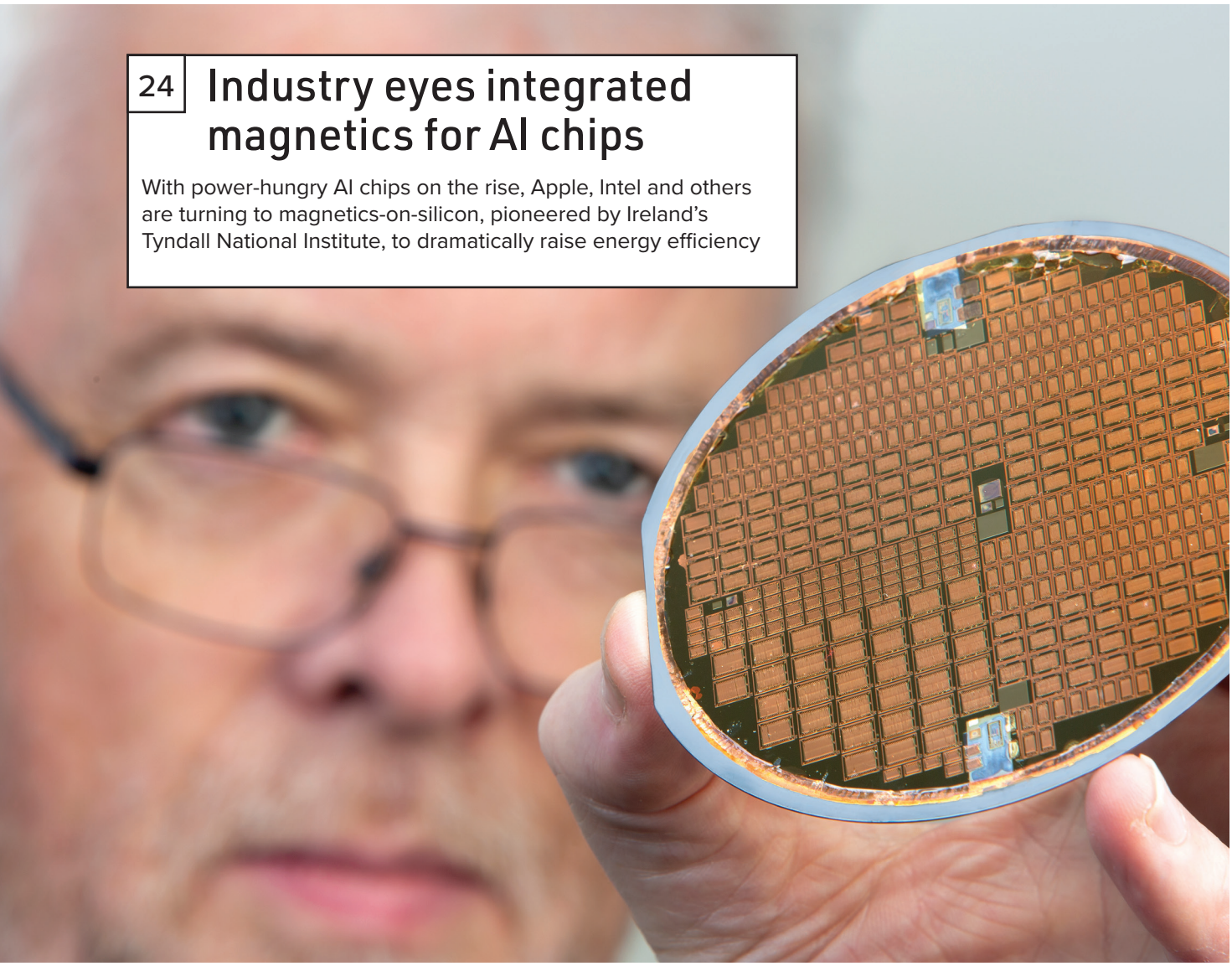

14

NEWS

10

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Editor
Phil Alsop
phil.alsop@angelbc.com
+44(0)7786084559

News Editor
Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Contributing Technical Writer
Rebecca Poole

Contributing Technical Editor
Richard Stevenson
richard.stevenson@angelbc.com
+44 (0)1923 690215

Sales & Marketing Manager
Shehzad Munshi
shehzad.munshi@angelbc.com
+44 (0)1923 690215

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Senior Event and Media Executive for Power Electronics International
James Cheriton
james.cheriton@angelbc.com
+44 (0)2476 718970

Publisher
Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

CEO Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

CTO Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Published by Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com W: angelbc.com

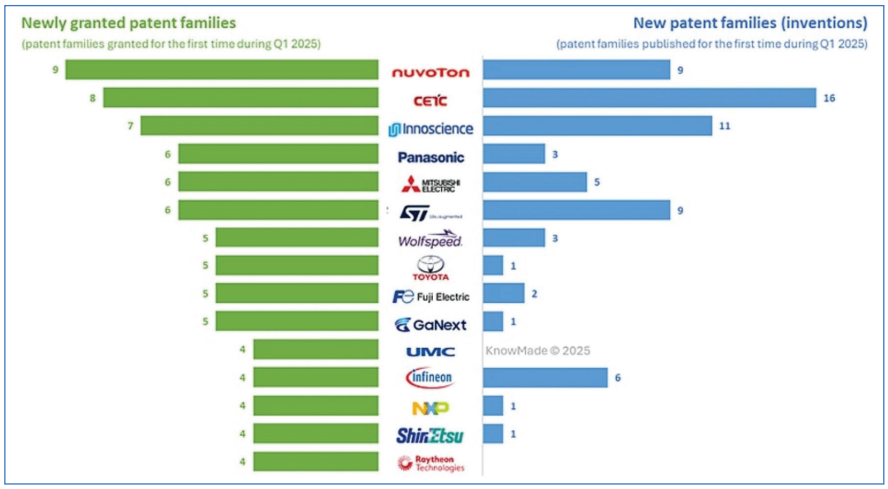
Angel BUSINESS COMMUNICATIONS

GaN companies strengthen patent portfolios

KnowMade Q1 IP patent report shows companies are addressing critical aspects of GaN technology.

KNOWMADE has published its Q1 2025 IP report on GaN electronics, highlighting robust patenting activity across both power and RF segments, amid on-going patent disputes between power GaN companies.

Recent patent filings emphasise critical aspects of power GaN technology such as gate design and packaging, resulting in sustained patent portfolio growth. Meanwhile, key RF market players keep expanding their IP activities in the RF GaN landscape, underlining the technology's role in next-generation wireless applications.



During the first quarter of 2025, a total of 540 new patent families were published, with Xidian University and major Chinese entities such as CETC and Innoscience leading the patent filings, followed by contributions from Nuvoton, STMicroelectronics, and Toshiba. Over 330 patent families were granted for the first time, notably reinforcing portfolios at Innoscience, STMicroelectronics, Infineon, Navitas, and EPC, alongside significant grants to Panasonic and TSMC. The quarter also saw more than 110 patents abandoned and over 70 patents expired, primarily from well-established patent holders including Wolfspeed, Infineon, and Fujitsu.

Approximately 10 IP collaborations (patent co-filings) were recorded, most partnerships formed between industry and academic organisations. For instance, Safran published a patent application with CNRS, CNAM and several universities in Paris, for an on-board aeronautical power circuit with active filtering. Also, Volkswagen cooperated with the University of Tennessee on GaN-based three-level active neutral point clamped power module designs, resulting in joint patent publications in Q1 2025. Nearly 40 patent transactions took place this quarter, predominantly within China, such as the transfer of several RF GaN patents from Xidian University to Huawei and power module company Macmic Science & Technology's acquisition of a GaN device patent from UESTC. In addition, a new lawsuit was initiated in February 2025 when Innoscience appealed to the US Court of Appeals to challenge the US International Trade Commission's ruling in last November on EPC's patent US 8,350,294.

Toshiba, Texas Instruments (TI), and Rohm each published more than six new inventions. In particular, Rohm introduced multiple innovations aimed at enhancing the reliability of normally-off GaN devices by leveraging *p*-GaN gate layer techniques and superlattice buffer structures. TI unveiled a novel gate structure incorporating a *p*-type poly-Si layer to decouple parasitic capacitances and improve gate depletion behavior, alongside trench-based substrate-to-source connections for GaN power devices and a HEMT design featuring a doped barrier to boost threshold voltage stability and drain current stability. Moreover, TI disclosed a packaging solution wherein a GaN FET is co-packaged with its driver for optimised half-bridge modules. Leading RF GaN Developments
Sony, Sumitomo Electric, and Macom disclosed six, five, and four RF-focused inventions, respectively. While Sumitomo Electric and Sony were focused on RF GaN device designs, Macom's patenting activity related to RF amplifier circuitry and advanced packaging techniques.

Interestingly, Sumitomo Electric focused on RF GaN-on-SiC devices fabricated on nitrogen-polarity GaN epitaxial structures. Academic research also made a significant contribution on this topic with UCSB publishing an invention that improves the linearity of deep-recess GaN MIS-HEMTs through corrugation of N-polar structures. MONDE Wireless, a UCSB spin-off, also mentioned N-polar GaN HEMTs grown on miscut substrates in another Q1-2025 patent publication.

New entrants to the GaN electronics IP landscape were predominantly Chinese, with LED manufacturer Anhui GaN Semiconductor filing several epiwafer patent applications for both power and RF uses, and battery manufacturer CATL submitting its first GaN-related invention targeting battery management systems.

GlobalFoundries boosts ‘re-shoring’ investment

Company commits to a further $3b on next-generation GaN tech, packaging innovation, and silicon photonics.

GLOBALFOUNDRIES says it is working with the Trump Administration, with support from tech companies Apple, SpaceX, AMD, Qualcomm, NXP and GM, to onshore critical components of the supply chain with a total $16 billion investment in expanding chip manufacturing and packaging across its facilities in New York and Vermont.

This latest announcement builds on the company’s existing US expansion plans of more than more than $13 billion funding to both advance manufacturing of 200mm GaN on silicon semiconductors at its facility in Essex Junction, Vermont; and for its recently launched New York Advanced Packaging and Photonics Center. GF is committing an additional $3 billion, which includes advanced research and development initiatives focused on next-generation GaN technologies, packaging innovation, and silicon photonics.

The company says its investment is a strategic response to the explosive growth in AI, which is accelerating demand for next-generation semiconductors designed for power efficiency and high-bandwidth performance across data centres, communications infrastructure and AI-enabled devices.

Tim Breen, CEO of GlobalFoundries said: “The AI revolution is driving strong, durable demand for GF’s technologies that enable tomorrow’s data centres – including GF’s leading silicon photonics, as well as GaN for power applications. Meanwhile at the edge, GF’s proprietary FDX technology is uniquely positioned to support AI functionality with low power consumption. With all these technologies and more manufactured right here in the US, GF is proud to play its part in accelerating America’s semiconductor leadership.”

“GlobalFoundries investment is a great example of the return of United States manufacturing for critical semiconductors,” said US Secretary of Commerce, Howard Lutnick. “President Trump has made it a fundamental objective to bring semiconductor manufacturing home to America. Our partnership with GlobalFoundries will secure US semiconductor foundry capacity and technology capabilities for future generations.”

“GlobalFoundries has supplied semiconductors for Apple products since 2010 and we’re excited to see them expand right here in the United States. These chips are an essential part of Apple products like iPhone, and they’re a powerful example of American manufacturing leadership,” said Tim Cook, Apple’s CEO Gwynne Shotwell, president and COO at SpaceX said: “Advanced semiconductors are critical to the advanced satellite capabilities which SpaceX has been pioneering for over two decades. We are excited by the expansion of GlobalFoundries’ manufacturing base right here in the US, which is core to Starlink’s growth and our commitment to manufacturing in the US, as well as our mission to deliver high-speed internet access to millions of people around the world.” “As a strategic supplier of Qualcomm, GlobalFoundries shares our vision for strengthening US chip production capacity. This commitment from GlobalFoundries will help secure a resilient semiconductor supply chain to support the next wave of US technology innovation, especially in areas vital to enabling power efficient computing, connectivity, and edge intelligence,” said Cristiano Amon, president and CEO of Qualcomm Incorporated “This collaboration allows us to scale efficiently, expand production in the US and continue delivering for our customers. It’s a strong step forward in building a resilient, high-performing semiconductor supply chain in the United States, ” said Kurt Sievers, CEO of NXP Semiconductors.

“Semiconductors are critical to the future of vehicles, and their importance will only grow. GlobalFoundries’ investment supports our work to secure a reliable, US-based chip supply – essential for delivering the safety, infotainment and features our customers expect,” said Mark Reuss, president of General Motors.

Texas Instruments to invest more than $60 billion in the US

More than $60 billion investment includes seven U.S. semiconductor fabs across three manufacturing mega-sites in Texas and Utah supporting more than 60,000 new US jobs.

Texas Instruments plans to invest more than $60 billion across seven U.S. semiconductor fabs, making this the largest investment in foundational semiconductor manufacturing in U.S. history.

Working with the Trump administration and building on the company's nearly 100-year legacy, TI is expanding its U.S. manufacturing capacity to supply the growing need for semiconductors that will advance critical innovations from vehicles to smartphones to data centers. Combined, TI's new manufacturing mega-sites in Texas and Utah will support more than 60,000 U.S. jobs.

"TI is building dependable, low-cost 300mm capacity at scale to deliver the analog and embedded processing chips that are vital for nearly every type of electronic system," said Haviv Ilan, president and CEO of Texas Instruments. "Leading U.S. companies such as Apple, Ford, Medtronic, NVIDIA and SpaceX rely on TI's world-class technology and manufacturing expertise, and we are honored to work alongside them and the U.S. government to unleash what's next in American innovation."

"For nearly a century, Texas Instruments has been a bedrock American company driving innovation in technology and manufacturing," said U.S. Secretary of Commerce, Howard Lutnick.

"President Trump has made it a priority to increase semiconductor manufacturing in America – including these foundational semiconductors that go into the electronics that people use every day. Our partnership with TI will support U.S. chip manufacturing for decades to come."

Today, TI is the largest foundational semiconductor manufacturer in the U.S., producing analog and embedded processing chips that are critical for smartphones, vehicles, data centers, satellites and nearly every other electronic device. In order to meet the steadily growing demand for these essential chips, TI is building on its legacy of technology leadership and expanding its U.S. manufacturing presence to help its customers pioneer the next wave of technological breakthroughs.

Renesas to abandon SiC production

Japanese giant halts SiC chip plans amid Chinese price war and Wolfspeed uncertainty.

RENESAS is abandoning plans to produce SiC chips for EVs. according to TrendForce, citing a report by Nikkei, This move by the Japanese semiconductor firm has apparently been prompted by slow growth in the EV market, coupled with a SiC chip supply glut driven by Chinese manufacturers. It follows news that Renesas' SiC partner Wolfspeed is preparing to file for Chapter 11 bankruptcy within weeks.

In July 2023, Renesas announced its entry to the power SiC market through a ten year partnership with Wolfspeed. The deal included a $2 billion deposit from Renasas to secure supply for both 150mm and 200mm SiC wafers.

Renesas had initially planned to begin manufacturing SiC power chips for EVs in early 2025 at its Takasaki plant in Gunma Prefecture. However, the company has since disbanded the SiC team at the facility, according to Nikkei. The latest research from TrendForce, shows weakening demand in the automotive and industrial sectors and slow shipment growth for SiC substrates in 2024.

Simultaneously, intensifying competition and sharp price declines have driven global revenue for N-type SiC substrates down 9 percent year-over-year to $1.04 billion.

Chinese vendors TanKeBlue and SICC have risen to prominence, capturing 17.3 percent and 17.1 percent of the global market share, respectively. Price competition with Chinese rivals is expected to intensify over the medium to long term, making it more difficult for a late arrival like Renesas to generate profits from SiC chip production.

TrendForce adds that while Renesas has reportedly decided to halt in-house production of SiC power chips, the company does not plan to exit the market entirely. Instead, it may continue to develop its own SiC designs while outsourcing manufacturing to foundries, then selling the finished products under its own brand.

Singapore opens GaN innovation centre

SINGAPORE has opened the National Semiconductor Translation and Innovation Centre for GaN; the country's first national facility dedicated to GaN semiconductors.

The centre addresses common challenges faced by companies and researchers – such as limited local access to advanced facilities and the need for closer collaboration. NSTIC (GaN) is the first facility in Singapore to host both 6-inch GaN-on-SiC and 8-inch GaN-on-silicon wafer fabrication lines.

It will also offer advanced GaN technology with gate lengths below 0.1µm and operation frequencies above 100GHz suitable for chips used in satcoms and a range of future communication and instrumentation technologies. NSTIC (GaN) will begin offering commercial foundry services from mid-2026.

First set up in 2023 as the National GaN Technology Centre (NGTC), NSTIC (GaN) is a partnership between the Agency for Science, Technology and Research (A*STAR), DSO National Laboratories (DSO), and Nanyang Technological University, Singapore (NTU Singapore).

NSTIC (GaN) is part of the broader National Semiconductor Translation and Innovation Centre (NSTIC) initiative led by A*STAR, which supports national efforts to deepen semiconductor R&D and innovation across priority domains such as photonics and advanced packaging.

The semiconductor industry contributes nearly 6 percent of GDP to Singapore's economy and supports around 35,000 skilled jobs across R&D, design, and advanced manufacturing.

"NSTIC (GaN) is not just a facility — it is a national platform for innovation and a catalyst for future technologies," said Cheong Chee Hoo, chairman of the NSTIC (GaN) Steering Committee. "Our goal is to build deep capabilities in GaN manufacturing and research, so that Singapore can help define the future of high-performance semiconductors."

Understanding the impact of radiation on SiC devices for space

ETH Zürich and ANSTO collaboration reveals mechanisms of single event leakage current radiation damage in MOSFETs and JBS diodes

THE FIRST results have been reported on a collaboration between ETH Zürich and Australia's Nuclear Science and Technology Organisation (ANSTO), looking at the impact of radiation on SiC devices for space.

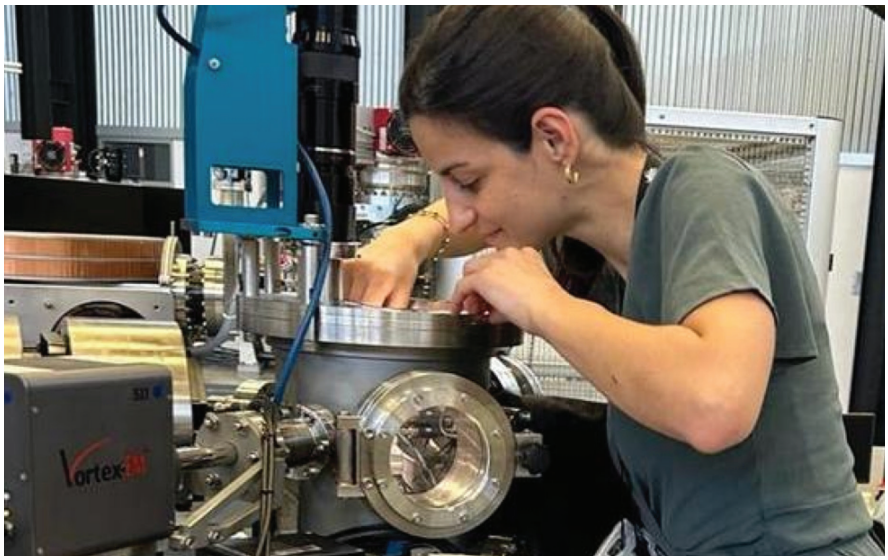
The results are covered in two articles both in IEEE Transactions on Nuclear Science. Corinna Martinella (pictured above), formerly a senior scientist at ETH Zurich, said in a LinkedIn post that the research advances an understanding of the basic mechanisms of radiation damage in SiC power devices exposed to heavy ions.

One paper describes how commercial SiC power devices, including MOSFETs and Junction Barrier Schottky (JBS) diodes, respond to space-like radiation at a microscopic level. By using a highly focused beam of particles at the Centre for Accelerator Science, that either travel deep or stay near the surface, Martinella and her team studied how different kinds of radiation affect the devices.

They found that short-range particles could cause a type of damage called single event leakage current (SELC) in both older and newer versions of these devices.

Monte Carlo simulations performed at ANSTO helped explain how particle depth affects the damage. In particular, when particles strike certain areas of a diode, they increase the electric field and trigger a chain reaction of ionisation, which may lead to lasting defects.

Some parts of the devices, such as the source and the gate metal lines showed no signs of damage. However, there were differences in how the devices reacted depending on whether the particle beam hit directly on the source pad or off to the side.



A protective polyimide layer reduced how deeply ions could penetrate in off-pad areas.

The second paper investigated the relation between single event effects (SEEs) caused by heavy-Ion Irradiation and defects in SiC devices.

First author student Helton De Medeiros used heavy-ion irradiation with different linear energy transfers and ion penetration ranges to investigate the radiation tolerance of SiC power diodes.

Single event leakage current degradation was observed for ion ranges shorter than the top crystalline layer. Other techniques were applied to explain the root cause of the observed radiation effects.

TSMC to exit GaN production

ACCORDING to various reports,Taiwanese chip giant TSMC will wind down its GaN wafer foundry services by July 31, 2027, with related production lines at its Hsinchu Science Park fabs ceasing operations.

The reason for the decision is thought to be rising price pressure from Chinese rivals.
TrendForce says that TSMC plans to repurpose its Hsinchu Fab 5, which handles GaN production, for advanced packaging.

By reusing existing cleanroom facilities, TSMC can accelerate expansion with minimal effort, addressing demand for Chip-on-Wafer-on-Substrate, Wafer-on-Wafer (WoW), and Wafer-Level System Integration (WLSI) technologies, the report says.

Navitas plans 200mm GaN production with PSMC

Partnership will support GaN's ramp into AI data centres, EVs, solar, and home appliances.

NAVITAS SEMICONDUCTOR has announced a strategic partnership with Powerchip Semiconductor Manufacturing Corporation (PSMC or Powerchip), to start production and continue development of 200mm GaN-on-silicon technology.

Navitas' GaN IC portfolio is expected to use Powerchip's 200mm in Fab 8B, located in Zhunan Science Park, Taiwan. The fab has been operational since 2019 and supports various high-volume manufacturing processes for GaN, ranging from micro-LEDs to RF GaN devices.

Powerchip's capabilities include an improved 180nm CMOS process, offering smaller and more advanced geometries, which bring improvements in performance, power efficiency, integration, and cost. "200mm GaN-on-silicon production on a 180nm process node enables us to continue innovating higher power density, faster, and more efficient devices while simultaneously improving cost, scale, and manufacturing yields", said Sid Sundaresan, SVP of WBG Technology Platforms at Navitas.

Powerchip is expected to manufacture Navitas' GaN portfolio with voltage ratings from 100V to 650V, supporting the growing demand for GaN for 48V infrastructure, including hyper-scale AI data centers and EVs. Qualification of initial devices is expected in Q4 2025. The 100V family is expected to start production first at Powerchip in 1H26, while the company expects 650V devices will transition from Navitas' existing supplier, TSMC, to Powerchip over the next 12-24 months.

Navitas recently made several announcements in the AI data center, EV, and solar markets, including its collaboration with NVIDIA to support GaN and SiC technologies for 800V HVDC architectures for 1 MW IT racks and beyond. Enphase announced that its next-generation IQ9 would include Navitas' 650 V bi-directional GaNFast ICs, and Changan Automobile announced its first commercial GaN-based OBC (on-board charger) using Navitas' GaNSafe technology.

"We are proud to partner with Powerchip to advance high-volume 200 mm GaN-on-silicon production and look forward to driving continued innovation together in the years ahead", said Gene Sheridan, CEO and co-founder of Navitas. "Through our partnership with Powerchip, we are well-positioned to drive sustained progress in product performance, technological evolution, and cost efficiency."

Toyota 'bZ5' uses Rohm SiC MOSFETs

TOYOTA is using a power module equipped with Rohm's 4th generation SiC MOSFET bare chip in the traction inverter of its new crossover BEV 'bZ5' aimed at the Chinese market.

The power module has started mass production shipments from Chinese module-maker Haimosic, a joint venture between Rohm and Zhenghai Group.

The bZ5 has a driving range of 550 km for the lower grade model and 630 km (CLTC mode) for the higher grade.

Reservations for the car began on April 22, 2025, the day before the opening of the 2025 Shanghai Motor Show, attracting significant attention.

Picture source: JustAnotherCarDesigner, CC0, via Wikimedia Commons

Rohm says it aims to complete the construction of the production line for the next-generation 5th generation SiC MOSFET by 2025, and is also accelerating the market introduction plans for the 6th and 7th generations.

Silvaco and Fraunhofer ISIT collaborate on GaN chip design

Project aims to explore and optimise the performance of GaN devices with greater depth and efficiency.

EDA company Silvaco has announced an R&D collaboration with Fraunhofer Institute for Silicon Technology (ISIT) to accelerate development of next-generation GaN devices.

Fraunhofer ISIT's Power Electronics division (which develops prototypes for power electronic and sensor systems) will use Silvaco's design tools — including the Victory TCAD platform, Utmost IV, and SmartSpice — to perform Design Technology Co-Optimisation (DTCO) for device development.

The idea is that Silvaco's DTCO platform will accelerate prototyping in Fraunhofer ISIT's post-CMOS process environment, which is set up to explore emerging processes for both GaN and MEMS technologies on 8-inch wafers. In addition, Silvaco's Victory Design of Experiments (DOE) solution will streamline development workflows and support rapid innovation during the evaluation of novel process modules and emerging device concepts.

"We are excited to expand our GaN design capabilities with Silvaco's Victory products," said Michael Mensing, head of the Advanced Devices Group at

Fraunhofer ISIT. "By using Silvaco's advanced TCAD solutions, our teams can explore, understand, and optimise the performance of GaN devices with greater depth and efficiency. Especially during our current development of high voltage lateral and vertical GaN devices based on engineering substrates, like Qromis Substrate Technology, we see many physical effects that require accurately calibrated process and device models.

This collaboration marks a significant step forward in strengthening Europe's semiconductor capabilities and driving the global evolution of GaN devices," said Eric Guichard, SVP and general manager of Silvaco's TCAD Division.

"Institutes like Fraunhofer ISIT are instrumental in pushing the boundaries of innovation in device and process technology. By collaborating with Fraunhofer ISIT, we not only accelerate their development efforts but also enhance our own TCAD tools to meet the demands of future device design."

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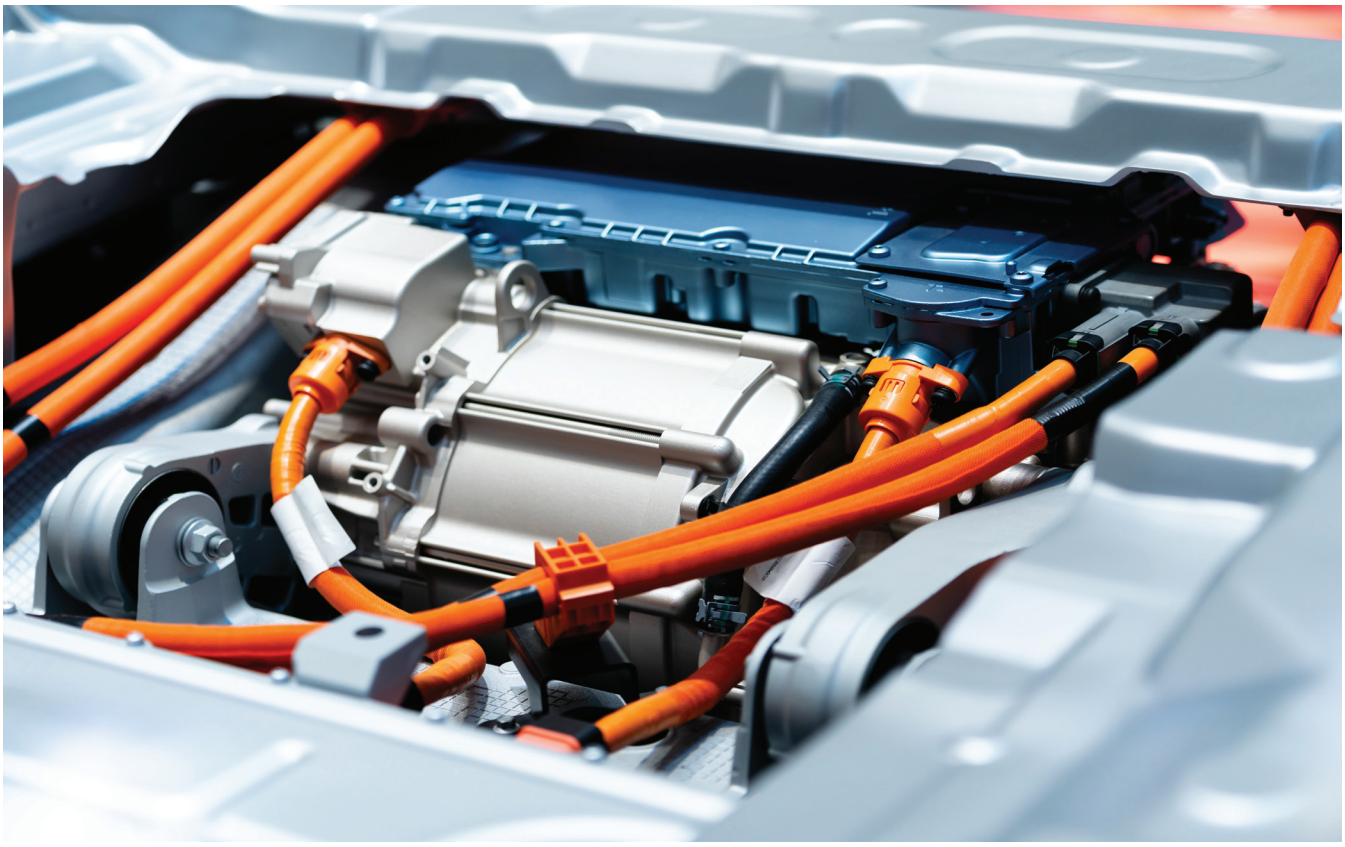


Smart GaN HEMT + IGBT = EV success?

Cambridge GaN Devices is targeting the powertrain of electric vehicles with the combination of IGBTs and its proprietary integrated circuit enhancement GaN technology.

BT RICHARD STEVENSON, EDITOR, CS MAGAZINE

TODAY'S DESIGNERS of power trains for electric vehicles face a difficult choice. Should they view cost as paramount and select silicon IGBTs; or should efficiency be the priority, and they deploy SiC MOSFETs? Whichever they choose, a significant compromise will be made.

But now there's the promise of a third way, pioneered by a handful of producers of GaN – they are claiming that they could offer products with a price close to that of silicon solutions, while delivering an efficiency similar to that of SiC, by pairing a GaN HEMT with a silicon transistor.

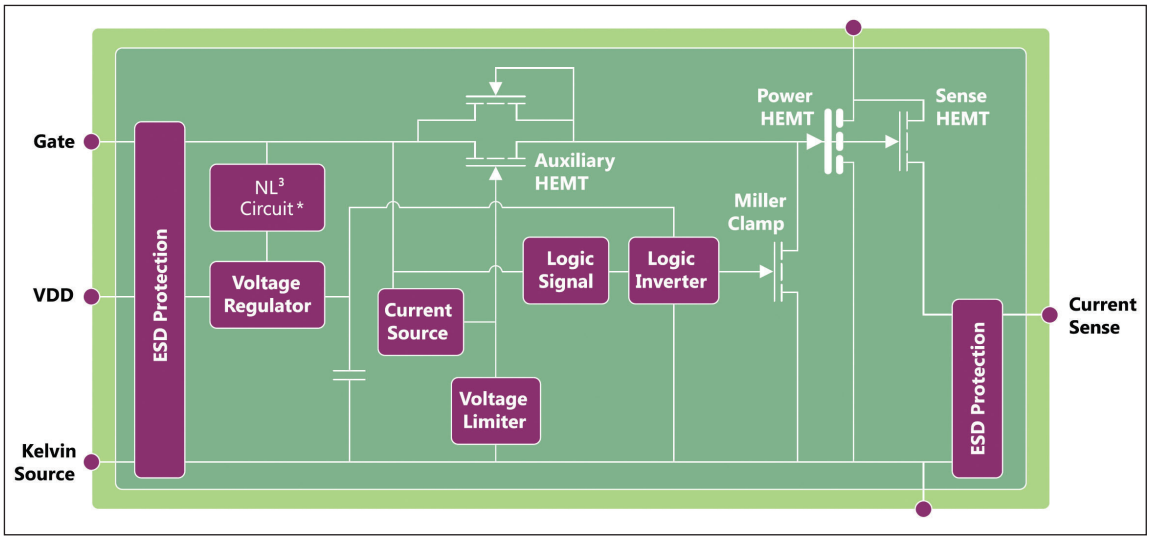
Amongst these trailblazers, Cambridge GaN Devices (CGD) claims that it is standing out from the crowd with its proprietary integrated circuit enhancement GaN technology, which it refers to as ICeGaN. The company is championing the combination of its 'intelligent' GaN HEMTs, which feature an enhancement-mode *p*-GaN HEMT rated at 650 V, and an IGBT. It's a patent-pending pairing with the moniker Combo ICeGaN.

According to Daniel Murphy, Director of Technical Marketing at CGD, the company's ICeGaN is its core technology, as well as its unique selling point. "This is what we're building the company around. The DNA of CGD, if you like."

One of the primary strengths of ICeGaN is that it provides ease of use. "You can essentially treat a GaN transistor like a MOSFET," says Murphy. Due to this, it's possible to use a very simple, low-cost driver to accompany the GaN HEMT.

Another great attribute of ICeGaN is that it facilitates zero-voltage switching, thanks to the inclusion of a Miller clamp. "There's no need for a negative voltage to be applied to switch the device," says Murphy, explaining that this refinement allows the driver to be simpler and cheaper. What's more, the Miller clamp ensures a very efficient turn-off of the GaN HEMT.

In addition to these valuable assets, absent in conventional GaN HEMTs, CGD's ICeGaN



➤ IceGaN is a form of smart power HEMT that features advanced sensing and protection capabilities.

technology has a slightly higher threshold voltage for the transistor.

"We've shifted it up to about three volts," says Murphy, explaining that this adjustment brings ICeGaN technology in line with standard silicon devices. "Hence, you can use standard silicon drivers."

The slight increase in threshold voltage also eliminates the danger of spurious turn-on.

With Combo IceGaN, higher efficiencies are realised by drawing on the complementary benefits of both classes of transistor.

"GaN comes into play at light loads, where you have very low switching losses. It brings increased efficiency," enthuses Murphy, who adds: "At high loads, and in some fault conditions, the robustness of the IGBT comes into play."

While the levels of efficiency provided by Combo IceGaN are not quite as high as they are with a full SiC solution, it provides a cost saving of around 40 percent to 50 percent, according to Murphy. And compared with only IGBTs, efficiency is 3 percent higher, based on measurements that consider the Worldwide Harmonised Light Vehicles Test Procedure cycle. "That obviously translates into either a less expensive battery or extended range," remarks Murphy.

As well as targeting the power train, CGD is pursuing opportunities in on-board chargers and DC-to-DC converters in electric vehicles, as well as industrial data centres, through the development of more innovative approaches. In this sector, power densities and power levels tend to increase year-on-year. "So, we're needing to improve the form factor all the time, and investigate different ways to address the packaging to meet the thermal requirements," says Murphy.

As all these applications involve very high power levels, the increase in chip area associated with additional features of ICeGaN, such as advanced sensing and the protection function, is relatively modest. Thanks to this, CGD is able to produce highly functional, competitively priced products.

Like many players in GaN power electronics, CGD is fabless, with chips produced at TSMC. This world-renowned Taiwanese foundry is responsible for the growth of epiwafers and their processing into devices. Packaging is undertaken at another partner, ASE.

As the Combo GaN technology can incorporate a range of IGBTs, CGD is planning to operate at the chip level within the supply chain. "We're looking for module partners, we're looking for car makers, tier ones that are interested to adopt this approach, and then we would support them with the sale of bare die," says Murphy.

One of the reasons why CGD is focusing on the traction inverter within the electric vehicle market is the volume of GaN that's required. "It is so much higher, because the power level is so much higher," claims Muphy, who adds that the other big draw is the substantial technical challenge. "We're a company with lots of smart people, and we're very ambitious. So that's why we're targeting traction."

Given the conservative nature of the automotive industry, it will take time for CGD to penetrate this market. The plan is to begin by launching discrete products for on-board chargers and DC-to-DC converters in 2026.

"The idea is for traction to try and enter a carmaker platform around 2028 timescale, and sooner than that with on-board chargers and DC-to-DCs," says Murphy.

So, while the makers of SiC MOSFETs are going to face stiff challenge from other wide bandgap devices, the competition is not going to begin immediately.

Infineon's expanding 2 kV portfolio

Joining Infineon's 2kV MOSFETs are Schottky barrier diodes with identical voltage ratings

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

HIGH ON THE AGENDA of many design engineers in increasing the electrical efficiency of their systems. Gains on this front trim carbon dioxide emissions and utility bills, while reducing heating, which simplifies thermal management and enhances reliability.

Today, two well-trodden routes may be taken to increase the efficiency of electrical systems. One of these proven pathways is to replace silicon power electronics with those that have a wider bandgap, as this reduces resistance. And the other common approach is to increase the voltage of the electrical system, and this enables a reduction in current and ohmic heating.

While both approaches pay dividends, rather than picking one over the other, it's better to adopt both practices. And helping to do just that is the trailblazer of the SiC Schottky barrier diode (SBD), Infineon Technologies: it added a 2kV SiC SBD last October, and has just introduced a sibling, rated at the same voltage and housed in a different package. This pair of diodes complement Infineon's 2 kV MOSFET, launched in March 2024.

➤ Infineon's 2kV SiC Schottky barrier diode in a TO-247-2 package majors on clearnace.

Infineon has been refining the SiC SBD for decades, having brought the first commercial device to market back in 2001. Major revisions to this diode since its debut include a new backside die metallisation and die attach technology, and more recently, the introduction of thin wafer technology, making an appearance in the fifth-generation portfolio. With these SBDs, the thickness of the die is slashed from 350 µm to just 110 µm.

In 2018, the European powerhouse introduced a sixth-generation of SiC SBDs, featuring an electrochemical barrier between the metal and semiconductor that reduces the knee voltage by around 0.1 volts.

"For 650 volts, this is a big advantage, but not so much for other blocking voltages," remarks Peter Friedrichs, Infineon's Vice President of SiC. "For that reason, Gen 6 remained at 650."

By offering fifth-generation 2 kV SiC SBDs in two different packages – initially TO-247PLUS-4-HCC, and now the TO-247-2 package – Infineon is giving design engineers the opportunity to select between a diode that majors on clearance and on creepage. The former metric is related to the physical distance between the pins, with a higher value reducing the chances of arcing, while creepage considers the conductance pathway along the package surface.

"[With the TO-247PLUS-4-HCC] there's an extra gap in the plastics that forms a longer creepage," says Friedrichs.

It's not clear which of the two variants will prove more popular. "We can scale both of them according to customer needs," says Friedrichs.

Infineon is mainly targeting two markets with its expanding portfolio of 2 kV power devices: the solar sector and the charging of electric vehicles.

To provide high-power, fast charging of electric vehicles, bus voltages as high as 1,500 V are employed. So, to ensure reliability in this application, power devices are ideally rated at 2 kV.

Within the solar market, one of the trends has been an increase in the output voltage of the panels. "Today, 1,500-volt panels are state-of-the-art, but there are already first solutions with 2 kV and even higher," says Friedrichs.

While it is theoretically possible to serve both these applications with silicon devices related at 2 kV, the electrical losses are unacceptable. So wide bandgap

By offering fifth-generation 2 kV SiC SBDs in two different packages – initially TO-247PLUS-4-HCC, and now the TO-247-2 package – Infineon is giving design engineers the opportunity to select between a diode that majors on clearance and on creepage

devices with a low voltage rating have been adopted, using what is referred to as a multi-level topology.

"You stack components with a lower blocking voltage in series to manage the higher voltage," explains Friedrichs, illustrating this point by suggesting that rather than using a 2 kV device, two 1.2 kV devices may be used in series. However, as well as doubling the number of devices, multi-level topology designs increase the complexity for controlling the circuit and magnify cost at the system level.

As one would expect, Infineon's 2 kV devices are more expensive than their 1.2 kV siblings.

"2 kV comes at a higher price, since we need a thicker epitaxial layer, a thick drift zone and a larger area. This, of course, contributes to cost, but it's still more affordable than putting two 1.2 kV in series," explains Friedrichs.

For SiC devices, the substrate accounts for a significant proportion of device cost, especially for SBDs, even though they are smaller than MOSFETs. However, substrates costs are falling, with a significant reduction in the last 12 to 15 months, according to Friedrichs.

For both of the applications that Infineon is targeting humidity is an issue, as electric vehicles and solar panels operate outdoors.

Friedrichs says that humidity is a particularly significant concern for solar applications, due to the low night-time temperatures that leads to condensation in the system. It's not possible to address these concerns with a perfect hermetic seal, and if moisture enters the power devices, this can impact long-term reliability.

Infineon has been aware of this issue for many years, having been supplying devices to makers of solar systems since 2010. "From that point onwards, we have integrated special measures to protect the silicon carbide chips against any moisture-related degradation," says Friedrichs.

Two sites for production of its SiC portfolio have been established by Infineon: Villach, Austria; and Kulim, Malaysia.

"In Kulim, we are just starting to ramp silicon carbide front-end production," says Friedrichs. "We start with the MOSFET. So, at the moment, all the diodes are produced in Villach."

But with demand for SiC power devices set to rise, it will potentially not be long before the Kulim fab is serving customers all around the world with a broad and expanding portfolio that includes high-voltage SBDs.

➤ Thanks to an extra gap in the plastics, the TO-247PLUS-4-HCC suits engineers requiring a high degree of creepage

Thermally conductive silicones

From electric vehicles (EVs) and electric bikes (e-bikes) to trucks and buses, demand for e-mobility solutions is rising.

BY LUC DUSART, MARKETING MANAGER FOR MOBILITY & TRANSPORTATION ELECTRONICS AT DOW

ACCORDING to the International Energy Agency (IEA), the global EV fleet is expected to grow 12-fold by 2035. Current and evolving e-mobility solutions depend on advances in power electronics that facilitate effective conversion and control of increasing amounts of electrical energy. E-mobility goals such as greater range and performance require new power electronics devices with higher efficiency, smaller formats and better thermal management properties. However, several factors present roadblocks to achieving these improvements. Advanced silicone-based materials can help address these challenges.

Managing heat, boosting reliability and streamlining production

When designers add more, and increasingly powerful components to printed circuit board (PCB) assemblies used in signal flow and power transfer, their additional generated heat can reduce the capacity, lifespan and performance of power electronics devices. Excessive heat can also increase the risk of thermal runaway in battery cells. These are two reasons why designers are seeking e-mobility materials, such as thermally conductive silicones, that can resolve heat-related issues with better thermal management. Designers are also looking for solutions to performance, safety and reliability concerns. For example, e-mobility power electronics applications like electronic control units (ECUs), inverters, converters and onboard chargers face environmental and mechanical challenges. Resistance to moisture, humidity, salt spray, shock and vibration is critical for e-mobility technologies that operate on roads or railways. Moisture, humidity and salt can lead to corrosion in PCB traces, while shock and vibration can cause solder joints to crack and PCB substrates to warp or bend.

There are also assembly issues to consider. Manufacturers of mass-produced e-mobility technologies such as EVs prefer materials that help facilitate high-volume production. For example, silicone-based materials can be applied quickly and precisely with automated mixing and dispensing equipment to reduce cycle times, labor costs and material waste. When curing is required, a material's curing method can also affect cycle times and operational expenses such as energy costs.

Advantages of advanced silicones

For thermal management, assembly and protection of electronic components, E-mobility designers have a choice of materials including silicone-based solutions and organics such as epoxies and urethanes. Compared to organics, advanced silicone-based materials provide important advantages. For example, silicones withstand higher temperatures than organics and provide longer-lasting heat resistance without a significant loss in mechanical properties.

Temperature fluctuations also pose a challenge for e-mobility power electronics. When materials used in PCB components have different coefficients of thermal expansion (CTEs), they expand and contract at

different rates. Advanced silicones can absorb some of the stress that results from inconsistent temperature changes. By contrast, epoxies and urethanes may crack because they have a higher modulus than silicones and relieve stress less effectively, due to their rigidity after curing.

With their low modulus, silicones can also absorb shock and vibration associated with operating an e-bike or EV. As mentioned previously, epoxies and urethanes are prone to cracking under stresses such as vibration. The hydrolytic stability of advanced silicones is also an advantage because it helps protect EVs from moisture related damage.

For productivity, silicones support high-volume, automated assembly and can cure at room temperature or with ultraviolet (UV) light instead of energy-intensive ovens. Dual-cure systems combine UV light with moisture to reach shadowed areas.

While epoxies and urethanes also support automated assembly and various curing methods, they cannot match silicones' other advantages.

Silicones offer a range of benefits for power electronics and one particularly beneficial application is thermal management. To leverage the benefits of these materials in thermal management, silicone materials are supplied in a variety of formulations and formats.

Thermally conductive silicones

Thermal conductivity (TC) is measured in Watts per meter Kelvin (W/m·K). Because air has a relatively low TC of 0.024 W/m·K, it is not efficient at dissipating heat from electronics. Therefore, filling the air gaps between heat sinks or heat spreaders and other components and substrates with a thermally conductive material is essential to optimize heat dissipation.

Silicones are inherently thermally insulating; however, with the addition of specialized fillers they can become thermally conductive. By conducting heat from power electronics, these silicones help prolong the life of power electronics, reduce energy consumption and prevent damage to surrounding components on a PCB. Depending on the application, operational requirements and preferred dispensing method, manufacturers can choose from silicone gap fillers, gels, greases/compounds, adhesives, and encapsulants.

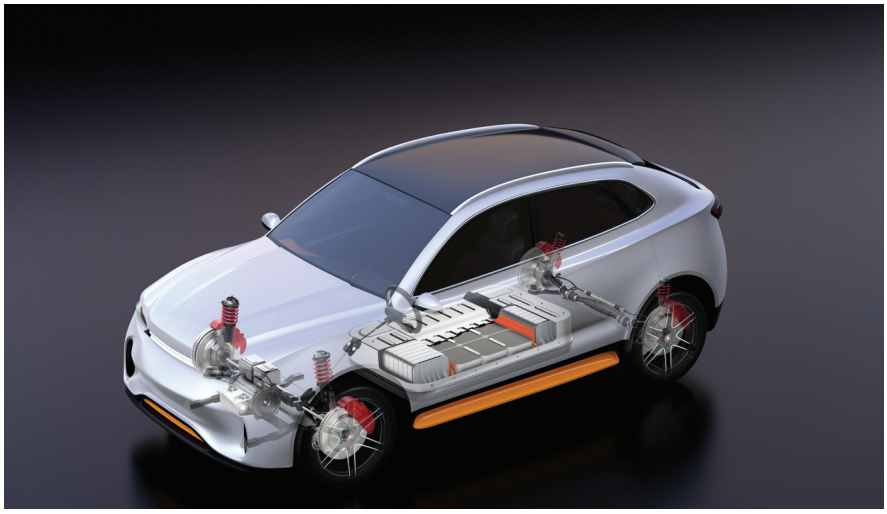
- **Gap Fillers:** Thermally conductive silicone gap fillers fill large gaps (0.5-5mm) between components on a PCB. These materials are available with a wide range of thermal conductivity values up to 12 W/mk. Some applications may need materials with a TC of 6 W/m·K, while other electronics may require a higher or lower TC.
- **Greases:** Thermally conductive silicone greases create a path between a heat source and a heat spreader. They are easy to dispense with automated equipment and do not require curing. These materials come in a range of thermal conductivities. Applications include heat dissipation from insulated-gate bipolar transistors (IGBTs) used with inverters. Importantly, thermally conductive silicone greases support thin bond lines for improved heat transfer.
- **Adhesives:** Thermally conductive silicone adhesives bond electronic components within a heat-generating assembly such as an ECU. They also are used to bond metal heat sinks to PCB substrates. They are available in one- and two-part formulations that are easy to dispense and can cure at room temperature. Thermally conductive silicone adhesives have TC values that range from 0.8 to 3.3 W/m·K.
- **Gels:** Thermally conductive silicone gels are highly conformable and reworkable, making them especially valuable for complex geometries of some e-mobility power electronics. These materials also have significantly lower viscosities than other thermally conductive products such as gap fillers because of their semi-solid state. Low viscosity makes gels easier to pump and mix, and flow more freely. Thermally conductive silicone gels cure at a wide range of temperatures and are easy to process.
- **Encapsulants:** Thermally conductive silicone encapsulants can cure at room temperature or with added heat. They flow easily and, after mixing, have viscosities ranging from 3,000 to 25,000 millipascal second (mPa·s). Products with a TC from 1.0 to 4 W/m·K are available. Applications include battery chargers where the small feature size of on-board-charger inductors need to be filled to ensure efficient heat transfer.

Other advanced silicone products

Unlike thermally conductive silicones, thermally insulating silicones prevent or reduce the spread of heat due to their low thermal conductivity and unique molecular structure. Some also meet specific flame ratings or provide electrical conductivity and shielding against electromagnetic interference (EMI).

As designers add more electronics to e-mobility vehicles, EMI shielding is becoming increasingly important because electronic noise or crosstalk can affect performance and safety.

Thermally insulating silicone products for e-mobility applications include encapsulants, conformal coatings, adhesives and greases.



- **Silicone Encapsulants** play a crucial role in protecting inverters, converters and e-motors from various environmental and operational hazards. They are also used with IGBT modules, high-voltage resistor packs, sensors, connectors, wires and LED lighting. These advanced silicone materials are waterproof, stress relieving, electrically insulating, vibration damping and flame resistant. Transparent silicone encapsulants also provide visibility of protected electronics during inspection or repair.
- **Silicone Conformal Coatings** are thin films that are applied to PCB substrates in one or more layers to resist moisture, dust, abrasion and mildew. Depending on their formulation, these materials may have UL94 V-0 or UL94 V-1 flame rating. Silicone conformal coatings are used in the automotive industry to replace potting or encapsulating materials that result in a brick-like structure, which can be bulky and heavy. By using conformal coatings instead, e-mobility designers can support light weighting without sacrificing performance.
- **Silicone Adhesives** are a broad category of materials with variations that are thermally insulating. They are used for assembly of inverters, converters, on-board battery chargers, e-motors and ECUs. Thixotropic silicone adhesives, featuring a thick, paste-like consistency, are used for gasketing, typically as lid seals or covers. Silicone adhesives with high tensile strength are recommended for e-mobility applications that need to resist significant pulling forces, such as power electronics that are subjected to significant vibrations. Another option is adhesive sealants, which combine strong bonding with reliable sealing. These are well suited for e-motors due to a combination of their chemical, thermal, and mechanical properties. Silicones can withstand extreme temperatures, they are excellent electrical insulators and their elasticity help absorb shocks and vibrations, reducing wear and tear on components.
- **Electrically conductive silicone Adhesives** can be used in several formats such as a die attach adhesive, EMI gasketing, and grounding adhesives to maintain electrical connection. Depending on the application the EC silicone can provide electrical connection across a wide range of application temperatures and over a wide variety temperature, both low and high. of The EMI shielding provided by electrically conductive silicone adhesives can protect sensitive e-mobility electronics across frequencies in the 1 KHz to 70 GHz range.
- **Silicone Greases** can provide thermal protection but may also be used for protection against electrical arcing and voltage drop. Such dielectric greases protect electrical connections from dirt, water, moisture and contaminants.

Importance of the right supplier

Finding the right materials for e-mobility power electronics is only part of any solution.

Partnering with a leading supplier can help designers improve e-mobility performance, reliability, safety and durability. Dow takes a collaborative approach to help customers advance e-mobility technologies.

Hands-on collaboration is paired with Dow's scientific research, data generation and testing under real-world conditions to ensure quality and reliability of silicone-based products.

By leveraging advanced silicones and support services, designers can confidently drive innovation in power electronics and shape the future of e-mobility.

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#UltraLowLosses

This compact, low-power receiver could give a boost to 5G smart devices

Researchers designed a tiny receiver chip that is more resilient to interference, which could enable smaller 5G “internet of things” devices with longer battery lives.

BY ADAM ZEWE, MIT NEWS

MIT researchers have designed a compact, low-power receiver for 5G-compatible smart devices that is about 30 times more resilient to a certain type of interference than some traditional wireless receivers.

The low-cost receiver would be ideal for battery-powered internet of things (IoT) devices like environmental sensors, smart thermostats, or other devices that need to run continuously for a long time, such as health wearables, smart cameras, or industrial monitoring sensors.

The researchers’ chip uses a passive filtering mechanism that consumes less than a milliwatt of static power while protecting both the input and output of the receiver’s amplifier from unwanted wireless signals that could jam the device.

Key to the new approach is a novel arrangement of precharged, stacked capacitors, which are connected by a network of tiny switches. These miniscule switches need much less power to be turned on and off than those typically used in IoT receivers. The receiver’s capacitor network and amplifier are carefully arranged to leverage a phenomenon in amplification that allows the chip to use much smaller capacitors than would typically be necessary.

“This receiver could help expand the capabilities of IoT gadgets. Smart devices like health monitors or industrial sensors could become smaller and have longer battery lives. They would also be more reliable in crowded radio environments, such as factory floors or smart city networks,” says Soroush Araei, an electrical engineering and computer science (EECS) graduate student at MIT and lead author of a paper on the receiver.

He is joined on the paper by Mohammad Barzgari, a postdoc in the MIT Research Laboratory of Electronics (RLE); Haibo Yang, an EECS graduate student; and senior author Negar Reiskarimian, the X-Window Consortium Career Development Assistant Professor in EECS at MIT and a member of the Microsystems Technology Laboratories and RLE. The research was recently presented at the IEEE Radio Frequency Integrated Circuits Symposium.

A new standard

A receiver acts as the intermediary between an IoT device and its environment. Its job is to detect and amplify a wireless signal, filter out any

> “Our chip also is very quiet, in terms of not polluting the airwaves. This comes from the fact that our switches are very small, so the amount of signal that can leak out of the antenna is also very small”

interference, and then convert it into digital data for processing.

Traditionally, IoT receivers operate on fixed frequencies and suppress interference using a single narrow-band filter, which is simple and inexpensive. But the new technical specifications of the 5G mobile network enable reduced-capability devices that are more affordable and energy-efficient. This opens a range of IoT applications to the faster data speeds and increased network capability of 5G. These next-generation IoT devices need receivers that can tune across a wide range of frequencies while still being cost-effective and low-power.

“This is extremely challenging because now we need to not only think about the power and cost of the receiver, but also flexibility to address numerous interferers that exist in the environment,” Araei says.

To reduce the size, cost, and power consumption of an IoT device, engineers can’t rely on the bulky, off-chip filters that are typically used in devices that operate on a wide frequency range.

One solution is to use a network of on-chip capacitors that can filter out unwanted signals. But these capacitor networks are prone to special type of signal noise known as harmonic interference.

In prior work, the MIT researchers developed a novel switch-capacitor network that targets these harmonic signals as early as possible in the receiver chain, filtering out unwanted signals before they are amplified and converted into digital bits for processing.

Shrinking the circuit

Here, they extended that approach by using the novel switch-capacitor network as the feedback path in an amplifier with negative gain. This configuration leverages the Miller effect, a phenomenon that enables small capacitors to behave like much larger ones.

“This trick lets us meet the filtering requirement for narrow-band IoT without physically large components, which drastically shrinks the size of the circuit,” Araei says.

Their receiver has an active area of less than 0.05 square millimeters. One challenge the researchers had to overcome was determining how to apply enough voltage to drive the switches while keeping the overall power supply of the chip at only 0.6 volts.

In the presence of interfering signals, such tiny switches can turn on and off in error, especially if the voltage required for switching is extremely low.

To address this, the researchers came up with a novel solution, using a special circuit technique called bootstrap clocking. This method boosts the control voltage just enough to ensure the switches operate reliably while using less power and fewer components than traditional clock boosting methods.

Taken together, these innovations enable the new receiver to consume less than a milliwatt of power while blocking about 30 times more harmonic interference than traditional IoT receivers.

“Our chip also is very quiet, in terms of not polluting the airwaves. This comes from the fact that our switches are very small, so the amount of signal that can leak out of the antenna is also very small,” Araei adds.

Because their receiver is smaller than traditional devices and relies on switches and precharged capacitors instead of more complex electronics, it could be more cost-effective to fabricate. In addition, since the receiver design can cover a wide range of signal frequencies, it could be implemented on a variety of current and future IoT devices. Now that they have developed this prototype, the researchers want to enable the receiver to operate without a dedicated power supply, perhaps by harvesting Wi-Fi or Bluetooth signals from the environment to power the chip. This research is supported, in part, by the National Science Foundation.

Industry eyes integrated magnetics for AI chips

With power-hungry AI chips on the rise, Apple, Intel and others are turning to magnetics-on-silicon, pioneered by Ireland's Tyndall National Institute, to dramatically raise energy efficiency

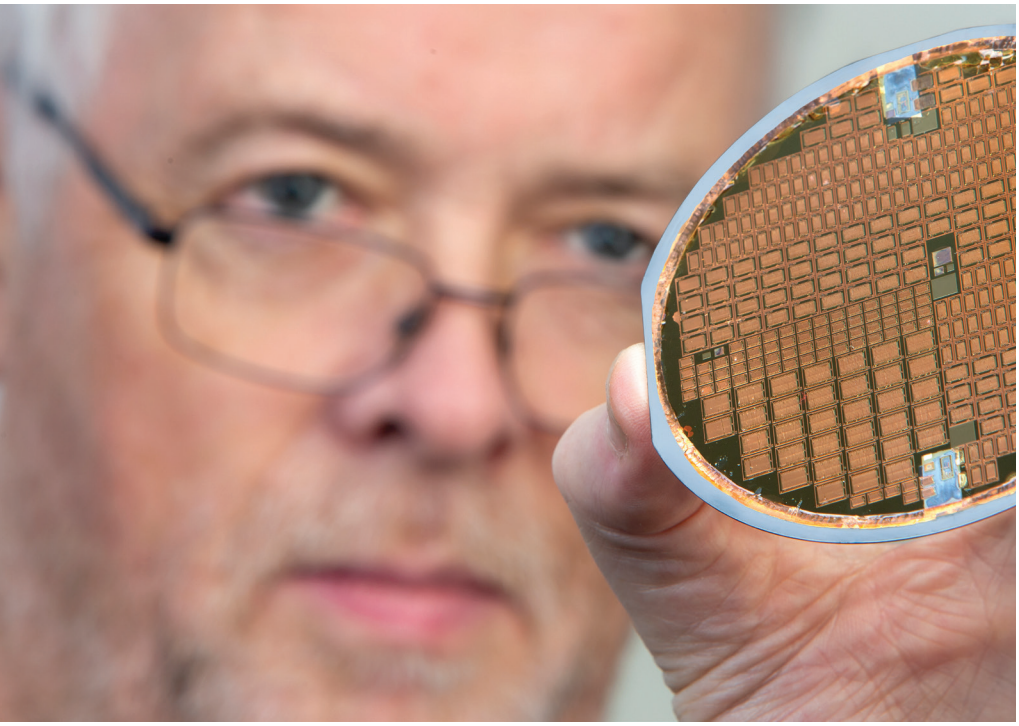
BY REBECCA POOL, TECHNICAL WRITER, PEW MAGAZINE

EARLIER THIS YEAR, Apple filed a US patent application for an inductor that uses magnetic films, designed to save board space and ultimately improve power supply efficiency in high performance portable computers.

The filing follows a series of applications relating to integrated magnetics on silicon spanning eight years, with listed inventors including Apple engineers as well as Professor Cian O'Mathuna, Director of Integrated Power and Energy Systems Research, and colleagues, at Ireland's Tyndall National Institute.

Such patent activity stems from nearly three-decades' worth of research on integrated magnetics at Tyndall, and comes at a time when the likes of Nvidia, AMD, Google and Intel are rolling out the hungriest of AI chips. Packed with hundreds of thousands - or more - processing units, vast on-chip memory and advanced interconnects, these chips easily eat up hundreds of watts, and then some, for massive parallel computations.

So how can integrating magnetics onto silicon chips help? It's largely about minimising the footprint and energy losses of DC-DC power supplies. Breakthroughs in both magnetic thin films on silicon and PCB-embedded magnetics have enabled the miniaturization of magnetic inductors that can replace bulky, wire-wound magnetic components. As O'Mathuna puts it: "For me, the best way to get the ultimate miniaturisation was always with integrated magnetics and magnetics-on-silicon technology."



➤ Professor Cian O'Mathuna is Director of Integrated Power and Energy Systems Research at Ireland's Tyndall National Institute. [Tyndall]

Smaller inductors can be integrated, alongside power management ICs (PMICs) and capacitors, onto a single chip, forming an advanced integrated voltage regulator or DC-DC converter. This serves as the final stage in the power supply system for a processor, and can be placed underneath the processor chip, either in the package substrate or embedded in the interposer, in a vertical configuration. Vertically integrating the power supply with the processor chip minimises parasitic losses and provides a faster transient response, dramatically enhancing the efficiency of power delivery. Critically, a large array of power supplies can deliver fast, efficient granular power, from directly beneath the compute die.

"When we build the inductor on silicon, we can make it really really small - we would even say we make the magnetics disappear onto the silicon chip, which is why we call this technology MagIC. We also have an array of inductors associated with an array of DC to DC converters," says O'Mathuna. "So now I can control the current going into each core or each part of the processor, while minimising interconnect losses."

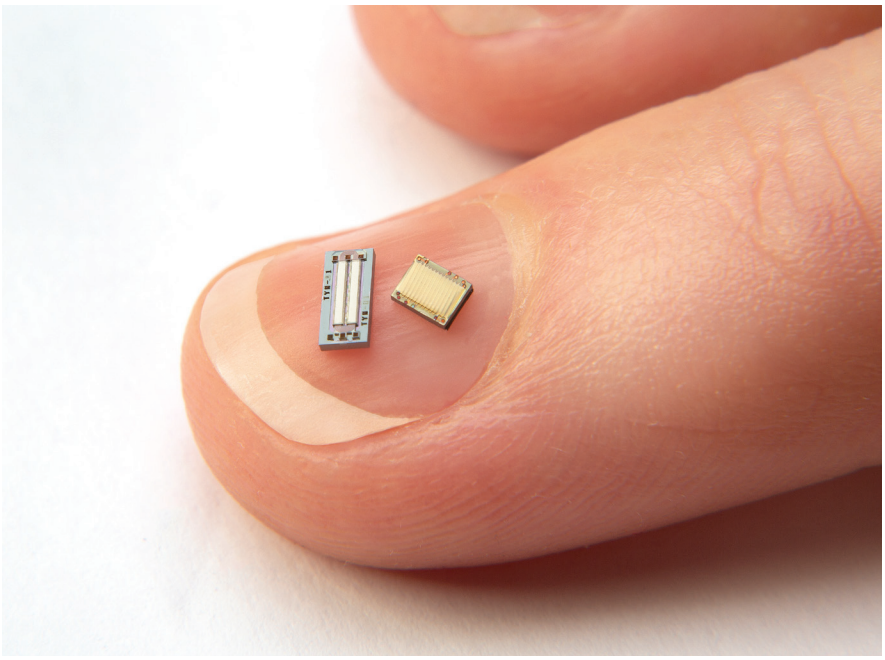
The Tyndall Director also believes an integrated magnetics approach makes manufacturing sense for the AI chips of tomorrow. “We’re introducing a new component but not a new manufacturing technology per se, as the magnetic disc-head industry has been using this type of technology for thirty years,” he points out. “So this is not a massive leap of faith.”

Indeed, integrated magnetics have already found their way into commercial chips, as part of a vertical power delivery set-up, to enable high performance computing. Intel, for one, has integrated coaxial magnetic composite core inductors to its processor chips. Meanwhile Apple uses magnetic thin-film inductor technology from TSMC. In late 2021, the tech-giant released its MacPro computers with an array of 140 integrated, thin-film coupled inductors fabricated on five silicon PMICs, which delivered vertical power to the processor, through the package substrate and interposer. According to reports, this integrated magnetics technology enabled Apple’s MacPro to last for 18 hours from a single battery charge, compared with between 6 to 9 hours for previous models. “We do hold a patent with Apple in this space,” confirms O’Mathuna.

Reaching out

At the start of this year, O’Mathuna and Tyndall colleagues were also granted a patent for a novel thin-film vertical inductor, again designed to boost power efficiency in AI applications. In the coming year, they will be working on proof-of-concept studies and then intend to licence the associated technology to Tyndall industry partners. This is an extension of their ongoing industry activities - various integrated magnetics technologies have already been licenced to multiple international companies.

While all license deals are confidential, Tyndall has published the results of collaborative research with many international companies including Global Foundries, Infineon, Intel, Murata (formerly IPDIA), Taiyo Yuden, Texas Instruments and Wurth Electronics. O’Mathuna highlights the Global Foundries silicon-based Ultimate Miniature Magnetic Inductors and Transformers (SUMMIT) platform. As part of this, 3mm^2 solenoid-type inductors and transformers can be monolithically integrated onto silicon substrates for power supply on chip (PwrSoC) DC/DC or integrated voltage regulator applications for AI accelerators and other high-performance computing systems. “Wurth Elektronic [Germany] has also been designing its own inductors, with fabrication through an external foundry, with some really impressive results,” he adds.



➤ Integrated magnetic chips fabricated at the Tyndall Institute. [Tyndall]

Along the way, chip inductor firms, including Taiyo Yuden, as well as Murata and TDK have also been developing their own high temperature magnetic materials for compact and very low profile PCB-embedded magnetics. For example, Taiyo Yuden’s LSCN series of multilayer power inductors has a thickness of only 0.2 to 0.3 mm, which according to O’Mathuna, meets the demands of high-end PCB suppliers, such as AT&S, Austria, keen to embed components in the circuit board. “You could imagine these companies saying; ‘So what can we do to stay competitive here - Intel is using soft magnetic composites in PCBs – could we put our inductors into the PCB? Yes we can but they need to be very thin,’” he says.

Other industry players, including Atlas Magnetics, Empower Semiconductor, Ferric and Texas Instruments, have taken a different approach, and have been manufacturing entire PMIC modules, (Power Supply in Package – PsiP), which include integrated magnetics. These modules typically include a small ASIC with multiple DC to DC converters and inductors, have a very low profile of some 0.6 mm, and are assembled using conventional surface mount assembly technology.

O’Mathuna highlights how Ferric, for one, manufactures a multi-phase output module and had previously been working with TSMC on thin film magnetics - but has since moved onto an alternative, undisclosed technology. “These companies set out to fit within the existing surface mount assembly supply chain and so developed PSiP modules,” points out O’Mathuna. “It’s pretty cool to see how [these companies] can get the power management, magnetics and possibly capacitors all into 0.6 mm thickness,” he says. “This indicates that there is a lot of innovative routes to creating integrated inductor solutions.”

Commercial moves

As more and more of their developments edge closer to commercialisation, Tyndall researchers continue to work with myriad magnetic materials. For example, as part of their magnetics-on-silicon development, they currently deposit thin films of cobalt-based and Fe-based alloys on silicon as well as cobalt-based thin magnetic films on vertical copper structures.

To drive magnetics-on-silicon fabrication forward, Tyndall researchers are currently part of the EU-funded FD-SOI FAMES Pilot Line, funded under the Chips for Europe initiative. With project partners CEA-LETI, in Grenoble, the researchers are developing a miniaturised DC-DC converter in which a PMIC and thin-film inductor will be flip-chipped or micro-transfer printed onto a high density trench capacitor interposer substrate. “For granular power, you could have a number of these chiplets in an array, so you can deliver power to multiple loads in a processor,” says O’Mathuna.

Apple processors developed by TSMC already have high density trench capacitors attached to the interposer. “With the Apple product, TSMC has demonstrated that it can put the magnetics on top of the silicon PMIC,” says O’Mathuna. “So I would suggest that the commercial application of FAMES technology, is not a million miles away – it could be three to five years away.”

O’Mathuna also highlights how global firms began to show significant interest in Tyndall’s magnetic-on-silicon technology more than a decade ago, prompting him and colleagues to start working on technology transfer.

“These companies had various levels of success in taking the technology forward – this isn’t an easy thing to do,” he says. “But now TSMC and Global Foundries have magnetics-on-silicon technology, it’s going to be much easier for the industry to progress.”
“You could say that after thirty years of research, magnetics-on-silicon has become an overnight success,” he adds.

> “We’ve got a complexity here that needs to be worked out in terms of who owns what, who’s going to be responsible for reliability issues that may arise in manufacture and whose problem is it”

Supply chain complexities

But is the integrated magnetic supply chain ready for commercial-scale manufacturing? Not quite yet. Right now, only a handful of firms are operating in the integrated magnetics-on-silicon, PCB-embedded magnetics, and PMIC/magnetics modules spaces. For example, only two industry players appear to be offering magnetic-on-silicon technology right now; TSMC in volume production and Global Foundries, which is currently sampling to customers.

O’Mathuna is well aware of the supply chain complexities that lie ahead, highlighting how magnetic components have yet to be built into the CAD EDA tools used by IC designers. “There is work to be done here... and who should be working on it? Should it be, say, TSMC?” he asks. “Or could the OSATs (Outsourced Semiconductor Assembly and Test) vendors do this? They take the wafers from companies and package them, so this could give them a significant competitive advantage to add integrated power delivery to their capabilities.”

He also points to Intel’s involvement in PCB embedded soft magnetic composites, and wonders if the technology is Intel-specific and therefore proprietary. “Even PCB embedding of chip inductors becomes complicated as you now have a package substrate but need to talk to the Taiyo Yudens of the world and ask them to work with a package substrate supplier on embedding the chip inductors,” he says. “We’ve got a complexity here that needs to be worked out in terms of who owns what, who’s going to be responsible for reliability issues that may arise in manufacture and whose problem is it?” Yet despite the complexities, O’Mathuna is optimistic that given recent industry developments, supply chain issues will be ironed out in the near-term. Reiterating how TSMC has Apple as its customer for magnetic thin-film inductor technology while Wurth Electronik’s interest in the technology can only drive business for the foundries, he asserts: “The future of integrated power is about making magnetics disappear.”

“All of these power companies are trying to get into the AI chiplet space and AI power delivery, and from a sustainability point of view you could save dramatic amounts of energy if you adopt a vertical power approach,” he says. “Some AI companies have said, we can do the power management chips but our problem is the magnetics... This is the bottleneck, which means there’s a big opportunity here.”

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Can an unassuming electrical component help unlock limitless energy?

The global push for clean, sustainable energy is driving efforts to unlock fusion as a transformative power source.

BY PETER MATTHEWS, TECHNICAL DIRECTOR, KNOWLES PRECISION DEVICES

NATIONAL LABORATORIES like the National Ignition Facility (NIF) and international megaprojects like ITER are advancing large-scale experiments. Meanwhile, start-ups are exploring their own innovative and cost-effective approaches. In the mix, high-voltage energy storage technologies like capacitors are emerging as critical enablers in advancing this breakthrough.

Unlike traditional fission, fusion produces nearly limitless energy with minimal long-lived radioactive waste by leveraging abundant fuel sources like hydrogen isotopes. Fusion's potential to combat climate change, while meeting the growing power demands of artificial intelligence and data centers, positions it as a transformative energy solution. Beyond these energy-intensive sectors, fusion could provide a more stable energy supply for the grid, reducing reliance on intermittent renewables. The pursuit of fusion is also driving innovation in plasma physics and materials science, fostering advancements that extend far beyond power generation.

How fusion (not fission) unlocks net positive energy

Fusion energy is grounded in the fundamental principles of nuclear physics and Albert Einstein's famous equation, $E=mc^2$, which demonstrates the relationship between mass and energy. Unlike nuclear fission, which splits heavy atomic nuclei, fusion combines light nuclei into a heavier nucleus. This process releases energy because the combined mass of the fused nucleus is less than the total mass of the individual nuclei. The "lost" mass is converted into the energy we're interested in.

The explanation lies in the nuclear binding energy curve, which shows that light elements, like hydrogen, release a lot of energy when joined, whereas heavier elements, like uranium, release energy when split. Fusion's ability to yield a net positive energy makes it an attractive candidate for meeting future green energy demands. In 2022, NIF achieved a major breakthrough in fusion energy by reaching fusion ignition, where the experiment

produced more energy from fusion than was used to initiate it. This milestone marked a pivotal step in showcasing fusion as a scalable energy source.

Strategies and challenges in plasma confinement for fusion

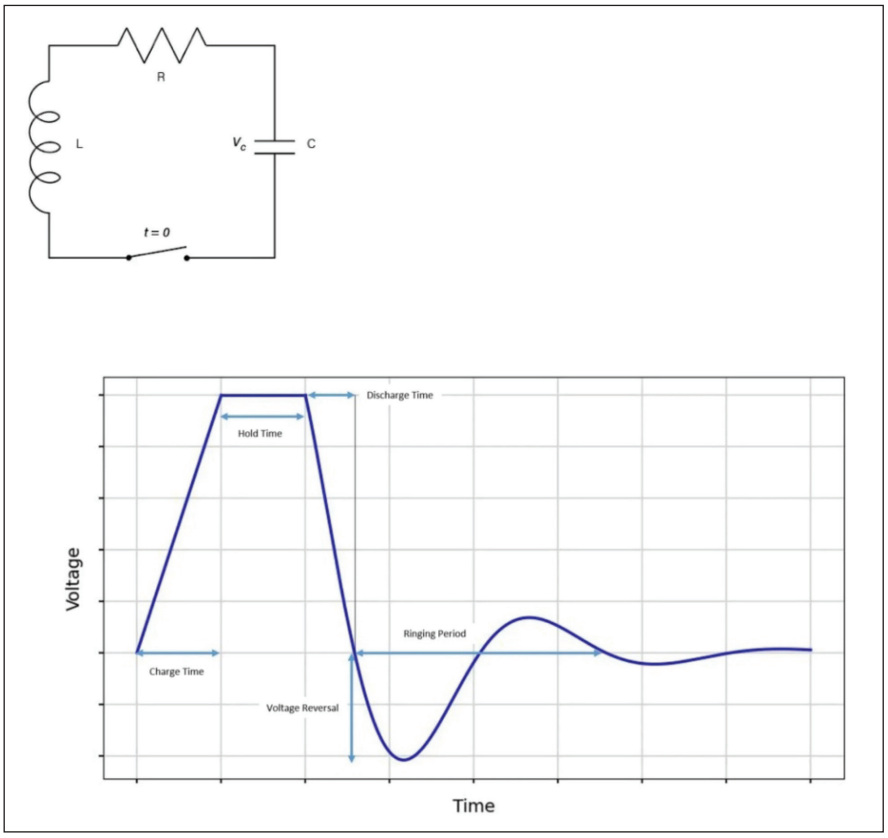
Confinement, a fundamental aspect of fusion experiments, involves maintaining precarious high-heat, high-pressure conditions for a naturally unstable state of matter: plasma. Physicists and engineers are tasked with overcoming the Coulomb Barrier, the energy barrier caused by the intense repulsion between two light nuclei when forced together. Physicists and engineers typically achieve this by applying concentrated, sustained pressure and high heat at the center of the fusion ignition chamber.

There are two main approaches to plasma confinement: magnetic and inertial. Magnetic confinement is made possible by strong magnetic fields that hold the hot, dense plasma in place. While effective if maintainable, the natural instability of plasma can cause it to shift or escape the magnetic fields. Inertial confinement requires compressing plasma from all sides, simultaneously. Even slight imperfections in compression can cause uneven heating and cooling. NIF, mentioned above, leveraged inertial confinement in their ignition experiments.

Capacitors in fusion energy experiments

Capacitors are indispensable components in fusion energy experiments, enabling the precise and powerful energy storage and rapid discharge needed to generate high-voltage pulses. Depending on the approach to confinement, these pulses drive pulsed laser beams or magnetic compression systems, which are central to achieving the extreme conditions required for fusion.

One of the ways physicists and engineers create high-energy pulses is with resistance, inductance, capacitance (RLC) circuits, shown in Figure 1. Examples include large capacitor banks like Marx Generators and Pulse Forming Networks. Marx Generators facilitate high voltage stacking to achieve high energy density by charging capacitors in parallel and discharging them in series. Pulse Forming Networks,



➤ Figure 1: A simple series RLC circuit (top left) and the charge, hold, and discharge profile of a capacitor (bottom).

which pair capacitors with inductors, enable precise control over pulse characteristics like discharge timing and energy levels.

The interplay between the resistance, inductance, and capacitance components determines the pulse rise time, duration, and energy delivery. Damping, influenced by the circuit's resistance, affects the voltage waveform during discharge, and by extension, the efficiency of energy transfer. By carefully adjusting the values of these components, engineers can shape pulses to meet specific requirements. Advancements in capacitor technology and switching mechanisms are pivotal to further fusion research and scale experiments.

Modern capacitor designs incorporate self-healing characteristics with metallized electrodes, which significantly extends their operational lifetime and enhances reliability. Highly engineered components can withstand over 10,000 charge/discharge cycles with reduced failure rates, making them ideal for these high-stress fusion environments.

High-voltage switches, such as gas-insulated and water-insulated self-break switches, complement capacitor functions. These switches ensure precise and efficient energy delivery during pulsed operations, further optimizing the performance of fusion energy systems.

To make fusion energy commercially viable, optimizing pulse performance is essential. Key areas of focus include improving energy efficiency, minimizing losses during discharge, and ensuring repeatable, consistent performance. Additionally, lowering the cost per joule of stored energy is critical to achieving economic scalability.

For continuous power generation, future fusion systems must achieve higher and more reliable repetition rates, supported by pulse architectures designed to maximize power density and precision. Capacitors are unsung heroes in this effort, serving as the backbone of fusion's intense energy bursts. The challenge now? Packing even more energy into these components to push fusion technology forward.

Vertical power takes centre stage on AI chips

As AI accelerators from AMD, Google, and Nvidia push beyond 1 kW power consumption, Empower Semiconductor is overhauling how power reaches these high-performance chips

BY REBECCA POOL, TECHNICAL WRITER, PEW MAGAZINE

IN June this year, a handful of integrated voltage regulator (IVR) manufacturers teamed up with US-based Marvell Technology - a frontrunner in custom silicon and SoC development - to optimize power delivery to AI and cloud infrastructure. Empower Semiconductor, US, was amongst these firms, and will now work on integrated power technologies for Marvell's silicon platforms.

Empower's IVR will be integrated underneath advanced processors to demonstrate how a vertical power delivery architecture can reduce power transmission losses, improve efficiency and provide a lightning-fast power delivery response – all with a view to satisfying the power-hungry XPUs of tomorrow. As CEO, Tim Phillips, points out: "With integrated voltage regulation, we're delivering power where it's needed – right at the point of load – with exceptional density, precision and efficiency."

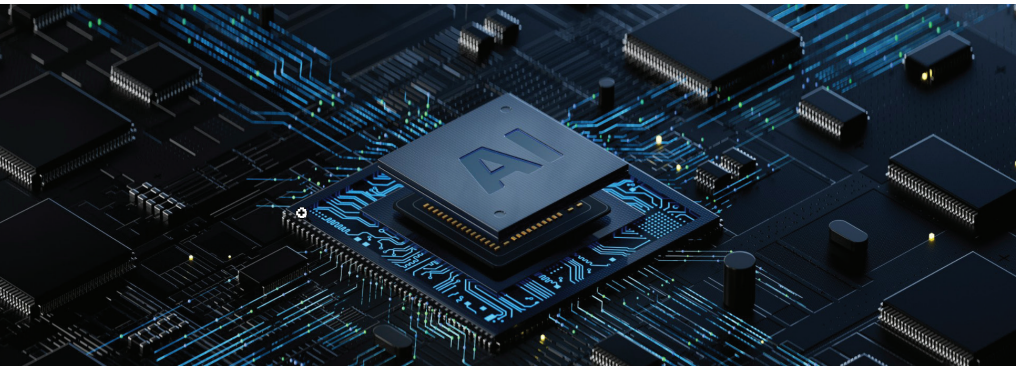
The collaboration is timely. Datacentre AI accelerators from the likes of Nvidia and AMD currently comprise more than 100 billion transistors, with these some of chips now guzzling more than 1kW of power. Not surprisingly, today's lateral power delivery architectures are struggling to meet these remarkable, and rising, power demands.

To deliver power efficiently, these traditional systems operate slowly, creating a large footprint of bulky power stages, capacitors and magnetics across the printed circuit board. Getting power across this 'last inch' results in substantial lateral transmission losses that will only get worse as chips consume more power.

What's more, in a lateral power delivery architecture, the further away the power components are from the processor, the noisier the voltage gets. To prevent noise from interfering with the power delivery, it's standard practice to use higher voltages – but that also wastes power. And this set-up doesn't get any easier with the massive voltage spikes and dips that accompany high density AI workloads.

This is where the latest IVRs can provide relief for AI chips. "IVRs are very small and have a great current density with great performance, so you can actually get the regulator itself very close to the AI chip," explains Phillips. "When you do this, you eliminate the entire transmission loss in the system – in an accelerator card right now, this can be 15 to 20% [of the power]."

The IVRs are designed to counteract voltage dips and peaks, delivering a cleaner, more stable output voltage. This also means the devices can reduce the relatively high operating voltages. "In an AI chip, power spikes up and down constantly from almost no load to full load, and keeping up with the speed of change has been a massive challenge," points out Phillips. According to the Empower CEO, the IVR chips run at very high frequency, imparting a fast transient response and high bandwidth to adjust the supply voltage of the load rapidly. "We eliminate a lot of these spikes in voltage, which helps with the throughput of the chip," he says. "So [the IVR] not only saves electricity, but allows the AI chip to perform better."



➤ Straight to the silicon: Empower Semiconductor has released an integrated voltage regulator that delivers power directly to the AI chip via a vertical architeuctre. [Empower]

Early days

Empower launched around ten years ago to build extremely dense power supplies, releasing several high-density power management IC, designed to

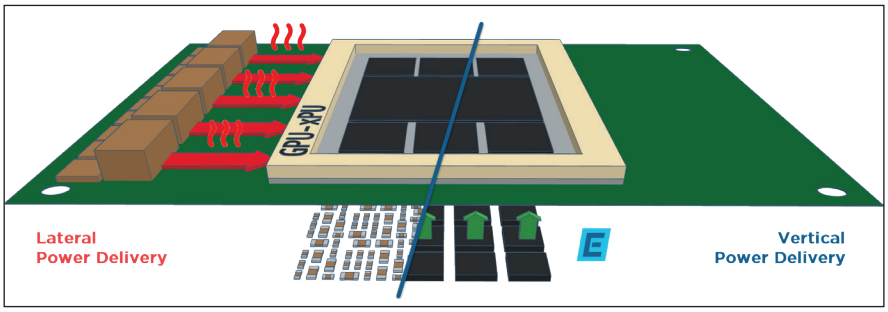
supply up to 30 W of power. However, according to Phillips, he and colleagues also realised that in high performance chips, ever-decreasing technology nodes were going to lead to higher current densities in processors, which would really strain power delivery. So development of the integrated voltage regulator semiconductor technology began. “We knew that at some point [this process] was going to break, so we said, ‘hey look, we need a clean sheet of paper’. How do I rethink the magnetics, the power and the architecture?” he recalls.

Come 2020, AI was in full swing, which Phillips reckons ‘changed everything’. “We knew AI was the perfect application for high-speed [integrated] voltage regulation technologies – it was like we’d found our Holy Grail,” he says. “So we pivoted the company and worked out how to scale [our developments] into a multi-kilowatt, scalable technology.”

Empower initially won $45 million in venture capital funds in 2021 to further develop its IVRs. Then in 2023, and with an extra $30 million finance in tow, volume production commenced. Today, the company has around 116 patents awarded or pending, and is shipping its vertical power platform, ‘Crescendo’, and associated technologies, to hyper-scalers.

Designed to handle the higher data rates and processing speeds of multi-kilowatt AI chips, Empower’s IVRs lie at the heart of Crescendo. To develop the vertical architecture - designed to meet the demands of 3000A processors - Empower started with its ‘FinFast’ power design. This technology repurposes FinFETs to operate at high speeds whilst also handling high currents and high power. The FinFast technology was combined with on-chip control logic to deliver IVRs that operate at very high frequency with low noise, whilst having very fast response times, said to be 1000 times greater than conventional converter technologies.

In parallel, Empower worked to integrate high-frequency magnetics into this vertical architecture whilst also replacing bulky, ceramic capacitors with wide-bandwidth silicon versions. (See pxx to learn how the Tyndall National Institute developed integrated magnetics.) Factor in the custom, thermally-resistant packaging designed for high frequency and high power operation, and you have Crescendo, which as Phillips points out is between 1 mm and 2 mm in height, an order of magnitude shorter than traditional DC to DC converters. Critically, the package is thin enough to fit underneath the processor, on the bottom-side of an accelerator card, and deliver high efficiency, vertically-coupled power to the AI chip.



Left: Lateral power delivery - a large footprint of bulky power stages, capacitors and magnetics deliver powers the printed circuit board. Right: Vertical power delivery – thin integrated voltage regulator packages are placed beneath the advanced processor to deliver power across a shorter distance. [Empower]

“The hardest thing was getting a piece of silicon to switch at very high speeds efficiently without generating a tonne of noise,” highlights Phillips. “You have to get the magnetics to match the silicon – those speeds have to align. And these have to be combined in a small, thermally-resistant package.”

“Part of the challenge has been to balance all of these needs,” he adds. “We did, and we can now regulate voltages and deliver currents in nanoseconds versus traditional power supplies that do this in several microseconds.”

Technology adoption

Phillips is certain vertical power delivery spells good news for hyper-scalers, rapidly scaling data infrastructure to accommodate the already massive workloads. As anticipated in the early 2020s, he asserts that high-end processors from Marvell and Nvidia have indeed ‘broken’ traditional, lateral power delivery architectures. “[Systems based on discrete subsystems] no longer work well enough for these advanced processors… This passive way to provide charge is just too slow and really hurts AI performance,” he says. Phillips also highlights how more and more industry players are adopting the technology. “A year and a half ago, adoption was zero, but today it’s about 10% in some [applications] and I think this will [continue] to move quickly, certainly over the next five year period,” he says.

“AI is really the first application that’s forcing the world to adopt vertical power,” he adds. “Without this, I think it would be difficult to hit the performance targets that hyper-scalers are looking for.”

So what now for Empower and vertical power delivery? Development will continue and the company’s roadmap plots a course that will provide up to 5000 A processors an even faster transient response for higher density workloads.

As Phillips puts it: “Sure, we’ve brought the technology a long way to get to this point… but that’s not actually good enough for [what hyper-scalers will face] five years from now, right?”

Phillips also points out how Marvell is just one of many firms that his company is collaborating on hyper-scaler, and HPC, challenges. “A power supply company can’t just sit back on its own now and develop technology,” he asserts. “I’d say that this challenge is so interlocked with the processor technology, the packaging technology and the memory technology, that it requires very close collaboration on all of these.”

“We really are changing the performance of the power supply to match the needs to the processor,” he adds. “This will take several years to hash it out, and a lot of innovation has to happen between that now and then.”

A step change in low-power circuit design

How the nPZero power-saving IC enables sensor system operation at the nanoamp level.

BY JAN FRODE BERGSØ, BUSINESS DEVELOPMENT MANAGER, NANOPOWER SEMICONDUCTOR

A MAJORITY of IoT devices are powered by primary battery cells, also known as non-rechargeable batteries, but limited battery life and the need to replace discharged batteries create numerous problems:

- The cost to maintain a battery power supply, and to replace a discharged battery. This is particularly problematic in commercial and industrial environments, in which a large number of sensors might need regular battery replacement.
- The risk of suspension of system operation in the interval between the failure of a discharged battery, and its replacement with a fresh battery.
- The cost and environmental damage attributable to disposal of a battery at the end of its life.

In battery-powered IoT systems, which typically include a wireless connection to the internet, a smartphone, or to a central control system, the device's RF system-on-chip (SoC) or microcontroller (MCU) is responsible for most of the energy consumption. Peripherals such as sensors also drain energy from the battery, but typically at a lower rate than the SoC does.

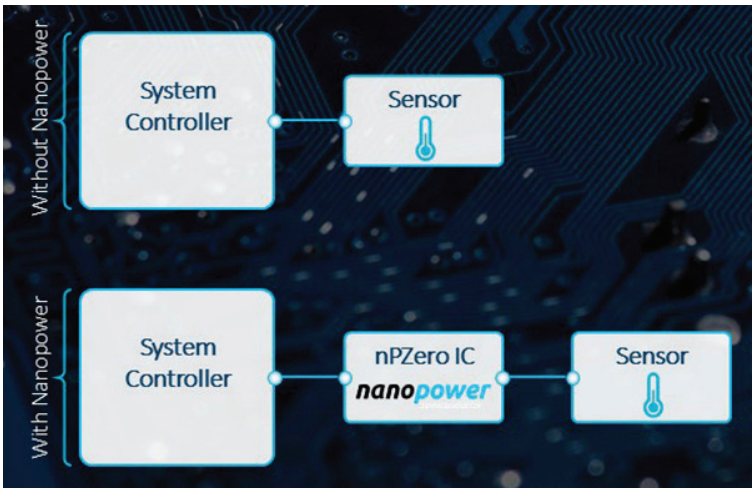


Figure 1. The nPZero IC operates as a companion chip to the SoC.

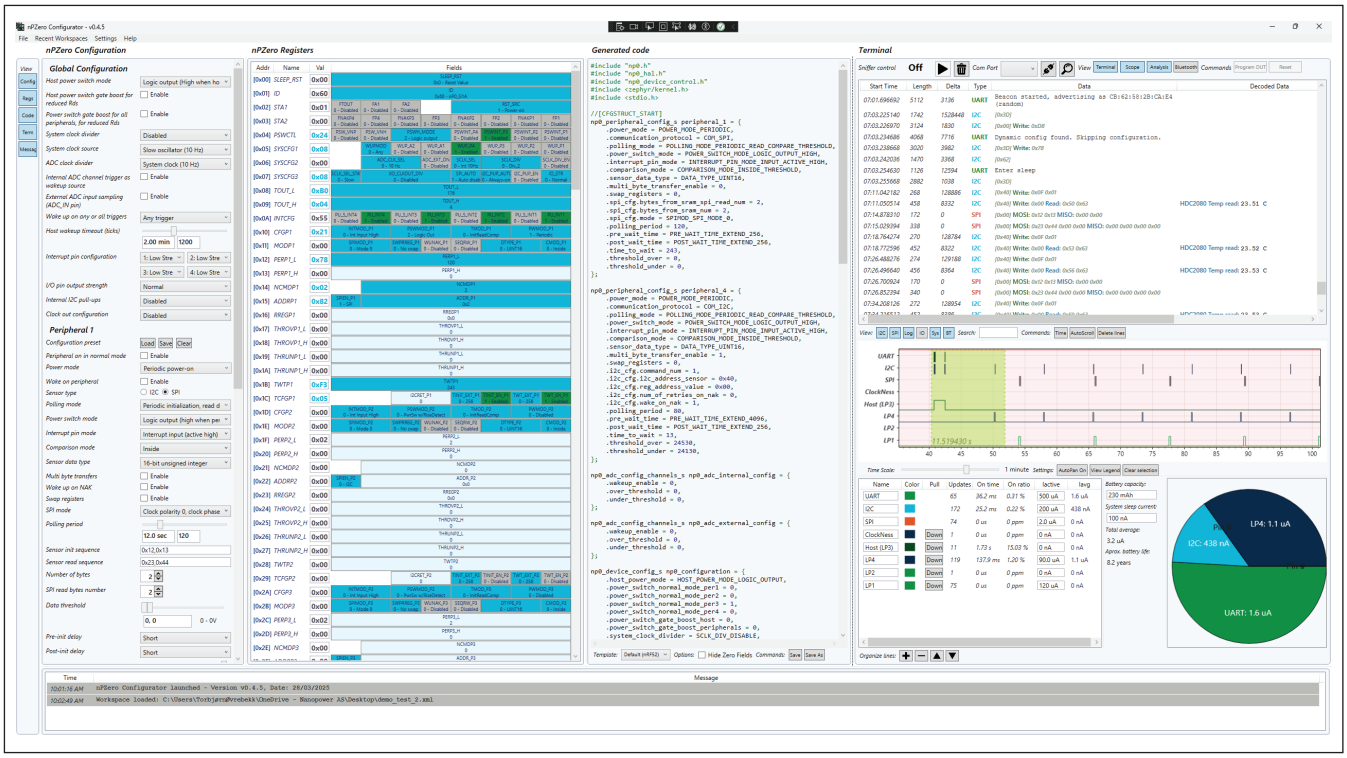
The power problem is inherent to a wireless SoC: the device needs a relatively high-performance, high-power compute system to handle the complex operation of a Bluetooth® Low Energy or similar radio protocol, as well as to perform control logic operations in response to significant sensor or user inputs. Yet in many applications, the full capability of this compute and communications circuitry is only deployed for a tiny fraction of the time. For more than, in some cases, 99% of the system's operating time, the host device is greatly over-specified for the quiescent-state operations it performs.

MCU manufacturers have put a lot of research and development effort into trying to reduce their products' power consumption in sleep mode, when the device is not performing communications or control operations. But there is a floor below which the power consumption of these big, sophisticated chips will not fall. And so embedded device manufacturers have previously had no choice but to build their power budget and to size their battery to cope with an SoC's high power consumption even when their application is doing nothing apart from periodically monitoring sensor values.

Now Nanopower Semiconductor has developed a dedicated power-saving chip, a companion to the SoC, which reduces average system power consumption in typical endpoint wireless IoT devices by up to 90%.

Finding a way to turn off the SoC

If the problem is the power consumed by the SoC when it is running, even in sleep mode, a solution



➤ Figure 2. The zero-code tool for configuring the nPZero's operation features an intuitive GUI

might be found in switching off the SoC entirely. This is the theory behind the introduction of a new type of power-saving IC, a device which can perform the functions that the SoC performs when it is not active, but at a small fraction of the SoC's power consumption.

This concept of this power-saving IC has been developed by European start-up company Nanopower Semiconductor, and has been implemented in its first-generation nPZero product.

The nPZero is compatible with most SoCs and sensors on the market (see Figure 1). In an IoT endpoint device comprised of one or more sensors and other peripherals, the nPZero takes over sensor monitoring and system control functions between radio transmissions or trigger events, enabling the SoC to shut down completely until a threshold event occurs that requires the nPZero to wake up the SoC and hand over control to it.

Thanks to the implementation of innovative sub-threshold mixed-signal technology developed by Nanopower, the nPZero draws less than 100nA when actively monitoring and controlling sensors.

Nanopower has proved the potential of the nPZero to make system power savings in typical IoT device designs of between 50% and 90%. This results in:

- Greatly extended battery life, reducing replacement frequency and cost
- The option to reduce battery size, allowing for more compact device designs
- The potential for battery-free operation. The Nanopower power-saving technology can enable the addition of a harvested energy source, eliminating the risk of battery power failure, or even enable a system to run on harvested energy alone.

How the nPZero minimizes power consumption in the quiescent state

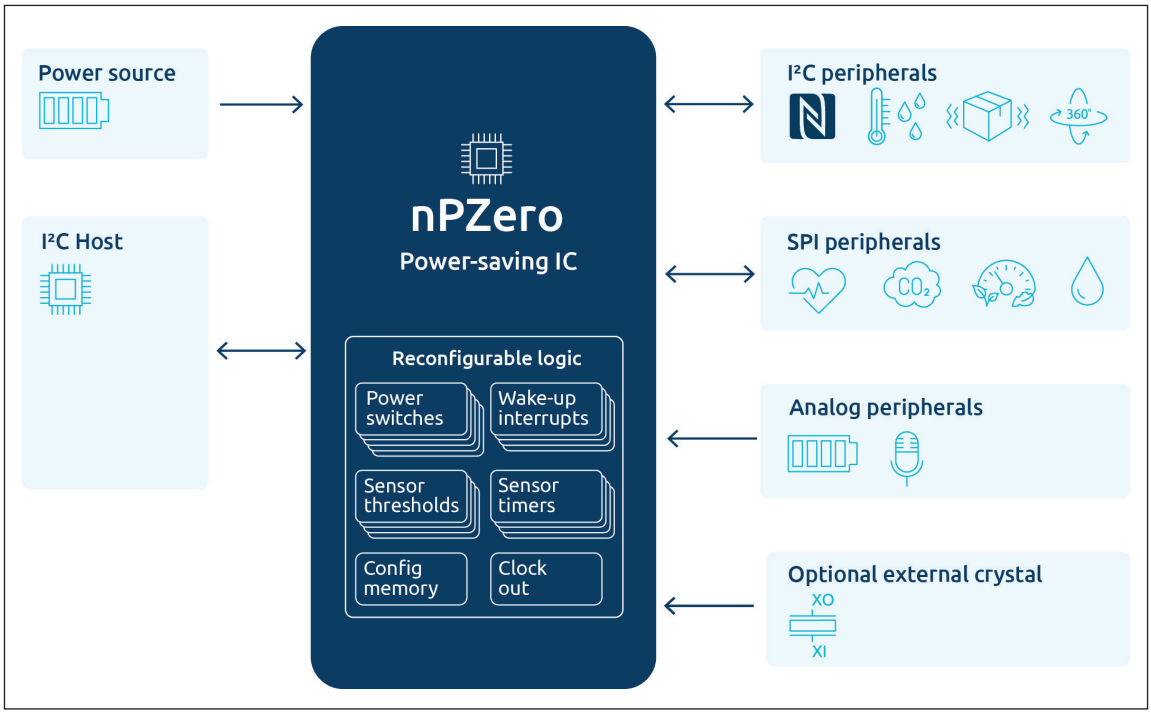
The typical use case for the nPZero is in IoT endpoints which monitor system parameters, such as temperature or motion, and which only communicate when a notifiable event occurs (such as the temperature crossing a pre-set threshold value, or excessive vibration).

The nPZero performs system monitoring with the host SoC switched off, and wakes up the SoC only when a notifiable sensor value has to be transmitted. The nPZero might typically also wake up the SoC at a regular interval to send a system update.

In system monitoring mode, the nPZero can operate on an interrupt basis: here, the sensor is always on, and its state machine interrupts the nPZero when an event needs to be triggered.

Alternatively, the nPZero can operate in I2C or SPI mode: here, the nPZero polls sensors on a pre-set schedule. This means that the sensors can be switched off between polling events, saving even more power.

Nanopower provides a zero-code nPZ Configurator tool for configuring sensors in the system, applying polling schedules, and setting the parameters for triggering events (see Figure 2). The nPZ Configurator tool automatically generates the firmware code needed for the host MCU to configure the nPZero. The code can be inspected



➤ Figure 3. In the nPZero EVB, the nPZero manages sensors' operation with the SoC host switched off, and only wakes up the SoC when a sensor's threshold value is crossed, or for scheduled data uploads.

and manually edited in the tool if needed. Additionally, the tool can analyse the state of power switches and serial interfaces in a running system, allowing the user to evaluate the efficiency of a given implementation, and tune the configuration of the nPZero device to their requirements. Hardware implementation is also straightforward: the nPZero requires only a few external passive components, and an optional crystal for more accurate time keeping.

Test system demonstrates power-saving potential of nPZero

The potential for power-saving in endpoint IoT devices can be seen in a comparison between a conventional design implementation and a demonstration system based on the nPZero IC. The test system is based on the nPZero Evaluation Board (EVB). This is a modular system which makes it easy to add sensors to the nPZero baseboard via PMOD headers, and to add an SoC daughtercard via an Arduino Uno-compatible interface.

The demonstration design uses the ams OSRAM AS6212 temperature sensor and STMicroelectronics LIS2DW12 accelerometer boards that are shipped by Nanopower with the EVB. The SoC is an nRF52840 Bluetooth Low Energy microcontroller from Nordic Semiconductor (see Figure 3).

Designers of endpoint IoT devices can evaluate this performance themselves with the nPZero EVB and their choice of PMOD sensor boards and SoC daughtercards

Such a system might typically be used in applications such as monitoring the condition of goods in transit, or for cold-chain data logging. The test system is set up to provide frequent measurements. The temperature sensor is read every 4s and the accelerometer every 0.625s. The nPZero IC is set to wake the host if a movement is detected or the temperature is outside the range 18°C to 28°C. Regardless of sensor measurements, the host also wakes up every 5 minutes to send the most recent sensor readings via Bluetooth link. The test compared total energy consumption of the EVB system first without the nPZero – that is, with the nRF52840 SoC controlling the sensors' operation directly – and then with the nPZero, allowing the SoC to be switched off between radio transmissions.

With the nRF52840 controlling the sensors via I2C interfaces, and the nPZero disabled, average current over an hour's operation was 395.4µA. After enabling the nPZero to control the system via I2C, allowing the nRF52840 to be switched off between transmissions and the sensors to be duty-cycled, average current falls to 49.6µA – a reduction of 87%, while providing exactly the same functionality and performance.

How to evaluate the nPZero's operation

Designers of endpoint IoT devices can evaluate this performance themselves with the nPZero EVB and their choice of PMOD sensor boards and SoC daughtercards (see Figure 4). The nPZero Configurator tool is available free for users of the EVB.

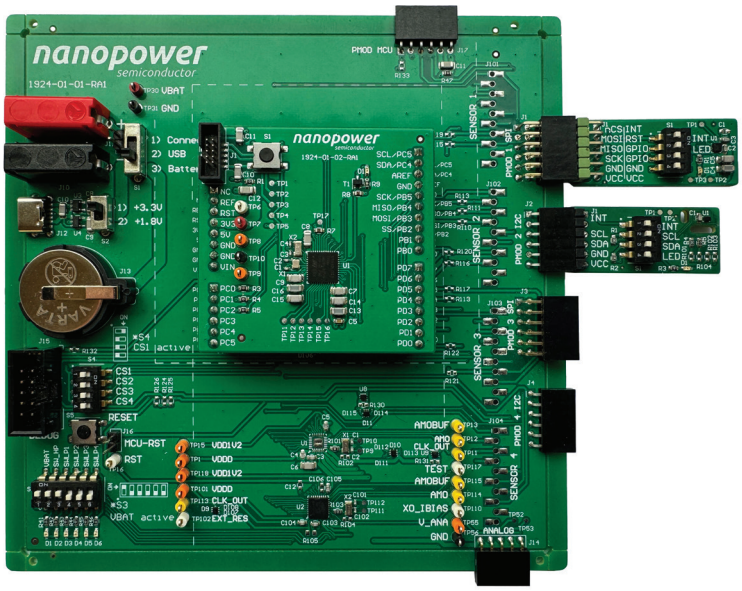
OEMs can also emulate a demonstration design developed by Nanopower which shows how the

nPZero can be used to substitute harvested energy for a battery power supply. Developed jointly with TDK, this system features the nPZero power saving IC continuously controlling environmental sensors including the TDK CH201 time-of-flight sensor. The battery-free system is powered by TDK CeraCharge solid-state batteries energized by Epishine indoor photovoltaic cells.

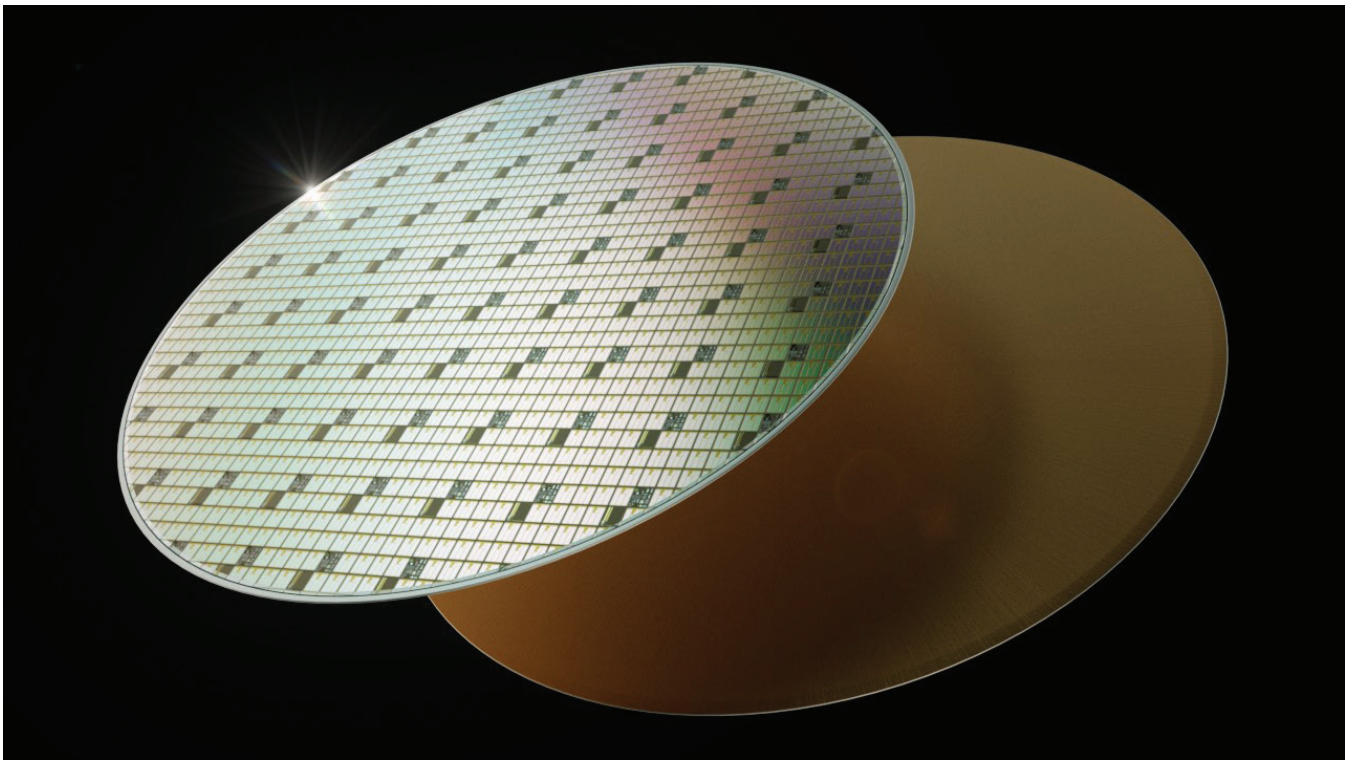
Naturally, power is not the only aspect of a system design that an OEM cares about: decisions about the use of the nPZero IC are also affected by the question of system cost and size. Here as well, the nPZero has a powerful case to make: as Figure 3 shows, the nPZero includes an internal low-power oscillator and power switches, enabling external components implementing these functions to be eliminated from the bill-of-materials.

In addition, the power savings produced by the nPZero can enable the OEM to reduce the size of the battery and the system enclosure.

So the nPZero offers considerable advantages to designers of wireless endpoint IoT devices, and thanks to the availability of the nPZero EVB, these advantages can readily be evaluated in the user's application.



➤ Figure 4. The nPZero EVB enables users to add their choice of PMOD sensor board and SoC daughtercard.



Thick homoepitaxy on 200 mm SiC

The cost of SiC substrates needs to come down. But are we going to hamper these efforts by imposing limits on the thickness of this foundation?

BY THOMAS KUHR FROM WOLFSPEED

SiC is benefitting from the electric vehicle boon, with uptake of power devices based on this wide bandgap semiconductor enabling higher-efficiency electronics that reduce system losses by 80 percent or more. However, while this is impressive, it is only the tip of the iceberg. As well as its wide band gap, SiC has a high thermal conductivity and an excellent saturation drift velocity, allowing devices made from this material to operate at high electric field densities and serve in many technologies, including high-voltage DC, pulsed power, and solid-state transformers. Using single SiC MOSFET chips that can handle up to 10 kV, or even-higher-voltage bipolar devices, equips designers with the opportunity to simplify systems and reduce resistive-heating losses across many applications.

As SiC continues to demonstrate an improved performance over incumbent technologies, it is facing heavy scrutiny for its higher cost. Within the semiconductor industry, the common solution to this challenge is to move to larger wafers, which divide fixed processing costs over many more devices. This is underway, with SiC substrates currently undergoing a transition from 150 mm to 200 mm diameters. However, in contrast to the silicon industry, which increased wafer thickness with diameter, the SiC industry is considering retaining the 350 μm thickness used for today's 150 mm-diameter wafers for the 200 mm format.

At Wolfspeed, a world leader in SiC substrates and devices, we have been investigating how epitaxial layers of different thicknesses vary in quality, when using wafers with thicknesses of 350 μm and 500 μm. The growth of 'thin' SiC layers, used for production of 650 V and 1200 V devices does not tend to result in significant stresses from temperatures profiles, or from differences in doping between the substrate and the epitaxial film. However, when epitaxial layers are thicker and lower doped – they are the two key requirements for higher-breakdown-voltage devices – stresses are magnified, generating new defects and wafer shape concerns.

Additionally, epitaxial defects increase in size and area, because they are often generated at or near the substrate interface and grow commensurately with the film. The compounding effect of greater stress and larger defects, coupled with higher-voltage devices often being larger in size, results in much lower usable area of the wafer, leading to lower die yields and a higher cost per device.

What could go wrong?

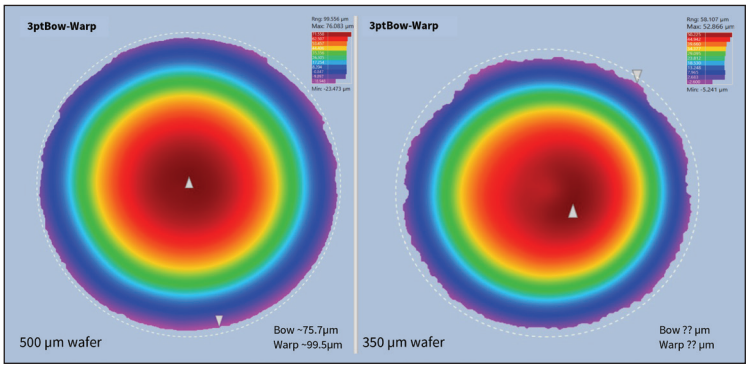
To deepen our understanding of the interaction of thinner substrates and thicker epitaxy, we have investigated the performance of homoepitaxial layers with three different thicknesses, grown on 200 mm SiC substrates that are 350 μm-thick and 500 μm-thick, using two commercially available reactor platforms. Admittedly, the best way to approach this evaluation would be to cut a single boule into multiple substrates with different thicknesses, as this would normalise the starting point for substrate defects – but for this work we used internal production wafers as they became available. We selected doping and thickness targets based on specific device requirements, chosen to hit the lowest resistance at the required breakdown voltage, and we have been able to identify if there are any potential manufacturing limits by utilising a suite of measurements that are part of our standard production fab flow.

One concern during epitaxy is the stability of wafer shape at high growth temperatures. The wafer shape may differ at room temperature and at more than 1600°C, and thinner wafers may change shape unpredictably. Any variations will adversely affect growth through thickness or doping non-uniformity, and in the worst-case scenario the wafer may break or be ejected from the carrier during processing.

Our results have dispelled this concern when reducing wafer thickness from 500 μm to 350 μm. If anything, the thinner wafers lead to improvements in film thickness and doping uniformity, although this is likely to depend on the reactor furniture design. Note that we need many more growth runs to establish statistically significant conclusions. However, our initial investigations indicate that there are no concerns associated with using thinner 200 mm wafers for the epitaxial growth process.

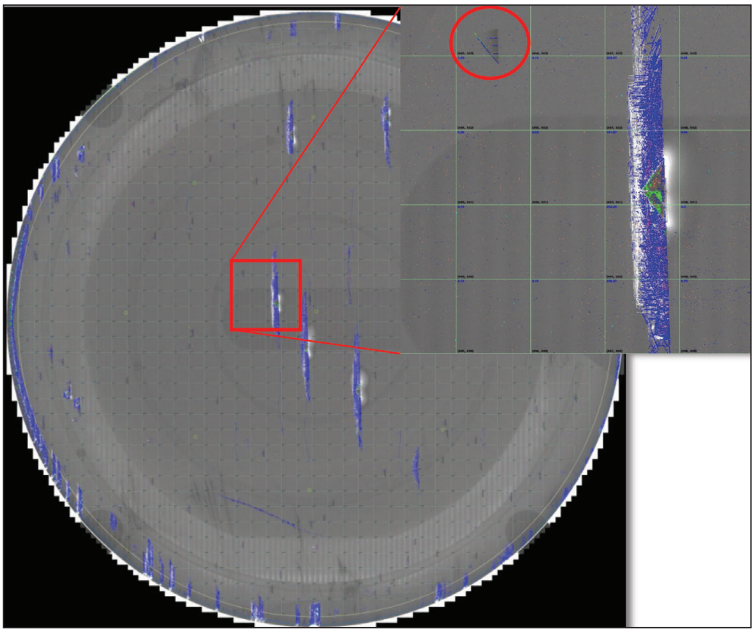
Due to similarities in the processing chemistry and device design for thin and thick SiC devices, our device fabrication team prefers a similar state for the surface of all epiwafers. To see if this is the case, we scrutinised our material with atomic force microscopy (AFM) and confocal imaging. AFM, useful for gauging short-range roughness, shows a matched performance in roughness, with the average roughness (Ra) less than 0.2 nm for thin and thick films. According to confocal imaging, long-range roughness for thicker films is greater than it is for thin films, with an average roughness (Ra) of around 0.6 nm.

These finding are independent of substrate thickness, though a bit more roughness is slightly more spatial on the confocal imaging scale. This suggests that like doping and thickness uniformity, surface roughness may be treated as a non-issue with respect to wafer thickness. However, there's a need to reduce surface roughness in thicker films, and to further refine spatial dependencies.

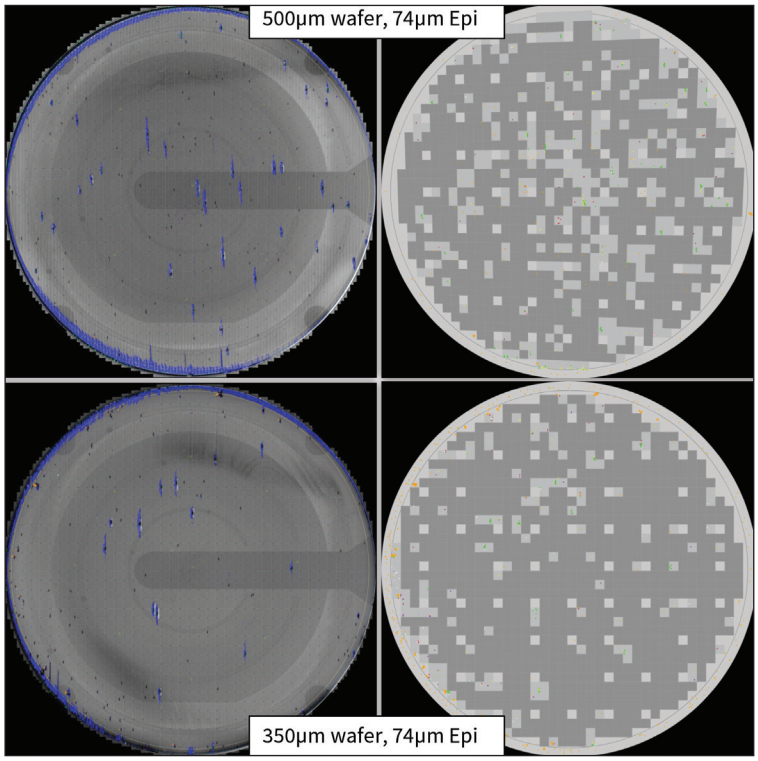


➤ Figure 1. Comparison of wafer shape maps for 500 μm (left) and 350 μm (right). Notice that in both cases the full map has not been generated, though the left scan is more complete. The bow and warp of the 350 μm wafer is clearly higher and outside the measurement range of the current tool configuration.

With thicker epitaxial layers resulting in larger defects and higher film stress, selecting thinner substrates exacerbates the stress problem. Due to this, we were not surprised to find a shape issue when growing thicker epilayers on thinner substrates. Using 200 mm-diameter SiC, growing a 13 μm-thick epilayer on a 500 μm-thick substrate leads to a bow of 20-40 μm; and increasing the thickness to 115 μm, and dropping the doping to the mid-10^{15} cm^{-3}, increases the bow to around 80 μm. If the substrate is then thinned to 350 μm, bow increases to more than 100 μm, leading to threats of handling errors and wafer breakage during device fabrication processes. While 100 μm of wafer bow may seem miniscule compared with the hundreds



➤ Figure 2. Stitched image map with preliminary inking to estimate usable area for devices for 115 μm epitaxy on 500 μm-thick 200 mm substrates. An arbitrary 5 mm x 5mm grid was used for visualisation. Note that not all defects are correctly identified, but that area effect of gross defects like triangles can be seen, as shown in the insert.



➤ Figure 3. Stitched image maps with preliminary inking to estimate usable area for devices for 74 µm epitaxy on 500 µm and 350 µm thick 200 mm substrates. 5x5 usable areas of 75-85 percent shown.

of microns of bow that may occur during ion implantation, not all fabrication tools are capable at that starting point. Our view is that more work may be needed to compensate for wafer shape concerns, if substrates that are just 350 µm-thick are going to be used for growing thicker epitaxial layers.

The biggest disadvantages of SiC are its defectivity that's inherent in its crystal growth process, and the relative ease of defect formation. The defects that are generated during boule growth and reside in the substrate will propagate into the epilayer by either continuation of the growth, or by conversion to other types of defects. The sources of defects could be micropipes, threading dislocations, stacking faults, subsurface damage from surface preparation, or simply a dirty surface from inadequate cleaning; more generally speaking, anything that disrupts the natural stacking of the crystal lattice. For example, a common defect called a 'triangle' – it's a crystal stacking disruption that manifests as a triangular shape visible on the growth surface – increases in size with epitaxial growth, from 0.4 mm-long for 13 µm of epitaxial growth to 3.2 mm for a 115 µm-thick film. You might think what's the big deal, given that devices are typically 25 mm^2 or more in size, so a triangle defect should only affect one or two die.

Well... As we have already mentioned, film stress increases with thickness, and the doping offset between the film and the substrate. Due to this, and the very low formation energy for basal plan dislocations in SiC, it's possible for defects, such as triangles, to generate basal plane dislocations that glide vertically along the wafer, emanating from the source defect. Consequently, a defect that originally affected just one or two devices may now impact five-to-ten times as many die, slashing yield.

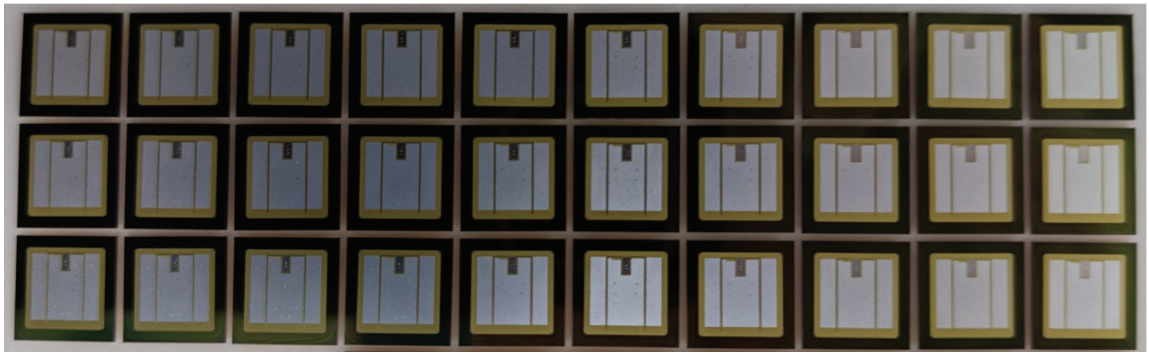
The good news is that by careful management of the temperature distribution on the wafer during epitaxial growth, it's possible to reduce excessive film stress. Even if this gain comes at the expense of an increase in wafer bow, this enables the processing of thinner wafers without increasing film defectivity.

Unfortunately, not all our measurements went particularly smoothly. Due to incomplete scans, our values for maximum bow on our thin wafers with thick epitaxial layers were initially incorrect. Correcting this error, a simple tooling limitation that can be overcome with minor adjustments, took time and effort.

We also encountered problems associated with automated inspection of defects, due to inspection algorithms that are trained for a different size defect or a smoother surface. This meant that applying our accurate defect classification and data acquisition to thinner epitaxial layers was initially troublesome for thicker epitaxial films.

Our issues related to wafer bow scans and defect inspection are far from insurmountable, and in the case of defects, they are not even substrate-thickness dependent. However, intervention and development are needed before these techniques can serve in a high-volume manufacturing process.

To summarise, thinner wafers will result in shape concerns that must be addressed, either before or during epitaxial growth. But if the temperature distribution and stresses are effectively managed,



➤ Figure 4. 10kV die ready for packaging.

additional stress-induced defects should not be problematic. This doesn't sound too bad... except the predicted yields don't look great, and the costs are still high.

Illustrating this point, let's consider 5 mm by 5 mm devices for a 1200 V MOSFET wafer. In this case, the useable area is more than 90 percent. But if thicker epitaxy is needed, the useable area falls to around 70 percent, due to the increased area effect – and if the device size increases, there's an additional fall in usable area, determined by simple Poisson statistics. Now that SiC wafer with a usable area of more than 90 percent for a 1200 V MOSFETs is potentially below 40 percent for 10 kV MOSFETs – and that's before the epiwafer has even ever entered a device fab.

A feasible thickness?

Let's return to the original question: does thinning the SiC substrate limit the capability of using thicker epitaxial layers to make high-voltage devices? Well maybe... and maybe not. It's clear that it's critical to get the wafer shape under control and manage the epitaxial growth stresses, in order to prevent complications during device fabrication and thus keep cost low. To support such efforts, adjustments are needed to ensure continuity of measurement and metrology methods with current best practices and industry standards. But what's also really importantly is for SiC substrate manufacturers to continue to focus on defect reduction. Without lower defect concentrations, device size and capability or device yield will continue to be trade-offs, and costs will remain high regardless of the optimisation of the epitaxial growth process.

In closing, the drive for thinner SiC substrates will continue, because reducing their cost remains a huge motivator. Against this backdrop, innovators will find ways to deal with wafer shape, and substrate manufacturers will continue to decrease defect density, helping to improve device yields and trim costs.

Out of shear technological need, adoption of higher-voltage devices will continue to rise, with 10 kV MOSFETs eventually paving the way for even higher voltage IGBTs. The SiC revolution will continue!

➤ Left. High-performance half-bridge 10 kV, 50 mΩ all-SiC power module.

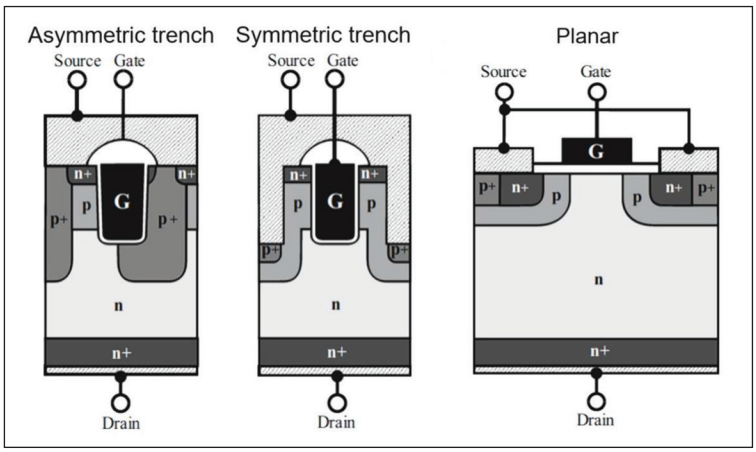
Scrutinising SiC MOSFETs

Efforts by chipmakers to improve the SiC MOSFET include investigations to understand how the design of the trench influences ruggedness, the role of the substrate on device quality, opportunities for superior screening, and the origin of shifts in threshold voltage

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

It is now 15 years since the launch of the first SiC MOSFETs by two of its pioneers, Rohm and Cree, subsequently renamed as Wolfspeed. Since then, there has been a substantial increase in the number of producers of this device, as well as an expansion in blocking voltages, improvements to performance, and a growth in sales to more than $1 billion per annum, according to many analysts.

Judged in these terms, there's no doubt that the SiC MOSFET is already a tremendous success. But there is still more to do on many fronts. To increase the supply and trim the cost of this class of transistor, more fabs are being built, and production is switching from 150 mm to 200 mm wafers. And to improve yield, performance and robustness, many leading manufacturers of the SiC MOSFET are scrutinising its behaviour.



➤ Figure 1. Infineon has compared the short-circuit ruggedness of MOSFETs with an asymmetric trench, a symmetric trench, and a planar trench.

At this year's International Reliability Physics Symposium (IRPS), held in Monterey from 30 March to 3 April, researchers from a number of the leading manufacturers of SiC MOSFETs detailed insights gained from investigations into this class of transistor. Studies of short-circuit ruggedness for different channel designs were outlined by Infineon; STMicroelectronics revealed the influence of the starting material on final device characteristics; NoMIS Power presented screening methods using high gate-voltage pulses and unclamped inductive switching; and investigations into threshold voltage shift were reported by Mitsubishi Electric.

Short-circuit ruggedness

In power-conversion systems, ruggedness and reliability are critical, particularly when short-circuit events occur. Due to this, there is a need for SiC MOSFETs to be robust under repetitive fault operating conditions.

Investigating this, a team from Infineon has compared the performance of three types of SiC MOSFET produced by four different manufacturers: that with an asymmetric trench, the technology that Infineon employs; another with a symmetric trench; and two variants with planar structures with different

oxide thickness (see Figure 1 for the device designs, and Table 1 for key details of the device structures).

Discussing this study at this year's IRPS, Andrea Piccioni noted that the active areas of the MOSFETs with a trench architecture are smaller than those with a planar geometry, enabling a lower on-resistance.

Piccioni explained that their investigation involved using normal distribution channels to purchase 15 commercial 1.2 kV devices from each of the four manufacturers. These devices, with on-resistances in the range 62 mΩ to 82 mΩ, were housed in TO247-4 pins packages, and had not been used prior to the stress test. The team decapsulated one of each of the 15 devices to analyse its characteristics in the pristine state.

The repetitive short-circuit stress test is relatively straightforward, involving the repeating of short-circuit events at a certain frequency, and ensuring that the time between each of them is long enough to avoid heating accumulation. The researchers applied 1,000 cycles at a frequency of 1 Hz, using pulses with a duration of 2 µs to provide the short-circuit. This test involved a drain-source voltage of 800 V, and values for the positive gate-source voltage varying from device to device – they ranged from 14.2 V to 15.5 V – to ensure similar values for the energy density of the four different devices.

During testing, destructive failure can occur, due to leakage from the drain to source. In addition, there can be non-destructive failure, such as leakage from the gate to source, and variations in key characteristics, such as threshold voltage.

The team had to consider how to spot all these possible issues with one unique criterion. "We decided to use short-circuit energy variation over the short-circuit cycle," explained Piccioni, who added that they considered a variation of more than 5 percent a failure.

Results of the stress tests show significant variation with device architecture (see Figure 2). All the MOSFETs with the asymmetric trench stay well within the ± 5 percent limit, as do those with the symmetric trench – although in that case there is a slight increase in short-circuit energy over the duration of the test, due to a negative shift in threshold voltage. In sharp contrast, the planar SiC MOSFETs performed poorly. All those with a thicker oxide failed the test, two from thermal runaway that led to destruction, and the remainder from an elevated gate-to-source leakage. The latter issue also led to the failure of ten planar devices with a thinner oxide.

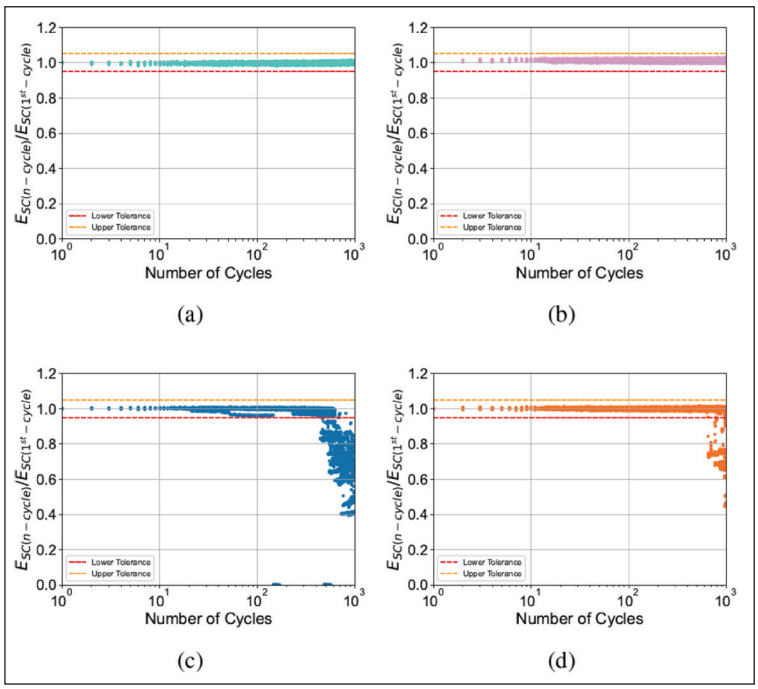
Piccioni also shared a Weibull plot, showing the probability of failure as a function of the number of cycles. This demonstrated that the gate oxide thickness in planar structures plays a pivotal role in robustness, within thinner oxides leading to greater reliability.

Param.	Channel	$^{*}R_{DS(on)}$	AA	d_{GOX}
Unit	[/]	$[m\Omega]$	$[mm^2]$	$[nm]$
M1	Asym.trench	78	2.28	~67
M2	Sym.trench	62	3.52	~50
M3	Planar	62	5.62	~50
M4	Planar	75	4.55	~35

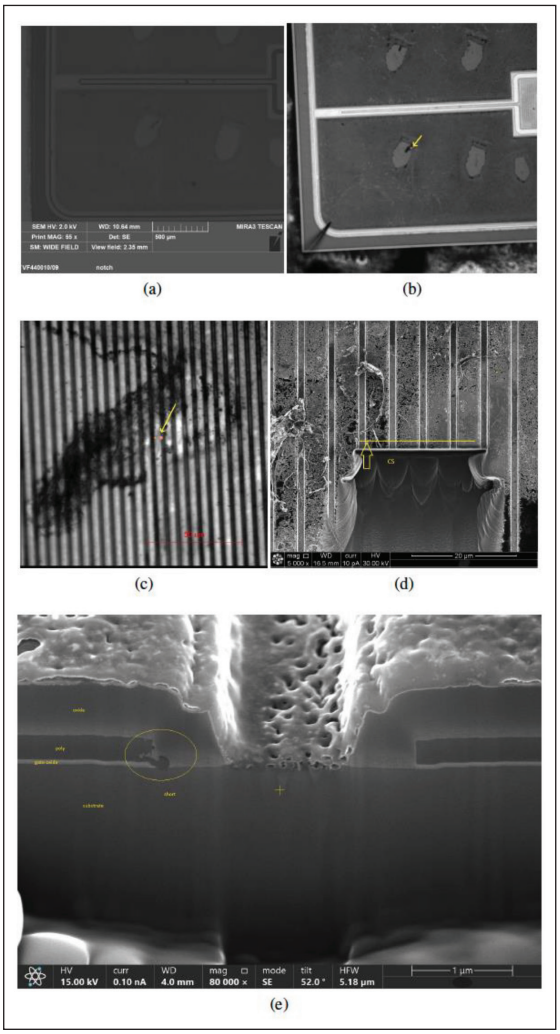
➤ Table 1. Details of the different forms of SiC MOSFET used in Infineon's study of short-circuit ruggedness. AA is the active area, and d_{GOX} is the thickness of the gate oxide.

Failure analysis has been conducted by Piccioni and co-workers, initially with decapsulation and optical inspection, before removing the top side of the device and turning to scanning electron microscopy. "After that, photo-emission microscopy helped us to locate the spot where the leakage current is flowing," remarked Piccioni, who explained that the team would then extract a cross-section, and view this using a focused ion beam. With this approach, a short is observed between the substrate and the corner of the polygate (see Figure 3).

To understand the origins of the weakness of planar devices, Piccioni and co-workers turned to Technology Computer-Aided Design (TCAD) simulations to gain an insight into the temperature profiles of different designs of MOSFET. These simulations show that compared with a trench device, that with a planar geometry has a higher temperature at the top side metallisation and at the SiC substrate. In the planar device, the hot spot occurs at 2.17 µm. Meanwhile, in the trench MOSFET,



➤ Figure 2. The short circuit energy over 1,000 cycles reveals the superior reliability of the (a) asymmetric and (b) symmetric trench MOSFETs over their planar equivalents (c) and (d).



➤ Figure 3. To uncover the origin of the failure in the planar SiC MOSFETs, the team from Infineon began by removing the top-side metal and inspecting the device with a scanning electron microscope (a). Failure localisation by photo-emission microscopy followed (b) and (c), before a focused ion beam provided a cross-section (d) and its visualisation (e), exposing a short at the edge of the gate.

the hot spot is deeper, at 3.38 μm, reducing the stress at the gate oxide.

Material considerations

A key question for the producers of any semiconductor device is this: How does the impact of the starting material influence the final device? This is far easier to answer for companies that are vertically integrated, such as STMicrolectronics, which spans powders to products.

Speaking on behalf of this European powerhouse at IRPS, Advanced Metrology Material Manager Nicolò Piluso offered some insights into this matter, by considering 650 V MOSFETs subjected to high-temperature reverse-bias tests.

SiC material is grown by physical vapour transport, with SiC powder heated at the bottom of a chamber, beneath a SiC seed crystal. The growth of SiC is imperfect, with bulk material riddled with a range of defects, including micropipes, threading screw and edge dislocations, basal plane dislocations and point defects.

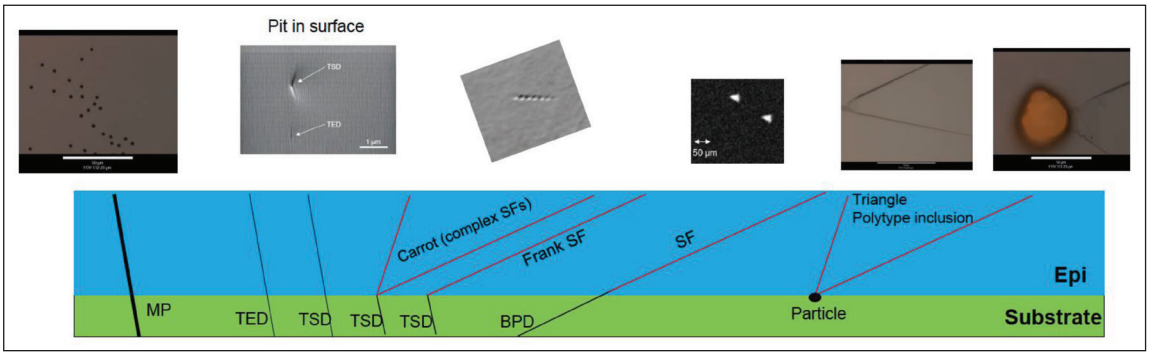
Production of SiC power devices involves growth by MOCVD on substrates that are off-axis to realise the best compromise between surface kinetics and growth rate.

“The aim is to achieve a high thickness and good doping uniformity, keeping low the defectiveness,” remarked Piluso. Due to this, there’s a need for a fast epitaxial process and repeatability.

Piluso outlined how many types of defect can propagate from the substrate to the epilayer (see Figure 4). In the case of threading screw dislocations and Basal plane dislocations, growth tends to lead to a conversion into stacking faults.

Different types of defect impact the MOSFET in different ways. Micropipes, which now have a typical density below 0.1 cm^{-2}, are destructive, while threading screw dislocations that are accompanied by a pit, and have a similar degree of prevalence, lead to reliability issues, and can cause an increase in leakage current. MOSFETs can also suffer from a significant decline in blocking voltage, caused by in-grown stacking faults, complex stacking faults and downfalls – typical densities are 0.01 cm^{-2} to 1.0 cm^{-2} for the first of these, and 0.1 cm^{-2} to 1.0 cm^{-2} for the other two.

Piluso explained that a number of techniques are used to follow the defectivity from the substrate to the epilayers. The most common are optical microscopy, light-scattering methodologies and photoluminescence. All three are relatively quick, have a high spatial resolution, and can uncover morphological defects, but are unable to reveal dislocations. This is possible with X-ray topography and atomic force microscopy, but both those approaches have a low throughput.



➤ Figure 4. SiC substrates suffer from many types of defect.

"The recent enlargement of the wafer from 150 mm to 200 mm brings several drawbacks, in terms of defects, at the beginning," remarked Piluso. He explained that stacking faults were detected near the edge of the wafer, which is symptomatic of a physical vapour transport process issue that needs to be fixed. Another concern is scratches, due to a lack of optimisation in the chemical mechanical polishing process.

"I can say that currently, such kinds of evident defects have been almost completely removed and 200 mm high-quality silicon carbide substrates are available."

A major weakness of today's metrology tools is that they are unable to detect defects that lead to failure. The likes of micropipes, nanopipes and threading screw dislocations are exposed though electrical failures.

"In such cases, electrical testing is the only way to test the quality of the material," said Piluso.

The spokesman for ST shared a map of die from a wafer, with those impacted by a defect suffering from inferior electrical characteristics, including a significant reduction in the Schottky barrier height. Raman microscopy is able to clearly identify the nature of the defect – inclusion of the 6H polytype.

Piluso also discussed electrical failure caused by a threading screw dislocation accompanied by a pit. The non-destructive optical technique emission microscopy exposed the hot spot, associated with device failure. Scanning electron microscopy then uncovered a triangular-shaped defect at this hot spot, suggesting a dislocation that originates in the substrate and propagates to the epilayer. Scrutinising this area with atomic force microscopy identified surface pitting, caused by threading screw dislocations that are clearly exposed by etching with potassium hydroxide.

The team from ST have also studied a hard failure, seen by an abrupt increase in drain leakage current after about 30 minutes. Again, emission microscopy identified the location of the device. After delayering, Piluso and co-workers applied a potassium hydroxide etch, which revealed the typical symmetry exhibited by a micropipe defect.

"It can be supposed that the defect led to a very high current density in a narrow region," remarked Piluso, adding: "The material is brought to a high temperature, exceeding the limit imposed by conductivity, and for this reason suffered corrosion and breakage."

He added that scanning electron microscopy revealed a core hole in the centre of the defect at a depth of more than 30 μm, indicating that this defect starts in the bulk and goes through the entire epilayer.

The success of the SiC MOSFET over alternatives, such as the SiC JFET and SiC BJT that got to market first, stems from providing a drop-in replacement for the silicon MOSFET. However, while both forms of MOSFET are similar, they differ in threshold voltage characteristics

When concluding his presentation, Piluso called for strong activity to improve characterisation, by enabling scanning electron microscopy, profilometery, and atomic force microscopy within standard metrology inspection at the manufacturing level.

Threshold voltage shifts

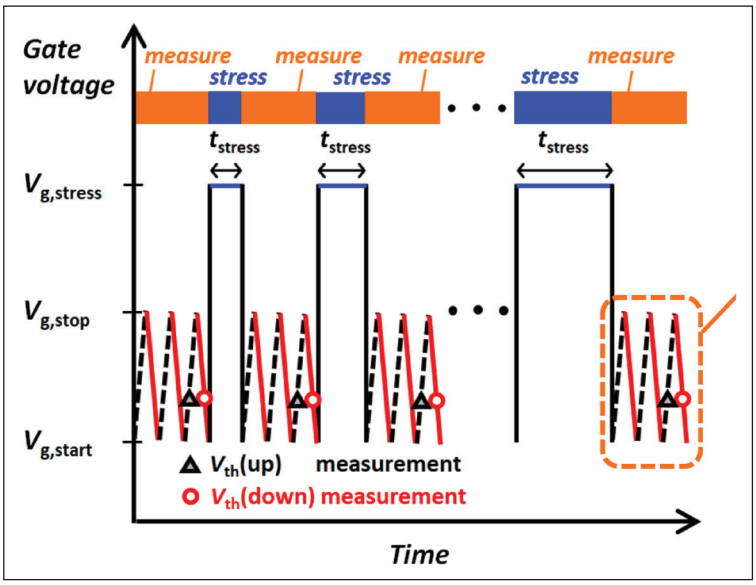
The success of the SiC MOSFET over alternatives, such as the SiC JFET and SiC BJT that got to market first, stems from providing a drop-in replacement for the silicon MOSFET. However, while both forms of MOSFET are similar, they differ in threshold voltage characteristics.

These differences in threshold voltage characteristics, seen under different temperatures and stress conditions of the oxide, are related to the SiO_2 dielectric in both types of transistor. Due to its wider bandgap, energy levels of the defects present in SiO_2 differ to those found when this oxide is paired with silicon.

Given the importance of threshold voltage – a key characteristic for any transistor – changes in the threshold voltage of SiC MOSFETs have been extensively studied. These investigations have established that the threshold voltage changes when a positive or negative electric field stress is applied to the gate oxide, as this leads to a charging of defects in the gate oxide, especially in the vicinity of the SiO_2/SiC interface.

Under a moderate electric field stress, there is a monotonic change in threshold voltage with stress time, due to the capturing of only electrons or holes, depending on the bias.

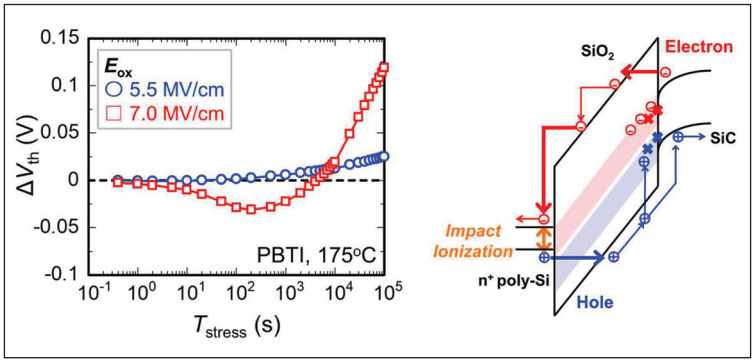
When the electric field stress is either highly positive or negative, SiC MOSFETs display a markedly different behaviour. In this case, the threshold voltage shift is initially negative, but over time it turns around and switches to positive, due to the capture of both electrons and holes in both SiO_2 and beside the SiO_2/SiC interface. Under these conditions, there's the filling of bulk traps in SiO_2, as well as interfacial traps at or near the SiO_2/SiC interface.



➤ Figure 5. Mitsubishi Electric's positive and negative bias temperature instability measurements were undertaken with measure-stress-measure sequences. Double sweeps of the gate voltage were performed three times to ensure a reducible readout of the threshold voltage.

According to Munetaka Noguchi and co-workers from Mitsubishi Electric, the influence of a high gate voltage on bias temperature instability of SiC MOSFETs has been well reported, accurately capturing the physical phenomena involved. "However, the impact of a high oxide electric field stress is not fully understood, and requires a systematic investigation." So, to shed light on this issue, they have conducted a thorough study on this, reporting results for SiC MOSFETs under a range of stresses, including both high negative and positive bias, and different temperatures.

For this work, the team from Mitsubishi used vertical planar silicon-face *n*-MOSFETs, with the gate oxide, roughly 47 nm-thick, formed by thermal oxidation and subsequent nitridation in diluted NO. On top of the oxide is n^+ poly-silicon.



➤ Figure 6. Measurements by Mitsubishi Electric of positive-bias temperature instability reveal a shift in threshold voltage under cumulative stress that depends on the applied oxide field stress. Under high oxide stress (right), electrons injected from SiC trigger impact ionisation in the n^+ poly-silicon, and holes that are generated are subsequently injected back into the SiO_2, where they are partially captured.

As well as these vertical devices, Noguchi and co-workers studied lateral devices that do not have the JFET region. Investigating these lateral devices allows evaluation of the gate leakage current and the hole current flowing into the gate oxide from the channel region.

For testing both positive- and negative-bias temperature instability, for each value of threshold voltage that's recorded, the team performed a double sweep of the gate voltage on three occasions, to ensure a reproducible readout of the threshold voltage (see Figure 5). The researchers defined the threshold voltage as the gate voltage at which the drain current reaches 1×10^{-6} A cm^{-2}, and defined the change in threshold voltage as the shift in threshold voltage in the downward sweep from its initial value.

Investigations for the positive-bias temperature instability at 175°C show that under an oxide electric field stress of 5.5 MV cm^{-1}, a condition referred to as 'not so high', there is a monotonic increase in threshold voltage with stress time, resulting from electron capture in SiO_2 (see Figure 6). But at a higher oxide electric field stress of 7 MV cm^{-1}, the change in threshold voltage exhibits turnaround behaviour, shifting from initially negative to positive. "This indicates that hole capture occurs initially, and after a while this process saturates, and in the following phase electron capture becomes dominant."

The holes that are observed during this measurement possibly result from anode hole injection. This could occur under a high positive oxide electric field stress, with some electrons injected from SiC triggering impact ionisation in the n^+ poly-silicon, and holes that are generated subsequently injected back into SiO_2, where they are partially captured.

At 175°C, under an oxide electric field stress of 7.4 MV cm^{-1}, the negative change in threshold voltage is larger than it is at 25°C, suggesting that at a lower temperature more holes are captured by SiO_2.

To delve deep into electron capture, Noguchi and co-workers have studied the change in threshold voltage after turnaround, which is considered at the starting point for these measurements. Plots (see Figure 7) show that in the region where the shift in threshold voltage is less than 0.2 V, the curves for different oxide electric field stresses have an almost parallel shift, with the slope becoming more gradual as time increases. According to the team, this gradual saturation suggests the presence of as-grown electron traps in SiO_2. Meanwhile, where the shift in threshold voltage is more than 0.4 V, the slope becomes steeper with time, suggesting the generation of

as-grown electron traps in SiO_2 and/or the interfacial region.

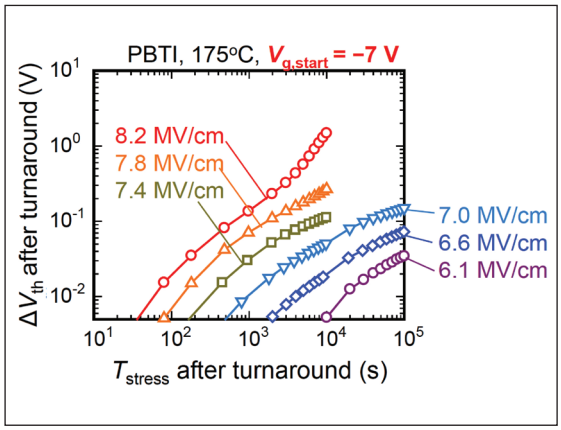
The team have also investigated the impact of the starting gate voltage on the change in threshold voltage after turnaround, comparing plots for 0 V and -7 V. Under the same oxide electric field stress, the change in threshold voltage is larger for 0 V, implying greater capture of electrons in SiO_2. This may occur because the surface potential at SiO_2/SiC is more bent at -7 V, leading to efficient emission of captured electrons.

Noguchi and colleagues have also carried out a thorough study of the shift in threshold voltage under stress under a negative bias. Similar to under positive bias, the plots at 175°C vary with the oxide electric field stress: there's a monotonic decrease observed at -5.8 MV cm^{-1}, due to hole capture in SiO_2; and, under -7.5 MV cm^{-1}, a turnaround from a decrease to an increase, attributed to electron capture in SiO_2 and/or near the interface between SiO_2 and SiC (see Figure 8).

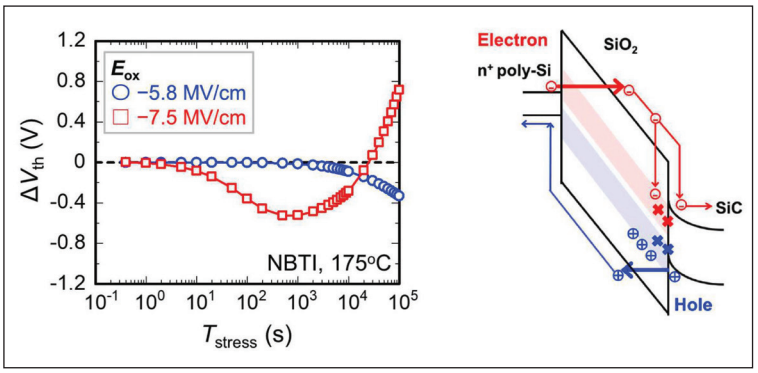
Previous studies on hole injection into SiO_2 on silicon have shown that the build-up of negative charges can be attributed to the generation of electron traps in SiO_2 and/or interfacial traps at the interface between SiO_2 and SiC.

Under a negative oxide-electric-field stress, holes injected from SiC are captured by SiO_2. It's possible that these injected holes could generate electron traps in SiO_2 and at the interface.

"To understand the phenomena, it's helpful to start the discussion with a threshold voltage shift at lower temperatures, such as 25 degrees C," remarked Noguchi.



➤ Figure 7. Measurements of the shift in threshold voltage after turnaround can be categorised into: curves with an almost parallel shift, with the slope becoming more gradual as time increases, suggesting the presence of as-grown electron traps in SiO_2; and curves that get steeper with time, suggesting the generation of as-grown electron traps in SiO_2 and/or the interfacial region.

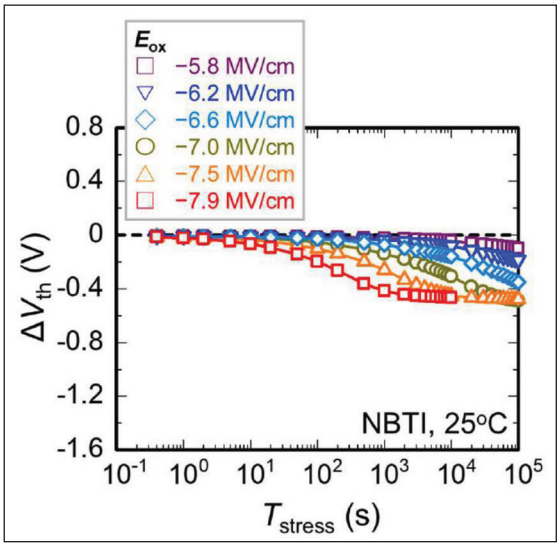


➤ Figure 8. Negative bias temperature instability measurements by Mitsubishi Electric reveal a shift in threshold voltage under cumulative stress that depends on the applied oxide field stress. The turnaround from a decrease to an increase in threshold voltage under -7.5 MV cm^{-1} is attributed to electron capture in SiO_2 and/or near the interface between SiO_2 and SiC.

Plots of this behaviour show a saturation in threshold voltage shift for all the applied oxide electric field stresses, which range from -5.8 MV cm^{-1} to -7.9 MV cm^{-1} (see Figure 9). At a higher oxide electric field stress, the change in threshold voltage is accelerated, attributed to faster hole capture.

Investigating the change in threshold voltage at -7.5 MV cm^{-1} for a range of temperatures shows that the minimum value does not change, and it is reached more quickly at higher temperatures, due to as-grown hole traps being filled more quickly, without additional generation of hole traps. Turnaround from a negative to a positive change in threshold voltage does not occur at 25°C, but does at 125°C and 175°C.

Noguchi and co-workers have investigated the change in threshold voltage after turnaround at 25°C and 175°C. "At both temperatures, the threshold voltage shift after turnaround can be universally described by the gate-injected charges after the turnaround," remarked Noguchi,



➤ Figure 9. Saturation of the threshold voltage shift, attributed to hole capture, is faster under a higher oxide electric field stress.

who pointed out that the shift is smaller at the lower temperature, and that the electron capture component of the threshold voltage shift can be attributed to the electron traps in silicon dioxide and at the interface.

To investigate these interfacial electron traps, the team studied the sub-threshold swing as a function of gate-injected charges. They found two phases in the generation of interfacial electron traps. "This indicates that the generation of interfacial electron traps on the negative oxide electric field stress partially contributes to the threshold voltage shift after turnaround."

Screening SiC MOSFETs

Over the last decade, advances in SiC substrates, epitaxial growth and the gate oxidation process have improved gate oxide reliability, but the risk of extrinsic failure in SiC devices still persists. This is an issue for the adoption of SiC MOSFETs in the electric vehicle market.

To address this concern, manufacturers of SiC power devices employ burn-in, at the package or wafer level, to provide a reasonable reduction in the 'failure-in-time' (FIT) rate – it's the number of failures per billion hours. For this task, harsher burn-in conditions enhance screening efficiency and further reduce the FIT rate, but may induce parametric shifts in the devices. What's more, the use of high-temperatures and extended testing during burn-in leads to a hike in overall production costs.

Due to these concerns, there is much interest in approaches that can cut the cost and time required to screen SiC MOSFETs.

One company developing a solution to this that's based on high gate-voltage pulses and unclamped inductive switching is NoMIS, a spin-off of the University at Albany, New York, that manufactures 1.2 kV, 1.7 kV and 3.3 kV SiC MOSFETs with worldwide foundry partners. Speaking on its behalf at this year's IRPS, Head of SiC Device Development at NoMIS Power, Seung Yup Jang, described this effort, which also involves contributions from the University at Albany and The Ohio State University.

Screening Type	Name	Conditions
High Gate Voltage Pulse (HVP)	HVP1	8.4 MV/cm, 1 s
	HVP2	8.6 MV/cm, 0.5 s
	HVP3	8.6 MV/cm, 1 s
Unclamped Inductive Switching (UIS)	UIS1	20% of Max E_{AS}
	UIS2	40% of Max E_{AS}
	UIS3	70% of Max E_{AS}
HVP + UIS	Combo	HVP1 + UIS1

➤ Table 2. NoMIS has screened SiC MOSFETs using high-voltage pulsed (HVP) and unclamped inductive switching (UIS) tests.

Jang explained that unclamped inductive switching is an effective method for identifying early failures under off-state high drain bias. While originally designed to evaluate edge termination robustness, uniform avalanche current distribution in active cells, and suppression of the parasitic bipolar junction, it has broader utility. During avalanche breakdown the maximum electric field in the gate oxide will typically exceed 3 MV cm^{-1}, and may be as high as 4 MV cm^{-1}. If a negative bias is applied during unclamped inductive switching, the oxide electric field can be even higher, causing the temperature in the active region to rise, often exceeding 500°C. "These extreme conditions impose considerable stress on the gate oxide, making unclamped inductive switching a rigorous and informative screening method."

The team has developed an approach that aims to screen out all early failures using regular, automatic testing tools, as this is a cost-effective and efficient approach. The combination of high gate-voltage pulse screening and unclamped inductive load screening has been evaluated twice – after wafer fabrication and after packaging.

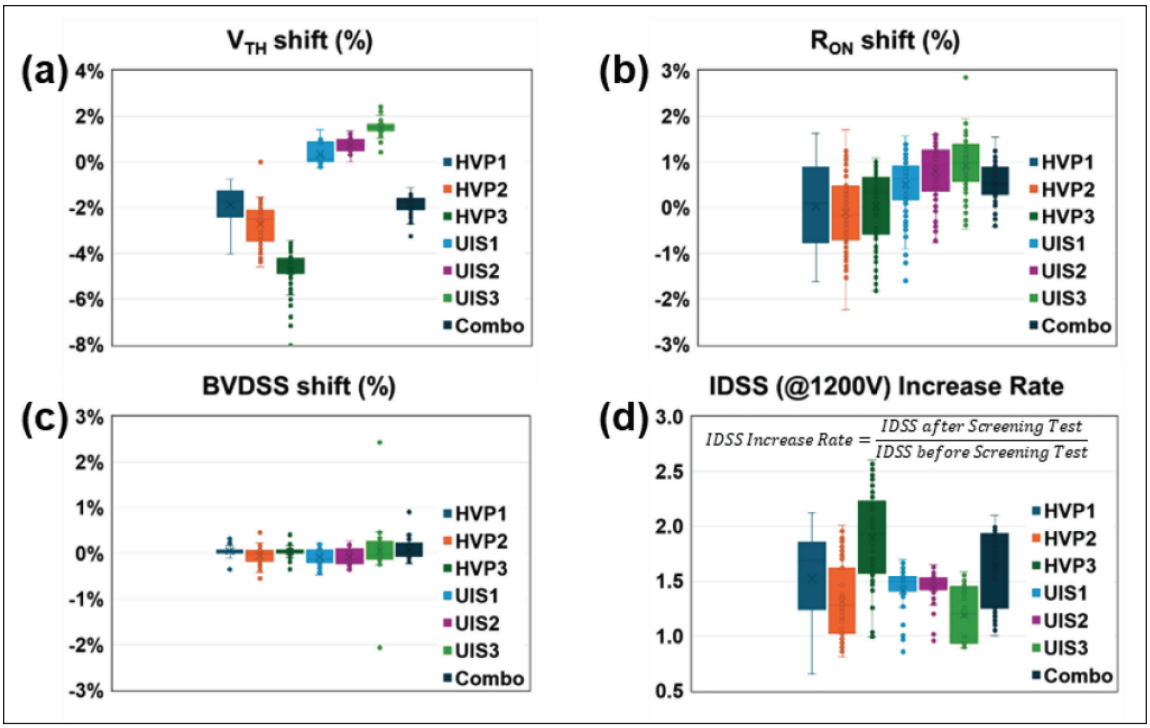
For this study, Jang and co-workers have investigated 1.2 kV, 35 mΩ and 80 mΩ planar SiC MOSFETs produced in a commercial foundry using 150 mm wafers. Gate oxides were thermally grown on 4H SiC substrates, with interface quality improved with post-oxidation annealing in nitric oxide.

To evaluate the gate oxide lifetime distribution of devices without any screening process, the team conducted constant-voltage time-dependent dielectric breakdown (TDDB) tests on 80 devices from each group.

Some devices in the 35 mΩ group failed instantly during TDDB testing, as the voltage ramped up, indicating infant failure, despite having passed prior DC testing under positive 5 MV cm^{-1} and negative 2 MV cm^{-1} pulsed gate-bias conditions.

To develop an effective screening method that minimises stress and duration conditions while addressing infant gate oxide failures, Jang and co-workers applied various screening conditions to their 35 mΩ devices (see Table 2 for details). The high-voltage pulse test conditions were devised to avoid severe degradation to the threshold voltage while providing sufficient stress, and unclamped inductive switching conditions delivered a fraction of the maximum single-event avalanche energy.

The team's testing sequence began with an initial DC test, and then more than 100 functional 35 mΩ devices were subjected to the various screening tests. 80 devices passed a second DC test, and were then subjected to TDDB tests using 9 MV cm^{-1} at 150°C.



➤ Figure 10. NoMIS has undertaken a range of screening tests: (a) threshold-voltage shift; (b) on-resistance shift; (c) avalanche breakdown voltage; and (d) drain-to-source leakage.

Results of the tests (see Figure 10) show that high-voltage pulse tests produce a shift in threshold voltage of up to 5 percent, attributed to impact ionisation in the oxide and trapping of holes in the SiO_2 and at the SiO_2/SiC interface. "This is an undesirable effect, as it may lead to the generation of new defects, and the negative threshold voltage shift is relatively permanent," remarked Jang. In comparison, the unclamped inductive switching test had a smaller impact on threshold voltage.

The changes in on-resistance mirror those in the shift in threshold voltage, but are less than 1 percent; and the avalanche breakdown voltage (BV_{DSS}) and drain-to-source leakage (I_{DSS}) do not show consistent trends.

"Overall, with the exception of the threshold voltage shift, the major parameter changes appear to be negligible," said Jang.

According to hysteresis measurements, there is no noticeable degradation of the SiO_2/SiC interface associated with the screening tests.

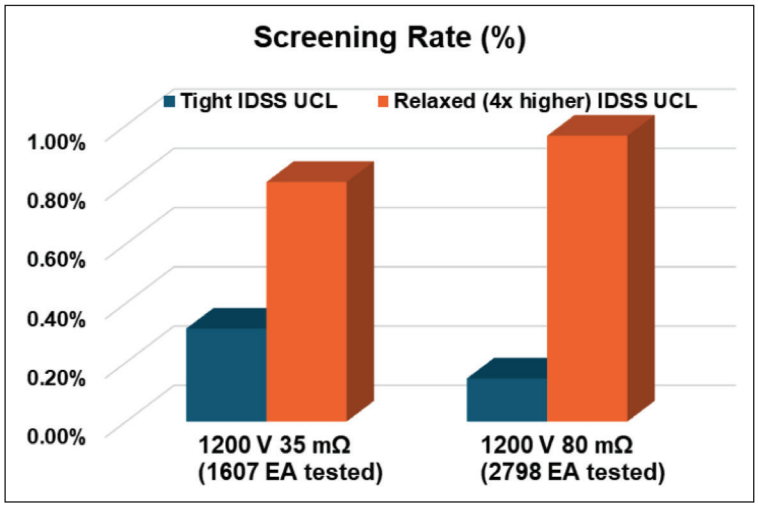
Jang and co-workers have undertaken constant-voltage TDDB tests of devices that have undergone screening, to see if this impacts infant failure, extrinsic failure, and intrinsic lifetime of the gate oxide. These investigations found that: screening did not degrade the intrinsic lifetime of the gate oxide; that after unclamped inductive switching, one infant failure in 80 devices occurred; and that no infant failures occurred after high-voltage pulse tests.

"It should be acknowledged that a sample size of 80 devices is insufficient to make definitive conclusions regarding statistical distributions, [but] the combined results from both the unclamped-inductive-switching-tested and the high-voltage-pulse-tested groups allow for a qualitative interpretation," argued Jang. "Specifically, unclamped inductive switching alone cannot screen out infant failures," added Jang, who pointed out that direct gate stressing under high-voltage pulse conditions proved to be more effective.

When it comes to extrinsic failures, the screening tests are not that effective, warned Jang, who added that only the HVP3 condition has a positive influence – that involves applying a field of 8.6 MV cm^{-1} for 1 s.

To avoid excessive negative shifts in threshold voltage and minimise excessive stress associated with unclamped inductive switching, Jang and co-workers adopted the 'combo' condition (defined in Table 2) for baseline screening. They used this to test a larger sample size, consisting of 1,607 MOSFETs with an on-resistance of 30 mΩ, and 2,798 with an 80 mΩ on-resistance.

The use of a tighter condition for screening produced a yield drop of around 1 percent compared with the more relaxed variant. This is a small trade-off against the benefit of screening-out potential risk factors.



➤ Figure 11. A comparison of the screening rate with tight and relaxed I_{DSS} unclamped inductive switching criteria.

Results (see Figure 11) show that the I_{DSS} criteria effects the screening rate. Many failures of high I_{DSS} devices during HVP1 and unclamped inductive switching indicate that leaky devices are vulnerable not only to unclamped inductive switching, but also gate oxide reliability.

Jang and colleagues have speculated that it is local defects, which contribute to a high I_{DSS} leakage, that are responsible for failures during both the high-voltage pulsed and unclamped inductive switching tests, as these defects may lead to non-uniform gate oxide formation and a non-uniform avalanche current distribution. The team plans to investigate this matter.

The use of a tighter condition for screening (see Figure 11) produced a yield drop of around 1 percent compared with the more relaxed variant. According to the team, this is a small trade-off against the benefit of screening-out potential risk factors. These insights into screening, along with the greater knowledge of the impact of oxide electric field stress, substrate material and gate oxide architecture, will help to refine the production of SiC MOSFETs. As well as the increase in availability over the coming years, customers are destined to get their hands on better products.

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A GaN-on-silicon foundation for Ga_2O_3 transistors

GaN buffer underpins high-voltage, normally-off Ga_2O_3 transistors

ENGINEERS from King Abdullah University of Science and Technology are claiming to have unveiled the first Ga_2O_3 transistors grown on GaN-on-silicon.

According to these researchers, turning to this particular form of heterogeneous integration allows the Ga_2O_3 transistor to retain its strengths, including a very high breakdown field that makes it a very promising device for power electronics, while potentially addressing its weaknesses – it is held back by a low thermal conductivity and inefficient *p*-type doping. What's more, this combination of materials could open the door to large-scale manufacturing.

When considering the various material options for underpinning the Ga_2O_3 transistor, the team dismissed SiC. While this substrate has a high thermal conductivity, it is expensive and incompatible with silicon process technology, hampering monolithic integration

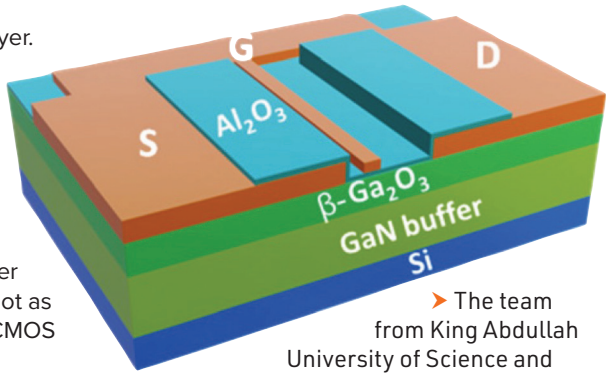
The team from Saudi Arabia view their combination of a Ga_2O_3 transistor, a GaN buffer, and a silicon substrate as a compelling one, because it is more scalable, more cost-effective, and it avoids compromising performance.

By adopting this approach, devices benefit from the strengths of GaN, including its high thermal conductivity. In addition, according to team spokesman Xiaohang Li, it's possible that *p*-type GaN might be able to tackle the poor *p*-type doping in Ga_2O_3.

Another asset of this combination is that it could create monolithic ICs that feature: high-speed control circuitry, drawing on the superior mobility of GaN; and high-power devices, produced from Ga_2O_3.

To fabricate their devices, Li and co-workers began by using pulsed laser deposition (PLD) to grow a roughly 50 nm-thick film of silicon-doped Ga_2O_3 on a semi-insulating 4.7 μm-thick GaN buffer layer.

Explaining this choice of growth technology, Li remarks: "PLD has proven to be a viable tool to grow high-quality epitaxial Ga_2O_3. MOCVD may offer moderately better materials, but MOCVD is not as compatible to the silicon CMOS process as PLD."



➤ The team from King Abdullah University of Science and Technology claim that their β-Ga_2O_3 MOSFETs break the record for breakdown voltage for this class of device on silicon substrates.

Electrical measurements determined that the film of Ga_2O_3 has an electron concentration of around 1.2×10^{18} cm^{-3}, and a mobility of just 2.1 cm^2 V^{-1} s^{-1}. Low mobility is attributed to the polycrystallinity of the Ga_2O_3 layer and defects induced by lattice mismatch.

It's claimed that mobility can be increased by adopting advanced growth techniques, such as MOCVD, and applying post-growth high-temperature annealing, which enhances crystallinity and reduces defect density.

To fabricate devices, Li and co-workers added source and drain Ti/Au terminals to their epistructure, before depositing a 25 nm-thick Al_2O_3 gate dielectric by atomic layer deposition, adding a gate metal, and then using reactive ion etching to open up source and drain pads. Transistors produced with this process have a gate length of 4 μm, a source-to-gate separation of 3 μm, and a gate-to-drain distance of 18 μm.

Electrical measurements on these devices enabled the team to calculate a sub-threshold swing of 167 mV dec^{-1} – a value that indicates a high-quality interface between Ga_2O_3 and Al_2O_3 – and determine an on-off ratio of around 10^6. At a gate-to-source voltage of 8 V, the off-state gate leakage current is around 10^{-7} mA mm^{-1}, and at a drain-source voltage of 5 V the threshold voltage is 3 V, enabling fail-safe operation.

The breakdown voltage, measured at a gate-source voltage of 0 V, has a maximum value of around 540 V. According to the team, this is the highest value for β-Ga_2O_3 MOSFETs on silicon substrates.

One alternative to the team's β-Ga_2O_3 MOSFETs on GaN-on-silicon substrates are variants produced on AlN-on-silicon. Earlier this year, such devices were reported by a collaboration led by researchers at National Chung Hsing University.

"That's a very nice work," says Li. However, he argues that there are a number of issues with β-Ga_2O_3 MOSFETs on AlN-on-silicon, including a rough surface morphology, depletion-mode operation, and a lower breakdown voltage.

"In addition, AlN-on-silicon is prone to cracks, and it is not as mature as GaN-on-silicon as a platform," adds Li. However, he believes that with more development, it is possible that AlN-on-silicon can become a good platform.

Li says that the next goals for the team include developing various power technologies associated with Ga_2O_3-on-silicon, through the use of GaN, as well as integration with *p*-GaN.

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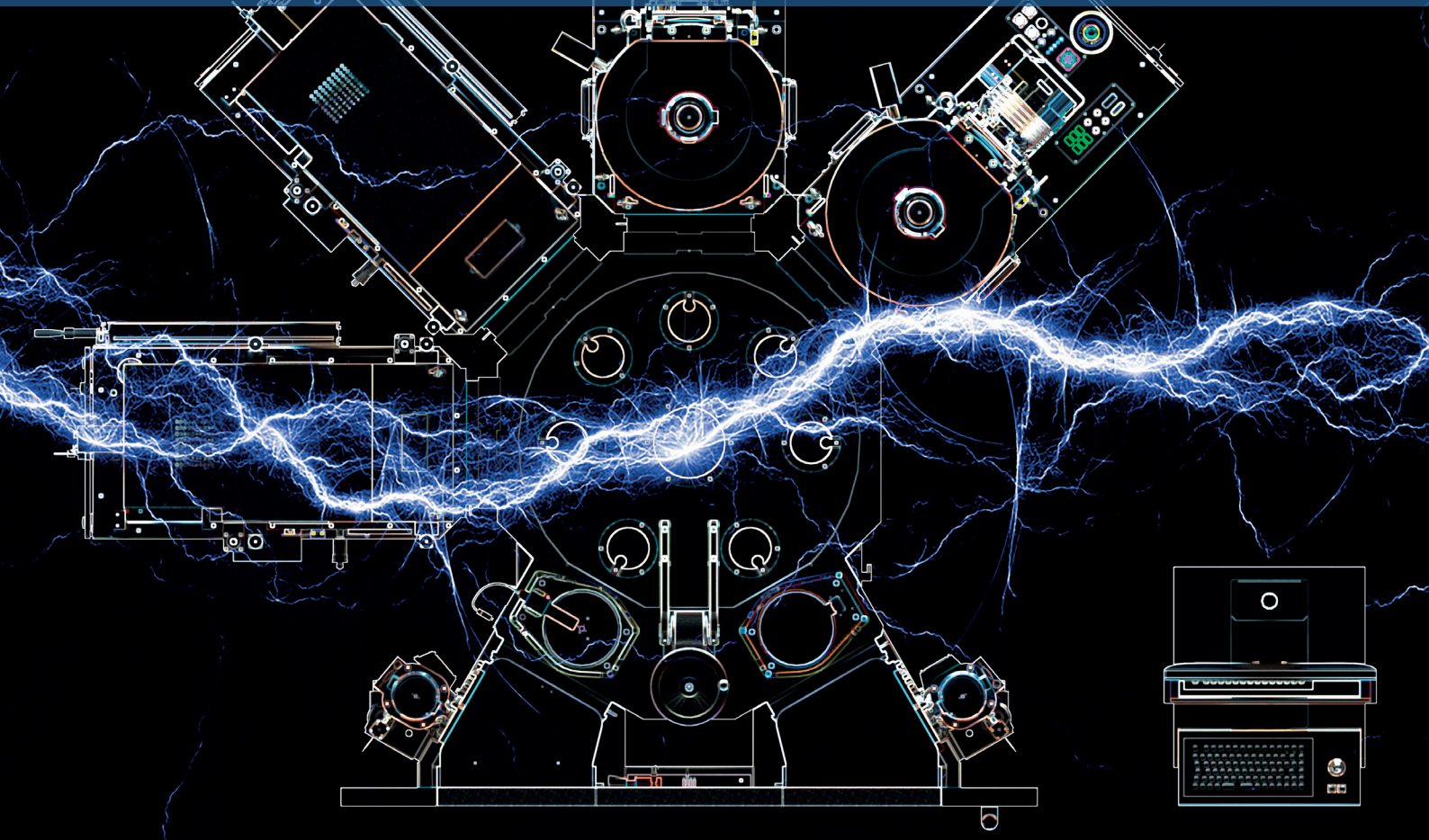

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