POWER ELECTRONICS WORLD

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Smart manufacturing in the sub-fab

Steer tech for car, power applications

Better etching enhances selective area doping

IEDM improvements in power electronics

KLA steers tech for power applications

Photoluminescence captures carbon contaminants in GaN

By researchers at Tohoku University and SCIOCS

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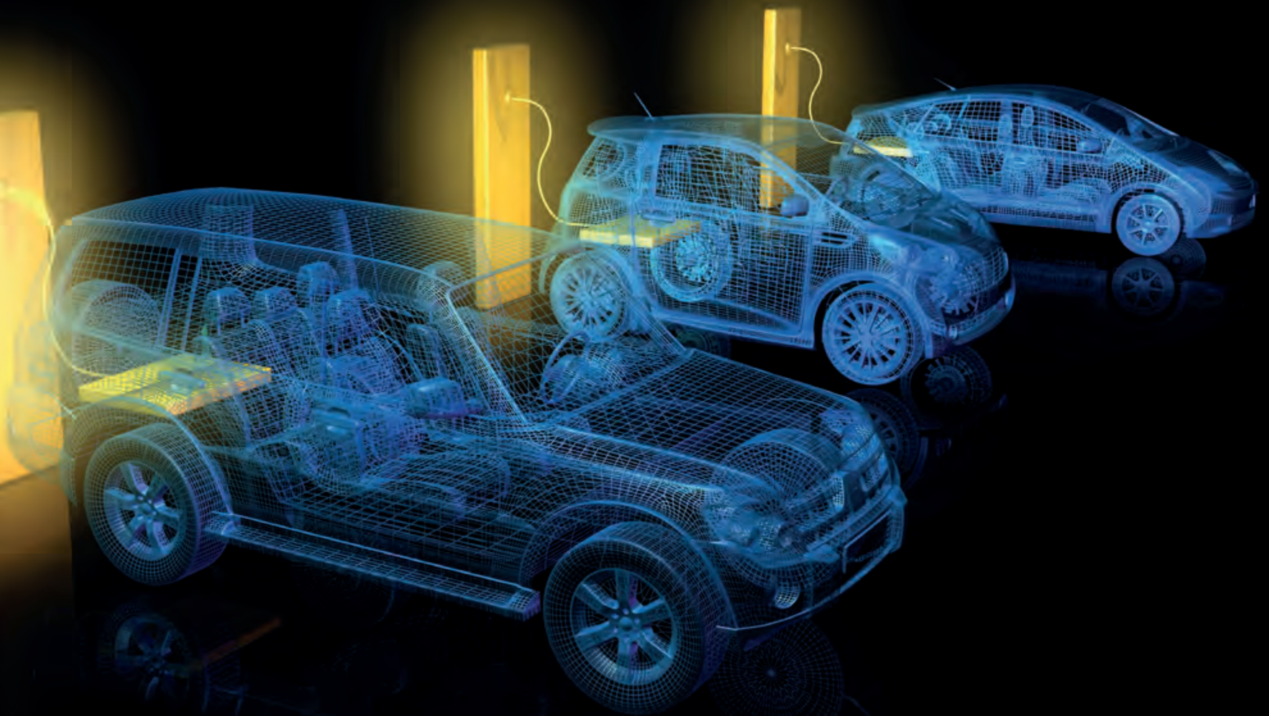

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Viewpoint

By Jackie Cannon, Publisher & Editor

Powering into 2020:

IEDM new technologies, dealing with defects

THE NEW YEAR got off to a roaring start across the power electronics industry with announcements from all supply chain sectors pointing to greater innovation and more capable products backed by R&D programmes filling product pipelines.

In this edition we profile some of the most exciting power electronics advances including an article from the editor of Compound Semiconductor magazine, Dr. Richard Stevenson in his profile of the recent International Electron Devices Meeting (IEDM). He explores methods to enhance today's mainstay of non-silicon MOSFET transistors and Schottky diodes: Silicon Carbide (SiC). Dr. Stevenson details ways to further enhance SiC performance while exploring new wide bandgap technologies including gallium oxide (Ga_2O_3). While the first commercial GaO devices will soon debut, high volume is years away as researchers seek to improve stability and yield – issues that typically impact the adoption of all technologies.

Whether at IEDM or other major industry events, ideas enabling cost reduction, defect elimination and auto sector design wins were common themes. In this edition we hear from KLA Corporation, a global leader in metrology, device inspection, packaging and emerging automotive IC applications. KLA demonstrates how to meet stringent vehicle quality and lifetime requirements that can be a decade or more compared to consumer electronics lifetimes that sometimes shrink to months.

In this Power Electronics World we also speak with Onto Innovation CEO Mike Plisinski who dives into the customer-centric advantages his team is engineering as leaders of the recently merged Rudolph Technologies and Nanometrics. We also highlight the work being undertaken by Edwards Vacuum in its quest to enhance sub-fab performance through 'Industry 4.0' preventative maintenance systems that are elevating cost savings and uptime to new and exciting levels.

Explore the latest advances in power device technologies at the Compound Semiconductor International Conference held in conjunction with the Sensor Solutions and PIC International Conferences, 31 March-1 April in Brussels. Visit: **www.csinternational.net** for more information.

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Supressing degradation in SiC p-i-n diodes and IGBTs, enhancing channel mobility in SiC MOSFETs, and improving the blocking voltage and on-resistance of Ga_2O_3 transistors all featured at the most recent IEDM meeting

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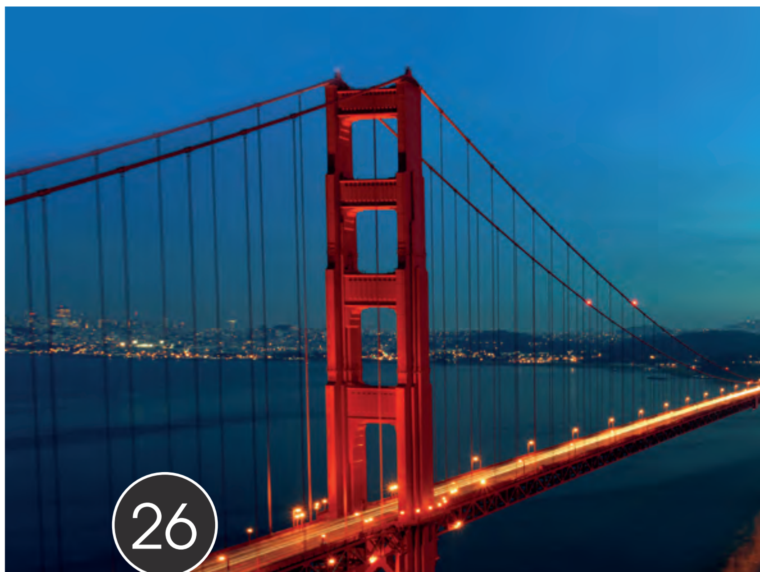
Silicon Semiconductor technical editor Mark Andrews speaks with Robert Cappel, Senior Director of Marketing, about advances that KLA Corporation has made to enable defect reduction and quality improvement processes for automotive applications



38 **Rudolph Technologies, and Nanometrics merge to form Onto Innovation**

Silicon Semiconductor technical editor Mark Andrews recently asked Onto Innovation's CEO Mike Plisinski about the merger of Nanometrics and Rudolph Technologies that formed a new company

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ib vogt sells and constructs 180 MWp PV plant in Badajoz, Spain

ib vogt has announced the sale and start of construction of the 180 MWp "Bienvenida" photovoltaic project in Badajoz, Spain. The Talanx Group, one of the major European insurance groups and institutional investor, has acquired the plant. ib vogt has set up an innovative long-term power purchase agreement (PPA) for the project with Shell Energy Europe and will perform all operational contracts for the project delivery and operation.

The Bienvenida project was initially acquired as an early stage development project by ib vogt in 2017 and developed to achieve a capacity of 180 MWp on only 175 hectares of land located in Extremadura, one of the sunniest places in Spain. With a fully wrapped EPC contract and full lifetime operation for the client, ib vogt provides a one-stop service to meet the investors needs whilst removing interface risks otherwise widely common in the market.

ib vogt has developed and successfully implemented an innovative power contracting structure with Shell Energy Europe, who will buy the produced energy. The agreement between the parties includes an attractive price hedging that balances price volatility while remaining exposed to opportunities in the Spanish power market.

"The solar park 'Bienvenida' represents an excellent fit with our direction and strategy," explained Dr Thomas Mann, Chief Investment Officer of Talanx. "The investment allows us to diversify our asset portfolio and this enables us to manage the volatility in our portfolio in a more controlled way, since we will benefit equally from wind and solar power.

"Moreover, the sheer size of the solar park allows us to better support the environmental transformation to a zero-carbon emission society – in this case by means of industrially generated green energy," he added. "Furthermore, it helps us to counteract the low-interest phase with higher returns on investment." Anton Milner, CEO of ib vogt GmbH, stated: "This project is the culmination of a number of years of development work and is the first of a series of major "grid parity" projects that we are developing in Southern Europe.

{Importantly, these will help drive the penetration of clean electricity in Europe on a stand-alone economic – unsubsidised – basis. We are delighted and proud to be working with the Talanx Group and to be able to support their sustainability and portfolio objectives.

"In Talanx we have a partner that shares our objectives and approaches in driving the implementation of this important technology in the fight against climate change. We would also like to thank all of our partners in this complex project and especially the local commune where we will be creating long term employment opportunities."

Littelfuse board helps designers try out SiC chips

Littelfuse has announced the Gate Drive Evaluation Platform (GDEV)to help designers evaluate SiC MOSFETs, SiC Schottky diodes, and other peripheral components like gate driver circuitry, so that they can better understand how SiC technologies will behave in converter applications under continuous operating conditions.

The GDEV offers quick connect header pin terminals that allow for rapid and consistent comparison of different gate drive circuits, unlike most other SiC evaluation platforms. The GDEV supports an 800 V DC link input voltage and up to 200 kHz switching frequency. Typical markets and applications for the GDEV include automotive EC/HEV charging stations, industrial powersSupplies, data centre servers, telecom case stations and solar / wind power inverters.

"The Gate Drive Evaluation Platform (GDEV) is a critical addition to our SiC technology portfolio because SiC is still relatively new and there are some unknowns surrounding the operating characteristics under various conditions," said Corey Deyalsingh, director, Power Control at Littelfuse.

"The GDEV helps engineers understand the operating characteristics of SiC devices. By utilszing this evaluation platform, designers will be better informed about the incredibly energy efficient opportunities that SiC technologies present. Equipped with that knowledge, we anticipate that designers will be more likely to incorporate SiC into their future designs."

The Gate Drive Evaluation Platform from Littelfuse enables users to evaluate continuous operation of SiC power MOSFETs and diodes under rated voltage and rated current, delivering real power to the load. It also lets them analyse system-level impacts associated with SiC-based designs including efficiency improvements, EMI emissions and passive components (size, weight, cost). Other features are include the ability to compare the performance of different gate driver solutions under well-defined test conditions, and to test gate driving circuits under continuous working conditions to evaluate thermal performance and EMI immunity.

Octopus electric vehicles and EO charging launch EV charging solution

OCTOPUS ELECTRIC VEHICLES and EO Charging launch an all-in-one EV home charging bundle to help consumers take advantage of the electric driving revolution – at hugely discounted rates.

The EO Mini Smart Home is the smallest smart electric vehicle charger in the world and is now available through Octopus Electric Vehicles in conjunction with Octopus Energy's EV energy tariff, Octopus Go.

Founded in 2015, EO has set the bar for EV charging solutions, and to date has shipped over 20,000 chargers to more than 30 countries around the world. It has released a sleek and stylish smart charger that is designed to be inconspicuous when installed at an EV owner's home. It is smaller than an A5 piece of paper, making it the most compact at-home electric vehicle charger in the world.

Octopus Electric Vehicles is an independent EV advisory and leasing business that has helped thousands of people find the right combination of vehicle, charger and tariff. It works alongside Octopus Energy's Go EV tariff, which uses dynamic time of use pricing to allow drivers to charge their car when it's cheapest or greenest – including at 5p/Kw overnight. That's 70% cheaper than legacy suppliers' equivalent tariffs and is ten times cheaper than fossil fuel cars – at just 1p per mile driving.

From April 2020, changes to Benefit In Kind taxation mean employees can get electric vehicles tax-free, via salary sacrifice schemes, at no cost to their employers. This launch anticipates a huge increase in demand for effective home charging solutions for savvy drivers looking to go electric.

Currently, many electric vehicles are sold in silo without the home charging technology and the green energy tariff. This collaboration integrates all the key components that are required for customers planning to transition to an electric vehicle.

The game-changing compact charger is available for an introductory price of £369.00. For an initial leasing cost plus £271 ongoing, customers who take advantage of the OEV bundle will get the Nissan Leaf with 8,000 miles per year, the EO Mini Smart Home charger including installation, plus the Octopus GO tariff, offering charging for just 1p per mile. The bundle is available for a limited time only.

Fiona Howarth, CEO of Octopus Electric Vehicles comments:

"Octopus Electric Vehicles is delighted to partner with EO to be able to offer this incredibly sleek, stylish and smart charger to customers. We want to make electric vehicles the go-to option for anyone considering a new car.

At-home charging technology can be a stumbling block for people looking at transitioning to EVs, as previous models available are often large and clumpy.

"The EO Mini Smart Home makes this a problem of the past. We are incredibly proud to partner with a business that has similar values to ours, one that breaks the mould and is constantly looking to innovate within the electric vehicle market to deliver affordable, convenient electric vehicle solutions."

Charlie Jardine, CEO of EO comments:

"Getting a charger installed at home should be hassle-free - and that's why we've partnered with Octopus Electric Vehicles to create the ultimate electric vehicle package."

"Electric vehicle chargers are more than 'just a plug'. They're the first piece of the puzzle in giving people energy autonomy and the future of mobility relies on the smart charging technology we're developing.

"Together with Octopus Electric Vehicles, we're making the process of getting a charger installed at home and using the government grant as simple as shopping online."

Controllis introduces high capacity rectifiers with solar integration

CONTROLLIS, a leading global supplier of low carbon and carbon neutral hybrid power solutions has added the Smart48 DC power system to its portfolio. An efficient and highly scalable power platform, the Smart48 DC power system will help telecoms, mobile and tower companies provide more reliable, efficient and green power for their networks. Operators looking to reduce their carbon footprint now have the option of combining mains rectification and solar power using a single integrated solution.

The Smart48 DC power system can provide 2kW to 300kW of power from a single 19"" rack which can be split between MPPT solar inputs and mains rectifiers. The system can also prioritise solar power over mains power, saving energy and massively reducing an operator's carbon footprint. The Smart48 can be deployed in any part of the network, from small mobile cell sites to large data centres, and will allow operators to quickly and easily upgrade their networks to run on both mains and / or solar power.

The compact system includes highly efficient hot swappable rectifier and solar modules, n+1 redundancy, intelligent fan cooling and advanced battery monitoring and management. The system also includes a controller module, multi-channel Low Voltage Disconnects and circuit breakers to protect the batteries and the site as a whole.

"The Smart48 DC power system provides the ideal solution for telecoms operators looking to save energy costs and reduce their carbon footprint." says Lee Johnson, Head of Sales and Marketing at Controllis. "It allows operators to incrementally upgrade the power to any part of their network infrastructure and easily add solar power where and when required, all from a single compact shelf."

He continues "Because we are able to prioritise solar power over mains power, operators benefit from reducing their power costs and having greener, more efficient and reliable networks."

The Smart48 DC power system is the latest offering in a series of initiatives from Controllis to provide highly efficient, reliable and green site power solutions to the telecoms industry. Alongside their low carbon and carbon neutral DC generator based hybrid power systems, Controllis provide lithium ion telecoms batteries and a range of solar power solutions.

As a data driven company, all Controllis products have comprehensive remote management with data analytics capabilities. The Controllis Smart48 DC power system is globally available along with its comprehensive portfolio of DC hybrid power solutions.

Maserati starts testing its first 100% electric powertrain

IMPLEMENTING its plans for the electrification of its range, as previously announced, Maserati has started the testing phase of its new full electric propulsion systems that will equip the future models of the brand.

Some experimental vehicles have now been built equipped with the new innovative powertrain, 100% electric with 100% Maserati technology, developed at the new Innovation Lab in Modena. During this experimental phase, the sound that will characterise the electric engine will also be developed. The next full electric models will have a distinctive signature sound, already a unique attribute of all Maserati cars equipped with traditional combustion engines.

Customers will therefore benefit from 100% electric propulsion vehicles that will combine driving pleasure, comfort and performance with a unique and unmistakable sound.

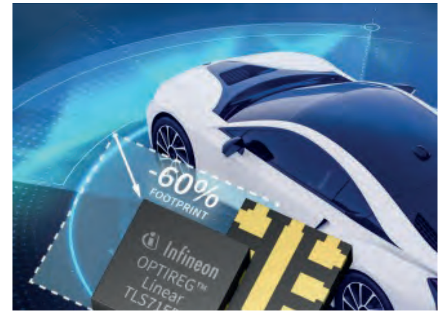
Thanks to the tests conducted in various conditions of use on both road and track, important data will be acquired for the development and definition of the new electric powertrains, which will be used for future models in the Maserati range. The new Maserati GranTurismo and GranCabrio will be the brand's first cars to adopt 100% electric solutions and will be built at the Turin production hub.

Next steps towards miniature power supplies

INFINEON TECHNOLOGIES AG is taking the next step towards smallest power supply devices for automotive electronics. As first chipmaker, the company set up a dedicated production process for flip-chip packages that is fully aligned with the high quality requirements of the automotive market. Infineon now launches the first respective product: the linear voltage regulator OPTIREG™ TLS715B0NAV50.

With flip-chip technology, the ICs are installed upside down in the package. With the heated part of the IC facing the bottom of the package and being closer to the PCB, thermal inductance can be improved by a factor between 2 and 3. The higher power density enables a significantly smaller footprint than conventional package technologies. The footprint of Infineon's new linear voltage regulator (TSNP-7-8 package, 2.0 mm x 2.0 mm) is more than 60 percent smaller than that of an established reference product (TSON-10 package, 3.3 mm x 3.3 mm) while the thermal resistance stays the same. This makes the new device particularly suitable for applications with very limited board space, such as radar and cameras. The OPTIREG TLS715B0NAV50 provides 5 V with a maximum output current capability of 150 mA.

Flip-chip technology has been used in consumer and industrial markets for several years. Due to increasingly strict space requirements, particularly in the growing number of radar and camera systems, also automotive electronics require smaller power supply solutions – albeit with much higher quality requirements. In order to offer best-in-class flip-chip quality Infineon does not rely on a subsequent qualification



of existing consumer and industrial products but rather on a dedicated production process for automotive devices.

In the future, flip-chip technology will strengthen Infineon's overall portfolio of automotive power supply products in the OPTIREG family. The chipmaker is planning to apply it also to its switch mode voltage regulators and power management ICs.

MOSFET driver for synchronous rectification from diodes incorporated

DIODES INCORPORATED announced the introduction of the APR348 secondary-side, multi-mode synchronous rectification MOSFET driver, designed for AC-DC rectification circuits in general consumer applications, notebooks, and USB adapters.

The APR348 is capable of driving the external MOSFET in both high-side and low-side secondary-side synchronous-rectifier configurations. This flexible and efficient device supports secondary-side output voltages up to 20V in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and quasi-resonant (QR) flyback modes. These options give development teams total freedom over how they implement synchronous rectification.

Manufacturers often choose an external MOSFET when implementing synchronous rectification as it provides greater efficiency converters. As the APR348 requires very few additional external components, engineers can still realize extremely small and efficient power supply designs that meet the

demands of the consumer sector. A key design feature of the APR348 is fast turn-on and turn-off times, which reduces power loss and ensures safe operation when in CCM mode. The device also features a blanking period to set the minimum turn-on period for the MOSFET; this significantly improves performance by limiting the impact of voltage ringing.

The APR348 also features a light load (LL) mode, which uses an internal timer to skip cycles when there is no load or only a light load detected at the output. This design delivers lower standby power at no load. In addition, high-side switching does not require an additional transformer winding, further minimizing the bill of materials cost.

Opel to build plant manufacturing battery cells in Kaiserslautern

SUPPORTED by the Federal Government and the state of Rhineland-Palatinate, the largest battery cell production for electric vehicles in Germany is to start at the traditional Opel location from 2024. According to Opel CEO Michael Lohscheller, around €2 billion ($2.22 billion) will be invested in the future project.

Around 2,000 jobs are to be created at the location. The Mayor of Kaiserslautern, Klaus Weichel, and the Chairman of the Opel Works Council in Kaiserslautern, Thorsten Zangerle, also paticipated in the working meeting.

Federal Minister for Economic Affairs Peter Altmaier expressed his pleasure on the European Commission reviewing and approving the first major battery project for Europe in just a few weeks. Kaiserslautern will be a part of this first joint battery project. Together with the parent company Groupe PSA and Total's subsidiary, Saft, Opel wants to found a joint venture called ACC (Automotive Cell Company) that produces battery cells for electric cars.

From 2023, the automaker wants to gradually build three blocks with a capacity of 8GWh each. Around half a million vehicles per year can thus be supplied with battery cells that will be 'Made in Kaiserslautern'.

A total of two plants with a total capacity of 48 GWh are to be built – in addition to Kaiserslautern in the Hauts de France region.

This would correspond to a production of about 10 to 15% of the expected European market. The total investment volume for this project is almost €5 billion ($5.55 billion).

ABB wins $30m power equipment order to bolster Germany's renewable energy integration

ABB has won an order worth around $30 million from Amprion GmbH, a German transmission grid operator that provides electricity to more than 29 million people, from the Alps in South of Germany to Lower Saxony, to supply phase-shifting transformers (PSTs) that will optimize power flow in the German electricity network and help in the integration of renewable resources. These transformers have the potential to offer savings of more than $110 (€100 million), over 3 years.

Power generated by windfarms is unpredictable. To keep the grid stable, electricity produced in conventional power plants must be increased or decreased at very short notice, which is both inefficient and costly. For these so-called redispatch costs Germany is paying about $1.7 billion (€1.5 billion(1)) annually.

To better control the flow of power in the existing grid infrastructure, ABB is supplying two PSTs with 2,494 megavolt amperes (MVA) capacity each, from its transformer factory in Bad Honnef, Germany.

These PSTs, amongst the most powerful in the world will enable Amprion to integrate wind power more efficiently.

ABB has been at the forefront of developing PST technology. First developed by Westinghouse Electric Corporation T&D in the 1950s and acquired by ABB in 1989, PSTs require a deep evaluation of the power system to define their optimum application and location. Their demanding size and complexity require advanced design and manufacturing skills along with stringent quality control. "Phase-shifting transformers are a specialized solution that carry out the complex task of controlling power flow in the electricity grid. This enables our customers to optimize grid investments and avoid costs when integrating renewable power like offshore wind while improving their economic viability" said Bruno Melles, Managing Director of ABB's Transformers business line, part of ABB's Power Grids business.

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Better etching enhances selective area doping for vertical GaN power devices

Multi-step etching slashes the leakage current in regrown GaN *p-n* junctions for selective area doping.

BY HOUQIANG FU, KAI FU AND YUJI ZHAO FROM ARIZONA STATE UNIVERSITY

GaN IS A VERY ATTRACTIVE material for making power electronics. It has a bandgap that is three times wider than the incumbent, silicon, and a critical electric field that is more than ten times higher. Thanks to these attributes, devices made from GaN can realise higher breakdown voltages when they have the same thickness as those made from silicon, or a similar breakdown voltage with less material.

	Si	4H-SiC	GaN
E_g (eV)	1.2	3.2	3.4
ε	11.9	9.7	10.4
μ (cm^2/Vs)	1240	980	1000
K (W/mK)	145	370	253
V_{sat} (×10^7 cm/s)	1	2	3
E_C (MV/cm)	0.3	3.1	4.9
BFOM	1	710	3,200
BHFFOM	1	84	215
JFOM	1	20	49

Table 1. Material properties and power electronics figures-of-merit (FOMs) for silicon, SiC and GaN. E_g: bandgap; ε: permittivity; μ: mobility; K: thermal conductivity; V_{sat}: saturation velocity; E_C: critical electric field; BFOM: Baliga's FOM; BHFFOM: Baliga's high frequency FOM; JFOM: Johnson's FOM. The FOMs of silicon are normalised to 1 to ease comparison.

Additional strengths of GaN devices are a low on-resistance and a high switching speed, merits that are reflected in outstanding values for various figures-of-merit (see table 1).

However, these excellent material properties are of no practical benefit unless they are harnessed in electronic devices that excel on many fronts, and lead to efficiency gains in the likes of the power grid, electric vehicles, renewables, data centres, wireless charging, and consumer electronics.

Building great GaN devices is far from trivial, with success hinging on the use of the best geometry. Early development focused on lateral GaN power devices, such as HEMTs, grown on foreign substrates. With this architecture, breakdown voltages are held laterally, and currents flow laterally. That's not ideal. Part of the problem is that there are issues associated with surface states that can lead to performance degradation, and also result in reproducibility and reliability concerns. In addition, the heat that is generated concentrates in a very narrow region, causing device temperature to rise; and the higher breakdown voltages require a larger chip area, an impediment to scalability.

To tackle these issues, our research team at Arizona State University has been developing high-performance vertical GaN power devices on bulk GaN substrates. One merit of this architecture is that it employs homoepitaxial growth, significantly reducing the density of defects, which can deteriorate breakdown voltages and increase leakage currents.

What's more, the vertical device geometry offers: higher voltages and forward currents, without

sacrificing chip area; better scalability and heat dissipation; and freedom from the effects of surface states.

This approach may raise a few eyebrows, given the high cost of GaN substrates. However, volumes have been steadily growing over the years, large size substrates with diameters of up to 6 inch are starting to emerge, and the substrate price is expected to continue to decrease, due to further expansion of both the power electronic market and that for GaN optoelectronic devices, such as laser diodes.

Vertical GaN power devices can be divided into four regions: the buffer layer, the drift layer, the channel layer and the edge-termination region (see Figure 1). We have strategies for improving each of these, leading to a boost in device performance. For the channel layer we are pursuing selective-area doping, an ongoing hot topic.

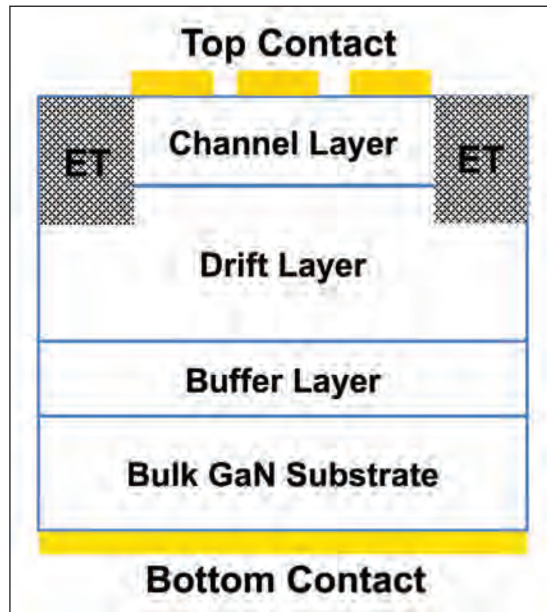

Figure 1. A cross-sectional diagram of the simplified structure of vertical GaN power devices on heavily doped bulk GaN substrates. ET indicates edge terminations

Doping challenges

Selective-area doping remains a huge hurdle for realising the full potential of GaN power electronics. The purpose of this form of doping is to create laterally patterned *p-n* junctions (see Figure 2(a)). This type of junction is needed for the fabrication of various GaN power devices, including: junction barrier Schottky diodes or merged *p-n*/Schottky diodes (see Figure 2(b)); and vertical junction FETs (see Figure 2(c)). These structures have been produced in silicon and SiC by ion-implantation, but not in GaN.

There are two reasons why it is very challenging to realise ion-implantation in GaN, especially for the production of *p*-type material. One issue is related to the subsequent thermal annealing process, needed to activate implanted atoms and recover crystal damage caused by ion-bombardment. To anneal, often the temperature has to exceed 1200 °C, but GaN begins to decompose at only 900 °C.

The second concern relates to the success of approaches to overcome this decomposition. To alleviate GaN decomposition at high temperatures, researchers have turned to capping layers such as AlN, multi-cycle rapid thermal annealing, and ultra-high pressure, but in all cases the conductivity of the implanted *p*-GaN is still very low – and judged from the perspective of power devices, it is far from satisfactory.

To overcome this particular hurdle, we have developed a re-growth method that realises selectively doped *p-n* junctions. With our approach, we can produce high conductivity *p*-GaN without having to worry about high annealing temperatures and associated GaN decomposition. This process currently remains one of the most important and promising methods for selective-area doping.

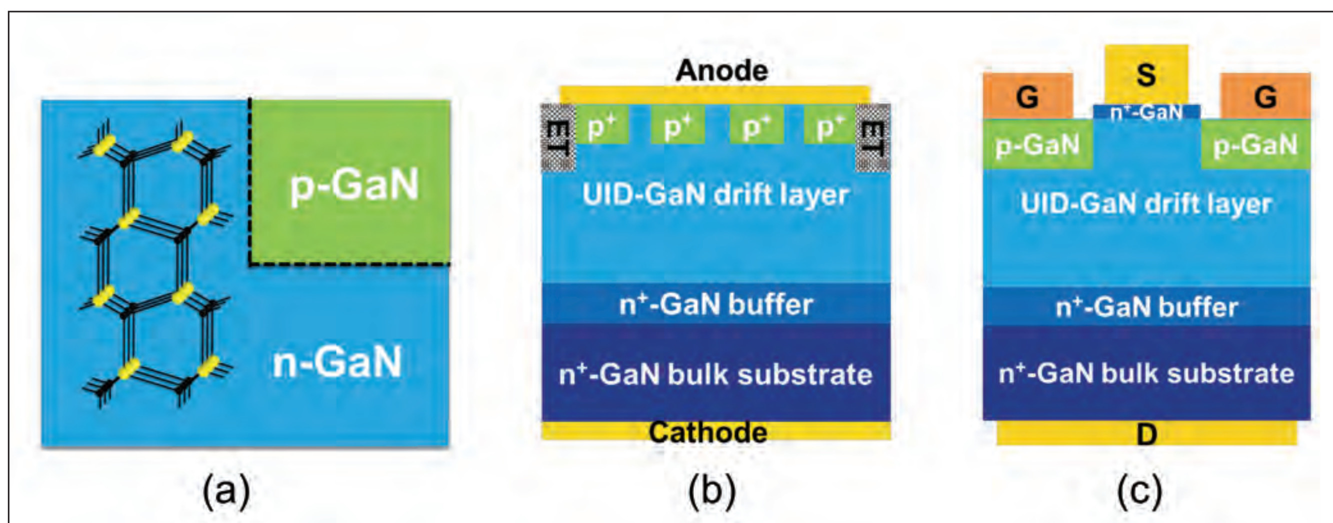

Figure 2. a) schematics of selectively doped *p-n* junctions. (b) JBS diodes or MPS diodes. (c) VJFETs.

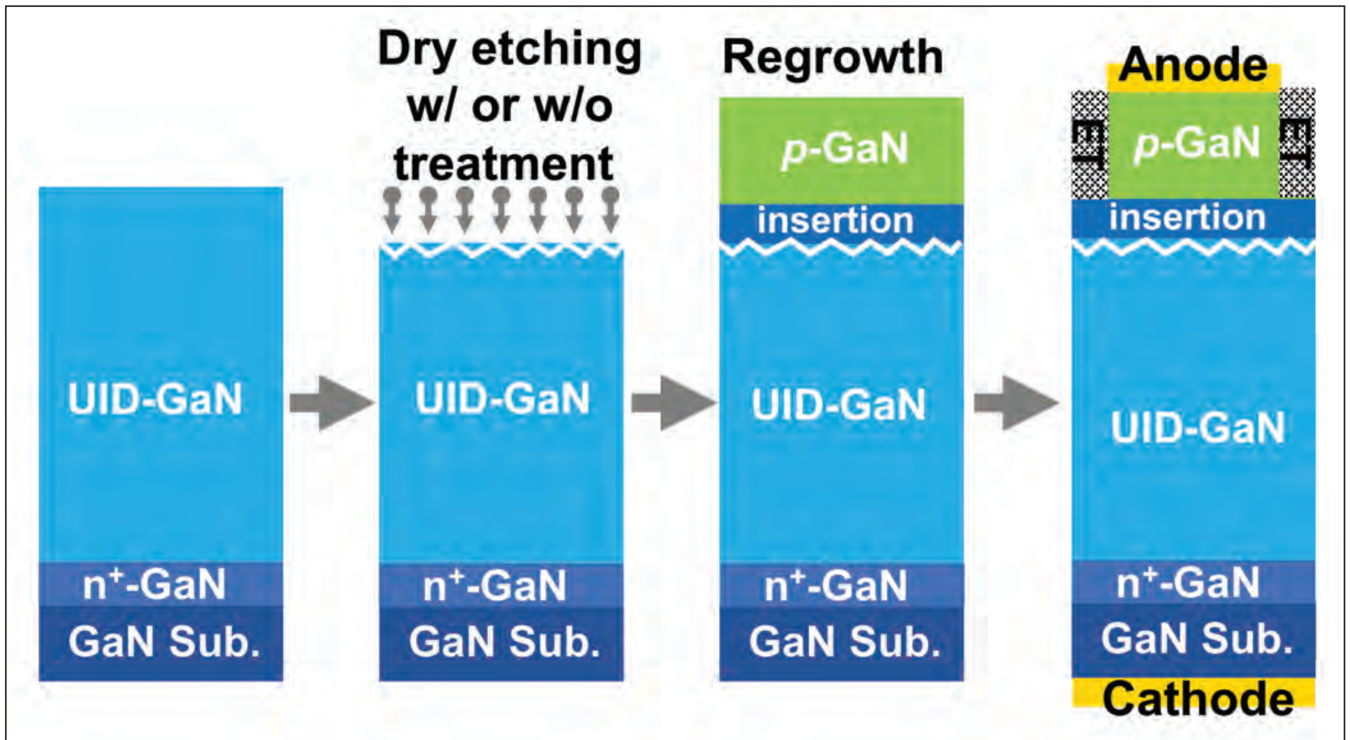

Figure 3. The growth and fabrication process of regrown *p-n* junctions formed by MOCVD. The structure is homoepitaxially grown on (0001) bulk GaN substrates. It is formed by the growth of an n^+-GaN buffer layer and an unintentionally doped (UID) GaN drift layer, before undertaking ICP dry etching and surface treatments, followed by the regrowth of a thin insertion layer and *p*-GaN. Diode fabrication includes the deposition of metal stacks for anodes and cathodes, mesa isolation and edge termination.

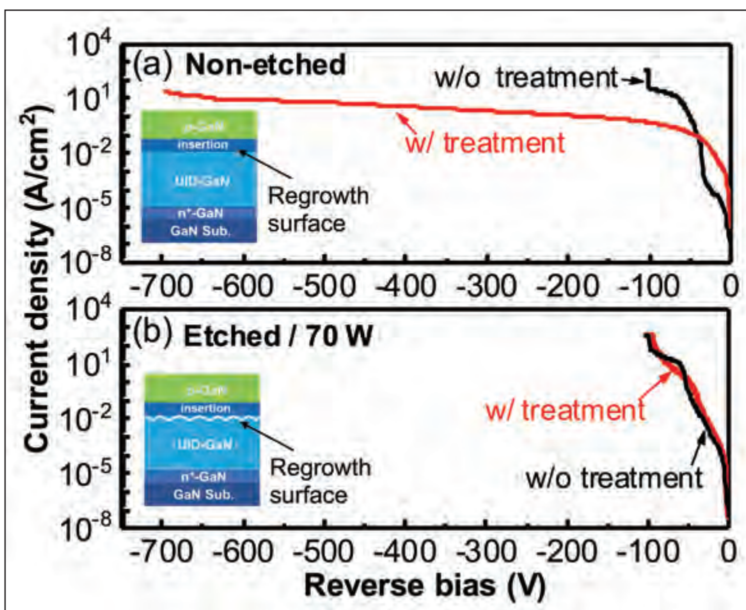

Figure 4. Reverse current-voltage characteristics of (a) non-etched and (b) etched samples with and without surface treatments. The non-etched sample was not subject to ICP plasma etching before regrowth. The etched sample was subject to ICP plasma etching, using a power of 70 W. Etching proceeds at around 200-300 nm/min, a reasonable rate for most device fabrication processes. A high etching power results in stronger ion-bombardment and more severe etching damage.

When we undertake our regrowth process, it is essential to ensure that the subsequent devices are not impaired by large reverse leakage currents, which can limit the ultimate breakdown voltage and increase power conversion losses in power electronics. Our research has uncovered two contributors to large leakage currents: surface contaminations at the regrowth interface, caused by impurities such as silicon, oxygen and carbon, all identified by secondary ion mass spectrometry; and etching damage, often caused by inductively coupled plasma etching, which is a widely used dry etching technique during GaN device fabrication.

To obtain selectively doped *p-n* junctions (as shown in Figure 2(a)), we could selectively remove part of *n*-GaN by inductively coupled plasma etching. This step would form trenches for subsequent *p*-GaN regrowth. However, this process would complicate experiments and analysis, because when two interfaces are exposed there is the possibility that leakage currents will flow in two directions. What's more, this approach is time-consuming.

To avoid these complications and speed turnaround, we begin by making planar regrown *p-n* junctions (see Figure 3). These junctions, regrown by MOCVD, have provided us with a test vehicle for obtaining fundamental knowledge on regrowth, such as the impact of inductively coupled plasma etching and surface treatments.

Evaluating etching damage

For our first set of experiments, we co-load two samples into the MOCVD reactor and regrow without any surface treatment. With this approach, we compared a non-etched sample and one etched with an inductively coupled plasma etching power of 70 W. Both samples suffer from large reverse leakage currents, highlighting the need to properly treat the surface prior to regrowth.

To realise this, we adopt a combination of UV-ozone and acid surface treatments. The former utilises powerful oxygen radicals to oxidize the surfaces and organic residue contaminants. The beauty of this treatment is that it is purely chemical, and thus free from plasma discharging. Note that with inductively coupled plasma etching, ion-bombardment takes place that can lead to charging damage and deterioration of the device's electrical characteristics. After the UV-ozone treatment, both samples are immersed in hydrofluoric acid and hydrochloric acid to remove oxidised materials and future clean the surface.

Electrical measurements reveal a massive reduction in the reverse leakage current in the non-etched sample. But that's not the case in the etched sample (see Figure 4). Our hypothesis for explaining this stark difference is that in the etched sample, etching damage is so severe that it cannot be repaired by surface treatments.

To put this theory to the test, we have carried out another set of experiments involving a lower etching power. This is reduced to just 5 W, a condition that slows the etching rate. We compare the reverse leakage currents in an as-grown sample with three samples that are first subjected to the aforementioned surface treatments. Two samples are etched with a power of 5 W, with an insertion layer thickness of 25 nm and 50 nm, respectively, and a third is etched at 70 W.

Results indicate that slow etching dramatically reduces the reverse leakage currents, and that an insertion layer helps to move the junction away from the regrowth interface, further reducing the reverse leakage current (see Figure 5). For the etched sample with an inductively coupled plasma etching power of 5 W and a 50 nm insertion layer, the reverse leakage current is lower than that in the non-etched sample and similar to the as-grown sample. The key conclusion from this experiment is that the combination of slow etching and proper surface treatments is very effective for regrowth.

Our findings prompt this question: What really drives the difference in reverse leakage currents between these samples? To find out, we have taken a closer look at the regrowth interface.

One of its characteristics that can have a significant impact on the regrowth interface, and ultimately reverse leakage currents, is the charge density. Our

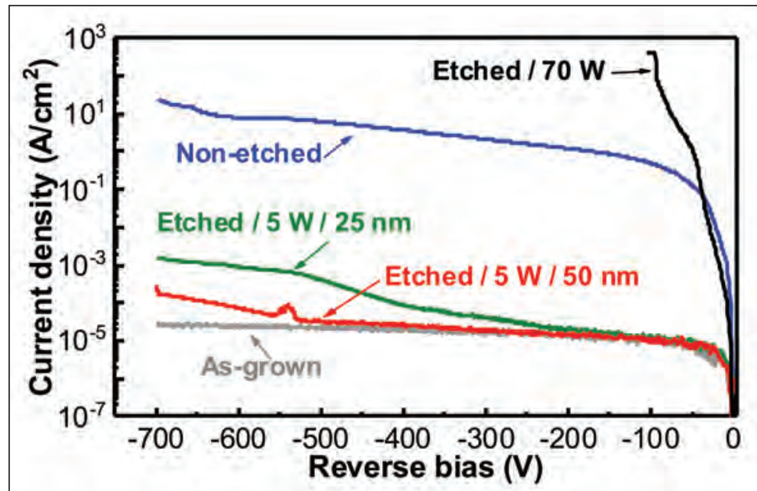

Figure 5. Reverse current-voltage characteristics of the non-etched sample and different etched samples. The power indicates the ICP etching power, and the thickness indicates the insertion layer thickness. An etching power of 5 W corresponds to an etching rate of around 20 nm/min.

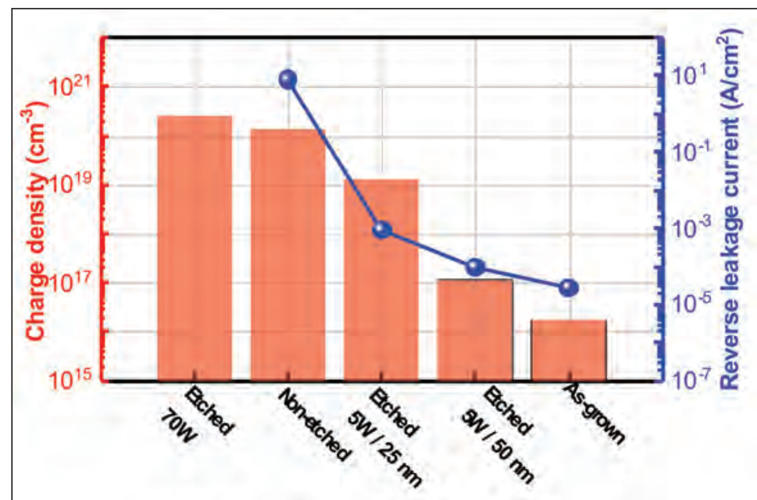

Figure 6. Charge density at the regrowth interface (histogram) and leakage current (line-shape) at −600 V for the five samples measured in Figure 5. The charge density is extracted from capacitance-voltage measurements.

measurements show that the higher the interface surface density, the larger the leakage current (see Figure 6). The as-grown sample has a low, constant charge distribution, on the order of 10^{16} cm^{-3}, while the regrown sample has a peak charge density at the regrowth interface in the range 10^{17}-10^{21} cm^{-3}. Measurements also show that a reduction in the etching power lowers the charge density at the regrowth interface, and trims the leakage current.

It is not surprising that a high density of surface charges has profound physical consequences. These charges will create a large electric field at the regrowth interface, and help carriers to tunnel through the potential barrier in the *p-n* junction and make a significant contribution to the leakage current.

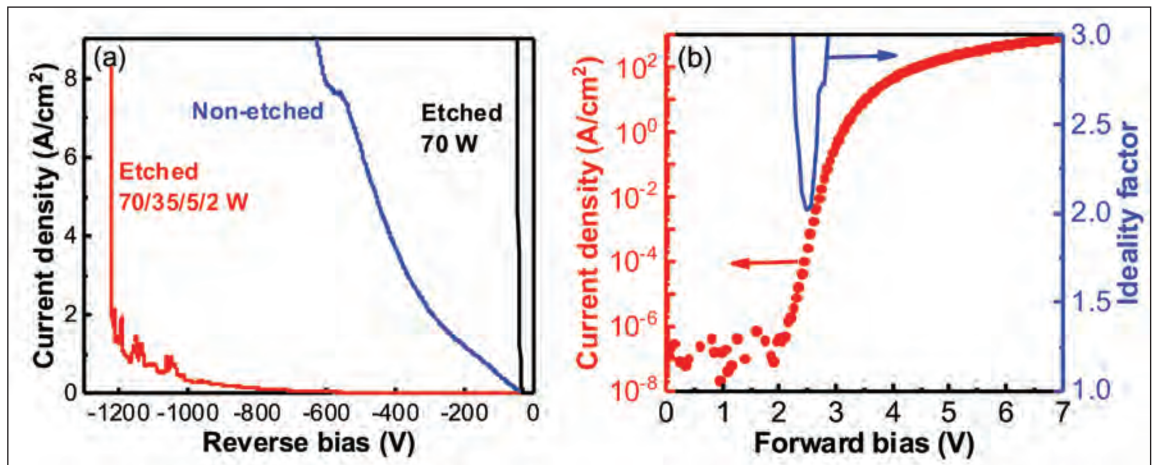

Figure 7. (a) Reverse current-voltage characteristics of the non-etched sample, the sample with the single-step etching, and the sample with the multi-step etching. All samples are subject to the aforementioned surface treatments. (b) Forward current-voltage characteristics and ideality of the sample with the multi-step etching.

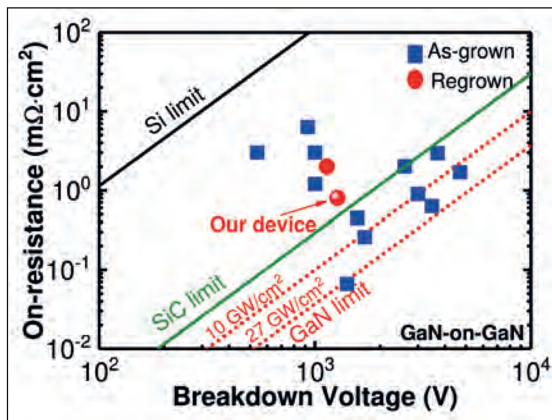

Figure 8. Benchmark plot of on-resistance versus breakdown voltage for reported as-grown and regrown GaN-on-GaN *p-n* diodes.

Multi-step etching

Although slow etching delivers the best results, it's not always practical. It can be very time-consuming, a significant impediment for some device structures with deep trenches and mesas.

To address this concern, we have evaluated multi-step etching, decreasing the ICP power from 70 W to 35 W, and then down to 5 W and finally 2 W. The four-step etching process pays dividends, producing samples with significantly reduced reverse leakage currents and the highest breakdown voltage – it can be over 1.2 kV (see Figure 7(a)).

Another benefit of this multi-step etching process is that it produces a good regrowth surface. We have compared two etched samples, both subject to a 70 W etching power. Subsequent slow etching steps, using multi-step etching, produce significant improvements in surface quality. We postulate that during multi-step etching, slow etching probably plays a role in recovering the plasma etching damage caused by previous high-power etching steps. In other words, slow etching is more like healing than etching.

Before we can herald multi-step etching as a great success, we need to make sure that it doesn't degrade the forward characteristics of regrown *p-n* junctions. Our measurements are encouraging. Samples exhibits excellent forward rectifying behaviours, with an on-off ratio of around 10^{10} and an on-resistance of 0.8 mΩ cm^2. The ideality factor, which can be used to evaluate the performance of a *p-n* junction, is also promising. Its value is around 2.0, a figure that compares favourably with previously reported values for regrown *p-n* junctions, and is close to that of our as-grown samples – they are in the range 1.5-1.8.

Baliga's figure-of-merit provides another opportunity for us to benchmark our regrown *p-n* diodes. For these devices, it is 2.0 GW cm^{-2}. That's very close to the SiC limit, and even comparable to some values reported for as-grown *p-n* diodes. Given that this work is still in its infancy, we are very encouraged by this result. We anticipate improvements in inductively coupled plasma etching, surface treatments and device fabrications, spurring the performance of GaN regrown *p-n* junctions towards the GaN limit.

In short, our results show that it is possible to produce high performance regrown *p-n* junctions via epitaxial regrowth. Our next step is to apply the obtained fundamental knowledge on regrowth to selective area doping. When progress follows, it will make a significant contribution to improving the performance of advanced GaN power electronics, and helping this class of device to create a greener planet.

Further reading

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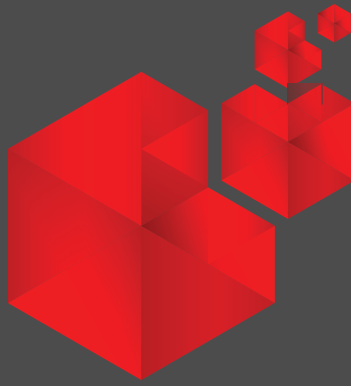

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Smart manufacturing enabled in the sub-fab

The Industry 4.0 movement is rapidly becoming the de facto means to optimize cost-effective manufacturing. Power electronic device makers want to leverage any practical idea. The experts at Edwards Vacuum point their customers to proven methods that can rapidly reduce costs while improving uptime by focusing on a part of the fab that manufacturers don't always think of first in the quest for a healthier bottom line.

BY ALAN IFOULD, ERIK COLLART, ANTONIO SERAPIGLIA, AND MICHAEL MOONEY, EDWARDS VACUUM

IN THE BROADEST TERMS, smart manufacturing refers to collecting data from all aspects of the manufacturing process and by using advanced analytical and modeling capabilities, like artificial intelligence and machine learning, process performance and productivity are improved. It has been embraced by manufacturers in all industries and hailed as the fourth industrial revolution (Industrie 4.0).

Semiconductor manufacturers have a long history of collecting and analyzing process data, a key smart manufacturing concept, to improve performance in the fab. Now semiconductor manufacturers are realizing the potential benefits of extending smart manufacturing technologies to the support systems housed in the sub-fab.

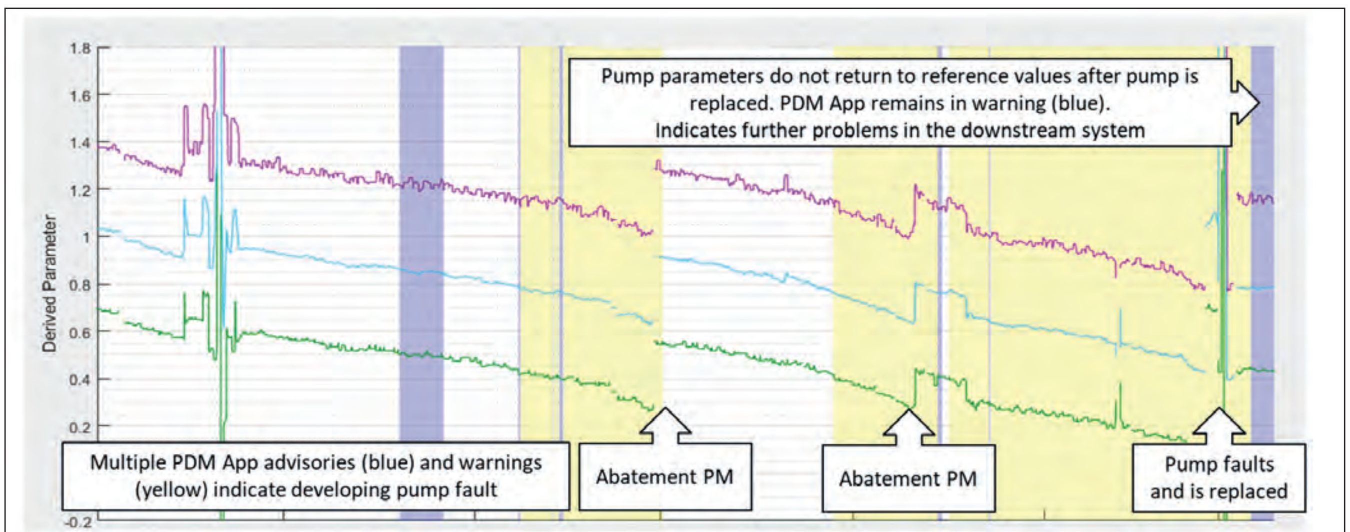

Figure 1: Output from a predictive maintenance application (PdM app) monitoring a vacuum pump

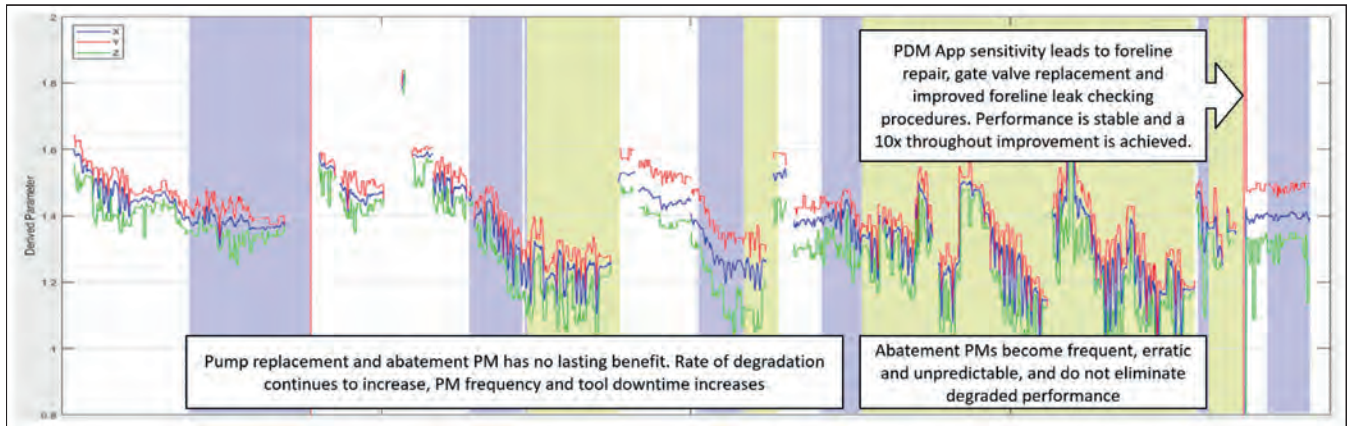

Figure 2: PdM data from a process tool in an HVM environment was delivering only 10% of the wafer throughput of other comparable tools

Driven by recent developments in the fields of sensors, data management, analytics and artificial intelligence, a new vision for manufacturing has emerged. This vision includes integrating supply chains; creating virtual factories with cyber-physical systems and digital twins; using big data techniques to interrogate tool, process, yield and facility data; and accumulating and applying critical domain knowledge. Smart manufacturing is a broad concept that is perhaps best generally described as combining technologies and solutions to optimize operations by reducing and/or managing risk and uncertainty. In more practical terms, it is using big data infrastructure and information technology to provide advanced analytics and create a knowledge network of subject matter expertise and operational excellence models. It connects people, machines and processes in a more effective way.

Semiconductor manufacturers have been using advanced automation and statistical control techniques for a long time. As fabs have become more expensive and the cost of unexpected downtime has increased, they have enhanced their capabilities using smart manufacturing concepts. They are also extending them to the critical process support systems found in the sub-fab. The sub-fab has evolved dramatically over the years, from what was originally simply a location outside the fab in which to house supporting equipment, to an environment that is in many ways as sophisticated as the fab itself. A typical HVM fab, starting 40,000 wafer per month, may have 1,500 process tools. It's sub-fab will have 2,000 vacuum pumps and 1,000 abatement systems plus other ancillary systems. Most of the critical steps in a chip manufacturing process require high vacuum conditions and the unexpected failure of a pump can bring significant disruption to the manufacturing process, imposing heavy penalties in lost productivity and scrapped product.

Smart manufacturing in the sub-fab enhances vacuum security with comprehensive monitoring of process critical vacuum and abatement equipment. Using specifically designed models and algorithms, it can predict catastrophic failure modes related to hazardous process chemicals, high flowrates of flammable gases, ingestion of solid materials and condensation of liquids and solids.

It can also deliver rapid root cause analysis for new and harsh process steps and materials, provide real-time intelligence on critical process vacuum state, accelerate yield ramp by correlating vacuum behaviour with wafer yield, and support fast installation of new sub-fab equipment.

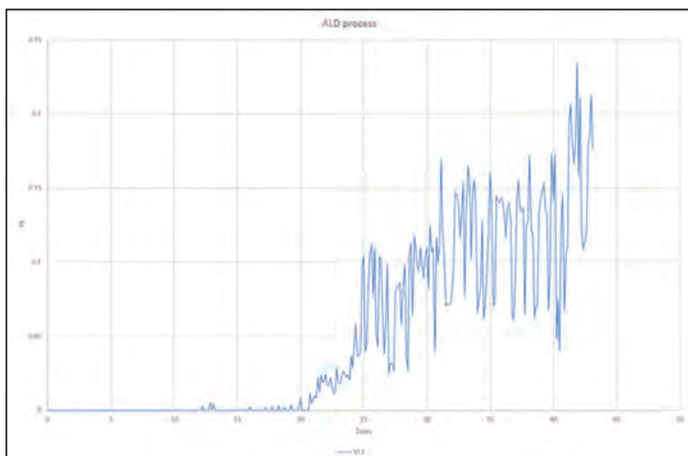

Figure 3 Vibration signal from a pump on an atomic layer deposition tool (left) and a photo of material deposited on internal components.

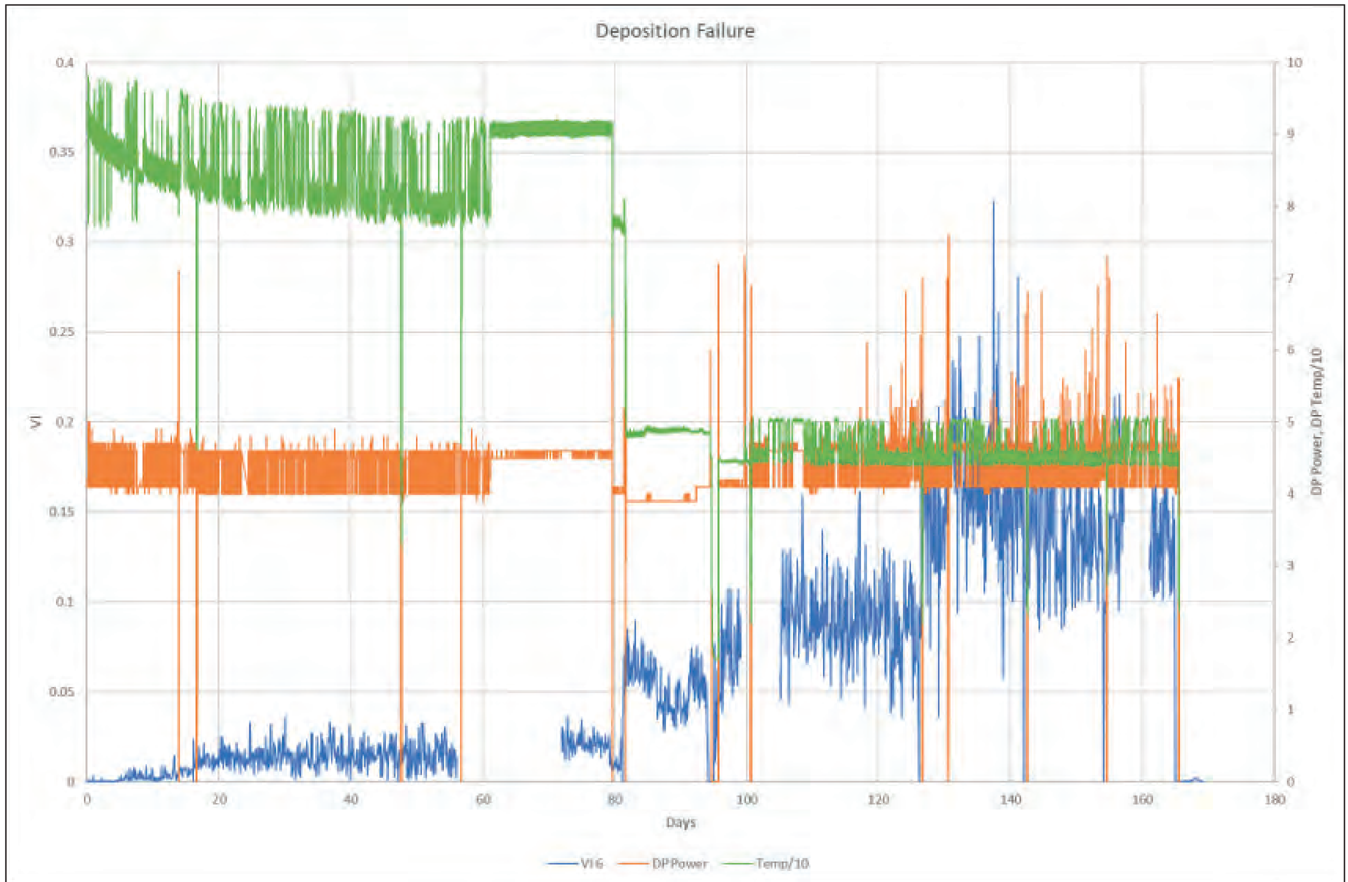

Figure 4: Dry pump power (orange) and temperature (green), and vibration data (blue) taken from a pump supporting an LP-CVD Si_3N_4 batch deposition process

A systems approach to the sub-fab

There is a growing understanding that vacuum pumps and abatement systems are not isolated, self-contained pieces of equipment. They react to each other and to the wider vacuum system that includes forelines, gate valves, other vacuum components and fab process tools. Monitoring pump parameters can reveal the health of individual pumps and also the health of up- and downstream components, including forelines, gate valves, and process chambers. Data acquired at the pump or abatement system can help determine the size and location of vacuum system leaks.

Algorithms based on vacuum science and thermodynamics can lead engineers to problems that, over time, can have a significant impact on yield. Figure 1 shows output from a predictive maintenance application (PdM app) monitoring a vacuum pump in an HVM environment. The plotted parameter is derived from a multivariate analysis and is responsive to various fault types.

The downward trend in this plot indicates gradual degradation, interrupted by a temporary re-setting. Comparing sub-fab maintenance records with parameter time stamps showed a one-to-one correspondence between reset events and preventive maintenance procedures performed on the abatement system for the same process tool, indicating that the degradation was connected to the state of the abatement equipment, rather than the health of the pump itself. This was corroborated by other pump parameters not part of the PdM app. The evolution over time further suggested that the abatement PM's themselves did not fully address the issue at hand: the derived parameters did not return to their default values and the downward trend resumed immediately. Ultimately, successful diagnosis of pump faults, combined with the successful segmentation of external downstream issues, resulted in reductions in unscheduled tool down time.

Figure 2 illustrates a case where a process tool in an HVM environment was delivering only 10% of the wafer throughput of other comparable tools. A multivariate PdM App was monitoring the vacuum pump health. The time-series plot of derived parameters clearly showed degradation over time, interrupted by abatement PM-driven re-sets. Initially, the degradation was not as severe and abatement PMs re-set the pump health as indicated by the multiple step changes. But degradation resumed almost immediately after each step improvement.

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As time went on this degradation worsened, in spite of the increasing frequency of preventive maintenance on pumps and abatement units. Multiple PdM App alerts were issued. This and other indicators pointed to leaks in the upstream vacuum system. Ultimately a thorough review and repair of forelines and gate valves resolved the issue and resulted in an improved, integrated vacuum system leak check procedure. The wafer throughput gradually returned to match the throughput of peer systems, a 10x improvement for this particular tool.

Sensorization

One of the key requirements for smart manufacturing is the development and implementation of sensors to collect and record new signals, beyond the power and temperature sensors typically used to monitor pump health and performance. An innovative vibration sensor (EdCentra Vision, Edwards Vacuum) illustrates some of the requirements and challenges encountered in this "sensorization".

Measuring vibration to monitor the health of rotating machines has a long and successful history. Intrinsic bearings frequencies can be calculated from rotation speeds, and wear-generated perturbations of these frequencies can indicate bearings faults. However, these methods do not translate well to a semiconductor environment where process-induced failure modes are more common than wear-induced. The effects of process-induced failure modes on standard vibration spectra is largely unknown and analysis is complicated by high noise levels.

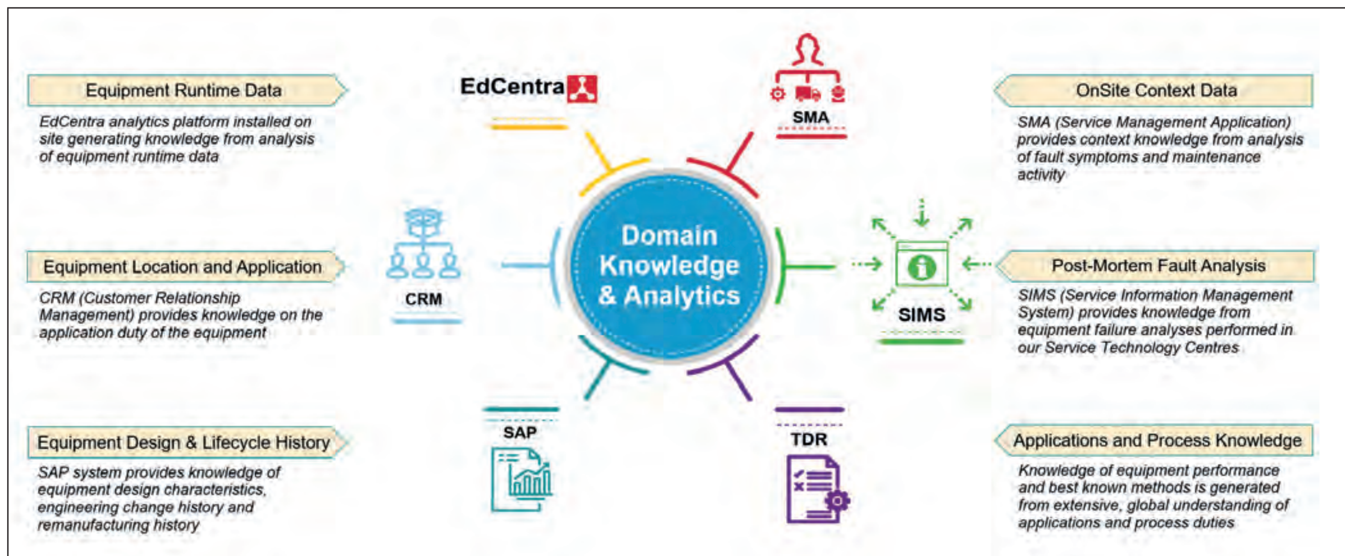
The new method unlocks key predictive information from vibration data and can detect failure modes that cannot be seen by conventional vibration detectors. It uses a retrofittable "edge" sensor module that includes both sensing and data processing capability to reduce bandwidth requirements on the communications network. Its innovative data analytics methodology translates the complex, noisy vibration signal into a single dynamic coefficient that is easy to compare with existing predictive maintenance parameters. Further vibrational sub-band analysis can provide specific failure mode identification and root-cause analysis, thus providing valuable fault classification (FC) capability.

Compared to conventional methods, the new approach increases sensitivity and provides extended, and in some cases unique, predictive maintenance capability for mechanical pump failure modes. Figure 3 shows the vibration signal from a pump on an atomic layer deposition tool. This pump was pro-actively removed from service based on the progression and value of some of the vibration parameters, even though the next calendar-based maintenance was not imminent.

Other pump parameters (not shown), failed to indicate pump deterioration. A detailed analysis of the pump after removal indicated that it was very close to faulting. The picture on the right in figure 3 shows part of the internal pump mechanism with significant process deposition and confirming the vibration-based prediction. Early replacement prevented unscheduled process downtime and potential losses from wafer scrap. The data management system used to collect this data can combine it with other pump and abatement data in a multi-variate analysis to significantly enhance predictive power and accuracy.

Figure 4 demonstrates the sensitivity of vibration analysis in tandem with traditional pump parameters used historically to monitor conditions. The figure shows an example of pump parameters, dry pump power (orange) and temperature (green), and vibration data (blue). The failure mode in this case was deposition related. As shown in Figure 4, from day 80 onward changing process conditions caused a step-change in temperature. The power curve shows developing patterns at around the 120-day mark, indicating a predictive time horizon of about 40

Figure 5: Information sources for domain knowledge



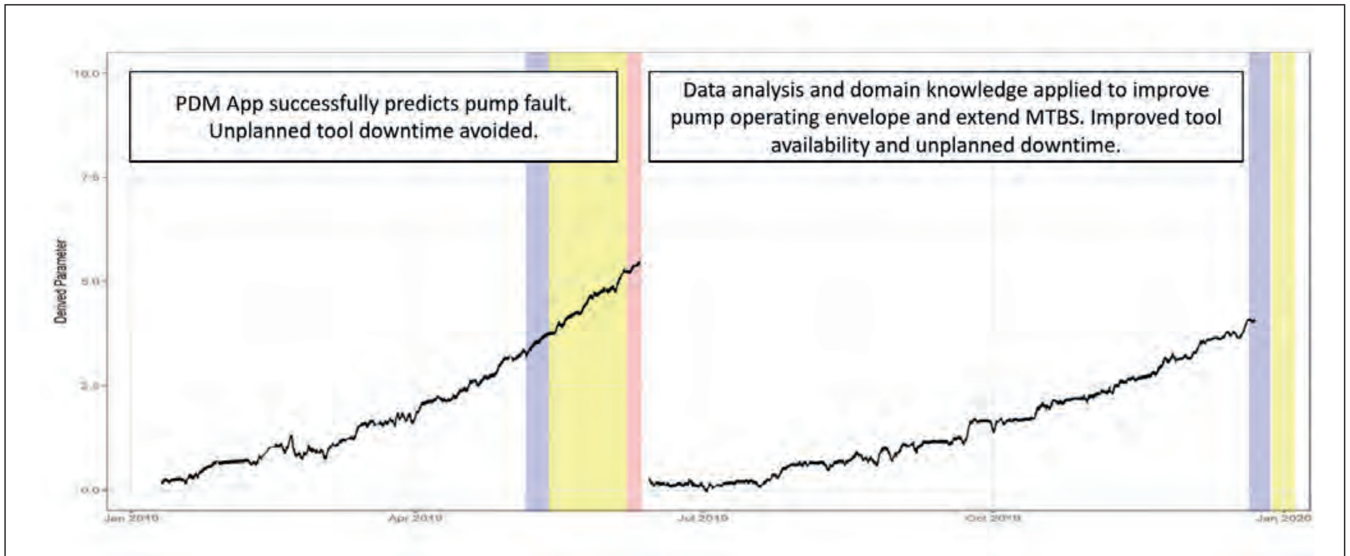


Figure 6: Application of domain knowledge improves pump operating envelop and extends MTBS

days. An important observation to make here is that the vibration data (blue curve) reacted immediately to the modal change and the increased impact of condensable process by-product adversely affecting the operation of the pump.

The heightened sensitivity of vibration gave a point-of-detection time period of around 75 days, 25 days greater than traditional pump parameters. Although vibration analysis is not a new technique, the new vibration sensor detected anomalies otherwise missed by traditional monitoring techniques. Importantly, it has added considerably to the ability to detect process-induced changes to the vacuum pump. Its implementation of edge computation reduces data volume, enables real time analytics and shortens detection latency.

Safety

No discussion of smart manufacturing can be complete without considering its potential impact on safety in the sub-fab. The sub-fab is a dangerous place, and safe working practices must be maintained alongside new business processes enabled by smart manufacturing. Examples of potential benefits include: providing advance notice of required equipment interventions so that activities can be better planned, thereby reducing risk and uncertainty associated with the time pressure of urgent activities; using technology to deliver safe standard operating procedures (SOP) and best known methods (BKM) for equipment installation; and incorporating safety data and observations along with asset performance data in the domain knowledge that drives a holistic approach to reducing risk and uncertainty.

Domain knowledge is central

Domain knowledge and subject matter expertise are key in providing the right context for any type of machine learning and data science application within smart manufacturing. They are key for several reasons, including the complexity of the manufacturing process, the dynamic nature of day-to-day operations and the general unavailability of large, unambiguous and consistent data sets. People will manage, operate and optimize machines with the

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help of digital technologies. Processes will define the interaction of machine to machine, people to machine, and people to people. This constitutes a domain knowledge supply chain essential to enabling smart manufacturing.

For sub-fab vacuum and abatement equipment, domain knowledge encompasses multiple areas of know-how, ranging from specific knowledge of how a process or a piece of equipment works to all the ways the process interacts with the world in which it exists. Vacuum science and thermodynamics provide the basic laws governing critical parameters such as pressure, flow, temperature, and pumping speed. These all display linear and non-linear responses, instantaneous changes, and long-term trends that need to be considered.

Equipment behavior is also ruled by the details of electronic sub-assemblies and mechanical construction. This specific domain knowledge is, for instance, required to distinguish between normal, instantaneous power spikes from pump-vent cycles or powder ingestion and abnormal power spikes from gradual film deposition over long periods of time. A third area relates to the sequence of wafer processing vs. idle and how it affects parameter behavior over time.

Equipment behavior is also ruled by the details of electronic sub-assemblies and mechanical construction. This specific domain knowledge is, for instance, required to distinguish between normal, instantaneous power spikes from pump-vent cycles or powder ingestion and abnormal power spikes from gradual film deposition over long periods of time

The last areas of domain knowledge, measured and inferred alert states and measured degradation states, relate to quantifying and calibrating the progression of abnormal behavior against PdM alert states. Depending on process and equipment type different parameter sets and thresholds may be needed to accurately capture this.

Figure 5 summarizes sources of information that provide critical input for developing domain knowledge.

Figure 6 shows a practical example of domain knowledge at work. PdM Apps, built using domain knowledge, were used to monitor the condition of the pump. The first blue/yellow/band indicates a successful fault prediction that eliminated an unscheduled tool down event. Domain knowledge was then applied to change the operating envelope of the vacuum system. Note the right-hand side of the graph shows a much slower degradation of performance before a second successful fault prediction. This delivers the additional benefit of a longer MTBS and thus tool availability.

Tying it together – operational excellence

Smart manufacturing connects people, machines and processes. The full benefit of any smart manufacturing strategy is only realized once these three elements work effectively together to reduce and/or manage risk and uncertainty. Considering the examples discussed, a PdM App may provide a good indication of a fault condition, but further action is needed to eliminate the root cause of the problem and design out the cause of faults from machines or the processes that support them. New sensors provide more information than ever, but processes are needed to bring new learning to fruition. It is always worth reiterating safety: safe working practices must be maintained alongside new business processes enabled by smart manufacturing. A strong subfab management strategy includes a strong operational excellence model to drive safe and stable operations. Operational excellence incorporates four key areas: standards and procedures; team competency and capability; operational models; and knowledge systems. This is the holistic approach required to provide the solid foundations from which data-driven decision making and improvement activities can be achieved.

Summary

Smart manufacturing in the sub-fab combines real-time data with specific domain knowledge to optimize equipment performance. Improved performance enables significant improvements in productivity and yield. A successful implementation of smart manufacturing requires that sub-fab vacuum and abatement systems be treated as a whole as well as individually. Application of big data techniques, data mining, artificial intelligence and machine learning will certainly reveal new relationships within the data, especially as the number and types of sensors grows and data is integrated across the fab, sub-fab and entire manufacturing ecosystem. Operational excellence models will provide the safe and solid foundations needed to realize the full benefits of new learning.

Photoluminescence captures carbon contaminants in GaN

Omidirectional photoluminescence offers a non-destructive method for measuring the density of carbon contaminants in GaN

CARBON IMPURITIES limit the performance of GaN devices. They create deep levels in the material, leading to leakage currents.

To reduce the levels of carbon contaminants, the first step is to quantify this impurity in the nitrides. Unfortunately that's not easy, because conventional approaches are slow, destructive, and limited in sensitivity. But all these issues can be overcome, according to recent work by a collaboration in Japan between researchers at Tohoku University and SCIOCS.

Spokesperson for this partnership, Kazunobu Kojima from Tohoku University, claims that the team have shown that omidirectional photoluminescence spectroscopy offers a non-contacting, non-destructive, high-sensitivity technique for detecting carbon levels in GaN. Kojima says that even when they examine some of the world's purest GaN crystals, they can measure their carbon content.

The established approach for determining the concentration of elements in compound semiconductor materials is a destructive method known as secondary ion mass spectrometry (SIMS). Using standard depth profiling, this technique has a detection limit for carbon of 3 x 10^{15} cm^{-3}. This limit falls to 5 x 10^{14} cm^{-3} by switching to a raster change approach.

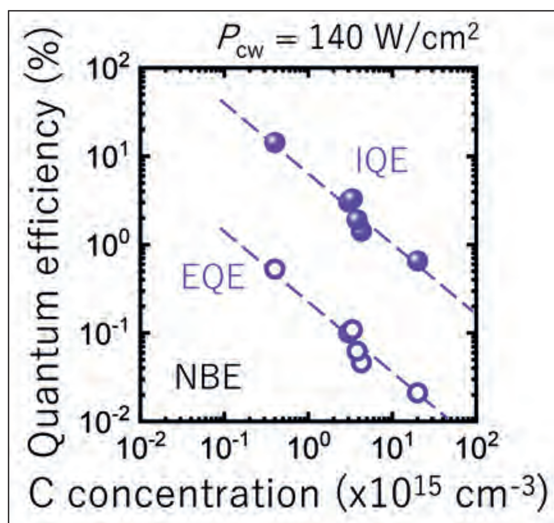
In comparison, the limit for omidirectional photoluminescence spectroscopy is far lower. A conservative estimate is 10^{14} cm^{-3}.

Another strength of omidirectional photoluminescence spectroscopy is its capability to detect very deep levels formed by point defects. "[These levels are] too deep to detect by deep-level transient spectroscopy, a popular method to detect impurity and defect levels in semiconductors," says Kojima.

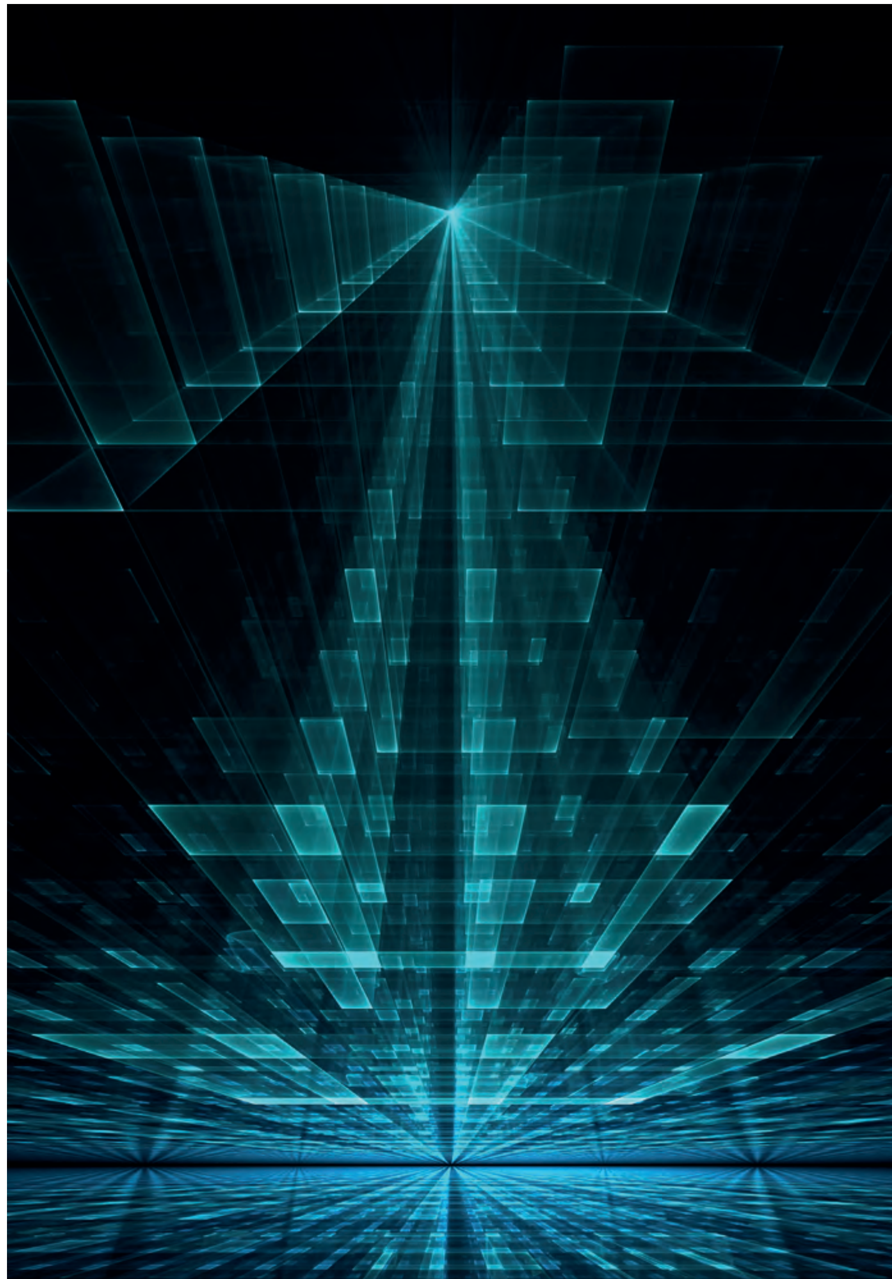
The team have studied six samples – four grown by MOCVD, and the other two by HVPE. Measurements with a SIMS tool with a detection limit of 7 x 10^{14} cm^{-3} reveal that these samples provide a range of carbon impurities. One of the HVPE-grown samples has a carbon concentration below the detection limit, another a value of 2 x 10^{16} cm^{-3}, and MOCVD-grown materials have values between 3 x 10^{15} cm^{-3} and 4.3 x 10^{15} cm^{-3}.

In addition to measuring the external quantum efficiency of the samples, Kojima and co-workers have calculated the internal quantum efficiency by using a streak camera to record the photoluminescence lifetime.

Under excitation, the GaN samples produce photoluminescence over wavelengths ranging from 1.5 eV to 3.5 eV. For the near band-edge emission, which is related to carbon impurities, both the internal and external quantum efficiencies monotonically increase with carbon concentration (see figure). As the



Internal and external quantum efficiencies of near band edge (NBE) photo-;luminescence provide a method to measure carbon concentrations in GaN.



near-band edge external quantum efficiency is only 1 percent at a carbon concentration of 4 x 10^{14} cm^{-3}, it is possible that concentrations below 10^{14} cm^{-3} could be measured with this technique.

Measurements of photoluminescence lifetime show that this decreases from 0.78 ns to 0.32 ns as the carbon concentration falls from 2 x 10^{16} cm^{-3} to 3 x 10^{15} cm^{-3}. For lower concentrations, the photoluminescence lifetime plateaus. To try and understand the reason for this, Kojima and co-workers have plotted the radiative and non-radiative lifetimes as a function of concentration – the former has a steady increase with concentration, while the latter mirrors the photoluminescence lifetime. This led the team to postulate that samples contain vacancy-related intrinsic non-radiative recombination centres, with an estimated density of 2.1 x 10^{15} cm^{-3}.

IEDM details improvements in power electronics

Techniques for supressing degradation in SiC *p-i-n* diodes and IGBTs, enhancing channel mobility in SiC MOSFETs, and improving the blocking voltage and on-resistance of Ga_2O_3 transistors were all unveiled at the most recent IEDM meeting

BY RICHARD STEVENSON

TURN ON THE NEWS and there's a good chance you'll hear a story related to climate change. Recently the focus has been on the devastating fires in Australia, but in the last few months you may also have read of accelerated ice-melting in Greenland, demolition of homes in Rwanda to protect citizens from flooding, and the breaking of global temperature records.

For those of us that see climate change as man-made, our challenge is to modify our lifestyle, so that we help to curb carbon emissions. Some of the changes that we could consider may not be to our liking, such as switching to a more plant-based diet and taking fewer flights to sunny climes. But there is one change that we will applaud: far greater deployment of more-efficient power electronics, based on devices made from alternatives to silicon.

Leading this charge is SiC. Sales of diodes and transistors made from this material are ramping fast, as the uptake of these devices branches out from their deployment in power supplies and inverters to electric vehicles, where they enable an extension to the driving range. Far behind, but with even greater promise, is gallium oxide, a material with an even wider bandgap. It will not be long before the first commercial Ga_2O_3 devices appear on the market, but significant sales are still some years away.

For both SiC and Ga_2O_3, long-term success hinges on making the devices better and better. Performance must improve, alongside reliability. To succeed, more research is needed to understand the behaviour of the diodes and transistors, and how modifications to designs impact device behaviour.

Presentations detailing progress of this nature were detailed at the latest International Electron Devices Meeting (IEDM). Held in San Francisco between 7 and 11 of December, researchers at IEDM 2019 described techniques to suppress bipolar degradation in SiC *p-i-n* diodes and IGBTs, improve the characteristics of the channel in SiC MOSFETs,

and a Ga_2O_3 transistor architecture that sets a new benchmark for breakdown voltage.

Supressing bipolar degradation

Sales of SiC power devices are dominated by Schottky barrier diodes and MOSFETs. Within this commercial product portfolio there are devices designed to operate between 600 V and 3.3 kV. Higher voltages are possible, but for values of 10 kV and above, SiC *p-i-n* diodes and IGBTs appear to be better alternatives. However, if this pair of devices are to fulfil their potential, a condition known as bipolar degradation must be addressed. This degradation occurs when current passes through these devices and stacking faults arise, leading to an increase in forward voltage. Note that a solution to this impediment could have wider implications, as this type of affliction may also occur in body *p-n* diodes of SiC MOSFETs.

The origin of stacking faults in bipolar devices is basal plane dislocations in the substrate. This form of imperfection comprises two partial dislocations, on either side of a narrow single Shockley stacking fault. Fortunately, during the growth of the epilayer, most of basal plane dislocations are converted into threading edge dislocations. However, a few propagate into the epilayer – most of them are in the form of screw-type basal plane dislocations.

When basal plane dislocations are in the epilayers, once the carrier density exceeds a threshold, there is an expansion of single Shockley stacking faults (see Figure 1). Eventually, right-angled triangular single Shockley stacking faults are formed across the current pass of the device, leading to an increase in forward voltage.

At IEDM several approaches to combat bipolar degradation were described by Hidekazu Tsuchida from Japan's Central Research Institute of Electric Power Industry (CRIEPI).

Tsuchida, who is working with colleagues at CRIEPI, the National Institute of Advanced Industrial Science and Technology and Fuji Electric, says that it is unrealistic to expect a complete elimination of basal plane dislocations through refinements in bulk growth technology. "The average basal plane dislocation density on 'good substrates' has decreased a lot in the last decade. However, we still have a large variation in the quality of commercial SiC substrates." In his opinion, the way forward is to eliminate basal plane dislocations in the epilayers by growing well-chosen heterostructures on good commercial substrates.

Back in 2018, Tsuchida and co-workers reported a study involving the fabrication of SiC *p-i-n* diodes. This effort involved using electroluminescence to determine the threshold current associated with the expansion of single Shockley stacking faults. By measuring the charge in the drift layer during turn off, the researchers converted the current density to a hole density. This revealed that the threshold for the hole density in an *n*-type layer is 1-2 x 10^{15} cm^{-3}.

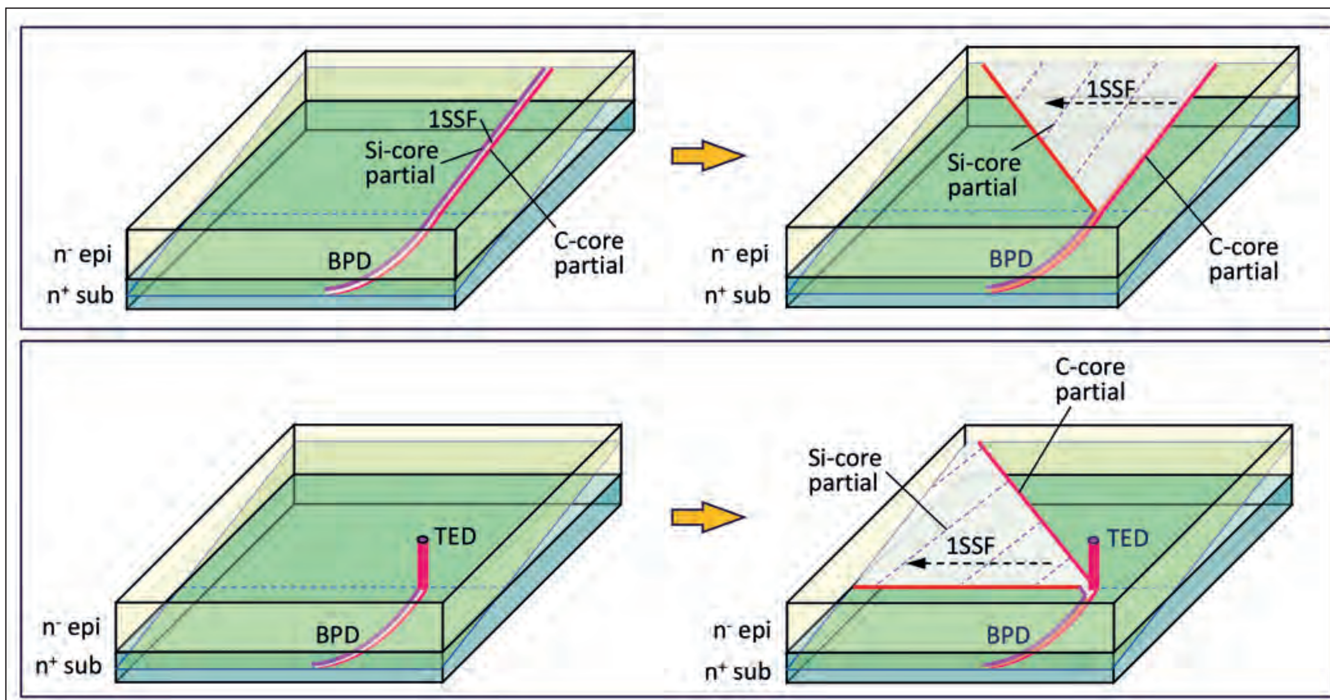


Figure 1. Basal plane dislocations (BPDs) in the substrate can propagate into the epilayer (top left), or be converted into threading edge dislocations (TEDs). Most of the BPDs in the epilayer contain a pair of partial dislocations – one with a silicon core, and the other with a carbon core – with a single Shockley stacking fault (1SSFs) between them. Once the carrier density exceeds a threshold, there is an expansion of 1SSFs from the BPDs in the epilayers to create a right-angled triangular 1SSF (top right). This expansion forms across the current pass of the device, leading to an increase in forward voltage. There can also be an expansion of 1SSFs, involving bar-shaped 1SSFs to expand from the BPD segment below the BPD-TED conversion point (bottom right). This can be caused by the injection of minority carriers into a region below the BPD-TED conversion points located near the epilayer and substrate interface, and also in substrates with a high density of BPDs.

Based on this insight, Tsuchida and co-workers argue that two criteria must be met to ensure the suppression of bipolar degradation. They are the elimination of basal plane dislocations from the region where minority carriers are injected, and the reduction in the minority carrier density to a level below threshold in the region where basal plane dislocations exist.

According to Tsuchida, both these requirements are needed because even if basal plane dislocations in the substrate are perfectly converted to threading edge dislocations at the interface between the epilayer and the substrate, minority carriers are still injected into the substrate. Here, the danger is that the density of these carriers exceeds the local threshold, triggering conversion of the basal plane dislocations in the substrate into stacking faults.

The solution, according to Tsuchida, is to insert a buffer layer with a short carrier lifetime between the substrate and drift layer. This addition reduces the injection of minority carriers into the substrate region.

Initially, the team turned to nitrogen doping to reduce the carrier lifetime in the buffer. However, when the nitrogen concentration exceeded 1-2 x 10^{19} cm^{-3}, this introduced an imperfection known as a double Shockley stacking fault. Keeping the nitrogen concentration low enough to avoid this shortened the carrier lifetime to around 40 ns.

To further reduce this lifetime, Tsuchida and co-workers have recently switched to doping with vanadium, a deeper dopant. When present at a concentration of just 7 x 10^{14} cm^{-3}, room-temperature carrier lifetime is shortened to just 13 ns.

The benefit of vanadium doping has been assessed by comparing two sets of SiC *p-i-n* diodes. Controls features a 10 mm-thick, nitrogen-doped drift layer grown on an *n*-type substrate, and modified variants have an additional buffer, doped with vanadium and nitrogen, inserted between the substrate and drift layer.

To evaluate the impact of the buffer, measurements were made on 16 controls and 16 variants. Initial forward voltages, recorded at a 18 A drive current, were compared with values after one stress test and then another. The first involved driving diodes at 300 A cm^{-2} for an hour, and for the second, devices were run at 600 A cm^{-2} for an hour. Analysis of the results showed that the buffer layer leads to a substantial reduction in variation of forward voltage after operation.

Further insight into the difference between standard devices and those with a doped buffer has come from photoluminescence measurements. This optical technique exposed single Shockley stacking faults in the conventional diode, and the absence of these faults in the modified design (see Figure 2).

Buffer layers may also benefit SiC IGBTs. This type of device would require a *p*-type buffer layer with a short carrier lifetime. Aluminium, which forms a shallow acceptor, is a candidate for doping, as increases in its concentration reduce carrier lifetime. Tsuchida and co-workers suggest that this might be combined with boron, which greatly shortens carrier lifetime.

One of the goals for the team is to map, with precision, the locations across a wafer where basal plane dislocations are converted into threading edge dislocations. Such a study promises to enable a more detailed, quantitative understanding of the expansion of single Shockley stacking faults, and could also aid the development of drift and buffer layers that improve the performance of bipolar devices.

Another target for the researchers is the development of a fast growth technique for making 4H SiC that will trim the density of basal plane dislocations and threading dislocations. The team have already made much progress, realising a growth rate of 3 mm/hour. "[That's] about ten times higher than a typical PVT growth," says Tsuchida.

MOSFET modifications

The introduction of a new dopant is also behind the improvements made to the performance of SiC MOSFETs. This success, realised by a team from Mitsubishi, involved the introduction of oxygen doping. It led to a significant reduction in channel resistance and an increase in the threshold voltage.

Both of these attributes are highly desired by the designers of power electric systems. Reducing resistance cuts energy losses, and a higher threshold voltage makes it easier to control the system. Normally these improvements are realised by nitridation. However, if the threshold voltage exceeds 3 V, this comes at the expense of a hike in channel resistance.

The team from Mitsubishi have previously addressed this weakness by switching to sulphur. And at IEDM they revealed the results of using another alterative, oxygen, which is a far deeper donor. Spokesman for the team, Munetaka Noguchi, claims that there are no downsides to the use of deep donors. He arrived at this conclusion after considering the results of pulsed measurements that enable an estimate of threshold voltage stability.

Noguchi and co-workers have produced vertical and lateral SiC MOSFETs with oxygen doping. For commercial sales, vertical MOSFETs are preferred.

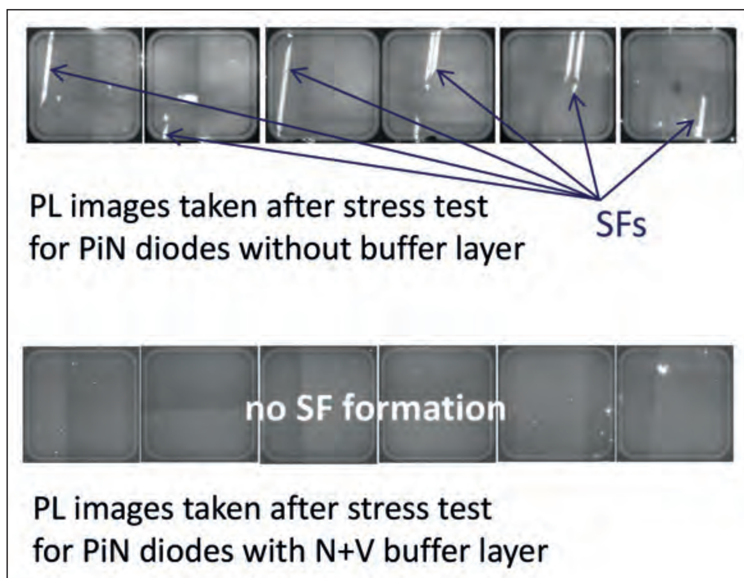


Figure 2. Photoluminescence measurements on *p-i-n* diodes that have been subjected to a stress test show that the addition of a buffer layer (bottom set of devices) eradicates the formation of single Shockley stacking faults.

"We used lateral MOSFETs as a test structure to evaluate channel performance," explains Noguchi.

Ion implantation provided a relatively high concentration of oxygen near the channel. Note that such a high concentration is not possible with simple thermal oxidation. Following thermal activation of oxygen, the team formed the gate oxide with thermal oxidation and nitridation in dilute nitrogen oxide.

Measurements of the capacitance of the MOS capacitors in the lateral MOSFETs revealed that at elevated temperatures the introduction of oxygen increases capacitance in the depletion region. This work also revealed that oxygen acts as a donor, rather than an acceptor-like trap.

Additional benefits of the introduction of oxygen in lateral SiC MOSFETs include a 46 percent reduction in channel resistance, realised for a threshold voltage of 3.9 V.

Vertical MOSFETs with oxygen doping also produce encouraging results. Devices with a threshold voltage of 4.5 V have a 32 percent reduction in the total on-resistance.

When using any deep level donor, there is an increase in the threshold voltage drift at elevated temperatures. "However, the magnitude is suppressed in the oxygen doped sample," says Noguchi. Compared to sulphur, this shift is almost halved.

Another benefit of using oxygen rather than sulphur is that it produces a smaller shift in negative bias temperature instability. This indicates that the reliability

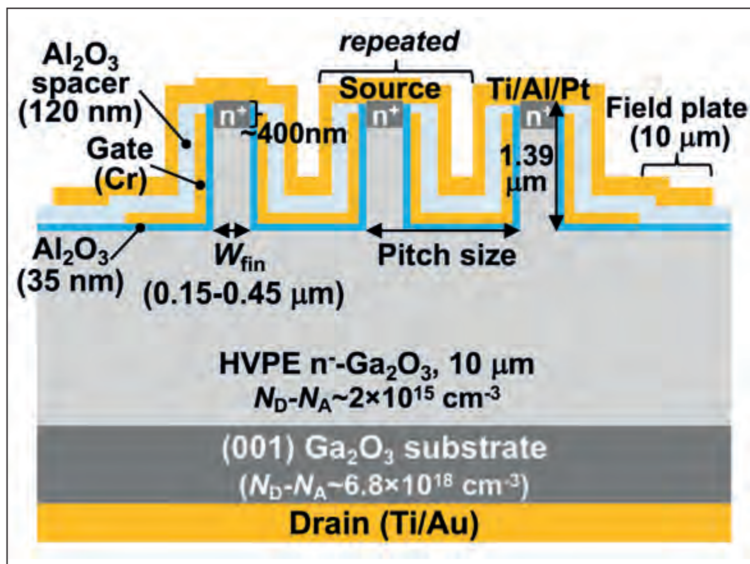


Figure 3. Ga_2O_3 transistors with multiple fins have broken the record for the blocking voltage for this class of transistor. A portfolio of devices has been produced, with fin channel widths ranging from 0.15 µm to 0.45 µm, and pitch sizes from 1.2 µm to 2 µ m.

of the gate is better – it is, in fact, comparable to that in a conventional device.

Noguchi and co-workers will continue to investigate the impact of deep level donors on the electrical characteristics of the MOSFET. In particular, they will consider its ruggedness as a power switching device.

Another option for decreasing the resistance of a SiC MOSFET is to use a trench architecture. This design also allows a smaller cell pitch, leading to an increase in channel width.

However, the trench MOSFETs that have been fabricated on commercial SiC (0001) substrates are failing to fulfil their promise. The field-effect channel mobility is lower than that expected for planar MOSFETs, for reason that are not clear.

To shed light on this matter, a team from Toyota Central R&D Labs has tried to determine the mobility in the channel. To extract an accurate channel resistance, they remove parasitic series resistance from their calculations.

According to the researchers, the key to calculating the field-effect channel mobility is to determine the threshold voltage. Due to the high density of charge traps at the interfaces of SiO_2 and SiC, there are inaccuracies associated with calculations of threshold voltage that are based on linear extraction. To avoid this, the team determines the threshold voltage by drawing on values of the ideal threshold voltage and experimental measurements of the relationship between the drain current and the gate voltage.

The first step towards this involved growing *n*-type and *p*-type epilayers of SiC on a heavily doped *n*-type SiC substrate. After adding source and drain regions, the researchers fabricated a trench gate. Following trench etching, they used three different forms of high-temperature annealing to produce different surface morphologies in the trench walls. To complete the fabrication of the structure, they added a 75 nm-thick layer of SiO_2, followed by nitridation of the device in diluted nitrogen oxide.

Plotting the drain current as a function of gate voltage at a range of temperatures enabled the team to calculate the density of fixed charges and the distribution of interface states. From these values, the researchers concluded that the interface states contribute to Coulomb scattering.

To relate the level of scattering to the quality of the channel, the team scrutinised the surface morphology of the trench sidewalls with atomic force microscopy. This revealed a significant difference in the roughness of the three samples. By combining this finding with the electrical measurements, they deduced that Coulomb scattering is suppressed when the trench sidewalls are flat enough to form atomic steps and terraces. In this case channel mobility is higher, due to a decrease in the distribution of interface states that arises from dangling bonds at the edge of the step region.

Record-breaking voltages

Helping to improve the performance of Ga_2O_3 transistors is a partnership between researchers at Cornell University and Hosei University. This team has broken the record for blocking voltage with a vertical transistor that can withstand 2.66 kV. This raises the bar from 2.32 kV, a figure obtained with a lateral variant.

Team spokesman Wenshen Li from Cornell University says that one of the merits of the vertical architecture, which leads to vertical current flow, is a more efficient use of the device footprint. "[Devices] typically have a smaller area, especially under high current ratings."

By using a sub-micron fin-channel structure for the device architecture (see Figure 3), Li and co-workers avoid the need for *p*-doping. That's a significant advantage as *p*-doping in Ga_2O_3 is impaired by: deep acceptor levels that hamper the thermal activation of these carriers; a very flat valence band, which leads to a high effective mass for holes and impairs conductivity; and self-trapping of holes.

One of the reasons why Ga_2O_3 transistors are failing to fulfil their potential is that the channel mobility is far lower than it is in the bulk, due to etch damage and sidewall depletion. Effective channel mobility is typically just 30 $cm^2 V^{-1} s^{-1}$, compared to values of up to 200 $cm^2 V^{-1} s^{-1}$ for bulk material.

To address this, Li and co-workers use a post-

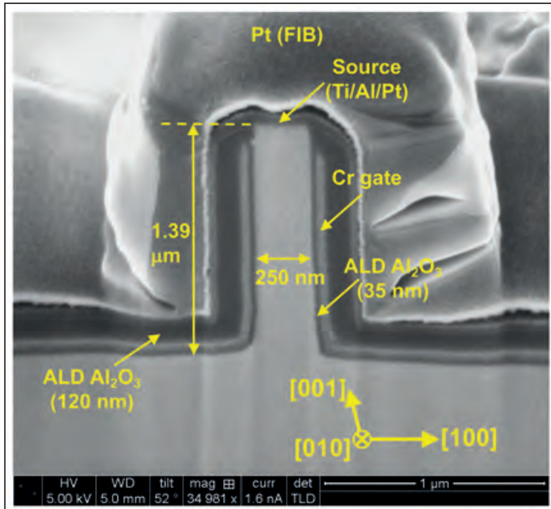


Figure 4. A scanning electron microscopy image of the fins in the Ga_2O_3 transistors highlight the near-vertical sidewall profile produced by dry etching.

deposition annealing step during the production of their transistors. Some of these devices contain several fins, enabling unambiguous evaluation of the specific on-resistance – it breaks new ground for Ga_2O_3 transistors.

Fabrication of the team's devices began by loading an *n*-type Ga_2O_3 substrate into a HVPE chamber and depositing a 10 µm-thick, lightly doped *n*-type drift layer. Silicon implantation and subsequent activation at 1000 °C created a heavily doped *n*-type top layer that provided an ohmic contact. Electron-beam lithography defined the fins (see Figure 4), which were formed by dry etching.

After treatment with HF to remove plasma damage, the team added a Ti/Au drain contact and a gate contact, comprising a 35 nm-thick Al_2O_3 gate dielectric created by atomic layer deposition and a 50 nm-thick layer of chromium, deposited by sputtering.

During the formation of the source electrode of Ti/Al/Pt by sputtering, Li and co-workers simultaneously created a source-connected field plate. This refinement to the design provided a significant improvement to edge termination, and is behind the increase in breakdown voltage.

"However, we found that the breakdown voltage is still limited by the edge termination, indicating that the source-connected field plate is not an optimal design," admits Li.

The team have used electrical measurements to evaluate the benefit of post-deposition annealing. It leads to a significant increase in current density, an improved source contact resistance, and a reduction in interface trapped charges, leading to a lowering of the sidewall depletion in the fin channels.

Using simulations and fits to experimental data, channel mobility in single-fin devices is found to be around 130 $cm^2 V^{-1} s^{-1}$. This figure drops to just 40 $cm^2 V^{-1} s^{-1}$ in multi-fin devices, due to rougher sidewalls that result from plasma loading effects during the dry-etching step. "By tweaking the plasma condition during the dry etching for a more anisotropic etch, the roughness can be reduced," say Li.

The multi-fin device outperforms its single-fin variant in blocking voltage, realising a value of 2.655 kV, compared with 2.46 kV. Additional measurements on the multi-fin transistor reveal an on-off ratio in excess of 10^8; a threshold voltage of 1.8 V at 0.1 mA cm^{-2}; and a specific on-resistance of 23.2 mΩ cm^{-2}, based on pulsed-measurements that are expected to reduce self-heating and charge trapping (see Figure 5 for benchmarking of the single-fin and multi-fin devices) .

Plans for further work include optimising the dry etching process, in order to improve channel mobility in multi-fin channel devices, and developing better edge termination designs for improved breakdown behaviour. Li says that additional goals are to undertake thermal characterisation of their devices, and the testing and analysis of dynamic behaviours.

The presentations at IEDM by Li on Ga_2O_3 transistors, and by other speakers on SiC devices, show that power electronic devices are getting better. That bodes well for the future, where greater deployment of more efficient power electronics is set to play its part in global efforts to tackle climate change.

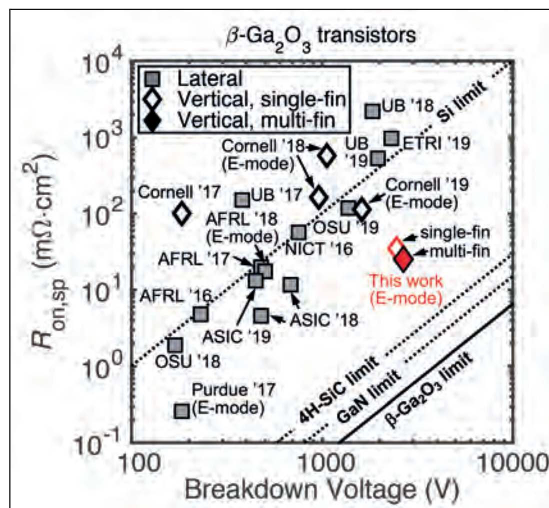


Figure 5. Multi-fin Ga_2O_3 transistors produce by a partnership between researchers at Cornell University and Hosei University have broken the record for blocking voltage for this class of device. Note that the on-resistance is normalised using an effective conduction width of about 10 µm, as normalising this resistance to the source contact area would grossly over-estimate the figure of merit.

KLA steers tech for automotive IC power applications

Silicon Semiconductor technical editor Mark Andrews speaks with Robert Cappel, Senior Director of Marketing, about advances that KLA Corporation has made to enable defect reduction and quality improvement processes for automotive applications. As chip makers go after new auto IC opportunities they face challenging reliability and performance standards up to 10 times those of consumer electronics

MA – *Auto electronic systems present unique challenges for IC manufacturers due to quality and lifetime requirements that are years longer than consumer electronic device standards. Please describe the landscape they are entering*

RC – Process control requirements for automotive electronics are extremely stringent and much greater than for business and consumer grade products like laptops and mobile phones. While an acceptable failure rate for consumer type products might be 10% within the first two years, automotive requirements are significantly tougher. As semiconductors are now a critical part of Advanced Driver Assistance Systems (ADAS) that are critical to the function and safety of the vehicle, failures cannot be tolerated. The rapid push of the automotive industry to incorporate autonomous

driving features, and the eventual transition to fully autonomous driving, further drives the needs for all the semiconductor chips to work perfectly together to protect the safety of both the car's occupants and others in the surrounding environment. This is the biggest driver of a requirement for zero defects in parts per billion within the automotive semiconductor industry today and in turn has increased the emphasis on strategies to handle stronger process control requirements.

MA – *How can KLA systems help device manufacturers new to the automotive market succeed?*

RC – The bulk of automotive devices have historically been manufactured at established 200mm fabs with design rules of 65nm or above, or to a lesser degree, in mature 300mm foundries. Manufacturing processes in these fabs are well characterized and established. The move to smarter, connected and autonomous cars will require additional computational power that cannot be served by these older devices. The need for advanced technology, as well as more manufacturing capacity, will speed the migration of automotive capacity to advanced logic foundries.

Anticipating this trend, foundries are already gearing up to serve 14nm SOCs (system on a chip) in the automotive space, with even smaller automotive chip designs in preparation. These newer processes have not enjoyed the lengthy time (years) to mature compared to many of the larger design node automotive chips currently in use, and therefore, will still suffer from baseline yield challenges and excursions. Manufacturers using methods that are better suited to consumer mobile devices, where 10% failure rates from reliability issues is acceptable, will result in unsatisfactory reliability for automotive grade parts. This increased quality requirement has been creating additional pressure on fabs new to the automotive space to ramp to extremely mature yields even faster than before, with much lower defectivity levels than with advanced consumer grade parts. KLA's inspection and metrology process control systems and strategies are the enabling technology to enhance this necessary yield learning. KLA works with these new customers in a collaborative effort to help them define inspection and metrology requirements, and then develop sampling strategies to reduce overall defectivity, which in turn drives down potential reliability failures.

MA – *For established auto device IC manufacturers, what changes are coming to the market and how are market expectations changing? How does KLA address these challenges?*

RC – Automotive semiconductor manufacturers are adopting a new mentality focused on increased quality to prevent chip reliability issues in the field. For example, general continuous improvement programs reduce the random defectivity introduced by process tools, while more stringent characterization and monitoring strategies also ensure that the process tools are in top operating condition. With a Zero Defect focus, fabs can no longer settle for "good enough" or traditional yield optimization. The quality mentality will need to shift to "the best possible" – running the processes under the best possible conditions in order to achieve strict reliability goals. This quality mentality may increase fab costs in the short term but will result in long term savings from delivering the higher reliability IC chips required by automakers.

When looking at automotive semiconductor best known methods, the defect pyramid (figure 1)

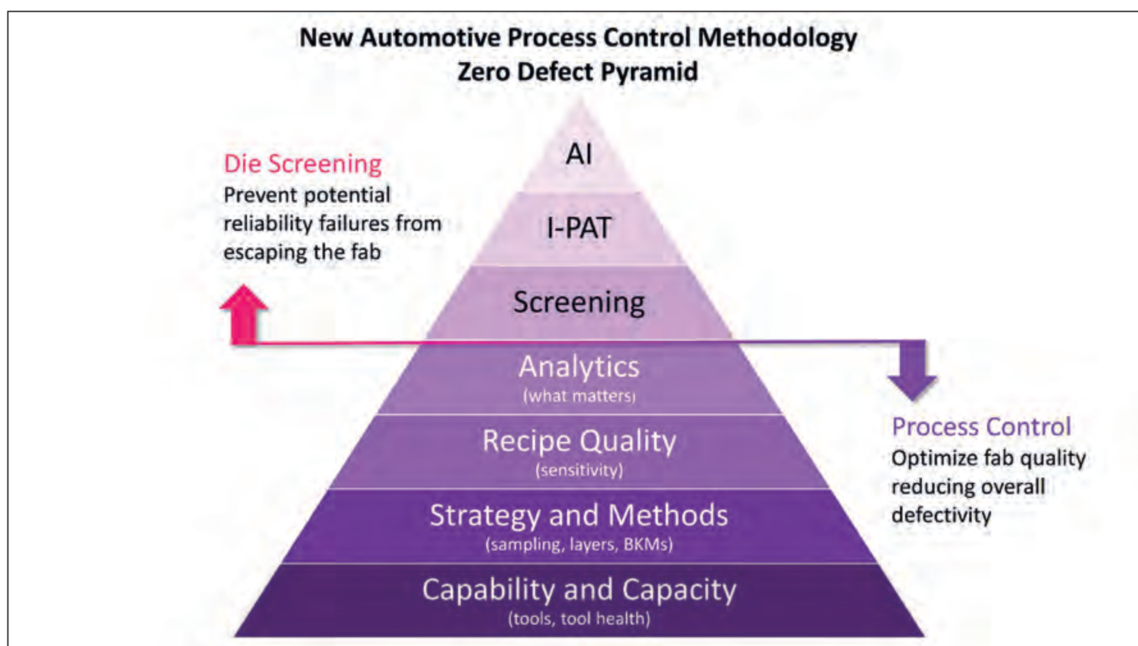


Figure 1: New automotive process control methodology Zero Defect pyramid

provides a blueprint for the types of strategies needed for success in producing automotive grade semiconductors.

As shown, the optimal base is to start with having the best performing process control tools in place. An effective way of finding and removing chips with latent reliability defects is to increase parametric and defectivity margins. Increasing parametric margins means requiring that the chips not only function, but also operate within a tighter parametric window. Increasing defectivity margins means setting the acceptable defect size to be smaller than what has been proven to be yield-killer defects. For a fab to find more subtle parametric variations or smaller defects, fabs need to implement higher sensitivity process control strategies – either by increasing the recipe sensitivity or by utilizing inspection and metrology systems designed to detect smaller defects or variations. With more capable process control systems, automotive fabs can detect, monitor and control the latent defects that might otherwise cause premature chip reliability failures.

The next approach is to manufacture fewer overall defects by closely controlling the process and employing continuous improvement programs that reduce the random defectivity introduced by the process tools or environment. This approach requires the fundamental baseline yield improvement techniques of tool monitoring (equipment may include Surfscan® unpatterned wafer and Puma™ patterned wafer inspection systems) and defect discovery or root-cause partitioning (equipment may include 39xx/29xx broadband plasma patterned wafer inspection systems) that fabs have utilized for years, but have now taken to a new higher standard to provide the absolute best in class tools for sensitivity, accuracy, reliability and matching. The approach also requires that the process is sampled frequently enough to provide traceability. When the inevitable process excursion happens, Zero Defect fabs know definitively where the problem started and stopped and can quarantine the affected parts until they can be effectively dispositioned or culled. The combination of the two requirements has resulted in the automotive fabs adopting process control tools at a higher rate, as well as using tools designed with sensitivity for one design rule node more advanced than they are manufacturing, so they can detect the smaller defects that may affect reliability.

Finally, a method that is receiving increased interest is to utilize inline defect information not only to control the process, but to identify die at risk for reliability problems while they are still in the fab--where the cost of correcting the problem is the lowest. Automotive fabs have long relied on "screening" where a high throughput tool inspects 100% of the die on all wafers at a handful of final layers late in the process. Die that meet the defined failure criteria (defect size/type/location) are excluded or "inked." While effective for large defects, this method is inadequate alone for smaller latent reliability defects. A new inline technique, called I-PAT™ (Inline Parts Average Testing), may be the answer. It leverages a 20-year-old automotive industry technique known as Parametric Parts Average Testing (P-PAT). This original e-test based method identifies any die whose test results lie outside of the normal distribution of the population, even if they are within the operating specifications. For a small sacrifice of 0.5-2.5% of yield, significant

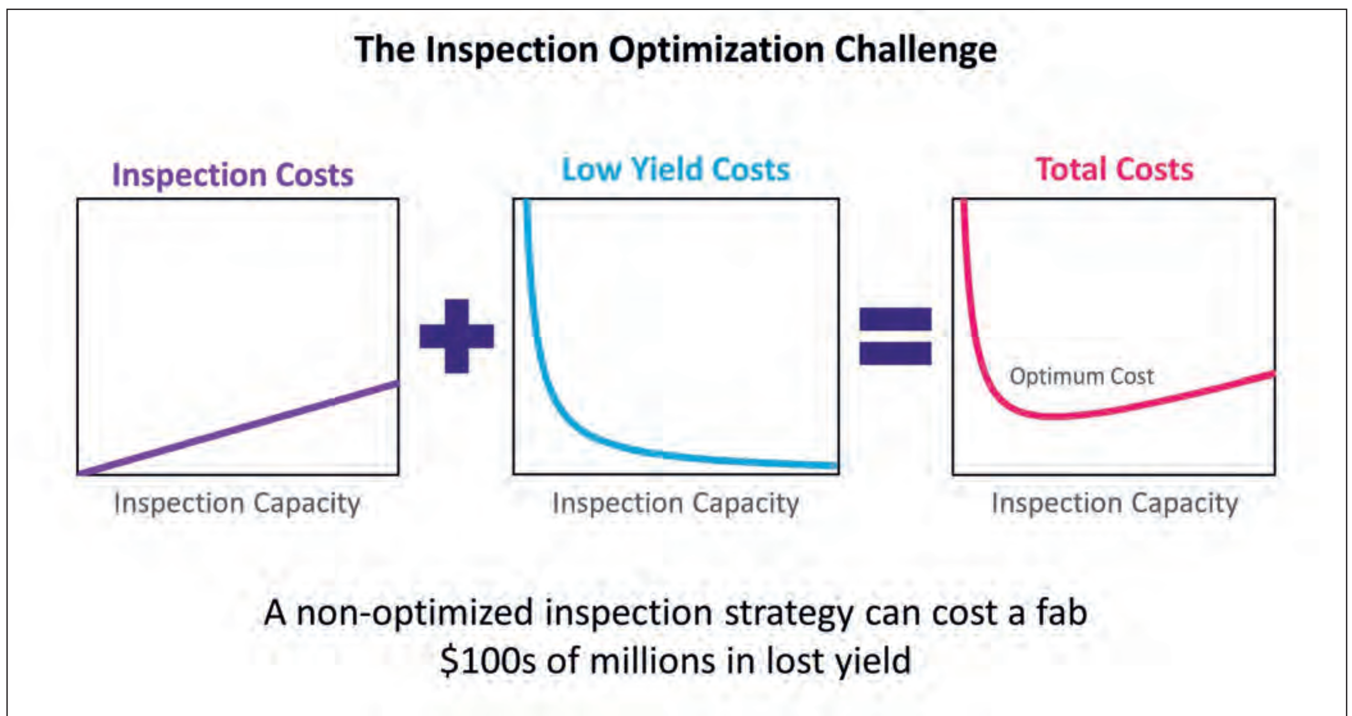


Figure 2: The inspection optimization challenge

improvements in reliability are gained, with some automotive fabs seeing 20-30% improvement when the outlier die are culled. I-PAT moves this concept inline using massive data sets and artificial intelligence to identify die with outlier defect populations across the multiple steps within the manufacturing process. The outlier die are statistically more likely to contain the latent defects that the industry desperately wants to eliminate. I-PAT results could be used to cull these at risk die to improve the overall go/no-go decision for die.

Automotive quality standards are driving the combined requirements for additional sensitivity to small reliability defects. Faster yield learning cycles resulting in higher overall yield levels at advanced design rules and increased sampling for continued traceability all point to the value of process control in the automotive space. Additionally, the introduction of I-PAT will help automotive semiconductor suppliers better utilize their process control equipment to identify the latent defects that are a top priority.

MA – *Please describe KLA's specialized inspection systems for SiC substrates as well as processing within GaN-on-silicon manufacturing flows that target present and future requirements for automotive power devices?*

RC – SiC power devices pose unique yield and cost challenges in comparison to Si-based devices. Some of these challenges include:

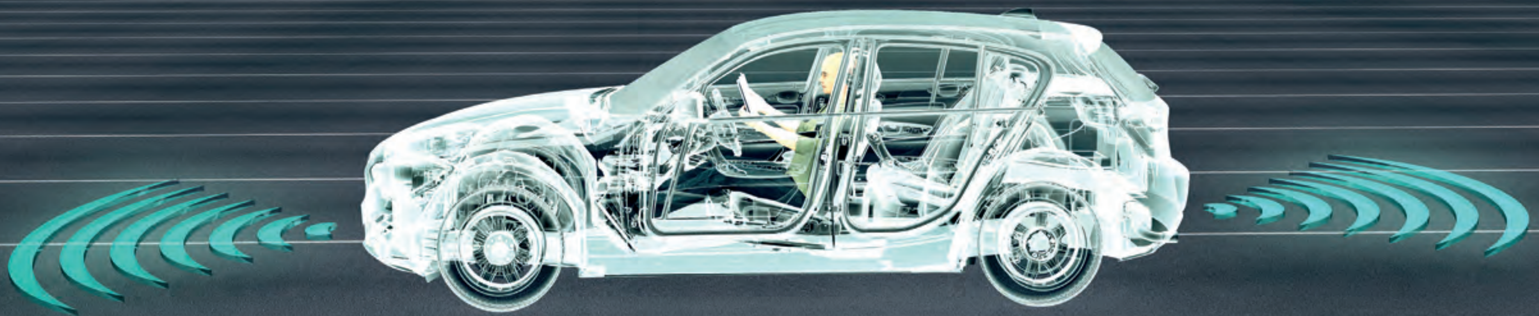
- Much higher intrinsic material defect densities than Si-based devices
- High level of defect transference from substrate to epitaxy to device fabrication
- Variation in quality among substrate suppliers. Wafers graded and sold by dislocation density.
- Key defect issues include both crystallographic and morphological defects (carrots, surface triangles and stacking faults)
- Defect mechanisms act in the z-direction instead of x/y-plane.

KLA's Candela 8720 compound semiconductor material surface inspection system and the 8 Series patterned wafer inspection system have been developed to address these challenges. The Candela® compound semiconductor material surface inspection system enables GaN-related materials, GaAs substrate and epi process control with high sensitivity to critical defects for the production of power devices, communications and RF devices, and advanced LEDs (as well as upcoming micro LEDs).

With its proprietary optical design and detection technology, the Candela inspection tool utilizes signals from scatterometry, reflectometry, ellipsometry, slope and photoluminescence detectors to detect and classify yield-limiting, sub-micron defects to support production-line monitoring. The Candela 8720 system is used to monitor the substrate IQC (incoming quality control) and OQC (outgoing quality control) processes for a variety of defect types including particles, scratches, stains, pits, micropipes, stacking faults and other crystallographic defects. For the post epitaxial growth process step, the inspection system can detect and monitor process issues such as cracks, macro epi disturbances (such as droplets), epi pit, epi bump, crystal-oriented defects (such as single/bar stacking faults, BPDs, etc.), micropits and particles. Defects in the substrate and post epi growth can significantly impact end of the line yield, so detecting and correcting such process issues at the source – where cost is the lowest – is critical.

Patterned wafer inspection of SiC semiconductor devices is important for reducing defectivity and maintaining traceability, but inspection can present several unique challenges. Wafer thickness and warpage are outside typical SEMI standards. The transparent (SiC) substrate can create challenges

Automotive quality standards are driving the combined requirements for additional sensitivity to small reliability defects. Faster yield learning cycles resulting in higher overall yield levels at advanced design rules and increased sampling for continued traceability all point to the value of process control in the automotive space



for focus systems and create unwanted noise when imaging the wafer. The 8 Series patterned defect inspection tool addresses these challenges through a specialized prealignment and chuck, selectable illumination wavelengths and depth of focus for inspection, multiple inspection channels and increased wafer handling flexibility.

With simultaneous brightfield and darkfield inspection capability, it captures all types of surface defects with a multi-level defect binning solution. With optional backside inspection capability, the 8 Series system can handle and inspect both frontside and back side of 6" SiC pre- and post-grind wafers offering high precision frontside to back side correlation and die inking for process-induced killer defects on both sides of the wafer.

It is important to note that beyond some of the early SiC process steps, the many remaining steps for SiC are very similar to a standard silicon chip process, so SiC fabs will utilize similar process control strategies compared to silicon IC fabs.

MA – *Automotive ICs and packaged products can present production challenges beyond higher reliability such as the need to produce spare parts for years longer than consumer electronics. How does KLA technology help device manufactures meet these critical needs?*

RC – Automotive fabs have faced this problem for years and they do it by maintaining the process control strategies and standards that they used successfully in the past. This is shown through the defect pyramid referenced earlier. In order to help maintain these strategies along with the best performing tools, KLA works with our customers in two areas:

- KLA helps customers by making continuous improvements on the process control platforms through product upgrades.
- KLA provides an extensive service package that helps our customers ensure that the process control tools are performing at the highest levels.

In addition, KLA also offers metrology and inspection tools that enable component sorting to prevent defective devices arriving at the assembly line and to keep track records of each device. Metrology helps verify whether device dimensions are within tolerance and thus confirming the quality of packaged products; inspection verifies that there are no particles, burrs or other defects present that could impact the yield.

MA – *IC manufacturers accustomed to serving non-automotive applications focus on increased yield at lower costs; there is typically no heavy emphasis on long-term reliability. Is it possible to 'have it all' – to keep yield high at low cost while substantially improving quality and long-term reliability?*

RC – There are always going to be trade-offs when looking at scenarios where risk tolerance is the biggest factor in making these decisions. Do I sacrifice equipment capital costs or the costs of lost yield and reputation? Most choose to err on the side of caution as generally the costs of lost yield far outweigh the costs of additional process control. Lost yield or reliability failures that result from a process with lower yields cost significantly more than inspection costs as shown in figure 2. But more importantly, these failures can cost fabs critical contracts within the automotive ecosystem that typically are never regained. Auto OEM's and Tier 1 companies don't want to take on the risk of a fab that produces parts that fail.

MA – *As electric vehicles increasingly enter mainstream product lines, what special challenges are seen in the shift from traditional mechanical cars to EVs for IC manufacturers pursuing this emerging market?*

RC – As more electric vehicles are introduced into the market, a significant challenge with this transition is the move to SiC and GaN materials for power applications. This is highlighted in the previous question regarding SiC solutions. Another challenge from increased electrification and electronic content in modern vehicles is the continued growth of semiconductor content within the car. IC manufacturers that want to participate in this fast-growing market will need to meet the new stringent quality requirements.

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Rudolph Technologies and Nanometrics merge to form **Onto Innovation**

Silicon Semiconductor technical editor Mark Andrews recently spoke with Onto Innovation's CEO Mike Plisinski about the merger of Nanometrics and Rudolph Technologies. Plisinski explores the benefits, challenges and opportunities of forming a new semiconductor supply chain entity by combining two industry leaders.

MA – *When resources combine post-merger, each company contributes expertise, viewpoints and strategies which creates both challenges and opportunities. Looking at the merger from the perspective of each company, what are the primary near-term benefits and what might the industry expect from Onto Innovation over time?*

MP – When I think about the benefits of the merger, I put them primarily in three categories: scale, scope, and synergy. Onto Innovation is now the fourth largest (by revenue) wafer fab equipment supplier in the U.S. and among the top 15 in the world. We have over $300 million in cash, cash equivalents or marketable securities and no debt. That gives us a lot of options to invest in our future. We are one of a few companies that is an end-to-end supplier, with products and applications ranging from unpatterned wafer quality, through advanced front-end metrology and macro defect inspection to advanced packaging lithography and inspection in the back-end, with enterprise software solutions spanning the entire value chain.

The synergies between Nanometrics and Rudolph were tremendous, with the positive complementary product lines, markets and organizations with no overlapping products. Nanometrics' strengths were in the optical metrology space where the company had been quite successful with the top manufacturers in the industry. While Nanometrics' metrology sales were concentrated at relatively few customers, those customers were industry leaders in the front end, producing advanced nodes. Rudolph's strengths were in different product technologies: macro defect inspection, acoustic metrology, advanced packaging lithography and software, serving a much broader customer base. Yes, some of the same customers, but the Rudolph customer base was fairly diverse across the entire supply chain. So, by bringing these companies together, we now have a broader product portfolio to offer to a broader customer base and those products have very little to no overlap.

The two companies were built around the same core competencies in software and optics. So, R&D investments are magnified. Let's say we develop a new artificial intelligence engine for fab wide software. We can apply that to help with automatic defect classification in our inspection systems and now to optical metrology as well. The same goes for optics. If we're developing new high-speed camera technology or new illumination technology, we can apply it across a broader set of product lines. We will ultimately develop common platforms, common staging, common end effectors, robots, etc. All that provides tremendous leverage on the R&D investment.

One other point relates to the commonalities of the two companies. We share a common understanding of our products and markets. Putting two companies together that don't share that common understanding and background can be very challenging. Without it, decision making processes can easily become contentious, based on emotion and descending quickly into chaos. With it, discussions stay focused on the facts, on the merits of the case. It was an important consideration in our evaluation of the integration risk. I know it resonated strongly with both boards of directors.

With regard to longer term benefits, we expect some gains in our existing markets as well as expansion of our SAM (served available market). What we ultimately want to do is expand our TAM (total available market) by developing new products and technologies and entering new markets. With two healthy companies coming together there will be some immediate gains in efficiency, primarily from cutting out duplicate public company expenses, but we also have substantial financial resources available to invest. There are opportunities to gain share by combining technologies to open up other aspects of the optical metrology market, like planar films, that we are not serving now. We're also looking at ways to bring software onto the metrology platforms to make them even more competitive and differentiate them in ways that competitors can't match. It is the same approach that was successful for Rudolph for inspection and lithography. There are other options to consider as well, including further M&A activity to accelerate our entry into other markets and expand our SAM and TAM.

MA – *Why now? Can you point to any events or trends that made this the right time to merge?*

MP – I get that question a lot. Neither company was dying, neither company was even sick. Both had growth, both had strong operations and financial statements, etc. The better question might be why did it take so long? And I would say there is no real answer to that. Different personalities, different points of view. Finally, the viewpoints converged. The importance of software was becoming more and more clear and it's not easy to build the kind of software assets Rudolph had. I also believe that, with the consolidation in the industry, the importance of diversity became clearer and more critical to Nanometrics. I think Rudolph saw the exploding growth in the logic and memory spend and they were only partly participating in it. The two boards started to see that a merger really did make sense, that it was an enhancement more than a change in direction.

MA – *Since the two companies that have merged are well known within the industry, why not use one name or the other rather than an entirely new name, or is that the point?*

MP – That is exactly the point. A lot of investors ask that, and customers do too. Both companies had strong brand recognition and long histories – Rudolph from the 1940s and Nanometrics from the 1970s. It is not easy to walk away from such strong legacies, but we are building a company for the future and the future is changing dramatically. What each brand was known for did not really reflect the power and the focus and the potential for this new company in the future. We wanted to reflect the new world moving forward. The pace of innovation is only going to accelerate. We are constantly looking to the future. The electronics/semiconductor market is no longer just the PC/server refresh. Technology is part of every aspect of people's lives. So, Innovation, because we are always looking toward the next innovation, and Onto, because it brings a sense of movement and immediacy. We also did not want to be tied to any specific market. We want a new name that reflects the exciting potential we see.

MA – *2019 has been a tough year for many across the semiconductor industry supply chain due to the fact that two of its largest host countries (the US and China) have been in a months-long trade dispute. Is this situation creating new opportunities or challenges for Onto Innovation as 2020 begins?*

MP – China has been a source of great growth for both companies. So, of course the trade situation has impacted us, but we are still doing very well. Bringing the companies together only allows us to serve our Chinese customers better. Both companies' technologies are clearly important to the Chinese markets because both have seen great growth, and that we expect that to continue. Business in 2019 was down but I think the trade dispute was a minor consideration.

Memory and smartphone adoption were down, but the refresh cycles haven't really occurred. So, there was sort of a natural slowdown. But logic is growing, and certain advanced packaging. Even though it's slowing, memory is transitioning from wire-bonding to advanced packaging and that's an opportunity for us. One of the benefits of bringing these companies together is that it should mute some of these cycles by having more diverse platforms, portfolios and markets.

MA – *Identifying and controlling defects; eliminating potentially damaging contaminants from process flows and related tactics/strategies are all common for work at the extreme limit of CMOS scaling – Does the merger primarily benefit companies working at 7nm and below, or seen another way, what benefits could MEMS makers and other such as power device manufacturers gain from the merger?*

MP – The merger does not enhance, specifically, our ability to do something at 7-8nm. There are areas where we may leverage our software or other core technologies to enhance the value of our tools for 8nm and below. For example, we may be able to leverage acoustic technology to enhance signal generation. Advanced nodes require higher quality wafers and we have seen increasing demand for our bare wafer edge inspection technology.

We also see opportunities to go the other way, taking advanced film metrology and optical metrology from sub 8nm into other markets and specialty devices. Wafer handling requirements for a lot of these specialty devices are very different from the traditional front-end requirements. Rudolph already had the handling and it may enable us to go after specialty applications for optical metrology that Nanometrics could not pursue because developing the handling was too expensive.

MA – *Every merger brings with it good and bad prospects: economies of scale can be optimized, but this sometimes leads to job cuts. A fresh approach can benefit growth opportunities, but the challenge of melding two corporate cultures can be considerable. Can Onto Innovation delve into what they see occurring in the next few years in terms of both challenges and benefits?*

MP – Integration strategies generally fall somewhere between two extremes. Either you force an immediate integration of everything and risk creating chaos because everything changes. Or you let them run more or less independently in the hope that they will merge naturally over time.

Unfortunately, this often results in the creation of silos that grow apart rather than together. We have tried to follow a middle path that balances between silos and forced integration, trying to address integration issues in the most sensible way on a case-by-case basis. In our organization, individual business units are responsible for R&D.

We combined metrology R&D from both companies together under one leader. But R&D for the other business units is largely staying focused on what they did, so not a lot of chaos. But we did centralize each of the manufacturing, marketing, and sales organizations. In manufacturing, one leader looking across the whole company is better able to see things like supply chain opportunities. In marketing, we have all the product lines under one group, so they are better able to develop a coherent Onto Innovation strategy and message. As for staff reductions, the lack of overlap has kept them very few.

The real focus has been on driving efficiency and driving the positive synergies through organizational development. This really leads back to the commonality between the two companies' cultures that I mentioned earlier.

hat common understanding makes it easier to choose the best people for each role and balance between silos and forced integration. R&D is probably hardest to get the synergies. Supply chain, manufacturing improvements, channels to market, those are the quicker and easier places to find synergies.

We were both American companies with similar business cultures: competing on value, competing on technology, understanding the importance of the pace of innovation, emphasizing profitable growth. Shared values make it a lot easier to avoid constant fighting.

If we are considering a big R&D spend, we share a common set of criteria for the decision. We go through a disciplined process and that is engrained in our common culture. I've been very pleased by the progress we have made in only a few short months.