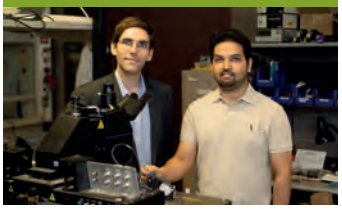
POWER ELECTRONICS WORLD

CONNECTING THE GLOBAL COMMUNITY

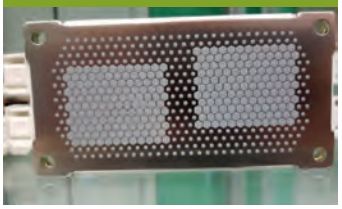
ISSUE II 2020

WWW.POWERELECTRONICSWORLD.NET

Getting ready for GaN CMOS



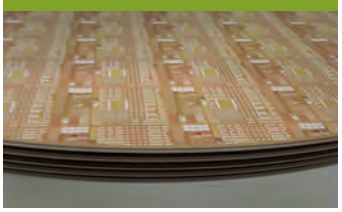
Improving the lifetime of LoPak1 Modules

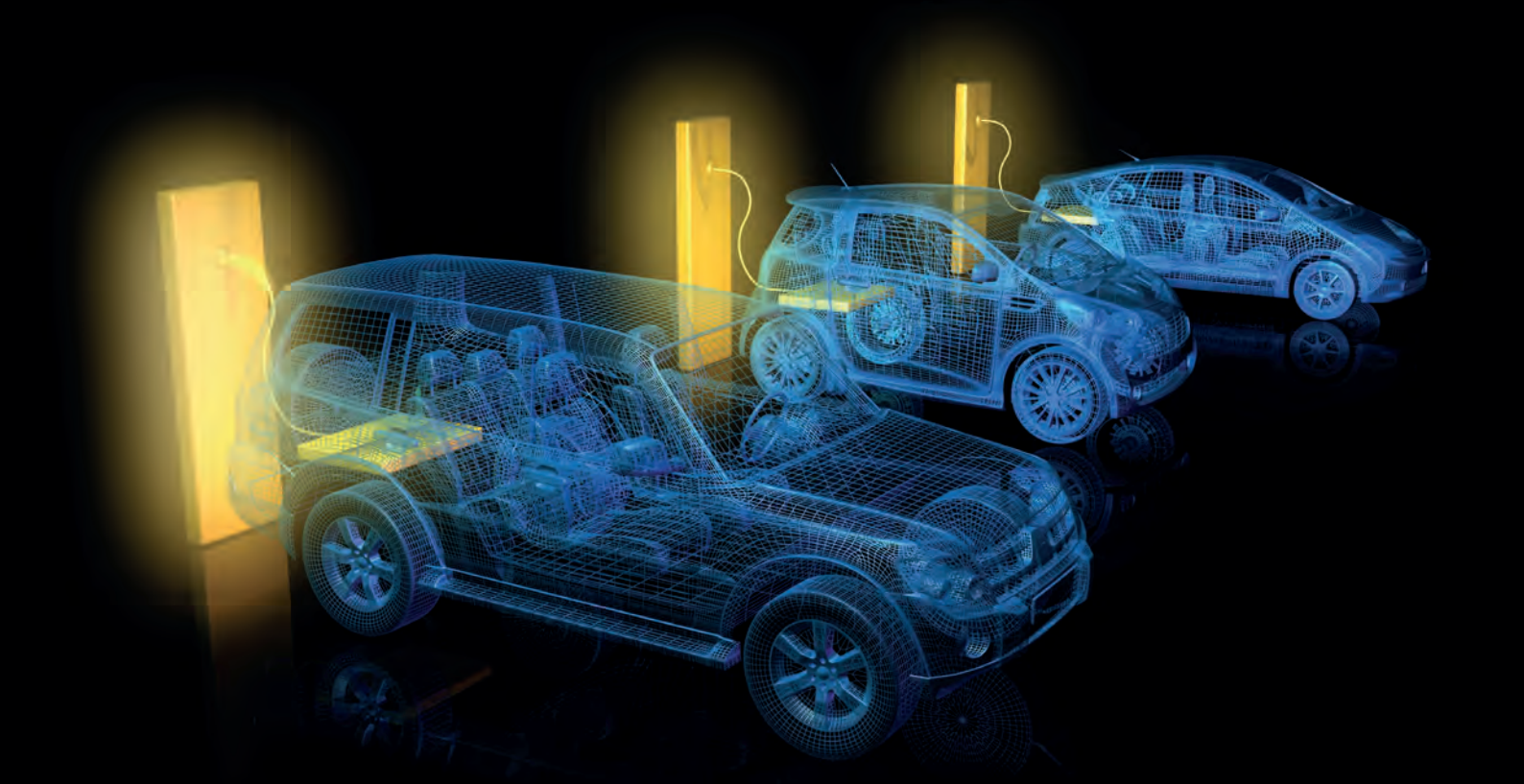


Charging the UK to power an EV future

Focuses on next-gen power applications

Qromis: ready for business





Best performance for next generation SiC power electronics to address global mega trends

AIX G5 WW C

- Electric vehicles: on board chargers, power inverters
- Infrastructure: charging stations
- Renewables: solar and wind
- Industrial: motor drives, power supplies
- Power distribution: HVDC

Discover our SiC epi production *batch tool* with *single wafer* performance

Made in Germany

AIXTRON

info@aixtron.com
www.aixtron.com

Viewpoint

By Mark Andrews, Technical Editor

Power Electronics and the 'New Normal' of 2020

IT WASN'T SO LONG AGO that new work-from-home-office solutions created about as much media excitement as rearranging one's sock drawer on a rainy afternoon. That was before the word 'pandemic' entered daily conversations and more than one-third of worldwide tech employees were in fact working from home. Welcome to the New Normal of summer 2020.

While many of us are still trying to achieve balance between many important and sometimes conflicting objectives, the pandemic has given us all a new perspective on what is important, like our health, families, and our collective futures, and what isn't worth our time or worry.

Throughout all that is happening to us and around us, technology continues to fill the gaps and enable all types of work and life scenarios that didn't necessarily cross our minds just six short months ago. I'm reminded of a former colleague, a poster child for Old School business, who couldn't quite get the knack of email protocol – more than once he hit 'reply all' with comical results. How trivial thoughts like this sound today compared to the global health emergencies we have all experienced. Even though tech industries face unprecedented challenges and opportunities, there are solutions and means to help tomorrow be better than what we have experienced last week or the month before that.

In this issue of Power Electronics World we look at ways that industry leader KLA Corporation is addressing the changing needs for power device inspection, test and metrology. We look

at more efficient, highly accurate wafer singulation technologies from Panasonic that reduce waste and increase throughput, while exploring new thermal interface materials from ABB that enable faster, more consistent module installations. We also delve into the potential of graphite to create new generations of SiC power modules while exploring monolithically integrated GaN ICs. We also consider different GaN possibilities being advanced by UK startup Porotech.

'Business Unusual' has challenged us like never before. But we have also seen the resilience of individuals across the globe who have demonstrated how we can live and work safely and productively even amidst a very changed world. Stay safe!

Editor & Publisher	Jackie Cannon	jackie.cannon@angelbc.com	+44 (0)1923 690205	**Joint Managing Director**	Sukhi Bhadal	sukhi.bhadal@angelbc.com	+44 (0)2476 718970
Technical Editor	Mark Andrews	mark.andrews@angelbc.com		**Joint Managing Director**	Scott Adams	scott.adams@angelbc.com	+44 (0)2476 718970
Sales Manager	Shehzad Munshi	shehzad.munshi@angelbc.com	+44 (0)1923 690215	**Directors**	Jackie Cannon, Sharon Cowley		
USA Representatives	Tom Brun Brun Media	tbrun@brunmedia.com	+001 724 539-2404				
	Janice Jenkins	jjenkins@brunmedia.com	+001 724-929-3550				
Director of Logistics	Sharon Cowley	sharon.cowley@angelbc.com	+44 (0)1923 690200				
Design & Production Manager	Mitch Gaynor	mitch.gaynor@angelbc.com	+44 (0)1923 690214				
Circulation Director	Scott Adams	scott.adams@angelbc.com	+44 (0)2476 718970				
Chief Executive Officer	Stephen Whitehurst	stephen.whitehurst@angelbc.com	+44 (0)2476 718970				

Published by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 E: info@angelbc.com

Angel BUSINESS COMMUNICATIONS

recycle When you have finished with this magazine please recycle it.

Rohm and Leadrive establish joint lab for SiC automotive modules

JAPANESE electronics firm Rohm and Leadrive, a Chinese maker of automotive power devices, have established a joint research lab in Shanghai to develop power modules and inverters for vehicles around Rohm's SiC MOSFET bare chips and isolated gate drivers.

Rohm and Leadrive have been collaborating on automotive applications using SiC power devices since 2017. Establishing a joint research lab is designed to give both companies the opportunity to further accelerate the development of innovative power solutions.

"The adoption of power modules that integrate SiC chips for new energy vehicles will become an industry trend over the next couple of years. Commercialising mature SiC-equipped devices by collecting resources from around the world and carrying out R&D gives us a competitive edge as an automotive Tier 1 manufacturer," says Jie Shen, chairman and general manager at Leadrive Technology.

"Rohm has been a strong partner since Leadrive was founded. This joint research laboratory will allow us to deepen our collaboration," Shen continues. "As a pioneer and leading supplier of SiC power devices, Rohm has a proven track record for providing high quality power solutions that combine industry-leading device technology with driver ICs, and we are committed to promote the use of SiC for xEV applications," adds Kazuhide Ino, CSO, and senior director of power device business at Rohm.

"Understanding customer needs and market trends is extremely important when developing SiC power device technology. Leadrive plays an important role in the applied research of SiC as a manufacturer of automotive power modules and inverters. Through this joint research lab, we can strengthen our partnership and contribute to the technical innovation of automotive power solutions centred on SiC," Ino concludes.

Heraeus launches new bonding ribbon for SiC modules

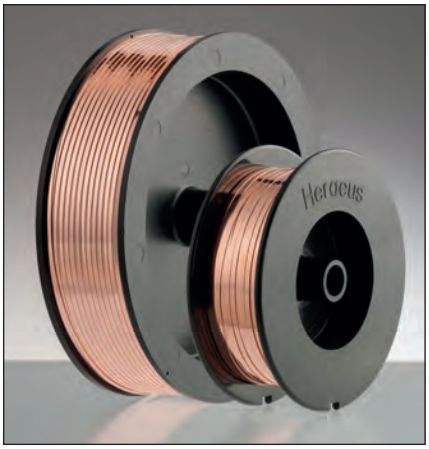
HERAEUS has announced a copper bonding ribbon called PowerCuSoft Ribbon that it has optimised for surface contacting on SiC semiconductors.

Copper offers better thermal, electrical and mechanical properties compared to aluminium wire and ribbons. The material heats up less than aluminium and can withstand higher module temperatures – this improves the lifespan and reliability of power modules, according to the company.

PowerCuSoft Ribbon can withstand module temperatures of up to 250degC. In tests, copper ribbons show a ten to twenty times longer service life than comparable products made of aluminium, while at the same time increasing the energy density in the module.

"SiC semiconductors are in the fast lane due to their high power density," says Christian Kersting, product manager power bonding wires at Heraeus Electronics. "In order to be able to use the advantages of these products, module manufacturers need high-performance packaging and interconnection technologies."

Compared to copper wires, ribbons also offer cost advantages, as one ribbon replaces several copper wires. Manufacturers are thus able to optimise the manufacturing costs per module as output increases. Depending on the module design, even twice the number of modules per hour can be produced.



GaN and SiC power semi markets to pass $1B in 2021

WORLDWIDE revenue from sales of SiC and GaN power semiconductors is projected to rise to $854 million by the end of 2020, up from just $571 million in 2018, according to Omdia's SiC & GaN Power Semiconductors Report – 2020. Market revenue is expected to increase at a double-digit annual rate for the next decade, passing $5 billion by 2029. These long-term market projection totals are about $1 billion lower than those in last year's edition of this report. This is because demand for almost all applications has slowed since 2018. Moreover, device average prices fell in 2019. A note a caution: The equipment forecasts used to create this year's forecast all date from 2019, and do not take account of the impact of the COVID-19 pandemic.

SiC Schottky diodes have been on the market for more than a decade, with SiC metal-oxide semiconductor field-effect transistors (SiC MOSFETs) and junction-gate field-effect transistors (SiC JFETs) appearing in recent years. SiC power modules are also becoming increasingly available, including hybrid SiC modules, containing SiC diodes with Si insulated-gate bipolar transistors (IGBTs), and full SiC modules containing SiC MOSFETs with or without SiC diodes. SiC MOSFETs are proving very popular among manufacturers, with several companies already offering them. Several factors caused average pricing to fall in 2019, including the introduction of 650, 700 and 900 volt (V) SiC MOSFETs priced to compete with silicon superjunction MOSFETs, as well as increasing competition among suppliers.

By the end of 2020, SiC MOSFETs are forecast to generate revenue of approximately $320 million to match those of Schottky diodes. From 2021 onwards, SiC MOSFETs will grow at a slightly faster rate to become the best-selling discrete SiC power device. Meanwhile, SiC JFETs are each forecast to generate much smaller revenues than those of SiC MOSFETs, despite achieving good reliability, price and performance. Hybrid SiC power modules, combining Si IGBTs and SIC diodes, are estimated to have generated approximately $72 million in sales in 2019, with full SiC power modules estimated to have generated approximately $50 million in 2019. Full SiC power modules are forecast to achieve over $850 million in revenue by 2029, as they will be preferred for use in hybrid and electric vehicle powertrain inverters. In contrast, hybrid SiC power modules will be used in photovoltaic (PV) inverters, uninterruptible power supply systems and other industrial applications, mainly, delivering a much slower growth rate. There are now trillions of hours of device field experience available for both SiC and GaN power devices. Suppliers, even new market entrants, are demonstrating this by obtaining JEDEC and AEC-Q101 approvals. There do not appear to be any unexpected reliability problems with SiC and GaN devices; in fact, they usually appear better than silicon.

SiC MOSFETs and SiC JFETs are available at lower operating voltages, such as 650V, 800V and 900V, allowing SiC to compete with Si Superjunction MOSFETs on both performance and price. End-products with GaN transistors and GaN system ICs inside are in mass production, particularly USB type C power adaptors and chargers for fast charging of mobile phones and notebook PCs. Also, many GaN devices are being made by foundry service providers, offering in-house GaN epitaxial crystal growth on standard silicon wafers, and potentially unlimited production capacity expansion as volumes ramp.

CoolSiC for ultra-fast pit stops ...

SPAIN based power conversion group Ingeteam and Infineon have teamed up for best customer experience in superfast electric vehicle (EV) charging. Rated at 400 kW, the converter INGEREV RAPID ST400 from Ingeteam is based on CoolSiC MOSFETs in an EasyDUAL 2B housing.

A single charging point implements eight of Infineon's FF6MR12W1M1_B11 modules. Depending on the charging capabilities of the respective car, an EV now only needs to stop for a minimum of 10 minutes for an 80 percent percent battery charge. This is comparable to refueling a conventional car with internal combustion engine. The design of the INGEREV RAPID ST400 converter has proven to operate successfully at real life conditions. Already last year, the first project integrating this technology was developed, implemented, and commissioned by IBIL, the leading recharge technology services company in Spain, for Repsol, the multienergy provider and leading spanish petrol station operator.

Located at Ugaldebieta in the Bay of Biscay region, it was commissioned in October 2019 as a lighthouse project in the field of electro mobility. The facility on the heavily frequented A-8 motorway features four ultra-fast charging points. These units guarantee optimal distribution of the available power between the four vehicles that can be connected simultaneously. More importantly, the technology is flawless and operates without any major downturns since the start.

Panasonic Plasma Dicing

For higher throughput and increased yield per wafer

Plasma dicing addresses the challenges of dicing smaller and thinner dies.

BY PANASONIC

EVERY PERSON with a passing interest in electronics has heard of Moore's Law: the processing power of affordable CPUs – or the number of transistors on a chip - will roughly double every two years. It is credit to both Gordon Moore's foresight, and the technical and engineering teams around the world who continue to innovate, that the 'Law' is still even being discussed today.

Part of the reason for chip size reduction lies in the shrinking of technology nodes (process geometries). Currently the smallest node that is being manufactured in mass volume is 7nm, and even smaller sizes are under development in the industry. The increase in processing power and speed and the miniaturisation and integration of electronic functions that continue to result from such technological advances lie at the heart of the pervasiveness of electronics in our everyday lives: the smart phones that we rely on; the uptake of artificial intelligence in smart homes and cities; driverless vehicles; remote medical home diagnostics – there is not one aspect of life that electronic products and systems have not penetrated.

But for this to continue, it is not only in the area of photolithographic processing that technology needs to keep innovating. Once a wafer has been created it must be singulated into individual dies, and as dies are becoming smaller and thinner, many products are facing difficulties caused by the singulation or dicing process.

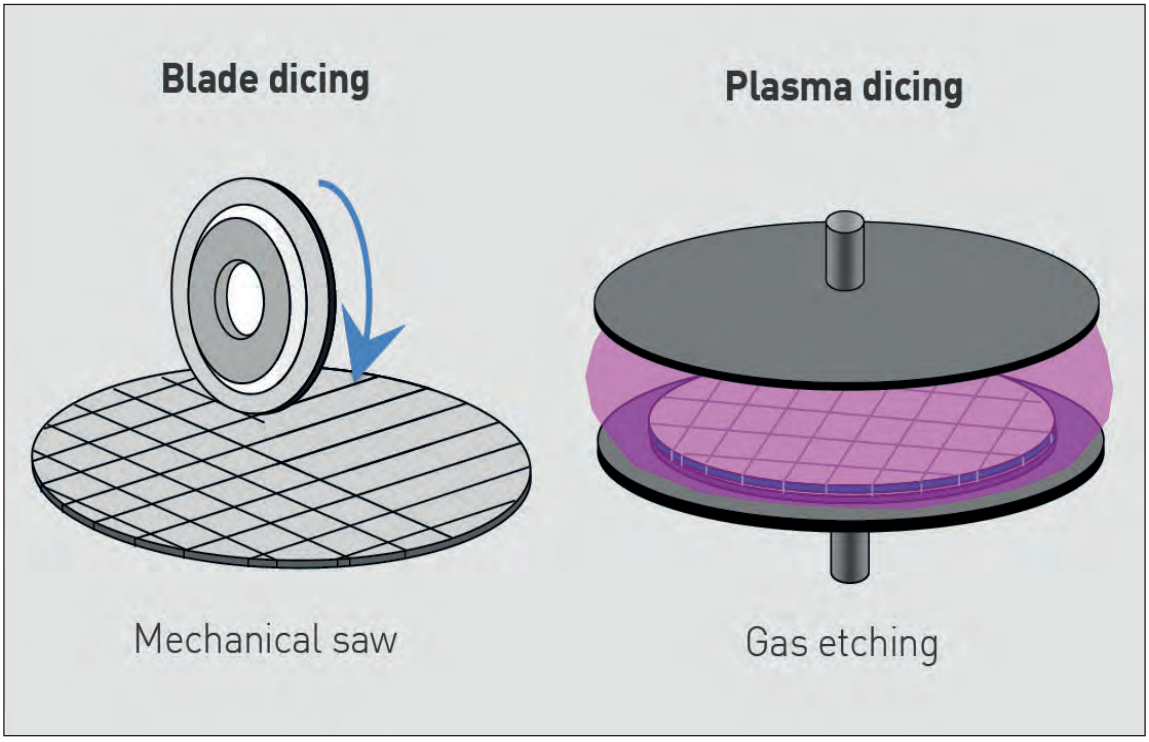


Figure 1: Blade dicing & Plasma dicing processing

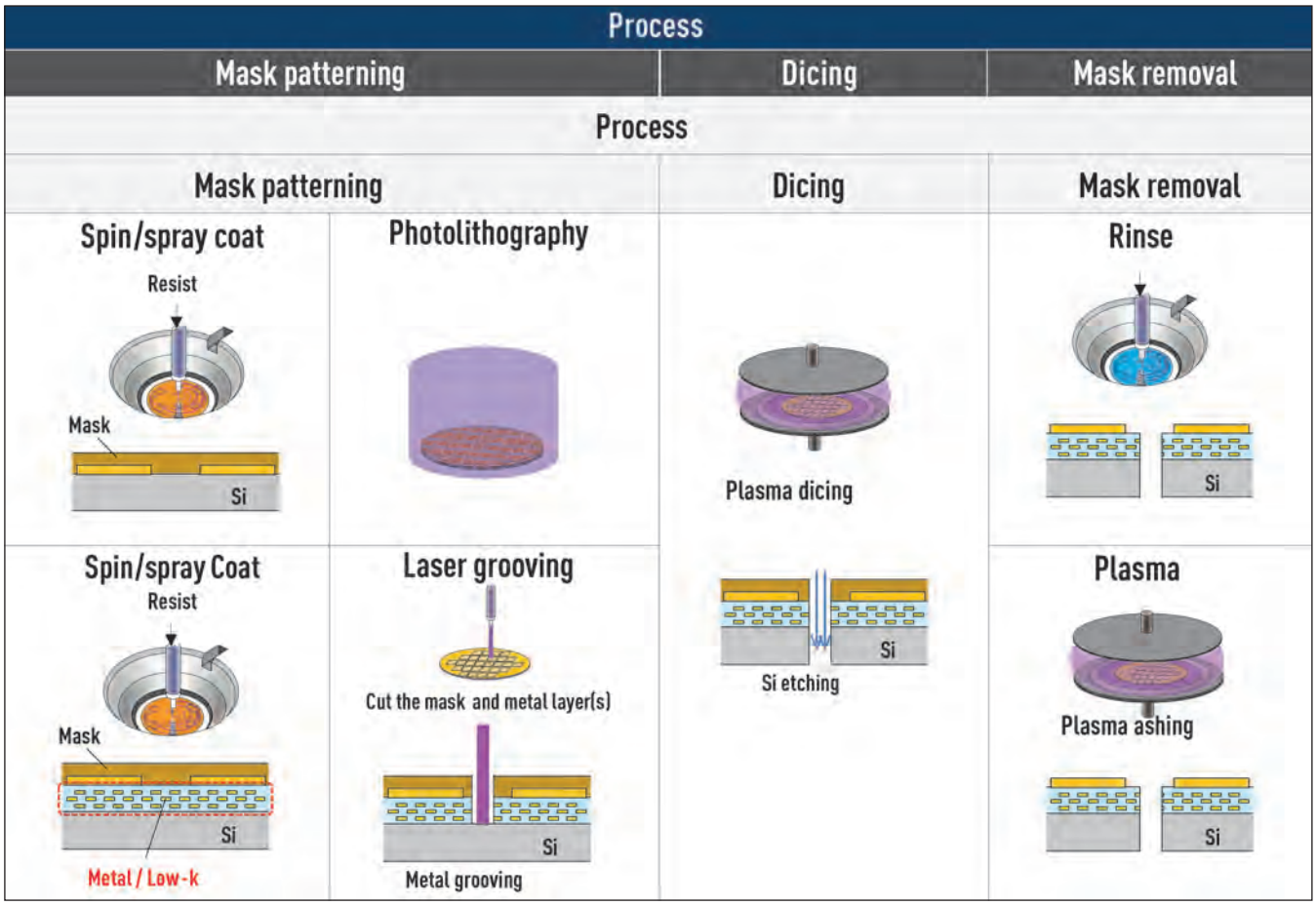


Figure 2: Panasonic's chemical etch dicing process

New challenges include: increasing material loss due to the width of the dicing street; mechanical damage such as chipping; and increasing processing time. Now, Panasonic has developed a plasma dicing process that in certain circumstances can replace mechanical dicing, which addresses these issues.

Types of dicing process

Traditionally, two dicing technologies have been used: scribing and breaking, and mechanical cutting using a dicing saw ("blade dicing"). Scribing and breaking causes stresses on the wafer and die and results in chipping and yield inefficiencies. Blade dicing also introduces stresses and contaminants which are more problematic as the die size and process geometries shrink. Laser dicing is another method which is faster than using a saw but can also cause cracking and damage to the chip.

Now, a new dicing process has been introduced which uses a plasma chemical etching process, where all the 'cuts' are achieved in a single batch process, with no die stressing, no contamination, and an increase in wafer dicing throughput. Also, more chips can be designed onto the wafer as narrower dicing 'streets' can be used due to mask patterning. In addition, the

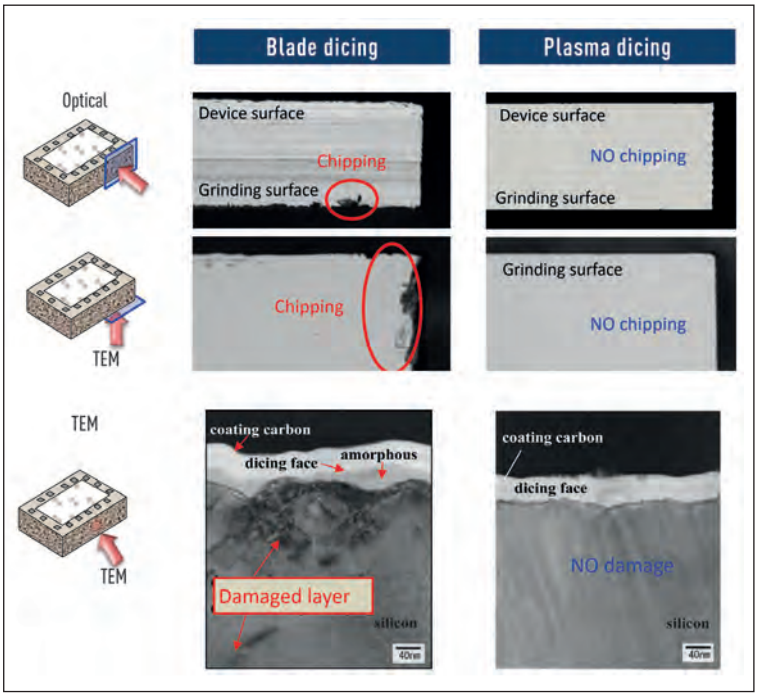


Figure 3: Damage evident on chip samples using blade dicing (left); none present when plasma dicing is used

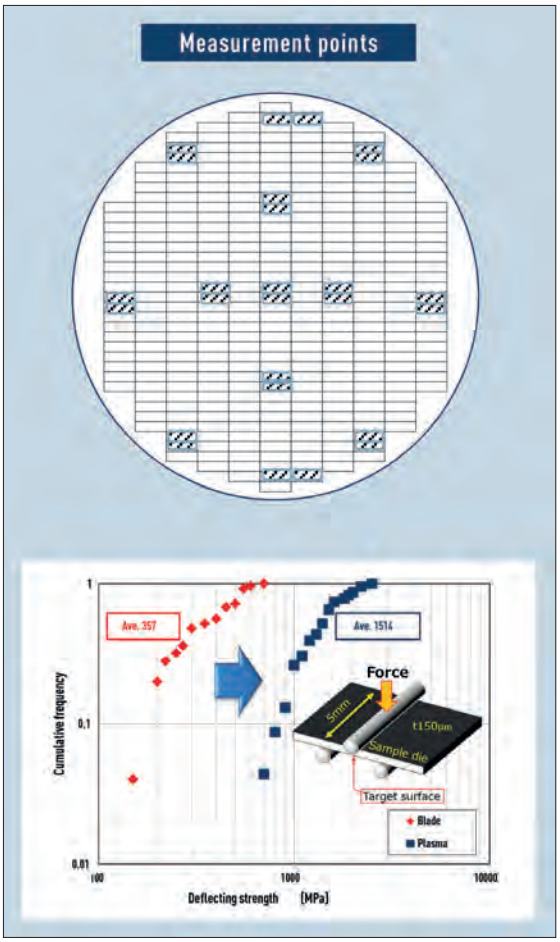


Figure 4: Strength tests prove the benefits of plasma dicing

mask pattern enables flexibility in the choice of chip sizes, shapes, positioning. The two approaches are shown in Figure 1.

Figure 2 shows Panasonic's plasma dicing process which uses a dicing mask. The plasma process etches the streets by chemical reaction. Plasma dicing uses pulsed or time-multiplexed etching, with the process cycling repeatedly between two phases: a near-isotropic plasma etch where ions attack the wafer in a near-vertical direction; followed by the deposition of a chemically inert passivation layer which protects the entire substrate from further chemical attack.

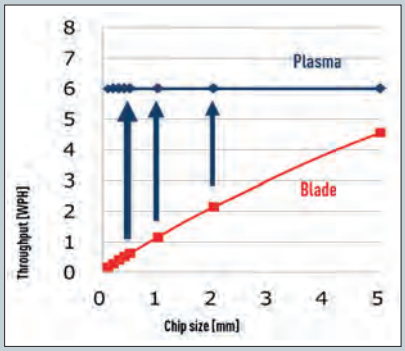
During etching, the vertically-directed ions attack the passivation layer only at the bottom of the trench (not along the walls), exposing the substrate to the chemical etch. This two-phase process results in side-walls that increase and decrease with an amplitude of between 100 and 500nm. The cycle time is adjustable: short cycles yield smooth walls; longer cycles yield a higher etch rate.

Particle-free and damage-free process

The action of the saw blade during the dicing process causes mechanical damage and affects inner layers of the die. Figure 3 demonstrates damage and chipping at the edge and of the inner layers. By contrast, the micro-photographs show no damage when the individual dies are separated using the plasma dicing process. Also, unlike blade dicing which causes micro particles of the wafer (e.g. silicon) to be freed up, potentially causing devices to fail, by using plasma etching, no contaminating particles are released.

Greater chip strength

Chip breakage tests show the typical range of fracture strength for silicon chips to be in the range of 100MPa up to 3000MPa. Dies from several positions on a 150μm thick wafer were sampled and a Weibull plot was used to compare the statistical data for chip strengths of lots using blade and plasma dicing preparation methods.



Left: Figure 5: Productivity curves show increasing benefits with smaller chip

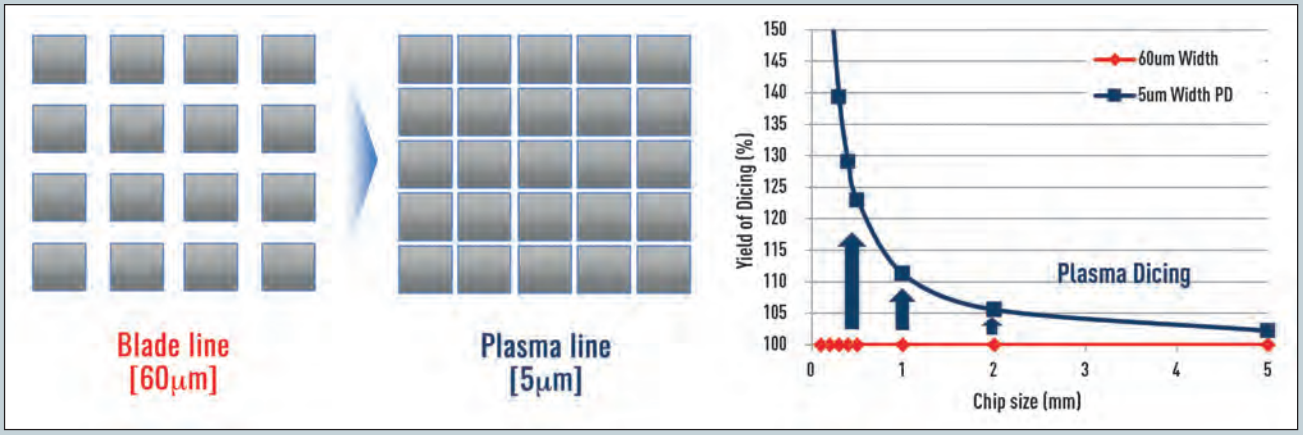


Figure 6: Reduced street widths result in more

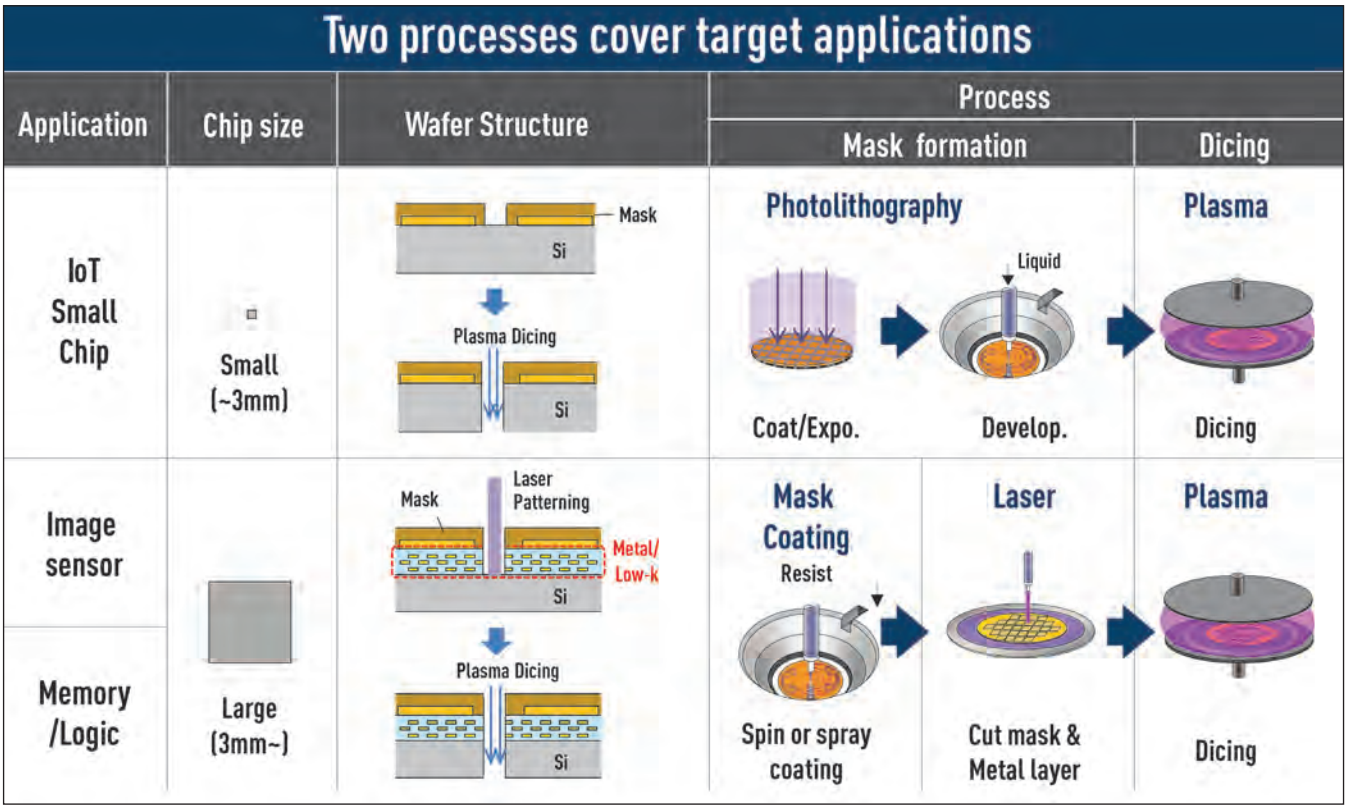


Figure 7: Panasonic plasma dicing

Figure 4 shows that the plasma dicing process results in chips that are about five times stronger than those which underwent blade dicing. With a fracture stress pressure of 600MPa, all samples of chips that had been processed using blade dicing broke due to internal micro- cracks, whereas all of the plasma diced chips shattered at a pressure close to the breaking-strength of silicon. Therefore the plasma dicing process is proven to result in dramatically higher chip strength, especially if thin wafers are being processed.

Higher throughput and yield

The processing time of blade dicing depends on the number of dicing lines. If the die size is small, longer dicing processing time is required and throughput is reduced. However, with the plasma dicing process, etching is performed across the whole wafer in one pass, so throughput remains constant, no matter how many dicing streets are required (see Figure 5).
In addition, the plasma dicing process uses a narrower dicing street design. With blade dicing, there is always a minimum cutting street width, due to the thickness of the blade. A simulation prepared by Panasonic shows that for a 0.5mm² chip size, reducing the dicing street width from 60μm to 5μm, yield will be increased by 23% using the new plasma process (see figure 6). However, the method of avoiding chips contacting other chips when handling a wafer with 5μm dicing street width needs to be considered.

Suitability for different wafer processes

The Panasonic plasma dicing process can be applied to wafer dicing with mask patterning either performed by photolithography or laser patterning methods. The appropriate process flow should be selected to fit the wafer design (Figure 7). Plasma dicing is a high quality innovation which offers different benefits depending on the end application, as shown in Figure 8. In small chips, for example, RFID tags, IoT devices or MEMS sensors, the ability to obtain a higher number of chips per wafer, plus the reduction in process time is paramount. For devices such as image sensors, the elimination of contaminating particles is essential, and the smoother, damage-free sidewalls, with no heat-affected zones or cracking, allows an increase in the active area. For makers of memory ICs, the elimination of damage is most significant.

Panasonic plasma dicing demo center

In order to demonstrate the plasma dicing process, Panasonic has built a customer demonstration centre

The processing time of blade dicing depends on the number of dicing lines. If the die size is small, longer dicing processing time is required and throughput is reduced

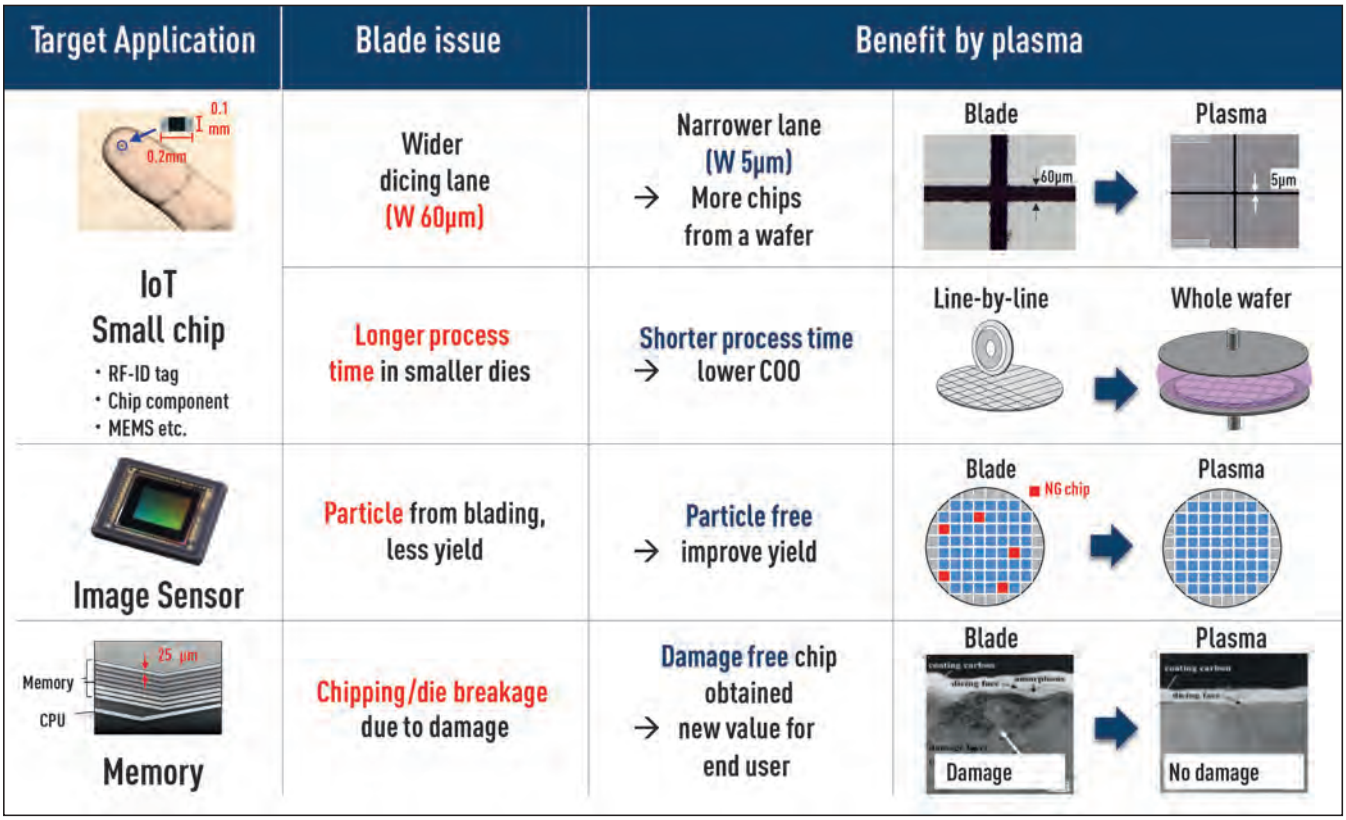


Figure 8: Benefits of Plasma

in Osaka, Japan. This Class 1000 facility is capable of processing 200mm and 300mm diameter wafers with a minimum thickness of 25μm. It is fully-equipped including two APX300 plasma dicing machines, laser pattern- ing equipment, polisher / grinder, lithography and measurement equipment, enabling customers to quickly and thoroughly evaluate different products and materials.

Total Solutions Approach

In addition to supplying the APX300 Plasma Dicer, Panasonic is in close contact with vendors globally to assist our customers with the integration and selection of appropriate equipment and material, and implementation of decades of process know-how.

Conclusion

Panasonic's plasma dicing process achieves damage-free and particle-free dicing, resulting in inherently stronger chips and increased yield. Throughput is increased and production costs reduced.

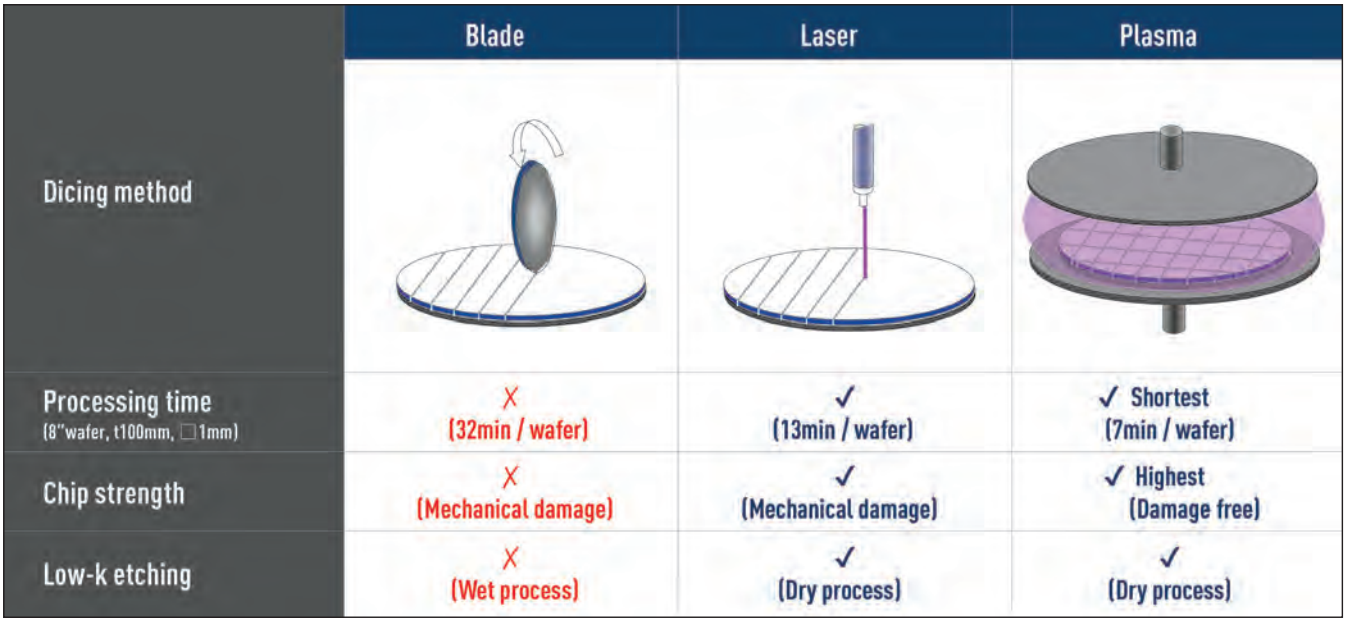


Figure 9: Summarises the different dicing processes and the advantages of the plasma dicing process

Power semiconductors

Perfecting the art of ultimate reliability.

Whether efficiently driving industrial motors, smoothly accelerating trains or transmitting gigawatt power over long distances and underwater – failure is not an option! That's why you need ABB Power Grids' power semiconductors that provide the ultimate in reliability and are the epitome of quality.

abb.com/semiconductors

KLA Corp. focuses on next-gen solutions for power applications

Power Electronics World technical editor Mark Andrews recently asked representatives of KLA Corp. to detail the ways that they are assisting customers address unique inspection and metrology requirements for power devices for automotive applications in addition to SiC and GaN technologies that seek to displace incumbent silicon technologies.

BY KLA CORP.

MA: Please describe KLA's specialized inspection systems for SiC substrates as well as processing within GaN-on-silicon manufacturing flows that target present and future automotive power requirements.?

KLA: SiC power devices pose unique yield and cost challenges in comparison to Si-based devices. Some of these challenges include:

- Much higher intrinsic material defect densities than Si-based devices
- High level of defect transference from substrate to epitaxy to device fabrication
- Variation in quality among substrate suppliers. Wafers graded and sold by dislocation density.
- Key defect issues include both crystallographic and morphological defects (carrots, surface triangles and stacking faults)
- Defect mechanisms act in the z-direction instead of x/y-plane. KLA's Candela 8720 compound

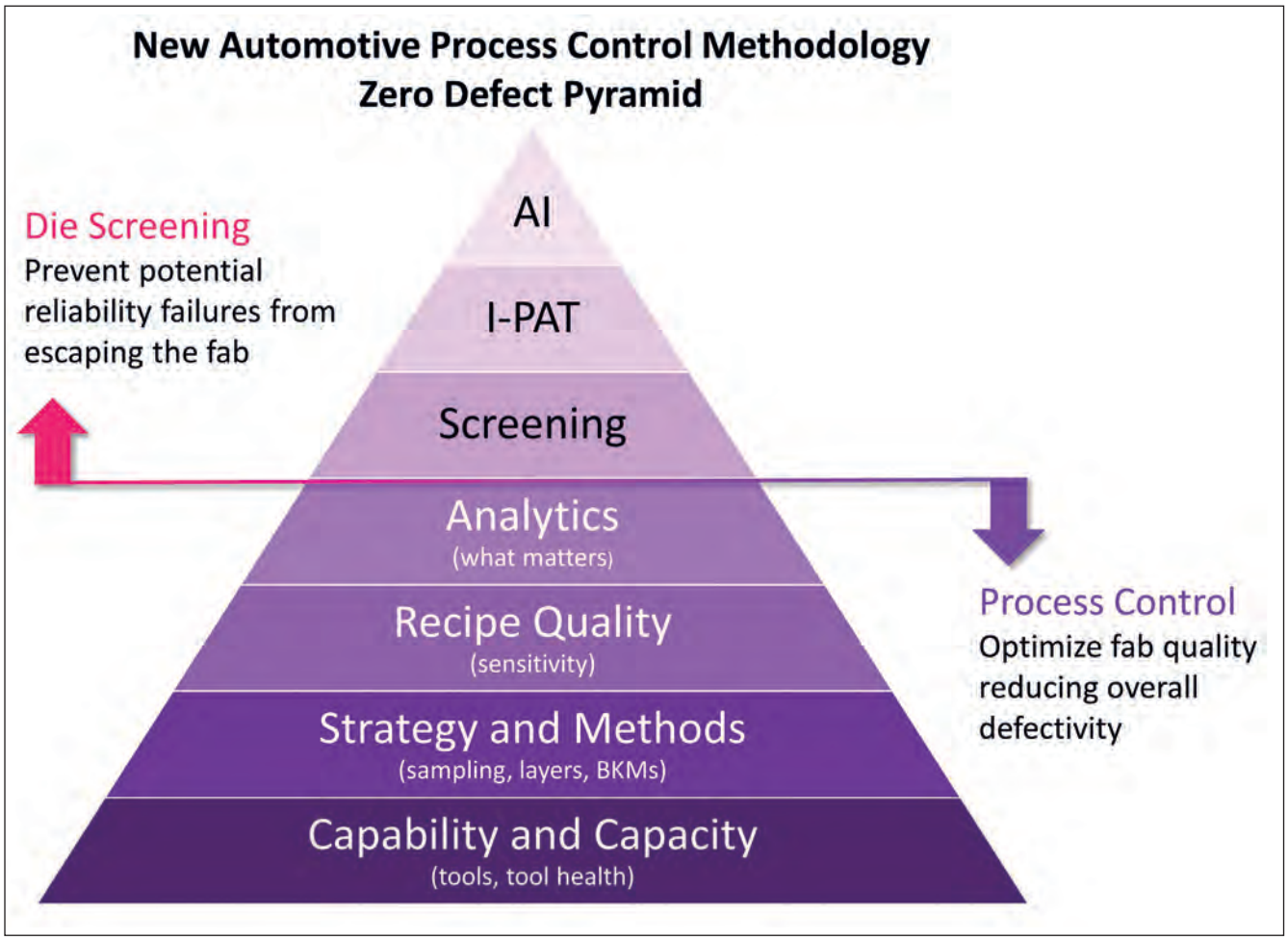


Figure 1: New automotive process control methodology Zero Defect pyramid

semiconductor material surface inspection system and the 8 Series patterned wafer inspection system have been developed to address these challenges.

The Candela® compound semiconductor material surface inspection system enables GaN-related materials, GaAs substrate and epi process control with high sensitivity to critical defects for the production of power devices, communications and RF devices, and advanced LEDs (as well as upcoming micro LEDs).

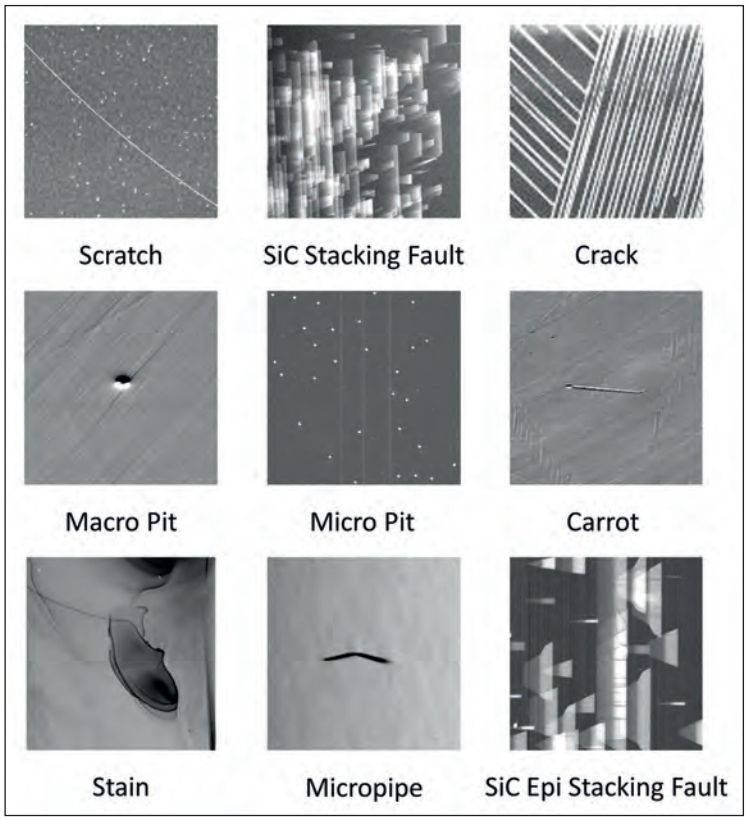
With its proprietary optical design and detection technology, the Candela inspection tool utilizes signals from scatterometry, reflectometry, ellipsometry, slope and photoluminescence detectors to detect and classify yield-limiting, sub-micron defects to support production-line monitoring.

The Candela 8720 system is used to monitor the substrate IQC (incoming quality control) and OQC (outgoing quality control) processes for a variety of defect types including particles, scratches, stains, pits, micropipes, stacking faults and other crystallographic defects.

For the post epitaxial growth process step, the inspection system can detect and monitor process issues such as cracks, macro epi disturbances (such as droplets), epi pit, epi bump, crystal-oriented defects (such as single/bar stacking faults, BPDs, etc.), micropits and particles. Defects in the substrate and post epi growth can significantly impact end of the line yield, so detecting and correcting such process issues at the source – where cost is the lowest – is critical. Patterned wafer inspection of SiC semiconductor devices is important for reducing defectivity and maintaining traceability, but inspection can present several unique challenges.

Wafer thickness and warpage are outside typical SEMI standards. The transparent (SiC) substrate can create challenges for focus systems and create unwanted noise when imaging the wafer. The 8 Series patterned defect inspection tool addresses these challenges through a specialized prealignment and chuck, selectable illumination wavelengths and depth of focus for inspection, multiple inspection channels and increased wafer handling flexibility.

With simultaneous brightfield and darkfield inspection capability, it captures all types of surface defects with a multi-level defect binning solution. With optional back side inspection capability, the 8 Series system can handle and inspect both frontside and back side



of 6" SiC pre- and post-grind wafers offering high precision frontside to back side correlation and die inking for process-induced killer defects on both sides of the wafer.

It is important to note that beyond some of the early SiC process steps, the many remaining steps for SiC are very similar to a standard silicon chip process, so SiC fabs will utilize similar process control strategies compared to silicon IC fabs.

MA: Producing automotive ICs and packaged devices present unique challenges beyond greater reliability such as the need to produce spare parts for years longer than consumer electronics. How does KLA technology help device manufactures meet these critical needs?

KLA: Automotive fabs have faced this problem for years and they do it by maintaining the process control strategies and standards that they used successfully in the past. This is shown through the defect pyramid (see Figure 1). In order to help maintain these strategies along with the best performing tools, KLA works with our customers in two areas:

- KLA helps customers by making continuous improvements on the process control platforms through product upgrades.
- KLA provides an extensive service package that helps our customers ensure that the process control tools are performing at the highest levels.

In addition, KLA also offers metrology and inspection tools that enable component sorting to prevent defective devices arriving at the assembly line and to keep track records of each device. Metrology helps verify whether device dimensions are within tolerance and thus confirming the quality of packaged products; inspection verifies that there are no particles, burrs or other defects present that could impact the yield.

MA: Can KLA detail its approach to supporting the power devices market and how experience in supporting other areas of the IC industry benefit their approaches to power electronics?

KLA: The company has been delivering solutions and support to the SiC and GaN power device market segment for some time. Leveraging our vast experience in developing new technology capable of solving complex inspection and metrology challenges across the IC industry to help drive yield improvements, we have developed a comprehensive portfolio of process control solutions specialized for the unique needs of power devices. In addition, through our subsidiary SPTS Technologies, we offer industry leading plasma etch, PVD and CVD wafer processing systems that are used in the manufacture of SiC and GaN devices.

There are several unique challenges in the manufacturing of power devices. Although the design rule is larger, there are special requirements beginning with the substrate and the early epitaxial process. These include, but are not limited to, thickness, wafer handling, substrate shape and quality, epitaxial dislocations, stacking faults and a number of other defect types which could limit the final device yield.

Working closely with our world-wide customers, both in development and in high volume manufacturing (HVM), KLA has engineered, delivered and improved our inspection and metrology offerings to provide the high quality inline data required to help drive yield and continuously improve cycle times.

MA: Packaging power electronics is often a challenge in and of itself. In the past, manufacturers often needed to create new package designs, especially for GaN and SiC. How does KLA support packaging requirements and what are its essential advantages?

KLA: The demand for packaging power electronics is widespread across different application types, including mobile and automotive, which results in the development of a wide variety of new packaging technologies to meet different requirements for overall performance, power, form factor and price.

The growth of 5G communication brings an increase in device power consumption, resulting in unique requirements for including more power management ICs. Therefore, development of advanced packages for these types of power devices is expected to

increase, and the resulting innovation will bring greater complexity and new process flows. Generally, IC packages are getting smaller, thinner and more complex, as seen with the integration of multiple dies and passive components into a system in package (SiP), but at the same time requiring higher power density and demanding stricter yield requirements. To meet the yield targets for new packaging technologies, more automated inspection of packages in the assembly and test processes will be required to ensure that defects are identified and sourced quickly during the manufacturing process.

Today's evolving automotive market is being driven by several key areas, most notably connectivity, electrification, and autonomous driving, which is resulting in increased IC content in every car. High reliability requirements for automotive push for Zero Defect standards in manufacturing. Because reliability affects both warranty and liability, as well as the brand image of car manufacturers – and potentially the safety of their customers – process control in packaging, from wafer level to component, will increase significantly in the coming years to find and eliminate the sources of defects and screen for costly excursions. Manufacturers must leverage every available opportunity for continuous improvement across the entirety of their manufacturing value chain to reach that goal.

and adopted. Tolerances on key features (i.e. size, thickness, warpage, interconnect size, alignment, etc.,) for these advanced packages are becoming tighter. Requirements for defect detection and classification accuracy are also increasing. Inline, non-destructive inspection and metrology characterization provide the signals required to enable customers to deliver advanced packaging innovation and differentiated solutions to the market.

High-end 3D profiling and metrology on wafer and panel can be measured with KLA's Zeta 5xx and 6xx systems. Wafer-level inspection and metrology process control with the Kronos™ wafer inspection system meets the requirements of high sensitivity and production-worthy throughput, while simultaneously addressing the challenges of wafer warpage, thin and thick substrates and numerous process variations typical of advanced packaging processes.

After dicing, the detection of hairline cracks in bare dies or in fan-in wafer-level packaging is achieved with the ICOS™ F160 die sorting and inspection system. It examines packages after wafers have been diced, delivering fast and accurate die sort based on detection of key defect types – including sidewall cracks, a new defect type affecting the yield of high-end packages.

To meet the yield targets for new packaging technologies, more automated inspection of packages in the assembly and test processes will be required to ensure that defects are identified and sourced quickly during the manufacturing process

For more traditional packaging types, the focus is largely on cost. Automatic inspection is available, providing the benefit of reducing overkill and then increasing yield. ICOS™ T3/T7/T8 and MV component inspection systems provide automated inspection and metrology capabilities across all different types of packages. With modular tool architecture, KLA can offer solutions to meet the requirements of many package types with varying size and interconnect styles.

Beyond traditional packages, mobile applications have been driving the development of smaller (dimensions below 3mm) and more complex packages. These include new technology such as fan-in wafer level packaging (FI-WLP), bare dies, fan-out wafer level packaging (FO-WLP) and SiP (system in package) for silicon-based packages.

We also expect similar levels of packaging innovations for SiC/GaN devices as they are further developed

Once packaged, the ICOS component inspectors provide higher accuracy and repeatability in characterizing key features of advanced packages. With high resolution defect detection, ICOS component inspectors enable discovery and classification of defects smaller than 10μm in mold or substrates and below 1μm for cracks in die.

The unique process control capabilities described thus far are critical to ensure performance of power electronics, but also to ensure optimal yield. Achieving high yields and meeting cycle time goals are challenging with new complex process schemes. Smarter, faster methods of analyzing large data sets and extracting critical information quickly to make decisions is required. Deep learning methodologies paired with advanced defect detection of packages helps to optimize the classification process, reduce overkill and maximize yield. KLA has extensive experience in working with customers to solve new packaging challenges and helping them succeed in

ramping new products while improving overall yield in a cost-effective manner.

MA: How does KLA support the unique inspection/ metrology challenges presented by SiC and GaN?

KLA: Starting with the substrate, dimensional wafer metrology systems from KLA's MicroSense offer precise, non-contact, automated geometry measurements including thickness, thickness variations, bow, warp, and 2D and 3D mapping on a wide range of substrates including sapphire, silicon, SiC, GaAs, glass, quartz, ceramics and graphene. For measurement and control of multilayer bonded wafers, our systems can measure total wafer stacks and individual layers throughout the wafer bonding, thinning and de-bonding process steps.

For metrology of power devices, our optical film thickness, overlay patterning and critical dimension instruments are successfully being deployed for inline process control at leading SiC and GaN customer fabs. We have developed a unique transparent wafer option to handle, transfer, align and measure various thin films on SiC on the F5x Pro film metrology system. The KLA Pro Archer™ overlay metrology platform enables production control of overlay and CD to help provide the data required for correcting the scanner.

For inspection, both SiC and GaN are complex material systems and each have very specific and unique process related defects that manifest in the substrate and after epitaxial growth process. Some of the similarities and differences between the two material systems include:

- Much higher intrinsic material defect densities in SiC based power devices
- Variation in quality among SiC substrate and GaN epi suppliers. SiC substrates are graded and sold by dislocation densities that are native to the substrate
- Morphological defects, crystallographic defects on SiC (such as carrots, triangles, stacking faults, basal plane dislocations), interfacial defects (such as cracks that originate at the interface of GaN and the substrate on which the epi is grown)
- Defects on SiC post epitaxy growth are directional while on GaN the defects are non-directional

KLA has developed unique solutions to meet the inspection requirements of both SiC and GaN materials systems.

The Candela® 8720 compound semiconductor material surface inspection system enables GaN-related materials, GaAs substrate and epi process control with high sensitivity to critical defects to produce GaN based power devices, communications and RF devices, and advanced LEDs (as well as upcoming microLEDs). With its proprietary optical design and detection technology, the Candela inspection tool utilizes signals from scatterometry, reflectometry, ellipsometry, slope and photoluminescence detectors to detect and classify yield-limiting, sub-micron defects to support production-line monitoring.

The next generation of the award winning Candela® CS920 – the industry's first integrated surface and photoluminescence SiC inspection tool - is enhanced with greater sensitivity for monitoring the substrate IQC (incoming quality control) and OQC (outgoing quality control) processes for a variety of defect types including particles, scratches, stains, pits, micropipes, stacking faults and other crystallographic defects. For the post epitaxial growth process step, this inspection system can detect and monitor process issues such as cracks, macro epi disturbances (such as droplets), epi pit, epi bump, crystal-oriented defects (such as single/bar stacking faults, BPDs, etc.), micropits and particles.

Defects in the substrate and post epi growth can significantly impact end of the line yield, so detecting and correcting such process issues at the source is critical--where cost is the lowest. Patterned wafer inspection of SiC semiconductor devices is important for reducing defectivity and maintaining traceability, but this need presents several unique challenges. Wafer thickness and warpage are outside typical SEMI standards. The transparent substrate can create challenges for focus systems and create unwanted noise when imaging the wafer. The 8 Series patterned defect inspection tool addresses these challenges through a specialized pre-alignment and chuck, selectable illumination wavelengths and depth of focus for inspection, multiple inspection channels and increased wafer handling flexibility.

With simultaneous brightfield and darkfield inspection capability, the tool captures all types of surface defects with a multi-level defect binning solution. With optional back side inspection capability, the 8 Series system can handle and inspect both the front side and back side of 6-inch SiC pre- and post-grind wafers offering high precision front side to back side correlation and die inking for process-induced killer defects on both sides of the wafer. As the demand for power devices continues to grow, we are adapting our portfolio to the needs of our customers, so they have the data they need to control their process. Both SiC and GaN have unique challenges compared to silicon; inspection and metrology data can help provide valuable information required to move the process from R&D to high volume production.

Replies from KLA Corporation were supplied by:
Robert Cappel, Senior Director of Marketing;
David P. Price, Sr. Director, Automotive Technical Solutions;
Mukundkrishna Raghunathan and Oliver Dupont, Product Marketing Managers."

Angel
BUSINESS COMMUNICATIONS

WEBINARS

Specialists with 30 year+ pedigree and in-depth knowledge in these overlapping sectors:

Expertise: Moderators, Markets, 30 Years + Pedigree
Reach: Specialist vertical databases
Branding: Message delivery to high level influencers via various in house established magazines, web sites, events and social media

Semiconductor (Silicon/Compound)
Publications include: Compound Semiconductor, Silicon Semiconductor, CS China, SiS China

Power Electronics
Publications include: Power Electronics World

Future Mobility
Publications include: TaaS Technology, TaaS News

Data Centres
Publications include: DCS Europe, DCS UK, SNS International

SmartSolar UK & Ireland
Publications include: Solar and Power Management, Solar UK and Ireland

Sensors
Publications include: Sensor Solutions Magazine, Sensor Solutions International

Digitalisation
Publications include: Digitalisation World, Information Security Solutions, Managed Services

Photonics
Publications include: PIC Magazine, PIC Conference

Expert Moderators

Dedicated technical and time-served experts/editors

MARK ANDREWS
Mark Andrews is technical editor of Silicon Semiconductor, PIC Magazine, Solar+Power Management, and Power Electronics World. His experience focuses on RF and photonic solutions for infrastructure, mobile device, aerospace, aviation and defence industries

PHIL ALSOP
Journalist and editor in the business to business publishing sector for more than 30 years currently focusing on intelligent automation, DevOps, Big Data and analytics, alongside the IT staples of computing, networks and storage

JACKIE CANNON
Director of Solar/IC Publishing, with over 15 years experience of Solar, Silicon and Power Electronics, Jackie can help moderate your webinar, field questions and make the overal experience very professional

DR RICHARD STEVENSON
Dr Richard Stevenson is a seasoned science and technology journalist with valuable experience in industry and academia. For almost a decade, he has been the editor of Compound Semiconductor magazine, as well as the programme manager for the CS International Conference

For more information contact:

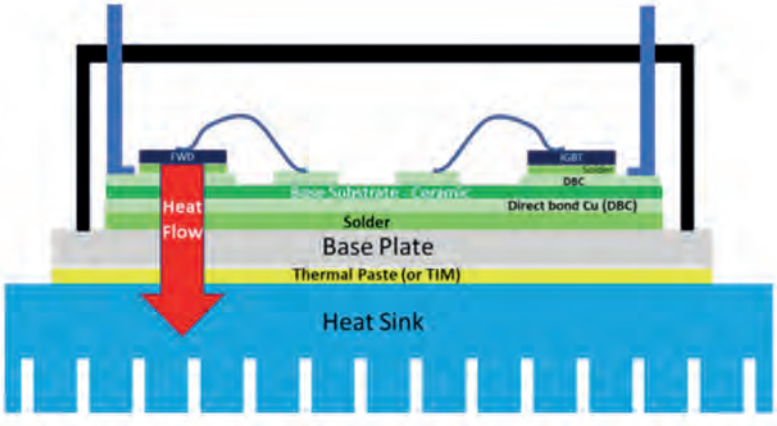
Jackie Cannon **T:** 01923 690205 **E:** jackie@angelwebinar.co.uk **W:** www.angelwebinar.co.uk
6 Bow Court, Burnsall Road, Coventry, CV5 6SP. UK
T: +44(0)2476 718 970 **E:** info@angelbc.com **W:** www.angelbc.com

New Thermal Interface Material (TIM) improves lifetime and performance of LoPak1 modules

Heat generated during the operation of IGBT switches is a constant threat to the survival of microelectronic chips within power modules. ABB has developed a new thermal interface material (TIM) that can be applied to the base plate surface; the company has demonstrated its new TIM layer can effectively extend the life and improve performance of power modules across a wide range of high voltage applications.

HEAT GENERATED by power losses during the operation of IGBT switches must be removed from the chip to prevent the junction temperature of semiconductor devices from rising beyond maximum allowable limits. Heat is transferred through the module to a heat sink, with the interface between the module baseplate; the heat sink typically has the highest thermal resistance and therefore contributes most strongly to the module thermal path resistance (Figure 1). The use of the TIM improves the thermal conduction across this interface ensuring more stability over long-term operation than commonly used conventional heat conductive pastes (Figure 2). The use of the TIM can increase the amount of current that can be safely switched by the IGBT and improve the module's lifetime, since the TIM's thermal resistance does not increase with the number of switching cycles.

ABB's 1700V LoPak1 modules will be available with improved lifetime and enhanced electrical performance derived from (optional) pre-applied thermal interface material (TIM) that is deposited on the outside module base plate surface that contacts the heat sink. Module orders scheduled for delivery from June 2020 onward will be able to specify this enhancement.



Layer	Contribution To Thermal Resistance
Baseplate to Terminal Material (Thermal Paste)	50%
Device	3%
Solder	6%
Base Substrate - Ceramic	33%
Base Substrate - DBC	3%
Base Plate	5%

Figure 1: Heat flow pathway through module and layer contributions

Appearance	Paste	TIM
Color	White or Grey	Grey
Base Material	Silicone Fluid with filler	Phase Change Material with filler
Consistancy @ room temperature	Viscous	Hard
Thermal Conductivity (W/mK)	0.8 – 3.0	5.2

Figure 2: Comparison of materials used between base plate and heat sink

The amount of thermal material applied, and its application pattern critically affect the thermal resistance of the interface. ABB Power Grids applies the TIM in a paste form using automatic stencil printing during module fabrication. This paste transforms into a solid through the use of a curing / drying process performed after coating. The TIM layer remains solid at room temperature reducing the potential for damage to the print pattern by accidental contact. Being a solid also makes module handling and installation easier for the customer. The design of the TIM pattern takes into account the locations of highest heat generation and the module's intentional baseplate bending; it ensures that the best metal-to-metal contact is made between the module baseplate and the heatsink (figure 3). The process is automated to ensure the repeatability required for volume production.

An alternative to ABB's thermal interface material involves the application of conventional heat conducting paste, which is applied by the customer manually using stencil printing. This process leads to higher variability in the amount of material applied and non-uniformity of its application across the interface area. The paste also remains viscous throughout the process.

The improved thermal stability of TIM, as compared to heat conductive pastes, can be seen during power cycling (figure 4), which is a standard test to simulate the degradation of the module over its lifetime by thermo-mechanical stress. The test was run for 9,400 cycles, in line with the JESD51-14 specification, using the maximum allowable junction temperature of 150oC, with a total cycle time of 120 seconds (ton = toff = 60s), dTc = 65-75K.

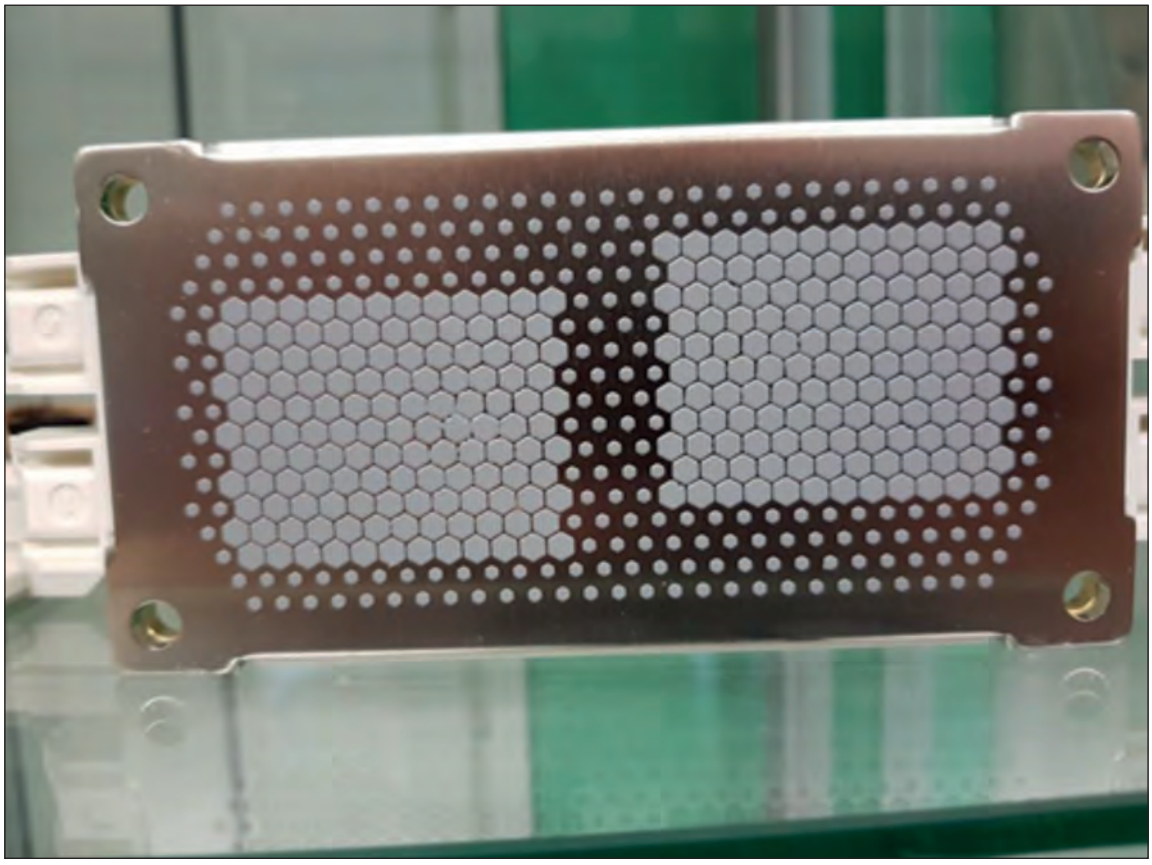


Figure 3: Base plate bottom surface with TIM applied

Thermal Resistance, Average over 9400 Cycles	Paste	TIM	Improvement
Junction to Ambient (K/kW)	114.75	106.66	7%
Case to Ambient (K/kW)	73.92	65.93	11%

Figure 4: Performance of TIM compared to heat conductive paste

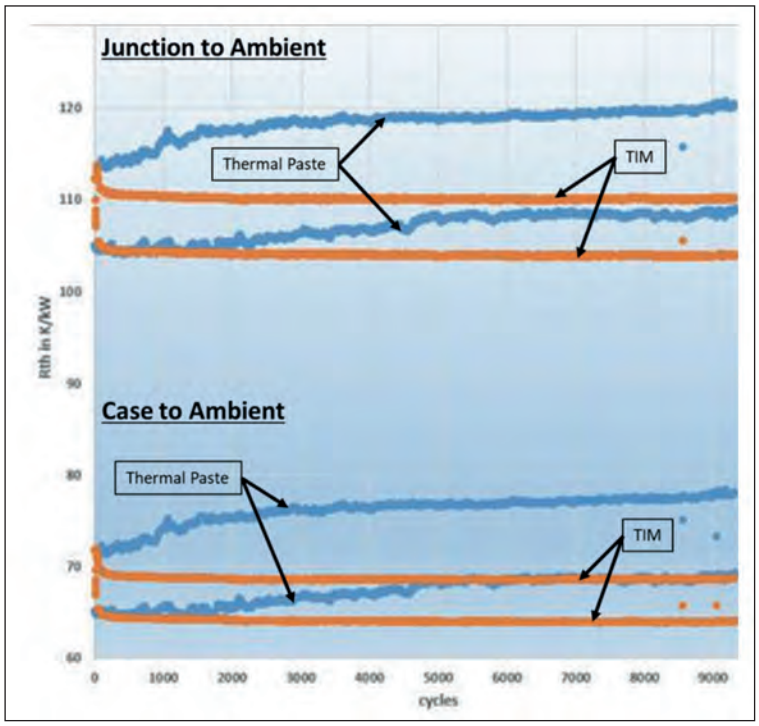
The results of this testing showed:

- A 7 percent improvement in the average thermal resistance for the entire pathway from the IGBT junctions to ambient when the TIM is used instead of heat conductive pastes
- An 11 percent improvement in the average thermal resistance from the case to ambient when the TIM is used instead of heat conductive pastes

The impact of using ABB's TIM rather than heat conductive paste can be seen by looking at data from the cycling test (figure 5) for the partial thermal resistance from the case to the heat sink (where the TIM is located) and for the entire path between the transistor junction and the heat sink. While the initial thermal conductivity of pre-applied TIM is comparable with the heat conductive paste, the modules using TIM show no increase in thermal resistance with cycling, while those using the heat conductive paste show increasing thermal resistance during the test.

These results imply degradation of the thermal interface for the heat conductive paste and demonstrate the better long-term stability of the TIM. The improved consistency of performance is because the TIM becomes viscous when it is heated to temperatures above 45°C by the operation of the transistors. This allows it to spread out evenly across the interface during thermal cycling to provide a homogeneous coating across the base plate/heat sink interface while dramatically reducing material pump-out. The use of the TIM improves the thermal transfer between power module and heat sink when compared to conventional heat conductive pastes, improving the long-term reliability and performance of the module. The TIM option will be available for LoPak modules beginning in June 2020.

Figure 5: Comparison of TIM and heat conductive paste stability



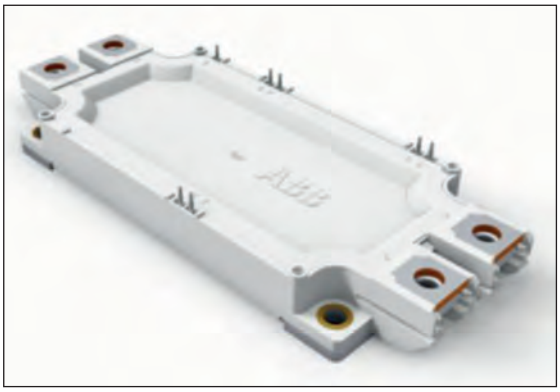


Figure 6: Image of ABB's LoPak 1.7kV 450A IGBT module

About LoPak

LoPak devices are medium power IGBT modules (figure 6) that enable extra transient over-current capability by taking advantage of the IGBT module's maximum operating junction temperature of 175°C, compared to the typical 150°C. The configuration is a 1700V phase-leg (half-bridge) IGBT module with a copper base plate that utilize ABB's uniquely designed SPT++ IGBT and diode devices. Current ratings of 450A, 300A and 225A are available.

The LoPak devices provide outstanding safe operating area (SOA) and over-temperature capability and benefit from ABB's expertise in ensuring robust electrical performance and high reliability. The careful design and virtual prototyping used by ABB makes the LoPak module's current distribution well-balanced during switching and ensures control under overload conditions. Extensive customer feedback confirms that LoPak modules have the same 'DNA' for high reliability and robustness as the entire family of ABB's high-power semiconductors.

Applications for LoPak modules include renewable energy and industrial sectors; LoPak plays a key role in ABB's expanding catalog of products that support existing and emerging market requirements.

Industry counts on SEMI standards.

SEMI is the global industry association serving the product design and manufacturing chain for the electronics industry.

Check out our new standards on SMT & PCB Manufacturing Equipment Communication, Panel Level Packaging & Energetic Materials at:

www.semi.org/collaborate/standards

semi™

Charging the UK to power an EV future

Julian Skidmore, Senior Software Engineer at embedded systems consultancy ByteSnap Design

DRIVEN BY CONCERNS over global heating and improvements in battery technology, electric vehicles are the most promising solution for emissions-free transit, but one barrier to adoption is the slower-developing EV charging infrastructure which can be inconsistent and difficult to use.

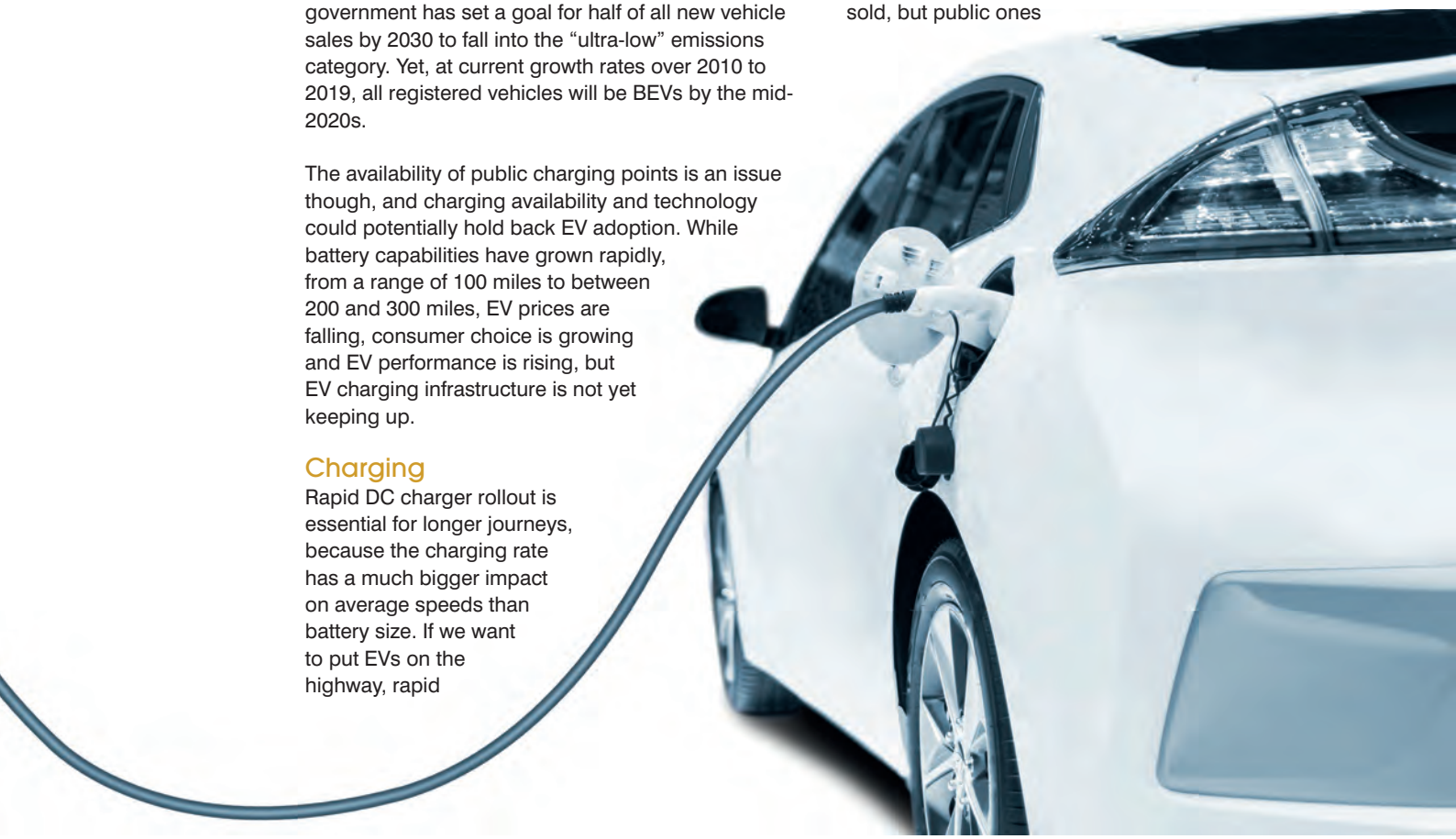
Battery electric vehicle (BEV) sales in the UK are projected to be around 100,000 during 2020 and the government has set a goal for half of all new vehicle sales by 2030 to fall into the "ultra-low" emissions category. Yet, at current growth rates over 2010 to 2019, all registered vehicles will be BEVs by the mid-2020s.

The availability of public charging points is an issue though, and charging availability and technology could potentially hold back EV adoption. While battery capabilities have grown rapidly, from a range of 100 miles to between 200 and 300 miles, EV prices are falling, consumer choice is growing and EV performance is rising, but EV charging infrastructure is not yet keeping up.

Charging

Rapid DC charger rollout is essential for longer journeys, because the charging rate has a much bigger impact on average speeds than battery size. If we want to put EVs on the highway, rapid charging matters more than a large battery, but for local or urban driving there will be a market for smaller battery, slow charging EVs.

AC chargers, like those at home, with slower charging and lighter loading are best for grid management with local or urban driving. That's because most journeys are short, so their energy requirements won't change over time. Home chargers obviously keep up with EVs sold, but public ones



aren't so they should be targeted, because they're cheap and cover most cases. Some of the new cars in 2020 will have modest batteries, short ranges and 7KW charging as standard.

User experience

EV chargers are less user-friendly than we'd expect from something that is powering our driving future. Billing mechanisms can be "nasty" and payment methods inconsistent; connections can be faulty or intermittent; systems can crash and user interfaces that are on the opposite side of the charger from the plug cause inconvenience. We wouldn't accept this lack of service at a petrol station and EV journeys shouldn't have to be that stressful.

Revolution

While we are at the beginning of the EV revolution, which presents an opportunity without the constraints of fossil fuel powered cars which need piping, tankers, stations and Just In Time logistics, better government support and initiatives are needed to support charging locations and a good geographical distribution of chargers. Subsidies for charging network providers may also be needed, along with consideration of load balancing, as distributed energy could cause intermittent supply.

Usage restrictions and non-standardised interfaces represent wasted engineering effort that actually slows down adoption and finally charging points are unmanned, resulting in maintenance issues. However, that could actually present an opportunity for a new service industry.

Although charger manufacturers would like a comprehensive networking protocol between the charger and the car, the IEC 61851 and 62196 specifications have led to a plethora of CAN bus, IP over Power and crude PWM communications along with incompatible plugs. Combined with that, manufacturers' reluctance to provide useful EV battery charging status (to protect their patents) will also continue to inhibit the potential for Smart EV charging.
Vehicle to Grid (V2G)

Because batteries also represent a source of base-load microgeneration, EVs can be part of the energy solution. ByteSnap, in collaboration with a consortium of partners, is working on a two year project called VIGIL (Vehicle-to-Grid Intelligent Control), which will see the development of a new communication and control platform for vehicle-to-grid (V2G) and vehicle-to-building (V2B) systems.

V2G technology could mean that EVs can return energy to the power grid when stationary and plugged in, increasing energy grid resilience and providing payback for EV drivers. V2G connectivity could also take advantage of the new phenomenon of renewable energy surplus. Germany is one country where consumers can experience negative energy prices,

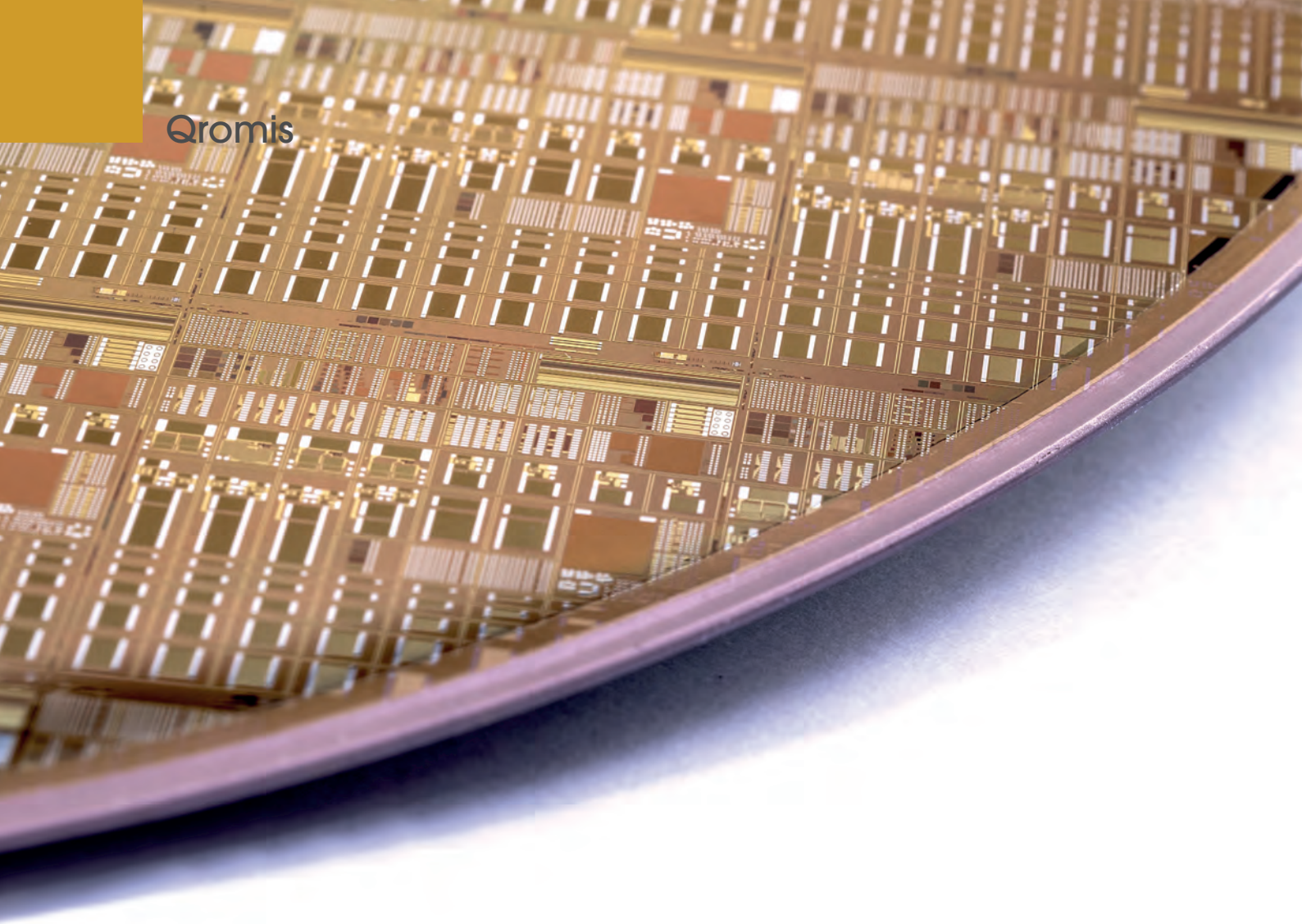
thanks to renewable and green energy initiatives. VIGIL would promote comprehensive charging communications, in turn aiding EV adoption, with ByteSnap's smart communications controller (called RAY) managing the charge going back into the smart building, or substation. In turn, substation energy can flow into the smart building; charge EVs or return power to the grid.

Future

Appless charging, where EV owners can tap a credit or debit card on a charging post to start and stop charging is something every EV driver would like. Some Polar Ultrachargers already have a contactless payment method and Ecotricity Electric Highway plans a similar upgrade, despite the plan bringing with it higher charging costs.

Combining substations with urban car parks could help solve issues of kerb-based charging sockets which can be inaccessible or easily damaged. Secure multi-storey car parks with built-in charging facilities where the infrastructure is in one place and therefore cheaper to implement, upgrade and maintain, would clear streets of EVs and provide security.

Alongside V2G facilities, fully automated charging is the dream of every EV driver. Intuitively, robots would plug in charging cables, but this over-engineering of a human oriented interface might better be met by inductive charging, though since that requires charging mechanisms to change yet again it's more likely in the long term. EVs are the most likely technology to replace fossil fueled vehicles and the nascent world of EVs is a rapidly accelerating, disruptive market, which charging technology and infrastructure is as critical to as the vehicles themselves. Driving the deployment of EVs will come from making EV driving as effortless and attractive as petrol and diesel vehicles.



Qromis: ready for business

As the GaN market gathers momentum, Qromis is serving up fab-friendly substrates and epi-wafers to ease device manufacture, reports Rebecca Pool.

IN JANUARY THIS YEAR, Silicon Valley based Qromis revealed two developments that signal the company is on the cusp of rapid expansion.

For starters, the fabless, wide bandgap materials business has just received an undisclosed investment from The Mirai Creation Fund, led by Japan-based investors SPARX.

At the same time, it has also signed a licensing agreement with Shin-Etsu Chemical, a Japan-based silicon wafer and materials manufacturer, to produce substrates and epiwafers for GaN power/RF electronics, LED devices and more.

Qromis' latest developments follow five years of development of its novel materials technology for substrates. And right now, chief executive, Cem Basceri, is excited.

"We've developed this unique CMOS fab-friendly substrate technology that is scalable and stress-matched to GaN," he says. "It sounds simple but it's taken years of development and investment."

"Now, a device manufacturer can take our substrate, and without any challenges, make many different device features," he adds. "This is extremely valuable."

Rapid progress

Qromis launched back in 2015 to commercialise its Qromis Substrate Technology, QST. Ready for GaN epi-growth, these substrates comprise an engineered coefficient of thermal expansion (CTE)-matched core onto which several engineered layers are deposited. A top thin silicon interface is also deposited onto the engineered layers.

Crucially, the CTE-matched core has a thermal expansion that closely matches the thermal expansion of the GaN-AlGaN epitaxial layers, enabling the deposition of low dislocation density, crack-free GaN epitaxy from a few microns to bulk-like thickness.

As Basceri highlights: “We did this so that the substrate would be stress-matched with GaN without any cracking or wafer breakage issue and also to prevent substrate cross-talk in integrated circuits, which is a big issue on silicon.”

Qromis has already released 6- and 8-inch GaN-ready QST substrates as well as 6- and 8-inch ‘templates’ with 5 µm and 10 µm GaN layers. What’s more, 200 V and 650 V GaN HEMT epi-wafers, based on 6-inch and 8-inch QST substrates, are being fine-tuned for commercial devices while 900 V and 1200 V GaN HEMT epi-wafers are also being developed and sampled.

The company’s rapid technology development follows partnerships and collaborations with a host of industry players up and down the supply chain. Within a year of launching, the company had partnered with Vanguard International Semiconductor, licensing its key technologies to the Taiwan-based silicon foundry for manufacturing.

Since 2016, the company has also worked closely with microelectronics innovation hub, imec, Belgium, on device fabrication, developing GaN power devices, in discreet and monolithically-integrated ICs forms, on 200 mm QST substrates in an advanced CMOS silicon pilot line.

Imec and Qromis have also been collaborating with GaN MOCVD equipment manufacturer, Aixtron, Germany, on GaN-on-QST epitaxy development. The results have been quite remarkable.

As Basceri points out, the industry standard platform for GaN-on-silicon has been 150 mm wafers. And while imec has pioneered the development of 200 mm GaN-on-silicon wafers for HEMTs to 650 V operating voltages, thermal mismatch between the GaN/AlGaN layers and silicon has stymied device fabrication at higher voltages.

Imec and Qromis have since developed enhancement mode *p*-GaN discrete and IC power devices on 200 mm QST substrates with epitaxy layers grown in Aixtron’s G5+ C 200 mm MOVCD platform. Crucially, imec was able to port its *p*-GaN e-mode power device technology to Qromis’ 200 mm GaN-on-QST wafers in its silicon pilot line, and also demonstrate high-performance power devices.

“Vanguard then decided to licence imec’s device technology, GaN power epitaxy and processes and the company is currently manufacturing and tuning devices to [partner’s] specifications,” says Basceri. “This has been a big turning point.”

Ramping manufacture

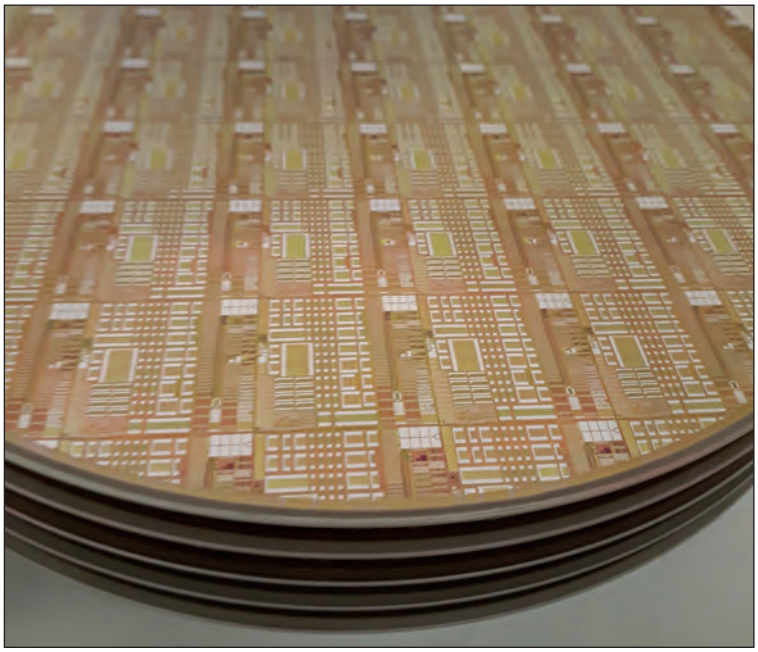
In line with healthy GaN growth forecasts, Basceri says Vanguard will ‘open its doors to everybody’ later this year, offering GaN power, and later RF, device manufacturing services on the 200 mm diameter QST platform. This has also prompted the Qromis chief executive to establish a second manufacturing source for QST substrates and GaN-on-QST epitaxy wafers, in the form of Shin-Etsu Chemical. Importantly, with this partnership, QST-based materials products will be commercially available from both Shin-Etsu and Qromis for industry players.

According to Basceri, Shin-Etsu is going to aggressively move ahead with the development of GaN-related products, supplementing its existing line-up of GaN-on-silicon, SOI and silicon wafers. As he says: “From what we hear from our partners and customers that use Vanguard, we are expecting wafer demand to reach tens of thousands of wafers in the next three-to-four years.”

With its substrates, Qromis will address a range of applications starting with GaN power and RF devices and later LED devices, such as microLEDs, and sensors. One of the key markets will be electric vehicles – as Basceri points out, a significant portion of SPARX’s Mirai Creation Fund comes from Toyota Motor Corporation, which is heavily entrenched in this market.

“We expect to start ramping up 200 millimetre manufacturing between 2021 and 2022, and I would also expect to see an overall demand for 300 millimetre wafers starting by 2025 for which we have already started to receive some initial inquiries,” says Basceri. “Several years ago, there were missing links in the GaN business, but the tipping point is now here.”

Qromis, Chief Executive, Cem Basceri



Unlocking the potential of SiC power modules with graphite

Replacing the copper core in insulated metal substrates with highly oriented graphite boosts thermal conductivity of the SiC power module while trimming its weight

BY WEI FAN AND DAWN KRENCISZ FROM MOMENTIVE QUARTZ TECHNOLOGIES, GARRY WEXLER FROM HENKEL CORPORATION AND EMRE GURPINAR AND BURAK OZPINECI FROM OAK RIDGE NATIONAL LABORATORY

CHOOSING YOUR NEXT CAR is far from easy. As part of being environmentally responsible, you will certainly want to consider purchasing a vehicle that runs solely on battery power. While such a vehicle will undoubtedly help to curb your carbon footprint, will it have sufficient driving range? Or will your car run out of juice on one of your long trips?

To avoid agonising over this dilemma, what is needed is the development of vehicles with a longer range between recharges. Increasing energy storage in the battery will help, along with a hike in the performance of the power electronics.

Such efforts are already underway in the United States supported by a Department of Energy roadmap that details requirements for next-generation electric drive systems. Targets include: a doubling of power handling capability to allow the electric traction drive system to handle peak powers of up to 100 kW; and a hike in power density from 13.4 kW/litre in 2020 to 100 kW/litre in 2025. Research institutes and industrial partners have been pouring tremendous resources and efforts into the development of the next-generation power electronics for electrical vehicles (see Figure 1).

Increases in power density must be accompanied by improvements to the thermal management system. However, this must be accomplished without adding weight to the vehicle, as weight will negatively impact travel range. Meeting this requirement demands more advanced thermal management methods beyond traditional heat pipes, water cooling, and fans.

Tackling this challenge of improving the thermal management of SiC power modules while trimming their weight is the objective of a collaborative partnership between Momentive Quartz Technologies, Henkel Corporation (Henkel) and Oak Ridge National Laboratory (ORNL). Working within the US Department of Energy Electric Drive Technologies Consortium, this partnership – from now on referred to collectively as the 'Group' – is redesigning the insulated metal substrate. This technology is light weight, featuring a thermally conductive graphite core. Armed with this approach, engineers can cut substrate weight by 30 percent and increase the power loading for the SiC power module by 15 percent or more, thanks to a near doubling of thermal conductivity.

Figure 1. An EV test platform at ORNL that was used to evaluate power modules for wireless charging

This technology promises to revolutionise the standard isolated multi-chip SiC power module. Today, if you cut open one of these modules you are likely to find SiC dies, on either a direct bonded copper or insulated metal substrate, mounted to a thick copper

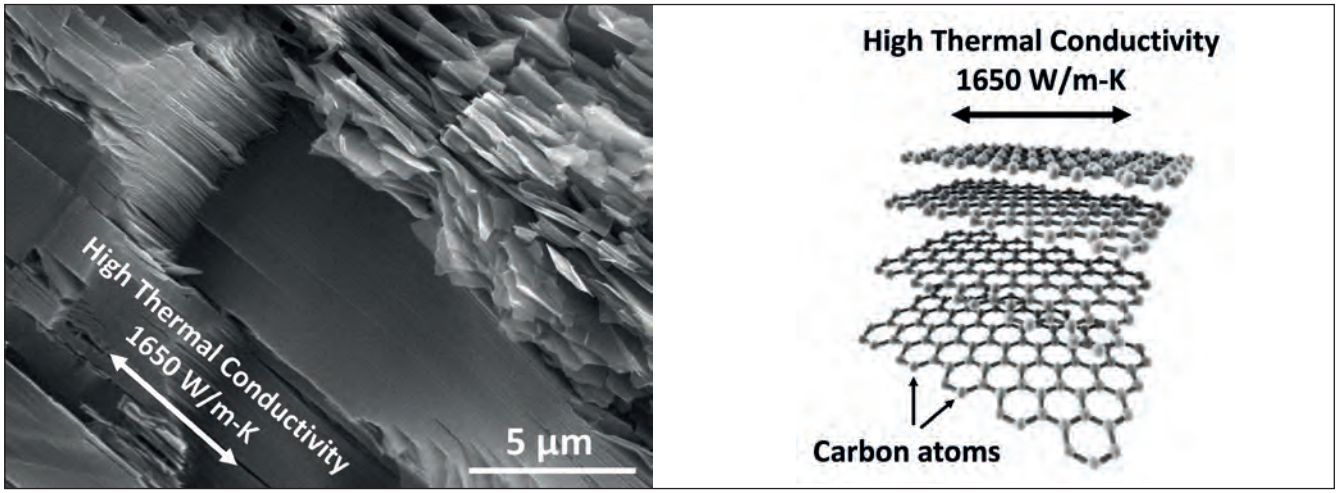


Figure 2. Cross-sectional view, provided by a scanning electron microscope, of Momentive Quartz Technologies' thermal pyrolytic graphite cores (left). An illustration of this material, showing well-aligned graphene basal planes (right).

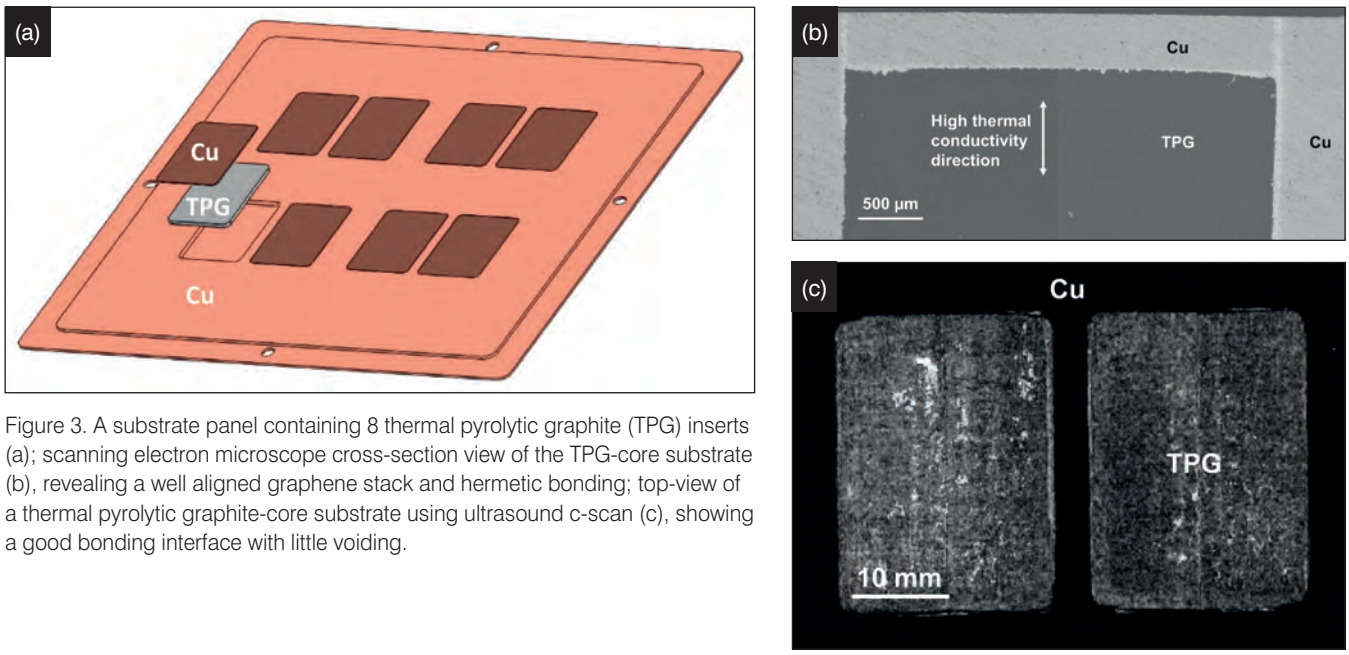


Figure 3. A substrate panel containing 8 thermal pyrolytic graphite (TPG) inserts (a); scanning electron microscope cross-section view of the TPG-core substrate (b), revealing a well aligned graphene stack and hermetic bonding; top-view of a thermal pyrolytic graphite-core substrate using ultrasound c-scan (c), showing a good bonding interface with little voiding.

base plate. These parts will be united by solder or epoxy bond layers.

When a direct-bonded copper substrate is used, it will typically provide good thermal conductivity and electrical isolation. Unfortunately, this usually comes at the expense of a thermal expansion mismatch, chemical instability, substrate rigidity, and a limit to layer thickness. These restrictions tend to hamper the performance of SiC power modules.

The common alternative, the insulated metal substrate, is made by stacking metal layers – often copper or aluminium – to a thermally conductive, electrically isolating dielectric layer. The result is a low-cost, flexible circuit structure that can be tailored by varying the thickness of the metal and dielectric layers. Unfortunately, the thermal conductivity in the dielectric has shown to be inferior to that of the ceramics in a direct-bonded copper substrate. However, given the design flexibility and reliability of this technology, there is no doubt that insulated metal substrates could trump those based on direct-bonded copper, as long as there is an increase in the thermal conductivity of the metal layer in contact with the SiC dies.

The Group's collaboration is able to draw on the expertise of Momentive Quartz Technologies, which, along with its legacy, has been an industry leader in thermal management in the aerospace, telecommunications and defence sectors for more than half a century. Within its portfolio, there is the: TC1050

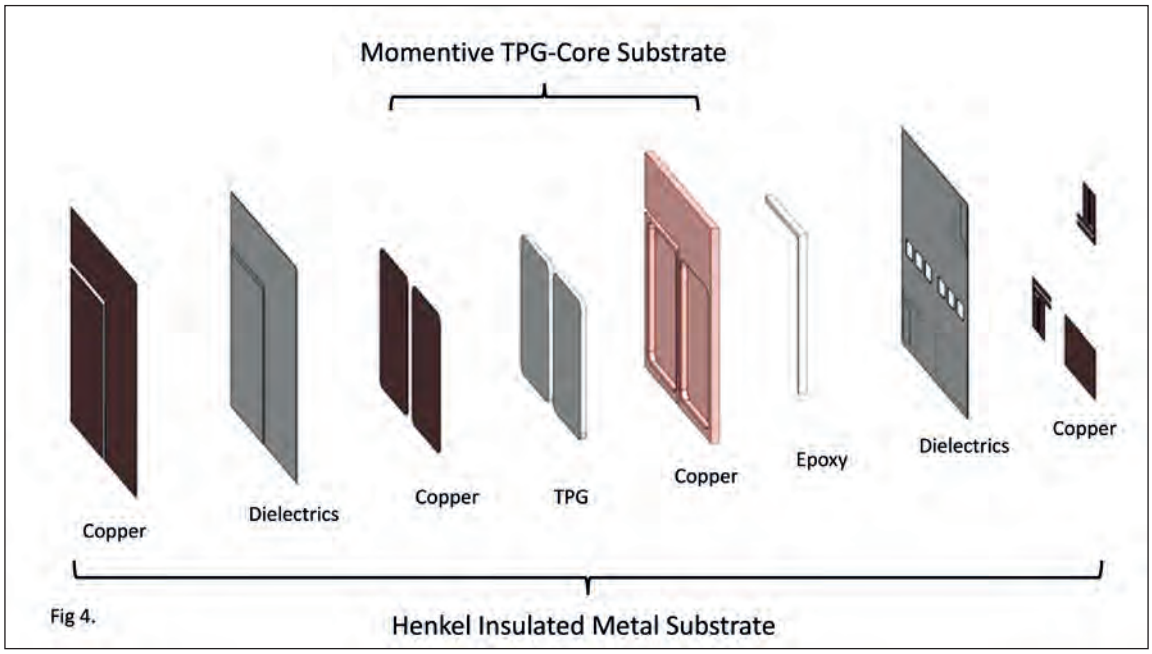


Figure 4. A seven-layer thermal pyrolytic graphite-core insulated metal substrate structure utilising proprietary materials and processing technologies from Momentive Quartz Technologies and Henkel.

heat spreader, deployed since the 1990s for board-level thermal management; the TMP-EX heat sink, introduced in 2011, that matches the coefficient of thermal expansion of the chip; and the TMP-FX thermal straps, which provide flexible heat conduction in tight spaces.

Glorious graphite

For all these products, the key ingredient is Momentive Quartz Technologies' thermal pyrolytic graphite, a material first produced in the 1960s when the current business was part of Union Carbide. This form of graphite, produced by CVD at over 2000 °C, is made up of millions of stacked layers that are highly oriented graphene planes. They equip the material with extremely high thermal conductivity (see Figure 2). Parallel to its basal plane, the thermal conductivity is 1650 W m^{-1} K^{-1} – four times the value of copper. Another merit of this material is that it is light weight. Its density is just 2.25 g/cm^3 for thermal pyrolytic graphite, which is one-fourth the density of copper.

Encapsulating a core of this form of graphite into a copper substrate enables a high thermal conductivity to be combined with a low mass. The Group was able to accomplish this by drawing on Momentive Quartz Technologies' proprietary bonding technology to ensure excellent thermal and mechanical joints between the graphite insert and the copper enclosure. The high quality of this bond is evident in the scanning electron microscopy and ultrasound c-scan images (see Figures 3 (b) and (c)). They reveal a hermetic, nearly void-free encapsulation.

One of the characteristics of the thermal pyrolytic graphite inserts is their anisotropic thermal conductivity. This allows the orientation and layout of the graphite within the copper enclosure to be tailored to the application. Measurements with a Netzsch Nanoflash 476 reveal a thermal conductivity of 760 W m^{-1} K^{-1} in a structure of thermal pyrolytic graphite sandwiched between copper. This conductivity is nearly double that of copper. At Momentive Quartz Technologies, researchers have subjected the metal-encapsulated graphite to a range of other tests, including thermal cycling and mechanical shock and vibration. This examination demonstrates the outstanding thermal performance and reliability of this hybrid structure.

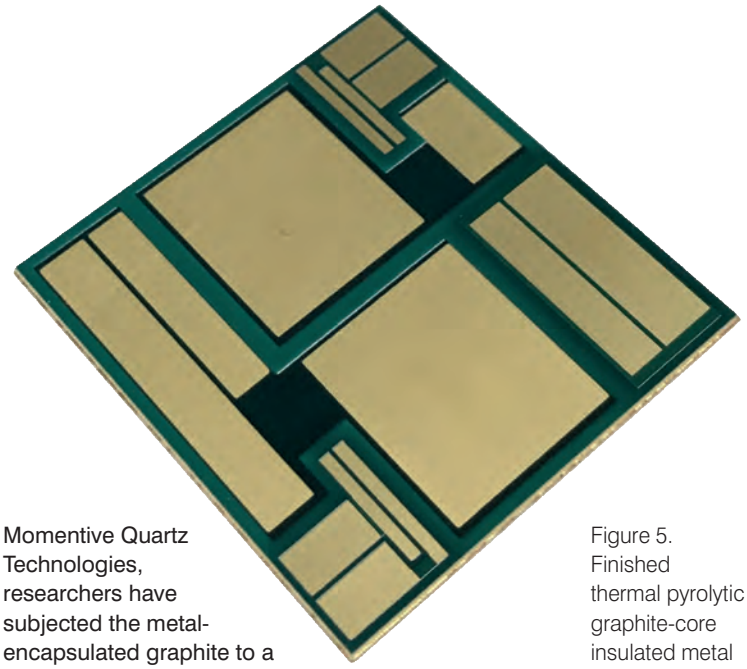


Figure 5. Finished thermal pyrolytic graphite-core insulated metal substrate with patterned copper circuit layers and dielectrics on both sides.

To ensure that this material technology can be used as a functional circuit for a SiC power module, collaborator Henkel Corporation deployed Momentive Quartz Technologies' graphite-core heat spreader in its insulated metal substrates. For more than two decades, Henkel has provided thermal-cladded insulated metal substrates to the power electronics and LED lighting industries. These substrates have proven to be particularly well suited to today's higher-watt-density and surface-mount applications, such as SiC power modules. Once the graphite is encapsulated inside the copper, it can be used directly in place of monolithic metal in Henkel's lamination process (see Figure 4). Note that the benefits of switching from a solid copper core to one

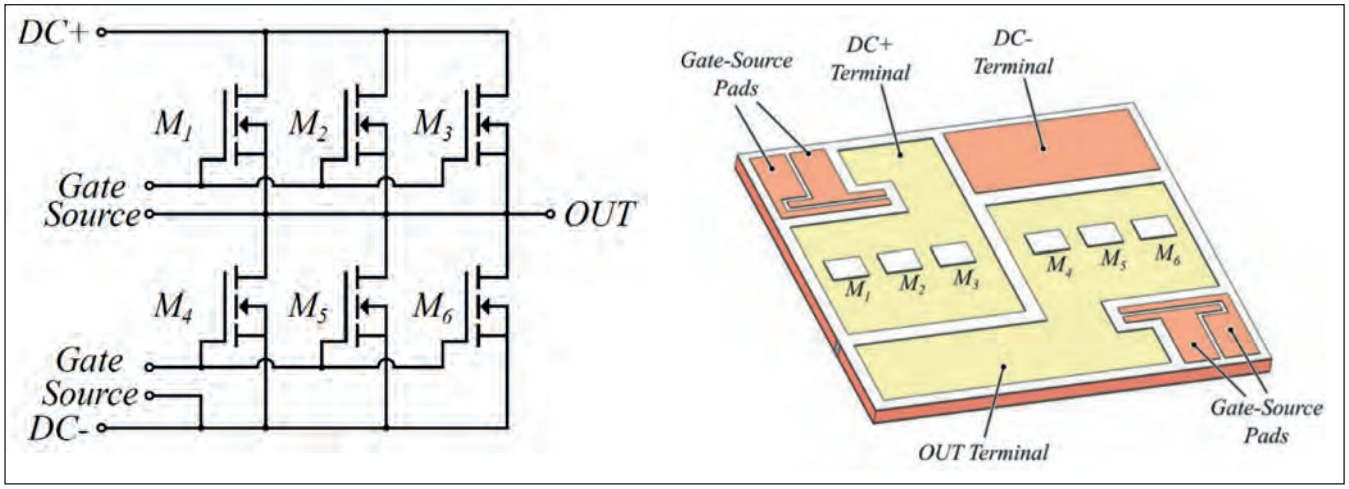


Figure 6. Electrical schematic of a half-bridge module (left) and insulated metal substrate circuit layout (right). More details are given in https://doi.org/10.1115/IPACK2019-6436

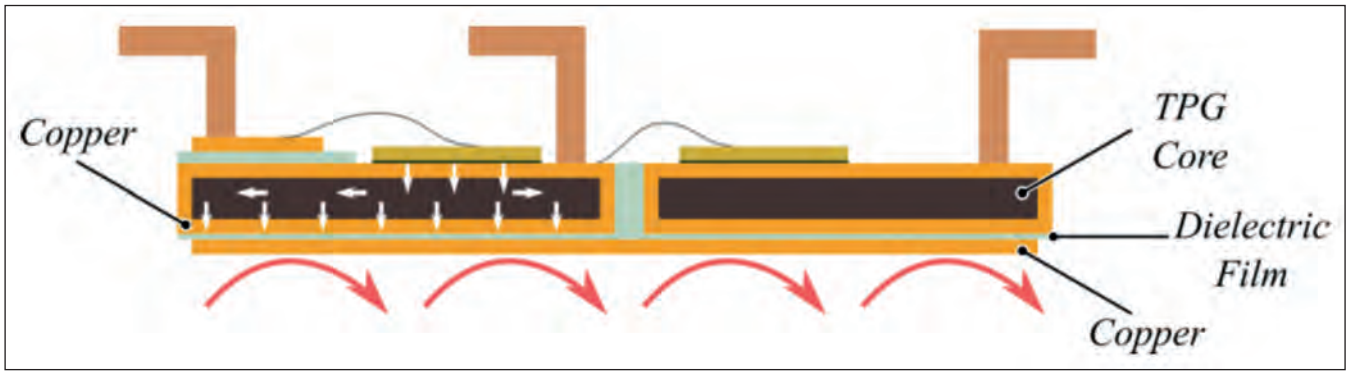


Figure 7. Conceptual module design using thermal pyrolytic graphite core to channel the waste heat away from the dies. More details are given in https://www.energy.gov/sites/prod/files/2019/06/f63/elt208_gurpinar_2019_o_4.9_3-41t.pdf

that contains graphite are not limited to an increase in thermal conductivity, as they also extend to a 30 percent weight reduction.

During the fabrication of the insulated metal substrates, technologists at Henkel uses a proprietary coating technology to apply dielectric layers to the graphite-core substrate plane and the copper foil layers (see Figure 5). Adding these dielectric layers is critical to meeting the breakdown voltage requirements. Engineers at Henkel can also include features such as non-conductive, epoxy-filled grooves that provide electrical isolation between poles.

Proven credentials

To demonstrate the power of this approach, the Group constructed a testing platform, a common half-bridge SiC MOSFET inverter module (see Figure 6). In this design, Momentive Quartz Technologies' graphite inserts were positioned directly under the SiC dies. With this arrangement, waste heat was extracted through the thickness, towards the terminals, where it could transfer to Henkel's thermally conductive dielectric layers (see Figure 7). In addition to reducing the thermal resistance of the copper substrate, the heat spreading provided by the thermal pyrolytic graphite increased the effective contact area of the dielectric layer, and thus its heat conductance. According to modelling by those on our team at ORNL, there was an immediate improvement in temperature uniformity for the insulated metal substrate with the thermal pyrolytic graphite core, associated with the higher in-plane heat conduction of this form of graphite (see Figure 8).

An additional insight provided by the thermal analysis was a significant reduction in junction temperature – it is 11 °C cooler in both steady and cycling states. As a result of this, 15 percent more power can be generated by the SiC power module for the same temperature as a standard insulated metal substrate. Yet another demonstrated advantage of using graphite is the reduction in the difference in the junction temperature when the power is on versus when it is off (see Figure 9).

To validate their modelling, the scientists at ORNL conducted bench-top measurements to compare the performance of SiC power modules of insulated metal substrates with copper cores and thermal pyrolytic graphite cores (see table 1). Preliminary measurement of the assembled power modules confirmed the earlier

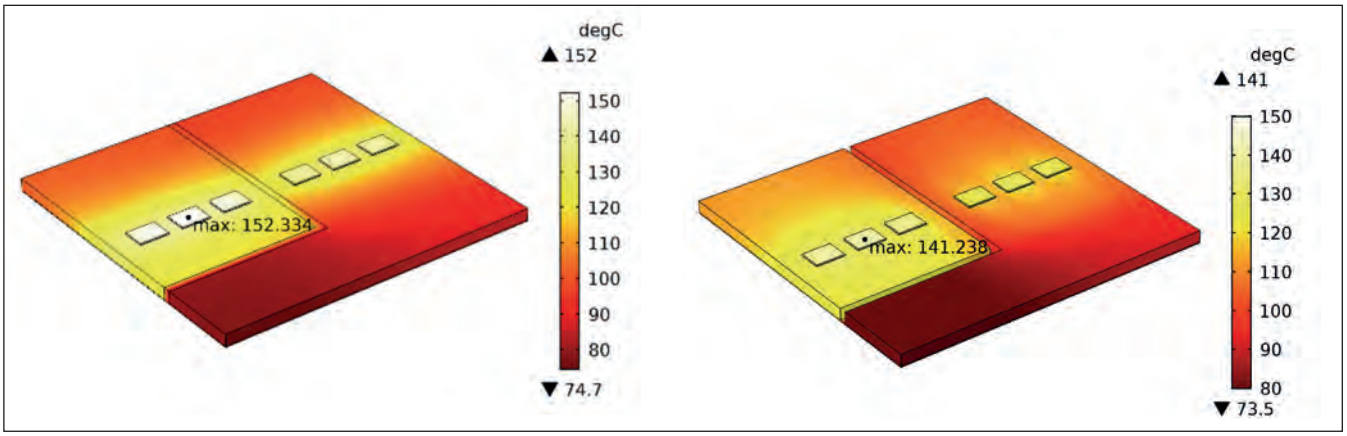


Figure 8. Thermal analysis of a SiC module using insulated metal substrates with a copper-core (left) and thermal pyrolytic graphite core (right). The results demonstrate the improvement in heat spreading by the two thermal pyrolytic graphite cores. More details are given in https://www.energy.gov/sites/prod/files/2019/06/f63/elt208_gurpinar_2019_o_4.9_3-41t.pdf

modelling results. The testing is on-going, with those at ORNL assessing the final package performance, durability and reliability of insulated metal substrates with thermal pyrolytic graphite cores (see Figure 10).

The efforts of this collaboration showcased the merits of using thermal pyrolytic graphite cores in insulated metal substrates. Compared to conventional copper cores, the switch to this form of graphite effectively doubled thermal conductivity, while trimming weight by almost one third. This solution, with demonstrated manufacturability, can also enable an increase in heat load, improved reliability, simplified module design and a reduction in both assembly costs and the number of steps. By orienting the graphite within the copper core, heat conduction can be optimised for die size, location, circuit pattern and power loading.

The technology could also enable more sophisticated multi-layer power board designs that address thermal, electrical and weight issues simultaneously. Working under the support of the Department of Energy, the Group is playing its part in working toward this goal as a continued effort to refine its technology, so that it can unleash the potential of SiC devices and push their implementation in electric drive systems.

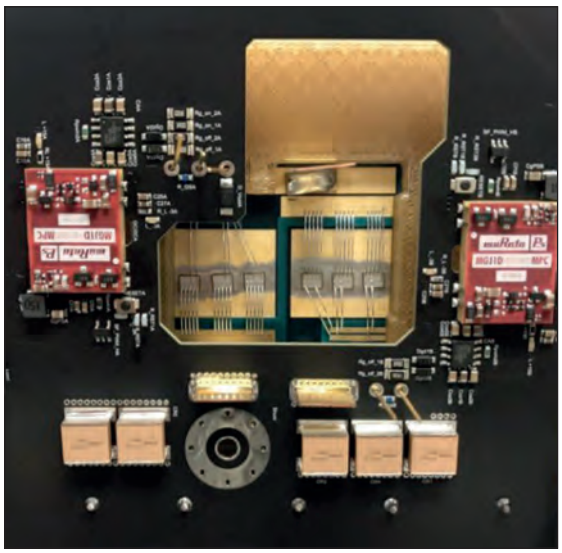


Figure 10. Assembled SiC power module using a thermal pyrolytic graphite-core insulated metal substrate.

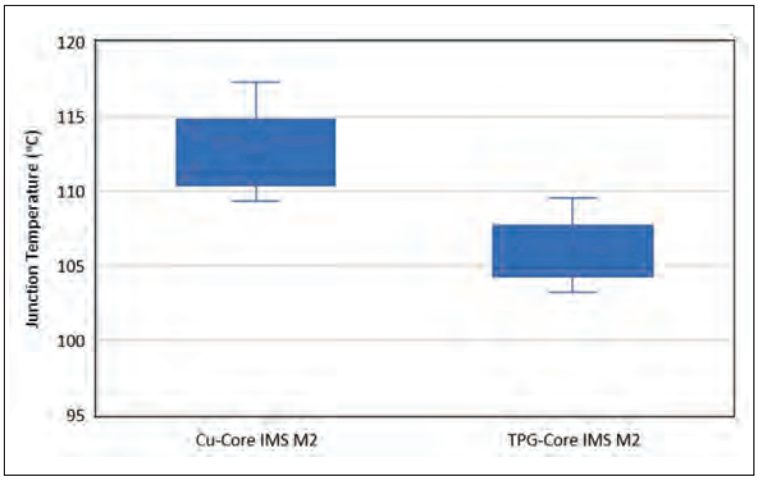


Figure 9. Plotting the SiC MOSFET junction temperature during power cycling revealed a 1.8 °C reduction in temperature range using the thermal pyrolytic graphite-core insulated metal substrate.

Further reading

W. Fan *et al*. "Improving Heat Conduction of Insulated Metal Substrate with Thermal Pyrolytic Graphite Core for SiC Power Module", Materials Science Forum (2020)

US Department of Energy, Office of Energy Efficiency and Renewable Energy, "U.S. Drive Electrical and Electronics Technical Team Roadmap," https://www.energy.gov/eere/vehicles/plans-and-roadmaps, October 2017

W. Fan *et al* International Symposium on Microelectronics 2014 (1) (2014) 433

A. W. Moore *et al* Mathematical and Physical Sciences **280** 153 (1964)

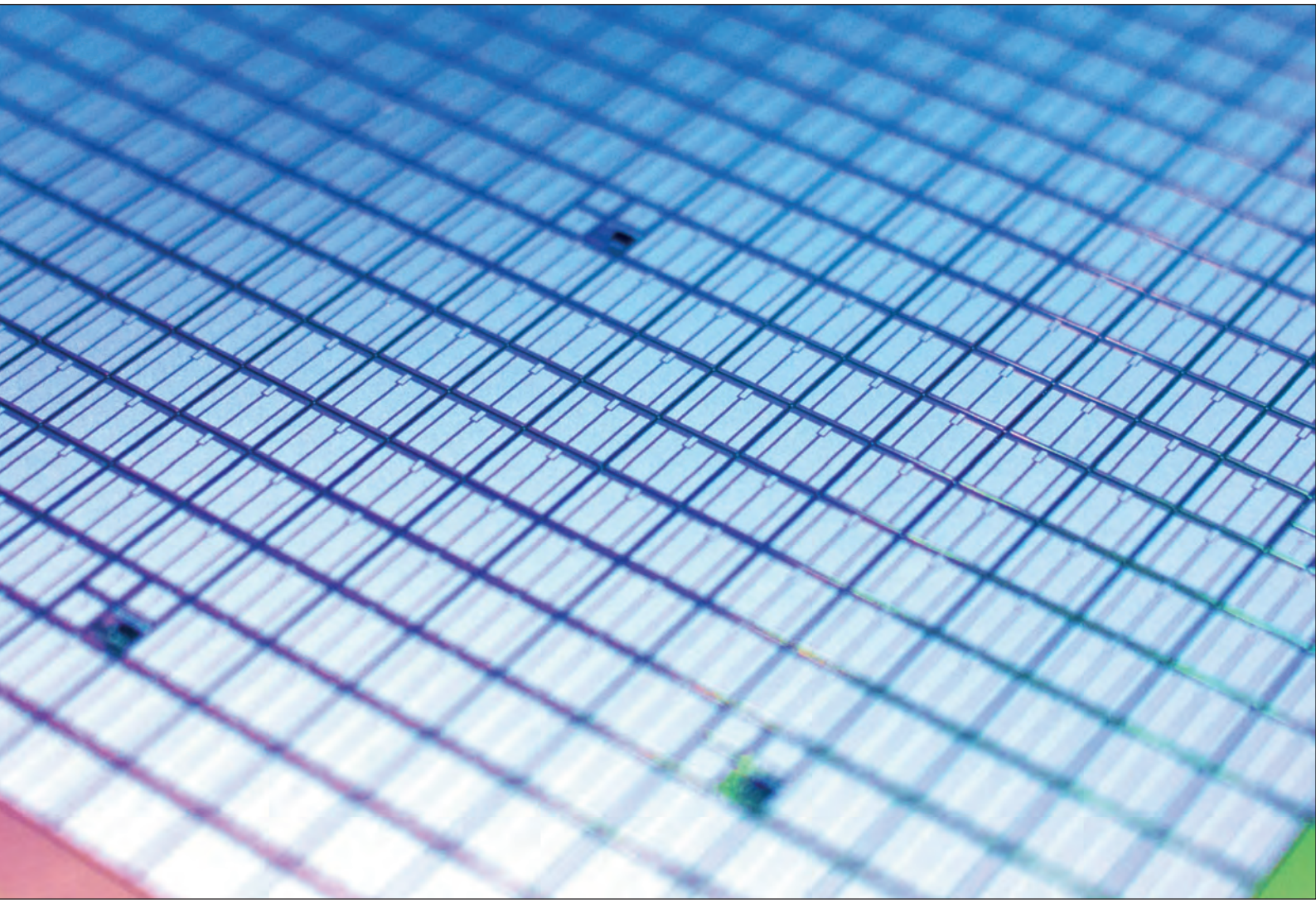
W. Fan *et al*. RF & Microwave Microelectronics Packaging II, (Springer International Publishing 2017) pp. 129

E. Gurpinar *et al*. Proceedings of the ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, V001T06A013. ASME. https://doi.org/10.1115/IPACK2019-6436

Highly Integrated Power Module, DOE VTO Annual Merit Review Meeting https://www.energy.gov/sites/prod/files/2019/06/f63/elt208_gurpinar_2019_o_4.9_3-41t.pdf

	Thermal Conductivity [W/m-K]			Junction Temperature T_{max}		Junction Temperature Variation
	x	y	z	@ steady state	@ power cycle	@ power cycle
Cu-core IMS	395	395	395	152°C	113°C	8.6°C
TPG-core IMS	1155	130	760*	141°C	104°C	6.8°C

Table 1. Thermal performance comparison of insulated metal substrates with a copper core and a thermal pyrolytic graphite core. * Measured value using Nanoflash method.



A better face for the SiC MOSFET

SiC MOSFETs with a V-grooved trench reduce on-resistance and trim switching losses

BY KOSUKE UCHIDA AND TAKASHI TSUNO FROM SUMITOMO ELECTRIC INDUSTRIES

WHEN THE LEADERS of the most powerful countries met at the World Economic Forum in January, one topic dominated the agenda – climate change. For many of them, this is by far the biggest issue of our age, with action needed right now to cut carbon footprints.

There are so many opportunities to do this. Some are at the national level, such increasing the number of nuclear power plants and solar farms. There are also changes that companies can make, such as investing is more efficient machinery, and there are personal decisions, such as moving to a more plant-based diet and taking fewer flights.

Within this mix, one of the options for saving energy and curbing carbon dioxide emissions is the introduction of more efficient power control technologies. They are widely deployed, playing an

essential role in electric vehicles, in renewable energy systems, and in industrial motor drives.

Most of today's power devices are made from silicon. Their performance has improved over many decades, but they are now encroaching theoretical limits, calculated from their physical properties. This means that it is no longer possible to make significant reductions in power loss, which comes from conduction and switching losses.

What's needed is to replace silicon devices with those made from wide bandgap materials, such as SiC and GaN. This pair attract much attention because they have the upper hand over silicon on many fronts, including a higher dielectric breakdown electric field, a superior electron saturation velocity, and a greater thermal conductivity. Thanks to these characteristics, SiC and GaN provide a higher breakdown voltage and a reduced on-resistance, leading to lower conduction losses.

A noteworthy difference between SiC and GaN is the quality of the crystal. Bulk SiC has fewer crystal defects, enabling the manufacture of high-quality SiC epitaxial substrates, and in turn the production of vertical SiC power devices. These devices, which use the whole surface of the epitaxial layer, combine a high current with a breakdown voltage of 600 V or more. Due to this, SiC is expected to have its greatest success in high-voltage applications that achieve high power, while GaN is expected to be used in low output power applications.

SiC devices will displace the silicon insulated-gate bipolar transistor (IGBT), which combines a high breakdown voltage with a low resistance. Due to this device's bipolar operation, switching losses increase with the electron-hole recombination time. That's not the case with the SiC MOSFET, a unipolar device that provides high-speed switching and a higher breakdown voltage.

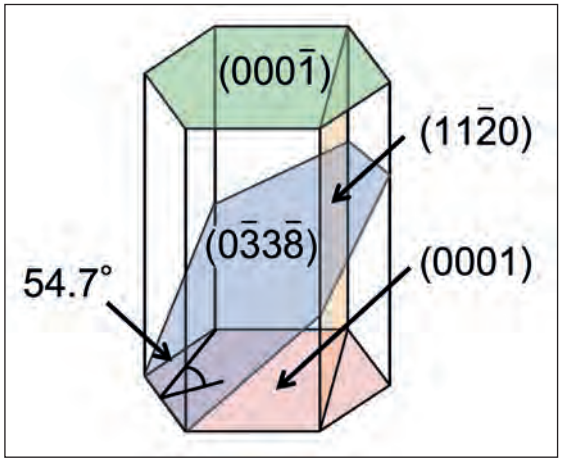


Figure 1. Major crystal faces in 4H-SiC. The (03$\bar{3}$8) face is located at an off-angle of 54.7 degrees from the (0001) face.

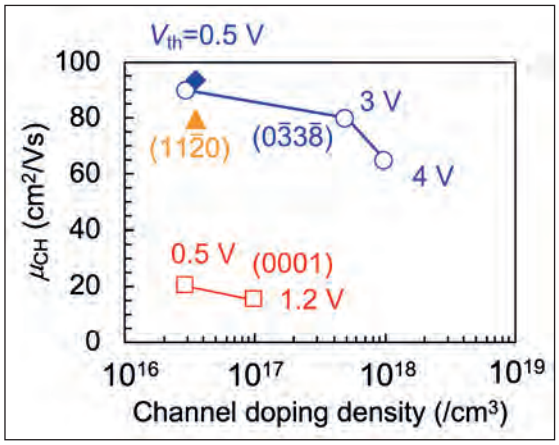


Figure 2. The doping density dependence of channel mobility of SiC lateral MOSFETs. The (03$\bar{3}$8) face shows a higher channel mobility and a higher threshold voltage than other crystal faces.

A great groove

At Sumitomo Electric Industries Ltd., Japan, we have developed a new architecture for the SiC MOSFET. It features V-groove trenches, enabling us to exploit a face with a higher mobility.

This development is able to draw on our vast experience surrounding the production of compound semiconductor products, which include GaN HEMTs, GaAs FETs and the substrates that form their foundation. More recently, we have been developing SiC crystals, and have gone on to start mass production of 6-inch SiC epitaxial substrates, which we refer to as EpiEra. They are produced using a high-quality, cost-effective growth technology – we have named this our multi-parameter and zone-controlled SiC growth technology. We use a unique simulation technique to determine the most appropriate doping concentration uniformity for realising the intended device performance and yield. Through vertical integration of our SiC material and device technologies, we produce SiC MOSFETs with a high performance and a high yield.

We have developed our novel MOSFET architecture because the channel mobility in conventional designs is substantially lower than the bulk mobility, due to a high interface state density. To demonstrate what can be achieved, we fabricated a lateral MOSFET on 4H-SiC(03$\bar{3}$8) face, which is located at an off-angle of 54.7 degrees from the (0001) face (see Figure 1).

Our results show that this is the best face for making SiC MOSFETs, because the channel mobility is highest for all doping concentrations, due to a lower interface state density and a higher free-electron ratio (see Figure 2). When employing a doping concentration of 10^{18}/cm³, a high channel mobility of 60 cm² V^{-1} s^{-1} is realised alongside a threshold voltage that is as high as 4 V – this is high enough to suppress erroneous ignition at high temperatures.

To exploit the benefits of this face, over the last few years we have developed and commercialised the 4H-SiC V-groove trench MOSFET, a device we refer to as a VMOSFET. Recently, efforts have been

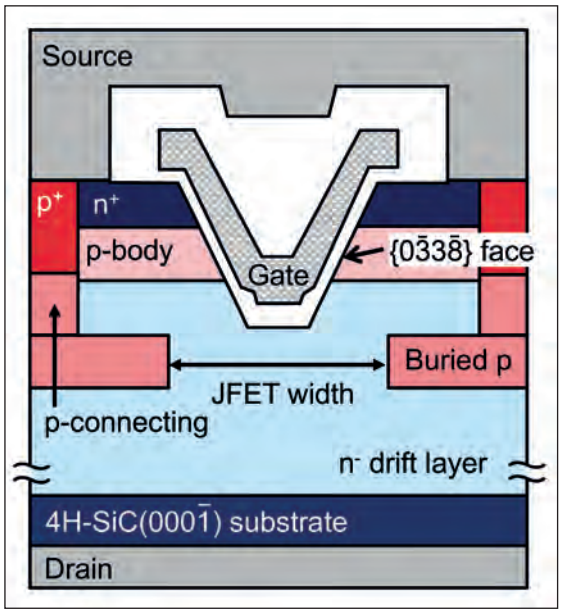


Figure 3. A cross-sectional view of a SiC VMOSFET.

directed at high power conversion efficiency, so that the devices can handle hundreds of amps and have a breakdown voltage above 1 kV. These transistors feature 4H-SiC{0338} trench side walls that have a higher channel mobility than other SiC crystal faces (see Figure 3 for a diagram of this structure). Using this design, channel resistance can be reduced while realising a high channel density.

The key to producing this device is the use of a chemical etching process to form the V-groove trenches. We use silicon dioxide as the etching mask, with etching undertaken at around 900 °C in a chlorine ambient. During this process, chlorine produces a chemical change in the surface, with SiC converted to carbon, which then reacts with oxygen. The resultant silicon chloride and carbon dioxide vaporizes at a high temperature (see Figure 4).

This process exposes {0338} faces, which are extremely stable. Note that with a conventional process to form U-shaped trenches, such as reactive-ion etching, this would lead to etching damage and the formation of sub-trenches. The high-quality of the faces

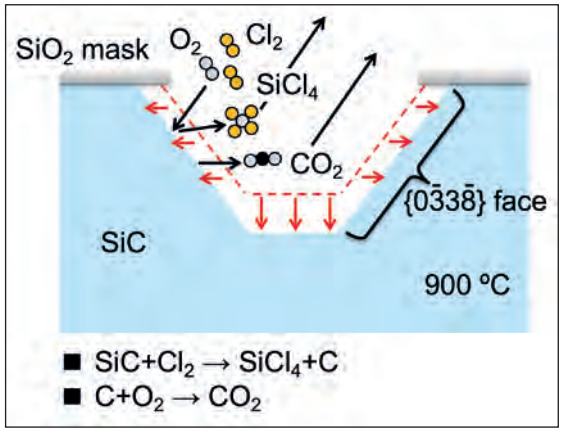


Figure 4. Chlorine etching creates the V-grooves of the MOSFET.

produced by our process can be seen in the images of a scanning electron microscope (see Figure 5).

A shortcoming of the trench structure is that the gate oxide film that forms on the bottom of the trench breaks easily when a high voltage is applied to the device. When this happens, the electric field concentrates on the gate oxide film. To address this and enhance the reliability of the VMOSFET, we implant *p*-type electric-field-alleviating regions around the groove bottom. With this addition, the application of a high voltage to the drain electrode causes the electric field to concentrate on the buried *p*-region edge. Making this modification alleviates the electric field on the gate oxide film.

With this design, we are able to increase the switching speed and reduce switching loss by reducing the parasitic capacitance between the gate and drain electrodes. This is accomplished by creating a source potential, by electrically connecting the buried *p*-regions to the source electrode with *p*-connecting regions.

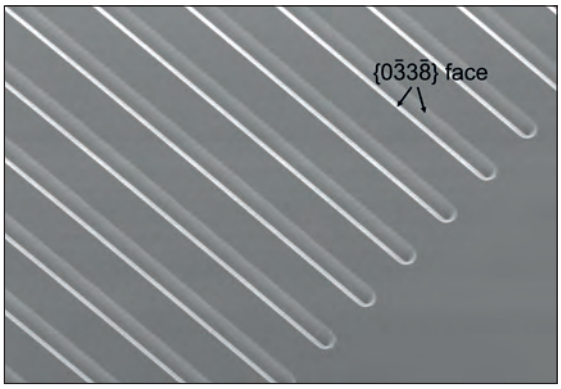


Figure 5. Scanning electron microscopy (SEM) image of a V-groove.

Proven reliability

To ensure a low on-resistance, and a low oxide electric field that leads to long-term reliability, it is crucial to optimise the JFET width and the width between the buried *p*-regions. Our efforts related to this include our investigation of the relationship between the oxide electric field and the lifetime under a drain bias condition.

An estimate of the lifetime under a high-temperature reverse-bias condition has been obtained with test dies that have a dedicated structure. To increase the oxide electric field, dies with a V-groove gate trench structure have a large JFET width compared with the VMOSFETs designed for mass production. These tests have been conducted at an ambient temperature of 175 °C. The oxide electric field in these transistors has been calculated using Technology CAD simulation. Calculations of the electric field distribution reveal that the oxide electric field is highest on the bottom oxide edge, due to electric field crowding (see Figure 6).

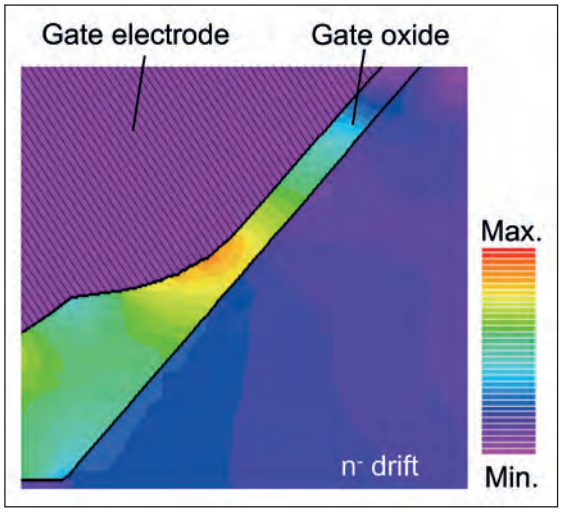


Figure 6. Electric field distribution around the V-groove trench bottom calculated by technology CAD for a lifetime estimation.

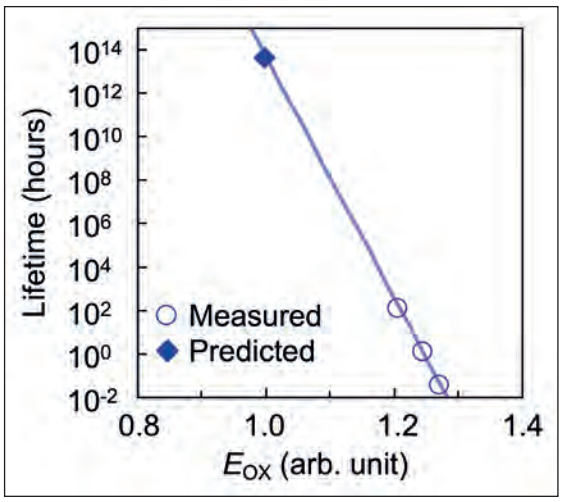


Figure 7. Long-term lifetime of VMOSFETs. Lifetime is estimated under a drain bias condition at T_a = 175 °C in the case of a 10 percent cumulative failure rate. The predicted lifetime is equal to 200 years under a 0.1 ppm cumulative failure-rate condition.

After we carried out the high-temperature reverse-bias tests, we analysed the damaged point of the VMOSFETs. We found that its location corresponded to our simulation's highest point for the oxide electric field.

Using these measurements, we have determined the impact of the oxide electric field on the lifetime. A plot for a 10 percent cumulative failure rate is shown in Figure 7.

For high-reliability applications, our target lifetime is more than 20 years for a 0.1 parts-per-million cumulative failure rate. We exceed this by a significant margin. For an oxide electric field of 1.0 – note that this is an arbitrary unit – the predicted lifetime is 4.5 x 10^{13} hours. That equates to a lifetime of 200 years under a 0.1 ppm cumulative failure rate condition, according to our calculations that relate the lifetime to the cumulative failure rate.

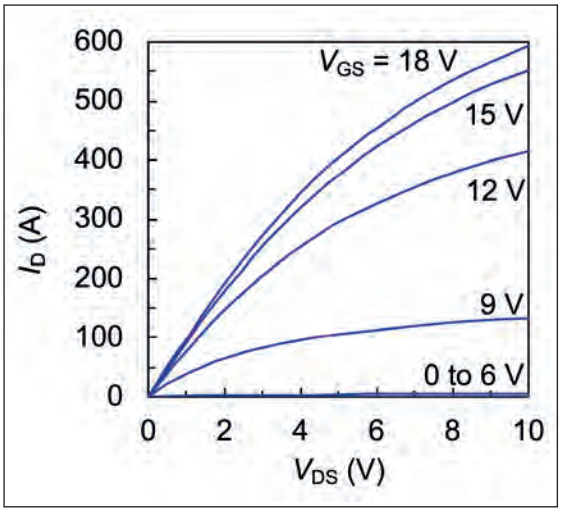


Figure 8. I_D-V_{DS} characteristics (V_{GS} = 0 – 18 V) at T_j = 25 °C. The VMOSFETs exhibit a high current capability of 200 A DC and 600 A pulse.

Drawing on the high-temperature reverse-bias tests, we used simulations to design a structure that has a low on-resistance and an oxide electric field of 1.0 at a drain bias of 1200 V. This led us to fabricate VMOSFETs with an optimised design on a 150 mm wafer. Operating at a junction temperature of 25 °C, the resultant 6.0-mm-square die can handle a DC current of 200 A and pulses up to 600 A (see Figure 8). The specific on-resistance is just 3.1 mΩ cm^2 for a gate-source voltage of 15 V and a drain-source voltage of 1 V; and at 25 °C, the threshold voltage is 4.6 V, for a drain-source voltage equal to the gate-source voltage, and a drain current density of 1 mA/mm^2.

The breakdown voltage is well above the target, capable of withstanding up to 1640 V (see Figure 9). Another encouraging attribute is the small gate-to-drain capacitance – it is just 15 pF at a drain-source voltage of 800 V – enabling effective suppression of

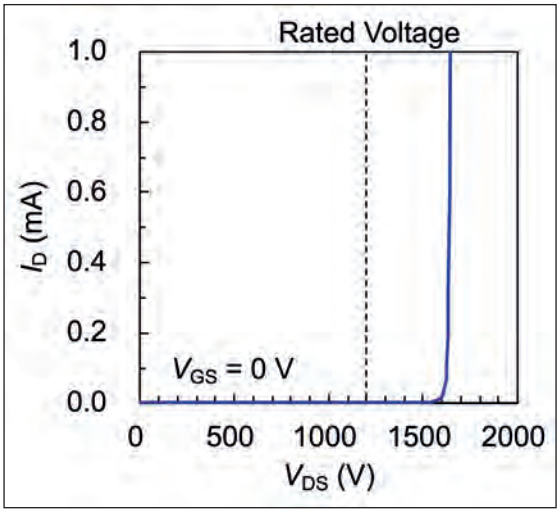


Figure 9. Blocking characteristics. The VMOSFETs show an adequate margin against a rated blocking voltage of 1200 V.

Table 1. Sumitomo Electric Industries' line-up of VMOSFET products.

Current Range		<10A	30A	100A	≦200A	≦400A	≦600A
Discrete	600-900V	✓	✓	✓			
	1,200V	Now	Now	Now			
	1,700V	Now	Now	Now			
Module	1,200V				Now	Now	✓
	1,700V				Now	Now	
	3,300V					✓	

Available Now | Coming Soon

Discrete
- TO-247-3L
- TO-247-4L
- TO-3PF

Various packages upon requests

Module
- Si compatible Package
- Custom Package

self-turn-on, due to the grounded buried *p*-regions that effectively block lines of electric force from the drain electrode.

We have also performed a double pulse test with an inductive load, using a SiC Schottky barrier diode for the free-wheel device (see Figure 10 for details). This test highlights our VMOSFETs fast switching speed and low switching loss. Rise and fall times are 16 ns and 7 ns, respectively; and turn-on and turn-off energy loss are just 260 μJ and 270 μJ, making the total switching loss only 530 μJ.

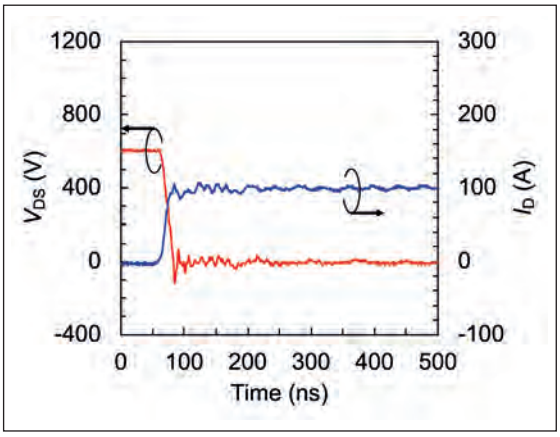


Figure 10. Fast switching characteristics of VMOSFETs under double pulse test. Conditions for this test are: R_G = 1.0 Ω, V_{GS} = +15/-5 V, V_{DD} = 600 V, I_D = 100 A, L = 100 μH.

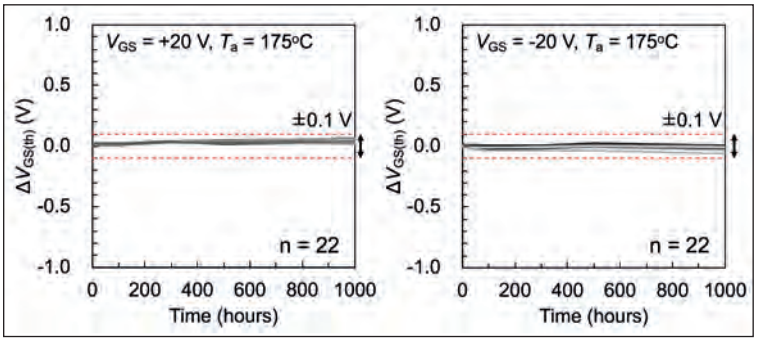


Figure 11. Stable threshold voltage of a VMOSFET under a high temperature gate bias test of V_{GS} = +20 V (left) and -20 V (right) at T_a = 175 °C.

Further testing involved evaluating the threshold voltage stability of our VMOSFETs. Evaluation of 22 samples at 175 °C revealed threshold voltage shifts of less than 0.1 V after a 1000 hour high-temperature gate-bias test. This small shift is evidence of the stability and high quality of the gate oxide on {0$\bar{3}\bar{3}$8} crystal faces.

Our successful development of our 1200 V / 200 A VMOSFET has enabled us to expand our line-up for this class of transistor (see Table 1). From a user's perspective, the adoption of VMOSFETs allows: better performance at both the component and system level; greater capability in designing far smaller components; and a stable supply chain and better quality management. We anticipate that the superior characteristics of our VMOSFETs, which combine low power loss and high reliability, will underpin further expansion in the SiC market.

A part of this R&D was carried out as one of the Super clean room Power Electronics Line (SPEL) joint research consortium activities hosted by the National Institute of Advanced Industrial Science and Technology.

Further reading

K. Wada *et al.* Mater. Sci. Forum **105-108** 963 (2019)
T. Hiyoshi *et al.* Mater. Sci. Forum **740-742** 506-509 (2013)
T. Hatakeyama *et al.* Appl. Phys. Express **12** 021003 (2019)

semi

Registration is Now Open

SEMICON® WEST 50 YEARS

JULY 20-23, 2020
VIRTUAL EVENT

Yes, you heard it right, SEMICON West 2020 is going virtual!

Join us online for LIVE and On-Demand programs from the comfort of your home or work office using any mode of connection through your laptop, desktop, tablet, or mobile device. You'll have four days of programs on electronics manufacturing and design topics presented by experts and driven by technology and innovation.

Accessible On-Demand 24/7 through Sept. 20

EXPERIENCE LIVE KEYNOTES

- **Al Gore**, Former United States Vice President
- **Gary Dickerson**, Applied Materials
- **John E. Kelly III**, IBM
- **Tetsuro Higashi**, Tokyo Electron
- **Steve Brown**, The Innovation Ultimatum
- **Lea Gabrielle**, Global Engagement Center U.S. State Department
- Plus many more

PROGRAMS

- Bulls & Bears
- SEMI Market Symposium
- Test Vision Symposium
- imec
- SOI Industry Consortium
- Southeast Asia Pavilion
- Diversity & Inclusion
- TechTALKS
- SMART Pavilions

PLATINUM SPONSORS

APPLIED MATERIALS make possible · Deloitte. · KLA · Lam RESEARCH · TEL · ThermoFisher SCIENTIFIC

GOLD SPONSORS

ADVANTEST · EDWARDS

Get your All-In Pass for access to all the LIVE and On-Demand program content and more!

#SEMICONWest

@SEMIAmericas

www.SEMICONWest.org

A different kind of GaN

UK start-up, Porotech, is set to commercialise porous GaN, opening the door to high-performance optoelectronic devices with unexpected properties, reports Rebecca Pool.

A RELATIVELY UNKNOWN MATERIAL from a newly minted UK start-up is set to make waves in the rapidly growing GaN market.

With a host of novel properties that open the door to high-performance optoelectronic devices, 'porous GaN' is attracting more and more interest in compound semiconductor circles. And thanks to £1.5 million in investment funds, University of Cambridge spin-off, Poro Technologies – or Porotech – is on course to be one of the first companies to bring this mesoporous version of GaN to market.

Seed round investment is being used to develop a pilot plant in Cambridge, UK, and Porotech's first products.

Porous GaN can be regarded as a semiconductor composite of solid GaN and air. As Rachel Oliver, Co-founder and Chief Scientific Officer of Porotech, and Director of the Cambridge Centre for Gallium Nitride puts it: "Porous GaN is basically GaN with holes in it that are a few tens of nanometres across."

"With porous GaN we can engineer a wide range of material properties... and offer a new material platform to build semiconductor devices on," she adds.

The Porotech team creates the nanoscale porosity in GaN wafers using electrochemical etching. The etch is conductivity selective and responds differently to the material depending on its doping density. Porosity is created in doped layers while undoped layers are left undamaged, allowing complex three-dimensional nanostructures to be created.

According to Oliver, the etchant flows to and from the doped layers via the many nanometre-scale channel-like defects – dislocations – that exist within any GaN wafer.

"Even your best quality GaN wafer will still have around 10^5 dislocations per square centimetre," she explains. "So the etchant will flow down a dislocation and when it hits the doped layer will etch it very quickly to create the porosity before continuing down that channel to the next doped layer."

"We can take an entire wafer, and using this conductivity selective etching mechanism, create GaN [structures] with a whole new set of properties that haven't been available before," she adds. "It's very cool from a commercial perspective."

Indeed, both Oliver and Porotech chief executive and co-founder Tongtong Zhu are certain their porous GaN fabrication process lends itself to commercial exploitation. The method has been tried and tested for wafers up to eight inches in diameter and Zhu reckons it will seamlessly scale to even larger wafer sizes.

"The first thing that inspired us to pursue this process commercially is that it works with wafers," says Zhu. "What's more, during the process we preserve the surface quality and the integrity of the materials so anyone can take the porous GaN wafer and insert it into their production processes without any disruption."

Devices to go

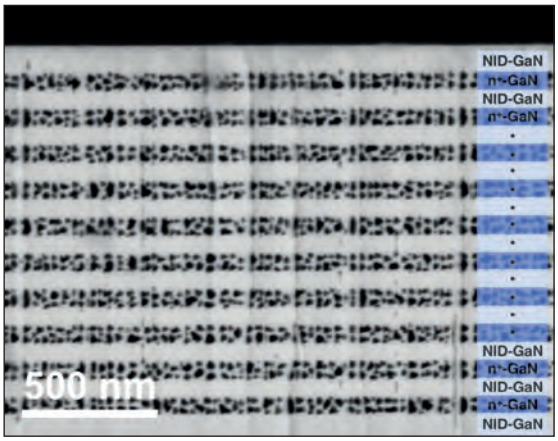
Oliver, Zhu and colleagues have already fabricated several components and device prototypes. They have demonstrated highly reflective Distributed Bragg Reflectors (DBRs) – or 'Poro Mirrors' – based on wafers comprising alternating layers of solid and nanoporous GaN. InGaN LEDs were then grown on these epi-ready DBR pseudo-substrates that were some 25 percent more energy efficient than standard LEDs.

"This DBR substrate is fully compatible with GaN so a customer doesn't need to process anything differently during LED fabrication, but can still get a brighter and more efficient LED," points out Zhu.

Porotech has also joined forces with other institutions and start-ups to fabricate thermal sensors that use porous GaN layers as on-chip thermal insulation. And in a novel technology twist, the team has filled the pores in a porous GaN wafer with a halide perovskite to create an optoelectronic material with longer-lasting luminescence.

"These luminescent perovskites are useful in solar cells and LEDs but degrade very quickly," says Oliver. "We can slow this degradation down with porous GaN."

Excitingly, novel porous GaN devices could be reaching commercial markets sooner rather than later. Despite the coronavirus pandemic, the Porotech pilot plant is currently being built at Cambridge, and Oliver, Zhu and colleagues are transferring production process from the laboratory to the plant.

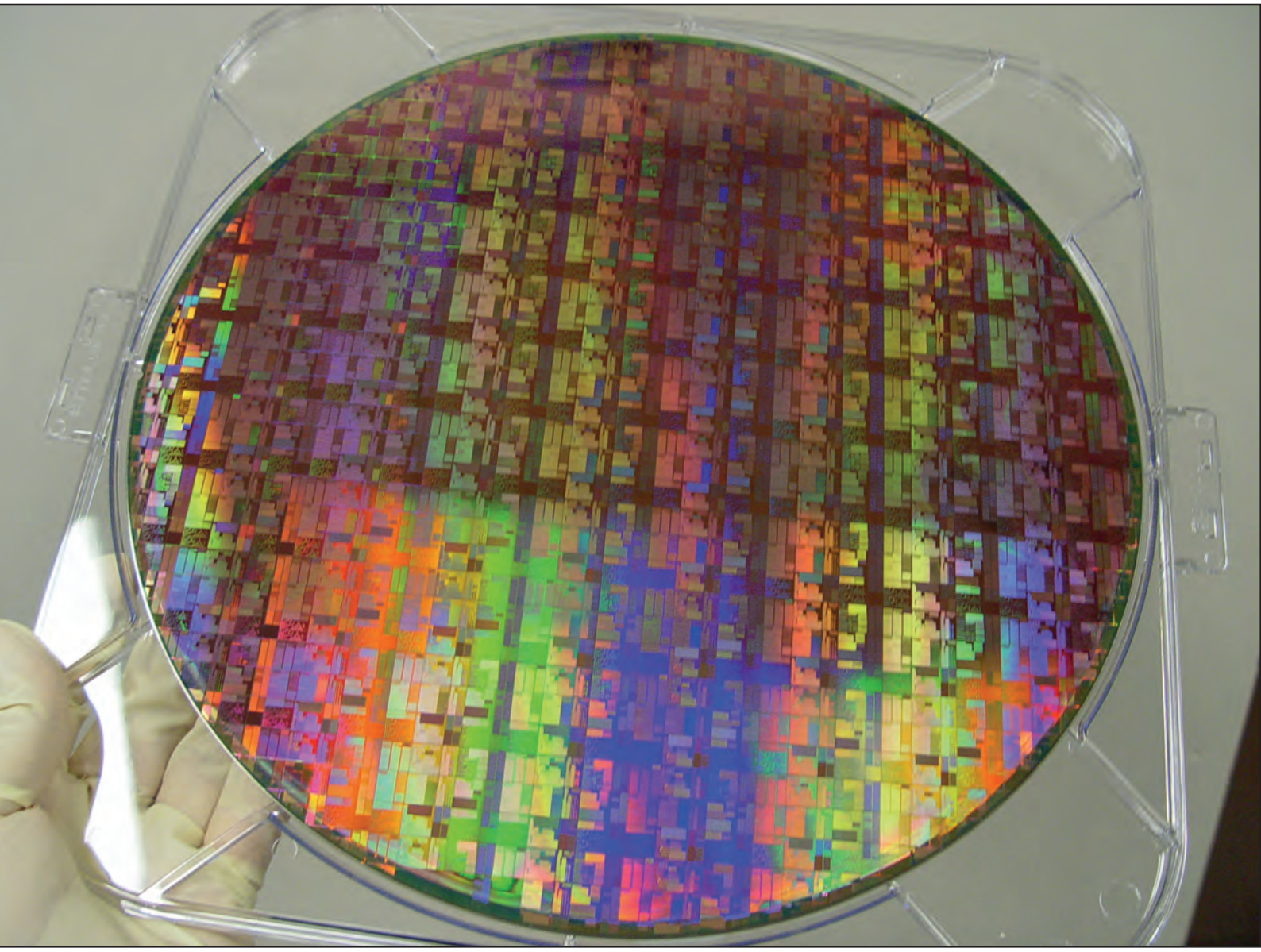


Electrochemical etching provides nanoscale porosity

"The plant will be operational before June this year and we're going to start with small-scale production to show that our wafers can be produced in volume," says Zhu. "We're currently preparing tens of wafers for customer trials and eventually intend to demonstrate that we can produce thousands of wafers a year."

The company is also working with foundry services, wafer producers and integrated device manufacturers, and hopes to license out technology in the coming years. "We've been working to get the company off the ground for several years and we aren't going to stop now," says Oliver. "There has been no other time when GaN is rising so quickly and we have to keep up our momentum."

Poro Technologies co-founders (left to right): Tongtong Zhu (CEO), Rachel Oliver (CSO), Yingjun Liu (CTO)



Stacking GaN and silicon transistors on 300 mm silicon

Next-generation mobile devices, data infrastructure and communication networks could be aided by three-dimensional, monolithic integration of GaN and silicon CMOS on 300 mm wafers

BY HAN WUI THEN FROM INTEL CORPORATION

THE TRANSITION to 5G and beyond is tipped to drive an exponential increase in the number of connected mobile devices. The integrated circuits that power them will need to provide greater energy efficiency, in a smaller form factor. Consequetly, there is much demand for more capable transistors and the integration of ever-larger numbers of components on the microchip.

Fulfilling these requirements is far from easy, as none of today's transistor technologies are capable of meeting the diverse needs associated with power delivery and RF front-end design. Due to this issue, circuit designers are combining many distinct, separate chips. This is not great, as it results in a bulky package.

To tackle this problem, our team at Intel's Components Research division in the Technology Development Group of Oregon has developed the first monolithic, three-dimensional GaN and silicon transistor stacking technology. It delivers best-in-class performance and efficiency, while allowing diverse functionalities to be integrated on a single chip.

Combining silicon and GaN is an attractive proposition. Silicon is today's workhorse for power electronics and RF switches, but it struggles to deliver high-frequency, high-power performance, so it is not a good choice for RF power amplification (see Figure 1). For that particular task, GaAs HBTs, GaAs HEMTs and GaN HEMTs are the front runners. However, these technologies are not ideal for making efficient power electronics: depletion mode GaAs HEMTs and GaN HEMTs are not favoured, due to their always-on nature; and the GaAs HBT is unsuitable, being current-driven rather than field-driven.

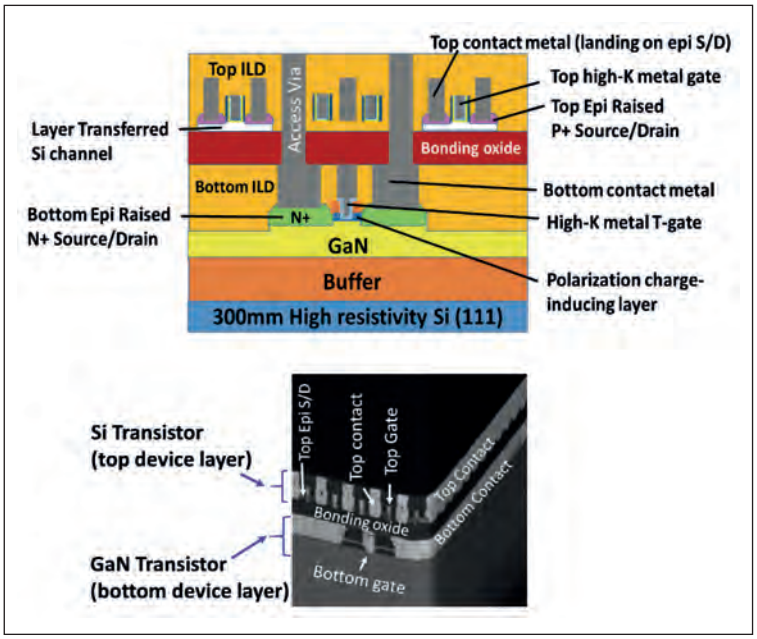


Figure 2. Intel has produced the first GaN transistors on a 300 mm silicon (111) wafer in one of its leading CMOS fabs. Its researchers have employed a new technique of three-dimensional monolithic integration by layer transfer to stack silicon PMOS transistors on top of GaN NMOS transistors to enable CMOS functionalities, for the first time in industry.

Fortunately, there is a transistor that excels on all fronts: the enhancement-mode (e-mode) GaN transistor. Recently, we have shown that when this class of device is equipped with high-κ dielectric metal gate technology, it can deliver best-in-class performance, in both power delivery and RF front-end functionalities. We have built on this success by using three-dimensional monolithic integration to unite GaN power and RF transistor technology with silicon

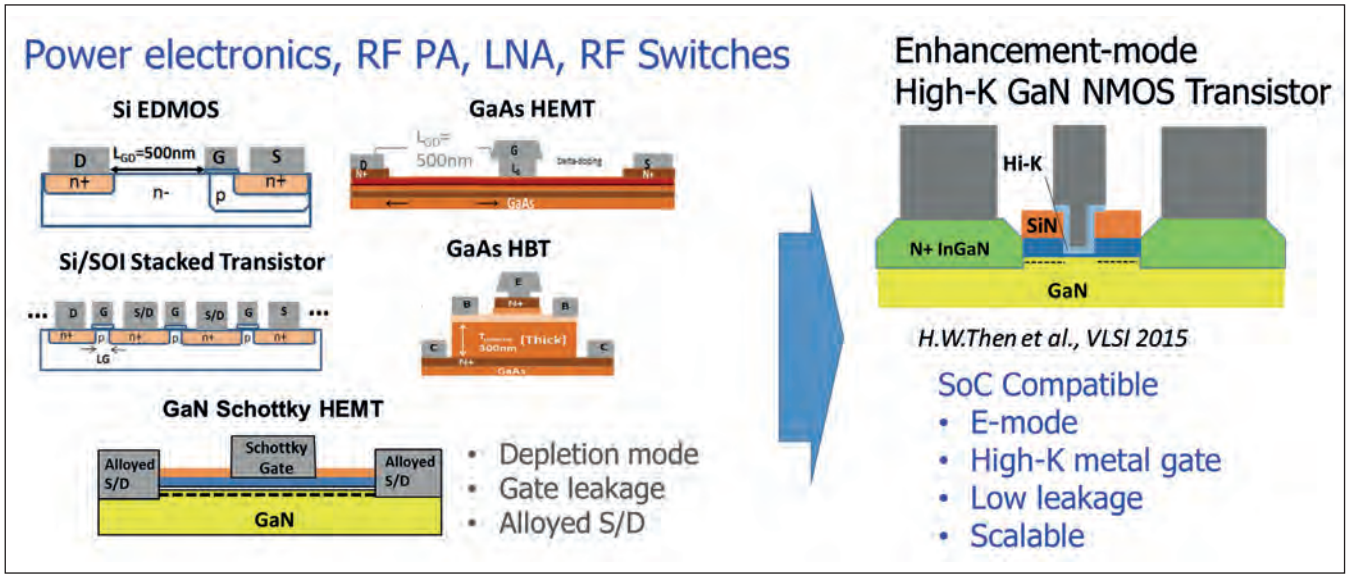


Figure 1. In today's power delivery and RF front-end solutions, dissimilar technologies come in multiple distinct and separate chips that have to be made to work together in a bulky package. Enhancement mode GaN transistors enabled by high-κ dielectric and metal gate technology can enable, for the first time, all these functionalities to be integrated on a single chip, realising a system-on-chip (SoC).

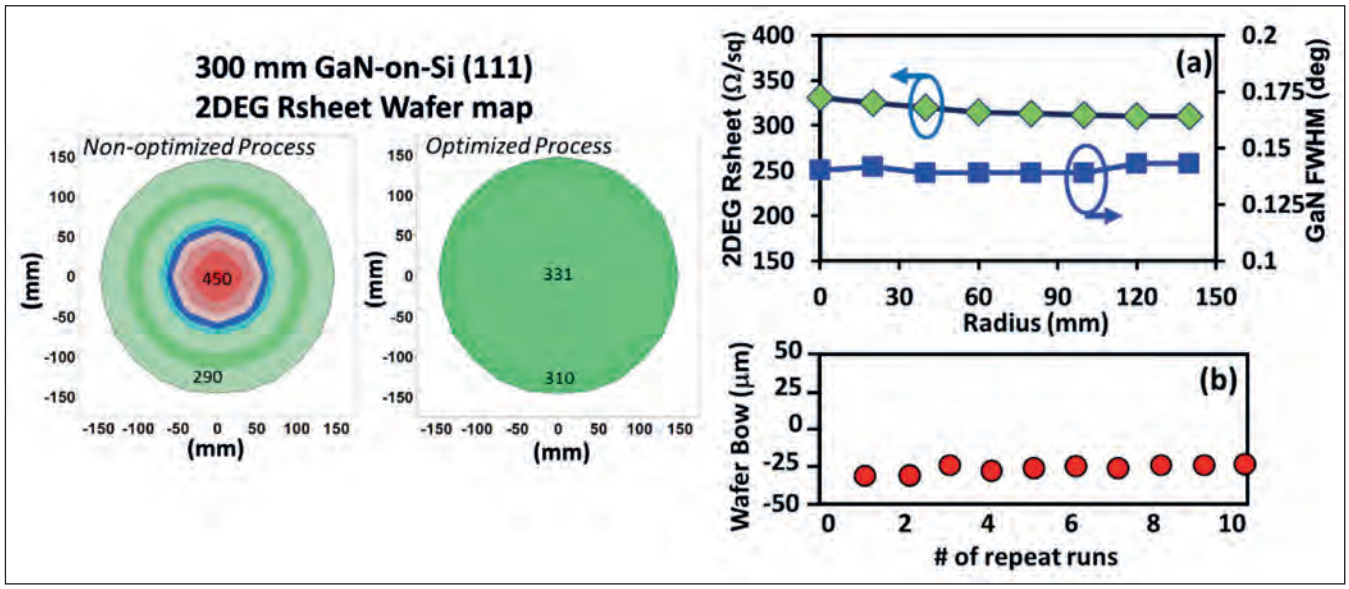


Figure 3. Optimised and uniform data from a manufacturable 300 mm GaN epitaxy process at Intel. Data distributions shown include: two-dimensional electron gas sheet resistance; GaN crystal quality, evaluated in terms of the the x-ray diffraction peak's full width at half-maximum (FWHM); and 300 mm wafer bow.

PMOS on 300 mm silicon substrates. Thanks to this, all functionalities can be integrated on a single chip to yield a system-on-chip for the very first time.

One of the successes that has come from our efforts is the fabrication of the first high-performance GaN transistors on 300 mm silicon (111) wafers (see Figure 2). We make these transistors with a 300 mm process technology that is compatible with leading CMOS fabs.

Another accomplishment is our use of a new technique of three-dimensional monolithic integration, based on layer transfer. With this approach we are breaking new ground by stacking silicon PMOS transistors on top of GaN NMOS transistors to enable CMOS functionalities.

This new technology significantly expands the universe of solutions that can be implemented and integrated in an efficient, tiny system-on-chip.

Using one of our leading CMOS fabs for processing our GaN transistors on 300 mm silicon reaps an additional reward – it opens the door to all the latest process innovations. They include high-κ technology, three-dimensional layer transfer, chemical-mechanical polishing, lithographic techniques and copper interconnects. In addition, we benefit from the significant reduction in cost associated with cheaper 300 mm silicon substrates and high-volume production.

Leveraging larger wafers

Due to the lack of native substrates, nearly all GaN is

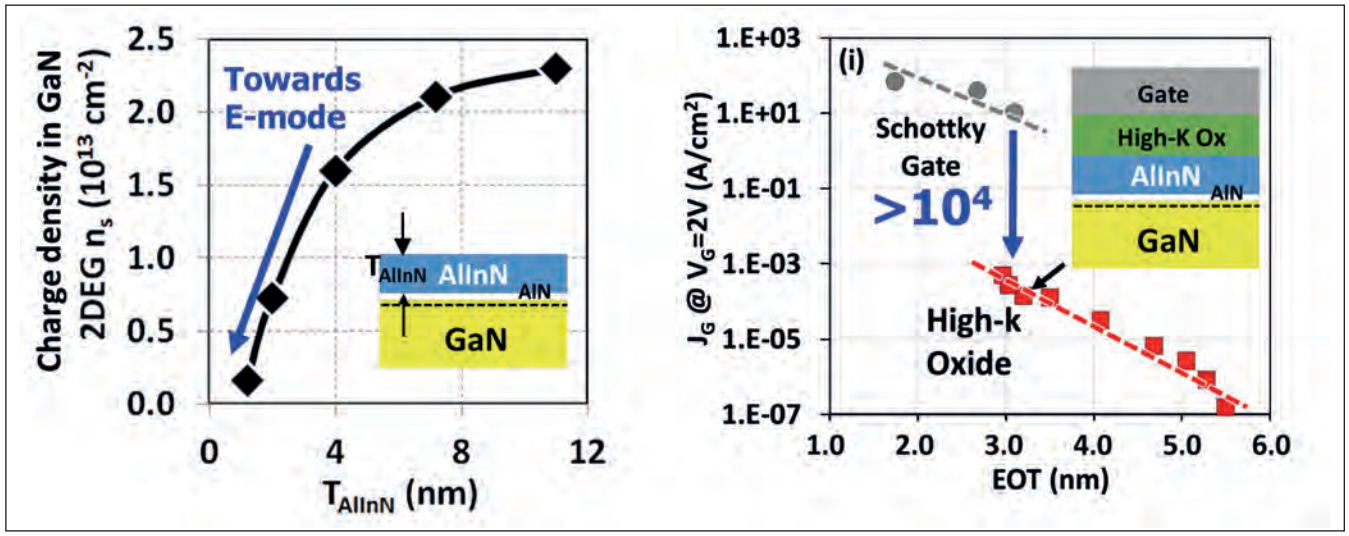


Figure 4. A high-κ gate dielectric reduces gate leakage by more than four orders of magnitude at scaled equivalent oxide thickness (EOT) for higher performance.

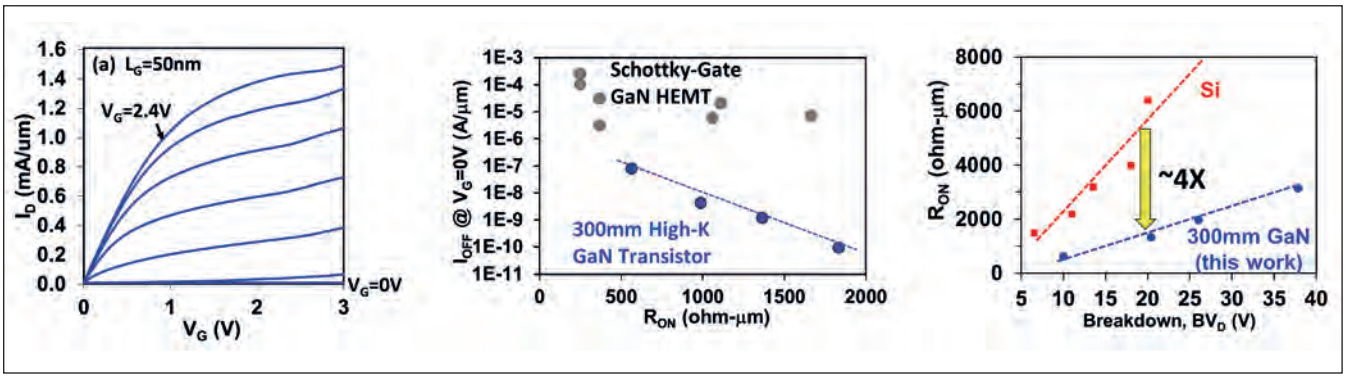


Figure 5. The I_D-V_D characteristics of Intel's e-mode high-κ dielectric GaN NMOS transistor on a 300 mm silicon wafer showing a high drive drain current that is approaching 1.5 mA/μm, a low knee voltage (it is below 1 V), and an on-resistance, R_{ON}, of just 610 Ω-μm. Low drain leakage, with I_{OFF} as low as 100 pA/μm at 5 V drain voltage, and excellent R_{ON} can be achieved simultaneously. The high-κ e-mode GaN NMOS transistors are about four times better than silicon transistors used for power delivery.

grown on foreign substrates, such as sapphire, SiC and silicon. The most popular platforms are 3-inch and 4-inch SiC, which are both relatively expensive, and 4-inch, 6-inch and 8-inch silicon (111). In contrast, we are using cost-effective 300 mm silicon (111) substrates (see Figure 3). On this platform we marry GaN with the most advanced high-κ dielectric metal gate technology in our 300 mm fab. This enables enhancement-mode operation and gate-stack scaling, and it ultimately realises high performance and low leakage, the keys to higher efficiencies. Note that this reduction in leakage is significant – it can exceed four orders of magnitude (see Figure 4) better than a Schottky gate GaN HEMT.

Another virtue of enhancement-mode, GaN transistor technology is that it simplifies the circuit architecture. As the enhancement mode transistor is normally-off, it does not require a negative power supply. Instead, this device can be driven directly from a battery, saving precious real estate on the microchip.

Measurements on our high-κ dielectric enhancement-mode GaN NMOS transistors on 300 mm silicon reveal excellent electrical characteristics and best-in-class performance for power delivery and RF. The devices have low drain leakages, high drive drain currents, low knee voltages and low on-resistances. Such characteristics show that high-κ dielectric technology enables a GaN transistor to combine a low leakage with excellent performance – it is about four times better than industry-standard silicon transistors for power delivery (see Figure 5).

Our devices also deliver excellent RF performance. Our high-κ GaN NMOS transistor significantly outperforms those based on GaAs and silicon/SOI transistors in power-added efficiency across a wide frequency range that spans 1 GHz to 30 GHz (see Figure 6). Due to the excellent knee voltage and on-resistance, efficient power amplifier (PA) operation is realised at drain voltages as low as 1 V (see Figure 7).

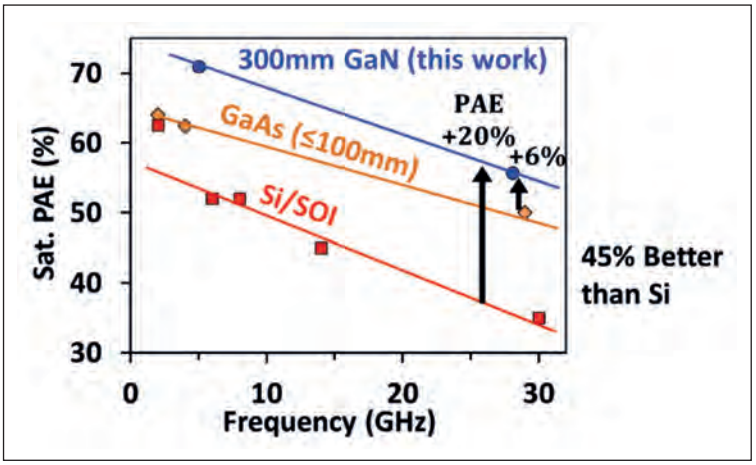


Figure 6. Intel's high-κ e-mode GaN NMOS transistor significantly outperforms GaAs and silicon/SOI across a frequency range spanning 1 GHz to 30 GHz.

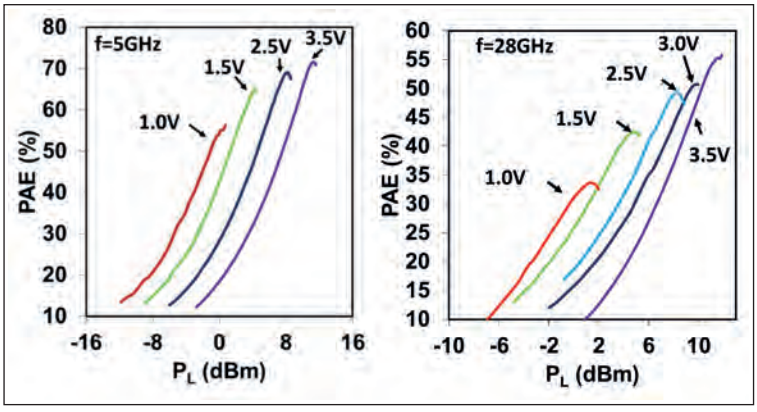


Figure 7. High power-added efficiencies are demonstrated with supply voltages from 3.5 V to as low as 1 V. Efficient PA operation well below 2 V surpasses the minimum cut-off supply voltage achievable by typical GaAs HBTs and highlights the potential of Intel's high-κ GaN transistor to extend battery life, and to realise efficient envelope-tracking RF PA.

The merits of GaN

Thanks to its wide bandgap, GaN has vastly superior Johnson and Baliga figure-of-merits when compared with GaAs and silicon (see Table 1). These virtues enable GaN to operate at high frequencies and high power.

An additional strength of GaN stems from the spontaneous and piezoelectric polarization effects associated with this family of materials. Due to this, a two-dimensional electron gas is produced in the GaN channel at the interface of GaN and a related ternary alloy, without the need for impurity doping. The resulting GaN heterostructure has a high carrier concentration, and also a high electron mobility, due to the low effective mass of the electrons and the absence of impurity scattering.

Yet another strength of GaN is that, due to its wide bandgap, it has a critical breakdown field that is at least ten times that for GaAs and silicon. This allows GaN transistors to be scaled to smaller lengths, leading to a higher performance. For example, for a supply voltage of 3.7 V, which is that provided by a lithium-ion battery, GaN transistors can be shorter, have a lower resistance and provide a higher drive current. Strengths such as these have made GaN the best semiconductor technology in production today for power and RF performance.

	Si	GaAs	GaN
Bandgap (eV)	1.1	1.42	3.4
Critical breakdown field, E_{crit} (MV/cm)	0.3	0.4	3.3
Electron Mobility, μ ($cm^2/V/s$)	1350	8500	2000
Peak velocity, v_{peak} (10^7 cm/s)	1	2	2.5
N-channel Baliga FOM$\propto\mu E_{crit}^2$ (normalized to Si)	1	11	179
N-channel Johnson FOM$\propto v_{peak}E_{crit}$ (normalized to Si)	1	2.7	27.5
Hole Mobility ($cm^2/V/s$)	<450	<400	<50
Active p-doping ($/cm^3$)	~10^{21}	~10^{19}	~10^{17}

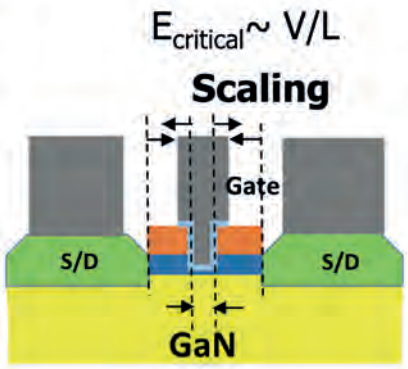


Table 1. Intrinsic semiconductor properties and figure-of-merits (FOM) for silicon, GaAs and GaN. N-channel GaN has the highest Baliga and Johnson FOMs, but P-channel GaN remains challenging due to low active *p*-doping and low hole mobility. The silicon PMOS transistor has a proven complementary P-channel with high hole mobility and high active *p*-doping.

This value is well below the minimum cut-off supply voltage for a typical GaAs HBT, highlighting the potential of the high-κ GaN NMOS transistor to significantly extend battery life while providing unrivalled efficiencies using the envelope-tracking RF PA architecture. High-κ GaN NMOS transistors also make excellent RF switches and low-noise amplifiers. For example, they have an excellent figure-of-merit for the switch, with a product of on-resistance and off-capacitance of just 110 fs. The minimum noise figure is only 0.4 dB at 5 GHz and 1.36 dB at 28 GHz (see Figure 8).

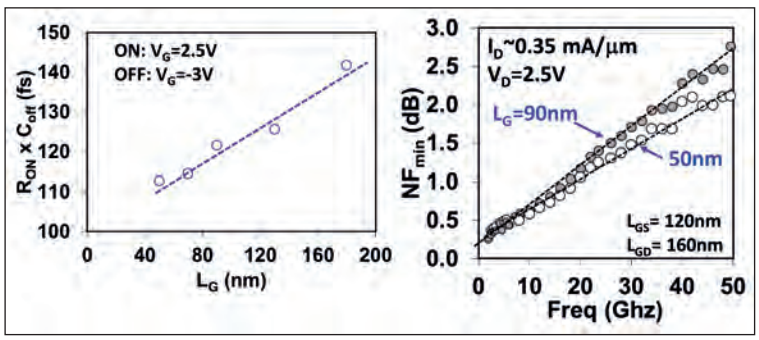


Figure 8. The excellent switch figure-of-merit, R_{ON} x C_{OFF}, and noise performance, NF_{min}, of the high-κ e-mode GaN NMOS.

The combination of the great performance as a power amplifier, a low-noise amplifier, an RF switch and a power transistor enables the enhancement-mode high-κ GaN NMOS transistor technology to boost the efficiency and performance of RF front-end and power delivery systems beyond what is capable today with GaAs and silicon technology. But that's not all – by turning to high-κ GaN NMOS transistor technology, we realise compact integration of multiple functionalities on a single chip, saving space and achieving unmatched small form factors.

Three-dimensional integration

A selling point in today's marketplace is tight on-chip integration of CMOS analog and digital logic/control functionalities, along with CMOS memory. These types of CMOS chips are currently built as standalone units, but as functionality and complexity increases, monolithic system-on-chip solutions will be needed to provide higher efficiency, lower cost and a higher integration density (see Figure 9).

However, it is extremely challenging to implement a design based on monolithic complementary GaN CMOS, due to the low hole mobility in GaN, and the difficulty in realising high *p*-type doping in this material.

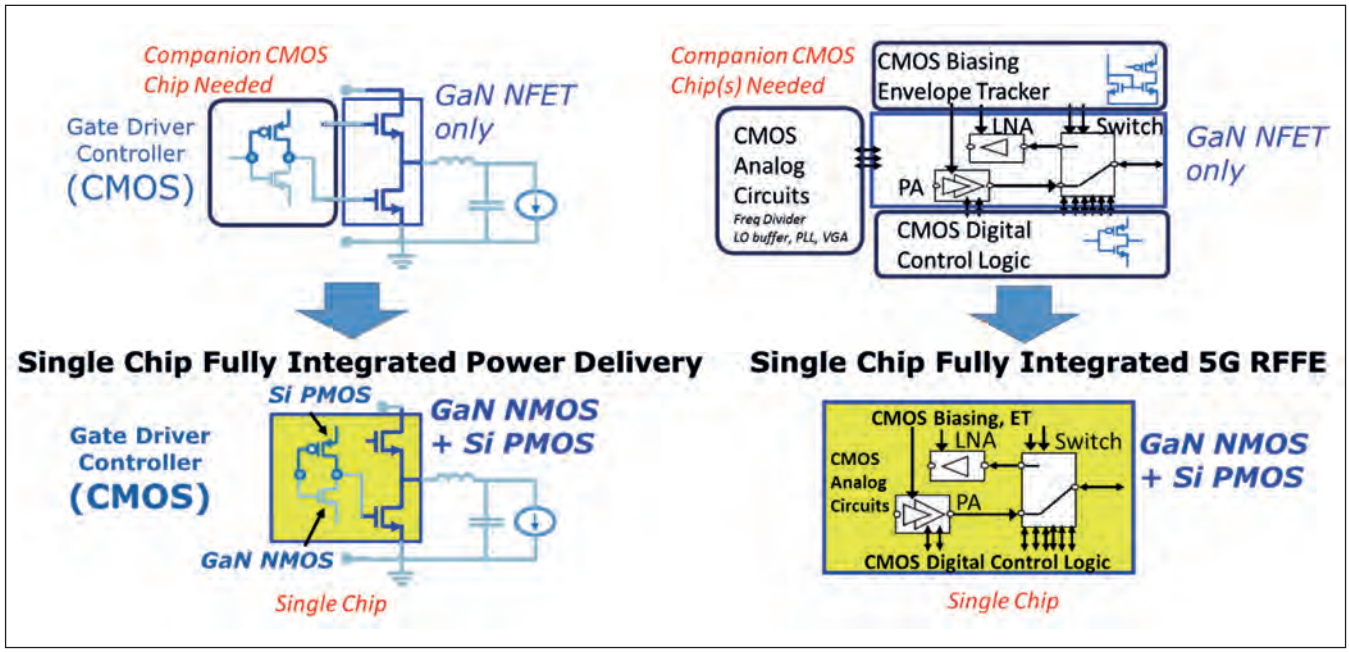


Figure 9. Single-chip fully integrated power delivery and RF front-end units can be realised with Intel's three-dimensional monolithically integrated silicon PMOS stacked on GaN NMOS transistor technology.

The good news is that progress is being made by a partnership between our team and research groups at Cornell and MIT. This effort hopes to fulfil the promise of wide bandgap, high-voltage operation of GaN PMOS. While this work is in its infancy, the hope is that standard high-κ metal gate silicon PMOS can step in to provide an excellent complementary p-channel technology to GaN NMOS, due to its high hole mobility and possibility to realise a very high *p*-doping for source-drain contacts.

To monolithically integrate multiple dissimilar semiconductor materials on a single silicon substrate, we have turned to layer transfer techniques. This enables us to monolithically stack silicon PMOS transistors on top of GaN NMOS transistors.

Drawing on this form of three-dimensional monolithic integration has much merit, as it allows each constituent transistor technology to be built and optimised separately to offer the best performance and cost.

We begin our three-dimensional layer transfer process by oxide fusion-bonding a standard 300 mm crystalline silicon (100) donor wafer to a completed 300 mm GaN-on-silicon (111) wafer. After this, we remove the bulk donor wafer and fabricate silicon PMOS transistors (see Figure 10). We ensure high-performance silicon PMOS by aligning the finfet in an orientation that boosts hole mobility. This is accomplished by having the transistor channel on the

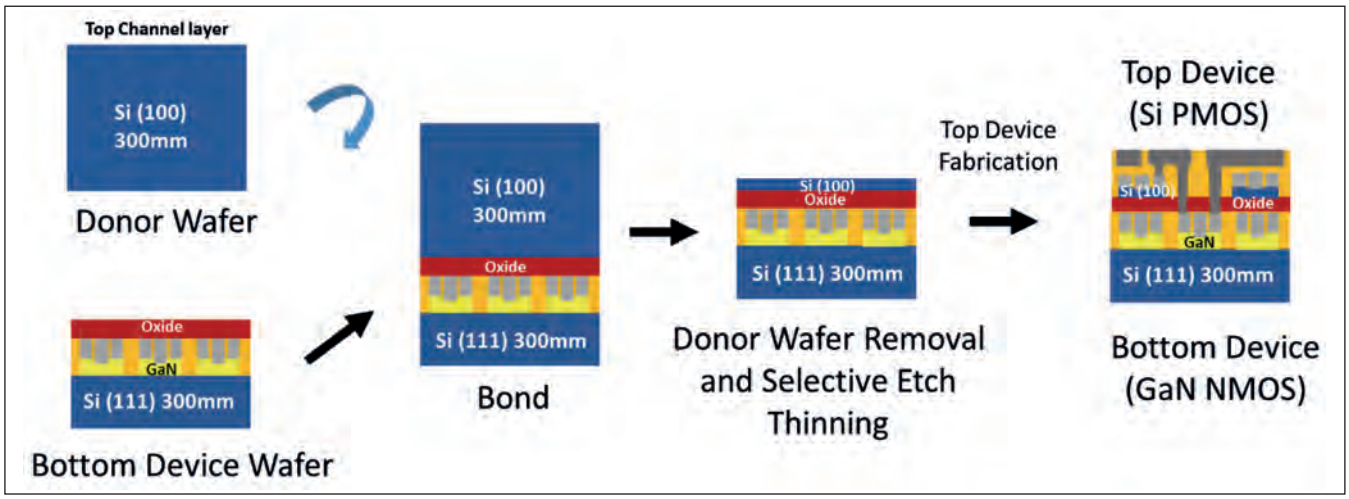


Figure 10. Intel's monolithic three-dimensional layer transfer process flow involves the transfer of a layer of single crystalline silicon from a 300 mm silicon (100) donor wafer onto a completed 300 mm GaN-on-silicon (111) wafer, prior to fabrication of the top silicon PMOS transistors.

sidewalls orientated in a particular crystal plane and current-carrying direction (see Figure 11). There is much freedom with our approach. The silicon PMOS transistor design and architecture can be made independently of the choices for the bottom GaN transistors. For example, by selecting the appropriate channel orientation for the silicon PMOS and the channel length for the GaN NMOS, the drive current and the off-state leakage can be matched for both channels (see Figure 12).

Our monolithic three-dimensional stacking of GaN NMOS and silicon PMOS transistors provides a powerful way to integrate two dissimilar best-in-class semiconductor technologies on the same wafer and deliver the best performance, increased density, and greater functionality.

This technology has tremendous promise as it could enable entirely new classes of products with game-changing capabilities. Many exciting opportunities lie ahead, including the full integration of efficient, high-performance RF and power delivery with standard silicon-based processors. Such a technology has the potential to meet the demands of next-generation mobile devices, data infrastructure and communication networks for 5G and beyond.

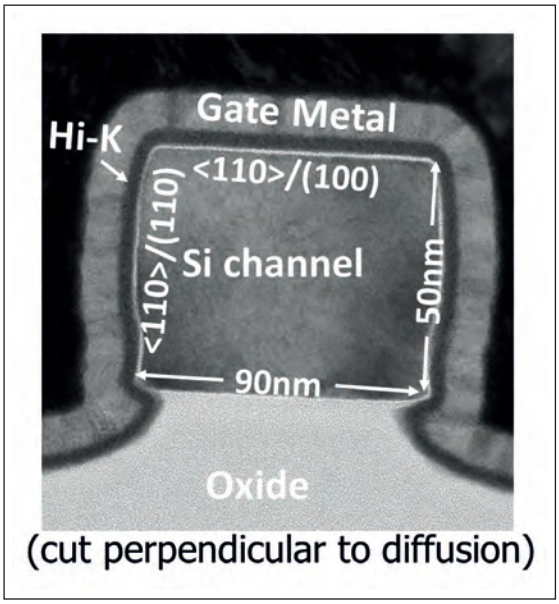


Figure 11. The cross-section of the top silicon PMOS transistor showing its finfet architecture, crystal orientation and current-carrying direction to boost hole mobility and performance. These silicon transistor design and architectural choices can be made independent of the choices made for the bottom GaN transistors.

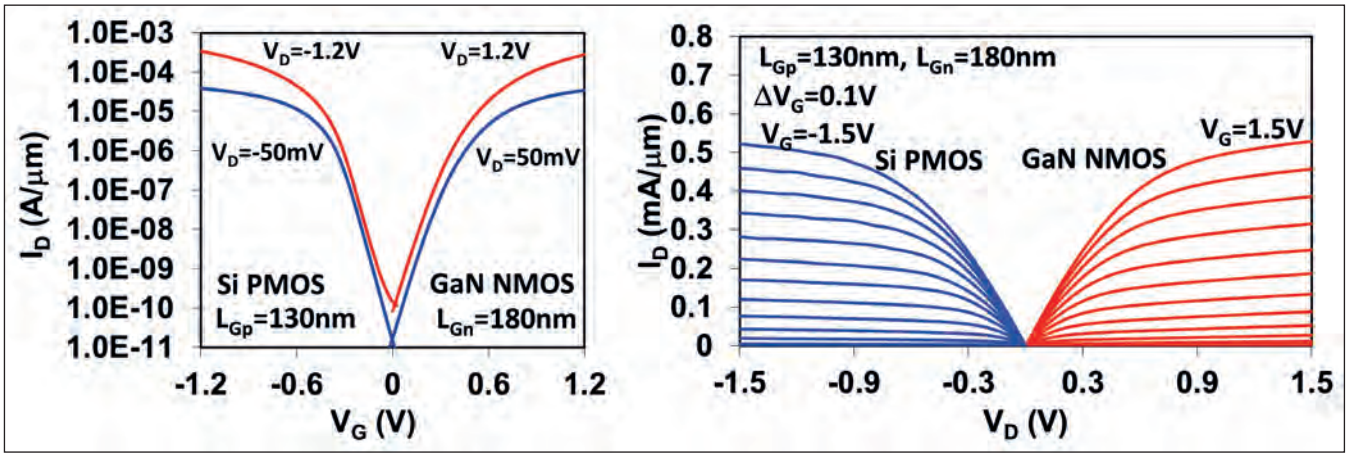


Figure 12. Current-voltage characteristics of the top layer channel length (L_G is 130 nm) silicon PMOS transistor and the bottom channel length (L_G 180 nm) GaN NMOS transistors. Dimensions have been chosen independently, to match drive current strengths and off-state leakages.

Further reading

H. W. Then *et al.* "3D heterogeneous integration of high performance high-κ metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications", IEDM, 2019.

H. W. Then *et al.* ""High-Performance Low-Leakage Enhancement-Mode High-κ Dielectric GaN MOS-HEMTs for Energy-Efficient, Compact Voltage Regulators and RF Power Amplifiers for Low-Power Mobile SoCs", VLSI Technology Symposium, 2015.

S. Bader *et al.* "GaN/AlN Schottky-gate *p*-channel HFETs with InGaN contacts and 100mA/mm on-current", IEDM, 2019.

N. Chowdhury *et al.* "First Demonstration of a Self-Aligned GaN *p*-FET", IEDM, 2019.

3 EVENTS
2 DAYS
1 TICKET

17-18 November 2020

Sheraton Brussels Airport Hotel, Belgium

One ticket gives you access to a 2 day event which will see 3 groups of device makers gathered under one roof.

Hear over 100 presentations covering the entire spectrum of the compound semiconductor, integrated photonics photonics and global sensor supply chain.

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

www.csinternational.net

Talk to us about sponsorship NOW as it will be another sellout

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

www.picinternational.net

SSI INTERNATIONAL CONFERENCE

Sensor Solutions: Market opportunities

www.sensorsinternational.net

REGISTER NOW, AND SECURE YOUR PLACE. REGISTRATION ALLOWS ACCESS TO: CS INTERNATIONAL, PIC INTERNATIONAL AND SSI INTERNATIONAL

AN ANGEL EVENT