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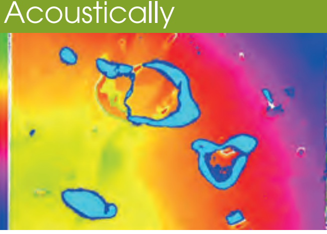

STEAG seeks to grow UK PV market

Banishing the buffer for power devices

GaN Systems releases automotive transistor

Xilinx

Enabling the aggregation of real-time power quality analysis in electric grids

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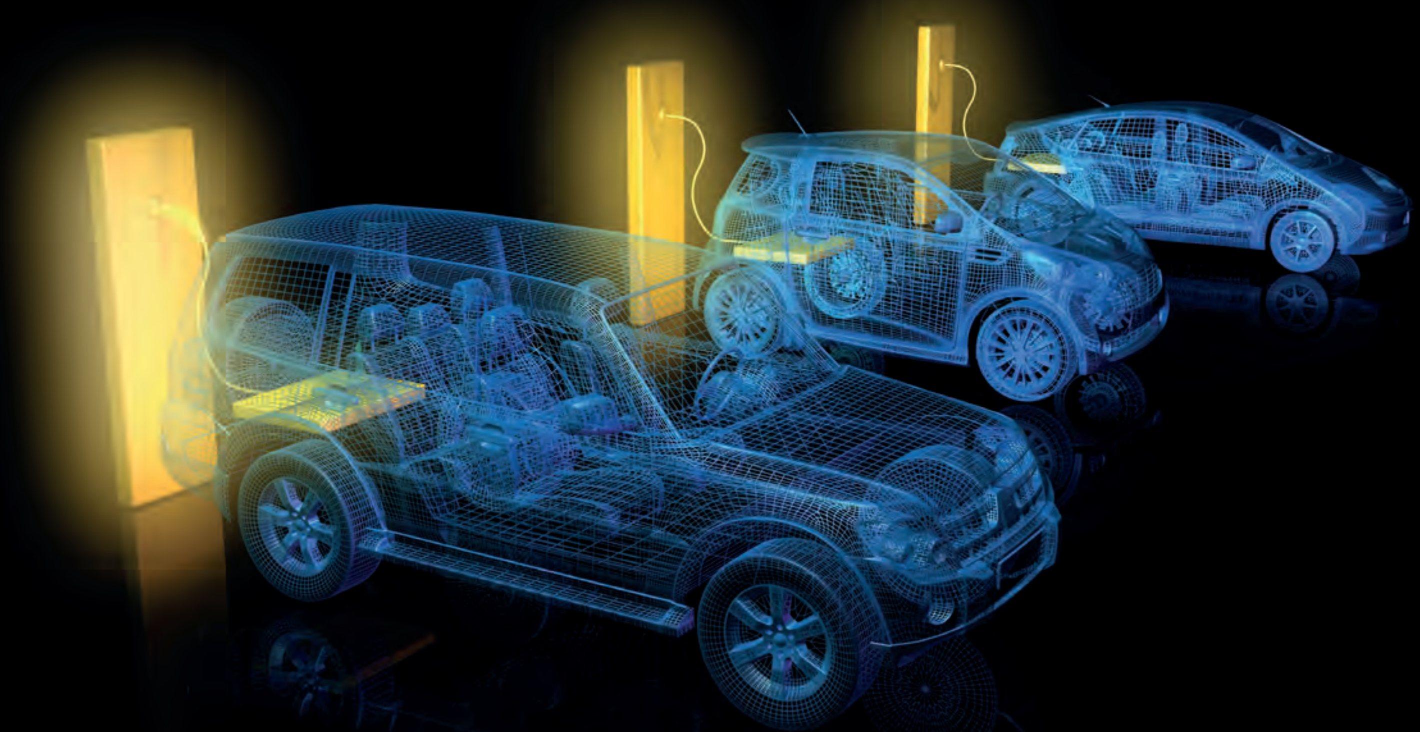

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Viewpoint

By Mark Andrews, Technical Editor

Powering through the year we didn't expect

COUNTING THE FINAL DAYS of any year is a time we traditionally reflect upon what happened while speculating about the year to come. No one across industry can say 2020 wasn't full of 'surprises.' Some good. Some bad. Some ***very*** bad. How do we assess the Year of the Pandemic?

Firstly, when we realized a new, potentially fatal virus was impacting the whole earth, we reacted with fear, denial, preparation, confusion and dread – And then we got on to deal with it, even while life as we knew it changed in previously unimaginable ways.

Secondly, while scores of business sectors remain under water, the semiconductor supply chain has managed growth despite hurricane headwinds. The SEMI industry trade group recently reported that fab investments grew 13 percent in 2020, eclipsing 2018's record performance. SEMI attributed the growth to accelerating digital transformation spurred by the COVID-19 pandemic.

Lastly, some companies have managed to actually prosper throughout the pandemic despite no direct connection to medical treatment or sectors that tend to grow when infectious disease captures headlines. Cases in point: in October, the International Monetary Fund (IMF) raised its GDP forecasts, saying that while it expects a 4.4 percent global decline in 2020, it forecasts a 5.2 percent expansion in 2021. What's more, semiconductor companies across the board fared better than many sectors. As we entered November, SEMI reported there were 38 new fabs under construction around the world.

In this edition of Power Electronics World we look at important trends and innovations driving success. STEAG Solar Energy Solutions details its ambitious plans to grow the renewable energy portion of its five-continent portfolio. Xilinx explains how its Alveo product line is bringing fast data analytics deeper into electricity transmission grids to enhance performance.

We also explore ways to power next-generation medical diagnostic and treatment tools that rely on the latest sensors, AI and machine learning – power for a new wave of devices that imec describes as 'Careable' technologies.

We also delve into multiple research advances that are accelerating the way that power electronics may shape future manufacturing opportunities.

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CONTENTS

10 COVER STORY

Enabling aggregation of real-time power quality analysis in electric grids

Data analytics is a significant and emerging force in the digitalisation of electricity transmission grids that can empower grid operators with a deeper understanding and precise control of their infrastructure

16 STEAG SENS seeks to grow UK PV market & global opportunities

The STEAG Solar Energy Solutions division of STEAG Energy Services GmbH has been a part of the UK photovoltaic (PV) energy market since the 2019 approval of its Gildemeister Energy Services acquisition

20 Buffer-free GaN-on-SiC epiwafers enable cost-competitive, higher performance power devices

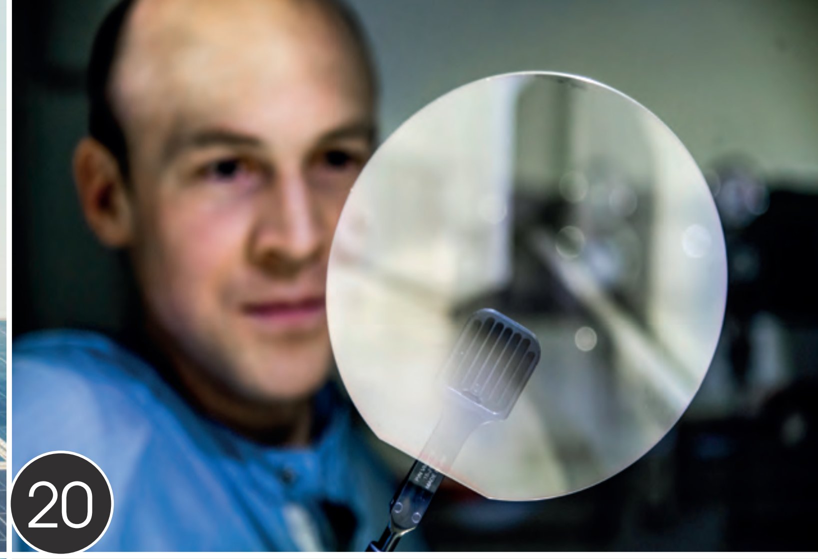
Following several decades of intensive research and development in both materials and devices, GaN-on-silicon HEMTs are starting to make inroads into the mainstream consumer market

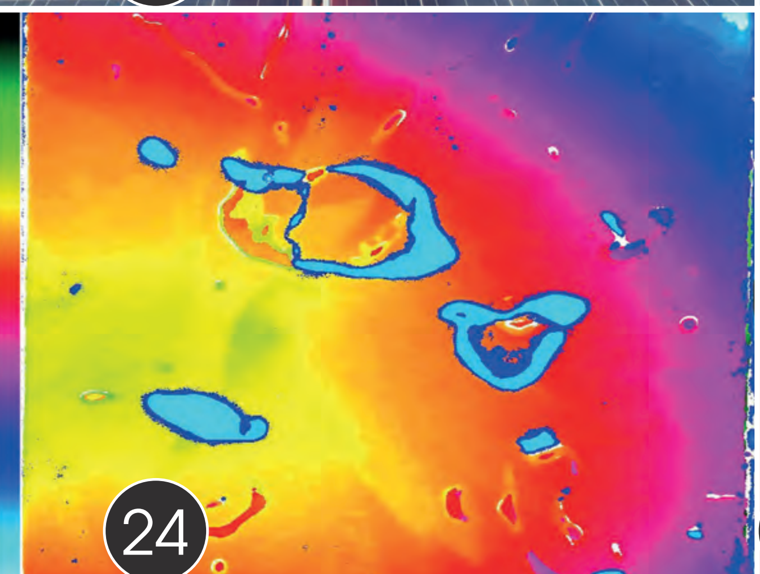
24 IGBT modules interrogated acoustically

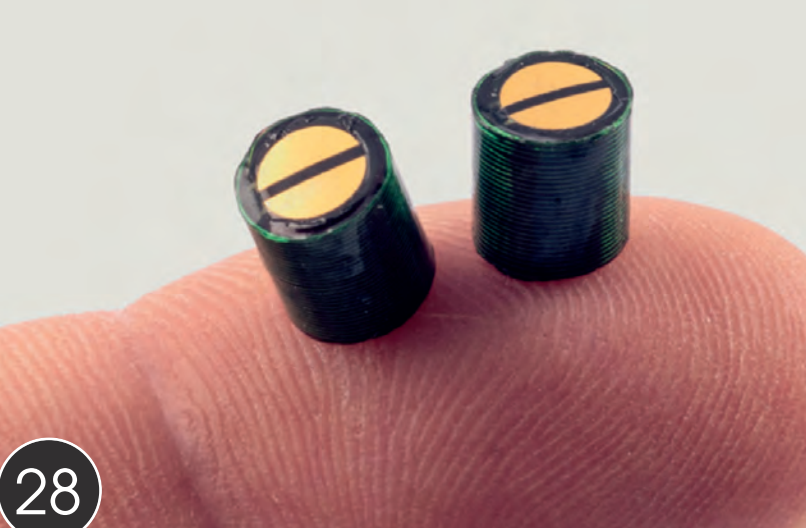
IGBT failures, because of the typically high voltage and power levels, can be both costly and dangerous. It makes sense to find internal structural defects be-fore they have an opportunity to go wrong

28 From wearables to ‘careables’: closing the loop in connected health

If we could combine vital sign sensing capabilities with smart algorithms and actuation features in order to not only diagnose but also ‘fix’ a problem in the body? Just like a pacemaker does today, a multitude of closed-loop systems will help us in the future







34 GaN Systems: all eyes on audio amplifiers

With the Class D audio amplifier market poised for massive growth, GaN Systems has set its sights on snaring a big chunk of the sector

36 Heterojunction enhances power diodes

Double-layered NiO contact provides a great p-type layer for ultra-wide-bandgap devices

37 Simplifying VCSEL design

Adding a nanoscale cylindrical waveguide to a GaN VCSEL yields record-breaking output powers

38 Slashing the on-resistance of GaN p-n diodes

Oxide vapour phase epitaxy enables an incredibly low on-resistance in GaN p-n diodes

news

06 Picosun's cluster ALD solutions enable next generation power electronics

07 Cadence announce IP solution for TSMC N5 process technology

08 Toshiba launches 1200V SiC MOSFET

09 GaN Systems releases 650V, 60A automotive transistor

Picosun's cluster ALD solutions enable next generation power electronics

PICOSUN GROUP, the supplier of AGILE ALD (Atomic Layer Deposition) thin film coating solutions for global industries, strengthens its position in power electronics market with several cluster ALD system sales to prominent manufacturers in Europe, USA and Asia.

"Power electronics is an important, fast growing market for Picosun. ALD has potential to solve various challenges manufacturers are facing in this field, and our solutions have enabled our customers to create significant added value in terms of device quality and throughput. At Picosun, we have developed several turn-key production ALD solutions specifically for 4-8 inch wafer markets such as power devices. Especially our cluster ALD systems, such as the PICOSUN Morpher which we launched last year, have been extremely well received by our customers," says Juhana Kostamo, Head of Customer Solutions/Deputy CEO of Picosun.
Power components are crucial in a wide range of applications from consumer electronics to transportation, energy production and distribution, including renewables such as wind and solar power generation. These components are typically manufactured on 4-8 inch compound semiconductor wafers such as GaN and SiC. These materials provide various benefits compared to pure silicon, for example higher electron mobility, higher threshold voltage, and ability to operate at higher temperatures. Challenges do exist, however, as GaN and SiC power devices are prone to high interface trap density (leading to parasitic currents and reduced electron mobility) and gate leakage current, and poor threshold voltage stability.

Interface trap density can be reduced by combining pre-cleaning methods with high permittivity, large bandgap insulators. High quality, defect-free high-k dielectric layers such as Al2O3, AlN or ZrO2 etc. are key in reducing power devices' gate leakage current and to improve electron mobility and threshold voltage stability. A good example here are GaN-based HEMTs (high electron mobility transistors), which are important in various large scale practical applications, and which require efficient gate insulation and surface passivation to achieve optimal functionality.
ALD stands as a superior deposition method here compared to other thin film coating technologies such as PECVD, as ALD produces the most conformal, uniform, and defect-free films with accurate, digitally repeatable thickness control and sharp interfaces. With the right selection of ALD deposition equipment, even multilayer processing is possible i.e. various functional material layers and/or stacked films/ nanolaminates can be manufactured in one process run.

PICOSUN Morpher is a disruptive ALD production platform designed for up to 8 inch wafer industries such as power electronics, MEMS, sensors, LEDs, lasers, optics, and 5G components. Morpher's operational agility makes the system adaptable to various and changing manufacturing needs, on all business verticals from corporate internal R&D to production and foundry manufacturing, where both the end products and/or customers' requirements may change rapidly. Morpher can handle several substrate materials, batch and substrate sizes, and ALD materials with leading process quality. Multilayer deposition is possible, and cluster design allows integration of also other processing units such as pre-clean, RIE etc. for fully automated, high throughput continuous vacuum operation.
"In its versatility and transformability, Morpher is the epitome of our principle 'Agile ALD'. Innovation, constant development and improvement of our ALD solutions to enable our customers' success is our driving force at Picosun. This applies also to Morpher platform and we have some truly exciting additions to this product family coming in the near future," summarizes Kostamo.

Cadence announce IP solution for TSMC N5 process technology

CADENCE DESIGN SYSTEMS,has announced the immediate availability of a complete, silicon-proven Cadence IP supporting the DDR5 and LPDDR5 DRAM memory standards on TSMC N5 process.

The multi-standard IP includes Cadence PHY and controller Design IP and Verification IP (VIP) and supports a wide variety of applications including data center, storage, artificial intelligence/ machine learning (AI/ML) and hyperscale computing. Customers using Cadence and TSMC technologies can design advanced-process chips that connect to multiple memory types more quickly and with low risk.

Cadence's IP collaboration with TSMC is critical in today's market landscape. For example, the union of DDR5 and LPDDR5 protocol solutions in the same memory interface IP offers a high-speed, scalable solution from large to small memory footprints.

The goal of this Cadence IP is to make DDR5 and LPDDR5 implementation predictable and successful and to make it a flexible solution. The multi-standard DDR5/LPDDR5 IP solution allows users to use a single chip to support multiple memory types in different environments, enabling their chips to be used in different markets and products with different DRAM requirements.

"Designers of next-generation intelligent products require simple, efficient access to high-performance memory," said Malcolm Humphrey, vice president and general manager of the core compute business for the Compute and Networking Business Unit at Micron.

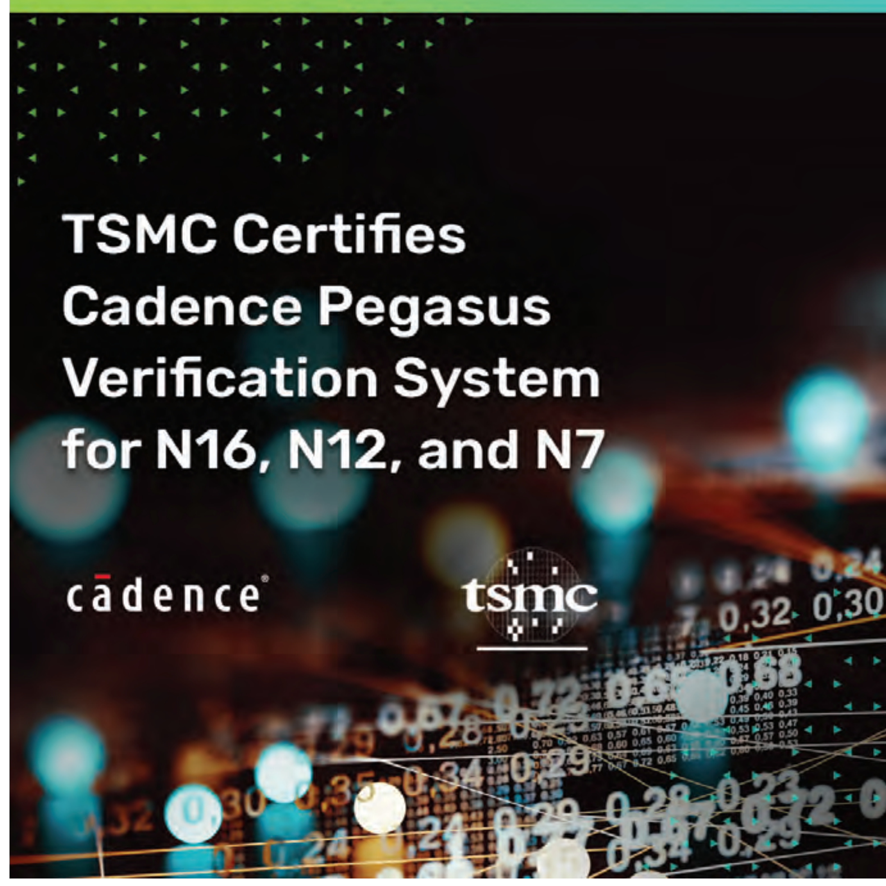
"Micron's collaboration with Cadence and TSMC enables leading-edge memory interface IP on advanced technology nodes, empowering the ecosystem by bringing complete DDR5 and LPDDR5 DRAM memory solutions to the most advanced systems on chips."

"We're pleased to see the delivery of Cadence's DDR5/LPDDR5 IP on the TSMC 5nm process technology, which is optimized for the latest emerging application areas," said Suk Lee, Senior Director of the Design Infrastructure Management Division at TSMC.

"Through our continued collaboration with Cadence, we're enabling mutual customers to design with these solutions, benefiting from the remarkable performance and power boost of our most advanced process technology and quickly launching their new product innovations to market."

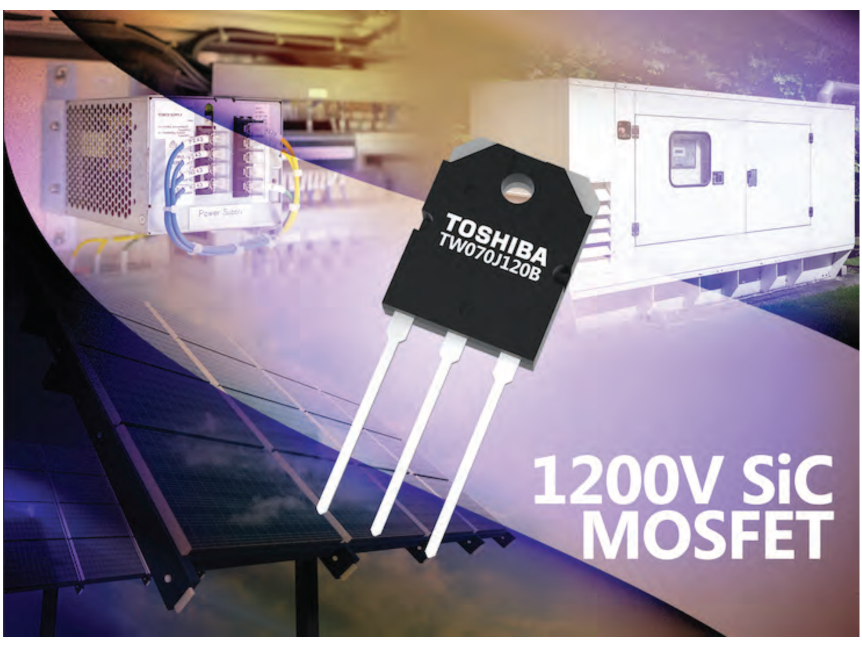
"As we continue to expand our collaboration with TSMC, our latest DDR5/LPDDR5 IP in TSMC's 5nm process technology uniquely addresses the needs of next-generation data center, AI/ML and hyperscale applications," said Sanjive Agarwala, corporate vice president, R&D in the IP Group at Cadence. "Cadence IP solutions help customers simplify the design process so they can successfully deliver innovative, intelligent semiconductor products in a timely manner."

The DDR5/LPDDR5 IP supports the Cadence Intelligent System Design strategy, which enables advanced-node system-on-chip (SoC) design excellence. The IP leverages technology from Cadence's silicon-proven DDR and high-speed SerDes designs as well as comprehensive verification capabilities with Cadence VIP, providing designers with the utmost confidence when implementing SoCs.



Toshiba launches 1200V SiC MOSFET

Toshiba Electronics Europe GmbH has launched a 1200V silicon carbide (SiC) MOSFET for high power industrial applications including 400V AC input AC-DC power supplies, Photovoltaic (PV) inverters and bi-directional DC-DC converters for uninterruptible power supplies (UPS).



The new TW070J120B power MOSFET is based upon SiC, a new wide bandgap material that allows devices to deliver high voltage resistance, high-speed switching, and low On-resistance when compared to conventional MOSFETs and insulated gate bipolar transistor (IGBT) products based upon silicon (Si). As a result, the new MOSFET will make a significant contribution to reduced power consumption and improved power density, leading to opportunities for system downsizing.

Fabricated with Toshiba's second-generation chip design[1], the new SiC MOSFET offers enhanced reliability. Additionally, the TW070J120B realizes low input capacitance (CISS) of 1680pF (typ.), a low gate-input charge (Qg) of 67nC (typ.), and a drain-to-source On-resistance (RDS(ON)) of just 70mΩ (typ.). When compared with a 1200V silicon IGBT such as Toshiba's GT40QR21, the new device reduces turn-Off switching loss by approximately 80% and switching time (fall time) by around 70%, while delivering low On-voltage characteristics with a drain current (ID) of up to 20A.

The gate threshold voltage (Vth) is set high (in the range 4.2V to 5.8V), which reduces the possibility of unintended or spurious turn On or Off. Furthermore, incorporation of a SiC Schottky barrier diode (SBD) with a low forward voltage (VDSF) of just -1.35V (typ.) also helps to reduce losses.

Housed in a TO-3P(N) package, the new TW070J120B MOSFET will enable the design of higher efficiency power solutions, especially in industrial applications, where the increased power density will also contribute to reduced equipment size and weight.

Infineon SiC shrinks EA Elektro-Automatik power supply

HYBRID and fully electric vehicle sales are picking up speed worldwide. While this is great news for reducing CO2 emissions, this is challenging for testing capacities of electronic components, namely motor, control, and battery. Testing, however, is a critical part of bringing any electric drivetrain into production. Traditional test setups require a dedicated DC source and electronic load in parallel to deal with bidirectional energy flow.

The power supply PSB 10000 of EA Elektro-Automatik, Germany's leading manufacturer of laboratory power supplies and electronic loads, offers a bidirectional solution for this application. It simplifies the test setup and reduces test time. Additionally, it offers great potential for savings in both acquisition and maintenance costs. And thanks to discrete 1200 V CoolSiC MOSFETs from Infineon Technologies, the system operates with efficiencies of over 96 percent. Used as an electronic load, the energy is fed back into the power grid, and only a small amount of energy is dissipated in the form of heat. The power density is industry-leading with 30 kW in a single 4U 19inch housing.

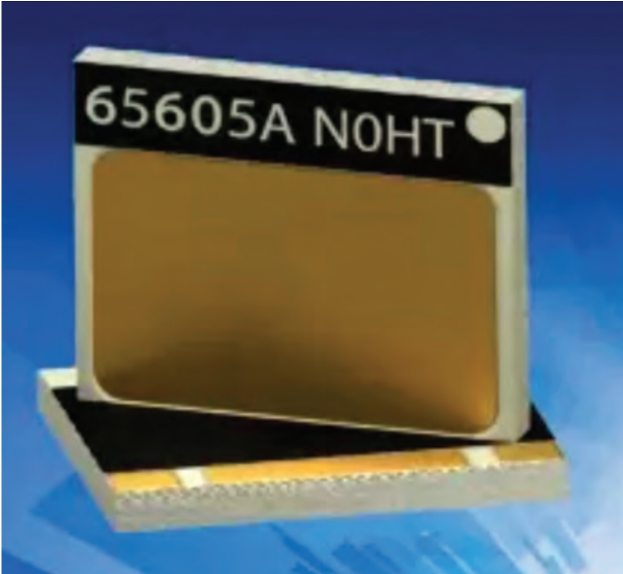
The device series PSB 10000 features an output stage with an extended scope of operation. Typical programmable DC sources offer full output power only at maximum voltage and current. The devices from EA Elektro-Automatik, on the other hand, offer full power from as little as one-third of the output voltage or output current. Charging or discharging a vehicle battery can serve as a good example.

Even if the battery voltage rises or falls, the current automatically adjusts and thus provides full power. The flexibility of the devices can save a lot of equipment when testing different electronic components.

GaN Systems releases 650V, 60A automotive transistor

GaN Systems has announced the release and availability of the first product in a family of new 650V, 60A transistors for the automotive market. The GS-065-060-5-T-A is designed to meet automotive reliability standards including AEC-Q101 qualification and GaN Systems' AutoQual+ testing and qualification.

AutoQual+ is an enhanced AEC-Q test sequence based on the company's collaboration with automotive partners to prove its transistors lifetimes exceed market requirements.



The new GaN transistor provides low RDS(on) (25 mΩ) and features a 60A IDS rating and GaN Systems' high-performance GaNPX® packaging, which enables ultra-low inductance and best thermal resistance in a compact form factor. Leveraging these transistors, wide ranging automotive applications from onboard battery chargers, DC-DC converters, EV traction inverters, electronic power steering, and motor drives can benefit from high reliability and reductions in volume, weight, and cost.

GaN Systems' methodology for the qualification of its transistors is based upon a collaboration with select customers in the global automotive industry. This joint effort resulted in an enhanced test methodology, AutoQual+, using AEC-Q101 tests as a baseline and then adding additional tests that address GaN-specific wear-out mechanisms. The additional testing of AutoQual+ ensures GaN Systems' power semiconductors are reliable and robust in the rigors of the automobile environment. As a result, GaN Systems products meet the lifetime requirements the automotive industry requires with demonstrated FIT rates much less than 1, setting new benchmarks in the GaN industry.

"GaN Systems transistors have been tried and tested through the AutoQual+ test methods, a testing regimen that stemmed from our many workshops with automotive partners," said Maryam Abouie, director of reliability engineering at GaN Systems.

"The knowledge these experts provided, including sharing decades of experience of silicon failure mechanisms identified in field-based applications, was critical in the development of our qualification strategy and process."

ENGIE and Kiwi Power enter Netherlands' grid flexibility market

Advanced energy technology company Kiwi Power has entered its tenth European market with the completion of an innovative aggregation project in the Netherlands.

The Engie project uses Kiwi Power's bespoke hardware and virtual power plant software to provide grid flexibility to the system operator in the local Primary Frequency Response (FCR) market.

The so-called 'Battery Box' project will deliver up to 3MW for system operator TenneT and is designed to be mobile, powering construction sites, events or when the grid capacity isn't sufficient enough.

Between projects it will be placed into the local FCR market, boosting grid reliability for the local area and providing a consistent revenue stream for asset owners ENGIE and Bredenoord , an independent specialist that develops, supplies, maintains and operates decentralised energy systems worldwide.

The Netherlands is one of Europe's highest ranking and active regions for demand side flexibility according to Delta-EE's forward looking 2019 EU Market Monitor Map for Demand Side Flexibility.

The use of the platform signals the latest milestone in Kiwi Power's continuing European expansion. Established in 2009, Kiwi Power has used its market-leading distributed energy solutions platform to deliver greater grid reliability and resilience across the continent.

The technology company now counts several of Europe's most active Demand Side Response (DSR) markets among its client roster including France, the UK and Germany.

Stephan Marty, Chief Commercial Officer at Kiwi Power said: "Step-by-step we're seeing changing regulation allow more countries to benefit from distributed energy resource flexibility, which will be a critical enabler of Europe's sustainable recovery post COVID-19. Becoming active in our tenth market not only marks our own success but is reflective of our continuing momentum in Europe."

The EU Market Monitor Map predicts a rapid and dynamic evolution of flexibility markets across all territories reviewed in the report in differing value streams, customer segments, asset types and market stakeholders.

Marty continues: "As further European markets open up to distributed energy resource flexibility, Kiwi Power is perfectly positioned to enter these key regions as early as possible, enabling us to continue our European success story."

Enabling the aggregation of real-time power quality analysis in electric grids

Data analytics is a significant and emerging force in the digitalisation of electricity transmission grids that can empower grid operators with a deeper understanding and more precise control of their infrastructure. Efficient and accurate data analytics requires sufficient compute power to achieve desirable results. Xilinx is pioneering new approaches to bringing the benefits of large-scale data analytics to legacy and future electrical grid infrastructure.

BY ARMANDO ASTARLOA, CEO AT SYSTEM-ON-CHIP ENGINEERING S.L. AND MICHAEL ZAPKE, ISM PRODUCT MARKET MANAGER AT XILINX

THE DIGITIZATION of the grid is a continuous process, both for operational and user networks. Specifically, the Ethernet broadcasting of current and voltage values for control and protection applications is a reality on the newest digital power substations.

Emerging applications like DER system coordination, electric transmission lines continuous monitoring, and power quality assessment demand virtual technologies capable of processing in real-time a large volume of these streams.

This article presents an innovative solution to accelerate the computation of hundreds of SMV streams combining a silicon IP and a new generation FPGA based accelerator cards. This solution uncovers the complexity of SMV processing and offers a high-level interface for application designers.

Standards & Regulations

The electric utility sector is strongly standardized and regulated. The International Electrotechnical Commission (IEC) organization is in charge of

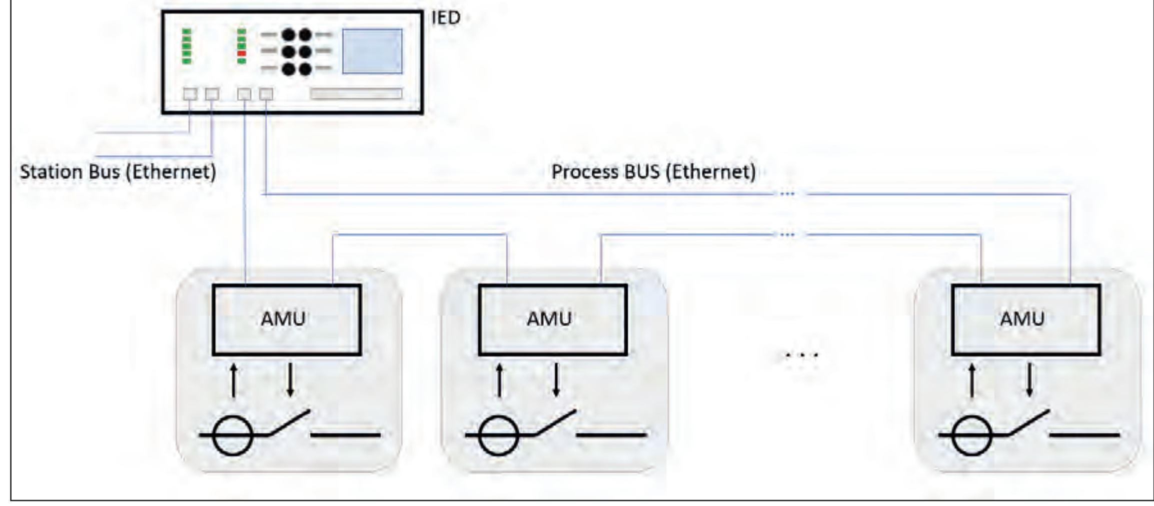


Figure 1: Typical Analog Merging Units (AMU) and Intelligent Electronic Devices (IEDs) in Power Substations Process Bus

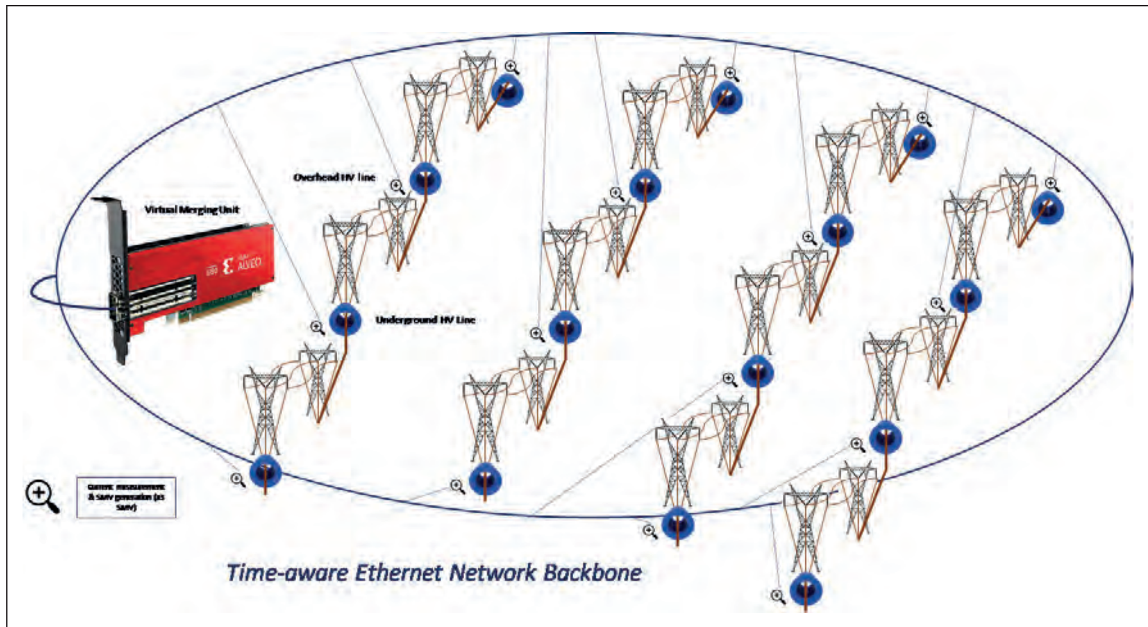


Figure 2: Extending the protection of mixed HV lines (overhead and underground) to the grid using virtual merging units

developing and maintaining the International Standards and Conformity Assessment for all electrical, electronic and related technologies. In the context of the digitalization of the electric grid, the IEC 61850 international standard defines the automatization basis and communication protocols for Intelligent Electronic Devices (IEDs) at electrical substations.

One key innovation defined in this standard [61850-9-2] was the digitization of current and voltage transformer (CT and VT) and other signals at the source and then communication to those devices using an Ethernet-based local area network (LAN). These digital frames are called Sampled Measured Values (SMV) and are typically published values of current and voltage for the four phases (A, B, C and N).

The original application for the SMVs was simplifying the cabling infrastructure and improving the availability at the process bus of power substations. In this context, the grid protection mechanisms are managed based on the fault analysis of the current and voltage magnitudes. This analysis is done by the IEDs based on the SMV frames broadcasted by the merging units (MU) installed on the secondary of the transformers.

A typical example of this setup is represented in Figure 1. In these set-ups, the number of SMV streams broadcasted on the network usually is not high. Thus, the embedded computers of IED can handle them, which fulfils the tight real-time requirements enforced by IEC 61850 for grid protection.

Once this digitalization mechanism had gained acceptance in the sector, new applications and use-cases have started to arise. As an example, the Industry has identified that the fault detection on cable sections in the transition from aerial to underground high-voltage lines [CFD19] can benefit from this digitalization. In scenarios where the number of measurement points is reduced (as an example, three pylons) and the longest distance to the further pylon is less than 20 km, a solution based on optical flexible transformers and analogue merging units can be engineered.

However, if this approach is to be scaled to the whole high-voltage line or to wider sections of the Smart Grid, a centralized computation solution is desirable. This solution is capable of receiving SMV streams by using high-bandwidth data backbones and may enable a new range of applications while a significant reduction of overall costs is also obtained.

Figure 2 represents this use-case schematically. As it can be observed, if this approach is scaled in several strategic locations of the grid, the number of SMV streams that would need to be transmitted and processed increases drastically. This challenge cannot be achieved by conventional IEDs due to their constrained networking and computation capabilities.

A representative example of the emerging applications based on the analysis of detailed values of the grid was the power quality analysis done at Sundom Smart Grid (SSG), a pilot programme of ABB Oy. [CIRED19]. The emerging spread renewable energy sources identified as distributed energy resources (DER) and microgrids demand real-time response. This actuation needs to be evaluated in base of real-time measurements and high-speed networking. In this context, technologies like big data analysis, machine learning (ML) and artificial intelligence (AI) play vital roles.

These new technologies need to manage a large volume of data, and in some of the use cases,

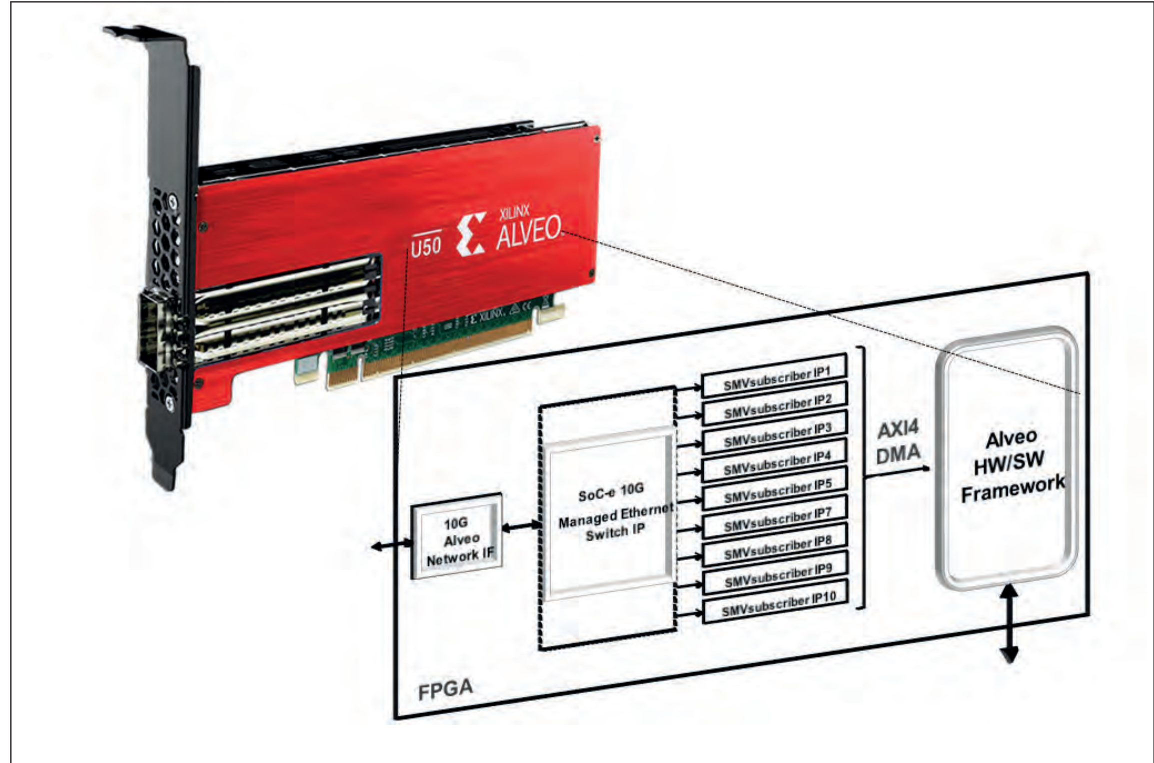


Figure 3: A SMV Subscriber Accelerator over Xilinx Alveo U50 card; compact and low-profile acceleration card models like the Alveo™ U50 from Xilinx specifically target on-premises acceleration.

with real-time requirements. The following analysis quantifies a potential real set-up: the maximum size of a SMV frame is 140 bytes, and a typical sampling rate is 4 Khz. Therefore, the required data bandwidth for each SMV is 448 Mbps.

According to the Wind Europe report 2019, the number of wind installations in Europe (on-shore and off-shore) is close to 190,000 [ENTSO19]. In a potential on-premises aggregation of information from 200 DERs in a small region, assuming 80 measurement points in each, the number of SMV that should be processed in real-time would be 16,000. In total, approximately 72 Gbps of net data would need processing under real-time conditions.

These magnitudes are far from the typical computing capacity of IEDs, which are usually capable of processing less than 10 SMV per unit. And is even for dedicated CPU processors like Intel Quad-Core i5 that saturates with 80 SMV [CIRED19]. Therefore, the need for a hardware acceleration would really help to enable this new generation of big data analysis applications.

Solution at Reconfigurable Silicon Level

Acceleration of computation using dedicated hardware is a hot topic. GPUs and FPGAs are massively used in the latest generations of edge and cloud equipment. The acceleration in applications that process very high numbers of SMVs requires high-speed data packet processing and digital signal processing (DSP). Specifically, the extraction and reordering of the payload is done at the packet processing level. Typical DSP operations include the Discrete Fourier Transformation (DFT) to extract the harmonic composition; the root mean square (RMS) computation to know the effective values of current and voltage; phase calculation and custom decimation of the raw SMV stream for further computations.

This hardware processing requires flexibility. The format of the SMV frames varies depending on the standard and configuration that applies. Moreover, the computation that shall be accelerated by hardware may vary depending on the final goal. The new generation FPGAs and reconfigurable SoC offer this flexibility and allow a fully pipelined implementation in the logic of the packet processing followed by the custom DSP.

The product SMVsubscriber from SoC-e [SMVsubscriberIP] is running on Xilinx devices and therefore benefits from this approach. It allows the deterministic processing of massive SMV streams with very low latency. Each IP instance is able to process in parallel from 128 to 320 simultaneous SMV streams on the process Window configuration. The computation is deterministic in the range of 6 μs of latency for a full computation.

Each IP instance supports a standard stream on-chip bus, AXI-4 stream, which enables the interconnection with Ethernet switch IPs, like the 10G Managed Switch Ethernet IP. Internally, this switching IPs work as a SMV frame splitter to distribute the load among the parallel SMVsubscriber instances as it is depicted in Figure 3.

Acceleration al Platform Level: Xilinx Alveo Accelerator Card

The new generation of acceleration cards based on reconfigurable logic are boosting data driven workloads including high performance computing, networking, computational storage acceleration, data analytics and video processing, many of these are tied to Industrial IoT applications.

Recently, new compact and low-profile acceleration card models like the Alveo™ U50 from Xilinx specifically target on-premises acceleration. This combination is very attractive to implement aggregated and accelerated computations focused on industrial or energy applications. These sectors demand a practical trade-off between edge and cloud computing and typically rely on small data centres or isolated high-end industrial PCs on-premises.

Xilinx Alveo is the product line of accelerator cards with the variants: Alveo U200, Alveo U250, Alveo U280, as well as the new Alveo U50 referred to in this article. All cards of this product family are made for the acceleration cloud and edge (on-premises) applications. A key differentiator of the entire Alveo line-up is the existence of local data (Ethernet) interfaces in addition to the PCIe connectivity, which makes them ideal for networked applications like the one that has been described in our article.

Xilinx Alveo U50 is a high-performance accelerator with a smaller form factor than previous generations of Alveo boards. It is passively cooled with a max thermal design power (TDP) of 75W (typical 50W) and it has passive thermal design in a single slot (half height, half length) and is therefore significantly smaller than the other Alveo boards. It comes with a QSFP28 cage for 100 Gbit traffic over the local interface in addition to the PCIe connectivity with up to 2x PCIe Gen4 x 8 lanes. 8GB HBM on board are accessible with a memory bandwidth of 316GB/s.

The specified application SMV processing benefits from the adaptability of the board function with programmable logic. This is true in particular as described below:

- **Parallel processing:** Dedicate SMV processor functions scale with multiple instantiations
- **High bandwidth network interfaces:** Data can be transmitted and received directly without the need to go through an external host processor.
- **Customization for application-specific network protocols:** For IEC 61850 HSR and PRP are high availability network protocols that benefit from programmable logic.

The existence of this card enables a more cost-efficient network architecture by collapsing compute functions into one place.

The SMVsubscriber IP can be implemented in these kind of accelerator cards. Additionally, these boards provide high-speed networking interfaces that would provide a comprehensive solution for these applications as shown in Figure 3. Each IP instance accommodates a net Ethernet throughput of 1 Gbps supporting 128 SMV streams using the maximum precision. For a regular on-site location with 10G networking capabilities, if a single 10G link were attached to the card, it would provide a workload for 10 IP instances running in parallel.

This combination gives support for the processing of 1.280 SMV streams. This quantity could be doubled if the second network interface of the card were used following the same approach. The networking capabilities of these acceleration cards goes beyond

Figure 4: High level application for analysis of SMV streams.

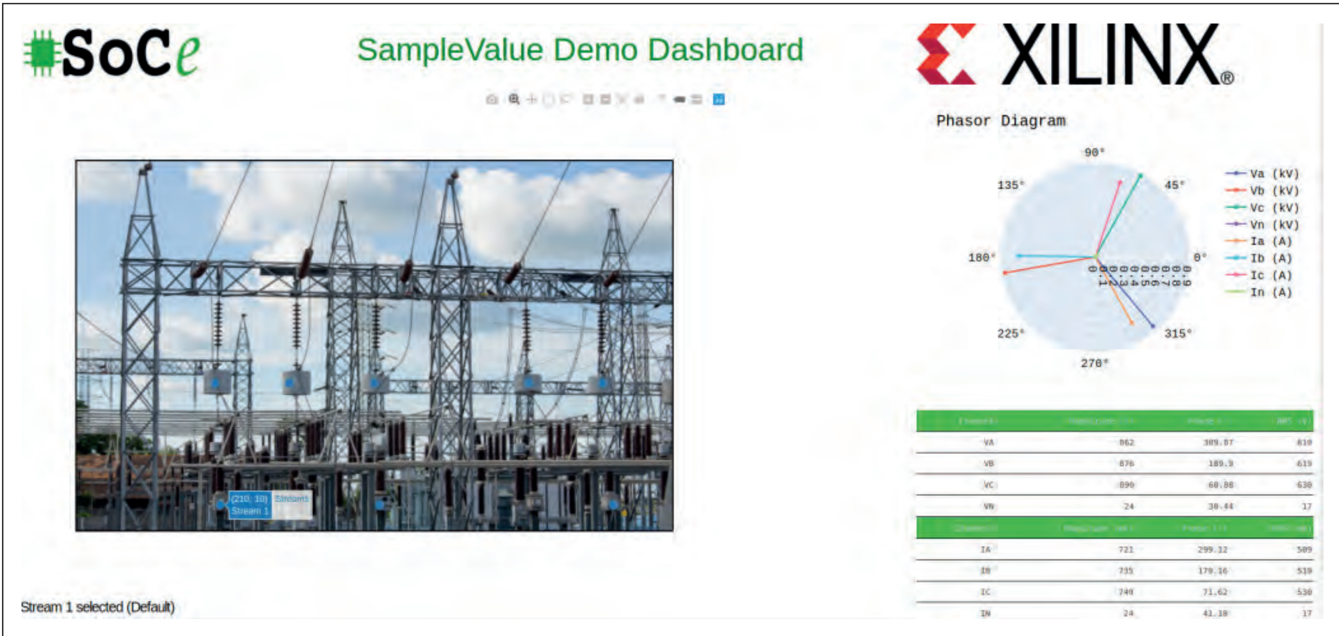


Figure 5: SMV Subscriber Accelerator application over Alveo in a dedicated PCIe expansion chassis.

10G, supporting 100G links. Therefore, the scalability of the solution is feasible by selecting card models with higher FPGA capabilities.

In order to benefit from accelerated computation in on-premises servers or in the Cloud, a high-speed networking backbone is required. Alveo U50 supports 10G and 100G Ethernet speeds. Currently, IT operators and infrastructure suppliers offer these options to the utilities. Therefore, the availability of this connectivity in the Smart Grid will limit or enable the proliferation of new applications based on the massive and real-time processing of the status of the Grid.

Thanks to the reconfigurability of the technology implemented on Xilinx Alveo, combined with the network capabilities of the card, it is feasible to support not only legacy networking but also high-availability and deterministic Ethernet. As an example, zero-delay recovery time protocols, Parallel Redundancy Protocol (PRP, IEC 62439-3-Clause 4) and high-availability seamless redundancy (HSR, IEC 62439-3-Clause 5) are used in modern digital power substations to communicate GOOSE and SMV values. Additionally, time-sensitive networking -TSN- [TSN20] – new generation Ethernet with support for real-time traffic, is also considered in the sector. All these specific protocols are integral on Alveo FPGA via IPs [HSRPRPSOCEIP, TSNSOCEIP].

With a single acceleration card, 16 smart-grid locations, e.g. DERs, could be served, assuming an estimation of 80 real-time measuring points for each premise done in the introduction. Figure 4 and Figure 5 (respectively) show a monitoring tool developed for SMV monitoring purposes and the Alveo setup running SMV subscriber accelerator application on a dedicated high-bandwidth PCIe expansion system in Bilbao (Spain).

The accelerator card model used in this setup is the Xilinx Alveo U50. It provides PCIe Gen4 to a host processor and also local Ethernet ports for 4x10 Gbit/s, 4x25 Gbit/s or 1x100 Gbit/s through QSFP28. 8 GB HBM is on board. It comes with a standard single slot PCIe card with a power consumption of 75 W maximum and passive cooling.

Conclusion

The digitization of the grid is a continuous process, both for operational and for user networks. Specifically, the Ethernet broadcasting of current and voltage values for control and protection applications is a reality on the newest digital power substations. New DER systems and power quality assessment applications demand technologies to process in real-time a large volume of these streams.

This article has presented an innovative solution to accelerate the computation of hundreds of SMV streams combining a silicon IP and a new generation FPGA based accelerator card. Specifically, SoC-e SMVsubscriber and 10G MES IPs have been implemented on a Xilinx U50 acceleration card in a pilot setup located in Bilbao (Spain).

This solution uncovers the complexity of the SMV processing and offers a high-level interface for the application designers.

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STEAG SENS seeks to grow UK PV market & global opportunities

The STEAG Solar Energy Solutions division of STEAG Energy Services GmbH has been a part of the UK photovoltaic (PV) energy market since the 2019 approval of its Gildemeister Energy Services acquisition. While STEAG many not yet be a familiar UK brand, the Germany-based company with its diversified portfolio stretching across five continents is built around the idea of transitioning from fossil fueled generation to a portfolio encompassing PV, thermal, wind, coal and gas. Put simply: STEAG intends to be a leader within a diversified, global energy future that centers on renewables.

BY ANDRÉ KREMER, STEAG SENS UK MANAGING DIRECTOR

IF GREENHOUSE GASES are the arch enemy of a healthy planetary ecosystem, STEAG Energy Services GmbH seeks to deal a death blow to its foe. Yet like many energy companies with decades-long histories, STEAG has a mixed portfolio of generation facilities across Europe comprising traditional fossil-fueled plants and an ever-growing mix of renewables including photovoltaic (PV), thermal, wind, gas and load leveling energy storage.

STEAG has been successfully growing its portfolio of owned and managed energy properties across five continents for more than a decade, expanding into UK markets with the acquisition of Gildemeister

Energy Services (GES) that was finalized in 2019. While its UK portfolio is small compared to the overall balance of owned and managed properties, STEAG Solar Energy Solutions (STEAG SENS,) is a company that is changing the idea of what a centralized energy provider is in the 21st century. Rather than fight the transition away from fossil fuels, STEAG has embraced change and sees ample economic opportunity in transforming the way that Europe and many other parts of the world generates, stores and uses its electrical energy.

(Publication name) technical editor Mark Andrews recently spoke with STEAG SENS UK Managing Director, André Kremer, about the company's diverse portfolio, ongoing expansion and approach to a market that offers both great opportunities and challenges akin to the original electrification of society that has been an ongoing global 'project' since the early 1900s.

Today's energy market – 120 years in the making, is still centered on fossil fuels, but set to transform into a mix of technologies with an emphasis on low- to no-carbon. Most EU / UK regions plan on renewables taking a 50 percent or greater share of energy production by 2050. Although the global COVID-19 pandemic made 2020 a year like none other, the promise of vaccines, treatments and a gradual return to 'business-as-usual' awaits on the horizon. Realizing its plans amidst these challenging times remains what could be described as a moving target.

Q: STEAG has been growing its portfolio while it diversifies its assets. Can you provide insights into the company's goals and how a diversified portfolio meets consumer needs as well as corporate objectives?

A: STEAG has been following a growth strategy in the renewable energy segment for quite some time. Wind, CHPs, mine gas and storage technology have been part of their portfolio in the past. However, there has been a lack of know-how in the solar sector. Through the acquisition of the former GILDEMEISTER energy solutions (GES), the transformation of STEAG into a global player in the field of renewables will be accelerated. The takeover of GES by STEAG was a transaction desired by all parties. DMG Mori, the former (GES) shareholder and leader in the machine tool industry, could not continue to serve the growth and related requirements.

The focus is simply different. STEAG wants to grow in the solar market and was fortunately able to acquire an international team of experts (by) investing in GES. Today, SENS wins multiple times. We have been given the freedom and support to further accelerate our enormous growth and can now offer our customers the entire product range of the STEAG Group. In addition to wind, storage and PPAs, this will also include hydrogen in the future.

The focus is simply different. STEAG wants to grow in the solar market and was fortunately able to acquire an international team of experts (by) investing in GES. Today, SENS wins multiple times. We have been given the freedom and support to further accelerate our enormous growth and can now offer our customers the entire product range of the STEAG Group

Q: Was the acquisition of GES mostly driven by their existing portfolio, or, more of a belief that growing solar and other renewable assets in the UK, Ireland and elsewhere represented the future of electric utility growth?

A: STEAG has already been successfully active for some time in growth areas, such as renewables, beyond its previous core business and they will become more and more important in the future. Therefore, it was an investment in a growing market but also an investment in its own transformation. STEAG is going greener and is strengthening its position in the international market of renewable energies. The takeover has strategically strengthened the service portfolio, particularly in the area of the megatrend of photovoltaics. With the extensive know-how and the international network of SENS, STEAG has taken a big step towards a green future.

Q: Can you share insights concerning STEAG's plans for the UK, Ireland and elsewhere? Also – what strengths does STEAG SENS bring to its markets?

A: SENS has a clear target to develop >500MWp in UK and Ireland by end of 2022. For the rest of Europe we are looking at a Pipeline of >3GW. We would like to bring a minimum of 50% to grid connection in the same period.

Our long-term international experience and our worldwide network of partners allows us to operate efficiently, reliably and flexibly. However, what sets us apart from our competitors is our passion and the

joy we feel for our customers' success. We develop innovative solutions on the sunny side of the energy transition and with the greatest commitment.

Q: Could you please highlight key challenges/ opportunities as you see them in the UK and across Europe?

A: Beside the consequences of COVID-19 the enormous growth of renewable energies will be both an opportunity and a risk. Areas will become scarcer, the impact on the grid will increase, more and more solar energy will be fed into the grid at the same time and the steadily decreasing LCOEs will accelerate this effect.

This will lead to cannibalisation effects in many countries, which will have a negative impact on the economic efficiency of the plants. This, in turn, opens up new opportunities for storage projects. Within STEAG, we are extremely well positioned and prepared for all developments. We are motivated and look forward to the upcoming projects and the coming years.

Q: Transforming the way the world generates electricity can be seen as a daunting task. Was there anything in particular that triggered the GES acquisition at this point in time or 'now' relatively speaking?

A: 'Now' is probably not quite right – As mentioned, STEAG has been active in the field of renewable energies for a long time. The pressure due to the approaching coal phase-out is increasing, so that STEAG is undergoing a complete cultural change and is focusing more than ever on renewable energies. In addition to wind, this now also includes solar energy.

Q: Is the development of SENS part of a larger strategy that you wish to discuss?

A: Absolutely. Wind and solar are still the central drivers and most important cornerstones of the energy transition. Since STEAG SENS has experience and project developments on all five continents, the international expansion of the solar division is an essential part of STEAG's corporate strategy.

Q: The UK and Ireland have lower PV penetration rates than other countries in the region – Is the STEAG SENS value proposition a new reason why more homes, businesses and communities should 'Go Solar' in these regions?

A: This would of course be a desirable outcome. STEAG SENS makes it easier for companies, municipalities and institutional investors to enter the renewable energy supply market. We know that our partners particularly appreciate the personal, individual support provided by SENS and the security we give them. Europe and the world are heading for economically uncertain times, intensified by the COVID-19 crisis. We help our partners to make a balanced, but above all secure investment that suits their needs. These needs are naturally different for commercial and industrial clients than for investment funds, of course. It is more important to find an individual solution for each customer. So yes, we give customers in the UK and Ireland a new reason to invest in PV.

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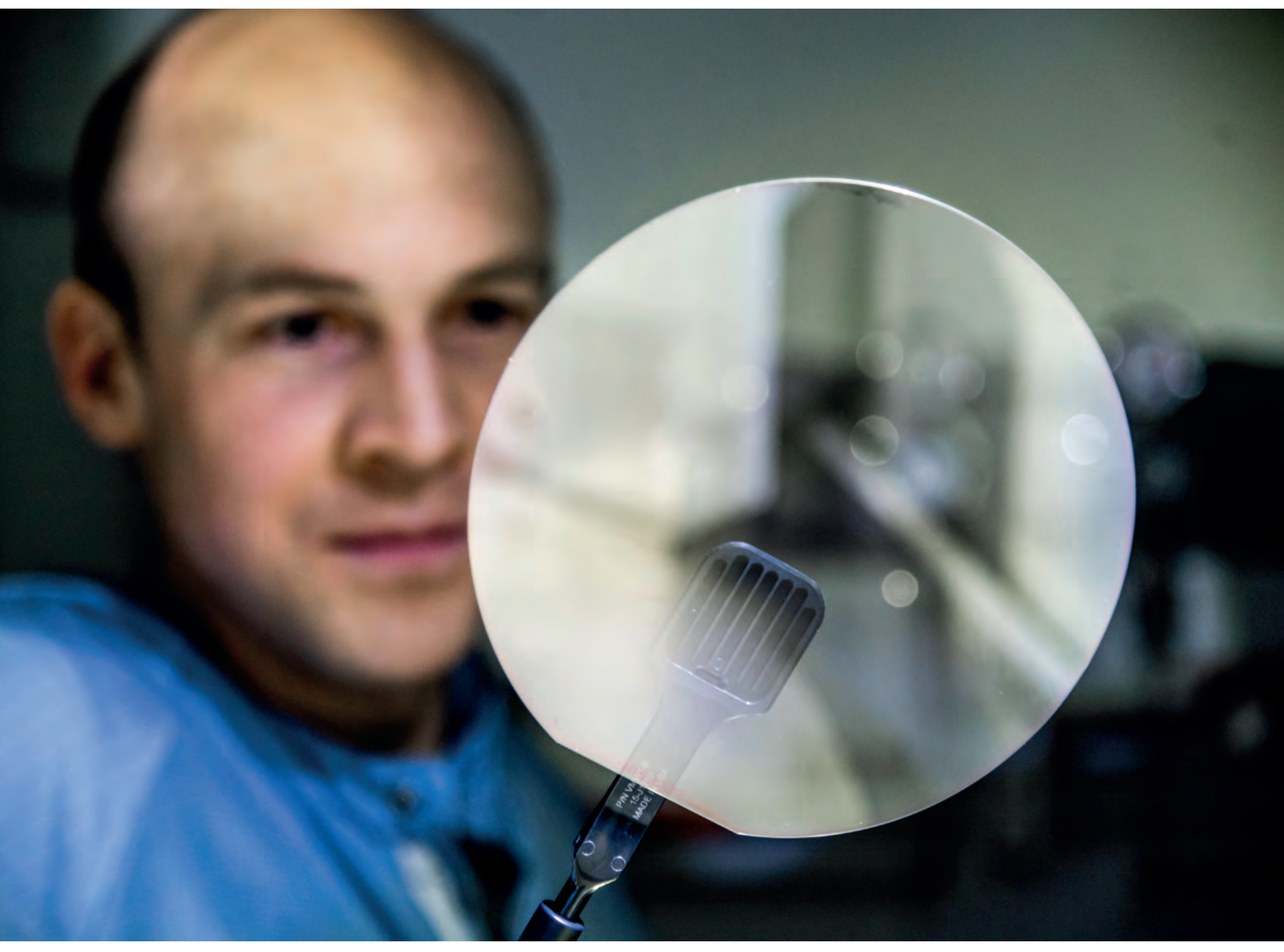

Banishing the buffer

Buffer-free GaN-on-SiC epiwafers enable cost-competitive, higher performance power devices

BY JR-TAI CHEN FROM SWEGAN AB

2020 is the year of the GaN power device. Following several decades of intensive research and development in both materials and devices, GaN-on-silicon HEMTs are starting to make inroads into the mainstream consumer market. One example is the shipment of more than one million units of ultra-fast portable GaN chargers for mobile phones.

While these substantial orders are a triumph, there is an opportunity for significant further improvement. GaN-on-silicon HEMTs are failing to operate close to electric field strengths promised by this wide bandgap material, and that shortfall is holding back performance on many fronts, including operating voltages, device miniaturisation and on-resistance, which has the potential to fall by an order of magnitude. The good news is that such progress is within the grasp of the entire power electronics industry. All that is needed is to move to a recently developed, buffer-free GaN-on-SiC material known as QuanFINE, which has been developed by our team at SweGaN AB in Linköping, Sweden.

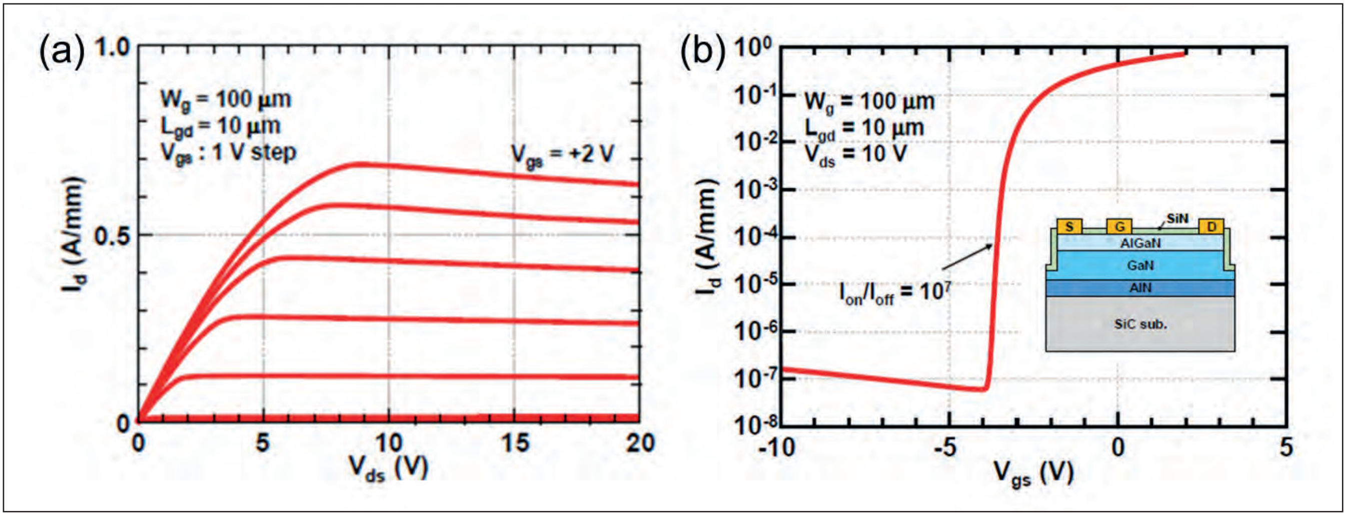

Figure 1. (a) DC plots of the drain current as a function of drain-source voltage (a) and gate-source voltage (b) for a power HEMT produced with SweGaN's buffer-free GaN-on-SiC technology.

We have been developing this material for several years. Back in 2018, we demonstrated the world's first high-quality, high-performance, buffer-free GaN-on-SiC HEMT. This features a revolutionary epitaxial stack, which is free from the conventional thick carbon-doped buffers that are used in high-voltage GaN-on-silicon based HEMTs – and also, for that matter, GaN-on-SiC HEMTs used for RF applications. By removing the buffer that is at least 5 µm thick and a drift layer of comparable thickness, device production costs fall and reactor up-time increases, thanks to a reduced cleaning frequency for the MOCVD chamber.

Armed with our technology, the total epitaxial layer thickness of GaN-on-SiC heterostructures is below 350 nm, a feat accomplished without any compromise in material properties. At the heart of our buffer-free, GaN-on-SiC heterostructure is a completely new growth mechanism: transmorphic heteroepitaxy. Its distinctive feature is that there is no abrupt change in either the composition or the atomic configuration at the material interface. Instead, there is a gradual transition from one to the other over a nanometre, occurring via vacancy ordering.

The success of our material hinges on its capability to withstand a high electrical breakdown field. According to theory, the critical breakdown field of GaN is approximately 3 MV/cm. We are not far from that upper limit, with a recent study based on a two-terminal lateral breakdown test showing our material can handle close to 2 MV/cm. That figure, obtained on a structure featuring a 200 nm-thick GaN channel layer, a 60 nm AlN nucleation layer and no field plates, is far higher than that for GaN-on-silicon devices with a carbon-doped buffer – for that class of HEMT, even with the benefit of field plates, the breakdown electrical field is typically 0.6-0.7 MV/cm.

Device testing

To further explore the potential of our buffer-free technology for power applications, we have collaborated with the research group at the University of Fukui, Japan, led by Masaaki Kuzuhara and Joel Asubar. This team, which has been developing techniques to increase the breakdown strength of GaN HEMTs for many years, have previously used low-dislocation-density, iron-doped GaN substrates to propel the breakdown field to 1 MV/cm. These devices reach a breakdown voltage of 5 kV.

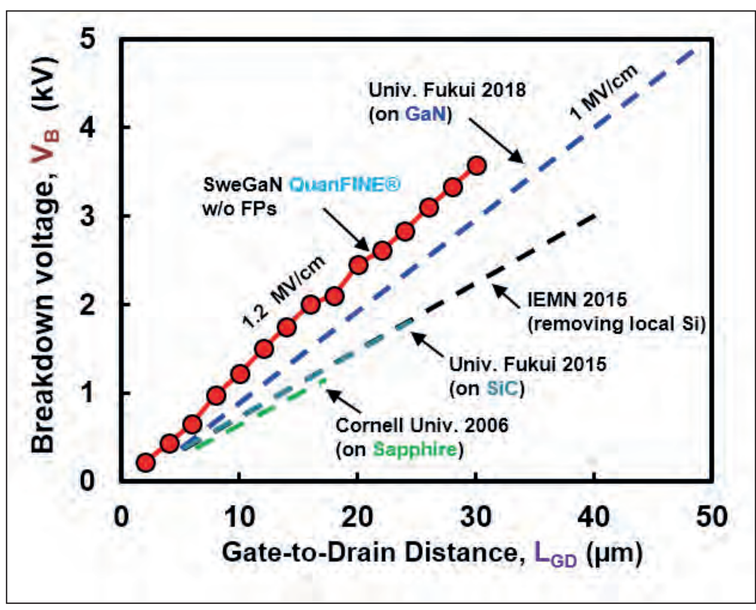

Figure 2. Benchmarking the breakdown voltage at different gate-to-drain distances for GaN HEMT power devices based on different epitaxial growths. Some data comes from J, Asubar *et al*. "Pushing the GaN HEMT Towards Its Theoretical Limit," Compound Semiconductor, October 2016, pp. 26-31. In addition, there are results associated with a buffer-free epiwafer measured in this work.

	Without field plates (FPs)		With FPs	
	E_C	V_B (@ L_{GD}=20 µm)	E_C	V_B (@ L_{GD}=20 µm)
GaN-on-Si (Commercial)	0.3 MV/cm	600 V	0.7 MV/cm	1400 V
QuanFINE®	1.2 MV/cm	2400 V	to be measured	to be measured

Table. 1. A comparison of the critical electric field strength, E_c, and the breakdown voltage (V_B) for commercial GaN-on-silicon epiwafers and those made by SweGaN, featuring buffer-free technology. Measurements are reported for devices with and without field plates. Note that field plates are commonly used in GaN HEMTs to enhance breakdown voltage. In most cases field plates enhance the magnitude of the electric field strength and the breakdown voltage more than two-fold.

Our collaborative effort has involved undertaking breakdown tests on buffer-free HEMTs that have a nominal 25 nm $Al_{0.25}Ga_{0.75}N$ barrier and a 250 nm GaN channel layer. These transistors, fabricated using standard technology developed by the University of Fukui, have a 3 µm gate length, a gate-to-source spacing of 3 µm, a 200 nm mesa isolation depth and a SiN passivation layer 150 nm-thick (see the inset of Fig. 1(b) for details of the device configuration).

DC current-voltage measurements on these buffer-free HEMTs reveal that they have a reasonable current density (see Figure 1(a)) and a remarkably low leakage current (see Figure 2(b)) that leads to an I_{on}/I_{off} ratio of 10^7. Note that the entire epitaxial structure is unintentionally doped. The low leakage current is testament to the high-quality, ultra-wide bandgap AlN nucleation layer that provides a back barrier.

Breakdown tests on a range of our devices, with gate-to-drain distances varying from 0.2 µm to 30 µm, have enabled benchmarking of the critical field strength with state-of-the-art values for GaN grown on different substrates (see Figure 2). As one would expect, the breakdown voltage of our HEMTs increases in a linear manner with the gate-to-drain distance, reaching 3.6 kV at a distance of 30 µm. This translates to a field strength of 1.2 MV/cm, a value higher than that for GaN HEMTs grown on native substrates. Such an impressive result validates the high structural quality of our buffer-free epiwafers, and the effectiveness of using an AlN nucleation layer and a semi-insulating SiC substrate to block high voltages.

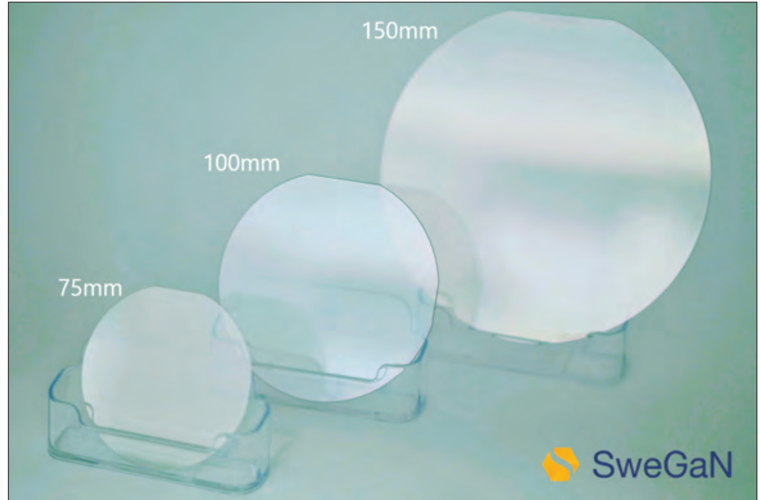

Figure 3. SweGaN's product portfolio of buffer-free GaN-on-SiC epiwafers.

Eagle-eyed readers will have spotted that the breakdown field strength for our HEMTs is lower than that recorded for the two-terminal measurement. This discrepancy might result from differences in the methods used to create device isolation. For the two-terminal measurement, a nitrogen ion-implantation provided isolation; and for the HEMTs this resulted from the mesa. We are planning an additional investigation, targeting further optimisation of our buffer-free HEMTs, so that they offer a better breakdown performance.

To put our value for field strength in perspective, the figure of 1.2 MV/cm is four times that for equivalent, commercial, field-plate-free GaN-on-silicon HEMTs (see Table 1). These results show that our buffer-free technology has the potential to reach a lateral breakdown voltage of about 5 kV with standard GaN power device designs.

Another opportunity that is created with our technology is to shrink device dimensions while retaining the voltage rating of commercial GaN-on-silicon devices. For example, by switching from GaN-on-silicon material to our buffer-free technology, it is possible to trim the gate-to-drain spacing in 600 V GaN power devices without field plates from 20 µm to 5 µm. This miniaturisation would result in a significantly reduced power loss. According Baliga's figure-of-merit, on-resistance is inversely proportional

to the cube of the critical electric field strength, so a HEMT made with our technology should exhibit an on-resistance that is 1/64th that for an equivalent GaN-on-silicon device with the same voltage rating.

Building on these benchmark results, and in preparation to enter the GaN power market, we have expanded our portfolio of products from 75 mm and 100 mm epiwafers to include those with a 150 mm diameter. Progress with the latter has led to a highly uniform growth process, and deliveries of this new product to customers in the first quarter of this year.

As we grow our business, we are well-positioned to benefit from steadily increasing in orders within the power industry for 150 mm semi-insulating SiC substrates, and the increasing volume by suppliers meeting this demand. The price of 150 mm semi-insulating SiC is expected to fall, aligning with the price of 150 mm *n*-type SiC wafers. This will enable our technology to become even more competitive.

We are targeting the markets where device performance and reliability are the top priorities for customers and end users. As volumes increases for wide bandgap power electronics, material costs will naturally fall through economies of scale, creating a vast opportunity for our buffer-free technology in the cost-sensitive power market.

Our technology is also destined to enjoy success in the RF device industry. It has already attracted the attention of the majority of GaN RF foundries worldwide, and we expect that it will not be long before it is used in RF device production.

The ECSEL Joint Undertaking (JU) under grant agreement No 826392, UltimateGaN.

Further reading

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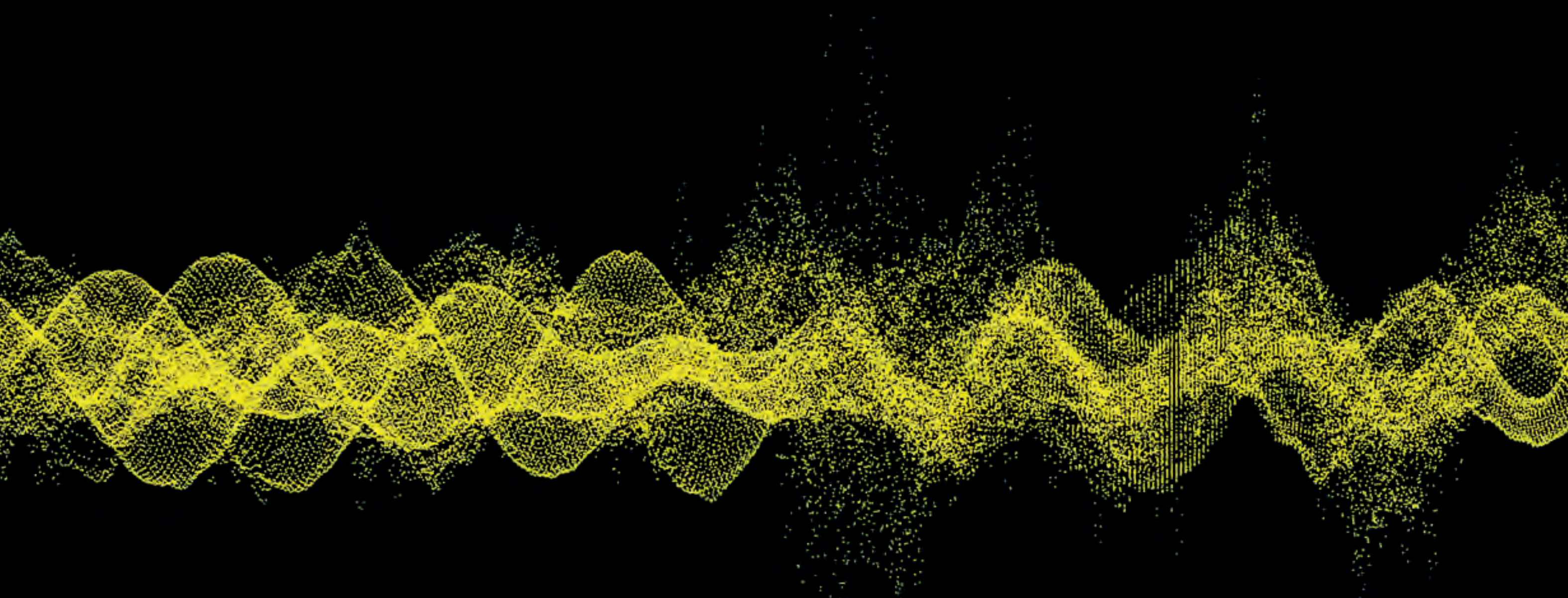


IGBT modules interrogated acoustically

IGBT failures, because of the typically high voltage and power levels, can be both costly and dangerous. It makes sense to find internal structural defects be-fore they have an opportunity to go wrong.

BY TOM ADAMS, CONSULTANT, NORDSON SONOSCAN

A GROUP of three small air voids is trapped in the solder that bonds an IGBT module to its heat sink. The voids happen to lie close enough to each other to prevent some of the heat from escaping cleanly from the area of the die just above them. Over time, the area above the voids may overheat and the die may fail electrically - and along with it the system it is part of.

IGBT failures, because of the typically high voltage and power levels, can be both costly and dangerous. It makes sense to find internal structural defects before they have an opportunity to go wrong.

X-ray and ultrasound can both perform the nondestructive imaging that is needed, but with some differences. The first is penetration. X-ray may not ade-quately penetrate the heat sink on some IGBT modules, to deliver its data. The X-ray beam reports local differences in attenuation, and the most frequent de-fects in IGBTs are air gaps and non-bonds.

If the gaps are relatively thick, such as a void in solder, imaging may succeed, but if they are very thin, as in a non-bonded area, they may remain invisible because their impact on the beam's at-tenuation is too slight.

An Acoustic Micro Imaging tool such as a C-SAM® tool from Nordson SONOSCAN can readily penetrate the heat sink, but first it needs to solve an-other problem: the small water column that on other components couples the tool's transducer to the top

of the component cannot be used on the top surface of an unencapsulated IGBT module. Impure water coming in contact with the face of the module could invariably leave some residue from evaporation, and the IGBT's voltage level is so high that the residue could become a con-ductive pathway, with disastrous consequences. IGBT modules area one the few comps types the only component type having this limitation.

For this reason an inverted acoustic micro imaging tool was developed in order to image IGBTs from below, through the heat sink. The transducer and its wa-ter column both point upward at their station below the module, whose top surface remains dry. Because the bottom side of an IGBT module not covered by encapsulant, the modules can be imaged even after encapsulation.

As the tool's transducer scans back and forth along the bottom surface of the heat sink, it carries out its pulse-echo function at individual x-y locations tens of thousands of times per second, and contributes one pixel for the acoustic image with each pulse. The sequence is this:

- the transducer launches a pulse upward into the column of water.
- the pulse strikes the water-to-heat sink interface, and is in part reflected back to the transducer and in part transmitted upward into the module.
- the reflected echo reports, among other things, the distance from the transducer to the surface of the heat sink at the bottom of the module
- the transmitted portion travels through the heat sink and reaches the interface between the heat sink and the solder
- the heat sink-solder echo is reflected to the transducer, where it reports the distance and other data about the interface.

The process will continue upward through additional material interfaces until the pulse reaches the attachment of the die to the raft. But before it reaches the raft, it will report any unintended features it encounters in the solder. The unintended features consist almost entirely of air gaps, which may take the form of air bubbles in the solder or flat delaminations between two solid materials. This is when the three voids mentioned in the first paragraph would be imaged, and their distance from the heat sink surface recorded.

The air bubbles are actually the most imageable features in the module, because instead of presenting a solid-to-solid interface, they present a solid-to-gas (air) interface, which reflects more ultrasound (nearly 100%) back to the transducer than any other type of interface. Solid-to-solid interfaces tend to reflect 10 to 50 percent of the energy in an arriving pulse. No ultrasound penetrates the solid-to-air interface, so x-y locations lying directly beyond it will not be imaged. You can see these effects at work in the monochrome acoustic image in Figure 1. To make this image, ultrasound was pulsed upward through the heat sink, the solder, the raft, and the die attach material, and returned to the transducer by the same route.

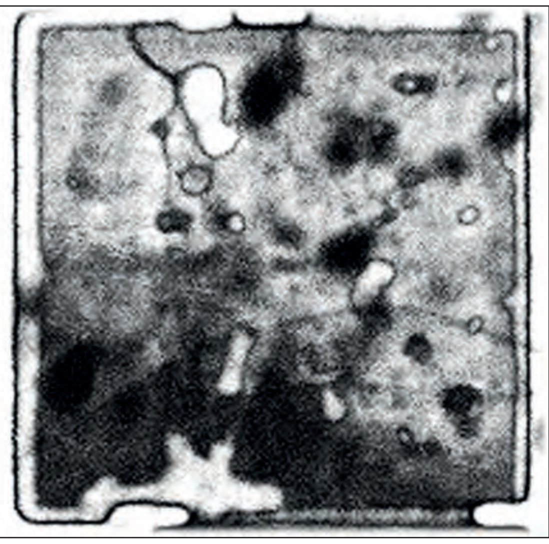


Figure 1. Monochrome acoustic image made by scanning through bottom of module shows defects in one die attach.

The rounded white feature near the upper left is an air-filled void in the layer bonding this chip to the ceramic raft in the module. There is another large void near the lower left, and several smaller ones.

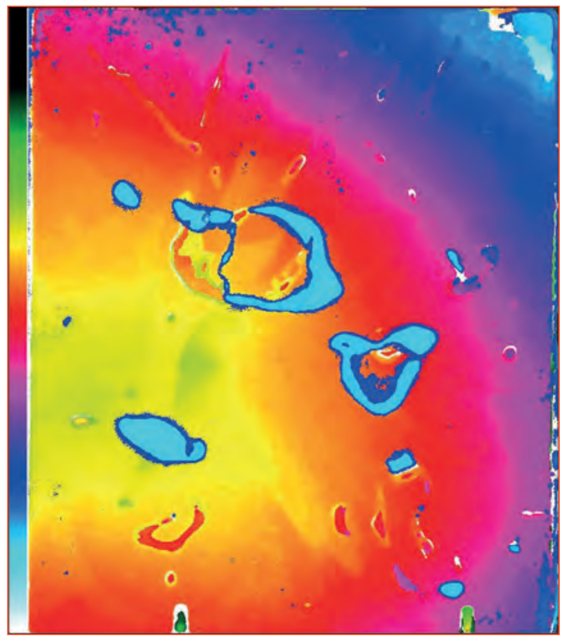
This image was made by using a 'gate.' Since the pulse was launched three ma-terial layers below, to make the desired image the receiver needs to select only the echoes from the small slice of time during which echoes were reflected by this die.

At each x-y location, the transducer's receiver waits after a pulse is launched until at precisely the right nanosecond after launch it is activated to accept whatever arrives from the gated depth - anything from no echo to, as here, the strongest possible echo. Probably thousands of 'strongest possible' echoes arrived at the receiver to make the x-y shape of this void appear white. Weaker echoes produce gray. No echo at all yields black.

There seem to be a few cracks in this die, visible as dark lines; one reaches the void at upper left. The indistinct black features mostly on the right half of the die are voids in the solder layer, which is closer to the transducer. They are above the gate set for the die that is being imaged. They are black because they are shadows from voids above the gate.

Being voids, and filled with air, they sent back their own echoes when the pulses coming from the transducer struck them, but their own echoes arrived at the transducer too early to be within the collecting gate and were ignored. But by preventing pulses from reaching the die, they sent their own acoustic shad-ows to the transducer. One might also explain the same phenomenon by saying that during the brief moment when the transducer was receiving echoes

Figure 2. Light blue features are closest to heat sink, pale green are farthest above.

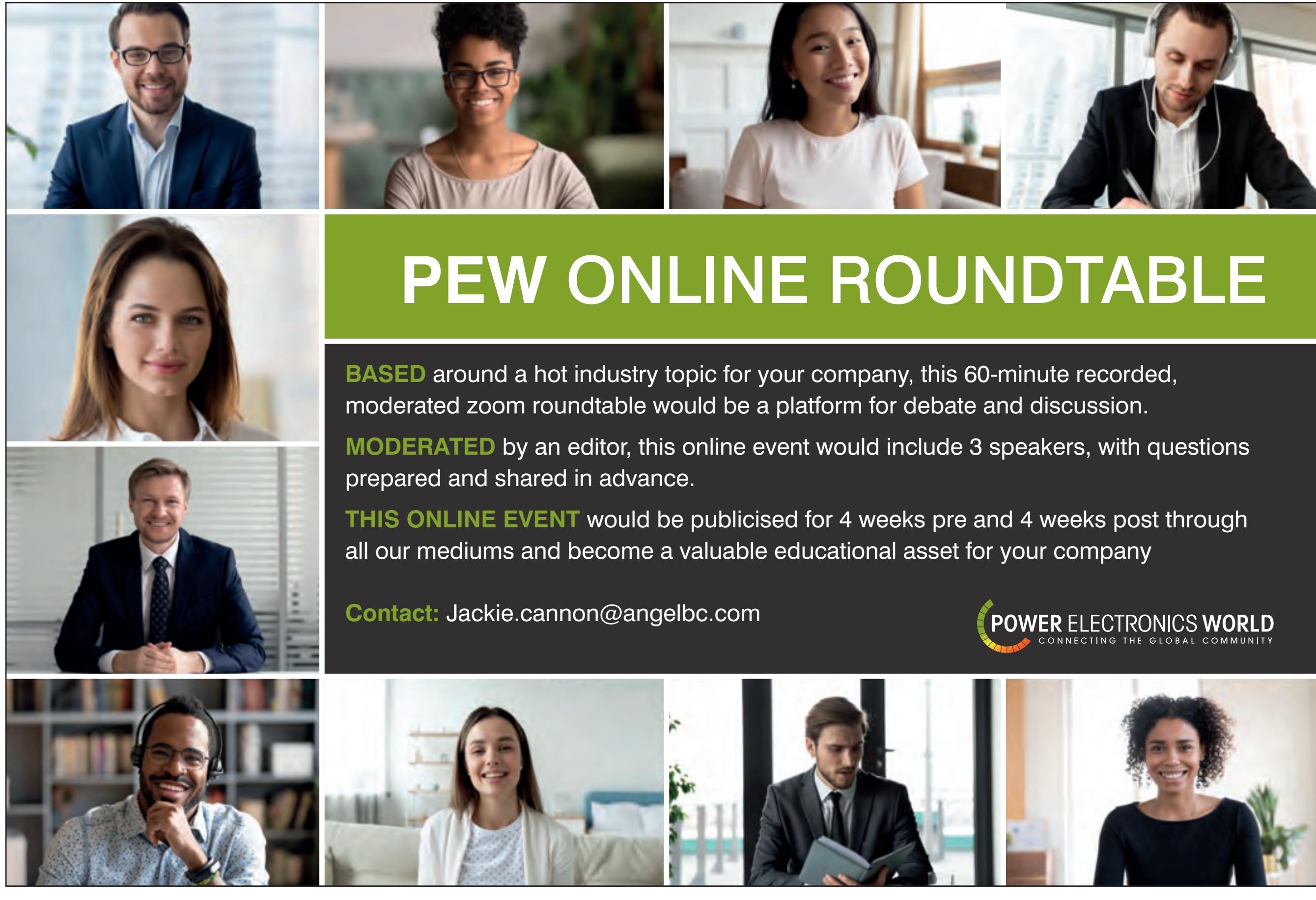


from the die attach, the areas beyond these voids had nothing too contribute.

Figure 2 is the acoustic image of the raft surface on one of the die on a IGBT. The colors here are reporting the vertical distance of the solder-filled space between the raft and heat sink surfaces. This figure extends vertically through the whole thickness of the solder. The raft is deepest in small areas at left center (pale green in color map at left) and highest at upper right (pale blue in color map), where there is so little solder that the raft surface probably comes close to touching the heat sink.

The key features here are the non-uniform thickness of the solder and the numerous heat-blocking voids, some of which are quite large. Collectively they may be capable of causing a region of the die just above to overheat and fail. Those voids that are light blue are likely in contact with the heat sink. But note that part of the upper right corner is the same color, because the solder in this region is very thin.

The large blue C-shaped void near the center lies above an-other large void that lies in the red-yellow depth. Non-uniform solder layers may lead to uneven heat dissipation and therefore unwanted stress. Non-uniform solder layers may lead to uneven heat dissipation and thus unwanted stress.Neither of the IGBT modules shown here would be candidates for incorporation into a product: they are simply too filled with anomalies. But in these high-power modules even a single small anomaly could lead to failure if the modules are being used close to their design specifications.



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From wearables to 'careables':
Closing the loop in connected health

What if we could combine vital sign sensing capabilities with smart algorithms and actuation features in order to not only diagnose but also 'fix' a problem in the body? Just like a pacemaker does today, a multitude of closed-loop systems will help us in the future. **Vojkan Mihajlovic, senior researcher, and Evelien Hermeling, principal scientist at imec**, share their vision on how closed-loop systems, consisting of wearables, implantables, invisibles and smart algorithms, will transform healthcare.

THE BEST-KNOWN EXAMPLE of an autonomous and closed-loop therapy device is a pacemaker. Second in line, although not yet commercially available, are intelligent insulin pumps. With artificial intelligence, and miniaturized sensors and actuators, the ingredients are there to shape a future with a multitude of closed-loop systems for remote, preventive and curative healthcare.

Think of medical-grade wearables measuring blood pressure and assisting in finding the right dose of blood pressure-regulating medicine. Think of small implants that stimulate specific nerves based on biomarkers for migraine sensed in real time. Or think of invisibly integrated sensors in (car) seats and office chairs to access the breathing capacity of lung patients and advise them on their fitness program.

Key building blocks of a closed-loop therapy system. The dark blue circles are typically hardware components, while the white-colored blocks are mainly software modules.

From pacemakers to anesthesia

If you Google 'closed loop in healthcare' you immediately get thousands of hits on the artificial pancreas. **Evelien Hermeling:** "In fact, the evolution of diabetes care is ideal to illustrate what a closed-loop therapy system is. Patients moved from finger pricks and insulin pens to glucose monitors on their abdomen or upper arm that measure continuously and send alarms to their cellphones."

"More advanced systems today (such as the Minimed 670G Insulin Pump System of Medtronic) go one step further and add a small wearable computer to the continuous glucose monitor. That computer captures the data, calculates how much insulin is needed and sends this info to the insulin pump that is also attached to the patient's abdomen. In this way, blood sugar remains steady day and night, automatically. That vision is pursued for other diseases as well to make the lives of patients healthier and more comfortable. The artificial kidney for dialysis patients is another typical example, although still far in the future. Imec, together with leading research organizations in the field, has and will continue to work on a roadmap to make such an artificial kidney a reality."

It is also forecasted that for other chronic or acute conditions, next-generation treatments will no longer

be restricted to chemical medications alone. Doctors might soon be able to prescribe drug treatments in combination with devices that monitor the effect of the drug or suggest changes in its dosage (medically known as titration process). These kinds of treatments are known as drug-device combinations.

Vojkan Mihajlovic: "Also for doctors, closed-loop systems are there to make life easier. Think of a closed-loop system for anesthesia: the anesthesiologist sets a target blood pressure and the system automatically maintains this target by dosing the appropriate medication. This allows specialists to focus on the patient and relieves them from repetitive, automatable tasks."

Compose your future closed-loop therapy system

With the advent of miniaturized, wireless, reliable sensor and actuator systems, and artificial intelligence for interpretation of the data, the time has come to fully invest – both money and brains – in new systems that are smarter and more autonomous when it comes to keeping an eye on patient's health.

Closed-loop therapy devices can take on many forms. Think for example of medical-grade wearables measuring blood pressure and assisting in finding the right dose of blood pressure-regulating medicine.

Evelien Hermeling: "A typical closed-loop system is made up of different key parts, each with its specific requirements. The sensing part measures one or more parameters of the patient's body, such as heart rate, ECG, blood pressure etc. Sensors must be accurate, small, and able to wirelessly transmit their data to the cloud or a device in the patient's vicinity."

"Next, a small processing unit is needed, executing algorithms that can interpret these sensor data into actionable insights. Depending on the use cases, time constraints need to be considered. For example, a heartbeat needs to be acted upon immediately (as with a pacemaker), while blood pressure is known to take time to change and here it is more important to watch a trend over a few hours or even days. Also, personalization is key. 50 beats/minute may be a normal resting heart rate for one person and an abnormally low heart rate for someone else. Algorithms need to add this kind of intelligence to the system so that useful and accurate actionable insights can be deducted from the sensor data. Next to time constraints and personalization, contextual and environmental parameters also need to be considered. Blood-pressure-lowering drugs, optimally titrated to a person for an average day, might cause the blood pressure to drop during hot weather. This can be a dangerous situation that needs to be corrected. Algorithms would be able to adjust the doses, taking such contextual and environmental parameters into account."

"A third building block is the control algorithm that translates the insights into a control action. For example, too much fluid buildup in the body can result in an increased medication dosage for a patient. Again, personalization and time constraints are key here. Imagine you are dealing with diuretics (pills to help increase urine volume), then the control algorithm should accommodate that the body needs some time to get rid of the excessive fluids. Delivering a medicine in the bloodstream will not immediately change the fluid status."

"And the last part is the actuator hardware, e.g. the micropump delivering a drug into the blood stream, based on the instructions it received from the control algorithm. A small form factor, and accurate and timely operation are the most important features of this building block."

These closed-loop therapy systems can have many different form factors: wearables, implantables, invisibles. As **Vojkan Mihajlovic** notes: "Invisibles are sensors that are seamlessly integrated into the patient's environment. Think of sensors in a (car) seat, a car's dashboard, a mattress or even a toilet seat. While wearables and implantables measure continuously, invisibles only measure occasionally, which is sufficient for certain types of measurements. Think for example of a daily check of blood pressure, urine composition or lung capacity."

Imec has all the building blocks in-house

Imec is known for its work on miniaturization of electronics, which is researched in state-of-the-art cleanrooms. **Evelien Hermeling:** "Some 15 years ago, work started on making sensing systems for vital sign monitoring. This work resulted in collaborations with industry leaders such as Samsung and Biotelemetry, in a large study on stress monitoring

Imec's EEG headset research platform with optical and electrical modalities to both measure and stimulate brain activity. Possible applications are treatment of depression, migraine, and epilepsy. Imec looks for partners to work out a system for specific applications.

in real-life conditions, and in different prototype devices for measuring brain waves, eye movements, gait, sleep patterns, respiration, pain and stress, and general health parameters."

"The focus has been on making very compact, low-power and wireless sensor systems, with efficient data acquisition, using different modalities (activities of the heart, lungs, muscles or nerves) and integrating them in different form factors (watch, patch, headset, ...) We are now working towards expanding the efficient acquisition portion, with smart algorithms to provide actionable insights, and actuation principles to close the loop."

"We invest a lot of work into algorithm development for good interpretation of the collected sensor data and to ensure reliable data quality in real-life conditions and in uncontrolled environments. Also, algorithms allow the fusion of all available sensor data, from different kinds of sensors, in order to draw even more reliable conclusions." In another imec article, "Inhale the future: bringing respiratory monitoring to the 21st century" the use of algorithms (signal-level, digital-biomarker level and application-level) is further explained.

Imec's phantom head. It can be used in the development of closed-loop EEG and tCS applications, before doing trials on humans.

Vojkan Mihajlovic: "In the domain of actuation and stimulation, imec explores the possibilities of non-invasive brain stimulation (with its EEG headset) and electrical stimulation of nerves with small implantable nodes. Also, we are developing a general-purpose software framework that facilitates multimodal data acquisition, signal interpretation and specification of control rules required for optimal actuation. This framework links all these ingredients into a true closed-loop system. The development currently focuses on timing requirements and feedback/ actuation modalities. Of course, imec looks for partners and users to complement this expertise, especially from the application side."

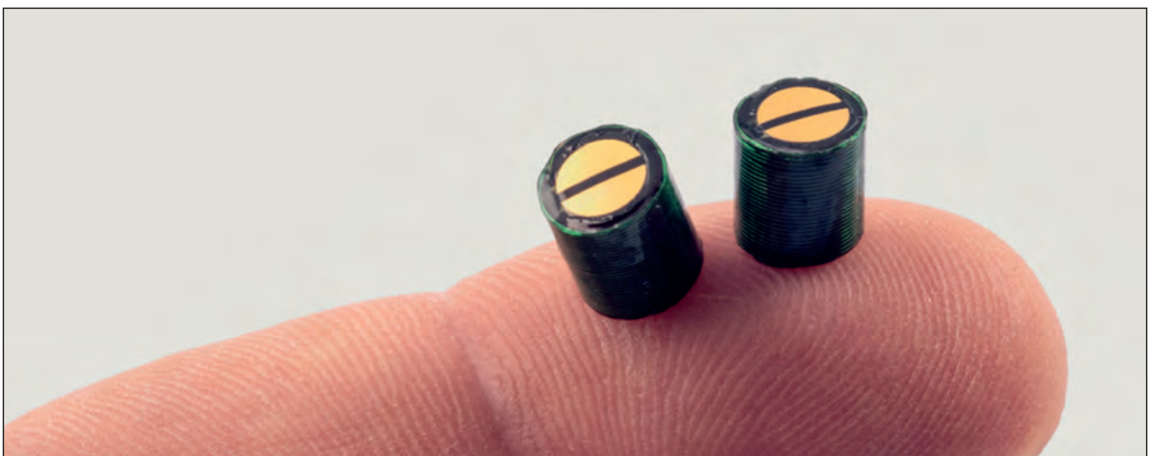
Below are 3 examples of work that imec has done over the years related to closed-loop systems. As said previously, closed-loop feedback systems can be embodied in multiple form factors, such as wearables, implantables and (non-contact) invisibles or combinations of these. For each of these form factors, we highlight one example. At imec, we specialize in using our knowledge and experience to solve customer-specific challenges, hence the following examples are meant as a source of inspiration. Each application requires different building blocks used in different manners.

A headset that combats depressions, migraines and more

Transcranial current stimulation (tCS) relies on injecting currents (a few mA) over the human scalp in order to modulate ongoing brain activity.
Vojkan Mihajlovic: "The applications for tCS are numerous, ranging from treatment of depression and migraine to epilepsy and anxiety disorders. In a closed-loop system, it is important to measure the brain waves while and after applying stimuli, such that the stimuli can be adapted to facilitate personalized treatment."

"Traditionally, the method involved two large electrodes placed at different locations on the scalp with current going from one electrode to the other. The electrodes were made of conductive polymer enclosed in a sponge-like housing, soaked in a saline solution. More recent approaches of tCS rely on a larger number of smaller (1 cm²) electrodes. Imec developed EEG monitoring headsets with small dry electrodes (together with Datwyler). They are very easy to use and deliver high-quality measurements. Currently, such dry electrodes are being adapted for tCS.

For this application, imec also plans to extend the headset's capabilities with digital active electrodes, with both electrical and optical features. By using



Examples of implantable node sensors

two different modalities, it becomes possible to simultaneously measure and stimulate without interferences (e.g. electrical stimulation, optical sensing and vice versa).

Imec developed a phantom head to facilitate the exploration of safety aspects and the impact of tCS on head tissue. Also, it allows to optimize closed-loop brain monitoring and stimulation. This phantom head is the electrical equivalent of a human head consisting of different head tissue layers. It enables probing the current paths at different surface locations and tissue depths. Tests done using brain monitoring and tCS systems applied on the phantom head, along with simulated EEG signals (generated by using signal generators), are a steppingstone to closed-loop EEG & tCS trials in humans.

Small implantable nodes that tickle your nerves

Next to wearables, implanted devices can also do sensing and actuation of vital sign parameters as part of a closed-loop therapy system. **Vojkan Mihajlovic:** "An important field, with an enormous potential, is bioelectronic medicine, in which the central or peripheral nervous system is electrically stimulated. Stimulation can be done in the brain region, the spinal cord, or the Vagus, hypoglossal, phrenic, sacral or tibial nerves."

"In the brain, microneedles are the preferred form factor whereas tiny stimulation nodes placed next to nerves or miniaturized cuff electrodes wrapped around the nerve bundles, can be used in the rest of the body. Imec develops both neuroprobes and small stimulation nodes. With both form factors, the focus is on miniaturization and wireless powering and communication."

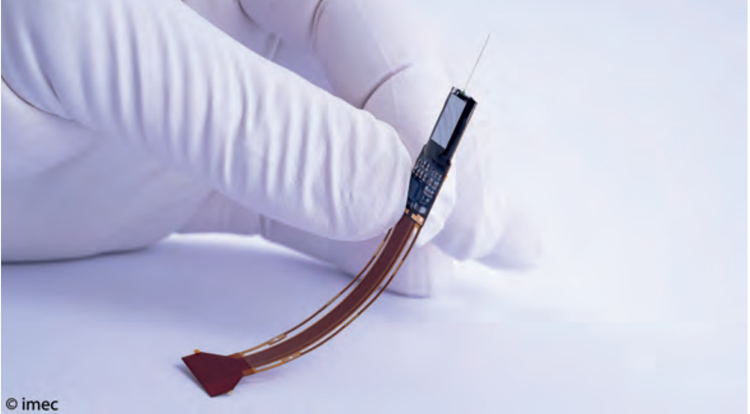
An important milestone in 2018 was the release of a neural microneedle probe, Neuropixels, to the global neuroscience research community. The probes were developed through an international collaboration funded by the Howard Hughes Medical Institute (HHMI), Wellcome Trust, Gatsby Charitable Foundation and Allen Institute for Brain Science and designed, developed and fabricated at imec, in collaboration with HHMI Janelia Research Campus, Allen Institute for Brain Science, and University College London.

The probes have almost a thousand electrodes and 384 recording channels on a single shank, providing an unprecedented resolution for mapping brain activity. Now, first steps are being taken in extending the Neuropixel platform towards stimulation.

Vojkan Mihajlovic: "Another example, with a different form factor, are the implantable stimulation and sensing nodes that we developed and that allow the stimulation of human tissue and at the same time capture impedance and temperature. They are powered and communicate using wireless protocols, hence they can be deployed in the human body for an extremely long time. You could also combine implantable nodes with wearable devices. Think, for example, of an external wearable sensor that measures heart rhythm, respiration or digestive activity from the skin surface. This would then communicate with the implanted neurostimulators that counteract any sensed abnormality."

Use the patient's environment to monitor vital signs

Next to, or in combination with wearables and implantables, one can also use sensors in the



Imec develops both microneedles and implantable nodes for electrical sensing and stimulation of nerve cells.

Capacitive sensors can be incorporated into an armchair, bed, office chair or car seat. Imec has developed a system that can support up to 64 sensors. If you want to use capacitive sensors to record respiration rates, it is important in practical applications to make a record of the reliability of the readings as well.

environment to monitor patient's vital signs, at specific moments of the day. Miniaturized sensors can be integrated in chairs, car seats, beds, toilets etc.

Evelien Hermeling: "Imec explores capacitive, optical and radar technology to do vital sign monitoring 'from a distance.' For example, in a car one could build sensors into the driver's seat, steering wheel and dashboard to measure respiration rate, blood pressure, heart rate and cardiac activity."

"As a demonstrator, we integrated capacitive sensors in an office chair and a car seat to carry out ECG readings and detect respiration rates through clothing. This principle is not new, but the technology has not been used before in practical applications because the quality of the readings was poor due to movements of the person in the chair."

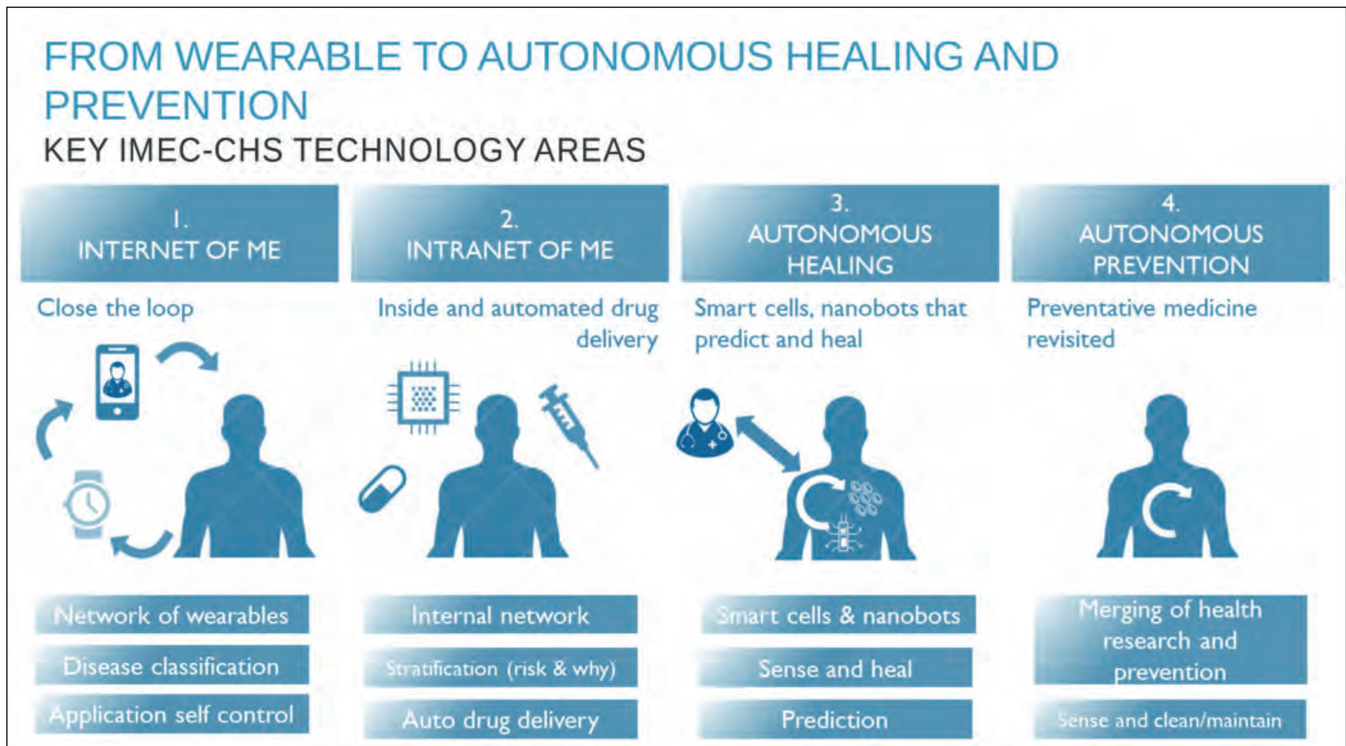
"The solution lies in the use of smart algorithms. First, algorithms can compensate for variations when movements and artifacts are detected, which makes the readings more reliable. Second, algorithms can make the system adaptive. This means that, in good conditions, an (ECG) signal of medical quality can be recorded. When conditions are not so good, the sensors switch to robust mode and take more general readings. For example, although you can still record the heart rate, obtaining an accurate ECG graph is not possible. This variable quality is factored into the readings and passed on as such – together with the results recorded."

Such sensing information could for instance be used as input to dynamically and automatically adapt the driving conditions and the level of self-steering of the car, or to generate actionable alarms. **Vojkan Mihajlovic:** "It's also possible to use wearables to capture how our senses react to different stimuli in the environment and use this info to adapt the environment. For example, we are collaborating with one of the largest South Korean cosmetics companies, Amorepacific, on capturing user reactions to different fragrances.

Based on this, a real-time selection of preferred fragrances is performed. Also, we are setting up a European project in which an avatar adapts its interaction with a real-life person to this person's emotional state. The possibilities are enormous."

Future vision: closing the loop with nanobots

Evelien Hermeling: "These are indeed some of the possible future applications of closed-loop therapy. At imec, we have a vision on how these closed-loop systems could evolve (see figure below). In the near future, we foresee a multitude of closed-loop therapy examples using wearables or sensors in the environment, communicating with (e.g. one's smartphone and doctor,) resulting in an action to be taken by the person (being monitored.) Image your smartwatch measuring your blood pressure and alerting you via your smartphone to take one extra pill."



Imec's future vision on the evolution of closed-loop therapy systems.

"In a next phase, the sensors and actuators could be implanted in the body, so the closed-loop system would be an integral part of the patient, regulating blood pressure, etc. We could think of 'nanobots' inside the body detecting certain abnormalities (e.g. atherosclerotic plaques inside blood vessels) and a doctor injecting some form of a smart cell to fix the problem. Or could this one day be executed in a completely autonomous way, giving a whole new meaning to preventive medicine? At imec, we like to think big, and lay out truly visionary roadmaps to inspire our researchers and to fuel the discussions with our partners."

Conclusion

Thanks to the miniaturization of sensors and actuators, and thanks to the enormous progress made in artificial intelligence and deep-learning algorithms, it becomes possible to close the loop on health: not only sensing vital signs but also interpreting the data, getting actionable insights, and triggering some action.

This leads the way to artificial organs, drug-device combinations, the targeted treatment of depression and chronic pain, and many other applications. Every closed-loop therapy system will look different and will rely on (a combination of) different form factors (wearable, implantable, invisible) and building blocks to find the perfect fit for a specific application.

Imec researches and develops the key building blocks for such a closed-loop therapy system of the future. Together with application and research partners, this technology can be translated into a tailored solution for specific patient conditions. Partner with us to shape this future!

About Vojkan Mihajlovic
Vojkan Mihajlovic is a senior researcher at imec. He received his PhD degree from the University of Twente, Enschede, The Netherlands and has worked as a senior scientist at Philips Research from 2006 to 2012. Since 2012 he has been working on system level and biomedical algorithms at imec. He has extensive experience and leads research activities in the area of wearable brain monitoring and noninvasive neuromodulation. He is also coordinating connected health solution innovation activities.

About Evelien Hermeling
Evelien Hermeling received her PhD degree in 2009 at the Maastricht University, the Netherlands. After a few years of post-doc at Maastricht University, she started as senior researcher at imec in 2015 and became principal scientist in 2019. Her drive is to bridge the gap between hardware, software, biomedical engineers and medical doctors. She is leading the competence team focused on biomedical algorithms and models within imec-Netherlands.

GaN Systems:
all eyes on audio amplifiers

With the Class D audio amplifier market poised for massive growth, GaN Systems has set its sights on snaring a big chunk of the sector, reports Rebecca Pool.

WHEN IT COMES to the wonderful world of audio, not all solid-state amplifiers are created equal. For decades, the analogue-based linear amplification Class A audio system has reigned supreme, with audiophiles tolerating its very low efficiency.

Not anymore. Today, a growing number of power semiconductor suppliers are delivering a new breed of GaN-based Class D audio amplifier that promises far higher power efficiencies than your archetypical Class A amplifier.

For example, Infineon Technologies has developed its 'MERUS' class D audio amplifier ICs that are said to maximize power efficiency and dynamic range while providing stunning audio performance in small product

form factors. And GaN Systems has recently released a Class D amplifier evaluation kit that also promises to deliver unprecedented efficiency and sound quality.

"When some of my very discerning customers from Japan first listened to our GaN amplifier, they told me that it was like arrows of sounds coming from the speaker," says Rick Reigel, Vice President of Sales at GaN Systems. "On closing their eyes they said they could feel the music and it felt as if it were live, rather than an artificially reproduced sound – this is the kind of reaction that we get."

Gathering momentum

Operating as electronic switches rather than linear gain devices, Class D amplifiers were initially developed in the 1950s. However, these systems didn't truly reach the market until the 1990s, with the advent of adequate-performing silicon MOSFETs.

Historically, these systems have been relegated to lower-quality audio systems as the use of silicon can lead to audio distortion arising from imperfect switching and high on-state resistance. However, Reigel is confident that the new wave of GaN MOSFET-based amplifier systems will change this, offering sound quality as well as higher efficiencies.

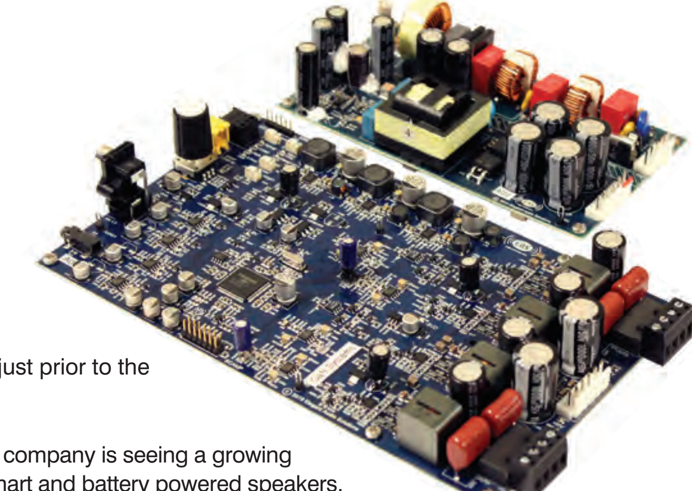
"GaN is going to continue the curve of improvement and can deliver a smaller, lighter, more efficient amplifier," he says. "The GaN MOSFET ensures much cleaner switching, enabling better linearity in the amplifier as well as less intermodulation distortion, which means [suppliers] can continue to shrink amplifier size without sacrificing sound quality, which is a trend we're seeing across the industry."

"We can get a high-fidelity sound using GaN in this Class D topology, as well as this great blend of size, weight, efficiency and cost," he adds. "This is the real value proposition of GaN in this application, and you just can't achieve it in any other way."

GaN Systems' recent evaluation kit includes a 2 channel, 200 W-per-channel class D audio amplifier and companion 400 W continuous power audio-grade switched-mode power supply (SMPS) without heatsinks. A single GaN FET design is used for front-end power factor correction with a dual GaN FET half-bridge used for the back-end SMPS.

Crucially, the set-up allows for a low-cost three FET design that doesn't demand a massive external heat-sink for full-power operation. And GaN Systems has also developed a low inductance GaN transistor package.

"In the pre-amplifier part of the design, we have a lot of silicon and this links to the audio source, say, a CD player or music files," highlights Reigel. "If you want to drive a stereo application with the full bridge, then there's actually eight GaN transistors in the output stage, just prior to the speaker."



Right now, the company is seeing a growing demand for smart and battery powered speakers, multi-channel automotive and high-end home-audio systems, and is also targeting traditional home theatre and professional audio markets, including stadiums. And according to Reigel, feedback from reviewers in the audio industry, so far, is good.

"We've taken our systems to the [Consumer Electronics Show] CES and carried out a side-by-side test with a silicon Class D amplifier," he says. "We got a great response – you literally hear the difference right away, and we believe we can provide a premium sound with a consumer price."

Reigel reckons for the transistors alone, this audio market is worth somewhere between $3.5 bilion and $4 billion, and has a compound annual growth of up to 10 percent. "GaN has an opportunity to grow very fast here as it's substituting for silicon in a market that already exists," he says. "Right now we're only encroaching on silicon here but I believe that eventually GaN will take the majority of the market, which is very nice for GaN transistor suppliers."

What's more, the Vice-President of Sales doesn't believe that competing technology, SiC, is a threat. As he puts it: "Silicon carbide is great for certain applications but still has a reverse recovery problem, so doesn't quite cut it in this application."

So where next for GaN Systems and Class D amplifiers? Reigel is confident that GaN Systems is set to be a frontrunner in the Class D amplifier market, which, he is sure, will switch entirely from silicon to GaN in around a decade.

"In five years I think GaN will have around 50 percent of this market and will hold close to 100 percent in ten years," he says.

"GaN is still in its infancy and there are still years of improvement ahead of us – over the next five years to a decade, we will see more improvements to the GaN transistor and these will directly benefit the audio amplifier," he adds. "This is a huge market commercially and so it makes sense for us to go after it by enabling designers with this ready-to-go kit."

Heterojunction enhances power diodes

Double-layered NiO contact provides a great *p*-type layer

ENGINEERS at Nanjing University, China, have poineered a new architecture for the Ga_2O_3 *p-n* diode. Their device features a double-layered NiO *p*-type layer.

Even without field plates and edge-termination structures, this new design is claimed to offer a higher breakdown voltage and a lower leakage current than comparable Ga_2O_3 devices based on either Schottky barriers or *p-n* junctions.

Spokesman for the researchers, Jiandong Ye, points out that the merits of their novel device are not limited to a high breakdown voltage – they also include a low leakage current density and a high thermal stability.

Ye and colleagues are developing diodes with a *p-n* junction, rather than a Schottky barrier, because the latter fails to take full advantage of the intrinsic breakdown field of Ga_2O_3. Due to tunnelling and thermionic emission currents, the maximum surface electric field for a typical Schottky barrier diode, employing nickel contacts, is only 2.4-3.2 MV cm^{-1}. That's well short of the intrinsic breakdown field, which is 6-8 MV cm^{-1}.

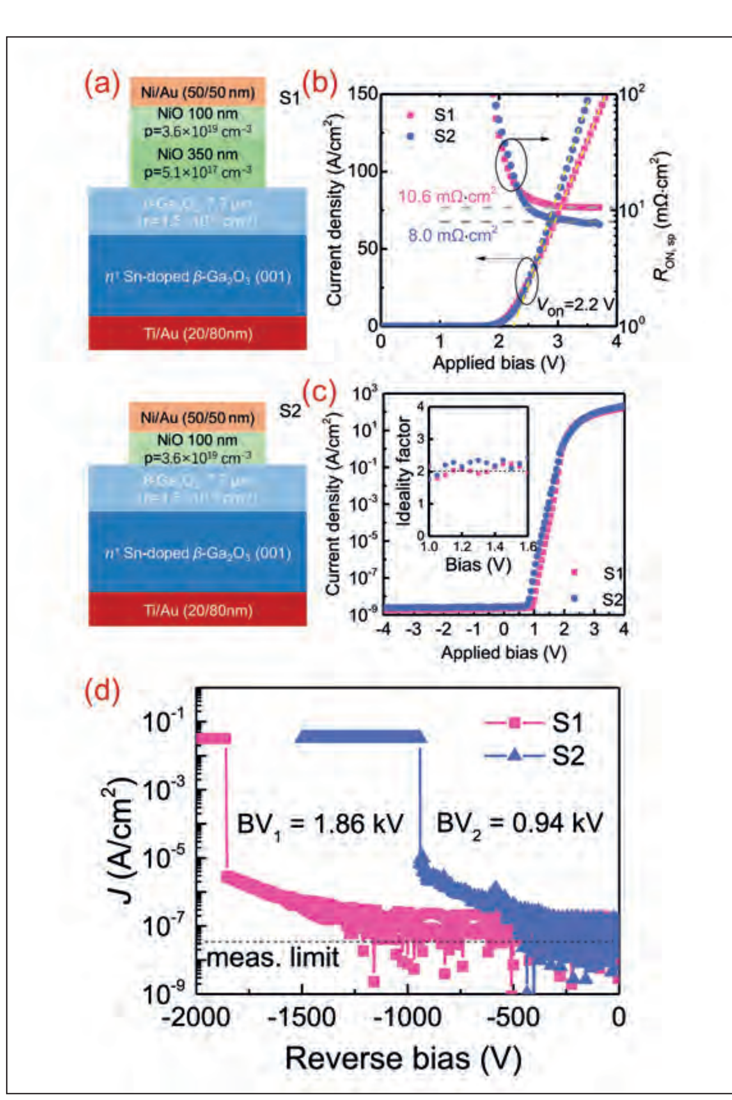
Switching to a *p-n* junction realises higher breakdown fields. As it is incredibly challenging to produce *p*-type Ga_2O_3, several research groups have investigated other oxides for the *p*-type layer. There are reports of Ga_2O_3 diodes with *p*-type CuO_2 that have a breakdown voltage of 1.49 kV, and variants with a NiO *p*-type layer with a breakdown of 1.06 kV. Ye and co-workers have taken the latter to a new level by introducing a double-layer of NiO.

To evaluate the benefits of the double layer of NiO, the team constructed two diodes. One had a 350 nm-thick lower-side layer doped to 5 x 10^{17} cm^{-3}, followed by a 100 nm-thick upper-side layer doped to 3.6 x 10^{19} cm^{-3}; while the control just had the lower side layer. A Ni/Au stack provided the top contact. Electrical measurements revealed that replacing the single layer of NiO with two layers led to an increase in the blocking voltage from 0.94 kV to 1.86 kV. Simulations suggest that the higher breakdown voltage stems from suppressing electric crowding, thanks to a reduction in the hole concentration in NiO.

As defects within NiO films and at the interface between NiO and β-Ga_2O_3 inevitably serve as conduction paths for the reverse leakage current, interface engineering is needed to suppress interfacial states.

"To solve the electric field crowding problem at the device edge, field management such as a field plate, guard ring, trench structure and a bevelled mesa structure is also essential," explains Ye.

The team is taking on these tasks, using a laser MBE technique to produce NiO with well-define doping, and introducing new designs to prevent high peak fields.



(a) Cross-section of a vertical NiO/β-Ga_2O_3 heterojunction diode with two structural designs; (b) linear plots of current-voltage characteristics and extracted specific on-resistance as function of forward bias, with the turn-on voltage obtained by fitting the linear segment; and (c) semi-logarithmic plots of current-voltage characteristics. The inset of (c) illustrates the extracted ideality factor. (d) semi-logarithmic plots of breakdown characteristics.

Reference

H. Gong *et al.* Appl. Phys Let. **117** 022104 (2020)

Simplifying VCSEL design

Adding a nanoscale cylindrical waveguide to a GaN VCSEL yields record-breaking output powers

COMPLEX METHODS for controlling the transverse mode in blue-emitting VCSELs are holding back commercialisation of this device. But this issue can be addressed by introducing a nanoscale cylindrical waveguide, a technique recently pioneered by researchers at Stanley Electric and Meijo University.

Single- and multi-mode GaN VCSELs produced in this manner can deliver a high level of performance, making them attractive candidates for a variety of applications. Single-mode variants, which combine a circular emission profile with low divergence and high spectral purity, could be deployed in retinal scanning displays, atomic clocks and bio-sensors. And more powerful cousins with multi-mode operation could be used in colour projectors and car headlamps.

Many complex approaches have already been used to control the transverse mode in GaN VCSELs, including: silicon-diffusion confinement; the insertion of photoelectrochemically etched air-gap structures; the addition of either a monolithic curved structure or a Nb_2O_5 convex structure; and the construction of a tunnel-junction intercavity contact.

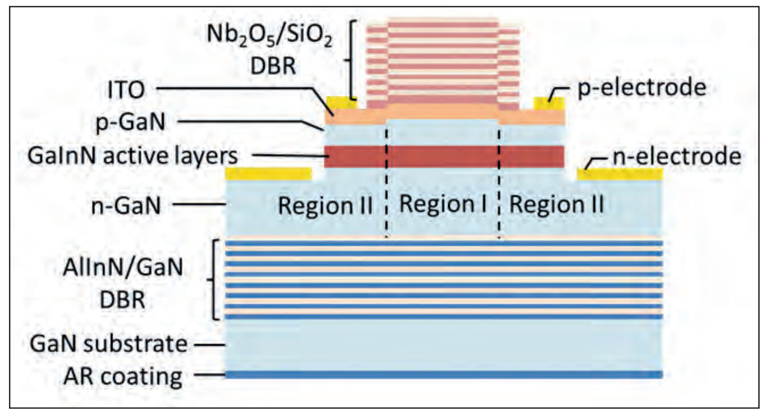
The team from Stanley Electric and Meijo University have previously added to this list with the formation of a buried lateral waveguide. It was created by dry-etching *p*-type GaN, before depositing SiO_2 with a self-aligned process. A high-performance VCSEL resulted, which used the insulating oxide for optical confinement, but not lateral current confinement.

Building on this development, the team are now using reactive-ion etching to create even better VCSELs. They feature a GaN cylindrical waveguide with a step height of just 5 nm that provides current and optical confinement.

Spokesman for the team, Masaru Kuramoto from Stanley Electric, points out that reports in other papers show that dry-etching using chlorine-based gases causes compensation of acceptors in *p*-type GaN surfaces, due to the generation of nitrogen vacancies. This degrades rectifying quality and limits the formation of *p*-type ohmic contacts.

“Based on these studies, it is expected that a newly designed structure, using chlorine-based reactive-ion etching plasma treatment, can also be employed to achieve current confinement.”

To produce VCSELs, the team loaded a GaN substrate into an MOCVD reactor and deposited a 40-pair AlInN/GaN distributed Bragg reflector and a cavity containing five 3 nm-thick InGaN quantum wells. Chlorine-based reactive-ion etching defined a 5 nm-high cylindrical waveguide, before addition of an indium tin oxide layer, followed by a top mirror formed of 10.5 pairs of SiO_2 and Nb_2O_5, completed device fabrication.



A cylindrical waveguide with a height of just 5 nm provides lateral confinement for the current and optical modes.

Measuring the near-field profile of this VCSEL, operating below threshold, revealed a homogeneous emission pattern across the aperture, which is defined by the waveguide. This finding indicates the high degree of optical and current confinement within the VCSEL.

Operating at 20 °C, devices with a 7 μm-diameter cylindrical waveguide produced a continuous-wave output power of 23.7 mW, a maximum slope efficiency of 1.2 W A^{-1}, and an external differential quantum efficiency of 43.6 percent. Operating temperature for these 450 nm lasers could reach 140 °C. According to the team, all these values break new ground.

The researchers also produced a variant with a smaller waveguide, delivering single-mode emission. Using a diameter of just 3.3 μm, this VCSEL, which emits at the slightly shorter wavelength of 442 nm, produced a continuous-wave output power of 7 mW, a maximum slope efficiency of 0.7 W A^{-1} and an external differential quantum efficiency of 25 percent.

One of the goals for this team is to further improve the efficiency of their GaN-based VCSELs. “They are still relatively low in comparison with GaAs-based VCSELs and GaN-based edge-emitting laser diodes,” says Kuramoto.

Reference

M. Kuramoto *et al.* Appl. Phys. Express **13** 082005 (2020)

Slashing on-resistance in *p-n* diodes

Oxide vapour phase epitaxy enables an incredibly low on-resistance in GaN *p-n* diodes

A TEAM from Japan has produced vertical GaN *p-n* diodes with an on-resistance of just 0.08 mΩ cm^2.

"The on-resistance is a record for gallium nitride, and lower than values for gallium oxide, as far as I know," says team spokesman Junichi Takino, who is affiliated to Panasonic Corporation and Osaka University.

The key to this incredibly low on-resistance is a high-quality substrate produced by oxide vapour phase epitaxy (OVPE). Substrates have a dislocation density of 8.8. x 10^4 cm^{-2} and a resistivity of just 7.8 x 10^{-4} Ω cm.

Takino believes that the technique used to make these substrates is compatible with high-volume manufacturing. The OVPE method does not generate solid by-products and reactor maintenance is easy. What's more, this growth technology produces GaN wafers with far simpler apparatus than that associated with HVPE, the mainstream method for GaN wafer manufacturing.

The team from Panasonic, Osaka University and Hosei University produced their high-quality material by loading a free-standing, HVPE-grown GaN seed wafer into a growth chamber and introducing ammonia and Ga_2O gas, which is generated by reacting gallium metal with H_2O gas. Hydrogen and nitrogen act as carrier gases.

Using temperatures in the growth and source zones of 1200 °C and 1130 °C, respectively, 500 μm-thick films were produced using a growth rate of 60 μm/hour. Following substrate removal, polishing yielded high-quality free-standing wafers (see Figure 1).

Given the growth conditions, it's not surprising that the GaN substrate is heavily doped with oxygen. However,

Figure 1. OVPE produces freestanding 2-inch GaN substrates with very low defect densities.

10 mm/div.

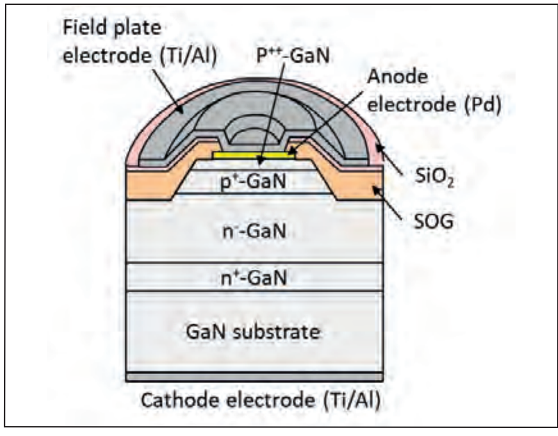


Figure 2. The diode contains: a 2 μm-thick GaN buffer layer; 13 μm-thick and 0.5 μm-thick GaN layers doped with silicon to a concentrations of 2 x 10^{18} cm^{-3} and 1 x 10^{16} cm^{-3}, respectively; and GaN layers, with thicknesses of 0.5 μm and 30 nm, magnesium-doped to concentrations of 1 x 10^{18} cm^{-3} and 2 x 10^{20} cm^{-3}, respectively.

this did not lead to cracks, dislocations and unwanted doping in an MOCVD-grown GaN epilayer, due to lattice mismatch and diffusion of oxygen.

Diodes were produced on OVPE-grown GaN substrates, and, to provide a control, also on HVPE-grown substrates. After growth of the epistructures (shown in Figure 2), dry etching defined mesa structures. Depositing a spin-on glass and SiO_2 film added an anode and cathode, completing device fabrication. Measurements on the *p-n* diodes revealed that the device produced on OVPE-grown GaN had a current density of just 10^{-4} A cm^{-2} up to 1.8 kV. For the control, the breakdown voltage is slightly lower for reasons still under investigation.

Driven at 4.5 V, the diode on the OVPE-grown GaN substrate had an on-resistance of just 0.08 mΩ cm^2, compared with 0.68 mΩ cm^2 for the control. Enhanced conductivity modulation is thought to account for this dramatic difference.

Goals for the team are to produce 6-inch wafers with their growth technology, and demonstrate diodes and transistors capable of handling 100 A or more.

Reference

J. Takino *et al.* Appl. Phys. Express **13** 0710101 (2020)

TRAINING DEVELOPMENT SKILLS

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Specialists with 30 year+ pedigree and in-depth knowledge in these overlapping sectors:

Expertise: Moderators, Markets, 30 Years + Pedigree
Reach: Specialist vertical databases
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Publications include: Compound Semiconductor, Silicon Semiconductor, CS China, SiS China

Power Electronics
Publications include: Power Electronics World

Future Mobility
Publications include: TaaS Technology, TaaS News

Data Centres
Publications include: DCS Europe, DCS UK, SNS International

SmartSolar UK & Ireland
Publications include: Solar and Power Management, Solar UK and Ireland

Sensors
Publications include: Sensor Solutions Magazine, Sensor Solutions International

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