POWER ELECTRONICS WORLD

CONNECTING THE GLOBAL COMMUNITY

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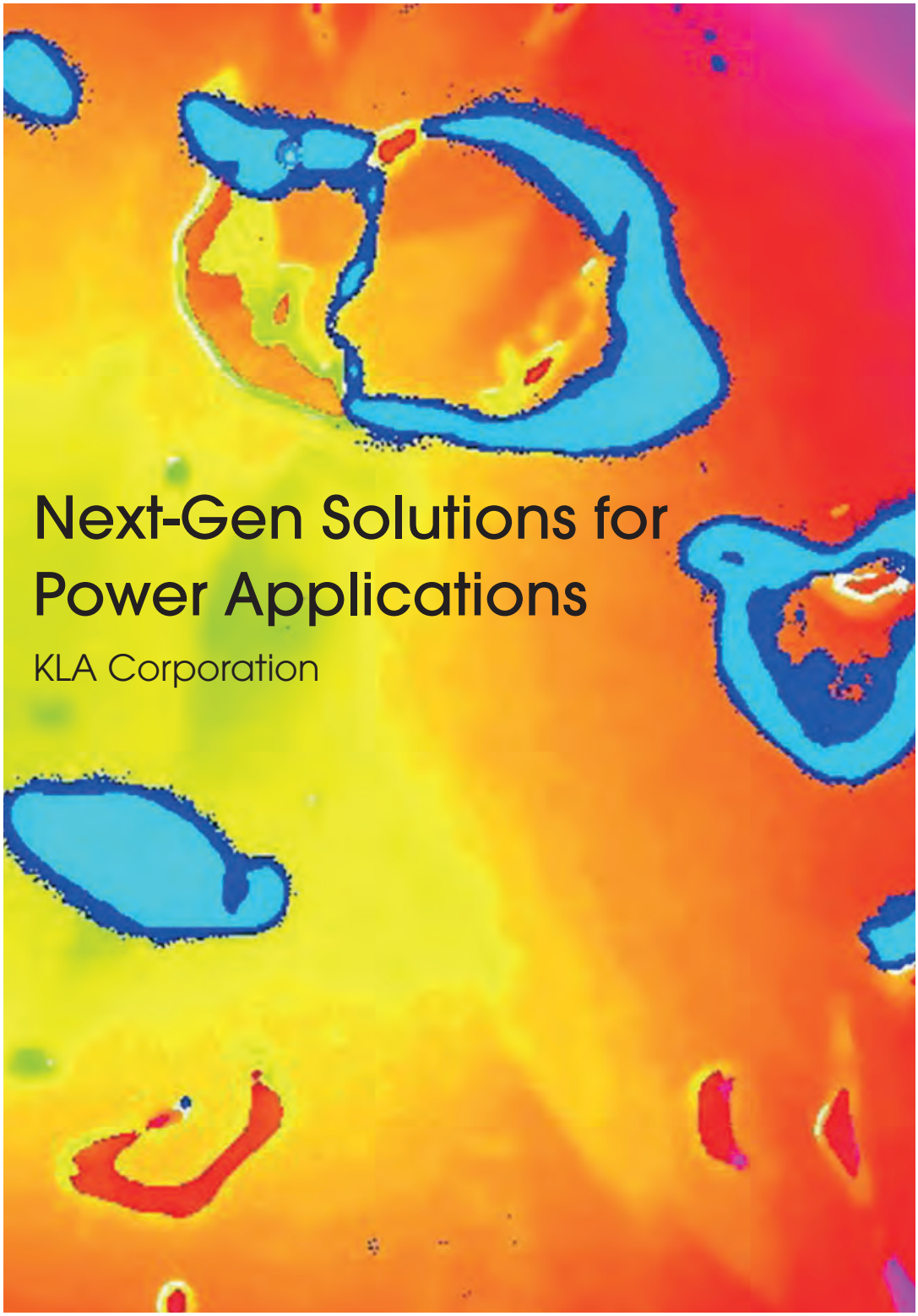
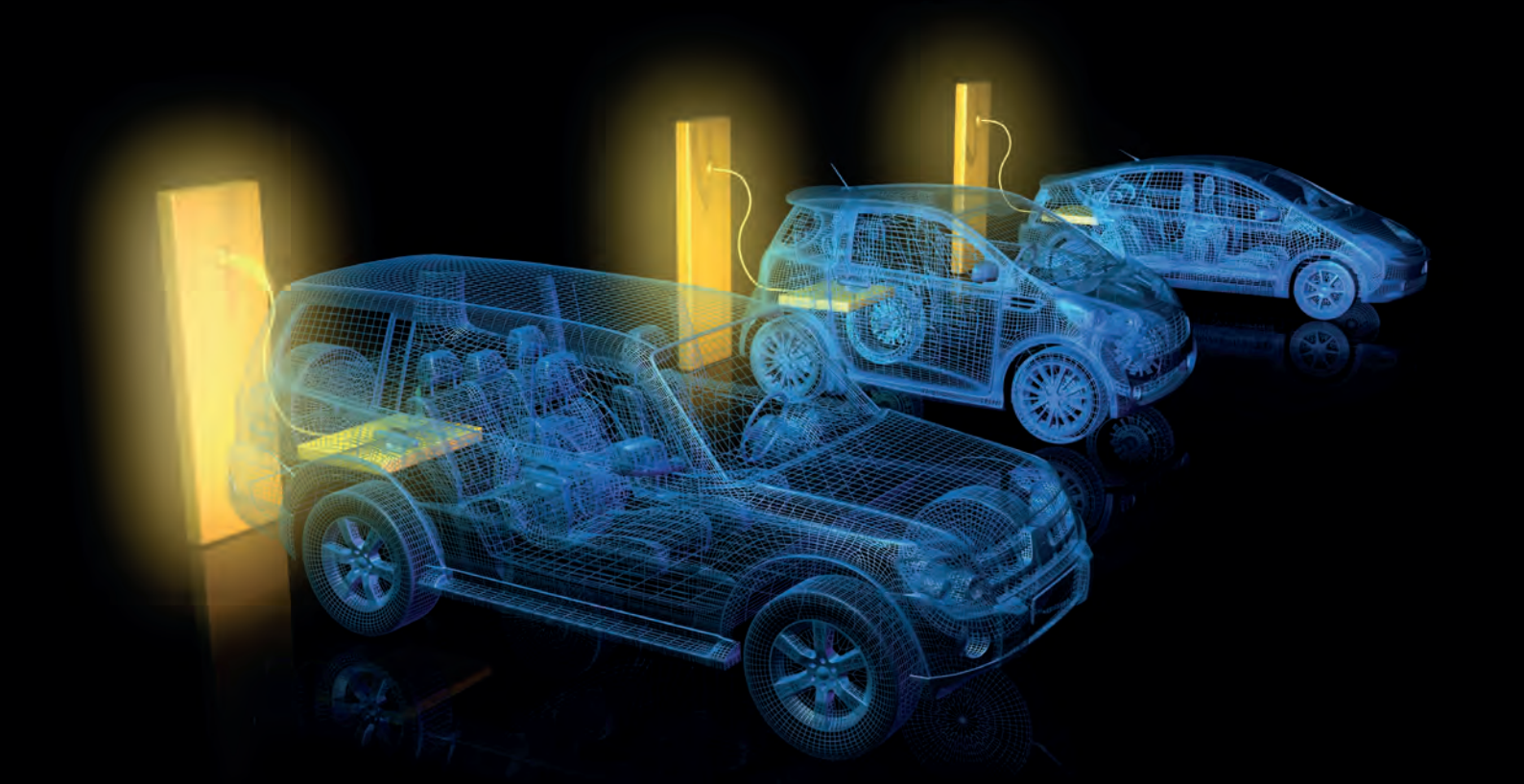


Next-Gen Solutions for Power Applications

KLA Corporation



Best performance for next generation SiC power electronics to address global mega trends

AIX G5 WW C

- Electric vehicles: on board chargers, power inverters
- Infrastructure: charging stations
- Renewables: solar and wind
- Industrial: motor drives, power supplies
- Power distribution: HVDC

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Viewpoint

By Mark Andrews, Technical Editor

Looking ahead to a brighter & better 2021

WE COULD ALL USE A BREAK. A pause. A respite. Take heart—the holidays are here, and the glass is half full, not half empty. Brighter days are indeed ahead.

After many grim months of infection tallies growing ever greater, the world received a much needed 'shot-in-the-arm' as COVID-19 vaccines began distribution in the UK, Europe and North America. Developing a new vaccine typically requires years, but by pooling resources, the global pharmacological community did the almost-impossible in mere months. Even as the latest surges bring more sad statistics, we at last have reason for hope. Instead of just raising our glasses to welcome a New Year, we'll soon be rolling up our sleeves.

If 2020 was plotted as a misery index, one could hardly find its equal in the past 50 years. While there were horrors aplenty, 2020 also had its heroes. These were not cape-clad Big Screen stars fighting mythical villains; 2020's heroes wore PPE, scrubs, and risked their lives each day to mend what was broken and comfort those facing their last hours without kith and kin. Each harrowing day became another, and then another—yet they prevailed. Looking for Superman? Thank a nurse. Or Wonder Woman? Hug a doctor. Iron Man? Thank the orderlies, the med techs and everyone giving their all to bring hope. Thank-you to our 2020 heroes and all who give us hope that we can soon de-mask and gather with friends (safely) while planning a future beyond living day-by-day.

We have a great final 2020 edition of Power Electronics World to share. This year saw increasing sales of electric vehicles thanks to ever-improving SiC's in fast chargers along with range improving batteries utilizing the latest lithium tech. We take a look at Wolfspeed's ongoing SiC improvements and parent company Cree's future beyond LED lighting. We examine new switching technology, better solar cells and amazing advances in concentrated solar power cells for satellites.

Despite the seemingly impossible challenges of 2020, industry met them head-on, delivering performance that was hard to envision amidst seemingly endless pandemic challenges.

Here is to brighter days ahead!

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news

EPC Launches eGaN FET for 48V synchronous rectification

EPC has advanced the performance while lowering the cost of off-the-shelf GaN transistors with the introduction of the EPC2059 (6.8mΩ, 170V) eGaN FET. This device is the latest in a family of 100 to 200V solutions suitable for a wide-range of power levels and price points.

They are designed to meet the increasing demands of 48 to 56V server and data centre products as well as an array of consumer power supply applications for high end computing, including gaming PCs, LCD/LED TVs, and LED lighting.

The EPC2059 is suitable for DC-DC secondary-side synchronous rectification in AC/DC adaptors, fast chargers, and power supplies with power ranges between 100 W and 6 kW. The performance advantage of GaN devices helps designers achieve the demanding efficiency requirements for 80 Plus Titanium power supplies, while providing smaller, faster, cooler, and lighter systems with lower system costs then currently available solutions.

According to Alex Lidow, EPC's co-founder and CEO: "There are very significant performance advantages gained from using GaN in the secondary-side synchronous rectification socket of AC/DC adaptors.

In a 400V to 48V conversion, switching at 1 MHz, GaN has shown to have one-sixth the losses and run 10 degrees cooler than a silicon MOSFET with equivalent on resistance. This enables designers to meet the latest stringent energy efficiency standards for high-end computing, where growth is exploding for multiple applications, such as artificial intelligence (AI), cloud computing, and high-end gaming systems."

Development Board

The EPC9098 development board is a 170V maximum device voltage, 25A maximum output current, half bridge with onboard gate drives, featuring the EPC2059 eGaN FETs.

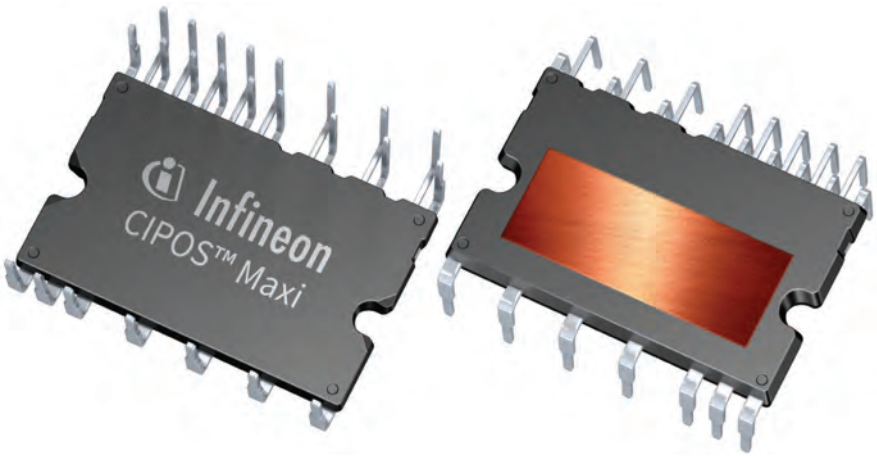
This 50.8 mm x 50.8 mm board is designed for optimal switching performance and contains all critical components for easy evaluation of the EPC2059.

Infineon launches CoolSiC CIPOS Maxi

INFINEON has launched a 1200 V transfer moulded SiC integrated power module (IPM) and concludes the roll-out of SiC solutions for this year.

The CIPOS Maxi IPM IM828 series is believed to be the industry's first in this voltage class. The series provides a compact inverter solution with an excellent thermal conduction and a wide range of switching speed for three-phase AC motors and permanent magnet motors in variable speed drive applications. Amongst others, these can be found in industrial motor drives, pumps drives, and active filters for heating, ventilation, and air conditioning (HVAC).

The CIPOS Maxi IPM integrates an improved 6-channel 1200 V silicon on insulator (SOI) gate driver and six CoolSiC MOSFETs to increase system reliability, optimise PCB size and system costs. The new family member is packaged in a DIP 36x23D housing. This makes it the smallest package for 1200 V IPMs with the highest power density and best performance in its class. The IM828 series features an isolated dual-in-line moulded housing for excellent thermal performance and electrical isolation. It meets EMI requirements and overload protection of demanding designs.



The rugged 6-channel SOI gate driver of the SiC IPM provides built-in dead time to prevent damages from transients. It also offers under-voltage lockout (UVLO) at all channels and over current shutdown protection functions. With its multi-function pin, this IPM allows high design flexibility for various purposes.

Adding to the protection features, the IPM is equipped with an independent UL-certified temperature thermistor. The low side emitter pins can be accessed for phase current monitoring making the device easy to control.

Infineon expands SiC supply base with GTAT

INFINEON TECHNOLOGIES AG and GT Advanced Technologies (GTAT) have signed a supply agreement for SiC boules. The contract has an initial term of five years. With this supply contract, the German semiconductor manufacturer adds a further element to secure its growing base material demand in this area.

Under the brand name CoolSiC Infineon now already markets a large product portfolio for industrial applications and is rapidly expanding its offerings towards consumer and automotive products.

"We are seeing a steadily increasing demand for SiC-based switches, especially for industrial applications," says Peter Wawer (pictured above), president of Infineon's Industrial Power Control Division.

"However, it has become clear that the automotive sector is quickly following suit. With the supply agreement we have now concluded, we ensure that we will be able to meet the rapidly growing demand of our customers with a diversified supplier base. GTAT's high-quality boules will provide an additional source for competitive SiC wafers fulfilling the best-in-class material standards now and in the future. This supports our ambitious SiC growth plans, making good use of our existing in-house technologies and core competencies in thin-wafer manufacturing."

"We are very excited to enter into a long-term supply agreement with Infineon," says Greg Knight, president and CEO of GT Advanced Technologies. "GTAT will enable Infineon to achieve a secure high-quality internal SiC wafer supply by applying their proprietary thin-wafer technology to GTAT's crystal. The growth of SiC device adoption is tied largely to the aggressive cost down of the substrate, and this agreement is a significant step towards achieving that goal."

SiC has mainly been used up to now in photovoltaic inverters, industrial power supplies, and the charging infrastructure

for electric vehicles. This is where the advantages of SiC at the system level, compared to classical silicon solutions, have already come into play.

Other industrial applications such as uninterruptible power supplies and variable-speed drives are increasingly making use of the new semiconductor technology. In addition, electric vehicles show enormous potential for application options, including the main inverters for the drive train and onboard battery charging units.

UnitedSiC introduces new SiC FETs on Gen 4 technology

UNITEDSiC, a US manufacturer of SiC power semiconductors, has launched the first four devices based on its advanced Gen 4 SiC FET technology platform. As the first and only 750V SiC FETs currently available on the market, these Gen 4 devices enable new performance levels, based on high Figures of Merit (FoM), that benefit power applications across automotive, industrial charging, telecom rectifiers, datacenter PFC, and DC-DC conversion as well as renewable energy and energy storage.

Available in 18 and 60 mohm options, these new SiC FETs deliver unmatched FoMs with reduced on-resistance per unit area, and low intrinsic capacitance.

In hard-switching applications, the Gen 4 FETs exhibit the lowest RDS(on) x EOSS (mohm-uJ) resulting in lower turn-on and turn-off loss. In soft-switching applications, their low RDS(on) x Coss(tr) (mohm-nF) specification provides lower conduction loss and higher frequency.

According to the company, these devices not only surpass existing competitive SiC MOSFET performance whether running cool (25degC) or hot (125degC), but also offer the lowest integral diode VF with excellent reverse recovery delivering low dead-time losses and increased efficiency.

In expanding UnitedSiC's offering to 750V, the new devices offer more designer headroom and reduced design constraints. This higher VDS rating also makes these FETs beneficial for 400/500V bus voltage applications.

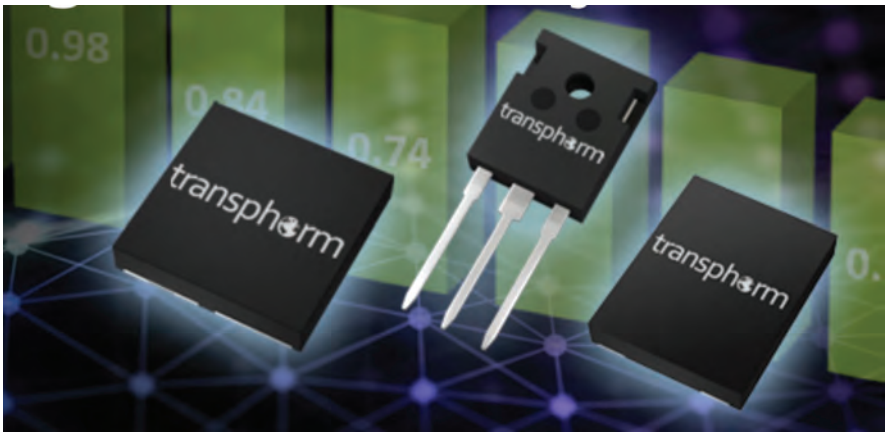
With a widely compatible gate drive of +/-20V, 5V Vth, all devices can be driven with 0 to +12V gate voltages. This means they work with existing SiC MOSFET, Si IGBTs and Si MOSFET gate drivers.

As Anup Bhalla, VP Engineering at UnitedSiC, explains: "These devices help address the challenges facing engineers working across sectors with the highest

voltage and power demands - from DC-DC conversion and on-board charging to power factor correction and solar inverters.

"We will be announcing many new Gen 4 devices over the next 9 months which will further improve on cost-effectiveness, heat efficiency and design headroom. This will support all sectors in overcoming the challenges of mass adoption and to accelerate innovation."

Transphorm selects Veeco platform for GaN-based devices



VEECO has announced that Transphorm, a supplier of GaN chips products for high voltage power conversion applications, has selected Veeco's Propel HVM MOCVD System for high-volume production of GaN-based RF (DoD and Commercial/5G) and power electronics epiwafers. The Veeco system was purchased under a US DoD Office of Naval Research (ONR) contract N68335-19-C-0107 from an OUSD (R&E) TAM/MINSEC program to establish a US based dedicated production source of GaN Epitaxy for high performance RF and mmwave electronics.

"Being at the forefront of GaN-based power and 5G devices that offer efficiency and high-power density, requires world-class manufacturing solutions that are capable of scaling to mass production while offering flexibility to continuously innovate," said Umesh Mishra, chief technology officer and co-founder of Transphorm. "Veeco's Propel HVM system is uniquely qualified to do that. The multi-reactor, single-wafer technology provides flexibility and exceptional throughput at a low cost of ownership."

The Propel system's single-wafer reactor platform enables the processing of six- and eight-inch wafers or two- to four-inch wafers in a mini-batch mode. It is said to accelerate production ramping due to faster recipe capabilities up to 50 percent quicker than when using traditional tools.

In addition to Veeco's proprietary TurboDisc technology, the system also includes Veeco's IsoFlange and SymmHeat technologies, which are designed to provide homogeneous laminar flow and uniform temperature profile across the entire wafer.

"We are proud to have our MOCVD technology selected by a pioneer and recognised world leader in the GaN revolution," commented Ajit Paranjpe, Veeco's CEO. "Transphorm's decision to adopt our high-volume MOCVD technology is proof of the system's uniformity, throughput, repeatability and cost of ownership advantages over batch technology."

Denso adopts SDK SiC epi-wafers for EVs

SiC epitaxial wafers, the main material for power semiconductors, with a diameter of six inches (150mm) and manufactured by Showa Denko, have been adopted by Denso Corporation for its latest booster power modules for fuel cell electric vehicles (FCEVs).

SDK's SiC epi-wafers, launched in 2009, have been adopted by electronic device manufacturers for various devices including power supply for servers of cloud computing systems, quick charging stands for EVs, and railcars. DENSO adopted SDK's SiC epi-wafers for its next-generation power modules recognizing the track record of adoption by device manufacturers, highest-grade epi specifications, low density surface defects, and low frequency of basal plane dislocation. When compared with current mainstream silicon-based semiconductors, SiC-based power semiconductors can operate under high-temperature, high-voltage, and high-current conditions, while substantially reducing energy loss.

These features enable device manufacturers to produce smaller, lighter, more energy-efficient power control modules. SiC power semiconductors are already used in on-board battery chargers and quick charging stands for EVs, and railcars. Demand for SiC power semiconductors is expected to grow, with full scale use in power control units (PCUs) for EVs in and after 2025.

The Showa Denko Group aims to contribute to the solution of SDGs-related issues through its business activities and become "a social contribution company" that contributes to the creation of society where affluence and sustainability are harmonised. The size of the market for SiC epi-wafer, which realises efficient use of energy, is expected to be about 100 billion yen in 2025, and will grow further because of the start of its full-scale use as parts of PCUs.

As the largest independent manufacturer of SiC epitaxial wafers, and under a motto of "Best in Class," SDK will continue coping with rapid expansion of the market for SiC epitaxial wafers and providing the market with high-performance and highly-reliable products, thereby contributing to the spread of SiC-based devices.

Tektronix releases TekDrive, groundbreaking data collaboration software

TEKTRONIX, INC. announced the availability of TekDrive, the first native oscilloscope-to-cloud software solution to facilitate global data collaboration directly on an oscilloscope, PC, phone or tablet. Created to enable ultimate ease and accuracy in data accessibility and collaboration, TekDrive provides engineers the ability to instantaneously share and recall data directly on an oscilloscope, eliminating the need for cumbersome data-sharing practices. TekDrive allows for data to automatically become accessible, usable and shareable across teams and partners, making remote work easier – all with industry-leading security practices built in.

In addition, TekDrive is the first general purpose test and measurement file system with scope-like data visualizations. The software provides ultra smooth visualization and analysis capabilities that support any modern browser, including options to view, zoom, pan, measure, decode and analyze full test and measurement data on any device without the need for any additional software. “This technology is a game changer for teams,” says Tami Newcombe, president of Tektronix. “Clients tell us about insecure data-sharing practices that are awkward and unreliable, and now with TekDrive, data sharing is secure and lightning fast. Launching TekDrive today marks a major expansion of our Tektronix vision to focus on relevant and cutting-edge software solutions that directly correspond to the latest industry needs.”
Seventy percent of oscilloscope users have the need to transfer data off scope. Through TekDrive, data updates are instantly saved in globally-accessible shared folders in which owners can manage secure access and permissions at a granular level.

“I joined Tektronix to help inspire the next wave of innovation in electronics engineering, and projects like this will do exactly that,” says David Sulpy, chief information officer at Tektronix. “Engineers needed their own workspace in the cloud to securely manage complicated, real-time data from their oscilloscopes. TekDrive fulfills that need, whether they are working in the lab or at home.” TekDrive was built with the engineer in mind, and boasts a clean, easy-to-use interface for file organization, management, search, upload and download. It’s also architected for ease-of-integration with secure vendor-agnostic REST APIs for scripting, automation and analysis. Tektronix provides SDKs and examples in multiple languages, such as Python, Matlab and LabVIEW. The TekCloud Developer Program also provides a secure way for third party developers to add native TekDrive capability to their devices, instruments and software applications. With a quick integration, any vendor of hardware or software can unleash the ecosystem of TekCloud storage, streaming, visualization and analysis into their products.

TekDrive is now available in many regions worldwide and will be released globally over the coming months. All TekDrive users receive a free contributor account, which grants participation rights in shared files and folders, with the Enterprise Tier boasting unlimited contributors. A 14-day trial is also available.

EPC adds 300W bidirectional 16th brick

EPC announces the availability of the EPC9151, a 300 W bidirectional DC-DC voltage regulator in the 16th brick format which is just 33 mm x 22.9 mm.

The EPC9151 power module features Microchip’s dsPIC33CK digital signal controller (DSC) with the EPC2152 ePower Stage integrated circuit from EPC to achieve greater than 95 percent efficiency in a 300 W 48 V to/from 12 V converter design. Additional phases can be added to this scalable 2-phase design to further increase power. Brick DC-DC converters are widely used in data centre, telecommunication and automotive applications, converting a nominal 48 V to (or from) a nominal 12 V distribution bus. Advances in GaN integrated circuit (IC) technology have enabled the integration of the half bridge and gate drivers, resulting in the EPC2152 single chip solution employed in the EPC9151 module to simplify layout, minimise area, and reduce cost for these applications.

Transphorm samples first SuperGaN Gen V FET

TRANSPHORM has announced it is sampling of its first Gen V device under its proprietary SuperGaN brand, the TP65H015G5WS. The new Gen V device, which is for electric vehicles, is claimed to offer the world's lowest packaged on-resistance, delivering a 25 percent lower power loss over SiC in a standard TO-247-3 package.

In March 2020, Marelli, a large independent supplier to the automotive sector, announced a strategic partnership with Transphorm to collaborate on new GaN-based automotive/EV power conversion solutions including on-board chargers (OBCs), DC-DC converters and powertrain inverters for electric and hybrid vehicles. To date, Marelli has made a $4 million equity investment in Transphorm and has committed to an additional $1 million equity investment in Q1 2021.

Joachim Fetzer, CEO, Electric Powertrain Marelli, commented: "Transphorm's demonstration of achieving 10 kilowatts of power from a discrete packaged GaN device in a bridge configuration is further validation of the exciting promise of GaN for electric vehicle converters and inverters. As part of our previously announced partnership, we will continue to evaluate Transphorm's industry-leading GaN devices and work together in support of a multi-year EV systems product roadmap."

"We continue to innovate Transphorm's SuperGaN FET technology, now offering the world's lowest on-resistance in a standard TO-247-3 package in the

market, targeted for electric vehicles and other higher power conversion applications. This allows customers to drive into double digit kilowatts with a single device, continuing to demonstrate GaN's ability to provide higher performance, lower system cost and higher power density," said Primit Parikh, COO and co-founder, Transphorm. "Our Gen V GaN platform is creating new design opportunities for power levels that previously required paralleling, while still offering the greater than 99 percent efficiency."

Outperforming SiC

According to Transphorm, the SuperGaN Gen V platform incorporates all the learnings from its Gen IV predecessor, patented reduced packaging inductance technology, ease of designability and drivability (Vth of 4 V for noise immunity), and gate robustness of +/- 20 Vmax along with a simplified and reduced assembly structure. In a recent article published in EEWorld, "Pushing the Boundaries of High Voltage GaN Power Conversion," the company's TP65H015G5WS was compared to a similar on-resistance leading-edge SiC MOSFET in a standard TO-247-3 package.

The devices were both operated up to 12 kW at 70 kHz in a half bridge synchronous boost converter, resulting in Transphorm's GaN device demonstrating up to 25 percent lower losses.

Transphorm has begun sampling the SuperGaN Gen V FET, a 15 mΩ 650 V device, which is unavailable with today's single chip e-mode GaN technology due to its gate sensitivity.

Matching the lowest R available from typical SiC MOSFETs in a discrete package, the solution is capable of driving more than 10 kW depending on the target application, such as EV OBCs and powertrain inverters, power supplies for rack powered data center servers, uninterruptible industrial power applications, and renewable photovoltaic inverters.

The TP65H015G5WS will also be available for die level module solutions that enable further paralleling for even higher power.

The ompany anticipates its Gen V FET device to receive JEDEC qualification in mid-2021 with AEC-Q101 qualification expected thereafter.

EPC Launches 40V eGaN FET

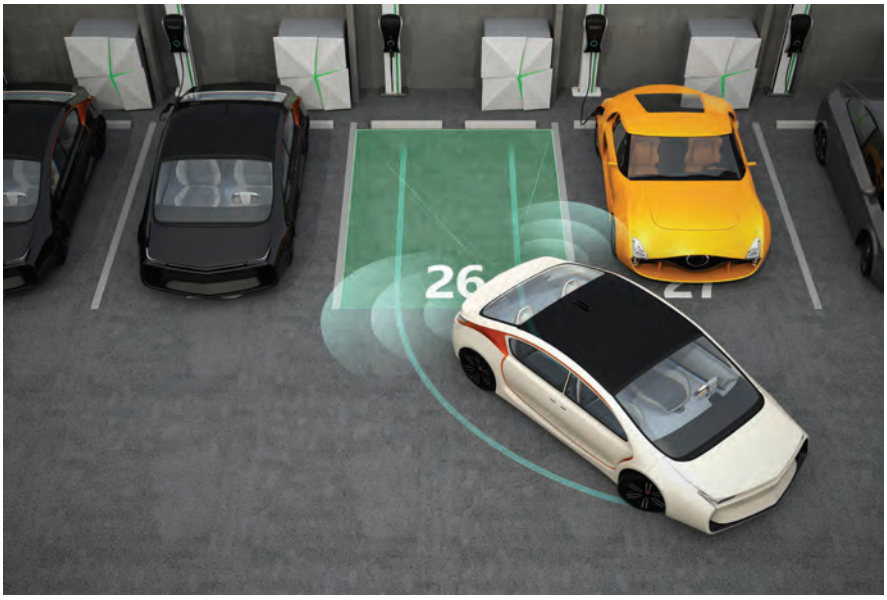
EPC, a maker of enhancement-mode GaN on silicon (eGaN) power FETs and ICs, has introduced the EPC2055 (3 mΩ, 40 V) eGaN FET.
This device is suitable for applications with demanding requirements for performance in space-constrained form factors including USB-C battery chargers and ultra-thin point-of-load (POL) converters. Other low-voltage applications benefiting from the fast-switching speeds and ultra-high efficiency of the EPC2055 include LED lighting, 12 V – 24 V input motor drivers, and lidar systems for robotics, drones, and autonomous cars.

According to Alex Lidow, EPC's co-founder and CEO: "The EPC2055 is a very good example of the rapid evolution of GaN FET technology.

This 40 volt device offers both smaller size and reduced parasitics compared with previous-generation 40 V GaN FETs and at lower cost; thus, offering designers both improved performance and cost savings." The EPC90132 development board is a 40V maximum device voltage, 25 A maximum output current, half bridge with onboard gate drives, featuring the EPC2055 eGaN FETs. This 50.8 mm x 50.8 mm board is designed for optimal switching performance and contains all critical components for easy evaluation of the EPC2055.

EnergyHub and Enel X partner to expand EV charging as a grid resource

EnergyHub has partnered with Enel X, the Enel Group's advanced energy services business line and EV charger manufacturer and service provider, to expand the availability of smart electric vehicle (EV) charging stations as a flexible distributed energy resource (DER) for utilities. Through the partnership, utilities can now manage customer-owned Enel X smart EV charging stations through EnergyHub's Mercury DERMS platform, expanding the breadth of EnergyHub's EV charging solution and increasing the EV charging resources available for utilities to manage. Utilities including Baltimore Gas & Electric (BG&E) and Eversource are the first to leverage the partnership and enroll customers with JuiceBox residential smart charging stations, with more to come.



Preparing for transportation electrification has emerged as a top priority for utilities. Bloomberg New Energy predicts EVs will account for the majority of passenger car sales by 2040. According to the same research, smart EV charging technology, which encourages customers to charge at optimal times, is estimated to save grid operators 30 to 70 percent of electrical infrastructure upgrade costs, representing hundreds of millions to billions of dollars a year in savings.

"We see managed EV charging as an important and growing piece of our DER portfolio, which we leverage not just during the hottest days of the year, but to manage demand year round," said Michael Goldman, Director of Energy Efficiency for Eversource. "We're glad to be able to allow more customers to participate by offering incentives to our customers with JuiceBox EV chargers." The partnership with Enel X, with over 60,000 consumer charging stations deployed nationwide, expands the ecosystem of EV chargers that utilities can manage with EnergyHub's Mercury DERMS.

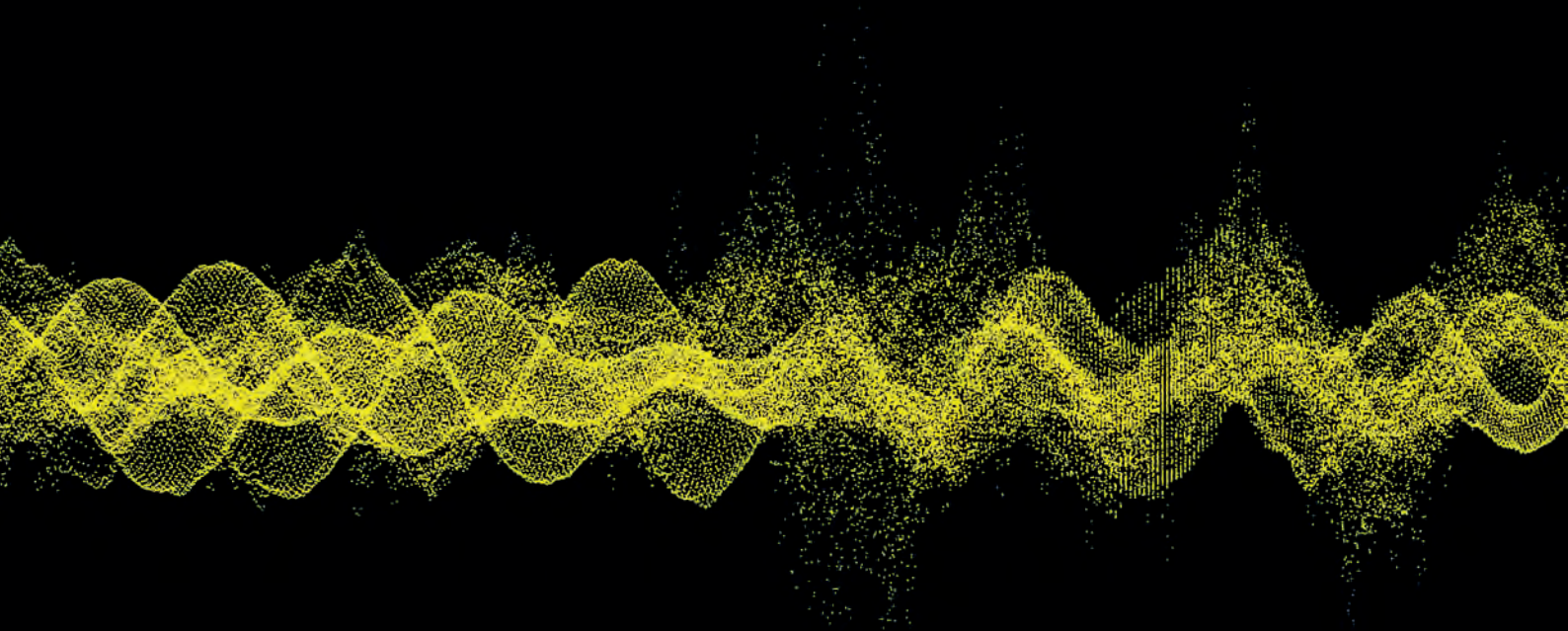
"Working with EnergyHub and Enel X allows us to partner with our customers to manage flexible EV charging load, preparing us for the future of transportation electrification, while also supporting the grid as whole" said Kristy Fleischman Groncki, manager of strategic programs at Baltimore Gas and Electric. "Our EV Smart program managed with EnergyHub rewards customers for contributing to the grid while using their preferred EV charging equipment."

EnergyHub and Enel X are working with electric utilities to harness the benefits of EV adoption and smart charging for the grid. The partnership enables utilities to grow their DER portfolios deployed with EnergyHub by managing enrolled Enel X JuiceBox smart charging stations in a service territory. Through the integration of EnergyHub's Mercury DERMS platform with Enel X's cloud-based JuiceNet smart EV charging software, utilities can forecast load, intelligently instruct, and monitor load results from customer-owned Enel X charging stations.

Utility time-of-use (TOU) rates incentivize EV owners with Level 2 smart charging stations to utilize off-peak charging, generating bill savings for the customer and reducing strain on the grid during peak periods. In Maryland, where the state has a goal to deploy 300,000 EVs by 2025, the Public Utilities Commission authorized local utilities to install a network of 5,000 residential, workplace, and public charging stations.

To best support the rollout, BGE deployed EnergyHub's Mercury DERMS to implement an EV-TOU rate that incentives off-peak charging, through the gathering and analyzing of charging data. This charging data is provided at a 15 minute granularity from customers' Level 2 charging equipment, including Enel X JuiceBox smart chargers.

The integration of EnergyHub's Mercury DERMS plaform with Enel X's JuiceNet smart EV charging software platform is enabled by JuiceNet, which optimizes the energy consumption of the JuiceBox EV charging station to align with grid conditions, while ensuring customer mobility requirements are met. EnergyHub's Mercury DERMS platform allows utilities to monitor, coordinate, and orchestrate EV charging in concert with other DERs. EnergyHub works with utilities on multiple types of EV management solutions: time of use (TOU) enablement, peak management, and dynamic load shaping. EnergyHub and Enel X previously partnered to provide utilities with access to certain portfolios of Enel X commercial and industrial demand response assets.



IGBT modules interrogated acoustically

IGBT failures, because of the typically high voltage and power levels, can be both costly and dangerous. It makes sense to find internal structural defects be-fore they have an opportunity to go wrong.

BY TOM ADAMS, CONSULTANT, NORDSON SONOSCAN

A GROUP of three small air voids is trapped in the solder that bonds an IGBT module to its heat sink. The voids happen to lie close enough to each other to prevent some of the heat from escaping cleanly from the area of the die just above them. Over time, the area above the voids may overheat and the die may fail electrically - and along with it the system it is part of.

IGBT failures, because of the typically high voltage and power levels, can be both costly and dangerous. It makes sense to find internal structural defects before they have an opportunity to go wrong.

X-ray and ultrasound can both perform the nondestructive imaging that is needed, but with some differences. The first is penetration. X-ray may not ade-quately penetrate the heat sink on some IGBT modules, to deliver its data. The X-ray beam reports local differences in attenuation, and the most frequent de-fects in IGBTs are air gaps and non-bonds.

If the gaps are relatively thick, such as a void in solder, imaging may succeed, but if they are very thin, as in a non-bonded area, they may remain invisible because their impact on the beam's at-tenuation is too slight.

An Acoustic Micro Imaging tool such as a C-SAM® tool from Nordson SONOSCAN can readily penetrate the heat sink, but first it needs to solve an-other problem: the small water column that on other components couples the tool's transducer to the top

of the component cannot be used on the top surface of an unencapsulated IGBT module. Impure water coming in contact with the face of the module could invariably leave some residue from evaporation, and the IGBT's voltage level is so high that the residue could become a con-ductive pathway, with disastrous consequences. IGBT modules area one the few comps types the only component type having this limitation.

For this reason an inverted acoustic micro imaging tool was developed in order to image IGBTs from below, through the heat sink. The transducer and its wa-ter column both point upward at their station below the module, whose top surface remains dry. Because the bottom side of an IGBT module not covered by encapsulant, the modules can be imaged even after encapsulation.

As the tool's transducer scans back and forth along the bottom surface of the heat sink, it carries out its pulse-echo function at individual x-y locations tens of thousands of times per second, and contributes one pixel for the acoustic image with each pulse. The sequence is this:

- the transducer launches a pulse upward into the column of water.
- the pulse strikes the water-to-heat sink interface, and is in part reflected back to the transducer and in part transmitted upward into the module.
- the reflected echo reports, among other things, the distance from the transducer to the surface of the heat sink at the bottom of the module
- the transmitted portion travels through the heat sink and reaches the interface between the heat sink and the solder
- the heat sink-solder echo is reflected to the transducer, where it reports the distance and other data about the interface.

The process will continue upward through additional material interfaces until the pulse reaches the attachment of the die to the raft. But before it reaches the raft, it will report any unintended features it encounters in the solder. The unintended features consist almost entirely of air gaps, which may take the form of air bubbles in the solder or flat delaminations between two solid materials. This is when the three voids mentioned in the first paragraph would be imaged, and their distance from the heat sink surface recorded.

The air bubbles are actually the most imageable features in the module, because instead of presenting a solid-to-solid interface, they present a solid-to-gas (air) interface, which reflects more ultrasound (nearly 100%) back to the transducer than any other type of interface. Solid-to-solid interfaces tend to reflect 10 to 50 percent of the energy in an arriving pulse. No ultrasound penetrates the solid-to-air interface, so x-y locations lying directly beyond it will not be imaged. You can see these effects at work in the monochrome

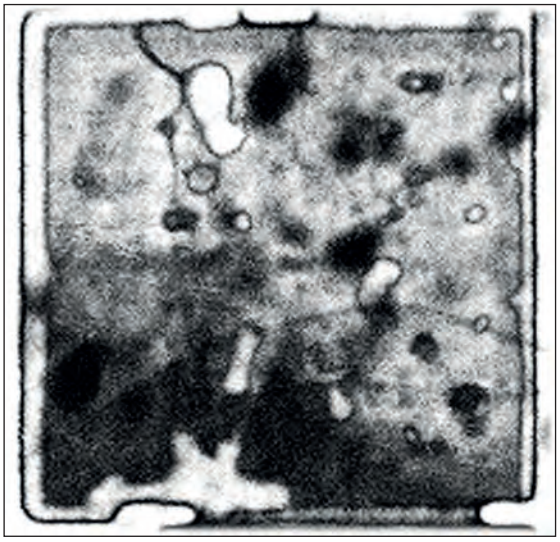


Figure 1. Monochrome acoustic image made by scanning through bottom of module shows defects in one die attach.

acoustic image in Figure 1. To make this image, ultrasound was pulsed upward through the heat sink, the solder, the raft, and the die attach material, and returned to the transducer by the same route.

The rounded white feature near the upper left is an air-filled void in the layer bonding this chip to the ceramic raft in the module. There is another large void near the lower left, and several smaller ones.

This image was made by using a 'gate.' Since the pulse was launched three ma-terial layers below, to make the desired image the receiver needs to select only the echoes from the small slice of time during which echoes were reflected by this die.

At each x-y location, the transducer's receiver waits after a pulse is launched until at precisely the right nanosecond after launch it is activated to accept whatever arrives from the gated depth - anything from no echo to, as here, the strongest possible echo. Probably thousands of 'strongest possible' echoes arrived at the receiver to make the x-y shape of this void appear white. Weaker echoes produce gray. No echo at all yields black.

There seem to be a few cracks in this die, visible as dark lines; one reaches the void at upper left. The indistinct black features mostly on the right half of the die are voids in the solder layer, which is closer to the transducer. They are above the gate set for the die that is being imaged. They are black because they are shadows from voids above the gate.

Being voids, and filled with air, they sent back their own echoes when the pulses coming from the transducer struck them, but their own echoes arrived at the transducer too early to be within the collecting gate and were ignored. But by preventing pulses from reaching the die, they sent their own acoustic shad-ows to the transducer. One might also explain the same phenomenon by saying that during the brief moment when the transducer was receiving echoes

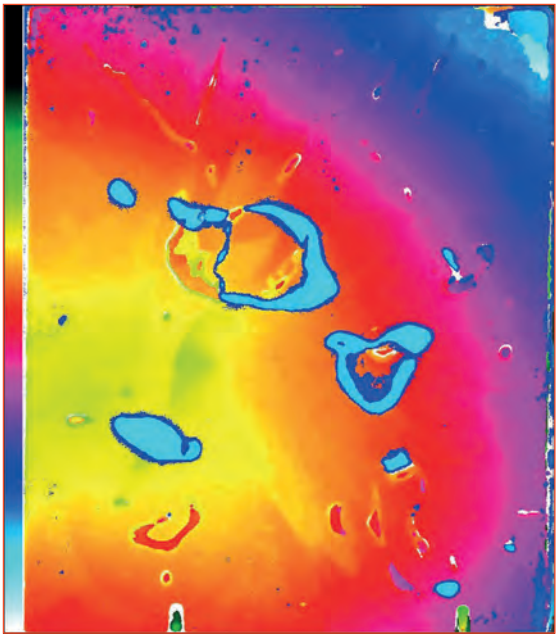


Figure 2. Light blue features are closest to heat sink, pale green are farthest above.

from the die attach, the areas beyond these voids had nothing too contribute.

Figure 2 is the acoustic image of the raft surface on one of the die on a IGBT. The colors here are reporting the vertical distance of the solder-filled space between the raft and heat sink surfaces. This figure extends vertically through the whole thickness of the solder. The raft is deepest in small areas at left center (pale green in color map at left) and highest at upper right (pale blue in color map), where there is so little solder that the raft surface probably comes close to touching the heat sink.

The key features here are the non-uniform thickness of the solder and the numerous heat-blocking voids, some of which are quite large. Collectively they may be capable of causing a region of the die just above to overheat and fail. Those voids that are light blue are likely in contact with the heat sink. But note that part of the upper right corner is the same color, because the solder in this region is very thin.

The large blue C-shaped void near the center lies above an-other large void that lies in the red-yellow depth. Non-uniform solder layers may lead to uneven heat dissipation and therefore unwanted stress. Non-uniform solder layers may lead to uneven heat dissipation and thus unwanted stress.Neither of the IGBT modules shown here would be candidates for incorporation into a product: they are simply too filled with anomalies. But in these high-power modules even a single small anomaly could lead to failure if the modules are being used close to their design specifications.

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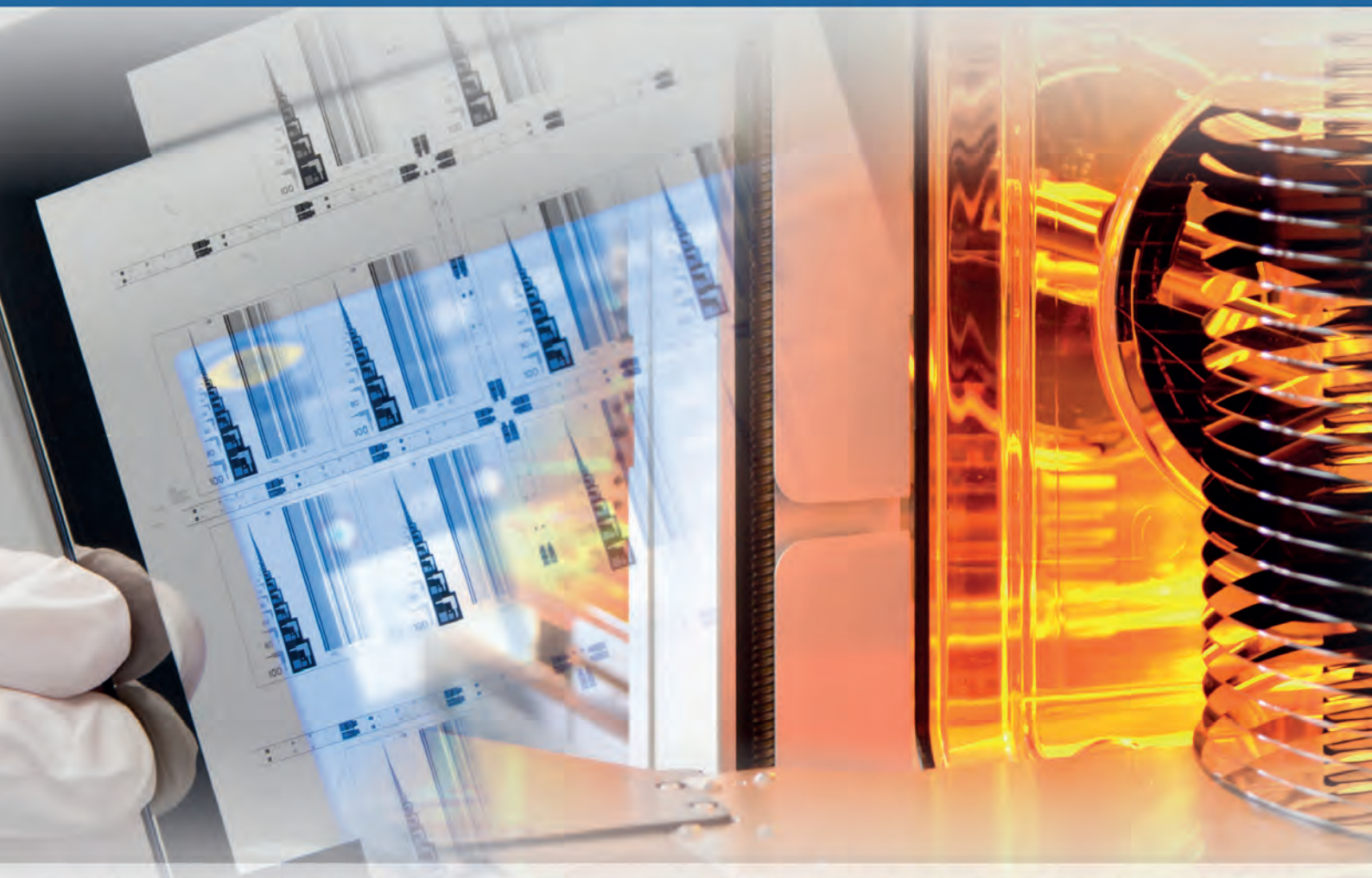

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KLA Corp. focuses on next-gen solutions for power applications

Power Electronics World technical editor Mark Andrews recently asked representatives of KLA Corp. to detail the ways that they are assisting customers address unique inspection and metrology requirements for power devices for automotive applications in addition to SiC and GaN technologies that seek to displace incumbent silicon technologies.

BY KLA CORP.

MA: Please describe KLA's specialized inspection systems for SiC substrates as well as processing within GaN-on-silicon manufacturing flows that target present and future automotive power requirements.?

KLA: SiC power devices pose unique yield and cost challenges in comparison to Si-based devices. Some of these challenges include:

- Much higher intrinsic material defect densities than Si-based devices
- High level of defect transference from substrate to epitaxy to device fabrication
- Variation in quality among substrate suppliers. Wafers graded and sold by dislocation density.
- Key defect issues include both crystallographic and morphological defects (carrots, surface triangles and stacking faults)
- Defect mechanisms act in the z-direction instead of x/y-plane. KLA's Candela 8720 compound

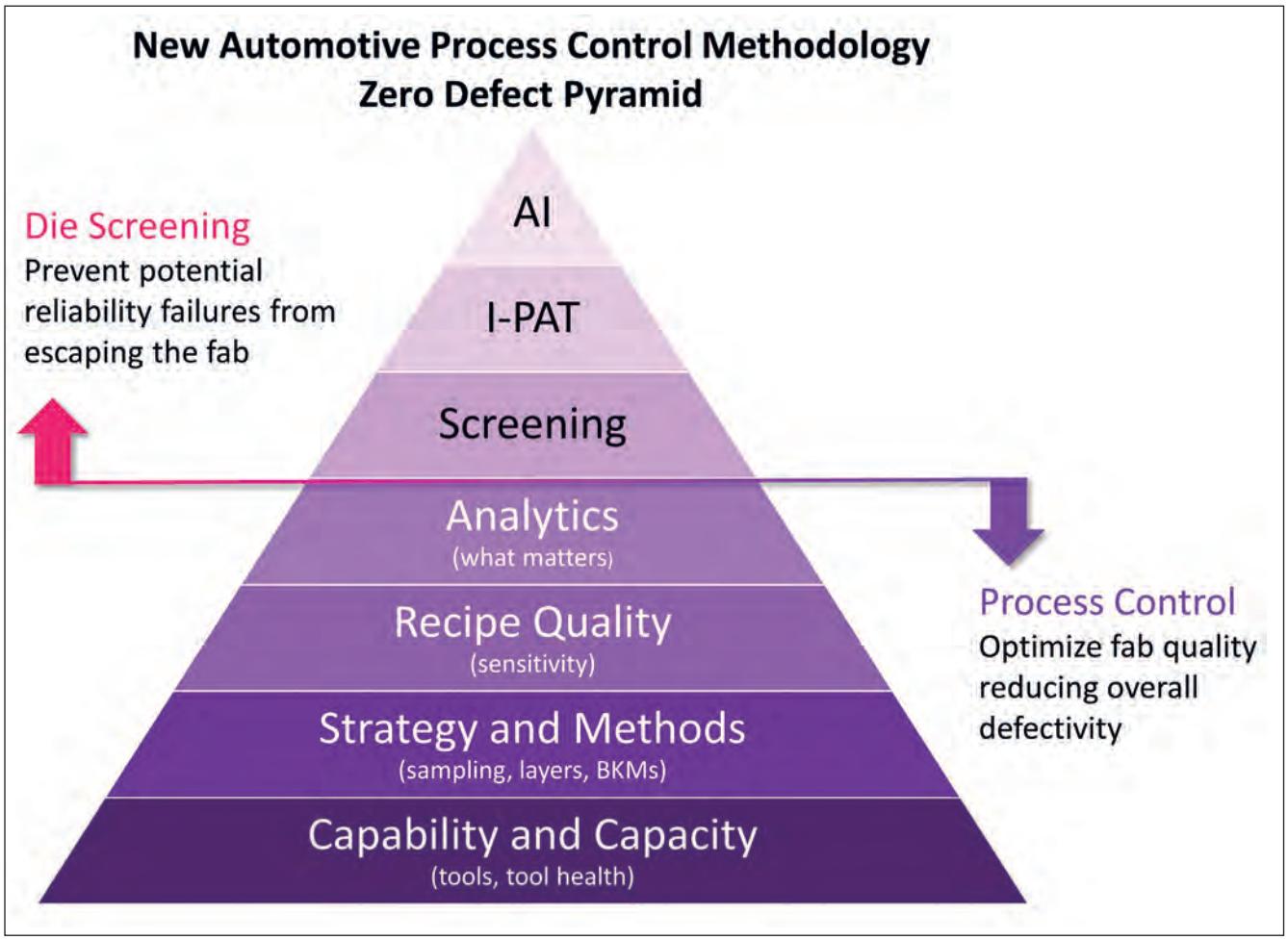


Figure 1: New automotive process control methodology Zero Defect pyramid

semiconductor material surface inspection system and the 8 Series patterned wafer inspection system have been developed to address these challenges.

The Candela® compound semiconductor material surface inspection system enables GaN-related materials, GaAs substrate and epi process control with high sensitivity to critical defects for the production of power devices, communications and RF devices, and advanced LEDs (as well as upcoming micro LEDs).

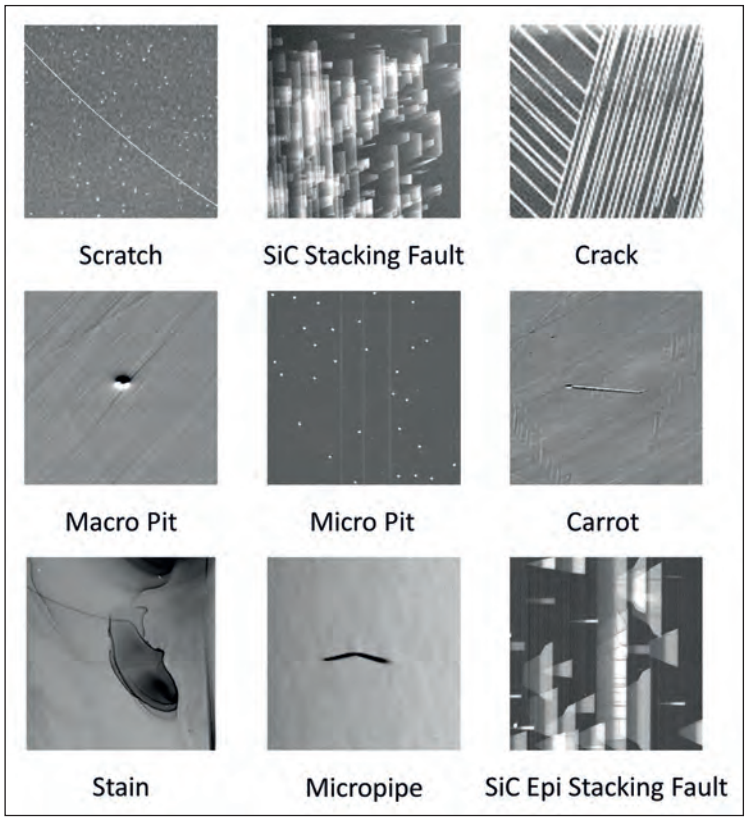
With its proprietary optical design and detection technology, the Candela inspection tool utilizes signals from scatterometry, reflectometry, ellipsometry, slope and photoluminescence detectors to detect and classify yield-limiting, sub-micron defects to support production-line monitoring.

The Candela 8720 system is used to monitor the substrate IQC (incoming quality control) and OQC (outgoing quality control) processes for a variety of defect types including particles, scratches, stains, pits, micropipes, stacking faults and other crystallographic defects.

For the post epitaxial growth process step, the inspection system can detect and monitor process issues such as cracks, macro epi disturbances (such as droplets), epi pit, epi bump, crystal-oriented defects (such as single/bar stacking faults, BPDs, etc.), micropits and particles. Defects in the substrate and post epi growth can significantly impact end of the line yield, so detecting and correcting such process issues at the source – where cost is the lowest – is critical. Patterned wafer inspection of SiC semiconductor devices is important for reducing defectivity and maintaining traceability, but inspection can present several unique challenges.

Wafer thickness and warpage are outside typical SEMI standards. The transparent (SiC) substrate can create challenges for focus systems and create unwanted noise when imaging the wafer. The 8 Series patterned defect inspection tool addresses these challenges through a specialized prealignment and chuck, selectable illumination wavelengths and depth of focus for inspection, multiple inspection channels and increased wafer handling flexibility.

With simultaneous brightfield and darkfield inspection capability, it captures all types of surface defects with a multi-level defect binning solution. With optional back side inspection capability, the 8 Series system can handle and inspect both frontside and back side



of 6" SiC pre- and post-grind wafers offering high precision frontside to back side correlation and die inking for process-induced killer defects on both sides of the wafer.

It is important to note that beyond some of the early SiC process steps, the many remaining steps for SiC are very similar to a standard silicon chip process, so SiC fabs will utilize similar process control strategies compared to silicon IC fabs.

MA: Producing automotive ICs and packaged devices present unique challenges beyond greater reliability such as the need to produce spare parts for years longer than consumer electronics. How does KLA technology help device manufactures meet these critical needs?

KLA: Automotive fabs have faced this problem for years and they do it by maintaining the process control strategies and standards that they used successfully in the past. This is shown through the defect pyramid (see Figure 1). In order to help maintain these strategies along with the best performing tools, KLA works with our customers in two areas:

- KLA helps customers by making continuous improvements on the process control platforms through product upgrades.
- KLA provides an extensive service package that helps our customers ensure that the process control tools are performing at the highest levels.

In addition, KLA also offers metrology and inspection tools that enable component sorting to prevent defective devices arriving at the assembly line and to keep track records of each device. Metrology helps verify whether device dimensions are within tolerance and thus confirming the quality of packaged products; inspection verifies that there are no particles, burrs or other defects present that could impact the yield.

MA: Can KLA detail its approach to supporting the power devices market and how experience in supporting other areas of the IC industry benefit their approaches to power electronics?

KLA: The company has been delivering solutions and support to the SiC and GaN power device market segment for some time. Leveraging our vast experience in developing new technology capable of solving complex inspection and metrology challenges across the IC industry to help drive yield improvements, we have developed a comprehensive portfolio of process control solutions specialized for the unique needs of power devices. In addition, through our subsidiary SPTS Technologies, we offer industry leading plasma etch, PVD and CVD wafer processing systems that are used in the manufacture of SiC and GaN devices.

There are several unique challenges in the manufacturing of power devices. Although the design rule is larger, there are special requirements beginning with the substrate and the early epitaxial process. These include, but are not limited to, thickness, wafer handling, substrate shape and quality, epitaxial dislocations, stacking faults and a number of other defect types which could limit the final device yield.

Working closely with our world-wide customers, both in development and in high volume manufacturing (HVM), KLA has engineered, delivered and improved our inspection and metrology offerings to provide the high quality inline data required to help drive yield and continuously improve cycle times.

MA: Packaging power electronics is often a challenge in and of itself. In the past, manufacturers often needed to create new package designs, especially for GaN and SiC. How does KLA support packaging requirements and what are its essential advantages?

KLA: The demand for packaging power electronics is widespread across different application types, including mobile and automotive, which results in the development of a wide variety of new packaging technologies to meet different requirements for overall performance, power, form factor and price.

The growth of 5G communication brings an increase in device power consumption, resulting in unique requirements for including more power management ICs. Therefore, development of advanced packages for these types of power devices is expected to

increase, and the resulting innovation will bring greater complexity and new process flows. Generally, IC packages are getting smaller, thinner and more complex, as seen with the integration of multiple dies and passive components into a system in package (SiP), but at the same time requiring higher power density and demanding stricter yield requirements. To meet the yield targets for new packaging technologies, more automated inspection of packages in the assembly and test processes will be required to ensure that defects are identified and sourced quickly during the manufacturing process.

Today's evolving automotive market is being driven by several key areas, most notably connectivity, electrification, and autonomous driving, which is resulting in increased IC content in every car. High reliability requirements for automotive push for Zero Defect standards in manufacturing. Because reliability affects both warranty and liability, as well as the brand image of car manufacturers – and potentially the safety of their customers – process control in packaging, from wafer level to component, will increase significantly in the coming years to find and eliminate the sources of defects and screen for costly excursions. Manufacturers must leverage every available opportunity for continuous improvement across the entirety of their manufacturing value chain to reach that goal.

and adopted. Tolerances on key features (i.e. size, thickness, warpage, interconnect size, alignment, etc.,) for these advanced packages are becoming tighter. Requirements for defect detection and classification accuracy are also increasing. Inline, non-destructive inspection and metrology characterization provide the signals required to enable customers to deliver advanced packaging innovation and differentiated solutions to the market.

High-end 3D profiling and metrology on wafer and panel can be measured with KLA's Zeta 5xx and 6xx systems. Wafer-level inspection and metrology process control with the Kronos™ wafer inspection system meets the requirements of high sensitivity and production-worthy throughput, while simultaneously addressing the challenges of wafer warpage, thin and thick substrates and numerous process variations typical of advanced packaging processes.

After dicing, the detection of hairline cracks in bare dies or in fan-in wafer-level packaging is achieved with the ICOS™ F160 die sorting and inspection system. It examines packages after wafers have been diced, delivering fast and accurate die sort based on detection of key defect types – including sidewall cracks, a new defect type affecting the yield of high-end packages.

To meet the yield targets for new packaging technologies, more automated inspection of packages in the assembly and test processes will be required to ensure that defects are identified and sourced quickly during the manufacturing process

For more traditional packaging types, the focus is largely on cost. Automatic inspection is available, providing the benefit of reducing overkill and then increasing yield. ICOS™ T3/T7/T8 and MV component inspection systems provide automated inspection and metrology capabilities across all different types of packages. With modular tool architecture, KLA can offer solutions to meet the requirements of many package types with varying size and interconnect styles.

Beyond traditional packages, mobile applications have been driving the development of smaller (dimensions below 3mm) and more complex packages. These include new technology such as fan-in wafer level packaging (FI-WLP), bare dies, fan-out wafer level packaging (FO-WLP) and SiP (system in package) for silicon-based packages.

We also expect similar levels of packaging innovations for SiC/GaN devices as they are further developed

Once packaged, the ICOS component inspectors provide higher accuracy and repeatability in characterizing key features of advanced packages. With high resolution defect detection, ICOS component inspectors enable discovery and classification of defects smaller than 10μm in mold or substrates and below 1μm for cracks in die.

The unique process control capabilities described thus far are critical to ensure performance of power electronics, but also to ensure optimal yield. Achieving high yields and meeting cycle time goals are challenging with new complex process schemes. Smarter, faster methods of analyzing large data sets and extracting critical information quickly to make decisions is required. Deep learning methodologies paired with advanced defect detection of packages helps to optimize the classification process, reduce overkill and maximize yield. KLA has extensive experience in working with customers to solve new packaging challenges and helping them succeed in

ramping new products while improving overall yield in a cost-effective manner.

MA: How does KLA support the unique inspection/ metrology challenges presented by SiC and GaN?

KLA: Starting with the substrate, dimensional wafer metrology systems from KLA's MicroSense offer precise, non-contact, automated geometry measurements including thickness, thickness variations, bow, warp, and 2D and 3D mapping on a wide range of substrates including sapphire, silicon, SiC, GaAs, glass, quartz, ceramics and graphene. For measurement and control of multilayer bonded wafers, our systems can measure total wafer stacks and individual layers throughout the wafer bonding, thinning and de-bonding process steps.

For metrology of power devices, our optical film thickness, overlay patterning and critical dimension instruments are successfully being deployed for inline process control at leading SiC and GaN customer fabs. We have developed a unique transparent wafer option to handle, transfer, align and measure various thin films on SiC on the F5x Pro film metrology system. The KLA Pro Archer™ overlay metrology platform enables production control of overlay and CD to help provide the data required for correcting the scanner.

For inspection, both SiC and GaN are complex material systems and each have very specific and unique process related defects that manifest in the substrate and after epitaxial growth process. Some of the similarities and differences between the two material systems include:

- Much higher intrinsic material defect densities in SiC based power devices
- Variation in quality among SiC substrate and GaN epi suppliers. SiC substrates are graded and sold by dislocation densities that are native to the substrate
- Morphological defects, crystallographic defects on SiC (such as carrots, triangles, stacking faults, basal plane dislocations), interfacial defects (such as cracks that originate at the interface of GaN and the substrate on which the epi is grown)
- Defects on SiC post epitaxy growth are directional while on GaN the defects are non-directional

KLA has developed unique solutions to meet the inspection requirements of both SiC and GaN materials systems.

The Candela® 8720 compound semiconductor material surface inspection system enables GaN-related materials, GaAs substrate and epi process control with high sensitivity to critical defects to produce GaN based power devices, communications and RF devices, and advanced LEDs (as well as upcoming microLEDs). With its proprietary optical design and detection technology, the Candela inspection tool utilizes signals from scatterometry, reflectometry, ellipsometry, slope and photoluminescence detectors to detect and classify yield-limiting, sub-micron defects to support production-line monitoring.

The next generation of the award winning Candela® CS920 – the industry's first integrated surface and photoluminescence SiC inspection tool - is enhanced with greater sensitivity for monitoring the substrate IQC (incoming quality control) and OQC (outgoing quality control) processes for a variety of defect types including particles, scratches, stains, pits, micropipes, stacking faults and other crystallographic defects. For the post epitaxial growth process step, this inspection system can detect and monitor process issues such as cracks, macro epi disturbances (such as droplets), epi pit, epi bump, crystal-oriented defects (such as single/bar stacking faults, BPDs, etc.), micropits and particles.

Defects in the substrate and post epi growth can significantly impact end of the line yield, so detecting and correcting such process issues at the source is critical--where cost is the lowest. Patterned wafer inspection of SiC semiconductor devices is important for reducing defectivity and maintaining traceability, but this need presents several unique challenges. Wafer thickness and warpage are outside typical SEMI standards. The transparent substrate can create challenges for focus systems and create unwanted noise when imaging the wafer. The 8 Series patterned defect inspection tool addresses these challenges through a specialized pre-alignment and chuck, selectable illumination wavelengths and depth of focus for inspection, multiple inspection channels and increased wafer handling flexibility.

With simultaneous brightfield and darkfield inspection capability, the tool captures all types of surface defects with a multi-level defect binning solution. With optional back side inspection capability, the 8 Series system can handle and inspect both the front side and back side of 6-inch SiC pre- and post-grind wafers offering high precision front side to back side correlation and die inking for process-induced killer defects on both sides of the wafer. As the demand for power devices continues to grow, we are adapting our portfolio to the needs of our customers, so they have the data they need to control their process. Both SiC and GaN have unique challenges compared to silicon; inspection and metrology data can help provide valuable information required to move the process from R&D to high volume production.

Replies from KLA Corporation were supplied by:
Robert Cappel, Senior Director of Marketing;
David P. Price, Sr. Director, Automotive Technical Solutions;
Mukundkrishna Raghunathan and Oliver Dupont, Product Marketing Managers."

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Smart manufacturing enabled in the sub-fab

The Industry 4.0 movement is rapidly becoming the de facto means to optimize cost-effective manufacturing. Power electronic device makers want to leverage any practical idea. The experts at Edwards Vacuum point their customers to proven methods that can rapidly reduce costs while improving uptime by focusing on a part of the fab that manufacturers don't always think of first in the quest for a healthier bottom line.

BY ALAN IFOULD, ERIK COLLART, ANTONIO SERAPIGLIA, AND MICHAEL MOONEY, EDWARDS VACUUM

IN THE BROADEST TERMS, smart manufacturing refers to collecting data from all aspects of the manufacturing process and by using advanced analytical and modeling capabilities, like artificial intelligence and machine learning, process performance and productivity are improved. It has been embraced by manufacturers in all industries and hailed as the fourth industrial revolution (Industrie 4.0).

Semiconductor manufacturers have a long history of collecting and analyzing process data, a key smart manufacturing concept, to improve performance in the fab. Now semiconductor manufacturers are realizing the potential benefits of extending smart manufacturing technologies to the support systems housed in the sub-fab.

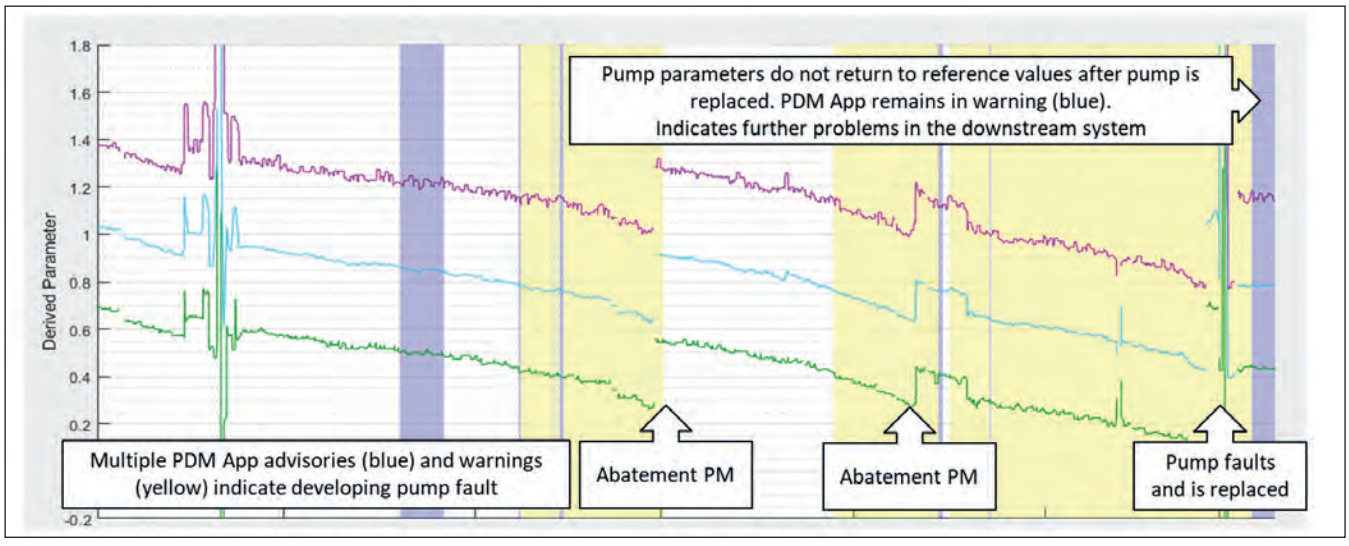

Figure 1: Output from a predictive maintenance application (PdM app) monitoring a vacuum pump

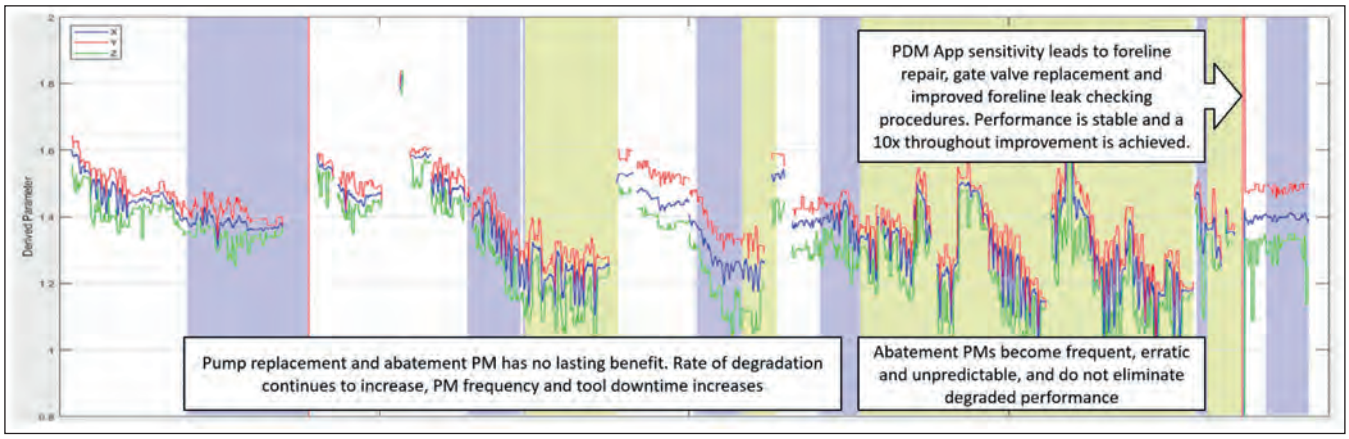

Figure 2: PdM data from a process tool in an HVM environment was delivering only 10% of the wafer throughput of other comparable tools

Driven by recent developments in the fields of sensors, data management, analytics and artificial intelligence, a new vision for manufacturing has emerged. This vision includes integrating supply chains; creating virtual factories with cyber-physical systems and digital twins; using big data techniques to interrogate tool, process, yield and facility data; and accumulating and applying critical domain knowledge. Smart manufacturing is a broad concept that is perhaps best generally described as combining technologies and solutions to optimize operations by reducing and/or managing risk and uncertainty. In more practical terms, it is using big data infrastructure and information technology to provide advanced analytics and create a knowledge network of subject matter expertise and operational excellence models. It connects people, machines and processes in a more effective way.

Semiconductor manufacturers have been using advanced automation and statistical control techniques for a long time. As fabs have become more expensive and the cost of unexpected downtime has increased, they have enhanced their capabilities using smart manufacturing concepts. They are also extending them to the critical process support systems found in the sub-fab. The sub-fab has evolved dramatically over the years, from what was originally simply a location outside the fab in which to house supporting equipment, to an environment that is in many ways as sophisticated as the fab itself. A typical HVM fab, starting 40,000 wafer per month, may have 1,500 process tools. It's sub-fab will have 2,000 vacuum pumps and 1,000 abatement systems plus other ancillary systems. Most of the critical steps in a chip manufacturing process require high vacuum conditions and the unexpected failure of a pump can bring significant disruption to the manufacturing process, imposing heavy penalties in lost productivity and scrapped product.

Smart manufacturing in the sub-fab enhances vacuum security with comprehensive monitoring of process critical vacuum and abatement equipment. Using specifically designed models and algorithms, it can predict catastrophic failure modes related to hazardous process chemicals, high flowrates of flammable gases, ingestion of solid materials and condensation of liquids and solids.

It can also deliver rapid root cause analysis for new and harsh process steps and materials, provide real-time intelligence on critical process vacuum state, accelerate yield ramp by correlating vacuum behaviour with wafer yield, and support fast installation of new sub-fab equipment.

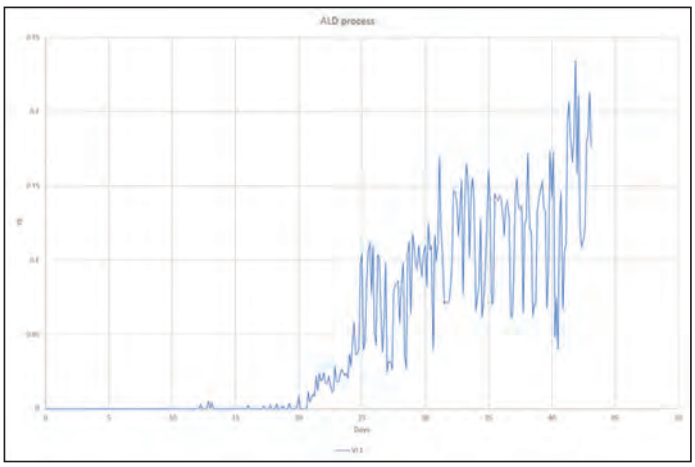

Figure 3 Vibration signal from a pump on an atomic layer deposition tool (left) and a photo of material deposited on internal components.

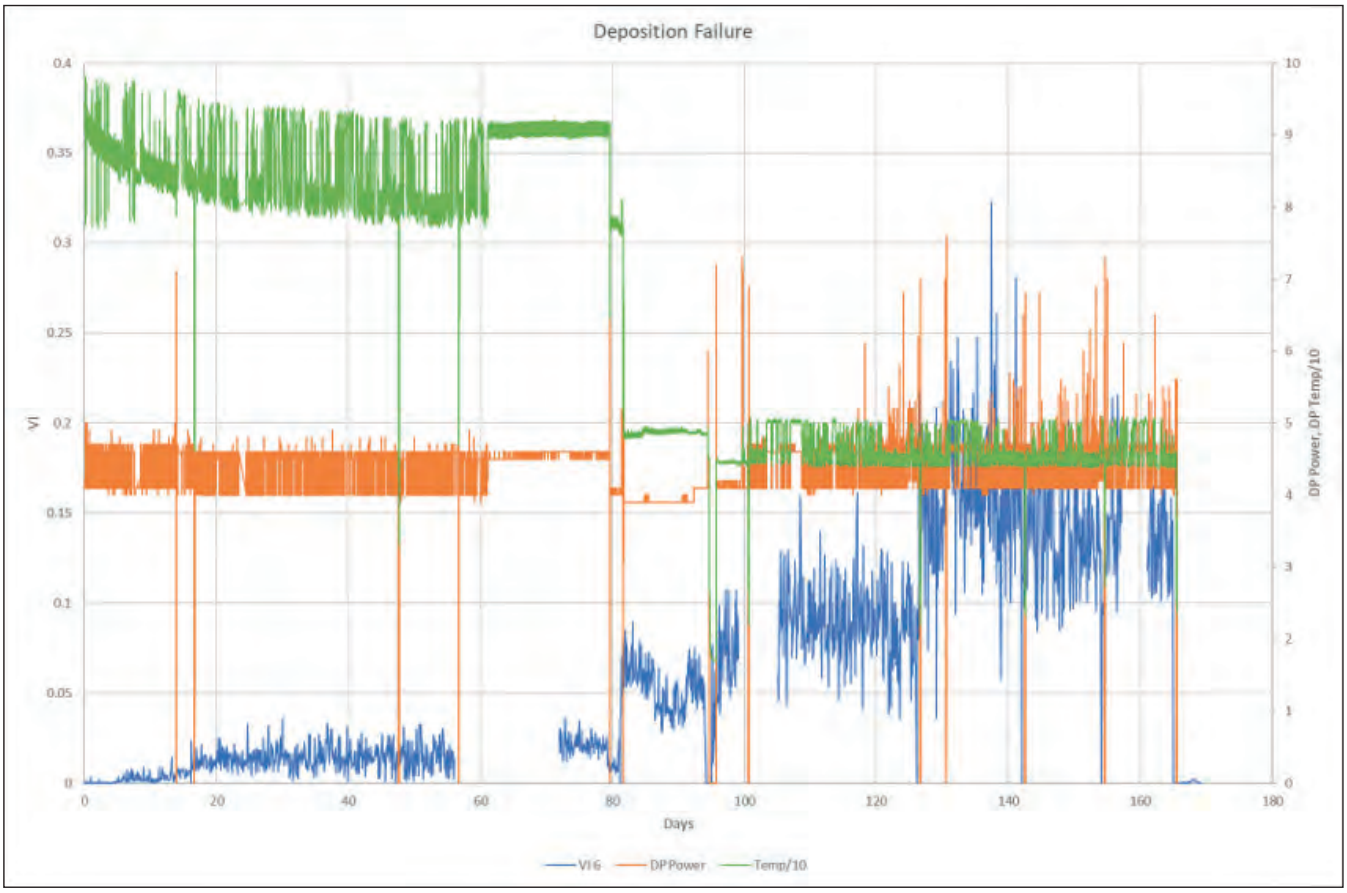

Figure 4: Dry pump power (orange) and temperature (green), and vibration data (blue) taken from a pump supporting an LP-CVD Si_3N_4 batch deposition process

A systems approach to the sub-fab

There is a growing understanding that vacuum pumps and abatement systems are not isolated, self-contained pieces of equipment. They react to each other and to the wider vacuum system that includes forelines, gate valves, other vacuum components and fab process tools. Monitoring pump parameters can reveal the health of individual pumps and also the health of up- and downstream components, including forelines, gate valves, and process chambers. Data acquired at the pump or abatement system can help determine the size and location of vacuum system leaks.

Algorithms based on vacuum science and thermodynamics can lead engineers to problems that, over time, can have a significant impact on yield. Figure 1 shows output from a predictive maintenance application (PdM app) monitoring a vacuum pump in an HVM environment. The plotted parameter is derived from a multivariate analysis and is responsive to various fault types.

The downward trend in this plot indicates gradual degradation, interrupted by a temporary re-setting. Comparing sub-fab maintenance records with parameter time stamps showed a one-to-one correspondence between reset events and preventive maintenance procedures performed on the abatement system for the same process tool, indicating that the degradation was connected to the state of the abatement equipment, rather than the health of the pump itself. This was corroborated by other pump parameters not part of the PdM app. The evolution over time further suggested that the abatement PM's themselves did not fully address the issue at hand: the derived parameters did not return to their default values and the downward trend resumed immediately. Ultimately, successful diagnosis of pump faults, combined with the successful segmentation of external downstream issues, resulted in reductions in unscheduled tool down time.

Figure 2 illustrates a case where a process tool in an HVM environment was delivering only 10% of the wafer throughput of other comparable tools. A multivariate PdM App was monitoring the vacuum pump health. The time-series plot of derived parameters clearly showed degradation over time, interrupted by abatement PM-driven re-sets. Initially, the degradation was not as severe and abatement PMs re-set the pump health as indicated by the multiple step changes. But degradation resumed almost immediately after each step improvement.

As time went on this degradation worsened, in spite of the increasing frequency of preventive maintenance on pumps and abatement units. Multiple PdM App alerts were issued. This and other indicators pointed to leaks in the upstream vacuum system. Ultimately a thorough review and repair of forelines and gate valves resolved the issue and resulted in an improved, integrated vacuum system leak check procedure. The wafer throughput gradually returned to match the throughput of peer systems, a 10x improvement for this particular tool.

Sensorization

One of the key requirements for smart manufacturing is the development and implementation of sensors to collect and record new signals, beyond the power and temperature sensors typically used to monitor pump health and performance. An innovative vibration sensor (EdCentra Vision, Edwards Vacuum) illustrates some of the requirements and challenges encountered in this “sensorization”.

Measuring vibration to monitor the health of rotating machines has a long and successful history. Intrinsic bearings frequencies can be calculated from rotation speeds, and wear-generated perturbations of these frequencies can indicate bearings faults. However, these methods do not translate well to a semiconductor environment where process-induced failure modes are more common than wear-induced. The effects of process-induced failure modes on standard vibration spectra are largely unknown and analysis is complicated by high noise levels.

The new method unlocks key predictive information from vibration data and can detect failure modes that cannot be seen by conventional vibration detectors. It uses a retrofittable “edge” sensor module that includes both sensing and data processing capability to reduce bandwidth requirements on the communications network. Its innovative data analytics methodology translates the complex, noisy vibration signal into a single dynamic coefficient that is easy to compare with existing predictive maintenance parameters. Further vibrational sub-band analysis can provide specific failure mode identification and root-cause analysis, thus providing valuable fault classification (FC) capability.

Compared to conventional methods, the new approach increases sensitivity and provides extended, and in some cases unique, predictive maintenance capability for mechanical pump failure modes. Figure 3 shows the vibration signal from a pump on an atomic layer deposition tool. This pump was pro-actively removed from service based on the progression and value of some of the vibration parameters, even though the next calendar-based maintenance was not imminent.

Other pump parameters (not shown), failed to indicate pump deterioration. A detailed analysis of the pump after removal indicated that it was very close to faulting. The picture on the right in figure 3 shows part of the internal pump mechanism with significant process deposition and confirming the vibration-based prediction. Early replacement prevented unscheduled process downtime and potential losses from wafer scrap. The data management system used to collect this data can combine it with other pump and abatement data in a multi-variate analysis to significantly enhance predictive power and accuracy.

Figure 4 demonstrates the sensitivity of vibration analysis in tandem with traditional pump parameters used historically to monitor conditions. The figure shows an example of pump parameters, dry pump power (orange) and temperature (green), and vibration data (blue). The failure mode in this case was deposition related. As shown in Figure 4, from day 80 onward changing process conditions caused a step-change in temperature. The power curve shows developing patterns at around the 120-day mark, indicating a predictive time horizon of about 40

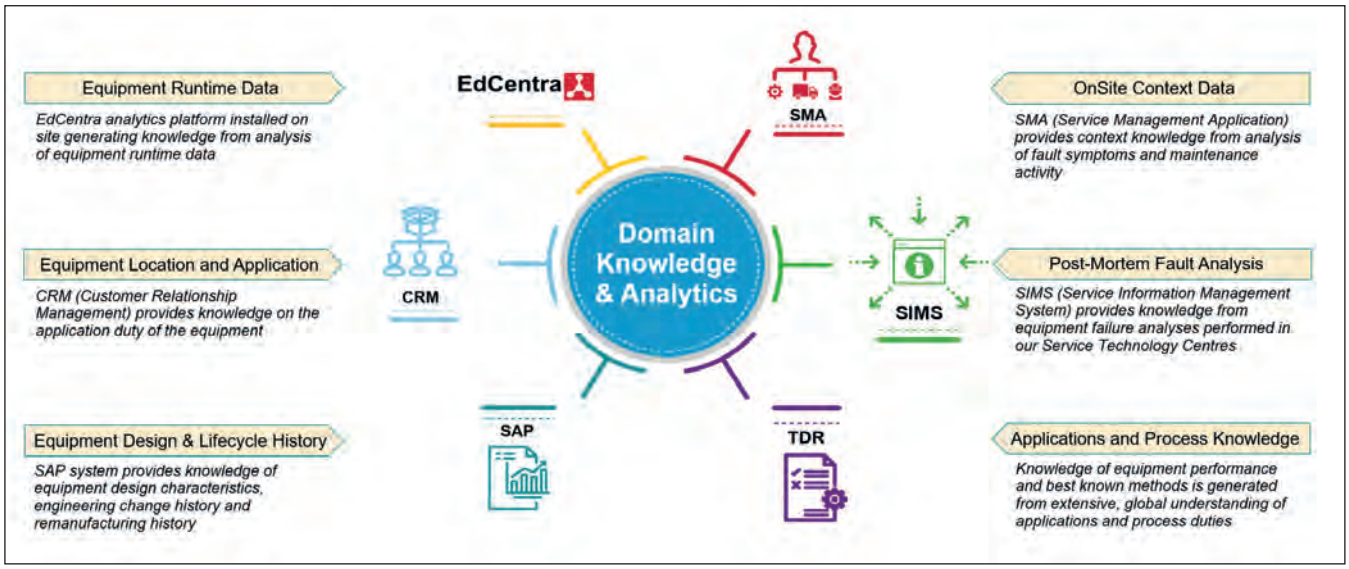

Figure 5: Information sources for domain knowledge

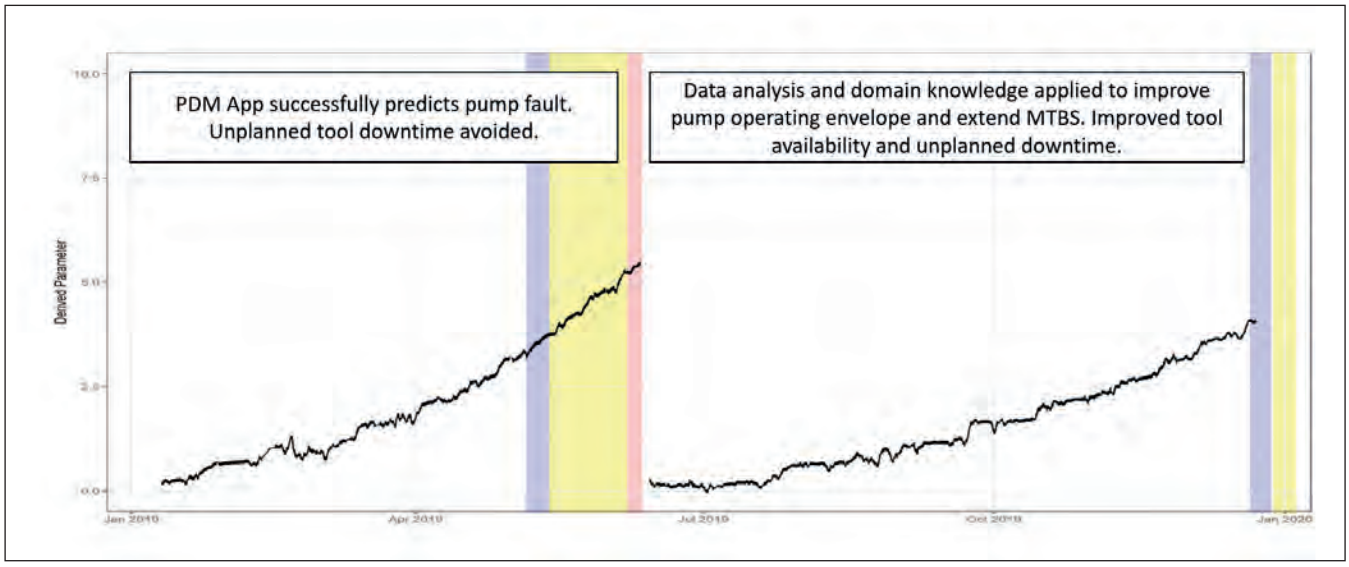

Figure 6: Application of domain knowledge improves pump operating envelop and extends MTBS

days. An important observation to make here is that the vibration data (blue curve) reacted immediately to the modal change and the increased impact of condensable process by-product adversely affecting the operation of the pump.

The heightened sensitivity of vibration gave a point-of-detection time period of around 75 days, 25 days greater than traditional pump parameters. Although vibration analysis is not a new technique, the new vibration sensor detected anomalies otherwise missed by traditional monitoring techniques. Importantly, it has added considerably to the ability to detect process-induced changes to the vacuum pump. Its implementation of edge computation reduces data volume, enables real time analytics and shortens detection latency.

Safety

No discussion of smart manufacturing can be complete without considering its potential impact on safety in the sub-fab. The sub-fab is a dangerous place, and safe working practices must be maintained alongside new business processes enabled by smart manufacturing. Examples of potential benefits include: providing advance notice of required equipment interventions so that activities can be better planned, thereby reducing risk and uncertainty associated with the time pressure of urgent activities; using technology to deliver safe standard operating procedures (SOP) and best known methods (BKM) for equipment installation; and incorporating safety data and observations along with asset performance data in the domain knowledge that drives a holistic approach to reducing risk and uncertainty.

Domain knowledge is central

Domain knowledge and subject matter expertise are key in providing the right context for any type of machine learning and data science application within smart manufacturing. They are key for several reasons, including the complexity of the manufacturing process, the dynamic nature of day-to-day operations and the general unavailability of large, unambiguous and consistent data sets. People will manage, operate and optimize machines with the

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help of digital technologies. Processes will define the interaction of machine to machine, people to machine, and people to people. This constitutes a domain knowledge supply chain essential to enabling smart manufacturing.

For sub-fab vacuum and abatement equipment, domain knowledge encompasses multiple areas of know-how, ranging from specific knowledge of how a process or a piece of equipment works to all the ways the process interacts with the world in which it exists. Vacuum science and thermodynamics provide the basic laws governing critical parameters such as pressure, flow, temperature, and pumping speed. These all display linear and non-linear responses, instantaneous changes, and long-term trends that need to be considered.

Equipment behavior is also ruled by the details of electronic sub-assemblies and mechanical construction. This specific domain knowledge is, for instance, required to distinguish between normal, instantaneous power spikes from pump-vent cycles or powder ingestion and abnormal power spikes from gradual film deposition over long periods of time. A third area relates to the sequence of wafer processing vs. idle and how it affects parameter behavior over time.

The last areas of domain knowledge, measured and inferred alert states and measured degradation states, relate to quantifying and calibrating the progression of abnormal behavior against PdM alert states. Depending on process and equipment type different parameter sets and thresholds may be needed to accurately capture this.

Figure 5 summarizes sources of information that provide critical input for developing domain knowledge.

Figure 6 shows a practical example of domain knowledge at work. PdM Apps, built using domain knowledge, were used to monitor the condition of the pump. The first blue/yellow/band indicates a successful fault prediction that eliminated an unscheduled tool down event. Domain knowledge was then applied to change the operating envelope of the vacuum system. Note the right-hand side of the graph shows a much slower degradation of performance before a second successful fault prediction. This delivers the additional benefit of a longer MTBS and thus tool availability.

Tying it together – operational excellence

Smart manufacturing connects people, machines and processes. The full benefit of any smart manufacturing strategy is only realized once these three elements work effectively together to reduce and/or manage risk and uncertainty. Considering the examples discussed, a PdM App may provide a good indication of a fault condition, but further action is needed to eliminate the root cause of the problem and design out the cause of faults from machines or the processes that support them. New sensors provide more information than ever, but processes are needed to bring new learning to fruition. It is always worth reiterating safety: safe working practices must be maintained alongside new business processes enabled by smart manufacturing. A strong subfab management strategy includes a strong operational excellence model to drive safe and stable operations. Operational excellence incorporates four key areas: standards and procedures; team competency and capability; operational models; and knowledge systems. This is the holistic approach required to provide the solid foundations from which data-driven decision making and improvement activities can be achieved.

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Summary

Smart manufacturing in the sub-fab combines real-time data with specific domain knowledge to optimize equipment performance. Improved performance enables significant improvements in productivity and yield. A successful implementation of smart manufacturing requires that sub-fab vacuum and abatement systems be treated as a whole as well as individually. Application of big data techniques, data mining, artificial intelligence and machine learning will certainly reveal new relationships within the data, especially as the number and types of sensors grows and data is integrated across the fab, sub-fab and entire manufacturing ecosystem. Operational excellence models will provide the safe and solid foundations needed to realize the full benefits of new learning.

Opening up **SiC substrate** production

A manufacturer of crystal growth equipment pivots to materials manufacturing, creating a more competitive supply chain for the production of SiC power electronics

BY SANTHANARAGHAVAN PARTHASARATHY FROM GT ADVANCED TECHNOLOGIES

SILICON, the most widely used material across the entire electronics industry, has dominated power electronics for decades. But its vice-like grip is slipping. The silicon power devices used in all forms of power conversion – that includes AC-DC rectifiers, AC-AC transformers, DC-DC converters and DC-AC inverters – are struggling to keep up with demands for higher power ratings, faster switching frequencies and elevated operating temperatures. Failing to fulfil these requirements has undesirable implications, as circuits then need additional cooling and take up much more space, because they require large 'passive' components, such as inductors and capacitors.

Addressing all these weaknesses is a portfolio of materials with wider bandgaps, such as SiC. The wider bandgap is a wonderful attribute, delivering multiple benefits. For SiC, the bandgap is three times

that of silicon, providing a breakdown field ten times that of the incumbent (see table 1). Additional merits of SiC devices are efficient switching at far higher frequencies than silicon equivalents, enabling the use of far smaller passives, and a thermal conductivity three times better than silicon. Drawing on all these attributes allows SiC to hold the key to smaller, lighter circuits that are more efficient, handle higher voltages, and have reduced requirements for thermal management.

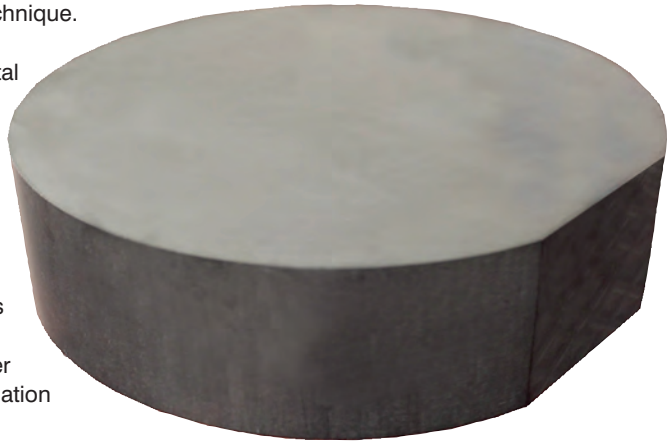
Such circuits are in growing demand as markets and applications push toward the 'electrification of everything'. Although this is most evident in the electric-vehicle industry, which is literally driving the transition from traditionally used silicon-based power electronics to SiC, other industries are also benefitting from this wide bandgap material. They include: power conversion systems featuring in other forms of transport, such as electrified trains, ships and aircraft; renewable energy applications, including solar photovoltaics and wind energy; and industrial/commercial applications, such as power supplies for servers, uninterruptible power supplies for data centres, motor drives and medical imaging systems.

In addition to all of these all-SiC devices, SiC provides the foundation to a variety of devices based on GaN. High-frequency GaN-on-SiC transistors are deployed in 5G telecommunication systems, such as repeater stations; and also in digital TV, radar and optoelectronic devices. In 5G applications, the combination of GaN epilayers and a semi-insulating SiC substrate creates devices that are superior to silicon LDMOS, and deliver increased capacity and coverage. Switching from silicon LDMOS to GaN-on-SiC doubles the number of users per tower and increases data transmission by more than an order of magnitude.

Substrate supply

As awareness of the superior properties of SiC grows, the demand for power electronics made from this material is ramping fast. Only a few companies are meeting this demand by growing high-quality SiC crystals, which begs the question: why aren't SiC crystals produced in volume?

The answer is multifaceted, and relates to the challenges of growing SiC. The wide bandgap material cannot be produced by the melt growth processes used to make boules of elemental semiconductors, such as silicon, which is manufactured by the Czochralski method. That's because a stochiometric melt is not realised under normal conditions. Instead of melting, SiC sublimes at about 2100 °C. For this reason, the growth of SiC requires a vapour-phase crystal growth process – generally a physical vapour transport or sublimation technique.



The fundamental crystal growth steps are essentially the same for vapour growth and melt growth. The process begins by generating reactants, either through sublimation or melting, and

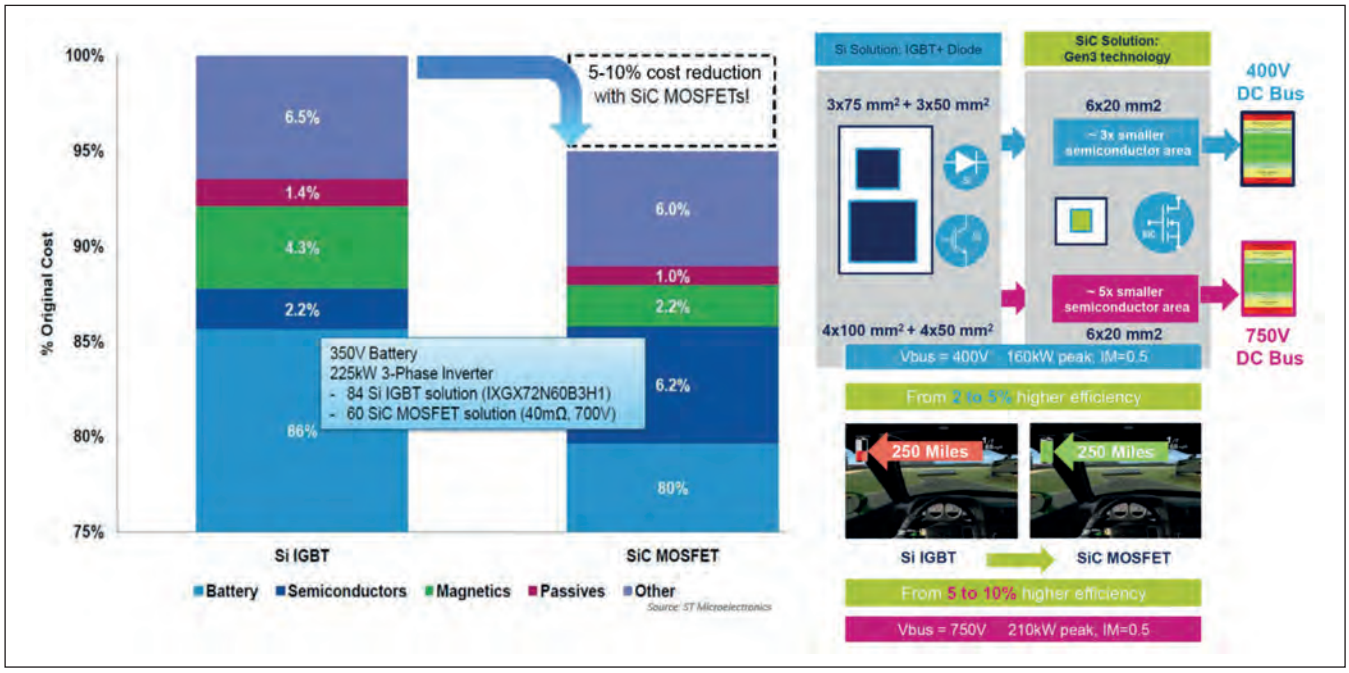


Figure 1. Switching from silicon to SiC offers savings at the system level. Source: ST Microelectronics

transporting them to the growth surface using specific temperature gradients. After this adsorption occurs at the growth surface – known as supersaturation – nucleation takes place, followed by crystal growth, which proceeds via either the advancement of the gas-solid interface or the solid-liquid interface.

Differences in the processes used for SiC and silicon boule growth are behind differences in the cost, size and availability of these substrates. For silicon, ingots produced in state-of-the-art crystal growth equipment have a diameter of 450 mm and a length exceeding 2 m, and are realised at a growth rate of around 100 mm/hour. Growth is initiated using a thin seed with a 10 mm by 10 mm cross section.

In contrast, SiC crystals are grown with a diameter of 150 mm, and have a length up to 50 mm, with growth proceeding far more slowly – it occurs at 100-300 μm/hour. This process begins with a starting seed that has a diameter of 150 mm or more and a thickness of 1-2 mm.

One significant barrier to entry for any company wanting to manufacture SiC substrates is that the high-quality starting seeds, which are needed to initiate the process, are not commercially available. Trying to get around this by using a commercial substrate as a seed for bulk crystal growth is not an option, as this is prohibited by SiC wafer manufacturers. Hence any new entrants to this market must spend considerable development time and resources generating high-quality seeds.

Like silicon, the SiC industry needs 'pure play' material suppliers. GT's supply chain strategy will enable this, opening up opportunities for existing silicon substrate providers to add SiC to their portfolios, leveraging established scale, mature value chains and established relationships with the IDMs who buy silicon substrates. Similarly, IDMs can rapidly add wafer capacity and increase their level of vertical integration.

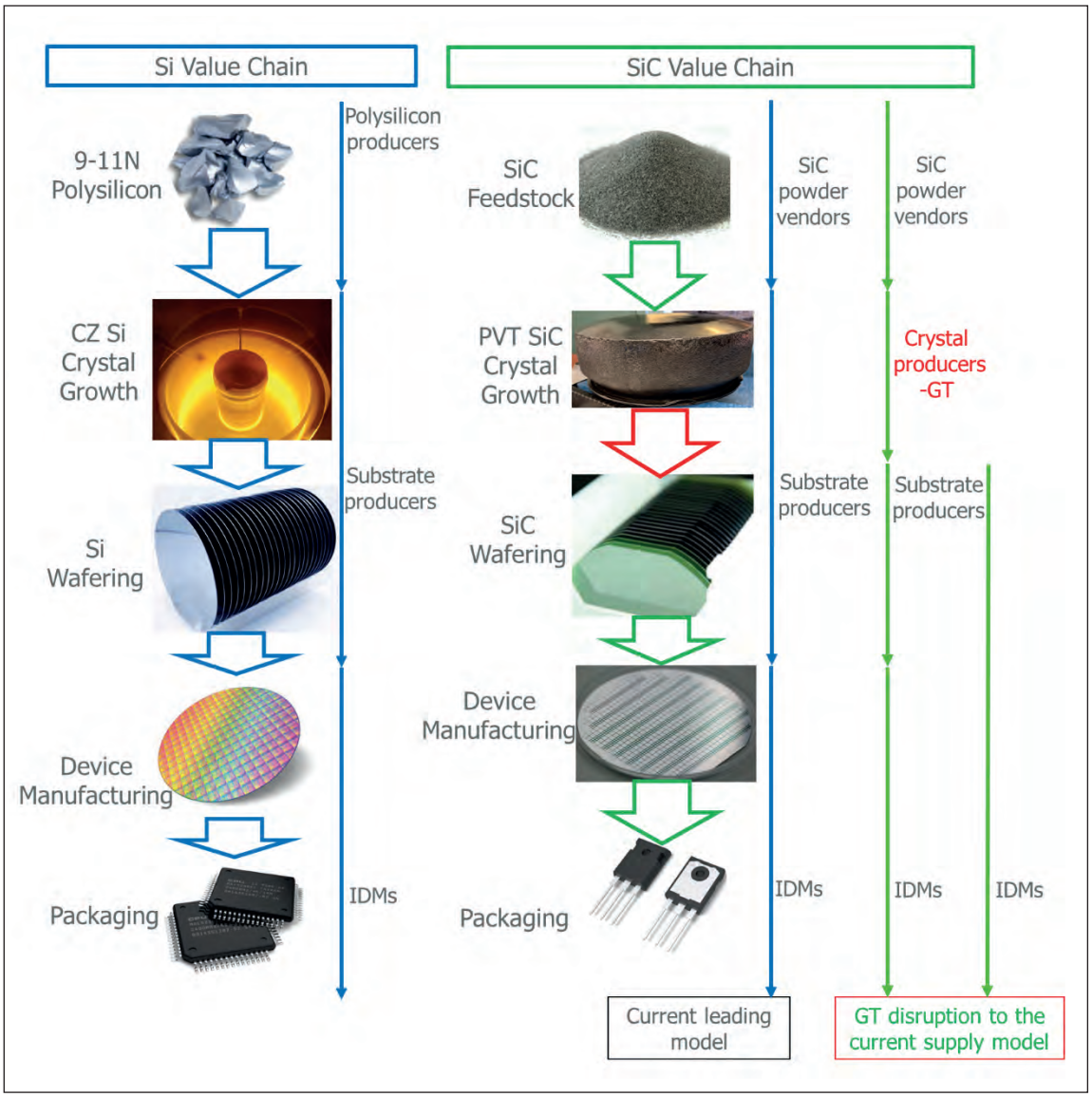


Figure 2. The SiC value chain has different challenges to that for silicon.

Along with slow growth rates and limitations to crystal size, difficulties associated with yield in the vapour growth process account for the far higher production costs of SiC crystals, compared with those made from silicon. Yet, despite the far higher substrate cost, even today a circuit designer that switches from using silicon devices to those made from SiC gets a 5-10 percent cost reduction at the system level. So the material already pays for itself, and its winning margin is only going to grow as the costs of SiC substrates and devices fall significantly over time. Note that in addition to the cost savings, SiC devices enable smaller, lighter systems, primarily due to their higher power densities (see Figure 1 for details of cost savings).

Another challenge associated with SiC relates to the many forms of this material. There are three crystal structures – cubic (3C), rhombohedral (15R) and hexagonal (2H, 4H, 6H, etc.) – and the number of polytypes exceeds 200. The 4H polytype of SiC, used for power electronics, accounts for around 60 percent of the SiC market. Devices are made on *n*-type SiC, produced by doping with nitrogen gas. This results in a resistivity in the 0.015 to 0.025 Ω cm range – it is typically 0.020-0.022 Ω cm. Sales of substrates for making RF devices account for 40 percent of the SiC market. These devices involve the growth of GaN-based heterostructures on 4H semi-insulating substrates. Produced by either doping with vanadium, or the absence of doping, they have a resistivity exceeding 10,000 Ω cm. For opto electronic device application, 6H polytype is used.

The quality of SiC lags that of silicon. The latter can be grown free of defects, while SiC suffers from fundamental issues associated with vapour-phase growth, multiple polytypes and a spiral growth mechanism. Part of the problem is that the stacking fault energy needed for the atoms to migrate to, and sit in, the right place is far lower in SiC than silicon. This introduces a wide range of defects,

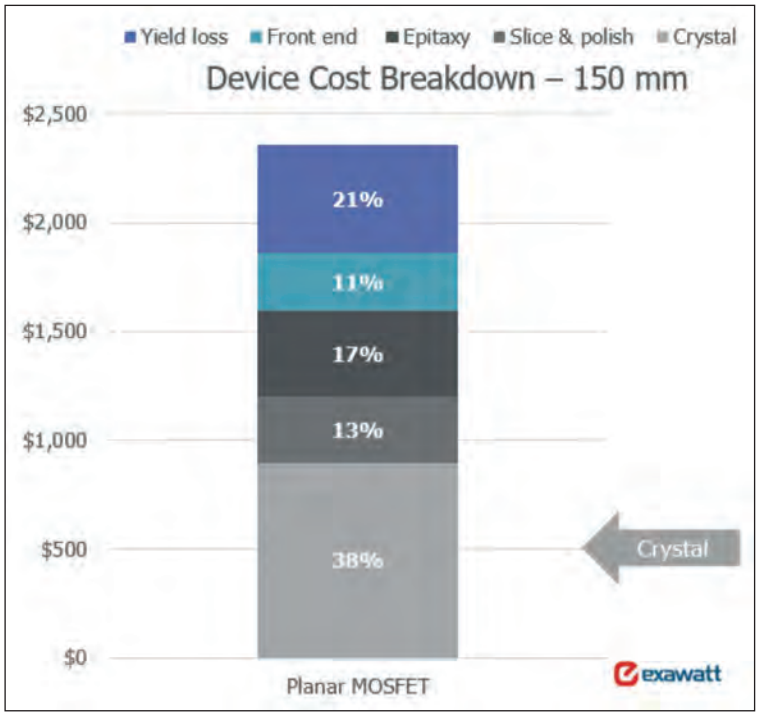


Figure 3. The cost breakdown for a SiC MOSFET produced on a 150 mm wafer. Source: Exawatt

including micropipes, carbon inclusions, and extended crystal defects, such as threading screw dislocations, threading edge dislocations, basal planar defects and stacking faults. Mitigating these defects is not easy, requiring a combination of equipment expertise and process knowhow. Just one without the other is insufficient for delivering the results demanded by high-growth markets.

Accelerating cost parity

At GT Advanced Technologies, also known as GT, we have developed and refined a high-yielding crystal growth process for large-volume, low-cost SiC boule production. This is helping us meet our primary objectives of accelerating cost parity between silicon and SiC, and greatly increasing the supply of this high-demand material.

Our efforts have enabled us to produce 150 mm diameter SiC substrates using mainstream production processes. As the availability of larger-diameter wafers is key to lowering device cost and improving die yields, we have also started development work on 200 mm boules.

The price of the SiC substrate is governed by the costs associated with the furnace architecture and infrastructure – factors such as the cooling water supply, the cost and need for uninterruptible power, the space occupied, the exhaust system and HVAC. There are two options for creating the high temperatures needed for SiC sublimation: a resistively heated furnace, with heat transferred from the heater to the crucible by radiation; and inductive heating of the crucible, which acts as the heater. One downside of resistive furnaces is a high fixed cost profile, stemming from equipment capex, the large footprint and infrastructure. Using this form of heating, there is limited opportunity to trim costs through operational and technical improvements. The promise of savings is far greater with inductive platforms. They offer a much lower fixed cost burden, due to lower capex, higher productivity, a lower electrical consumption, and a smaller footprint.

By adopting the inductive approach for reasons just outlined, we have positioned ourselves as a cost leader today, with a tremendous headroom for further improvements. Our production process enables high yields, high-quality and low cost, thanks to extensive thermal modelling skills, combined with excelled equipment design and process control innovations. The boules we produce have low defects, both for micropipes and other crystalline defects, and are manufactured in a cost-effective manner, due to a very high run-to-run reproducibility.

We are also able to draw on established supply-chain resources, equipment design and build capabilities, and process expertise. These strengths put us in a great position to scale quickly with demand and further improve our production processes over time. This will steadily increase our competitiveness in providing a low-cost, high-volume supply of SiC bulk materials.

The challenges of SiC substrate production are not limited to crystal growth. Processing boules into wafers is not easy, due to in-built thermal stresses arising from the growth process and a high material hardness – it is second only to diamond. Substrate production begins by grinding the SiC crystal to a specific diameter and then undertaking multi-wire sawing, using either a diamond slurry, a diamond-fixed abrasive wire, or laser-based wafering. This is followed by coarse and fine grinding of the surface, edge grinding and chemical-mechanical polishing.

Device makers will take the epi-ready substrates, load them into an MOCVD chamber, heat this to 1600 °C, and grow an epilayer using propane as the source of carbon and silane or trichlorosilane as the source for silicon. Depending upon the intended device breakdown voltage, the thickness of this drift layer will be somewhere between 5 μm and 100 μm (the drift layer thickness is approximately 1 μm per 100V, so for a 11 kV device, the epilayer thickness needs to exceed 100 μm).

To realise excellent reliability and drive improvements in yield and cost, device production may draw on recent refinements, such as gate oxide and thermal oxidation processes. Such techniques have helped expand the portfolio of SiC devices, which include Schottky barrier diodes, MOSFETs, HEMTs, MesFETs, JFETs, cascodes and BJTs, with operating voltages spanning 600 V to 30 kV. Power modules have also been produced from SiC devices, using developments

	Ge	Si	GaAs	4H SiC	4H SiC comments
Bandgap (eV)	0.67	1.1	1.4	3.3	Larger bandgap, lower leakage current, higher operating temperature and radiation resistance
Breakdown field E_c (MV/cm)	0.1	0.3	0.4	2.5	Higher breakdown field, lower on-resistance and higher blocking voltage
Thermal conductivity W cm^{-1} C^{-1}	0.58	1.3	0.55	3.7	Higher thermal conductivity, which increases heat spreading and power density
Relative dielectric constant ε	16	11.8	12.9	9.7	Lower dielectric constant – less parasitics
Electron velocity υ_s (cm/s) x 10^7	0.6	0.9	1	1.5	High electron saturation drift velocity leads to smaller devices
Electron mobility μ (cm^2Vs^{-1})	3900	1400	8000	1000	
Johnson Figure of Merit (Maximize Frequency and Voltage)	1	5	7	63	
Baliga Figure of Merit (Minimize conduction losses)	1	7	106	2429	

Table 1. Physical properties of germanium, silicon, GaAs and SiC.

in packaging technology, such as direct-bonded copper and direct-bonded aluminium-on-AlN. These modules can operate at temperatures beyond 200 °C.

The supply chain for SiC power electronics is markedly different from that for silicon (Figure 2). The former is held back by the limited availability of SiC crystal, a major bottleneck that we are eliminating through our supply chain strategy. In comparison, integrated device manufacturers (IDMs) in the silicon industry are buying material from multiple substrate producers. Complicating matters, the leading incumbent SiC substrate vendors also make their own devices, so they compete against their downstream customers.

Like silicon, the SiC industry needs 'pure play' material suppliers. GT's supply chain strategy will enable this, opening up opportunities for existing silicon substrate providers to add SiC to their portfolios, leveraging established scale, mature value chains and established relationships with the IDMs who buy silicon substrates. Similarly, IDMs can rapidly add wafer capacity and increase their level of vertical integration. In either case, costs should rapidly decline as scale is added and industry freed from its dependency on just a few merchant suppliers.

This transformation of the SiC industry will deliver much success in the power electronic industry. Today, a single epi-ready 150 mm SiC substrate retails for $800-$1,100, accounting for a significant proportion of the device cost (the cost breakdown of a MOSFET is given in Figure 3). The cost of this substrate can tumble – we expect it to fall to just $300 in the years to come. One of the keys to this price reduction is increasing the useable height of the grown crystal, as run costs are relatively independent of crystal height.

Additional drivers are lowering capex, reducing operating costs, increasing productivity, tightening process control and increasing factory yield – crystal growth yield must be pushed above 98 percent, while crystal fabrication yields needs to go beyond 95 percent.

Our expertise in SiC crystal growth has led us to make the strategic decision to focus solely on this, drawing on our knowledge and experience in crystal growth equipment and SiC growth. We are offering the world's wafer producers a large supply of high-quality SiC crystal. This offering broadens and deepens the global supply of SiC wafers, helping drive down costs.

The power device industry is already welcoming these market developments. Illustrating this, in August 2019 GTAT signed a long-term agreement with GlobalWafers to supply its CrystX SiC crystal, and in early 2020 signed a long-term supply agreement with ON Semiconductor, one of the leading IDMs.

Evaluating new switching technologies

It takes more than a change in part number to move to a wide bandgap technology; what's required is a systemic approach, considering all aspects of design

BY STEFAN OBERSRIEBNIG FROM INFINEON TECHNOLOGIES

TRANSISTORS ARE EVERYWHERE. They are in our mobiles, tablets and PCs, providing the key ingredient in integrated circuits, with each device tuned for a specific function, such as fast switching or a low operating voltage. Transistors also appear in a discrete form, serving in power switching applications. Here there is also a need for optimisation, a task made more challenging by an ever-growing range of products. But select the right one and the rewards are greater than ever.

This expansion in the range of power transistors has taken place against a backdrop of 'More than Moore', an era where the use of new materials offers a route

to improved performance. During this time, we have learnt that the latest fabrication node may not provide the most optimal solution; instead, it may be more prudent to choose the appropriate node for each function and integrate at a modular level.

When it comes to discrete transistor technologies, particularly for high-power applications, the expansion in choice comes from the introduction of new materials. It may be perceived that the technologies on offer, namely silicon, SiC and GaN, follow a path comparable to integrated digital transistors; that each new step is a linear improvement on the last, and should be adopted without question as the right replacement. But this is a misconception. The reality is more nuanced, with the optimal solution hinging on adopting the lessons learned through the development of More than Moore to the power domain. One must not simply view the newest technology as the best, without first giving it closer inspection. When engineers do this, they need to consider many aspects associated with design, so that they select the technology that is best for the respective application.

For makers of silicon, SiC and GaN power electronic devices, two of the biggest applications are power conversion and power management. Many devices are deployed in conversion topologies, based on variations of the common switched-mode power supply. The basic switched-mode power supply takes advantage of a transistor's ability to turn on and off rapidly and precisely, with variants manipulating specific features to deliver higher efficiency under specific conditions. New wide bandgap technologies are enabling innovative ways to exploit these topologies through faster switching and higher power capabilities.

It is often overlooked that even without changes to switching frequencies and turn-off/turn-on timings, the replacement of silicon devices with those with a wider bandgap can still deliver improvements. These gains relate to specific features, such as the integrated body diodes of SiC MOSFETs that allow them to take the place of conventional diodes in synchronous rectification designs. Merits of the body diode of the SiC MOSFET include a negligible reverse recovery charge and a high forward-voltage drop when

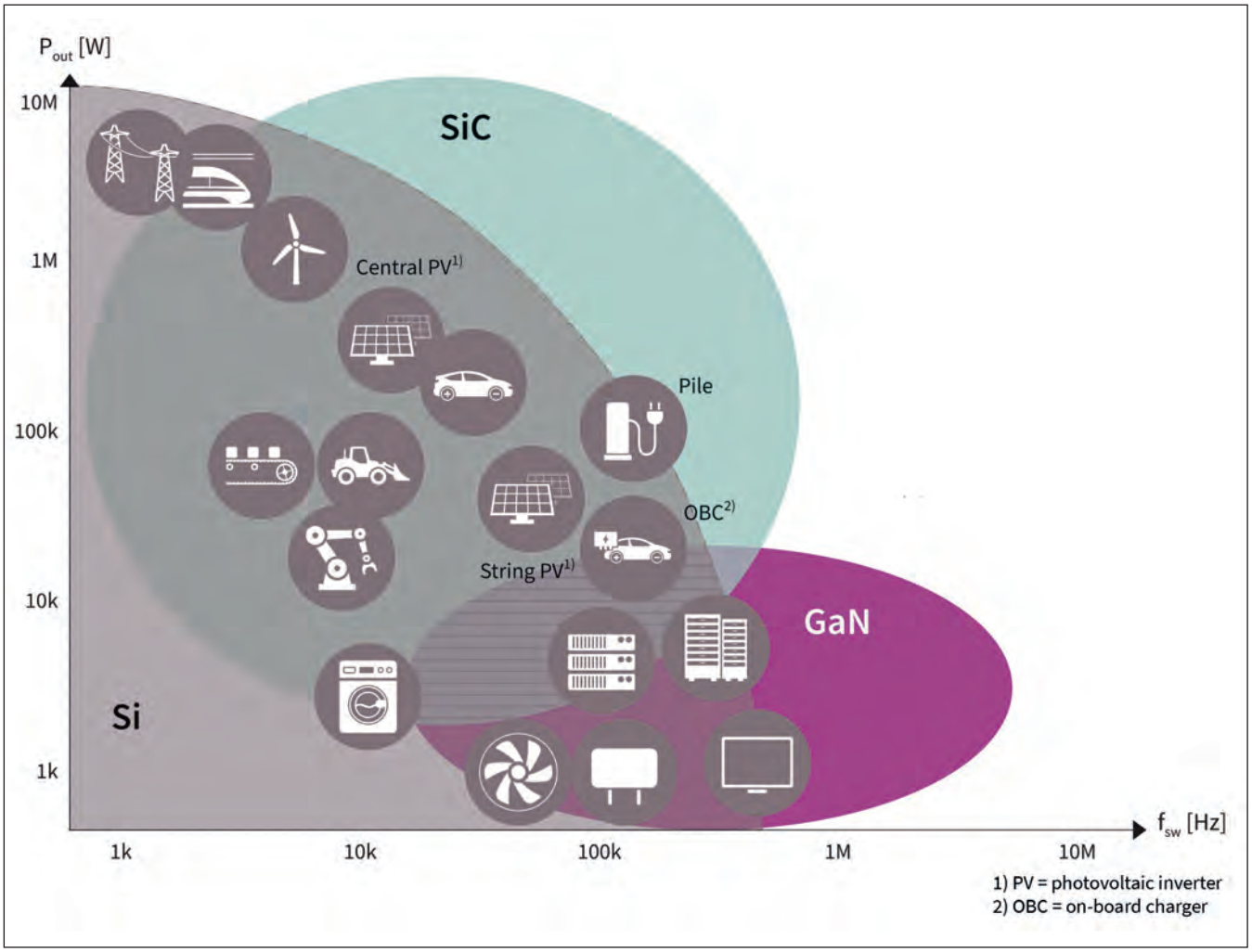
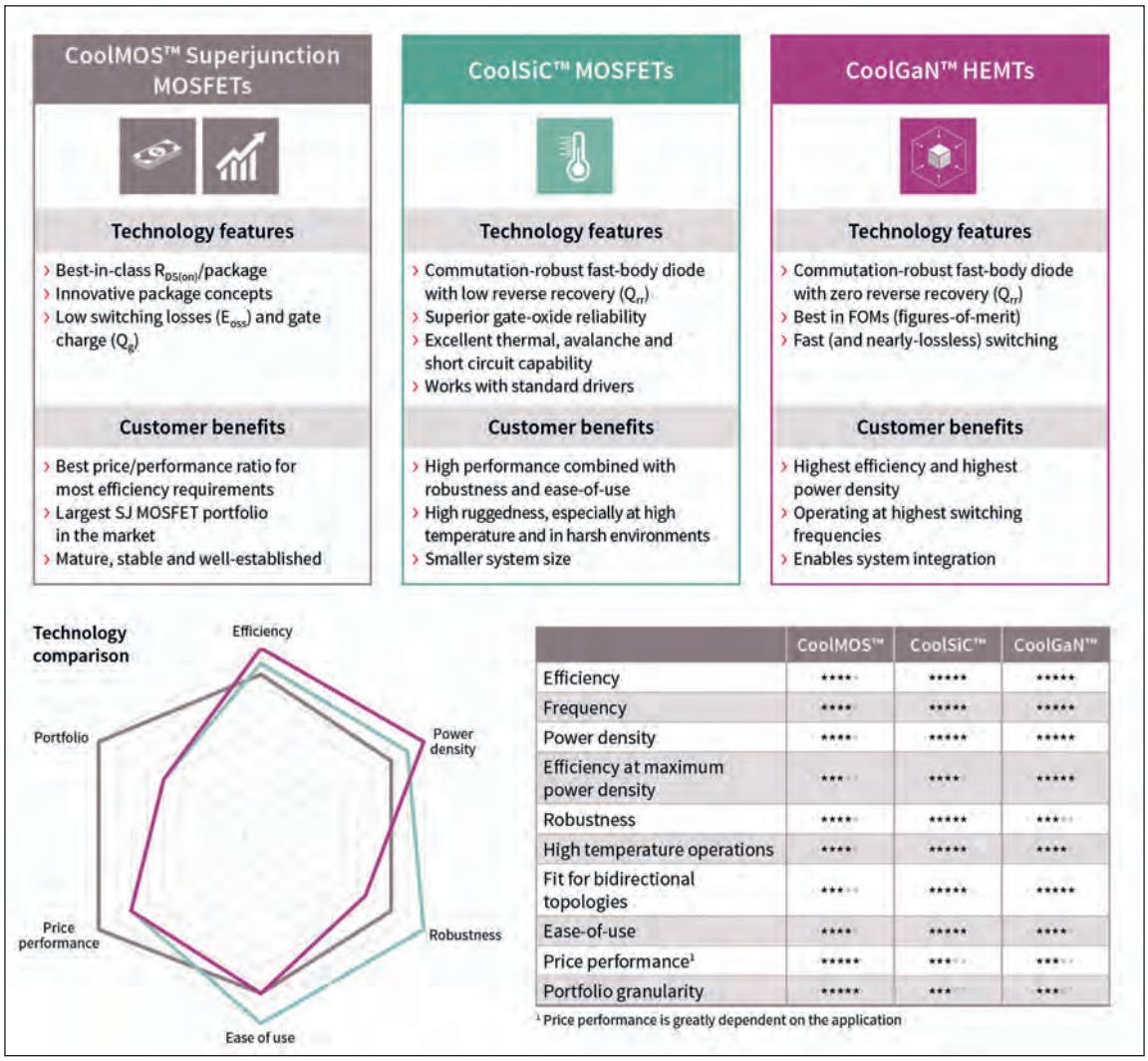


Figure 1: Mainstream silicon, complemented by SiC and GaN, delivers increased efficiency and a higher power density.

Figure 2: Different power switching technologies and application areas.



conducting, which dissipates the energy build-up that limits the switching frequency of silicon devices. It is the switching characteristics of SiC that are behind its capability to deliver higher efficiency.

Many different types of switching topology are in use today, including inverters, active clamp flyback converters and phase-shifted bridge topologies. This diversity is unlikely to change, as each topology has its own merits.

When designers select a topology, their decision tends to be governed by the requirements of the application rather than the ideal substrate. Due to this hierarchy within the decision-making process, GaN is not always the best option for applications requiring high voltages and currents. The reasoning is that although GaN is better than silicon in half-bridge topologies when implementing hard-switching, SiC has the upper hand for soft- and resonant-switching topologies (see Figure 1 for an evaluation of the suitability of today's available semiconductor technologies to several key applications).

As new applications emerge, such as electric vehicles and renewable energy, and existing applications evolve, like data centres and cellular telecommunications, the requirement isn't simply for more power. Instead, there is a need for more power, delivered in the same or a smaller form factor, using different voltage levels, currents, stability and response times. This list of requirements puts pressure on power supply developers, who may need to explore new topologies. However, the demands also create an opportunity to evaluate new transistor technologies for fulfilling these needs.

At a high level there is much to be garnered by considering the characteristics of all the classes of transistor technology. Taking this approach provides a snapshot of their respective merits and goes some way to explaining why the industry is pursuing their development.

Transistor characteristics

At Infineon Technologies, a multi-national device manufacturer operating in the power electronic industry, we have devoted much time and effort to developing a range of technologies based on silicon, SiC and GaN, as well as the corresponding drivers needed to maximize the potential of each technology.

We can advise what will provide the best cost-to-performance ratio – it may be silicon; in some high-power applications it could be SiC; and in other scenarios – for instance for high frequency designs, GaN might deliver the best performance, making it the right option.

We have a rich history of innovation, including invention of Superjunction technology and the launch of the world's first SiC Schottky barrier diode (in Figure 2 we offer a graphical representation of where each semiconductor technology fits in terms of power transistors).

Our experience is that the demand for silicon-based power devices remains strong. It is still the best technology for many applications, and it has reached a level of maturity that makes it highly cost-competitive. Although at one stage regular silicon appeared to be running out of steam, the introduction of superjunction technology injected a new lease of life, reducing the on-resistance. This led to a trimming of switching losses, allowing this class of device to serve in high-voltage, high-power applications.

When SiC launched, it lowered the on-resistance of the transistor for a given area by a factor of three. Another advantage, also coming from its wider bandgap, is that it enabled devices to handle far higher voltages without failure.

Recently, GaN has entered the fray, sporting a very similar bandgap to SiC. However, its transistor architecture is markedly different from that of SiC MOSFETs and superjunction devices. GaN FETs feature an undoped layer that increases electron mobility and results in an even lower on-resistance.

At first glance, the reductions in on-resistance associated with moving from silicon to SiC and then on to GaN suggest that the latter is always the preferred solution for power switching. However, while the material used for the transistor determines its strengths, the characteristics of each class of device differ under the same operating conditions. Due to this, when GaN is employed in a topology implementing a continuous conduction mode, it only delivers a superior efficiency to a silicon MOSFET under certain load conditions. So, when designers make a decision, they must take into account how the technology behaves under all operating conditions; they should not view any two technologies as drop-in replacements for one another.

With these factors at play, designers must evaluate the difference in the performance of SiC, of GaN and of silicon MOSFETs and superjunction devices in different types of power-converter circuits – the right approach for one application is not necessarily the right one for another. Due to this, the best results do not come from simply standardizing on one wide

bandgap technology, as this will not lead to efficiency gains across all applications.

We are in an enviable position of offering industry-leading devices made from silicon, SiC and GaN; and we can draw on our system expertise to support our customers through every generation of their application. This allows us to supply the best technology for the most appropriate topology, whether that is silicon, SiC or GaN, making us a great power-design partner. We can advise what will provide the best cost-to-performance ratio – it may be silicon; in some high-power applications it could be SiC; and in other scenarios – for instance for high frequency designs, GaN might deliver the best performance, making it the right option.

Note that the right decision is not set in stone. SiC and GaN are still evolving, and it is also crucial to consider the driver technology used for power switching, as matching the best transistors with the best drivers plays a big part in optimising design.

Power integration

Each application comes with its own requirements, which dictate the right topology and in turn the most appropriate semiconductor technology. However, there is also a trend towards more integrated solutions, which combine transistors and drivers into modular solutions. In much the same way as More than Moore is bringing together the most appropriate nodes for given functions, power modules are starting to simplify power supply design for various applications with similar requirements.

The semiconductor industry is moving towards greater integration at a modular level. This is already apparent in the wireless communication sector, where entire radio systems are being integrated closely alongside controllers, allowing the end device to pass certification with less effort. In many cases, wireless modules are supplied pre-certified, making them a 'plug and play' solution.

Within the power systems sector, a similar trend is underway and set to continue. We are well-positioned to respond, thanks to a portfolio of products and the experience required to develop and bring to market high-quality integrated power modules.

Merits of power modules are not limited to simplifying the design process for the customer. By optimising the design, we also provide two major performance benefits: a reduction in size compared with discrete components, resulting in higher power density at 'no extra cost'; and a higher efficiency, which is an overriding requirement in power conversion and one of the key drivers behind the development of wide bandgap technology.

Using a module also has practical benefits. It is not easy for an engineering team to realise a high level of efficiency, because they need to understand how the power supply will behave under all possible modes of operation when selecting the design that delivers a performance curve that best fits their objectives. With discrete devices this could be an iterative process, with no guarantee that the results deliver the best efficiency under all operating conditions. By turning instead to a power module, complexity is eliminated, allowing an out-of-the-box solution to deliver a superior efficiency while increasing ease of use.

There is no doubt that the introduction of wide bandgap semiconductor technologies improves the power conversion landscape. They are complementing silicon-based technology by extending power and switching frequencies to support new applications with improved topologies. However, they must not be seen as a drop-in replacement for existing technologies. It is also critical that the underlying requirements of the application define the switching topology used and in turn guide engineers in their selection of the best transistor technology for meeting power efficiency goals.

We have an incredibly strong track record in the power semiconductor industry, having more than 40 years of power MOSFET know-how at our hand. Our portfolio includes silicon, SiC and GaN power devices, plus optimised complementary drivers. We continue to expand our offering, with recent steps in this direction including the acquisition of Cypress Semiconductor, which will increase our offering at the system level. By putting all of this experience into practice, we are uniquely positioned as a trusted advisor and partner within the semiconductor industry.

POWER ELECTRONICS WORLD
CONNECTING THE GLOBAL COMMUNITY

ONLINE ROUNDTABLE

- Based around a hot topic for your company, this 60-minute recorded, moderated zoom roundtable would be a platform for debate and discussion
- Moderated by an editor, this can include 3 speakers
- Questions prepared and shared in advance
- There would be an opportunity to view and edit out any unflattering bloopers

Contact: Jackie Cannon
jackie.cannon@angelbc.com

This event would be publicised for 4 weeks through all our mediums including:

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Imec offers new wireless charging solutions for implantable, insertable and ingestible medical devices

Researchers from imec presented a novel, new system for wireless medical device communication and power at the 2020 ISSC conference. The devices, 30 times smaller than today's start-of-the-art systems, considered system power requirements alongside medically relevant data communication. As Mark Fichman, team lead for medical device development at imec explains, the new approach is designed to make diagnoses and treatment less invasive, more reliable and easier to administer.

IMEC has built a unique toolset for wirelessly communicating and powering implantable devices including those close to the skin surface or deeper in the body as well as for 'smart pills'. This toolset allows the development of customized solutions for medical device companies in a relatively short period of time.

In February 2020, imec presented an ultra-small radio chip at the renowned ISSCC conference in San Francisco. The chip – 30 times smaller than today's state of the art systems performing the same functionality – can be used to set up a wireless link with a wide variety of medical devices (e.g. smart pills [ingestibles], or small implantables and insertables [devices close to the skin], to exchange data.) The presentation highlighted one example of the work that imec is doing in the field. Mark Fichman, team lead for medical device development, explains how such chips can be used for both communication and for charging. The latter can enable more user-friendly rechargeable implants or even battery-less devices.

Safety and longevity are key for implantables

Implantables, insertables and ingestibles typically consist of several building blocks: a sensing module, an actuation or stimulation module, a communication module, a power source, and – typically – a programmable component orchestrating all operations. Additionally, implantable devices require encapsulation technology to survive within the human body for long periods of time. For this, imec relies on its CMST research group at Ghent University. This group is developing a unique multicoating technology for a.o. implantables.

The requirements for all these building blocks are extremely stringent. "It's like sending a part to space. When you implant a device, nothing can go wrong. You don't want to put the patient through an extra surgery procedure just because some electronic part is failing," said Fichman.

"The same goes for the power source. You don't want to operate on the patient every year to replace the battery. Single-use or primary batteries are used in devices such as pacemakers. After a lifetime of 5 to 7 years, the batteries need to be replaced. But because the main pacemaker device is situated relatively close to the skin surface, this is considered a localized invasive procedure.

Another small drawback is the fact that the battery is relatively large (to guarantee the long lifetime)

and that the patient will 'feel' where it is located. A similar approach is taken for ingestibles or smart pills. Because the lifetime of the device is only one gastrointestinal cycle, primary batteries are the choice in this case."

Other medical implants are powered by so-called secondary batteries, as Fichman explains: "These are rechargeable batteries, typically used for devices that are implanted deeper in the body, such as neurostimulators. A patient with such a device needs to recharge it, typically at home. This implies that the charger should be attached for some time, up to a few hours. For some specific applications, there are also more advanced solutions available, like the charging belt for spinal cord stimulators of Boston Scientific."

"At imec, we believe that new technologies can change the life of patients with implants. We are developing radio chips and systems for wireless communication with the implantable or insertable. These could be used to make recharging much easier and more user-friendly, or to even make devices that don't require any battery. Also, low-power system design is an essential part of this research."

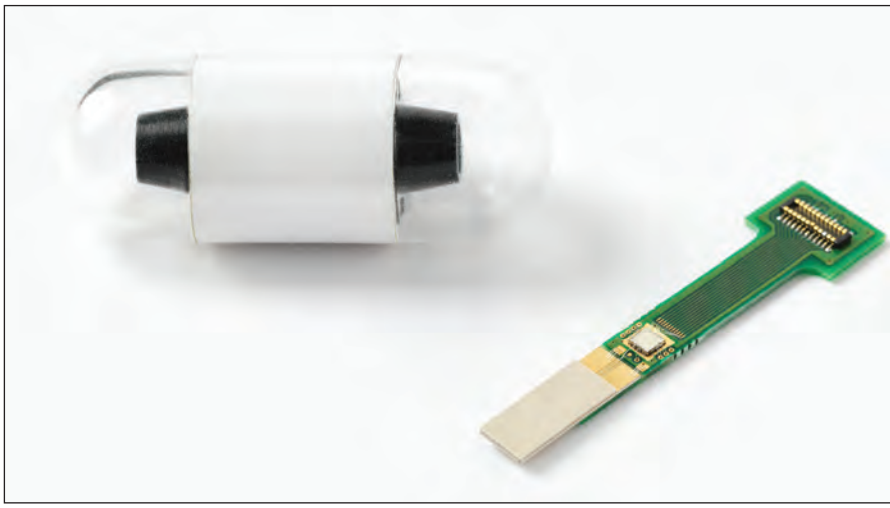
In the latter case – the battery-less implant – the patient would wear an external device like a patch or belt with a battery, a radio chip and an antenna that sends wireless signals to power the implanted device for a short period of time to do the necessary sensing and actuation. The implant would afterwards be depowered.

Which wireless technology to choose?

Imec has a lot of expertise in all kinds of wireless communication technologies. For each application, a perfect match must be found to meet all requirements. According to Fichman, "The most common wireless communication technology is RF-based. A tradeoff needs to be made between signal penetration in the body, size of required antennas, and data rate requirements.

If you use high-frequency radio signals, you can use small antennas (beneficial for the size of the recharging wearable) but the signal will not penetrate deep in the body. Low-frequency radio signals on the other hand are less absorbed by the soft tissue of the body but require larger antennas. Inductively coupled communication has the benefit of almost no tissue absorption, but tends to have limited data rates and requires good alignment between transmitter and receiver. Finally, there are other techniques like ultra-sound, but these also have their specific benefits and drawbacks."

"We believe that every application has different requirements when it comes to wireless communications with an implant (for exchanging sensor data and actuation instructions, for reprogramming, etc.). For the wireless charging, we are investigating inductive coupling, RF signals and ultrasound technologies."



Mock-up of an ingestible pill (left) with prototype transceiver (right). The small rectangular chip is imec's ultra-small 400MHz radio (including antenna) for communication with the ingestible. It is pictured here on a green test board.

"Inductive wireless powering is the most used technique for powering implants because the magnetic permeability of the body is almost equal to that of air. Because of that, the path losses in human tissues are close to insignificant. Another important advantage is the relatively large power density safety limit, up to 100mW/mm^2. In addition, since energy is not transferred via wave propagation, no energy is lost because of reflections by the skin and between tissues with different properties. However, inductive powering suffers from strong sensitivity to misalignment between the power transmitting coil outside the body and the implanted receiving coil. This limits its adoption to cases in which the location of the implant is known in advance."

"Wireless powering using mid-field or far-field radio frequency electromagnetic waves on the other hand is less sensitive to misalignment. However, radio frequency power transmission suffers from significant path losses in human tissue. Additionally, safety limits are 1,000 times lower. Also, since the energy transfer happens via wave propagation, significant reflection occurs at the interface between air and skin. Finally, since the body is not a homogeneous medium, multi-path reflections will occur also inside the body, further reducing the effectiveness of this technique."

"Wireless power transfer can also occur via mechanical means, via ultrasound pressure waves. Given that the body is mostly composed of water, the propagation of sound waves is very effective and path losses are low while the safety power limits are reasonable. The main challenge with ultrasound

power transfer is the reflection coefficient between air and skin, which is as high as 99.9%. In order to mitigate this loss, good acoustic coupling must be ensured in the whole path from transmitter to receiver.

This implies the use of acoustic gels and the implant must remain in close contact with the tissue in order to receive power. Even then, good acoustic coupling cannot be guaranteed throughout the body; for example due to the presence of bone tissue. So again, every application has different requirements and a different optimal technological solution."

"Thanks to our expertise in IC design, system design and integration, it is possible to make very compact radio solutions that support different radio technologies for wireless communication and charging. For every specific application, a customized solution may work. Because we have a long track record in building radio solutions with a variety of technologies, this development can be done in a relatively short period of time. For quick iterations, we can start with discrete component-based solutions but also go all the way to make custom chips for the application"

Multiple implants tightly in synch

Making a customized solution for communicating with and charging your medical implant, has an extra, unique advantage. The radio chip, present in the patch or belt worn by the patient, can also be used to synchronize the operation of several implants in the body. This can be an extremely interesting feature for certain applications, Fichman remarked.

"Think for example of a localized stimulation that is used for pain relief in a certain part of the body. The stimulus triggers a chain reaction that passes through many neurons, both to the targeted spot and to the brain.

The latter causes a typical sensation with the patient, which is a well-known side effect of this treatment. What if a second stimulation site could be used to prevent the stimulus from going all the way to the brain? This would certainly make the solution much more pleasant for the patient," he stated.

Implanting a dialysis machine in the patient's body

What if radio chips could be so small that they could be worn unobtrusively by the patient, while communicating with, charging and synchronizing the implants that the patient has inside its body? Fichman believes the technology has far reaching possibilities.

"For sure, this innovation paves the way for many new medical solutions and treatments. Medical device companies can probably imagine what this feature could mean for their specific application. One application that imec is focusing on is the artificial kidney. Indeed, as an active member of the Kidney Health Initiative (KHI), which (in cooperation with the

FDA) is stimulating the development of technologies for future dialysis methods, imec wants to contribute to this noble goal. In fact, we even helped writing the KHI innovation roadmap."

"We envision that our radio chips could be used in external wearables (such as patches) in which the main function is to communicate with and power an implanted artificial kidney (IAK). The patient would wear a patch with an integrated antenna and radio chip, attached to a small rechargeable battery. To guarantee a secure wireless link, imec has developed very robust anti-hacking technology, based upon physically unclonable features (PUFs)."

"Depending on the energy consumption and internal battery of an IAK, charging of the IAK by the patch could be done intermittently, while the IAK would dialyse in a continuous way. To save on energy, the IAK can be connected between an artery and a vein, without the need for any energy-guzzling blood pumps. Instead, it would run on the body's internal blood pressure while the artificial urine from the IAK would be dumped via the bladder in the natural way. And, by focusing on ultra-low-power system design, the internal electronics for monitoring and control would only consume very little power."

"An IAK would be an enormous improvement compared to today's big bed-side dialysis machines that usually require three hospital visits per week (with 4 hours of treatment each). Dialysis patients would gain much more freedom to go where they like and when they like, just like patients with a pacemaker, or an implanted electronic nerve stimulator for pain relief."

With small radio chips integrated in a patch, it would be possible to power an artificial kidney and extract its data and send it to the cloud.

Taking passive implants to the next level

When thinking of implants, most of us think of pacemakers and neurostimulators. These are active devices, performing an active function inside the body, like sending out a pulse. Next to this, there are also passive implants such as screws, stents, hip replacements, stomach reduction staples, etc. Fichman explained how next-generation technology can benefit these types of implants as well.

"Passive devices can sizably benefit from our implantable technologies. One could add sensors or actuators to these passive devices to check for certain parameters. These 'upgraded' implants would not need to have any batteries. Instead, they would only get activated if the patient puts an external powering device close by. Then, the sensor would wake up for a short period of time, do some sensing or actuation, and send its data to the external device."

"Or take the example of the stomach reduction staples. By 'smartifying' the staples, one could get sensing info from the implanted staples. Information collected from such smart staples can be paramount in the post-surgery follow-up and through the recovery program. Because imec's technology allows data collection from multiple sensors with respect to each other, this could provide some useful information on the functioning of the reduced stomach."

Conclusion

Imec has long-standing expertise in wireless radio technologies, miniaturization and design for ultra-low power consumption. These capabilities can be extremely interesting for medical device companies to innovate in the field implantables, insertables and ingestibles, according to Mark Fichman.

"We have an extensive toolset ready to mix and match our knowledge and our technological building blocks to make a dedicated solution for each specific application. With dedicated radio-enabled external units (incorporated in a wearable, patch, belt, etc.), one could readout an implanted device, send instructions, synchronize readout or activation of several devices, or power a rechargeable or battery-less (active and passive) device."

"The long track record of IMEC in the development of wearable solutions (including regulatory approved medical devices both in the US by the FDA and Japan's PMDA) strengthens the system level proposition, being able to offer both implants and external wearable solutions to power them. The possibilities are enormous, and, together with medical device companies with much more experience on the application-end, we can make true innovations happen. The cross-fertilization between technology and application knowledge is key in this."

About Mark Fichman

MARK FICHMAN is a senior engineer and team leader at imec. His background is primarily as a hardware engineer; he has spent most of his career in the area of active implantable medical devices working for a number of start-ups for 20 years. He is product-oriented, seeking solutions in the most challenging environments that often require multi-discipline abilities, with extensive knowledge of standards within that area as well as for wearable devices. Mark joined the connected health solutions group at imec in 2017 to lead the implantable program, working on next-generation implantable devices intended for diagnosis and therapy.

Supercritical carbon dioxide spawns superior MOSFETs

A low-temperature treatment with supercritical CO_2 improves the interface between SiC and SiO_2

THE PERFORMANCE of the SiC MOSFET is held back by the quality of the interface between SiC and SiO_2. But this weakness can be addressed with a supercritical CO_2 treatment that slashes the density of interface states, claims a partnership between researchers at Xi'an Jiaotong University and Xidian University.

Spokesman for the team, Weihua Liu from Xi'an Jiaotong University, told *Compound Semiconductor* that in conventional SiC MOSFETs the interface is not optimised by high-temperature annealing, because this can create carbon clusters and other defects.

Formation of these imperfections is quashed with a lower temperature supercritical CO_2 treatment that promises higher carrier mobility, a lower leakage current and a hike in the critical breakdown field of the gate oxide.

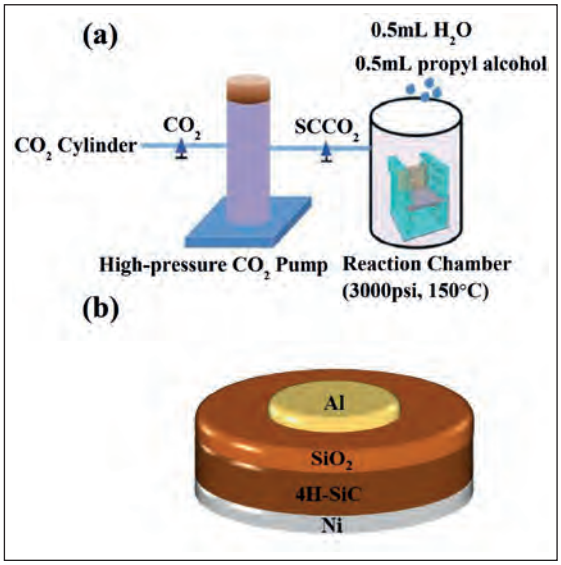
In a supercritical fluid there is a co-existence of liquid and gas phases. Thanks to this, supercritical CO_2 combines gas-like solubility with liquid-like penetration, enabling damage-free diffusion into nanoscale structures.

The use of supercritical CO_2 to improve interfaces in semiconductor devices is not new. Back in 2007, reports appeared describing the benefits this can bring to thin-film transistors made from amorphous silicon.

When supercritical CO_2 treatment is applied to SiC MOSFETs at temperatures as low as 150 °C, it is thought to terminate traps at the oxide-semiconductor interface and supress the interfacial parasitic oxide.

To assess the benefits of the supercritical CO_2 process, the team began by producing MOS structures. They took epiwafers with an *n*-type layer that has a doping concentration of 3.5 x 10^{15} cm^{-3} and, after applying a standard cleaning process, used dry oxidation to create SiO_2 films with a thickness of 55-60 nm.

Some sample were treated in supercritical CO_2 at 150 °C for 60 minutes, using a pressure of 20 MPa (see Figure). To the process chamber the team added 0.5 ml of water and 0.5 ml of propyl alcohol. The latter acts as a surfactant between non-polar CO_2 molecules and polar water molecules, enabling water to be uniformly distributed in supercritical CO_2.



Treatment with supercritical CO_2 (a) is applied to MOS structures (b).

To benchmark results, the team did not treat some samples and processed others in a pure water vapour at 150 °C for 60 minutes.

Fabrication of MOS structures, featuring aluminium electrodes with a diameter of 300 μm, allowed the team to evaluate the density of near-interfacial oxide traps. Using capacitance-voltage measurements, they found a near-interfacial oxide trap density of 1.62 x 10^{11} cm^{-2} in the untreated sample, while samples treated in water vapour and supercritical CO_2 produced values of 6.63 x 10^{10} cm^{-2} and 1.84 x 10^{10} cm^{-2}, respectively. The lowest value is claimed to result from the termination of traps in SiO_2 through the creation of Si-O-Si feature bonds.

Additional benefits of the supercritical CO_2 treatment are a reduction in leakage current and an increase in breakdown field.

Measurements of the interface state density also revealed the benefit of supercritical CO_2 treatment.

Liu says that one of the next tasks for the team is to optimise the experimental conditions, in order to further reduce the interface state density. Another goal is to verify that the supercritical fluid process delivers benefits to 4H-SiC MOSFETs by applying this treatment to those devices.

Reference

M. Wang *et al*. Appl. Phys. Express **13** 111002 (2020)

Building better Ga_2O_3 transistors

Wrapping modulation-doped Ga_2O_3 FETs in highly conductive materials addresses concerns related to thermal management and carrier transport

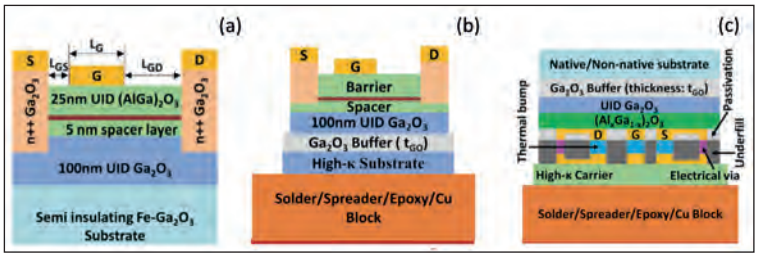
IF Ga_2O_3 transistors are to fulfil their potential in RF and power electronics, issues must be addressed that relate to a low electron carrier mobility and heat extraction.

Offering promising solutions to both these concerns is a US collaboration between engineers from The Pennsylvania State University, The Ohio State University, Kyma Technologies, Modern Microsystems and the University of Utah. This team is making the case for replacing the MOSFET with a FET featuring modulated silicon δ-doping – a class of transistor known as the MODFET – and incorporating materials with a high thermal conductivity, to allow the device to run harder without overheating. Using the most capable architecture for heat extraction enables a five-fold increase in power handling.

Investigations by the team involved experimental studies and simulations. They included the use of thermo-reflectance thermal imaging to determine the surface temperature of the MODFET under various operating conditions. To validate those results, the engineers turned to nanoparticle-assisted Raman thermometry. Both techniques, which probed the temperature rise of the gate metal, gave excellent agreement. Values were replicated in simulations produced by Synopsys Sentaurus and COMSOL Multiphysics software.

Simulations were employed to consider the impact of changes to gate-to-drain distance in MODFETs with a gate-to-source separation of 1 μm and a gate length of 3 μm (see Figure (a)). To increase the breakdown voltage in power FETs, designers tend to employ a gate-to-drain spacing that exceeds the gate-to-source separation. According to simulations, by increasing the gate-to-drain spacing from 3 μm – the distance used in the devices produced for the thermal measurements – to 20 μm slashed the peak electric field by an order of magnitude. In turn, the rise in peak temperature fell by almost 40 percent.

The engineers have also used simulations to consider the impact on power handling of the insertion of high thermal conductivity substrates underneath the MODFET. For a MODFET with a 10 μm-thick Ga_2O_3 buffer (see Figure (b)), mounting this device on a 4H-SiC wafer led to a reduction of 46 percent in the rise in maximum temperature. Replacing 4H-SiC with diamond, which has a thermal conductivity around four times higher, delivered further improvement. However, gains were modest, delivering just a 5 percent decrease in the maximum temperature,



The thermal management of a Ga_2O_3 MODFET (a) can improve by inserting a high thermal conductivity substrate (b). Even better results are possible with a double-sided cooling design (c).

because the 10 μm-thick Ga_2O_3 buffer dominates the thermal dissipation of this device.

To evaluate the role that the buffer has on device heating when switching from 4H-SiC to diamond, the team also simulated MODFETs with Ga_2O_3 buffer thicknesses of 100 μm and 1 μm. For the former, diamond delivers only a 1 percent gain over 4H-SiC, but for the latter it is an improvement of 14 percent. However, the team is quick to point out that the feasibility of thinning a Ga_2O_3 buffer to just 1 μm is yet to be established.

Experimental verification of these trends came from infrared thermography measurements, supported by finite-element thermal modelling. The engineers demonstrated that the addition of a 500 μm-thick 4H-SiC wafer to MODFETs with a 10 μm-thick Ga_2O_3 buffer provided a 66 percent reduction in the peak temperature.

Further reductions in peak temperature can result from a double-sided cooling design. With this architecture, the best results come from a combination of: depositing nanocrystalline diamond over the FETs; using gold bumps, rather than those made from indium; and mounting the transistor on polycrystalline diamond.

Simulations suggest that for MODFETs operating with a channel temperature of 200 °C, moving from the conventional homo-epitaxial design to an optimum double-sided design enables a hike in power density from 1.7 W/mm to 9.5 W/mm.

Reference

B. Chatterjee *et al.* Appl. Phys. Lett **117** 153501 (2020)

AlPN enlarges the nitride family

Growth of AlPN epilayers promises better HEMTs and VCSELs

A PARTNERSHIP between researchers at Nagoya University and Japan's Institute for Material Systems for Sustainability claims to have broken new ground by producing the first epilayers of AlPN. This ternary, latticed-matched to GaN, promises to improve the performance of GaN HEMTs and VCSELs.

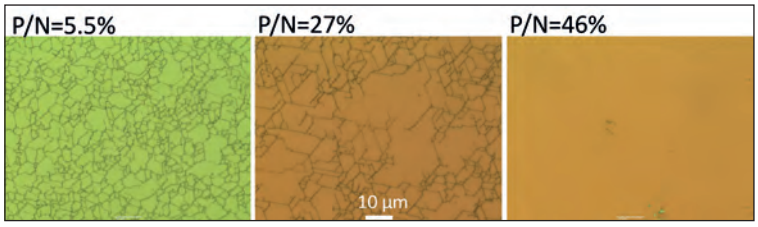
Latticed-matched AlPN could transform HEMTs by introducing a very high polarisation that leads to a high carrier concentration in the channel. Early results are very encouraging, with an unoptimised sample producing a sheet resistance of just 150 ± 50 Ω/square.

For GaN VCSELs, AlPN could be a game-changer, simplifying and improving the fabrication of the mirrors. Prior to the work of the Japanese team, GaN and AlInN provided the only pair of nitrides that could be used for growing mirrors. With this duo, the growth of a mirror takes 12 hours or more, due to drawbacks on three fronts: there is a need for many mirror pairs; the ternary has a slow growth rate; and temperature ramping is needed between GaN and AlIN, which must be grown using a temperature deviation below 3 °C.

Those issues are to blame for a growth time that is far too long for the production of VCSELs incorporating two GaN-based mirrors. Instead, devices tend to combine one GaN-based mirror with another made from a dielectric.

Switching to mirrors made from AlPN and GaN promises to slash the growth time to 2-3 hours, says the spokesman for the team that is pioneering this novel alloy, Markus Pristovsek from Nagoya University. According to him, the substantial time saving stems from the faster growth rate for the ternary and the reduction in the number of mirror pairs, realised thanks to a much larger difference in refractive index between the two nitrides.

The development of ternary nitrides has a long history, with efforts between 1996 and 2005 directed at a cousin of AlPN, GaPN. During those years researchers discovered that when the phosphor content exceeded 3-4 percent, phosphor atoms head for gallium sites, due to the shorter bond length and smaller size. Adding aluminium offered a solution.



Cranking up the flow of tertiary-butylphosphine increases the ratio of phosphor-to-nitrogen and reduces the density of cracks in the AlPN layer.

In 1999 Panasonic filed a patent for AlPN and AlGaPN. "However, there was never a publication," points out Pristovsek, who reasons that either attempts failed or the patent was filed simply to expand an intellectual property portfolio.

Pristovsek started to actively pursue AlPN in 2012. "A first attempt to patent it at TU Berlin failed, because they thought there is absolutely no commercial value and the patent would not earn its fee."

A move to the University of Cambridge enabled Pristovsek to secure funding for AlPN research. However, by the time an order had been placed for a tertiary-butylphosphine (tBP) bubbler that would provide a source of phosphor – phosphine is toxic, so forbidden in many labs – Pristovsek had an offer of a professorship at Nagoya University.

Taking that up in 2016, he took some time to find an underused reactor for his experiments and convert a metal-organic line to tBP. The first epiwafers were riddled with cracks, but cranking up the tBP flow addressed this issue.

Pristovsek and co-workers turned to X-ray diffraction to investigate the crystalline structure of a 60 nm-thick layer of AlPN, grown on a GaN-on-sapphire template. Measurements produced reflections only from GaN, sapphire, and strained $AlP_{0.103}N_{0.897}$, revealing that the ternary is pure wurtzite AlPN. Based on the position of the diffraction peak for this alloy, to ensure lattice-matching the composition of this ternary needs to be $AlP_{0.106}N_{0.894}$.

Ellipsometry measurements on samples with AlPN thicknesses of 180 nm, 315 nm and 665 nm indicate that the refractive index of this ternary, when lattice-matched to GaN, is around 1.95 to 2.05. There are Fabry-Perot oscillations associated with the 655 nm-thick sample that suggest that the bandgap for this alloy is around 5.5 eV.

One of the next goals for the team is to develop GaN HEMTs with an AlPN layer.

Reference

M. Pristovsek *et al.* Appl. Phys. Express **13** 111001 (2020)