PEW
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REVOLUTIONISING POWER:
THE IMPACT OF LASER-BASED OHMIC CONTACT FORMATION IN SiC SEMICONDUCTORS

3D MICROMAC

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VIEWPOINT

By Phil Alsop Editor

Revolution, not evolution?

"IN ITALY, for thirty years under the Borgias, they had warfare, terror, murder, and bloodshed, but they produced Michelangelo, Leonardo da Vinci, and the Renaissance. In Switzerland, they had brotherly love, and they had 500 years of democracy and peace. And what did that produce? The cuckoo clock."

Possibly my favourite quote of all time – taken from the film The Third Man. In the interest of balance, I should perhaps also point out that the Swiss also developed perhaps the world's finest banking industry.

However, the central point - that disruption, chaos and revolution are almost prerequisites for ingenuity, innovation and radical change – holds good.

And it's great to see in this issue of PEW so many ways in which the technology sector is leading the way when it comes to profound and beneficial innovation and change across all aspects of the workplace and our leisure time. Our cover story confirms that we are witnessing something of a 'paradigm shift' as silicon carbide (and other compound semiconductors) continues to demonstrate significant possibilities and advantages over 'traditional' silicon-based solutions – especially when it comes to electric vehicles, renewable energy systems and high-voltage power transmission.

Elsewhere in the magazine, we have some fascinating research breakthroughs as reported by imec and CEA-Leti. Imec has introduced 'a breakthrough architecture that lays the foundation for a whole new generation of analog-to-digital converters (ADCs), which it anticipates will have a major impact in the AI/power hungry data centres of the near future; while CEA-Leti and the University of California San Diego have developed 'a ground-breaking piezoelectric-based DC-DC converter that unifies all power switches onto a single chip to increase power density'. Applications for this include smart phones, computers and servers and AR/VR head sets.

Testing is a key part of any product/technology innovation process, and the article from Keysight Technologies explains the importance and increasing needs of parametric tests and the test challenges for high-voltage parametric tests as next-generation power devices are developed to meet a growing quantity and variety of applications in the automotive industry and beyond.

Meanwhile, the AmberSemi article promises nothing short of 'the second electrical revolution' -solid-state based, DC extraction directly from AC mains without the use of rectifier bridges, transformers and high voltage, bulk capacitors.

I hope you enjoy these and the other articles in this issue of PEW and, like me can agree with Mr Wordsworth who, commenting on a revolution of a different kind, wrote: 'Bliss was it in that dawn to be alive'!

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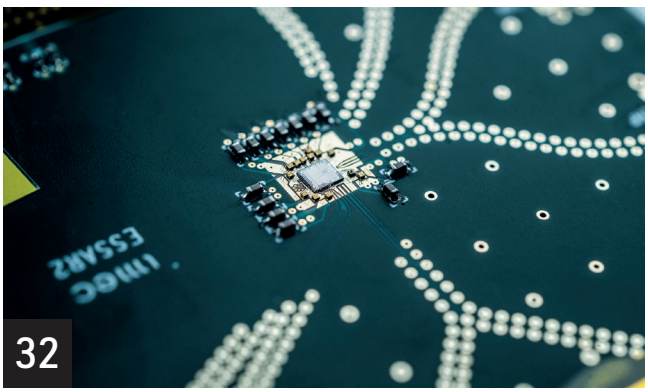

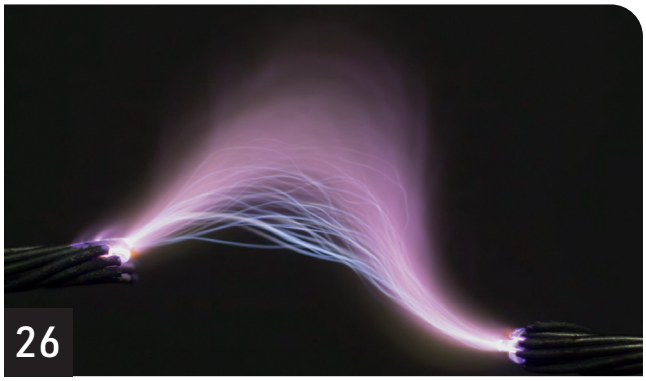

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Vishay acquires Newport Wafer Fab for $177M

Acquisition accelerates Vishay's SiC production plans

US-BASED Vishay Intertechnology has completed the acquisition of Nexperia's wafer fabrication facility and operations located in Newport, South Wales, UK for approximately $177 million.

The Newport wafer fab, located on 28 acres, is an automotive-certified, 200mm semiconductor wafer fab with capacity to produce more than 30,000 wafers per month. The fab is the UK's largest semiconductor fab with a long history in supplying components to the automotive and industrial markets.

Vishay plans to position the facility as a manufacturing excellence center focusing on Net Zero Transformation of decarbonisation and electrification.

As a new member of the Compound Semiconductor Cluster in South Wales, Vishay plans to collaborate with local universities and others in the UK to enhance its research and development efforts on power compound semiconductors.

"The acquisition of Newport aligns with the strategic shift the Board envisioned with its decision to appoint new leadership. Under Joel's leadership,

Vishay is making this shift, investing in technologies and incremental capacity to drive faster growth and enhance returns to stockholders. The goal is to prepare Vishay to capitalise on the megatrends of e-mobility, sustainability, and connectivity," said Marc Zandman, executive chairman of the board.

"With a Vishay-owned fab to qualify and scale our SiC portfolio, we are accelerating our participation in the SiC MOSFETs and diodes marketplace, as desired by our customers," said Joel Smejkal, president and CEO of Vishay. "In late 2022, the MaxPower acquisitio

n advanced our SiC intellectual property and MOSFETs product technology. We are excited to further develop our SiC and GaN technology as a new member of the Compound Semiconductor Cluster in South Wales."

"We welcome the highly skilled and dedicated employees at the Newport wafer fab into the Vishay family. Vishay is committed to investing in Newport to grow capacity, and to accelerate our SiC and GaN production and technology development.'

"We look forward to the contributions of Newport's employees to our shared success," added Smejkal. "With the completion of the acquisition, we are now preparing to share our plans for Newport at our upcoming Investor Day on April 2, 2024."

The transaction was funded by Vishay with cash on-hand. To affect the transaction, Vishay acquired a 100 percent interest in the legal entity Neptune 6 Limited, and its wholly-owned operating subsidiary, Nexperia Newport Limited, which owns and operates the Newport facility. Neptune 6 Limited is expected to be renamed 'Vishay UK Holdings Limited' and Nexperia Newport Limited is expected to be renamed 'Vishay Newport Limited'.

Taiwan Semi launches new line of automotive rectifiers

TAIWAN SEMICONDUCTOR has announced a new line of automotive-qualified rectifiers featuring ESD withstand capability.

The new TSD Series rectifiers simultaneously provide repetitive peak reverse voltage (VRRM) of up to 600V as well as ESD protection of >10,000V (per IEC-61000-4-2). Devices in the series have optional current ratings of 1A, 2A, and 3A and operating temperature ranges from -40°C to ±175°C. All have a maximum forward voltage drop of 1.1V and feature low-reverse leakage current and fast response time.

Qualified to automotive standards, the TSD Series offers input polarity protection where DC input voltage is applied; bridge and general purpose rectification circuits; LED strings and POE I/O protection, ESD protection, clamping, snubber networks and transient protection for datacom systems.

They also provide reliable protection for smoke detectors, industrial controls, security systems, communication systems, lighting and other systems that depend on continuous operation.

"Typical rectifiers are limited to ESD capability of less than 1.5kV and cannot meet industry standards for ESD protection required by IEC-61000-4-2 contact mode," said Sam Wang, vice president, TSC Products."

"Also, ESD will punch through standard polarity-protection rectifiers, resulting in failure modes that can immediately damage the TVS – or else create 'walking wounded' damage that later manifests as failure during normal operation. In contrast, our ESD-capable TSD Series devices were developed to survive and protect customers' end equipment now and in the future."

Innoscience launches 700V integrated GaN HEMT range

Chips include HEMT, driver, current sense and protection functions

INNOSCIENCE has announced a family of four new integrated devices that combine power GaN HEMT, driver, current sense and other functions within a single, industry-standard QFN 6x8mm package.

The 700V ISG610x SolidGaN devices cover the range from 140mΩ to 450mΩ, and save PCB space and BOM count, while increasing efficiency and simplifying design for applications including USB-PD chargers, LED lighting, and AC/DC power supplies and PFC, QR flyback, ACF, and LLC converters.

The devices feature a 9V-80V VCC range which is beneficial in USB-PD applications that require up to 28V output. Competitive devices which have a limited 30V input voltage require an external high voltage LDO or several discrete components to achieve higher than 15V output. Innoscience says these new SolidGaN parts can easily cover the USB-PD output voltage requirements without external LDO or other parts, saving BOM cost and board area.

For low power operation, ISG610x family ICs also feature a low, 115µA quiescent current, thanks to an innovative automatic standby mode which is activated when the PWM signal voltage remains low for a certain time period. During this time, most of the internal circuitry is turned off, reducing energy wastage

For low power operation, ISG610x family ICs also feature a low, 115µA quiescent current, thanks to an innovative automatic standby mode which is activated when the PWM signal voltage remains low for a certain time period. During this time, most of the internal circuitry is turned off, reducing energy wastage, enabling devices to meet the No-Load standby power specifications of regulatory bodies such as ENERGYSTAR.

The loss-less current sensing with 7 percent accuracy of the new SolidGaN devices offers several benefits. Firstly, because the current sensing resistor loss is eliminated, a larger RDS(on) can be accommodated with no loss in performance, leading to cost reduction. Secondly, component count is reduced and PCB footprint is minimized.

Commented Min Chen, VP of Design Engineering, Innoscience: “The high level of integration with high current sense accuracy and low quiescent current makes the ISG610x family suitable for simple-to-use, low component count, and high efficiency applications.”

Devices also feature a programmable switch turn-on slew rate to enable EMI reduction. An internal linear voltage regulator is included to assure a tightly regulated 6.5V driver supply, maximizing GaN HEMT current capability while ensuring the reliability of the GaN HEMT. Finally, built-in under-voltage lock-out (UVLO), over-current protection (OCP) and over-temperature protection (OTP) are incorporated within the IC.

A demo board, INNDAD120B1, is available, describing a quasi-resonant flyback power supply with 90V~264V AC input and 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/6A (120W peak) output.

Infineon unveils power modules for AI data centres

INFINEON has launched a new series of dual-phase power modules to help reduce energy consumption in AI data centres.

(AI servers require three times more energy than traditional servers, and data centres consume more than 2 percent of the global energy supply).

The new TDM2254xD devices, introduced at the Applied Power Electronics Conference (APEC), combine OptiMOS MOSFET technology with novel packaging and proprietary magnetic structure to deliver high electrical and thermal performance with robust mechanical design.

According to the company, the modules allow for efficient heat transfer from the power stage onto the heat sink through a novel inductor design optimised to transfer current and heat. The results is 2 percent higher efficiency than industry average modules at full load.

Improving power efficiency at the core of a GPU yields significant energy savings at scale. This translates into megawatts saved for data centres computing generative AI and in turn leads to reduced CO2 emissions and millions of dollars in operating cost savings over the system’s lifetime.

US DoE announces $2.25M SiC packaging prize

Contest invites groups to propose, design, and build new high voltage SiC packaging prototypes

THE US Department of Energy (DOE) has launched the American-Made SiC Packaging Prize; a $2.25 million contest that invites competitors to propose, design, build, and test state-of-the-art SiC semiconductor packaging prototypes.

The idea, which comes from the DoE's Office of Electricity, is to find ways to make SiC devices work more effectively in high-voltage environments such as energy storage.

The prize is part of the American-Made Challenges program, which fosters collaboration between entrepreneurs and innovators, DOE's National Labs, and the private sector.

To enable these devices to work most effectively and to advance energy storage of renewable energy generation, SiC power modules need to be expanded to higher voltage and higher current ratings. The SiC Semiconductor Prize offers a total prize pool of $2.25 million across three phases:

Phase 1 – Design Study:
In this phase, prize participants will describe their team, plan to make progress toward developing SiC semiconductor packaging and showcase any prototypes. As part of this phase, participants will show evidence of a design prototype that meets or exceeds Phase 2 metrics. Up to ten winning teams will receive $50,000 each and will be eligible to compete in Phase 2. Up to 10 winning teams will receive $50,000 each and will be eligible to compete in Phase 2. (Total prize pool: $500,000)

Phase 2 – Initial Demonstration:
In Phase 2, winning teams from Phase 1 will develop a physical prototype of their SiC packaging solution that meets Phase 2 metrics. In this phase, teams must send their prototypes to a national lab for testing to validate the metrics achieved. At the end of Phase 2, four winning teams will receive $250,000 each and become eligible to compete in Phase 3. (Total prize pool: $1 million)

Phase 3 – Final Demonstration:
In Phase 3, teams from Phase 2 will continue the development of their SiC packaging solution and showcase their working prototypes. In this phase, teams will work to achieve the high voltage and high current targes while continuing to innovate towards an improvement in packaging. In Phase 3, one winning team will be named Grand Prize winner and be awarded $750,000. (Total prize pool: $750,000)

The competition is open only to private entities (for-profits and nonprofits); non-federal government entities such as states, counties, tribes, and municipalities, academic institutions; and individuals. Submissions are due by August 30, 2024.

GF GaN fab to benefit from $1.5B CHIPS act funding

THE US Department of Commerce has announced $1.5 billion in planned direct funding for GlobalFoundries as part of the US CHIPS and Science Act. This investment will enable GF to expand and create new manufacturing capacity and capabilities including securing essential GaN chips for automotive, IoT, aerospace, defence, and other vital markets.

GF is the first pure-play foundry to receive a major award (over $1.5 billion) from the CHIPS and Science Act, designed to strengthen American semiconductor manufacturing, supply chains and national security. Part of the proposed funding will support the creation of the first US facility capable of high-volume manufacturing of next-generation GaN semiconductors for use in TVs, power grids, data centres, 5G and 6G smartphones and other critical technologies. This will be at the site of GF's longest continuously operated fab, a 200mm facility in Essex Junction, Vermont. The GaN project was also awarded £35 million in US government funding in October 2023.

The $1.5 billion investment will also help upgrade and expand capacity at GFs existing Vermont facilities. In addition, it will go towards GF's Malta, NY, fab by adding technologies already in production in GF's Singapore and Germany facilities geared towards serving the US auto industry.

Overall, based on market requirements and demand, GF plans to invest more than $12 billion over the next 10 plus years across its two US sites through public-private partnerships with support from the federal and state governments as well as from its ecosystem partners, including key strategic customers.

To attract and cultivate a pipeline of semiconductor talent that will be needed in New York and Vermont, GF has announced a new student loan repayment program to help current employees and new recruits pay down student loan debt. The new benefit program is part of the company's multi-million-dollar investment to strengthen the semiconductor talent workforce

Hitachi Energy announces first 300mm IGBT wafer

Breakthrough will increase chip production capacity and deliver complex structures for 1200V devices

HITACHI ENERGY has achieved a breakthrough in its power semiconductor technology by introducing a 300 mm IGBT wafer.

The development will boost production capacity and enables more complex structures in 1200V IGBTs. Applications include variable frequency drives (VFD), uninterruptible power supply (UPS) systems, electric cars, trains and air conditioners, among others.

The larger wafer offers the potential to yield over double (2.4 times) the number of functioning integrated circuits per wafer as compared to the existing 200 mm wafer, leading to significant cost savings. It uses the latest fine pattern trench IGBT design, resulting in energy-efficient power conversion and control and minimising power losses during operations.

"It is impressive to see how seamless and fast the introduction of the 300mm wafers has been. The team's success not only advances Hitachi Energy's semiconductor technology but offers our customers enhanced competitiveness and capacity. In the future, we plan to expand our 300 mm wafer platform to support higher voltage IGBTs," said Rainer Kaesmaier, managing director of Hitachi Energy's semiconductors business.

Pictured above from left: Makan Chen, VP of sales & business development; Rainer Kaesmaier, managing director of semiconductors; Tobias Keller, VP of global Product management & marketing; Luca De Michielis, R&D team manager for BiMOS Chips, Roc Blumenthal, global program manager of Low Voltage IGBT

Semiconductor experts at Hitachi Energy achieved the milestone through collaboration with a cross-functional team, including product management, business development, R&D, and a chip foundry partner.

Power Integrations launches InnoMux-2

New GaN-based ICs combine AC-DC and DC-DC stages into a single power converter

POWER INTEGRATIONS has announced the InnoMux-2 family of single-stage, independently regulated multi-output offline power-supply ICs.

InnoMux-2 ICs combine AC-DC and downstream DC-DC conversion stages into a single chip, providing up to three independently regulated outputs for use in white goods, industrial systems, displays and other applications requiring multiple voltages.

Elimination of separate DC-DC stages slashes component count, reduces PCB footprint and increases efficiency by as much as 10 percentage points compared to traditional two-stage architectures, according to the company. Efficiency is aided by the ICs' 750 V PowiGaN transistors, zero-voltage switching (without an active clamp) and synchronous rectification.

Roland Saint-Pierre, vice president of product development at Power Integrations said: "Most modern electronic systems rely on multiple internal voltages to operate various functions such as computing, communication and actuation function – typically heat, light, sound or motion of some kind. But losses in each conversion stage are compounded, degrading system performance and generating heat. The InnoMux-2 IC overcomes this challenge by providing up to three independently regulated voltage outputs or two voltage output and a constant current output from a single stage, achieving a compact and efficient power sub-system with low component count."

InnoMux-2 ICs deliver up to 90 watts of output power with regulation of better than ±3 percent across the full input line, load, temperature and differential current step conditions.

Total power system efficiency (AC to regulated low-voltage DC segment) is above 90 percent; the advanced InnoMux-2 controller also manages light-load power delivery, avoiding the need for pre-load resistors and reducing no-load consumption to less than 30 mW.

This conserves power for necessary functionality in applications subject to the 300 mW allowance for standby usage under the European energy-using product (EuP) regulations. InnoMux-2 devices benefit from Power Integrations' thermally efficient InSOP24 and InSOP28 packages with PCB cooling, so no heatsink is required. Device options include dual- and three-output constant voltage (CV); optionally, one output may be dedicated to constant current (CC) drive, suitable for powering LEDs in displays or for high-speed charging of an internal battery.

Typical applications include TVs, monitors, appliances, networking, home and building automation, LED emergency lighting and industrial power supplies.

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TI announces new power ranges

100V GaN power stages reduce solution size by over 40 percent and increase power efficiency with 50 percent lower switching losses

TEXAS INSTRUMENTS has introduced two new power conversion device portfolios to help engineers achieve more power in smaller spaces.

TI's new 100V integrated GaN power stages feature thermally enhanced dual-side cooled package technology to simplify thermal designs and achieve high power density in mid-voltage applications at more than 1.5kW/in3. And the new 1.5W isolated DC/DC modules with integrated transformers are said to be the industry's smallest and most power-dense, helping engineers shrink the isolated bias power-supply size in automotive and industrial systems by over 89 percent.

Devices from both portfolios will be on display at this year's Applied Power Electronics Conference (APEC), Feb. 25-29 in Long Beach, California.

"For power-supply designers, delivering more power in limited spaces will always be a critical design challenge," said Kannan Soundarapandian, general manager of High Voltage Power at TI. "Take data centres, for example – if engineers can design power-dense server power-supply solutions, data centres can operate more efficiently to meet growing processing needs while also minimising their environmental footprint. We're excited to continue to push the limits of power management by offering innovations that help engineers deliver the highest power density, efficiency and thermal performance."

With TI's new 100V GaN power stages, LMG2100R044 and LMG3100R017, designers can reduce power-supply solution size for mid-voltage applications by more than 40 percent and achieve industry-leading power density of over 1.5kW/in3, enabled by GaN technology's higher switching frequencies. The new portfolio also reduces switching power losses by

50 percent compared to silicon-based solutions, while achieving 98 percent or higher system efficiency given the lower output capacitance and lower gate-drive losses. In a solar inverter system, for example, higher density and efficiency enables the same panel to store and produce more power while decreasing the size of the overall microinverter system.

A key enabler of the thermal performance in the 100V GaN portfolio is TI's thermally enhanced dual-side cooled package. This technology enables more efficient heat removal from both sides of the device and offers improved thermal resistance compared to competing integrated GaN devices.

With over eight times higher power density than discrete solutions and three times higher power density than competing modules, TI's new 1.5W isolated DC/DC modules are said to deliver the highest output power and isolation capability (3kV) for automotive and industrial systems in a 4mm-by-5mm very thin small outline no-lead (VSON) package. With TI's UCC33420-Q1 and UCC33420, designers can also easily meet stringent electromagnetic interference (EMI) requirements, such as Comité International Spécial des Perturbations Radioélectriques (CISPR) 32 and 25, with fewer components and a simple filter design.

> For power-supply designers, delivering more power in limited spaces will always be a critical design challenge

The new modules use TI's next-generation integrated transformer technology, which eliminates the need for an external transformer in a bias supply design. The technology allows engineers to shrink solution size by more than 89 percent and reduce height by up to 75 percent, while cutting bill of materials by half compared to discrete solutions.

According to TI, with the first automotive-qualified solution in this small package, designers can now reduce the footprint, weight and height of their bias supply solution for electric vehicle systems such as battery management systems. For space-constrained industrial power delivery in data centres, the new module enables designers to minimise printed circuit board area.

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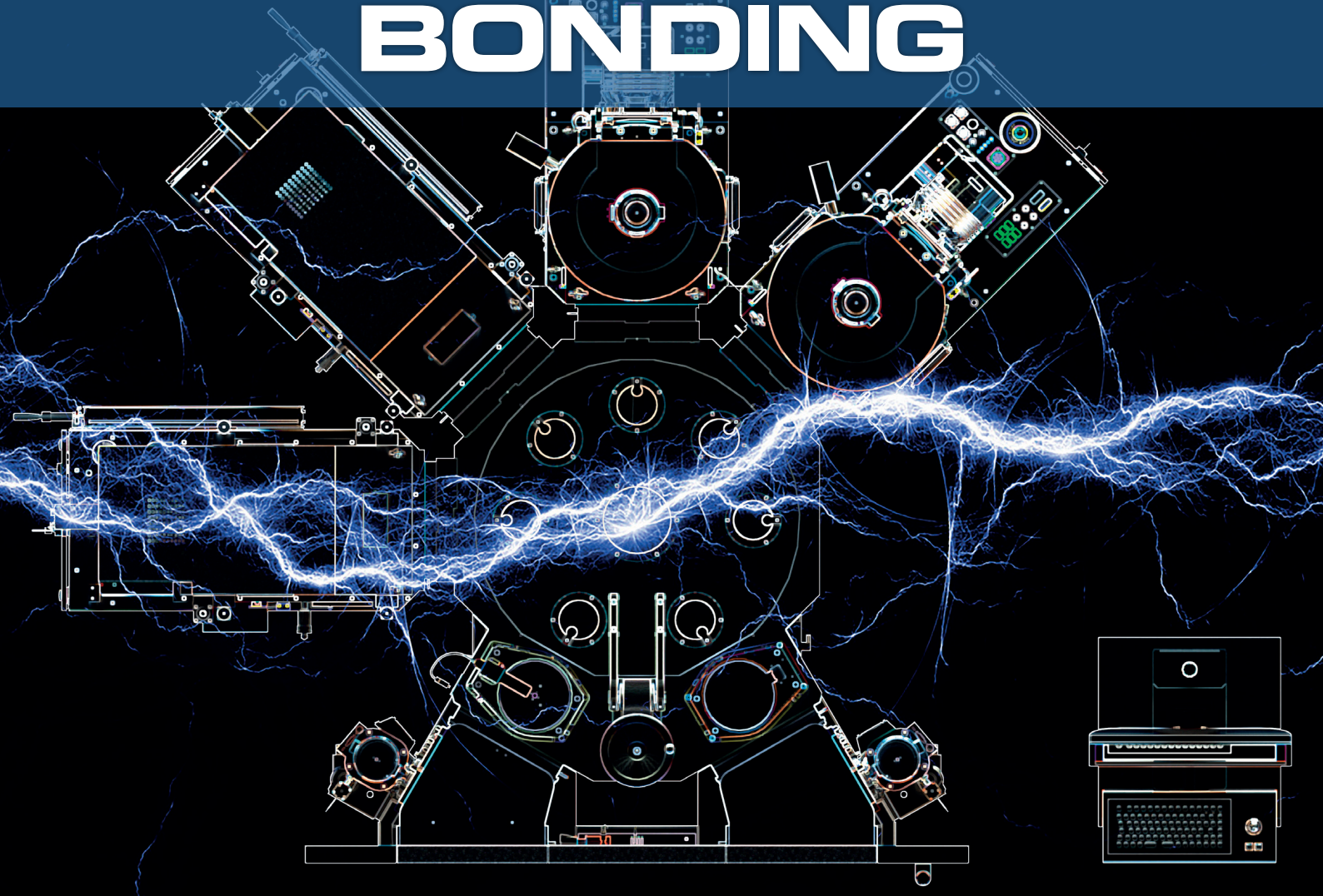

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Revolutionising power: the impact of laser-based ohmic contact formation in SiC semiconductors

The realm of power electronics is witnessing a paradigm shift with the advent of silicon carbide (SiC). SiC is especially advantageous for applications in electric vehicles, renewable energy systems, and high-voltage power transmission.

BY 3D-MICROMAC

A PIVOTAL FACTOR in harnessing these advantages is the Ohmic Contact Formation (OCF) process, especially for 4H-SiC power semiconductor devices with their complex vertical structures. Efficient backside processing, which is integral to OCF, is a critical aspect in ensuring the operational efficacy and reliability of these devices.

The basics of ohmic contact formation

OCF is a fundamental yet complex process in the manufacture of semiconductor devices. It involves the creation of metal contacts on the semiconductor material, facilitating efficient current flow. For SiC devices, OCF is a challenging endeavor due to the material's inherent properties. The conventional approach typically involves the application of nickel or titanium layers. This process facilitates the transition from Schottky to Ohmic contacts, which is essential for efficient device operation. However, the traditional OCF methods, including high-temperature

annealing, pose significant challenges. They often lead to contact degradation, increased stress on the device and limited electrical properties, particularly in thinner SiC wafers, thereby necessitating more innovative and delicate approaches.

Advancements in laser-based OCF

The evolution of OCF in SiC semiconductors has taken a significant leap forward with the introduction of laser-based techniques. This innovative approach stands in stark contrast to the traditional high-temperature annealing methods. Laser-based OCF utilizes specialized laser systems, such as those employing nanosecond pulses, to form Ohmic contacts with a high degree of precision and control. The key advantage of using laser systems lies in their ability to deliver targeted energy to specific areas of the semiconductor. This localized approach minimizes thermal stress and potential damage, a crucial factor for maintaining the integrity of thinner SiC wafers – especially when their front side has been already processed with heat sensitive electrical applications.

Impact on SiC-Ni interface and device performance

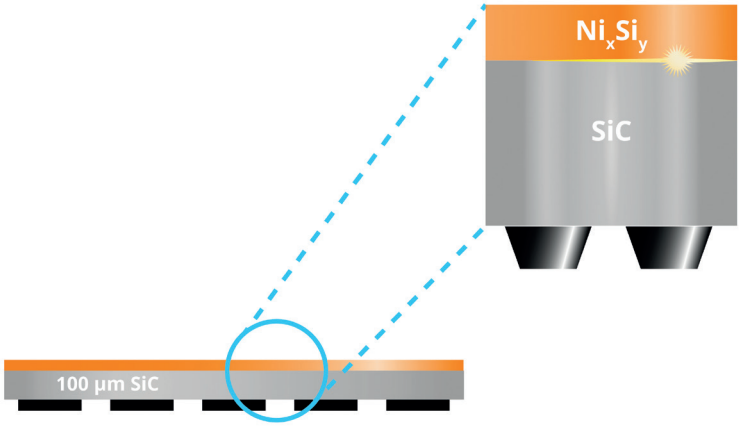
A study conducted by 3D-Micromac provides pivotal insights into the effects of laser-based OCF on the SiC-Nickel (SiC-Ni) interface, a critical aspect in the performance of power semiconductor devices.

This research is instrumental in demonstrating how advanced laser techniques enhance the efficiency and reliability of SiC devices, marking a significant advancement in semiconductor technology.

The study meticulously analysed the outcomes of using different types of lasers, including those with distinct beam profiles and pulse durations. The results clearly indicated that specific laser systems, particularly those with finely-tuned beam profiles and controlled energy output, were more effective in creating uniform and defect-free Ohmic contacts.

The key findings of the 3D-Micromac study revolve around the comparison of various laser systems and their impact on the SiC-Ni interface:

- **Laser System Comparison:** The top hat profile (see Figure 2), as used in 3D-Micromac's microPRO XS OCF system, demonstrated lower forward resistance compared to the Gaussian beam process, indicating a more efficient OCF process.
- **Impact of Wafer Parameters:** Wafer thickness and the grinding process significantly influenced forward resistance. Thinner wafers showed reduced forward resistance, underlining the importance of precise OCF in thinner wafers.
- **Laser Parameters Optimisation:** Adjusting the pulse to pulse overlap and the pulse energy density was found to be crucial. Higher energy density or pulse overlap resulted in lower forward resistance, though it was possible to increase throughput by reducing the overlap.



- **Wafer Material Influence:** Variations in dopant concentration within the wafer material affected the electrical characteristics, highlighting the need for uniform wafer processing.
- **Front Side Structure Preservation:** The study also confirmed that thermal laser annealing for OCF does not affect the surface structures, even with higher laser energy, making it suitable for thin wafers.

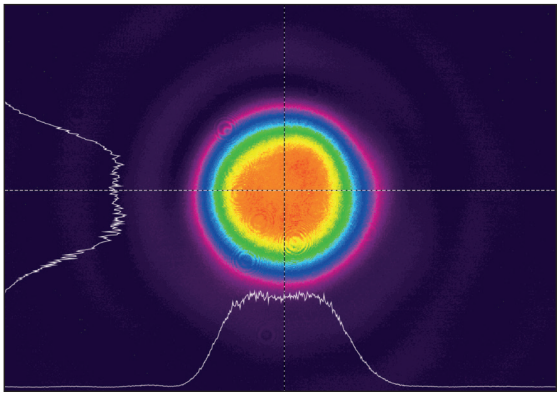
➤ Figure 1: The Ni-layer is annealed by exposure to laser radiation forming an ohmic contact formation based on Ni_xSi_y.

For this study two wafer runs were performed on SIC wafers with vertical resistor structures.

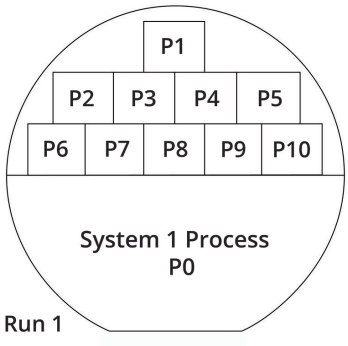
The wafers had a thickness of 80 and 175 µm. In particular for this evaluation, low forward resistance was the main quality criterion. A reference process (system 1) with a single annealing parameter was compared with the 3D-Micromac process, for which a parameter sweep was performed. With this, the pulse energy density and the pulse overlap were varied (Figure 3).

Figure 4 shows the results of forward resistance measurements on three wafer types. As can be seen the vertical resistance depends mostly on the substrate thickness, but also the grinding process.

The overall aim is to reduce vertical resistance. Following Ohm's law, a reduction in resistance leads to a decrease in the required forward voltage, improving the device's overall efficiency. The top hat process (P1 to P10) shows lower vertical resistance than the Gaussian beam process (P0) with an optimal resistance 10% lower than the reference.



➤ Figure 2: Flat top of laser spot



Parameter #	Pulse energy density [%]	Pulse overlap	Beam profile
P0	System 1	System 1	Gaussian
P1	78	Max	Top hat
P2	78	Middle	Top hat
P3	85	Max	Top hat
P4	85	Middle	Top hat
P5	93	Max	Top hat
P6	93	Middle	Top hat
P7	93	Min	Top hat
P8	93	Min	Top hat
P9	100	Max	Top hat
P10	100	Middle	Top hat

➤ Figure 3: Parameters of Run 1

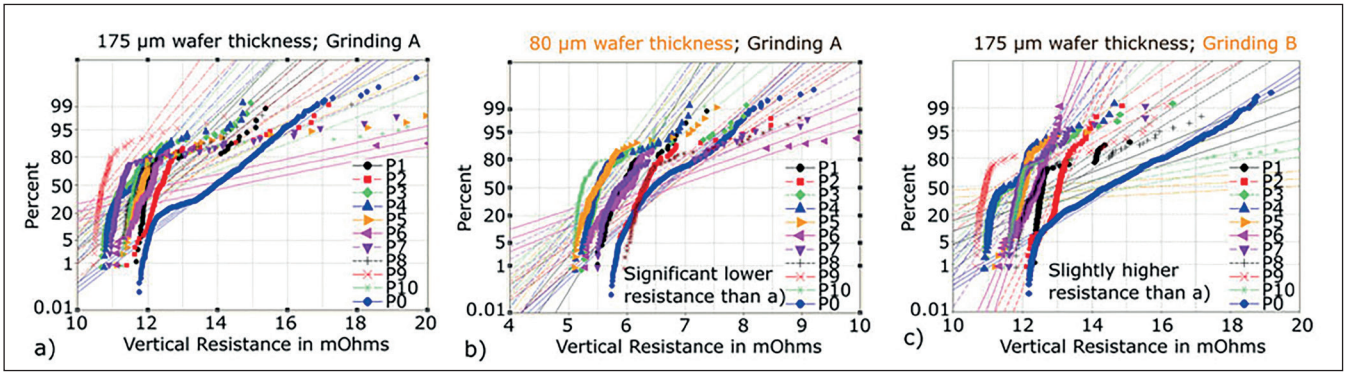
The second run was performed on 110 µm and 150 µm thick wafers with SiC JBS diodes to analyze the influence of the backside heat load generated by the OCF laser process on the front side structures. If the heat load at the front side is too high, it influences the electrical characteristic. This test is to prove the usability of the process for production. Again, only one OCF parameter set was used in the reference system 1. In the 3D-Micromac process, a parameter sweep was performed by varying energy density and pulse overlap (Figure 5).

It can be seen that minimum energy density with low pulse overlap increases forward voltage due to not entirely performed ohmic contact formation. This can be partially compensated by an increase in pulse overlap. A general increase in energy density beyond the mid value does not influence the forward voltage, independent from the actual pulse overlap. It has to be noted that the higher forward voltage at the wafer edge region results from inhomogeneous dopant distribution in wafer material (Figure 6).

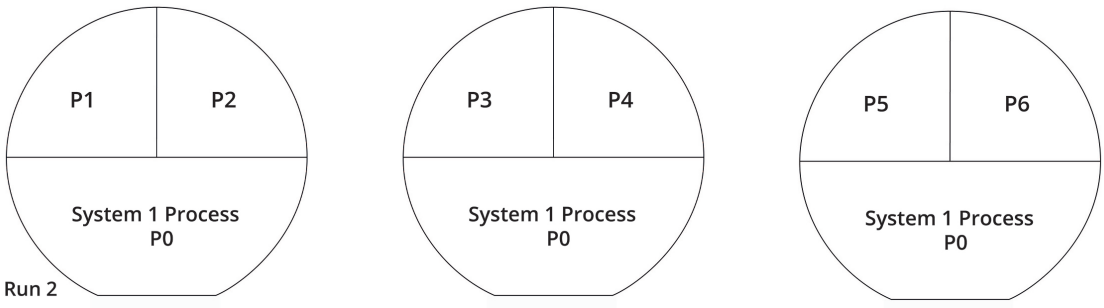
These advancements are not just incremental improvements but represent a significant leap forward in SiC device manufacturing. The enhanced interface quality, coupled with the increased efficiency and reliability of the devices, opens up new possibilities for complex semiconductor architectures. This could lead to the development of more powerful and versatile SiC-based devices, catering to the ever-increasing demands of modern power electronics applications.

These improvements at the SiC-Ni interface have profound implications for device performance. The study reported a marked reduction in contact resistance and an increase in the overall electrical conductivity of the devices. This translates to several key benefits:

- **Enhanced Device Efficiency:** The reduced contact resistance means that SiC devices can operate with greater efficiency, a crucial factor in applications where energy conservation and performance are paramount.
- **Increased Reliability:** The uniformity of the contacts ensures consistent performance across the device, reducing the likelihood of failures and enhancing the device's reliability.
- **Improved Thermal Management:** With better electrical conductivity, the devices can manage heat more effectively, which is vital for maintaining performance and longevity, especially in high-power applications.



➤ Figure 4: Distributions of forward resistance measurement on three wafer types. a) Grinding A with 175 µm thickness, b) Grinding A with 80 µm thickness, c) Grinding B with 175 µm thickness.



Parameter #	Wafer #	Pulse energy density [%]	Pulse overlap	Beam profile
P0	1,2,3,4,5,6	System 1	System 1	Gaussian
P1	1, 4	100	Min	Top hat
P2	1, 4	100	Max	Top hat
P3	2, 5	90	Min	Top hat
P4	2, 5	90	Max	Top hat
P5	3, 6	78	Min	Top hat
P6	3, 6	78	Max	Top hat

➤ Figure 5: Parameters of Run 2

Moreover, the study by 3D-Micromac highlighted the potential for further advancements in laser-based OCF techniques. The researchers noted that ongoing refinements in laser technology could lead to even more significant improvements in the fabrication of SiC devices.

Future implications and industry perspective

The advancements in laser-based OCF for SiC semiconductors are not just a breakthrough in manufacturing technology; they herald a new era in the power electronics industry. The implications of these developments extend far beyond improved efficiency and reliability of individual devices. They signal a transformative shift in how power semiconductor devices will be produced and utilized in the future.

One of the most significant implications of laser-based OCF is its potential to revolutionize wafer processing. By enabling more precise and controlled contact formation, this technique can lead to the development of SiC devices with even

Selective laser annealing going beyond

GENERALLY, selective laser annealing offers significant advantages over conventional annealing methods. Another innovative field of application for selective laser annealing is the programming of GMR and TMR (Giant- and Tunneling Magneto Resistance) sensors.

Conventional approaches such as large magnetic annealing furnaces or the utilization of special heating chucks limit the obtainable throughput for the proper programming of complex sensor wafers. Further, those approaches generate high production costs in combination with potential yield loss due to processing complexity.

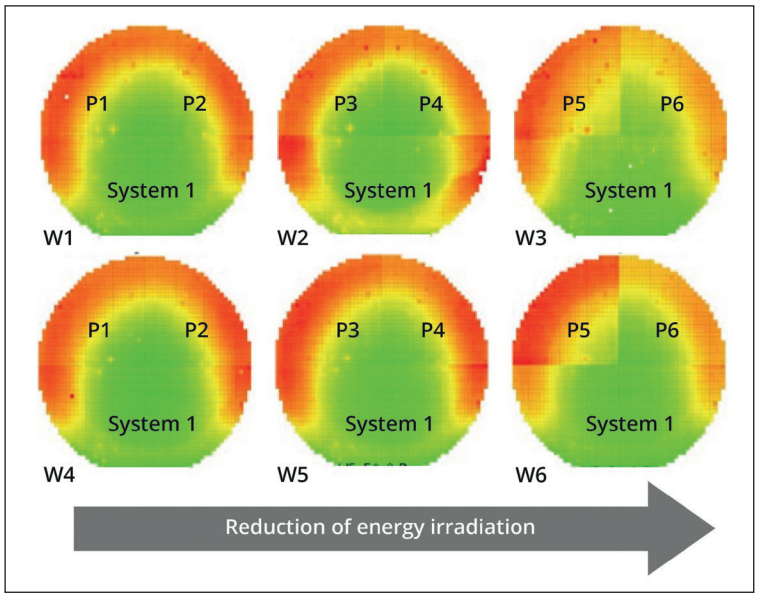
In contrast, selective laser annealing allows precise control of the annealing process, enabling targeted adjustments to material properties. The heat-affected zone beyond the sensor chip is only within a range of a few micrometers. As a result, individual sensors can be placed closer to one another and closer to logic elements, creating the perfect base for monolithic sensor designs.

By enabling a one-step process and eliminating additional production steps such as dicing or chip transfer, laser-based programming also grants high throughputs.

3D-Micromac has developed a solution enabling selective laser annealing in the production chain of GMR and TMR sensors. Their microVEGA xMR laser annealing system combines a selective laser spot with a local, in-situ rotatable magnetic field. The laser spot heats exactly one sensor area while a magnetic field with the correct orientation is applied. The system's unique selectivity and precision and its high flexibility in process parameters such as laser pulse energy, orientation, and sensor dimensions enable smaller sensors and new sensor designs.

This novel approach leads to superior sensor quality and streamlines the manufacturing process, presenting a notable shift towards more efficient and cost-effective production methods.

more complex and sophistica ted architectures. This opens up new possibilities for applications requiring high power density and efficiency, such as in electric vehicle powertrains and renewable energy systems. Furthermore, the scalability of laser-based OCF is a critical factor in its potential industry-wide impact.



➤ Figure 6: Forward Voltage: Colors green to red correspond to a minimum to a maximum per wafer. Wafers 1 to 3 are 150 µm thick. Wafers 4 to 6 are 110 µm thick.

The ability to efficiently produce high-quality SiC devices on a larger scale could lead to a reduction in manufacturing costs, making these advanced semiconductor devices more accessible and affordable.

This cost-effectiveness, coupled with the enhanced performance of SiC devices, could accelerate the adoption of SiC technology across various sectors, driving innovation and efficiency in power systems globally.

Conclusion

The exploration and implementation of laser-based Ohmic Contact Formation in Silicon Carbide semiconductor manufacturing mark a milestone in the field of power electronics. This technology not only enhances the efficiency and reliability of SiC devices but also paves the way for more advanced semiconductor architectures and applications.

As the industry continues to evolve, the significance of such innovative manufacturing techniques cannot be overstated. They are key to meeting the growing demand for high-performance electronic components and will play a crucial role in shaping the future of power electronics, propelling the industry towards more sustainable and efficient power solutions.

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Increasing power density, reducing power consumption

At the recent International Solid-State Circuits Conference (ISSCC) 2024, CEA-Leti and the University of California San Diego reported on the development of an IC for piezoelectric resonator DC-DC conversion achieving a 310% loss reduction. In a separate paper, CEA-Leti also described a novel architecture for keyword-spotting in always-on, voice-activated edge-AI systems – delivering accurate speech recognition at power consumption below one microwatt.

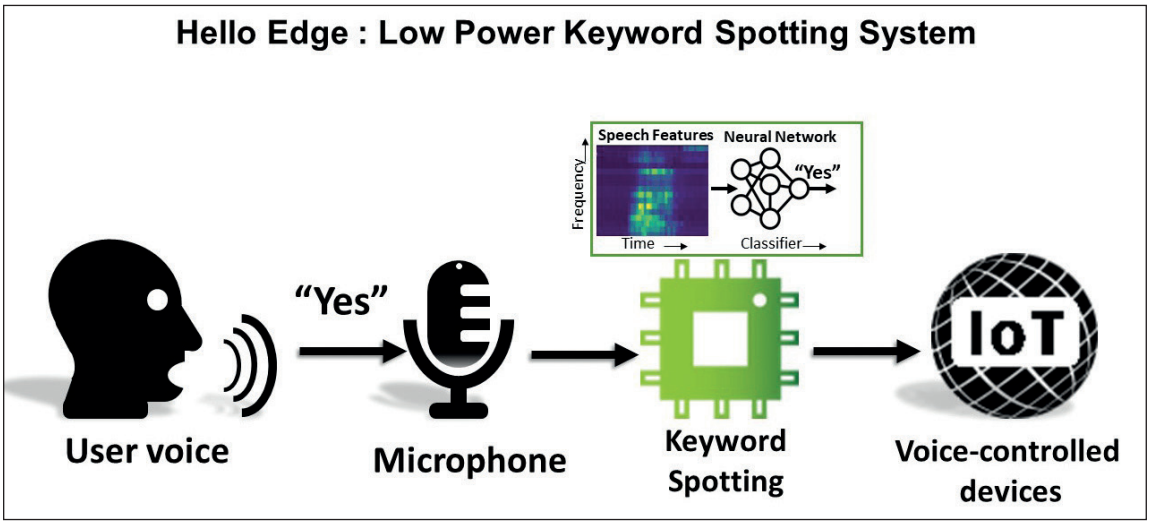
UNIVERSITY OF California San Diego and CEA-Leti scientists have developed a ground-breaking piezoelectric-based DC-DC converter that unifies all power switches onto a single chip to increase power density. This new power topology, which extends beyond existing topologies, blends the advantages of piezoelectric converters with capacitive-based DC-DC converters.

The power converters the team developed are much smaller than the huge, bulky inductors currently used for this role. The devices could eventually be used for any type of DC-DC conversation, in everything from smart phones, to computers, to server farms and AR/VR headsets. The results were presented in the paper, “An Integrated Dual-side Series/Parallel Piezoelectric Resonator-based 20-to-2.2V DC-DC Converter Achieving a 310% Loss Reduction”, Feb. 20 at ISSCC 2024 in San Francisco.

“The Dual-side Series/Parallel Piezoelectric Resonator (DSPPR) is the first IC used for PR-based power conversion, and achieves up to 310% loss reduction over prior-art published and co-designed discrete designs for VCRs<0.125,” the paper reports.

“This innovative approach enhances performance, especially at low voltage conversion ratios—an area where prior works struggled to sustain both high efficiency and optimal utilization of piezoelectric materials,” said Patrick Mercier, a professor in the Department of Electrical and Computer Engineering at UC San Diego and a senior author of the paper.

The paper explains that a hybrid DSPPR converter exploits integrated circuits’ ability to offer sophisticated power stages in a small area compared to discrete designs, and enables efficient device operation at voltage conversion ratios (VCR) of less than 0.1.



"The IC provides a distinct opportunity to consolidate all power switches onto a single chip, significantly diminishing the PCB footprint and enhancing phase-control precision," said Gael Pillonnet, scientific director of CEA-Leti's Silicon Component Division.

In addition, incorporating additional capacitive-based converter stages, both pre- and post- the piezoelectric DC-DC converter, contributes to performance improvement. "This strategic integration reduces the demand on piezoelectric material, resulting in a more compact converter with a notably smaller total volume. The marginal increase in additional capacitors, which is less than 10 percent, pales in comparison to the substantial gains facilitated by the proposed topology," Pillonnet said.

"The DC-DC converter, particularly in the low VCR range, which was a focus of our work, has widespread applications in various sectors, such as high-power computing servers, automotive systems, USB chargers, and battery-powered devices," said Wen-Chin Brian Liu, a Ph.D. student in Mercier's research group and the lead author of the paper.

Accurate speech recognition, low power consumption

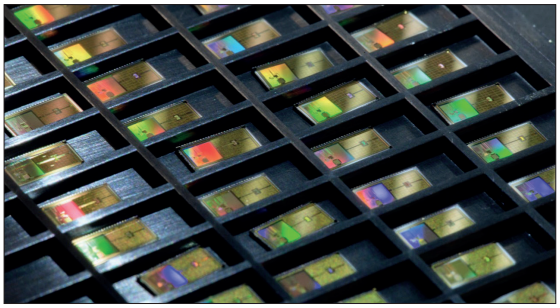
CEA-Leti has developed a keyword-spotting system that dramatically improves accuracy in always-on, voice-activated Edge-AI systems and that consumes less power in a far smaller silicon footprint than current technology.

Presented in a paper at ISSCC 2024 in San Francisco, the new architecture uses time-domain signal processing on oscillators locked by injection and is suitable for devices running on energy harvesters, which supply power below 0.5V. The paper, "0.4V 988nW Time-Domain Audio Feature Extraction for Keyword Spotting Using Injection-Locked Oscillators", reports accurate speech recognition at power consumption below one microwatt. It describes the first injection-locked, oscillator-based time-domain audio feature extraction (TD-FEx) demonstrating keyword spotting operating down to 0.4V, while achieving 91 percent accuracy on 10 words. TD-FEx information is not coded as a voltage but as a time delay of two clocks' signals. In addition to being well suited for advanced nodes, its advantages are digital-like implementation with low-supply voltage and better noise immunity than current systems. CEA-Leti's system demonstrated accurate speech recognition with power consumption below 1 µW.

Some analog-based audio feature extraction (FEx) units using multi-channel Gm-C bandpass filters can supply 10 times the power efficiency of digital FEx units in a comparable silicon area. "However, analog FEx circuits have not demonstrated KWS with more than four keywords," the paper reports. "They also suffer from a large footprint, challenging technology migration and limited dynamic range at low supply voltage, while speech signals have inherently a high dynamic range."

"Our system's silicon area of 0.15mm2 is at least 3.5 times smaller than prior art on the same process node of 65nm," said Ali Mostafa, lead author of the paper. "With a power of 988nW, our system is nine times more power-and-area efficient than ring-oscillator-based TD-FEx."

Applications beyond speech recognition for this system include predictive maintenance and health monitoring that require on-line frequency decomposition of the sensor data.



Enabling the future with next generation power devices

KAZUHIRO UEDA, PRODUCT PLANNER OF WAFER TEST SOLUTIONS AT KEYSIGHT TECHNOLOGIES JAPAN, explains the importance and increasing needs of parametric tests and the test challenges for high-voltage parametric tests as next-generation power devices are developed to meet a growing quantity and variety of applications in the automotive industry and beyond

THE MOVE towards carbon neutrality and zero emissions is a global industrial challenge. As a result, we are seeing a new wave of initiatives, applications, and technologies coming to the market that offer a more sustainable approach, with a focus on green and renewable energy, power savings, and power efficiency.

The automotive industry in particular has achieved great strides with the move towards electric vehicles (EV) and hybrid electric vehicles (HEV). However, we also need to look beyond the vehicles themselves and consider how sustainable and efficient the entire infrastructure and industry is. This means looking for new power technologies when it comes to the wider infrastructure such as charging stations and adjacent applications.

Central to many of these applications is the use of semiconductors. Although silicon (Si) based power devices have been mainly used across the industry, there is a growing need for more innovative technology that can provide power efficiency while enhancing device performance. To address this, Wide Band Gap (WBG) devices such as silicon carbide (SiC) and gallium nitride (GaN) have been intensively researched as they offer superior characteristics such as higher breakdown voltage, power density, and efficiency. For example, the EV sector is already migrating towards higher voltage (800V) battery systems to improve driving distance, charging time, weight, and space. This requires higher performance capabilities that go beyond what conventional devices can offer, with the need for higher voltage tolerance to exceed 1kV. Next-generation power devices such as SiC/GaN can meet these needs in a smaller footprint when compared to traditional silicon.

These challenges also transcend the automotive space, with several other industries seeing the need for power device innovations as well. All of which is driving a robust demand for the manufacturing of next-generation power devices. Leading power device manufacturers are gearing up to produce SiC/GaN devices more than before. Yole Group, a French market research firm, predicted that SiC/GaN devices will capture a 30% share of the total power semiconductor market within the next five years.

Increasing parametric test needs for power devices

As the manufacturing of power devices continues to accelerate, parametric tests are critical to ensure device reliability. New process and device technologies such as GaN on Si enable integrating low-voltage (LV) device block and high-voltage (HV) device block on the same chip. This provides

a smaller footprint while also enhancing functional integration and voltage beyond 1kV to be able to support automotive applications. Growing demand from EV/HEV and automotive electrification requires the high-volume production of these advanced power devices. As a result, the wafer size is also becoming larger in diameter, progressing from 6 inches to 8 inches and even up to 12 inches to meet the demand. This shift is not only confined to traditional Integrated Device Manufacturers (IDM) but also extends to foundries that are entering the wafer manufacturing market in a move to meet the diverse market needs.

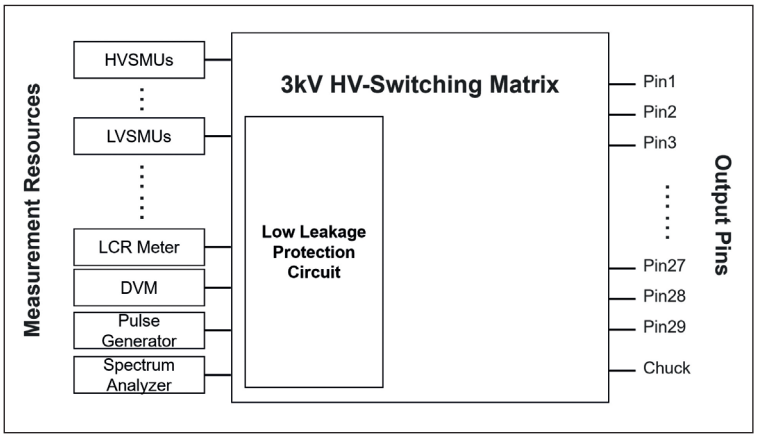
As we move towards the wafer manufacturing of high-performance/high-voltage integrated power devices, manufacturers need to manage device reliability, yield, the overall cost of final products as well as the potential risks that market failure presents. In order to achieve this, it is critical to proactively test at the wafer process phase, much earlier than the final product testing.

To control and improve these manufacturing goals, it is key to perform electrical characteristics measurements in the production line of power semiconductor wafers. This is more commonly referred to as a "parametric test", and it is an established wafer test process in the front-end production line, used particularly for low-voltage devices such as advanced semiconductor devices. The purpose is to control and improve the product quality.

The parametric test involves taking electrical measurements for the test element group (TEG), which consists of a group of devices such as resistors, capacitance, and transistors. These are dedicatedly designed for parametric test purposes, rather than for final product chips. In a parametric test, various measurements are performed such as sub-pA leakage current, threshold voltage, breakdown voltage, capacitance, resistance, and much more as part of process control monitoring (PCM). Those electrical measurements help to detect the failure and variation on a wafer and improve the wafer manufacturing process when it comes to quality, reliability, and yield. The parametric test data is also widely used by wafer foundries as wafer acceptance test (WAT) data for wafer users.

As explained above, various devices and characteristics need to be tested on a wafer. Therefore, the test system needs to have a wide range of accurate and precise measurement capabilities, coupled with flexible switching capabilities of the test equipment/measurement unit, and seamless connectivity with a wafer prober and a probe card for conducting measurements. For this purpose, the industry widely relies on a dedicated parametric tester.

These are designed to enable automated measurement with high accuracy, speed, and



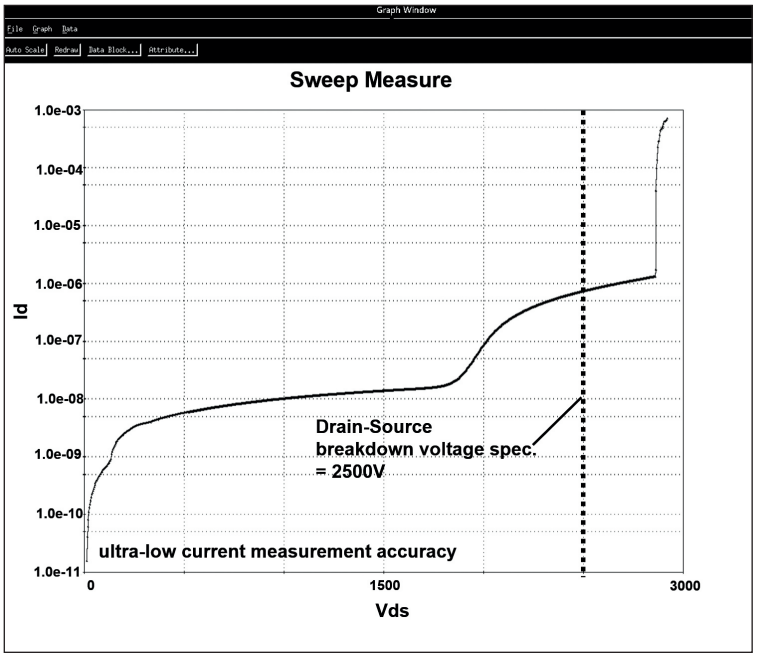
➤ Figure 1. 3kV HV-Switching Matrix (HV-SWM).

efficiency while switching the measurement resources using a switching matrix (SWM). Typically, a parametric tester is equipped with a source measure unit (SMU) for current-voltage (IV) characteristics, ensuring precision in sub-pA low current measurements. In addition, it usually features an LCR meter for capacitance-voltage (CV) measurement, a pulse generator, a digital volt meter (DVM), and much more.

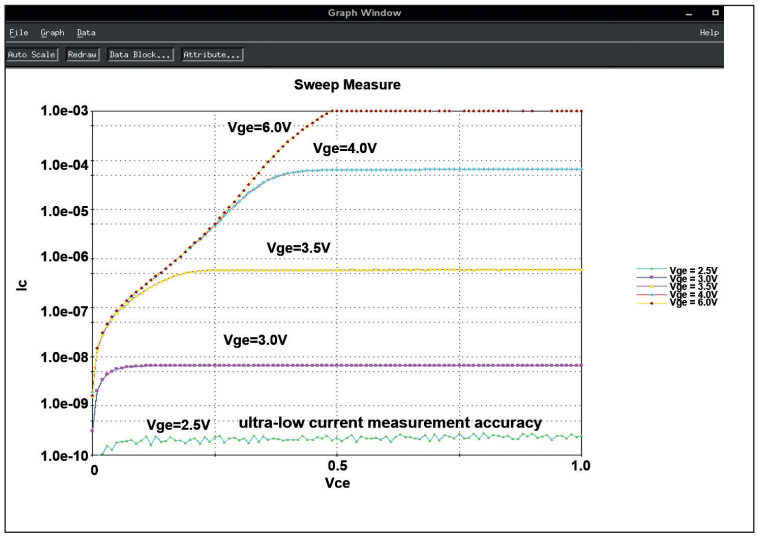
Parametric test challenges for high voltage power devices

While the need for parametric testing is essential in order to improve device reliability and yield, there are several challenges when it comes to performing the parametric test with high-volage devices that don't appear in low-volage testing.

The first challenge is that most parametric testers are in fact designed for low-voltage device testing. Therefore the voltage range is limited to several



➤ Figure 2. The measurement example as a result of a high-voltage MOSFET (Vdss spec = 2500V) using Keysight's new high-voltage parametric tester.



➤ Figure3. The measurement result of output characteristics (Vce-Ic) of transistor (IGBT).

hundred volts, and it cannot cover high-voltage device testing requirements. One possible solution is using an existing high-voltage test system such as a chip tester in combination with the low-voltage parametric tester to complement the missing high-voltage coverage. However, such high-voltage test systems are not designed for parametric tests, so the low current measurement performance, measurement accuracy, measurement flexibility and connectivity are not optimised for parametric tests for TEG. In addition, the combination of a low-voltage tester and high-voltage tester would be costly when it comes to both test efficiency and footprint.

A second idea explored is using a special parametric tester designed to cover both high-voltage and low-voltage measurements. However, usually high-voltage parametric testers have some limitations when it comes to the number of high-voltage applicable pins and the flexibility of connections due to the technical difficulties of high-voltage relays and switches.

In addition, typical high-voltage parametric testers don't have sufficient voltage coverage for next-generation power devices exceeding 1kV or more. This means that the device under test needs to be changed, such as changing the probe cards to test all desired devices leading to additional effort and test time.

Wafer manufacturers also need to pay attention to operator safety, and they need to ensure they have the right protected equipment to safeguard against hazardous voltage and other areas of concern when it comes to high-voltage testing. For example, compressed dry air (CDA) would need to be used with a high-voltage probe card to suppress arc/discharge at the probe pin tips.

From a facility management perspective, wafer manufacturers will need to ensure safety regulations are met and in compliance with SEMI S2 for a test system. Considering the automotive space as an example, the test system would be required to meet the general requirements for the competence of testing and calibration laboratories to satisfy the requirements of the International Automotive Task Force (ISO-17025).

There is no comprehensive solution in the market that can meet the increasing needs of parametric tests for high-voltage devices. Thus, power device manufacturers are facing the challenges of test limitation, test cost, test time, and safety and regulatory requirements.

The breakthrough solution for high voltage parametric test up to 3kV

To overcome the challenges posed by high voltage parametric testing, a new type of parametric tester with a switching matrix (SWM) tolerant beyond 1kV is needed. One of the key solutions is to develop a switching matrix that can support both high-voltage and low current in one pass test.

The use of newly designed high-voltage relays allow 3kV switching while meeting the isolation and safety requirements to comply with the safety requirements for electrical equipment for measurement, control, and laboratory use (IEC61010). The new high-voltage relay also provides active guarding to enable sub-pA current measurement by preventing leakage current.

As shown in Figure 1, the low leakage protection circuits are built in to protect and prevent the low-voltage measurement sections from damage due to misconnection even for a 3kV measurement environment. The system is equipped with so many unique and breakthrough technologies to make itself the only choice for high-voltage parametric tests. The new high-voltage parametric tester integrates new HV-SWM up to 30 pins including a

Keysight is a leading parametric tester company and Keysight's 4080 parametric tester has a large install base at many customers in worldwide. Keysight's Wafer Test Solutions (WTS) developed a high-voltage switching matrix (HV-SWM) to strike this balance in various ways.

chuck terminal with high-voltage SMU(HVSMU) up to 3kV and low-voltage SMU (LVSMU) proven by de-facto standard B1505A power device analyser in SiC/GaN research and development. In addition, capacitance measurement up to 1kV, pulsed measurement and traditional measurement can be performed by other instruments used in low-voltage parametric tester. This system is also designed to meet regulatory needs such as safety regulations, SEMI S2 compliance and ISO17025 certificate. This system can integrate with a wafer prober and probe card to perform high-voltage testing as a total system.

These comprehensive measurement capabilities will enable manufacturers to perform various measurements across different devices more accurately and with flexibly.

In this measurement, the voltage is swept from low-voltage (0V) to high-voltage (3kV) seamlessly. Measurement captures the Idss characteristics (Vds-Id) from pA range low current and rapid current increase by breakdown around 2900V.

As shown, low-voltage device characteristics can also be measured accurately as well as conventional low-voltage parametric tester up to 1A. As of early 2024, the new high-voltage parametric tester is being jointly evaluated by multiple power semiconductor leaders.

KAZUHIRO UEDA is a Product Planner of Wafer Test Solutions at Keysight Technologies Japan. He has a wealth of experience in R&D and marketing of semiconductor products and industrial solutions. He received B.S. and M.S. degrees in information engineering from Hiroshima City University, and received a MBA from Waseda University, Japan.

Looking ahead

Carbon neutrality and the move toward zero emissions continue to be the next-generation challenge across all industries as we look to mitigate the effects of global climate change. As shown in the EV/HEC space we are starting to see strong strides being made.

As we look ahead, the innovation of power semiconductor technologies and next-generation power devices such as SiC/GaN are expected to be a key solution, and will enable the industry to move from research and development to production on a mass scale. With this in mind, the importance and increasing needs of parametric tests and the test challenges for high-voltage parametric tests should not be overlooked.

The second electrical revolution?

Solid-state based, DC extraction directly from AC mains without the use of rectifier bridges, transformers and high voltage, bulk capacitors.

BY THAR CASEY, AMBERSEMI CEO

IT'S JUST POWER...or is it? With the continued flourishment of intelligence and automation in homes, workplaces and public spaces, smart technology in buildings has continued to evolve at a breakneck pace over the last few years. However, the industry that powers these various devices and electrical endpoints accessed daily by billions of people in residential, commercial, and even industrial buildings around the world, has ironically remained largely stagnant for decades.

But why has the power electronics sector lagged so far behind the very products it supports? One reason: slow, uninspiring innovation to 1950s-era industry standard components and limited topology options, lacking the kind of true disruptive technology breakthroughs that pushed so many other categories forward into the 21st century.

The good news? There's an opportunity for power electronics to finally evolve (modernize) their power architecture and fundamentally break through the limitations they face from legacy status quo power products; it's an opportunity to tap a once in a generation fundamental architecture change - an upgrade and modernization of the core technology foundation that powers these solutions globally.

How so? With the adoption of modern, solid-state silicon chip solutions that digitally manage electricity, breakthrough functions and feature expansions are now possible in electrical products without a change in standard form factors. This includes the capabilities of AmberSemi's AC Direct DC Enabler™ architecture to extract DC directly from AC mains without the use of rectifier bridges, transformers and high voltage, bulk capacitors.

This breakthrough solid-state power technology allows for new electric product design possibilities and intelligence capabilities that were previously unatainable. And once industries complete the shift to solid-state solutions, they never turn back, as with categories like tube TVs conversion to solid-state TVs or computer's spinning magnetic hard drives to solid-state hard drives.

At its core, this generational architecture upgrade is a classic Silicon Valley semiconductor story. It's the consolidation of old-school, outdated technologies into a tiny silicon chip, capable of replacing the function of standard electromechanical components. And, in the process, it enables more features potential and much beter operational flexibility, all with smaller size footprint and improved reliability that comes from solid-state architecture.

However, the potential impact of this "second electrical revolution," led by companies like Amber Semiconductor, is far more profound than merely being another step in the iterative progression that has defined this space for years. Let's dive into the specifics behind how this technology will truly harness the potential of innovation.

Footprint Efficiency, Power density and configurability

Today, electrical products companies are feature constrained by BOTH power delivered and product form factors. Any increase in feature scope is highly likely to require an increase in form factor size which can be costly at best - not viable at worst.

AmberSemi's breakthrough digital control of electricity, integrated into a semiconductor IC device allows for more compact, more dynamic power designs, and represents a generational architecture

upgrade to power technology across the electrical product landscape. And it delivers such capabilities without requiring deviation from universal form factors of end products. The dramatically smaller system size enabled by AmberSemi's AC Direct DC Enabler IC's, for example, open physical space for more features and/or slimmer product form factors, which can generate cost savings and provide a myriad of benefits.

In fact, AmberSemi's AC Direct DC Enabler IC's are the industry's most size-effective and claims the industry leading power density at 5 Watts per 0.21 in3 (1.47 cm3). This creates enhanced power density, making solid-state architecture particularly appealing in applications where space is limited, such as portable electronics, circuit breaker boxes, power distribution units, and even electric & traditional gas-powered vehicles.

In addition to AC Direct DC Enabler ICs' competitive breakthrough benefits (smaller, more modern and more programmable), the devices offer additional functionally and configurability by providing access to the internal programmable registers through the embedded Serial Peripheral Interface (SPI). When paired with a processing unit, the result is an intelligent power conversion solution, enabling real-time reporting on a range of internal operations, such as monitoring of alarm events and data-logging of sub-system loads.

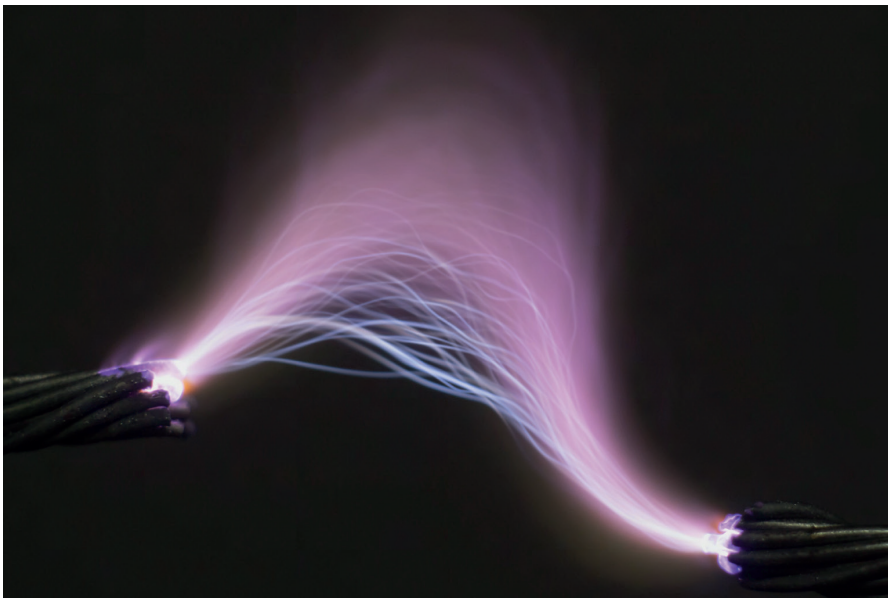
Reliability and Durability

Solid-state architecture enables power electronics companies to achieve higher levels of reliability and durability compared to traditional solutions. The AC Direct DC Enabler™ architecture uses lower voltage rated capacitors than traditional systems, which means our IC can support ceramic, polymer, and electrolytic capacitors. Therefore, designers have flexibility to more easily optimize their design for performance, cost, space constraints, and reliability.

A dramatically lower component count also contributes to increased reliability, as well as enhanced sustainability. With up to 50% fewer components for the power delivered versus standard power supplies, AmberSemi's unique AC Direct DC Enabler ICs' technology reduces electrical and thermal stress of critical components, enabling efficient heat dissipation and reducing the risk of component failure due to overheating. It even offers the ability to use ceramic capacitors instead of electrolytics in cases where reliability is of the highest importance (as in switch mode power supplies.) As a result of all of these and other capabilities, electrical products companies can leverage more reliable and longer-lasting power solutions that truly enhance the quality, and value, of their products.

Flexibility and scalability

Modern solid-state power architecture solutions, such as AmberSemi's AC Direct DC Enabler™ ICs,



enable a change in design engineers thinking about what is now possible in their products. The reason for this is that solid-state architecture and digital management of electricity offers greater flexibility and scalability compared to traditional power electronics solutions. This flexibility opens up new possibilities for design engineers to optimize their products for specific applications, meet a wide variety of customer requirements, and accommodate future technological advancements - while keeping the same solid-state system architecture /device. With a wide input voltage range of 24- 277VAC AmberSemi's AC Direct DC Enabler ICs allow a single design to be used across a global product portfolio.

In future designs, the input voltage independence of Amber's technology will provide even more value to higher voltage industrial applications in which traditional products struggle.

Additionally, products like AmberSemi's AC Direct DC Enabler™ ICs offer the opportunity for consolidated architecture. The chip can be easily integrated into a variety of generic and modular design architectures, allowing for scalability and system expansion, where architecture can be more dynamic and have broader power application. In addition, it uniquely delivers global compatibility within a single device. Design engineers can leverage this feature to develop solutions that can adapt to varying power demands, creating the potential for end product line SKU reduction, and allowing them to be adaptable to changes in the system architecture.

In the end, integration of AmberSemi's new power management architecture provides customers with versatile and future-proof power supply solutions, while also enabling the opportunity for streamlined end product footprints with the power flexibility to also include more functions.

Dynamic power & sustainability

In addition to being smaller, safer, and more reliable, the power derived from AmberSemi's AC Direct DC Enabler IC's are far more dynamic because electricity is managed digitally, which enables substantially more control. It delivers dynamic power through software, enabling configurable output voltage ranges with automated mode switching to optimize efficiency for all power outputs.
By embracing solid-state chip architecture, power module companies can actively support the transition to a more sustainable energy landscape. This advantage can be attained because the architecture, as discussed above, requires fewer components and is more durable - reducing the need for replacement parts, which contribute negatively to the carbon footprint through production emissions.

Conclusion

The opportunity for electrical product companies to upgrade their power supply solutions to solid-state is not just another iterative step in the longstanding pattern of technological advancement – it's a generational architecture breakthrough. Solid-state transformation changes the design calculus of electrical engineering in ways that were previously thought to be: impossible. History tells us that once market categories move to solid-state, they convert quickly, and never look back to the legacy old tech standards. With AmberSemi's innovations knocking on the electrical product industry's door, the dawn of a second electrical revolution may be right around the corner.

Nordic Semiconductor and AmberSemi announce partnership to explore opportunities with Amber's breakthrough power products and Nordic Semiconductor solutions

NORDIC SEMICONDUCTOR and Amber Semiconductor have entered a multi-faceted partnership to explore sales, marketing, and development initiatives to bring new solutions to markets, such as smart electrical products, and other wirelessly integrated applications.

The initiatives anchor on the partners offering Nordic technology platforms powered by Amber Semiconductor's products, as well as developing unique reference designs for targeted customer segments. In addition, as the partnership matures, deeper development opportunities may be targeted as key customer requirements and opportunities are identified, refined, and addressed.

"We are pleased to partner with AmberSemi on exploring productization and market opportunities around its breakthrough AC to DC conversion products and our semiconductor solutions," said Geir Kjosavik – Director for Power Management ICs with Nordic Semiconductor. "As Nordic is expanding into wireless IoT markets that require AC power, we find AmberSemi's compact power solutions an ideal complement to our own power management solutions for battery powered products. We feel that together, with AmberSemi, we can bring new transformative and very competitive semiconductor solutions to our current and new customers," he concluded.

"We are very excited by our partnership with such a great, forward-leaning partner as Nordic," said Thar Casey, CEO at AmberSemi. "As we enter the commercialization phase for our silicon products, this partnership with Nordic represents a significant inflection point and accelerator towards adoption of truly compelling and unique semiconductor solutions in the market."

AmberSemi discovered a way the physics of electricity is managed differently - digitally - in silicon chips. The company's mission is to transform electrical product power management architecture globally from outdated, 1950's-era electro-mechanical power technologies, standard today in every electrical product, to smaller, safer, and smarter silicon chips.

"Building & home control and video surveillance together constitute a $3 billion market for power semiconductors, said Paul Pickering, Semiconductors Practice Lead, Omdia. "The smart building market, in particular, includes numerous applications that require AC/DC conversion in a space-constrained environment. Examples include building safety (smoke and gas detectors) security (video surveillance, building access control), climate control and smart lighting. Omdia forecasts growth in low-power AC/DC regulators will outpace the overall market by 31% from 2022 to 2027," concluded Pickering.

Mr. Casey continued: "Our products enable dramatically smaller power solutions, creating space for a significant expansion of features in wirelessly integrated smart products, without a change in product formfactors. This dynamic is relevant and disruptive to the crowded product structures of today's IOT products."

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AI increases data centre energy demands

No two individuals might agree on the exact impact of AI, both in terms of the demands it will make on the data centre environment which will host these new, compute-hungry applications or its wider impact on our work and leisure activities. However, all would agree that this disruption will be profound and that ways of deploying AI workloads without a corresponding huge increase in data centre energy consumption need to be found.

INFINEON TECHNOLOGIES recently launched its TDM2254xD series dual-phase power modules, designed to enable best-in-class power density, quality and total cost of ownership (TCO) for AI data centres. The TDM2254xD series products blend innovation in robust OptiMOS MOSFET technology with novel packaging and proprietary magnetic structure to deliver 'industry-leading' electrical and thermal performance with robust mechanical design. This lets data centres operate at higher efficiency to meet the high power demands of AI GPU (Graphic Processor Unit) platforms while also significantly reducing TCO.

Infineon introduced the TDM2254xD series' design allows for efficient heat transfer from the power stage on to the heat sink through novel inductor design that is optimised to transfer current and heat, thereby allowing for a two percent higher efficiency than industry average modules at full load. Improving power efficiency at the core of a GPU yields significant energy savings at scale. This translates into megawatts saved for data centres computing generative AI and in turn leads to reduced CO 2 emissions and millions of dollars in operating cost savings over the system's lifetime.

Meanwhile imec (as reported elsewhere in this issue) has introduced a 'breakthrough' architecture that lays the foundation for a whole new generation of analog-to-digital converters (ADCs). Imec's massively time-interleaved slope-ADC design offers high power efficiency and a very compact footprint, while promising to enable exceptional conversion speeds. As such, it is ideally suited to meet data centres' exploding data processing and throughput demands, driven by the surge in cloud computing and (generative) AI applications.

Joris Van Driessche, program manager at imec, explains: "On the one hand, our massively time-interleaved slope-ADC design exploits the paradigm that slow-speed, but extremely small channels make for a more efficient conversion per area. Secondly, by arranging (lots of) these channels in a two-dimensional array, the length of the interconnection lines is minimized, and the power dissipated through parasitics is reduced. As a result, higher power efficiency and scalability can be achieved, while significantly reducing the ADC's surface area."

These are just two examples of the way in which the semiconductor industry is responding to the anticipated huge growth in data-driven AI applications. While many existing data centres are wrestling with the practicalities of attempting to adapt their existing infrastructure to be AI-capable, there is also a whole programme of new, AI-optimised data centre builds planned across the globe.

A recent Uptime Intelligence Keynote Report, 'Five Data Center Predictions for 2024', acknowledges the potential for something of an AI-powered applications 'arms race', with demand for AI-accelerators currently outstripping supply. This competitive situation will push chip power envelopes as chipmakers compete for superior performance. The report suggests: "Cloud infrastructure will also inevitably push up silicon design power further and faster. In a few years, mainstream servers with up to 1 kW of realized power use will be common. This trend affects the design of all current and future server processors and accelerators, and shapes model line-up and pricing decisions.'

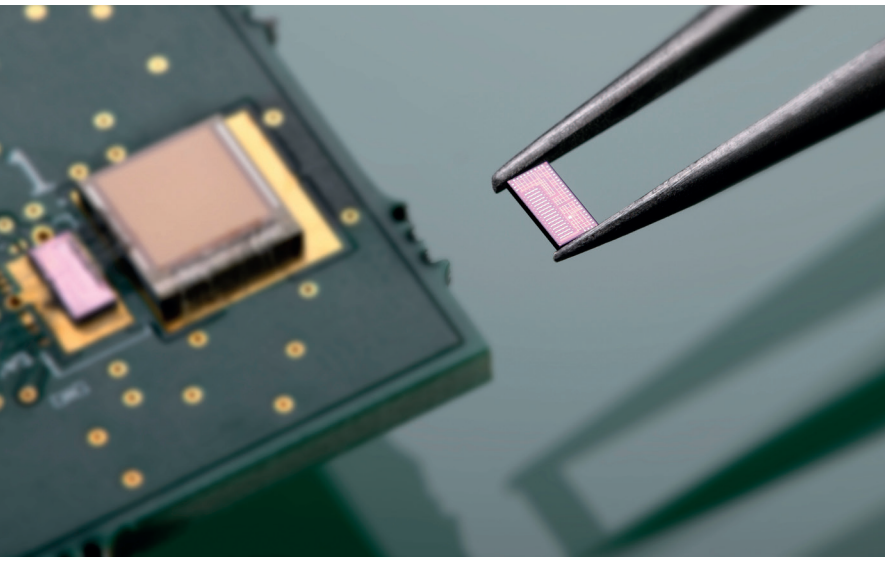
The challenge (and opportunity) that lies ahead, as evidenced by the Infineon and imec examples featured, is how can data centre capacity and the high-performance compute requirements of AI and other demanding workloads be met without a correspondingly significant increase in power consumption? At a time when data centres are increasingly being portrayed as power-hungry 'enemies' of the road to Net Zero (never mind that they only exist to serve the needs of our digital world), such work is urgent.

ADC 'breakthrough' highlights power efficiency innovations

Imec research developments featured at the recent International Solid-State Circuits Conference (ISSCC) 2024, included a massively time-interleaved slope-ADC prototype chip demonstrating 'superior scalability' to meet data centers' exploding bandwidth and data processing demands; a novel ultrasound-powering technology paving the way to miniaturised and minimally invasive neural implants; and a low-power, ultra-Wideband (UWB) receiver chip said to be ten times more resilient against interference from Wi-Fi and (beyond) 5G signals.

IMEC INTRODUCED a breakthrough architecture that lays the foundation for a whole new generation of analog-to-digital converters (ADCs). Imec's massively time-interleaved slope-ADC design offers high power efficiency and a very compact footprint, while promising to enable exceptional conversion speeds. As such, it is ideally suited to meet data centers' exploding data processing and throughput demands, driven by the surge in cloud computing and (generative) AI applications.

Training AI models requires massive computing power, necessitating data centers to invest in increasingly powerful optical networks for fast, reliable communications between servers, storage devices, and networking equipment. But since data centers' optical communication networks need to operate at higher and higher speeds, their components grow in size and power consumption.



A new architecture that overcomes the limitations of time-interleaved SAR ADCs

A critical component of optical transceivers, today's wireline ADCs are mostly based on time interleaving of (large numbers of) successive approximation register (SAR) ADCs that feature tens of parallel high-speed channels. As such, when scaling to sampling rates far beyond 100GS/s, the SAR ADC approach results in a significant area increase and long interconnection lines, translating into substantial parasitics and energy loss. To support the insatiable bandwidth and data processing demands of wireline applications and their need for ever faster ADCs, imec proposes a new ADC architecture that overcomes these limitations.

"On the one hand, our massively time-interleaved slope-ADC design exploits the paradigm that slow-speed, but extremely small channels make for a more efficient conversion per area. Secondly, by arranging (lots of) these channels in a two-dimensional array, the length of the interconnection lines is minimized, and the power dissipated through parasitics is reduced. As a result, higher power efficiency and scalability can be achieved, while significantly reducing the ADC's surface area," said Joris Van Driessche, program manager at imec. Proof-of-concept: a 42GS/s 7b 16nm massively time-interleaved slope-ADC prototype chip.

At ISSCC, imec presented a proof-of-concept of its new ADC architecture in the form of a 42GS/s 7b massively time-interleaved slope-ADC prototype chip.

"Even at the relatively modest speed of 42GS/s, the benefits of our approach are clear. Implemented in 16nm FinFET technology, our prototype chip

contains an array of 768 slope-ADCs – with a core active area of just 0.07mm^2. This is at least a factor of two smaller than conventional approaches. It also has a state-of-the-art power consumption of 96mW," commented Joris Van Driessche. "In other words, this is the first proof that our novel architecture works. And its benefits will only become more significant as we move to higher speeds (150GS/s and beyond)."

In fact, a 5nm ADC using the same architecture is currently being completed – targeting sampling rates well above 150GS/s while achieving extremely low power consumption. In parallel, the team has started exploring a 2nm implementation, targeting speeds in excess of 250GS/s.

"We believe this is an important stepping stone in the development of a whole new generation of small-area, low-power ADCs to support tomorrow's wireline applications. It overcomes the limitations of SAR ADC implementations, which risk running out of steam when required to operate at extremely high speeds," concluded Van Driessche.

Imec is inviting additional partners to join this research effort – such as fabless companies specializing in the development of wireline connectivity building blocks. Moreover, licensing options are available for those companies seeking access to imec's ADC IP blocks.

Imec has a long track record in developing high-speed integrated circuits for photonics applications. One of its research tracks is aimed at creating optical transceivers (and their various building blocks) that can keep up with the exploding data rates of wireline applications. Late last year, for example, imec researchers at Ghent University developed an optical receiver achieving a gross data rate of 200 Gbps by co-integrating a traveling-wave SiGe BiCMOS transimpedance amplifier with a silicon photonics Ge photodetector to combine the need for speed with a scalable and affordable implementation. The pursuit of a new generation of ADCs and DACs clearly complements this research effort, taking ADC development to a whole new level.

Compact wireless powering technology

Imec's ultrasound-based proof-of-concept for wireless powering of implantable devices is a solution of just 8 mm x 5.3 mm enableing precise beam steering (up to a 53-degree angle) and requires 69 percent less power consumption – believed to make it the smallest, lowest power consuming, wireless ultrasound powering unit among state-of-the-art systems. The cutting-edge concept of global charge-redistribution adiabatic driver addresses challenges associated with traditional tethered connections or batteries and paves the way for minimally invasive, wireless (neural) implants.

The need for wireless powering

Intracortical neural recordings, key for understanding and treating neurological disorders, face challenges in their powering. Traditional invasive wiring risks complications such as scarring and infection, while battery integration (removing the necessity for tethering) brings size and chemical leak concerns.

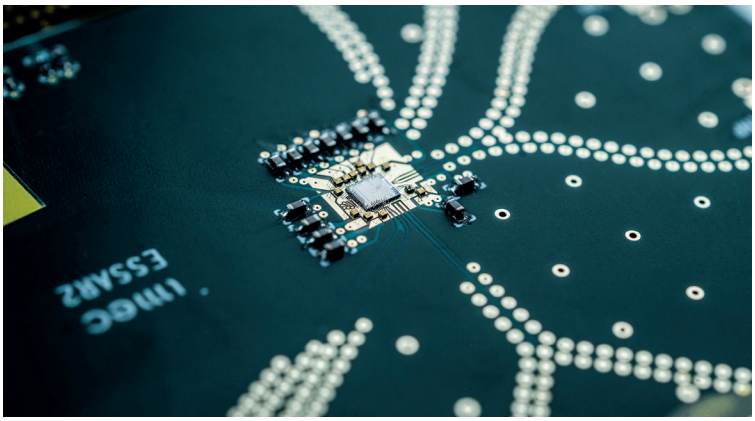
The use of global charge-redistribution adiabatic drive: a paradigm shift

Eliminating the need for invasive procedures or bulky components, imec and Delft University of Technology have designed ultrasound technology that wirelessly delivers power to neural implants, successfully traversing distances from the skull to the brain's cortex, within the ERC-funded "Intranet of Neurons" project.

To realize this, the researchers introduced a unique adiabatic driving technique based on the concept of "global charge redistribution" (GCR). Unlike traditional adiabatic driving methods, this approach leverages the parasitic capacitors of the ultrasound transducer array itself and recycles charges. This eliminates the need for external capacitors to redistribute charges and allows for a more compact design. The chip, fabricated in 65nm CMOS, features a fully integrated 116µm×116µm driving unit that allows for 69 percent power savings compared to conventional class-D driving. This design makes it both the smallest ultrasonic adiabatic driving unit with the lowest power consumption among state-of-the-art systems.

For in vivo use, beam steering up to large angles (>45°) is critical to maximize power delivery and compensate for brain micro-movements and misalignments (such as those occurring during surgery and respiration). With the introduction of a beam steering controller, imec's GCR scheme enables beam steering up to 53 degrees.

"While many neural implant technologies are currently making significant progress in sensing



and stimulation, wireless interfaces, as one of the crucial components of implants, still have much room for improvement - particularly in terms of power efficiency and form factor. To bridge this gap and unlock the full potential of neural implants, we are leveraging our unique wireless-, powering-, and telemetry technologies, to develop minimally invasive wireless systems tailored for miniaturized implants, with applications beyond intracortical neural implants", commented Yao-Hong Liu, Scientific Director at imec. "We aspire to showcase the practical application of our technology in real in vivo conditions, with our ongoing advancements, particularly in areas such as micro-system integration and packaging, and welcome collaborations with medical professionals or researchers."

The article "An Ultrasound-Powering TX with a Global Charge-Redistribution Adiabatic Drive Achieving 69% Power Reduction and 53° Maximum Beam Steering Angle for Implantable Applications," provides a detailed overview of the technological advancements, including the proposed architecture, circuit design, and performance metrics. This project Intranet of Neurons has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation program (grant agreement No. 101001448).

Low-power UWB receiver chip

Imec's low-power ultra-wideband (UWB) receiver chip is said to be ten times more resilient against interference from Wi-Fi and (beyond) 5G signals than existing, state-of-the-art UWB devices. Imec's breakthrough chip is a major step forward in developing and deploying next-generation UWB applications, which are becoming increasingly safety-critical. Think of child presence detection systems in the automotive sector, where reliability and assured availability are paramount, or manufacturing environments, where UWB's precise localization capabilities could ensure the safety of human workers operating near robotic arms, AGVs, and other automated machinery.

In the coming months and years, the spectrum allocated for ultra-wideband communications (typically spanning the 6 to 10GHz frequency range) will face increasing competition from other wireless technologies that eye the same frequencies to extend their reach. The recent approval of Wi-Fi 6e, for instance, positions it to operate in the 5.925 to 7.125GHz band. And (beyond) 5G technologies are also expanding into the upper 6GHz band – given that their existing frequency ranges risk running out of steam. For the UWB industry, this requires proactive measures, especially as UWB technology moves beyond (traditional) secure keyless entry applications to safety-critical automotive and industrial automation functions. In other words, there is a growing need for solutions that allow UWB and other wireless technologies to coexist seamlessly in the same frequency bands.

Imec's new IR-UWB receiver: -13dBm blocker resilience, and 7.6mW power consumption
Imec's new impulse radio (IR) UWB receiver chip – implemented in a 22nm FDSOI process, and with a compact active area of 0.32mm^2 – stands out as a pioneering solution to avoid interference between UWB and other wireless signals.

To enhance the receiver's blocking performance, a transformer-coupled bandpass filter (BPF) is integrated into the complementary common gate (CCG) stage of the UWB low-noise amplifier (LNA) front-end. As such, imec's receiver exhibits an exceptional -13dBm blocker resilience, making it ten times more resilient against Wi-Fi and (beyond) 5G interference compared to existing solutions. Moreover, several circuit design optimizations enable the receiver to achieve its outstanding interference resilience at the lowest power consumption (7.6mW). This efficiency allows the receiver analog front-end (AFE) to operate ten times longer on the same (battery) power compared to current IEEE 802.15.4a/z compatible UWB devices, and twice as long as described in recent research papers. The use of bandpass filters is a widely accepted method for dealing with unwanted signals, such as Wi-Fi, before they enter the receiver. However, imec's patented implementation to reduce intermodulation distortion significantly increases the receiver's robustness at low power and low supply design.

"To foster its industrial adoption, our UWB receiver not only complies with the existing IEEE 802.15.4z standard; it is also ready to support the upcoming IEEE.802.15.4ab standard. We believe this research, and the underlying collaboration in high-impact industrial ecosystems, are critical steps to enable future wireless technologies to coexist seamlessly across various use cases," said Christian Bachmann, program director of wireless sensing at imec.

Imec works with industrial partners across the UWB ecosystem through R&D partnerships and IP licensing. Looking ahead, imec is committed to remain at the forefront of UWB innovation. imec invites companies to join its UWB R&D program and extensive partner network.

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Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

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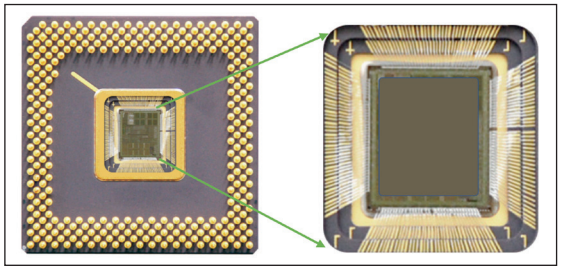
Effective hermetic sealing for next-generation microelectronic packaging

A perfectly sealed electronic package can fulfill its intended function without disruption, error or a significant reduction in performance for decades. However, design and field engineers can only achieve this level of performance by applying the right materials and sealants, and employing the correct tools, equipment and process steps to build semiconductor-driven electronic packages for the next generation. The confidence engendered by a well-sealed package inevitably leads to the development of better chips with more features.

BY RAMESH KOTHANDAPANI, TECHNICAL DIRECTOR, MICROELECTRONIC PACKAGING, MATERION CORPORATION

HERMETIC SEALING is an important process for packaging semiconductor chips. The word "hermetic," in this case, suggests leak-safe sealing. A semiconductor chip goes through several process steps, starting as a wafer before being cut into individual chips and eventually ending up in a discrete package. Such chips are strongly bonded to die pads with a die-attach epoxy or eutectic solders. They are then electrically connected to the ceramic package bond pads with very fine wires.

The ceramic package – in effect a "chip carrier" – is generally multi-layered with electrical feedthroughs within its ceramic body. These layers are internally connected to the bottom or sides of the package to be mounted onto printed circuit boards along with other electrical components. An array of packages is available for chip bonding, including leaded chip carrier (LCC); ceramic, quad, flatpack (CQFP), and quad-flat package (QFP), among others.



➤ The ceramic package with semiconductor chip attached via bonding materials. The image on the right shows the fine wire bonds to the bond pads. Each bond pad is internally connected to the pins surrounding the package.

The ceramic package containing the chip with wire bonds must eventually be hermetically sealed to prevent the entry of contaminants such as moisture or loose particles.

The hermetic sealing process is vital to determining the viability of the assembly in operation. Illustration 1 shows the semiconductor chip and its hundreds of very fine wire bonds. These chips range in size from a few millimeters to tens of millimeters. Smaller chips may have fewer wire bonds, while larger chips can have hundreds. These bonds are thinner than a human hair, with diameters as small as 0.0007 inch (17.78 microns).

Discrete chips contain micro-electromechanical systems (MEMS) with super-fine gears, clocks and moving actuators that cannot be seen with the naked eye. Any particles that deposit on these chips are likely to interfere with their performance. Equally, with the bonded fine wires so close to each other, conductive particles or moisture between the wires could cause a malfunction. This makes proper hermetic sealing of the assembled packages even more important.

Before focusing on the sealing process, it's important to know about materials which are used for sealings, its limitations, the design guidelines, storage, and handling processes.

There are, for example, several types of ceramic packages:

- Surface mount ceramic packages
- Ceramic pin grid array packages
- Ceramic quad flat packages
- Ceramic hybrid packages
- Fiber-optic communication packages
- The bonding materials or solders
- The components which have to be attached to he package such as dies, die attach materials, wires and etc.

Depending on the level of hermeticity required, packages undergo one or two sealing processes: seam-sealed with a metal lid, or solder-sealed with a plated metal lid.

SEAM-SEALED WITH METAL LID:
This is a reliable hermetic sealing process in which a pair of round electrodes run around the edge of the lid, melting and fusing it to the package's seal ring area. Seam sealing is useful when:

- The semiconductor chip cannot accept high levels of heat. Seam seal offers localized edge heating.
- The user may not have oven reflow capability.
- The end application is RF-related with a low level of hermeticity required (i.e., RF packaging).

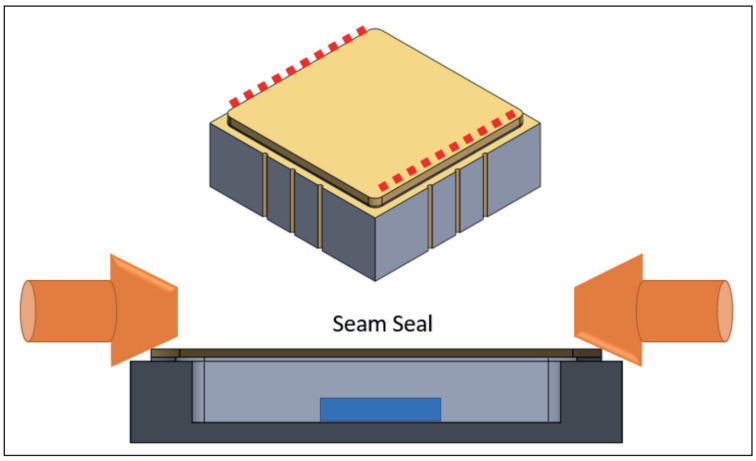
SOLDER-SEALED WITH PLATED METAL LID:
This process can also achieve high levels of reliable, airtight sealing. Several post-seal tests are available to confirm its effectiveness.

Some factors are common to all package types, including the use of die-bond pads, wire bond pads and seal rings. Illustration 3 shows some key features of the ceramic package.

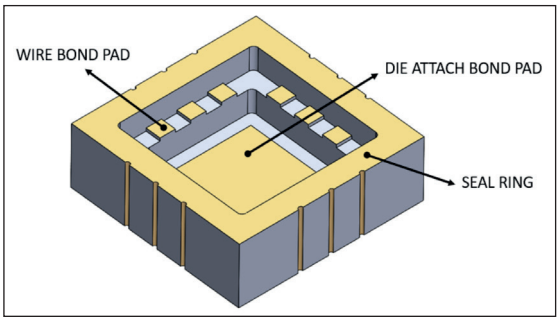
DIE-ATTACH PAD: This is the area where the semiconductor chip is attached with the aid of eutectic solder alloy or epoxy materials. Epoxy-based die-attach adhesives typically comprise a resin and a hardener, which must be well mixed before being applied to the die pad. The chip is then put into place and scrubbed with pressure to initiate wetting and release any trapped gasses in the bonding materials. The assembly is cured at high temperatures to harden it, a potentially tricky process that must be properly controlled.

Both 88Au12Ge and 80Au20Sn can be used as eutectic bonding materials. They melt at 361°C and 280°C, respectively. After considering the heat loss into the fixtures and other components, the set temperature is usually higher. Both types of eutectic solders are pure alloys without any binders or bonding agents.

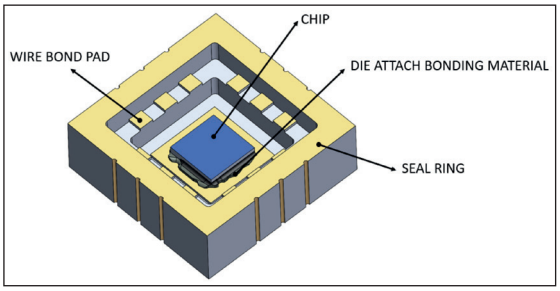
The selection of the die-attachment bonding material is subject to the coefficient of thermal expansion (CTE) of the chip and other neighboring materials with which the bonding agent may come



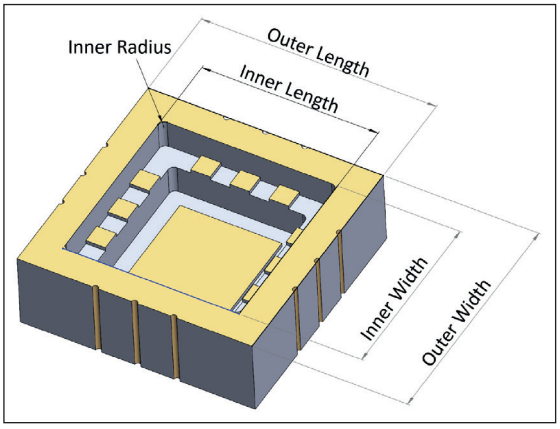
➤ The ceramic package is seam-sealed with two electrodes running parallel to melt the lid and seal it to the ceramic or metal package.



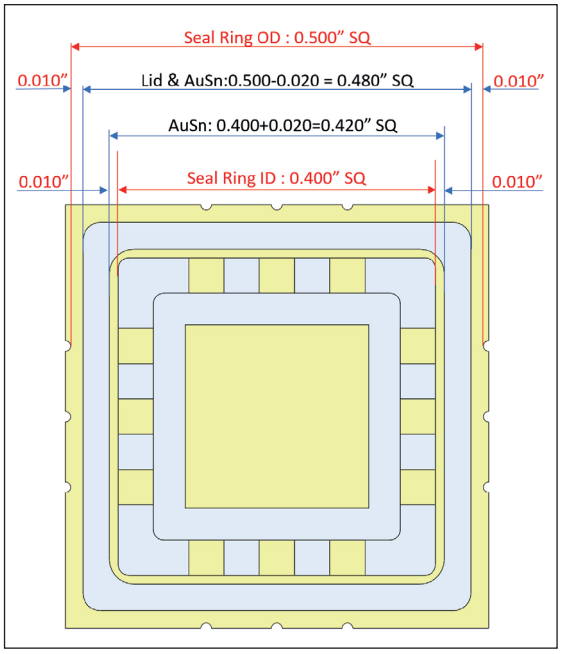
➤ The ceramic package with seal ring and wire and die-bond pads.



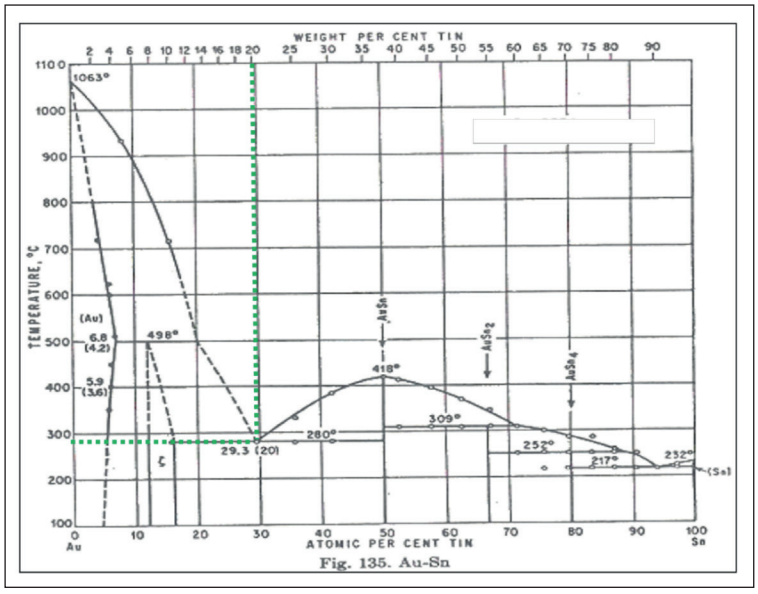
➤ The ceramic package with chip attachment.



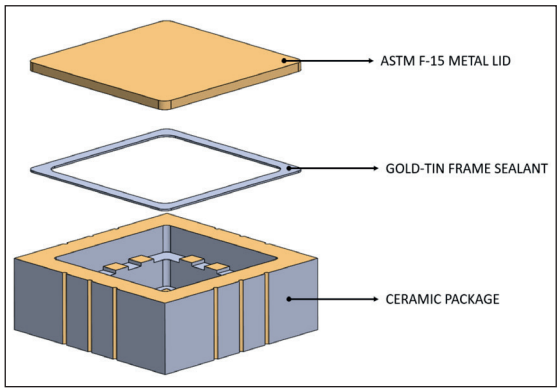
➤ Ceramic package with seal ring dimensions.



➤ Design guidelines for package lid and solder.



➤ Illustration 7. Gold-Tin phase diagram.



➤ Exploded view of ceramic package, solder frame and plated metal lid.

into contact. Melting and curing temperatures and conditions must also be determined.

CHIP ATTACH POST-SEAL CONDITIONS:

It is important to validate secure bonding and ensure the release of trapped gasses. Suppliers will generally provide curing instructions and process steps to remove organics and binders. Otherwise, hydrogen-saturated hydrocarbons or moisture could release during the solder hermetic sealing process. Trapped gases within the package will negatively affect its overall electrical performance and lifespan.

Consequently, a well-controlled die-attach process is important for achieving void-free bonding. Unfortunately, post-seal validation can be costly and may produce irregular or misleading results. Close attention must be paid, then, to storage conditions, expiry date, mixing ratio, duration of use, and volume required per unit per shift. There is also the looming possibility of moisture absorbed from the environment.

SEAL RING:

This is one of the most important components in the ceramic package when it comes to hermetic sealing. As is the case with die and wire bond pads, nearly the full surface of the seal ring is used in the soldering process. The seal ring surface is generally porous and plated with nickel and gold, which could lead to nickel migration to the seal ring at elevated temperatures. This in turn may result in pin holes and solder voids. Thus, careful handling and temperature control are essential.

Effective hermetic sealing: Step-by-step

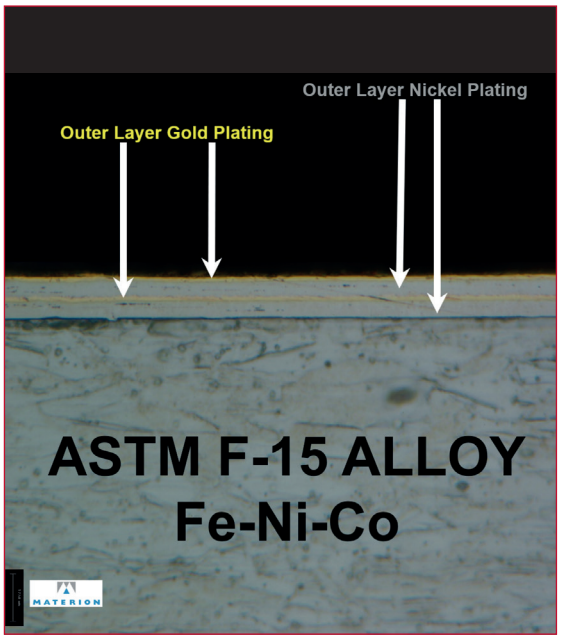
Successful hermetic sealing is dependent upon several factors, including:

- Design guidelines for the package seal ring
- Sealant and lid material selection
- Sealing methods and process controls
- Post-hermetic sealing tests and troubleshooting
- Next-generation packaging material options

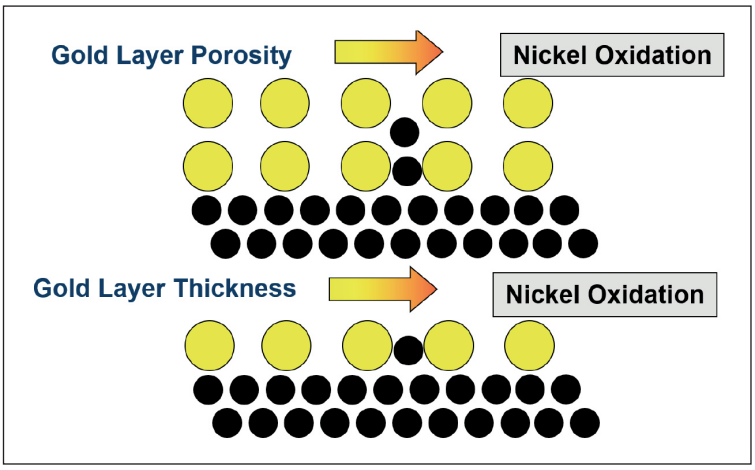
DESIGN GUIDELINES OF THE PACKAGE SEAL RING:

Consider the size of the hermetic cover lid and its solder. The outer seal ring, the metal lid, and the gold-tin frame are key design elements. For example, if the package seal ring outer length and width is 0.500” square, the lid should 0.500 inch - 0.010” - 0.010”, or 0.480” square.

Next is to determine the gold-tin solder inner dimensions. For this, both inner and outer dimensions must be considered. If the seal ring inner dimensions are 0.400” square, then the gold-tin solder inner dimensions should be 0.400” + 0.010” + 0.010”, or 0.420” square. The inner and outer radii are also important for the overall design, as is the thickness of the solder and lid. These dimensions will be based upon the size of the final package.

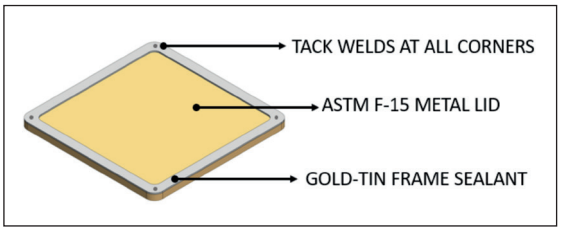


➤ Cross section image of four layers plated sequentially with nickel and gold.



➤ Nickel migration process.

The 0.010” clearance relies on the availability of space for the seal ring. It can be as low as 0.002” for the outer gap, and almost as low for the inner seal ring if the ring is narrow.

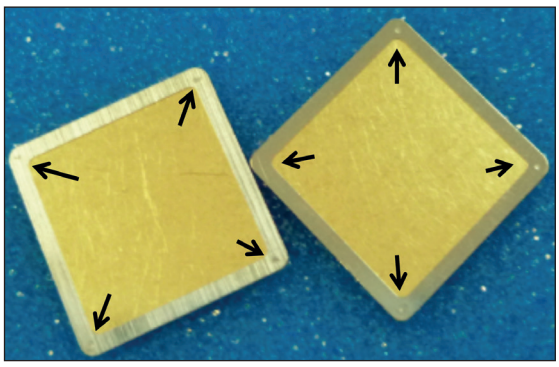


➤ Frame lid assembly.

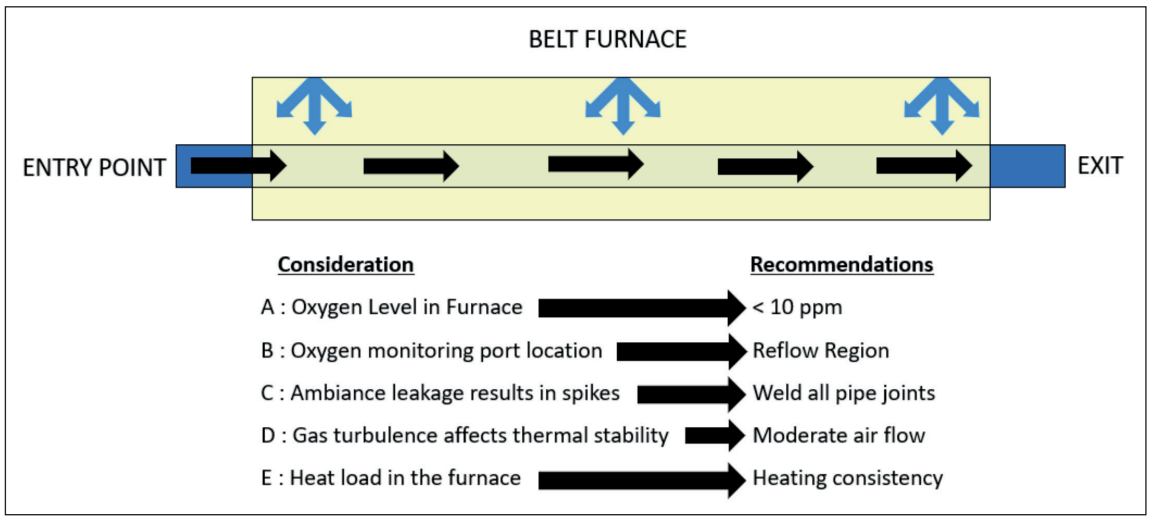
SEALANT MATERIAL SELECTION:

There is a variety of suitable solder alloys and eutectic solders for leak-safe hermetic joints. Gold-tin has been proven particularly effective for bonding metal lids to ceramic or metal packages. The 80% gold/20% tin solder melts at 280°C and holds up well when subjected to temperature cycle testing.

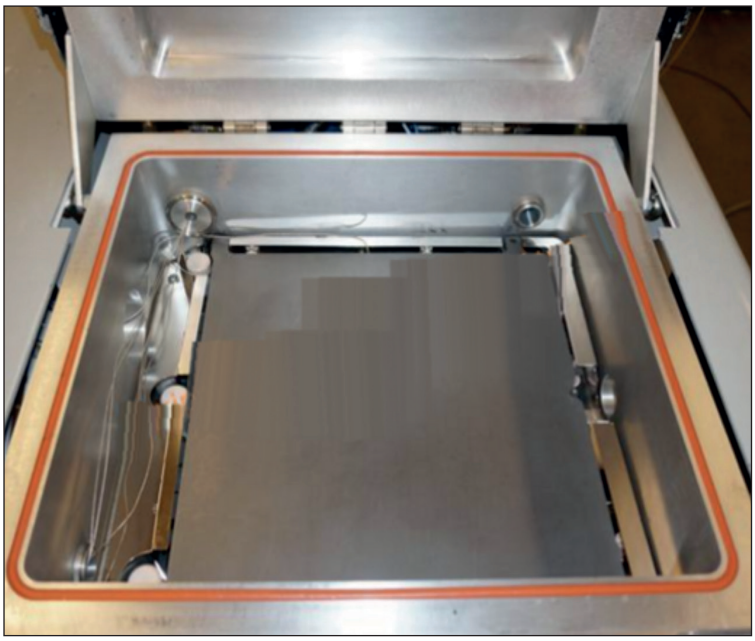
The 80% gold/20% tin alloy must be manufactured with very few impurities and must be within its nominal weight percentage to achieve a good bond.



➤ Tack weld points at corners.



➤ Illustration 13. Critical parameter controls and recommendations for effective hermetic sealing using a belt furnace.



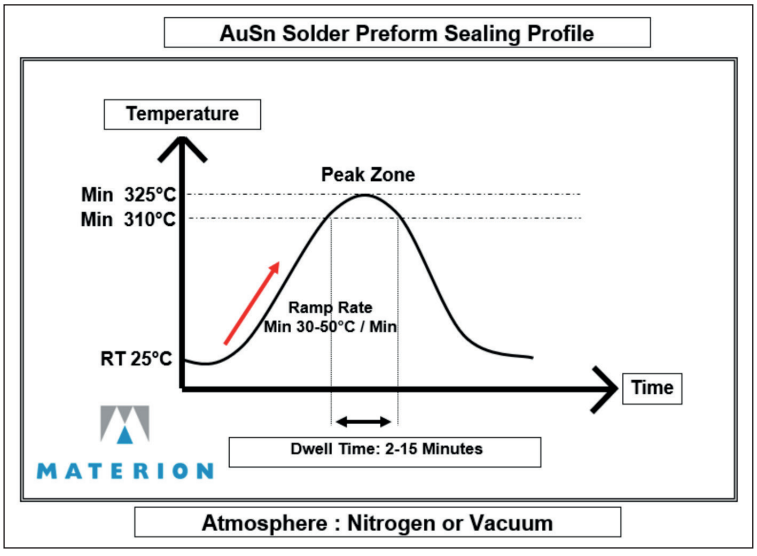
Vacuum furnace inner chamber.

- **Gold-tin purity:** Decrease in heat conductivity
- **Gold-tin contamination:** Oxides, organics
- **Gold-tin interfacial contact area**

COVER LID MATERIAL SELECTION:

The metal lid is an alloy of iron, nickel and cobalt, also known as ASTM F-15. In order for the gold-tin solder to bond well with the package, the metal lid must be well prepared. A lid composed of more than 50% iron (Fe) elements could oxidize over time. A bare lid will not allow gold-tin solder wetting. Reliable gold plating is therefore essential.

The lid is electroplated with 100 to 350 microinches of nickel, followed by gold at a thickness of 50 microinches. Additional nickel and gold are plated for high-reliability applications, though the sum of both nickel films cannot exceed 450 microinches, while the sum of the gold-plated films must be at least 50 microinches. The idea is to prevent excess build-up at the edges. which could eventually have a negative effect on the hermetic seal. The following illustration shows a cross-section of the four-layer plated lid.



Gold-tin reflow profile.

EFFECTIVE PLATING:

The plating process is extremely critical. Edge build-up, for example, must be avoided. The electroplate bath and chemistry maintenance are both important. It should be noted that this plating is not cosmetic in nature, but is rather designed for high-quality hermetic sealing, which also entails good solder bonding. Poor maintenance plating could trap unwanted gases.

Post-plate tests are available to check the quality of the plating, particularly to quantify hydrogen content in the plated films.

Plating bath maintenance and bath chemistry checks should be performed periodically for preventative reasons. Post-plate bakeouts are also sometimes performed following last-stage plating at lower temperatures (between 120°C to 150°C) for 8 to 12 hours.

High-temperature bakeouts for longer durations could cause the inner layer of nickel to migrate to the gold layer and interfere with solder wetting. The gold-tin solder alloy will not wet with nickel. Nickel migration may also occur if the plated layer is too thin or demonstrates high porosity on the plated surface.

Sealing methods and process controls

- **Tack Welding or Spot Welding:** The gold-tin solder must be attached to the plated lid by spot or tack welding. This process is crucial to avoiding misalignment and other defects that could eventually affect seal yield. It also creates additional benefits for end users who must assemble the frame and lid as a single component before final sealing. Tack welding requires very small portions of the eutectic gold-tin solder at all four corners to melt and adhere to the plated lid.

- **Reflow equipment and process controls:** It's important to select the proper reflow equipment prior to sealing. Hermetic sealing with gold-tin or other solders requires an inert environment; otherwise, oxidation might affect the integrity of the seal. If a belt furnace is used, the maintenance and seal profiles must be well monitored. Oxygen content within the reflow chamber should be tracked and controlled. Similar monitoring is required if a vacuum seal furnace is chosen, with the additional benefit of removing unwanted gasses. In both cases, equipment performance will ultimately determine the quality of the hermetic seal.

- **The gold-tin seal profile:** Following are key considerations for the gold-tin seal profile:

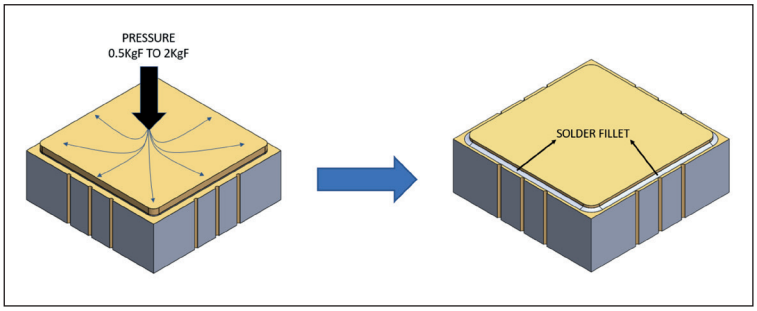
- **Rise rate:** The rise rate must be gradual and slow. This helps to release gasses from the various components without promoting nickel migration. Such migration may result from a quicker ramp-up, especially with porous-plated layers. Vacuum furnaces will evacuate any outgasses, while a belt furnace with nitrogen pressure should do the same.

- **Peak temperature:** Eutectic gold-tin solder melting temperature is 280°C. In addition to the sealing components, fixtures, clips and other materials can also pull in heat. Once the solder and lid reach peak temperature, the goal should be the complete removal of gases, complete solder flowing, solder fillet formation, and the elimination of pin holes or void removal. Duration of exposure to peak temperature is very subjective and depends on product size, ssembly tools and conditions. Reducing this duration while critical processes are in progress can uncover failure modes, which can be observed visually, through leak tests or under X-ray.
- **Ramp down from peak zone:** Product cooling must also be done gradually, as sudden cooling or ejection of the product from the oven can be quite harmful.

- Adequate pressure should be applied to gold-tin solder to achieve a good hermetic joint. Interestingly, though, only about 0.5 to 4 kilogram-force is required. In all cases the pressure is transferred from the lid down to the gold-tin sealant (see Illustration 16). As mentioned, this pressure is very helpful during the peak temperature phase to press the lids and squeeze out molten solder to form a fillet.

SEAL CLIPS:

There are many different types of readily procurable clips. Depending on the type of package and production volume, pressure clips can be customized and fabricated. The aligning fixture should also be considered if increased production volume is desired.



➤ llustration 16: Left, assembly with pressure applied. Right, post-seal with solder fillet.

POST-SEAL RELIABILITY TEST:

Post-seal reliability tests validate process and material selection. Several different levels of tests are performed one after another. Details of all listed tests can be found in standard Mil-883 guidebooks.

NEXT-GENERAL PACKAGING MATERIAL OPTIONS:

These tests are intended to confirm successful hermetic sealing. Similarly, an effective packaging process can significantly prolong the life of the package in field. Many applications, such as a board-level module installed in a satellite or space vehicle, are not reachable for replacement or repair. Thus, they are made to last even in the most adverse conditions.

A variety of new materials and processes are coming into the market. For next-generation hermetic sealing applications, for example, a range of innovative cover lids are now available. These include hermetic covers or Visi-Lids for optical communications, non-magnetic Combo Lids for electromagnetic nose controls, and Getter Combo Lids to contain the release of hydrogen from the package.

No	Reliability Tests	Purpose
1	Gross leak test or die penetrate test	Hermeticity, identify leaks
2	Fine leak test (with helium bombing)	Hermeticity, identify leaks
3	Optical leak test	Hermeticity, identify leaks (mass scale)
4	Krypton leak test	Hermeticity, Identify leaks (quicker than helium)
5	Electrical test	Assembled unit performance
6	Temperature cycle test	Accelerated test for field performance
7	X-ray imaging	Solder joint integrity
8	Salt Atmospheric Test (SAT)	Accelerated test for field performance
9	PIND Test	Sealed unit internal particle identification
10	Visual inspection	Visual assurance of sealed unit, solder flow, etc.

➤ Various reliability tests.

Boosting performance with the merged *p-i-n* SiC Schottky diode

Delivering greater reliability at high efficiency, the merged *p-i-n* SiC Schottky diode combines a low forward voltage with high surge-current capability

BY LLEW VAUGHAN-EDMUNDS FROM NAVITAS SEMICONDUCTOR

THE WIDE-BANDGAP REVOLUTION in power conversion is well under way. To fulfil efficiency and power density targets in energy-conscious applications, designers are now rejecting silicon devices in favour of alternatives delivering superior performance.

Offering the greatest commercially maturity within the wide bandgap fraternity is SiC. Producers of this class of semiconductor have now released several generations of diodes and power MOSFETs, each offering successively improved performance. Sales of these devices have soared in recent times to hit nearly $3 billion last year, and growth is forecast to continue at around 40 percent per year as deployment expands into evermore applications.

SiC devices outperform their silicon counterparts in both conduction and switching characteristics. First to market within this family of power devices is the SiC Schottky barrier diode. Compared with the silicon fast-recovery diode, it has a lower forward voltage and a superior reverse recovery. One upshot of these strengths is a tremendous reduction in overall energy losses. Yet another merit of the SiC

Schottky barrier diode is a stable reverse-recovery time over the full operating temperature range. In comparison, the silicon fast-recovery diode is impaired by an lengthening recovery time at higher temperatures.

However, the SiC Schottky barrier diode is far from perfect. All Schottky diodes, regardless of material system, are inherently vulnerable to current surges. This is a known hazard in power-factor correction circuits, used in power supplies for converters and inverter systems.

One option for addressing this issue is to turn to *p-i-n* diodes, which offer greater reliability in such situations. However, reliability is traded for reduced efficiency, due to a higher forward voltage. It's not a great compromise, as a lower energy efficiency is undesirable. In equipment such as server power supplies, a diminished efficiency leads to a higher electricity bill, increased cooling management and a slower return on investment.

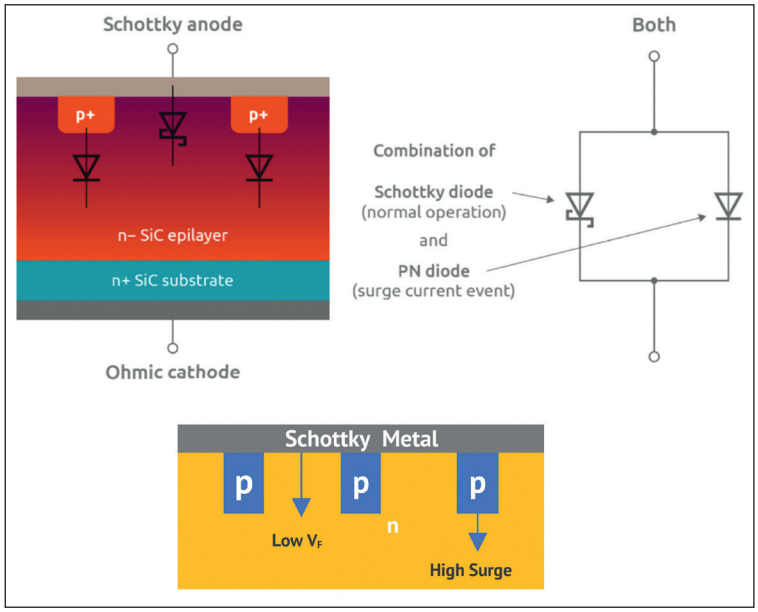
A compelling solution is the merged *p-i-n* SiC Schottky (MPS) diode. This device marries the best features of Schottky and *p-i-n* diodes in a single device by combining the surge-current robustness and low reverse leakage of the *p-i-n* diode with the low forward voltage of the Schottky structure. Equipped with a superior breakdown voltage, excellent reverse-recovery characteristics, stability over temperature, and the high-temperature operating capability associated with all SiC devices, the MPS diodes that have been introduced in power factor correction and boost circuits are enhancing reliability and significantly increasing the overall efficiency of the power-conversion system.

Design and optimisation

A key difference between a conventional Schottky part of the device structure and the MPS diode is that the latter contains additional *p*-doped wells, implanted in the drift zone. These wells form a *p*-ohmic contact with the metal at the Schottky anode, while also creating a *p-n* junction with the SiC drift layer. The result is effectively the combination of a Schottky diode and a *p-i-n* diode, connected in parallel (see Figure 1).

With this design, in normal operation the Schottky carries almost the entire current. On the other hand, during high-current surges, the voltage across the MPS device rises, causing conduction in the drift layer of the *p-i-n* diode. As this intrinsic diode has a lower resistance than the Schottky, current is diverted, reducing dissipation and relieving thermal stress.

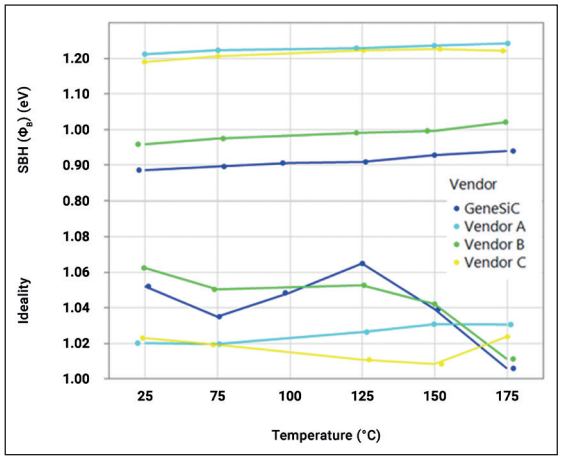
When the MPS diode operates under reverse bias, the maximum field strength occurs across its drift region. This contrasts with the situation in a standard Schottky architecture, where the greatest field strength occurs at the metal barrier. A downside of the Schottky diode is that imperfections in the barrier allow a relatively large leakage current to flow. That's not the case with the MPS diode, which benefits from moving the maximum field strength away from the metal barrier. This design ensures that the leakage is lower than that of a standard SiC Schottky diode.



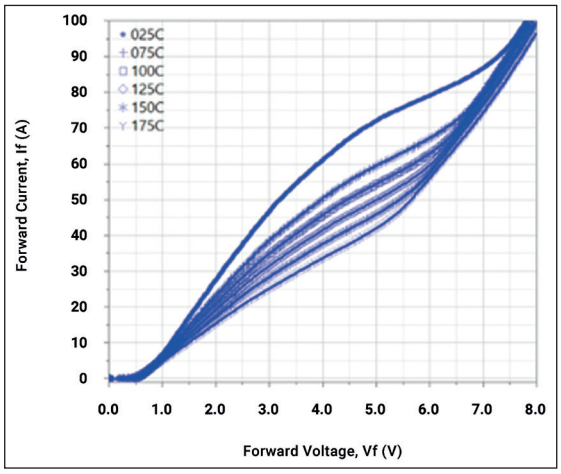
➤ Figure 1. MPS diodes combine *p-i-n* and Schottky diode attributes.

By optimising the dimensions and doping of the *p*-type wells, device designers can engineer the forward voltage drop, surge-current capability and leakage current of the MPS diode to meet specific requirements. Additional improvement comes from thinning the substrate below the drift region. This trims the MPS forward voltage and the thermal resistance between the Schottky area and back-side metallisation, leading to lower energy losses, enhanced thermal efficiency and greater reliability.

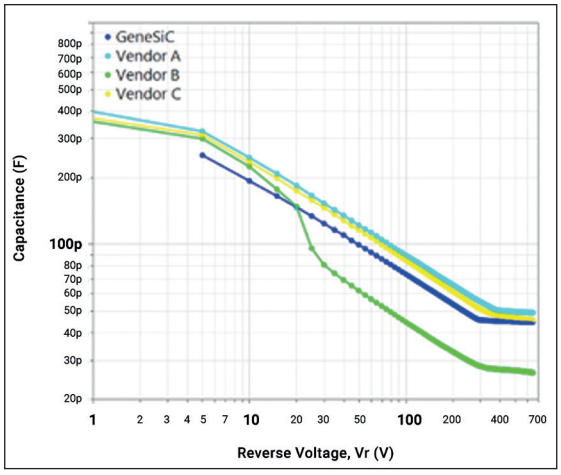
At Navitas, we have an enviable track record in developing and producing SiC MPS diodes. Now in their fifth generation, our 650 V SiC MPS diodes feature a high surge-current capability and a low forward voltage to minimise losses in the forward-biased mode. Our devices also offer an extremely low reverse-leakage current and high avalanche



➤ Figure 2. Low-current, forward current-voltage (I-V) characteristics for 10 A SiC MPS diode.



➤ Figure 3. High-current, forward current-voltage (I-V) characteristics from 25 °C to 175 °C.



➤ Figure 4. Capacitance-voltage (C-V) curves for Navitas and competitor SiC MPS diodes.

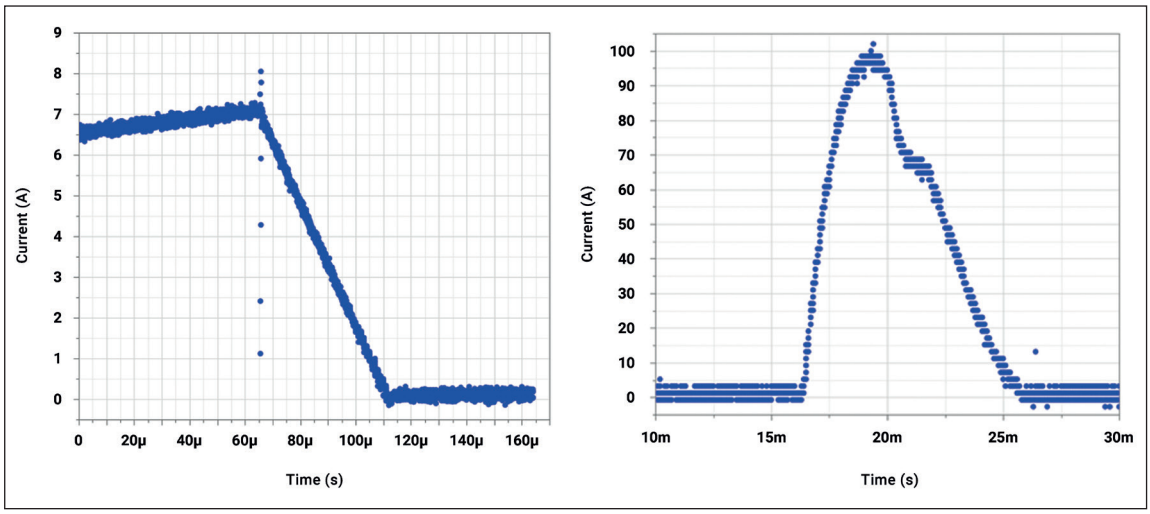
robustness. It is a combination of attributes that comes from optimising the device architecture and engineering the barrier metallurgy to ensure an ultra-low Schottky barrier height of just 0.88 eV at 25 °C.

One of the downsides of typical Schottky and MPS diodes, which feature a titanium metal barrier, is a trade-off between the Schottky barrier height and the reverse leakage current. Thanks to our novel, proprietary barrier metal, our MPS SiC diodes have a Schottky barrier height that's more than 26 percent lower than alternative titanium-barrier devices, and a leakage current of just 100 nA – that is at least six times lower than the norm. In addition, our devices offer enhanced shielding of the Schottky metal interface, minimising any increase in reverse leakage current at higher voltages.

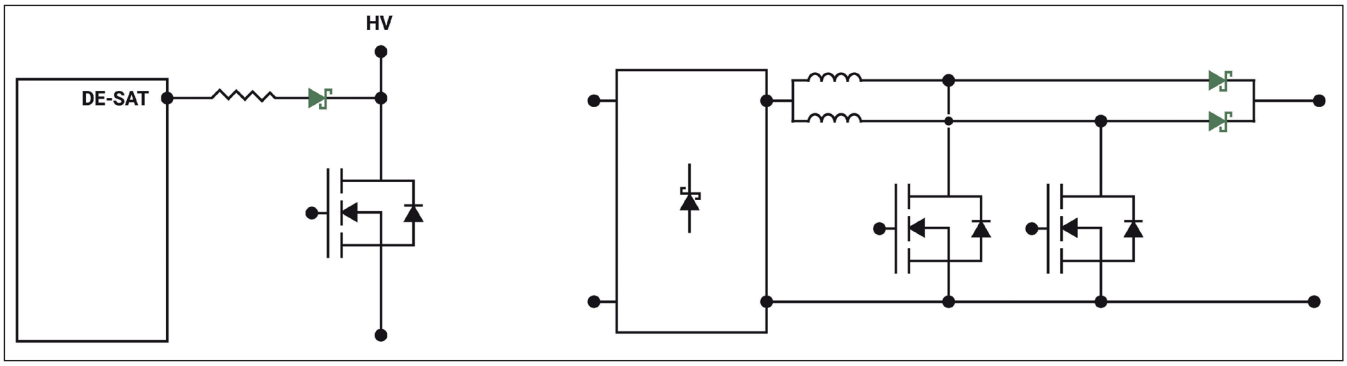
We have measured the forward current-voltage characteristics of these diodes at low currents and at temperatures from 25 °C to 175 °C (see Figure 2). These results reveal consistent linearity across this wide temperature range, indicating a stable Schottky barrier height, indicative of a good spatial homogeneity of the Schottky metal interface.

There is a small increase in the Schottky barrier height. That's a common tendency amongst MPS diodes from various vendors. One way to evaluate this increase is to consider 'ideality', a measure of how closely the diode's behaviour conforms to the ideal diode equation under different conditions. Ideality typically decreases with temperature, and has a value that's close to 1 in well-behaved diodes under normal conditions. If there are deviations from this value, they tend to come from unwanted effects, such as recombination currents and parasitic series resistances. Note that real-world diodes can depart from ideal behaviour, and often display an ideality greater than 1.

We have also recorded the current-voltage characteristics of our MPS diodes at higher currents (see Figure 3). These plots, taken at various



➤ Figure 5. (a) Avalanche testing and (b) surge current characteristics of Navitas MPD diodes.



temperatures, show that there is a cross-over from unipolar (SiC Schottky) to bipolar (*p-i-n*) operation at about 90 A at 25 °C. This cross-over decreases to 50 A at 150 °C. Our plots also show a lowering of the knee-voltage at higher temperatures, which helps maintain a low temperature co-efficient of the on-state voltage drop at the rated current of 10 A.

To benchmark our devices, we have compared the capacitance-voltage curves of our diodes with those of rival products. These plots reveal that our MPS diode has one of the lowest values of capacitance charge, which ensures low reverse-recovery losses.

The low capacitance charge also enables our MPS diodes to have a good value for the common figure-of-merit for this device, defined as the product of capacitance charge and forward voltage. While improvement on one of these fronts tends to be detrimental to the other, a good figure of merit balances a low forward-voltage drop, key to trimming power losses, with a low capacitance charge that ensures superior switching performance. Attaining the lowest possible value for each helps to enhance the overall diode performance in power electronics applications.

Another important characteristic for the MPS diode is its level of avalanche robustness. We assess this with unclamped inductive switching tests. Values for the current waveform under unclamped inductive switching and current-surge conditions reveal a high value for the non-repetitive surge current, confirming our diode's robustness (see Figure 5).

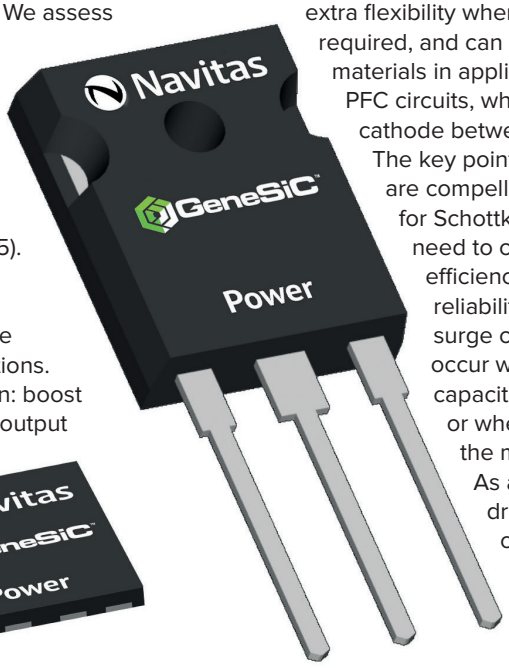
Made for TV

Our MPS diodes can make a positive contribution to a number of applications. They offer a superior performance in: boost circuits, which raise the solar-panel output voltage to the 450-600 V required for the inverter; and in power-factor correction circuits, which are mandatory in line-powered applications above 75 W, according to IEC/EN 61000-3-2. Power-factor correction circuits are used in power supplies for telecom equipment, for data centre servers and for lighting systems.

SiC MPS diodes can also deliver benefits in consumer devices, such as televisions. With the advent of 4K UHD, the latest displays are demanding significantly more power than their predecessors, leading to a greater emphasis on efficiency, for both realising a suitable energy rating and for maintaining proper performance. As well as satisfying this requirement, efficient power supplies usually improve the performance of the display. Often the power supply is positioned directly behind the display, and if it generates too much heat due to a low efficiency, this impairs colour rendition.

We offer our SiC MPS diodes in various package options, which can deliver several advantages in different applications. For high-voltage sensing circuits, like desaturation detectors for overcurrent protection, as well as in the gate-drive bootstrap circuits of high-side switches (see Figure 6), the DO-214 and TO-252-2 packages are ideal solutions.

On the other hand, the TO-247-3 package provides extra flexibility when high-power density is required, and can help reduce the bill of materials in applications like interleaved PFC circuits, which share a common cathode between two diodes.



The key point is that SiC MPS diodes are compelling direct replacements for Schottky diodes in circuits that need to combine a high energy efficiency with robustness and reliability when exposed to surge currents. Such conditions occur when powering highly capacitive or inductive loads, or when the power quality of the main AC line is poor.

As a straightforward drop-in replacement, our devices are easy to design-in for a significant boost in power-conversion efficiency.

➤ Figure 6. Navitas MPS diodes in a desaturation detection circuit and an interleaved power-factor correction (PFC) circuit.

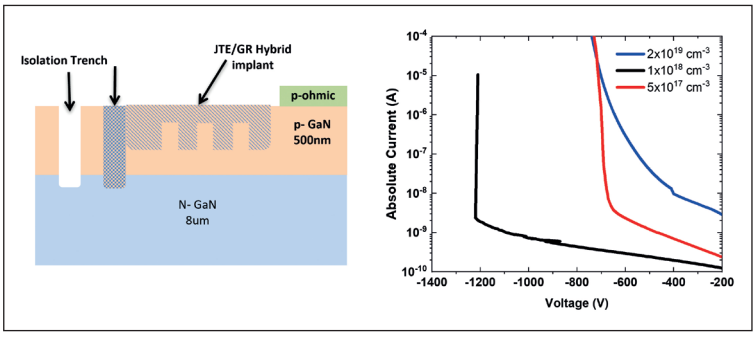
Advancing vertical GaN diodes

Optimising doping with a foundry-compatible process produces vertical *p-i-n* diodes with avalanche behaviour

THERE ARE MANY merits of vertical GaN *p-i-n* diodes grown on native substrates, including a simple architecture, low leakage and a high breakdown voltage.

While high-volume production of these devices is hampered by the absence of a foundry process, progress on this front is being made by a collaboration between Vanderbilt University, the Naval Postgraduate School, the Naval Research Laboratory and Sandia National Laboratory. This US team is pursuing a foundry-compatible planar process that controls the electric field and prevents current crowding by managing the dose in the anode extension region. Building on previous work that reported how the dose depends on the thickness of the anode, they are now unveiling the relationship between the dose and the anode doping level.

Commenting on their findings, Mona Ebrish from Vanderbilt University remarks: "The devices with a moderate anode doping have performed the best, and our TCAD simulation shed some light on the reasoning behind our experimental finding."



➤ The *p-i-n* diodes produced by the team (left) have breakdown characteristics that show a tremendous variation with doping level (right).

She believes that the approach they have adopted, involving a combination of experimental analysis and simulation, could be extended to other device designs.

A highlight of this study is that in one of the diodes the team recorded avalanche breakdown at different temperatures, a trait indicative of a non-destructive process.

The researchers also found that current increases as function of temperature, leading to a higher breakdown voltage. According to Ebrish, this behaviour suggests successful management of the electric field in the device, an asset not found in all *p-i-n* diodes: "Often devices either do not respond to the increase in temperature, or they experience a surge in current and burn – destructive breakdown."

The team produced their devices by loading non-homogenous GaN substrates into an MOCVD reactor and growing 500 nm-thick anode layers with magnesium doping levels of either 5 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3} or 2 x 10^{19} cm^{-3}. For all three samples, which have a 8 μm-thick lightly doped drift layer with a doping concentration of 1-2 x 10^{16} cm^{-3}, thermal annealing at 900 °C activated the anode dopants.

To form devices from the epiwafers, the team employed an edge-termination process that involved: etching a 1 μm-deep trench about 140 nm from the anode edge; applying a nitrogen implant with a box profile, using three different energies and a total depth of 650 nm; and using a nitrogen implant to define the junction termination extension and the guard rings (see figure for the architecture of the device). To completed the fabrication of the diode, the team added a Pd/Pt/Au stack for the *p*-GaN anode and a Ti/Al/Ni/Au stack for the cathode.

Electrical measurements on the three devices uncovered significant differences in breakdown voltage and leakage current, despite the identical drift layer thickness, doping level and edge termination process. The variant with anode doping of 1 x 10^{18} cm^{-3} exhibits a sharp breakdown at 1.2 kV, implying superior field management in the anode extension region. It is argued that the other two devices do not exhibit the same breakdown behaviour because the extension region is not fully depleted of charges, with the remaining charges to blame for premature breakdown.

The team also carried out avalanche tests, involving temperature-dependent reverse sweeps at 25 °C, 100 °C, 150 °C and 200 °C. They found that devices with doping levels of 5 x 10^{17} cm^{-3} and 2 x 10^{19} cm^{-3} struggled to avalanche, due to high leakage and an inconsistent trend with temperature, while the *p-i-n* diode with a doping of 1 x 10^{18} cm^{-3} avalanched, with an increasing breakdown voltage of 10 V for every 50 °C.

Ebrish says that further improvement to device performance could come from optimising the ion-implantation process.

"We are also evaluating the same process for GaN *p-i-n* diodes that are rated for higher voltages, like 3 kV or 6 kV."

REFERENCE
➤ M. Ebrish *et al.* Appl. Phys. Express. **16** 116501 (2023)

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