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ISSUE I 2026

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

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VIEWPOINT

BY PHIL ALSOP
EDITOR

AI – full speed ahead?

ANGEL BUSINESS COMMUNICATIONS' recent Data Centre Solutions Roadshow in Newcastle – the North East being one of the UK's designated AI Growth Zones (AIGZ) – provided some fascinating insights into how the data centre industry supply chain is attempting to come to terms with the ongoing AI explosion. Everyone in the room was confident that AI was set to have a massive impact on all aspects of our lives over the coming years (indeed, is already doing so); however, no one was able to say with any degree of confidence just what that impact would look like. Seems as if we are back to Donald Rumsfeld territory – with known knowns (not many of these!), known unknowns and, worst of all, unknown unknowns...

Perhaps the only certainty to emerge from the event was the insatiable demand for the power to drive the data centres, which in turn drive AI. A local power provider suggested that, while the current power capacity for his region was 6GW, if all of the planned data centres in the region were actually built, he would need to find somewhere between an extra 7-9GW of power to meet this demand. Mapped across the UK, there is very likely to be a shortfall when it comes to power capacity versus data centre capacity. One imagines that other many other countries are facing a similar challenge.

While the speed with which new energy resources are added to the grid was a major cause for concern, there's little doubt that the ongoing focus on energy efficiency at all stages of the power supply chain will continue to increase in importance – 'wasteful' power use is no longer an option.

The power electronics industry has, of course, already realized this truth and is busy innovating to develop ever more energy efficiency components and systems – the power not used is the 'greenest' power of all. For now, the data centre is very much the power electronics' industry sweetspot – something which will be reflected in our Power Electronics International Conference in Brussels at the end

of April. I'm very much looking forward to hearing about the many ways in which vendors are embedding energy efficiency at every level of their components, systems and devices to ensure that AI is delivered to the consumer as (energy-) efficiently as possible.

It will also be good to hear what's going on in the, not unrelated, renewable energy sector – green energy is pretty much table stakes for today's data centre operators; and to understand what's going on in the previously buoyant EV sector, with some mixed messaging as to the phasing out of diesel and petrol engines, along with the slower than anticipated acceptance of autonomous vehicles.

At the time of writing, the Middle East is, sadly, once again, witnessing a major conflict – adding a further layer of uncertainty to the power electronics sector. The only silver lining being that, as oil and fuel prices climb, there should be a renewed emphasis on renewable energy resources.

Contents

14

NEWS

09

Editor
Phil Alsop
phil.alsop@angelbc.com

News Editor
Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Technology Editor
Rebecca Pool

Contributing Technical Editor
Richard Stevenson
richard.stevenson@angelbc.com
+44 (0)1923 690215

Sales & Marketing Manager
Shehzad Munshi
shehzad.munshi@angelbc.com
+44 (0)1923 690215

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Graphic Design & Multimedia Assistant
Harvey Watkins
harvey.watkins@angelbc.com

Sales and Product Manager
James Cheriton
james.cheriton@angelbc.com
+44 (0)2476 718970

Publisher
Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

CEO Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

CTO Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Power Electronics International Magazine is published six times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher.

Published by Angel Business Communications Ltd
6 Bow Court,
Fletchworth Gate,
Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com
W: angelbc.com

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Mitsubishi samples new SiC-MOSFET bare dies

Advanced trench technology dies reduce power loss by approximately 50 percent

MITSUBISHI Electric has announced that it will shortly start shipping samples of four new trench SiC-MOSFET bare dies designed for use in power electronics equipment, such as electric vehicle (EV) traction inverters, onboard chargers, and power supply systems for renewable energy sources including solar power.

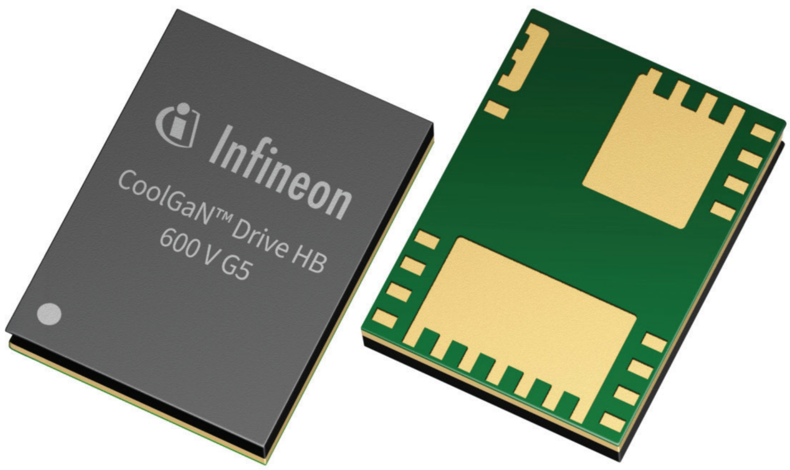
These new power semiconductor bare dies will contribute to efforts to embed advanced bare dies in various power electronics equipment to lower power consumption while maintaining performance, according to the company.

Mitsubishi Electric will exhibit the new trench SiC-MOSFET bare dies at the 40th Nepcon Japan R&D and Manufacturing show in Tokyo from January 21 to 23, as well as exhibitions in North America, Europe, China, India and elsewhere.

The four new trench SiC-MOSFET bare dies are similar to the company's existing trench SiC-MOSFET bare dies, but use a proprietary trench SiC-MOSFET structure to reduce power loss by approximately 50 percent compared to planar SiC-MOSFETs.

Furthermore, manufacturing processes including Mitsubishi Electric's proprietary gate oxide film manufacturing method suppress variations in power loss and on-resistance to ensure stable quality over a long period of use.

Infineon expands CoolGaN range with Drive HB family



INFINEON has expanded its CoolGaN portfolio with the CoolGaN Drive HB 600V G5 product family.

The four new devices – IGI60L1111B1M, IGI60L1414B1M, IGI60L2727B1M, and IGI60L5050B1M – integrate two 600V GaN switches in a half-bridge configuration together with integrated high- and low-side gate drivers and a bootstrap diode, delivering a compact, thermally optimised power stage that further reduces design complexity.

According to the company, by bringing key functions into one optimised package, the family lowers external component count, eases PCB layout challenges typically associated with fast-switching GaN and helps designers shorten development cycles while achieving the core advantages of GaN technology: higher switching frequencies, lower switching and conduction losses, and greater power density.

"GaN is transforming power conversion, and Infineon's mission is to maximise the transformation with scalable and easy-to-use solutions for customers," says Johannes Schoiswohl, head of GaN Business Line at Infineon. "With these new integrated solutions, we combine high-speed GaN performance with a level of integration and robustness that helps designers move faster, shrink their systems, and raise efficiency – pushing the boundaries of what's possible in compact power electronics."

Targeting low-power motor drive systems and switched-mode power supplies, the integrated half-bridge enables smaller magnetics and passive components, higher efficiency across operating conditions, and improved dynamic performance in space-constrained designs.

Engineered for high-speed precision, the device achieves ultra-fast switching with a 98 ns propagation delay and minimal mismatch, supporting efficient high-frequency operation while maintaining predictable timing behavior. For simplified system integration, it offers a PWM input compatible with standard logic levels and operates from a single 12 V gate driver supply, while fast UVLO recovery helps ensure robust behavior during start-up and transient supply events.

For superior thermal performance, the products are housed in a 6 x 8 mm^2 TFLGA-27 package with exposed pads, enabling efficient heat spreading and supporting heatsink-less designs in many applications.

Improving MBE for GaN power devices

Dividing the growth of a channel into a dozen layers boosts the blocking voltage of MBE-grown GaN HEMTs

A TEAM from China has strengthened the case for manufacturing GaN HEMTs by plasma-assisted MBE by producing simple devices that can block more than 2.5 kV.

While MOCVD dominates the manufacture of GaN HEMTs for power electronics, there are a number of benefits associated with plasma-assisted MBE.

One of the strengths of this class of epitaxy is that it is capable of producing an insulating buffer without the need for doping. Avoiding doping is a significant asset, as it eliminates current collapse when switching GaN HEMTs between their on and off states.

Another advantage of plasma-assisted MBE is the suppression of background impurities and defects, thanks to growth under ultra-high vacuum.

Exploiting these assets, the team from Massphoton, Suzhou Powerhouse Electronics Technology, and Suzhou Institute of Nano-Tech and Nano-Bionics, have produced GaN HEMTs that feature a 70 nm-thick channel produced with a novel growth scheme.

To form this device, the team divides the growth of the channel into 12 layers and employs a gallium droplet depletion treatment. This approach is said to enhance the quality of the GaN channel, due to fewer defect states and a lower pore defect density.

Fabrication of the HEMTs began by loading a 3-inch sapphire substrate with a 2° off-cut into a plasma-assisted MBE chamber and depositing a 1000 nm-thick AlN buffer at 920°C, followed by growth of the 70 nm-thick GaN channel, two monolayers of AlN and a 28 nm-thick layer of Al0.22Ga0.78N, all at 815°C. After growing this III-N stack, the team added, in situ, a 10 nm-thick SiN passivation layer. In addition, the team produced a control device with a slightly thicker channel (see Figure for details).

Processing these epiwafers into devices began with the deposition of a 30 nm-thick SiN layer by low-pressure CVD, followed by nitrogen implantation to realise mesa isolation, and the addition and annealing of source and drain ohmic contacts. After the growth of a 150 nm-thick layer of SiN, gate windows with a recess depth of 120 nm were defined, to leave 30 nm of SiN as the gate insulator. Deposition of Ti/Al/Ti followed, creating a gate metal and field plate, prior to the addition of interconnects and deposition of a 2 μm-thick SiN top passivation layer.

Electrical measurements using the transmission line method determined a contact resistance of 3.6 Ω mm and a sheet resistance for the wafer of 491 Ω sq-1. Meanwhile, Hall measurements provided values for the two-dimensional electron gas density of 1.07 x 1013 cm-2 and the field-effect mobility of 884 cm2 V-1 s-1, suggesting a sheet resistance of 660 Ω sq-1. The engineers attribute a discrepancy between values for sheet resistance obtained from different measurements to a buffer layer below the GaN channel that's not sufficiently insulating and leads to parasitic conduction.

It's claimed that improving the growth conditions of the buffer layer would reduce the sheet resistance and enable a thicker channel layer.

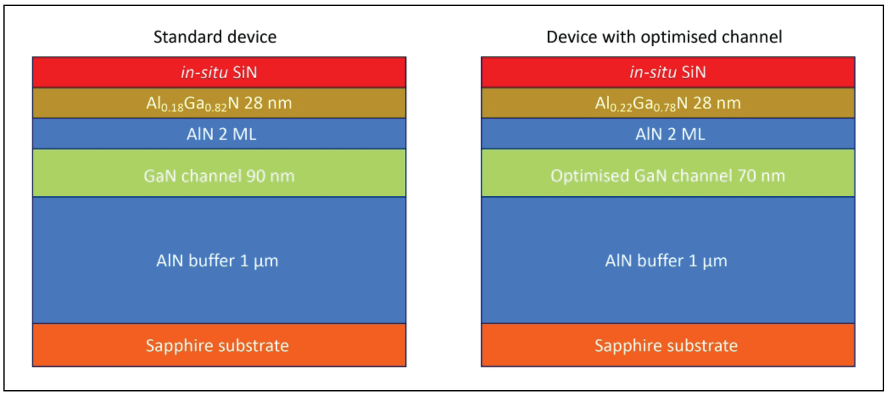
Transfer measurements of the GaN HEMT featuring modified channel growth show current saturation in the output characteristics. This characteristic, not observed in a control device with a conventional channel, is attributed to the superior channel produced with subdivided layers.

Additional benefits associated with the superior channel include an increase in the on-off ratio to 107 and a reduction in the drain leakage current at a drain bias of 0.5 V to 1 nA mm-1 – in both cases, there is an order-of magnitude improvement over the HEMT with the conventional channel.

Both forms of HEMT have a relatively high on-resistance, due to the thin GaN channel thickness.

According to the team, increasing the channel thickness will help to reduce the on-resistance, which can also fall by introducing a graded layer and improving the growth process.

The control device breaks down at 1000 V, while the HEMT with the superior channel can withstand around 2500 V. The team speculates that the far higher value stems from the superior insulating properties of the GaN channel.



A superior channel improves the HEMT's blocking voltage, leakage current and on-off ratio.

VIS signs GaN licensing agreement with TSMC

Taiwanese foundry first to offer dual-substrate GaN solutions across high- and low voltage

TAIWANESE FOUNDRY Vanguard International Semiconductor (VIS) has signed a technology licensing agreement with TSMC for high-voltage (650V) and low-voltage (80V) GaN technologies.

Through this licensing agreement, VIS will expand its GaN-on-Si technology into high-voltage applications and offer a comprehensive GaN-on-Si platform for power applications. Combined with its existing GaN-on-QST technology platform, VIS will become the only foundry in the world capable of offering power GaN technologies on both silicon and QST substrates.

VIS will support complete product solutions covering low voltage (<200V), high voltage (650V) and ultra-high voltage (1200V), further strengthening its technology roadmap for high-efficiency power conversion.

The aim is to accelerate the development and expansion of next-generation GaN power technologies for applications such as data centres, automotive electronics, industrial control, and energy management, which are key areas that demand high-efficiency power conversion.

The technology will be validated on VIS' mature 8-inch manufacturing line to ensure process stability and high yield. Development activities are expected to commence in early 2026, with production scheduled for the first half of 2028.

"This technology licensing agreement not only underscores the engagement and ongoing collaborative efforts between VIS and TSMC, but also represents our continued commitment to advancing a comprehensive power GaN product portfolio and strengthening our strategic position in compound semiconductors," said John Wei, President of VIS.

"Through this collaboration, we will accelerate our support for customers in high-performance power conversion applications, enabling the semiconductor power technology to move into the next generation and helping realise a future of green energy and intelligent technologies."

Toyota picks Infineon SiC chips for new SUV

INFINEON'S CoolSiC MOSFETs have been adopted in the new bZ4X model from Japanese car company Toyota.

Integrated into the on-board charger (OBC) and DC/DC converter, the SiC MOSFETs leverage the material's advantages of low losses, high thermal resistance, and high voltage capability to help extend driving range and reduce charging time.

"We are very proud that Toyota, one of the world's largest automakers, has chosen Infineon's CoolSiC technology. SiC enhances the range, efficiency and performance of electric vehicles and is therefore a very important part of the future of mobility." said Peter Schaefer, executive VP and chief sales officer automotive at Infineon.

Infineon says its CoolSiC MOSFETs feature a trench gate structure that reduces normalised on-resistance and chip size, enabling reductions in both conduction and switching losses to contribute to higher efficiency in automotive power systems.

In addition, optimised parasitic capacitance and gate threshold voltage enable unipolar gate drive, contributing to simplification of drive circuits for automotive electric drive train and supporting high-density, high-reliability design for OBC and DC/DC converters.

EPC releases GaN-based design for robot joints

BLDC motor drive inverter board features highly integrated 3-phase ePower Stage module

The EPC91122 highlights how GaN-based power stages enable unprecedented integration and power density in humanoid robotics," said Marco Palma, director, Motor Drives Systems and Applications at EPC

EFFICIENT POWER CONVERSION (EPC) has released the EPC91122, a 3-phase BLDC motor drive inverter evaluation board engineered for humanoid robot joint applications.

Featuring EPC's highly integrated EPC33110 3-phase ePower Stage module, the EPC91122 delivers up to 20 ARMS (28 Apeak) phase current in an ultra-compact form factor optimised for space-constrained robotic joints, integrating all key functions of a complete motor drive inverter, including a microcontroller, motor shaft angular sensor, housekeeping power supplies, accurate voltage and current sense.

"The EPC91122 highlights how GaN-based power stages enable unprecedented integration and power density in humanoid robotics," said Marco Palma, director, Motor Drives Systems and Applications at EPC.

The EPC91122 is mechanically optimised to fit directly inside humanoid joint motors. The complete GaN inverter occupies a 32 mm diameter inner circle, surrounded by a 55 mm external frame that supports mechanical mounting and lab connectivity. This design lets the inverter fit inside the motor chassis, which lowers loop inductance and makes the power density and dynamic performance higher.

The EPC33110 is the main part of the system. It is a three-phase co-packaged module with a maximum voltage of 100 V. It has three monolithic GaN half-bridges with built-in gate drivers, bootstrap circuits, and level shifters. The device has an RDS(on) of 11.7 + 13 mΩ and can switch at frequencies of up to 150 kHz, which means it may use smaller passive components and respond quickly to changes.

The board operates from a wide input range, making it well-suited for battery-powered robotic systems. It integrates all critical subsystems required for a complete motor drive inverter, according to EPC.

The EPC91122 comes preprogrammed to operate at 100 kHz PWM with 50 ns dead time, showcasing the high-speed switching capability enabled by GaN technology. Thermal testing under real-world operating conditions confirms the board's capability for continuous and pulsed operation.

As well as humanoid robot joints, the EPC91122 is suitable for compact servo drives, robotics, drones, and eMobility platforms. Complete design support files, including schematic, bill of materials (BOM), and Gerber files, are available.

EPC announces GaN licensing deal with Renesas

Licensing and second sourcing agreement adds low-voltage eGaN technology to Renesas portfolio

EFFICIENT POWER CONVERSION (EPC) has announced a licensing agreement with Renesas Electronics under which Renesas will gain access to EPC's low-voltage eGaN technology and its established supply-chain ecosystem.

EPC and Renesas will collaborate over the next year to establish internal wafer fabrication capabilities for these products. In addition, Renesas will second-source several of EPC's popular GaN devices that are already in mass production, enhancing supply-chain resilience for customers.

"Together, EPC and Renesas are forming a global alliance to deliver state-of-the-art power efficiency - cutting costs in AI data centres and enhancing autonomous systems. This is an exciting moment for our industry and our company," said Alex Lidow, CEO of EPC.

Renesas' GaN technology targets applications such as AC-DC power supplies, EV chargers, solar inverters, and industrial motor drives .It recently completed its acquisition of Transphorm to strengthen its high-voltage GaN portfolio.

The addition of EPC's low-voltage eGaN expertise now allows Renesas to offer a GaN power portfolios that spans low- to high-voltage applications.

"Expanding our business into low voltage GaN allows us to serve the fastest growing power segments," said Rohan Samsi, VP, GaN business division at Renesas. "This agreement with EPC complements our established high-voltage 650V+ portfolio and enables us to capitalise on high-volume markets such as AI power architectures from 48V down to 12V and 1V, as well as client computing and battery-operated applications."

Vishay adds 1200V SiC MOSFET modules in SOT-227

VISHAY has introduced five new 1200 V MOSFET power modules designed to increase power efficiency for medium to high frequency applications in automotive, energy, industrial, and telecom systems.

The VS-SF50LA120, VS-SF50SA120, VS-SF100SA120, VS-SF150SA120, and VS-SF200SA120 feature Vishay's latest generation SiC MOSFETs in the industry-standard SOT-227 package.

Offered in single switch and low side chopper configurations, each power module features a SiC MOSFET integrated with a soft body diode offering low reverse recovery. The result is reduced switching losses and increased efficiency for solar inverters; off-board chargers for electric vehicles (EV); SMPS, DC/DC converters, UPS, and HVAC systems; large scale battery storage systems; and telecom power supplies.

The compact SOT-227 package allows the devices to serve as drop-in replacements for competing solutions in existing designs, enabling designers to adopt one of the newest SiC technologies without the expense of changing PCB layouts. The moulded package offers electrical insulation up to 2500 V for one minute, lowering costs by eliminating the need for additional insulation between the component and heatsink.

The power modules provide continuous drain current from 50 A to 200 A and low on-resistance down to 12.1 mΩ. The RoHS-compliant devices deliver high speed switching with low capacitance and offer a high maximum operating junction temperature of +175 °C.

Samples and production quantities of the VS-SF50LA120, VS-SF50SA120, VS-SF100SA120, VS-SF150SA120, and VS-SF200SA120 are available now, with lead times of 13 weeks.

Rohm adds smaller package to 40V/60V MOSFET line

4.9mm × 6.0mm HPLF5060 package offers smaller footprint for automotive applications

ROHM has expanded its lineup of low-voltage (40V/60V) MOSFETs for automotive applications – such as main inverter control circuits, electric pumps, and LED headlights – by introducing latest products adopting the new HPLF5060 package (4.9mm × 6.0mm).

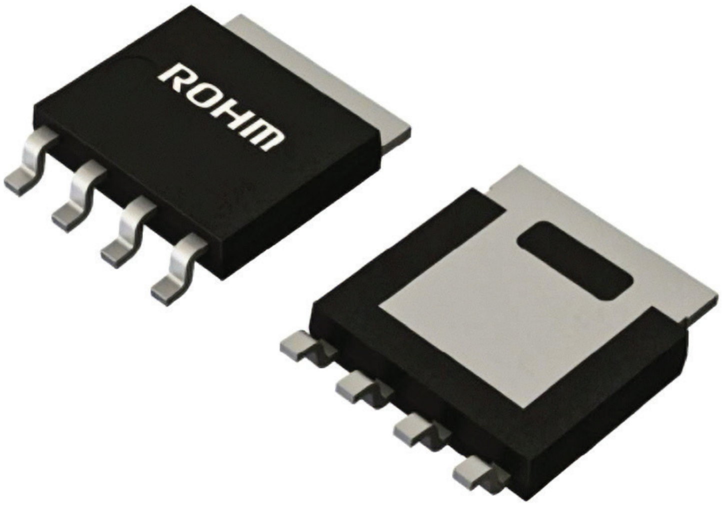
In recent years, automotive low-voltage MOSFETs have been trending toward smaller packages, such as the 5060-size and even more compact options. However, this miniaturisation introduces significant challenges for achieving reliable mounting, primarily due to narrow terminal spacing and leadless designs.

To address these issues, the new HPLF5060 package offers a smaller footprint compared to the widely used TO-252 package (6.6mm × 10.0mm) while enhancing board-mount reliability through the adoption of gull-wing leads. Additionally, the use of copper clip junction technology enables high-current operation, making the HPLF5060 an ideal solution for demanding automotive environments.

Mass production of new products using this package began in November 2025 (sample price: $3.5/unit, excluding tax). Online sales have also started, and the products is also available for online purchase through online distributors such as DigiKey and Farnell.

In addition to expanding the lineup of products using this package, mass production of the smaller DFN3333 (3.3mm × 3.3mm) package, which employs wettable flank technology, is scheduled to begin around February 2026.

Furthermore, development has commenced on a TOLG (TO-Leaded with Gull-wing) package (9.9mm × 11.7mm) to further expand the lineup of high-power, high-reliability packages.



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Key Themes for 2026

Putting the Automotive Industry in Pole Position

What are the most effective ways to improve reliability, efficiency, and fast-charging for electric vehicles while managing thermal and wide bandgap challenges?

Ensuring a Renewable, Sustainable Future

Can greater efficiency in power conversion and better integration of renewables lead to a more stable and low-carbon energy grid?

Delivering AI-driven Data Centre Densification

What solutions will deliver reliable, high-density power for AI data centres as space and thermal demands grow?

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ANGEL EVENTS

New materials could boost the energy efficiency of microelectronics

By stacking multiple active components based on new materials on the back end of a computer chip, this new approach reduces the amount of energy wasted during computation

BY ADAM ZEWE, MIT NEWS OFFICE.

MIT RESEARCHERS have developed a new fabrication method that could enable the production of more energy efficient electronics by stacking multiple functional components on top of one existing circuit.

In traditional circuits, logic devices that perform computation, like transistors, and memory devices that store data are built as separate components, forcing data to travel back and forth between them, which wastes energy.

This new electronics integration platform allows scientists to fabricate transistors and memory devices in one compact stack on a semiconductor chip.

This eliminates much of that wasted energy while boosting the speed of computation.

Key to this advance is a newly developed material with unique properties and a more precise fabrication approach that reduces the number of defects in the material. This allows the researchers to make extremely tiny transistors with built-in memory that can perform faster than state-of-the-art devices while consuming less electricity than similar transistors.

By improving the energy efficiency of electronic devices, this new approach could help reduce the burgeoning electricity consumption of computation, especially for demanding applications like generative AI, deep learning, and computer vision tasks.

"We have to minimize the amount of energy we use for AI and other data-centric computation in the future because it is simply not sustainable. We will need new technology like this integration platform to continue that progress," says Yanjie Shao, an MIT postdoc and lead author of two papers on these new transistors.

The new technique is described in two papers (one invited) that were presented at the IEEE International Electron Devices Meeting. Shao is joined on the papers by senior authors Jesús del Alamo, the Donner Professor of Engineering in the MIT Department of Electrical Engineering and Computer Science (EECS); Dimitri Antoniadis, the Ray and Maria Stata Professor of Electrical Engineering and Computer Science at MIT; as well as others at MIT, the University of Waterloo, and Samsung Electronics.

Flipping the problem

Standard CMOS (complementary metal-oxide semiconductor) chips traditionally have a front end, where the active components like transistors and capacitors are fabricated, and a back end that includes wires called interconnects and other metal bonds that connect components of the chip.

But some energy is lost when data travel between these bonds, and slight misalignments can hamper performance. Stacking active components would reduce the distance data must travel and improve a chip's energy efficiency.

Typically, it is difficult to stack silicon transistors on a CMOS chip because the high temperature required to fabricate additional devices on the front end would destroy the existing transistors underneath.

The MIT researchers turned this problem on its head, developing an integration technique to stack active components on the back end of the chip instead.

"If we can use this back-end platform to put in additional active layers of transistors, not just interconnects, that would make the integration density of the chip much higher and improve its energy efficiency," Shao explains.

The researchers accomplished this using a new material, amorphous indium oxide, as the active channel layer of their back-end transistor. The active channel layer is where the transistor's essential functions take place.

Due to the unique properties of indium oxide, they can "grow" an extremely thin layer of this material at a temperature of only about 150 degrees Celsius on the back end of an existing circuit without damaging the device on the front end.

Perfecting the process

They carefully optimized the fabrication process, which minimizes the number of defects in a layer of indium oxide material that is only about 2 nanometers thick.

A few defects, known as oxygen vacancies, are necessary for the transistor to switch on, but with too many defects it won't work properly.

This optimized fabrication process allows the researchers to produce an extremely tiny transistor that operates rapidly and cleanly, eliminating much of the additional energy required to switch a transistor between off and on.

Building on this approach, they also fabricated back-end transistors with integrated memory that are only about 20 nanometers in size. To do this, they added a layer of material called ferroelectric hafnium-zirconium-oxide as the memory component.

These compact memory transistors demonstrated switching speeds of only 10 nanoseconds, hitting the limit of the team's measurement instruments. This switching also requires much lower voltage than similar devices, reducing electricity consumption.

And because the memory transistors are so tiny, the researchers can use them as a platform to study the fundamental physics of individual units of ferroelectric hafnium-zirconium-oxide.

"If we can better understand the physics, we can use this material for many new applications. The energy it uses is very minimal, and it gives us a lot of flexibility in how we can design devices. It really could open up many new avenues for the future," Shao says.

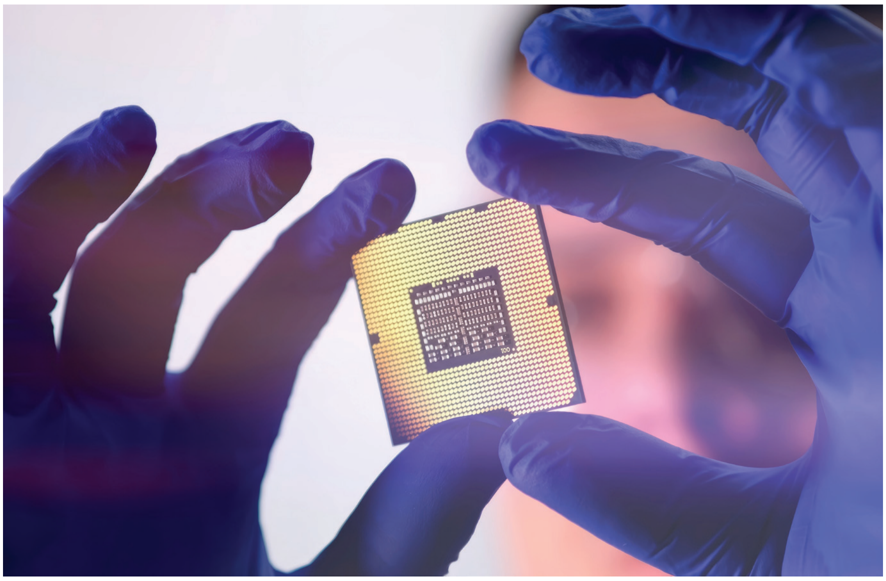
The researchers also worked with a team at the University of Waterloo to develop a model of the performance of the back-end transistors, which is an important step before the devices can be integrated into larger circuits and electronic systems.

This optimized fabrication process allows the researchers to produce an extremely tiny transistor that operates rapidly and cleanly, eliminating much of the additional energy required to switch a transistor between off and on

In the future, they want to build upon these demonstrations by integrating back-end memory transistors onto a single circuit. They also want to enhance the performance of the transistors and study how to more finely control the properties of ferroelectric hafnium-zirconium-oxide.

"Now, we can build a platform of versatile electronics on the back end of a chip that enable us to achieve high energy efficiency and many different functionalities in very small devices. We have a good device architecture and material to work with, but we need to keep innovating to uncover the ultimate performance limits," Shao says.

This work is supported, in part, by Semiconductor Research Corporation (SRC) and Intel. Fabrication was carried out at the MIT Microsystems Technology Laboratories and MIT.nano facilities.



AONDevices: Listening without limits

Ultra-low-power edge AI processors and algorithms from AONDevices are set to banish the power limits holding back always-on sensors in wearables and IoT.

BY REBECCA POOL, TECHNOLOGY EDITOR

FOR YEARS, always-on sensing has been held back by power budgets. Continuously monitoring surroundings for voice, sound and motion demands persistent processing that can quickly drain batteries, leaving designers treading a fine line between device responsiveness, feature sets and battery life. However, a raft of recent partnerships from California-based AONDevices, which has developed ultra-low-power edge AI processors and algorithms for always-on voice and sensor fusion applications, suggests these limitations are beginning to ease.

At this year's CES, AONDevices and three partners - P-logic, Realtek and TDK - demonstrated how ultra-low-power edge AI can enable devices to continuously listen, sense, and respond, without sacrificing battery life. AONDevices integrated one of its processors **into** an always-on sensor tag from edge-AI device designer P-Logic, **reporting battery lifetimes of several years from a single coin cell.** Edge AI was also integrated into a wearable safety device, demonstrating voice confirmation, acoustic event recognition and environmental hazard monitoring.

As Mouna Elkhatib, CEO and CTO of AONDevices, said: "Our focus is enabling meaningful intelligence under strict power limits. Running advanced machine learning features at super-low-power levels is what unlocks the next generation of smart wearables, tags, and safety devices. P-Logic's products show how powerful these capabilities become when integrated into real designs."

P-Logic's Beacon AI Tag is a compact, always-on sensing device designed to add acoustic, motion, and environmental intelligence to existing systems. [AONDevices]

AONDevices also combined its processor with Realtek's Bluetooth Low Energy chipset and software stack to showcase always-on, context-aware, smart remote controls. The company also demonstrated how its edge AI processor, integrated to TDK InvenSense's digital microphone, could enable always-on voice and sound detection.

"This is where our super-low-power edge AI architecture shines," said Elkhatib. "[Our processor] doesn't just run AI at ultra-low power – it manages the entire sensing pipeline. By controlling the microphone and system flow at the hardware level, we eliminate the traditional trade-off between low power and high accuracy."

Early days

Elkhatib co-founded AONDevices with Daniel Schoch and Adil Benyassine back in 2018 to provide low-power signal processing devices with integrated machine learning. With $2.6 million seed funds following over the next couple of years, all three founders were keen to develop robust, low-cost on-chip AI-based algorithms to give battery-powered devices always-on capability for listening and responding to voice and audio.

Elkhatib had already worked at Conexant, semiconductor provider of voice and audio processing chips. "I led most of the audio codecs in the industry here for laptops, PCs, smart speakers – all in the embedded space," she told Power Electronics International. Along the way, she was also system lead and architect for the voice and audio chipsets for the Galaxy S7 and later generation smartphones at US semiconductor firm, Qualcomm, and was instrumental in designing low power neuromorphic voice activation systems at AI computing firm, BrainChip.

"I started AONDevices with a view to enabling always-on with as many features as possible," she said. "From the beginning, our vision was to enable full sensor fusion in this [always-on] state, so not only voice and not only motion. We wanted to detect, for instance, an elderly person falling, a baby crying, someone calling for help at any time – use always-on [technology] to help human daily life."

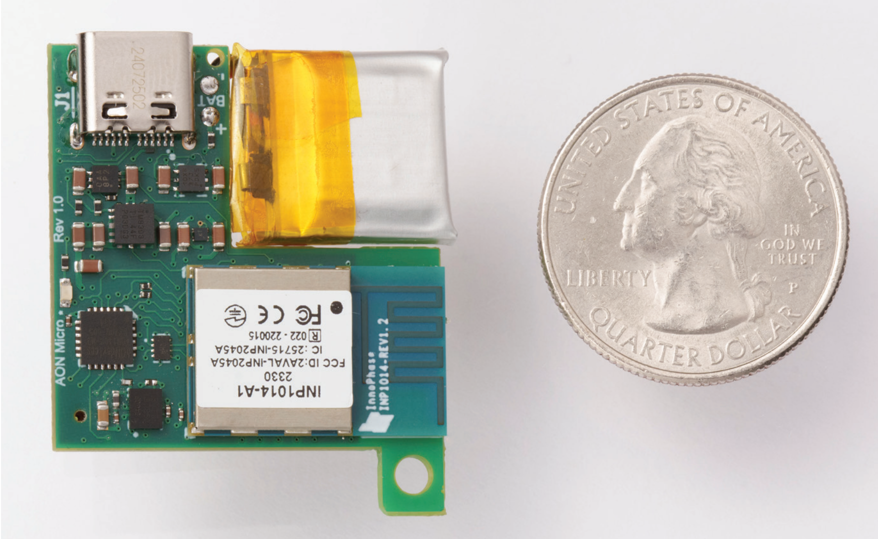
According to Elkhatib, processor development has been inspired by the human brain. "Think about it - we're always listening, our brains are always active in a lower power state, and wake up only when there is an interesting event to process," she said. With this in mind, she and colleagues designed the hardware, algorithms - deep learning neural networks for audio applications - and software all together, tailoring their developments for ultra-low-power systems.

"We didn't want to just build a chip and worry about algorithms, we co-designed the machine learning algorithms with the chip, software and entire system in mind," she said. "I don't believe in a generic machine learning chip that works for any AI workload, as that big chip will just [consume] too much power. Yet a tiny chip will not fit a programmer's machine learning models."

"So now we are seeing industry moving towards co-designing the machine learning models with the hardware," she added.

AI processors and more

To date, the company has released two ultra-low-power AI processors, with a third processor under development. The existing processors integrate custom-neural network cores into



Released in December 2024, the AONix Edge AI Sensor Module was developed in collaboration with P-Logic Consulting and features sensor integration from TDK InvenSense. [AONDevices]

40 nm ULP (Ultra-Low Power) silicon chips – silicon that is designed to minimize power consumption and leakage current for IoT, wearables and battery-powered applications. The processors contain dual neural processing units, a RISC-V core, and hardware DSPs tailored for on-device, always-on AI processing. Multi-sensor fusion supports myriad inputs, including microphones and accelerometers, so the processor can detect voice commands, gestures, and environmental sounds simultaneously.

"[In many applications] the focus has been on the voice, but we need to detect full motion; is a person running or sitting, are they snoring or laughing," said Elkhatib. "We want to detect all of these emotions with speech, motion – with everything. That is the only way to really recognise the true state of a system – which in this case is the human body."

Critically, each chip is designed to operate in the microwatt power range - consuming less than 260 µW during full processing and less than 80 µW in listening mode - enabling long battery life for IoT devices, wearables, and hearables. "When we present [our processors] to OEMs, we can say, for instance, this will support wake-word recognition, voice command, siren detection plus speaker identification - all of these features within the budget of a few hundred microwatts," said Elkhatib.

Elkhatib and AONDevices colleagues have also developed an online tool suite for creating, training and deploying machine learning models for edge AI devices. The platform enables data collection via, say microphones or accelerometers, and synthetic data augmentation so training can take place on small datasets - while traditional AI training typically requires extensive data collection, the platform generates accurate models with as few as 100 samples. Building lightweight machine learning models for the ultra-low-power silicon is part of the platform, as is performance testing to ensure models perform in the real world.

Elkhatib highlighted how her company's micro-machine learning models learned parameters, or weights, are less than

Mouna Elkhatib is CEO, CTO, and Co-Founder of AONDevices.

50 kilobytes – incredibly small, and suitable for on-device inference. "The AONDevices platform is optimised to guarantee small ML models without compromising on accuracy," she says. "So we end up with efficient deep learning for voice, sound, context, any type of pattern recognition, that is always running on super-low power."

But what about privacy? Always-on devices have raised significant privacy concerns because they constantly monitor their environment to detect user activity - yet Elkhatib is adamant this will not be the case for AONDevices' technology. "Some features in, say, a smart watch use an app to transmit data to the cloud," she said. "We don't want that and will reject those devices – and that's where our technology also comes into a big play."

Reaching markets

So with the tech developed and demonstrated, Elkhatib and AONDevices colleagues have their sights firmly fixed on markets. Market forecasts are solid: latest figures from The Business Research Company, forecast the event-driven audio edge chip market to grow from today's $2.06 billion to $4.06 billion in 2030, corresponding to 18.6% CAGR.

Meanwhile, for the global sensor fusion market, Roots Analysis predicts a 18.32% CAGR with the market reaching $55.69 billion by 2035. Fortune Business Insights forecasts the global wearable AI market to reach $359.32 billion by 2034 and a 24.7% CAGR over the forecast period.

AONDevices has worked with Taiwan-based ASIC design services and silicon IP provider, Faraday Technology, for several years, and in March 2025 announced plans to bolster production and ensure scalable manufacturing - positioning the company to capture a share of this growth with its AI processors. As the IC design partner of UMC (United Microelectronics Corporation), Faraday can offer priority access to advanced semiconductor manufacturing processes to help support reliable production amid fluctuating market conditions. "Faraday's experience and priority access to UMC's manufacturing capabilities provide us with the scalability and reliability necessary to meet the growing demand for our products," highlighted Elkhatib.

The latest partnerships with P-Logic, TDK InvenSense and Realtek are also clear signals that AONDevices is edging towards more and more commercial application. As Elkhatib put it: "Today we have wins in headsets and remote-control [devices], and we're moving into wearables – these are the low hanging fruits."

But as the CEO points out, the technology can apply to any always-on device. Pointing to TVs and kitchen appliances, she highlights how these devices in standby should consume very little power to meet EU energy label standards. "Large system-on-chips cannot run continuously on low power but [if the device also has] a chip like ours, it can," she said.

Why silicon still matters

Silicon IGBTs in the spotlight: Thomas Hauer, Avnet Silica, explains why the enduring workhorse of power electronics is here to stay

BY REBECCA POOL, TECHNOLOGY EDITOR

What applications are driving demand for silicon IGBTs right now?

Hauer: Both induction heating and heat pumps are the main drivers – and with heat pumps, it's getting interesting. Suppliers specify plus 20-year lifetimes, and with IGBTs, the [long-term] effects of switching on the motor winding to winding insulation are understood. But silicon carbide [devices] switch faster, and so the insulation is under much more stress. Many suppliers are left thinking, 'well, we cannot really [harness] the positive effects of silicon carbide because we need to make it switch slower, like the IGBT.' So why should they implement a more expensive silicon carbide MOSFET, which only makes life more complex, instead of just sticking with the silicon IGBT?

Where else might a supplier prefer silicon IGBTs over SiC MOSFETs?

Hauer: This is a little dependent on how the module is designed, but silicon is more resilient when it comes to short-circuit ruggedness and is usually more rugged in terms of overload capabilities – this is why the industrial motor inverter can be designed to last more than 20 years or so. I know there are all the bells and whistles and marketing going into wide bandgap semiconductors at the moment, but silicon still has its space, and it will stay there. I'm not going to advocate a customer towards silicon carbide, if they don't want this - if the application makes sense in silicon, why would you waste your time investigating wideband gap alternatives?

> Silicon is more resilient when it comes to short-circuit ruggedness and is usually more rugged in terms of overload capabilities

Are there applications where silicon persists despite expectations of a switch to SiC?

Hauer: Personally, for me, it's the industrial motor sector. We had a big, big push from customers who wanted silicon carbide, but then they faced obstacles, with the output filters, the pricing, the wiring and more. They finally decided, 'well, why should we do this?' Silicon carbide-based inverters are really good if you are integrating them on top of the motor, say, but in most industrial robots, the inverter sits close to fabrication, next to the robot arm – so we've seen customers trying to figure out if there are any benefits to silicon carbide here. I recently had a discussion with a customer that wanted a five-amp DIN-rail power supply, and they asked, 'why on Earth should I use a silicon carbide MOSFET that can do 50 amps for absolutely no reason?' I think customers are now well educated and understand what silicon carbide can bring and what it can't bring. Silicon has stayed [in this application], and will stay here way longer than I thought it would.

Have you seen customer requirements for IGBTs shifting in the last 12 to 24 months?

Hauer: On performance, customers are increasingly looking into topside cooling – this started with silicon carbide in automotive drives but now the first IGBT is also available for topside cooling. We need to see if this application properly materializes for IGBTs and I have not yet made up my mind if this actually provides any benefits to the design – but topside cooling is nice, once you find a way to [apply] it.

Are you seeing any concerns over security of supply?

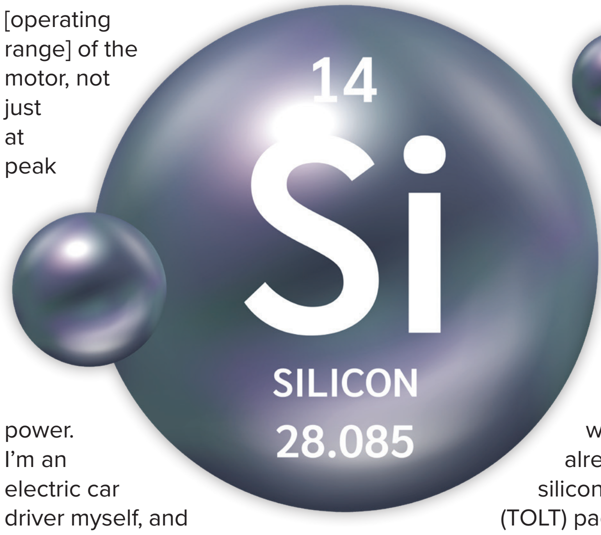
Hauer: Global politics are making customers nervous. As a distributor, we spent the last 15 years running around and asking customers to have a second supply source – many dropped this as it required a lot of effort in design, qualification and certification. Now, customers are very cautious. We have customers based in Europe and their customer base is European – while some are pushing purely for European suppliers, others want to have access to suppliers from other regions of the world but with a first, second, and even third source of supply.

What key hardware developments do you see taking place right now?

Hauer: A current trend in PV inverters is getting high input voltages and high input currents into bigger modules. The tricky thing here is that if you increase the input voltage, you also increase the link voltage, which means the B6 bridge output, [a three-phase inverter bridge with six switching devices], needs to run at lower duty cycles - so the losses you save at the input stage, you then gain on the output stage. In my point of view, this is the kind of thing that needs to be worked on.

Other hardware developments?

Hauer: In the four-wheel-drive of electric vehicles, we see silicon IGBTs being used in the boost motor [on the front axle] of these vehicles whilst silicon carbide MOSFETs are mostly used in the inverters on the rear [axle] inverter. Suppliers are now thinking of combining the silicon carbide MOSFETs and silicon IGBTs. It makes sense, because you want high efficiency from your automotive drive-train inverters across the entire [operating range] of the motor, not just at peak power. I'm an electric car driver myself, and use my first electric car as an example: peak power is 210 kW but average power consumption is roughly 19 kWh per 100 km. This means the inverter runs, on average, below 20 kW, and achieving high efficiency here is a big challenge for automotive OEMS. But you can use the silicon carbides for fast switching and then use the IGBTs for the heavy lifting - and the big advantage here is the IGBT is still cheaper than silicon carbide, which makes this a tempting 'thinking exercise' for lots of automotive customers. Still - there is a missing piece of the puzzle: IGBTs and SiC MOSFETs have very different gate drive conditions, and you cannot combine these two devices with simple gate drivers. And as I understand it, this gate driver problem isn't yet solved.



Where are opportunities for silicon in the coming years?

Hauer: Heat pumps are a steady business that's here to stay as we see this huge push to get away from gas and coal heating. In the DACH region [Germany, Austria, Switzerland] almost all of the newly built houses have heat pumps – so there is a huge business opportunity here. But I see opportunities everywhere where there is imminent price pressure and where efficiency is not the [metric] that is monitored the most – if you can spare, say, half a percent in efficiency then fine, go for the cheap option. One heat pump customer recently moved from wide bandgap semiconductors to silicon again, and then another customer decided to stay with IGBTs for their lower-end motor inverter.

Any silicon MOSFET innovations?

Hauer: Silicon MOSFETs are more about incremental innovation, and optimising certain figures of merit. I recently asked one supplier a semi-provocative question: you now have two by two millimetre MOSFETs, so when do we see one by one [devices]? This was a joke - two by two is already small. But we see silicon MOSFETs in top-cooling (TOLT) packages and also HiperFET Q3 package; the package variety in silicon MOSFET is enormously huge. The MOSFET market is under pressure because of global discounts, but silicon MOSFETs will continue to have their place in many applications where they are just good enough.

What about power management ICs?

Hauer: Last year, at ECCE Europe, a big discussion was the vertical integration of PMIC processors. Technically, it makes perfect sense – you need to have a stable voltage close to the processor. But thermally, it's a nightmare because on the bottom, the processor is producing losses and heat, and then you have the same again on the top - so cooling will be, for sure, a challenge. I do think that this is a problem that will be solved quite soon, because a lot of groups are working on this – but I'm interested to see how they will manage to solve this. When you look at the gigawatt hours of energy that run into a data centre - well that's a lot of cooling that needs to be applied.

What packaging innovations are you excited about?

Hauer: For discretes, I think the most famous package is the HU3PAK (made by ST Microelectronics). Development was triggered by Tesla, and the package was originally designed for 650 V silicon carbide devices in onboard charging - ST was the first to publicly release these devices to the market. Around 80% of the silicon carbide lines now have this package, but it's also being used for IGBTs. For power modules, injection-moulded dual-side [substrates] are interesting for IGBTs. So here, you basically have a sandwich construction, where the modules sit in between some aluminium blocks, through which cooling liquid flows.

What does the future hold for silicon devices?

Hauer: I see suppliers working on a new generation of IGBTs – and this is a good thing. Budgets are not as big as wide bandgap semiconductor budgets, but as long as suppliers continue to invest in a technology, that's a good sign. I had a conversation with an analyst about IGBTs about growth numbers, and while the figures for silicon carbide and gallium nitride are, of course, shiny, we see steady growth in IGBTs, and I don't think we will see this going away.

KEY TAKEAWAYS FROM THOMAS HAUER

- Silicon IGBTs remain relevant in applications requiring ruggedness, long life, and cost.
- SiC offers fast switching and efficiency gains but adds stress to motors and complexity in design.
- Silicon is being used with SiC packaging innovations, such as HU3PAK, to enhance thermal management.
- Hybrid designs (IGBT and SiC) are being explored but require advanced gate drive solutions.
- Heat pumps and industrial inverters represent steady growth opportunities for silicon devices.

The current status of 800V for EVs

THE TRANSITION to 800V EVs affects the entire powertrain, including the power electronics.

K automotive industry is increasingly adopting 800V platforms for battery electric vehicles (BEVs). While 400V systems will remain relevant in the coming decade, the performance and efficiency benefits of 800V architectures are compelling and, in most cases, justify the required powertrain re-engineering. John Li, a technology analyst at market intelligence firm IDTechEx, explains the advantages of 800V platforms and how the transition is being achieved.

The transition to 800V EVs is one which affects the whole powertrain, including the power electronics. In IDTechEx's report, Power Electronics for Electric Vehicles 2026-2036: Technologies, Markets, and Forecasts, these trends are analysed and used to forecast the adoption of wide bandgap semiconductors SiC and GaN, as well as the entire power electronics market for electric vehicles (EV).

800V is mature and proven

The automotive industry is converging on 800V platforms for battery electric vehicles (BEVs), when earlier generations of vehicle were 400V. While 400V will certainly have a part to play in the next decade, the advantages of 800V platforms are undeniable, and in most cases worth the re-engineering of the powertrain to accommodate this.

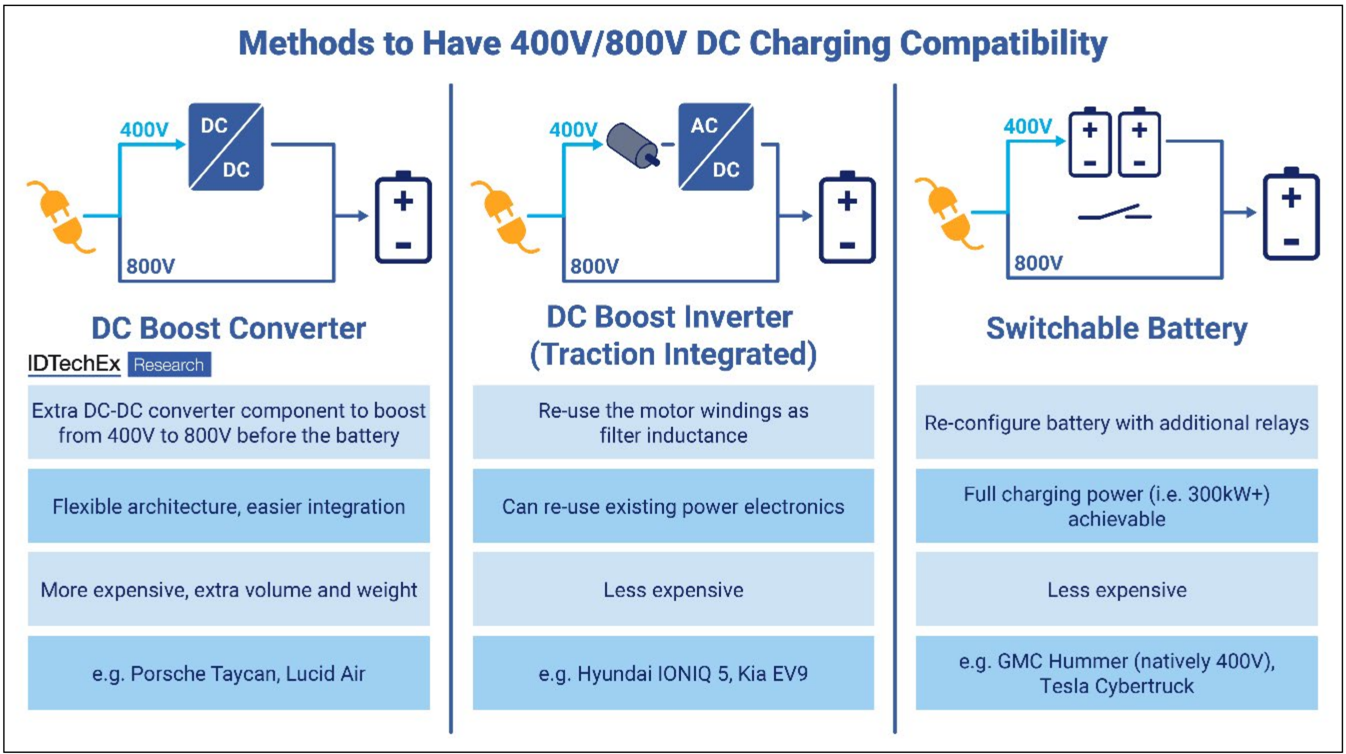
Firstly, the higher voltage means that the battery can charge at greater power while using less current. For consumers that want charging to be as quick as refueling an internal combustion engine (ICE) vehicle, 800V vehicles can deliver greater average and peak rates of power. While this is generally the case, other parameters in the vehicle and also in the charger will determine the actual charging speed.

Secondly, since the voltage is much higher, significantly less current is required to deliver the same amount of power to the traction inverter and the motor. The end result is fewer losses and greater efficiency, allowing for either a small increase in range, or a reduction in battery size (and therefore weight and cost). Either case is advantageous, and SiC MOSFETs are much more efficient than Si IGBTs at 800V due to its material and device properties, such that the transition to 800V EVs and SiC MOSFETs go hand in hand.

Finally, since less current runs through the wiring harnesses in the vehicle, the diameter of the wiring harness can be significantly reduced. Copper is heavy and expensive, so a theoretical halving of the wiring harness diameter (excluding insulation and cooling requirements) delivers a compounded cost and weight saving. Even though BEVs are much more efficient than ICE vehicles, squeezing out extra efficiency at lower cost is beneficial to the consumer, but also to the OEM, many of which have struggled with the profitability of their BEVs.

There are different ways to achieve 400V to 800V compatibility

There is one glaring issue with building an 800V platform EV: the majority of DC chargers in the world are 400V, meaning that there needs to be an onboard system to convert the 400V DC from the charger to 800V DC to charge the high voltage battery. Without such a system, the majority of DC chargers cannot be used.



➤ IDTechEx compares the three different ways to have charging compatibility between 400V and 800V. Source: IDTechEx.

Mercedes controversially did not include an 800V booster in its announcement for the Mercedes CLA EV earlier in 2025, although this has since been reversed.
IDTechEx has identified three key ways to achieve 400V to 800V charging compatibility, each with its own advantages and disadvantages. While each system is complex, IDTechEx has found that battery switching, DC boost converters, and traction integrated onboard chargers are the three main approaches from OEMs and tier-one suppliers to achieve 800V compatibility.

Boost converters are the simplest method, whereby an extra DC-DC converter is installed onto the vehicle to boost the voltage from 400V to 800V before feeding into the high voltage battery. While this is simple, it is also costly to add this extra unit, especially when space in a vehicle is limited to begin with. This is the method used in the Porsche Taycan.

By switching the configuration of cells in charging, the battery pack can be charged as a mix of series and parallel connections to match the incoming voltage from the DC charger. The GMC Hummer and Tesla Cybertruck run variants of this technique to ensure charging compatibility.

Finally, traction integrated onboard chargers are a unique way to boost the voltage without the need for a separate DC-DC converter. The windings in the electric motor act as filter inductance, and are used to boost the voltage of the incoming DC from the charger without requiring a separate DC-DC converter unit. This is the approach used by Hyundai and Kia, and multiple tier-one suppliers have similar methods to boost voltage.

Rising power densities and thermal management for semiconductors

The increase in demand for high performance computing is resulting in the need for enhanced semiconductor performance, of which thermal management is a large component. IDTechEx's report, "Thermal Management for Advanced Semiconductor Packaging 2026-2036: Technologies, Markets, and Opportunities", covers some of the main materials and applications relevant to this growing technology sector, providing forecasts spanning the next decade.

The increasing need for semiconductor thermal management

AI-oriented CPUs and GPUs are seeing increased power density, providing a 'critical engineering bottleneck', as described by IDTechEx. As a result, thermal throttling, voltage droop and accelerated electromigration are highlighted as some of the key issues arising with this growing power density, which can create problems with performance, system reliability, and the lifespan of the silicon device. There are also increased energy requirements to dissipate heat with higher power densities, meaning costs of cooling methods and infrastructure grow simultaneously. Increasing computational demands and power densities from semiconductors are also creating challenges for advanced semiconductor packaging. However, dynamic voltage/frequency scaling, power gating, and advanced power delivery networks are outlined by IDTechEx as potential means of solving these problems.

TIMs and material benchmarks

Thermal interface materials (TIMs) are necessary to transfer heat from the source to a heatsink. The movement from 2.5D packaging to 3D packaging will see a desire for TIMs to achieve low thermal resistance. However, the TIMs selected are likely to be determined by a number of factors including thermal conductivity, mechanical reliability, ease of testing, cost, contact quality, and ability to be manufactured at high volumes. The TIMs currently available for semiconductor packaging include liquid metals, solid metals such as Indium foils, graphene sheets, and polymer-based TIMs.

Liquid metals are known for being expensive, though can provide the desirable low thermal resistance, meaning there is always a trade-off to be had between performance and cost.

The exploration of new TIMs is ongoing, and includes materials such as thermal gels, indium foil, graphene sheets, and liquid metals, along with some novel and research-staged materials such as copper nanotube-based TIMs. Their qualities, including thermal conductivity, mechanical compliance, and ease of integration, are becoming increasingly important with the development of advanced semiconductor packaging. IDTechEx's report, "Thermal Interface Materials 2026-2036: Technologies, Markets and Forecasts", exclusively covers TIMs and their expected uptake over the next ten years.

Cooling approaches for HPC

Active liquid cooling will be necessary with the movement towards 3D packaging, according to IDTechEx, despite high-performance TIMs being able to provide some level of cooling functionality. Microfluidic cooling is one approach explored in the report, currently used within defense and miliary chip applications on a small scale, and therefore likely to be paving the way for wider commercial use in the future, despite its many challenges.

Air cooling, cold plate cooling, immersion cooling, and remote cooling, are four other types of technologies used within high performance computing (HPC) and are currently at different stages of scalability and commercialization. Cold plate cooling, both single and dual phase, is currently adopted in production HPC systems, and immersion cooling is primarily used for cooling multiple densely packed boards. Air cooling, however, is reportedly not scalable for high power density applications, while remote cooling, though not yet commercially available, is promising for future HPC applications. Their individual thermal capabilities, system impacts, integration complexities, and design constraints, are benchmarked in greater detail in IDTechEx's report.

Air cooling, however, is reportedly not scalable for high power density applications, while remote cooling, though not yet commercially available, is promising for future HPC applications.

IDTechEx's report further analyzes power trends, performance impacts, and power management in reducing arising challenges within the thermal management for semiconductors market.

Silicon Carbide inverter for heavy vehicles market to reach $5.8 billion by 2033

According to Research intelo, the Global Silicon Carbide Inverter for Heavy Vehicles market size was valued at $1.2 billion in 2024 and is projected to reach $5.8 billion by 2033, expanding at an impressive CAGR of 19.3% during the forecast period of 2025–2033

ONE OF THE major factors fueling this robust growth trajectory is the increasing adoption of electric heavy vehicles, particularly in sectors such as public transportation, logistics, mining, and construction. The superior efficiency, compactness, and high-temperature tolerance of silicon carbide (SiC) inverters make them highly attractive for heavy-duty applications, where power density and operational reliability are paramount. As governments worldwide intensify efforts to decarbonize transportation and manufacturers strive for greater vehicle range and performance, SiC inverters are fast becoming the technology of choice for next-generation heavy electric vehicles.

The growing need for tougher, smarter power electronics

Heavy-duty vehicles—trucks, buses, construction machines, and long-haul trailers—are entering a transformative phase as global industries push toward cleaner, electrified mobility. But electrifying heavy vehicles is not as simple as scaling up EV technologies designed for passenger cars. These machines demand **extreme endurance, massive torque, rapid charging, and uncompromised reliability.**
At the heart of this shift lies a breakthrough technology: **Silicon Carbide (SiC) inverters.**

SiC inverters are fast emerging as the “muscle and brain” of heavy electric drivetrains. They ensure that every watt of power is converted with maximum efficiency, enabling electric heavy vehicles to travel farther, carry more, and perform better than ever before.

Why silicon carbide? The technical advantage behind the revolution

Superior efficiency under heavy loads
Traditional silicon-based inverters struggle with thermal losses when dealing with high voltages and currents.SiC inverters, however, offer:

- Higher switching frequencies
- Lower conduction losses
- Consistently strong thermal performance

This directly translates into **longer driving ranges, reduced battery load, and lower operational costs.**

High voltage compatibility

Most heavy EVs operate in the **800V–1200V** range. SiC inverters can easily support these voltage levels, allowing:

- Faster DC fast-charging
- More energy-dense powertrains
- Better performance on steep gradients and heavy hauling

Compact and lightweight architecture

In an industry where every kilogram matters, SiC inverters offer:

- Smaller cooling systems
- Reduced inverter size
- More space for battery packs

For fleet operators, this means enhanced payload capacity and improved long-term profitability.

Market drivers: what's fueling the adoption of SiC inverters?

Electrification demands from logistics and mining

Global logistics giants and mining companies are under increasing sustainability pressure. SiC inverters support:

- High-duty cycles
- Continuous operations
- Rugged environmental conditions

As a result, heavy EV adoption is accelerating across ports, warehousing hubs, and mining fields.

Government policies and zero-emission mandates

Europe, China, and North America are tightening emission standards for commercial vehicles. This is pushing OEMs toward:

- Battery-electric trucks
- Hybrid heavy vehicles
- Hydrogen fuel-cell trucks (which also use SiC inverters for drivetrain efficiency)

Government incentives for cleaner transport are further boosting market momentum.

Growing demand for fast charging

Fleet vehicles cannot afford downtime. SiC inverters enable:

- Ultra-fast charging
- Reduced heat build-up
- Longer system lifetime

This makes them indispensable for high-utilization fleets.

Industry Applications: Where SiC inverters are making the biggest impact

Long-Haul electric trucks

SiC inverters help heavy trucks maintain performance across long distances while minimizing battery drain—critical for commercial fleet economics.

Electric buses and coaches

City buses benefit from:

- Higher efficiency
- Quieter operation
- Lower maintenance

SiC inverters support repeated stop-and-go cycles with minimal thermal stress.

Construction and agricultural vehicles

Bulldozers, loaders, harvesters, and cranes are increasingly adopting SiC-based powertrains for:

- High torque
- Precision control
- Reduced fuel dependency

Off-Highway and military vehicles

Extreme environments demand rugged electronics. SiC inverters excel under:

- Vibration
- Temperature extremes
- Heavy shock loads

Market Challenges: What still needs to be solved?

High Material and Manufacturing Costs

SiC wafers and device fabrication remain costlier compared to traditional silicon. However, economies of scale and improved manufacturing processes are rapidly narrowing the gap.

Supply chain constraints

As global SiC demand rises, ensuring steady wafer supply is becoming a challenge for OEMs.

Need for skilled integration

Incorporating SiC technology into heavy vehicle powertrains requires:

- Expertise in thermal management
- Advanced gate driver design
- High-voltage safety engineering

Despite these challenges, the overall market momentum remains overwhelmingly positive.

Competitive landscape

- STMicroelectronics
- Infineon Technologies AG
- Cree, Inc. (Wolfspeed)
- ON Semiconductor
- Mitsubishi Electric Corporation
- Rohm Semiconductor
- Hitachi, Ltd.
- Fuji Electric Co., Ltd.

- Dana Incorporated
- BorgWarner Inc.
- Danfoss Group
- Delphi Technologies (BorgWarner)
- Semikron Danfoss
- Vitesco Technologies

Future Outlook: A market set to accelerate

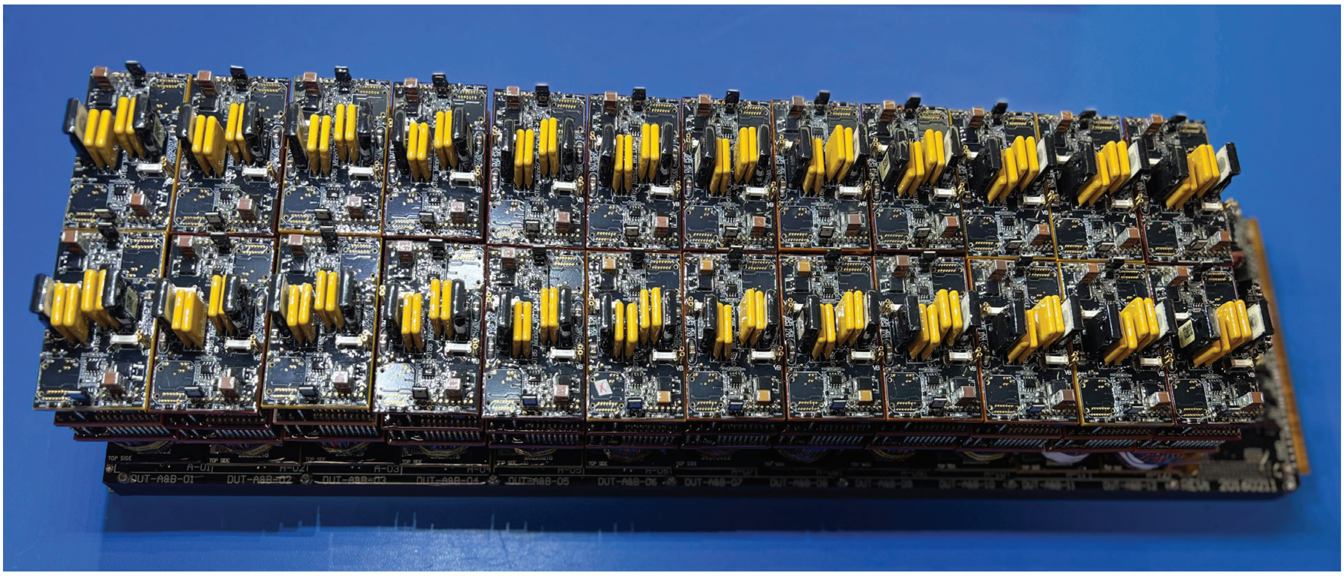
According to **Research intelo**, The Silicon Carbide inverter market for heavy vehicles is poised for exponential growth over the next decade. Key trends include:

- Wider adoption of 800V–1500V architectures
- Integration of AI-driven inverter control systems
- Increased SiC supply from new global fabs
- Rising investment from truck manufacturers and fleet operators

Analysts predict SiC inverters will become the standard in heavy electric vehicles by the early 2030s, replacing silicon-based systems almost entirely.

Source:- https://researchintelo.com/report/silicon-carbide-inverter-for-heavy-vehicles-market

> Despite these challenges, the overall market momentum remains overwhelmingly positive



GaN HEMTs enter SiC territory

Rigorous testing demonstrates the reliability and robustness of commercial 1250 V GaN HEMTs paired with a low-voltage silicon MOSFET to ensure normally-off operation

BY KAMAL VARADARAJAN, ALEXEI ANKOUDINOV, ROBERT YANG, ALEXEY KUDYMOV, BHAWANI SHANKAR, KARTHICK MURUKESAN AND SORIN GEORGESCU FROM POWER INTEGRATIONS

MATERIAL PROPERTIES govern the performance of power devices. And due to the superior properties of GaN, power devices made from this semiconductor are ideally suited for high-efficiency power conversion. Thanks to this, GaN HEMTs are being adopted in increasing number in commercial power-supply designs covering a broad range of applications, where they take advantage of this wide bandgap technology's fast switching capability with low losses.

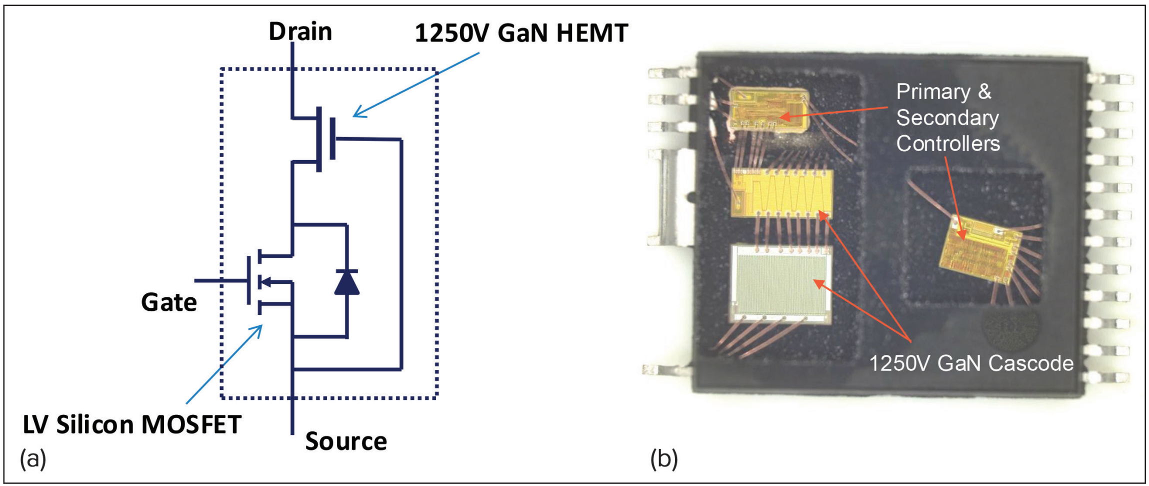
Today's designers have a broad choice, when it comes to the manufacturer of the GaN HEMT, but blocking voltages are limited. Many products on the market operate below 200 V, or in the 600 V - 650 V range. But beyond 650 V, only a few manufacturers have released devices with a rated voltage of 900 V or more. Part of the reason behind this limitation is that GaN HEMT technologies tend to employ silicon substrates, a foundation that hampers scaling to voltages beyond 900 V, due to the need for very thick buffer layers that add significant processing challenges.

Due to this, designers needing wide-bandgap power devices with a rating of 1200 V or more have been constrained to using SiC switches. However, this is an expensive choice, with cost still providing a significant barrier to SiC adoption.

To address this shortcoming, our company, Power Integrations, is breaking new ground by offering high-voltage GaN devices. Our proprietary technology enables extension beyond 900 V purely by device design and with no modification to the underlying epitaxial layer structure. These readily available products are a compelling alternative to SiC at 1200 V and beyond.

If a high-voltage power-conversion switch is to enjoy market success, lower cost and excellent performance has to go alongside reliability. We have devoted much effort on this front, involving high-voltage reliability qualification tests of a 1250 V GaN cascode switch, with a focus on some of the most critical aspects associated with high-voltage evaluation. Read on to discover our findings.

Power supply designers can reliably specify an operating peak drain-to-source voltage of 1000 V when employing a 1250 V GaN cascode device, as this caters for the industry-standard 80 percent de-rating. For industrial applications, this extent of de-rating provides significant headroom, and is particularly beneficial in challenging power grid environments where robustness provides an essential defence against grid instability, surge, and other power perturbations. Another market for the



➤ Figure 1. (a) Circuit schematic for the 1250 V GaN cascode switch. (b) Flyback switcher IC with the 1250 V GaN cascode, primary, and secondary controllers.

1250 V rated GaN switch results from the prevalence of 800 V bus architectures, with this device enabling cost-effective, significant performance improvements in various sub-systems in electric vehicles while providing the derating needed to ensure high system reliability.

A cascode configuration

Our 1250 V GaN HEMT is a normally-on, depletion-mode device. To realise effective normally-off operation, which is essential for safe operation of power electronic systems, it is connected in series with a low-voltage silicon MOSFET in a cascode configuration (see Figure 1 (a), which provides a circuit schematic for the cascode switch, comprising 1250 V GaN and a low-voltage silicon MOSFET). The 1250 V GaN cascode is incorporated as the primary side switch in a flyback switcher IC, which also includes primary and secondary side controllers (see Figure 1 (b)).

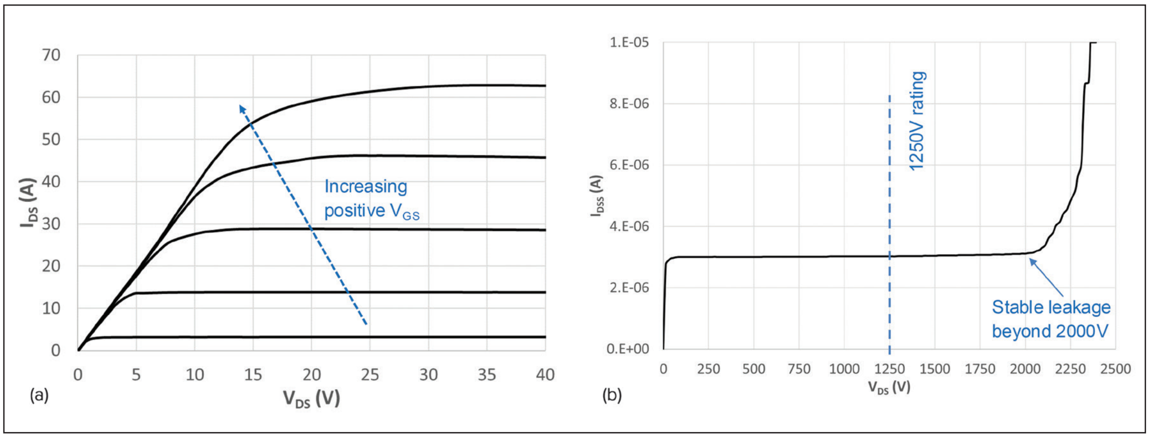
Measurements of pulsed output characteristics of a typical 330 mΩ, 1250 V GaN cascode device demonstrate its high-current capability and device scalability, assets that aid the addressing of high-power applications (see Figure 2 (a)). Our 1250 V cascode devices also exhibits excellent off-state characteristics, with measurements on a typical HEMT showing stable leakage to beyond 2000 V, ensuring excellent transient overvoltage capability (see Figure 2 (b)). This strength shows that our 1250 V devices offer a significant safety margin when compared with silicon and SiC devices with similar voltage ratings.

Ensuring field reliability

While good on-state and off-state characteristics are valued, they must go hand-in-hand with meeting and exceeding industry-standard reliability qualification requirements, in order to ensure reliable operation in the field. Here we share results meeting this goal, obtained from critical high-voltage reliability stress evaluations, covering both static and dynamic conditions. These tests were performed as part of our qualification of the 1250 V GaN HEMT for power-conversion applications.

One common test is the high-temperature reverse-bias (HTRB) test. This is an off-state reliability stress test that evaluates the long-term stability of the power device under a high drain-to-source bias, with a high temperature employed to accelerate thermally activated failure mechanisms under high electric-fields over an extended period.

We performed the HTRB stress test of our 1250 V GaN cascode device in a 150°C ambient environment, using an off-state drain-source voltage of 1000 V (80 percent of 1250 V rating) for 1000 hours. Our device passed this test, fulfilling all



➤ Figure 2. (a) Output characteristics of a 330 mΩ, 1250 V GaN cascode device illustrating high current capability. (b) Typical off-state characteristics demonstrating leakage remaining stable beyond 2000 V.

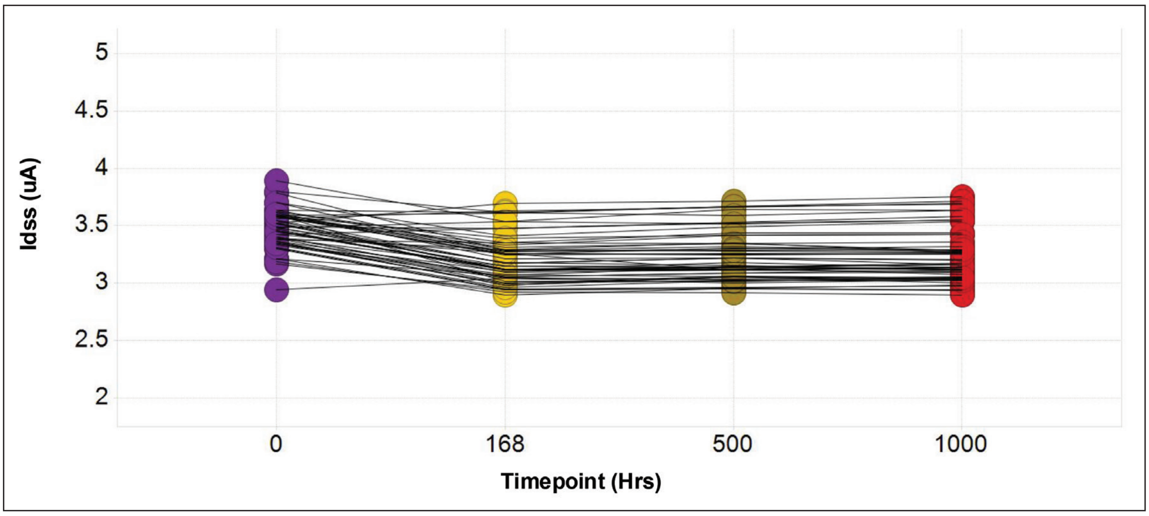


Figure. 3. Stable off-state drain leakage through 1000 hours of high-temperature reverse-bias stress at 1000 V/150 °C.

Voltage / Temperature	80°C	100°C	120°C
2100V		✓	
2150V	✓	✓	✓
2200V		✓	

Table 1. Accelerated evaluation conditions in the off-state.

specifications defined in JEP198 – it is the JEDEC guideline for reverse-bias reliability evaluation procedures for GaN power-conversion devices. One critical parameter to monitor during the HTRB stress test is the off-state drain-to-source leakage current. We observed excellent device leakage stability, validating the suitability of our cascode devices for high-reliability applications at high voltages (see Figure 3).

In addition to the HTRB qualification test, we determined intrinsic off-state failure rates, extracted by running tests on a large number of units under accelerated drain-source voltage conditions (2100 V to 2200 V) across multiple temperatures (80°C to 120°C). Test conditions are shown in Table 1.

Based on the time-to-failure Weibull distribution obtained from this set of experiments, we extracted: a voltage acceleration factor, using an exponential model; and a temperature acceleration factor, via an Arrhenius model. These factors enabled a projection of failure rate under typical use conditions. Our model predicts a cumulative failure rate of 1 part per million in more than 15,000 years of operation at 1000 V/100 °C (see Figure 4), indicating a significant built-in reliability margin for our 1250 V GaN cascode power device.

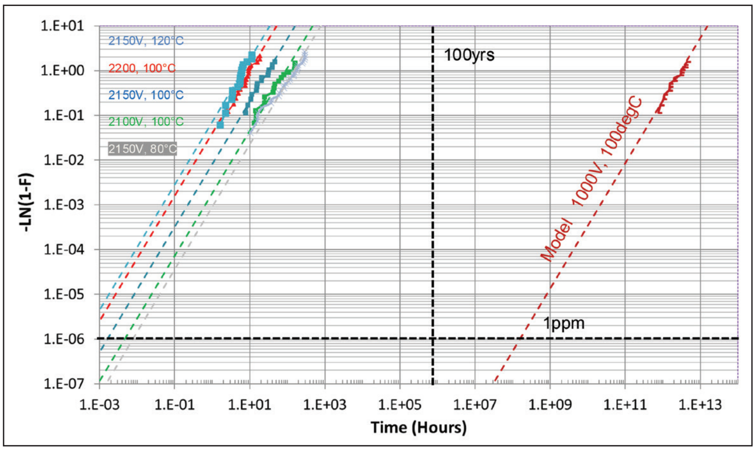


Figure 4. Weibull distributions indicating time-to-failure under multiple accelerated stress conditions and the projected distribution at 1000 V/100 °C.

For many high-reliability deployments, such as industrial applications, reliability requirements go beyond just passing the HTRB-based off-state reliability qualification stress test. That's because HEMTs are often exposed to harsh external environmental conditions, where they have to operate continually, or for extended periods of time, in extreme mission-critical applications. In these demanding conditions, it is crucial for HEMTs to pass the HV-H3TRB test, which involves a controlled high humidity environment, an additional stressor to the original HTRB test. This stress test, incorporating additional failure modes produced by moisture penetration, examines all aspects of the device, including its passivation layer, active and termination design, and underlying structures.

We undertook the HV-H3TRB stress test of our 1250 V GaN cascode device in an 85°C ambient environment with a relative humidity of 85 percent, stressing with an off-state drain-source voltage of 1000 V for 1000 hours. These conditions follow JEDEC standard JESD22-A101.

Clean passing results were obtained for this stress test. We paid particular attention to the most critical

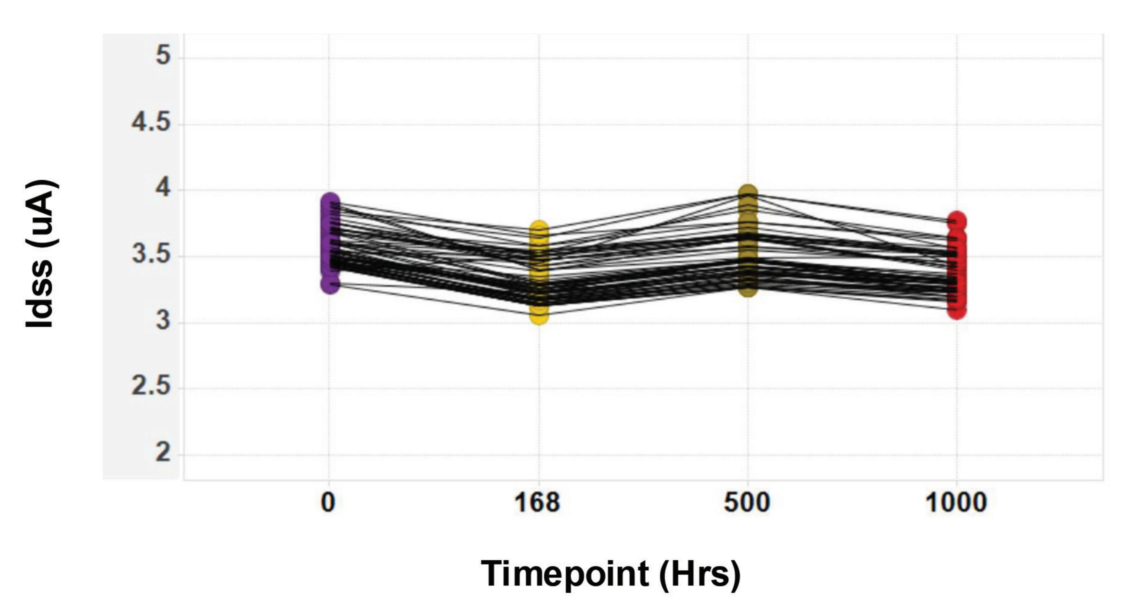


Figure 5. Stable off-state drain leakage through 1000 hours of HV-H3TRB stress at 85 percent relative humidity/85 °C/ 1000 V.

parameter, the off-state drain-to-source leakage current, monitoring this at various times during the HV-H3TRB stress test. Our device exhibited excellent leakage stability, validating its suitability for high-reliability industrial applications (see Figure 5).

A key concern that initially delayed the commercial introduction of GaN HEMTs by many of its manufacturers is reliability when switching in high-voltage applications. Studies would show that the device's on-resistance increased immediately after turn-on compared with the DC condition. This phenomenon, known as dynamic $R_{DS(ON)}$, is widely attributed to charge-trapping effects within the device under high electric-field strengths. A number of techniques have been employed to address this issue, including epitaxial structure engineering and carefully optimised processing techniques.
In response to the field reliability implication, JEDEC recently introduced a guideline JEP180, detailing dynamic high-temperature operating life (DHTOL) testing. This document specifies switching reliability evaluation procedures for GaN power-conversion devices.

Using the JEP180, we evaluated switching reliability of our 1250 V GaN cascode in a custom testbed with the capability to evaluate multiple units in parallel at 125°C. For this test we employed the most stringent operating conditions – hard-switched turn-on and turn-off at 1000 V – based on the

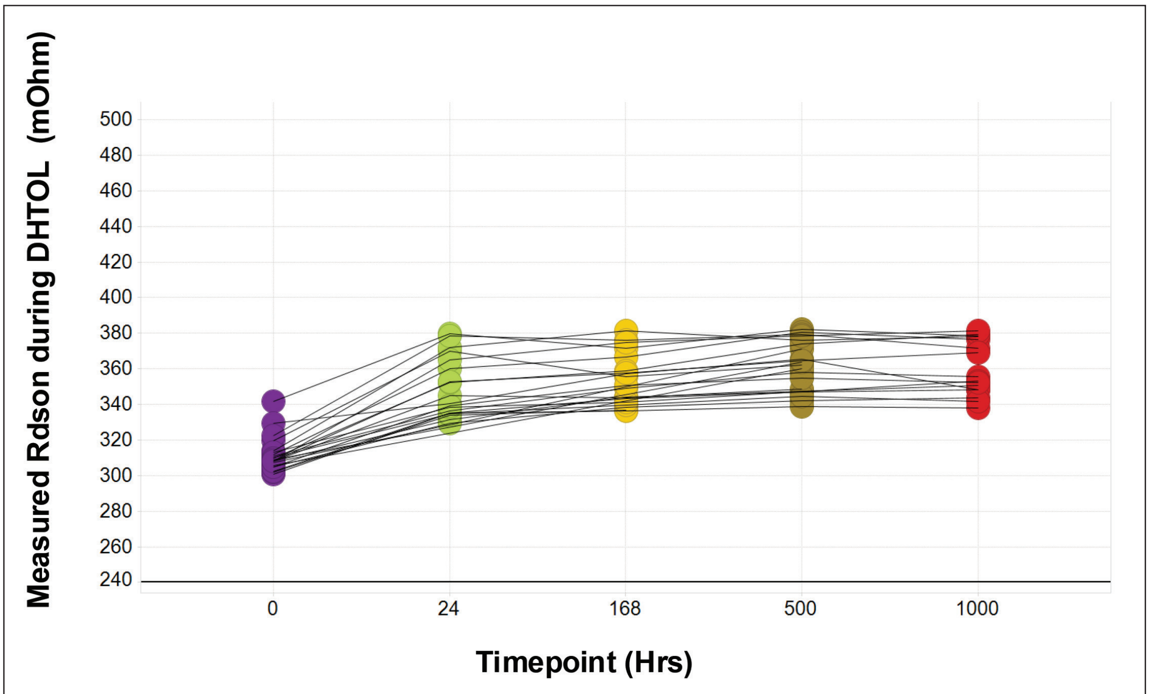


Figure 6. Stable $R_{DS(ON)}$ observed during 1000 hours DHTOL with minimal shift (less than 20 percent).

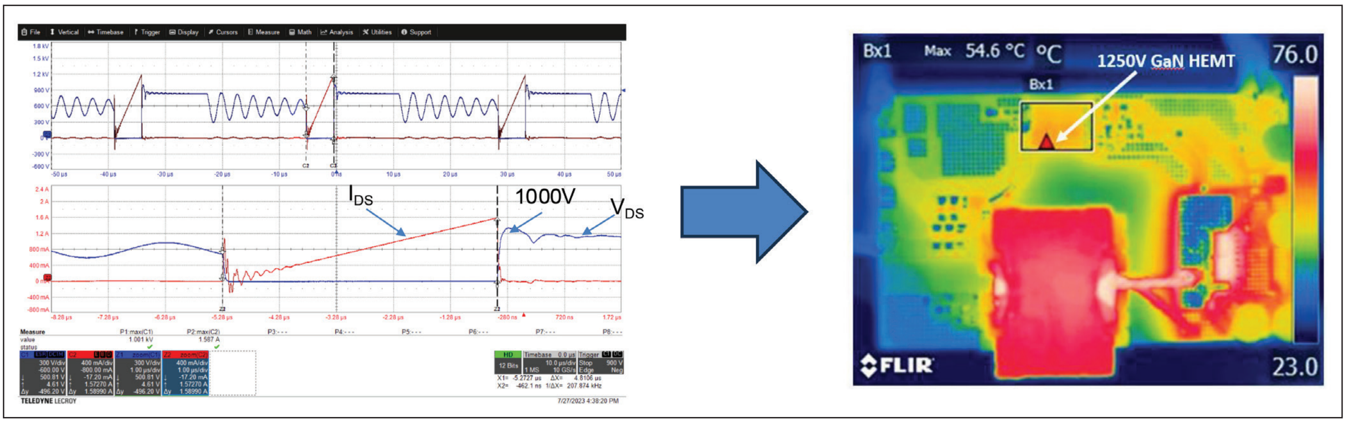


Figure 7. (a) Steady-state switching waveform illustrating 1000 V Peak V_{DSv}. (b) Steady-state thermals indicating temperature rise below 30 °C during continuous switching and a $V_{DS(PK)}$ of 1000 V.

switching locus described in JEP180. The dynamic $R_{DS(ON)}$ during high-voltage switching is of particular interest. Improperly designed GaN HEMT devices tend to exhibit a significant increase in $R_{DS(ON)}$ during high-voltage switching transitions due to additional electron trapping, which can have a detrimental effect on the converter efficiency, or in extreme case, result in hard failure.

We have monitored variations in the $R_{DS(ON)}$ of our 1250 V GaN cascode over the course of 1000 hours of DHTOL stress at 1000 V, a peak current of 2 A, and a junction temperature of 125°C. This test shows stable performance from the earliest timepoint, with a minimal shift of less than 20 percent (see Figure 6). It's a degree of stability that's on par with state-of-the-art 650 V GaN HEMTs tested under similar hard-switching conditions.

A key implication of this result, and the others described in this article, is that GaN HEMTs can be scaled to more than 1200 V without any compromise in performance, including critical hard-switching capability. Rigorous testing demonstrates their robustness to meet all potential high-reliability use cases.

A real-life application

To highlight the capability of our 1250 V GaN HEMT in real-life applications, we have deployed this device in a 60 W, 24 V/2.5 A flyback power supply, built using the switcher IC (see Figure 1 (b)). By evaluating the steady-state operation of the flyback power supply running at a peak drain-source voltage of 1000 V, we confirmed stable operation with corresponding switching waveforms (see Figure 7 (a)).

Measurements have determined low, stable operating temperatures for the power supply, realised without any external cooling over long periods of continuous operation, with a peak drain-source voltage of 1000 V. This is an encouraging result, validating the minimal magnitude and effect of the shift in $R_{DS(ON)}$ during DHTOL stress evaluation. The maximum temperature of the 1250 V GaN HEMT remained below 55°C (see Figure 7 (b)), indicating a temperature rise of only 30°C in this application compared to ambient.

While the GaN cascode is designed to operate with a peak drain-source voltage below 1000 V in a continuous mode, it can accommodate momentary increases in supply voltage up to a peak of 1250 V. This transient voltage capability allows the GaN cascode to continue to switch through the surge event for short periods without suffering a hard failure. We demonstrated this attribute by increasing the input voltage until the peak drain-source voltage during switching reached the maximum rated value of 1250 V without running into any abnormal operation (see Figure 8).

As well as being extremely robust, the flyback

While the GaN cascode is designed to operate with a peak drain-source voltage below 1000 V in a continuous mode, it can accommodate momentary increases in supply voltage up to a peak of 1250 V. This transient voltage capability allows the GaN cascode to continue to switch through the surge event for short periods without suffering a hard failure

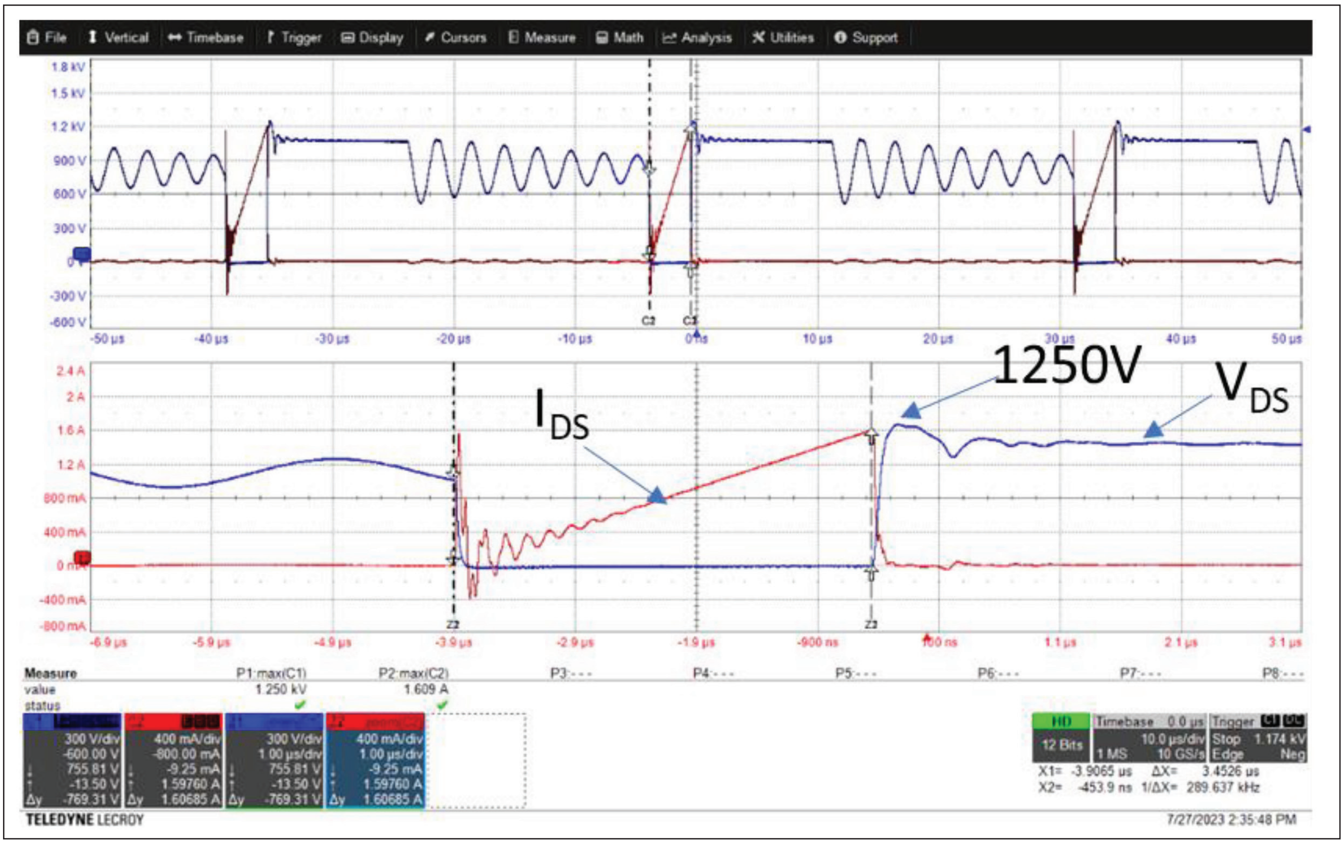


Figure 8. Switching waveform illustrating transient overvoltage capability up to a peak V_{DS} of 1250 V.

power supply designed with the 1250 V flyback switcher IC operates with a best-in-class full-load efficiency exceeding 92 percent at a 700 V input (see Figure 9).

High-voltage GaN HEMT roadmap

Our work demonstrates the capability of 1250 V GaN HEMTs as a credible alternative to SiC. We also offer flyback switcher IC products based on a 1700 V GaN HEMT, clearly establishing that our technology can be scaled to even higher voltages.

With our proprietary and improving GaN HEMT technology, particularly suited to ultra-high voltages, devices with ratings beyond 2000 V that are currently catered for by SiC are now within close reach. For power supply designers, the portfolio of reliable, alternative wide-bandgap power switch is expanding.

Though lateral GaN device structures have a fundamental limitation in matching the specific-on-resistance – that's the on-resistance per unit area – of vertical devices, it is possible to significantly increase power levels through improvements in packaging and thermal management.

When higher switching frequencies, improved efficiency, high reliability and lower costs compared with SiC are factored in, high-voltage GaN HEMTs are compelling candidates in industrial, data centre, automotive and other high-reliability applications over a wide power range.

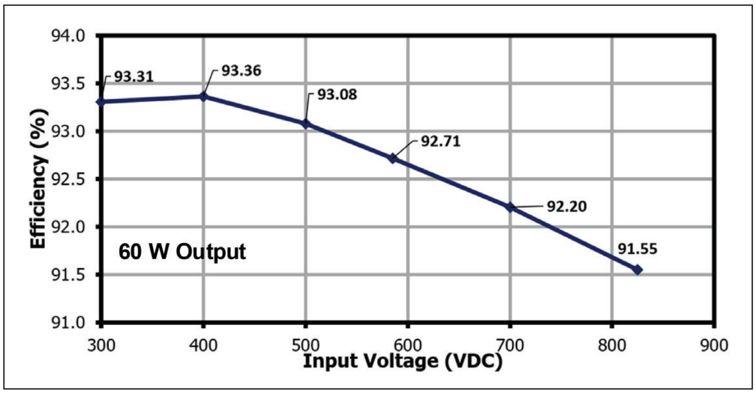
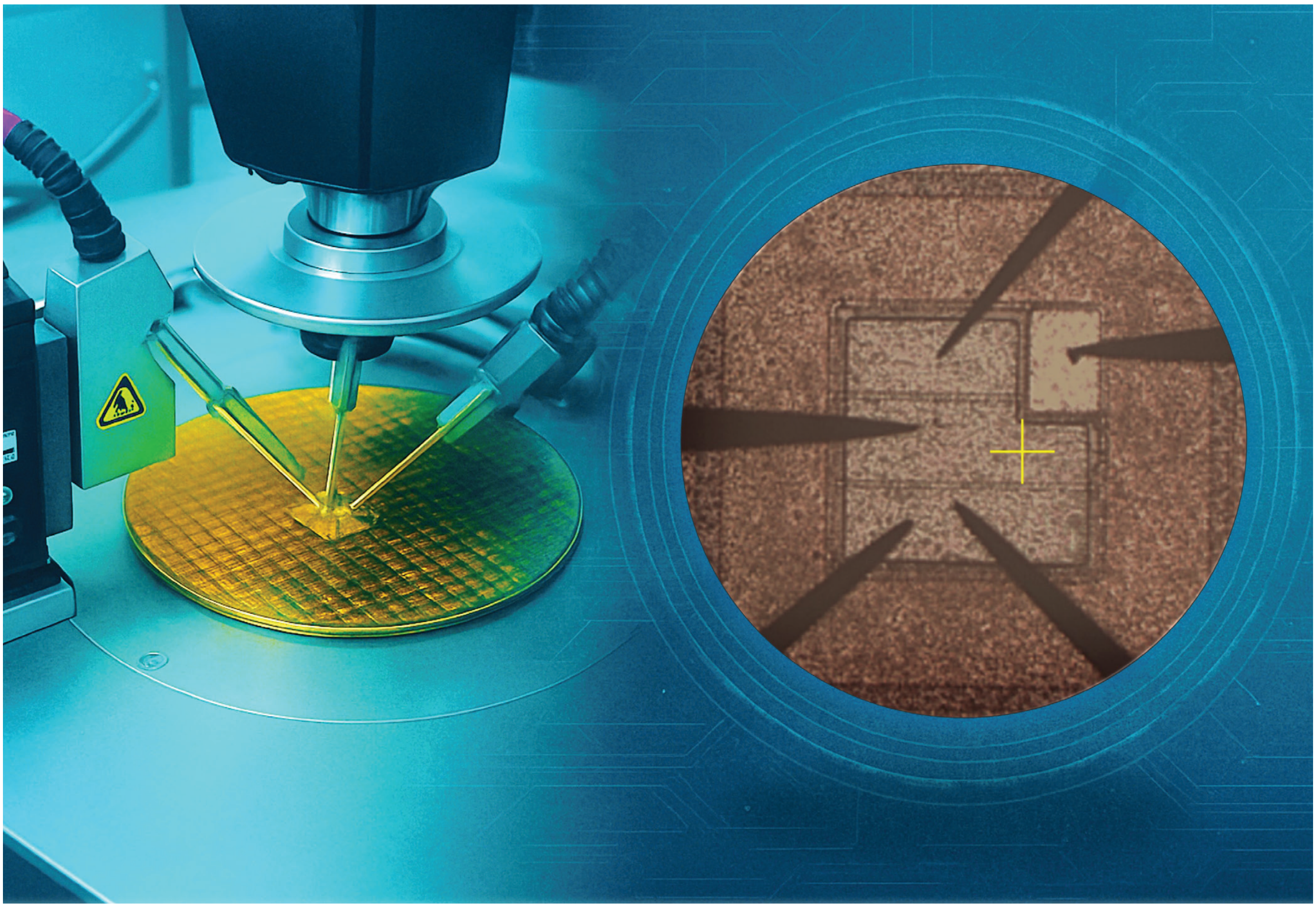


Figure 9. 1250 V GaN-based flyback power supply efficiency versus input voltage.

FURTHER READING

- K. Varadarajan *et al.* " Reliability Qualification of 1250 V Lateral GaN HEMTs for High Reliability Industrial Applications," IEEE International Reliability Physics Symposium proceeding, 3A2.1-3A2.6 (2025)
- K. Varadarajan *et al.* "Reaching Beyond 1200 V: Lateral GaN HEMTs for High-Reliability EV and Industrial Applications" PCIM Europe proceeding, 1593-1598 (2024)
- K. Murukesan *et al.* "State of the Art 1.7 kV Lateral GaN HEMTs, an Alternative to SiC", IEEE Applied Power Electronics Conference proceeding, 180-184 (2025)



Driving the electric revolution with SiC IGBTs

FOR²ENSICS, an EU-funded initiative, is targeting the simplification of medium-voltage DC converters with ultra-high-voltage SiC IGBTs

BY NAZARENO DONATO, UNIVERSITY OF CAMBRIDGE

THE GLOBAL DRIVE to trim carbon emissions and reach climate neutrality is rapidly transforming electricity supply and grid infrastructure. Critical to succeeding in this endeavour is the introduction of a new generation of power devices, delivering higher efficiencies at reduced costs, through a smart combination of reduced epitaxial layer thickness and a smaller form factor.

One promising route towards this goal is DC distribution, well matched to renewable sources and modern loads, such as solar arrays and battery systems, which already operate in DC. But the power electronics market still lacks low-cost, compact, high-performance DC-to-DC converters that are capable of handling voltages from below 1.5 kV to well over 10 kV.

Aiming to close that gap with a commercial-grade DC-to-DC converter featuring a medium-voltage stage based on ultra-high-voltage SiC IGBTs is our Horizon Europe-funded project entitled Future Oriented Renewable and Reliable Energy SiC Solutions (FOR²ENSICS). By turning from series-connected medium voltage (1.2 kV - 6.5 kV) SiC MOSFETs or silicon IGBTs to ultra-high-voltage SiC IGBTs, we promise to unleash a number of key benefits, including lower conduction losses, simpler drive requirements, a smaller footprint and reduced costs. However, delivering such technology demands coordinated expertise in device fabrication, passivation, packaging and converter assembly – goals realised by a joint effort, drawing on a broad range of expertise from industry and academia.

SiC IGBT technology

Silicon-based IGBTs have long been a mainstay in traction, industrial, automotive and high-voltage DC systems, typically operating from 900 V to 6.5 kV. Their bipolar conduction helps overcome MOSFET limitations, improving the trade-off between the static voltage drop and turn-off losses.

With the arrival of 4H-SiC unipolar devices in the 1.2 kV -3.3 kV range, silicon IGBTs – still extremely cost-competitive – are losing ground in medium-voltage applications. However, for 6.5 kV and beyond, SiC MOSFETs are up against scaling and cost limits, even with superjunction concepts. On one hand, yield and defect density limit the maximum achievable die area; on the other, scaling of the drift region resistance makes the SiC MOSFET less suitable for medium- to high-current applications.

For ultra-high-voltage applications – that's more than 10 kV – operating at moderate switching frequencies of tens to hundreds of kilohertz, the SiC IGBT offers a compelling alternative. Its advantages include avoiding some of the drawbacks of series-connected SiC MOSFETs, which are more susceptible to voltage imbalance and require more complex gate driving. In addition, SiC IGBTs benefit from a reduced drift-region thickness, compared with their silicon siblings. This gives the SiC IGBT a fundamental advantage, resulting from a lowering of stored charge that ensures reduced switching losses.

Enjoying the benefits of the SiC IGBT is not easy, as its design brings significant challenges, due to intrinsic material constraints. One issue is the higher forward voltage drop, stemming from a delayed bipolar turn-on. This drop – measured at room temperature it's 2.8 V for 4H-SiC, versus 0.7 V for silicon – leads to increased conduction losses at low and medium currents. The other noteworthy drawback is the limited minority-carrier lifetime – only recently extended into the microsecond range – that reduces the benefits of bipolar conduction when the diffusion length is smaller than the drift region thickness. The peak minority-carrier lifetime achieved in the last ten years also limits the maximum drift-region thickness between 100 µm to 200 µm, placing the optimal performance window between 10 kV and 20 kV – the target range for our FOR^{2}ENSICS project.

The backside processing conundrum

Manufacturing *n*-type SiC IGBTs for ultra-high-voltage applications is a non-trivial task. Challenges arise, due to the absence of high-quality *p*-type SiC substrates, and the need for thick, high-quality epitaxial layers to support blocking voltages beyond 10 kV. In recent years, researchers have explored different fabrication routes, like the flip-type process – this involves removing the n^+ substrate and forming the device channel and the gate oxide on the carbon face – alongside careful process and design optimisation. However, this promising route is yet to yield a commercial SiC IGBT, largely due to cost and performance constraints (as well as mechanical stability).

Our project is pursuing a more streamlined approach, which retains the thick epitaxial layer and substrate throughout processing. Starting with an n^+ substrate, our flow involves forming a highly doped *p*-type collector, adding a buffer layer, growing the epi, and then fabricating the top MOS cell. Backend processing includes substrate splitting or removal – using a combination of back grinding, chemical mechanical polishing and etching – to enable either reuse of the substrate (laser cut achieved through Kabra split or similar methods) or backside access (see Figure 1), prior to metallisation.

The consortium

FOR^{2}ENSICS is a Horizon EU-funded project that runs for four years, from January 2023 to December 2026. This effort is organised into eight work packages. The project brings together a consortium of leading European institutions and renowned semiconductor companies, each contributing complementary expertise to the development of disruptive ultra-high-voltage semiconductor devices and technologies. The overarching aim is to place European industry at the forefront of the energy transition, competing with efforts from semiconductor supply chains in the US and Japan.

Consortium members include: CSIC (Spain, coordinator), Coherent Corp. (Sweden), University of Cambridge (UK), Hitachi Energy (Switzerland), Deep Concept (France), University of Bremen (Germany), EPFL (Switzerland), and SuperGrid Institute (France). Together, these partners cover the full spectrum from materials and device design to packaging, system integration, and testing.

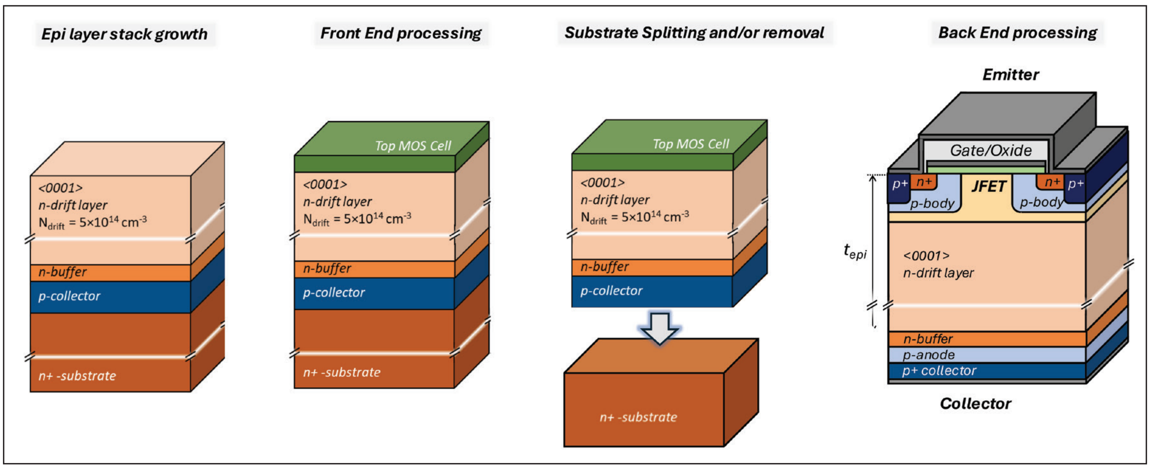
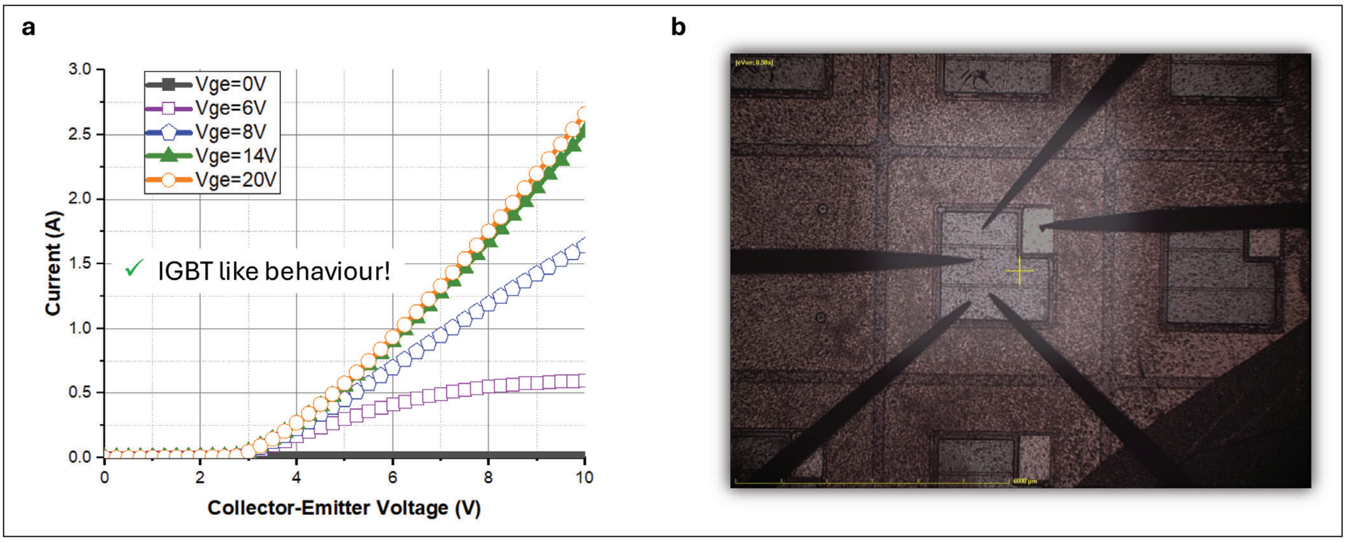


Figure 1. Schematic process flow for the fabrication of ultra-high-voltage SiC IGBTs.



➤ Figure 2. (a) IGBT characteristics prior to thick metal deposition and (b) a microscopic image of the IGBT under test in the Henry Royce High Voltage Characterisation Suite (Cambridge University).

Early trials have delivered encouraging results, indicating that our approach is a viable manufacturing route. Our first batch of SiC IGBT devices is currently under test, with preliminary results show promising gate modulation and successful backside substrate removal (see Figure 2).

In parallel, we are producing SiC MOSFETs rated at 3.3 kV, 10 kV and 15 kV to benchmark against our IGBTs in a DC-to-DC converter dual-active-bridge demonstrator.

Leading this high-voltage SiC device fabrication effort are our consortium members at The University of Cambridge, Coherent, CNM and Hitachi Energy.

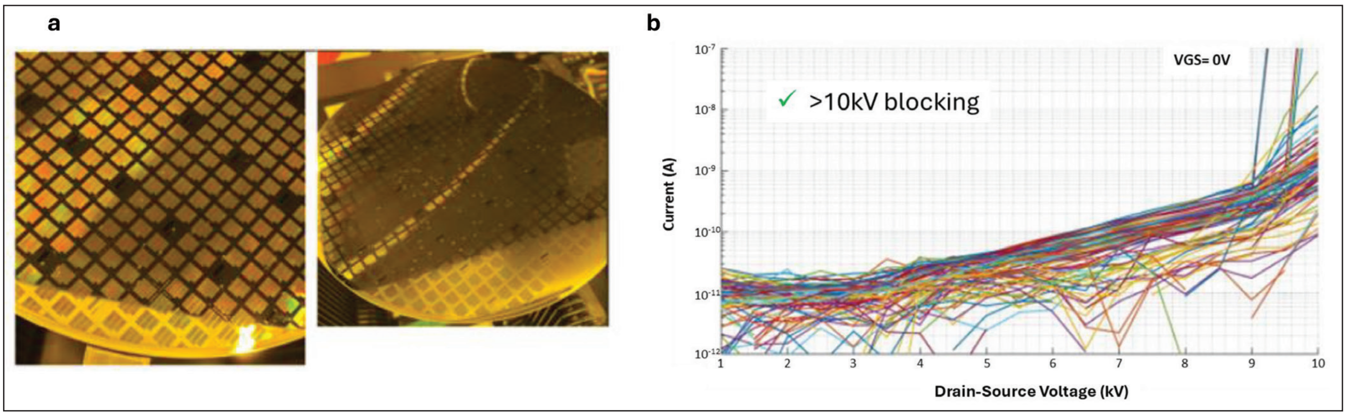
Edge termination design

For ultra-high-voltage SiC devices with ratings above 10 kV, it is critical to employ an efficient edge termination. Conventional termination designs capable of withstanding such voltages tend to require large die areas – and that's a costly design solution when working with epiwafers over 100 μm-thick that must deliver tens of Amps. The aim is to minimise the termination footprint while maintaining robust blocking performance and avoiding any compromise to passivation and oxide reliability.

Testing of a SiC MOSFET platform has already demonstrated edge terminations capable of blocking more than 10 kV during on-wafer measurements (see Figure 3). We have also developed a new test platform for packaged devices that evaluates up to 20 kV, along with a double-pulse test system operating above 10 kV using a dedicated DC supply. The next stage is to prove these termination concepts on IGBTs.

Packaging and reliability

To unlock the full potential of high-voltage SiC technology, packaging must combine electrical performance with long-term reliability at 15 kV. Our package design uses high-field passivation and gel materials to withstand extreme voltages, temperatures and humidity without degrading device performance. This package supports both the integration of high-voltage SiC MOSFETs



➤ Figure 3. (a) Photo of 10 kV SiC MOSFET wafer and (b) wafer-level forward-blocking characteristics for MOSFETs implementing D3 termination design, measured at room temperature with a gate-source voltage of zero.

and IGBTs (in parallel or series connection) with a high-voltage SiC diode – a MOSFET in diode mode – providing wide flexibility for all the devices manufactured within the project.

A PCB mezzanine within the module carries integrated passive components, such as gate driver resistors, a negative-temperature-coefficient sensor and an RC snubber (see Figure 4 (a)). Leading this work are Deep Concept and the SuperGrid Institute.

We have used a number of standard approaches to evaluate reliability. They include high-temperature reverse-bias tests, investigation of time-dependent dielectric breakdown and the high-humidity, high-temperature and high-voltage reverse-bias test. Results confirm the robustness of our high-voltage SiC IGBTs. In addition, there's a multi-die test platform for bipolar degradation studies – capable of testing up to 16 devices in parallel – that's now operational at the University of Bremen.

Upcoming events and demonstrators

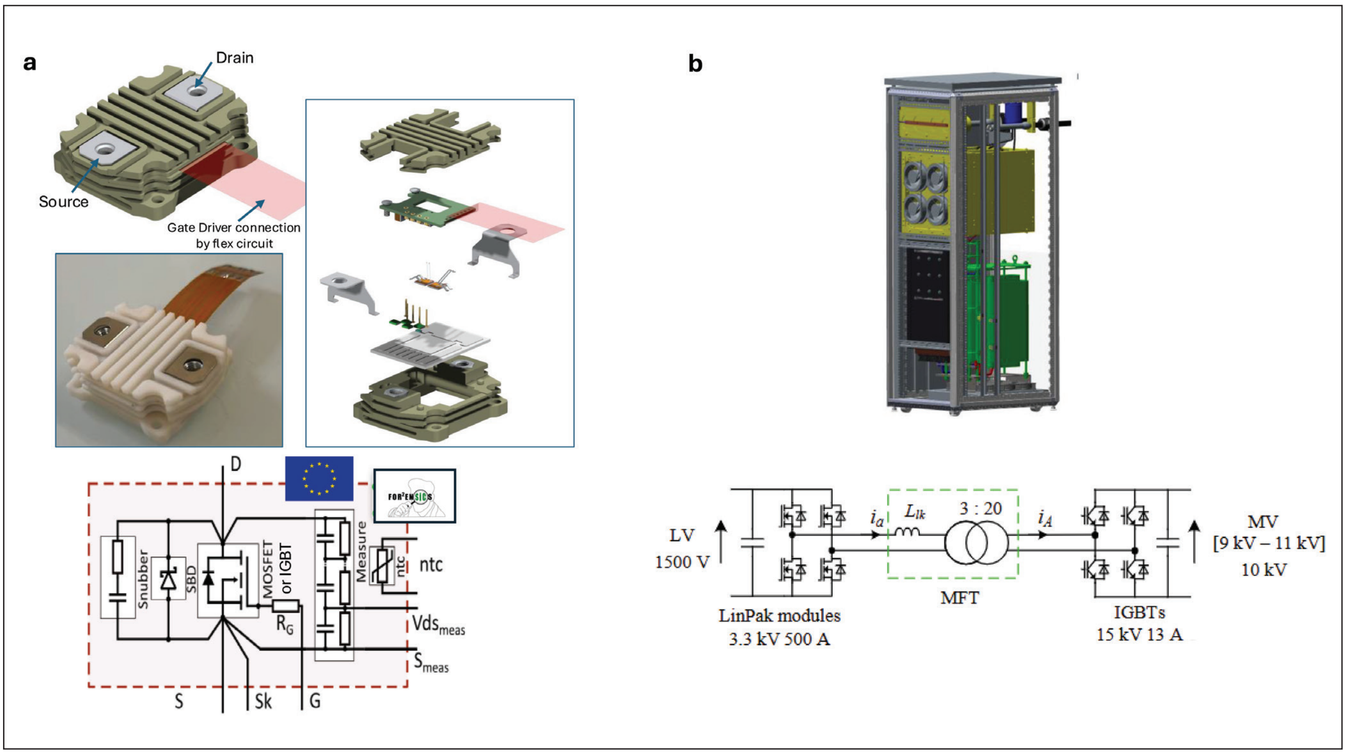
KEY upcoming milestones for the FOR²ENSICS project include the medium-voltage DC converter demonstrator, using series-connected SiC MOSFETs. After showcasing this at the SuperGrid Institute in Lyon in November 2025, a follow-up system demonstrator based on SiC IGBTs will take place in 2026 to mark the end of the project. The consortium will also host a Summer School on Power Semiconductors in Cambridge, UK, in 2026, aimed at training the next generation of researchers with a series of talks on power devices and electronics from worldwide experts. Results from the project have been presented at the ECPE Workshop in Lyon in November 2025.

All these events welcome participation from PhD students and postdoctoral researchers, including those from EU sister projects AdvanSiC and SiC4GRID. These gatherings can foster knowledge exchange across the European power semiconductor community.

Gate drivers and converters

A major demonstration target for our project is the dual-active-bridge converter, selected for its efficiency and adaptability in medium-voltage DC applications. The first prototype, showcased this November at the SuperGrid Institute in Lyon, uses a series-connected 3.3 kV SiC MOSFET (see Figure 4 (b)). This platform serves as our baseline for a follow-up demonstrator in 2026, using the project's 15 kV SiC IGBTs.

Our single-phase dual-active-bridge converter comprises two full bridges – one connected to the low-voltage bus, designed with LinPak SiC MOSFETs from Hitachi Energy; and the other to the medium-



➤ Figure 4. (a) Ultra-high voltage packaging concept for SiC IGBT and (b) dual active bridge demonstrator.

voltage bus – linked through a medium-frequency transformer. The converter benefits from the opportunity to operate at elevated switching frequencies of tens of kilohertz, because it is not tied to the grid's 50/60 Hz. Thanks to this freedom, the convertor can operate at a higher power density and be constructed from smaller passive components.

Moving to ultra-high-voltage SiC devices on the medium-voltage side also demands advanced gate driver technology. As well as translating control signals into required drive levels, the driver has to handle short-circuit events, limit over-voltage, and employ active Miller clamping to avoid parasitic turn-on. For series-connected switches, it's also critical to ensure precise voltage sharing during static and dynamic conditions. Fulfilling all these requirements enables the design to integrate voltage-balancing measures alongside tuned gate resistances. Leading this work are EPFL and the SuperGrid Institute.

Features of our dual-active-bridge converter include galvanic isolation of the gate driver's power supply, employed to withstand high common-mode transients, and a layout that's optimised to minimise parasitics that could impair superior switching performance. Together, these design choices ensure that the converter exploits the high efficiency and robustness of ultra-high-voltage SiC devices, and provides a strong platform for validating SiC IGBTs in demanding medium-voltage DC systems.

FURTHER READING

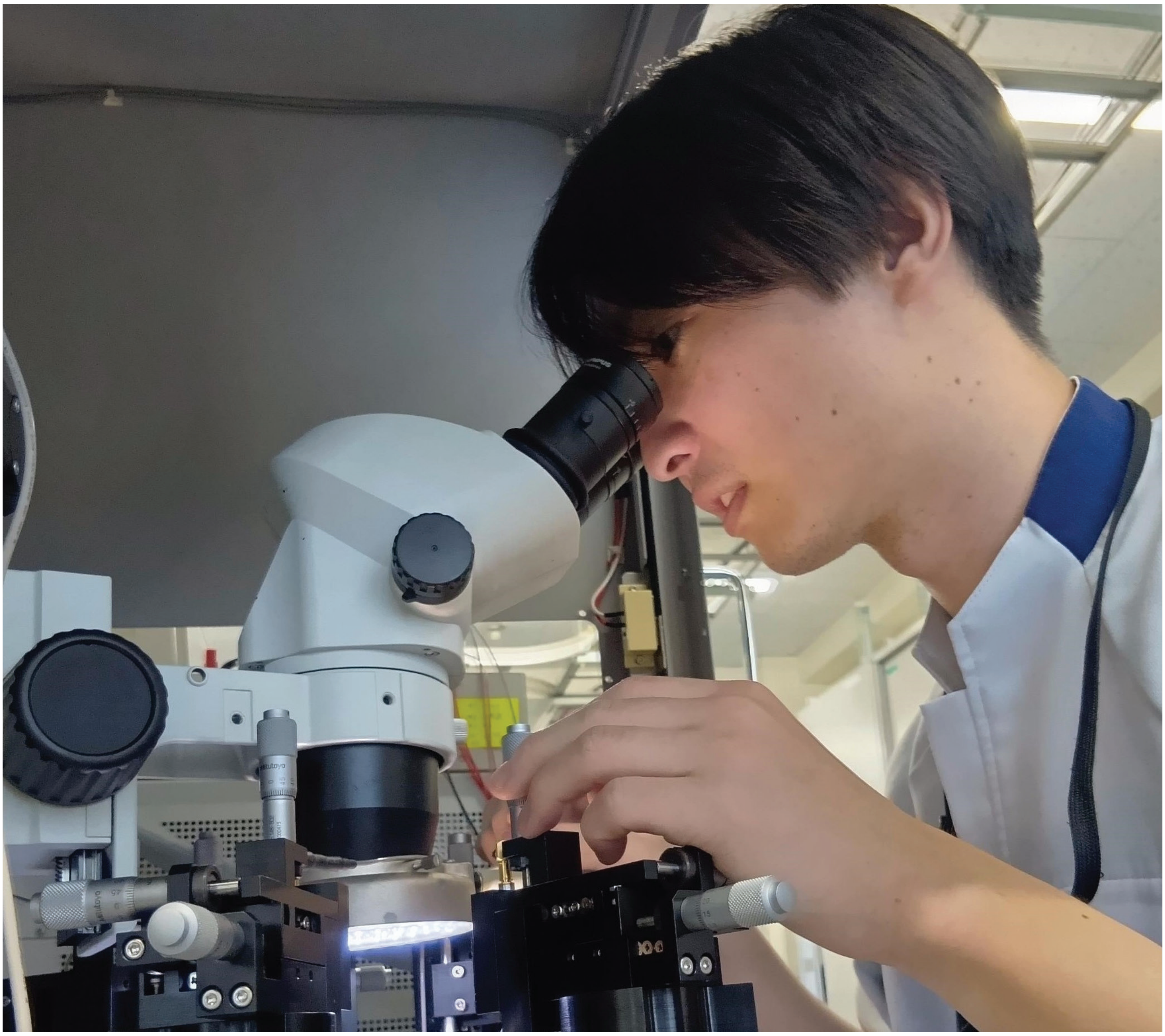
- https://for2ensics.imb-cnm.csic.es/ (FOR²ENSICs webpage)

Next steps

As the project enters its core phase, with new IGBT devices emerging from the fab and packaging activities underway, our consortium is moving into a more mature stage of development. Our recent research efforts have focused on making additional improvements to backside metallisation contact resistance and substrate removal, as well as developing multi-die packaging solutions – connecting up to four devices in parallel – to meet the higher current requirements of the final dual-active-bridge demonstrator. We are also progressing modelling and simulation activities in parallel, efforts that will help enhance IGBT performance in upcoming batches, particularly in terms of current capability and temperature coefficient.

Successful proof-of-concept demonstrations at both the device and system levels have encouraged our consortium to pursue new ideas. They include: advanced device concepts, such as reverse-conducting SiC IGBTs; further reductions in the edge termination footprint; novel packaging approaches, using ultra-high-field-strength passivation materials; and the development of larger active areas, as yields continue to improve. If you want to say informed, follow the project updates on our website and social media platforms.

FOR²ENSICS has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No 101075672.



Cranking up the switching speed with a *p*-GaN shield

Adding a *p*-GaN shield to a vertical GaN-on-GaN transistor trims capacitance and enhances high-power, high-speed switching

BY NAOKI TORII, DAISUKE SHIBATA, MASAHIRO OGAWA, MASAO KAWAGUCHI, HIROYUKI HANDA, NAOHIRO TSURUMI, SATOSHI TAMURA AND YOSHIO OKAYAMA FROM PANASONIC

SALES OF power electronics are tipped to soar throughout this decade and beyond. Driving this trend is the increase in production of electric vehicles and the growth of data centres, which have more demanding power requirements due to the uptake of AI.

For every application using power electronics, an increase in their efficiency is beneficial. Gains may include an increase in driving range, a reduction in electricity bills, less heating, and a lower carbon footprint.

Due to these benefits that result from a superior efficiency, there is an increasing uptake of devices based on wide bandgap semiconductors. So far, those based on SiC have generated the most revenue, with MOSFETs grabbing headlines for winning deployment in electrical vehicles.

However, despite enjoying much success, SiC devices have some significant deficiencies. They included the interface between SiC and SiO_2, which is far from perfect.

Avoiding these issues is the lateral GaN transistor, which is already netting significant sales by dominating the market for the fast-charging of mobile devices. One of the benefits of this class of device, which can be grown on large-area, low-cost silicon substrates, is that high levels of mobility are realised without doping. Instead, internal polarisation is exploited to produce a two-dimensional electron gas (2DEG).

This lateral device is a significant milestone for the GaN transistor, providing the first 'killer' application – premium fast-charging units for the likes of smartphones, tablets and laptops. But going beyond this is far from easy with these lateral devices, because it is very challenging to reach high values for output current and breakdown voltage and thus output power. With this device geometry, critical design considerations for high power are the area of the electrodes, and the spacing between the source and drain on the surface of the device.

Offering a very promising way forward is a new architecture, involving a shift from a lateral to a vertical geometry. With these more compact devices, which a number of teams have been developing from around the world over the last few years, source and drain electrodes are placed on opposite sides of the substrate, enabling design engineers to scale the power of the transistor while not significantly increasing its footprint.

Our company, Panasonic, is one of the trailblazers of the vertical GaN transistor. We have developed a variant that's a high-power vertical GaN JFET, which we refer to as a VJFET. It's produced using the re-growth of *p*-GaN/AlGaN/GaN channels.

For GaN devices to realise their full potential at the system level, where they promise to aid miniaturisation and trim loss, it is essential that they are capable of high-speed switching. Governing this key metric is the reverse-transfer capacitance – also known the capacitance between the gate and the drain – that impacts the mirror period required to charge the capacitance between the gate and drain.

Conventional VJFETs are held back by a high reverse-transfer capacitance, associated with opposing placement of gate and drain electrodes. But we have recently addressed this issue with a ground-breaking refinement to the device: the addition of a *p*-GaN shield on a normally-off GaN VJFET that's grown on a native substrate (see Figure 1 for details of its structure).

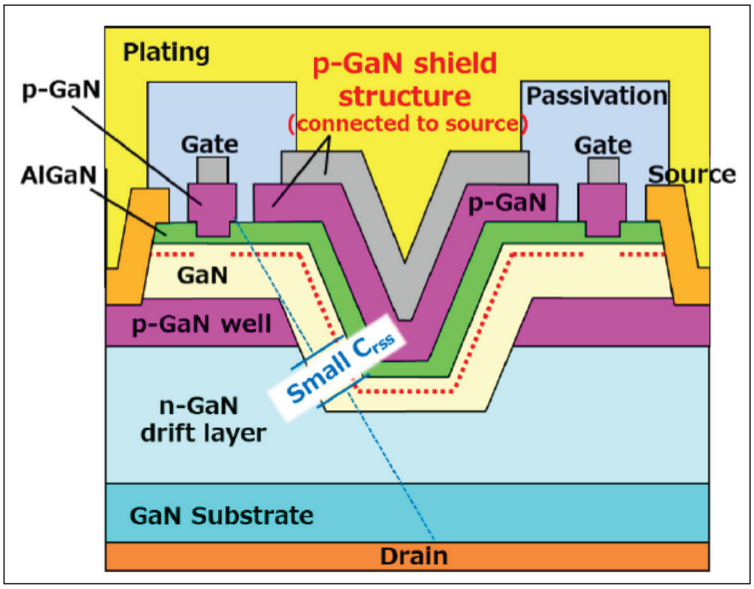
Simulation insights

To evaluate and understand the benefits and implications of this device, we have simulated its performance. This is benchmarked against the conventional VJFET that combines normally-off operation with a low on-resistance, and features a re-grown *p*-GaN gate/AlGaN/GaN structure formed on a V-groove.

Our novel VJFET has a strategically introduced *p*-GaN shield over the V-groove that is at the same potential as the source. For this device, the gate is formed on the plane separately from the *p*-GaN shield structure. This design has a far lower reverse-transfer capacitance than its conventional counterpart, thanks to effective shielding between the gate and drain by the *p*-GaN well and the *p*-GaN shield structure.

Simulations of both forms of VJFET show that our refinement to this transistor delivers a substantial reduction in the reverse-transfer capacitance over a wide range of drain-source voltages. Over a range of voltages up to 500 V, our device has a reverse-transfer capacitance that's well below a picofarad, while its conventional counterpart has a value of many tens of picofarads. These simulations also show that shortening the length between the edge of the *p*-well and the *p*-GaN gate enables an additional reduction in the reverse-transfer capacitance.

Our simulations have also revealed that with our VJFET with a *p*-GaN shield, the thickness of the AlGaN barrier has a strong influence over normally-off operation and a low on-state resistance. By modelling this device, we have determined the profile of the conduction band and the density of the 2DEG, for a gate-source voltage of 0 V. This work shows that in the gate region complete depletion is realised with a 20 nm-thick $Al_{0.2}Ga_{0.8}N$ barrier layer. Meanwhile, in the slanted region, an $Al_{0.2}Ga_{0.8}N$ barrier that's 80 nm-thick enables the



➤ Figure 1. Panasonic's vertical JFET features a *p*-GaN shield structure that enables superior switching, thanks to a reduced reverse-transfer capacitance.

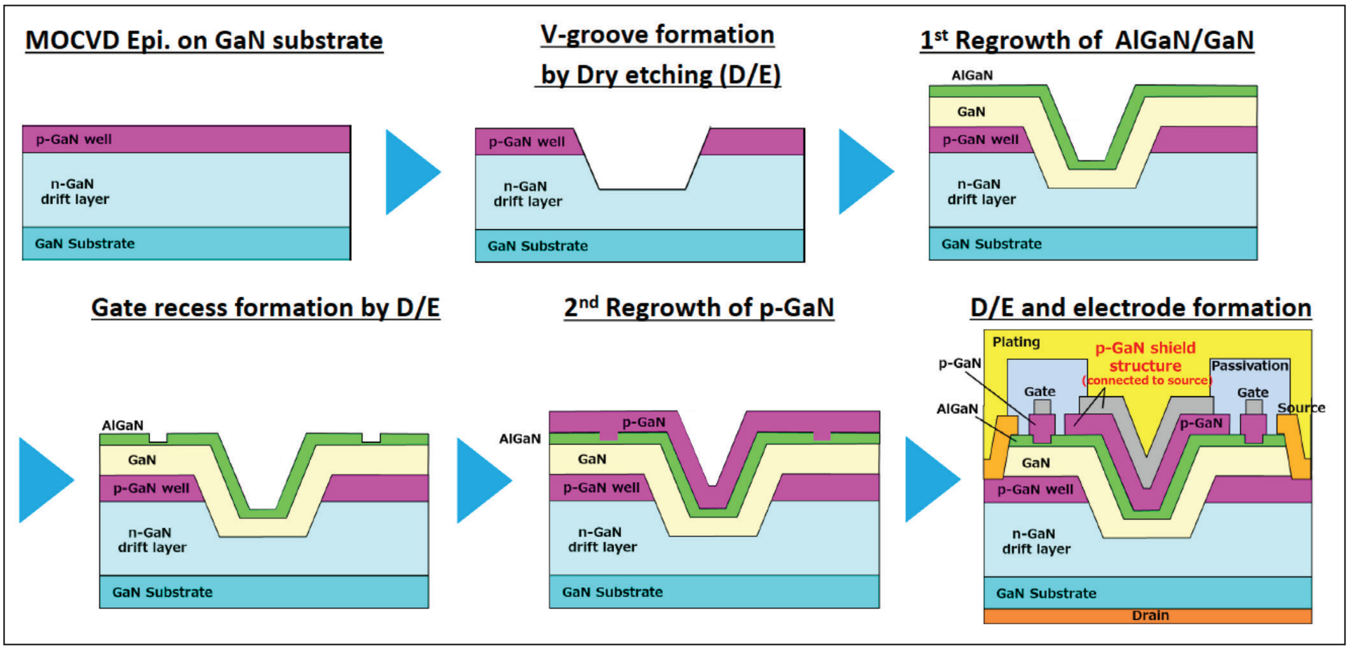


Figure 2. Panasonic's process for the fabrication of its vertical JFET with a *p*-GaN shield structure.

formation of a high-density 2DEG and a low channel resistance.

Further findings from our simulations reveal that as well as slashing the reverse-transfer capacitance, our V-shaped *p*-GaN shield structure in the V-groove suppresses the off-state leakage current by relaxing the electric field at the *p*-GaN well's edge, where there is damage caused by the dry etching process. This work has also determined that increasing the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield reduces the electric field strength at the edge of the *p*-GaN well, thanks to a relaxing of the electric field by the *p*-GaN shield structure. There is a price to pay for this benefit, however: as the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield extends, there is an increase in the electric field strength at the bottom of the *p*-GaN shield.

Based on these findings, we have concluded that experimental investigations are needed to optimise the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield while realising a low off-state leakage current.

Device fabrication...

Fabricating our novel VJFETs began by loading bulk GaN substrates into an MOCVD reactor and depositing a 7 μm-thick silicon-doped GaN drift layer with a carrier concentration of 1.3 x 10^{16} cm^{-3}, followed by a magnesium-doped *p*-GaN well with a carrier concentration of more than 1.0 x 10^{19} cm^{-3}. With this heterostructure, the blocking voltage should exceed 900 V.

The next steps in the fabrication process involved etching V-shaped grooves in the epiwafer with an inductively coupled plasma, and re-growth of $Al_{0.2}Ga_{0.8}N$ and GaN. We varied the thickness of the $Al_{0.2}Ga_{0.8}N$ barrier layer from 50 nm to 80 nm, and employed a thickness for this ternary of 20 nm under the gate, realised by partial removal with inductively coupled plasma etching.

To complete the fabrication of our VJFETs, we added a *p*-GaN epilayer, and selectively etched this to form the gate and *p*-shield structure. We then applied a selective etch to the $Al_{0.2}Ga_{0.8}N$/GaN/*p*-GaN well to form the source electrode. The final device features a Ti/Al source electrode, a Pd/Au gate electrode, a *p*-GaN shield electrode, and a Ti/Al/Ti/Pt/Au electrode on the backside of the GaN substrate (see Figure 2 for an overview of the fabrication process, and Figure 3 for a scanning electron microscopy image of our device).

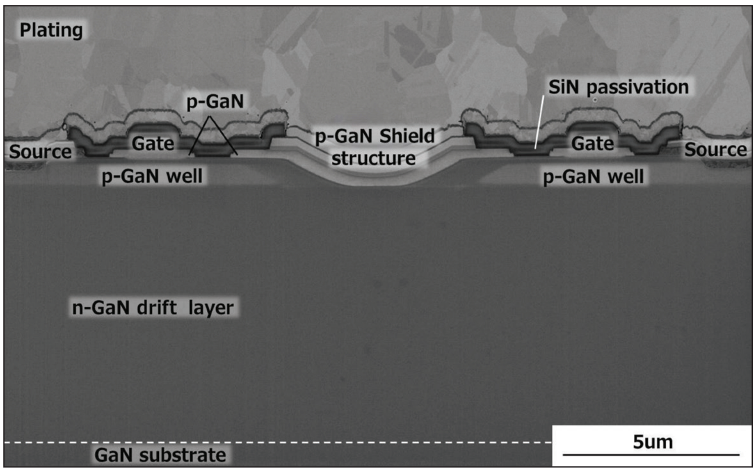
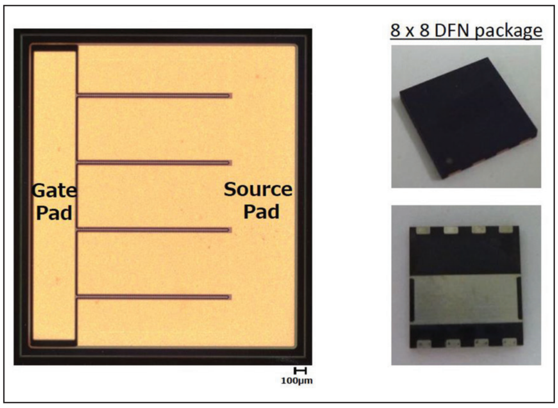


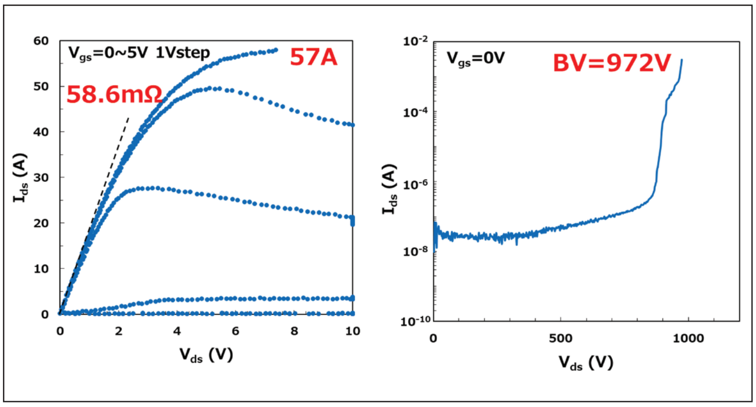
Figure 3. A scanning electron microscopy image of a *p*-GaN shield vertical JFET.

... and characterisation

Electrical measurements of our transistors, which have an active area of 0.002 mm^2, reveal a threshold voltage of 1.5 V. The on-state resistance decreases with the thickness of the barrier layer, and for an 80 nm thickness, the product of



➤ Figure 4. Designed for high-current operation, this *p*-GaN shield vertical JFET has a chip size of 2.9 mm by 2.6 mm.



➤ Figure 5. On-state (left) and off-state (right) DC output characteristics of the *p*-GaN shield vertical JFET.

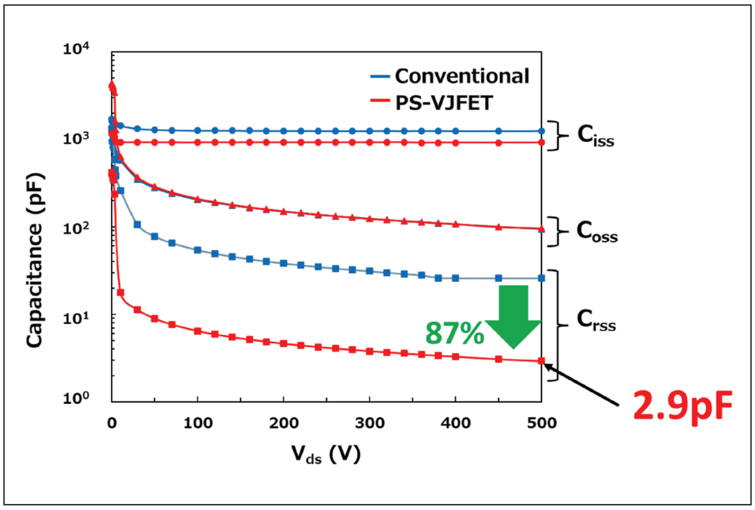
on-resistance and area is 1.23 mΩ cm². Plots of off-state leakage current at a range of drain-source voltages show that the leakage is far less when the distance between the bottom of the *p*-GaN well and the bottom of the *p*-GaN shield is 200 nm, rather than 0 nm or 400 nm. For the 200 nm distance, the drain-source voltage has little impact on leakage current, which is around tens of microamps per square centimetre.

We have also evaluated a 2.9 mm by 2.6 mm *p*-shield VJFET designed for high-current operation (see Figure 4). This device has a maximum drain current of 57 A, an on-state resistance of 58.6 mΩ, and a breakdown voltage of 972 V (see Figure 5). Encouragingly, at a drain-source voltage of 500 V, the reverse transfer capacitance is just 2.92 pF – that's less than one-eighth of the value for its conventional counterpart (see Figure 6). In addition, the input capacitance is lower, thanks to the reduced gate area.

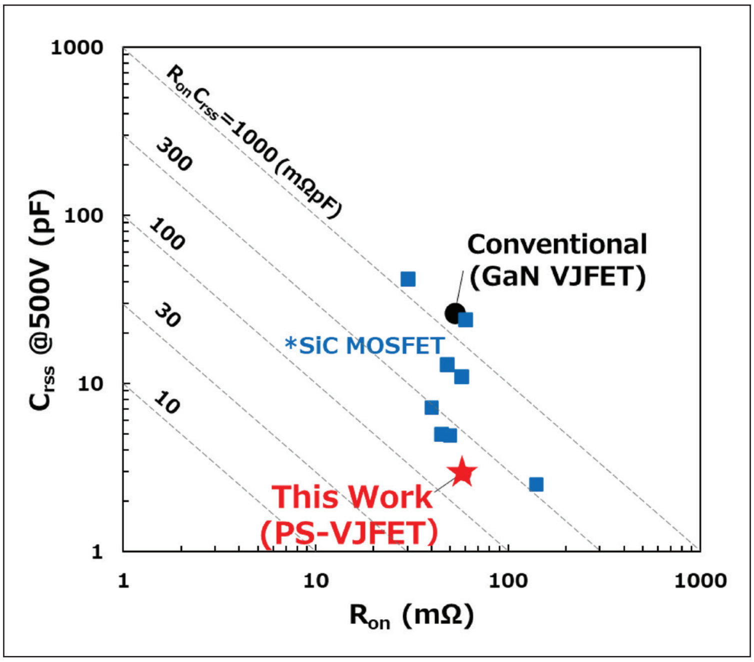
A key figure-of-merit for our *p*-shield VFJET is the product of its on-resistance and its reverse-transfer capacitance. This figure is just 171 mΩ pF, less than that for commercially available SiC MOSFETs (see Figure 7).

Using an inductive load, we have investigated the switching performance of our *p*-shield VJFETs at 400 V and 20 A. Values for turn-on are 14.3 V ns^{-1} and 76.7 V ns^{-1} for our conventional and *p*-shield VJFETs, respectively. The turn-on loss is reduced by 75 percent compared with that for a conventional device.

Based on a wide portfolio of results, we can conclude that our novel VJFETs are promising candidates for serving in applications requiring high powers and high speeds.



➤ Figure 6. The *p*-GaN shield enables a substantial reduction in reverse-transfer capacitance.



➤ Figure 7. Benchmarking the Panasonic *p*-GaN shield vertical JFET against its conventional counterpart and 650 V SiC MOSFETs, using figures provided by data sheets.

This work was partly supported by 'Project for Acceleration of Social Implementation and Dissemination of Components and Materials for Realizing Innovative CO_2 Emission Reduction' of the Ministry of Environment of Japan.

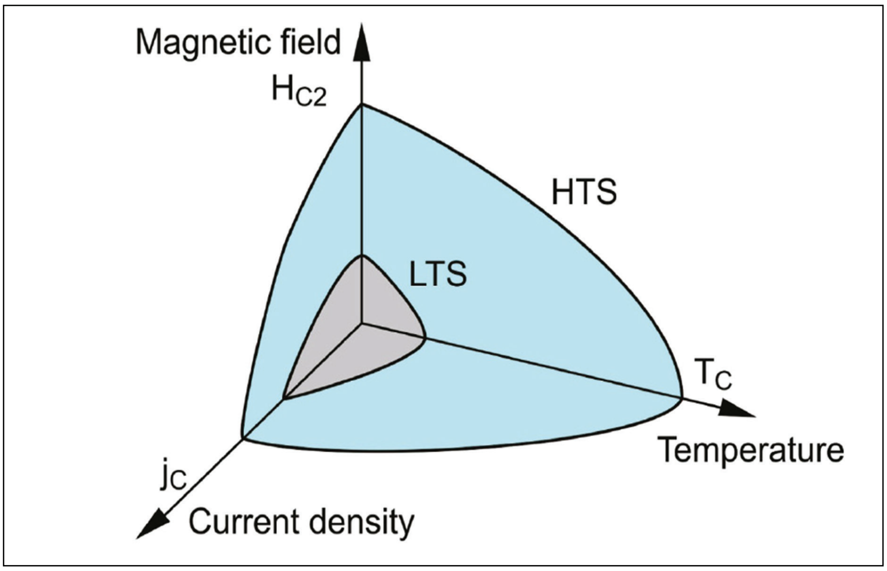
Transforming Data Centres: how 800 VDC and superconductors revolutionise power delivery for high-density AI infrastructure

Efficient, loss-free and scalable power distribution enabled by 800 VDC architecture and high-temperature superconductors

BY VISION ELECTRIC SUPER CONDUCTORS GMBH

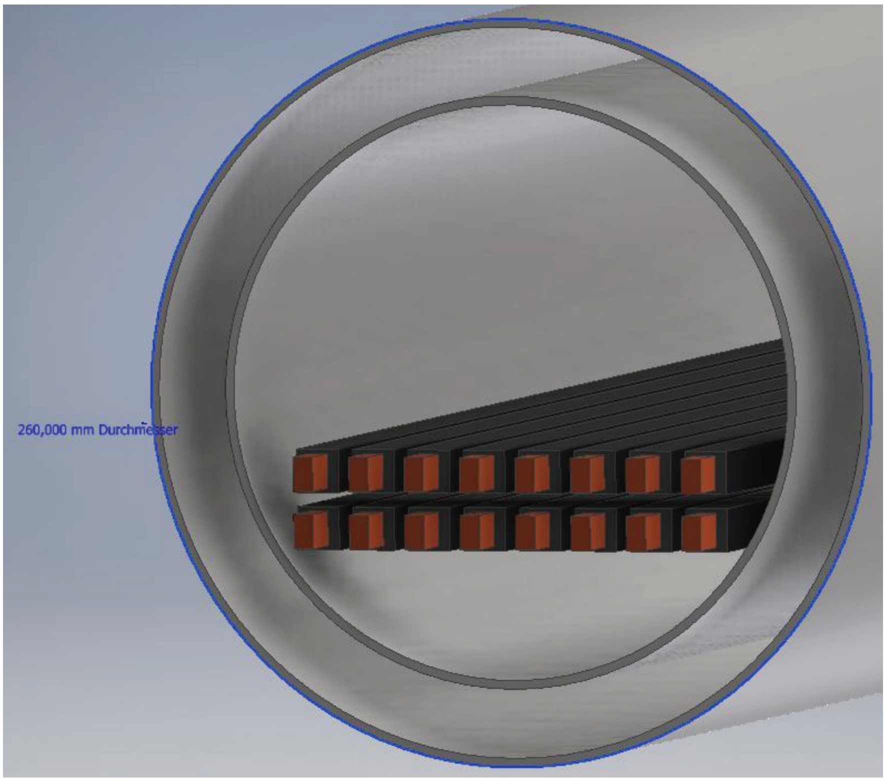
NO MATTER WHAT industry you are a part of it seems that a certain artificial intelligence craze has taken over. It has been a couple years since the breakthrough of the large language models. Open AI's first version of ChatGPT was made available in 2022 and AI's influence is becoming more apparent in everyday life. Search engine queries now have an AI answer attached, while generative AI is creating art and animation. Company AI adoption rate has been steadily increasing too. If you have a complaint or question about a product, it is now increasingly likely that you be talking to an AI chatbot instead of an actual human. Calling a plumber could indeed redirect you to an AI call center.

The AI breakthrough is based on the improvement of the algorithms and neural networks, that allowed for more parallel processes and so more scalable training on larger data volumes. More data equals better models. The growing adoption, the parallelization and need for large amounts of data inference leads us to the projected power demand growth of 165 % by 2030 [source].



➤ **Figure 1.** HTS and LTS operating ranges displayed. HTS can operate at higher temperatures and magnetic fields than their LTS counterparts.

These AI data centers work fundamentally differently than ordinary cloud services: the term AI factory is a new term that is thrown around. Instead of CPUs saving or loading cat pictures, GPUs either train, infer or generate according to prompts. The basic workload can be broken down into tokens, basic input and outputs of an AI model. The processing speed and efficiency of the tokens is key to the economic performance of the data center and like many processes, there



➤ Figure 2. 800 V power distribution using superconductors. Each conductor can carry up to 11 kA.

are economies of scale prevalent. For this reason, chip producers are pushing the processing power of the GPU racks into the MW range. Considering that a "normal" rack uses around 20 kW, this is power increase requires a total overhaul and rethinking of the data center architecture for the power supply.

Why 800 VDC is the new basis for AI factories

Supplying 20 kW with standard three-phase low-voltage AC is straightforward and widely practiced. However, delivering 1 MW at low voltage is simply not feasible. Cable cross-sections become too large, the systems too heavy, and the infrastructure too costly. In addition, IT hardware ultimately runs on DC, so rectification is required, further increasing size, losses, and expense. Although the concept of DC-based data centers dates back to the early 2000s and several have been built. The high rack powers of today are pushing data-center designers and hyperscalers to reconsider it.

An 800 V DC rack architecture is being investigated, operating either at 800 V or ±400 V. The higher voltage reduces the required current, and DC systems inherently exhibit lower effective resistance than AC systems due to the absence of the skin effect. As a result, less copper is needed for power distribution. Major hardware manufacturers are developing power shelves that step down the 800 V supply to hardware-level voltages such as 48 V. This approach reduces copper usage, increases efficiency, and simplifies the overall system.

The 800 V rack addresses the question of how power will reach the rack, but the design of the distribution system remains unclear. Typically, operating voltage is increased to deliver more power; however, bringing medium voltage into a data center creates additional space and regulatory challenges. This is where superconductors come in.

Increasing efficiency with high-temperature superconductors

Superconductors don't possess a DC electrical resistance. The current that can flow through them is dependent on the operating temperature and the magnetic field they are placed in.

Due to the absence of electrical resistance and ability to carry extremely high current densities, superconductors make it entirely feasible to transmit megawatts of power at low voltage. 50 MW at 800 V would require an operating current of around 60 kA, a realistic current for superconductors.

To date, low-temperature superconductors (LTS) have been widely used in MRI systems, particle accelerators, and fusion reactors as high-field magnets. High-temperature superconductors (HTS) are replacing LTS now. HTS can be cooled with liquid nitrogen, making them much more economical, as liquid nitrogen is much cheaper and helium.

With growing industrial adoption, they are also beginning to replace conventional copper and aluminum conductors. High voltage HTS cables have been recently tested for a distribution grid application in Munich, Germany in the SuperLink project and last year currents up to 200 kA were demonstrated in an industrial environment in an aluminum plant for the Demo200 project.

In short: superconductors extend the advantages of the 800 VDC rack architecture all the way to the data center's power distribution. Smaller, efficient conductors simplify the electrical infrastructure. The medium voltage distribution is exchanged for stainless-steel pipes (cryostats, 200 mm in diameter) that are thermally insulated and contain a liquid nitrogen circulation that keeps the conductors at operating temperature of around -200 °C. While decreasing the weight and size of the power distribution, operating costs are also reduced: 90% of the electrical losses are saved.

The main alternative to superconductors is water-cooled cables or busbars. Water can dissipate heat far more effectively than air, allowing these systems to operate at much higher current densities. It makes sense to use these for short distances inside a POD, bridging the distance between sidecar and rack, however, using them to distribute power in the data center is costly: much higher electrical losses and the need for active cooling to remove the additional generated heat.

At a current density of around 10 A/mm^2, a data center operating at 10 MW would incur nearly 1,000 kW of electrical losses for 100 m of water-cooled cables.

Using an HTS conductor, the electrical losses can be eliminated completely. Instead, only the heat leak into the system must be cooled away, around 1-2 W/m and the cooling for the initial current lead and sidecar terminations, around 100 W/kA in total for both. Also, no additional cooling is needed in the white space

What superconductivity in the data center looks like

What does the superconducting system look like? A superconducting power distribution system is built around compact, extremely high-current conductors cooled to cryogenic temperatures. Figure 2 shows 8 pairs of HTS conductors inside a cryostat. Each conductor can carry up to 11 kA, enough to supply a POD with 10 MW, or 20 rack at 500 kW.

The inner and outer stainless-steel pipe make up the cryostat, the thermal insulation. Between the two pipes a vacuum in created to limit the heat transfer. Inside the inner tube liquid nitrogen is circulated, with a temperature range of 68 to 77 K (-205 to -196 °C). It absorbs the heat entering the system from the outside.

At each end of the system, termination units interface with the rectifier on the input side and the POD sidecar on the output side. These terminations cool the conductors and provide the electrical and mechanical connection to the rest of the power infrastructure.

The technology is currently being engineered, with several components such as the sidecar terminations, DC-DC converters, and protection systems requiring further optimization. Vision Electric Super Conductors is actively developing the needed HTS-busbars, current leads and sidecar terminations.

Thanks to industry groups such as Current/OS and the Open DC Alliance (ODCA), direct-current applications are becoming better developed, more widely understood, and increasingly adopted. The Open Compute Project is also advancing 800 VDC system components and standards that will accelerate DC power distribution.

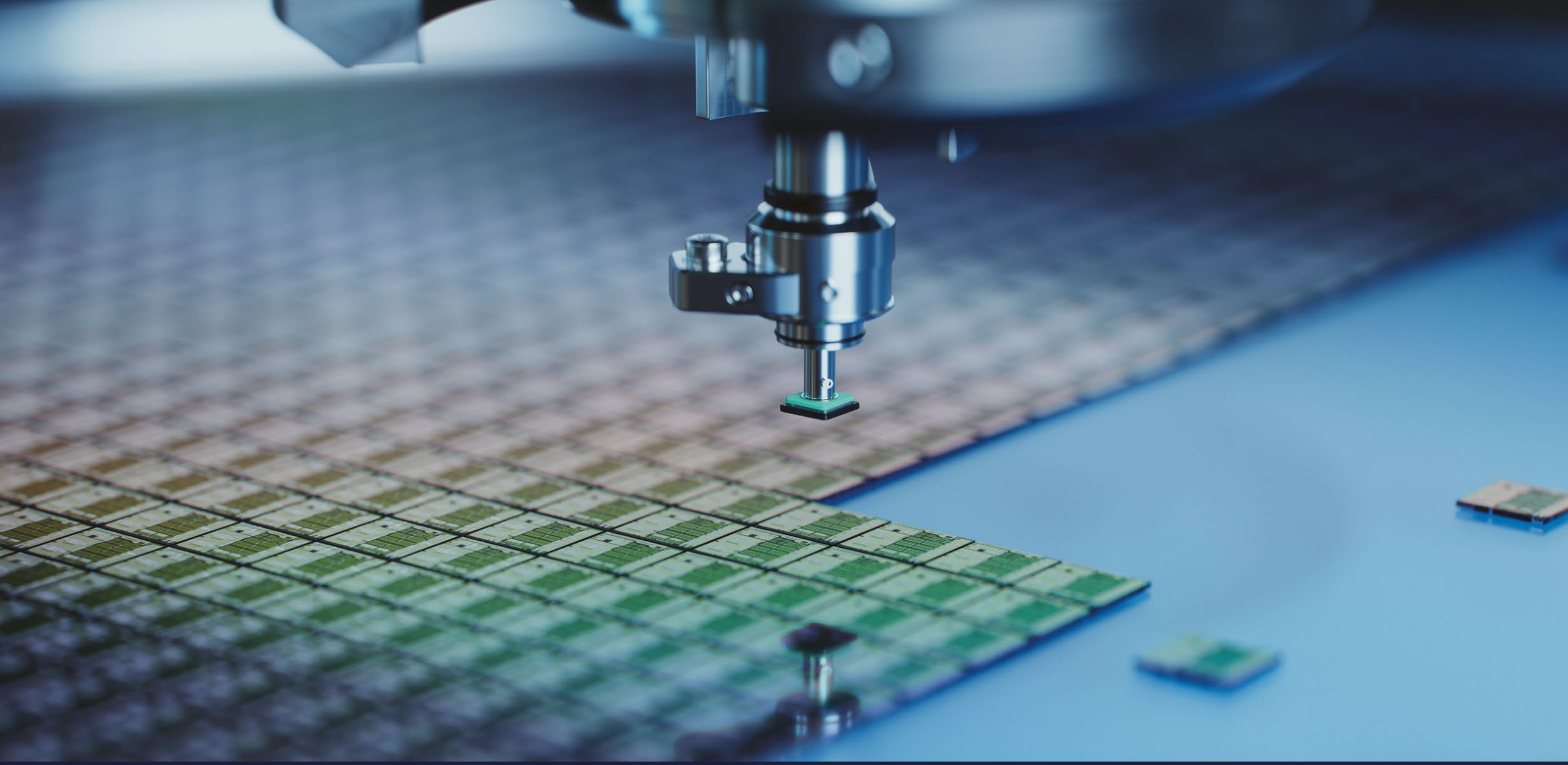
Energy savings on a massive scale

While the superconducting system is more complex than its copper-based counterpart, it compensates with lower operational costs, fewer voltage transformations, and significantly more space-efficient conwductors. For the data-center industry, the potential energy savings are substantial: even a 5% reduction in installed power translated into gigawatts saved across the globe.

However, before widespread adoption, data-center operators must be fully convinced of the reliability of cryogenic systems. In an industry driven by redundancy, uptime, and strict outage targets, reliability matters more than efficiency.

> While the superconducting system is more complex than its copper-based counterpart, it compensates with lower operational costs, fewer voltage transformations, and significantly more space-efficient conductors. For the data-center industry, the potential energy savings are substantial

Future trends point toward HTS as the conductor of choice. HTS tapes continue to decrease in cost while improving in performance and current-carrying capability. In contrast, c opper prices have been rising steadily and are expected to rise further as global demand for electrical infrastructure grows. Given the economic advantages and the trend toward ever-higher power densities, the question is no longer if superconductors will be adopted, but when.



Advancing 800 VDC architectures with all-GaN technology

As AI workloads scale to megawatt racks, GaN's blend of performance, efficiency, and manufacturability establishes it as the indispensable technology for powering the next generation of AI infrastructure

BY PENGJU KONG, JIANPING WANG, YI SUN, JINGHUA NI, HUAIFENG WANG, YULIN CHEN, CHARLES BAILLEY AND LEI WU

THE EXPLOSIVE growth of AI computing is driving a fundamental transformation in data center power architectures. NVIDIA's next-generation AI factories adopt an 800 V direct current (800 VDC) backbone to deliver megawatt-scale power with high efficiency and reliability. This shift imposes stringent demands on power devices. While silicon MOSFETs are approaching their physical limits, GaN high-electron-mobility transistors (HEMTs) offer superior performance with ample headroom for further innovation. In response to such demand, Innoscience is collaborating with NVIDIA to develop All-GaN power conversion solutions from 800V to GPU, which supports the 800 VDC power architecture. This paper analyzes the architectural challenges of 800 VDC AI systems and demonstrates why GaN's device physics, scalability, and manufacturing maturity make it the optimal and future-proof choice for AI-era power delivery.

Introduction

An 800 VDC architecture enables the safe and efficient delivery of megawatt-scale rack power with reduced material and infrastructure costs. However, a major challenge remains: delivering such high power to GPUs within the limited space of a rack server. Advances in power device technology are critical to overcoming this challenge.

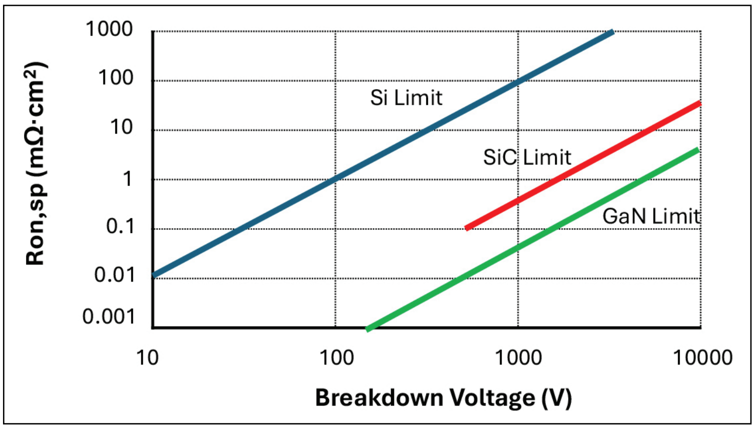


Figure 1. Physical Limits of Power Device RON,SP [1]

Challenges for power conversion to GPU in 800 VDC systems

Compared to a 54 V busbar, power conversion from 800 VDC to the GPU presents significant challenges. The high voltage conversion ratio traditionally results in larger, less efficient power converters—an unacceptable tradeoff for AI systems. Breakthrough technologies are required. Devices must switch at least 10× faster to shrink magnetics and

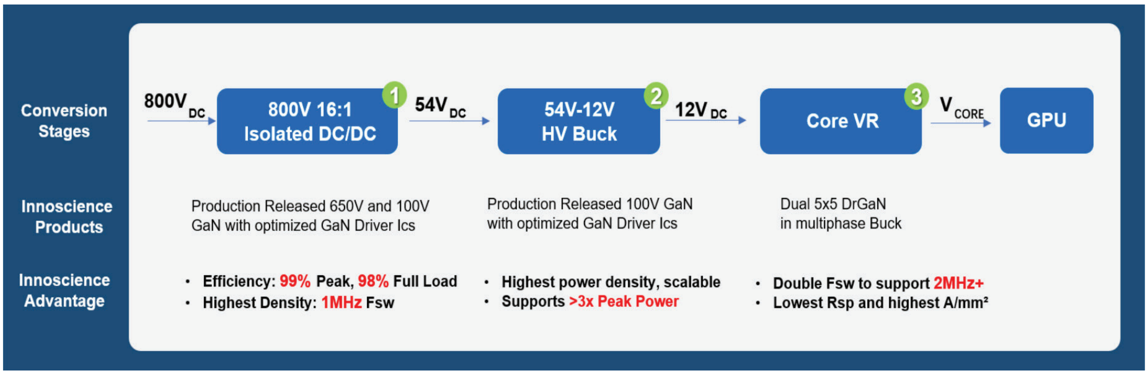


Figure 2. 800 VDC to GPU Power Conversion Block example and Innoscience All-GaN Solution [2]

capacitors, while also minimizing conduction loss to reduce heat and conserve valuable board area.

The advantage of GaN power device

GaN's intrinsic material and device-level properties uniquely position it to meet NVIDIA's demanding 800 VDC requirements.

The core strength of GaN HEMTs lies in their GaN/AlGaN heterostructure, which creates a two dimensional electron gas (2DEG) at the interface. This structure provides exceptionally high electron mobility and low parasitic capacitance, yielding reduced gate charge and superior switching performance. It eliminates minority carrier recombination issues, such as the reverse recovery losses seen in silicon MOSFETs, making GaN particularly effective at high switching frequencies. Additionally, GaN's wide bandgap supports high breakdown voltages with low specific on-resistance. These material advantages translate directly into lower on-resistance, reduced gate charge, and superior efficiency, enabling higher-frequency operation and greater power density in converters. Figure 1 [1] compares the RON,SP (Ron times die size) of Si, SiC MOSFET and GaN. GaN shows significantly lower physical limit compared to Si and SiC MOSFETs, indicating its superior advantage in reducing device size and parasitic capacitance at the same Ron.

Among GaN technologies, GaN-on-Silicon stands out as the most mature and cost-effective solution. It leverages well-established silicon manufacturing processes and equipment, enabling high-volume scalability while maintaining a competitive cost structure compared to conventional silicon power devices.

The All-GaN solution for 800 VDC and its performance advantage

A three-stage power conversion example, shown in Figure 2, illustrates the advantages of the All-GaN solution for 800 VDC. Innoscience provides a broad portfolio of GaN products spanning 15 V to 1200 V ratings, enabling an All-GaN architecture for power conversion from 800 VDC to the GPU. Specifically, the recommended component selection is listed in Table 1 below.

800V – 54V using 650V and 100V GaN HEMT

The 800 V to 54 V conversion stage is unique to 800 VDC architectures, making board size reduction a top priority. Achieving this requires both compact magnetics and high-performance power devices.

	800V – 54V	54V – 12V
Topology	3-Level LLC	Multiphase Buck
GaN HEMT	Primary: 650V/35mΩ or 20mΩ in TOLT INN650TP030C/INN650TP020E Secondary: 100V/1.5mΩ or 1mΩ in 5x6 INN100EBD018DAD/INN100EBD010EAD	High side: 100V/2.5mΩ in 5x6 INN100EBD025DAD Low side: 100V/1.5mΩ in 5x6 INN100EBD018DAD
GaN Driver	INS1001	INS2001

Table 1. Topology and Component Selection for 800 VDC Power

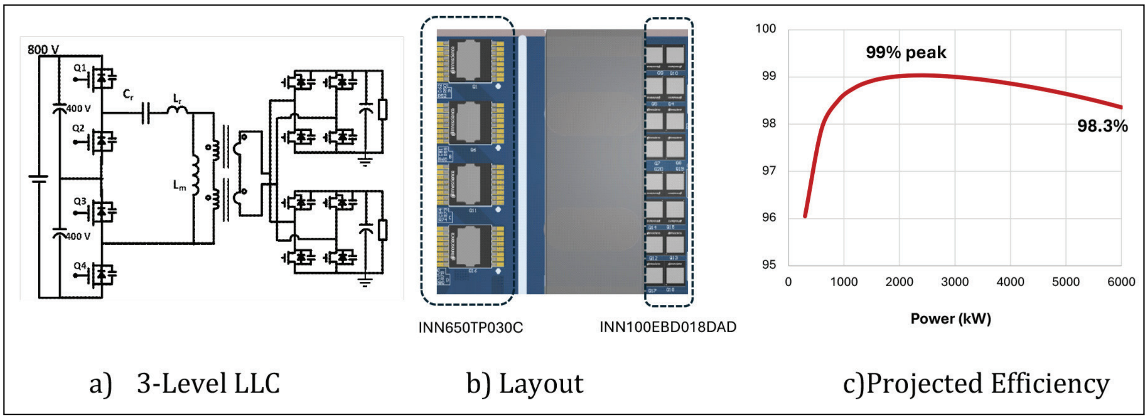
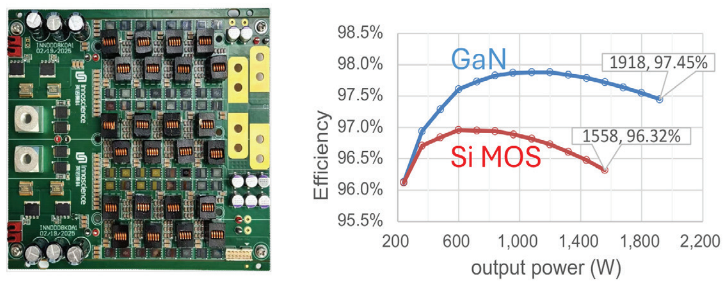


Figure 3. 800V – 54V Conversion with Innoscience All-GaN solution



1) 12kW PDB prototype 2) Efficiency comparison

Figure 4. 54V – 12V 12kW Power Distribution Board (PDB) with INN100EBD018EAD and INN100EBD025EAD

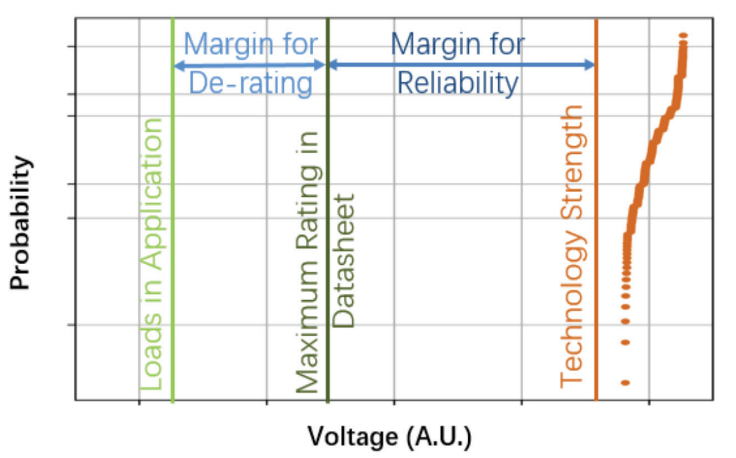


Figure 5. 54V – Load and Stress of drain voltage for an Innoscience technology platform.

Figure 3 demos the ultra-compact design of a 6kW 800V – 54V converter (power devices and transformer portion only) with targeted 99% peak efficiency using Innoscience All GaN solution.

The benefits of such solutions include:

- Innoscience 650V GaN HEMTs feature ultra-low input capacitance (Qg) and driving voltage, achieving merely 20% driving loss of a SiC MOSFET, which enables 1 MHz switching without driver overheating.
- Low Qg further minimizes the turn off loss (Eoff), allowing easier thermal handling at high switching frequencies.
- Innoscience 100V GaN HEMTs are available in 5x6 dual-cool packages as low as 1mΩ (INN100EBD010EAD), which reduce component count and board area by 50% compared to the 2mΩ silicon MOSFETs.
- Low Qg of 100V GaN cuts driving losses by 80%, further supporting high-frequency designs with compact auxiliary supplies.

54V – 12V using 100V GaN HEMT

Converting 54 V to 12 V using traditional 100 V silicon MOSFETs incurs significant reverse recovery and drive losses, forcing designers toward complex and expensive resonant converters. In contrast, Innoscience's 100 V GaN HEMTs eliminate reverse recovery loss and reduce drive loss by 80%, enabling simple multiphase buck converters to achieve higher power density.

Figure 4 demonstrates a 12kW Power Distribution Board with Innoscience GaN HEMTs. Comparison between GaN and Si MOSFET was done on the same board as they are pin-2-pin compatible. Efficiency of GaN is more than 1% higher, allowing more power delivery. At the same 115C operation temperature, GaN delivers 1.918kW while Si MOSFET only achieves 1.56kW.

12V – 1V using 25V GaN HEMT

Innoscience has demonstrated that 30 V GaN HEMTs deliver higher efficiency than the most advanced DrMOS solutions at 2X switching frequency.

Next-generation low-voltage GaN devices will further reduce Rds(on) and switching loss, driving even greater power density for conversions such as 12 V–1 V or 6 V–1 V. 5.

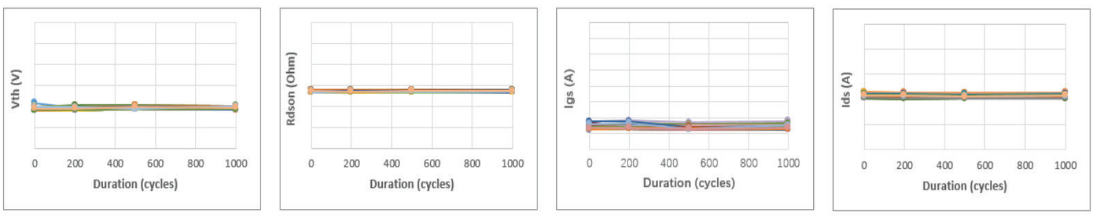
Maturity and reliability of GaN power devices

GaN power device industry has now reached its time for mainstream adoption and readiness for AI era, with almost all major power semiconductor suppliers offering GaN solutions.

Innoscience has been the pioneer and in the leading position with its world's largest manufacturing capacity, accumulated shipment and reliability data,

Figure 6. Electrical measure-ments and destructive physical analysis (DPA) data throughout the 1000-cycle TCoB test

Test Item	Package Type	Sample Size	Duration	Result	
				Electric	DPA
Board Level TC (3.1 mm thickness 16 layers)	EN-FCLGA	77ea	1000Cycle	Pass (no parametric drifts)	Pass (no solder crack or device crack)



as well as the understanding on how to make a reliable GaN product for AI and EV applications.

Manufacturing capacity and accumulated shipment

Innoscience is the world's first and largest 8-inch GaN-on-Si IDM, with capacity projected to reach 72,000 wafers per month by 2027. To date, the company has shipped over 1.5 billion GaN power devices at 95%+ yield, across consumer, industrial, datacenter, and automotive markets, consistently delivering low defect rates and proven reliability.

Reliability

Innoscience ensures GaN product reliability through rigorous design practices and extensive qualification. Each technology platform maintains significant margin between actual operating loads and fundamental device limits. For example, destructive breakdown voltage testing confirms wide safety margins, as illustrated in Figure 5. Beyond industry-standard qualifications, Innoscience extends test times (2000-hour HTOL), broadens conditions (175oC), and expands test categories to define reliability boundaries. Datacenter-specific tests, such as 1000-cycle temperature cycling on 16-layer, 3.1 mm boards, show zero degradation nor delimitation, as illustrated in Figure 6. With millions of device hours logged across wafer, chip, package, and system-level tests, Innoscience has built the industry's most extensive GaN reliability database, enabling continuous improvement of device robustness.

Category	Test Item	Device hour/Tested Sample size
Wafer level Reliability	BVD/TDDB/ BVG/TDSB	More than 1,200,000 ea
Chip Level Reliability	HTGB	42,659,088 Device hours
	HTRB	36,851,952 Device hours
	LTGB	7,360,584 Device hours
	LTRB	3,823,680 Device hours
Package-Level Reliability	THB(H3TRB)	26,138,784 Device hours
	HAST	5,203,584 Device hours
	TC	48,136,450 Device hours
	TS	1,674,288 Device hours
	IOL	1,123,000 Device hours
	HTS	5,750,640 Device hours
	LTS	1,471,176 Device hours
System-level	Buck/Boost/QR/ LLC/Always on	More than 5,000 test rounds (calculated the system sets)
	H-bridge	
Supporting equipment	Reflow	132,263 ea
	CSAM	620,516 ea
	X-RAY	406,482 ea

Table 2. EDevice hour/ sample size that has been tested in the reliability laboratory

Innoscience is the world's first and largest 8-inch GaN-on-Si IDM, with capacity projected to reach 72,000 wafers per month by 2027

Innoscience has built a reliability laboratory capable of supporting high volume mass production. Table below shows the device hour and tested sample size that has been completed in the past 3 years. This high throughput helped Innoscience accumulate the largest GaN reliability database in world and continues to improve its reliability to a higher level.

Conclusion

The adoption of 800 VDC architectures in AI data centers represents a decisive step toward higher efficiency, scalability, and future readiness. An All-GaN approach delivers minimal conduction and switching losses across the full 800 V to GPU conversion path, enabling compact, thermally manageable designs with fewer components.
As AI workloads scale to megawatt racks, GaN's unmatched blend of performance, efficiency, and manufacturability establishes it as the indispensable technology for powering the next generation of AI infrastructure.

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