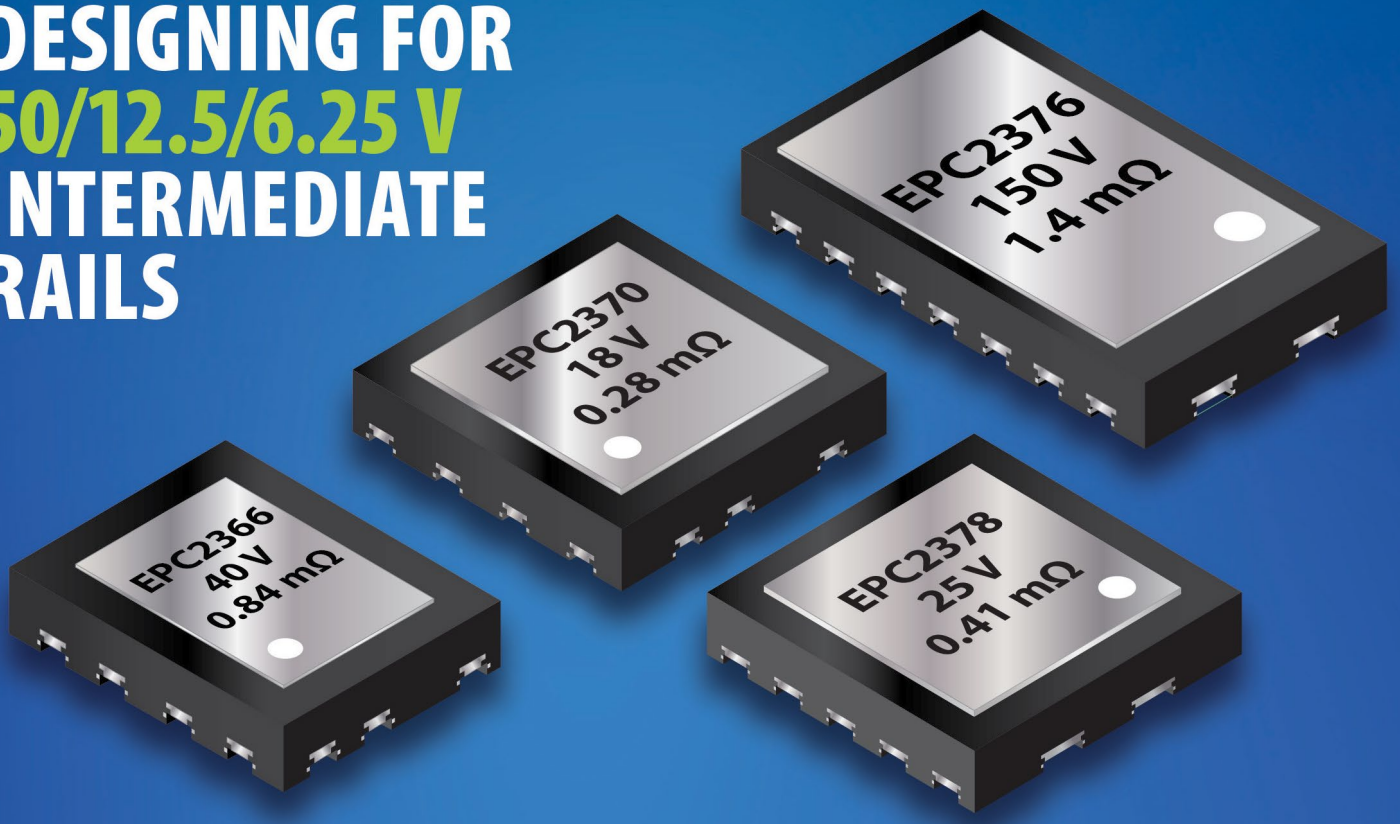
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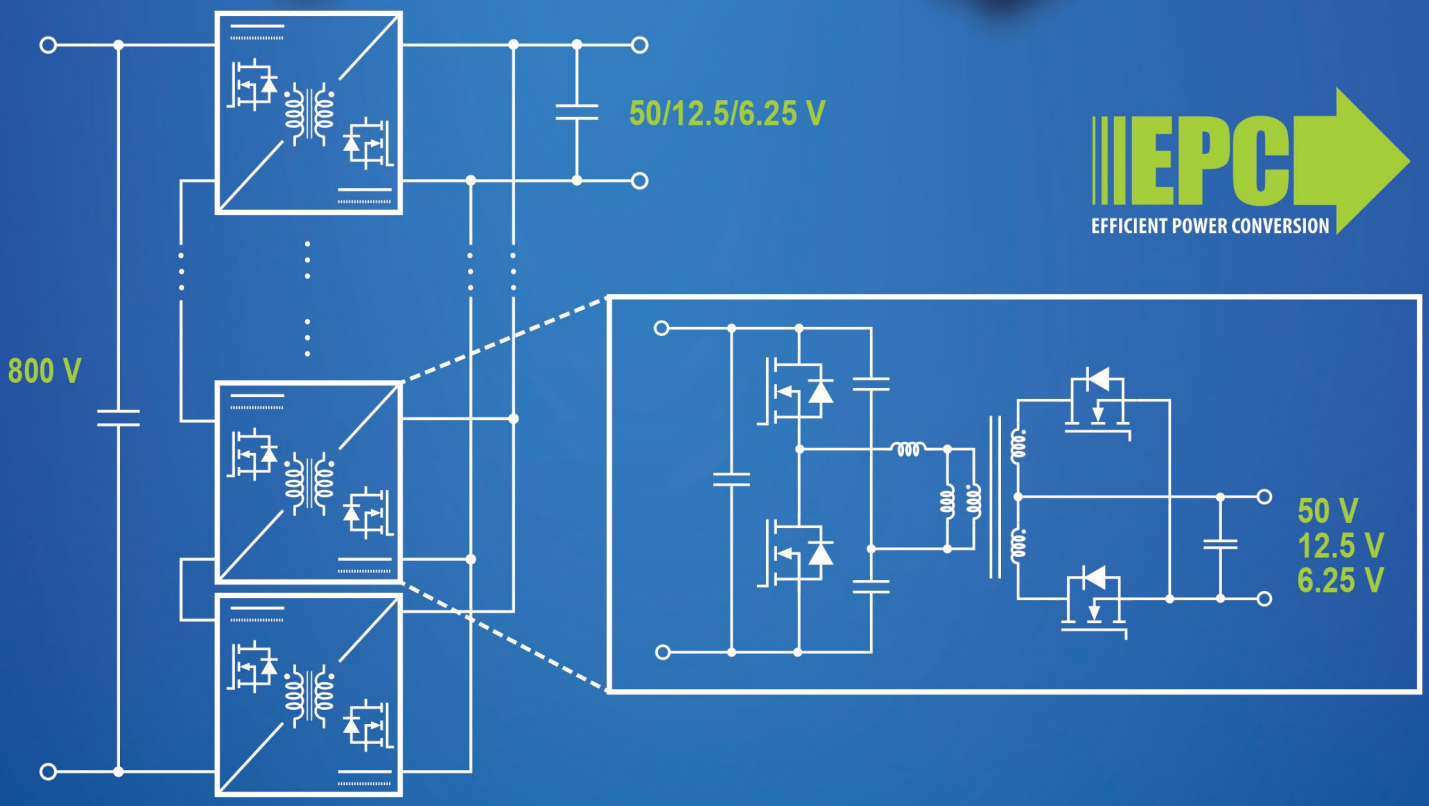
ISSUE VII 2026

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DESIGNING FOR 50/12.5/6.25 V INTERMEDIATE RAILS





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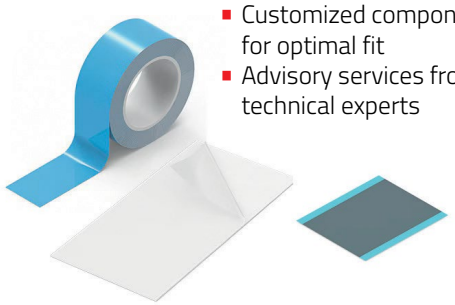
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VIEWPOINT

BY PHIL ALSOP, EDITOR



The new power electronics race is about more than devices

FOR years, power electronics has measured progress through lower losses, higher efficiencies, greater power density and the shift from silicon towards wide-bandgap technologies. But this month's announcements, research and partnerships reveal a deeper change.

The next phase of power electronics competition is no longer simply about who builds the best device. It is about who controls the ecosystem.

Europe's ReSiLient project, backed by Horizon Europe funding and joined by SEMI, is not focused on a new MOSFET or converter topology. Instead, it addresses raw materials. Silicon and silicon carbide are strategic resources, as critical to semiconductor competitiveness as lithography tools or fabrication capacity. Without resilient access to materials, technological leadership becomes vulnerable.

Navitas and GlobalFoundries are celebrating domestically manufactured GaN devices in the United States. Nexperia and Tata Electronics are partnering to establish new manufacturing routes in India. SemiQ is strengthening European distribution channels. These announcements show an industry reorganising around supply-chain security, regional resilience and geopolitical certainty.

In power electronics, the value chain has become as important as the technology. The boundaries of innovation are also shifting.

For decades, packaging was treated as following device design. Onsemi's Embedded Power Platform challenges that assumption by making the silicon wafer itself part of the package architecture. Similarly, STMicroelectronics is shrinking complete inverter modules, while AOS is redesigning thermal pathways through top-side-cooled MOSFETs.

Power electronics is moving from component optimisation towards system optimisation. Electrical, thermal and mechanical design can no longer be treated as separate disciplines.

The AI infrastructure boom is accelerating this convergence. Data centres are becoming major drivers of power semiconductor innovation, rivaling electric vehicles as a source of technical demand.

Consider the collaboration between Infineon and SolarEdge on solid-state circuit breakers for high-voltage DC data centre architectures. Or Navitas' acquisition of Claros to bring voltage regulation closer to the processor package itself. These developments highlight a growing industry consensus: computing is not the only bottleneck in AI infrastructure.

Power delivery has become a limiting factor.

As rack power rises, traditional approaches to power conversion, protection and distribution are struggling to keep pace. Power engineers face challenges similar to those confronting cooling specialists. More compute means more power. More power creates more heat. More heat requires new architectures.

Whether it is Onsemi's claims of dramatically improved thermal performance through advanced integration, AOS' focus on thermal dissipation, or the growing use of wide-bandgap devices in data centres and electric vehicles, heat remains the constant adversary.

Some of the most encouraging developments are in research laboratories.

This issue features examples across the innovation spectrum: Ga_2O_3 MOSFET development in the United States, a novel NbAlN material platform in Japan that dramatically increases carrier density in GaN heterostructures, new approaches to SiC wafer processing in China and EPFL's intrinsic polarisation superjunction concept that pushes GaN voltage capabilities towards levels previously regarded as unattainable.

Many breakthroughs may require years before commercialisation. Collectively, they show that power electronics innovation remains exceptionally healthy.

The diversity of approaches is notable. The industry is no longer betting on a single technology pathway. SiC continues gaining momentum. GaN keeps advancing into higher-power applications. Ga_2O_3 remains an intriguing long-term prospect. Materials scientists continue discovering entirely new mechanisms for improving device behaviour and manufacturing efficiency.

The technology roadmap is broadening.

That may be the key takeaway from this month's news.

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SEMI joins EU ReSiLient consortium

Joins project to tackle Europe's critical dependence on imported SiC and silicon raw materials

SEMI, the industry association for semiconductor and electronics design and manufacturing, has joined the EU ReSiLient project consortium to help fortify Europe's semiconductor ecosystem and improve supply chain resilience.

Co-funded by the European Union under the Horizon Europe program, ReSiLient — Innovative Primary Substitution and Secondary Valorisation Routes for Europe's Silicon and SiC Semiconductor Raw Material Value Chains — is a 48-month, €9.57 million project bringing together 18 partners from across nine European countries.

"Securing Europe's access to silicon and SiC is no longer simply a materials challenge—it is a strategic industrial imperative," said Laith Altimime, president, SEMI Europe. "ReSiLient tackles the critical raw-material bottlenecks at the very foundation of Europe's semiconductor and power-device industries. SEMI Europe is committed to ensuring these results reach the industrial stakeholders who can turn them into action. By strengthening the resilience of Europe's raw-material supply, ReSiLient will help reinforce Europe's semiconductor ecosystem, competitiveness, and global leadership."

The project addresses four objectives:
Supply chain resilience:
Map critical dependencies across the Si and SiC value chains, validate domestic and secondary feedstocks including olivine, aplite and Si-rich industrial waste streams, and align new production routes with the Critical Raw Materials Act, European Chips Act, Net-Zero Industry Act and EU Emissions Trading System.

Sustainable production at scale:
Develop and demonstrate two integrated production routes: a primary route based on domestic mineral sources, and a secondary route based on industrial by-products and waste streams, using hydrometallurgical leaching, agglomeration, hydrogen plasma refining and carbothermic conversion to deliver metallurgical-grade silicon and high-purity silicon carbide at pilot scale.

Semiconductor qualification:
Validate the purity and performance of project-produced Si, MG-Si and SiC for real semiconductor manufacturing, including Czochralski crystal growth and SiC boule production, benchmarked against commercial feedstock by end users STMicroelectronics Silicon Carbide AB and Infineon Technologies.

Competitiveness and exploitation:
Benchmark both production chains against conventional baselines on cost, carbon footprint and supply security, and define clear commercial pathways, Intellectual Property Rights (IPR) frameworks and regulatory compliance strategies for scale-up.

As part of SEMI's participation, SEMI Europe will serve as lead partner for Work Package 8 (WP8), Social Acceptance, Dissemination, Communication and Standardisation.



A new way to shape SiC semiconductor crystals?

Chinese team turns friction heat into a chemical cushion

SiC IS capable of handling enormous voltages, but shaping the raw ingots into mirror-smooth wafers can shatter the surface with microscopic cracks that can cause microchips to fail.

In the *International Journal of Extreme Manufacturing*, Shuiquan Huang at Yanshan University, Han Huang at Sun Yat-Sen University and colleagues claim to have flipped this manufacturing curse on its head, using the destructive friction heat of high-speed cutting to trigger a chemical reaction that lets diamond tools carve brittle crystals as smoothly as butter.

Grinding discs embedded with diamond grit can flatten SiC quickly, but the violent impacts leave behind deep sub-surface fractures. To buff out those cracks, manufacturers must rely on sluggish chemical slurries that take days to smooth away a single millimeter of material. Earlier strategies tried softening the crystal first using high-power lasers, which risk warping the wafer with excessive heat, or corrosive chemical oxidisers that gradually destroy the precision grinding machines themselves.

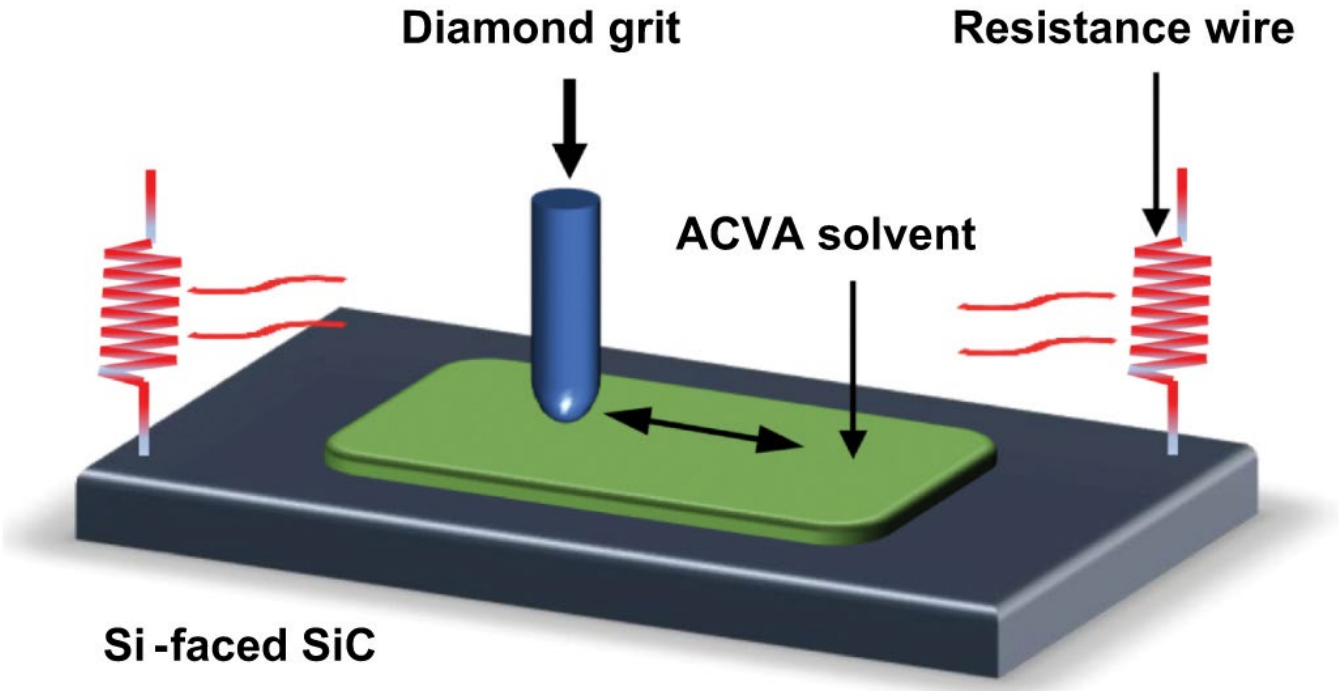
Huang's team have tackled the problem by turning to a clever chemical additive borrowed from 3D printing: a non-toxic azo compound called ACVA dissolved in an everyday liquid polymer coolant. This is described in the paper 'Atomic-scale damage control via thermochemical mechanical grinding induced amorphisation of single crystal SiC'.

Under resting conditions, the mixture behaves like standard industrial lubricant. But the moment a diamond grit strikes the wafer, the intense micro-contact friction instantly raises the localised temperature exceeding 45°C. This brief flash of heat causes the additive to split into fleeting free radicals, which immediately attack the top layer of silicon atoms.

Atomic simulations and electron microscopy reveal that this targeted reaction temporarily rewires the crystal surface, creating a pliable and 10nm-thick skin of amorphous silicon oxycarbide. Instead of splintering under mechanical force, this glassy top layer behaves like a sacrificial molecular cushion, deforming smoothly under the diamond grit and nearly doubling the crystal's crack-free cutting depth from 29 nm to 51 nm.

The resulting process slashes subsurface crystal defects to a depth of only 70nm while entirely preventing hidden microcracks. The researchers say that allowing chipmakers to bypass laborious intermediate polishing stages and jump straight from fast grinding to final finishing promises to streamline SiC manufacturing.

The researchers note that the immediate next step is scaling the chemistry to run on commercial 8-inch wafer processing equipment and engineering closed-loop fluid recycling systems for large-scale industrial foundries.



Onsemi introduces 'Embedded Power Platform'

New architecture uses silicon wafer as the package for combining electrical, mechanical and thermal design

ONSEMI has unveiled the Embedded Power Platform (EPP), a new architecture that uses the silicon wafer itself as the package to enable a more integrated approach to power system design.

Designed to be scalable, EPP brings electrical, mechanical and thermal design together from the outset to help customers achieve higher power density, improve system performance and accelerate development in AI, electrification and autonomous applications.

"For decades, the semiconductor and the package have been treated as separate technologies. EPP changes that by making the silicon itself part of the system architecture," said Hassane El-Khoury, president and CEO of Onsemi.

"EPP brings together advanced semiconductor technologies, manufacturing and system-level optimisation into a common architecture that can evolve alongside future innovations. This approach will redefine how power systems are built and create a new foundation for AI infrastructure, electrification and automation."

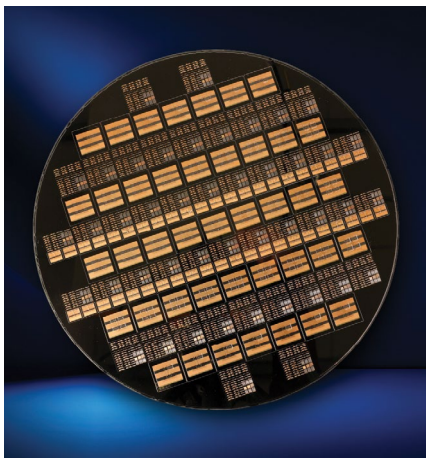
Onsemi describes EPP as 'reimagining' the package from passive housing into an active contributor to system performance. By using the silicon wafer itself as the package, EPP enables the seamless integration and interconnection of silicon, SiC and GaN technologies within a highly integrated wafer-level architecture.

Multiple devices, including FETs, drivers and controllers, can be embedded together in a single package and co-optimised for electrical, thermal and mechanical performance. This enables complete power-system co-design, allowing electrical, thermal and mechanical characteristics to be evaluated and optimised together from day one. The result is higher power density, improved system performance, reduced development complexity and faster time-to-market.

EPP uses Onsemi's standard 12-inch silicon wafer manufacturing capabilities, that apply mature semiconductor design tools, wafer-level manufacturing and advanced simulation capabilities to power-system integration, helping improve performance while accelerating innovation.

Subaru Corporation is one of the first early engagement partners for EPP, working with Onsemi to evaluate how the platform could support future electrified vehicle architectures. Through the collaboration, Subaru will gain early access to engineering samples, simulation models and technical expertise as the companies explore opportunities to improve vehicle performance, streamline development and accelerate innovation.

Onsemi says that EPP replaces that sequential model with a common platform that can be co-designed, co-simulated and co-optimised. This approach is designed to help customers achieve three to five times higher power density, depending on the application. Other benefits include development cycles as little as four months; better thermal performance and heat dissipation; reduced electrical losses through lower parasitic inductance; and the ability to scale a common architecture across power levels, device types, applications semiconductor technologies.



As an example, an early EPP-based solid-state circuit-breaker design for AI was approximately 50 percent smaller and 20 percent cooler than existing designs, according to Onsemi. By reducing packaging overhead and using the full EPP footprint to conduct heat, EPP can support more compact power systems, improve thermal management and enable greater power density in AI infrastructure.

Electric vehicle traction inverters are often constrained by efficiency losses, thermal limitations, development complexity and system size. Onsemi says EPP addresses these challenges with up to four times higher power density and 15 percent lower power losses compared to conventional approaches, enabling smaller, lighter and more efficient inverter designs.

In addition, its scalable architecture supports a single inverter platform spanning low-end to high-end vehicle applications, allowing automakers to reuse a common design across multiple vehicle models and power classes. This approach can reduce R&D and manufacturing costs, accelerate qualification and development cycles, improve vehicle range or lower system costs, and help bring new vehicle programs to market faster.

EPP is expected to begin sampling in 2026 with strategic customers and ecosystem participants across automotive and AI applications.

HiEFFICIENT: Powering tomorrow's EVs for a greener Europe

Two years on, the HiEFFICIENT project continues to drive a new era of electromobility

FROM 2021 to 2024, the EU-funded HiEFFICIENT project worked to advance one of the EU's key goals: making transport sustainable for all Europeans.

Its focus was electromobility, and, more specifically, creating more powerful and reliable power electronic solutions for electric vehicles based on wide-bandgap semiconductors. Now, HiEFFICIENT has transitioned from research to tangible industrial deployment, its innovative technologies paving the way for cost-effective, eco-friendly next-generation vehicles.

Since 2024, HiEFFICIENT partners have built on the collaboration fostered during the project, devoting themselves to generating market-ready technologies, follow-up projects and commercialisation activities across Europe. Advancements in semiconductor embedding in printed circuit boards for automotive converters have attracted strong interest from European and Asian OEMs and Tier 1 suppliers.

The development of a highly compact, bidirectional 22 kW on-board charger achieving over 97 percent efficiency has strengthened industrial relevance, leading to follow-up projects, collaborations with OEMs and suppliers, and the new EU-funded project HiPower 5.0. Launched in 2025, HiPower 5.0 is expected to lead to even more efficient, compact and reliable solutions.

Further advances include enhanced motor control algorithms – with improvements in efficiency, noise, vibration and harshness – and simulation/thermal models. These are already being used in demonstrator vehicles and delivered to customers as product-level solutions.

A new dual-inverter family and an updated demonstrator have also been developed for emerging applications such as electric vertical take-off and landing aircraft, opening new business opportunities.

Belgium-based EMAXSIS, an advanced tech spin-off taking advantage of HiEFFICIENT results, specialises in edge-monitoring technologies and Internet of things software solutions that make the power electronics in electric vehicles and charging networks safer, more reliable and longer lasting. Also built on project results is a next-generation electric vehicle fast-charging power module that is being industrialised, targeting over 98 percent efficiency, full bidirectionality and high-volume production. Last but not least, the next generation of the 100 V GaN half-bridge solution developed during HiEFFICIENT has now been completed and is currently being tested by key customers before entering the market.

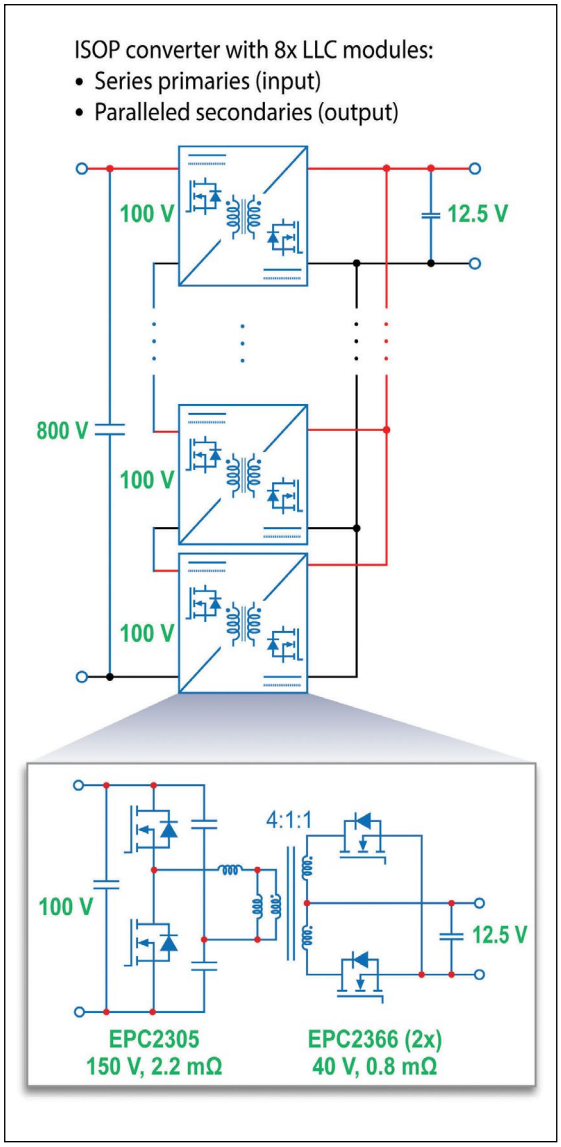
"EU funding was pivotal to HiEFFICIENT's success, acting as the primary enabler for both technical innovation and cross-sector collaboration," comments Christoph Abart, senior program manager at AVL List GmbH, a mobility technology company that coordinated HiEFFICIENT.



800 V_{DC} to AI server board power architecture: Designing 50 V, 12 V, and 6 V intermediate rails

Three GaN-based ISOP converter designs demonstrate how 800 V_{DC} AI rack power can be efficiently stepped down to 50 V, 12.5 V and 6.25 V, achieving peak efficiencies above 98%.

BY ALEX LIDOW, CEO, EFFICIENT POWER CONVERSION,
ALEJANDRO POZO, DIRECTOR OF APPLICATIONS ENGINEERING, EFFICIENT POWER CONVERSION,
IONEL "DAN" JITARU, CEO, ROMPOWER ENERGY SYSTEMS



➤ Figure 1: A block diagram showing an ISOP converter with eight stages. The inset shows the LLC converter in greater detail.

THE INDUSTRY shift toward 800 V_{DC} power distribution for AI server racks requires novel DC-DC converter architectures to optimize delivery. Because of its superior efficiency and power density, the Input-Series-Output-Parallel (ISOP) topology [1,2] is rapidly becoming the standard. This paper analyzes three 800 V-input ISOP converters tailored for 50 V, 12 V, and 6 V nominal output rails. Implementing gallium nitride (GaN) transistors [3] on both the primary and secondary switching sides enables these converters to establish new performance benchmarks for peak and full-load efficiency at each critical voltage node.

The ISOP topology is ideally suited for converting high voltages such as 800 V to much lower voltages due to its multi-stage architecture that enables the use of lower voltage transistors, in this case GaN transistors, switching at higher frequencies with lower overall switching losses and conduction losses than more conventional topologies that require higher voltage devices switching at lower frequencies. Figure 1 is a block diagram showing an ISOP converter with eight stages. Each stage is an LLC converter with an input voltage of 100 V and an output voltage of 12.5 V.

This article evaluates three input series, output parallel (ISOP) converter architectures designed for an 800 V input rail. Each topology incorporates eight LLC resonant converters to generate output levels of 50 V, 12.5 V, and 6.25 V, with power ratings ranging from 11 kW at 50 V to 6 kW at the lower output voltages.

In general, the advantages of the eight-stage converter over other solutions are as follows:

- Better semiconductor devices: lower voltage devices lead to better performance and smaller FET area.
- Simpler transformer design.

- More phases for interleaving, which leads to smaller output capacitance.
- Distributed power losses, which lead to easier and more efficient cooling.

A detailed analysis of efficiency curves and bill of materials (BOM) requirements for each design is included.

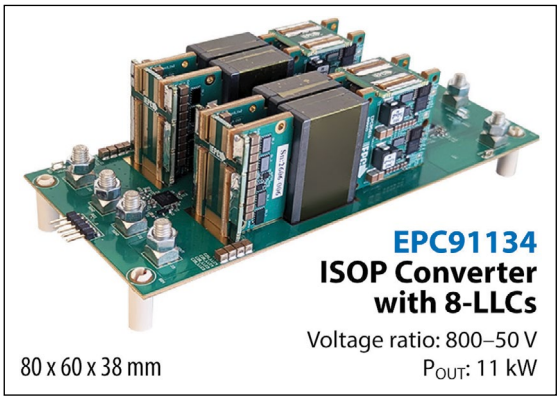
How to get from 800 V to 50 V

An 11 kW, 800 V-to-50 V, 8-module ISOP converter was developed to demonstrate the scalability of ISOP architectures for AI rack power distribution. The converter consists of 8 LLC modules with their inputs connected in series and outputs in parallel. With this arrangement, each module processes 100 V of input voltage and 1.375 kW of output power, while the complete converter handles 800 V and 11 kW. The modularity of the architecture also enables straightforward adaptation to other input configurations. For example, a 5.5 kW, 400 V-to-50 V converter can be implemented by using only four of the eight LLC modules. Similarly, the architecture can be configured for a ±400 V input with a single 50 V output.

Based on the diagram shown in Figure 1, each module uses a primary half-bridge and a center-tap full-wave rectifier coupled through a 1:1:1 transformer for 800V to 50V design. In this configuration, the primary and rectifier FETs experience the same voltage stress and similar RMS currents, allowing the same transistor to be used in both positions. The selected device is a 150 V-rated GaN transistor with a typical on-resistance of 2.2 mΩ in a compact 3 mm × 5 mm PQFN package with an exposed top for efficient top-side cooling. Owing to the single-turn transformer design, two parallel layers can be used for each winding, while using only 6 layers per LLC. An ELP38 core geometry with the ML95S material is used to complete the transformer. The major components used in each LLC module and in the complete converter are listed in Table 1.

This 800 V to 50 V ISOP is an evolution of a previous design [3,4] for a 400 V to 50 V. The earlier design used a four-module ISOP topology in which each module was implemented as a standalone LLC converter. The new implementation combines two LLC modules into a single PCB and magnetic structure, doubling the power density while simultaneously reducing the total volume of the magnetics by approximately half [5]. As shown in the photo of the converter in Figure 2, the 8-module ISOP is built using 4 vertical boards, each integrating 2 LLC modules. A larger horizontal board at the bottom accommodates the controller, digital isolators, and connections between boards.

The LLC converters operate at resonance to maximize efficiency, with a resonant frequency of approximately 1 MHz. The resonant tank and transformer are designed with a frequency-independent gain around the operating point. This characteristic helps maintain balanced input-voltage sharing among all modules in the ISOP configuration, even in the presence of component tolerances [6].

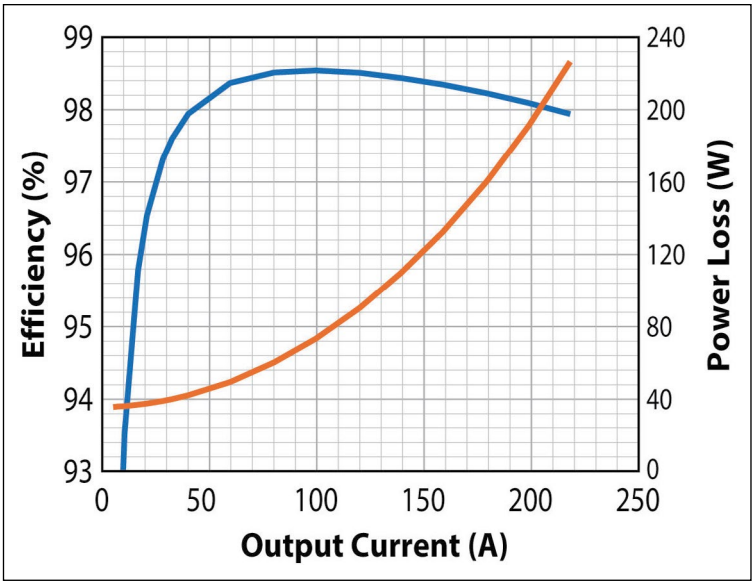


➤ Figure 2: Photograph of the 800 V to 50 V converter showing the integrated two-module PCB and magnetic structure.

COMPONENT	PART NUMBER	DESCRIPTION	QUANTITY	
			Per LLC	Total
Primary FETs	EPC2305	150 V GaN, 2.2 mΩ, 3 x 5 mm QFN	2	16
Secondary FETs	EPC2305	150 V GaN, 2.2 mΩ, 3 x 5 mm QFN	2	16
Primary Gate Driver	MP18831-4A	Isolated Gate Drive 2-ch	1	8
Secondary Gate Driver	LMG1020	Low-Side Gate Driver	1	8
Isolated 5 V/5 V Supply	MIE1W0505BGLVH	5 V/5 V 1 W Isolated DC-DC	1	8
Isolators	ISO7740DWR	Digital Isolator 4-ch	-	2
Controller	DSPIC33CK256MP605	100 MHz 16-bit MCU	-	1
Transformer Core Set	ELP38 + I38	ML95S material	0.5	4

➤ Table 1: Bill of Materials for an 800 V – 50 V, 11 kW ISOP Converter

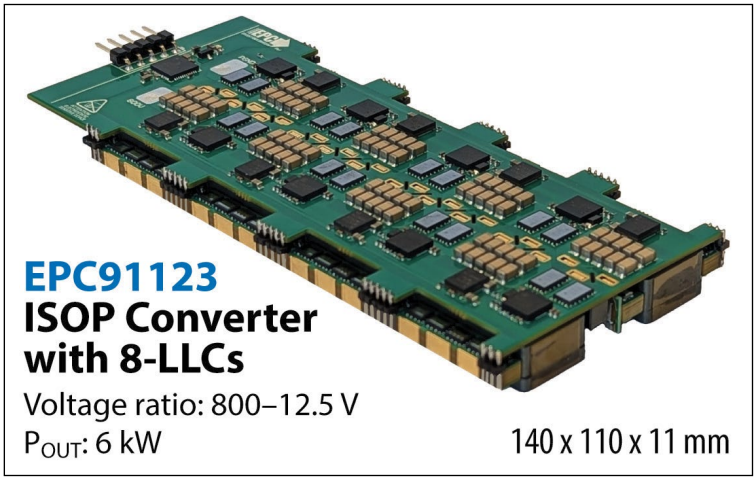
Figure 3 presents the experimental results of the converter, which delivers up to 11 kW to a 50 V load from an 800 V input. The graph shows the full-load efficiency of 98% and peak efficiency of 98.5%.



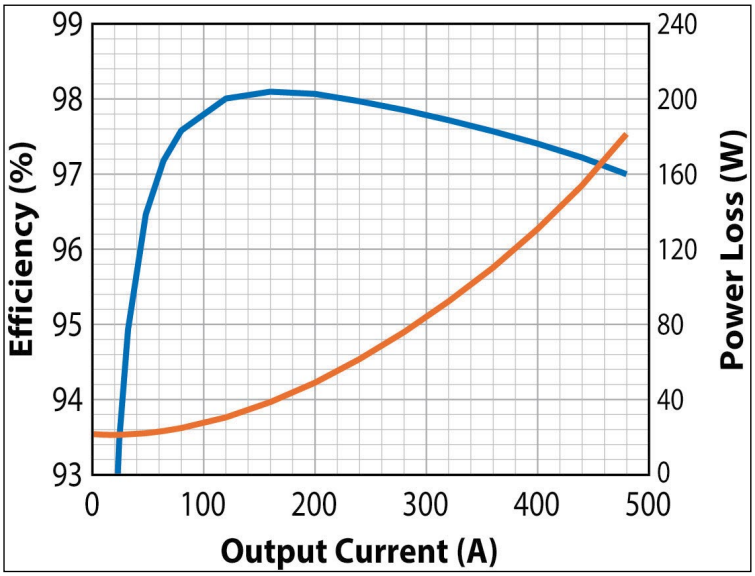
➤ Figure 3: Experimental results of the 800 V to 50 V ISOP converter

COMPONENT	PART NUMBER	DESCRIPTION	QUANTITY	
			Per LLC	Total
Primary FETs	EPC2305	150 V GaN, 2.2 mΩ, 3 x 5 mm QFN	2	16
Secondary FETs	EPC2366	40 V GaN, 0.8 mΩ, 2.6 x 3.3 mm QFN	4	32
Primary Gate Driver	MP18831-4A	Isolated Gate Drive 2-ch	1	8
Secondary Gate Driver	LMG1020	Low-Side Gate Driver	2	16
Isolated 5 V/5 V Supply	MIE1W0505BGLVH	5V/5V 1W Isolated DC-DC	1	8
Isolators	ISO7740DWR	Digital Isolator 4-ch	-	2
Controller	DSPIC33CK256MP605	100MHz 16-bit MCU	-	1
Transformer Core Set	Custom core	MLX9B material	2	16

➤ Table 2: Bill of Materials for an 800 V – 12.5 V, 6 kW ISOP Converter (ABOVE)



➤ Figure 4: Photograph of the 800 V to 12.5 V converter. (ABOVE)



➤ Figure 5: Results of the 800 V to 12.5 V ISOP converter as a function of output current.

How to get from 800 V to 12.5 V

A second 8-module ISOP converter was developed to demonstrate a fixed-ratio, 6 kW, 800 V-to-12.5 V isolated DC/DC converter for direct conversion from an 800 V AI rack bus to a low-voltage, high-current output. The converter implements an overall 64:1 voltage ratio, with each LLC module operating from 100 V to 12.5 V and delivering up to 750 W, corresponding to 60 A of output current. By connecting the inputs of the eight modules in series and their outputs in parallel, the 800 V input is distributed equally across the modules, while the output currents are combined to deliver up to 480 A at 12.5 V.

As in the previous example, each module uses the topology shown in Figure 1, consisting of a primary-side half-bridge and a center-tapped full-wave rectifier on the secondary side. The primary switches selected are EPC2305, the same 150 V-rated ones as in the 800 V to 50 V example. Two EPC2366 GaN transistors are used in parallel on each side of the center-tapped winding as rectifiers. The EPC2366 is a 40 V-rated device with a typical on-resistance of 0.8 mΩ and a 2.6 × 3.3 mm PQFN package with an exposed top, providing low conduction losses while maintaining a compact footprint. Primary and secondary sides are magnetically coupled through a planar transformer with a 4:1:1 turns ratio. The transformer windings are integrated into a 14-layer PCB, using an ER-core geometry fabricated with ML-X9B magnetic material. Table 2 lists the key components used in the design.

Figure 4 shows the converter, illustrating a highly compact mechanical implementation. The complete assembly, including all modules, the controller, and digital isolators with reinforced isolation, occupies less than 5000 mm^2 of PCB area and an overall thickness of only 8 mm. The converter is constructed from two types of PCBs: a large primary power board containing the primary-side GaN FETs, gate drivers, isolated 5 V-to-5 V power supplies, resonant capacitors, and input bus capacitors; and eight transformer boards, one for each LLC module, incorporating the secondary rectifier FETs and gate drivers, transformer windings, and output capacitors. The transformer boards are mounted right beneath the power board. All GaN devices are mounted on the top side of the PCBs, providing direct access to a heat spreader or water-cooled cold plate.

Figure 5 provides experimental results of the converter operating with an input voltage of 800 V and delivering up to 480 A, 6 kW, into a 12.5 V load. Peak efficiency exceeding 98% and full load efficiency of 97% are demonstrated, validating this eight-LLC-module ISOP implementation as a compact, high-efficiency solution for converting an 800 V bus directly to a 12.5 V, high-current output.

How to get from 800 V to 6.25 V

A third 8-module ISOP converter was developed to demonstrate a fixed-ratio, 6 kW, 800 V-to-6.25 V isolated DC/DC converter for direct conversion from an 800 V AI rack bus to a low-voltage, high-current output. The converter implements an overall 128:1 voltage ratio, with each LLC module operating from 100 V to 6.25 V and

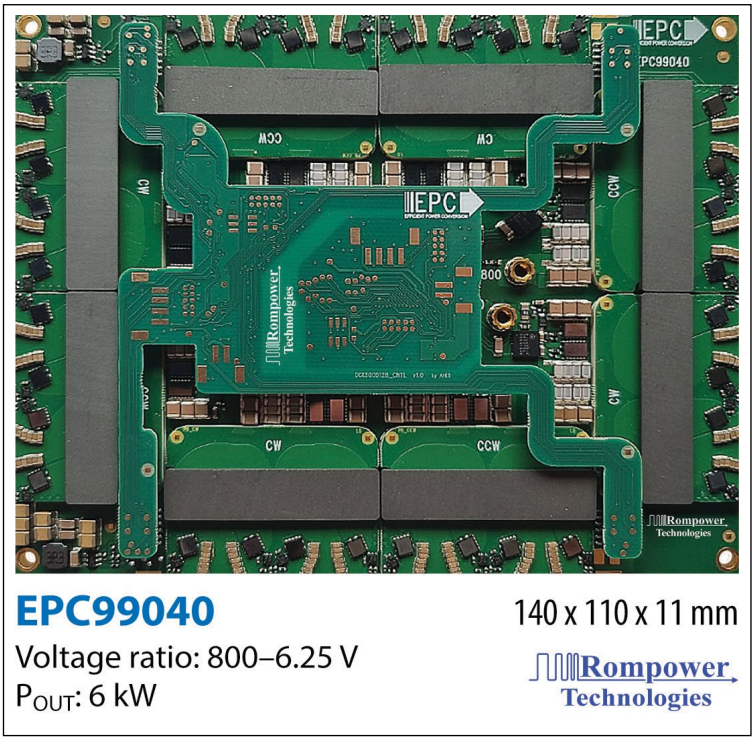
delivering up to 750 W, corresponding to 120 A of output current. By connecting the inputs of the eight modules in series and their outputs in parallel, the 800 V input is distributed equally across the modules while the output currents are combined to deliver up to 960 A at 6.25 V.

As in the previous example, each module uses the topology shown in Figure 1, consisting of a primary-side half-bridge and a center-tapped full-wave rectifier on the secondary side. The primary switches selected are EPC2376, whereas four EPC2370 GaN transistors in parallel on each side of the center-tapped winding are used as rectifiers. The EPC2370 is an 18 V rated device with a typical on-resistance of 0.28 mΩ and a 3.3 × 3.3 mm QFN package with an exposed top, providing low conduction losses while maintaining a compact footprint. Primary and secondary sides are magnetically coupled through a novel transformer [7,8] with an 8:1:1 turns ratio within a 12 PCB-layer with a core geometry depicted in Figure 8, using DMR53 magnetic material. Table 3 lists the key components used in the design.

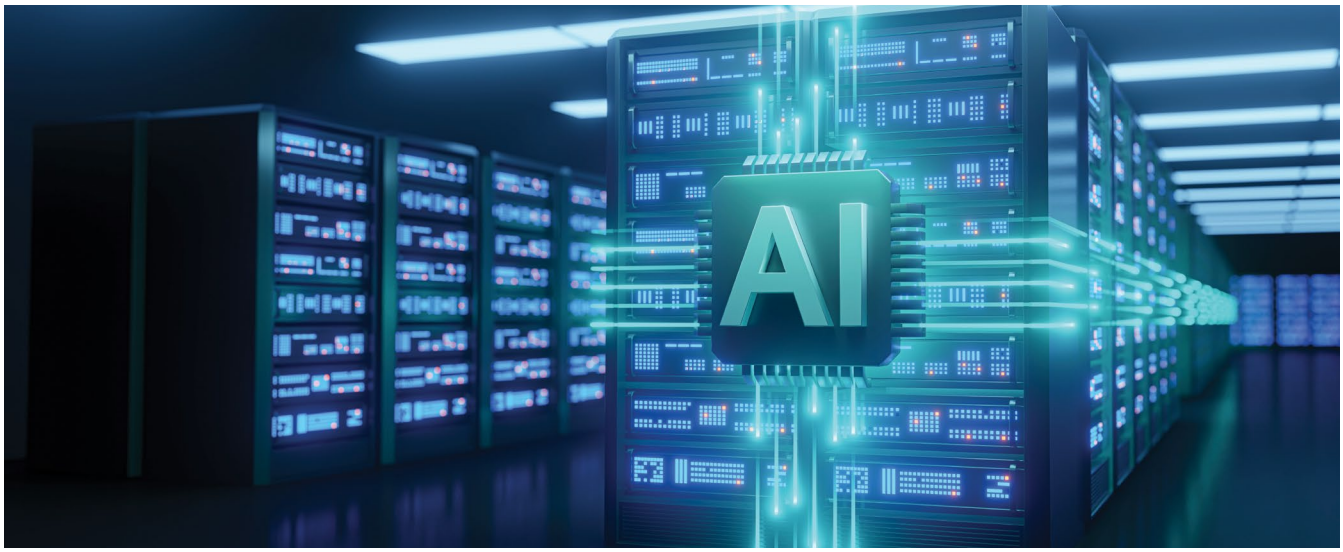
Figure 6 shows the converter, illustrating a highly compact mechanical implementation. The complete assembly, including all the power processing cells, each power processing cell using a novel [7,8] matrix transformer, the controller and digital isolators with reinforced isolation and the bias supply, occupies 15400 mm^2 of PCB area and an overall thickness of 11 mm. The converter is constructed by 8 layers of PCBs having SMD daughter boards, which incorporate additional transformer windings together with key components for the power cells such as synchronized rectifiers, gate drivers, and output capacitors. The 8-layer power board also contains the primary-side GaN FETs, gate drivers, isolated 5 V-to-5 V power supplies, resonant capacitors, and input bus capacitors and half of the transformer windings and output capacitors. The output current is extracted through side plating (edge metallization) distributed along the entire perimeter of the power board and the daughter

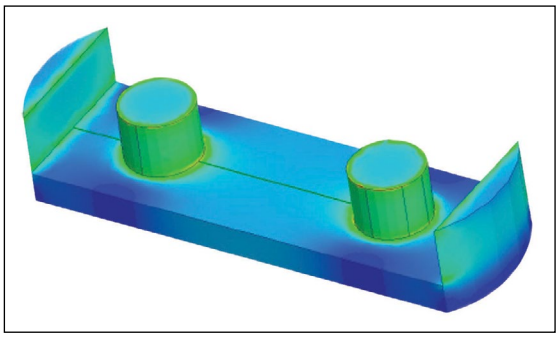
COMPONENT	PART NUMBER	DESCRIPTION	QUANTITY	
			Per LLC	Total
Primary FETs	EPC2376	150 V GaN, 1.4 mΩ, 3 x 5 mm QFN	2	16
Secondary FETs	EPC2370	18 V GaN, 0.33 mΩ, 3.3 x 3.3 mm QFN	8	64
Primary Gate Driver	2EDF7275K	Isolated Gate Drive 2-ch	1	8
Secondary Gate Driver	1EDN7116U	Low-Side Gate Driver	8	64
Isolated 5 V/5 V Supply	UCC33420	5V/5V 1.5W Isolated DC-DC	1	8
Isolators	ISO7721FDWVR	Dig. Isolator 1/1-ch	-	2
Controller	STM32G030F6P6 + GW1N-LV4	64 MHz 32-bit MCU + FPGA	-	2
Transformer Core Set	Custom core	DMR53 material	1	8

➤ Table 3: Bill of Materials for an 800 V – 6.25 V, 6 kW ISOP Converter (ABOVE)

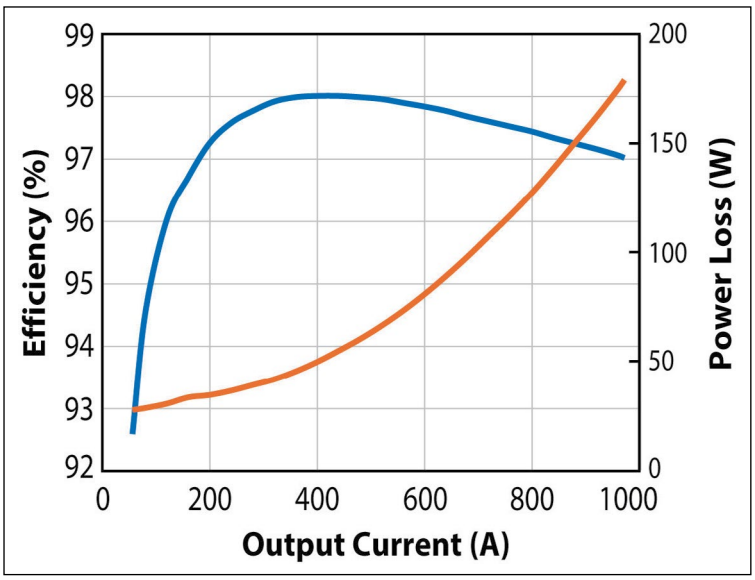


➤ Figure 6: Photograph of the 800 V to 6.25 V converter (ABOVE)





➤ Figure 8: An image of the magnetic core of the matrix transformer [7,8]



➤ Figure 7: Experimental results of the 800 V to 6.25 V ISOP converter as a function of output current.

boards. The output current is supplied by the power cells integrated within eight novel [7,8] matrix transformers strategically distributed around the perimeter of the power board. By positioning the power cells near the current-extraction perimeter, the design significantly reduces the current conduction path impedance and, consequently, the associated conduction losses. This architecture provides a low-impedance current-extraction structure and represents a key differentiating feature compared with competing solutions.

Figure 7 provides experimental results of the converter operating with an input voltage of 800 V and delivering up to 960 A, 6 kW, into a 6.25 V load. Peak efficiency exceeding 98% and full load efficiency of 97% are demonstrated, validating this eight-LLC-module ISOP implementation as a compact, high-efficiency solution for converting an 800 V bus directly to a 6.25 V, high-current output.

Summary

Three highly efficient, cost-effective power solutions converting 800 V_{DC} to lower voltages for next-generation AI servers demonstrate exceptional power density and efficiency. By utilizing low-voltage, ultra-low GaN transistors switching at approximately 1 MHz within an eight-stage input series-output parallel (ISOP) topology, these converters achieve peak efficiencies exceeding 98% and full load efficiencies above 97%. These results establish the architecture among the most efficient methods for stepping down 800 V rails to power leading-edge AI processing platforms.

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DS6 Pulsar



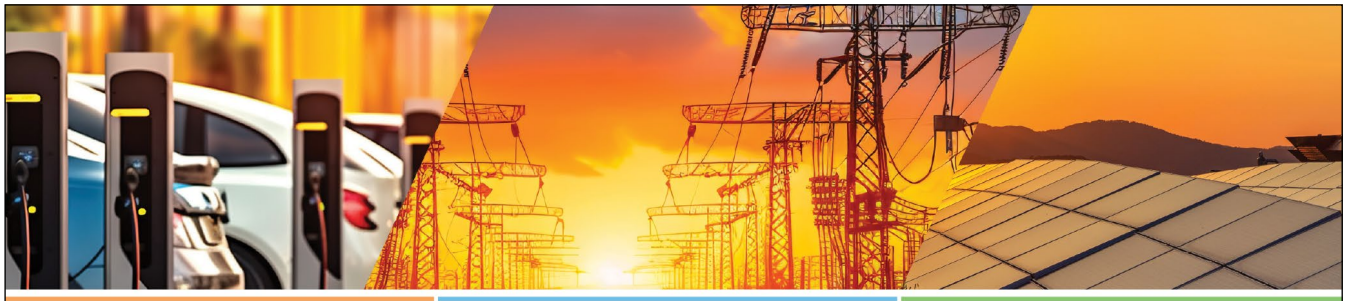
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From charging to AI: Power GaN's next growth chapter

The power GaN market is forecast to reach $3.5 billion by 2031, driven by data centers, EVs, and industrial systems.

BY YOLE GROUP

YOLE GROUP has released its annual report, Power GaN 2026, a comprehensive analysis of the power GaN semiconductor industry across markets, ecosystem, supply chain, and technology.

Power GaN has spent the past several years proving itself in consumer fast chargers. According to the new report, that phase is ending: GaN is now entering a broader, multi-market adoption cycle where AI data centers, electric vehicles, industrial systems, and renewable energy all become meaningful demand drivers. For chipmakers, foundries, and investors, understanding where this next wave of growth is concentrated and which companies are positioned to capture it is critical to strategic planning over the next five years.

Roy Dagher *PhD, Technology & Market Analyst, Compound Semiconductors, at Yole Group, comments*: "For years, power GaN's story was almost entirely about the phone charger in your pocket. That's no longer the full picture. AI infrastructure is opening a second, arguably bigger chapter for this technology, and it's moving fast."

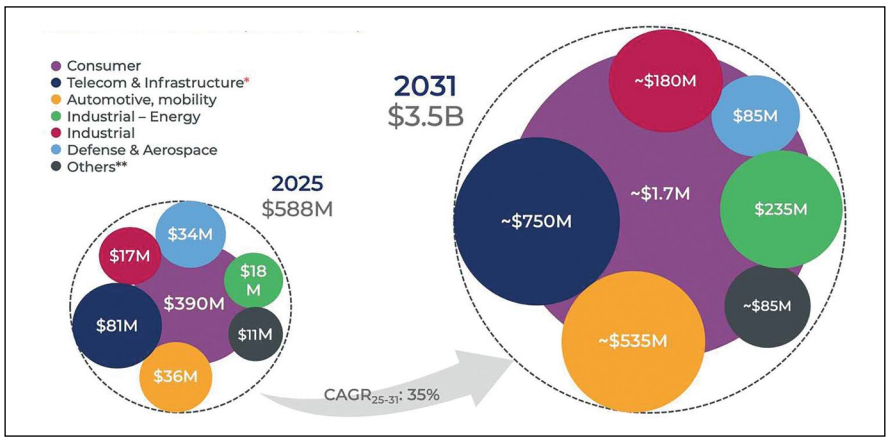
Consumer and mobile electronics remain the market's anchor segment by revenue, expected to reach $1.7 billion in 2031 with continued fast-charger and appliance adoption. But the report's sharpest growth curve belongs to automotive, where onboard chargers and emerging 48V architectures push the segment to a 57% CAGR, and to telecom/infrastructure, where AI-driven data center demand drives a 45% CAGR to $750 million. Further out, humanoid robots stand out as a potential growth engine beyond 2030. Actuator drives and battery management in a humanoid platform all call for high power density within tight weight and thermal budgets – the conditions where GaN's efficiency and small form factor matter most. Volumes are negligible today but if humanoid platforms reach commercial scale in the 2030s they would add a demand pool distinct from consumer, automotive, and data center applications.

The competitive landscape is shifting too.

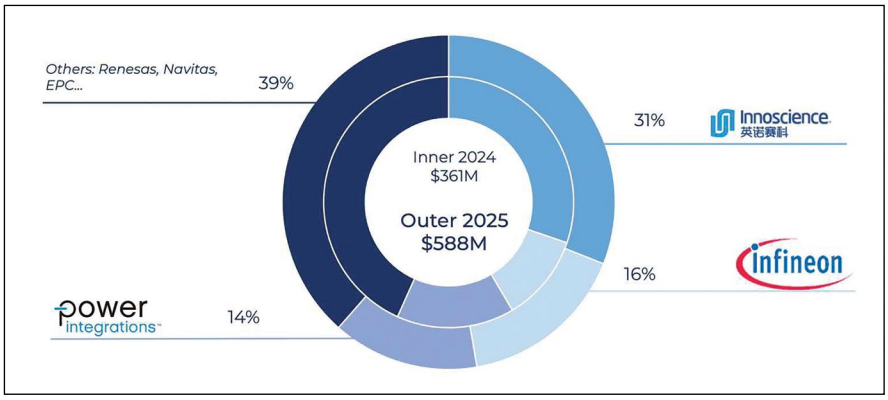
Innoscience holds the top spot in 2025 and continues to widen its footprint into automotive and data centers. Infineon Technologies posted the year's sharpest gains on the back of data center and renewable energy wins, and Renesas kept expanding across multiple fronts. Navitas took a different path, deliberately trading share in low-margin fast-charging for a foothold in higher-value segments. Onsemi is the most significant new entrant: it moved into power GaN through a collaboration with GlobalFoundries on 650V devices built on a 200mm GaN-on-silicon platform, alongside a parallel wafer-supply arrangement with Innoscience, with customer sampling starting in the first half of 2026 and AI data centers, EVs, and renewable energy as its stated targets. Behind the leaders, a fast-growing group of suppliers – ROHM, Texas Instruments, STMicroelectronics, Nexperia, and Chinese entrants including GaNext and Southchip,– is picking up share as GaN spreads to more corners of the industry.

The manufacturing shift is one of the report's central findings.

Rather than consolidating around a single dominant foundry, the industry is fragmenting productively:



➤ 2025-2031 Power GaN Device Market - split by end-market in $M
Source: Power GaN 2026 report, Yole Group



➤ Leading Power GaN Players' Market Shares - 2024 VS 2025
Source: Power GaN 2026 report, Yole Group

GlobalFoundries has licensed GaN technology from TSMC and is qualifying production in the U.S., VIS and PSMC are absorbing volume as customers move off TSMC, and Samsung, DB HiTek, and SK Keyfoundry are each building early GaN capabilities in Korea. At the same time, IDMs including Infineon, Renesas, onsemi, STMicroelectronics, ROHM, and Nexperia continue investing in their own capacity and vertical integration, often through acquisition.

Poshun Chiu *Principal Technology & Market Analyst, Semiconductor Substrates & Materials, at Yole Group, adds*: "TSMC stepping back from GaN foundry work could have been read as a warning sign for the industry. Instead, it's turning into one of the clearest signals of how much this ecosystem has matured. Other foundries are moving in fast, and the manufacturing base is coming out more distributed than before."

Cross-domain zonal controllers arrive: The next E/E step needs edge AI and redundancy

Last month, Yole Group forecast a $160 billion automotive semiconductor market by 2031 with a 31% CAGR between 2025 and 2031, in its *Automotive Semiconductor Trends 2026 report*. That growth is increasingly driven by the number of chips per car rather than higher-value content, and rebuilding the car's electrical and electronic (E/E) architecture is one of the main forces driving demand for that new silicon.

Yole Group now expands on this shift with a dedicated new report, *Automotive E/E Architectures 2026*. The analysis zooms in on the transition from over 100 scattered control units to a handful of domain, zonal, and central computers, the rise of the software-defined vehicle (SDV), and the specific processors, network chips, and power devices powering this evolution.

Decades of complexity being dismantled

The network of controllers, processors, communication chips, and power devices that make up a car's E/E architecture is undergoing its biggest change in decades. For years, the wiring harness was one of the heaviest and most expensive subsystems on board, as carmakers stacked function-specific ECUs until a single vehicle could carry over 100 units and kilometers of cable.

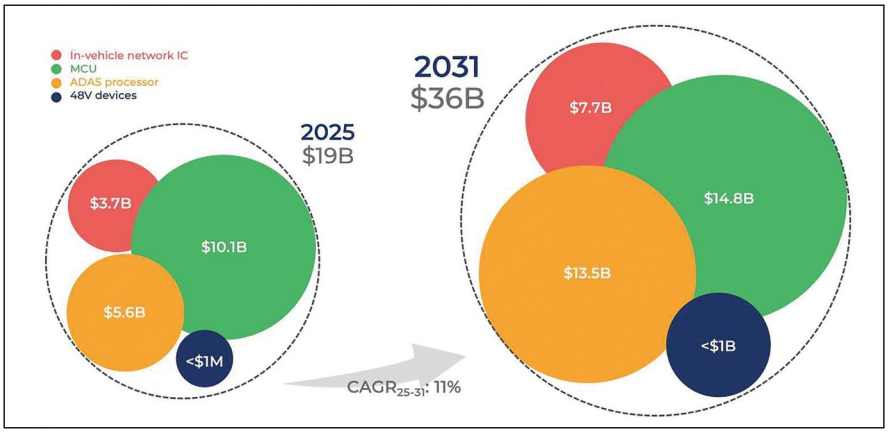
That model is being dismantled. Driven by the SDV, the rise of ADAS and AI, and the pressure to cut cost and weight, carmakers are consolidating scattered ECUs into a few high-performance domain, central, and zonal controllers. The benefits are already measurable: Tesla cut the wiring for the Model 3 to half that of the Model S, Rivian reduced its ECU count from 17 to 7, and BMW's Neue Klasse saves around 600 meters of cable while replacing up to 150 fuses with smart eFuses.

The Automotive E/E Architectures 2026 report quantifies who wins, when, and by how much, mapping the transformation end-to-end, from architectural strategy down to the individual chip.

Pierrick Boulay *Principal Analyst, Automotive Semiconductors at Yole Group, comments*: "This E/EA transition is creating new demand across the automotive semiconductor stack: advanced processors for central AI-based computation ($5.6B to $15.3B, 16% CAGR), high-performance MCUs for domain and zonal controllers (6.6% CAGR), in-vehicle network ICs as CAN/LIN give way to CAN FD and Ethernet (doubling from $3.9B to $8.1B), and a nearly new category of PMICs for 48V powernets (173% CAGR)."

Quantifying a region-by-region shift

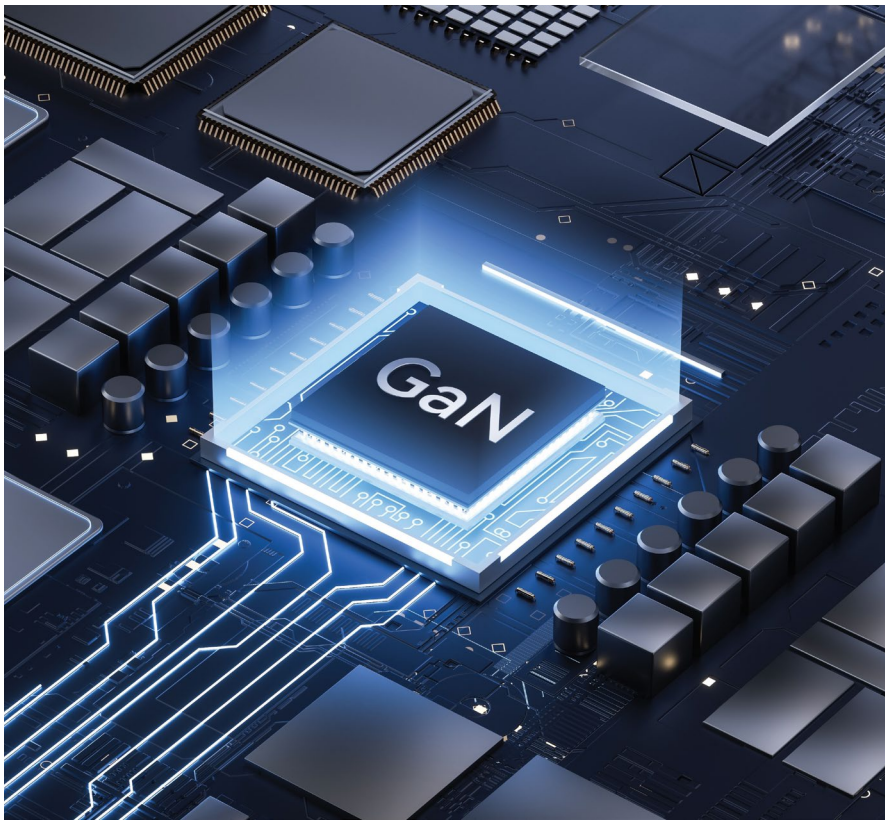
Focusing on light vehicles with forecasts spanning 2021–2031, Yole Group's report tracks the architectural shift from distributed to domain, zonal, and central designs, including one-box, one-board, and one-chip integration. It shows how the pace of change diverges sharply by region: Chinese OEMs are set to reach 56% zonal production by 2031, compared with just 18% outside China.



➤ 2025-2031 E/E Architecture Semiconductor Market by Device Type
Source: Automotive E/E Architectures 2026 report, Yole Group

Yu Yang *Principal Lead Analyst, Automotive & Robotics at Yole Group, adds*: "In the long-term trend of centralized E/E architectures, we are in the phase of upgrading backbone networks from domain-based to cross-domain zonal architectures plus a central computer for ADAS, infotainment, and vehicle control. Many new technologies are on the horizon, creating new opportunities for semiconductor devices: eFuses, 48V powernet, optical communication, etc."

The report also maps the semiconductor landscape enabling this transition, including automotive processors and the RISC-V ecosystem, microcontrollers, network chips, and power management ICs. It further examines how OEMs and Tier-1s are sourcing this silicon, weighing the make, buy, or partner decision that keeps full in-house design within reach of only high-volume players like Tesla and a handful of Chinese OEMs.



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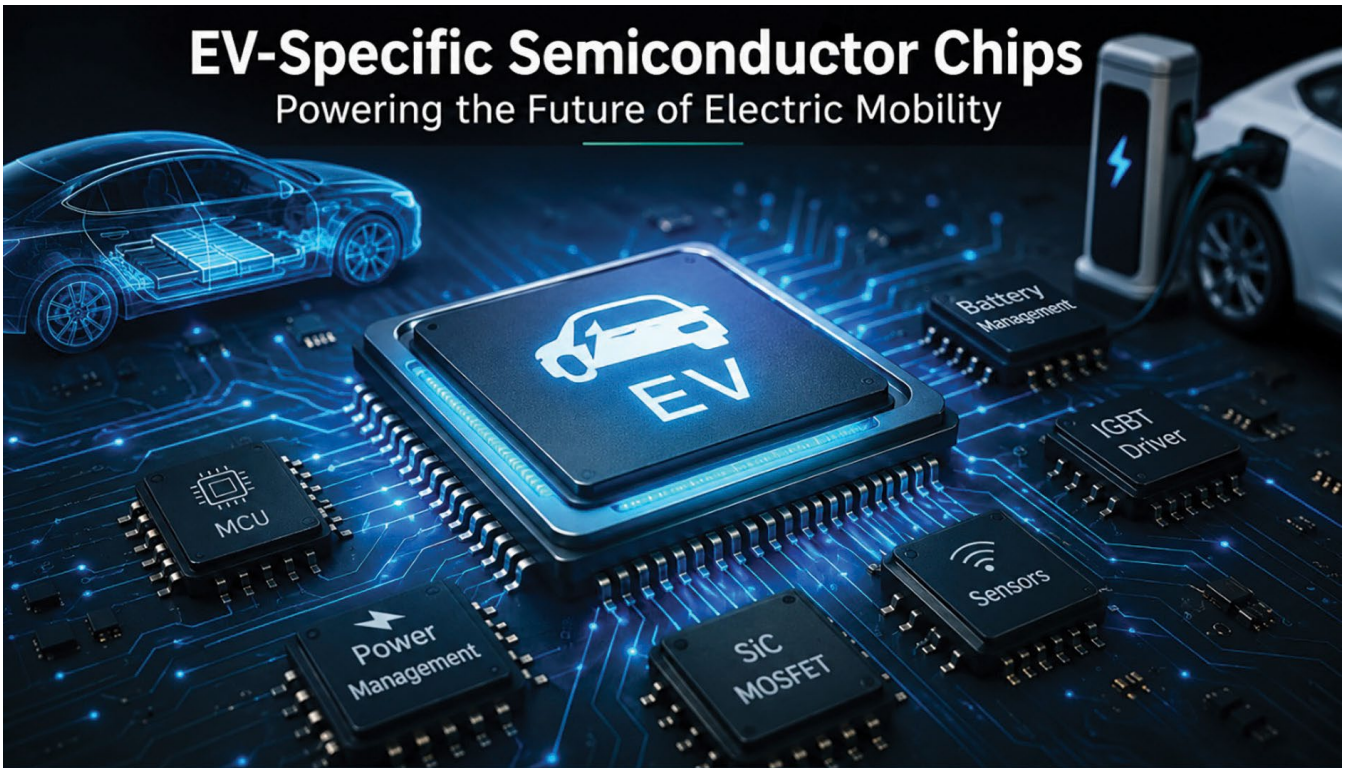


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EV-specific semiconductor chips market to reach $57.48 billion by 2034

According to **Research intelo**, the global EV-specific semiconductor chips market was valued at **$24.09 billion** in 2025 and is projected to reach **$57.48 billion** by 2034, expanding at a compound annual growth rate (CAGR) of **9.1%** during the forecast period 2026-2034.

AN ELECTRIC vehicle may look like a battery-powered machine, but beneath its body is a sophisticated network of semiconductor chips controlling power, motion, safety, charging, communication, and intelligence. This makes the **EV-specific semiconductor chips market** one of the most strategically important parts of the global electric mobility ecosystem.

As electric vehicles become more connected, software-defined, automated, and energy-efficient, semiconductor requirements are changing rapidly. Modern EVs need specialized chips capable of managing high voltages, switching power efficiently, processing enormous amounts of data, monitoring batteries, controlling motors, and communicating with charging infrastructure.

The scale of this opportunity is closely linked to EV adoption. According to the International Energy Agency, global electric car sales exceeded 20 million in 2025, representing around one-quarter of all new cars sold. The IEA expects global electric car sales to reach approximately 23 million in 2026.

This expansion creates a simple but powerful equation: **more EVs require more electronic intelligence, and more electronic intelligence requires more specialized semiconductor technology.**

What are EV-specific semiconductor chips?

EV-specific semiconductor chips are electronic components designed or optimized for the unique electrical, computational, and control requirements of electric and hybrid vehicles.

Unlike conventional automotive electronics that primarily support engine control and basic vehicle functions, EV semiconductor systems must handle high-voltage battery systems, electric motors, regenerative braking, sophisticated charging systems, thermal management, connectivity, and increasingly advanced driver-assistance technologies.

These chips can include power semiconductors, microcontrollers, systems-on-chips, battery-management ICs, gate-driver ICs, sensors, power-management ICs, communication chips, and processors.

Their importance extends beyond individual components. Semiconductor architecture increasingly influences an EV's **range, charging speed, acceleration, thermal efficiency,**

reliability, safety, and software capabilities.

Why is the EV-specific semiconductor chips market growing?

The strongest growth engine is the global transition from internal-combustion vehicles toward electrified transportation. EVs generally require more electronic control and power-management functionality than traditional vehicles, creating additional semiconductor content.

The evolution of vehicle architecture is another major factor. Automakers are moving toward higher-voltage platforms, including 800 V architectures, because higher voltage can reduce current requirements for a given power level and support faster charging and more efficient power delivery.

At the same time, electric vehicles are becoming computers on wheels. Advanced infotainment, connectivity, over-the-air software updates, digital cockpits, ADAS, automated driving functions, and centralized computing are increasing demand for high-performance automotive processors and controllers.

The result is a market where semiconductor demand is being driven simultaneously by **electrification and intelligence.**

What types of semiconductor chips are used in electric vehicles?

Power Semiconductors

Power semiconductors are among the most important chips in an EV because they control and convert electrical energy.

They are used in traction inverters, onboard chargers, DC-DC converters, battery systems, and other power electronics. Their efficiency directly affects how much electrical energy is lost as heat.

Traditional silicon devices remain important because of their established manufacturing ecosystem and cost advantages. However, wide-bandgap materials are increasingly attracting attention for demanding EV applications.

Silicon Carbide Chips

Silicon carbide, commonly known as SiC, has become one of the defining semiconductor technologies for high-voltage EV power electronics.

SiC devices can operate efficiently at high voltages and temperatures while switching rapidly with lower losses than many conventional silicon alternatives. These characteristics make them particularly attractive for traction inverters and high-power EV systems.

The transition toward 800 V vehicle platforms strengthens the case for SiC because manufacturers are seeking higher efficiency, faster charging, smaller power systems, and improved thermal performance.

Gallium Nitride Chips

Gallium nitride, or GaN, is another wide-bandgap technology gaining momentum.

GaN's ability to switch at high frequencies can help manufacturers develop smaller and highly efficient power-conversion systems. It is particularly relevant to onboard chargers, DC-DC converters, auxiliary power systems, and selected charging applications.

Industry research increasingly identifies GaN as a high-growth technology, although its automotive adoption remains more application-specific than SiC.

Battery Management Chips

An EV battery is only as useful as the electronics controlling it.

Battery-management semiconductor systems monitor voltage, current, temperature, state of charge, and state of health. They help maintain battery cells within safe operating conditions while supporting performance optimization and longevity.

As battery packs become larger and more sophisticated, accurate sensing and control become increasingly important.

Microcontrollers and Automotive Processors

Microcontrollers act as the electronic brains of numerous vehicle subsystems.

They can control battery functions, motor systems, thermal management, lighting, body electronics, charging functions, and safety systems. More powerful processors are also required for infotainment, ADAS, connectivity, and centralized vehicle computing.



The emergence of software-defined vehicles is pushing the industry toward higher-performance computing architectures, making processors increasingly central to vehicle design.

How do EV semiconductor chips improve vehicle performance?

Better Driving Range
Every percentage point of efficiency matters in an EV.

Efficient power semiconductors reduce electrical losses during energy conversion, helping more energy from the battery reach the motor. This can contribute to improved vehicle range without necessarily increasing battery capacity.

Faster Charging
Charging speed depends on much more than the charging station. The vehicle's onboard power electronics must safely manage substantial electrical power.

Advanced semiconductor technologies can support efficient high-power conversion and contribute to faster charging architectures.

Improved Thermal Management
Heat is an unavoidable consequence of electrical resistance and switching losses.

More efficient semiconductor devices generate less waste heat, reducing the thermal burden on cooling systems. This can help engineers design compact and efficient power electronics.



Higher Power Density
Higher-performing semiconductor technologies allow manufacturers to deliver more electrical power from smaller packages.

This is particularly valuable in EVs, where engineers continuously balance performance, weight, packaging space, cooling requirements, and cost.

The role of 800 V architecture

One of the most important technological developments influencing the EV semiconductor industry is the shift from traditional 400 V systems toward 800 V platforms.

For a given power output, increasing voltage reduces the current required. Lower current can reduce resistive losses and support more efficient high-power charging and power delivery.

However, higher-voltage architectures also demand semiconductor devices capable of safely handling greater electrical stress.

This creates opportunities for SiC power devices, advanced gate drivers, insulation technologies, sensors, and sophisticated power-management systems.

Consequently, the growth of 800 V EV platforms is not simply a vehicle-engineering development. It is also a semiconductor architecture opportunity.

EV semiconductors and software-defined vehicles

The next generation of EVs will increasingly be defined by software.

Instead of treating every vehicle function as an independent electronic system, automakers are moving toward centralized and zonal architectures. This can reduce wiring complexity while allowing computing resources to be allocated more dynamically.

Such architectures require high-performance processors, communication interfaces, memory, cybersecurity hardware, and sophisticated microcontrollers.

The semiconductor therefore becomes more than a power-control component. It becomes part of the vehicle's digital platform.

This shift could change how automakers select semiconductor suppliers. Hardware performance, software compatibility, security, upgradeability, functional safety, and long-term supply availability may increasingly become interconnected purchasing decisions.

What is driving demand for EV-specific semiconductor chips?

Several structural forces are shaping demand.

- **Electrification:** Increasing EV penetration expands demand for power electronics, controllers, sensors, and battery-management systems.
- **Fast charging:** Higher charging power requires increasingly capable semiconductor components.
- **800 V platforms:** High-voltage vehicle architectures create opportunities for advanced power devices.
- **ADAS:** More sophisticated driver-assistance systems require processors, sensors, memory, and communication chips.
- **Vehicle connectivity:** Connected EVs require communication and computing hardware for cloud interaction, navigation, diagnostics, and remote services.
- **Software-defined vehicles:** Centralized computing increases demand for high-performance automotive processors.
- **Energy efficiency:** Automakers are seeking semiconductor technologies that reduce losses and improve overall vehicle efficiency.
- **Charging infrastructure:** EV semiconductor demand extends beyond vehicles into charging stations, power conversion systems, and energy-management equipment.

What are the major challenges in the EV-specific semiconductor chips market?

High Automotive Qualification Requirements
Automotive semiconductors operate under demanding conditions involving temperature variation, vibration, electrical stress, and long service lives.

Manufacturers must therefore meet rigorous reliability and functional-safety requirements. Qualification can take significantly longer than in many consumer-electronics applications.

High Manufacturing Costs
Advanced semiconductor fabrication, SiC substrates, sophisticated packaging, testing, and automotive qualification require substantial investment.

This can create barriers for smaller semiconductor companies attempting to enter the market.

Supply Chain Concentration
The semiconductor ecosystem depends on specialized materials, wafers, fabrication facilities, packaging technologies, equipment, and geographically concentrated manufacturing capabilities.

Supply disruptions can therefore affect vehicle production.

Cost Pressure
EV manufacturers are under constant pressure to reduce vehicle prices.

A technically superior semiconductor does not automatically win the market. Suppliers must demonstrate a compelling combination of efficiency, reliability, scalability, and total system economics.

Technology Competition
Silicon, SiC, GaN, advanced packaging, and emerging semiconductor technologies are competing for different application areas.

The industry is unlikely to converge on one material for every EV function. Instead, the future will probably involve a technology portfolio optimized according to voltage, power, frequency, cost, and application requirements.

What is the future of SiC and GaN in EVs?

The future is unlikely to be a simple battle between SiC and GaN.

Instead, each technology is likely to find applications where its electrical characteristics provide the greatest system-level advantage.

SiC is particularly compelling for high-voltage and high-power applications such as traction inverters. GaN has strong potential in high-frequency, compact power-conversion applications such as onboard charging and DC-DC conversion.

Industry analysis indicates that wide-bandgap semiconductors are becoming increasingly important as EV manufacturers pursue higher efficiency and power density.

The more important question is therefore not **"Which material will replace silicon?"** but **"Which semiconductor technology delivers the best system economics for each EV application?"**

EV semiconductor chips and the charging ecosystem

The semiconductor opportunity extends beyond the vehicle itself.

Charging stations require power conversion, switching devices, communication controllers, sensors, protection systems, and intelligent energy-management hardware.

As charging becomes faster and more interconnected, semiconductor requirements will become increasingly sophisticated.

Bidirectional charging could further expand this opportunity by allowing compatible EVs to interact dynamically with the electricity grid. This could turn vehicles from passive electricity consumers into flexible energy assets.

Sustainability and semiconductor efficiency

EV sustainability is often discussed primarily in terms of batteries and tailpipe emissions. Yet semiconductor efficiency also matters.

A small improvement in power-conversion efficiency can translate into reduced energy losses across millions of vehicles and charging cycles.

This means semiconductor engineering has a role in reducing the amount of energy required to move, charge, and operate electric vehicles.

The significance becomes even greater as global EV battery demand rises. The IEA reported that EV battery demand exceeded 950 GWh in 2024 and projects demand to surpass 3 TWh by 2030 under its stated policies scenario.

Power devices will become more efficient. Computing platforms will become more centralized. Sensors will become more sophisticated. Semiconductor packaging will become increasingly important. Software and hardware will be designed together rather than independently.

What will the next generation of EV semiconductor chips look like?

According to **Research intelo**, future EV semiconductor development will likely focus on five interconnected objectives: **higher efficiency, greater integration, improved reliability, lower cost, and intelligent control.**

Power devices will become more efficient. Computing platforms will become more centralized. Sensors will become more sophisticated. Semiconductor packaging will become increasingly important. Software and hardware will be designed together rather than independently.

Another major development will be the integration of multiple functions into advanced power modules and system-level semiconductor architectures.

The objective is not simply to produce a faster chip. It is to create an electronic architecture that allows the entire vehicle to operate more intelligently and efficiently.

Source: https://researchintelo.com/report/ev-specific-semiconductor-chips-market

Yole forecasts solid growth as power device market dynamics shift

Yole Group tips the power device sector to top $40bn by 2031, as Chinese competition, price pressures and wide bandgap technologies reshape the market.

BY REBECCA POOL, TECHNOLOGY EDITOR

DESPITE geopolitical uncertainty, disappointing electric vehicle demand and manufacturing overcapacity, power device market growth will be robust in the next five years, reports France-based semiconductor analyst firm, Yole Group. Driven by a mix of electric mobility, industrial motor drives, photovoltaics, Battery Energy Storage Systems, power supplies for AI data centers, electric vehicle DC chargers, as well as rail and HVDC projects, the power device sector is forecast to grow from US$29.4 billion in 2026 to US$41.3 billion in 2031. That's a steady compound annual growth rate of 7.1%.

Yet alongside the healthy growth, Yole Group points out how the sector is also navigating an increasingly complex market environment. The rise of Chinese manufacturers and intensifying competition, pricing pressures, the evolution of wide bandgap technologies and an increasing role in defense and aerospace are all part of the mix. The end result is, power electronics players are now focused on consolidation, cost and competitive positioning.

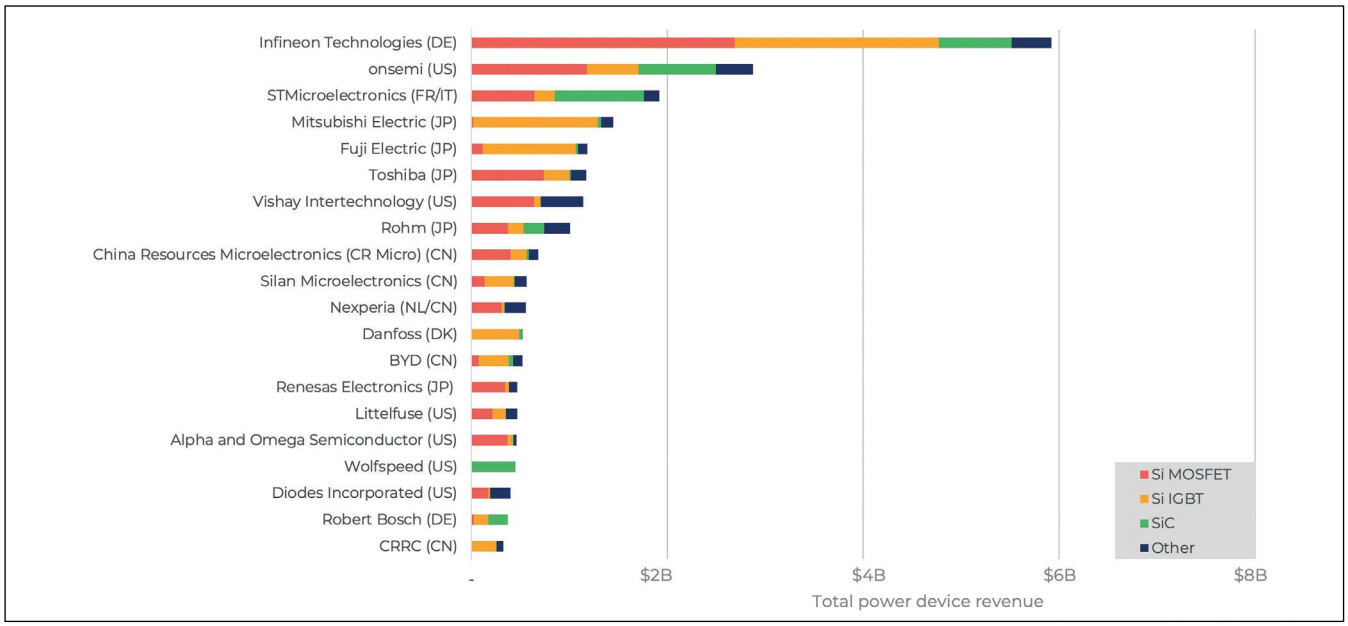
As Milan Rosina, Yole's Principal Technology and Market Analyst for Power Electronics and Batteries, highlights, the industry is focusing on business fundamentals. This includes a rapid ramp-up of newly built fabs, yield optimization on large-diameter wafers, "front-runner" products rather than breakthrough innovations, customer acquisition, sales execution, and management of the increasing competition and cost pressures.

"The power electronics industry is entering a new phase," he says. "While growth prospects remain robust, industry priorities are changing... the focus has shifted from expansion to competitiveness, cost optimization and market share."

Rosina also notes marked differences in the tech strengths from region to region. He outlines how Japan remains strong in materials, packaging, reliability, and industrial power electronics while Europe is focused on automotive, industrial, renewable energy, and high-reliability systems. The US prioritizes AI infrastructure, data centers, and high-performance applications, and China dominates electrification scale, manufacturing capacity, and domestic deployment. Overall, Asia continues strengthening its role as a global packaging and Outsourced Semiconductor Assembly and Test (OSAT) hub.

Chinese competition

Yole's latest market figures align with other predictions from analyst firms.



➤ Top 20 power device manufacturers' revenue: 2025 ranking and positioning on different device technologies
Source: Status of the Power Electronics Industry 2026 report, Yole Group

IDTechEx, UK, has predicted market growth from US$25.5 billion to US$ 56.2 billion in the next ten years – a 10% CAGR largely driven by electric vehicles and data centre applications. Mordor Intelligence has forecast a 7.21% CAGR for power electronics to 2031 with the market growing from US$30.78 billion to US$ 43.61 billion. The India-based analyst firm cites electric vehicles, industrial electrification and defence amongst key market drivers.

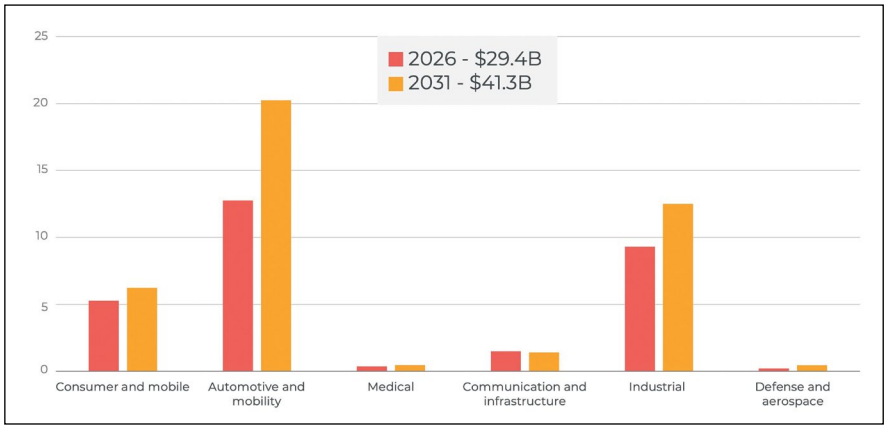
As Rosina highlights, the market remains dominated by European, US, and Japanese players, including Infineon, onsemi, STMicroelectronics, and Mitsubishi Electric - but for how long? According to the analyst, the market share of China-based suppliers is rapidly increasing.

In terms of total power device revenue, right now, Infineon Technologies maintains its leadership position, followed by onsemi and STMicroelectronics, reflecting strong capabilities across silicon, SiC, and GaN power semiconductor technologies. Mitsubishi Electric, Fuji Electric, Toshiba and Vishay Technologies follow behind.

However, Chinese firms are rapidly making inroads into SiC wafers – primarily used for power electronics – as well as power devices and industrial power modules, helped by strong domestic demand in electric vehicles, photovoltaics, wind energy, and battery storage systems. This is placing more pressure on the established global suppliers.

For example, Hong Kong and Shanghai Stock Exchange-listed, SICC (Tianyue Advanced), launched the world's first 300 mm n-type SiC substrate back in late 2024. TanKeBlue, holds a 15% share of the global SiC market and has just had its Shanghai Stock Exchange STAR Market IPO application accepted. The formidable market force now plans to raise 2.78 billion yuan - around $410.1 million - to expand large-size SiC material production. Infineon signed a long-term agreement with both SiC suppliers in 2023 to diversify its supply base.

As Yole also reports, Chinese firms such as CR Micro, Silan, BYD, and CRRC are amongst its Top 20 power device manufacturers in 2025. Key power module suppliers include CRRC and Macmic Science&Technology, which manufacture both silicon-based IGBT and SiC modules.



➤ Overall Power Electronics Market - 2025 VS. 2031, in $M and by application
Source: Status of the Power Electronics Industry 2026 report, Yole Group

Steady silicon

Amid the rise of China-based firms, Rosina is certain silicon will remain the backbone of power electronics for the next five years. He reckons MOSFETs and IGBTs will continue to dominate mainstream applications thanks to their cost, maturity, reliability, and broad ecosystem. "Silicon has a high level of technology maturity and proven field returns from many applications... it has high reliability even in very demanding applications such as grid and rail," he points out. "[The technology] has a well-established supply chain and ease of multi-sourcing, and has a lower cost compared to SiC and GaN."

Rosina also highlights how silicon devices cover a wide range of voltage and current values. "Silicon is also available in numerous package options matching the requirements of numerous converter designs and applications," he adds. "It will remain the technology of choice in applications where cost is crucial and its performance is satisfactory... and in applications [that require] a long product lifetime – that includes grid, rail and wind turbines."

Right now, the silicon wafer supply chain remains dominated by a small number of Japanese, Taiwanese, and Chinese players, says Rosina. These include SUMCO and Shin-Etsu Handotai, both based in Japan, as well as GlobalWafers and Wafer Works in Taiwan, among others. Siltronic of Germany remains the only major European silicon wafer supplier.

But while silicon remains steady for now, both SiC and GaN devices are expected to progressively increase market share driven by demand for higher efficiency and greater system power density. Inevitably, more investment in these technologies from industry players will follow.

According to Rosina, electric vehicles remain the largest market segment for SiC devices, thanks to high-temperature operation, faster switching speeds, a relatively small form factor, and weight and volume savings that ultimately support increased EV range and performance. But although SiC MOSFETs are swiftly gaining revenue in traction inverters, onboard chargers and DC-DC converters, market slowdown in battery electric vehicles has created SiC overcapacity and strong price pressure across the supply chain.

Meanwhile, Rosina also highlights how rising GaN use is still largely driven by consumer devices, although adoption is gathering momentum in high power, high voltage systems, such as power supply units for AI data centres. Both Power Integrations and Efficient Power Conversion (EPC) are manufacturing high-voltage GaN systems for 800 V AI server applications. Rosina also notes that Innoscience of China now has a strong position in the GaN power device market.

Together, these wide bandgap technologies are expected to account for 31% of the power device market value by 2031, up from 16% today. "The adoption of SiC and GaN technologies is growing rapidly to the detriment of silicon devices," says Rosina.

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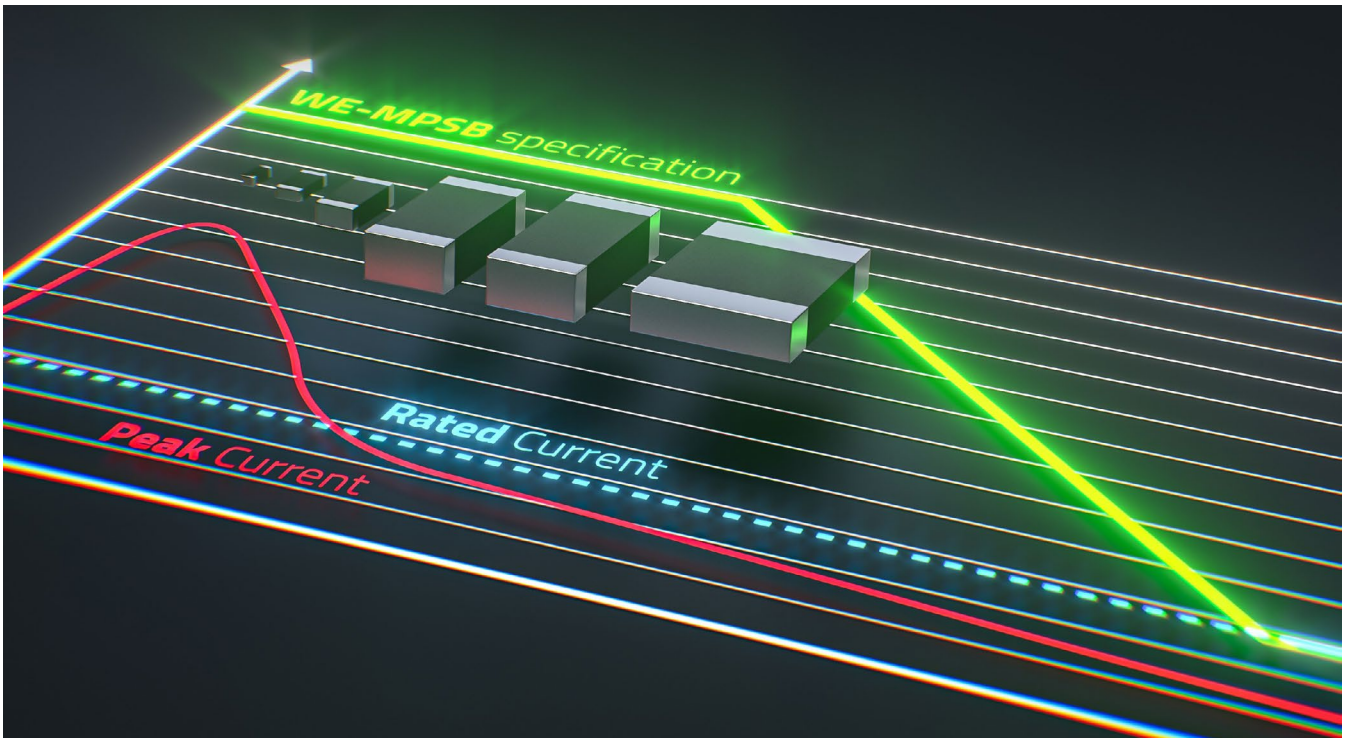
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Better resilience against current peaks

Due to their multilayer structure, chip bead ferrites are sensitive to current peaks, which typically occur when switching on power supplies or electric motors. However, an optimized layer design improves their resistance to short-term high current surges.

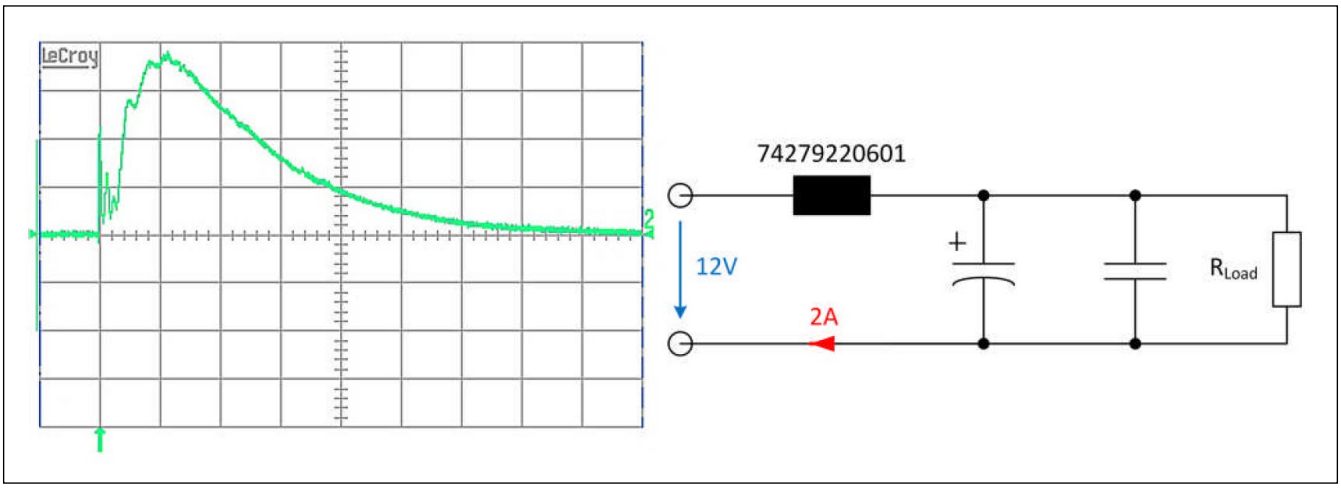
BY MARKUS HOLZBRECHER AND MOHAMED KOOBAR

CHIP BEAD ferrites are multilayer inductive components used mainly for EMC filtering. They consist of a nickel-zinc ferrite body with very thin internal silver conductor layers. This multilayer structure enables compact size and useful impedance behavior, but it also makes standard SMD ferrites sensitive to short current surges above their rated current. Such peaks typically occur during switch-on events in power supplies, motor drives, or lamp ballasts. If the current exceeds the permissible limit, the component can be damaged immediately. For conventional multilayer ferrites, the rated current in the data sheet therefore also represents the maximum permissible current amplitude for short-term loading.

Optimized layer design

The WE-MPSB series [1] from Würth Elektronik was developed specifically for applications in which short current peaks exceed the continuous rated current. The acronym stands for Multilayer Power Suppression Bead. Compared with conventional multilayer ferrites, the internal layer design is optimized for higher current capability, significantly lower DC resistance, and high impedance over a broad frequency range. Depending on the type, the DC resistance can be reduced by up to 75 percent. This lower resistance helps the component tolerate higher pulse currents while maintaining effective EMI suppression.

A common use case is an inline filter at the input of a power circuit **(Figure 1)**. During switch-on, the input capacitor may draw a very high inrush current because of its low ESR. As a result, the ferrite briefly sees a current far above the normal operating current. In the example described in Application Note ANP028 from Würth Elektronik [2], a 600 Ω WE-MPSB type with a rated current of 2.1 A is exposed to a single current peak of about 19 A for roughly 0.8 ms before the current decays to the steady-state value. This illustrates why standard ferrites can fail in such applications and why a dedicated pulse-current specification is useful.



Test procedure for pulse load capacity

Current peaks of this kind occur in many real circuits, but they vary strongly in shape and duration. To create reproducible data sheet values, Würth Elektronik developed a test method based on the fuse test approach for determining the melting integral I^2t. In that method, the component is stressed with defined pulses and sufficient cooling time between pulses. For WE-MPSB ferrites, a rectangular pulse shape was selected for testing because it represents the highest energy input over a given pulse duration and is therefore a conservative worst-case load. Standard tests cover pulse durations from 0.5 ms to 8 ms. A pause between pulses allows the component to cool before the next load cycle.

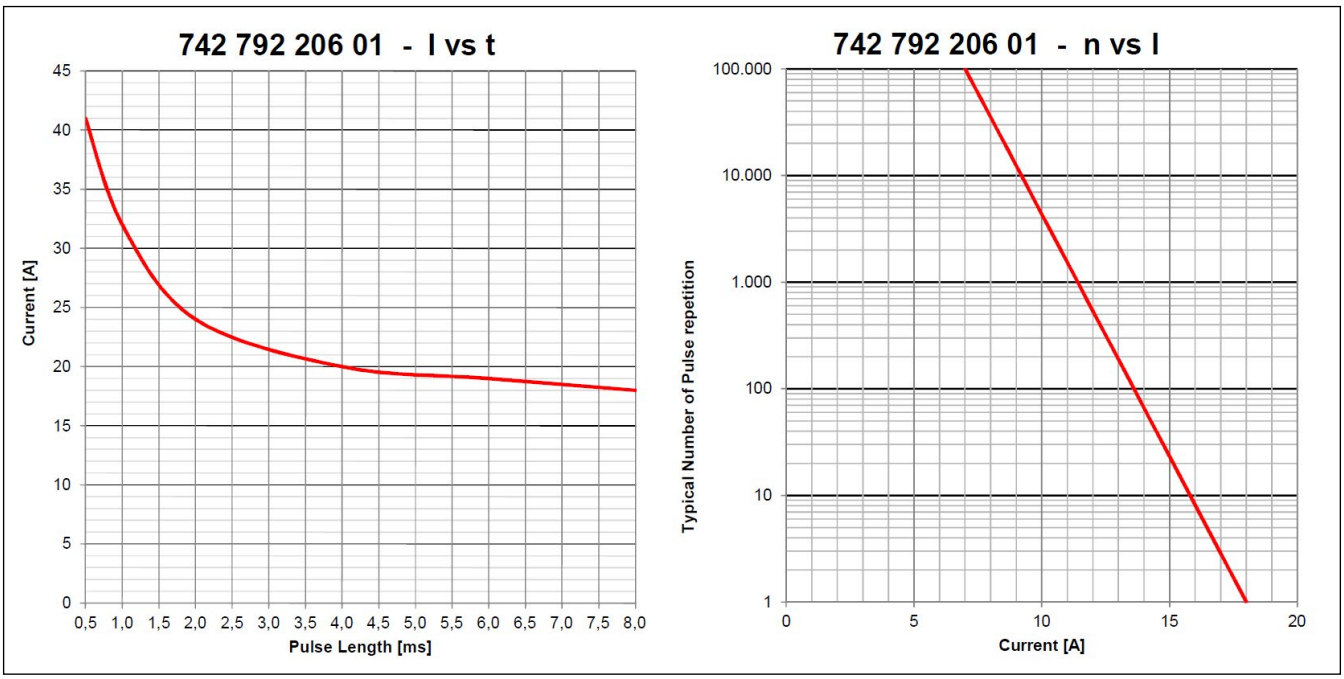
Although the fuse standard provided a useful starting point for a test routine, multilayer ferrites do not behave like fuses. Their pulse-current capability cannot be predicted reliably with a universal I^2t formula. Measurements demonstrate this with a 600 Ω WE-MPSB part. If an 8 ms pulse capability is used to calculate the allowable current for a 2 ms pulse via a constant I^2t assumption, the result differs significantly from the measured data sheet value. In practice, the maximum pulse current must therefore be determined empirically for each component type and test condition. The relevant values in the data sheet are the result of long-term measurements, not a simple theoretical conversion. **Figure 2** shows the maximum permissible peak current for the respective pulse durations tested. The tested range extends from 0.5 ms to 8 ms.

Permissible pulse current

Three parameters mainly determine pulse-load capability:

First, pulse duration: the longer the pulse, the lower the permissible peak current.

➤ Figure 1: Typical application with peak current at switch-on (5 A/DIV | 100µs/DIV).



➤ Figure 2: Representation of the current as a function of the pulse duration and the number of pulses at 8 ms.

Second, number of pulses: repetitive stress reduces the allowed pulse amplitude compared with a single pulse. Data sheets therefore distinguish between single-pulse and repetitive-pulse conditions.

Third, temperature: as temperature rises, the DC resistance increases, which further reduces the allowable pulse load. These parameters are interdependent, and the cooling pause between pulses also has a strong influence. For this reason, pulse-current capability must always be considered as a system of boundary conditions rather than as one isolated number.

The development target for the WE-MPSB series was to achieve impedance behavior comparable to the established WE-CBF ferrite family while increasing current robustness. Conventional WE-CBF components are generally not intended to withstand substantial overcurrent peaks above rated current. In contrast, WE-MPSB parts are designed for applications with short-term current surges during switch-on. Because of their lower resistance, they also offer higher rated current capability for comparable impedance values. The pulse-load capacity of an MPSB 600 Ω type is significantly higher than that of a comparable CBF type in the same package size **(Figure 3)**.

Wide range of components

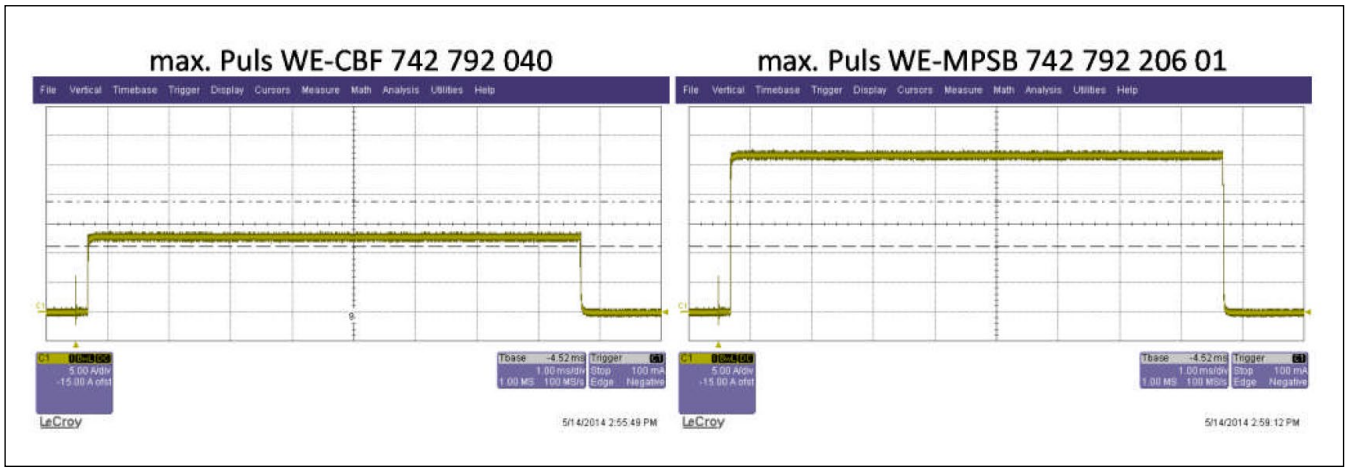
The WE-MPSB family covers impedance values from 8 Ω to 600 Ω at 100 MHz and is available in package sizes from 0603 to 3312. Depending on the type, rated current values range from 2.1 A to 10.5 A, while typical DC resistance spans roughly 1.0 mΩ to 80 mΩ. The specified usable frequency range extends from 1 GHz to 3 GHz, with extension toward 8 GHz under qualification. For higher currents, especially above 5 A, PCB layout becomes increasingly important because conductor width, copper thickness, and thermal behavior of the tracks can limit the overall current capability even if the ferrite itself is suitable.

Multilayer ferrites are indispensable EMI suppression elements, but conventional chip bead designs can be vulnerable to inrush and other short overcurrent events. The WE-MPSB series addresses this limitation with an optimized internal structure that combines lower resistance, strong impedance performance, and significantly improved pulse-current capability. Because the allowable peak current depends on pulse duration, repetition, temperature, and cooling conditions, practical design work should use the empirical pulse-current data in the data sheet rather than simplified I^2t calculations. For input filters and other circuits with pronounced current peaks, this makes WE-MPSB ferrites a more robust option than conventional multilayer beads.

The development target for the WE-MPSB series was to achieve impedance behavior comparable to the established WE-CBF ferrite family while increasing current robustness. Conventional WE-CBF components are generally not intended to withstand substantial overcurrent peaks above rated current.

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➤ [1] SMD-Ferrite WE-MPSB (EMI Multilayer Power Suppression Bead) from Würth Elektronik: https://www.we-online.com/en/components/products/WE-MPSB
➤ [2] Holzbrecher, M.: Peak current carrying SMD ferrites - Multilayer Power Suppression Beads. AppNote ANP028 from Würth Elektronik: https://www.we-online.com/ANP028



➤ Figure 3: Comparison of the pulse load capacity of the WE-CBF and WE-MPSB series.



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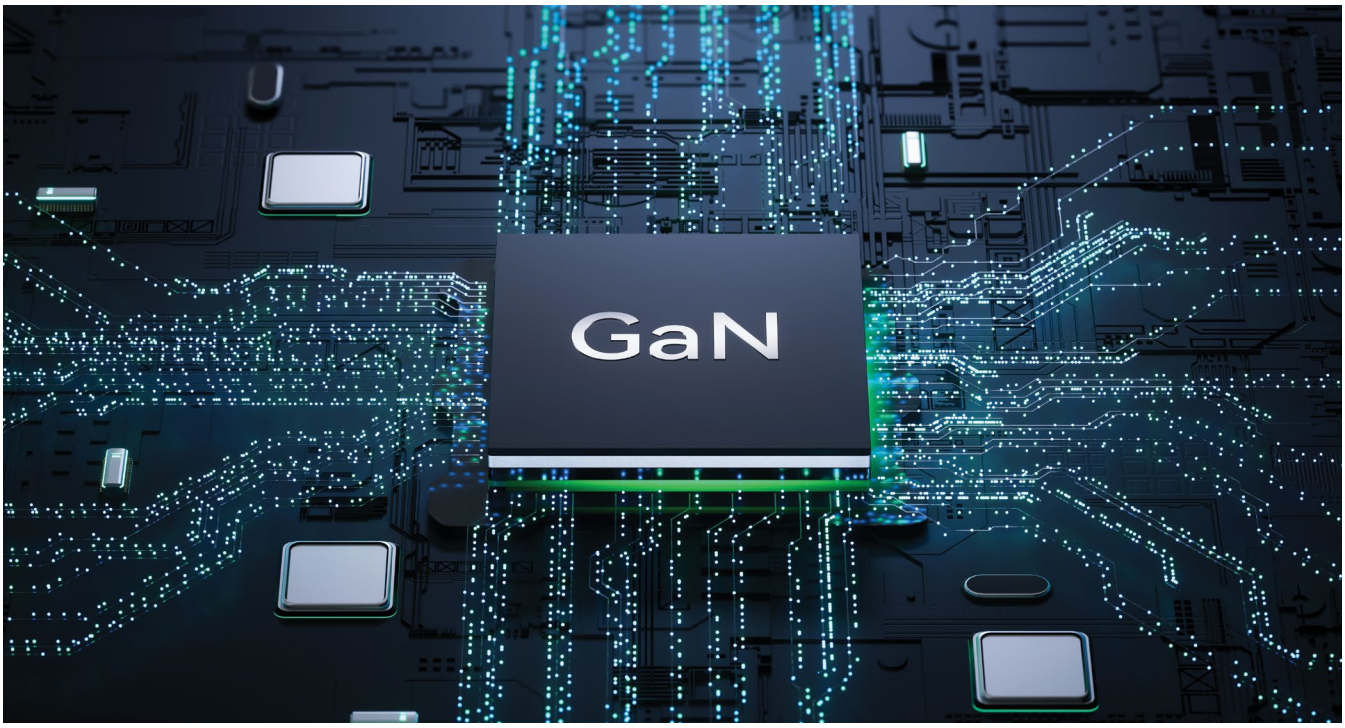
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GaN goes mainstream

Daniel Murphy, Senior Director of Product Management at Cambridge GaN Devices, discusses CGD's collaboration with NXP Semiconductors to accelerate time to market in the data centre and automotive sectors.

THE RACE to build the next generation of AI infrastructure is reshaping the power electronics industry. As hyperscale data centres push toward ever-higher power densities and electric vehicle manufacturers search for greater efficiency, compactness and performance, the limitations of traditional semiconductor technologies are becoming increasingly apparent.

Gallium nitride (GaN) has long been viewed as one of the industry's most promising technologies, offering switching speeds and efficiency gains that conventional silicon and, in some cases, silicon carbide struggle to match. However, unlocking the full benefits of GaN requires more than advanced transistor technology alone. It demands complete system-level solutions that combine power devices, control electronics, software intelligence and robust design methodologies.

That thinking sits at the heart of a newly announced long-term collaboration between Cambridge GaN Devices (CGD) and NXP Semiconductors.

The partnership brings together CGD's expertise in gallium nitride power devices and NXP's extensive capabilities in processing, control, analog technologies and automotive-grade electronics. The objective is ambitious: accelerate the adoption of GaN-based solutions in some of the world's fastest-growing markets, particularly AI-driven data centres and next-generation automotive platforms.

For Daniel Murphy, Senior Director of Product Management at Cambridge GaN Devices, the collaboration represents a natural alignment of complementary strengths.

A partnership built around complementary expertise

The power semiconductor industry is increasingly recognising that next-generation power architectures cannot be solved by individual device innovation alone. While semiconductor breakthroughs remain essential, end customers are increasingly looking for complete, validated solutions that reduce development risk and shorten deployment times.

Murphy sees the CGD-NXP relationship as a powerful example of that trend.

From CGD's perspective, the company contributes deep expertise in gallium nitride technology, a field in which it has established itself as a significant innovator. As demand grows for higher-frequency, more efficient power conversion systems, GaN is emerging as a critical enabling technology for future AI infrastructure.

At the same time, NXP brings strengths that extend beyond power semiconductors. The company possesses extensive experience in microprocessors, DSPs, control systems, analog technologies and automotive electronics, along with a substantial global customer footprint.

The result is what Murphy describes as a highly complementary partnership. Rather than focusing solely on individual components, both companies can collaborate on complete power architectures that combine advanced switching devices with sophisticated control and management capabilities. For customers, that means faster implementation and reduced engineering complexity. For the partners, it creates opportunities to address larger portions of the value chain while accelerating adoption of their respective technologies.

Addressing the time-to-market challenge

One of the central themes of the collaboration is reducing time to market. This has become particularly important in AI infrastructure, where demand is evolving at unprecedented speed and power requirements are increasing almost continuously.

According to Murphy, discussions with hyperscalers have revealed that some existing power semiconductor technologies are struggling to keep pace with emerging requirements. Switching frequency represents one of the most significant challenges.

Certain segments of the AI data centre ecosystem are already pursuing operation around the 1MHz level, creating performance requirements that Murphy believes exceed the practical limits of silicon carbide in some power conversion stages.

This is where GaN becomes especially attractive.

Its ability to operate efficiently at significantly higher switching frequencies allows designers to create smaller, lighter and more power-dense systems.

However, high-performance GaN devices require equally sophisticated control systems. Higher switching speeds place increased demands on gate drive technologies, digital control platforms and overall system design. The collaboration therefore addresses both sides of the equation.

CGD contributes the GaN switching technology required to achieve these higher frequencies, while NXP provides the processing and control expertise necessary to manage and optimise device operation. Working together allows both companies to accelerate customer adoption and reduce barriers associated with implementing advanced power architectures.

Why AI data centres need GaN

Few markets are creating as much excitement across the power electronics industry as AI data centres. The relentless growth of artificial intelligence workloads is driving dramatic increases in rack power, system density and overall facility energy consumption. These developments are forcing operators to rethink virtually every aspect of power delivery.

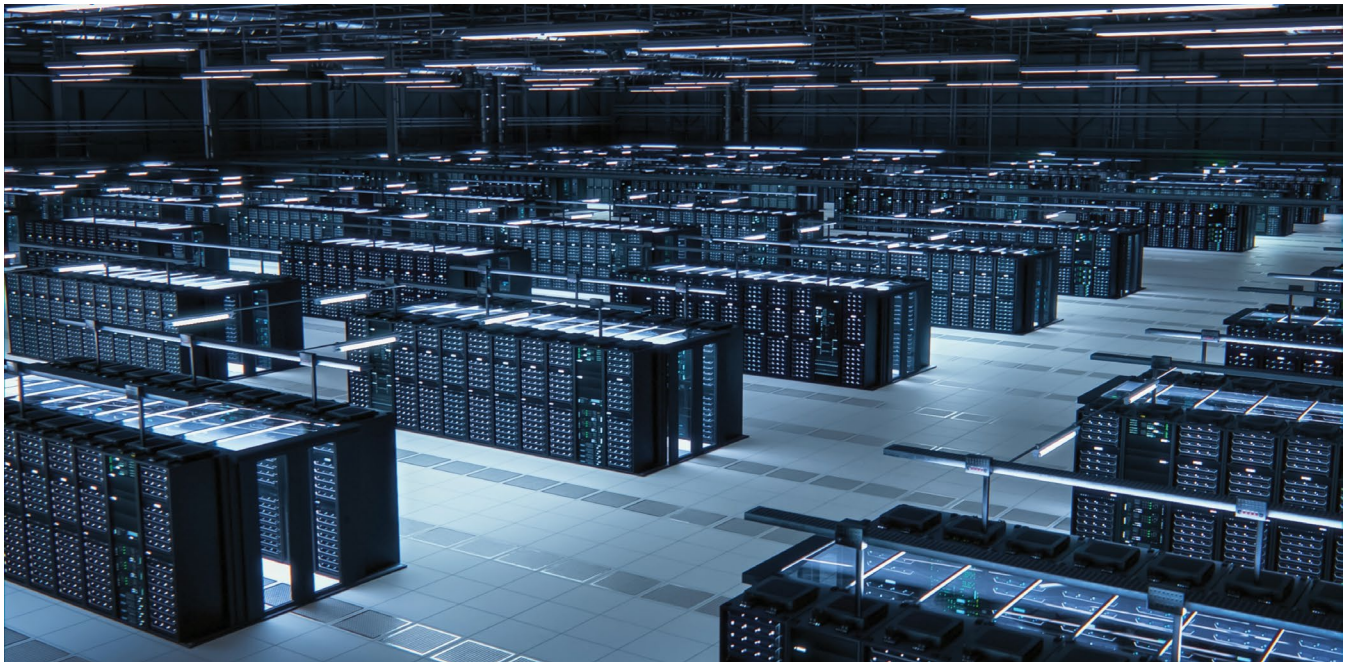
For Murphy, one of GaN's greatest advantages lies in its ability to support higher switching frequencies without introducing unacceptable efficiency penalties. As power converters switch faster, designers can reduce the size of passive components such as magnetics and capacitors. Smaller passive components translate directly into more compact power supplies. In AI facilities, where physical space is increasingly valuable, the benefits can be significant.

"The demand is to increase switching frequency so that you can reduce system size," Murphy explains.

Higher power density means more power supplies can be deployed within the same footprint, ultimately enabling greater compute density and processing capability.

According to CGD, silicon carbide performs exceptionally well across many applications but begins to encounter practical challenges as switching frequencies approach and exceed roughly 500 kHz in certain use cases. GaN, by contrast, can support operation at frequencies approaching 1 MHz. That distinction is becoming increasingly important as AI infrastructure evolves.

The industry's pursuit of higher efficiency and greater power density is making faster switching not merely desirable but necessary.



Solving the energy efficiency equation

The energy demands associated with AI infrastructure have become one of the defining challenges facing the technology industry. With data centre power consumption projected to rise substantially over the coming years, even small efficiency improvements can translate into significant reductions in energy usage, cooling requirements and operational costs. Murphy argues that GaN will play a crucial role in addressing those challenges.

While higher switching frequencies enable converter miniaturisation, they also create the potential for increased switching losses if unsuitable semiconductor technologies are used. Attempting to achieve 1 MHz operation with less capable devices could result in efficiency penalties that outweigh the benefits of smaller form factors. GaN changes that equation.

The technology allows designers to push switching frequencies higher while maintaining efficiency levels that remain commercially attractive. As a result, data centre designers can simultaneously pursue greater power density and improved energy performance.

Importantly, Murphy does not frame the future as an either-or battle between semiconductor technologies. Instead, he sees complementary roles for silicon, silicon carbide and GaN. Each technology occupies a particular position within the evolving power conversion landscape. However, when it comes to the highest-frequency applications emerging within AI infrastructure, GaN increasingly appears positioned as the preferred solution.

The differentiator: CGD's ICeGaN technology

While enthusiasm around gallium nitride continues to grow, competition within the GaN market is also intensifying. Manufacturers are pursuing a range of approaches to improve performance, reliability and ease of implementation.

For CGD, one of the key differentiators lies in its proprietary ICeGaN architecture and iDriver technology. Murphy highlights the company's integrated iScan interface as a particularly important innovation. The technology incorporates a Miller clamp that enables extremely rapid turn-off performance while supporting unipolar operation. This means designers do not require negative gate-drive voltages during turn-off, simplifying system implementation and improving overall efficiency. The approach also helps minimise losses associated with third-quadrant operation that can occur in more conventional GaN architectures.

For engineers, these improvements can translate into both higher efficiency and simplified system design. In practical terms, removing complexity from GaN implementation remains an important objective. While the technology's performance advantages are well understood, ease of adoption often determines how quickly new technologies move into mainstream applications. Solutions that simplify integration naturally accelerate market adoption.

Building complete power conversion platforms

Perhaps the most significant aspect of the CGD-NXP collaboration is its emphasis on system-level design.

Historically, semiconductor vendors often focused primarily on individual devices. Today's customers increasingly expect complete solutions. That expectation is particularly evident within AI infrastructure.

Rather than supplying only power switches, CGD and NXP are working together on reference platforms that combine advanced GaN devices with processing, control and management technologies.

One example involves the development of high-voltage DC power bricks for next-generation data centre applications. These platforms combine current-generation CGD devices with upcoming products still under development, providing customers access to the latest semiconductor capabilities. At the same time, NXP contributes expertise in control architectures and processing technologies. The goal is to create





validated reference designs that can be benchmarked, demonstrated and deployed more rapidly than individual component-based approaches.

This solution-oriented strategy offers several advantages.

Customers can evaluate complete architectures rather than assembling systems from disparate technologies. Development cycles can be shortened. Performance can be optimised across the entire platform rather than at the individual component level. As AI infrastructure continues evolving, such integrated approaches are likely to become increasingly influential.

Automotive: The next major opportunity

Although AI data centres are commanding enormous attention, Murphy is equally enthusiastic about the automotive sector.

The industry is currently undergoing a profound transition as manufacturers seek higher efficiency, improved performance and greater functional integration. Among the most promising opportunities is the evolution of onboard chargers.

Many automakers are exploring single-stage architectures capable of simplifying charging systems while improving efficiency. These topologies require bidirectional switching capabilities. According to Murphy, this is an area where GaN possesses a distinct advantage.

Unlike traditional silicon devices, GaN lacks a conventional body diode, allowing current to flow effectively in both directions. That characteristic makes it particularly attractive for future charger architectures. The benefits extend beyond charging systems. Traction inverter applications are also attracting growing interest.

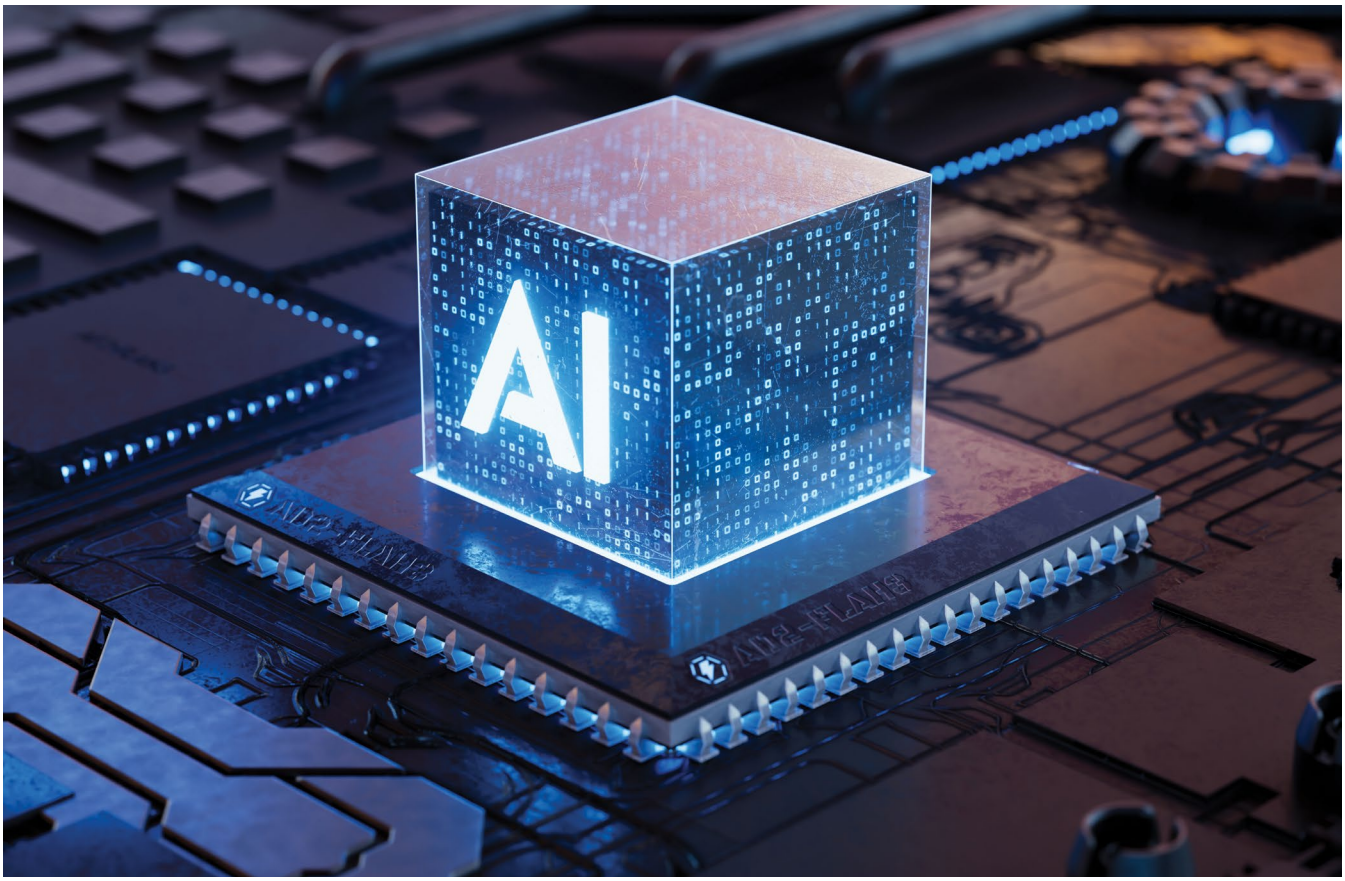
While silicon carbide currently dominates many high-voltage EV platforms, Murphy sees significant opportunities for GaN, particularly in vehicles operating on 400 V architectures. Increasing switching frequency enables cleaner motor drive waveforms and can reduce copper and iron losses within the motor itself. The result is not merely improved inverter efficiency but enhancements across the broader propulsion system. Such system-level gains are becoming increasingly important as automakers search for competitive advantages.

Reliability remains essential

Regardless of performance improvements, power electronics engineers consistently prioritise reliability. Whether the application involves a hyperscale data centre or a passenger vehicle, robust operation remains non-negotiable. Murphy believes the CGD-NXP collaboration strengthens both companies' ability to address this requirement. NXP contributes extensive automotive credibility, particularly through its longstanding relationships with OEMs and Tier 1 suppliers. Its reputation in microcontrollers, gate drivers and automotive-grade electronics provides confidence for customers considering next-generation power architectures.

The companies are already collaborating on projects involving major automotive manufacturers. One example involves a GaN traction inverter programme with a leading German automotive OEM, utilising CGD's advanced 9mΩ device technology alongside NXP gate-drive solutions. These projects provide valuable opportunities to validate GaN technology under demanding real-world conditions.

At the device level, CGD has also focused heavily on robustness. Murphy points to work conducted with Virginia Tech that demonstrated the resilience of the iScan architecture. Conventional GaN HEMTs often tolerate transient voltages only within limited ranges. Testing has shown that CGD's technology can withstand significantly higher voltage stress than many standard devices. Those results provide additional confidence as engineers evaluate GaN for mission-critical applications.



The industry's growing confidence in GaN

Perhaps one of Murphy's most notable observations concerns the changing perception of GaN within the automotive industry. Only a few years ago, many vehicle manufacturers viewed GaN largely as an exploratory technology. Interest existed, but commercial deployment remained distant. That mindset has shifted dramatically. Over the past 18 months, CGD has observed increasing engagement from OEMs, Tier 1 suppliers and engineering teams evaluating GaN for future vehicle platforms.

Several factors are driving the change.

One is the expectation that GaN costs will continue to improve as production volumes increase and manufacturing ecosystems mature. Another is growing awareness of the broader system-level benefits offered by the technology. GaN's lateral structure enables the integration of additional functions directly onto the semiconductor die. Features such as temperature monitoring and current sensing become easier to incorporate within future designs. These capabilities align well with industry trends toward smarter and more integrated power electronics.

As a result, discussions have evolved significantly. Where engineers once asked whether GaN might someday become useful, they are increasingly investigating how and when it should be deployed.

Looking ahead

The roadmap for the CGD-NXP collaboration is already taking shape. New products currently under development are expected to enter sampling programmes shortly, providing the foundation for a new generation of demonstrator systems and reference designs. For data centres, these platforms will be targeted at hyperscalers and power supply manufacturers seeking solutions capable of meeting future AI infrastructure requirements. For automotive customers, work continues across traction inverters, onboard chargers and advanced power modules. Murphy expects both sectors to deliver significant opportunities over the next several years.

What makes the partnership particularly compelling is its timing.

The AI revolution is increasing demands on power delivery systems at an unprecedented rate, while the automotive industry continues its shift toward more efficient, software-defined electric vehicles. Both trends require power electronics technologies capable of delivering greater performance without sacrificing reliability. By combining CGD's gallium nitride expertise with NXP's system-level capabilities, the companies are positioning themselves at the intersection of those two powerful market forces.

For the wider industry, the collaboration reflects a broader reality: the future of power conversion will not be determined by better transistors alone. It will be defined by complete ecosystems that unite advanced semiconductors, intelligent control, robust system architectures and scalable deployment strategies.

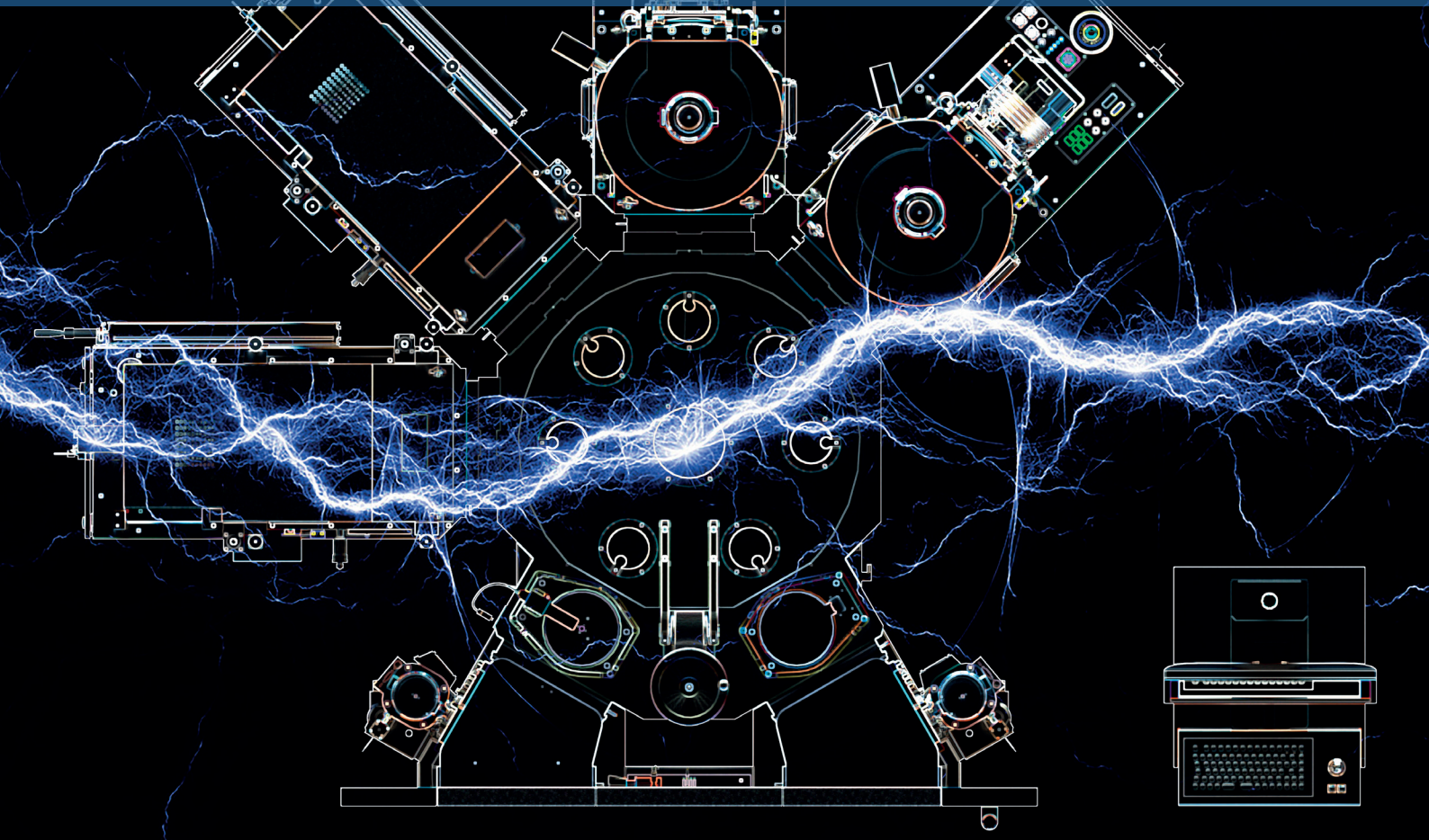
As AI infrastructure expands and vehicle electrification accelerates, GaN appears increasingly poised to move from emerging technology to mainstream solution. Partnerships such as the one between Cambridge GaN Devices and NXP may ultimately determine how quickly that transition occurs.

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From mechanical protection to intelligent power control: Why solid-state circuit breakers are poised to transform AI data centres

Frédéric Dupont, Chief Executive Officer of AlpSemi, explains how the company's recent €17 million funding round supports the industrialisation and commercial scale-up of AlpSemi's next-generation semiconductor power switches, purpose-built for solid-state circuit breakers (SSCBs) in residential and commercial buildings and 800 V direct current (DC) AI data centres.

THE GLOBAL power infrastructure landscape is undergoing one of the most profound transformations in its history. Electrification, renewable energy integration, distributed generation, software-defined energy management and the explosive growth of artificial intelligence are fundamentally changing how electricity is generated, distributed and consumed. At the centre of this shift lies an often-overlooked technology: circuit protection.

For more than a century, electromechanical circuit breakers have served as the backbone of electrical safety. They remain highly effective in traditional alternating current (AC) distribution networks, but emerging power architectures are exposing fundamental limitations, particularly as industries increasingly embrace direct current (DC) systems.

It is this challenge that French semiconductor innovator AlpSemi has set out to address. Following a €17 million funding round backed by investors including Yotta Capital, Schneider Electric Ventures and Navitas Semiconductor, the company is accelerating the industrialisation of a new generation of semiconductor power switches specifically designed for solid-state circuit breakers (SSCBs).

While AlpSemi's first products target residential and commercial electrical installations, the company's longer-term ambitions extend to one of the most exciting opportunities in power electronics today: enabling the transition toward 800 V DC AI data centres.

According to Frédéric Dupont, Chief Executive Officer of AlpSemi, the



opportunity extends far beyond simply replacing mechanical circuit breakers with semiconductor alternatives. Instead, SSCBs represent a foundational technology for the digitalisation of electrical distribution itself.

A market reaching an inflection point

AlpSemi's recent funding announcement comes at a time when interest in solid-state protection technologies is accelerating across multiple sectors.

The company was founded more than three years ago after identifying what Dupont describes as a fundamental mismatch between the requirements of modern power protection and the devices traditionally used to implement it.

"Customers were trying to use power transistors that were designed for power conversion and not for power protection," he explains.

For years, semiconductor vendors focused largely on devices optimised for power conversion applications, including power supplies, motor drives and charging systems. Protection applications, however, impose very different demands. Devices must remain continuously operational under load, present extremely low resistance during normal operation and withstand severe fault conditions when required to interrupt current flow.

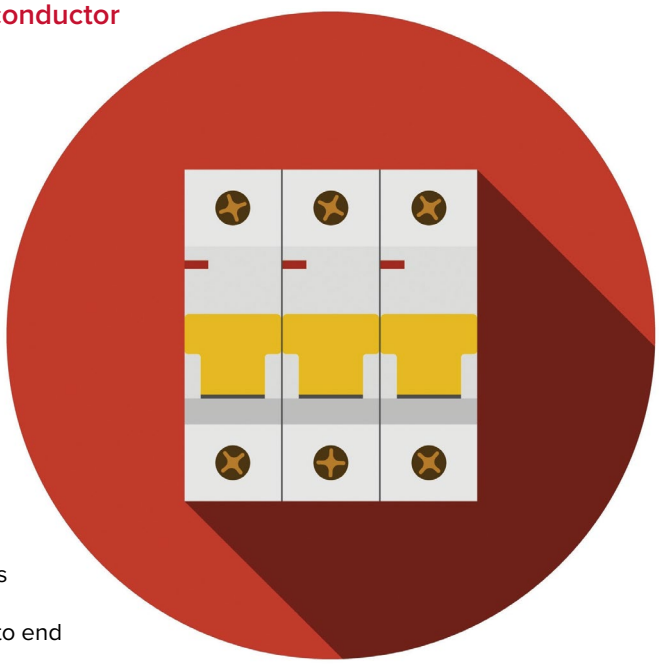
Recognising this gap, AlpSemi spent the past two years developing technology specifically engineered for solid-state circuit breaker applications rather than adapting existing semiconductor technologies designed for different purposes.

The latest investment round reflects growing confidence that the market is approaching a tipping point.

The increasing adoption of renewable energy sources, energy storage systems, electric vehicle infrastructure and AI-ready power architectures is driving demand for smarter forms of electrical protection capable of managing far more dynamic power networks than traditional systems were ever designed to handle.

Rethinking semiconductor development

One of AlpSemi's distinguishing characteristics is its vertically integrated development model. Traditionally, the semiconductor industry operates through multiple layers. Material suppliers develop substrates, device manufacturers create semiconductor components using those materials, and system designers ultimately integrate packaged devices into end products.



According to Dupont, solving the challenges of solid-state protection requires a more holistic approach: "We try to optimise everything."

That philosophy extends from material engineering and device architecture through packaging and system-level integration. The reason becomes clear when examining the technical demands placed on SSCBs.

Unlike switching devices used in power conversion applications, protection semiconductors must combine two characteristics that traditionally work against one another.

First, they require exceptionally low on-resistance because current flows through them continuously during normal operation. Lower resistance minimises energy loss and heat generation. Achieving very low resistance often requires physically larger silicon die areas.

At the same time, protection devices must withstand extremely high voltages when interrupting fault currents. Combining low resistance and high-voltage capability within a commercially viable product creates significant design challenges spanning materials science, semiconductor architecture and manufacturing processes.

By maintaining expertise across the entire stack, AlpSemi believes it can optimise performance more effectively than organisations focused on only one part of the value chain. Importantly, however, the company does not intend to become a traditional vertically integrated manufacturer.

Instead, its strategy combines internal technology development with external manufacturing partnerships, allowing innovations to scale through established production ecosystems.

Why mechanical circuit breakers have reached their limits

The emergence of SSCBs is not driven by technology trends alone. It is increasingly being dictated by physics.

Traditional electromechanical circuit breakers work by physically separating electrical contacts to interrupt current flow. In AC systems, this approach benefits from the fact that current naturally crosses zero multiple times each second, helping extinguish arcs generated when contacts separate.

For more than 100 years, this approach has proven remarkably effective. However, direct current systems introduce a fundamentally different challenge.

"When you move to DC electrical distribution or to a mix between AC and DC, electromechanical technologies will not be sufficient," says Dupont.

The primary issue is arc management.



In DC environments, electrical arcs generated during circuit interruption do not naturally extinguish in the same way they do in AC systems. Instead, they can continue conducting current, making reliable interruption significantly more difficult.

As power networks become increasingly dependent on DC architectures, the limitations of mechanical protection become more apparent.

Solid-state approaches replace mechanical contacts with semiconductor switches capable of interrupting current electronically. The performance difference is dramatic.

According to Dupont, SSCBs can interrupt fault currents in approximately one microsecond compared with the millisecond-scale response times typical of electromechanical alternatives. That thousand-fold improvement creates benefits extending well beyond faster protection. More rapid interruption dramatically reduces fault energy, improving safety while minimising damage to equipment throughout the power system.

The digitalisation of electrical distribution

While speed is an important advantage, Dupont argues that the real value of solid-state protection lies elsewhere.

The transition from mechanical to semiconductor-based protection effectively transforms circuit breakers into intelligent nodes within the electrical network.

Historically, circuit protection devices performed a single task: disconnecting circuits during fault conditions. Future SSCBs will perform many additional functions simultaneously. They can monitor current continuously, provide detailed metering information, enable remote control, support dynamic load management and interact directly with software-based energy management systems.

In essence, protection devices become part of a broader digital infrastructure. This capability is becoming increasingly important as electrical consumption patterns grow more complex.

Modern buildings are no longer passive consumers of electricity. Many generate power through rooftop solar systems, store energy within batteries and interact dynamically with utility networks. Electricity can be generated, consumed, stored and exported simultaneously. Managing such environments requires intelligence that traditional protection architectures simply cannot provide.

According to Dupont, SSCBs create the foundation for this next-generation approach to electrical control: “The historical breakers are becoming a very smart electrical management platform.”

The building as an intelligent energy hub

AlpSemi’s first commercial platform, the AS800, targets residential and commercial installations where the company sees immediate opportunities for intelligent protection systems.

The motivation is straightforward.

Today’s electrical panels often require separate devices to provide protection, switching, metering, communication and monitoring functions. Each function adds complexity, hardware and installation costs. An SSCB-based architecture allows these capabilities to be consolidated within a single intelligent device. The breaker itself becomes a computing platform containing an embedded microcontroller capable of executing advanced software algorithms.

Looking forward, Dupont anticipates increasing levels of intelligence, potentially including artificial intelligence functions capable of analysing network behaviour and optimising protection decisions. This evolution reflects broader trends throughout infrastructure management.

As energy costs fluctuate and electrical grids become more dynamic, buildings increasingly require tools that can optimise consumption automatically and adapt to changing conditions. Rather than acting solely as safety devices, protection systems become active participants in overall energy management strategies.

The AI data centre opportunity

Although residential and commercial markets provide an important entry point, Dupont makes it clear that AI data centres represent one of the company’s most significant long-term opportunities.

Over the past 12 to 18 months, industry momentum behind 800 V DC architectures has accelerated dramatically. The reason is simple: AI infrastructure demands unprecedented amounts of power.

Traditional AC power distribution schemes introduce multiple conversion stages between incoming utility electricity and the processors performing AI workloads. Each conversion step creates losses and adds complexity.

Higher-voltage DC architectures offer a pathway toward improved efficiency and power density. However, they also introduce significant protection challenges.

As Dupont notes, DC environments fundamentally require solid-state protection due to the difficulties associated with interrupting high-energy DC faults. At the same time, next-generation AI facilities require semiconductor switches capable of simultaneously achieving exceptional voltage performance and ultra-low resistance. Current semiconductor technologies are approaching their limits in this regard.

As a result, AlpSemi is developing a new technology platform designed to extend performance beyond what existing gallium nitride and silicon carbide solutions can deliver. The company is targeting substantially higher voltage operation while maintaining the efficiency required by future AI infrastructure.

Dupont explains: “We need very high voltage protection. We need to have the lowest possible resistance to limit the heat and improve heat management in the data centre.”

For operators already struggling with thermal constraints, those benefits could prove highly significant.

Enabling energy efficiency through software

The rise of software-defined infrastructure extends well beyond data centres. According to Dupont, semiconductor-based power protection creates opportunities to fundamentally optimise electrical consumption across entire buildings, facilities and networks. Because SSCBs inherently provide sensing, control and communication capabilities, they generate the data required for advanced energy management.

Electrical loads can be monitored at a granular level. Individual circuits can be activated or deactivated remotely. Consumption patterns can be analysed and optimised automatically. These capabilities create a foundation for intelligent energy management strategies based on real-world operating conditions.

For example, buildings may choose to increase electricity consumption during periods of grid surplus and low prices while reducing demand during periods of peak pricing or constrained supply. Such optimisation requires continuous visibility and control across the electrical network.

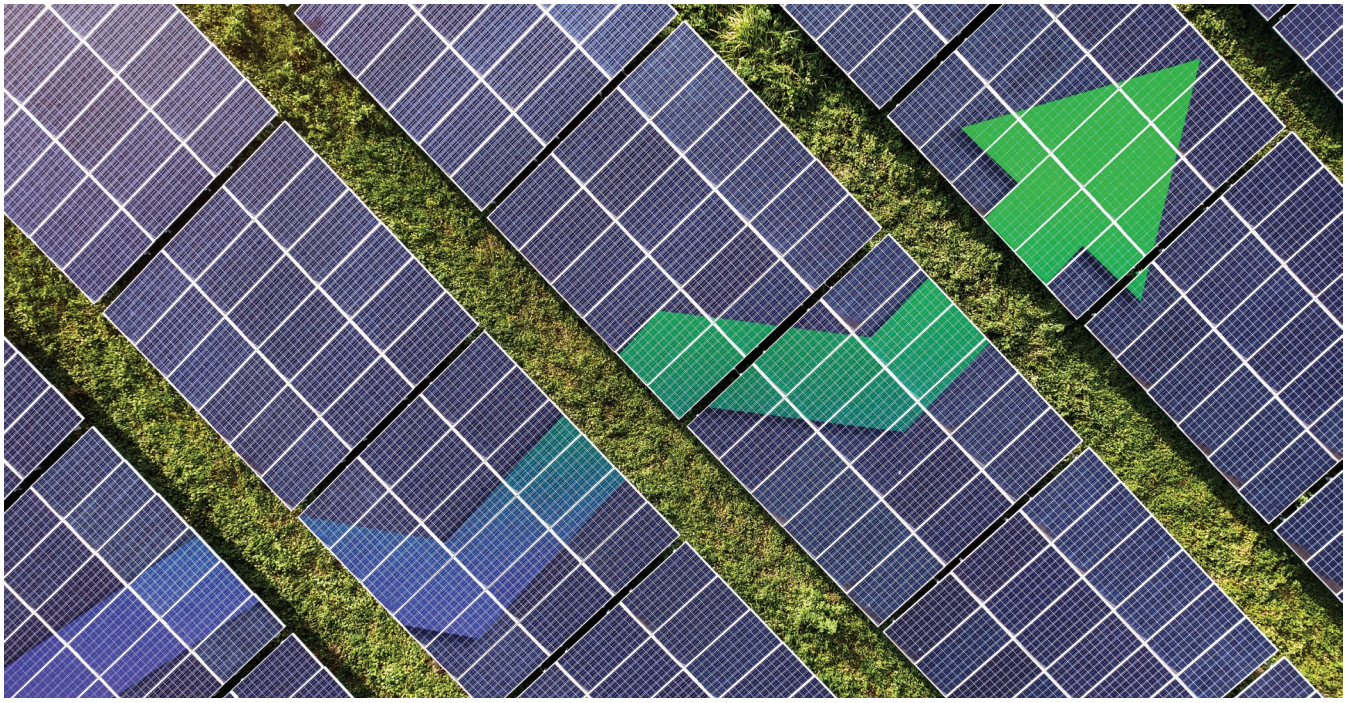
“Optimisation is software,” says Dupont. “Optimisation is also having the right intelligence or AI.”

In this sense, SSCBs become a key enabling technology for the broader digitisation of electricity.

Strategic partnerships driving adoption

The composition of AlpSemi’s investor base offers insight into how the company plans to translate technological innovation into commercial success. The funding round combines financial and strategic investors whose expertise aligns closely with the company’s market focus.

Yotta Capital provides financial support while sharing AlpSemi’s vision for technologies capable of improving energy efficiency and reducing carbon emissions. Meanwhile, Schneider Electric Ventures brings significant domain expertise in electrical distribution and protection. Schneider Electric has worked closely with AlpSemi since the company’s early stages, helping validate product



requirements, safety considerations and certification pathways.

For a company operating within highly regulated infrastructure markets, such partnerships can be invaluable.

Protection systems must satisfy extensive qualification, reliability and safety requirements before achieving widespread deployment. Direct engagement with established industry leaders helps ensure products address real-world customer needs while meeting regulatory expectations.

The involvement of Navitas Semiconductor adds another strategic dimension. With extensive exposure to high-performance power systems and data centre applications, Navitas provides valuable insights into the rapidly evolving infrastructure requirements associated with AI-driven computing growth.

Together, these partnerships create a powerful framework for commercial expansion.

Scaling semiconductor innovation

Developing breakthrough semiconductor technologies is notoriously difficult and capital intensive. Dupont acknowledges that while €17 million represents a significant milestone, semiconductor innovation requires careful allocation of resources.

The funding will serve two parallel objectives. The first is expanding commercial operations around the AS800 platform and supporting market entry activities across Europe and eventually North America. The second is advancing the company's next-generation platform targeting AI data centres and high-voltage DC infrastructure.

This development effort represents a substantial technical undertaking involving collaboration with major industrial partners across Europe, Asia and the United States. Fortunately, AlpSemi's manufacturing strategy is designed specifically to facilitate scaling. The company operates using a fab-light model that combines deep technology ownership with external manufacturing partnerships. Rather than constructing expensive fabrication facilities, AlpSemi develops technologies compatible with established manufacturing ecosystems.

Over the coming years, AlpSemi plans to expand progressively from low-voltage AC applications into medium- and high-voltage DC protection markets. The roadmap encompasses residential systems, commercial infrastructure, AI data centres, industrial platforms and eventually automotive applications built around emerging 800 V ecosystems. The goal is not simply to compete with established power semiconductor manufacturers.

Its first products, for example, are produced through a foundry partner in Germany using adapted versions of existing process technologies. This approach enables faster commercial scaling while minimising capital requirements. It also allows the company to focus resources on innovation rather than manufacturing infrastructure.

The future is software defined

Looking beyond individual products, Dupont believes the future of electrical distribution will increasingly be defined through software. Different markets face different regulatory requirements, grid conditions and infrastructure challenges. Historically, accommodating those differences often required region-specific hardware designs. Software-centric architectures offer a more efficient alternative.

A common hardware platform can be adapted through firmware and software configuration, enabling manufacturers to support diverse regional requirements while maintaining economies of scale. Parameters such as protection thresholds, operating ranges and response behaviours can be adjusted through software rather than redesigning hardware. This flexibility is particularly valuable within rapidly evolving energy systems. As electrification continues to accelerate, software-defined infrastructure may prove essential for balancing standardisation with local adaptation.

Building a global champion for intelligent protection

Over the coming years, AlpSemi plans to expand progressively from low-voltage AC applications into medium- and high-voltage DC protection markets. The roadmap encompasses residential systems, commercial infrastructure, AI data centres, industrial platforms and eventually automotive applications built around emerging 800 V ecosystems. The goal is not simply to compete with established power semiconductor manufacturers. Instead, Dupont sees AlpSemi as an innovation catalyst capable of accelerating the development and adoption of technologies specifically optimised for power protection.

By focusing exclusively on this growing market segment, the company hopes to drive innovation faster than larger competitors balancing broader portfolios.

As artificial intelligence drives unprecedented infrastructure investment and power consumption continues its global rise, electrical protection is moving from a background consideration to a strategic technology. The transition from mechanical circuit breakers to intelligent semiconductor-based protection may ultimately prove as significant as the shift from analogue to digital communications.

For AI data centres, distributed energy systems and software-defined electrical networks, SSCBs are no longer simply a new type of breaker. They are becoming the foundation for a smarter, faster and more intelligent power infrastructure. And if AlpSemi's vision proves correct, the real revolution is only just beginning.

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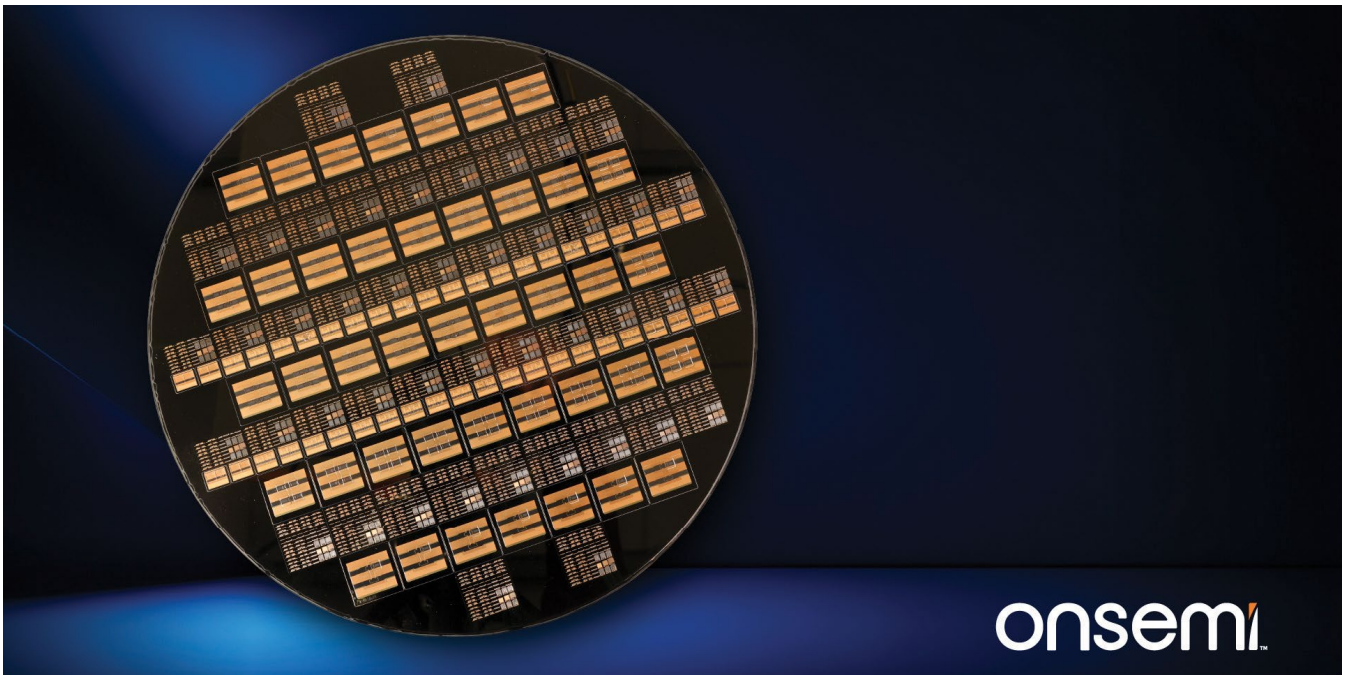
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Onsemi takes power integration to the wafer

With dies embedded directly into a silicon wafer, onsemi is targeting higher density, better thermal performance and tighter integration in AI and electric vehicle applications.

BY REBECCA POOL, TECHNOLOGY EDITOR

TARGETING the soaring power demands of AI infrastructure, onsemi has developed a silicon-wafer-based architecture that embeds multiple power and control dies within a single power module. The Embedded Power Platform promises three to five times higher power density than conventional approaches, depending on the application, while simplifying system-level integration.

“For decades, the semiconductor and the package have been treated as separate technologies. The Embedded Power Platform changes that by making the silicon itself part of the system architecture,” highlights Hassane El-Khoury, President and CEO of onsemi. “The platform brings together advanced semiconductor technologies, manufacturing and system-level optimization into a common architecture that can evolve alongside future innovations.”

In one of its EPP-based solid-state circuit-breaker designs for an AI rack, onsemi claims the design was around 50% smaller and 20% cooler than existing designs. According to the firm, by reducing packaging and using the full EPP footprint to conduct heat, multiple dies can be packed closer together - so the platform can support more compact power systems, improve thermal management and enable greater power density in AI infrastructure.

Meanwhile, in electric vehicle applications, the platform is said to provide up to four times higher power density and 15% lower power losses compared to conventional approaches, delivering smaller, lighter and more efficient inverter designs.

“This approach will redefine how power systems are built and create a new foundation for AI infrastructure, electrification and automation,” says El-Khoury.

Meet the platform

As AI, automotive and industrial systems demand more power in less space, designers face mounting pressure to improve efficiency while managing heat, size and cost. The EPP is a silicon wafer embedded power module designed to optimise electrical, mechanical and thermal performance within a single architecture. Here, individual silicon, silicon carbide and gallium nitride dies can be directly embedded into a 300 mm (12 inch) silicon wafer. These dies can be connected through wafer-level redistribution layers – this interconnect structure is fabricated using wafer-level semiconductor processes.

Importantly, the wafer is now functioning as the basis of the power module rather than a substrate from which the active devices are fabricated. According to onsemi, the design also integrates electrical, mechanical and thermal considerations from the

outset, which transforms the package from passive housing into an 'active contributor to system performance'.

Allyson Fairchild, Automotive Field Applications Engineer and Strategic Project Lead - Corporate Strategy and Advanced Projects at onsemi, emphasises how the platform supports myriad applications and different semiconductor materials, and is scalable across multiple power levels. "We can embed heterogeneous dies within the package... that could be the major power devices - MOSFETs and JFETs," she says. "But we can also embed controls, drivers and other supporting power devices – this enables really tight electrical coupling and we're reducing complexity at the system level."

"This allows us to get the most out of these products," she adds. "Customers are getting a product that is easier to integrate into, say, their data centre rack or any other application."

Onsemi has been working on designs that use half bridges for traction applications as well as multiple FETs connected in parallel for lower on-resistance, and dies connected to controller dies to minimise the loop inductance. "Whatever the application requires we can embed the dies and connect them into the [necessary] configuration," points out Fairchild. "This will also evolve with semiconductor innovation, and having this technology-agnostic platform will allow us to take the technology far into the future."

"The sky's the limit here – we really have the opportunity to be inventive," she says.

Instead of relying on conventional wire bonds and other assembly-level connections, the platform uses wafer-level metallization to form precise copper interconnects – an approach that reduces parasitic inductance, improves device control and enables high switching frequencies. "This is about getting performance into the system. We know what our bare silicon carbide dies are capable of, but when you connect [these] into the system, you can be introducing parasitics that then degrade that performance," says Fairchild. "But with this architecture, we can get more performance out of the die we already have."

Given onsemi's work with vertical GaN, minimising parasitic inductance and improving device control will be key to performance at higher switching frequencies. "We can now use these devices much more effectively," she adds.

Silicon architecture

Embedded in a silicon-based package, onsemi's power platform can use existing fab infrastructure as well as mature validation, simulation and digital twin tools, to provide a faster time to market. Onsemi reckons the platform can accelerate development cycles to as little as four months and help designers to identify design trade-offs earlier, reducing costly late-stage changes.

The silicon architecture promises to deliver low-resistance thermal conduction, rather than having portions of the package occupied by poorly conducting mould compounds and other materials. It also integrates high-voltage isolation into the package, potentially reducing dependence on insulating thermal interface materials (TIMs) and conventional direct bonded copper (DBC) arrangements.

"We're able to extract heat to drive better performance of the die within the package," says Fairchild. "We can use high-quality fab processes to get high-voltage isolation embedded directly into this package, enabling a more thermally efficient package and highly integrated power architectures within the package itself."

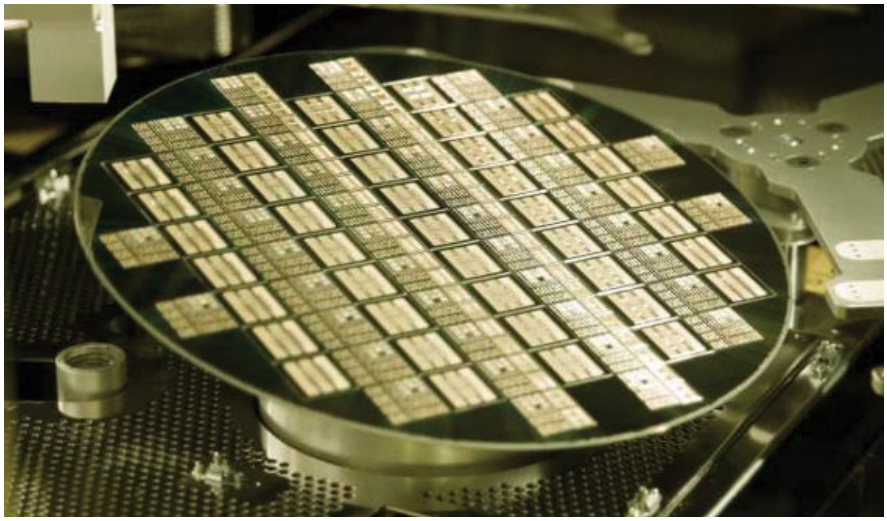
Looking ahead, the EPP could also integrate devices built on onsemi's Treo analog and mixed-signal platform alongside its power technologies. "We have the power, we have the intelligence, and now we have the integration," says Fairchild, pointing to increasingly integrated power, control and supporting functions in future designs.

"In AI data centres we can draw more power out of the die and better extract the heat and in automotive, we're getting more efficiency and more range," she adds.

Indeed, onsemi has just joined forces with Subaru – together the partners will evaluate how the EPP can support electric vehicle traction inverter architectures. According to Fairchild, the Japanese car manufacturer will be using onsemi's simulation models and engineering samples to understand how the platform can drive power system design, improve efficiency and support future architectures in hybrid and electric vehicles. "Subaru is the first partnership we have announced here," she says. "Advancing the embedded power platform into the customer evaluation phase and having this interaction is very exciting."



Hassane El-Khoury, President and CEO onsemi



Onsemi's Embedded Power Platform uses the silicon wafer as the package, and can integrate Si, SiC and GaN dies as well as drivers, controllers and other supporting power devices. [onsemi]

Why 48 V is becoming the practical intermediate bus for high-power AI servers

As AI server power rises into the multi-kilowatt range, moving from 12 V to 48 V can significantly reduce distribution current, conductor losses and connector stress, but it also changes where conversion losses, thermal challenges and protection requirements appear.

BY POWERNEXU TECHNOLOGY

AI SERVERS are changing the assumptions that shaped conventional server power architectures.

A traditional enterprise server might once have operated comfortably within a few hundred watts or around 1 kW. Today, GPU-intensive AI platforms can require several kilowatts per server, while rack-level power continues to increase as more accelerators are packed into each system.

As power rises, the design challenge is no longer limited to converting AC input power efficiently. Engineers must also move that power through the rack and across the server without creating excessive current, copper requirements, voltage drop, connector heating and thermal stress.

This is where 48 V distribution becomes increasingly attractive.

A 48 V architecture does not eliminate the low-voltage rails required by CPUs, GPUs, memory and accelerator devices. Instead, it allows the higher-power portion of the distribution path to operate at a higher voltage and lower current, while final conversion takes place closer to the load.

That change can have a significant impact on the electrical and mechanical design of high-power AI systems.

Why 12 V becomes difficult at multi-kilowatt power levels

The fundamental relationship is straightforward:
Power = Voltage × Current

For a fixed power level, a lower distribution voltage requires a higher current.

- At 1 kW, a nominal 12 V bus carries approximately 83 A.
- At 3 kW, the current rises to around 250 A.
- At 6 kW, it reaches approximately 500 A.

Once server power reaches this range, current handling



becomes one of the dominant design constraints.

Higher current requires more conductor cross-sectional area. PCB power planes may need to become thicker, wider or paralleled across multiple layers. Busbars become larger. Connectors require greater contact area, more terminals or more robust mechanical interfaces.

The consequences extend beyond conductor size.

Any resistance in the power path produces heat according to:
PLOSS = I^2R

Because current is squared, even very small resistances become important when current rises into the hundreds of amperes.

Connector contacts, busbar joints, PCB vias, cables and mechanical interfaces may each contribute only milliohms or fractions of a milliohm, but the resulting losses can become significant.

Voltage drop also becomes more difficult to manage.

A drop of several hundred millivolts may appear modest in absolute terms, but it represents a meaningful fraction of a 12 V distribution rail and reduces the available voltage margin at downstream converters.

This does not make 12 V unsuitable for all servers. It remains practical for many conventional compute, storage and enterprise platforms.

The challenge appears when the power level rises enough that current becomes the dominant physical limitation.

Worked example: 12 V vs 48 V at the same server power level

Consider a server requiring **6 kW** of power.

Ignoring conversion losses for the moment, the distribution current would be:
At 12 V
6,000 W ÷ 12 V = **500 A**

At 48 V
6,000 W ÷ 48 V = **125 A**

The 48 V bus therefore carries only one quarter of the current.

Now assume, purely for comparison, that the total resistance of the distribution path is **0.5 milliohm**.

Using:
PLOSS = I^2R
the difference becomes significant.

Parameter	12 V Bus	48 V Bus
Server power	6 kW	6 kW
Distribution voltage	12 V	48 V
Distribution current	500 A	125 A
Assumed path resistance	0.5 mΩ	0.5 mΩ
I^2R loss	125 W	7.8 W
Voltage drop	0.25 V	0.0625 V

For the same assumed path resistance, increasing the voltage by a factor of four reduces current by a factor of four and theoretical resistive loss by a factor of sixteen.

In a real server, the engineer would not necessarily keep conductor dimensions identical. Some of the current advantage may instead be used to reduce copper volume, connector size or busbar mass.

That is one of the most important benefits of moving to a higher-voltage distribution bus: it creates additional engineering margin.

The voltage-drop difference is also important.

A 0.25 V drop represents more than 2% of a nominal 12 V rail, while 0.0625 V represents only a small fraction of a 48 V bus.

At multi-kilowatt power levels, this influences not only electrical efficiency but also connector temperature, PCB stack-up, busbar geometry, mechanical packaging and cooling requirements.

How 48 V changes the power-distribution path

Moving from 12 V to 48 V changes where high current exists inside the system.

In a traditional architecture, an AC-DC power supply may generate a 12 V output that is distributed through the chassis. Point-of-load regulators then convert that 12 V rail into the lower voltages required by CPUs, GPUs, memory and other devices.

At several kilowatts, a large portion of the internal distribution system must therefore carry hundreds of amperes.

With a 48 V architecture, the AC-DC stage produces a higher DC voltage. The rack busbar, server input connector and upstream internal distribution path can therefore operate at approximately one quarter of the current required by a 12 V bus at the same power level.

The important point is that 48 V does not eliminate high current.



Figure 1: Current and resistive-loss comparison for a 6 kW server using 12 V and 48 V distribution. At the same power level, the 48 V bus reduces current from 500 A to 125 A and substantially reduces I^2R losses for an equivalent distribution resistance.

It changes where that high current appears.

For example, a rack carrying tens of kilowatts at 48 V can still require several hundred amperes. However, compared with distributing the same power at 12 V, the current is dramatically lower.

This reduces the burden on long conductors and shared interfaces.

Lower current can reduce the amount of copper required in busbars, cables and PCB planes. It can also reduce the thermal sensitivity of connector contact resistance.

At very high current, even a small increase in contact resistance caused by ageing, contamination, mechanical tolerance or repeated hot-swapping can create noticeable local heating.

By reducing upstream current, 48 V gives designers more flexibility to balance conductor size, connector design, temperature rise, cost and power density.

Moving conversion closer to the load

The main trade-off is obvious: processors do not operate directly from 48 V.

The voltage must still be stepped down before it reaches CPUs, GPUs and memory.

One approach is to distribute 48 V into the server or compute tray and convert it locally to an intermediate voltage such as 12 V. Final point-of-load regulators then generate the lower rails required by the silicon.

Another approach moves higher-ratio conversion even closer to accelerator boards.

The architectural objective is not to eliminate low-voltage, high-current operation entirely. That is impossible near a high-power processor.

Instead, the objective is to make the low-voltage, high-current path as short as practical.

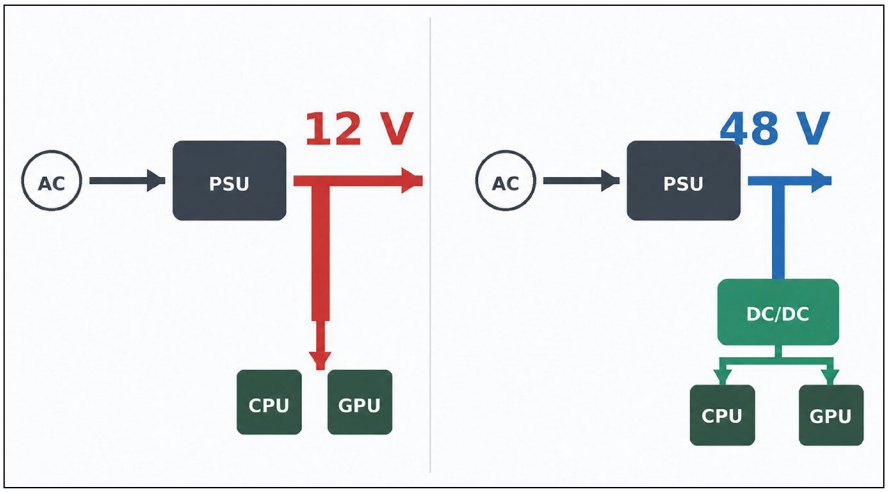
A traditional architecture may be simplified as:
AC input → AC-DC PSU → 12 V distribution → VRM → CPU/GPU

A 48 V architecture may instead look like:
AC input → AC-DC PSU → 48 V distribution → local DC-DC conversion → VRM → CPU/GPU

This architectural shift moves some of the design challenge away from the main distribution bus and towards the local converter.

That creates a different set of engineering requirements.

High-ratio DC-DC converters must provide high efficiency, strong transient response and high power density while operating close to thermally demanding processors.



➤ Figure 2: Simplified comparison of a traditional 12 V server power architecture and a 48 V intermediate-bus architecture. In the 48 V system, high-current low-voltage conversion is moved closer to CPUs and GPUs, reducing the distance over which very high current must travel.

Magnetics, semiconductor switching losses, control topology, cooling and board area all become important.

The best architecture is therefore not necessarily the one with the fewest conversion stages.

A system with an additional conversion stage may still achieve better overall performance if it substantially reduces distribution losses, conductor volume and connector heating.

The correct comparison must be made at system level rather than converter level alone.

Redundancy and fault behaviour

AI infrastructure cannot sacrifice availability in exchange for power density.

Redundancy, hot-swap capability and fault isolation remain essential.

At rack level, multiple power modules may be configured in N+1 or other redundant arrangements. The power shelf must manage current sharing between modules while continuing to support the load during insertion, removal or failure of an individual unit.

A higher distribution voltage can make individual module current more manageable, but the total energy available on the DC bus can still be substantial.

This makes protection architecture particularly important.

Hot-swap controllers, electronic fuses, MOSFET-based protection stages or mechanical contactors may be used to control inrush current and isolate faults.

Pre-charge behaviour is also important.

Large downstream capacitances can draw very high inrush current if connected directly to a low-impedance source. An uncontrolled inrush event may stress connectors, switching devices or upstream power modules.

Fault interruption also requires special attention in DC systems.

Unlike AC, DC current does not naturally cross zero every half cycle. As a result, interruption devices must

be selected for their DC breaking capability rather than only their steady-state current rating.

The architecture must also define fault domains carefully.

A failure in one accelerator tray should ideally be isolated without collapsing the shared rack bus or interrupting unrelated compute resources.

Current sharing, protection coordination, over-current thresholds and failure sequencing therefore become part of the overall 48 V architecture rather than isolated PSU functions.

Efficiency and thermal trade-offs

It is tempting to describe 48 V as automatically more efficient than 12 V.

The reality is more nuanced.

The distribution advantage is clear: reducing current lowers resistive losses in cables, busbars, connectors and PCB planes.

However, local conversion from 48 V introduces its own losses.

If an additional DC-DC stage is required, the efficiency of that stage must be included in the total system calculation.

A designer therefore needs to compare:
distribution loss saved
against
additional conversion loss introduced.

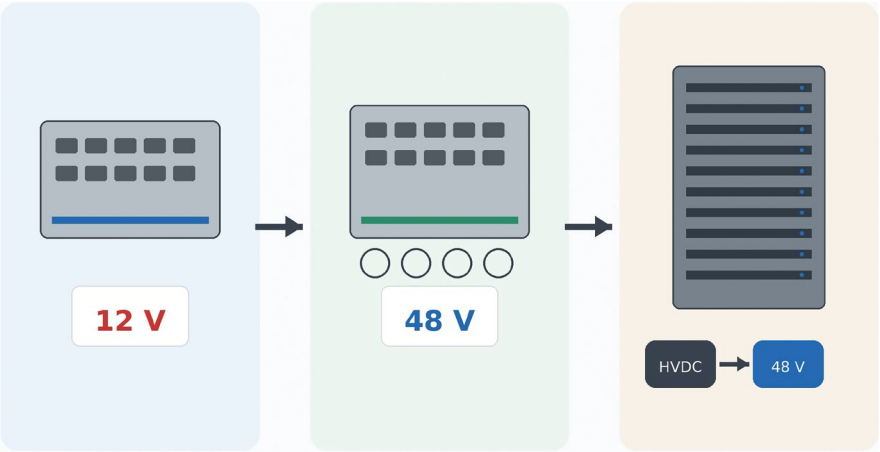
The answer depends on power level, conductor length, converter efficiency, mechanical layout, cooling architecture and load profile.

In a lower-power server with a very short 12 V distribution path, the benefit of moving to 48 V may be limited.

In a multi-kilowatt GPU server, where 12 V distribution would require several hundred amperes over meaningful physical distances, the balance changes considerably.

Thermal location also matters.

Ten watts of heat distributed over a large busbar or cable assembly does not create the same thermal challenge as ten watts concentrated inside a compact converter located next to a GPU.



➤ Figure 3: Possible evolution of AI power distribution. Conventional systems may distribute 12 V directly inside the server; current high-power architectures increasingly use 48 V intermediate buses; future ultra-high-power racks may use higher-voltage DC distribution before stepping down closer to the compute load.

For this reason, system efficiency cannot be evaluated only as a single percentage.

Engineers must consider where the losses occur and how easily those losses can be removed.

This becomes especially important as AI systems adopt direct liquid cooling.

Once CPUs and GPUs transfer a larger fraction of their heat directly into a liquid loop, air-cooled power components, connectors and conversion stages can represent a more important part of the remaining chassis thermal load.

Reducing upstream conduction losses can therefore provide benefits beyond the electrical efficiency number alone.

Where 48 V makes practical sense

The strongest case for 48 V appears where three conditions occur together: high power, meaningful distribution distance and tight constraints on copper, connector size or thermal performance.

This includes high-density GPU servers, accelerator trays, HPC platforms and rack architectures where a 12 V backbone would otherwise require several hundred amperes.

In these applications, 48 V offers an effective engineering compromise. It significantly lowers current without moving the entire server into a much higher-voltage operating environment.

However, 48 V should not be considered a universal replacement for 12 V.

Conventional servers with lower power requirements can continue to use 12 V effectively, particularly where existing infrastructure, components and service practices are already optimised around it.

At the other end of the spectrum, 48 V may eventually become insufficient as rack power moves towards several hundred kilowatts or even higher.

At such levels, distributing all rack power at approximately 48 V would again create very large currents.

The industry is therefore investigating higher-voltage DC distribution for future AI infrastructure.

One possible architecture is to use a much higher voltage for facility-to-rack or rack-level transmission, then convert down to a 48 V-class intermediate bus closer to the compute equipment.

A simplified progression could therefore look like:
Conventional server
AC ➔ PSU ➔ 12 V ➔ CPU/GPU power stages

High-power AI server
AC ➔ PSU ➔ 48 V ➔ local DC-DC ➔ CPU/GPU power stages

Future ultra-high-power AI rack
Facility power ➔ higher-voltage DC distribution ➔ rack conversion ➔ 48 V-class intermediate bus ➔ local DC-DC ➔ CPU/GPU

The important trend is not that one voltage will permanently replace another.

Rather, the power-distribution architecture is becoming increasingly hierarchical.

Higher voltage is used where power must travel over longer distances, while lower voltage is created progressively closer to the components that actually require it.

This is the same fundamental principle that has shaped power transmission at much larger scales: avoid moving very high current any farther than necessary.

For today's multi-kilowatt AI servers, 48 V therefore represents a practical intermediate point.

It substantially reduces current compared with 12 V, remains compatible with modular rack-level power architectures, and allows the final high-current conversion stages to be placed close to CPUs and GPUs.

Its value is not simply that 48 is greater than 12.

Its value is that it changes the balance between current, copper, efficiency, connector stress, thermal management and conversion complexity.

As AI compute density continues to rise, system designers will increasingly need to decide not only how efficiently power is converted, but also where each conversion should occur and at what voltage power should travel between those points.

That architectural decision may ultimately be just as important as the efficiency of the individual power supply itself.

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AI infrastructure requirements evolving beyond raw compute capacity

Pietro Scalia, Head of Power System Architecture and Marketing at Renesas Electronics, explains how AI's burgeoning power demands, amplified by inference workloads, are triggering a fundamental redesign of infrastructure architectures.

FOR MUCH of the artificial intelligence boom, the conversation has been dominated by compute. The race to build larger and more powerful AI models created unprecedented demand for GPUs, accelerators and high-performance compute clusters. However, as the industry transitions from a training-centric era toward one increasingly defined by inference, agentic AI and eventually physical AI, the constraints shaping infrastructure design are changing.

According to Scalia, the next phase of AI infrastructure will be determined not simply by how much compute can be deployed, but by how effectively systems can power, connect, manage and cool that compute.

"The training age has now started transitioning to inference and agentic AI," says Scalia. "It's a completely different scenario."

As AI infrastructure evolves, technologies such as digital power delivery, memory interfaces, advanced semiconductor packaging and embedded intelligence are becoming every bit as important as the processors they support.

The result is a fundamental rethink of data centre architecture, creating new opportunities and challenges across the entire power electronics ecosystem.

From training to inference: A different infrastructure problem

The first wave of generative AI deployment was focused primarily on training increasingly sophisticated foundation models. Training workloads demand enormous compute clusters operating at maximum performance for extended periods. As organisations move towards deploying AI at scale, however, inference is rapidly becoming the dominant workload.

Inference presents different performance characteristics and places new demands on infrastructure.

One of the most significant factors is memory. While AI processors continue to grow in size and capability, memory capacity and bandwidth have emerged as critical bottlenecks. Scalia points to the rapid evolution of leading accelerator roadmaps as evidence of how difficult balancing compute and memory requirements has become.

As GPU vendors push toward increasingly powerful chiplet-based architectures, they face growing challenges around integrating memory while simultaneously managing escalating power consumption. Designs originally intended to combine multiple high-power compute dies within a single package have encountered practical limitations related to power delivery, thermal management and memory integration.

The result is a growing recognition that simply adding more compute is no longer sufficient. Instead, future AI platforms will depend on balancing processing capability with efficient memory access and data movement. This becomes particularly important as inference workloads expand and AI systems increasingly need to respond in real time. Memory performance is therefore becoming inseparable from overall system performance.

“The challenge is really driven by the amount of memory,” Scalia explains. “The more we move closer to agentic AI, memory will still be very important.”

This trend extends beyond hyperscale data centres. As AI functionality begins moving closer to end devices and edge environments, memory constraints will follow. Whether supporting inference in cloud-scale facilities or enabling physical AI applications in intelligent systems, efficient memory architectures will remain central to performance.

The new bottleneck: Delivering power at scale

While memory may be one critical constraint, power delivery is emerging as another.

Historically, power was considered a supporting function within computing systems. Today, however, delivering energy efficiently to increasingly power-hungry processors has become a central engineering challenge. Modern AI accelerators already consume extraordinary amounts of power. Future generations are expected to push this further, demanding thousands of amps delivered with microscopic precision and near-instantaneous response times.

“The challenge is when we are talking about 6,000 amps, 8,000 amps, 10,000 amps,” says Scalia.

At these levels, power delivery ceases to be solely an electrical engineering problem. Instead, it becomes an interconnected electromechanical and thermal design challenge. Power semiconductor innovation is therefore shifting beyond individual devices and towards sophisticated packaging approaches that integrate multiple elements into highly compact power delivery systems. Manufacturers are increasingly incorporating capacitors, thermal structures and potentially inductive components directly within advanced power packages.

As current requirements climb, innovations in three-dimensional power architectures are becoming essential.

“It’s not really about the chip itself only,” Scalia notes. “It’s the way the chip can convey the current to the XPU and the way the chip can dissipate heat.”

The consequence is a new wave of research and development centred on packaging, current distribution, thermal performance and integration density.

Why 800-volt architectures are becoming the new standard

One of the most visible examples of this transformation is the industry’s growing adoption of 800-volt DC power distribution architectures. Until recently, 48 V systems represented the dominant approach for modern server power distribution. However, the rapid increase in rack power densities has exposed limitations in lower-voltage architectures. Once rack power exceeds roughly 250 kW to 350 kW, current levels become increasingly difficult to manage efficiently.

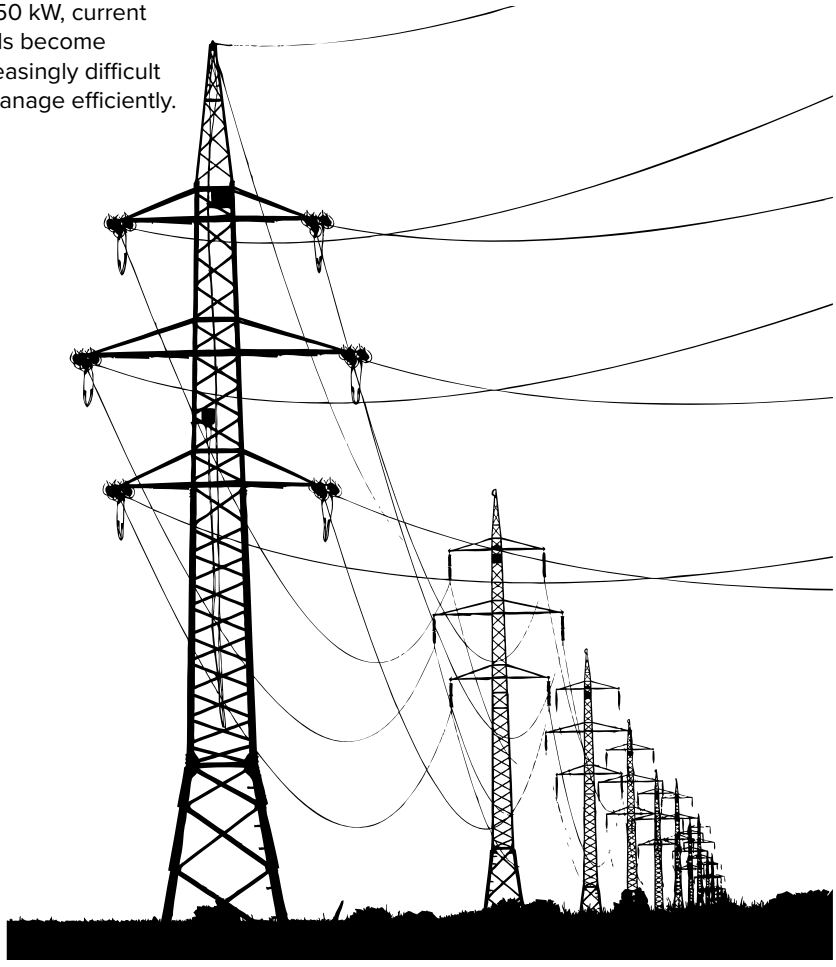
Higher-voltage distribution offers a practical alternative. By increasing voltage from 48 V to 800 V, current requirements fall dramatically, reducing losses throughout the distribution network and making high-density compute racks more feasible.

Scalia believes industry consensus around 800V has largely been achieved.

“As soon as the rack goes beyond 250, 300 or 350 kilowatts, it makes high-voltage distribution essential,” he says.

Importantly, the transition benefits from experience accumulated in other sectors, particularly electric vehicles, where 800 V architectures have gained significant traction over recent years.

Within AI infrastructure, the move to 800 V is also accelerating adoption of advanced semiconductor materials and power conversion technologies that offer higher efficiency and power density. The industry conversation has shifted from whether 800 V architectures will arrive to how rapidly deployments can scale.



"It's not anymore a trend," Scalia says. "It's more a reality."

The rise of gallium nitride

As power densities continue increasing, semiconductor materials are becoming a strategic differentiator.

Gallium nitride (GaN) has emerged as one of the most important technologies enabling the next generation of AI infrastructure. Its ability to switch at higher frequencies while reducing losses makes it particularly well suited to high-density power conversion. According to Scalia, GaN is already becoming dominant within key portions of the AI power stack.

At higher voltages, GaN enables significant improvements in power density compared with traditional silicon MOSFETs. In one example cited by Scalia, replacing silicon devices with GaN enabled a power supply design to achieve approximately 170% greater power density while significantly reducing physical size.

The implications are substantial. As compute modules become denser and cooling requirements intensify, reducing the footprint of power conversion systems becomes increasingly valuable. However, the transition is unlikely to be immediate or universal.

"There is no one solution that fits all," Scalia says.

Traditional silicon remains highly competitive in lower-voltage applications and continues to benefit from decades of optimisation. Nevertheless, as GaN technologies mature and move into lower-voltage domains, competition between the two approaches is expected to intensify.

Looking ahead, Scalia predicts that GaN will play an increasingly dominant role throughout AI infrastructure, while emerging materials and architectures continue to push performance boundaries even further.

Cooling and power are becoming the same problem

One of the most profound shifts underway is the growing convergence between power delivery and thermal management. In conventional server environments, cooling and power were often treated as separate engineering disciplines. AI is rapidly changing that assumption. High-current delivery, dense packaging and advanced liquid cooling solutions now require power and thermal engineers to work in tandem.

Scalia highlights innovations such as vertical power delivery and three-dimensional power structures that enable shorter electrical paths while simultaneously accommodating advanced cooling solutions. Renesas' own "tower power" concept, which stacks inductors above power stages within a structure measuring just a few millimetres in height, illustrates how closely packaging and cooling considerations are becoming linked. The objective is not merely to deliver power efficiently, but to do so while minimising inductance, controlling resistance and preserving the transient response required by modern processors.

Even minor parasitic effects can significantly impact performance when systems must respond to current changes measured in thousands of amps per microsecond.

"The packaging is definitely 50% of the entire approach," Scalia says.

This increasingly integrated view of architecture suggests future innovations may emerge as much from packaging technologies and cooling strategies as from semiconductor devices themselves.

Intelligence moves into the power layer

Another major trend shaping AI infrastructure is the growing role of embedded intelligence and software-defined power management. For decades, power electronics largely relied on fixed-function hardware. Today, digital control enables power systems to become programmable and adaptive. Scalia believes this flexibility will become increasingly valuable as



AI infrastructure grows in scale and complexity.

Modern power systems can already be modelled and simulated before processors even exist in hardware. Engineers can create virtual representations of future processors, evaluate power delivery networks and optimise performance well before physical prototypes become available. This digital design methodology significantly reduces development cycles while helping protect extremely expensive AI hardware.

More importantly, programmable power architectures allow infrastructure to dynamically respond to changing workload conditions. Future systems may actively adjust switching frequencies, transient responses and energy flows in real time, using embedded intelligence distributed throughout the power chain. The long-term vision extends beyond the rack itself.

As solid-state transformers and other intelligent power technologies mature, organisations could eventually gain software-defined control extending from medium-voltage grid connections all the way to individual AI processors. Digital power has existed as a concept for decades. AI may finally provide the compelling use case needed to unlock its full potential.

System-level thinking becomes essential

Perhaps the strongest theme emerging from Scalia's perspective is the importance of system integration.

Historically, semiconductor companies could focus on individual components. In the AI era, that approach is becoming insufficient. Power, memory, control, packaging, cooling and software increasingly interact in ways that determine overall system performance. Optimising one element in isolation no longer guarantees success. Instead, suppliers are being asked to deliver reference architectures, proof-of-concept systems and integrated design environments that help customers evaluate complex trade-offs across entire platforms.

"The orchestration of the system is what really can make the performance," says Scalia.



This reflects a broader shift occurring throughout the AI supply chain. Success increasingly depends on close collaboration between semiconductor suppliers, systems vendors, hyperscalers, foundries and software developers. No single participant can solve every challenge independently. As Scalia describes it, innovation is becoming a shared process in which each contributor provides specialised expertise that must be integrated into a unified system.

Looking five years ahead

When considering what AI infrastructure might look like in five years, Scalia offers an answer that focuses less on technology and more on market dynamics. He expects the industry to become significantly more diverse than it is today.

The first phase of the AI revolution was largely driven by a relatively small group of hardware leaders. The next phase, powered by agentic AI and inference, may see software companies, hyperscalers and cloud providers increasingly developing their own custom hardware platforms. Rather than a single dominant architecture, the future may consist of multiple competing approaches tailored to different workloads and deployment models. This diversification will have significant implications for power systems, memory technologies and infrastructure architectures, all of which must support an increasingly heterogeneous AI ecosystem.

"I think the equilibrium of the market will change," Scalia says. "There will be different platforms and different approaches that will proliferate."

For infrastructure providers, this means flexibility and adaptability may become every bit as important as raw capability.

The real opportunity beyond compute

The AI industry's obsession with compute performance is understandable. Accelerators remain the engines driving AI innovation. Yet as deployment scales and inference becomes dominant, attention is shifting toward the supporting technologies that make those accelerators useful. Power delivery, advanced semiconductor materials, memory interfaces, thermal management and intelligent control systems are rapidly becoming strategic battlegrounds in their own right.

In many ways, AI's future may depend less on how much compute can be added and more on how efficiently entire systems can be orchestrated. As infrastructure moves towards 800V architectures, advanced packaging, software-defined power and increasingly integrated system design, the biggest breakthroughs may come from the technologies operating behind the scenes.

The next decade of AI infrastructure will certainly require more compute. But according to Scalia, the real innovation will occur in the interconnected layers that power, manage and optimise it. And as AI enters its inference-driven era, those layers may ultimately prove just as important as the processors at the centre of the story.

Saras targets the AI power-delivery challenge

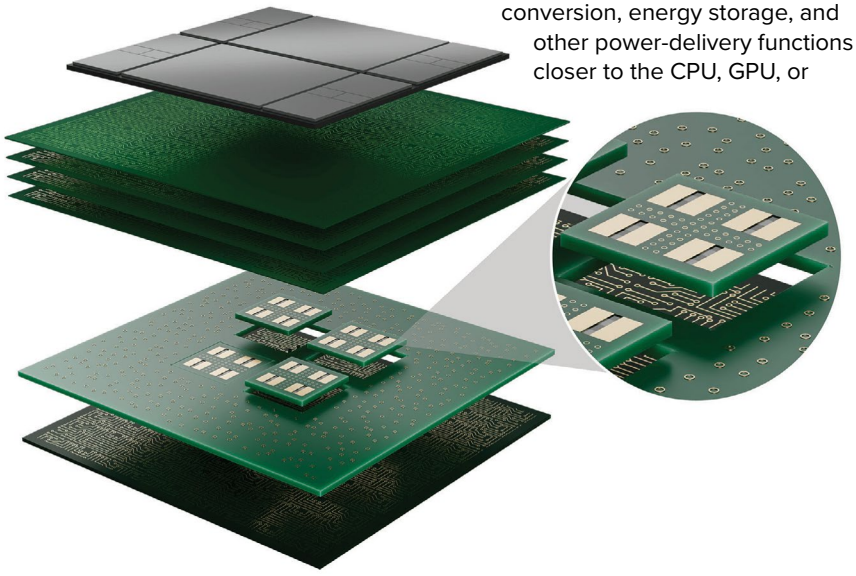
As AI and HPC push power densities ever-higher, Shaun Bowers of Saras Micro Devices explains how embedded passives, advanced packaging and vertical power delivery will help.

BY REBECCA POOL, TECHNOLOGY EDITOR

EARLIER THIS year, former Amkor executive, Shaun Bowers, joined US-based Saras Micro Devices as senior vice president of product management – just as the firm scales manufacturing of its PCB-embedded passive modules for integrated power delivery. *Power Electronics* caught up with Bowers to discuss the growing power-delivery challenges facing AI and high-performance computing, the role of embedded passives and advanced packaging, and Saras' plans for commercial production.

How is the rise of AI and high-performance computing changing the role of power delivery in system design?
As AI and high-performance computing systems become more power-dense, the power-delivery network is moving into the critical path of system design. It is no longer enough to optimize only the processor and advanced package. Designers must also minimize losses, maintain low PDN impedance, and deliver current quickly enough to support rapid workload transitions. That requires innovation across the components, materials, and architecture of the entire power-delivery path.

How is advanced packaging enabling a more efficient approach to power delivery?
Historically, power has travelled laterally across the board and package before reaching the processor. The industry is now moving toward more vertical approaches that bring voltage conversion, energy storage, and other power-delivery functions closer to the CPU, GPU, or memory. Embedding components within the PCB, package substrate, or chiplet environment can shorten the electrical path, reduce parasitic resistance and inductance, and use area more effectively.



➤ An exploded layer-by-layer structure of Saras Micro Devices' STILE technology, which embeds power-delivery passives directly into the semiconductor package substrate for AI accelerators.

How are customer priorities changing as more and more AI systems move toward commercialization?
Customer discussions are now becoming more practical. They are looking not only for higher component performance, but also for solutions that can be integrated predictably, customized for a particular architecture, tested before integration, and manufactured without introducing excessive cost or complexity. In other words, performance is essential, but manufacturability and scalability are becoming equally important.

STILE (Saras Tile) is an embedded integrated passive module for vertical power delivery – why develop this?
We see a growing need to integrate passive components at the PCB, package-substrate, and chiplet levels to meet the performance, power, area, and cost requirements of current and future AI and HPC systems. Saras developed this module to support that transition. It combines high-performance passive components with a configurable architecture and a repeatable integration approach, helping designers bring critical power-delivery functions closer to the processing elements without requiring a completely different manufacturing strategy for every design.



How does the module help to tackle the package-level power delivery challenge?
There are three parts to the challenge. First, passive components need to be positioned as close as practical to the processing elements to reduce the parasitic inductance associated with a longer delivery path. Second, the system needs sufficient local capacitance to respond to rapid changes in workload and current demand. Third, these capabilities must fit within a manufacturing approach that controls area, cost, and complexity. Our embedded integrated passive module is intended to address these requirements together rather than treating component performance and package integration as separate problems.

How can STILE improve the efficiency of AI and high-performance chips?
By design, the module is a configurable array of components for integration within a substrate core containing multiple embedded passive components. By placing high-density capacitance directly within the power-delivery structure, energy storage can be located much closer to the processor than with conventional approaches. Shortening that path can reduce parasitic losses and improve transient response. The array approach can also reduce the need to place and integrate many individual capacitor devices separately to meet total system requirements, while reducing the cost and complexity associated with manufacturing individual components at much lower density.

What are the key challenges involved in integrating capacitors and inductors directly into the chip package?
The challenge is not limited to the electrical performance of the individual components. Creating many separate cavities in a dense, expensive substrate can add manufacturing cost, yield risk, and routing complexity. We take a different approach by designing components to be embedded within commonly used core structures, either individually or as a pre-assembled and testable STILE array. The objective is to provide design flexibility while maintaining a more unified and repeatable method of integration at the substrate or PCB level.

How is Saras developing its technology roadmap to meet evolving power delivery network requirements?
Our roadmap begins with the passive components themselves. Saras determined that the available capacitor technologies did not meet our combination of density and integration requirements, so we developed a proprietary capacitor architecture. Today, the STILE concept is based on those capacitors, while inductive elements remain in development. Over time, we envision extending the platform to support a broader selection of qualified components, giving designers more flexibility to configure the passive array for their particular power-delivery architecture. All of this is built around a standardized integration method in a known-good array. We are aiming for customization without consequence, built around power delivery network requirements rather than a catalogue of standard components - all integrated into the core.

Do you have any examples of STILE in AI or high-performance computing applications?
Saras has built an interposer using our proprietary capacitors, demonstrating that the core integration concept is technically achievable. We are also engaged in product-level activity around potential capacitor and STILE applications.

With Saras' pilot line in Chandler, Arizona, up and running how is the facility supporting the company's path towards commercial production?
Our prototype and manufacturing line in Chandler, is operational and producing samples. The facility gives us the ability to customize individual components for form, fit, and function, as well as create STILE arrays that demonstrate the benefits of integrating a pretested group of passive components. The line also provides a foundation for incorporating inductive elements after that development is complete.



➤ Shaun Bowers is senior vice president of product management at Saras Micro Devices. He previously spent 23 years at Amkor Technology, where he held senior leadership roles including vice president of power products and vice president of package development and technology integration.



Optimising switching performance in SiC and GaN power designs

Sudhir Nagaraj, Director of Systems and Market Development, Allegro MicroSystems, explains that, while SiC and GaN devices support high-frequency switching, they frequently encounter system-level limitations – from bulky external bias supplies to slow protection loops – that impede optimal performance. Integration of sensing and gate driving removes these constraints to enable faster switching, improved efficiency and higher power density in applications like AI data centres and 800 V electric vehicle (EV) architectures.

AS SILICON CARBIDE (SiC) and gallium nitride (GaN) devices continue their rapid adoption across electric vehicles, AI data centres and industrial power systems, the conversation is shifting. For years, the industry focused on developing and commercialising wide bandgap semiconductors capable of delivering higher efficiencies, faster switching speeds and unprecedented power density. Today, however, a new challenge has emerged: how to fully realise their potential at the system level.

According to Allegro MicroSystems, the true bottleneck no longer resides within the switches themselves. Instead, it lies in the surrounding ecosystem of current sensing, gate control, system protection and power management technologies required to operate wide bandgap devices safely and efficiently.

Speaking about the company's latest innovations showcased at PCIM, Sudhir outlined a strategy centred on removing these system-level constraints, enabling engineers to push SiC and GaN technologies closer to their theoretical performance limits while reducing design complexity.

The system-level challenge

Wide bandgap technologies have transformed power electronics over the past decade. Both SiC and GaN devices offer significant advantages over conventional silicon, including faster switching frequencies, lower losses and higher operating temperatures.

Yet faster switching creates new engineering challenges.

"The last 10 years has really been about these switches coming to life and being optimised," explains Sudhir. "What needs to keep up is the whole system level, how to make these switches operate seamlessly, safely and optimally."

Two technologies, in particular, have become increasingly critical: current sensing and gate drivers.

As switching frequencies climb into the hundreds of kilohertz or beyond, power systems require significantly faster visibility into current behaviour. At the same time, SiC and GaN devices are highly capable but less forgiving

than legacy silicon technologies when subjected to fault conditions.

“These switches do not handle overcurrents and short circuits for long durations. You need to react within tens of nanoseconds to protect them.”

This requirement is reshaping how designers think about power conversion architectures. Effective sensing and control are no longer support functions. Instead, they are enabling technologies that determine how much performance can ultimately be extracted from the power stage.

Why current sensing has become strategic

Historically, current measurement technologies such as shunt resistors, amplifiers and Hall-effect sensors were often sufficient for power conversion systems. However, many of these solutions operate at bandwidths below 1 MHz. That creates limitations when monitoring modern wide bandgap power stages switching at dramatically higher frequencies.

Allegro’s latest current sensing technology pushes bandwidth up to 10 MHz, providing engineers with significantly greater visibility into switching behaviour. The implications extend beyond simply measuring current more accurately.

Because designers can observe current signatures in near real time and on a cycle-by-cycle basis, they gain a much deeper understanding of what is happening within the power stage. This increased visibility enables tighter control loops, more aggressive optimisation and greater confidence when operating devices closer to their performance envelope. Perhaps more importantly, higher-bandwidth sensing improves protection.

Traditional sensors may not respond quickly enough to detect overcurrent or short-circuit events before damage occurs. Wide bandgap power devices can transition from normal operation to failure in extremely short timeframes. By rapidly identifying fault conditions and communicating them to the system controller, fast current sensing helps ensure safe shutdown within the device’s operating limits.

For applications such as electrified transportation and hyperscale infrastructure, where reliability is paramount, these capabilities are increasingly becoming mandatory rather than optional.

Formula One cars need better drivers

Sudhir uses a simple analogy to describe the growing importance of gate driver technology. If SiC and GaN devices are Formula One cars, gate drivers are the drivers controlling them. The comparison is fitting. Wide bandgap switches are capable of extraordinary performance, but extracting that performance safely requires intelligent control. Driving devices too aggressively can trigger electromagnetic interference (EMI), excessive ringing and voltage overshoot. Drive them too conservatively and efficiency suffers while thermal losses increase. The challenge lies in finding the optimal balance.

Traditionally, this balance was established using fixed passive components such as gate resistors. Once selected, these hardware-based parameters remained fixed regardless of changing operating conditions. That approach becomes increasingly limiting as power systems grow more dynamic.

To address this challenge, Allegro has demonstrated software-defined gate control using SPI-based configuration methods. Rather than relying solely on fixed hardware parameters, engineers can dynamically adjust gate drive characteristics in response to changing operating conditions. This flexibility enables systems to switch faster when performance demands increase while simultaneously adapting to temperature shifts, changing loads or evolving operating environments. The result is a more intelligent power stage capable of optimising efficiency, reliability and safety in real time.



Eliminating the hidden complexity of isolation

One of Allegro's most notable PCIM demonstrations focused on its Power-Thru isolated gate driver architecture.

In conventional designs, isolated gate drivers typically require separate isolated bias supplies. Designing these supplies can add considerable complexity, particularly in multi-level architectures containing numerous high-side switches. While engineers want to focus on power conversion challenges, they often find themselves dedicating significant development effort to isolated power design. Integrating isolated power directly into the gate driver fundamentally changes that equation.

According to Sudhir, customer feedback has been overwhelmingly positive because the approach removes a layer of complexity that many power electronics designers would prefer not to manage.

Beyond simplifying development, the architecture also delivers significant space savings. By eliminating transformers and associated support components, designers can reduce board area while simplifying layouts. For applications where power density has become a primary competitive advantage, those savings can be substantial.

Real-time visibility changes everything

One recurring theme throughout the discussion is the importance of visibility.

Many engineers, Sudhir argues, still approach wide bandgap systems using assumptions developed during decades of conventional silicon design. A common misconception is that faster switches can simply be driven harder to maximise performance. In reality, switching speed must be carefully controlled. Excessive switching aggressiveness can introduce EMI problems and reliability concerns, while insufficient speed undermines efficiency gains.

Another misconception relates to sensing latency. Many legacy architectures effectively provide historical information, forcing controllers to make decisions based on switching events that occurred several cycles earlier. High-speed current sensing changes that paradigm. Instead of reacting to old data, controllers can respond to conditions occurring within the current switching cycle. This creates opportunities for more intelligent decision making, improved protection strategies and more aggressive optimisation techniques. As power densities continue rising, real-time awareness may become one of the most valuable assets available to system designers.

AI data centres and 800 V architectures

Few markets illustrate these trends more clearly than AI infrastructure.

The explosive growth of AI workloads is driving unprecedented power demands in data centres, forcing operators to rethink electrical architectures throughout the facility.

One notable development is the industry's growing interest in 800 V distribution architectures. Interestingly, Allegro sees strong parallels between data centres and electric vehicles. Both sectors are attempting to move large amounts of power through increasingly compact systems. Both require exceptional efficiency. Both are embracing higher voltage architectures to minimise losses and improve power density. And both increasingly rely on many of the same enabling technologies.

"AI data centres and EVs are not too different in the challenges they are facing," Sudhir notes.

In both markets, fast sensing and intelligent gate control help enable higher switching frequencies, more compact power conversion systems and improved efficiency. These advantages have become particularly valuable as operators attempt to balance power





availability, cooling constraints and total cost of ownership. For data centres, where operational energy expenses often exceed initial hardware costs over the life of a facility, incremental efficiency gains can translate into substantial economic benefits.

The importance of the ecosystem

As power electronics becomes increasingly sophisticated, no single supplier can optimise the entire system alone. Sudhir emphasises that ecosystem partnerships have become critically important for accelerating adoption. Collaborations with transformer providers, SiC and GaN manufacturers, passive component companies and system developers enable joint optimisation across the complete power chain. The result is a growing portfolio of validated reference designs that reduce risk for customers. That confidence matters.

Engineers are rewarded for minimising risk, shortening development cycles and delivering products to market quickly. Proven ecosystem solutions help satisfy all three objectives. By validating interactions between sensors, gate drivers, switches and passive components before customers begin development, ecosystem partnerships effectively reduce uncertainty and accelerate deployment.

As wide bandgap technologies enter mainstream markets, this collaborative approach may become increasingly important.

Rethinking legacy designs

Despite the advantages of integrated solutions, many engineers continue to rely on familiar architectures. Sudhir understands the hesitation. Legacy approaches are proven, well-understood and perceived as lower risk. However, the company warns against evaluating technology decisions solely through a near-term lens.

Power electronics platforms often require years to progress from initial design through validation and commercial deployment. By the time a system reaches production, market requirements may have evolved substantially. This is especially true in rapidly moving sectors such as electric transportation and AI infrastructure.

According to Sudhir, engineers must evaluate technologies according to long-term system benefits rather than immediate component costs alone. The broader economics frequently favour wide bandgap adoption. Higher efficiency reduces energy consumption. Improved power density lowers material requirements. Better thermal performance simplifies cooling strategies.

Collectively, these system-level gains can outweigh any initial increase in component cost. In data centres, where total cost of ownership remains a defining metric, the financial impact of better efficiency alone can be significant over an installation's lifetime.

Integration comes to the wheel end

While Allegro's PCIM demonstrations focused heavily on power conversion, the company has also been advancing integration within automotive electronics.

Its recently introduced A81415 PMIC combines power management and wheel-speed sensor functionality within a single ASIL-D safety architecture. The innovation reflects the automotive industry's migration toward zonal and distributed vehicle architectures.

In modern brake-by-wire systems, intelligence is increasingly moving closer to the wheel itself. Controllers, power management devices and sensing elements must operate within a highly constrained environment characterised by vibration, heat, electrical stress and severe space limitations. By integrating wheel-speed sensing functionality directly into the PMIC, Allegro eliminates up to nine external components and reduces PCB area by more than 50%.

The approach removes discrete wheel-speed sensor interfaces, decoders, level shifters and associated support circuitry while simplifying overall system architecture. For automotive engineers, the benefits extend beyond space savings. Fewer components reduce potential failure points, simplify qualification processes and accelerate development cycles. In safety-critical systems such as braking, these advantages carry particular importance.

Preparing for software-defined vehicles

Component consolidation is becoming increasingly important as automotive manufacturers transition toward software-defined vehicle architectures. Integrated solutions provide several benefits simultaneously.

They reduce system weight and complexity while simplifying compliance processes and improving reliability. They also allow engineering teams to focus on higher-level system functions rather than managing interactions between numerous discrete devices.

According to Sudhir, every additional component represents another potential point of failure. Carefully integrating functionality while maintaining safety and redundancy therefore becomes an important strategy for improving system robustness.

The company's latest automotive developments also acknowledge the industry's gradual transition toward 48 V electrical architectures. Although the new PMIC is optimised for 12 V operation, it has been designed to work seamlessly alongside Allegro's complementary 48 V-to-12 V conversion technologies, creating a migration path for future brake-by-wire platforms.

Looking ahead: Intelligence at the edge

Looking beyond today's products, Allegro's roadmap points toward increasing intelligence within both sensing and gate control technologies.

Future sensors, according to Sudhir, will do more than measure current.

They will help identify patterns, detect anomalies and potentially recognise conditions associated with impending failures before problems occur. This evolution aligns closely with broader trends toward predictive maintenance and intelligent power management.

Similarly, future gate drivers are expected to become increasingly adaptive, enabling faster reactions, more precise switching behaviour and higher system efficiency. These capabilities may prove especially important as emerging applications such as physical AI continue to gain momentum.

Robotic and autonomous systems introduce unique requirements around size, efficiency and noise immunity. Components must fit into increasingly constrained mechanical spaces while delivering high currents and operating reliably despite dense electronic integration.

For Allegro, these trends create opportunities to build on its core strengths in sensing, control and power management.

The company believes the future of power electronics will not be defined solely by better switches. Instead, success will increasingly depend on the intelligence surrounding those switches.

As SiC and GaN devices continue to mature, the competitive battleground is shifting from semiconductor performance alone to system optimisation. Faster sensing, adaptive gate control, integrated architectures and collaborative ecosystem development are becoming the critical technologies that determine who can unlock the full promise of wide bandgap power.

In that sense, the next chapter of power electronics may not be about building a faster Formula One car. It may be about creating a smarter driver.



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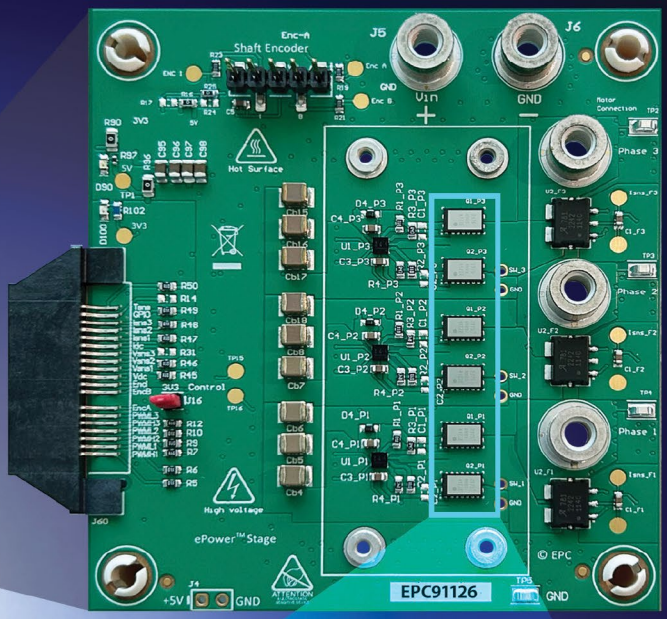
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