PICMAGAZINE

CONNECTING THE PHOTONIC INTEGRATED CIRCUITS COMMUNITY

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Novel photonics applications require vertical integration

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Viewpoint

By Mark Andrews, Technical Editor

Growth, tech innovation and TAP progress highlight 2019

THE ENORMOUS POTENTIAL of photonic integrated circuits (PICs) in all their forms continued to drive innovation throughout 2019. It became almost easy to lose track of all the times that 'first' characterized a new product or service. While the technologies, research and companies manufacturing PICs have achieved much, there is room to grow. The good news is that 2019 saw progress on many fronts.

As a relatively young industry, PICs face issues. In a feature article that first appeared in PIC Magazine's sister publication, Compound Semiconductor, Editor Richard Stevenson chronicles how much PICs have come to dominate content at such major conferences as the ECOC held in Dublin, Ireland in September. Indeed. A glance at the ECOC agenda had about a half-day of 'purely PIC' content, but looking deeper it was clear that PICs were a discussion point in nearly ***half*** the presentations.

In his article, 'ECOC offers a snapshot of PIC Progress,' Dr. Stevenson notes that such industry powerhouses as Intel, Infinera, and Hewlett Packard Enterprise offered their latest plans for incorporating PICs into their roadmaps. But like any new technology, integrating optical circuits with electronics presents potential stumbling blocks to PIC ascendency. One key debate centers around what materials can be standardized for the range of devices needed to construct PICs: lasers, amplifiers, modulators, and wave guides to name a few.

A fitting complement to the ECOC round-up is a look at the 2019 mid-year World Technology Mapping Forum (WTMF-3) that brought together 100 global photonics experts to help resolve materials questions along with other pressing issues to ensure sustainable markets much the way the ITRS enabled silicon transistor evolution decades ago. Beyond standardizing materials the WTMF also addressed the ongoing need for automated test, assembly and packaging (TAP) for better repeatability and reliability.

Our cover feature is from LioniX International, a Netherlands firm delivering a full range of innovative PIC services and products. The company explores new innovations based on its core silicon nitride (SiN) TriPleX™ wave guide technology, which is ideally suited for applications in telecom/datacom, life sciences, and metrology; TriPleX is also compatible with micro/opto-fluidics and MEMS devices.

Also in this edition, EPIC R&D Manager Ana Gonzalez examines unique PIC advantages for biosensors. An article from X-Celeprint explores ways that micro transfer printing (MTP) can ideally address PIC needs. We also delve into recent cooperative work by researchers at the TeCIP Institute, the Inphotech Foundation and the University of Glasgow in developing the first silicon-photonics (SiP) reconfigurable optical frequency comb (OFC) demultiplexer for flexible-grid optical networking.

Attend the PIC International Conference, 31 March-1 April in Brussels, Belgium to celebrate 2019's accomplishments, address the industry's challenges, and uncover new PIC opportunities for 2020 and beyond.

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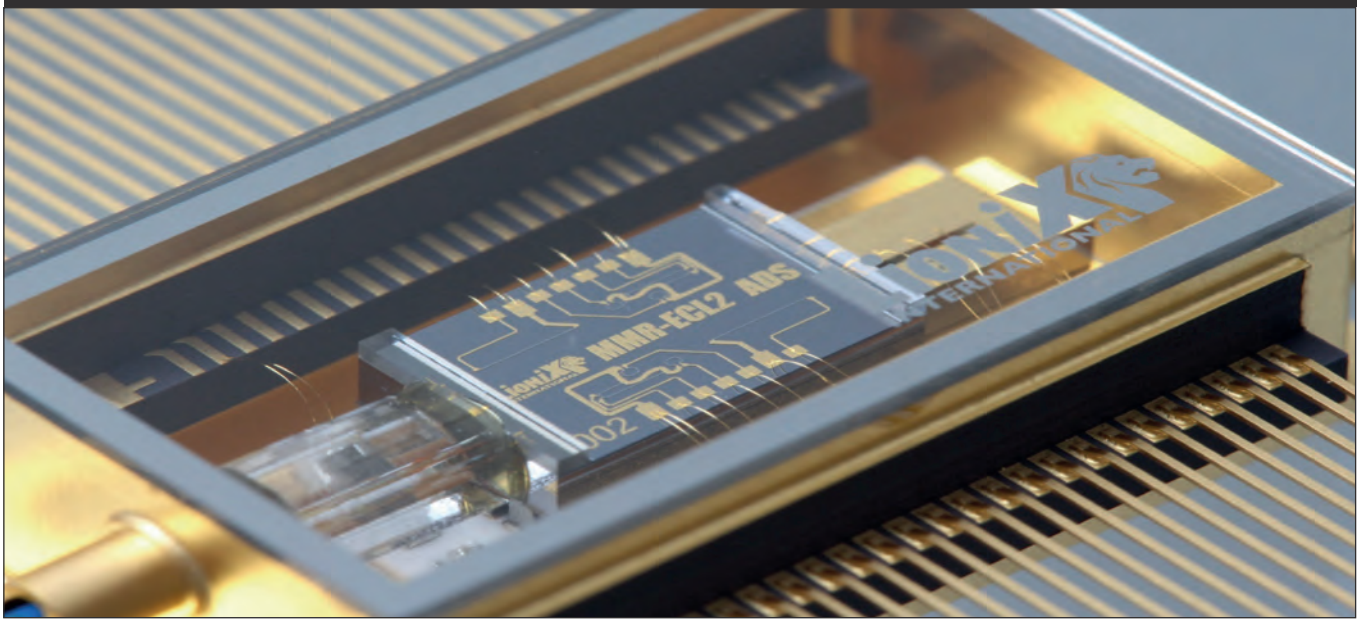
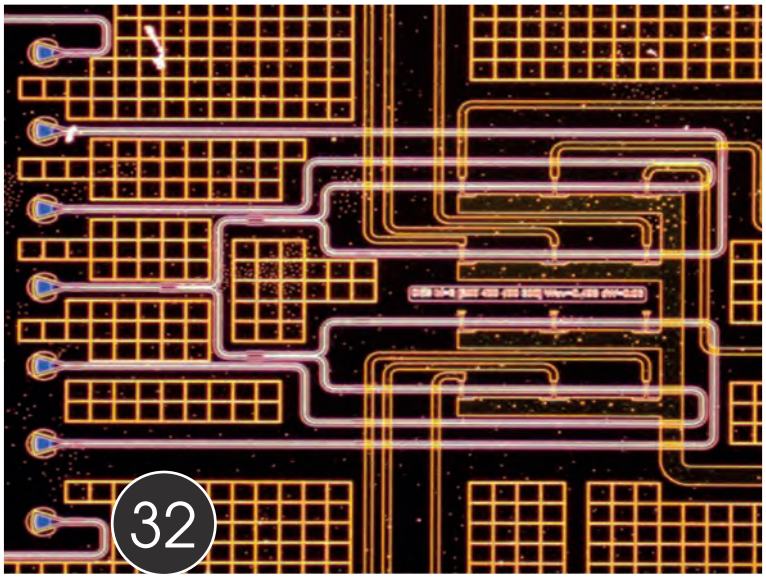
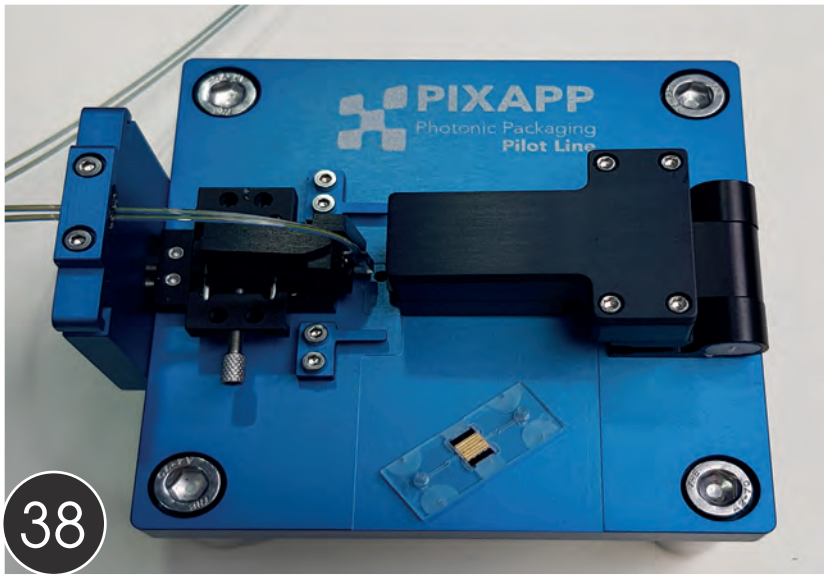
CONTENTS







news

EV Group and DELO partner to expand materials and process capabilities

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that it is partnering with DELO, a leading manufacturer of industrial high-tech adhesives, in the area of wafer-level optics (WLO).

Both companies, well-known for their roles in optical sensor manufacturing, are combining efforts to enable novel optical devices and applications, such as biometric authentication and facial recognition, for the industrial, automotive and consumer electronics markets utilizing EVG's leading lens molding and nanoimprint lithography (NIL) process equipment and DELO's advanced adhesives and resist materials.

The partnership, which is being carried out within EVG's NILPhotonics Competence Center at its headquarters in St. Florian, Austria as well as at DELO's headquarters in Windach, Germany, will contribute to improving and speeding up material development cycles. EVG's NILPhotonics Competence Center provides an open access innovation incubator for customers and partners across the NIL supply chain to collaborate to shorten development cycles and time to market for innovative devices and applications.

Infrastructure includes state-of-the-art cleanrooms and equipment supporting key NIL manufacturing steps such as step-and-repeat mastering, lens molding and EVG's SmartNIL technology, as well as wafer bonding and required metrology. This provides a unique offering to easily access the latest technologies and materials for WLO development, prototyping and manufacturing.

Advanced adhesives and resists play a pivotal role in enabling wafer-level production of next-generation optical sensors for mass markets.

The development of advanced optical materials requires extensive characterization of chemical, mechanical and optical properties as well as proven scalability for high-volume manufacturing (HVM).

Particular know-how of material requirements for automated molding and demolding processes as well as excellent material compatibility of working NIL stamps and resists are important as they enable optimal WLO performance at the smallest form factors using proven HVM processes.

Close collaboration between materials suppliers and process equipment manufacturers is key to enabling the development and refinement of processes needed to ensure high reliability and manufacturability of WLO for high-quality products.

This joint effort between EVG and DELO will support both companies in refining their processes and products, as well as strengthening their expertise to address current and future market requirements. The partnership will also provide mature material and process know-how to speed up new product design and prototyping, supporting the roadmaps of both companies' customers.

"EVG and DELO are known as technology and market leaders in WLO and NIL equipment and, respectively, optical materials, with a proven track record in ramping these technologies and processes into high-volume production," stated Robert Saller, managing director at DELO. "Together we can provide unique know-how in applying wafer-level processing technology to optical and photonics manufacturing, making EVG an ideal partner in the development of our latest products. This collaboration will in turn help us to serve our customers as an application expert and premium partner."

Trumpf delivers billionth VCSEL to STMicroelectronics

The partnership between Trumpf and STMicroelectronics reached a new high in autumn 2019 when Trumpf delivered the one billionth VCSEL to its European partner. Trumpf develops and produces its VCSELs at Photonic Components, a business located at the company's Ulm site in Germany. VCSELs are used in smartphones to improves the camera autofocus, enable face recognition to unlock the device's display and switch off the display when the user raises the smartphone to their ear when taking a call. Trumpf's VCSEL technology is now installed in more than 150 smartphones from a wide range of leading OEMs.

"We have been working successfully with STMicroelectronics since 2012 and intend to deepen this relationship to unlock the great potential for growth in many consumer electronics segments," says Joseph Pankert, the managing director in charge of the VCSEL line of business. "We also see strong growth potential for our VCSELs in other markets including higher resolution time-of-flight cameras. These cameras flood an object or a room with infrared light, measure the round-trip travel time or the phase shift of the emitted light, and calculate three-dimensional models based on this data," says Pankert.

"Our long-standing technology partnership with Trumpf has reached a hugely significant milestone - the shipment of 1 Billion VCSELs for use in our Time-of-Flight product families," says Eric Aussedat, STMicroelectronics executive VP and general manager of the Imaging sub-group. "ST's Time-of-Flight product families have been widely adopted by leading smartphone OEMs with more than 150 phone models already using our technology. Building on this success, we look forward to further co-work with Trumpf to address the exciting and rapidly growing 3D and depth sensing markets."

Alibaba Cloud silicon photonic based 400G DR4 optical transceiver to support next-gen networks

ALIBABA CLOUD, the data intelligence backbone of Alibaba Group, has announced the launch of a 400G DR4 optical transceiver based on Silicon-Photonic (SiPh) technology to support its next-generation data center network.

The new transceiver will be deployed in Alibaba Cloud's global data centers starting in 2020 and will increase the network speed by four times compared with current 100G optical transceivers. This important development will also lay a solid foundation for opto-electronic co-packaging technology in the future.

Alibaba Cloud will be conducting a live demo of the new transceiver at the upcoming Apsara Conference on September 25-27, 2019.

This is another milestone in the field of optical interconnection following Alibaba Cloud's full deployment of 40G and 100G optical transceivers in 2016 and 2017. The rapid growth of cloud computing and big data applications has meant that data centers have to handle a doubling in traffic every one to two years.

To meet the demand for high-bandwidth data transmission while maintaining the same cost, power consumption and size of data center, it is critical to increase the optical transceiver speeds with innovation in the field of optical interconnect technologies.

Silicon-Photonic is a key technology to address this challenge. It significantly reduces the physical size of transceivers while simplifying the design and production by integrating a large number of optical components onto a single silicon photonic chip. The technology utilizes existing CMOS manufacturing processes to achieve wafer-scale testing and packaging, thereby significantly reducing the production cost of photonic chips.

An additional benefit is the reduction in signal impairments within transceivers that lowers the signal-processing power consumption. Since Silicon-Photonics uses the same CMOS processes and manufacturing technologies, it is more suitable for opto-electronic co-packaging, which may ultimately solve the existing challenge of the electrical chip I/O bandwidth bottleneck.

Alibaba Cloud has been investing in SiPh technology in recent years. Through in-depth cooperation and joint technology development with Elenion Technologies and Hisense Broadband, Alibaba Cloud is involved in the entire production supply chain, from SiPh chip design, packaging and testing to the SiPh-based optical transceiver design, packaging, assembly and testing. The successful development of the SiPh 400G DR4 optical transceiver is the result of Alibaba's long-term investment in these technologies.

Through further cooperation within the industry, it is expected that the speeds of optical transceivers will reach 1T or higher in the next five years.

SMART announces novel integrated silicon III-V chips

THE SINGAPORE-MIT ALLIANCE FOR RESEARCH AND TECHNOLOGY (SMART), MIT's Research Enterprise in Singapore, has announced the successful development of a commercially viable way to manufacture integrated Silicon III-V Chips with high-performance III-V devices inserted into their design.

In most devices today, silicon-based CMOS chips are used for computing, but they are not efficient for illumination and communications, resulting in low efficiency and heat generation. This is why current 5G mobile devices on the market get very hot upon use and would shut down after a short time.

This is where III-V semiconductors are valuable. III-V chips are made from elements in the 3rd and 5th columns of the elemental periodic table such as Gallium Nitride (GaN) and Indium Gallium Arsenide (InGaAs). Due to their unique properties, they are exceptionally well suited for optoelectronics (LEDs) and communications (5G etc) - boosting efficiency substantially.

"By integrating III-V into silicon, we can build upon existing manufacturing capabilities and low-cost volume production techniques of silicon and include the unique optical and electronic functionality of III-V technology," said Eugene Fitzgerald, CEO and Director, SMART, MIT's Research Enterprise in Singapore. "The new chips will be at the heart of future product innovation and power the next generation of communications devices, wearables and displays."

Kenneth Lee, Senior Scientific Director of the SMART LEES research program adds: "However, integrating III-V semiconductor devices with silicon in a commercially viable way is one of the most difficult challenges faced by the semiconductor industry, even though such integrated circuits have been desired for decades. Current methods are expensive and inefficient, which is delaying the availability of the chips the industry needs. With our new process, we can leverage existing capabilities to manufacture these new integrated Silicon III-V chips cost-effectively and accelerate the development and adoption of new technologies that will power economies."

The new technology developed by SMART builds two layers of silicon and III-V devices on separate substrates and integrates them vertically together within a micron, which is 1/50th the diameter of a human hair. The process can use existing 200mm manufacturing tools, which will allow semiconductor manufacturers in Singapore and around the world to make new use of their current equipment.

Today, the cost of investing in a new manufacturing technology is in the range

of tens of billions of dollars, thus this new integrated circuit platform is highly cost-effective and will result in much lower cost novel circuits and electronic systems.

SMART is focusing on creating new chips for pixelated illumination/display and 5G markets, which has a combined potential market of over $100B USD. Other markets that SMART's new integrated Silicon III-V chips will disrupt include wearable mini-displays, virtual reality applications, and other imaging technologies. The patent portfolio has been exclusively licensed by New Silicon Corporation Pte. Ltd. (NSC), a Singapore-based spin-off from SMART. NSC is the first fabless silicon integrated circuit company with proprietary materials, processes, devices, and design for monolithic integrated Silicon III-V circuits (www.new-silicon.com).

SMART's new integrated Silicon III-V chips will be available next year and expected in products by 2021.

Skorpios shows 400G transceiver at ECOC 2019

SKORPIOS TECHNOLOGIES, a US-based integrated silicon photonics company, is demonstrating its 400G CWDM8 transceiver product at ECOC 2019 in Dublin. In addition, it is providing an update on its 100G CWDM4 QSFP28 product and unveiling the company's new product roadmap which includes FR4/FR8 and ZR products.

The 400G CWDM8 transceiver is claimed to be the world's first heterogeneously integrated (III-V and Silicon) 400G Tx device with eight lasers, eight modulators, in a 3x5mm package. The Tx device has two lasers implemented on each of four pieces of III-V material, demonstrating how the HPIC technology platform can easily scale to massively higher bandwidths, according to the company.

Skorpios says its HPIC III-V EAM modulators are capable of 50G NRZ and PAM4 based optical transmissions using the same architecture and are easily upgradeable to 100G per wavelength.

The company reports continued progress with its 100G CWDM4 QSFP28 module. The company has completed over 2,000 hours of successful reliability testing and is in system qualification with Tier 1 switch vendors. Skorpios is accepting purchase orders for its 100G product at differentiated pricing enabled by its unique technology platform. Skorpios also provided an update to its new product roadmap which features 400G FR4, 800G FR4x2, 800G FR8, 400ZR and 800ZR products. The company plans to ship 400G FR4 modules in Q1 2020 and sample 800G FR8 modules in Q4 2020.

"Our 400G demo and shipment of our 100G product underscore the power, scalability and disruptive nature of Skorpios' HIPIC technology platform," said James Czilli, vice president of engineering.

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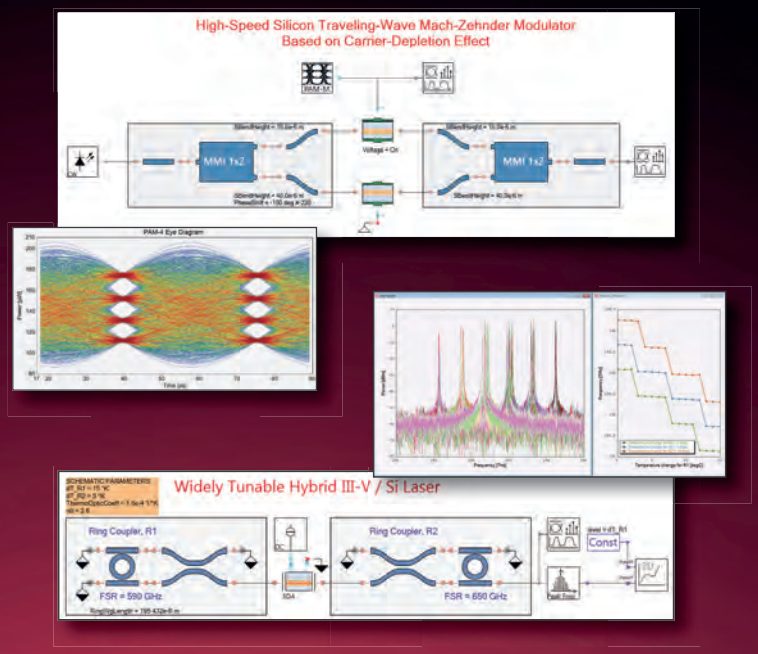

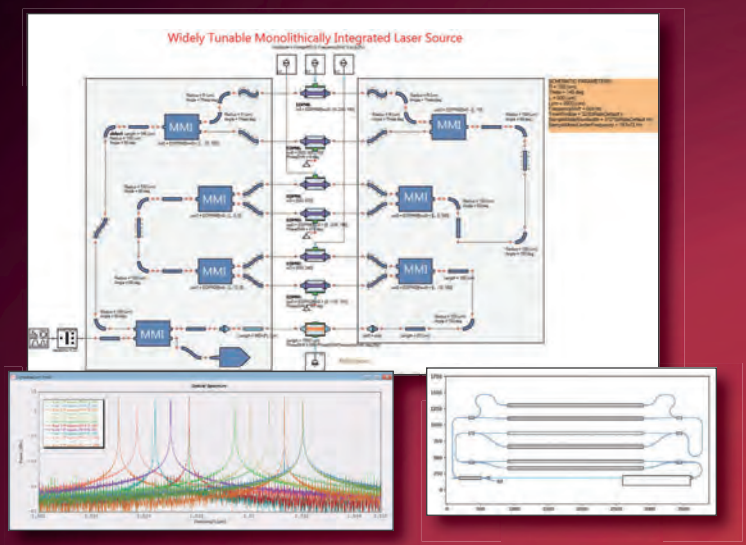

Waveguides & Fibers

- Facilitate advanced waveguide layout definitions and optimization tasks
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- Model bent waveguides and fibers made of dispersive isotropic and lossy materials

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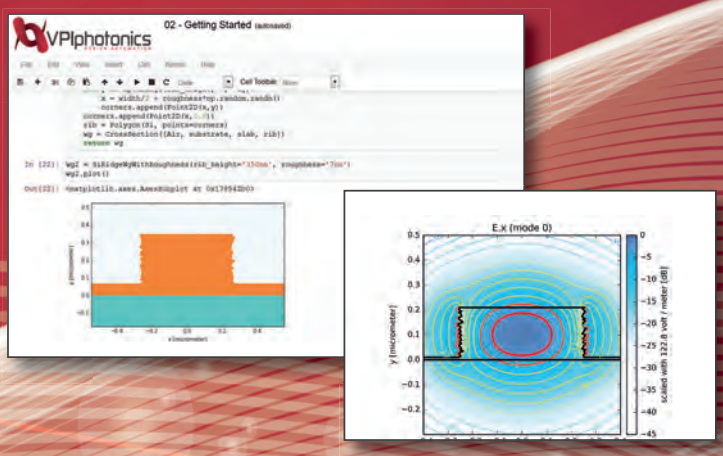

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Scintil Photonics raises €4 million in first-round funding

SCINTIL PHOTONICS, a Grenoble-based developer of silicon photonic fully integrated circuits including laser integration, has raised €4 million ($4.4M) in a first-round funding. Supernova Invest, Innovacom and Bpifrance are lead investors on the round. They were joined by Credit Agricole Alpes Développement and endowment Fund Foreis.

The proceeds will be used to develop prototypes (800Gbit/sec transceiver photonic circuits) in commercial semiconductor foundries in order to sample strategic customers in the data centre market. The team and development partnerships, including those with CEA-Leti in France and the University of Toronto in Canada, will be strengthened.

The success of this first tranche of funding reflects investor interest and confidence in the technology and the company, founded less than a year ago. Prior to its establishment, in November 2018, by CEO Sylvie Menezo, previously with CEA-Leti, and chairman Pascal Langlois, former CEO of Tronics Microsystems, the start-up project, incubated at CEA-Leti, received initial start-up funding as a winner of i-Lab 2018, a French government-sponsoredinnovation competition hosted by Bpifrance.

“We are very pleased to have the support of leading French investors to further develop to an industrial level our innovative silicon photonic integrated circuits,” said Sylvie Menezo,CEO of Scintil Photonics. “Integrating lasers onto silicon photonic circuits, mass produced in commercial silicon photonics foundries using standard manufacturing processes, is a key technology asset of Scintil. This will open up many opportunities, not only in optical communications, but also in computing and sensing applications, such as Lidar. We look forward to engaging with prospective customers and demonstrating the functionality and performance enhancements that Scintil Photonics can bring. With this first funding round, Scintil will be able to have its demonstrator and prototype circuits manufactured in commercial foundries, which will greatly accelerate our time to market.”

Drawing upon over 15 years of research on lasers, silicon photonics and 3D packaging conducted at CEA-Leti, Scintil’s technology enables higher speed optical communication through the integration of multi-wavelength lasers with silicon photonics standard technology. It also reduces implementation costs by avoiding several packaging steps. Besides developing solutions for high-speed data transmission, Scintil Photonics also targets sensing applications, such as Lidar, an enabling technology for autonomous detection and mobility.

Improving data centers efficiency is one of industry’s major challenges today. “We firmly believe in Scintil Photonics’ ability to implement the seamless integration of III- V semiconductor material on silicon. In particular, the collective manufacturing of lasers, reducing the cost of mass-producing fully integrated photonic circuits while improving the energy efficiency and other critical parameters, is a key differentiator in penetrating the market of data centre transceivers and sensors. It matches perfectly Supernova Invest’sambition to support game-changing Deep Tech startups,” said Christophe Desrumaux, investment director at Supernova Invest.

“Scintil Photonics aims to develop optical data interconnections over 800 Gbit/s at a very competitive cost and is uniquely positioned to address industry challenges in very high- speed data communication. This investment is an excellent illustration of our commitment to supporting Deep Tech companies,” said Marion Aubry, investment director at Bpifrance’sDigital Venture team. “Today, 80 percent of data transmission occurs over short distances and inside data centres. Fo rthis type of application, higher bit rates, cost and power consumption are critical factors. Scintil Photonics’ technology and products address those challenges and the company is a great example of the highly innovative digital start-ups and disruptive technologies Innovacom successfully supports,” said Vincent Deltrieu, partner at Innovacom.

“Led by an expert and knowledgeable team, Scintil is able to propose its leading-edge solution in a booming market. We are delighted to support this high-potential start-up,”said Rami Hassoun, investment manager at Crédit Agricole Alpes Développement. “Foreis is very proud to contribute to the development of Scintil Photonics, a promising venture in high-speed silicon photonics solutions, which will help create innovation and employment in the semiconductors industry in France,” said Jean-Yves Muller, president of the endowment Fund Foreis.

Novel photonics applications require vertical integration

Scalable assembly and packaging of photonic integrated circuits for emerging applications.

BY DOUWE GEUZEBROEK, PAUL VAN DIJK, ARNE LEINSE AT LioniX International B.V.

PHOTONIC INTEGRATED CIRCUIT (PIC) technology is becoming more interesting for applications outside telecom and data communications. New applications for PICs in metrology and life science are emerging as the promise of technology scaling enables lower cost and smaller form factors that well match novel application roadmaps.

Growth beyond traditional PIC applications is possible due to maturing photonic IC technology and a greater number of foundries providing new Silicon Photonics, InP and Silicon-Nitride processes. Rather than surmounting technology hurdles, the challenge faced by PIC designers and manufacturers is how to best address the broad scope of novel applications now possible.

These emerging applications have a broad range of requirements both in terms of Photonic IC functionality and also in making interconnections with other parts of the system. There is no single interface in this broad scope of applications like those typical for standard fiber optic cables. Furthermore, these diverse requirements often mean that optimizing on-chip functionalities only will not be sufficient to address the complete need.

An integral or vertical approach needs to be applied to product designs that takes into account overall system performance and interface needs as well as the chip design itself. We show a different set of interfaces available in the TriPleX waveguide platform [1] that will match the requirements of emerging applications such as bio-photonics and confocal microscopy, flow cytometry, molecular diagnostics, bio-sensing, DNA sequencing and micro spectroscopy. We conclude with an example of the vertical integrated approach for broadband beamformers in 5G antenna and satellite communications systems.

Standard building blocks

PIC technology relies on the use of validated standard building blocks. These building blocks, such as waveguide bends, taper sections and modulators (amongst many) are designed with a common use in mind. However, in assembly and packaging of these PICs, the field of emerging applications is so broad that there is no standard packaging scheme that is suitable for all, unlike the fiber pigtailed butterfly package that is used across telecommunications.

Assembly interfaces for future applications

The most common interface to Photonic ICs is the optical fiber. Adding one or multiple fibers to a PIC is a very common method of interfacing with the device, especially in telecommunications applications, where fiber is the main light transport means. Many interconnection techniques have been used here such as the fiber array; others include using a v-groove array in glass or silicon to assemble fibers at a certain pitch, or matching the waveguide pitch to the PIC.

However, these standard methods utilized in the infrared wavelength domain do not provide sufficient accuracy for interconnection requirements for visible light. Due to the application of lower wavelengths, the alignment tolerance decreases. Furthermore, the energy density increases due to the incremental photon energy at lower wavelengths; especially in the blue range within the color spectrum, any organic material like epoxies needs to be avoided. Through

careful design of the interconnect region and polishing the PIC facets, assembly methods have been developed which avoid use of any epoxy in the light path.

A second interface type demonstrates a true advantage of using PICs when very small pitches between the waveguide outputs need to be applied. For instance, it is possible to create pitches 10 μm apart coming from a splitter device that has divided incoming light into multiple output beams. These multiple beams interfere in free space after leaving the PIC; a behavior of a multitude coherent point sources is observed.

At a certain distance, this creates interference which patterns the emitted light in relation to the amount of point sources and their relative phase. By changing the phase of each channel in the splitter, the interference pattern can be shaped, or moved – all without any mechanical moving parts.

The direct free-space interface can be taken one step further, introducing vertical out coupling of the light, using 45 degree micro-machined mirrors. In this way the light leaves the PIC perpendicular to the planar waveguide layer, from any location on the PIC. FIB (Focused Ion Beam) milling provides accurate control to define a smooth mirror at the correct angle, here at 45˚. Since the mirror functions based upon the principle of total internal reflection, no additional metal layers are needed, and an efficient mirror can be made.

Coupling light using a free space interface is also possible. For some high-end visible light applications, it is favorable to couple light into the PIC using lenses. For instance, one or several laser diodes can be accurately aligned via a lens system, focusing the light on the input facets of the PIC. A high-end lens system is an alternative to the use of simple ball lenses, which is a better choice when a compact and cost sensitive application is targeted.

Another approach for connecting the PIC to devices on top of the chip are grating couplers. For example: in low-cost, even disposable bio-photonic sensors, integrated optical devices allow for label-free, real-time measurement of multiple parameters simultaneously. For example, in evanescent field-based micro-ring resonator sensors, the parameter to be sensed influences the propagation properties of a guided light signal in the on-chip sensing region. NIR (850 nm) applications are very attractive for absorption measurements, as both high quality light sources (GaAs VCSELS) and detectors (silicon PIN photodiodes) are readily available at very attractive price levels. These VCSELs and detector arrays can be flip chipped onto the surface of the PIC using grating couplers to direct the light in and out of the waveguides. This flip chip mounting of the devices onto the substrate opens possibilities for mass production.

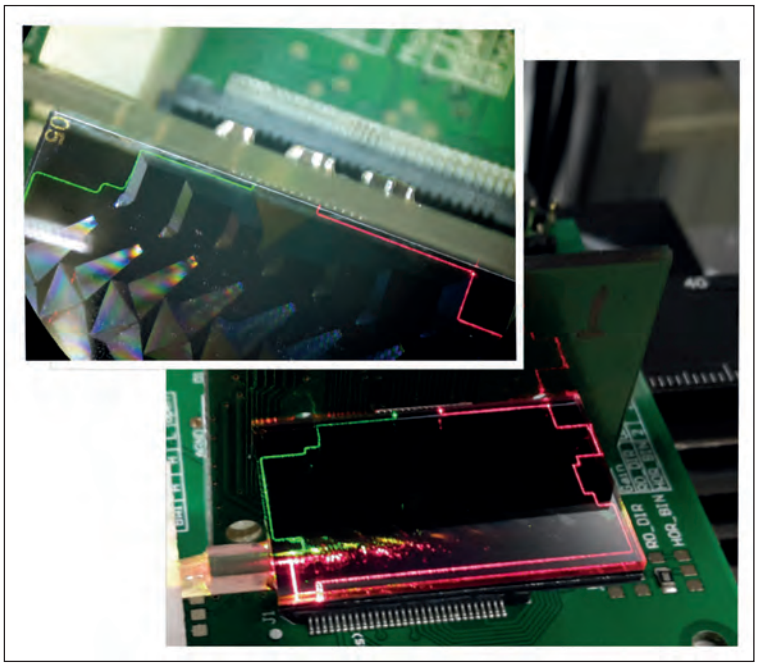

Figure 1. Photograph of an assembled integrated OCT system. The inset photograph shows the PIC containing the arrayed waveguide grating structures used to spectrally convert the signal to the attached CCD array utilizing a hybrid approach.

Hybrid assembly

The flip chip placement of VCSEL sources and detector arrays is already a first step towards hybrid integration. This approach enables the design to integrate multiple PIC or other microsystems parts based on different technologies to generate a new product. In this way, each component does what it is doing best and the applications or product that is designed is using various technology building blocks to mix and match into a new targeted design. To demonstrate this further we will show three applications using this hybrid approach: Optical Coherence Tomography (OCT); a tunable, narrow linewidth laser; and a microwave photonic beamforming solution.

The flip chip placement of VCSEL sources and detector arrays is already a first step towards hybrid integration: integrate multiple Photonic IC or other microsystems parts, based on different technology to generate a new product

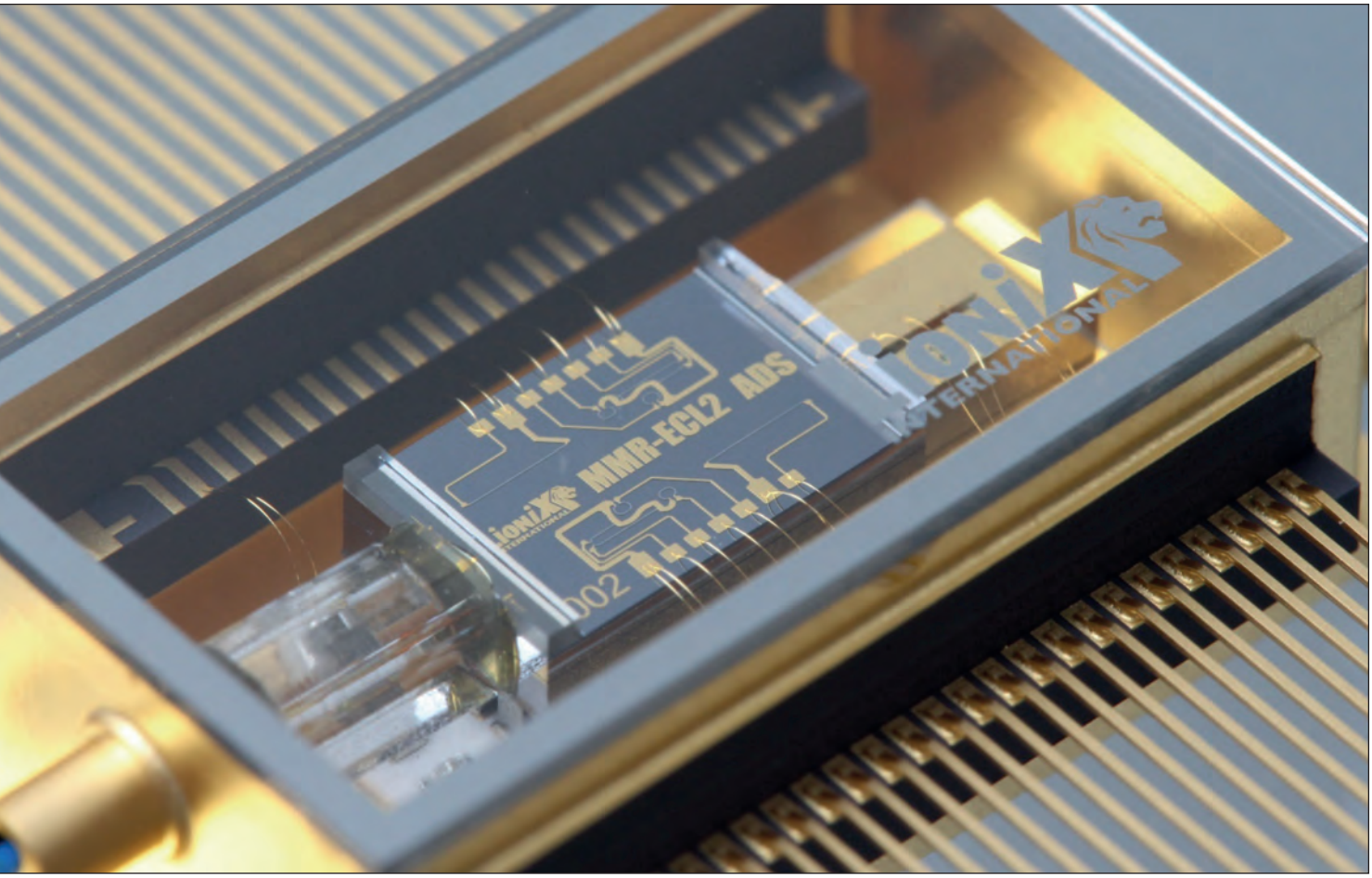

Figure 2. Narrow linewidth tunable laser based on hybrid assembly of an InP gain section and a tunable mirror made in TriPleX.

Optical coherence tomography

A promising application that can hugely benefit from photonic integration is OCT. This diagnostic method is the optical equivalent of the well-known acoustic echo (sonogram technology) that we use to picture our unborn children. In contrast to echoscope, OCT is a non-contact technology, making it applicable to eye research and retinal imaging as well, a 'surrogate biomarker' that could be used to detect Alzheimer's and a complementary, and less-costly, method to produce PET scans of the brain as well as testing the cerebrospinal fluid taken from the base of the spine, which is currently used to detect deposits of beta amyloid protein, which can indicate Alzheimer's.

Since the OCT system relies on many optical components, it is well suited for integration. The need for this is becoming evident when the size of the system needs to go down as the medical diagnostic tools need to transition out of hospital settings and towards point of care, such as a doctor's office or neighborhood clinic. An OCT module has been realized based on hybrid assembly that attached a linear CCD array to the side of a PIC. In this example, a readout for the wavelength filter (based on an array waveguide grating) became possible. A broadband light source like a SLED was also attached using hybrid techniques to realize a complete OCT module the size of a mobile phone. See Figure 1 for an example of a prototype OCT system. The PIC holds the complete OCT system including arrayed waveguide gratings to separate the wavelengths from the broadband light source reflected by the target.

Narrow linewidth tunable laser

Another novel application resulting from a hybrid assembly approach is the narrow-linewidth tunable laser. This module combines an InP gain chip and a TriPleX tunable mirror into an external cavity laser, tunable over a wide range, with record-low linewidths as low as 40Hz [2]. This application requires interconnection of two chips of different material systems with low interconnect losses at the hybrid interface, which is inside the laser cavity. An example of the hybrid coupling is depicted in Figure 2, showing an InP gain section with one side coated to act as a mirror and the other side having an antireflection coating. The second mirror of the external cavity setup is constructed on the TriPleX chip and consists of micro-ring resonators and other structures to create a long cavity and a wavelength tunable mirror. The low-loss hybrid assembly, combined with the low-loss large cavity length, makes this laser a world record holder for narrow line width and tunability over a wide range [2].

Microwave photonic beamformer

For next generation mobile networks and satellite communication systems, a broadband and

continuously tunable beamforming element is required. The element needs to process several RF signals and align the appropriate signals to steer a beam coming out of a phased array antenna. The given requirements of current and upcoming systems make a good case to perform the processing within the optical domain where broadband and continuous phase changes can be realized using true time delays. An example approach is a cascaded microring resonator structure. As the required delays are long (in the order of several nanoseconds), a photonic integration platform is required that has low loss.

In microwave beamforming, a fast modulator and detector for the signal conversion between RF and photonics is also required. The best solution is the hybrid assembly approach combining the low-loss TriPleX waveguide platform for true time delays and an InP platform to realize the active components: the modulator, detector and laser. Figure 3 shows an assembly of an RF-in/RF-out microwave photonic beamformer where the signal delays are processed in the optical domain. The full hybrid assembly principle based on co-operation of two PIC platforms as well as the driving electronics can only work when a vertical integrated design approach is taken. The latest results of the beamformer are given in the References section following this article's conclusion; please see reference [3].

Conclusion

Applications that benefit from Photonic Integration technology are moving fast and opportunities are growing. Since the total scope of applications is also broadening outside of the tele- and data communications range, the different interfaces that connect the PIC to the other portions of the total system are also expanding outside of standard fiber interface approaches. Therefore, a vertically integrated design approach needs to be taken to combine the design, the manufacturing and the assembly of a PIC into a complete module to ensure that novel applications will benefit from the capabilities of photonic integration.

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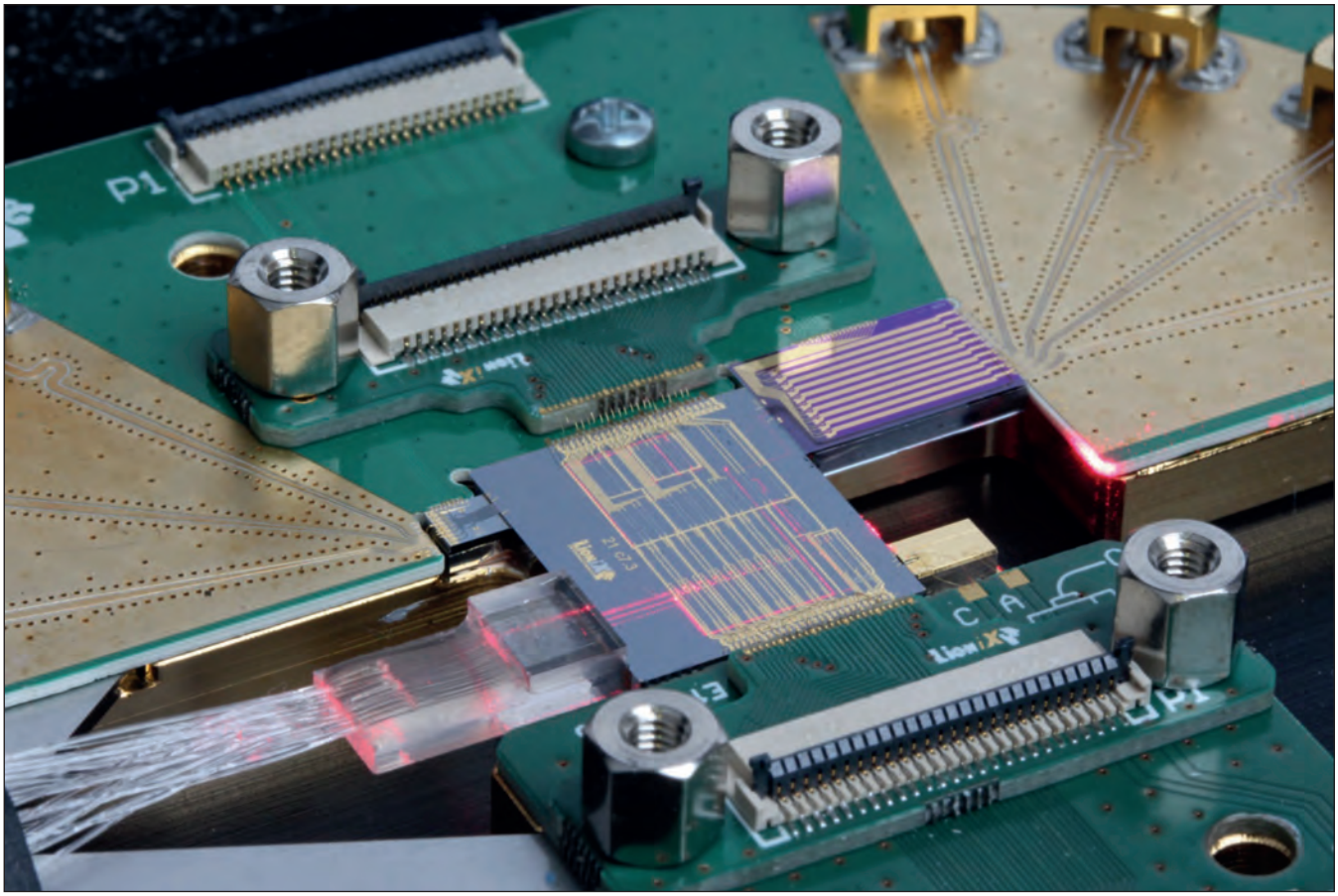

Figure 3. A RF-in/RF-out beamformer utilizing hybrid assembly to combine TriPleX true time delays and an InP laser, modulator and detectors.

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The PIC International Conference continues to grow in scale nd stature year on year and is now firmly established as the must-attend conference for the PIC industry. With an attendance in 2019 of 700 senior level delegates including representatives from Facebook, Intel, IBM, and the European Commission among many others, the event was our largest yet.

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The rapidly evolving nature of photonic integration, silicon photonics (SiP), optical computing and automotive SoCs tied to PICs offers new manufacturing opportunities. We will explore programmable PICs, the coherent vs. incoherent debate, quantum encryption and the latest integration/hybridization approaches for light sources and other PIC devices.

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Scalability is a key manufacturing interest as pilot lines set the stage for volume manufacturing. What metrics can best be applied to design and manufacturing as the industry pivots to higher production levels? Is a total quality management (TQM) approach vital to long-term vitality? We'll explore TAP within a quality matrix and how today's systems can be readied for long-term scalability and margin growth.

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As PICs move from 100G to 400G, the future will require 800/1600G devices - can we set the stage today for a smooth transition? We will explore leading pathways to a PIC-enabled future and what needs to be initiated in the short-term to satisfy long-term requirements. What role might quantum technologies play to increase performance, reduce power consumption and improve quality?

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Micro-transfer printing
From wafer to wherever

Micro-transfer printing (MTP) is already being used in many microelectronic applications for the large-scale transfer of die with exceptional accuracy. The experts at X-Celeprint offer insights into MTP PIC applications including mounting lasers, detectors, amplifiers and other components to SOI and SiN platforms utilized for today's datacom / telecom transceivers as well as PIC device evolution.

BY JAMES THOSTENSON, PHD, PROCESS DEVELOPMENT SCIENTIST AND JULIA ROE, OPERATIONS DIRECTOR, X-CELEPRINT INC

MICRO-TRANSFER PRINTING (MTP) enables the massively parallel transfer of dies to a target substrate - the surface to which microelectronic devices are printed. Transfers exceeding 82,000 dies per print at 99.94% transfer yield have previously been demonstrated. Many materials are suitable as target substrates.

Glass, silicon, III-V, plastics, and multiple other commonplace materials have been employed (see Linghu et al. for a brief overview)[2]. Target substrates can be round wafers, rectangular sheets (such as glass), or even flexible materials. MTP frees the target geometry from reticle size constraints, so very large area substrates (e.g. 600 x 600 mm) are possible. In many cases, a device can be printed to a target substrate without any further modification. The device is either directly bonded to the target substrate, or in some cases, the target substrate is planarized with an adhesive resin onto which a device is printed. Following printing, the resin is then back etched to reveal electrical contacts, and a metal redistribution layer (RDL) is made to electrically interconnect the devices to the target substrate.

How does it work?

Just as a gecko clings to a seemingly smooth surface, an elastomer stamp can grasp a microelectronic device. The means by which either grasps and releases an object relies on a physiochemical interaction known as Van der Waals forces. Named after the famed scientist Johannes Diderik van der Waals for his findings in intermolecular interactions, these forces exist in repulsive and attractive nature dependent on a number of molecular properties.

In the case of MTP, these forces can be exploited using a polydimethylsiloxane (PDMS) stamp to quickly pick up a microelectronic chiplet from a source material and then place it onto a target material. As highlighted in Figure 1, the rate at which the PDMS stamp picks and places the chiplet will determine the adhesive forces between the two objects and therefore can be tuned to accommodate printing of a number of microelectronic or photonic materials. This rate (dependent on its viscoelastic property) forms the basis for MTP.

Source wafer to target wafer process

As first demonstrated by Meitl et al.,[1] MTP can be used to pick and print a wide array of devices from a source to a target material en masse. A source wafer, a wafer from which devices are natively created and picked, requires two minor process additions to make it pickable.

An example of a pickable device can be seen in Figure 2. First, the creation of a sacrificial layer that can then be undercut to release a device is needed. In practice, buried oxide, photoresist, and other common-place sacrificial layers can (and have)[2] been used to release a device for printing. Second, and common to MEMs, tethers and anchors are employed to keep a released device from collapsing onto the source wafer. Commonly, the tether is made from photoresist, silicon nitride, or silicon oxide – all of which are ubiquitous in semiconductor fabs.

The anchor is usually of the same material and layer structure as the device. Orientation of the device, anchor, and tether are then chosen to increase the

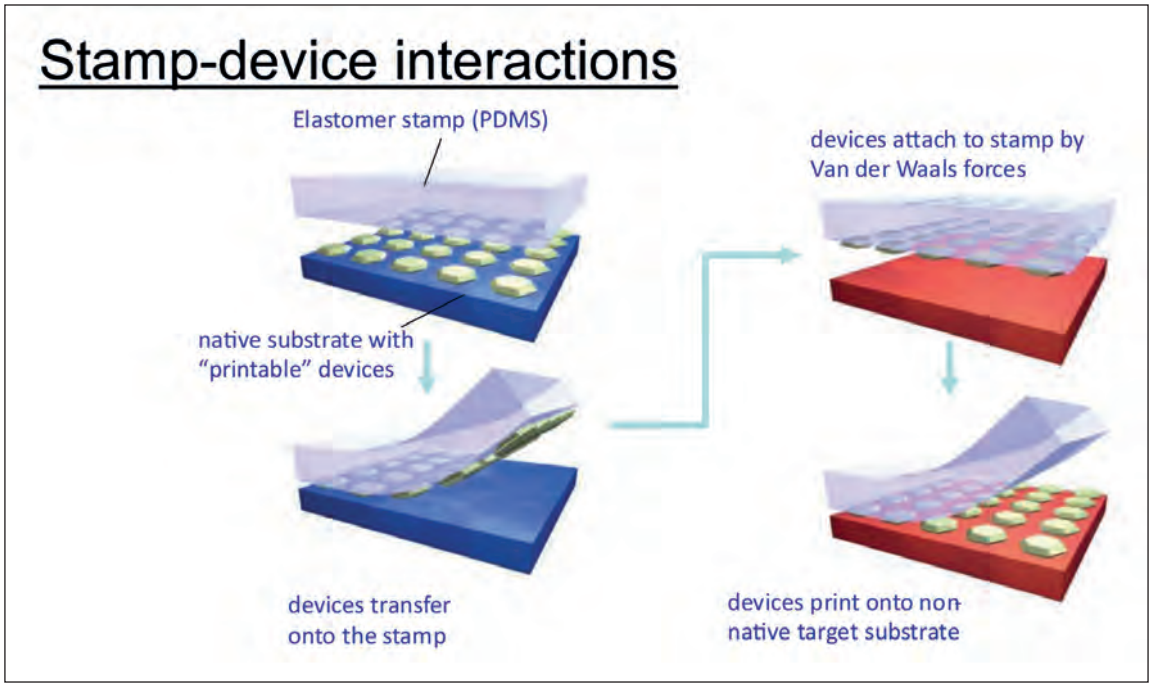

Figure 1: Basic process of micro transfer printing (MTP). Adapted from Meitl et al.[1]

speed at which the device is released and to limit the amount of undercut to the anchor.

What are the capabilities and benefits?

The unsung hero of MTP is the elastomer stamp. The elastomer stamp has multiple inherent benefits, a few of which will be listed here and are summarized in Figure 3. PDMS, the common elastomer material used for MTP, is low cost, has good Z-directional compliance to pick up almost any combination of topographical and smooth surfaced devices as a result of its soft and conformable material properties. Yet, it has lateral stiffness such that wide arrays of devices can be accurately picked and placed to sub-micrometer precision.

The material is largely chemically inert and robust; it has no residual effect on the materials with which it picks. Moreover, it can be used repeatedly, with demonstrations showing more than 25,000 prints with a device transfer yield of 100%. PDMS is transparent at millimeter thicknesses such that vision systems can be employed for quick registration and verification of device transfer. And last, but perhaps most importantly, the stamp is scalable for semiconductor manufacturing as shown in Figure 4.

Fan-out and Fan-in methods of device printing can be realized through MTP. Depending on the target die size and pitch, stamps can be created such that they pick from a densely populated source wafer and print

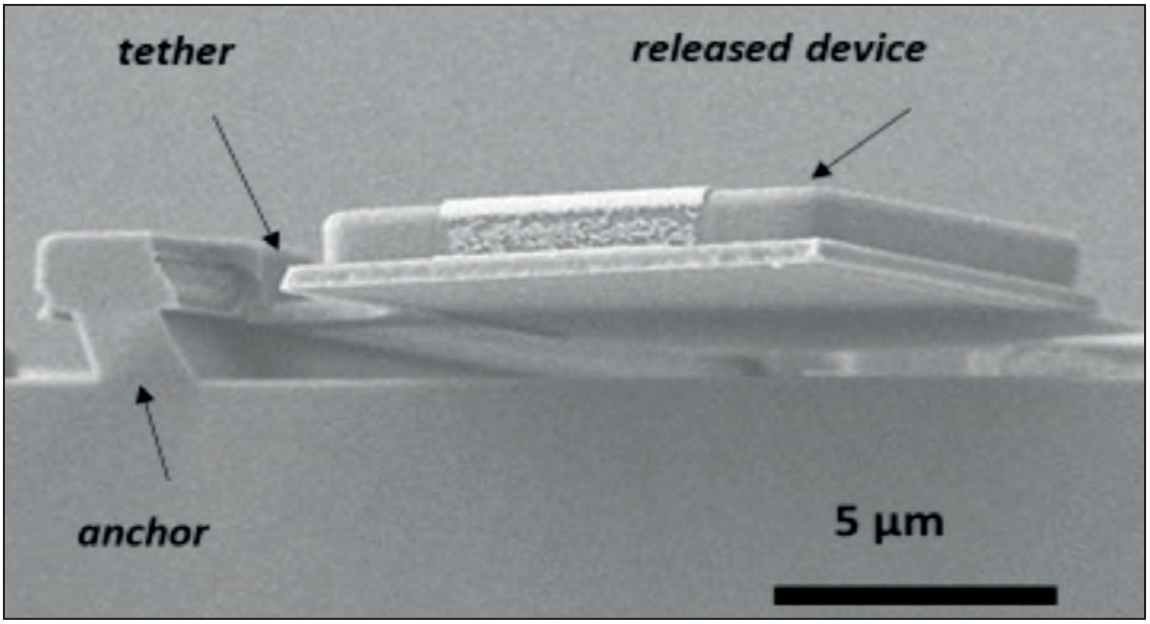

Figure 2: Scanning electron micrograph of a released device suspended above the open cavity by a tether and anchor.

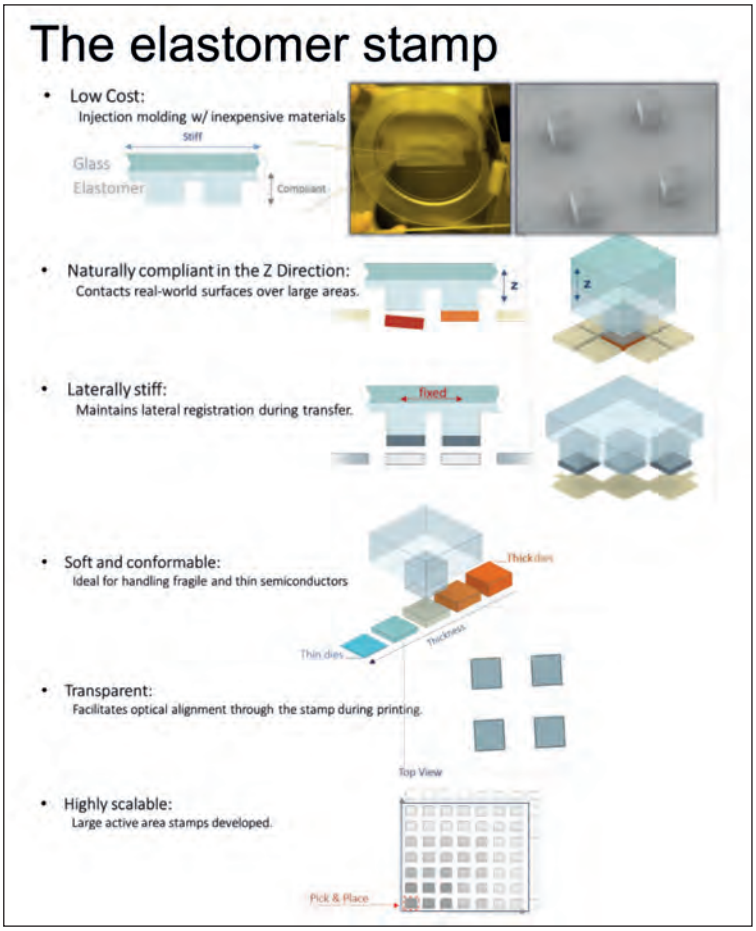

Figure 3: The multiple benefits of an elastomer stamp in MTP.

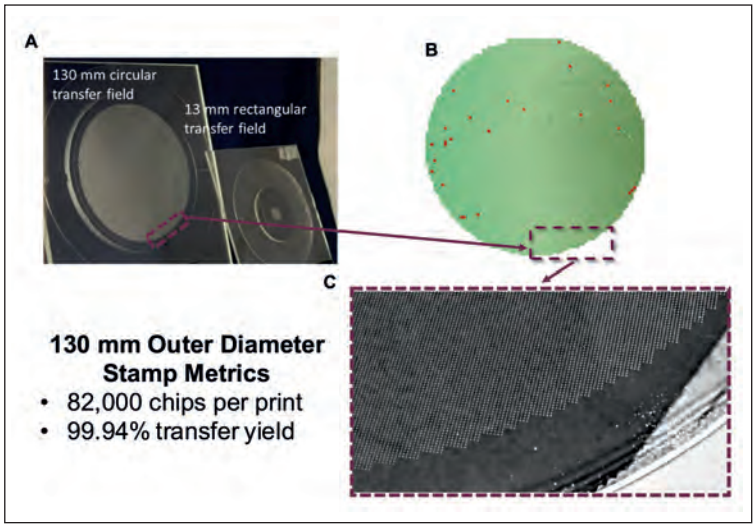

Figure 4: A) A PDMS stamp of a 130 mm circular (left) and 13 mm rectangular (right) transfer field. The 130 mm circular transfer field, matches a 150 mm wafer less a 10 mm edge, B) shows the device yield where pixels indicate successful prints and red pixels indicate failed prints. For 82,000 chips per print, 99.94% were successfully transferred. C) shows a close-up of the 130 mm circular transfer field at edge where the upper left portion is filled with PDMS stamp posts.

to a sparser source wafer – fan-out. Or, the opposite can be done such that a sparsely populated source wafer is picked and the target wafer is much denser in device population – fan-in. An example of fan-out from a dense source wafer can be found in Figure 5.

What are typical MTP applications?

MTP is an existing manufacturing technology – it is not just a research topic. To date, multiple technologies (as shown in Figure 6) have used MTP to enable heterogenous integration. Solar, biomedical, consumer electronics, telecom, and displays are just a quick list of the industries which have either demonstrated use of MTP capabilities or are actively using it. X-Celeprint has built an automated tool that can robotically load and unload wafers for true mass transfer of devices from source to target wafers. This tool (Figure 7) is also capable of automating the inspection of the transfers post-print to determine how many of the devices were picked from the source wafer and how many were printed to the target wafer: in other terms, it can automatically determine the effective yield of devices.

What industries can benefit from micro-transfer printing?

The disruptive promise of MTP has led the European Commission (EC) to spear-head two large initiatives between X-Celeprint and European industrial partners with the intent of placing the manufacturing technology centrally within European borders. These two initiatives are Caladan and Micro Prince. Caladan is funded by the EC Horizon 2020 program and the project aims to incorporate transfer printing to SiGe devices and quantum dot lasers over the next 3 years. Micro Prince is a €14.4 M ECSEL, 3-year program currently underway that is coordinated by X-FAB MEMS Foundry GmbH with partners Melexis, Optics Balzers, and IMEC. Other industrial beneficiaries of MTP are found wherever the need for heterogeneous integration has limited scalability. From a broad perspective, the photonics industry has perhaps the greatest potential in benefitting from MTP due to its inherent need of putting III-V components onto Silicon-based chips containing optical waveguides and

The photonics industry has perhaps the greatest potential in benefitting from MTP due to its inherent need of putting III-V components onto Silicon-based chips containing optical waveguides and electronics

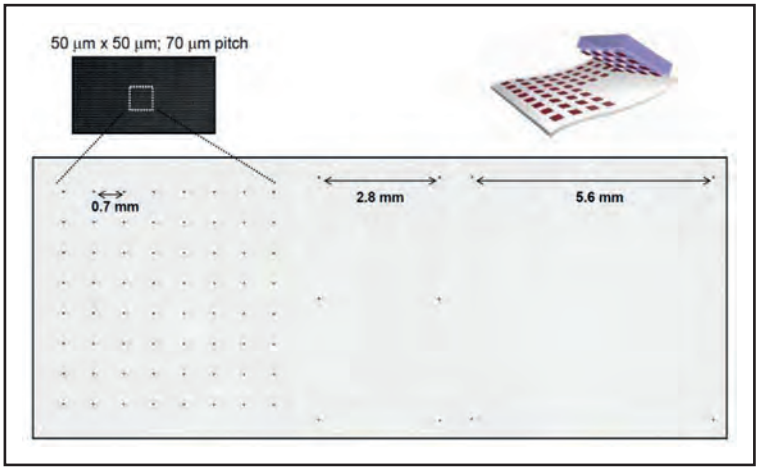

Figure 5: Example of fan-out capability for LEDs printed from a dense 70 micrometer source wafer (upper left) to a more sparsely populated target wafer of 0.7, 2.8, and 5.6 mm pitch (bottom). Adapted from Park et al. 3

Figure 7: Automated MTP X-Celeprint tool capable of up to 200 mm wafer diameter fabrication.

electronics. In multiple reports, MTP has demonstrated capability in mounting active components, such as lasers, detectors, amplifiers, modulators and other components from III-V materials, to high-transparency waveguide platforms such as silicon-on-insulator and silicon nitride to create high bandwidth transceivers for data in data center and telecom applications. While several companies are currently selling transceivers with photonic integrated circuits made using conventional processes, MTP is expected to enable the next generation of smaller and more powerful optical chips.

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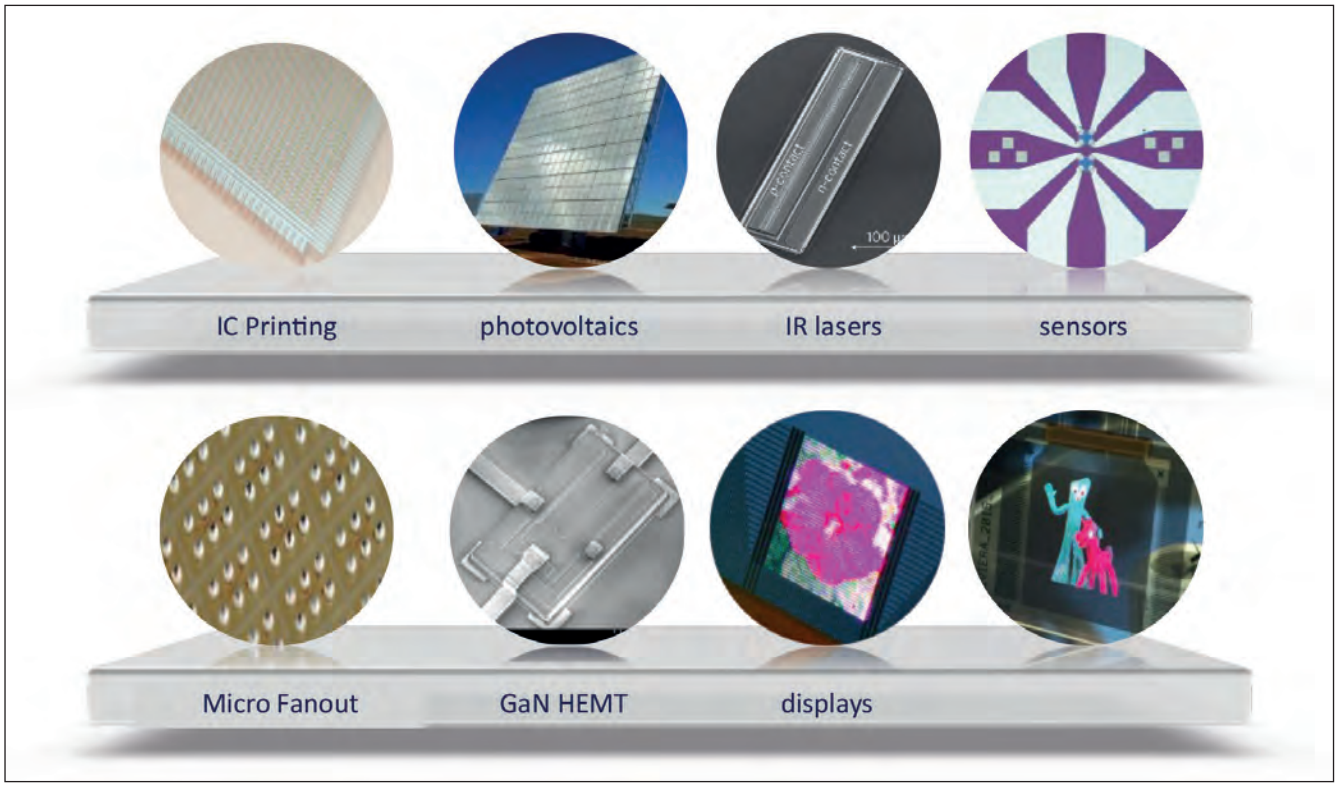

Figure 6: A list of technologies that have already benefited from MTP. Each image shows a device that was created using MTP.

EPIC reports results from the 2019 World Tech Mapping Forum

The Fraunhofer Heinrich Hertz Institute (HHI) hosted the World Technology Mapping Forum in June. Organizers PhotonDelta and the AIM Photonics Academy brought together 100 key participants from the growing photonic integrated circuits (PIC) ecosystem to work towards a unified roadmap for industry to accelerate innovation, reduce environmental impacts and cut costs.

BY JOSÉ POZO, CTO, EPIC

THE 2019 World Technology Mapping Forum (WTMF-3) was held in Berlin from 12-14 June with the aim of updating and discussing the Integrated Photonic Systems Roadmap (IPSR-I). The goal is to meet global technology needs in 2040 and beyond. The 3-day event comprised key notes on a range of topics including telecom & datacom; global packaging challenges; sensing; testing for network integration; automation and testing for volume production[1].

There were also workshops on challenges in managing the PIC ecosystem and interactive plenary discussions on packaging and testing solutions for the four main photonic integration platforms: silicon, indium phosphide, polymer and TriPleX[2].

Background and the significance of the WTMF-3

As with WTMF 1 & 2, a main focus of WTMF-3 was

how best to: 1) establish and sustain a trust-based global network of partners working together on photonic integrated circuits and systems in order to jointly enable the fastest possible technology and application developments in photonics; 2) reach company agreement and collaboration on problem definitions and solutions; and 3) develop ecosystems and establish close collaboration between integrated photonics and micro-electronics.

The need for standardisation

The emphasis on the terms 'trust based', 'working jointly', 'collaboration' and 'agreement' in many of the discussions underlines a fundamental challenge for the photonics sector: the need to establish globally agreed and trusted standards for design, fabrication testing and packaging.

As Professor Ton Backx, President of the Institute for Photonic Integration at Eindhoven University of Technology points out, the same problem was faced in the early days of the development of semiconductors. In the beginning, industries developed their own manufacturing processes and started to use specialized machines built by different commercial companies to their own standards. But this specialization worked against growth of the industry because a company could not successfully mass produce a new product if essential components and systems were not available around the same time. The semiconductor industry resolved this issue by creating the International Technology Roadmap for Semiconductors (ITRS), to establish a joint vision, common standards and an agreed timetable as to when a certain capability or performance would be needed. The ITRS grew into a trusted technology assessment network that worked because it was always independent of any commercial interests pertaining to individual products or equipment.

The need for a single global vision for photonics

It has been recognised for some time that the photonics industry will be unable to successfully scale up in the same way as semiconductors unless it adopts a global approach to mapping. This means shared manufacturing platforms and standards for photonic integrated circuit design to enable cost-effective, high-volume manufacturing. These are going to be needed by emerging industries like 5G Telecom, next generation data centres and a wide variety of smart "connected" sensors to facilitate the Internet of Things (IoT).

However, one of the problems for global standards in photonics is that, until recently, photonics roadmaps have been created at a regional rather than international level. This is due mainly to a different focus on materials available for chip wafers. For example, since 2012, Eindhoven University of Technology has been the driving force behind the Joint European Platform for the Integration of Photonics Systems and Circuits (JePPIX) with its focus on indium phosphide and silicon nitride (TriPleX) waveguide technologies. In contrast, the Integrated Photonic Systems Roadmap (IPSR), was established

World Technology Mapping Forum (Source: Jonathan Marks, Critical Distance BV)

Interactive Plenary Discussion (Source: Jonathan Marks, Critical Distance BV)

in 2017 for countries like France, Belgium, Japan, the USA, and Taiwan who had developed expertise in silicon photonics.

A truly international approach

In view of the fact that both roadmaps were set up to address technology gaps and challenges limiting the advancement of integrated photonic system manufacturing, it was decided in 2017 to move towards a single coherent roadmap - the Integrated Photonic Systems Roadmap International (IPSR-I) that would combine the experience and knowledge gained from JePPIX and IPSR. Additionally, organizations and companies in Asia would be invited to participate to make the roadmap a truly global initiative.

In the last two years, parallel technical working groups in the US, Europe and Japan have been discussing how to achieve a single coherent road map to accelerate the global photonics industry. For example, one proposal from the IPRS-I discussions is that next generation transceivers used for short distance links will be predominantly developed using silicon-based photonics fed by an external laser while indium phosphide based high speed transceivers will be used for longer distances.

Prof. Kimerling's keynote presentation (Source: Jonathan Marks, Critical Distance BV)

Outcomes of WTMF-3

The main findings from the keynote presentations, workshops and plenary discussions from WTMF-3 will be added to the existing draft version of the IPSR-I, which will be made more concise and published, targeting 4 quarter 2019. Follow-up meetings are in the process of being arranged for 2020 to be held in Japan, The Netherlands and the United States.

Technical challenges

As keynote speaker Michael Lebby of Lightwave Logic emphasised, it's important to appreciate that WTMF-3 and the IPSR-I roadmap is work in progress - a process that's as much about anticipating future challenges as it is about finding solutions.

As an example, he cites the concept of co-packaging, i.e. putting the photonic chip very near to the electronic chip on a printed circuit board, which will be unavoidable because microelectronics on its own is unable to deliver cost effective, reliable and high performance solutions for future market needs.

Limitations of microelectronics

As explained in Prof. Kimerling's keynote presentation, the main problem with microelectronics is that scaling in terms of cost, power dissipation and clock frequency is over: cost scaling of mass transistor sets ended in 2012 with 20M transistors per dollar but since then, the push for further miniaturisation has increased cost. Similarly, in 2005, power dissipation per chip peaked at 100W and clock frequency flattened at 3 GHz.

Moreover, Moore's Law scaling of 100 times every 10 years in the microelectronics industry will not fit future demand. In high performance computing, for example, floating point operations per second (FLOPS) are still scaling close to 1,000 times every 10 years, i.e. 10 times faster than Moore's Law. The reason for this is that these operations are based on a distributed system which is communication centric. i.e., when bandwidth is low, copper is adequate but as bandwidth demands increase so does the need for copper and the metal is no longer a cheap technology. Similarly, data centre bandwidth density is expected to increase a million times by 2040, which can only be achieved at constant cost and energy by integrating PICs into the systems.

The challenges for PIC integration

Due to the different physics involved, integrating both photonic and electronic functions is an extremely difficult challenge. For example, PIC operating speeds are too fast for long electrical tracks on a printed circuit board. Then there are issues caused by differences in power dissipation and heat while still maintaining high performance at the right price. Other challenges include connectivity of photonic and electronic components, and how to handle massive optical I/O (input/output) two or three generations down the road.

Interactive Plenary Discussion with José Pozo (Source: Jonathan Marks, Critical Distance BV)

Moreover, the increasing complexity of next generation chips will require a solution to the challenges of using silicon and indium phosphide on the same chip. The problem is that light losses in silicon based passive light processing will require additional light sources, which can only be provided by active PICs on indium phosphide substrates.

One way to achieve this is to build active islands using indium phosphide on the silicon photonics chip. Another option is an indium phosphide chip handling all photonics processing functions on top of a silicon carrier that can take care of the microelectronics driver and additional signal processing.

A new paradigm

Anticipating these challenges in photonics is akin to the "red brick walls" predicted on the semiconductor roadmap 30 - 40 years ago and it is helping to establish a new paradigm in photonics termed 'system level parallelism' under which internode spectrum bandwidth is the new scaling variable and is expected to double capacity every year.

Ultimately, perhaps the biggest challenge for the photonics sector is how to persuade the $400 billion semiconductor industry to align its supply chain in order to adopt the standardisation of materials, design, packaging, functionality and performance as well as transition in synchrony to this new scaling platform.

More involvement from Industry

In this context, a common call from WTMF-3 participants was for a stronger input from industry to: 1) make future forecasts more accurate and reliable; 2) foster greater awareness among the wider ecosystem of the inevitability of photonic integration in microelectronic systems; 3) promote greater appreciation for what the new technology can offer and the challenges involved. Trust needs to be built up in this area, which can only happen if the roadmap has many voices, especially from the large industry players.

But participation from industry is necessary for another reason. As José Pozo, EPIC's CTO points out in his WTMF-3 wrap up, the IPSR-I roadmap crucially needs input from companies involved in the manufacture of photonics products.

For example, companies in the automotive, aeronautic and telecom sectors, e.g. who want to collaborate with companies developing spectrometers or who are looking at the LiDAR market, because, as José concluded:
"Now is the time - we can make things smaller, low cost and reliable in large volumes. Photonics integration is the future, but the future won't exist without market pull."

At the conclusion of the June meeting a schedule for the IPSR-I in the coming year was established:

- 2019 Winter meeting: January 2020, Asia, (exact date and place to be announced)
- 2020 Spring meeting: March 2020, California, USA,
- 2020 Summer meeting: June 2020 Eindhoven, the Netherlands

[1] Videos of most keynote presentations can be found at: http://www.wtmf.eu/news1901/keynotes/
[2] Videos of interactive plenary sessions and results from the workshops can be found at: http://www.wtmf.eu/news1901/results

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ECOC
offers a snapshot of PIC progress

At ECOC many big names, including Intel, Infinera and Hewlett Packard Enterprise, unveiled their latest plans for their PICs.

RICHARD STEVENSON REPORTS

MOST OF US take our mobile phones for granted. We are so used to having them by our side that we easily overlook the phenomenal computational power they provide. This prowess stems from the tremendous miniaturisation of the transistors on the integrated circuit. By keeping pace with Moore's law, today's ICs pack billions of nanoscale transistors into a single chip that's no bigger than a fingernail.

Lagging far behind, in terms of miniaturisation, is the optical equivalent, the photonic integrated circuit (PIC). That's partly because this type of device is not so easy to scale, as optical features cannot plunge into the sub-wavelength domain. However, progress is also impaired by a far greater number of devices on the chip – the circuits contain lasers, amplifiers, modulators, gratings, and diodes, linked by optical waveguides. And last but by no means least, the rate of improvement is hampered by a lack of a consensus on the right material system for the circuit. While there is no question that silicon is the best choice for the all-electronic IC, there are several candidates for the PIC, including silicon architectures with either SiO_2 or SiN waveguides, and all-InP solutions.

Championing many of the different options were a number of speakers at the 45th European Conference on Optical Communications, held at the Royal Dublin Society, Ireland. At this meeting, presenters made their case for the right mix of materials for a particular application in several well-attended sessions, including three on Sunday, before the conference was in full swing.

Infinera extols InP

Without doubt, the darling of the InP PIC industry is Infinera, the Californian-headquartered vertically integrated manufacturer of optical transmission systems made with its own chips. This company launched its first product back in 2004, and over the intervening years its annual revenue has climbed to now net nearly $1 billion per annum. Speaking on behalf of the company at the Integrated Photonics Workshop, held on Sunday morning, Vice-President Mehrdad Ziari extolled the virtues of PICs that are based entirely on InP. He argued that this material is best-placed to increase capacity: it allows modulation schemes that transmit much data, such as 64 QAM; it enables 100 Gbaud; and it promises 1 Tbit/s per wavelength. One of the benefits of integration, argued Ziari, is that it offers a good route to increasing the number of channels – Infinera has had 10-channel PICs in production for several years.

Ziari went on to highlight other virtues of an all-InP PIC. These chips require a light source, and according to Ziari, one of the merits of the monolithic approach is "native gain", as InP is the ideal material for making the laser. Working with InP also enables devices to deliver low-noise, along with a high efficiency that reduces cooling requirements. What's more, according to Ziari, InP can deliver economic benefits. He argued that Infinera has put together an InP line that produces consistent yields, high-quality chips, and has the ability to offer scalable, future-proof production.

Infinera has recently developed its fourth generation of technology, detailed in a talk given by Ziari's colleague Stefan Wolf, a Senior Test Development Engineer at Infinera. Speaking during a technical session devoted to transmitters and photodiodes, Wolf explained that on the transmitter side of Infinera's latest PIC, there is a new addition, a widely tunable laser with a range of 50 nm.

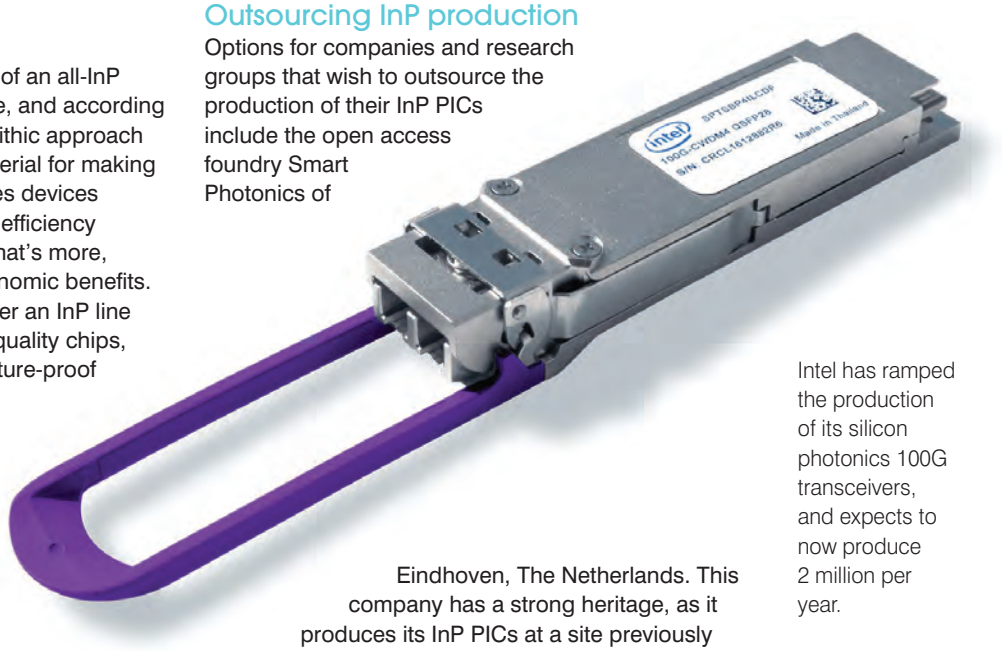
This is claimed to be a best-in-class laser, in terms of its bandwidth. For every laser on the chip, there are two modulators – one for each polarisation – and two semiconductor optical amplifiers. On the receiver side, the tunable laser acts as the local oscillator. For each of these lasers there are eight high-speed photodiodes.

Another significant departure from previous generations of technology is the use of a flip-chip technology for electrical connections, rather than wirebonds. Flip-chip bonding is providing more than 1000 connections between an Infinera InP chip and an application-specific IC that is made from SiGe and acts as a modulator driver and a transimpedance amplifier. Production of this IC is based on a 180 nm SiGe BiCMOS process, capable of producing transistors with a cut of frequency of more than 230 GHz, and a maximum oscillation frequency in excess of 270 GHz. According to Wolf, these high values contribute to the high linearity and low noise of the amplifier.

Infinera's fourth generation technology has enabled 100 GBaud, 32 QAM transmission over 500 km of fibre. The Q-factor associated with this is 6dB. "There is plenty of margin for error correction," said Wolf, indicating that transmission at 800 Gbit/s is feasible.

Outsourcing InP production

Options for companies and research groups that wish to outsource the production of their InP PICs include the open access foundry Smart Photonics of Eindhoven, The Netherlands. This company has a strong heritage, as it produces its InP PICs at a site previously owned by Philips and JDSU Uniphase. Since its founding in 2012, the workforce at Smart Photonics has mushroomed from four staff to more than 70.



Intel has ramped the production of its silicon photonics 100G transceivers, and expects to now produce 2 million per year.

Speaking on behalf of the company during a special event on Sunday that focused on the challenges and solutions associated with PIC Manufacturing, Smart Photonics' CTO Luc Augustin offered an insight into what his firm can offer its customers. To support the development of the PIC, it has developed a dedicated process design kit. This can be used to evaluate designs that incorporate the company's lasers – DFB and DBR designs with outputs in excess of 10 mW, and tuning ranges that can be more than 60 nm – and

other photonic components that an operate at more than 25 GHz.

To aid development of designs, Smart Photonics has been offering multi-project wafers since 2013. Runs start every quarter, providing customers with regular opportunities to modify and advance their chip architecture.

The perfect size?

Another company piquing the interest of delegates at ECOC was the fabless manufacturer of chipsets, Rockley Photonics. It uses a combination of silicon photonics and III-Vs in its products. Company's co-founder and VP R&D Silicon Photonics, Aaron Zilkie, described this combination of materials as "the best of both worlds", during a talk he gave at the Integrated Photonics Workshop.

What distinguishes Rockley Photonics from its peers is the size of the features in its chipsets. It pursues what it describes as a multi-micron waveguide platform.

Infinera builds networking equipment that features its own photonic integrated circuits, made from InP.

Working at this larger length scale, sensitivity to width variation is claimed to plummet by a factor of 60. Additional merits are: much smaller variations in the key characteristics of the filters; an increase in yield; simplification of the fibre-attach process; and a very high degree of light confinement, enabling the use of very tight bends.

Rockley's efforts include the development of a 400 Gbit/s transceiver PIC. Its manufacture requires the use of three different foundries. Laser and modulator die are produced on a III-V line, so benefit from being made with a III-V process. A CMOS process makes the electronics, and the silicon photonic structures are produced at a different foundry.

Supercomputing solution

One opportunity for integrated photonics is to 'green' supercomputers. Sales of these power-hungry machines are growing a rate of about 9 percent per year, thanks to huge support from governments all over the world. Dominating this market is Hewlett Packard Enterprise, with a 35 percent share – a figure that is set to climb even higher when it acquires Cray next year.

During an Industry Focus session entitled *Photonics integration and digital silicon photonics* Di Lang, a Senior Research Scientist at HP, outlined how PICs can come to the aid supercomputers. These machines are undergoing a change in architecture, with a shift from process-centric computing to one that is memory-driven, allowing advances that do not rely on maintaining the march of Moore's law. The new architecture needs low cost, small form-factor links. Liang and co-workers have been investigating the best solution for many years, and have considered both external lasers, including VCSELs, and the addition of InP-based lasers and InGaAs photodetectors onto a silicon chip.

Due to power constraints, the team at HP is pursuing quantum dots lasers for its PICs. HP is working with Innolume to produce these lasers, which produce a comb-like spectrum, and combine a high gain with stability at elevated temperatures.

Intel's milestones

A more well-known market for the PIC is in the data centre, where it can help to prevent a bottleneck in connectivity. This is the market Intel is targeting. After a decade of development, it is now enjoying significant sales of 100 G transceiver silicon photonic products.

Robert Blum, who leads strategic marketing and business development at Intel, told delegates attending the Integrated Photonics Workshop that the company had now shipped 2 million 100G transceivers since the launch of the first product in 2016. Thanks to a ramp in production, Intel is now manufacturing 2 million of these per year. The portfolio is also set to grow, with a planned ramp of 200G and 400G products throughout next year.

Production of these PICs involves the bonding of InP-based chips, containing a quantum well stack, to a handle wafer, before they are then attached to a 300 mm silicon wafer. No critical alignment is needed, and the laser cavity is formed on the silicon wafer in a manner that ensures 90 percent coupling between the laser and the silicon photonic waveguides.

Speaking at the market focus session, Blum's colleague Thomas Liljeberg, who has the role of General Manager of Photonic Integration within the Silicon Photonics Products Division at Intel, said that the approach that's adopted allows standard wafer testing. "Photonics looks more like silicon," said Liljeberg, who explained that the process aids production, as it only proceeds with known good die.

In the technical session on silicon photonics and hybrid integration, more details on the performance of Intel's lasers were given by another company spokesperson, Yuliya Akulova, who is Director of R&D within the Silicon Photonics Products Division. She revealed that the 1310 nm lasers on the chip can deliver more than 25 mW at room-temperature, and more than 15 mW at a substrate temperature of 120 °C. "Performance characteristics are exceptionally good."

These laser have been put through extensive reliability testing. Sampling of 30 devices revealed no degradation over nearly three years.

Engineers at Intel have also produced devices with four channels, operating at 1270 nm, 1290 nm, 1310 nm and 1330 nm. They can be used to produce a 400 Gbit/s chip, also featuring four Mach-Zehnder modulators and four spot-size converters.

Akulova explained that Mach-Zehnder modulators have pros and cons. They are robust, but their relatively large size hampers the production of compact photonic chips. For that reason, the team is investing the potential of ring-modulators in its designs.

Just silicon

If the laser is not put on the chip, the PIC can be made from just silicon. Offering a foundry service for this is Advanced Micro Foundry – it is a spin-off of the Institute of Microelectronics, part of Singapore's Agency for Science, Technology and Research.

Speaking on behalf of Advanced Micro Foundry, Patrick Lo Guo Qiang explained that the company has a capacity to process 9,000 8-inch wafers per year with a 0.13 μm CMOS technology. The facility runs round the clock, 7 days a week, employs 160 staff, and has a combination of class 10 and class 100 areas. Material combinations offered include SOI, SiN-SOI and SiN. The foundry also has capabilities associated with producing through-silicon vias, bumping and bonding.

The wide variety of PIC presentations at ECOC highlight the great diversity of this technology. This is something of a double-edged sword: it allows the most suitable technology to target a particular application, but it hampers efforts at standardisation.

The silicon industry has taken a very different approach, and it will be interesting to see whether the PIC industry ever heads down a similar path. In the short-term, that's surely unlikely – but look further ahead, and one never knows.

ECOC 2019 was held at the Royal Dublin Society, a campus with venues used regularly for exhibitions, concerts and sporting events

Silicon-photonics nanowire filters enable flexible comb demultiplexing for elastic networks

Researchers at the TeCIP Institute in collaboration with the Inphotech Foundation and the University of Glasgow have developed the first silicon-photonics (SiP) reconfigurable optical frequency comb (OFC) demultiplexer for flexible-grid optical networking.

BY CLAUDIO PORZI, GIOVAN BATTISTA PREVE, MARC SOREL, AND ANTONELLA BOGONI

PRACTICAL DEPLOYMENT of elastic optical networks (EONs) requires key enabling technologies supporting the miniaturization of flexible optical transponders for provisioning large-bandwidth services at low-cost per users. The concept of EONs has been introduced for maximizing the spectral efficiency of next-generation dense wavelength division multiplexing (DWDM) systems operating at 100 Gbit/s per channel and beyond [1].

In EONs, dynamic bandwidth allocation of optical connections allows a more effective sub-channel spectral occupancy depending on the actual temporary traffic demand and transmission reach of the connection. This requires the departure from the classic fixed frequency grid picture for the channels' carrier wavelengths, and the migration toward a flexible-grid approach where the channel bandwidth extends over a variable number of contiguous frequency slots defined on a finely-spaced spectral grid [2]. Optical frequency combs (OFCs) are then expected to play a key role in EONs, as they can provide the reference frequency grid with the equired granularity and stability. With many frequency-locked carriers generated from a single optical source, an OFC is a much more cost-effective solution with respect to using a bank of stabilized laser sources.

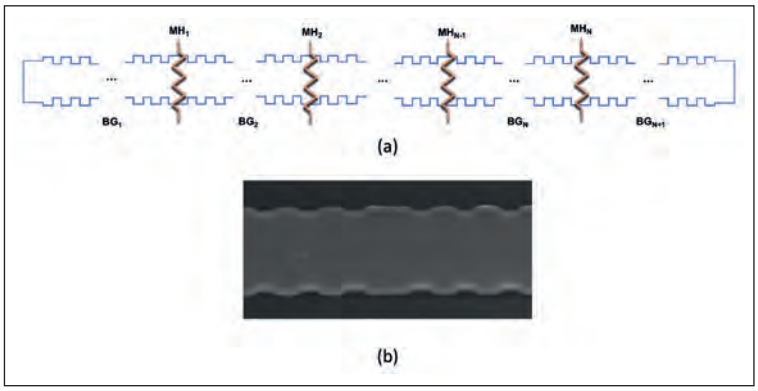


Figure 1. (a): Schematic top view layout of a Nth-order DFBR filter realized with a sidewall corrugated strip waveguide (b): Scanning electron microscope image of a fabricated grating. The devices were fabricated at the Inphotech Foundation facilities and at the James Watt Nanofabrication Centre at Glasgow University through the CORNERSTONE project.

However, in order to spark the level of flexibility envisioned by EONs, single tones need to be picked up from the comb before adding channel data encoding with the required modulation format. This task becomes increasingly difficult as the frequency spacing of the flexible grid reduces, which in turn increases the degree of organization of the network resources. The current ITU-T standard for DWDM frequency grids employs a minimum channel spacing of 12.5 GHz, which is expected to further reduce in the near future.

Although commercial optical filters based on liquid crystal on silicon (LCOS) technology can provide the required selectivity at these channel spacings, they are still too bulky and expensive for a cost-effective deployment of EONs. To this end, photonic integration can provide a key enabling solution by combining reduced size, weight, and power consumption offered by miniaturization with the potential for large-volume and low-cost manufacturing.

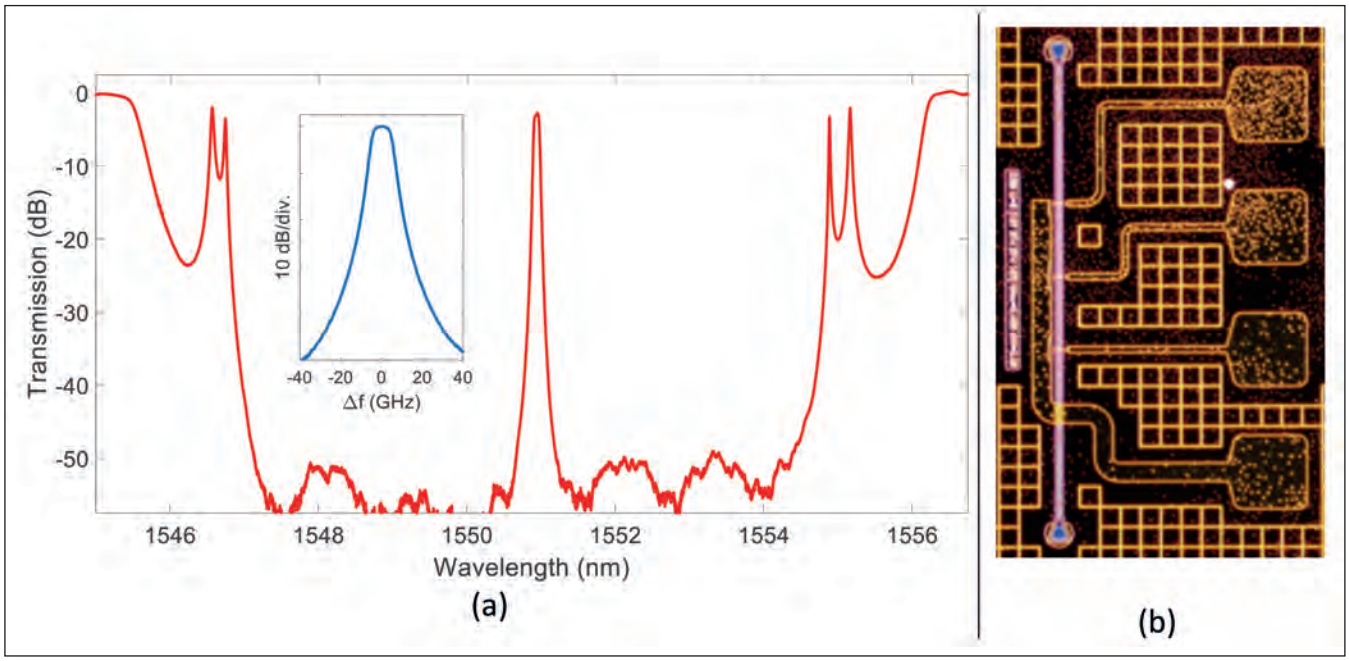


Figure 2: (a): Spectral transmission of a 3rd-order DFBR with a control signal applied to the MHs. The inset shows a close-up of the passband with a -3dB bandwidth of 10 GHz; (b): Micrograph of the fabricated sample consisting of the DFBR and metal pads and control lines for MHs.

However, realizing a photonic integrated filter matching the stringent requirements of EONs applications is not trivial. In order to be able to select a single carrier to be used in an DWDM system out of an OFC comprising several narrowly-spaced tones, a photonic-integrated filter should exhibit:

- narrow bandwidth and box-like transfer function
- large out-of-band rejection
- wide stopband region

Such filter features are simultaneously required to ensure large rejection of spurious tones over the entire OFC band as well as stable operation against possible fluctuations of the comb seed source or filter central frequency.

Silicon-photonics distributed feedback resonators

Our recently developed silicon nanowire filters fulfill all of the above requirements [3, 4]. The concept behind our design is not novel at all, as it stems from thin-film dielectric filters – a filter solution that has been widely employed in telecom applications. There, several coupled optical cavities are encompassed between mirrors formed by a stack of quarter-wave layers of two different dielectric materials.

The required filter transfer function can be synthetized by controlling the number of layers in the dielectric stacks. A photonic integrated version employs a cascade of symmetric waveguide Bragg gratings, where resonant cavities are formed at the interface between adjacent grating mirrors. Such structures, which have been originally referred to as distributed feedback resonators (DFBRs) [5], are not dissimilar from surface acoustic wave filters commonly used in modern smartphones. However, early DFBR implementations suffered from the low index contrast of the available technology, as well as from fabrication imperfections that limited the extension of the stopband and degraded the filter transfer function [6].

The use of large index contrast silicon waveguides for the fabrication of the DFBRs enables overcoming most of the limitations encountered with low-index contrast waveguides and provides unique performances with respect to others silicon-photonics filtering approaches. In fact, the strong mode confinement of strip silicon waveguides enables the realization of high quality (Q-) factor standing-wave cavities embedded between large-bandwidth waveguide mirrors with very compact dimensions.

The use of large index contrast silicon waveguides for the fabrication of the DFBRs enables overcoming most of the limitations encountered with low-index contrast waveguides and provides unique performances with respect to others silicon-photonics filtering approaches

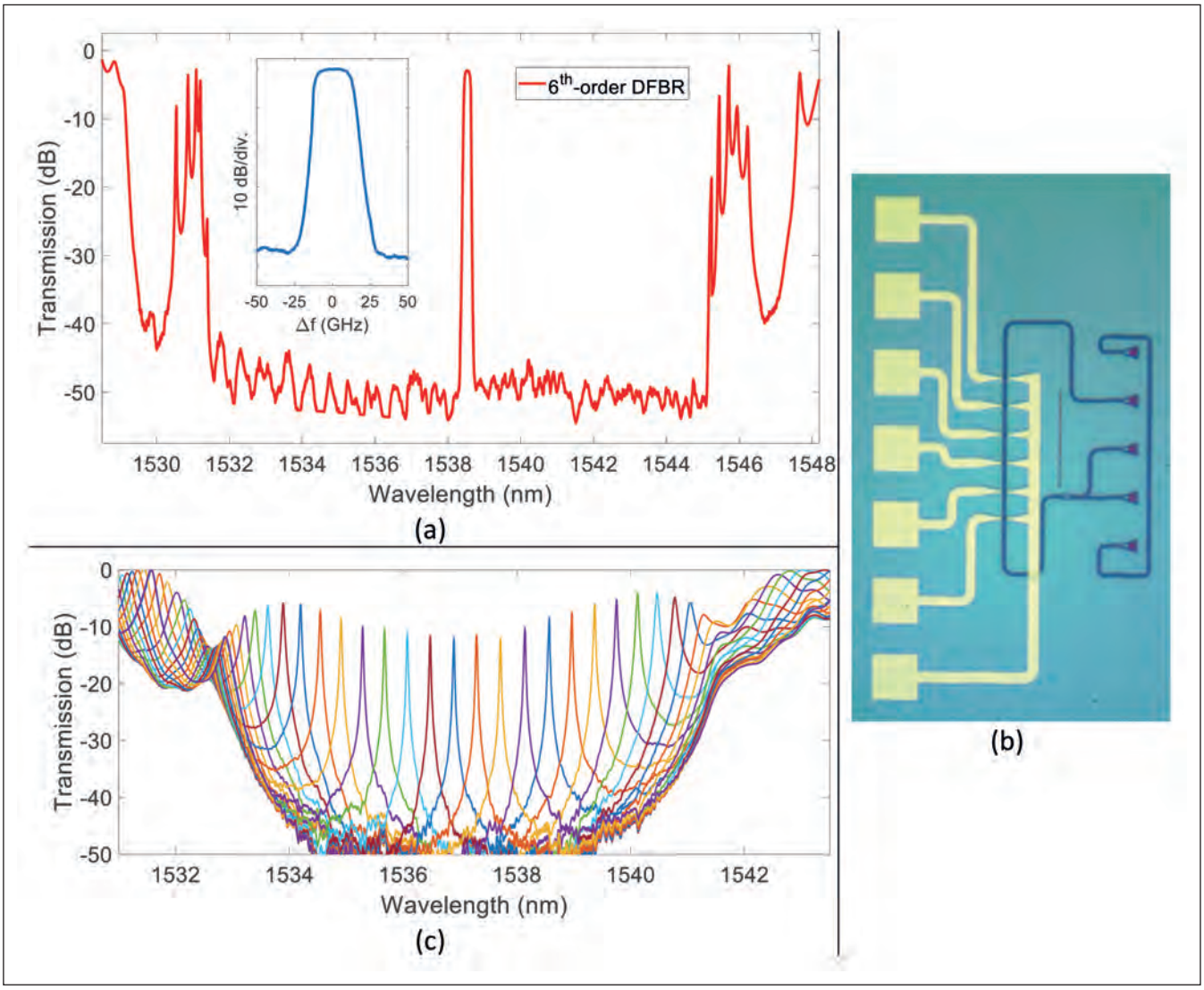


Figure 3: (a): Spectral transmission of a 6th-order DFBR; the inset shows a close-up of the passband with a -3 dB bandwidth of 25 GHz. (b): Micrograph of a fabricated 6th-order DFBR sample; (c): Tuning of the passband over the entire stopband for a 1st-order DFBR.

Filters with very narrow bandwidth down to a few GHz, fast roll-off up to 1,000 dB/nm, and exceptionally large values of the stopband-to-passband ratio can be flexibly designed in an un ultra-compact, wire-like geometry with lengths as short as a few hundreds of micrometres [4]. These features can be better appreciated when comparing high-order DFBRs with coupled microring resonator (MRRs) filters, the most commonly used approach for realizing high-order filter transfer functions in silicon waveguides. In fact, in MRRs, a bandwidth reduction is typically attained by increasing the resonator length, which in turns reduces the free-spectral range (FSR) of the filter (i.e., the frequency interval between consecutive cavity resonances), thus limiting its useful operating wavelength range besides enlarging filter footprint. However, much similarly to any resonant device realized with large index-contrast waveguides, also for DFBRs, there is a strong sensitivity to fabrication imperfections that can completely spoil the desired filter response. To solve this issue, we proposed placing local micro-heaters (MHs) in proximity of the coupled resonators so that the optical path of each cavity can be individually controlled for compensating fabrication imperfections. The schematic top-view of a typical device realized in a laterally corrugated silicon strip waveguide is reported in Figure 1, along with a scanning electron microscope image of a fabricated grating over few periods around a resonant cavity. The DFBR structures were fabricated using electron beam lithography on a standard Silicon-on-Insulator (SOI) wafer with a 220 nm-thick silicon layer and a 3μm-thick buried-oxide layer.

The MHs were implemented with narrow metal stripes deposited over a 1-um-thick silica cladding layer. A typical 3rd-order DFBR spectral transmission with control signals applied to the MHs to compensate for the resonance misalignments produced by fabrication imperfections, and a micrograph of the corresponding

fabricated device are shown in Figure 2. A narrowband transmission window with large rejection of more than 50 dB within an 8 nm-wide stopband, and low insertion loss of ~2.5 dB can be observed. Filter designs up to the 6th order have been successfully fabricated, as shown in the transfer function of Figure 3(a), in which the stopband region extends over 14 nm. The corresponding micrograph of the device is shown in Figure 3(b). The MHs also allows for passband tuning within the entire stopband while leaving the passband shape practically unaffected, for an extended filter operating wavelength range, as illustrated in Figure 3(c) for the case of a 1st order DFBR.

OFC demultiplexing with silicon-photonics DFBRs

The almost FSR-free feature of silicon-photonics DFBRs can be conveniently exploited to implement OFC demultiplexing [7]. To this end we have realized a photonic integrated circuit (PIC), implementing the 1x4 OFC demultiplexing architecture of Figure 4, in which an input optical comb is delivered to four replicas of a 3rd-order DFBR through a passive splitter. A picture of the fabricated PIC is also shown in Figure 4. The total footprint of the device is about 0.5 mm^2, excluding metal connections and pads. Figure 5 shows the spectral transmissions from the four output ports when the MHs of three out of four DFBRs are used to optimize the filters response.

The transmitted spectra from two different outputs when an OFC comprising four 12.5 GHz-spaced tones is sent to the demultiplexer input is shown in Figure 6, where the spectral response of the corresponding DFBRs selecting the two inner comb tones are also shown. A minimum spurious tone rejection of nearly 30 dB is attained, a value meeting the requirements for data transmission within a DWDM system. The low inter channel cross-talk between adjacent channels due to the presence of spurious modulated tones has been assessed by re-combining the output signals from the demultiplexer after data modulation and transmission along the same fiber link. The measurements indicated almost negligible additional received power penalty of about 0.5 dB for the bit-error ratio between the combined data after transmission through 40 Km of standard single mode fiber and the modulated signal obtained from a single demultiplexer output, as reported in Figure 7.

Future research

Further reduction of inter-channel cross-talk as well as narrower comb spacing can be attained by designing DFBRs with smaller bandwidth and larger roll-off. This is illustrated in Figure 8, which reports both the measured passband transfer functions of two 3rd-order filter designs suitable for operation with 6.25 GHz comb-spacing. Higher-order filter designs can also be conveniently employed to improve the roll-off while retaining the flatness of the passband for optimized demultiplexing operation. Several other aspects are currently being considered for improving

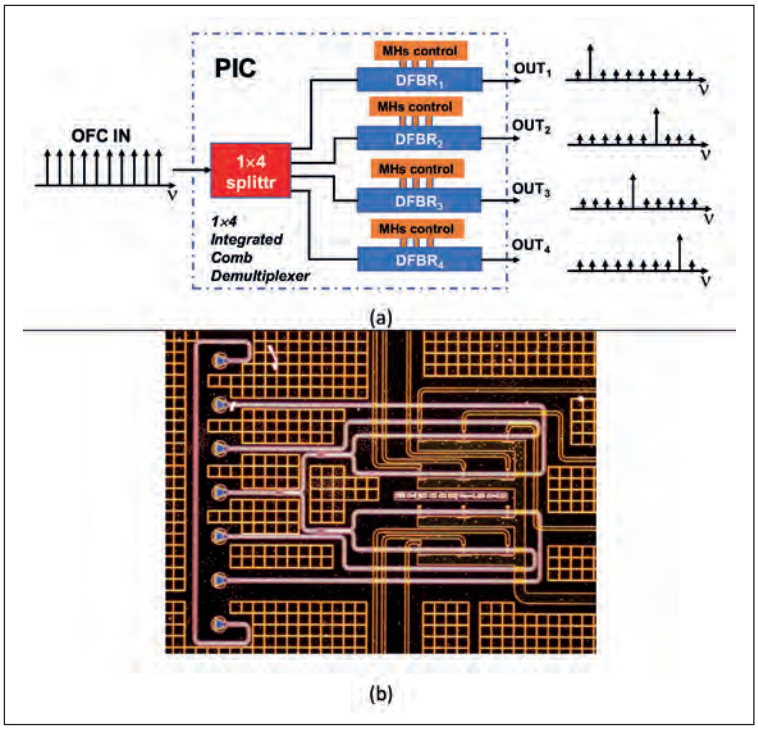


Figure 4: (a): Schematic operation of a photonic-integrated 1x4 OFC demultiplexer based on DFBRs; (b): Micrograph of fabricated device.

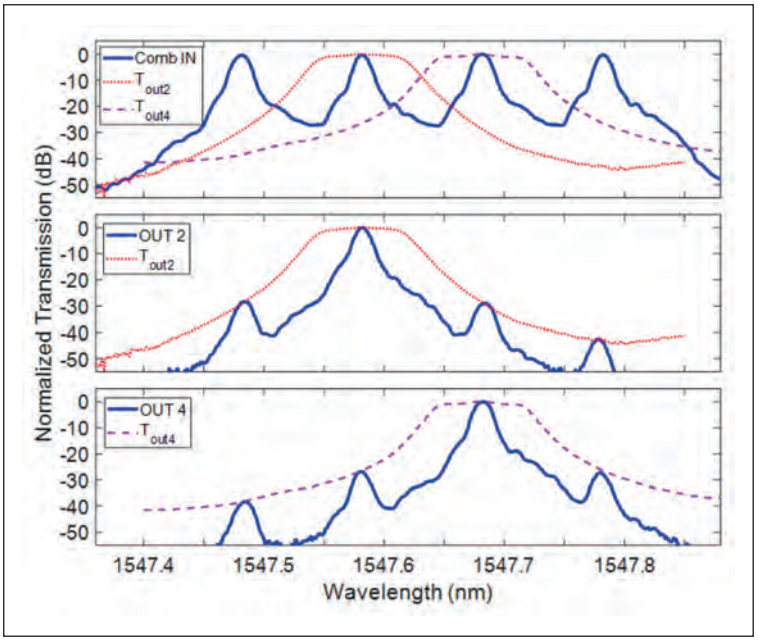


Figure 5. Normalized spectral transmission at the four output ports of the OFC demultiplexer when three DFBRs out of four are tuned through MHs for optimized response.

our results. For example, in order to avoid splitting loss for large output port count of the demultiplexer, an add-drop configuration using a contra-directional coupler architecture [8] is under study. Fabrication of the DFBRs using DUV lithography, more suitable for large mass production, is also an important aspect and different grating geometries aiming at

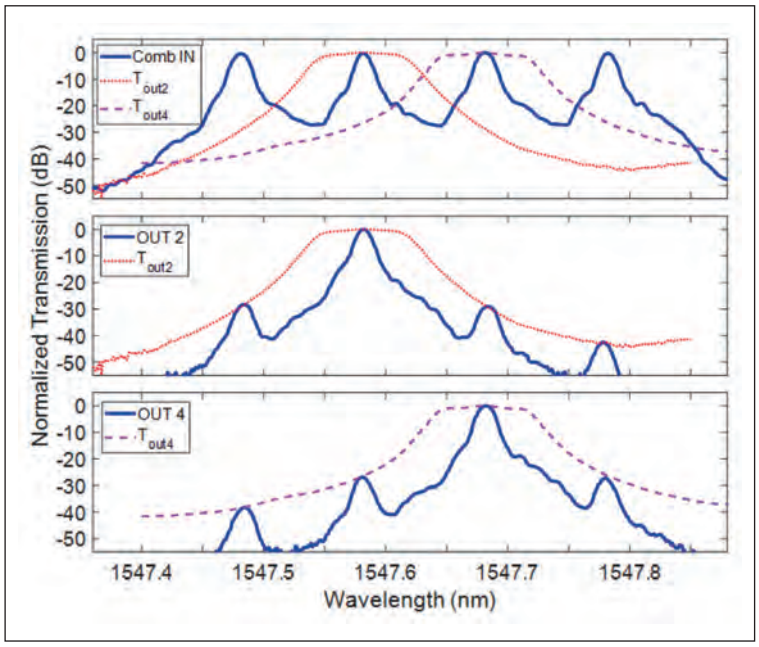


Figure 6. Spectral traces from two output ports of the demultiplexer when the DFBR filters are tuned to extract two adjacent tones from the input OFC (blue solid trace). Spectral transmissions of the corresponding DFBRs are also shown (dotted traces).

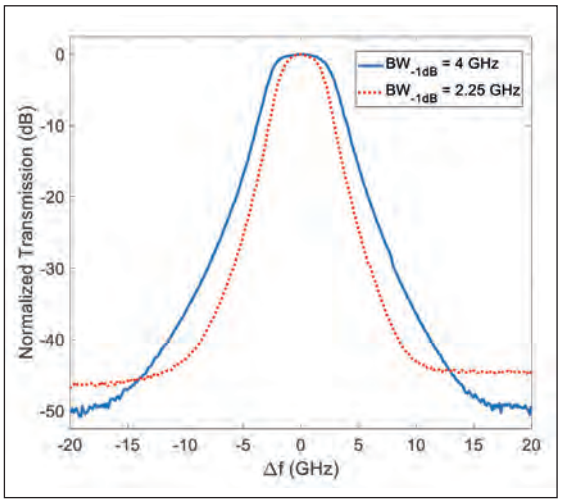


Figure 8. Different 3rd-order DFBR filter measured transfer functions also suitable for operation with 6.25 GHz comb spacing.

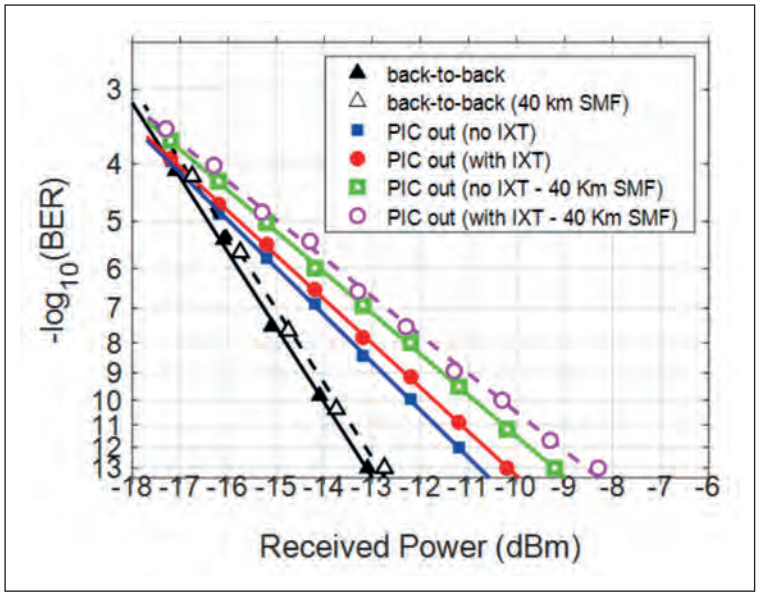


Figure 7. Results of BER measurements using the demultiplexed OFC tones for transmitting 12.5 Gbps-modulated on-off keying signals and evaluating the residual inter-channel crosstalk (IXT).

reducing propagation loss are also being considered. Although some technological challenges are still to be addressed, the DFBR-based OFC demultiplexer presented here is a key functional element that can conveniently be integrated on the same chip with silicon-photonics high-speed complex modulators and an OFC generators, enabling ultra-compact reconfigurable transmitters for flex-grid EON applications.

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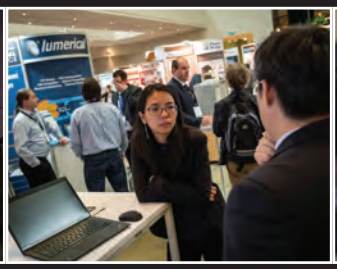



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Developing customized biosensors utilizing photonic circuit building blocks

Biomedical sensing devices that are portable and low cost hold the promise of making healthcare more widely available and affordable. Researchers at EPIC believe that without utilizing the capabilities of photonic integrated circuits (PICs), the development of these potentially life-saving devices will be delayed or even halted.

BY ANA GONZALEZ, R&D MANAGER AT EPIC

DURING THE LAST FEW YEARS, the promise of a technology enabling fast and affordable diagnostic tests using microscopic blood volumes has seemed very close. But the shutdown of one of the most famous start-ups for drop-blood test diagnosis in 2018 demonstrated that conventional microfluidic methods and analysis cannot fulfil this challenge by themselves.

Reliability, reproducibility and accuracy are key parameters in detection devices for clinical diagnosis. At present, medical device manufacturers have produced sensing systems that are big and costly. Moreover, such systems frequently require pre-treatment steps by skilled personnel before the sample can be introduced into the machine, which increases the overall time of the assay. For these reasons, new lower cost technologies must be made available to analytical clinics that simultaneously provide sensitivity and selectivity and enable direct, real-time and label-free detection in complex human samples such as blood or urine.

PICs allow the detection of a specific biomarker in a complex sample by opening a region of the waveguide cladding, which allows the interaction of the evanescent field of the light with the external environment. To achieve this, a light source, usually in the VIS/NIR wavelength range, must be coupled to the waveguide, and a detector is used to sense changes in the properties of the light (phase, frequency or intensity). In this kind of device, selectivity is provided by attaching a specific biomolecule, a bioreceptor, to the waveguide, and free spots on the surface must be blocked to avoid non-specific adsorption on the device, which will produce the same signal as the specific detection. Finally, it is necessary to flow the sample to the sensor area of the device in order to allow the interaction of the bioreceptor with the analyte. In this process, microfluidics techniques must be employed to prevent the formation of bubbles that can ruin the measurement.

By introducing a microliter sample in a miniaturized device, a PIC-based biosensor can provide a real-time diagnosis without the need of a doctor. So, what are the barriers for the introduction of this promising technology into the medical market?

Biosensors must be disposable; one sensor for each measurement. PICs offer a cheap option as these devices are fabricated at wafer level using CMOS technology. However, light must couple the PIC in the chip in a reproducible way, even if the chip is continuously replaced after use. How to couple light in these conditions is challenging considering the low dimensions of the photonic circuit. Other functionalities, such as the biofunctionalization of the sensor area and the microfluidics must be taken into account in the final optical module in which physics, engineering, chemistry and biology must be optimised

SiN-PIC chip	Imec BIOPIX 150 nm SiN, MZI refractive index sensing (670 nm wavelength)
Spring-loaded DC contacts	Metallic POGO pins attached to the SiN PIC using an actuating arm
Fiber-to-grating (μLens LIFT)	PIC with LIFT printed microlenses, which are used to create expanded beams for relaxed coupling to optical fiber
Lensed fiber array	1x8 fiber array with nanoprinted micro-lenses which are used create expanded beams for relaxed coupling to lensed Imec BIOPIX grating couplers.
Biofunctionalization: Surface activation and spotting of the bioreceptor	Chemical functionalization procedures for the attachment of the bioreceptors compatible with microfluidics processes
Injection Moulded Microfluidics & Assembly	UV curable process to assemble BIOPIX PICs within a standardised injection moulded microfluidic cartridge.

Table 1. PIXAPP biosensor PIC building blocks

for a specific application by mixing them together to achieve a direct analysis.

PIXAPP, the world's first open-access photonic integrated circuit (PIC) assembly and packaging pilot line, can meet these challenges. PIXAPP was established to enable the adoption of PIC biosensors for the medical industry based on standardized building blocks. In this approach, the customer can select between the different building blocks to build a customized optical module. PIXAPP has finalized the optimization of the different building blocks required for the development of biosensors for point-of-care applications (see Figure 1). These building blocks include the SiN-PIC chip, polymer microfluidics, spring-loaded DC contacts, lensed fibre array and a LIFT microlense system, as detailed in Table 1.

All these processes have been developed to be compatible with large-scale manufacturing. An alternative to direct bonding of optical fibers to PICs is free space coupling using microlenses. The laser transfer (LIFT) process with a polymer micro-optics replication process enable the low-cost assembly of micro-lenses on PICs - ideal for low-cost disposable applications. The target is a free-space coupling interface to on-chip grating couplers, with relaxed alignment tolerances and compatibility with biosensing applications. Regarding microfluidics, it is feasible to fabricate microfluidic parts in large quantities with higher repeatability in dimensions and smoother surfaces by injection moulding.

PIXAPP offers a single access point to these standardized building blocks and the complete ecosystem for the development of a customized biosensor. Building blocks are developed using the reference PICs that must be considered for the design of the PIC chip. They are available from various European foundries in the form of Photonic Design Kits, such as Fraunhofer HHI, III-V labs, Smart Photonics, Imec, CEA-Leti and LioniX International.

LioniX International offers a Multi Project Wafer run 850 nm for biosensing applications in a regular schedule running in the TriPleX™ technology making it compatible with low cost light sources like the VCSEL. LioniX International also offers standard PIC building blocks such as micro-ring resonator and asymmetric Mach Zehnder structures. The PICs are fully compatible with PIXAPP building blocks. To facilitate a direct operation of the biosensor chips, a fully integrated benchtop system is offered including automatic fiber array alignment, the controlled laser sources, the fluidic connections, handling and dedicated software (see Figure 3).

PIXAPP consists of a highly-interdisciplinary team of Europe's leading industrial and research organisations, able to provide services for companies

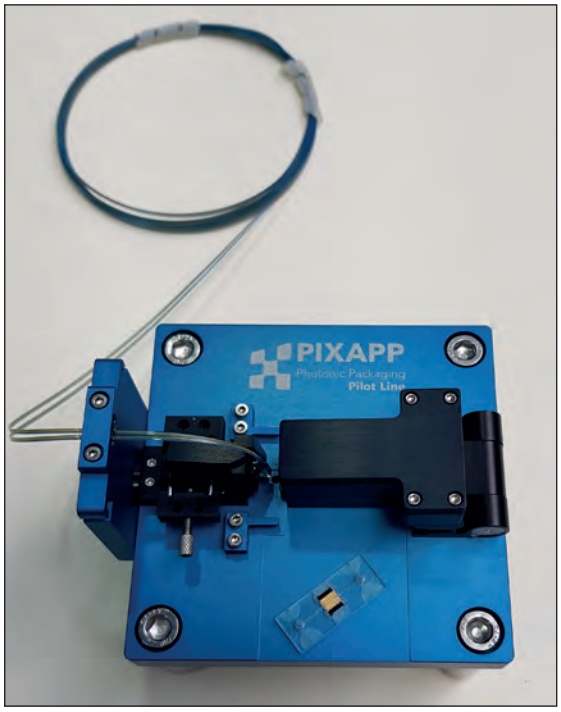

Figure 1. Final package for the PIXAPP biosensor

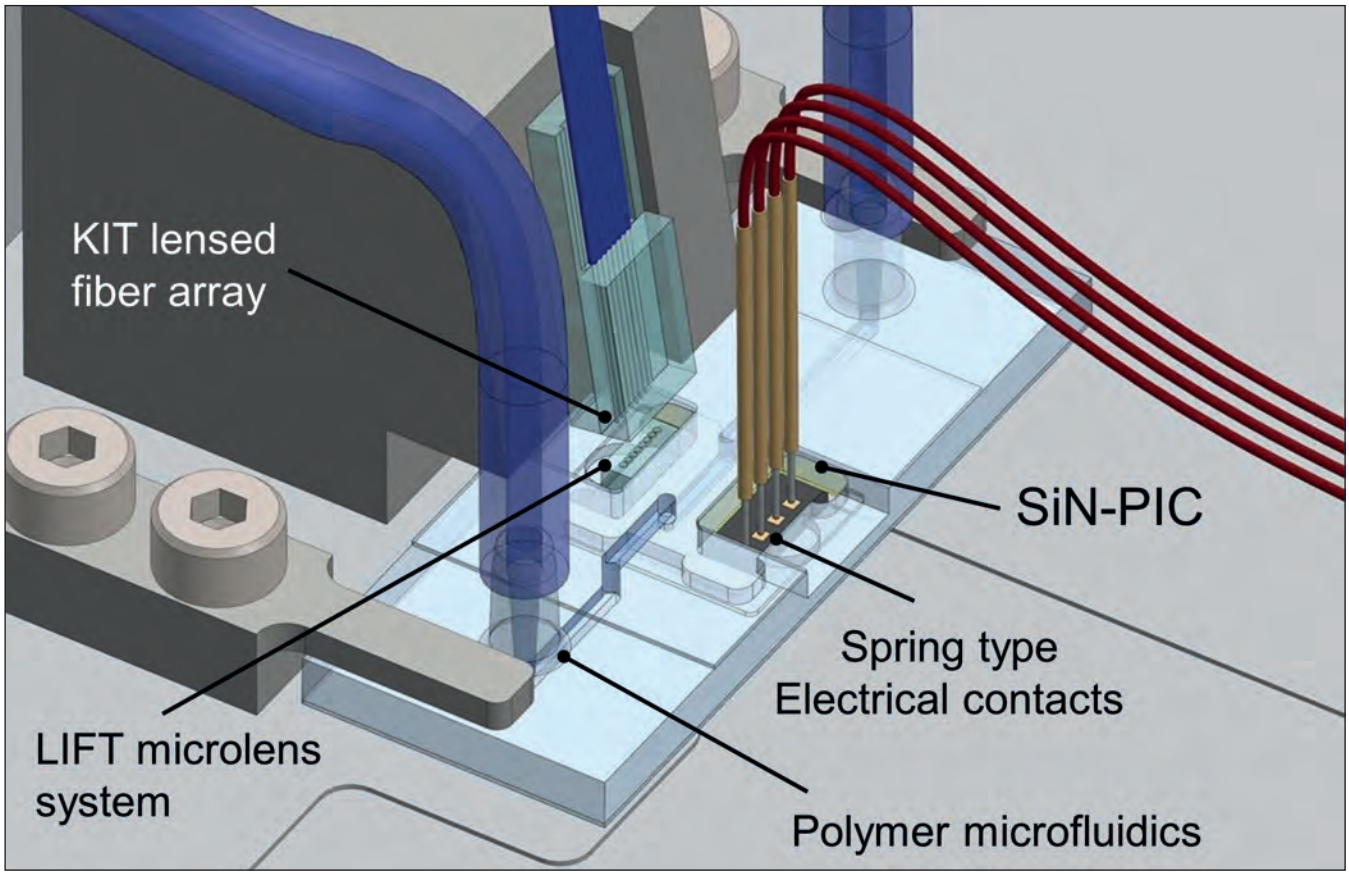

Figure 2. PIXAPP building blocks for free-space based disposable biosensors are ready for customized developments

that are looking to ramp up production of PIC based optical modules. PIXAPP is part of the pilot line initiative that includes MIRPHAB, Jeppix and PIX4Life, initiatives of the Photonics Public Private Partnership. These pilot lines complete the offer for all the wavelengths ranging from the VIS to the Mid-IR for the fabrication of chips that meet a wide range of applications and for different markets (see Figure 4). For medical, both biosensors and miniaturized Optical Coherent Tomography devices are needed. Optical communications applications include quantum random number generators, optical frequency discriminators, multi-wavelength transmitters and modulators. Other sensing applications they support include LIDAR sensors, chemical sensors, fibre sensors and interrogators.

The pilot line initiative offers a service for companies interested in developing a PIC based device, with the focus on ramping up production. It consists of various companies providing a range of services, such as the following examples: Companies providing software for design of PICs include Synopsys, Photon Design, VPI Photonics and Luceda. Companies that provide continuous support and consultancy for design, fabrication and packaging include Bright Photonics and VCL Photonics. And finally, companies involved in packaging and assembly include Eblana Photonics, KIT, the Tyndall National Institute, FiconTEC, CSEM, Cordon Electronics, Randox and the Microfluidic ChipShop.

Covering the entire supply chain for the pilot production of optical modules, the European ecosystem is developing the processes and the tools needed while positioning itself to facilitate large volume fabrication of the new generation of products that will be based on PICs.

For more information about how to access EU based pilot line services, please contact:
ana.gonzalez@epic-assoc.com

PIXAPP Photonic Packaging Pilot Line

PIXAPP is an EC funded initiative, in a public-private partnership with Photonics21, under the grant agreement H2020-ICT-2016-2017 n°731954. PIXAPP is the world's first open-access Photonic Integrated Circuit (PIC) Assembly and Packaging Pilot line, and help users exploit the breakthrough advantages of PIC technologies.

MIRPHAB CHEMICAL SENSING AND SPECTROSCOPY

MIRPHAB is an EC funded initiative in a public-private partnership with Photonics21, under the grant agreement 688265

H2020-ICT-2015. MIRPHAB is a Pilot Line for prototyping and production of Mid-IR chemical sensing devices able to operate in gas, liquid and solid media.

JePPIX (Pilot Line) is an EC funded initiative, in a public-private partnership with Photonics21, under the grant agreement 824980. H2020-ICT-2018-2020. JePPIX (Pilot Line) is the InP pilot Line for an up-scaled, low-barrier, self-sustained, PIC ecosystem.

PIX4Life is an EC funded initiative in a public-private partnership with Photonics21, under the grant agreement 688519 H2020-ICT-2015.

www.photonics21.org

EPIC is the European Photonics Industry Consortium, a membership-led not-for-profit industry association that promotes the sustainable development of organisations working in the field of photonics. Our members encompass the entire value chain from LED lighting, PV solar energy, Silicon photonics, Optical components, Lasers, Sensors, Displays, Projectors, Optic fiber, and other photonic related technologies. We foster a vibrant photonics ecosystem by maintaining a strong network and acting as a catalyst and facilitator for technological and commercial advancement. EPIC works closely with related industries, universities, and public authorities to build a more competitive photonics industrial sector, capable of both economic and technological growth in a highly competitive world-wide marketplace.

Figure 3. LioniX International starting biosensing kit

Dr. Ana González is currently R&D Manager at EPIC (European Photonics Industry Consortium). Her role is to understand the technology developed by EPIC members and to identify potential collaboration between them. She also participates in different EC initiatives such as PASSION, LAMpAS, PULSe and the Pilot Lines in Photonics in which she is involved in business development and marketing strategy. Her expertise lies in the development of optical systems and the investigation of applications such as sensing and datacom. She received her Bachelor's degree in Chemistry from the University Autonomous of Barcelona (UAB) and her PhD degree from the Catalan Institute of Nanoscience and Nanotechnology (ICN2).

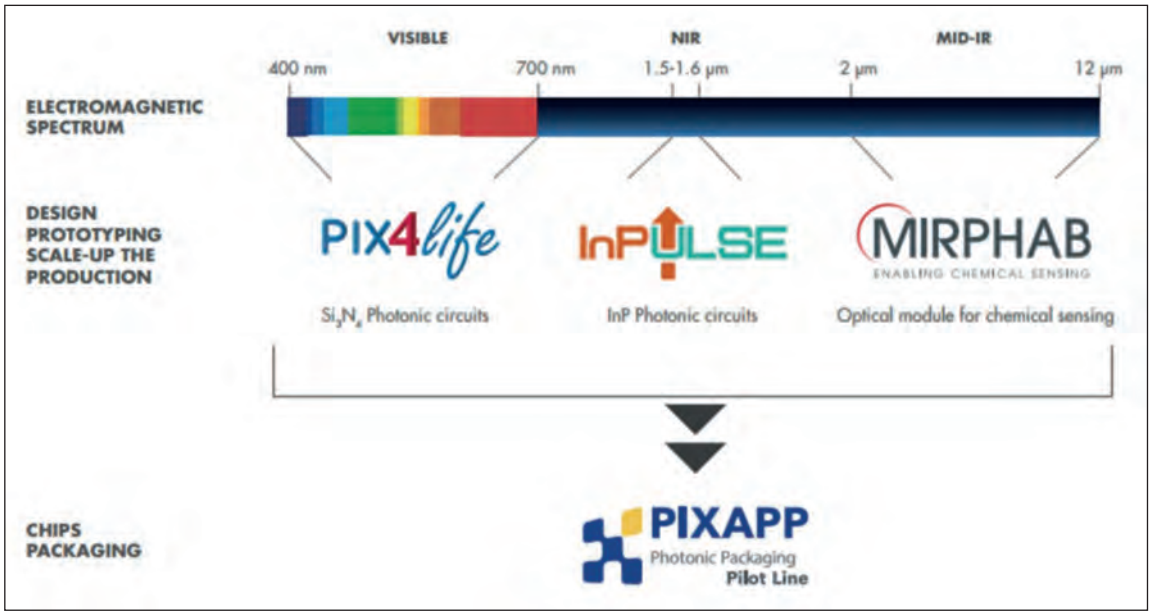

Figure 4. Pilot Line initiative, covering from VIS to Mid-IR wavelength devices

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We will explore sensors and SoCs for healthcare, AI's role, and the need for secure data processing to monitor, diagnose, and treat a wide range of medical conditions. We will also delve into steps needed to increase confidence regarding the medical efficacy of next-generation healthcare devices..

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Sensor Fusion: Processing / Networking / Connectivity / Cyber Security / AR & VR

We will explore the complementary roles of sensor fusion and data fusion as a means to integrate multiple data sources to produce more consistent, accurate, and useful information than is possible using a single data source. We will further explore the variety of key sensor fusion algorithms available to designers including those most commonly used across today's markets in consumer and commercial applications.

Harsh Environments: Space / Aviation & Aerospace / Subsurface & Extreme Heavy Industry

We will explore the challenges of manufacturing sensors that withstand harsh environmental conditions along with key issues tied to powering devices and securely collecting data from sensors deployed in harsh environments. We will also explore the expanding need for sensors and sensor fusion approaches specifically for use in harsh environments as well as the special challenges in designing for space, aviation and aerospace applications.

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TAP into the power of PIC

Photonic integrated circuits (PICs) promise dramatic size, power and efficiency advances compared to legacy bulk optical modules and CMOS electronics. The rapid roll-out of PICs has been hindered by slowly developing automated test, assembly and packaging technologies due to the complexities and variabilities common to PICs. The experts at EXFO share insights into ways that TAP needs are now being met.

BY FRANCOIS COUNY, EXFO SUBJECT MATTER EXPERT

PHOTONIC INTEGRATED CIRCUITS (PICs) are a well-known technology in the telecom world, mainly thanks to the frantic development of transceivers and passive components that are smaller, faster, cheaper and greener than their bulk-optics counterparts. PICs are also getting traction–both from a commercial and research perspective - in other sectors, too: lab-on-a-chip, LIDAR technology and quantum computing are but a few applications were PICs are of great benefit.

The move towards PICs at an accelerated rate is made possible by production techniques that allow more components to be fit onto a single, high-performance chip, cutting down on cost, size and power consumption. This is strikingly similar to what happened with electronic ICs some 40 years ago. A single PIC chip today can already contain thousands of components, each of them with multiple inputs and outputs.

Test, assembly and packaging (TAP) is, in this context, often referred to as 'the bottleneck,' i.e., the last hurdle to fully unleash the power of PICs. Whilst TAP is fully optimized for the electronic IC, it is still in its infancy when it comes to photonics—taking a large chunk of

the cost-per-chip (around 80%). Photonics has some stringent limitations due to the light itself: it is not as easy to manipulate photons as it is to 'play' with electrons! Coupling light in and out of a device using optical fiber with a 10 μm core requires expertise. This makes the whole business of testing and packaging PICs more daunting and, as a result, those final processes are left to the end-user. However, those processes now need to be addressed in a way that would allow hundreds of thousands of components to be made every year.

When it comes to testing PIC components, the need for speed comes with new requirements on more stringent specifications. Even more so when considering that data acquired during the testing phase is fed back throughout the various processes comprising PIC development: PIC manufacturers and the foundries can learn about performance tolerances of a particular fabrication process, while PIC design software can be made more accurate by calculating directly what the optical performance of a chip could be based on process design kits (PDKs) provided by the foundries. A new breed of components, not even available in bulk optics, have started to pop up over the past couple of years, making it even more difficult to measure spectral features that are, in some cases, a few picometers wide and exhibit spectral contrast well over 2000 dB/nm.

How do we unlock this photonic conundrum?

The key is to provide a flexible and scalable solution to test every parameter and function on a complex chip in a fast and reliable way. The testing capabilities needed must cover a wide range of things including a mix of optical, electronic and sometimes radio frequency (RF) signals and spans from fundamental measurements such as peak wavelength or optical power for active components (i.e., emitting light), to spectral characteristics such as insertion loss and polarization dependent loss for passive optical components (i.e., transmitting and transforming light), to fully functional characterization such as bit-error rate (BER) or constellation measurement. Consider all the various configurations of the component and you have an idea of the challenge when it comes to testing PICs effectively.

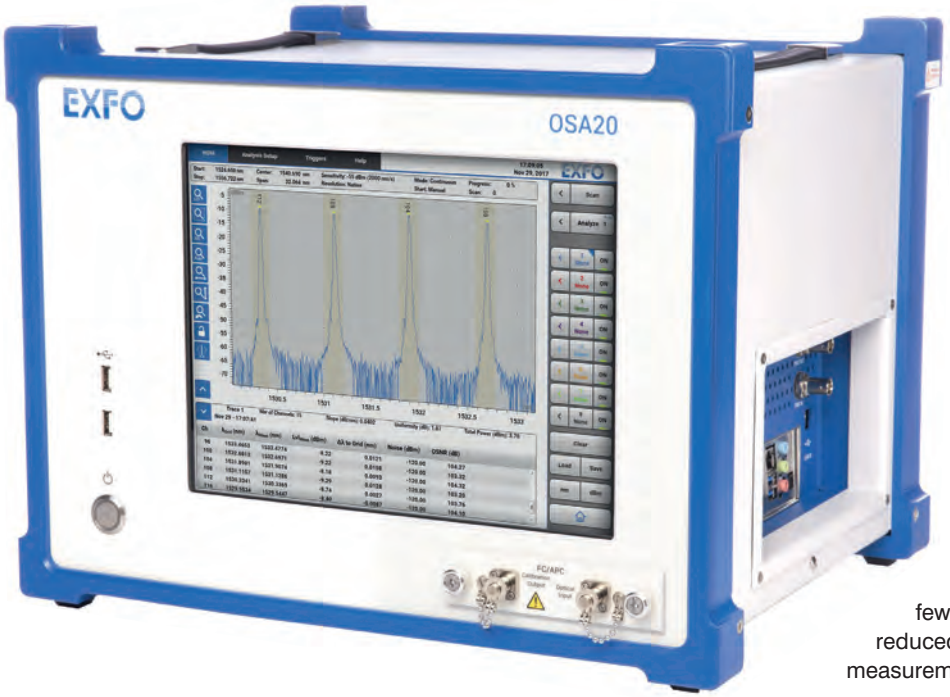
The recipe for success?

A comprehensive approach where the chip is designed to allow fast and reliable testing directly onto the wafer, i.e., before the chips are diced, is a viable solution. Wafer testing allows identification of bad chips and avoids costly packaging of defective devices. Multiple optical test points can be aligned, and light coupled from optical fibers hovering above the surface of the wafer into the chip on the wafer is possible. Using optical fiber arrays or bundles and/or photodiodes to monitor the optical output alleviates the need for repeated single fiber alignment whenever possible. In this context, fast and reliable alignment algorithms operate jointly with automated test equipment to sort out good chips from the bad ones or to provide an optimized test setup that can 'map' the characteristics of a wafer and provide feedback to foundries and create PDKs. The value of this automation is that non-specialist personnel can operate the test system with ease.

PIC-specialized wafer probe stations—such as those designed by MPI Corporation—can address the high requirements of testing 200mm or 300mm sized PIC wafers. This includes the seamless integration of the alignment equipment onto the probe station without consuming additional floor space and Sentio® software for convenient operations. Along with the development of the grating coupler, allowing the coupling of light from optical fiber to PIC wafer, those stations have come a long way to address problems specific to PIC devices. Besides the standard usage of electrical probing, the photonic test components also need to be integrated. Therefore, the probe station not only requires good vibration isolation towards the ground floor but also excellent stability of the probe plate where the photonic alignment positioners are placed.

Alignment needs can vary greatly depending on the devices to be tested. They can be as simple as a three-axis stage for single fiber applications where the fiber is aligned using a fiber holder with a predefined angle matching the grating coupler geometry for optimum coupling either in or out of the device. More sophisticated is the integration of a hexapod positioner which comes with three additional axis for rotation of yaw, roll and pitch. This functionality is mandatory for fiber array alignments.

Complete wafer PIC testing system, including the CTP10



OSA20: fast OSA with a maximum sweep speed of 2000 nm/s

Depending on the device being tested, the station could have one or two optical positioners. This is dependent on whether the test device has just one (Opto-Electric; O-E or Electro-Optic; E-O) or two (Optical-Optical; O-O) optical ports: one-sided devices may be light-emitting devices for instance, where the stimulation is done electrically (E) and the output measured optically (O) or light-detecting devices where the optical input (O) is transformed into an electrical signal (E). Setting up the alignment can be very time-consuming. Because of that, a lot of effort has been put into the automation of alignment procedures. State-of-the-art wafer probe systems can align single fiber devices under one second before taking a measurement. For fiber arrays, automatic alignment is even more critical as any rotational misalignment is automatically corrected. Fragile single fibers can easily cause damage if they are allowed to crash into each other or the wafer. Probe station software nowadays recognize the fiber positions relative to each other and to the wafer to prevent collisions.

It is clear from these developments that 'designed according to test' PIC chips are key in reducing testing time while boosting reliability. Symbiosis between design, fabrication and testing is the path to understanding and addressing any issue throughout the PIC development process. The same holistic principle can be applied during PIC assembly and the final packaging of the component to further reduce the impact of TAP on the final chip cost.

Another important challenge is photonic characterization, which requires speed and reliability at an unprecedented level in the photonics world, in a similar way to advances achieved in electrical testing over past decades. New characterization solutions based on state-of-the-art electronics and opto-mechanics enable accurate spectral measurements in under one second. Those instruments need to be able to measure large spectral contrast with an ever-increasing wavelength accuracy and over a large number of inputs and outputs. Although optical spectrum analyzers (OSA), such as EXFO's OSA20, provide high-resolution spectra in less than 300 ms for both active (i.e., light-emitting) and passive (i.e., light passes through) components, they are better suited for the former. For the latter, a laser swept technique provides optimal results. Using the CTP10 component testing platform from EXFO, picometer resolution spectral response of tens of output can be simultaneously obtained in a few seconds. Data post-processing time is also reduced thanks to onboard spectra analysis and measurement automation.

By integrating the CTP10 into the MPI probe station environment, it is possible to operate all required functions from just one single platform. Fiber-grating coupler alignment can be performed where the optical coupling signal is converted into a voltage information by the CTP10 to feed into the alignment system. The spectral measurement is then performed by CPT10 software on trigger from the probe station control software. This enables fully automated wafer testing including die-to-die stepping, fiber alignment and measurement.

Conclusion

Matching the maturity of electronic IC testing takes a strong roadmap that has to incorporate standardization testing throughout the PIC development process. This would ensure reliable methods for testing components that can be complex while allowing for the required scaling up to volume manufacturing. This, in turn, allows testing by non-specialist operators with limited training while providing accurate test data to PDKs so that some functionalities or characteristics are obtained 'by design' on a wafer: testing a few chips on the wafer could then validate the whole chip set. Finally, standardized optical testing using future-proof solutions is expected to dramatically reduce test time and cost whilst remaining flexible and evolutive.

Acknowledgement
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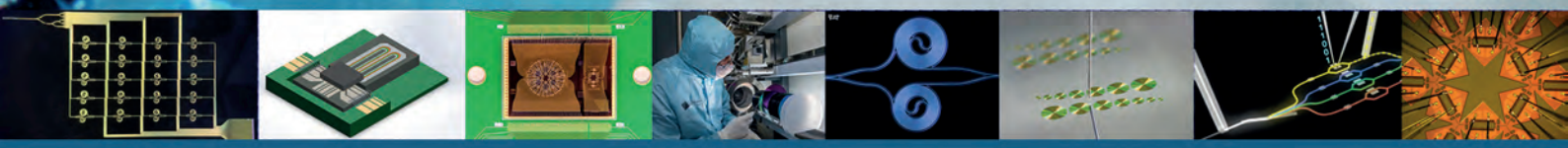

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