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CONNECTING THE PHOTONIC INTEGRATED CIRCUITS COMMUNITY

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Viewpoint

By Mark Andrews, Technical Editor

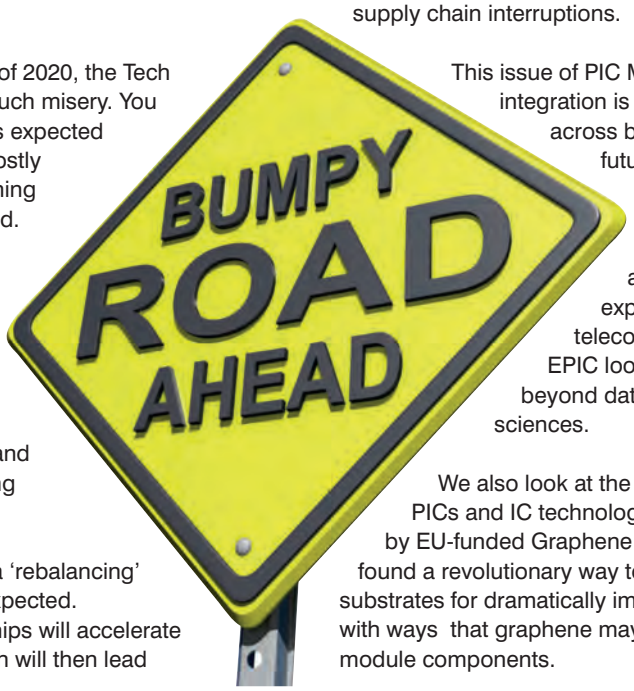
Shedding light on 2021's great expectations

AMONGST 2020's many lessons, photonic and semiconductor markets demonstrated why making even half-right forecasts may be a fool's gambit. Forecast revisions compounded in 2020 like toppling dominos. Regardless, the SEMI trade group gathered its most reliable analysts in January to use 2020 insights as New Year's guidance. The consensus? Caution: bumpy road ahead.

Despite the frequently awful news of 2020, the Tech Sector was a bright spot amidst much misery. You may recall that in 2019, forecasters expected 2020 to be a recovery year with mostly modest growth. But instead of inching ahead, semiconductor sales soared.

Photonic device and PIC revenue also grew owing mostly to continuing expansions in cloud computing driven by working and learning from home. Most analysts expect final 2020 figures to show high single-digit IC sales and about double that for manufacturing equipment.

Analysts agreed that 2021 will be a 'rebalancing' year; unevenness is once again expected. Demands for memory and logic chips will accelerate until supply meets demands, which will then lead to price erosion, temporary oversupply, and then another rebalancing round. 2021 will be surprise-rich. In what way? Could anyone have forecast in 2019 that in 2021, US President Joe Biden would ask for $37 billion to re-shore chip building? Expect similar surprises in other key global industries that struggled with demands thanks to off-shore manufacturing and supply chain interruptions.



This issue of PIC Magazine explores how photonic integration is again expected to deliver gains across broad sectors. We take a look at the future of photonic computing through an article by Ayar Labs. TAP remains a key PIC manufacturing concern, so we include a look at 2021 forecasts from the T&M experts at EXFO. While datacom/telecom PICs expect continued growth, EPIC looks deeply into PIC applications beyond data, including health and life sciences.

We also look at the role graphene will play in future PICs and IC technologies thanks to recent advances by EU-funded Graphene Flagship researchers that have found a revolutionary way to transfer graphene off growth substrates for dramatically improved manufacturability along with ways that graphene may soon benefit key photonic module components.

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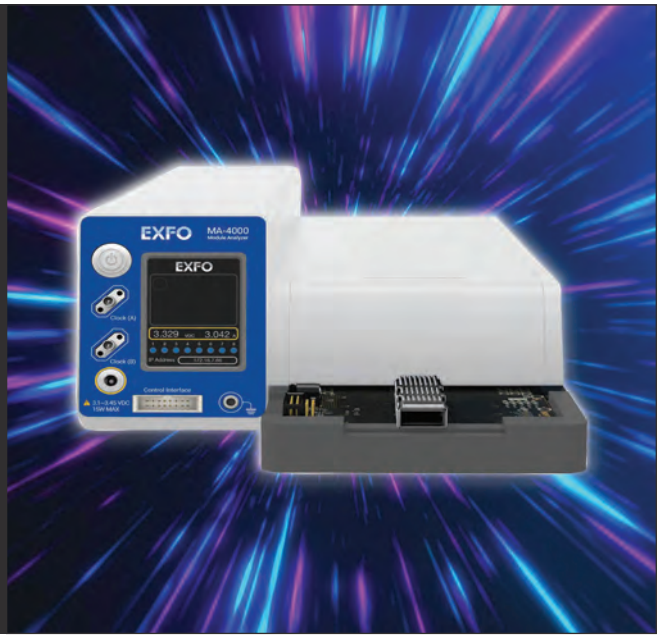
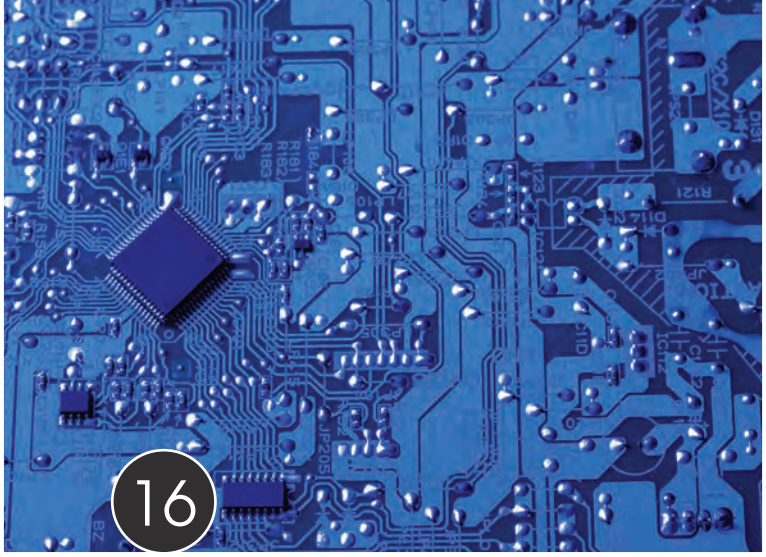
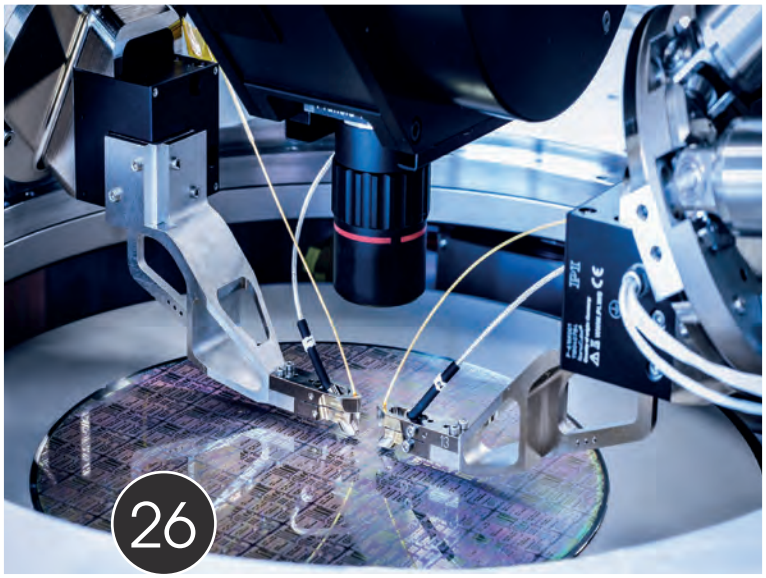
CONTENTS







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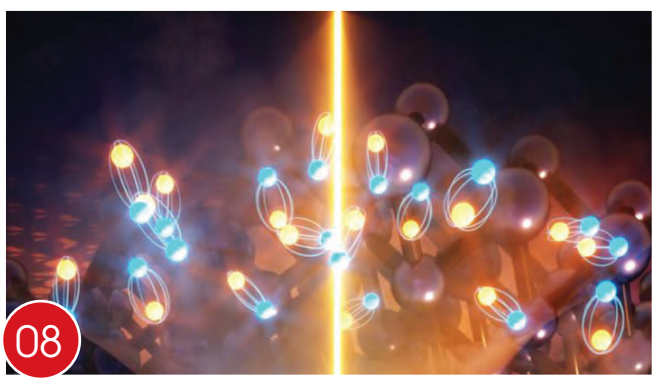

EV Group establishes state-of-the-art customer training facility

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology, and semiconductor markets, has announced that it has established the EVG Academy, a training facility for customers that provides technical training on all classes of EVG equipment as well as on EVG's CIM Framework software platform in an optimized environment. Established at EVG's headquarters in Austria, the EVG Academy comprises a new 800-square-meter facility created in tandem with the recently completed Cleanroom V expansion project. By attending in-depth, tiered training classes at the EVG Academy, customers can be qualified to perform basic repairs as well as preventative maintenance on EVG equipment without the need to contact EVG customer support -- providing customers with greater flexibility for tool maintenance. The new training facility also serves as the education and training hub for EVG's global organization.

The EVG Academy builds on EVG's existing training facilities at its headquarters, doubling the amount of training space and technical trainers. It includes eight individual training areas -- one for each major class of EVG equipment -- as well as four classrooms and a dedicated workshop area for electrical and mechanical training. Thanks to the additional floorspace, the EVG Academy has also expanded the number and type of tools available for training, including EVG's fully automated HVM platforms, such as the GEMINI® FB automated production wafer bonding system with SmartView® NT3 bond aligner and the BONDSCALE® automated production fusion bonding system.

"The EVG Academy was purpose-built with the goal to enable in-depth customer training on all EVG platforms utilizing the latest equipment and technologies, including our most advanced fully automated high-volume manufacturing (HVM) tools," stated Helmut Pfeifer, vice president of customer support. "EVG has made significant investments in updating our training infrastructure, and we are extremely proud of this world-class facility, which sets new standards for knowledge transfer in our industry. The new EVG Academy will greatly enhance the learning experience for both our customers and our international customer support teams."

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The EVG Academy is now open for training. Customers interested in learning more can contact EVG at: **academy@evgroup.com**

Researchers design next-generation photodetector

NORTHWESTERN UNIVERSITY researchers have developed a new approach to quantum device design that has produced the first gain-based long-wavelength infrared (LWIR) photodetector using band structure engineering based on a type-II superlattice material.

This new design, which demonstrated enhanced LWIR photodetection during testing, could lead to new levels of sensitivity for next-generation LWIR photodetectors and focal plane array imagers. The work could have applications in earth science and astronomy, remote sensing, night vision, optical communication, and thermal and medical imaging.

“Our design can help meet the urgent demand for ultra-sensitive photodetectors,” said Manijeh Razeghi, Walter P. Murphy Professor of Electrical and Computer Engineering, who led the study. “The architecture uses a unique type-II superlattice material that optimises LWIR photodetectors to run with low power, higher optical gain, and excellent stability.”

While recent advances in semiconductor materials and devices have led to notable progress in the development of photodetectors that can capture LWIR wavelengths, state-of-the-art LWIR detection technology still suffers from shortcomings. Many photodetectors rely on mercury cadmium telluride as a semiconductor, a material that can achieve excellent sensitivity and speed, but also produces low photocurrent gain and excess spectral noise.

Razeghi, who directs Northwestern’s Center for Quantum Devices (CQD), designed the photodetector using a type-II superlattice, a material system known for its growth uniformity and exceptional band structure engineering - the ability to control the band gap in a material, the space where no electron charge is present. This made it an optimal alternative semiconductor to mercury cadmium telluride for a LWIR system. Her team then applied the new material to a heterojunction phototransistor device structure, a detection system known for its high stability, but one previously limited to short-wave and near infrared detection.

During testing, the type-II superlattice allowed each part of the photodetector to be carefully tuned to use the phototransistor to achieve high optical gain, low noise, and high detectivity.

“The material’s demonstrated flexibility allows for meticulous quantum mechanics-based band structure

engineering for the heterostructure design, making it a versatile candidate to push the limits of infrared detection,” Razeghi said.

The research builds on CQD’s long history of work developing and understanding the physics of quantum semiconductor devices for novel applications, from military and earth science to medical systems. This novel artificial quantum structure opens the door toward next-generation high-gain photodetectors with potential for high-speed applications with ultra-sensitive detection capabilities for single photon detection.

‘Band-structure-engineered High-gain LWIR Photodetector Based on a Type-II Superlattice’ by Arash Dehzangi et al: Light: Science and Applications,14th January (2021)

Rockley closes an additional $65M

ROCKLEY PHOTONICS, an integrated optics solutions provider, has closed an additional $65m round of growth capital from both new private funds and follow-on existing investor Morningside Ventures. To date, Rockley has raised over $290m of financing to develop its silicon photonics platform from recent investors such as Credit Suisse backed SIG-I Capital and Applied Ventures, LLC, the venture capital arm of Applied Materials, Inc.

“There is tremendous need for technologies that can enable effective digital health and wellness, driven by the associated benefit provided to population health,” said Andrew Rickman, chief executive officer, Rockley Photonics.

“This funding provides the resources for Rockley to dramatically accelerate its product offerings, particularly our integrated optical sensors products. We are committed to our Tier-1 customers and our ability to help expand their product offerings and the innovative data-driven business models these products will enable.”

“We are very pleased to support Rockley at this juncture of the company’s development and contribute to the commercial success of their integrated optical chipsets and related products in multiple markets,” said Mick Sawka, investment manager at Morningside Group. “We believe that silicon photonics is at a tipping point, and the technical attributes of Rockley’s platform, coupled with the strong product roadmap and established high-volume production ecosystem, uniquely positions the company for growth in exciting verticals of interest including health care and communications. We have confidence in the deep expertise and proven track record of the Rockley team to deliver exceptional results.”

Rockley Photonics was recently named as an early constituent in the Lazard T100 Venture Growth Index (T100), a developing collection of carefully selected companies demonstrating the potential to disrupt multi-billion-dollar sectors and shaping the European venture growth ecosystem.

Switching nanolight on and off

A team of researchers led by Columbia University has developed a unique platform to program a 2D semiconductor WSe2, producing imaging capabilities beyond common limits on demand. The research appears Feb. 4 in the journal Science.

The discovery is an important step toward control of nanolight, which is light that can access the smallest length scales imaginable. The work also provides insights for the field of optical quantum information processing, which aims to solve difficult problems in computing and communications.

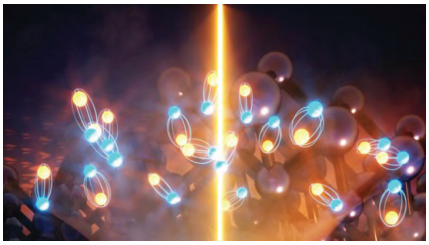
“We were able to use ultrafast nano-scale microscopy to discover a new way to control our crystals with light, turning elusive photonic properties on and off at will,” said Aaron Sternbach, postdoctoral researcher at Columbia who is lead investigator on the study. “The effects are short-lived, only lasting for trillionths of one second, yet we are now able to observe these phenomena clearly.”

Nature sets a limit on how tightly light can be focused. Even in microscopes, two different objects that are closer than this limit would appear to be one. But within a special class of layered crystalline materials--known as van de Waals crystals--these rules can, sometimes, be broken. In these special cases, light can be confined without any limit in these materials, making it possible to see even the smallest objects clearly.

In their experiments, the Columbia researchers studied the van der Waals crystal WSe2, which is of high interest for its potential integration in electronic and photonic technologies because its unique structure and strong interactions with light.

When the scientists illuminated the crystal with a pulse of light, they were able to change the crystal’s electronic structure. The new structure, created by the optical-switching event, allowed something very uncommon to occur: Super-fine details, on the nanoscale, could be transported through the crystal and imaged on its surface.

The report demonstrates a new method to control the flow of light of nanolight. Optical manipulation on the nanoscale, or nanophotonics, has become a critical area of interest as researchers seek ways to meet the increasing demand for



technologies that go well beyond what is possible with conventional photonics and electronics.

Dmitri Basov, Higgins professor of physics at Columbia University, and senior author on the paper, believes the team’s findings will spark new areas of research in quantum matter.

“Laser pulses allowed us to create a new electronic state in this prototypical semiconductor, if only for a few picoseconds,” he said. “This discovery puts us on track toward optically programmable quantum phases in new materials. “

‘Programmable hyperbolic polaritons in van der Waals semiconductor’ by A. J. Sternbach et al; Science 05 Feb 2021: Vol. 371, Issue 6529

Bay Photonics targets pitch placement of flip-chip photonics devices

PALOMAR TECHNOLOGIES has announced that Bay Photonics is working on projects that require the placement and bonding of flip-chip photonics devices that require the use of specialized equipment and are using a Palomar 3880 die bonder in the process.

Bay Photonics, a UK-based company specializing in advanced photonics assembly and packaging is involved in the prototype development stage of projects requiring fine pitch of hundreds of bonding pads, some at 60-micron level.

The Palomar 3880 die bonder recently purchased by EPIC Paignton is being utilized to ensure that the final layout of the photonic ICs (PICs) is suitable for the targeted assembly and packaging processes.

Glenn George, Managing Director of Bay Photonics commented: “I am particularly pleased that prospective customers have contacted us to help with these highly accurate PIC assembly and packaging projects. It’s exciting to see that the idea of creating a hub for Photonics development at EPIC is working, not only from Bay Photonics perspective of moving to this fantastic building, but also involving the eco-system that EPIC brings, using machinery that Palomar have commissioned and the willingness of EPIC and Palomar Technologies to help accomplish these advanced photonics technology requirements.”

Bay Photonics founded with former employees of Nortel/Bookham, Gooch & Housego, and Eltek Semiconductor have a deep understanding of the capabilities are of the various assembly methods for specific photonics applications and how to use that knowledge for building commercial prototypes that could transition to production volumes if so desired.

Josef Schmidl, Managing Director EMEA for Palomar Technologies said, “We are thrilled to work closely with Bay Photonics, particularly in this area of advanced photonics packaging. Today’s photonics applications are becoming extremely complicated and with our vision to create simple solutions for complex processes, we are dedicated to finding solutions for our customers. Our focus in placing our equipment with EPIC is to enable our customers to realize the high growth potential opportunities that are available in these exciting, rapidly evolving industry sectors.”

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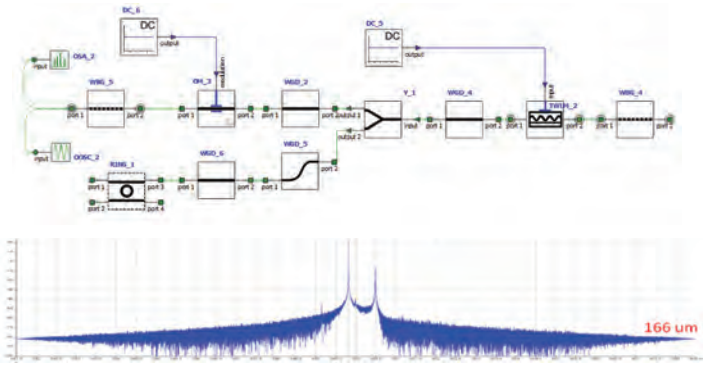

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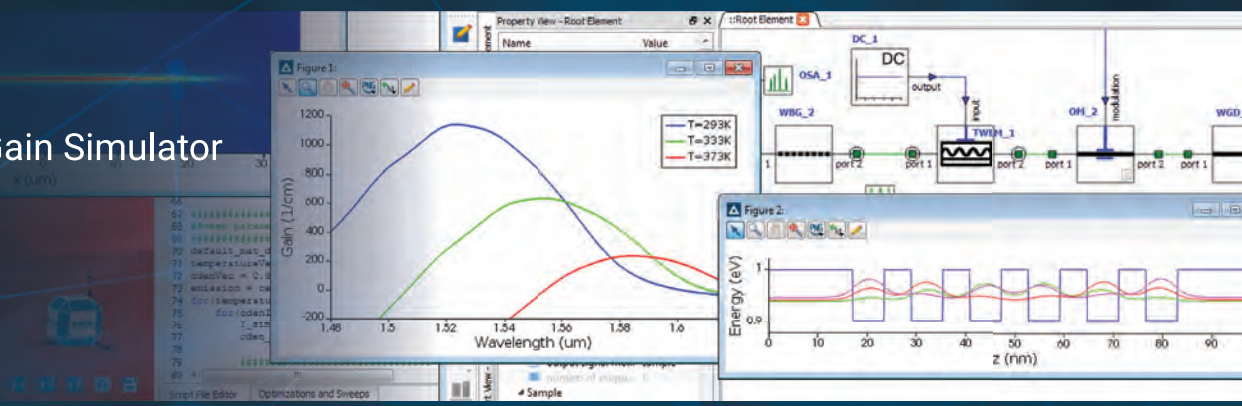

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USC team makes breakthrough in quantum photonics

RESEARCHERS at the University of Southern California have made a breakthrough towards building quantum optical circuits from quantum dot (QD) light sources.

QDs seem to be the most versatile on-demand single photon generators. But an optical circuit requires single photon sources to be arranged in a regular pattern. Photons with nearly identical wavelength from the sources must then be released in a guided direction. This allows them to be manipulated to form interactions with other photons and particles to transmit and process information.

Until now, there has been a significant barrier to the development of such circuits. For example, in current manufacturing techniques quantum dots have different sizes and shapes and assemble on the chip in random locations. The fact that the dots have different sizes and shapes mean that the photons they release do not have uniform wavelengths. This and the lack of positional order make them unsuitable for use in the development of optical circuits.

Researchers at USC have now shown that single photons can indeed be emitted in a uniform way from quantum dots arranged in a precise pattern. This method of aligning quantum dots was first developed at USC by the Anupam Madhukar and his team nearly thirty years ago.

In this recent work, the USC team has used such methods to create single-quantum dots. To create the precise layout of quantum dots for the circuits, the researchers used a method called SESRE (substrate-encoded size-reducing epitaxy) developed in the Madhukar group in the early 1990s. In the current work, the team fabricated regular arrays of nanometer-sized mesas with a defined edge orientation, shape (sidewalls) and depth on a flat semiconductor substrate, composed of GaAs. Quantum dots are then created on top of the mesas by adding appropriate atoms using the following technique.

First, incoming gallium atoms gather on the top of the nanoscale mesas attracted by surface energy forces, where they deposit GaAs. Then, the incoming flux is switched to indium (In) atoms, to in turn deposit InAs followed back by Ga atoms to form GaAs and hence create the desired individual quantum dots that end up releasing single photons.

To be useful for creating optical circuits, the space between the pyramid-shaped nano-mesas needs to be filled by material that flattens the surface. The final chip where opaque GaAs is depicted as a translucent overlayer under which the quantum dots are located.

The work, published in APL Photonics, was led by Jiefei Zhang.

“The breakthrough paves the way to the next steps required to move from lab demonstration of single photon physics to chip-scale fabrication of quantum photonic circuits,” Zhang said. “This has potential applications in quantum (secure) communication, imaging, sensing and quantum simulations and computation.”

Anupam Madhukar said that it is essential that quantum dots be ordered in a precise way so that photons released from any two or more dots can be manipulated to connect with each other on the chip. This will form the basis of building unit for quantum optical circuits. “If the source where the photons come from is randomly located, this can’t be made to happen.” Madhukar said.

“This work also sets a new world-record of ordered and scalable quantum dots in terms of the simultaneous purity of single-photon emission greater than 99.5 percent, and in terms of the uniformity of the wavelength of the emitted photons, which can be as narrow as 1.8nm, which is a factor of 20 to 40 better than typical quantum dots,” Zhang said.

Zhang concluded: “We now have an approach and a material platform to provide scalable and ordered sources generating potentially indistinguishable single-photons for quantum information applications. The approach is general and can be used for other suitable material combinations to create quantum dots emitting over a wide range of wavelengths preferred for different applications, for example fiber-based optical communication or the mid-infrared regime, suited for environmental monitoring and medical diagnostics,” Zhang said.

The research is supported by the Air Force Office of Scientific Research (AFOSR) and the US Army Research Office (ARO).

‘Planarized spatially-regular arrays of spectrally uniform single quantum dots as on-chip single photon sources for quantum optical circuits’ by Jiefei Zhang et al; APL Photonics 5, 116106 (2020)

II-VI Unveils VCSEL Arrays for next gen 3D sensing

II-VI HAS announced its double-junction VCSEL arrays, the first of its multi-junction VCSEL array platforms for next-generation world-facing 3D sensing applications. The growing adoption of 3D sensing in several markets, including in consumer electronics, automotive, and industrial, is driving the demand for depth sensors with longer and wider range, lower power consumption, smaller size, and lower cost.

II-VI´s new VCSEL arrays are based on a double-junction technology that doubles the power output per VCSEL emitter and improves the power conversion efficiency to 56 percent, compared with 46 percent in existing single-junction technology. This can be leveraged for a number of differentiating benefits, including higher output power to sense farther and wider, reduced battery power consumption, and smaller size to achieve lower cost and to enable more inconspicuous designs.

“We have developed over the years strong partnerships with our customers, closely collaborating on the development of long-term technology and product roadmaps aimed at providing breakthrough solutions and continuously elevating user experience in 3D sensing,” said Julie Eng, SVP, Optoelectronic & RF Devices Business Unit.

II-VI´s double-junction VCSEL arrays emit at 940 nm, and their steep slope efficiencies enable very short pulses of very high peak powers. The VCSEL arrays are designed for low-cost non-hermetic packaging and, like the single-junction arrays, can be reliably and cost-effectively scaled in total power by increasing the number of emitters per chip. They can also be produced in high volume on II-VI´s vertically integrated 6-inch platform. II-VI´s broad portfolio of products for 3D sensing includes diffractive optical elements (DOEs) and thin-film filters that are produced at wafer-scale for high-volume applications. DOE flat lenses and lenslet arrays collimate, focus, or transform beams from VCSEL arrays. DOE diffusers homogenize the output of VCSEL arrays and produce a uniform field of illumination. DOE splitters separate an input beam into multiple output beams.

Filters are used to improve the signal-to-noise ratio of the image sensor array. II-VI VCSEL arrays are available as chips or integrated with DOEs in surface-mount technology packages.

II-VI will show its line of lasers and optics for 3D sensing at the 2021 SPIE Photonics West Digital Forum, March 6-11, 2021.

Next-generation transceiver testing starts at design planning stage

The world's unquenchable bandwidth thirst was already well known by datacom operators and vendors as 2020 began. But the pandemic brought this home like nothing else. Suddenly, people everywhere found themselves working, educating children and living their lives online. A digitized life was no longer a sci-fi movie premise, it was reality. As overloaded networks crashed and numerous consequences of unprecedented demand abounded, the need for advanced PIC solutions was pushed to the forefront of vendor and operator planning.

PIC MAGAZINE ASKED FRANCOIS ROBITAILLE, DIRECTOR, NEMS MANUFACTURING, DESIGN, & RE SEARCH AT EXFO, to share his insights about what is happening at the design phase for transceiver testing and what trends he expects as 2021 unfolds.

Top: BA-4000: 400G/800G electrical bit-error-rate (BER tester

NETWORK EQUIPMENT MANUFACTURERS (NEMs) and service providers around the world are forging ahead with deployment of advanced technologies including 5G mobility, 400 Gbps and even 800 Gbps fiber optic networks. This rapid proliferation of next-generation networking technologies is causing a boom in demand for optical transceivers, as documented by recent market reports such as Light Counting's market research of 2020.

Light Counting forecasts strong global growth for optical transceivers, with acceleration in revenue growth of more than 20 percent projected for this year. NEMs everywhere are challenged with producing – and testing – thousands of transceivers and active optical cables (AOC) daily. Component vendors need more efficient test methods than ever before to keep pace with this burgeoning demand and to accommodate new optical component characteristics.

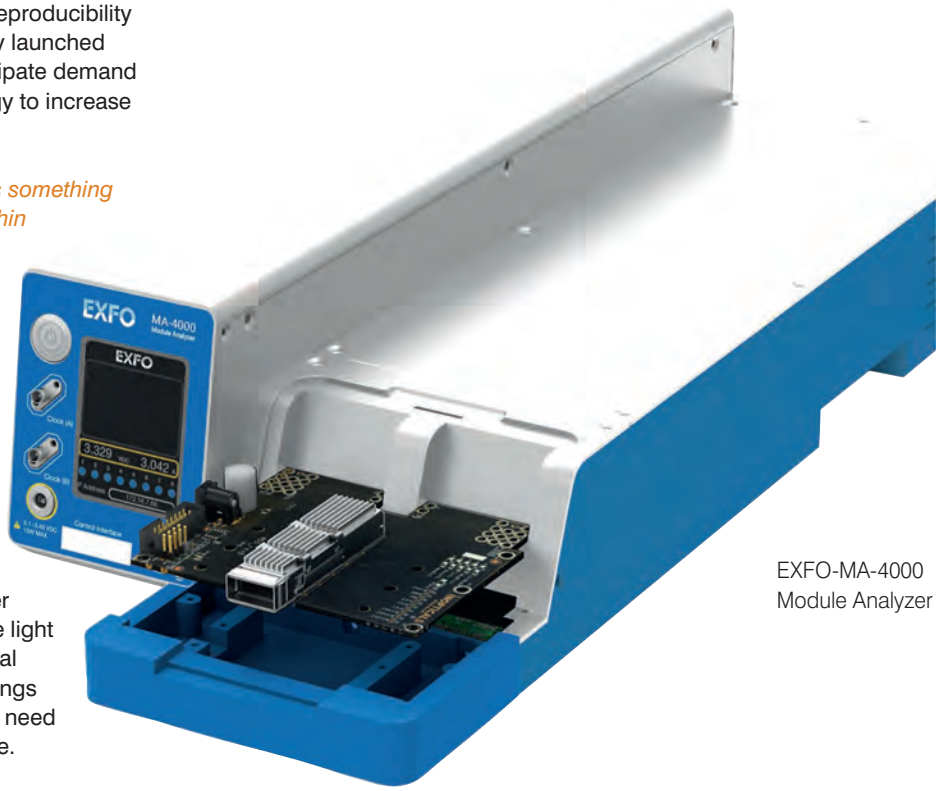
PIC: *Francois, what do you see happening with regard to advances in transceiver technology?*

FR: As you've mentioned, it's evident that the demand for transceivers is booming globally. In response, Photonic Integrated Circuits (PICs) have become the cornerstone for high-speed communications driven by 100 Gbps and 400 Gbps optical transceiver requirements for telecom and data centers. PIC technology is about to revolutionize the components industry by enabling a mix of optical and electronic functionalities on a single chip, reducing size, power

consumption, and cost while boosting reproducibility and yield. Several vendors have recently launched the first of their PIC solutions and I anticipate demand for transceivers based on PIC technology to increase exponentially in 2021 and beyond.

PIC: *Is the evolution to silicon photonics something that will become the norm or a niche within components manufacturing?*

FR: Silicon photonics is absolutely going to change the way optical systems are designed and built going forward. PICs will become 'table stakes' if NEMs want to remain competitive. With hyperscale datacenters expanding and 5G driving the proliferation of transmitters, the only way to meet that exponential demand will be to use PIC based solutions to reduce component size and lower power consumption. In fact, all sectors that use light for transmission including LiDAR, medical applications, sensing, the Internet of Things (IoT), and even quantum computing will need to adopt PIC technology to remain viable.



EXFO-MA-4000 Module Analyzer

PIC: *As manufacturers adopt silicon photonics what challenges could they encounter?*

FR: The high volume of components that will require testing coupled with the need for efficient and accurate testing at every stage of design, fabrication and packaging has inherent challenges for manufacturers. The primary goal in 2021 is to speed time-to-market for component manufacturers without compromising quality. To deliver peak performance, test solutions are needed to ensure the efficiency of PIC testing at the starting point -- which is the design planning phase.

A key trend this year will be the shift in mindset from focusing on testing the finished product, to testing at the wafer and the die level to ensure viability from the get-go. Next-generation transceiver testing starts at the design stage. By designing to test rather than testing after the fact, there are multiple benefits. Identifying issues at the wafer level can save thousands of dollars because faulty components are identified as early in the process as possible – before the packaging stage. The savings are impressive given that 70 to 80 percent of PIC-based device costs are incurred from packaging as compared to 20 to 25 percent for silicon electronics.

PIC: *Can you tell us about what needs testing during the manufacturing process and why?*

FR: NEMS need to develop their testing strategy during the design phase so that the type of testing required, access and injection points, how tests will be simulated and still more factors are taken into consideration in advance of production and testing. It's important to implement testing points and capabilities in the component design.

EA-4000: high-performance and ultra-fast electrical/optical sampling scope

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There are two types of testing to keep in mind when planning: die-level tests that perform parametric qualification of internal components; and functional testing for quality control, performed after the transceiver is produced. Of key importance during the manufacturing phase is ensuring compliance with industry specifications and standards.

As noted above, the earlier that testing can be conducted in the process, the more cost-effective and efficient the outcome. What we're seeing tested today 'post-packaging' is quite different from what we'll see in the near future with increased testing earlier at the die and wafer stage. Even some functional tests will happen earlier in the process than what occurs today. This will enable identifying faulty components as early as possible in the manufacturing process. Ultimately, component manufacturers are looking for a streamlined approach for fast, accurate validation of electrical and optical testing. Testing needs to be comprehensive, providing coherent end-to-end solutions for repeatable and accurate results wherever testing is done.

PIC: *What does that end-to-end testing solution for labs and manufacturing look like?*

FR: End-to-end transceiver qualification – and especially testing at the die-level stage – requires a complete range of high-end optical and electrical testers. To help transceiver vendors ensure compliance throughout the transceiver lifecycle, EXFO recently expanded its range of electrical and optical test solutions by acquiring InOpticals Inc., a technology leader providing ultra-high-speed test instruments for the lab and manufacturing markets.

InOptical's solutions are being integrated into EXFO's test & measurement product line to deliver comprehensive, modular test solutions. That will bring best-in-class performance across the end-to-end process for transceivers and optical components based on PICs. This is an exciting advance in delivering the capability of test solutions at the lab design stage that can potentially speed up quality component manufacturing processes.

Here are some of the new products now available from EXFO:

- BA-4000: 400G/800G electrical bit-error-rate (BER) tester
- MA-4000: the most compact solution in the industry that combines a BER tester and a module compliance board (MCB)
- EA-4000: high-performance and ultra-fast electrical/optical sampling scope.

These testers complement EXFO's expertise in optical testing to provide highly reliable and fast transceiver qualification, leveraging best-in-class testing performance from end-to-end.

PIC: *Where do you see the market headed in 2021?*

FR: This year we will certainly see wider adoption of silicon photonics and exponential availability of commercial components based on new silicon photonics technology. An opportunity in 2021 and beyond is to make better use of test data acquired during manufacturing to optimize the entire process, possibly using AI capabilities. So much information collected during testing is currently discarded or filed. I anticipate that NEMs will find ways to mine that data, which could then inform decisions for design, testing, and manufacturing; I believe this will benefit the optical industry as a whole.

François Robitaille joined EXFO in 2000. His main responsibilities include NEM market assessment, identifying potential growth areas and key product ideas as well as ensuring that products reach the market and are commercially successful.

François started his career as a Project Manager for Gentec Electro-Optics and from there moved to Bell Mobility Radio in Engineering and Sales, then to Davicom Technologies as Director of R&D. François holds a Master's Degree in Electrical Engineering from Université Laval, in Quebec City. He brings extensive expertise in both R&D and sales to EXFO.

For more information about designing, testing, and validating the next generation of transceivers, download EXFO's flyer and view the recent webinar.

Testing Silicon Photonic (SiPh) Structures at Wafer Level

If you want to optimize the functionality of your photonic design and the quality of your production processes, there is no better way than testing.

The challenge that must be overcome is the precise alignment of probe fibers with optical structures on the wafer.

Thanks to the Fast Multichannel Photonic Alignment (FMPA) systems from PI, which combine sophisticated mechanics with unique firmware, the alignment is possible in fractions of a second. An entire wafer is tested in just a few hours. Completely automatically.

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Exploring emerging applications for photonic integrated circuits

Photonic integrated circuits (PICs) have emerged as key component-level enablers of next generation datacom/telecom systems that require smaller, more efficient transceivers and switches. These same qualities are opening doors across widely varied applications ranging from vehicle autonomy to quantum computing and beyond.

BY ANA GONZALEZ, R&D MANAGER AT EPIC

MINIATURIZATION, higher performance, vibration immunity, reduced footprint and low heat generation are some of the clear benefits of adopting photonic integrated circuit (PIC) technologies for developing new photonic products. PIC technology meets the requirements for the development of new, exciting applications such as point-of-care devices, miniaturized LiDAR, quantum computing, structural monitoring and wearables for healthcare. In this article, we explore some of these emerging applications together with the companies at different levels of the PIC supply chain that can provide the technology required for the design, fabrication, packaging and scaling up volumes for PIC-based modules.

Although PICs have been used extensively in datacom and telecom, there are other application fields in which this technology is attracting increasing attention. An example is the automotive market, as a result of increasing demand for safety and advanced driver-assistance as well as autonomous driving systems, some companies such as Omnitron Sensors, Fastree 3D, Mouro Labs, Beamagine and LuxC are pushing the development of new LiDAR systems. LiDAR based on PIC technologies is potentially cheaper, lighter, more compact and more reliable—PIC based LiDARs have no moving parts.

To meet the increasing demand for automotive LiDAR systems, a growing number of companies have moved into the development of PIC-based LIDAR systems and components. Lumentum is one such company; for short-range LiDAR (10-50 m) and in-cabin monitoring, Lumentum provides high-power 940 nm VCSEL array illuminators. For long-range (200 m), they offer 1550 nm narrow-linewidth DBR diode lasers for long-range frequency-modulated continuous-wave (FMCW) coherent LiDAR. Both of these devices are designed to be time-of-flight (ToF) light sources for flash systems and are really intended to provide more power. To reach much higher power levels, longer distance, higher resolution and the performance required by automotive LiDAR, Lumentum have developed two innovative solutions: multi-junction addressable VCSEL arrays and bottom emitting devices.

MULTI-JUNCTION VCSEL ARRAYS:
By increasing the number of junctions, the number of photons emitted can be also increased with the same type of overall wall plug efficiency. This allows the low currents, typically used in two or three junctions, to produce higher levels of power and faster applications.

BOTTOM EMITTING DEVICES:
These allow fabrication of devices with no external optics and the ability to modify the beam profile. Basically, an external lens is put on the back of the device and the chip is flipped upside down and then mounted top down onto the sub-mount. This allows integration of multi-junction adjustable arrays and optics to create new and novel gallium arsenide patterns, which will be required for the next generation of detector devices (see Figure 1).

There are other companies providing VSCEL arrays for LIDAR, such as Array photonics, Bandwidth10 and Astrum. Different types of lasers can be also

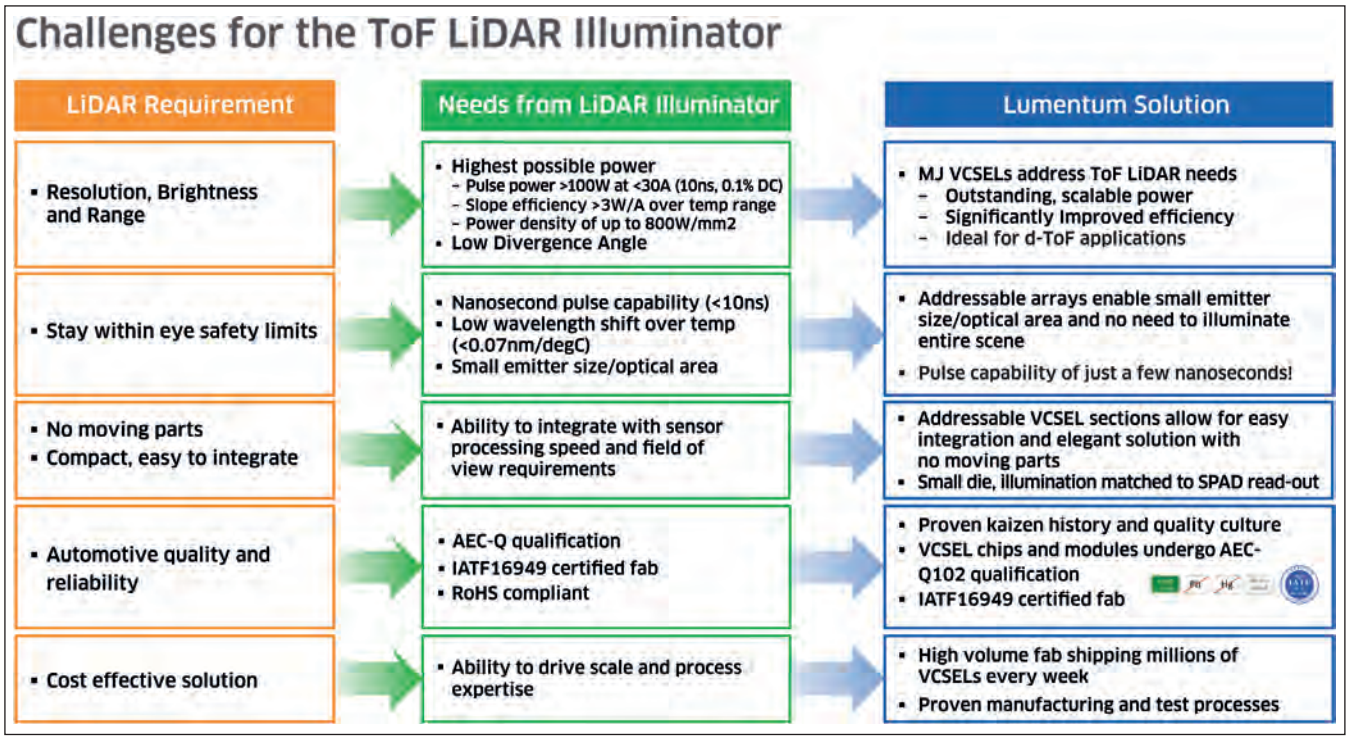


Figure 1. Bottom Emitting Integrated Optics Configurations (courtesy by Lumentum)

employed for LIDAR, such as the ones provided by companies including Lumibird, Bright solutions, Eblana photonics, BKtel and RIO.

Another company working on a cost-effective solution for improving vehicle perception is SCANTINEL PHOTONICS, a spin off from Carl Zeiss AG, that uses coherent Frequency-Modulated Continuous Wave (FMCW) ranging to achieve longer distance by using a 1550 nm integrated swept source with a narrow bandwidth and high linearity (see Figure 2). This enables the system to generate reliable, high range three-dimensional images of the environment required for autonomous navigation.

Coherent ranging allows the photonic integration of the lasers, detectors, and a large part of the optical components on a silicon wafer platform, which eliminates error-prone assembly and calibration steps. The core concept of the system is its scalability to high pixel rates through efficient multiplexing, which is achieved by using a high parallelization of different FMCW channels.

Using PICs to create an optical enhanced array (OEA), enables high integration of the system, low power, and solid-state scanning up to a range of 300 meters as well as the option to scale up to high volumes at very competitive price points.
SCANTINEL collaborates with partners such as imec, a leading European research centre in the field of silicon photonics with whom they are working on solid state beam steering, and PHIX, a packaging company for large-volume photonics manufacturing.

Fabricating proof of concept chips or taking proven designs to initial prototype stages is a costly process, so a number of European foundries offer mupliproject wafer (MPF) services including:

- **Silicon Nitride (SiN):** CNM, imec, LioniX and LIGENTEC
- **Indium Phosphide (InP):** Smart Photonics, Fraunhofer HHI, 3-5 labs
- **Silicon Photonics (SiP):** VTT, imec, ihp and Cornerstone

Multi project wafer foundries fabricate different chips in the same wafer to reduce costs in the prototyping phase. Another option is the JePPIX Pilot Line that was launched in 2019. JePPIX aims to provide companies with direct access to state-of-the-art manufacturing InP chips from proof of concept to industrial prototyping and pre-production. Applications include fibre-optic communication, biomedical devices, next generation mobile and portable devices, astrobiology, and quantum computing. Foundries also offer Process Design Kits (PDKs) for circuit simulation and mask design to aid in the process of turning concepts into chips. The PDKs can be implemented in different software packages offered through Synopsys, VPI Photonics, Luceda, Lumerical, Nazca and PhotonDesign.

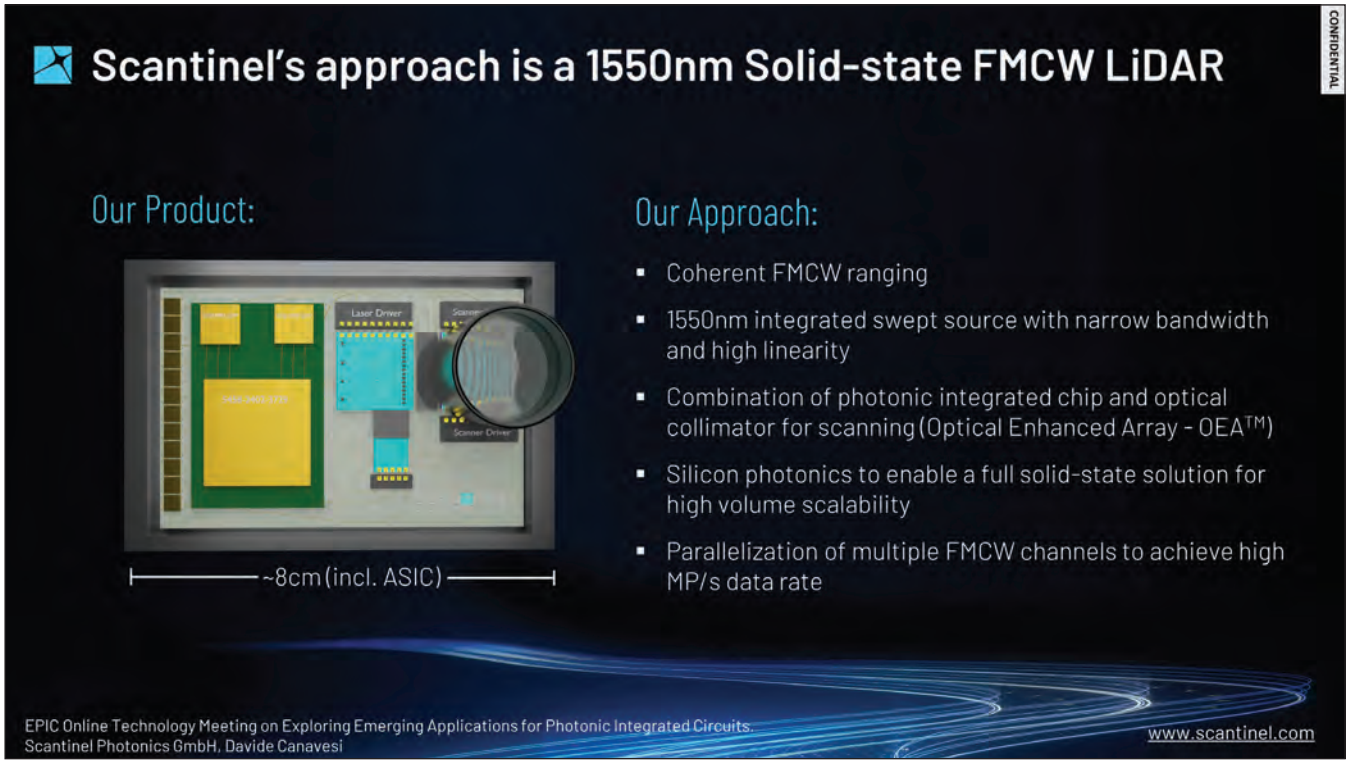


Figure 2. Scantinel's 1550 nm FMCW LiDAR approach (courtesy by SCANTINEL PHOTONICS)

Luceda Photonics, based in Belgium, provides software and services for an integrated approach, enabling photonics IC engineers to enjoy the same first-time-right design experience as electronic IC designers. To this end, they have their IPKISS integrated photonics design platform based on Python. This platform is a scripting environment that covers the complete photonic IC design flow up to measurement feedback for true component characterization and validation. The components rely on a single, centrally defined model for a smooth transition between the different design stages such as layout, physical and circuit simulation. This makes the design flow robust, reduces design errors and saves considerable design time.

The IPKISS platform is modular and can be extended to integrate with EDA design flows via their IPKISS.eda module. This module can be plugged into the IPKISS platform to allow parametric cells to be exported to EDA tools, thereby enabling PIC designers to enjoy the benefits of a professional EDA environment and the ability to exercise good control over the details of complex components. It affords automation and control across all levels from the component to the circuits - a feature particularly attractive for both LiDAR and quantum computing applications.

Another company working in the field of simulation software is VPI Photonics. They have participated in a number of industry-leading research projects, the most recent of which is PlasmoniAC, an EU-funded project that aims to develop a radically new circuit-technology for neuromorphic computing based on plasmons. The idea is to create high-speed neuromorphic chips that are low-cost, energy-efficient, and compact with the aim of strengthening the competitiveness of the European photonics industry to play a greater role in the global neuromorphic and deep learning market. The project basically leverages the energy and size efficiency of plasmonic circuits and applies them to neuromorphic computing architecture. VPI's contribution is to develop an add-on model library for plasmonic devices for use in conjunction with their photonic integrated circuit models to allow their customers to build and simulate neuromorphic circuits as well as evaluate their performance.

PICs are envisioned as a key technology in the near-term deployment of metropolitan quantum-key-distribution-based secure systems that leverage the fact that entangled photons can be individually generated, modulated and routed on the PIC. Companies such as QuSide Technologies and Quix develop PIC based devices for random number generation.

Another application is the development of quantum computing being pursued by companies such as XANADU, a quantum photonics computer company with a mission to build quantum computers that are useful and available to people everywhere. They currently have three cloud machines available, which are based on silicon nitride PIC systems that generate gaussian process sampling for near-

term applications. The advantage of silicon nitride is that the machines can operate primarily at room temperature and the system easily integrates into existing telecommunication infrastructure.

Personal health and agri-food applications are under development at OnePlanet Research Center, which was established in 2019 to initiate fundamental and applied research into applications to improve health and access to healthy and sustainable food. The centre focus on three main areas: sensing, including non–invasive, electrochemical, imaging techniques; digitizing and data analysis; and various applications as diverse as wearables, nitrogen sensor boxes and AI models. As shown in Figure 3, the photonics sensor technology is based on silicon nitride and is being developed by imec.

Health applications include devices to detect early markers in urine samples that could point to potential health issues and to provide insights into changes that occur in a certain timeframe; wearables for measuring mental well-being and stress; and digital techniques to measure how individuals absorb food and to detect problems in the gastrointestinal system.

Agri-food applications aim to use sensor and digital technology to make food production and processing more sustainable. Specifically, to enable farmers to monitor every tree, plant and animal individually so they can respond quickly and precisely at the right place and time. The aim is save time and use resources more effectively and efficiently while protecting the environment as much as possible. In this way, it may be possible to grow crops in places where the soil is less fertile, which has in turn led to food shortages.

Related to healthcare and environmental applications, the MIRPHAB Pilot Line was launched to scale up products based on miniaturized Mid-IR spectroscopic sensors, including PICs acting as the spectrometer by using arrayed waveguide gratings (AWG). Mid-IR light in the 3- 12 μm wavelength band interacts strongly with molecular vibrations that present unique adsorption spectrums that give superior detection capabilities and unambiguous detection of chemicals in gas and liquids, enabling high sensitivity and real-time detection, qualities that present interesting applications for the development of wearables, breath analysers, point-of-care applications and detection of chemicals for industry.

Optics11 offers high-end optical sensing systems for both industrial and life science applications. Their main focus is on developing high-end tuneable laser-based fiber Bragg grating (FBG) integrators for optical sensing systems that incorporate a high-end optical acoustic emission system called Optima, which can sample up to megahertz rates. The FBG integrators have high accuracy and high precision. The Optics11 FAZ 14 series integrators can sample up to kilohertz rates. The technology also features a broad portfolio of FP and FBG based to sensors to measure strain, acceleration, temperature, and pressure. The company has experience in a wide range of applications and is currently engaged in research for the next generation of PIC based interrogators for low-

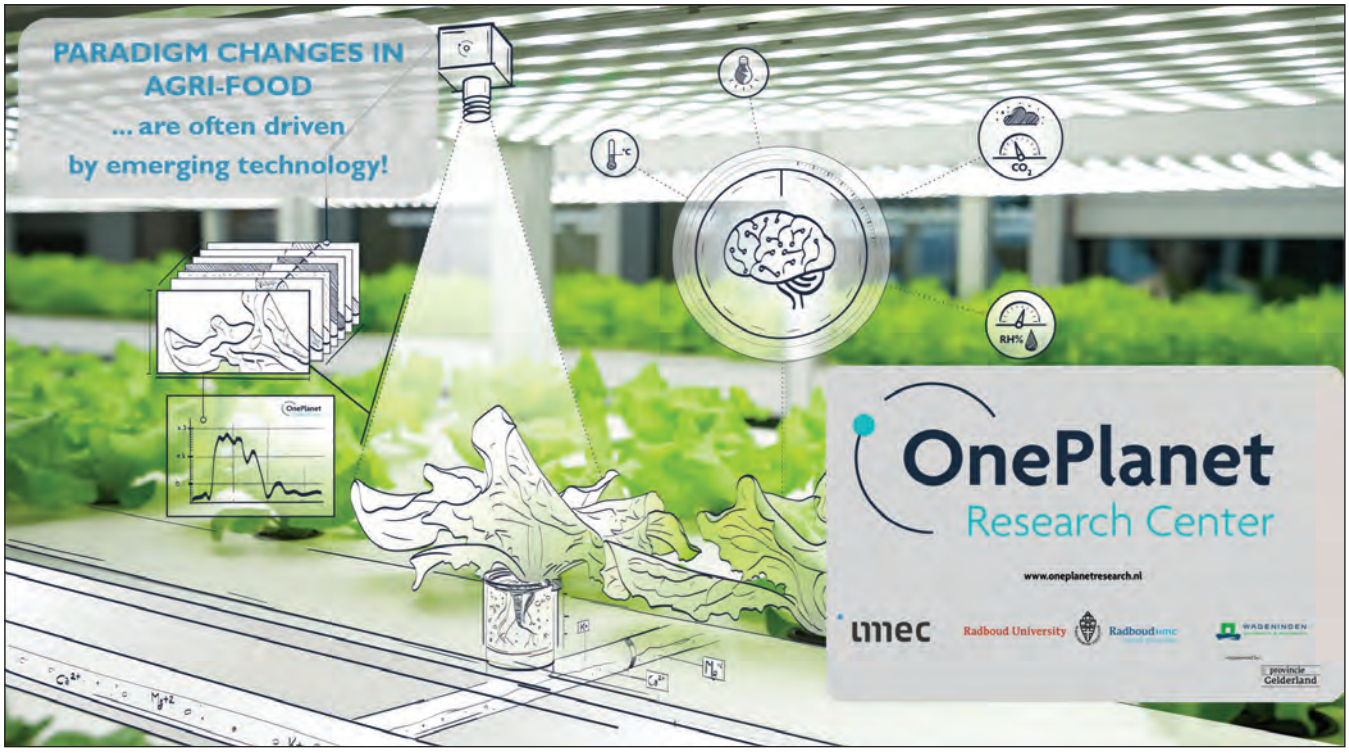
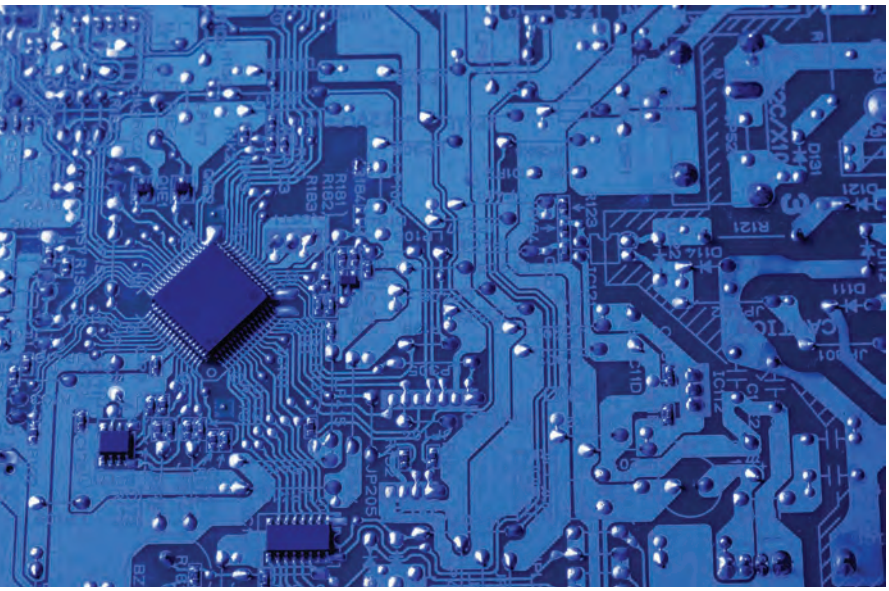


Figure3. OnePlanet Research Center focus on silicon nitride sensor technology (courtesy of OnePlanet)



cost, high volume applications, while maintaining high performance.

Optics11's technology is used in real-time structural health monitoring applications, for example, in bridges, caves and wind turbines to detect displacements and the need for repairs. Other industrial applications include acoustic emission for detecting partial discharge in high voltage applications and also road traffic monitoring, which involves installing fibre FBG arrays under the road surface to monitor the flow, speed and wight of traffic.

For life science, Optics11 technology is used in organ-on-a-chip and cell/tissue indentation applications that are able to simultaneously measure the mechanical properties of up to 92 samples of organ and tissue cells. This requires a platform and high-speed measurement system that can simultaneously integrate all the samples.

The MedPhab Pilot Line was created to ramp up the manufacture of devices for a particular application field, namely, medical diagnostics including fibre optics, microfluidics, surface functionalisation, instrumentation, opto-electronic integration, miniaturisation for micromodules and wearables applications. The MedPhab Pilot Line utilizes PIC technologies and other non-PIC advanced resources.

After designing and fabricating PICs, the next challenges include test, assembly and packaging. The PIXAPP Pilot Line provides a range of standardised photonic packaging technologies that can be scaled to high volumes; PIXAPP also provides training in optical, electrical, and mechanical packaging technologies. PIXAPP offers a menu of packaging processes in the form of building blocks to allow standardised manufacturing processes to be used across the entire supply chain for the production of PICs in the major photonic platforms (InP, SOI, SIN), with standard designs for electro-optical I/O ports and packaging assembly steps.

Companies and organizations such as Bay Photonics, PHIX, AEMtec, AMETEK, Chip Integration Technology Center (CITC), Catapult, Cordon Electronics, Focuz, Fraunhofer IZM, Hisense Broadband, Icon Photonics, INPHOTEC Foundation, PakPIC, Photonics42, Technobis group and VTT offer services for packaging PIC modules. Micro-optics is also a fundamental aspect when talking about packaging of PICs, PHABULOUS is a Pilot Line created to help mature manufacturing processes and increase manufacturing readiness of free-form micro-optical structures and functionalities.

PIC testing is now a hot topic in the photonic scene. There are a number of challenges in PIC testing, particularly in relation to speed, dynamic range, and accuracy, and also from the instrument perspective, the requirement for integration, flexibility, and a degree of automation. EXFO, a Quebec based company, has been involved in test measurement since 1985, and in the past five years, they have developed a line of products particularly for PICs.

The testing of PIC-based passive components, i.e. those that guide light, is challenging due to the high port count of some components like arrayed waveguide grating (AWG) or the large number of components to test on a single die. For passive components, EXFO provide a CTP10 component test platform, which is a multiport detection system that works in conjunction with their T100S-HP swept tuneable laser to measure optical insertion loss, return loss and polarization-dependent loss across the telecom spectral range, facilitating integration as part of an automated PIC testing setup, increasing PIC testing throughput while reducing test time.

Conclusion

Over the next few years, the increase in demand for PIC based systems for LiDAR, personal health, agri-food, life science, structural monitoring, and industrial applications present clear opportunities for PIC-based technology reaching beyond datacom/telecom. In this article, we have looked at some of the ground-breaking PIC technologies being developed for these application fields and the corresponding supply chain providing support services for PIC design and testing.

In addition to these important contributions, EU pilot lines are making great strides in helping European SMEs develop the tools and processes to scale up the manufacture of innovative PIC-based components by providing services for chip fabrication and standardised photonic packaging technologies.

EPIC is the European Photonics Industry Consortium, an association that promotes the sustainable development of organizations working in the field of photonics. EPIC members encompass the entire

value chain from LED lighting, PV solar energy, Silicon photonics, Optical components, Lasers, Sensors, Displays, Projectors, Optic fiber, and other photonic related technologies. EPIC fosters a vibrant photonics ecosystem by maintaining a strong network and acting as a catalyst and facilitator for technological and commercial advancement. EPIC works closely with related industries, universities, and public authorities to build a more competitive photonics industrial sector, capable of both economic and technological growth in a highly competitive world-wide marketplace. www.epic-assoc.com

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About the author:

Dr. Ana González is currently R&D Manager at EPIC (European Photonics Industry Consortium). Her role is to understand the technology developed by EPIC members and to identify potential collaboration between them. She also participates in different EC initiatives such the Pilot Lines in Photonics in which she is involved in business development and marketing strategy. Her expertise lies in the development of optical systems and the investigation of applications such as Sensing and Datacom. She received her bachelor's degree in Chemistry from the University Autonomous of Barcelona (UAB) and her PhD degree from the Catalan Institute of Nanoscience and Nanotechnology (ICN2).

EPIC PARTNERS

PIXAPP Photonic Packaging Pilot Line

PIXAPP is the world's first open-access Photonic Integrated Circuit (PIC) Assembly and Packaging Pilot Line. Developing multiple standardized packaging and packaging building blocks, the PIXAPP pilot line aims to help leading companies and SMEs to exploit PIC technologies for improving their current products and/or to transfer their PIC-related research(es) into PIC-based products. PIXAPP has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731954. (www.pixapp.eu)

JePPIX Pilot Line

JePPIX Pilot Line democratizes access to industrial prototyping and pre-production of high-performance InP photonic integrated circuits (PIC). The JePPIX Pilot Line is enabled by the InPulse project. InPulse has the ambition to transform business practices from vertical integration – where design, fabrication and product development are all in-house and inaccessible to new entrants, to horizontal where fabless and lab less businesses share the same manufacturing infrastructure. InPulse provides a low entry barrier access to low and medium production volumes of InP PICs. InPulse has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 824980. (www.inpulse.jeppix.eu)

MedPhab Photonic Medical Devices

MedPhab is Europe's first Pilot Line dedicated to manufacturing, testing, validation, and up-scaling of new photonics technologies for medical applications ranging from diagnostics to surgical tools and therapeutics. The purpose of MedPhab pilot production line is to accelerate the commercialisation of diagnostic devices and instruments for treatment based on photonics, and to reduce the R&D costs. The chosen areas are devices intended for hospital use (assist doctors), home care devices (monitoring patient) and equipment for chemical diagnostics (based on use of serum, saliva, or urine sample). MedPhab will also provide seamless transition from pilot line production to up-scaled production without a need for changing service providers. Use-case companies have been selected for the validation of the pilot line services covering both in-vivo and in-vitro domains. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 871345. (https://medphab.eu/)

MIRPHAB ENABLING CHEMICAL SENSING

MIRPHAB is a Pilot Line for prototyping and production of Mid-IR chemical sensing devices able to operate in both gas and liquid mediums. MIRPHAB provides a platform to ensure the bridging between technology and component development and the commercial availability of such component avoiding the risks associated with the introduction of new disruptive technologies. The aim of MIRPHAB is to become a commercially available prototyping line in 2020. The focus of the Pilot Line is to deploy your Mid-IR prototype swiftly in the market at a minimum of capital investment. MIRPHAB has received funding from the European Union's Horizon 2020 research and innovation programme under grant a greement No 688265. (https://mirphab.eu/)

Phabulous

PHABULOuS is to strengthen Europe's leading position as a technology and machine provider for the production of micro-optics based on a value selling model that retains the high-cost and high-value technology portfolio in Europe. It aims to develop easily accessible, world class manufacturing facilities to enable European companies to implement micro-optical components in their products and compete advantageously with their global competitors. The PHABULOuS Pilot Line has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 871710. (https://phabulous.eu/)

Integrated photonics benefit from emerging graphene flagship programmes

The-EU funded Graphene Flagship is an ambitious programme begun in 2013 to assist academic and industrial researchers in transitioning the many promising aspects of 2D graphene technologies into materials and processes for photonic and electronic applications. The consortium of 170 research groups in 21 countries recently announced the development of a €20 million experimental pilot lines (EPL) programme and results that appear foundational to future graphene-enabled photonics.

BY MARK ANDREWS, TECHNICAL EDITOR, PIC MAGAZINE

THE TANTALIZING PROMISES of utilizing 2D graphene to manufacture photonic and electronic devices has fueled billion-euro investments across industry and academia. But bringing graphene into practical, widespread use across industries has proved elusive. That old reality appears on the verge of changing as the EU-funded Graphene Flagship project is producing results, peeling back the curtain on what may be a new age of 2D materials across multiple sectors.

Why all the interest in graphene? For starters, graphene is considered by most as the world's thinnest material at only one atom thick. In its purest form, graphene has many properties of interest to photonic and electronic product developers. Even though 2D graphene is a million times thinner than a human hair, it is incredibly strong, besting steel and diamond gram for gram. Graphene can bring stiffness and durability in myriad applications without the bulk, weight or cost of legacy materials.

Yet even though it is strong, graphene is also flexible, which has fueled dreams of using graphene in wearable devices and foldable electronics. Since it is transparent, graphene could support bendable smartphone screens and has wide ranging photonic building block applications including modulators, sensors, and photodetectors. Graphene-enabled photonic devices can absorb light from ultraviolet to far-infrared, with promising applications in ultra-broadband communications. Graphene devices offer ultra-high carrier mobility that can enable data transmission exceeding 100 Gbps.

Enabling the full potential of graphene for European developers and manufacturers is a central goal of the EU's Graphene Flagship. Recently, the programme provided €20 million to fund experimental pilot lines (EPLs) that will enable a low volume means to test experimental devices on the road to full production. The EPL concept is designed to bridge the gap between lab-scale manufacturing and large volume production.

On 10 February Graphene Flagship researchers announced a new method to integrate graphene and other 2D materials into semiconductor manufacturing lines, an early milestone achievement of the EPL programme. That announcement was followed a day later by news that programme researchers had devised a wafer-scale production technique that could be foundational to new generations of graphene-based photonics.

As programme researchers noted in their announcement, two-dimensional materials have a huge potential for enabling devices with much smaller form factors and extended functionalities with respect to what can be achieved with today's silicon technologies. But to exploit this potential, manufacturers must be able to integrate 2D

materials into semiconductor manufacturing lines – a notoriously difficult step. Researchers in Sweden and Germany now report a new method to make this work.

Details of the new technique were published in 'Nature Communications,' which documented efforts from Graphene Flagship partners including RWTH Aachen University, the Universität der Bundeswehr München and AMO GmbH, in Germany, as well as efforts by the KTH Royal Institute of Technology, in Sweden, in collaboration with Protemics GmbH.

"There's always this critical step of transferring (graphene) from a special growth substrate to the final substrate on which you build sensors or components," remarked Arne Quellmalz, a researcher at KTH Royal Institute of Technology and lead author of the paper. "You might want to combine a graphene photodetector for optical on-chip communication with silicon read-out electronics, but the growth temperatures of those materials is too high, so you cannot do this directly on the device substrate."

So far, most documented methods for transferring 2D materials from their growth media to the target substrate are either non compatible with high-volume manufacturing or lead to a significant degradation of the 2D material along with its electronic properties. According to the team, the beauty of the solution proposed by Quellmalz and co-workers is that it lies in the existing toolkits of semiconductor manufacturing: to use a standard dielectric material called bisbenzocyclobutene (BCB), along with conventional wafer bonding equipment.

"We basically glue the two wafers together with a resin made of BCB," explained Quellmalz. "We heat the resin until it becomes viscous, like honey, and press the 2D material against it."

At room temperature, the resin becomes solid and forms a stable connection between the 2D material and the wafer, Quellmalz said. "To stack materials, we repeat the steps of heating and pressing. The resin becomes viscous again and behaves like a cushion, or a 'waterbed,' which supports the layer stack and adapts to the surface of the new 2D material."

Researchers demonstrated the transfer of graphene and molybdenum disulfide (MoS^2), as a representative for transition metal dichalcogenides, and stacked graphene with hexagonal boron nitride (hBN) and MoS^2 to heterostructures. All transferred layers and heterostructures were reportedly of high quality in that they featured uniform coverage across silicon wafers up to 100mm in diameter; after the transfer, the 2D materials showed little strain compared to other methods for moving graphene from its growth substrate to the target wafer.

"Our transfer method is in principle applicable to any 2D material, independent of the size and the

type of growth substrate", says Prof. Max Lemme, from Graphene Flagship partners AMO GmbH and RWTH Aachen University. "And, since it relies only on tools and methods that are already common in the semiconductor industry, it could substantially accelerate the appearance on the market of a new generation of devices where 2D materials are integrated on top of conventional integrated circuits or microsystems."

"This work is an important step towards this goal, and although many further challenges remain, the range of potential applications is large: from photonics, to sensing, to neuromorphic computing. The integration of 2D materials could be a real game-changer for the European high-tech industry," concluded Lemme.

Graphene Flagship researchers have also devised a wafer-scale fabrication method that paves the way to creating next generation photonic datacom and telecom devices. As PIC developers and manufacturers appreciate, the classic pluggable transceivers in today's data centers have limitations in terms of size and cost.

An especially vexing issue is power consumption, which is directly related to greenhouse emissions. Graphene could change this and transform the future of broadband communications. Graphene Flagship researchers have devised a wafer-scale fabrication technology that, thanks to predetermined graphene single-crystal templates, allows for integration into silicon wafers, enabling automated manufacturing that in turn paves the way to higher volume production.

Details of the researchers' work was published recently in the journal 'ACS Nano,' and represents the value of collaboration taking part in Graphene Flagship sponsored endeavors. Participants included CNIT and the Istituto Italiano di Tecnologia (IIT), in Italy; the Cambridge Graphene Centre at the University of Cambridge, UK; and Graphene Flagship associate member and spin-off, CamGraphIC. INPHOTEC and researchers at the Tecip Institute in Italy provided the graphene photonic integrated circuits (PICs) used in the study.

The adoption of single-crystal graphene arrays was instrumental in the group's success, according to study participants.

"Traditionally, when aiming at wafer-scale integration, one grows a wafer-sized layer of graphene and it is then transferred onto silicon," explained Camilla Coletti, coordinator of IIT's Graphene Labs, who co-led the study. "Transferring an atom-thick layer of graphene over wafers while maintaining its integrity and quality is challenging," she added. "The crystal seeding, growth and transfer technique adopted in this work ensures (placement of) wafer-scale high-mobility graphene exactly where it is needed; this is a great advantage for the scalable fabrication of photonic devices like modulators," Coletti concluded. By 2023 researchers estimate that the world will see over 28 billion connected devices, most of which will require 5G to maintain connections to various network infrastructure. These challenging requirements will demand new technologies.

"Silicon and germanium alone have limitations; however, graphene provides many advantages," said Marco Romagnoli from Graphene Flagship partner CNIT. "This methodology allows us to obtain over 12,000 graphene crystals in one wafer, matching the exact configuration and disposition we need for graphene-enabled photonic devices," he added. Furthermore, the process is compatible with existing fab toolsets and processing techniques, which should accelerate its industrial uptake and implementation.

In a 'Nature Communications' article, researchers from Graphene Flagship partners used this approach to demonstrate a practical implementation: "We used our technique to design high-speed graphene photodetectors," says Coletti. "Together, these advances will accelerate the commercial implementation of graphene-based photonic devices."

Frank Koppens, Graphene Flagship Leader for Photonics and Optoelectronics, remarked that: "This is the first time that high-quality graphene has been integrated on the wafer-scale. The work shows direct relevance by revealing high-yield and high-speed absorption modulators. These impressive achievements bring commercialisation of graphene devices into 5G communications very close."

Andrea C. Ferrari, Science and Technology Officer of the Graphene Flagship and Chair of its management panel added: "This work is a major milestone for the Graphene Flagship. A close collaboration between academic and industrial partners has finally developed a wafer-scale process for graphene integration. The graphene foundry is no more a distant goal, but it starts today."

For additional information about work of Graphene Flagship member organizations and industrial partners that support ongoing photonic and electronic applications, please visit: www.graphene-flagship.eu

Graphene Flagship researchers have also devised a wafer-scale fabrication method that paves the way to creating next generation photonic datacom and telecom devices. As PIC developers and manufacturers appreciate, the classic pluggable transceivers in today's data centers have limitations in terms of size and cost

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PI's fast alignment testing technology adds benefits of ACS controls

Fast, accurate and repeatable testing requirements have in the past impeded the rapid roll-out of photonic integrated circuits (PICs) and related components at cost-effective, high volume scale. Physik Instrumente has pioneered fast optimization technology and has added new algorithms and alignment-enabled controls from ACS to achieve productivity gains for large-format optic and photonic production processes.

BY SCOTT JORDAN, HEAD OF PHOTONICS; SENIOR DIRECTOR, NANOAUTOMATION; PI FELLOW, PI (PHYSIK INSTRUMENTE)

PHYSIK INSTRUMENTE'S (PI's) fast optimization technology has proven to dramatically improve production economics in processes as diverse as photonics wafer probing, device packaging, and chip testing and even laser and optical equipment manufacturing. The combination of speed, nanoscale performance and industrial robustness is reducing costs and improving yield worldwide.

Now the flexible combination of PI´s industrial stages and new alignment-enabled controls from ACS address additional tough throughput and yield challenges for photonics production. Large-format production processes can now be addressed, with each mechanism contributing intelligent alignment for test and assembly. This opens new possibilities for hyper-efficient systems architectures.

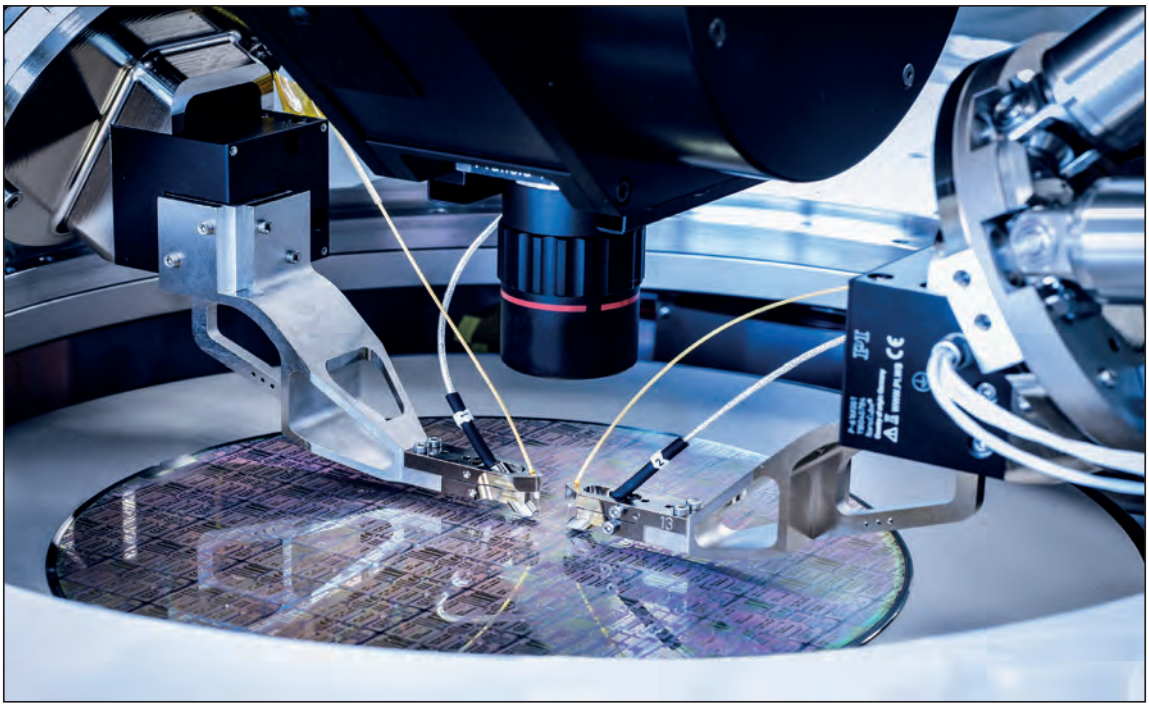


Image 1: The double sided fiber alignment systems from PI enables simultaneous positioning of input and output fibers for chip testing and wafer probing. (PI image)

PI's unique optimization functionality is firmware-based, offers the unique option of parallel alignment across multiple inputs, outputs and degrees-of-freedom, and can improve process throughput by a factor of 100 or more compared to legacy approaches.

Background

Alignment automation emerged three decades ago. In an era dominated by single-mode pigtailing applications, it was an enabler that helped eliminate costly manual submicron-alignment processes during device test and assembly.

The photonics world has advanced, though. Wafer-based photonics now drives the industry. Adoption volumes are orders of magnitude higher than in the 1997-2001 photonics boom, and the devices are quite different.

For example, multiple I/Os necessitating multiple degree-of-freedom optimization, with each coupling frequently presenting non-Gaussian multimode cross-sections and interactions across channels, inputs and outputs, and DoFs. While these challenges can often be met with legacy alignment techniques, the minutes-scale times required present serious challenges for production economics.

PI's unique, fifth-generation optimization technology, now well-proven in the field after its 2016 introduction, allows simultaneous alignment across channels, I/Os and DoFs, even when they interact due to optical or geometric crosstalk. The throughput improvement of this parallelism can often exceed a factor of 100, as PI routinely demonstrates in live demonstrations at conferences. So, for example, an array-device alignment that previously took a few minutes can often now be achieved in a second or less.

PI's first implementations of this technology were in fast piezo stages and hexapods. Now its key functionality has been extended to ACS controls, bringing the benefits of ground-breaking productivity to large-format applications as diverse as photonics wafer probing, device packaging, and chip testing and even laser and optical equipment manufacturing.

Moreover, the algorithms offer seamless compatibility with today's photonic devices, which often prove challenging for legacy approaches. For example, there is no implicit assumption of circular symmetry embedded in the algorithms. That posed no issues in 1997, but can be highly sub-optimal for latter-day photonic devices. It can practically be stated that these systems can virtually "optimize anything," which is definitely not the case for the decades-old approaches still commonly offered.

Deeper Dive

Two alignment techniques are most useful today: area scans, and gradient searches for fast optimization and tracking.

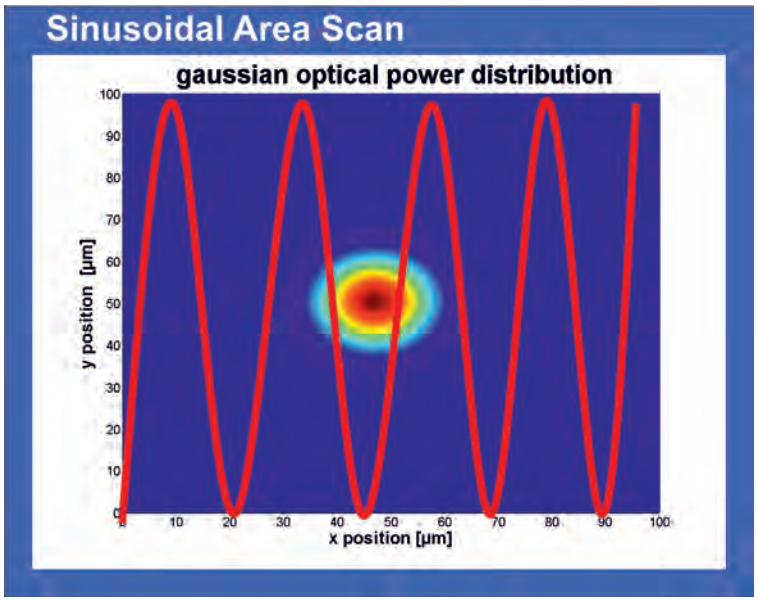


Image 2: In the case of the sinusoidal scan routine the defined surface is scanned continuously without vibration-inducing acceleration or deceleration phases. Surface, starting point, line distance, and success criteria can be defined by the user. (PI image)

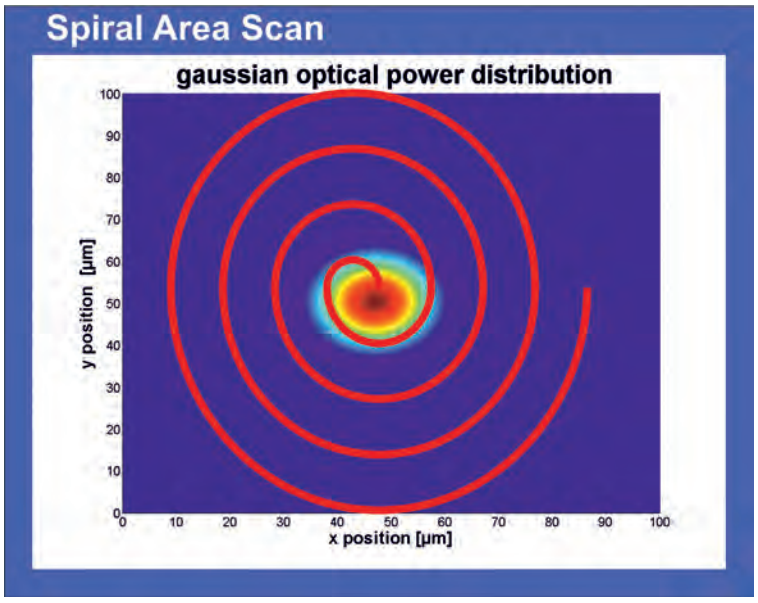


Image 3: In the case of the spiral scan routine, a defined area is scanned helically, whereby either a constant angle or a constant path velocity is maintained. Its selectable operating frequency helps to avoid system resonances. (PI image)

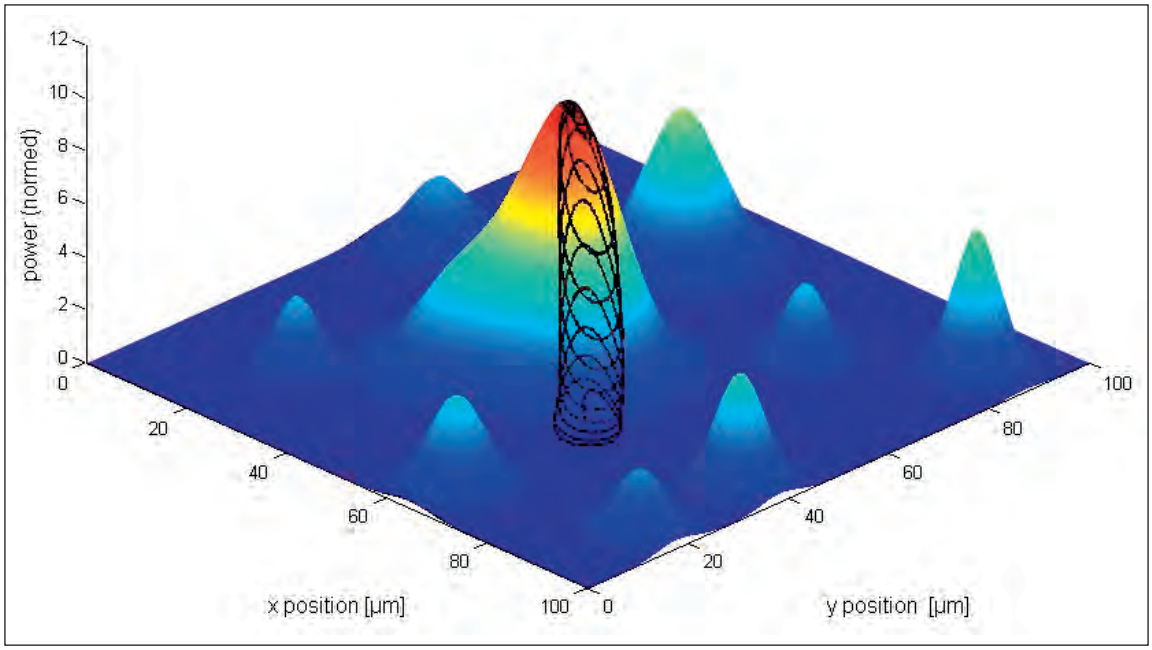


Image 4: Ground-breaking results can be achieved with the unique implementation of the gradient search algorithm. If the light signal is present, this gradient search makes it possible to find the signal maximum in typically less than 1 second. (PI image)

Area Scans

A good example of a legacy approach to an area scan is a classical raster or serpentine scan, which sweeps one axis, then increments its orthogonal axis, and repeats until the area is covered. Variations on this theme are common, including stepwise hill-climbs. But these approaches pose fundamental issues today. The stopping-and-starting adds settling time and causes vibration throughout the system, and the linear acquisitions can lead the system to actually de-align in common situations of asymmetric coupling profiles.

By comparison, PI's firmware-based area scans use smooth, continuous sinusoidal and spiral patterns of selectable frequency. System resonances can easily be avoided, allowing the non-stop scan to proceed without vibration. The result is considerably higher speed. Add built-in modelling in some controllers, and the system can determine the peak (or even the centroid of a top-hat coupling) with good accuracy and speeds down to a few hundred milliseconds.

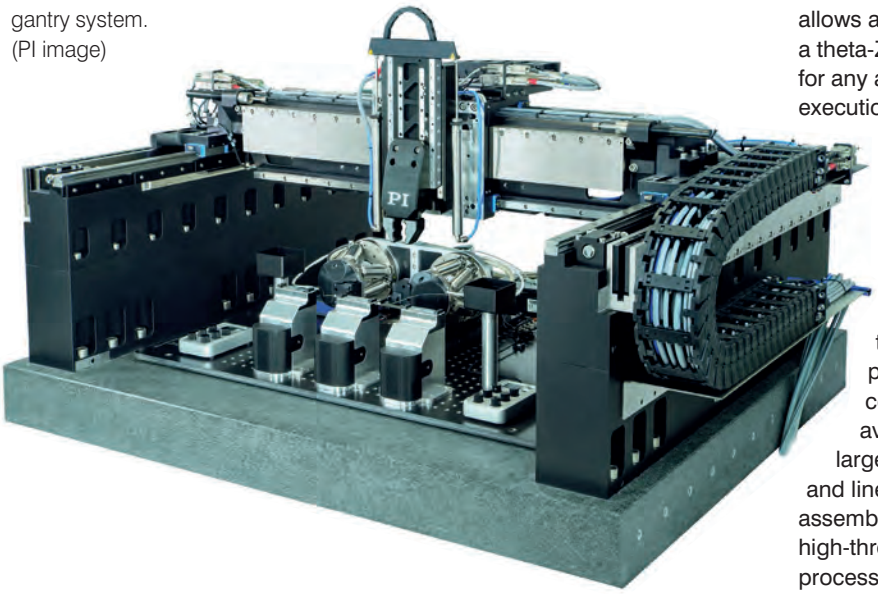


Image 5: Example of an automation subsystem for multi-channel automated photonic-device assembly tools, based on the proven double-sided F -712 HA2 alignment system and PI´s multi-axis gantry system. (PI image)

Gradient Search

The digital gradient search was first developed in 1987 and, until now, has been mostly unchanged in its implementation through four subtle generations of the technology. A small, circular motion causes the coupling signal (or other figure-of- merit) to vary, and this variation can be analyzed in phase and amplitude to determine the instantaneous gradient. This allows a fast and direct path to optimum, with tracking possible for appropriate mechanisms.

PI's radical fifth-generation approach builds on this classical foundation to enable multiple gradient searches to proceed in parallel. For example, this allows an XY lock-on to be performed at the same time a theta-Z optimization runs – an essential combination for any array-device alignment. This fast, parallel execution replaces the time-consuming iterative loop of separate XY and theta-Z alignments that was formerly required. One step, instead of dozens.

Breakthrough

Since 2016, firmware-based fast-area scan, gradient search, and parallel gradient search technologies have been implemented in PI's powerful piezo nanopositioner and hexapod controllers. Now fast alignment functionality is available for ACS controls. Combined with PI's large industrial stages (including spindle-driven and linear-motor stages, gantries and air-bearing assemblies), this forms a foundation for especially high-throughput applications involving large-area processing, such as when devices are processed in

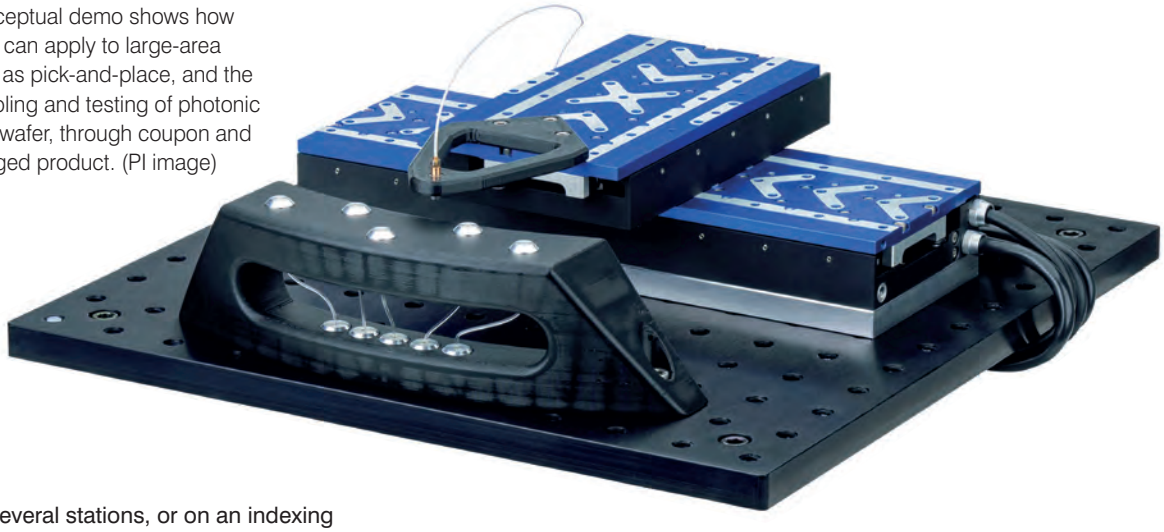


Image 6: This conceptual demo shows how PI's fast alignment can apply to large-area applications, such as pick-and-place, and the screening, assembling and testing of photonic devices. From the wafer, through coupon and chip, to the packaged product. (PI image)

trays, or across several stations, or on an indexing platform or conveyor.

ACS controls lead the industry in modularity and performance. Based on an EtherCAT open, distributed architecture, they support absolute encoders, minimizing system start up times, easing initialization approaches and reducing collision risks. ACS' yaw control (combined with PI's highly optimized joint construction) provides industry-leading orthogonality correction and minimizes risk of axis binding – a distressingly common issue for older architectures. True MIMO gantry control plus dynamic cross-axis control yields uniform performance over the gantry area, eliminating grid-based approximation methods and their consequent lowest.

common-denominator approach to tuning over large areas. Together, these mean higher performance and reproducibility in application.

These benefits come with PI's and ACS' rich offering of global support options, ranging from on-site Quick Start and training, to extended warranties and service plans, to consulting and co-engineering, to application and software consultation and quick-port approaches for key transiting from other architectures.

Summary

Photonics today is serious business, with a rapid rate of innovation and broad adoption by important semiconductor and networking players. Manufacturing and testing these devices demands flexibility and high performance from production systems and tooling.

Multiple studies have spotlighted alignment time as the highest cost contributor to photonic device fabrication, both from the lengthy process times formerly required and from the repeating requirement for alignment throughout the production process. PI's revolutionary fast alignment technology is unmatched for meeting these challenges, and now it is deployed in large-area mechanisms based on a modular, open-architecture approach ideal for systems integration and tooling platforms.

About the Author

Scott Jordan is head of the photonics market segment in the globally active PI Group, and a PI Fellow. He lives in Silicon Valley and has been with PI for over 20 years. Scott was active as Director of NanoAutomation Technologies and made a decisive contribution to continued technological development of the company. A physicist with an MBA in Finance/New Ventures, Scott is well known in the community for his passion and engagement.

About Physik Instrumente L.P.

Physik Instrumente L.P. (PI) is a leading manufacturer of nanopositioning, linear actuators and precision motion-control equipment for photonics, nanotechnology, semiconductor and life science applications. PI has been developing and manufacturing standard and custom precision products with piezoelectric and electromagnetic drives for over 40 years.

By acquiring the majority shares in ACS Motion Control, a worldwide leading developer and manufacturer of modular motion controllers for multi-axis and high-precision drive systems, PI has made a major step forward in providing complete systems for industrial applications with the highest demand on precision and dynamics. In addition to four locations in Germany, the PI Group is represented internationally by fifteen sales and service subsidiaries. The company has been ISO 9001 certified since 1994.

For more information please contact Stefan Vorndran, VP Marketing for Physik Instrumente L.P.; 16 Albert St., Auburn, MA 01501; Phone 508-832-3456, Fax 508-832-0506; email stefanv@pi-usa.us; www.pi-usa.us.

Rockley Photonics:
Bold plans in tough times

How an up and coming silicon photonics start-up plans to take on a soon-to-be multi-billion dollar industry

BY REBECCA POOL

BACK IN 2020, UK-based Rockley Photonics won $50 million in investment funds to grow its silicon photonics manufacturing technology, crucial for integrating III-V materials to silicon photonic integrated circuits. Investments now total more than $225 million, with the platform ready to take on large-volume production of high-density photonics circuits, including optical fibre and datacentre communication transceivers.

As chief executive, Andrew Rickman, says: “The latest funds are testament to the strength of our technology... We’re on track for the big wave of 400G transceivers and believe we’ll be in a pre-eminent position for the further wave of 800G transceivers for data centres.”

The timing of the funding isn’t surprising. Over the next few years, the global silicon photonics market is expected to mushroom, with analysts unanimous that this sector will be worth at least $3 billion come 2025 to 2027.

US-based Research and Markets predicts a mighty $3.77 billion by 2027, Global Market Insights, US, forecasts $3 billion by 2026, while Yole Développement of France, reckons the silicon photonic transceiver industry will be worth $3.6 billion come 2025. Today’s market comes in at around $800 million.

Growth looks set to be largely fuelled by increasing demand for high-speed broadband services and deployment of 5G technologies and data centres

worldwide, including developing nations, with applications such as LiDAR also emerging in the automotive sector. And like its competitors, Cisco, Intel, Macom, Mellanox, Neophotonics and more, Rockley Photonics is intent on capturing market share here.

However, Rickman and recently appointed chief commercial officer, Vafa Jamali, also believe the healthcare and wellness sector holds huge promise, with the company developing optical sensing chipsets for handheld and wearable devices.

Jamali spent more than 25 years working in the medical device industry, most recently at US-Ireland based Medtronic, and reckons that while home health has been an emerging trend for some time, the pandemic has accelerated demand.

"So many people now want to have a lab on their wrist [that provides] accurate and meaningful measurements that they can trust," he says. "This market is enormous and is growing at up to a 10 percent CAGR – I think there's a great opportunity to disrupt with a better technology, and we reckon we have something that can do this."

"So that's my thesis for coming to Rockley after 28 years in medical devices," he adds. "There's nobody that aggressively addresses this market [with non-invasive devices], I am excited."

Rickman is equally bullish, and highlights how wearables and smartphones are addressing a $45 billion market right now. "In our journey of 30 years in silicon photonics, we're always looking out for that massive opportunity, and we know that anything that really gets driven by an economy of scale is in a consumer market," he says. "So we saw this opportunity in devices for health and wellness – we believe that this is by far the single biggest opportunity in the field of silicon photonics."

Winning formula

But how does Rockley Photonics intend to compete with industry players such as Cisco and Intel? Rickman is no stranger to tech giants.

Cisco and Intel each invested $10 million in Bookham Technology, the silicon photonics components business he founded back in 1988. Meanwhile, the company he chaired from 2008, Kotura, was acquired by Israeli-American computer networking multinational, Mellanox Technologies, for its 100G photonic ICs in 2013.

Since launching Rockley Photonics, in 2013, Rickman has asserted that the company's 'third generation' silicon photonic platform is very different to the technology he helped to pioneer, and is offered, by rival firms. While most existing technologies integrate photonic structures with CMOS on a semiconductor chip, Rickman describes Rockley's silicon photonic process as 'engineered from the ground-up and optimised for photonics and not electronics'. And the platform still runs in large-scale silicon foundries.

According to the chief executive, difficulties arise when using a CMOS approach to integrate photonics structures at sub-micron dimensions as the wavelength of the photon is of the order of a micron. Rockley's platform counters this in a number of ways, including the use of multi-micron waveguides that lead to lower waveguide losses and more consistent performance.

The platform also: eliminates the need for active precision fibre alignment, a key stumbling block in the manufacture of transceivers; efficiently integrates III-Vs; removes expensive specialised processing techniques; and can pack a large number of components at high density. Indeed, in 2018, Rockley demonstrated how its technology could cost-effectively make high-density optoASICs for datacentre switching.

China links

But beyond the different platform approach, Rockley also hopes to have an edge on its competitors by having a foot in the Chinese market with its joint venture with optical fibre and cable provider, Hengtong Optic-Electric. The partners are manufacturing 400G optical transceiver modules based on Rockley's silicon photonics technology.

"We also realised that to be competitive we needed to take a vertically integrated approach to the market, and the Hengtong joint venture enables this," points out Rickman. "So we're now ramping up and shipping chips to our customers."

Indeed, the timing looks right and the market is growing. The silicon photonics industry has already shipped millions of units of optical transceivers, and beyond Hengtong, other China-based companies have entered the market.

For example, Chinese cloud computing business, Alibaba Cloud, teamed up with US-based and Nokia-owned silicon photonics developer Elenion Technologies to manufacture a 400G optical transceiver. And China-based optoelectronics device provider, Broadex Technologies, has also joined forces with German start-up Sicoya, which manufactures silicon photonics transceiver chips.

Rickman is excited. From word go, Rockley has been working closely with large silicon and III-V materials foundries, as well as packaging facilities, preparing for the all-important ramp to large-volume manufacture.

"We believe that we now have the lowest cost technology and the lowest cost business structure to address a market of a particular time, including this extraordinary opportunity in health and wellness," he says. "Next year is going to be all about ramping up production and from there on in we expect volumes to grow significantly."

Rockley Photonics chief commercial officer, Vafa Jamali.

Andrew Rickman: Founder, Chairman & CEO of Rockley Photonics

Super-fast optical interconnects

Universal chip-to-chip optical interconnects are delivering off-package communication at the bandwidth density and energy cost of in-package electrical incumbents

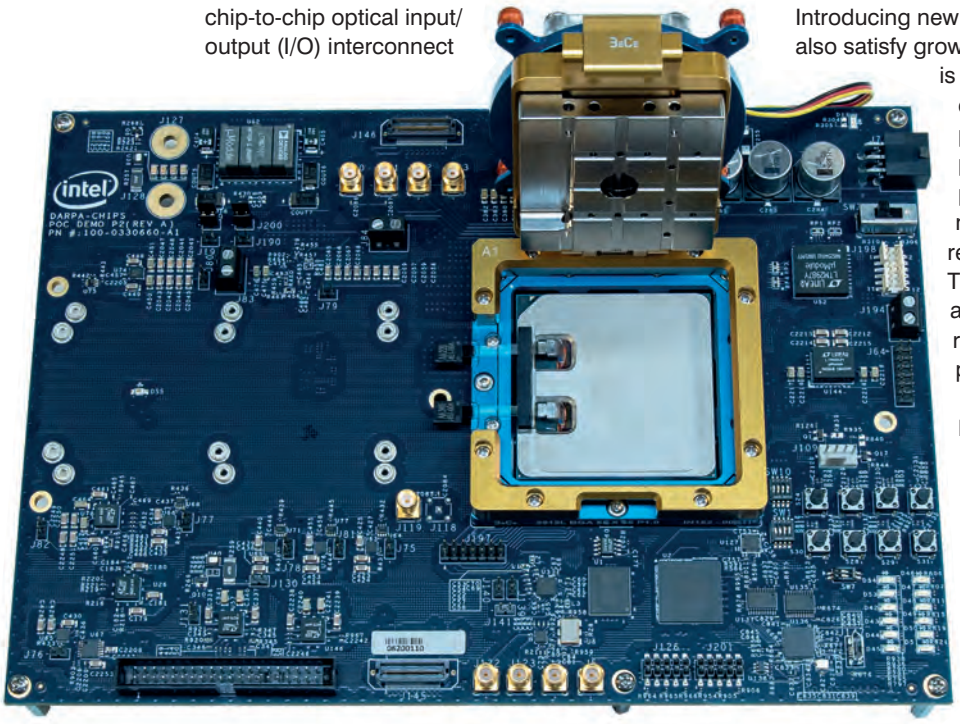
BY VLADIMIR STOJANOVIC FROM AYAR LABS

DATA DASHES through today's optical fibre system networks before it slows to a crawl at copper interconnects. These bottlenecks occur at copper pins and wires on circuit boards, where electrons transmit data at far lower speeds. So great are these delays that there will come a time when copper interconnects will have to be replaced by optical signalling.

Offering a universal solution to this issue is our team from Ayar Labs of Emeryville, CA. Founded in 2015 as a spin-out of three universities – Massachusetts Institute of Technology; University of California, Berkeley; and University of Colorado, Boulder – we are renowned for our pioneering work in micro-ring chip architectures.

We have developed a chip-to-chip optical input/output (I/O) interconnect technology that addresses several weakness associated with electrical interconnects and their scaling limitations. We tackle weaknesses associated with signalling speeds and pin count, which both apply the brakes to electrical I/O connections, and power consumption that is increasing at an unsustainable rate.

The latter concern should not be taken lightly, as it will not be long before the power drawn by the off-chip I/O will account for almost all the power consumption of the package. When this occurs, it will be infeasible to use electrical I/O interconnects, which are primarily made of copper. By then, there will need to have been a shift to chip-to-chip communications based on photonics, a technology that will eliminate electrical I/O bottlenecks.



Introducing new photonic I/O architectures will also satisfy growing throughput demands. There is an emergence of heterogeneous computing, involving central processing units (CPUs), graphic processing units (GPUs), field-programmable gate arrays (FPGAs), neural network accelerators, and resource pooling on the memory side. This trend demands more I/O at the application level, while electrical I/O is running into pin count, signalling and power limitations.

Providing an impetus to act sooner rather than later, the penalties for leaving the chip, package, and board are on the up (Figure 1). This begs the question: will the 112-Gbit/s serializer/deserializer be the last long-range electrical I/O solution? In field deployments, system integrators are already seeing the limitations of 112-Gbit/s long-

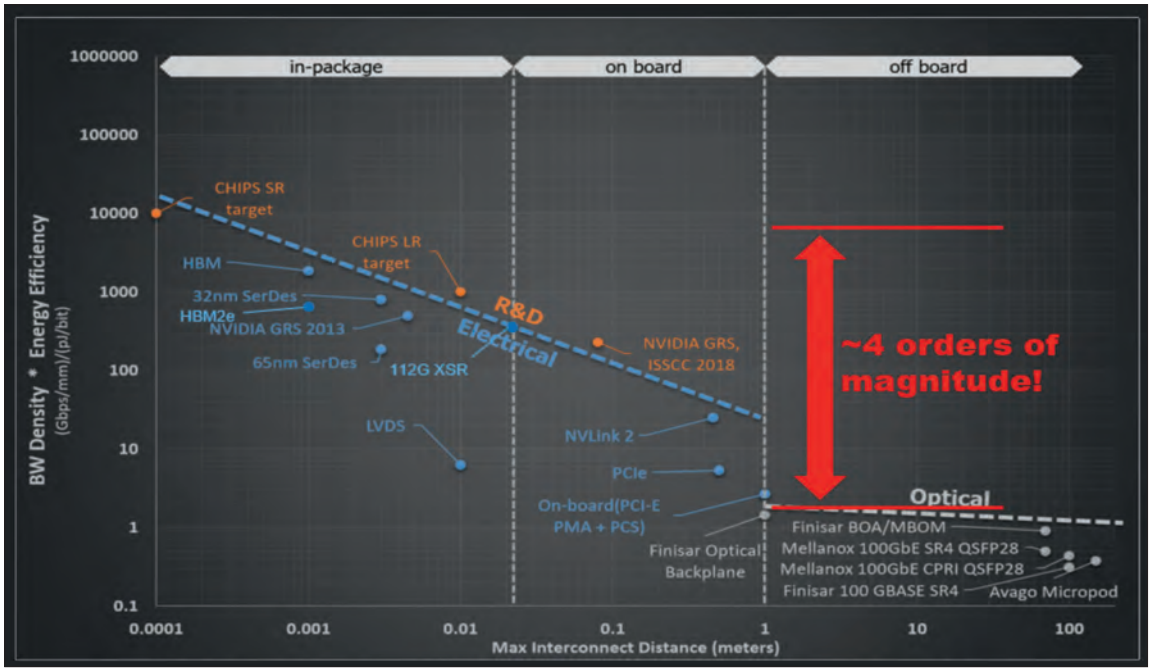


Figure 1. Large penalties will be incurred for leaving the chip, package, and board (Source: Gordon Keeler, DARPA MTO, ERI Summit 2019).

range electrical connections – they are incapable of spanning the signalling lengths required for off-board, rack-scale communication.

To evaluate the performance of the I/O technologies, we use a figure-of-merit involving quite a few terms. It considers the bandwidth density from the edge of the I/O solution, multiplied by its associated energy efficiency. This provides a yardstick that captures the Gbit/s per millimetre per pJ/bit, as a function of distance. When crossing the boundaries from package to board with I/O technologies, this metric plummets – there is a gap of about four orders of magnitude between in-package interconnect solutions and state-of-the-art optical solutions that provide off-board connectivity.

Into this challenging space comes our new optical I/O technology. It delivers a universal I/O solution that provides off-package communication at the bandwidth density and energy cost of in-package electrical incumbents.

An in-package solution

To pull off an optical I/O, certain requirements must be fulfilled (see Figure 2). We meet them with our own optical I/O system architecture. This is a chiplet-based solution that is co-packaged directly with the host system-on-chip (SOC) within a multichip module (MCM) package. By incorporating a monolithic electronic-photonic CMOS chiplet, which we call TeraPHY, we realise a flexible electrical I/O interface adapted to the host SOC, whether the geometry is wide parallel or high-speed serial. Adopting this approach offers flexibility, giving a choice between a silicon interposer and an organic substrate for the package.

One of the merits of our single-chip solution is that it enters a manufacturing ecosystem already established for MCMs. With our architecture, we keep the laser supply outside the module. This simplifies packaging, improves laser reliability, and alleviates issues related to the operational temperature mismatch of SOC packages and laser optical supplies. Due to these advantages, we realise further integration of lasers into a multi-port, multi-wavelength laser module solution, which we refer to as SuperNova.

Several system and technology requirements have to be met for in-package optical I/O to become a reality (see Figure 3). At the system level, the optical I/O requires high-density optical devices and circuits capable of fulfilling the high-bandwidth density demands of future SOCs and applications. To ensure success, it is critical to draw on existing CMOS processes and manufacturing infrastructure, while complying with I/O standards. And, perhaps most importantly, production must leverage scalable, high-volume manufacturing of the semiconductor technology.

We meet these requirements with wavelength-division-multiplexed (WDM) links that support multiple wavelengths per fibre and allow scaling of the data rate to meet the bandwidth density requirements of future applications. We use closely spaced wavelengths – they are separated by a few hundred GHz – running concurrently on the same fibre. Transmitters and receivers modulate/receive each wavelength separately. By leveraging monolithic integration and the CMOS process, we create a chiplet-driven technology with tight integration of electronics and photonics while improving bandwidth density and energy metrics. Finally, our monolithic approach taps into the ecosystem of CMOS foundries and scalable high-volume packaging manufacturing of multichip modules. Thanks to this, we have created a compatible solution for advanced packaging and fibre attach.

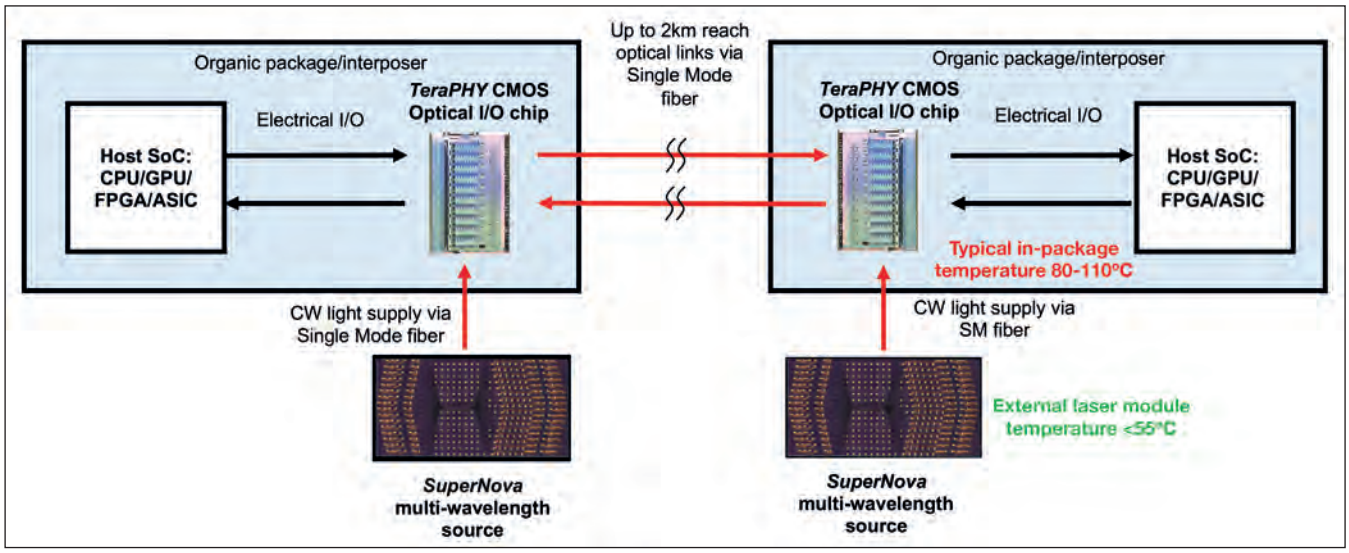


Figure 2. Ayar Labs' in-package optical I/O system architecture (Source: Ayar Labs).

Optimising the optical architecture

At the heart of our optical I/O architecture lies micro-ring modulator and WDM technology (see Figure 4). At its crux is an off-chip continuous-wave laser, based on non-proprietary standards. This emitter is driven by the Continuous-Wave WDM Multi Source Agreement (CW-WDM MSA), which provides optical power in one or more wavelengths to the TeraPHY chip. Light enters this chip through a coupler and then travels along it in an optical waveguide. The light encounters a micro-ring modulator, which converts data from an electrical domain to the optical domain.

Our micro-ring has a very narrow resonance, typically just 20-40 GHz that is repeated at a much larger period, such as 3.2 THz. With these conditions the micro-ring is wavelength selective. This allows the micro-ring modulator to act as both a modulator and a wavelength division multiplexer, enabling the addition of more wavelengths to the same fibre/waveguide. By making our micro-ring modulators out of silicon, we are employing the same material used to produce all the transistors and optics on the chip.

Output from our chiplets is coupled to the fibre and sent to the receiver chips. Here, micro-ring detectors convert data from the optical domain to the electrical domain. Micro-ring detectors actually perform a dual role, combining the tasks of detector with that of wavelength-division demultiplexer, picking the selected modulated wavelength for the receiver.

We can increase the bandwidth density of our links, alongside the overall throughput of the fibre, by adding wavelengths to the fibre. It's an improvement that we accomplish without increasing strain on backend electronics. Using cascaded micro-rings as independent communication channels, we realise up to 64 micro-rings per fibre. This yields a technology that provides up to 6 to 8 Tbit/s per fibre (see Figure 5).

Drawing on this development and others, we have constructed a complete WDM link system, formed by integrating electronic and photonic components. Electronics modulates and receives the data and controls micro-ring resonances through thermal tuning and wavelength locking (see Figure 6). With our technology, transmitter ring modulator resonances are locked to incoming laser wavelengths, prior to locking of the receiver. Working together, locking loops track local and global temperature fluctuations

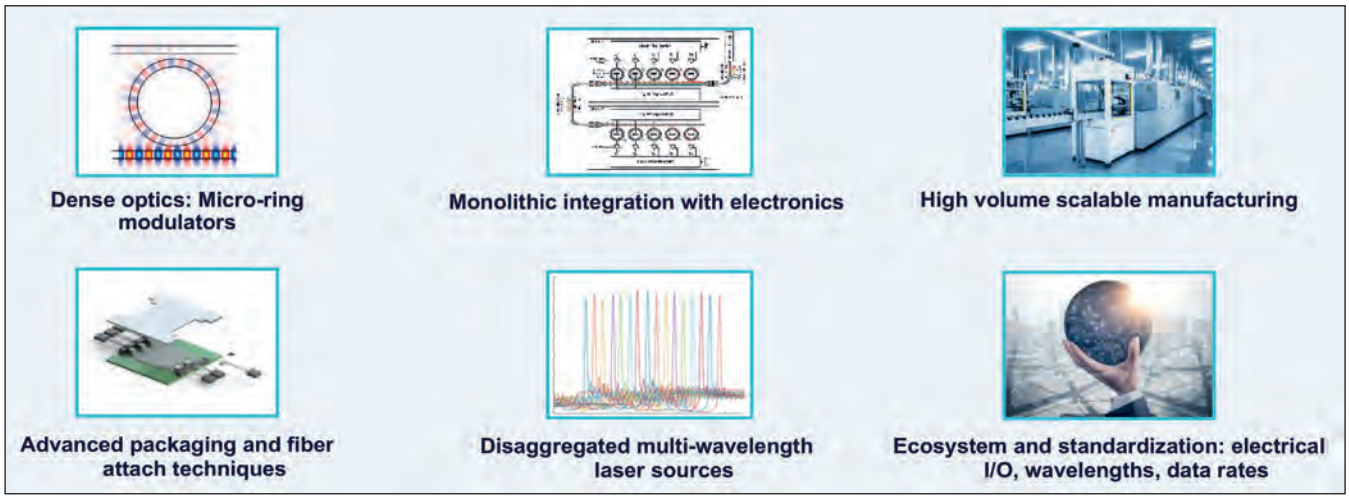


Figure 3. Six areas must be addressed to make in-package optical I/O a reality (Source: Ayar Labs).

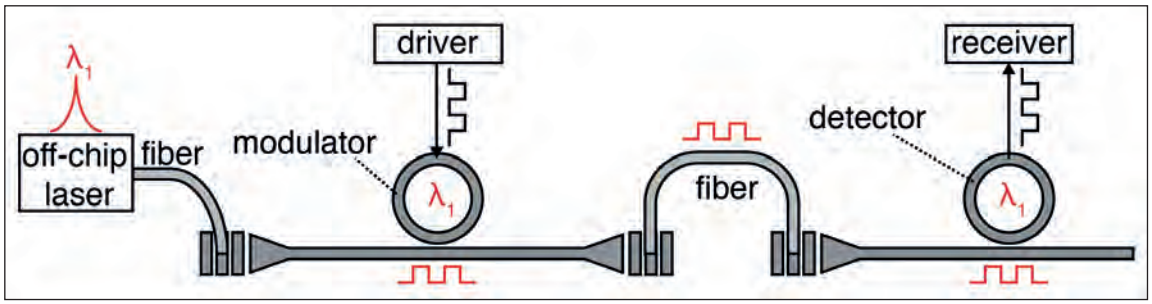


Figure 4. The TeraPHY optical I/O architecture, centred on a micro-ring modulator and WDM (Source: Ayar Labs).

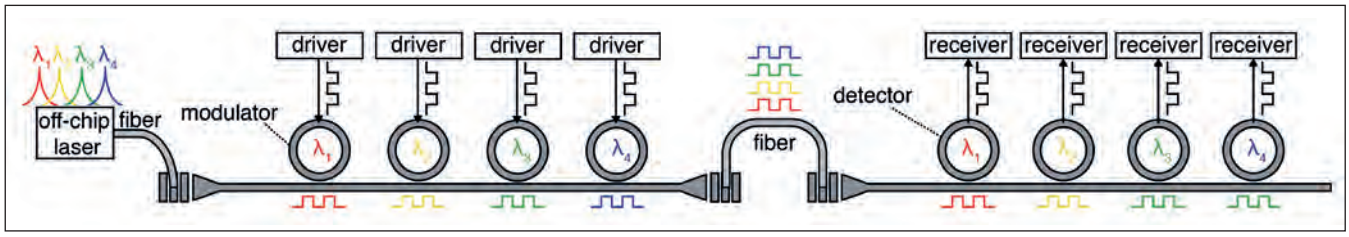


Figure 5. Wavelengths can be added to the fibre – without increasing the strain on the backend electronics – to improve energy-efficiency, bandwidth density and overall throughput of the fibre (Source: Ayar Labs).

while compensating for process-induced wavelength grid non-idealities that occur in the laser, transmit and receive chips.

Our interconnects excel in bandwidth density and energy efficiency, thanks to miniaturisation of the micro-ring devices, which are integrated with CMOS transistors. The link architecture has enabled us to create TeraPHY, which is essentially a chiplet that provides Tbit/s optical connectivity and offers an alternative to electrical serializer/deserializer chiplets. The main features of our demonstration chiplet are: a 24 channel advanced interface bus (AIB), providing a total data bandwidth of 906 Gbit/s; ten photonics Tx/Rx macro pairs, configurable to 125 Gbit/s to 256 Gbit/s per macro that equates to 1.28 Tbit/s to 2.56 Tbit/s per chip; a non-return to zero modulation format for the optical channel, eliminating the need for forward-error correction; a reach of up to 2 km; and an all-inclusive estimated energy efficiency of less than 5 pJ/bit.

Our TeraPHY chiplet operates like an electrical chip. To ensure this, we use a variety of pitch bumps – there is a combination of a tight 55 µm-pitch for the AIB interface standard, and a mixed pitch, because our chiplet uses a variant of an embedded multi-die silicon interconnect bridge (see Figure 7). With this arrangement, the main die is connected to others via a piece of silicon. It has been embedded within an organic substrate to provide fine-line connectivity using a 55 µm-pitch for the bump between the die. This enables fine-pitch 2.5D-type packaging without having to use a silicon interposer. Instead of that we can use an organic substrate, which provides greater flexibility in terms of area and yield. A major selling point of our in-package chiplet is that it provides a universal off-package interconnect solution for any SOC, including FPGAs, CPUs, GPUs, tensor processing units and switches. Applications include: radar; disaggregated resources for data and high-performance computing racks; 5G connections between front-panel RFIC array and back-end digital beam-forming processors; and artificial intelligence compute scale out, such as GPU to GPU, TPU to TPU, FPGA to FPGA, and CPU to GPU.

Delivering demonstrations

Back in March 2020 we provided a live demonstration of our chiplet technology. Working in partnership with Intel under the US Defense Advanced Research

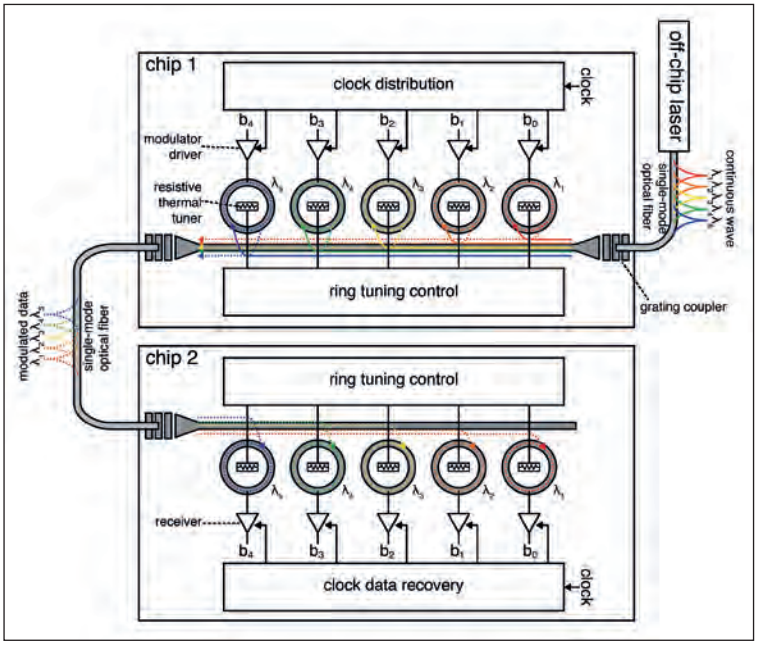


Figure 6. A complete WDM link system that integrates electronics with photonics components (Source: Ayar Labs).

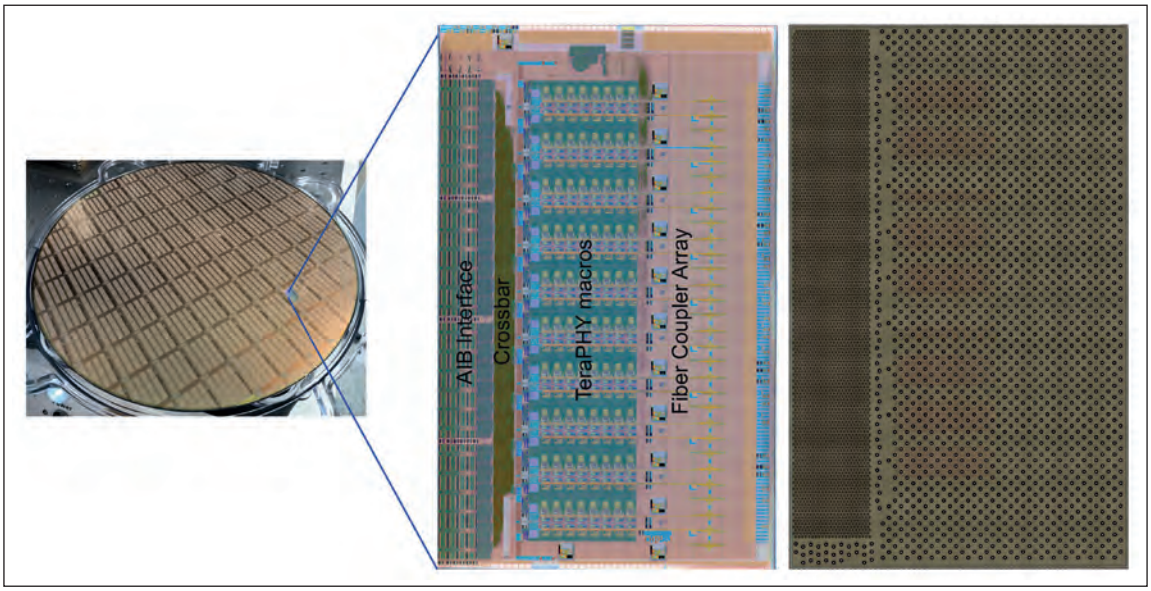


Figure 7. The TeraPHY chiplet with mixed-pitch bumps (Source: Ayar Labs).

Projects Agency's (DARPA) Photonics in the Package for Extreme Scalability (PIPES) programme, we replaced the traditional electrical I/O of a state-of-the-art FPGA with optical signalling interfaces.

This effort, which drew on Intel's advanced packaging and interconnect technology, involved the integration of TeraPHY optical I/O chiplets and an Intel FPGA core within a single package to create a MCM with in-package optics (see Figure 8). This MCM substantially improves interconnect reach, efficiency, and latency – and ultimately enables high-speed data links featuring single-mode optical lasers coming directly from the FPGA. The optical waveguides on our chiplet, which are patterned monolithically into the silicon, are the optical equivalents of copper wires. When we bring two waveguides in close proximity, we can transfer photons and power from one waveguide to another to create a coupler. Within the coupler, a 10 µm-diameter micro-ring resonator electrically modulates the light's phase and controls its direction. Light is either let through, directed to a drop port, or allowed to dissipate inside the micro-ring.

We use GlobalFoundries' 45 nm-platform for CMOS chip manufacturing. This supports the construction of our co-packaged chiplet that provides an I/O bandwidth of 2 Tbit/s, realised at a small fraction of the power compared with an electrical I/O.

DARPA's PIPES programme is targeting development of advanced integrated circuits that feature photonic interfaces capable of driving bandwidths greater than 100 Tbit/s I/O per package at energies below 1 pJ per bit. Deploying interfaces with this level of performance in FPGAs will improve high-performance computing, AI, large-scale emulation, and US Department of Defense capabilities, such as radio-frequency arrays, advanced radar, and 5G (see Figure 9).

Our demo featured eight wavelength-division-multiplexed channels per macro, using I/O data rates

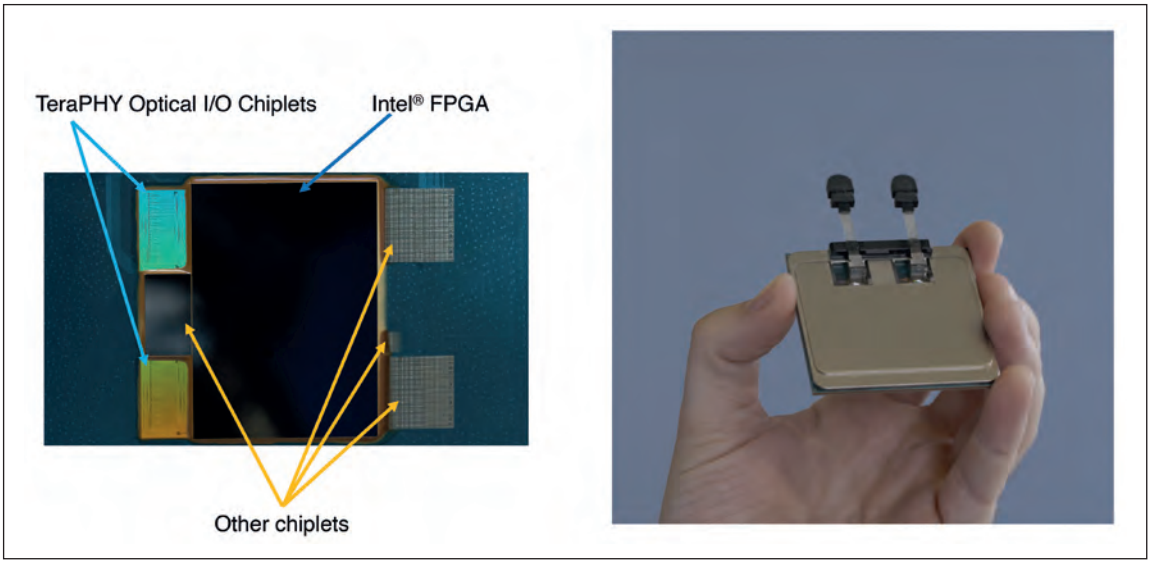


Figure 8. Multi-chip package assembly with in-package optics (Source: Ayar Labs).

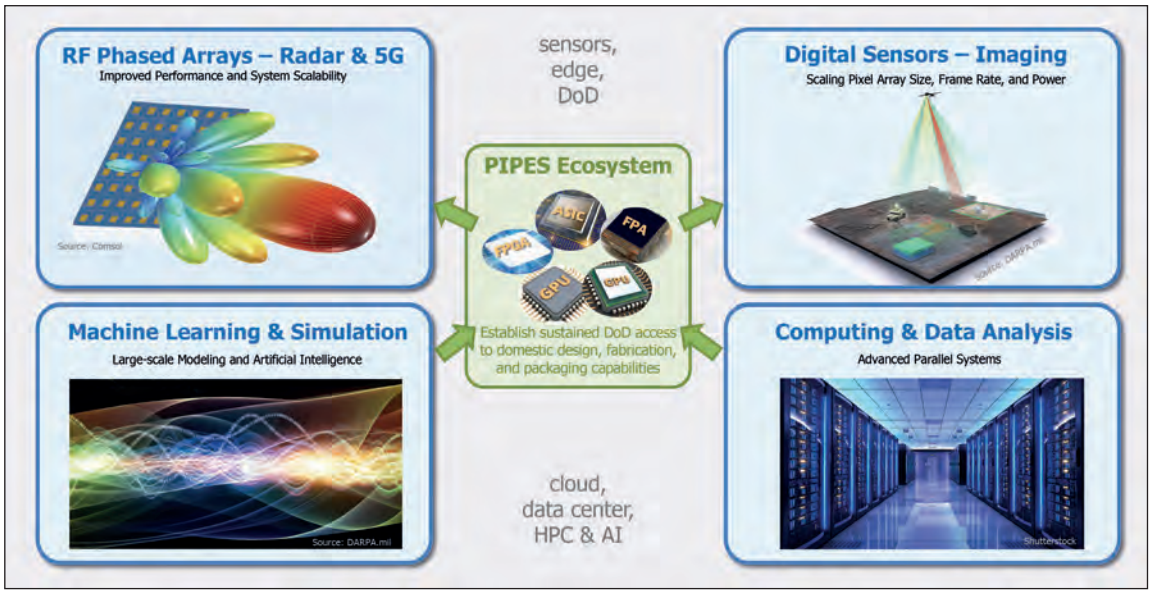


Figure 9. Application areas for advanced integrated circuits with photonic interfaces (Source: Gordon Keeler, DARPA, ERI Summit 2020).

of 16 Gbit/s/wavelength across four optical macros on a single chip. This provided connectivity at 512 Gbit/s.

The demonstration involved low-power signalling standards and chiplet packaging processes developed by Intel for another DARPA programme. This work also used Intel's common interface standard, known as AIB. It is a publicly available, open interface standard that enables us to integrate the MCM and in-package optics.

In production, our single chiplet is expected to reach up to 2 Tbit/s I/O over 64 wavelength channels, at 32 Gbit/s per wavelength. There is no need for forward-error correction, and latency is less than 10 ns. Our chiplet is also designed to work with an off-chip multi-wavelength continuous-wave laser source and integrate with any type of partner system on package – this could be a CPU, GPU, ASIC, or FPGA – to connect switches, servers, and cards over distances up to 2 km.

Beyond our work with DARPA and Intel, we are continuing to advance our in-package optical I/O technology. In a single-die package demonstration this July we took another step forward, highlighting that our micro-ring-based WDM can meet the requirements for next-generation high-performance chip-to-chip I/O. This effort showcased 25 Gbit/s transmitters and 25 Gbit/s receivers, with noteworthy accomplishments including an aggregate bandwidth of 800 Gbit/s on the transmitter side and a bit error rate below 1 x 10^{-12} on the receiver side (see Figure 10). Combined, energy efficiency came in at just 4.91 pJ/bit.

This demonstration is a milestone on our path towards showcasing the full capabilities of our chiplet. By running each wavelength channel at 32 Gbit/s, our single chiplet can deliver an aggregate bandwidth of 2 Tbit/s for transmit and receive. We plan to roll out a 2 Tbit/s TeraPHY chiplet. But that is just the beginning of the roadmap for our technology – we will trailblaze a path to 32 Tbit/s per chip, realised at just 1 pJ per bit.

The road ahead

By producing our devices using monolithic in-package optics, we are in a unique position to leverage both the existing chiplet ecosystem and the high-volume manufacturing of MCM assembly approaches. Thanks to the use of the same package for the optics, we are not shackled by the traditional distance trade-off in energy efficiency and bandwidth density. This opens the door to new high-performance computer architectures with off-package communication at the cost, energy, and bandwidth density of in-package interconnects.

It is worth emphasizing that the key to realising this chip, featuring integrated photonics and electronics on the same die, is the monolithic integration of photonic components. This approach bore much fruit in the university research that laid the foundations for our company, and through further development, it is now allowing us to make further breakthroughs. We are now refining a technology where photonics components are directly integrated with advanced transistors in a 45 nm process to create complex electronic-photonic systems, such as WDM links.

Using this approach, we can create single CMOS wafers that contain chiplets that integrate photonic components with transistors to support a wide variety of electrical interfaces.

Compare our approach with that of our peers and you'll see that many of the SOC manufacturers have come up with MCM technologies that are driven by the need to realise mixed-die functions on complex applications, such as GPU, CPU, memory, or I/O. One major drawback of that type of approach is that these functions require diverse processes and process nodes – whether it is a DRAM node or a CMOS node

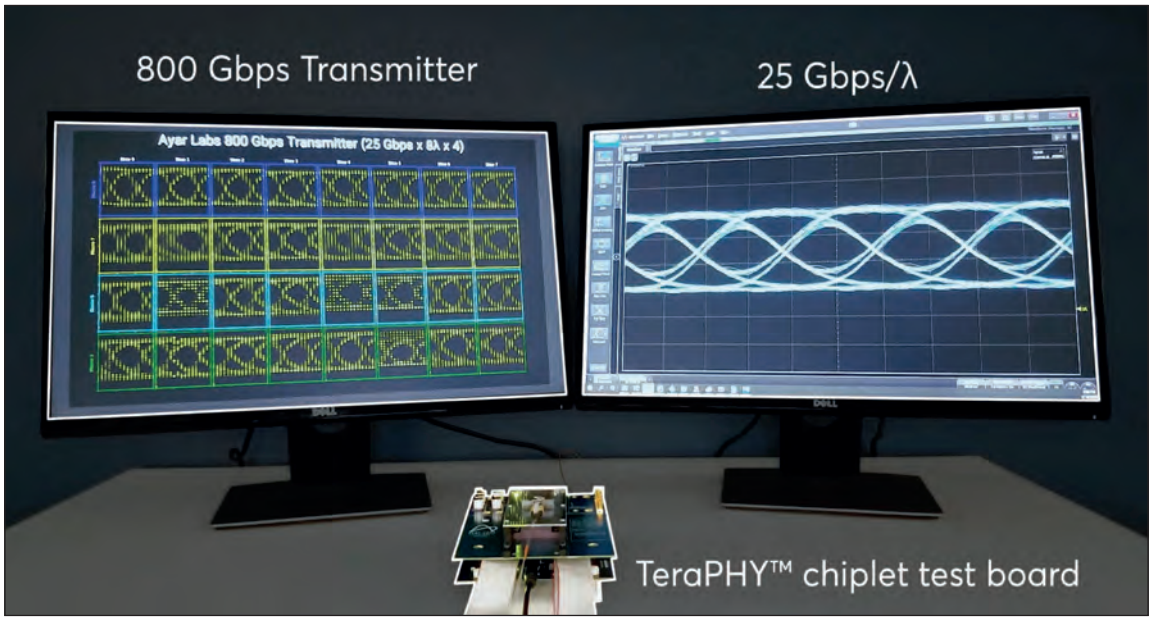


Figure 10. In a single-die package demo, Ayar Labs demonstrated 25 Gbit/s transmitters and 25 Gbit/s receivers with an aggregate bandwidth of 800 Gbit/s on the transmitter side (Source: Ayar Labs).

in 10 nm or 7 nm technology, and the complexity of MCM assembly is more cost-effective than the development of a process that encompasses all the features required by all the functions. Additionally, even for the same functions, the MCM approach enables significant cost reduction through yield improvement by breaking-up a large die (e.g. 64 core microprocessor) into smaller dies that yield better (e.g. eight 8-core dies).

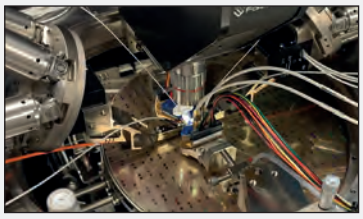
We are now starting to sample our first TeraPHY chiplet generation with select partners. This is the beginning of a journey, which will continue to new generations of the chiplet. We plan to advance our technology with electrical interface variants that address different host SoC needs and packaging scenarios, and deliver greater throughput by increasing the number of wavelengths and the data rate per wavelength. Target applications exist within artificial intelligence, supercomputing, data centres, aerospace, defence, telecom, and eventually autonomous vehicles.

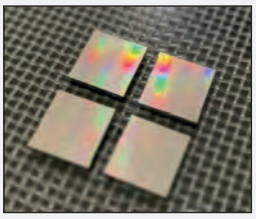
This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the US Government.

Ayar Labs achieves production milestone

Ayar Labs successfully demonstrated its patented monolithic electronic/photonic solution in December 2020 using GlobalFoundries (GF) next generation 45nm photonics manufacturing platform. This is an industry first and key milestone in providing chip-to-chip optical connectivity at scale for data-hungry applications such as artificial intelligence, high performance computing, cloud, telecommunications and aerospace.

According to Anthony Yu, Vice President of Silicon Photonics at GF, “The significance of the working silicon from Ayar Labs is important to GlobalFoundries, and more important to the industry, because the combination of working silicon in our next generation 45 nanometer platform, which is due for production qualification in the second half of next year, puts this product and in-package optical I/O using photonics on the cusp of high volume manufacturing and a much wider proliferation of photonics into the industry. This is a game changer.” In the demonstration, Ayar Labs showed functional high-performance analog transistor front ends,





connected to on-chip photonic devices, which are micro-ring modulators and photo detectors, at 32 gigabits per second, per wavelength. They also showed fully functional transmitters and receivers, both using commercial, off-the-shelf FPGAs with their TeraPHY optical I/O chiplets to send data out and receive that data optically with less than two picojoules (pJ) per bit of energy used. See the demo on ayarlabs.com.

The company also announced an expanded sampling program of its next-generation chiplet developed on GF’s latest silicon photonics manufacturing process that will be available by request at **ayarlabs.com/starterkit**

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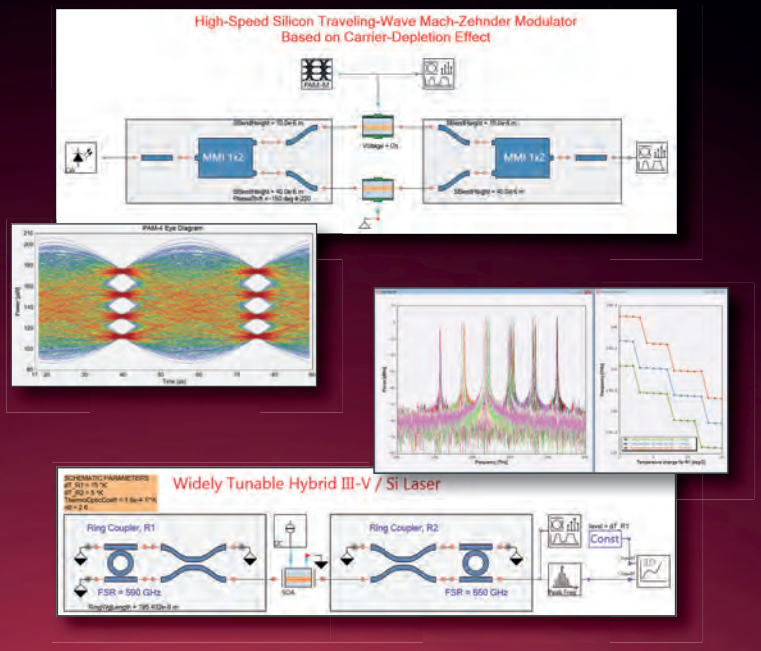

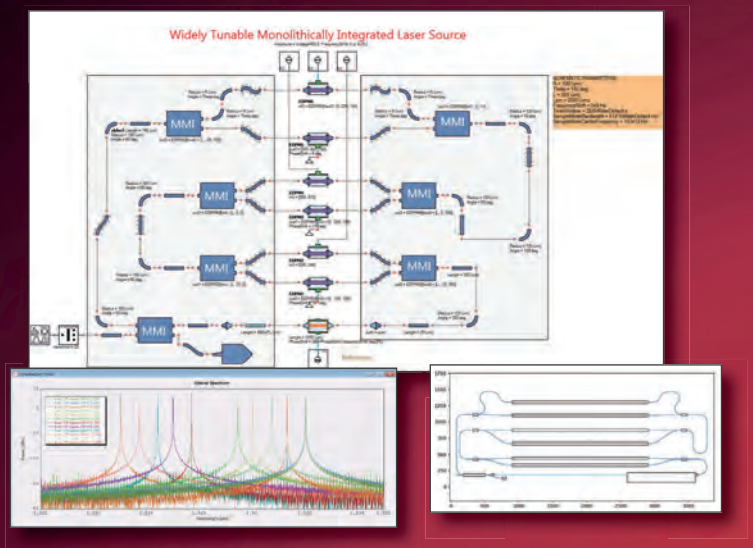

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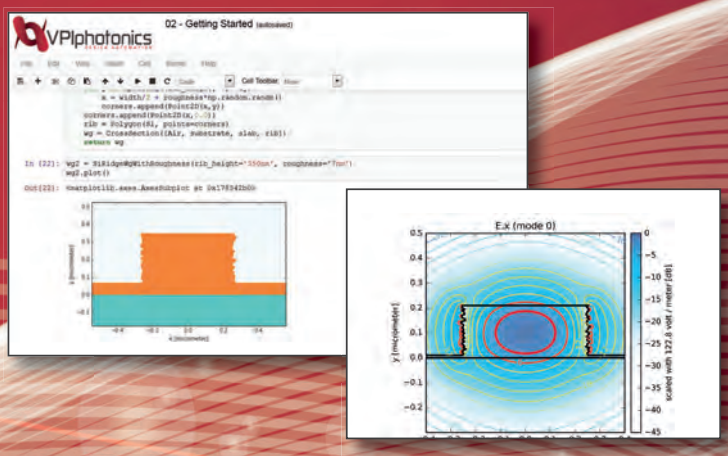

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