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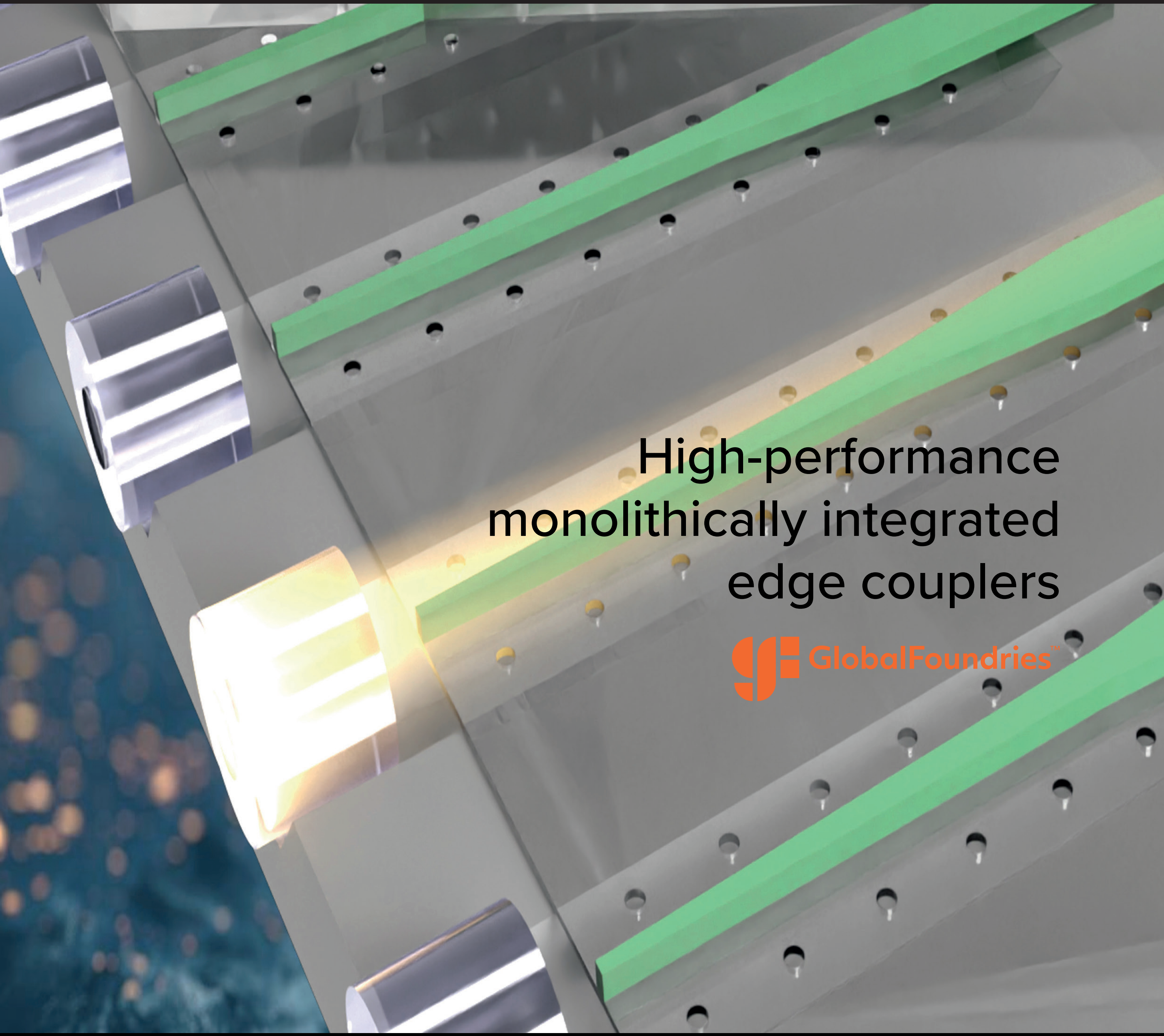

High-performance monolithically integrated edge couplers

GlobalFoundries™

ISSUE I 2023

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

PICMAGAZINE.NET

INSIDE

News Review, Features, News Analysis, Profiles, Research Review and much more...

Accelerating photonics with short R&D

The transition from electronic to PICs, is a breakthrough in cost and cycle time of the manufacturing process

Building phononic integrated circuits with GaN

The ability to guide high-frequency sound around a semiconducting chip positions GaN as a promising platform

Getting photonic crystal nano-lasers on silicon

Demonstrations of photonic crystal lasers on a silicon platform show the tremendous potential of these devices

VIEWPOINT

By Jackie Cannon, Publisher & Acting Editor

PIC International 2023: Unveiling the Future of PiC Innovation

AS WE prepare to publish this edition of PIC Magazine, the countdown to AngelTech 2023 and PIC International is well underway. This unique three-in-one conference event is just weeks away, offering the latest updates from industry leaders and showcasing innovations with the potential to transform your business, all in a single, convenient location.

This year's PIC International will gather representatives from top companies across the photonics ecosystem. Attendees can also expect to gain valuable insights from prominent industry analysts, shedding light on the evolving landscape of PIC design, development, and manufacturing. Over 30 expert speakers will cover a broad range of PIC-related topics, providing practical and actionable insights aimed at optimizing business success for attendees.

In this issue of PIC Magazine, researchers from GlobalFoundries share their recent progress in monolithically integrated, high-performance edge coupling solutions, featuring V-groove based fiber attach and cavity-based laser attach through hybrid flip-chip bonding.

We also turn our attention to POET Technologies, a company that has dedicated five years to developing a revolutionary platform technology. Their POET Optical Interposer is now gaining traction as companies like ADVA adopt it to enhance their own product offerings. Additionally, we explore the increasing demand for higher data rates and lower power consumption driving the growth of various photonic integrated circuit (PIC) technologies. Vario Optics suggests that the key to unlocking PIC benefits lies in on-board photonics – specifically, PCB-embedded planar waveguides.

This is an exciting time for PIC advancements, and we eagerly anticipate sharing the latest developments as they emerge at PIC International on April 18-19.

See you in Brussels.

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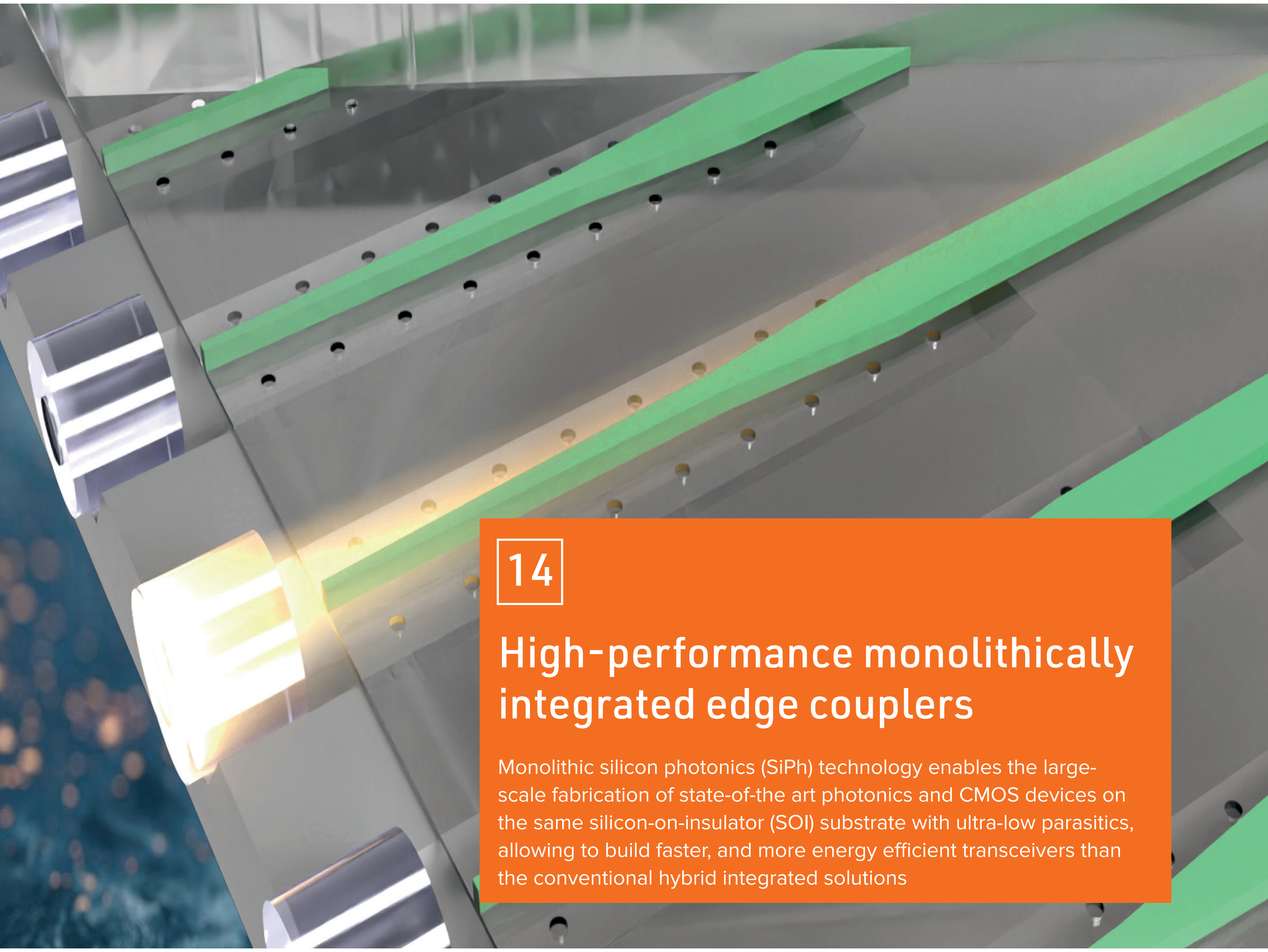

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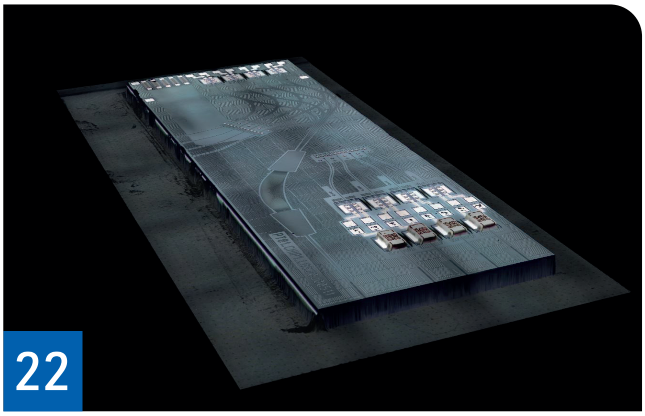

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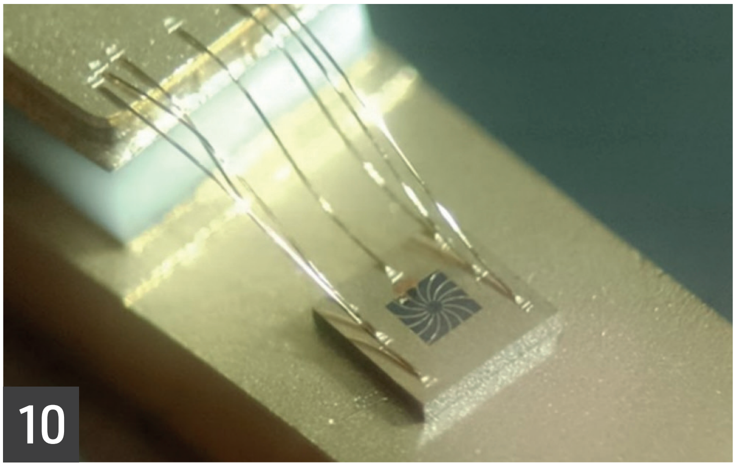

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Publisher & Acting Editor
Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Contributing Technical Editor
Richard Stevenson richard.stevenson@angelbc.com +44 (0)1923 690215
Sales & Marketing Manager
Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
Design & Production Manager
Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

CEO Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970
CTO Scott Adams scott.adams@angelbc.com +44 (0)2476 718970

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Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate, Burnsall Road,
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T: +44 (0)2476 718 970 E: info@angelbc.com

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Tower integrates QD lasers

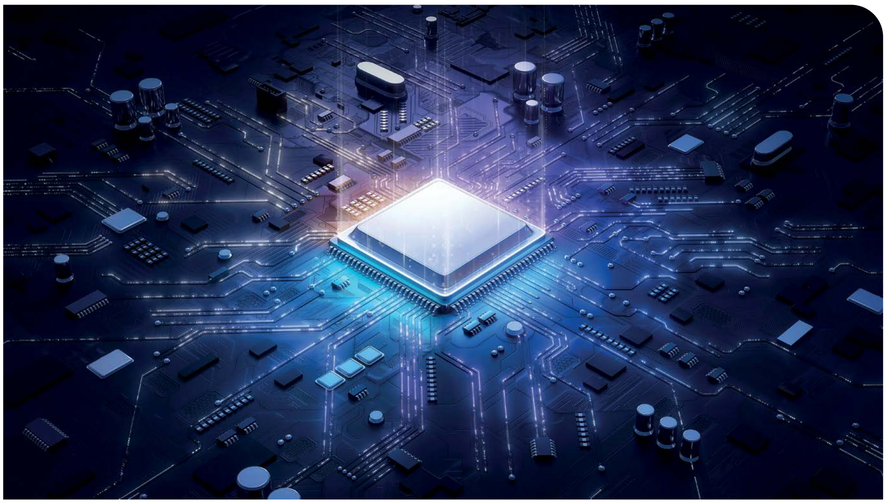
Company achieves heterogeneous integration of GaAs QD laser on high-volume SiPho foundry platform

TOWER SEMICONDUCTOR, in collaboration with Quintessent, has announced the world's first heterogeneous integration of GaAs quantum dot (QD) lasers and a foundry silicon photonics platform (PH18DB).

This PH18DB platform is targeted for optical transceiver modules in data centres and telecom networks, as well as new emerging applications in artificial intelligence (AI), machine learning, LiDAR and other sensors.

The new PH18DB platform offers GaAs based quantum dot lasers and semiconductor optical amplifier (SOA) built on Tower's high-volume base PH18M silicon photonics foundry technology, that includes low loss waveguides, photodetectors, and modulators heterogeneously integrated on a single silicon chip.

According to Tower, this platform will enable dense photonic integrated circuits (PICs) that can support higher-channel count in small form factor.



Open foundry availability of this 220nm SOI platform will provide access to a broad array of product development teams, to simplify their PIC design through use of laser and SOA pcells, in addition to the feature rich baseline PH18 process.

Initial process design kits (PDK) for PH18DB have been made available in partnership with DARPA under the Lasers for Universal Microscale Optical Systems (LUMOS) program, which aims to bring high-performance lasers to advanced photonics platforms for commercial and defense app lications, and MPWs are planned for 2023 and 2024.

This PH18DB platform complements Tower's previously announced, and now prototyping, PH18DA platform that offers heterogeneously integrated InP lasers, modulators and detectors.

This work was funded, in part, by the US Government under the DARPA LUMOS program.

ELPHiC samples EML for 224Gb/s per lane data centres

ELPHiC, a developer of new generation InP chips, has announced samples of its high speed electro-absorption modulator laser (EML) for data centre applications for 800Gb/s and 1.6Tb/s modules.

This follows the sampling of its 10G 1271 laser and its integrated PIN-TIA receiver for PON applications that has showed very high reliability.

According to Jim Hjartarson, CEO of ELPHiC: "By integrating key optical and electronic elements on the same InP semiconductor substrate with the analogue amplification circuitry, we create an architectural shift in building optics chipsets that significantly improve performance and power, lower cost, and reduce module form factor. Our patented PIN architecture also allows for sensitivity levels comparable to those of APDs."

Christian Ilmi, VP Worldwide Sales, added: "This revolution for 800G products will be similar to what we saw for the 400G products 4 years ago: moving from an eight-laser product to a four-laser product per module, leading to the subsequent cost reduction. Furthermore, it will enable the module manufacturers to fit eight lasers in a standard 1.6Tb/s module, which is not feasible today with the current laser technology."

Joe Costello, chairman of the board of ELPHiC and Silicon Valley veteran said: "Finally the promise of monolithic integration of optical devices and electronics are coming to market. With the benefits of ELPHiC's technology, the performance of optical links in PON, data centres and other emerging innovative markets will take a giant leap forward".

Avicena and Ams Osram partner on chip-to-chip interconnects

Companies to develop high-volume production of links using densely packed arrays of GaN microLEDs

SUNNYVALE-BASED AvicenaTech has partnered with Ams Osram to develop high-volume manufacturing of GaN microLED arrays for its LightBundle communication architecture.

Avicena's LightBundle links use densely packed arrays of GaN microLEDs to create highly parallel optical interconnects with typical throughputs of > 1Tb/s at energies of < 1 pJ/bit. A LightBundle cable uses a highly multicore multimode fibre to connect a GaN microLED transmitter array to a matching array silicon photodetectors (PDs).

Arrays of hundreds or thousands of LightBundle's microLEDs and PDs are said to be easily integrated with standard CMOS ICs, enabling the closest integration of optical interconnects with electrical circuits.

In addition to high energy efficiency and high bandwidth density, these LightBundle links also exhibit low latency since the modulation format of the individual links is simple NRZ instead of PAM4 which is common in many modern optical links but has the disadvantage of higher power consumption and additional latency.

The need for next generation computing power is here, driven by strong AI/ML and HPC application demand – for products like ChatGPT, DALL-E, autonomous vehicle training, and many others. Attempts to scale current architectures are running headlong into physical limits leading to slower throughput growth, power-hungry and hard to cool systems.

Avicena says its LightBundle architecture breaks new ground by unlocking the performance of xPUs, memory and sensors – removing key constraints of bandwidth and proximity while simultaneously offering an order-of-magnitude reduction in power consumption.

"We acquired our fab from Nanosys in October to accelerate our development efforts and support low-volume prototype manufacturing," says Bardia Pezeshki, founder and CEO of Avicena.

"However, we are addressing very sizeable markets requiring high-volume manufacturing. We are very pleased to partner with one of world's top GaN LED companies to provide a path to satisfy the expected high volumes required by our customers, including hyperscale datacenter operators and the world's leading IC companies."

"Avicena's LightBundle technology provides an opportunity for GaN microLEDs to impact numerous key applications including HPC, AI/ML, sensors, automotive and aerospace," says Robert Feurle, executive VP and managing director, OS Business Unit at Ams Osram. "As a global leader in GaN LEDs, we are excited to partner with Avicena to transform these very large and important markets."

Jabil's Photonics introduces 800G active optical cable

Jabil has announced that its photonics business unit is expanding its design, manufacturing, and testing capabilities, culminating in the launch of a new Active Optical Cable (AOC) family.

AS A RESULT, Jabil is uniquely positioned to address the rapid pace of advancements in optics-enabled network and data center architectures while supporting the continuing surge of artificial intelligence (AI), cloud, high-performance computing (HPC), and machine learning (ML) applications. Jabil will be showcasing its advanced photonics solutions at OFC'23 in San Diego (Booth #3425).

"Jabil's investments in key enabling technologies and world-class facilities are driving the availability of game-changing photonics solutions and capabilities," said KW Hoo, vice president of the photonics business unit, Jabil. "With the introduction of our 800G AOC family, we meet immediate needs for low-cost, high-performance, short-distance interconnects. Jabil's ability to push the boundaries of photonics technology is backed by strong product design, precision manufacturing, and packaging services that advance optical communications excellence on behalf of our global customers and valued partner ecosystem."

The first product in Jabil's new AOC family is available in two configurations to offer data center operators increased deployment flexibility. The first configuration supports point-to-point communications at speeds up to 800Gbps over distances of up to 100 meters. A breakout-cable configuration also is available, which connects a single 800Gbps interface with two 400G QSFP-DD modules. The breakout cable is ideally suited to connect next-gen switches operating at 800Gbps with existing ports operating at 400Gbps without requiring additional conversion or mapping. The new 800G AOC product will be available in both QSFP-DD and OSFP form factors.

In addition to decreasing deployment requirements and costs, Jabil's AOC offering delivers significant performance and efficiency benefits using Vertical Cavity Surface Emitting Laser (VCSEL) technology operating at 100Gbps per fiber and 800G PAM4 Digital Signal Processing (DSP) technology. VCSEL is gaining traction rapidly for its ability to address the rigorous requirements of demanding applications, including short-reach, high-speed optical communications, 3D sensing, and facial recognition. In addition to elevated performance, Jabil's AOC solution offers seamless compatibility with a vast range of Ethernet switch designs.

Jabil's first 800G AOC product will be available during the second half of 2023. Development is underway on 400G AOC products to extend the AOC product line while accommodating a wide range of applications.

Through its photonics business unit, Jabil empowers organizations to reduce the complexities of developing and deploying enhanced optical networking solutions by offering complete photonics capabilities and competencies encompassing component design, system assembly, and streamlined supply chain management. To that end, Jabil is expanding its large-scale manufacturing and advanced photonics packaging capabilities, including die bonding, flip chip, ball attachment, and fiber alignment. These extended capabilities complement Jabil's design and manufacturing of optical modules, subsystems, and photonics solutions.

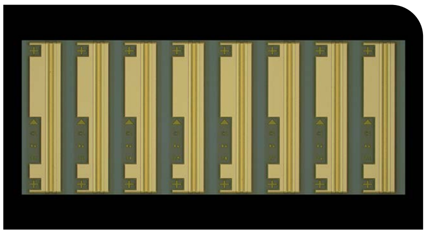
Coherent's DFB lasers enable 400G to 1.6T transceivers

Coherent has announced a 1300 nm high-power continuous wave (CW) distributed feedback (DFB) laser diodes for silicon photonics-based datacom pluggable transceivers.

The high power CW DFB laser diodes enable 400G to 1.6T silicon photonics-based transceivers, which are among the transceiver technology platforms deployed in the data centre mid-reach range of 500 m to 2 km.

"Coherent continues to advance the state of the art in InP semiconductor laser technology that will enable the cloud to continue to rapidly and sustainably scale capacity," said Kou-Wei Wang, VP and general manager, InP & Integrated Circuits Business Unit. "While our new lasers are ideally suited for today's high-speed silicon photonics-based pluggable transceivers, including our own designs, they are also perfect for future co-packaged optics applications."

The new lasers achieve 100 mW of output power when uncooled and 300 mW of output power when cooled,



to enable 100 Gbps and 200 Gbps per lane, respectively, for DR4 and DR8 transceivers. They are available in four coarse wavelength division multiplexing (CWDM) wavelengths for FR4 transceivers.

Advancing quantum photonics with transfer printing

Transfer printing produces CMOS-compatible integration of a silicon platform with quantum-dot single-photon sources

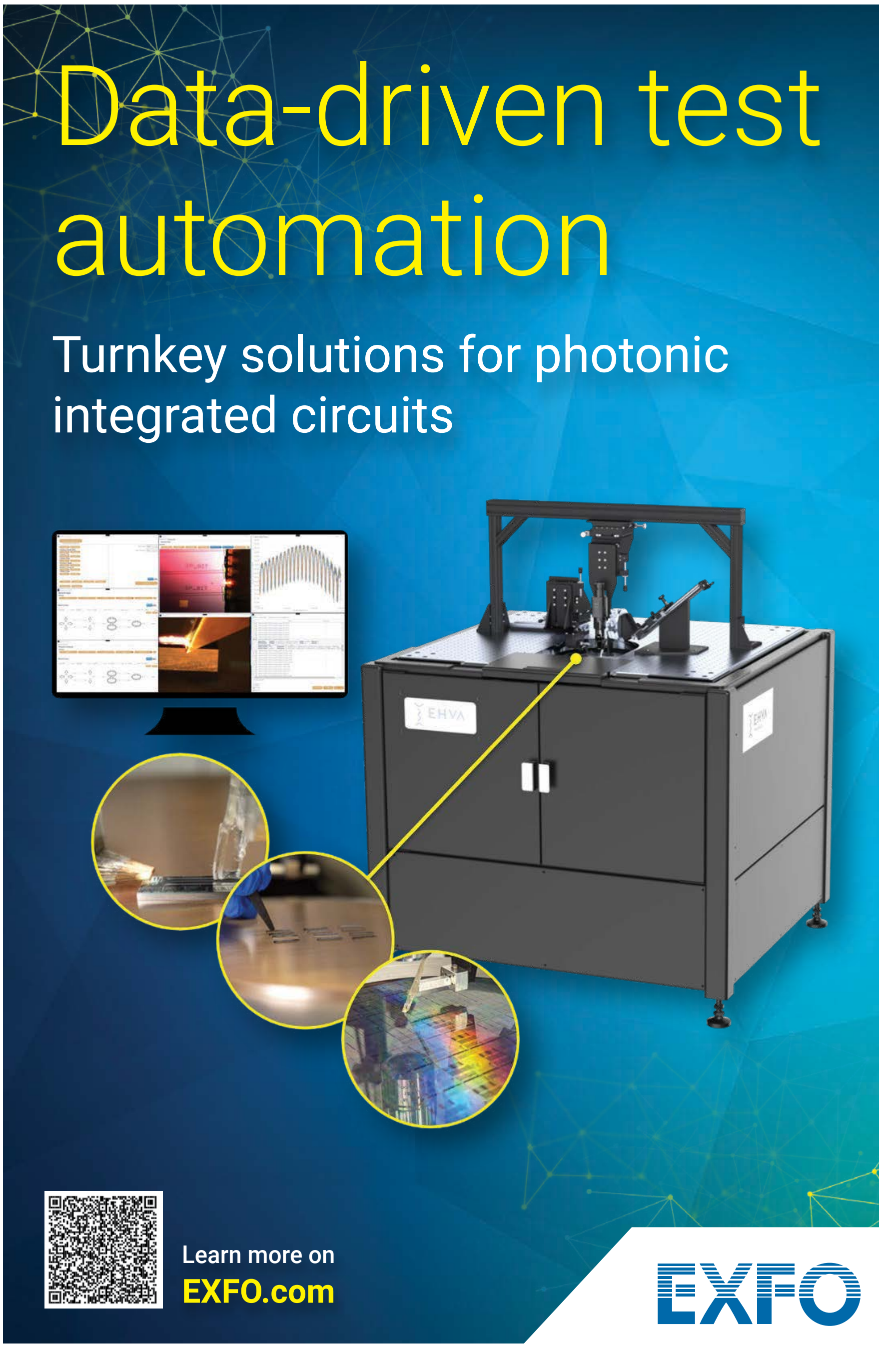
A COLLABORATION between researchers in Japan and Germany is claiming to have broken new ground in the integration of single-photon sources and silicon photonic integrated circuits. According to the team, they are the first to unveil hybrid integration of quantum-dot single-photon sources in the telecom band with silicon photonic integrated circuits made in silicon foundries.

This advance by engineers from a number of institutions – Toyohashi University of Technology, The University of Tokyo, Keio University, The University of Electro-Communications and the University of Kassel – promises to aid the construction of large-scale quantum photonic integrated circuits. Such circuits could be used for quantum simulation, quantum communication and quantum machine learning.

Options for providing single-photon sources for quantum circuits include III-V quantum dots, colour centres in diamond and SiC, and defects in two-dimensional materials. Of these, there's much merit in InAs/InP quantum dots, according to team spokesman Ryota Katsumi, who is affiliated to Toyohashi University of Technology and The University of Tokyo.

Katsumi told Compound Semiconductor that quantum dots are ideal for meeting the requirements for single-photon sources, which include bright single-photon emission, high purity, deterministic operation and high indistinguishability. "It is difficult for other single-photon sources to perform all of these requirements at once."

The team's latest triumph builds on previous successes, including using transfer printing to realise the hybrid integration of InAs/GaAs quantum-dot single-photon sources on a CMOS-processed chip. For that work, the sources produced emission outside conventional communication bands. By now moving to the O and L bands via the switch from dots on GaAs to those on InP, the researchers are benefitting from low loss and low dispersion propagation through optical fibre – this is advantageous for long distance and secure quantum networks.



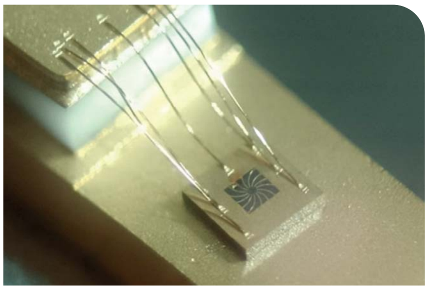
Vector Photonics to commercialise an uncooled, 1 Watt, 1310nm, CW PCSEL

The datacoms PCSEL is for the interconnects, silicon photonics and CPO used in next-generation, cloud datacentre applications.

A 1-WATT LASER offers significant, optical power increases over incumbent DFB technology, with countless manufacturing and energy saving benefits. The 1 Watt laser leverages Vector Photonics' existing PCSEL commercialisation work.

Dr. Richard Taylor, CTO of Vector Photonics, said, "An uncooled, 1 Watt PCSEL is a game-changer for cloud datacoms applications. Currently, next-generation datacentre interconnects must deliver 800Gbps, increasing to 1.6 Tbps and then 3.2 Tbps over the next decade.

The 1 Watt PCSEL enables this development, with a significant reduction in the quantity of lasers required over DFB technology. The interconnects, silicon-photonics chips and CPO systems, where they are used, become significantly easier to make, with the likelihood of improved yield and reliability. In addition, the 1 Watt PCSEL has a symmetrical far-field which requires less operational power to achieve the necessary performance.



"The full impact of a 1 Watt PCSEL is yet to be quantified. However, these high-power lasers will change the entire architecture of datacoms chips and systems. Further, significant benefits include reduced power consumption, heat, latency, and manufacturing costs."

Picocom and Antevia collaborate on 5G in-building solutions

PICOCOM, the 5G Open RAN baseband semiconductor and software specialist, have announced Antevia Networks has selected Picocom's award-winning silicon technology to empower its new innovative 5G in-building solutions. The partnership combines Antevia Networks' technology with Picocom's latest generation 5G system-on-chip silicon to drive innovations to address the many challenges of deploying indoor 5G private networks. The all-new Antevia Networks 5G solution delivers a cost-effective 5G private network deployment that enables intelligent routing of coverage and capacity within buildings or campuses to accommodate variable demand or simply to provide highly reliable 5G connectivity.

"Antevia Networks is pioneering a new class of 5G private network coverage for enterprises worldwide. In working together with Picocom, their state-of-the-art 5G silicon and collaborative approach is allowing us to innovate faster, reach the market sooner and deliver groundbreaking solutions for enterprises needing cost-effective 5G private networks," said Simon Cosgrove, CEO of Antevia Networks.

"I have been very impressed by the way that Antevia Networks has taken Picocom's Open RAN O-DU and O-RU components and built a truly innovative solution for indoor coverage, built on the standard open interfaces defined by the O-RAN Alliance", said Peter Claydon, President of Picocom. "This is a great illustration of how Open RAN enables network operators to create highly differentiated products on top of the building blocks that Picocom's flexible silicon provides."

Antevia Networks' approach to 5G in-building private networks revolutionises the RAN design, which improves coverage, capacity and service robustness whilst keeping the costs low enough to make it affordable for enterprise. PC802 is shipping in mass production quantities together with mature software for Open RAN Distributed Units (O-DU) and Radio Units (O-RU), as well as integrated small cells. In addition, PC802 supports both 4G LTE and 5G NR.

POET and Beijing FeiYunYi sign optical engine deal

POET to design optical engines for telecoms module markets, beginning in China

CANADIAN PIC company POET Technologies has announced an agreement with Beijing FeiYunYi Technology Ltd. (BFYY) to design optical engines for deployment in optical modules in the telecom market globally, beginning in China.

The agreement, valued at up to $1 million over a two-year period, includes NRE for POET and an initial purchase order for 10,000 units that will be used to sample customers.

BFYY was recently formed for the purpose of selling modules using POET-designed optical engines sourced from POET's joint venture company, Super Photonics Xiamen (SPX). BFYY is investing in assembly facilities to build, market and sell modules that will be competitive in the data center market, specifically focused on large telecom service providers.

POET has agreed to design a single-chip optical engine solution, that incorporates complete transmit and receive functionalities for implementation in a 100G optical transceiver for BFYY's initial product offering. POET says that the single-chip solution, called POET ONE, will offer significant performance advantages along with minimising the transceiver design cycle time for BFYY.

In addition to the cost benefits of POET's wafer-scale assembly, the single-chip solution will enable BFYY to cost effectively ramp to high-volume production. BFYY has forecasted optical engine purchases from SPX at over $30 million over a three-year period.

"The number of 5G and Fibre-to-the-Home (FTTH) subscribers in China is growing considerably. To keep up with the bandwidth demand several major service providers are exploring ways to transform their networks," said Wei Zhang (Wesley Zhang), CEO of BFYY.

"Top tier service providers in China believe that transceivers with POET's Optical Interposer technology can provide a cost effective and scalable solution to achieve their network automation goals. BFYY plans to utilise its transceiver design and manufacturing capabilities along with the benefits of POET's integration platform to quickly ramp to high volume production."

"We are excited to work with BFYY on this initial product and plan to leverage their capabilities and business relationships with service providers to be part of the network transformation journey in China. We will continue to offer differentiated solutions to our customers for high-speed optical communications in data and tele-communications markets," said Vivek Rajgarhia, president and GM of POET and vice-chairman of SPX.

Vector to commercialise PCSEL for next-gen data centres

VECTOR PHOTONICS will begin commercialisation of an uncooled, 1 Watt, 1310nm, CW PCSEL. The datacoms PCSEL is for the interconnects, silicon photonics and CPO used in next-generation, cloud data centre applications.

A 1-Watt laser offers significant, optical power increases over incumbent DFB technology, with countless manufacturing and energy saving benefits. The 1 Watt laser builds on Vector Photonics' existing PCSEL commercialisation work.

Richard Taylor, CTO of Vector Photonics, said: "An uncooled, 1 Watt PCSEL is a game-changer for cloud datacoms applications. Currently, next-generation datacentre interconnects must deliver 800Gbps, increasing to 1.6 Tbps and then 3.2 Tbps over the next decade. The 1 Watt PCSEL enables this development, with a significant reduction in the quantity of lasers required over DFB technology.

'The interconnects, silicon-photonics chips and CPO systems, where they are used, become significantly easier to make, with the likelihood of improved yield and reliability. In addition, the 1 Watt PCSEL has a symmetrical far-field which requires less operational power to achieve the necessary performance.

"The full impact of a 1 Watt PCSEL is yet to be quantified. However, these high-power lasers will change the entire architecture of datacoms chips and systems. Further, significant benefits include reduced power consumption, heat, latency, and manufacturing costs."

iPronics announce first shipments of reprogrammable photonic microchips

iPronics, the first company to develop plug-and-play, programmable photonic microchips, has announced that it has successfully delivered initial shipments to several companies in distinct sectors.

THE iPronics SmartLight Processor improves processing capabilities and moves data at the speed of light. A photonic microchip uses up to 10x less power and can be 20x faster than electrical chips while processing far more information.

This new processor allows the reconfiguration of a common photonic hardware platform through user-friendly software. This is the first-in-class fully programmable photonic chip, as previous photonic integrated circuits have been fixed-function or application-specific in operation.

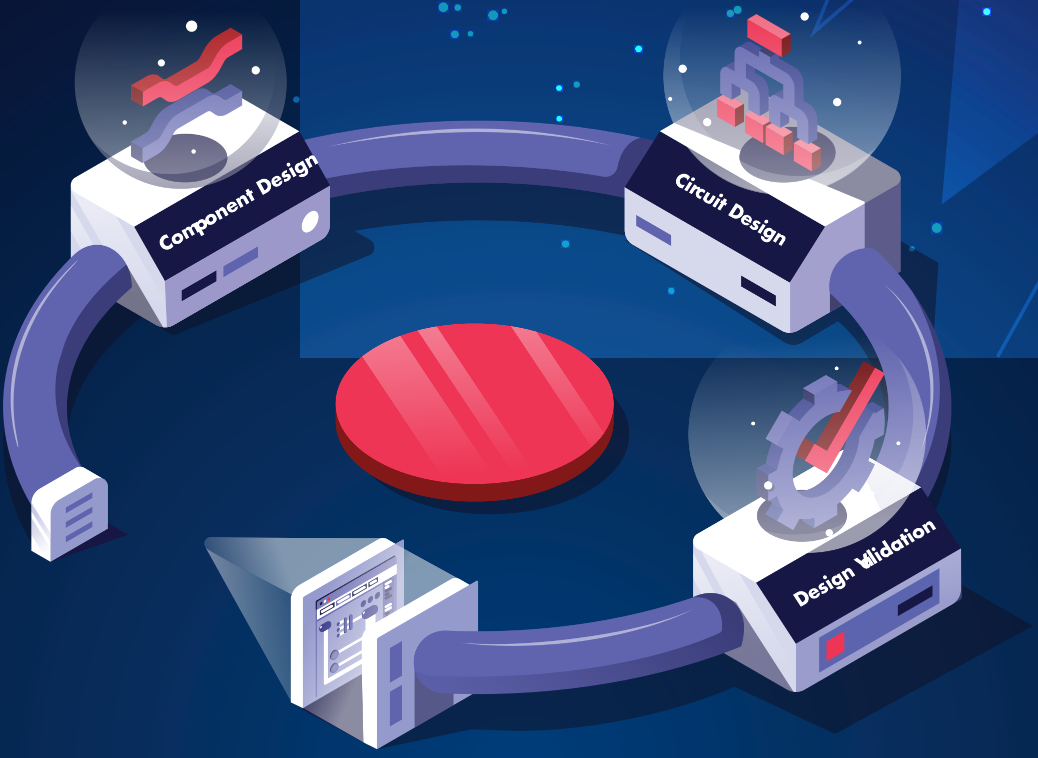
The new product has many applications throughout emerging markets and technologies, including 5G/6G signal processing, data centres, machine learning, AI, and computing. The programmable nature of this technology unlocks novel commercial applications as it allows the generation of optical functionalities in software, which critically reduces time to market and total costs for system design, prototyping, and production. iPronics' chips have been dispatched to customers in the US and Europe, including a multinational telecommunications and electronics company, a European-based optical networking company and a large US technology company.

The iPronics SmartLight Processor stands out from the crowd, as its photonic chip has significant time-to-market and cost benefits. Compared to custom photonic ICs, the development time can be cut from 18 months down to a couple of weeks.

This lowers the total cost and mitigates risk for iPronics' clients while delivering on the promise of photonic processing: lower power consumption, lower latency, and faster computation. The iPronics SmartLight Processor enables innovative tech companies to continue their cutting-edge silicon photonics work on several fronts such as high-speed optical communications, RF photonics, and neuromorphic computing.

Mark Halfman, iPronics CEO, commented: "For a company that was founded just prior to the pandemic, it is almost unprecedented to move so swiftly from development to shipping our first commercial orders supporting a variety of applications."

"Today's announcement is a testament to the vision of the company's founders and the dedication of the entire team. This is both a watershed moment for the photonics industry and an exciting time for the company."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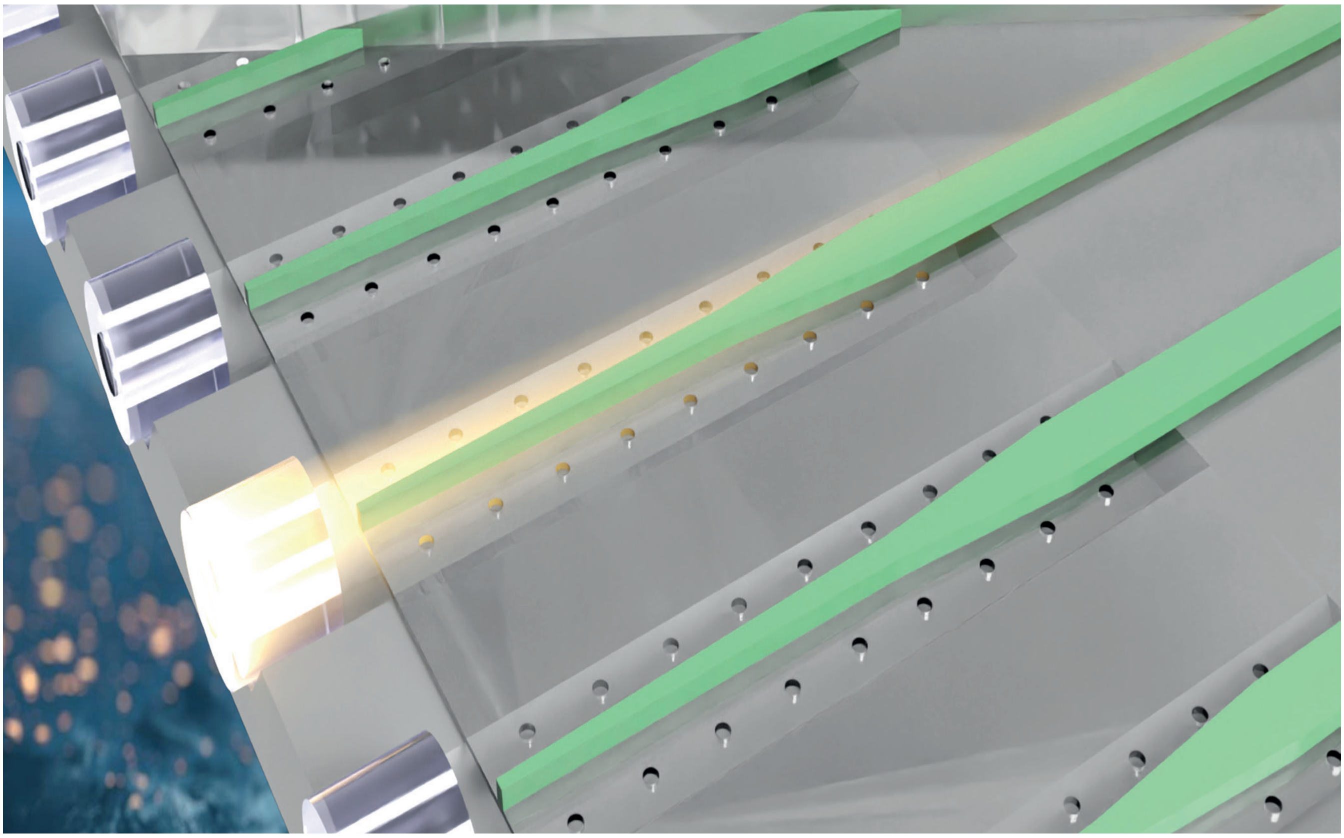


High-performance monolithically integrated edge couplers

Monolithic silicon photonics (SiPh) technology enables the large-scale fabrication of state-of-the art photonics and CMOS devices on the same silicon-on-insulator (SOI) substrate with ultra-low parasitics, allowing to build faster, and more energy efficient transceivers than the conventional hybrid integrated solutions. The realization of scalable, cost-effective and power-efficient optical inputs/outputs (I/Os) on the monolithic SiPh platform remains a significant challenge. In this article, GlobalFoundries researchers report on recent advances in their monolithically integrated high-performance edge coupling solutions, including V-groove-based fiber attach and cavity-based laser attach leveraging hybrid flip-chip bonding.

BY YUSHENG BIAN, TAKAKO HIROKAWA, KOUSHIK RAMACHANDRAN, KAREN NUMMY, KEN GIEWONT AND TED LETAVIC, GLOBALFOUNDRIES

THE EVER-INCREASING DEMAND in global data communication is driving the emergence of low-cost, disruptive interconnect solutions that can simultaneously meet the energy consumption, bandwidth and throughput requirements. SiPh based optical interconnection technology has been widely recognized as a key enabler to overcome the power and bandwidth capacity bottlenecks encountered by its electrical counterparts [1].

The well-established complementary metal oxide semiconductor (CMOS) manufacturing infrastructure, along with many intrinsic advantages of Si material such as high refractive index and optical transparency, has rendered SiPh a viable solution towards high-performance, cost-effective, and mass-manufacturable photonic integrated circuits (PICs).

Moreover, the ability to implement wavelength division multiplexing and advanced modulation schemes, in conjunction with high performance electronic components and CMOS-compatible materials onto the SiPh platform has further enabled unprecedented bandwidth scalability and naturally led to complex photonic systems suitable for a variety of applications such as datacom, telecom, automotive LiDAR, artificial intelligence, quantum computing and bio-chemical sensing.

Monolithic SiPh platform

Among the existing SiPh solutions that have been demonstrated so far, monolithic SiPh technology has been identified as one of the most promising candidates to simultaneously meet the scalability, power consumption and cost efficiency demands for the next generation optical interconnection schemes [2]. By enabling the large-scale fabrication of state-of-the art photonics and CMOS devices on the same SOI substrate, monolithic SiPh technology holds great potential for ultra-low parasitic integration [3], and allows to build faster, and more energy efficient transceivers than the conventional hybrid integrated solutions leveraging 2.5D or 3D packaging [4].

Fig. 1 shows the cross-section of a representative monolithic CMOS SiPh platform. By leveraging dual Si thicknesses and dual contact modules, this platform enables seamless integration of the best-in-class active and passive photonic devices with high-speed CMOS transistors. The front end of line (FEOL), middle of line (MOL) and back end of line (BEOL) of the stack-up are co-optimized for both photonics and electronics, while satisfying stringent integration requirements and maintaining excellent fabrication fidelity for all the pre-existing devices with varying feature sizes. The RF-friendly BEOL stack is highly attractive for building complex logic circuits, high-Q inductors and low-loss transmission lines, while simultaneously serving as high-quality contact interfaces for advanced active photonic devices.

The incorporation of silicon nitride (SiN) material has further enriched the capability of the monolithic SiPh platform [5]. Benefiting from the optimized stack-up and integration flow, low-loss and robust SiN passive photonic components can be realized, with extended capabilities in nonlinear loss mitigation, high power handling and thermal stabilization. Moreover, the combination of Si and SiN waveguides (WGs) provides additional degrees of design freedom to enable a variety of advanced devices featuring expanded functionalities such as low loss waveguiding, efficient polarization management, compact interlayer transition, high performance edge and vertical coupling with optical fibers, to name a few [6].

Monolithically integrated fiber attach solution

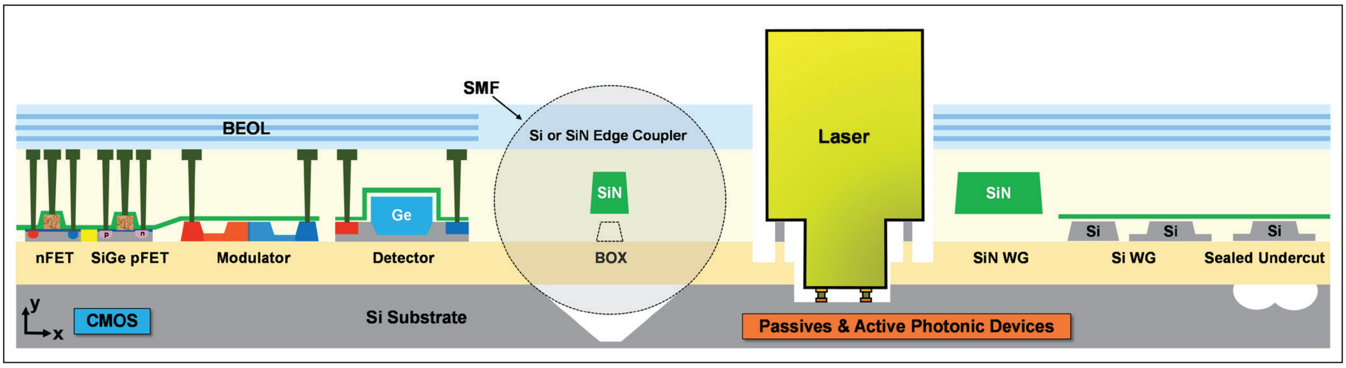
A high-performance optical I/O interface that allows for the efficient coupling with a standard single mode fiber (SMF) or fiber array has been recognized as a key enabler to improve the scalability and cost efficiency of SiPh interconnects. To realize robust and highly efficient fiber to PIC coupling on the monolithic platform, advanced crystallographic etch module and state-of-the-art 300mm manufacturing processes are adopted to form high quality V-grooves with high structural yield that allow high accuracy fiber attach with passive alignment.

To enable efficient coupling between the SMF and edge coupler (EC) while preventing mode leakage into the substrate, the BEOL cladding above the spot size converter (SSC) is replaced with a thick, homogeneous dielectric layer, and the Si substrate underneath is partially removed and filled with index matching liquid during the measurement (See Fig.1 and Figs.2 (a)-(b)).

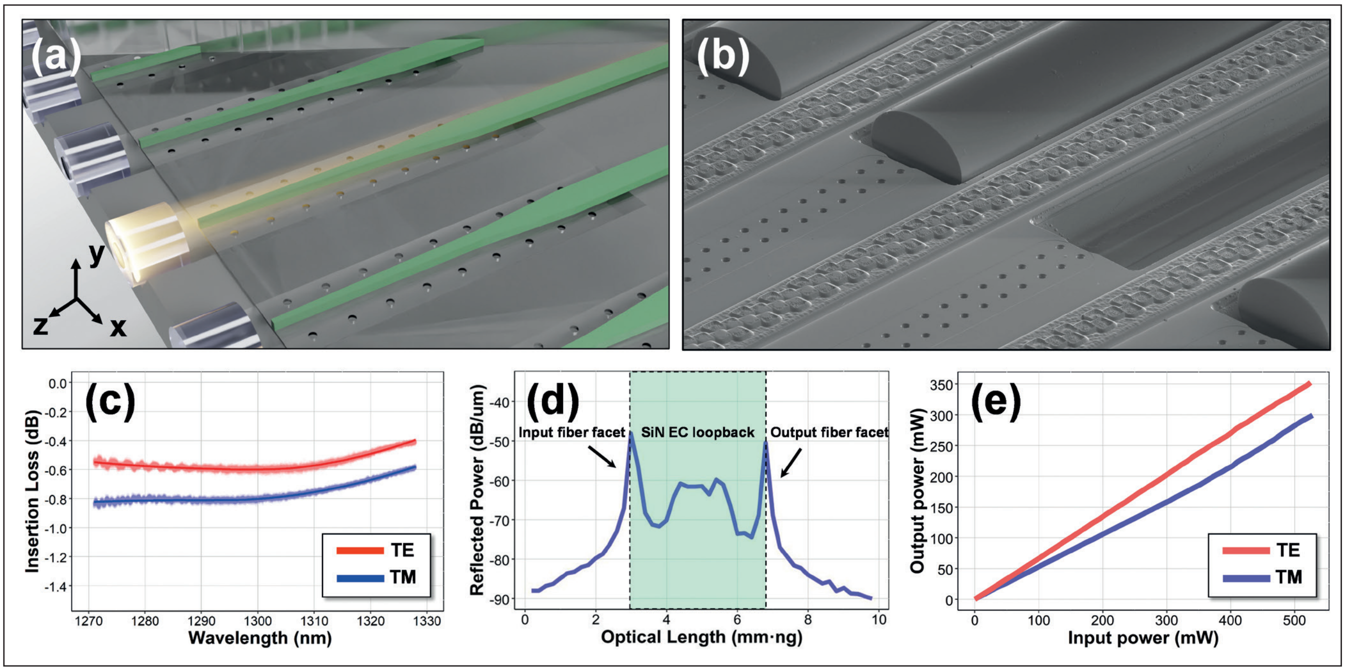
At OFC2020, we reported the demonstration of low-loss fiber attach on our monolithic SiPh platform, which leverages Si metamaterial SSCs to significantly improve the fabrication and assembly tolerances over traditional designs using solid inverse tapers [7]. Statistical data of the insertion losses (ILs) and early reliability assessment results were presented for two types of edge couplers (i.e. low optical return loss (ORL) and low polarization-dependent loss (PDL) SSCs), which are optimized for the transmitter and receiver circuits, respectively.

As SiPh begins to penetrate various emerging areas such as LiDAR and quantum computing, the ability of an optical I/O to handle high optical power while maintaining other performance metrics becomes increasingly important to address the unprecedented demands in performance scaling and power consumption reduction.

These challenging requirements call for an alternative SiPh I/O solution other than the conventional EC schemes utilizing Si because Si as a material inevitably suffers from nonlinear effects that can potentially cause irreversible physical



➤ Figure 1. Monolithic SiPh platform simultaneously integrating advanced photonic devices and CMOS components on the same SOI substrate.



➤ Figure 2. Monolithically integrated fiber attach solution. (a) 3D perspective view of SiN ECs. (b) SEM image of a V-groove array attached with SMFs. (c) Through-band insertion loss. (d) OFDR spectrum. (e) High power measurement results.

damage and excess loss at high optical power. Recently, by leveraging the SiN WG layer in the stack-up and incorporating additional process optimizations along with advanced free-form optical proximity correction, we realized for the first time, a low-loss, V-groove-based self-aligned SiN EC solution on our monolithic SiPh platform. This work will be presented at OFC 2023 [8].

Figs.2 (c)-(e) depict the measurement results of the SiN EC, which were extracted from a V-groove-based test structure comprising two ECs and a loop-back SiN WG. Fiber-attached chips using index matching fluid were prepared for both low-power and high-power measurements. With the assistance of a polarization controller to adjust the input polarization, the insertion loss and back reflection of the SiN EC can be measured separately by switching between the transmission and reflection modes of an optical vector analyzer (OVA).

The measured SMF to SSC IL spectrum shown in Fig.2 (c) clearly reveals a reasonable through-band performance over a 60 nm bandwidth centered at 1300 nm. <0.6 dB/0.8 dB IL for the TE and TM modes, along with a low PDL (<0.28 dB) and low wavelength dependence (<0.24 dB) were achieved simultaneously. Optical Fourier domain reflectometry (OFDR) centered at 1310 nm was then used to measure the back reflection of the loopback structure and the recorded spectra were converted into the spatial domain.

As illustrated in Fig.2 (d), two reflection peaks were observed near the input and output fiber facets. Based on the integrated reflection loss at the input facet, the back reflection at the first SMF-SSC interface was estimated to be less than -39 dB, which is a clear indication of the low ORL of the SiN EC.

Finally, the power handling capability of the EC was evaluated through ramping up the input laser power up to 520 mW. The measurement results shown in Fig. 2 (e) clearly reveals a linear relation between the input and output powers and the high-power tests were repeated to assure that there was no permanent physical damage or power-dependent loss in the PIC. These results further confirmed the robustness of the monolithically integrated SiN EC for high power applications.

> Fiber-attached chips using index matching fluid were prepared for both low-power and high-power measurements. With the assistance of a polarization controller to adjust the input polarization, the insertion loss and back reflection of the SiN EC can be measured separately by switching between the transmission and reflection modes of an optical vector analyzer (OVA)

Laser Attach Solution on the monolithic platform

As an indirect bandgap material, Si lacks the ability to emit light efficiently. The need to overcome such a challenge has led to the advent of various techniques with the aim of integrating other light-emitting materials onto the SiPh platform to enable low-cost and power-efficient on-chip lasers. By leveraging advanced flip-chip bonding techniques and butt-coupling scheme, we demonstrate the hybrid integration of III-V laser on our monolithic SiPh platform. The work was presented at OFC2021 [9] and more recently published on IEEE Journal of Selected Topics in Quantum Electronics as an invited paper [10].

A key feature to enable hybrid laser integration onto the monolithic platform is a precisely controlled laser cavity formed during the far BEOL processing (Fig.1). High-precision alignment of the laser can be realized by taking advantage of precise optical and mechanical features, allowing efficient direct butt-coupling of the laser beam into the SSC (Figs.3 (a)-(d)). This laser attach involves alignment and placement of the laser, followed by a laser-assisted solder reflow process to create p- and n-electrical connections to the laser.

The dimensions of the Si cavity are precisely controlled by using the locations of the SSC and the active multi-quantum-well region of the laser as references. A sub-micron accuracy pick-and-place soldering process enables precise alignment of the laser inside the cavity by utilizing high-precision alignment fiducials on the laser and SiPh chip. Standoff structures incorporating the existing layers are formed within the cavity, which serve as a mechanical stop feature allowing for the accurate vertical alignment of the laser. The metallization step is conducted to form the wiring levels within the cavity and provides lithographically defined solder connections that align and electrically connect with the p and n bottom contacts on the laser. The solder connections within the cavity also provide mechanical support and a thermal pathway for the laser during operation.

One key aspect of this scheme is the formation of a wiring level that steps up from the bottom of the cavity to the surface wiring levels of the PIC that are typically deployed for standard wire-bonding via last-metal bond pads or flip-chip interconnection through copper pillar receive pads. This unique approach enables standard electrical I/O to power the laser in a direct flip-chip configuration inside the cavity without the need for any additional assembly steps such as wire-bonding.

Figs. 3 (e) and 3 (f) show the optical image and SEM of a monolithic SiPh chip incorporating laser cavities and flip-chip-bonded lasers. Figs. 3 (g)-(j) depict the key performance metrics of the laser obtained from a series of wafer-level and module-level electro-optical testing. The coupling performance was evaluated by powering up the laser at 100 mA driving current and measuring the optical power output through both grating couplers and V-groove-based edge couplers.

The testing result shown in Fig. 3 (g) indicates > 14 mW optical power was coupled into the Si WG with the assistance of the inverse taper illustrated

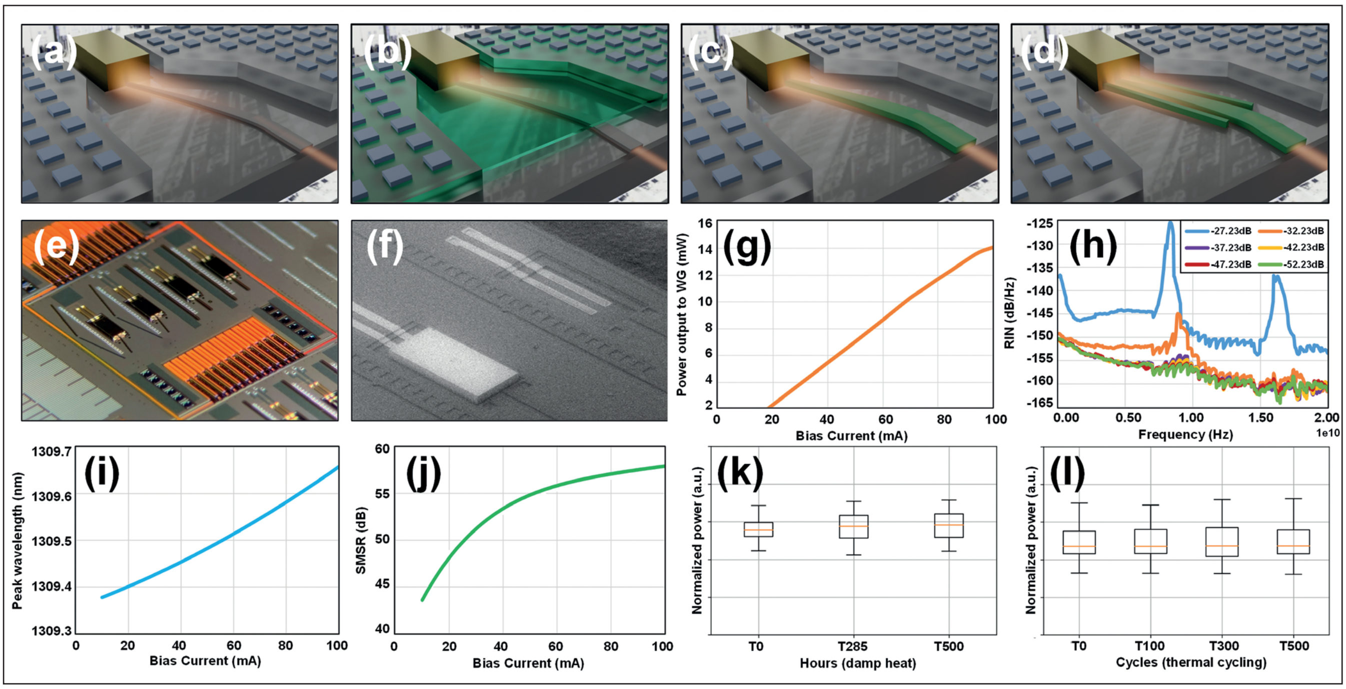
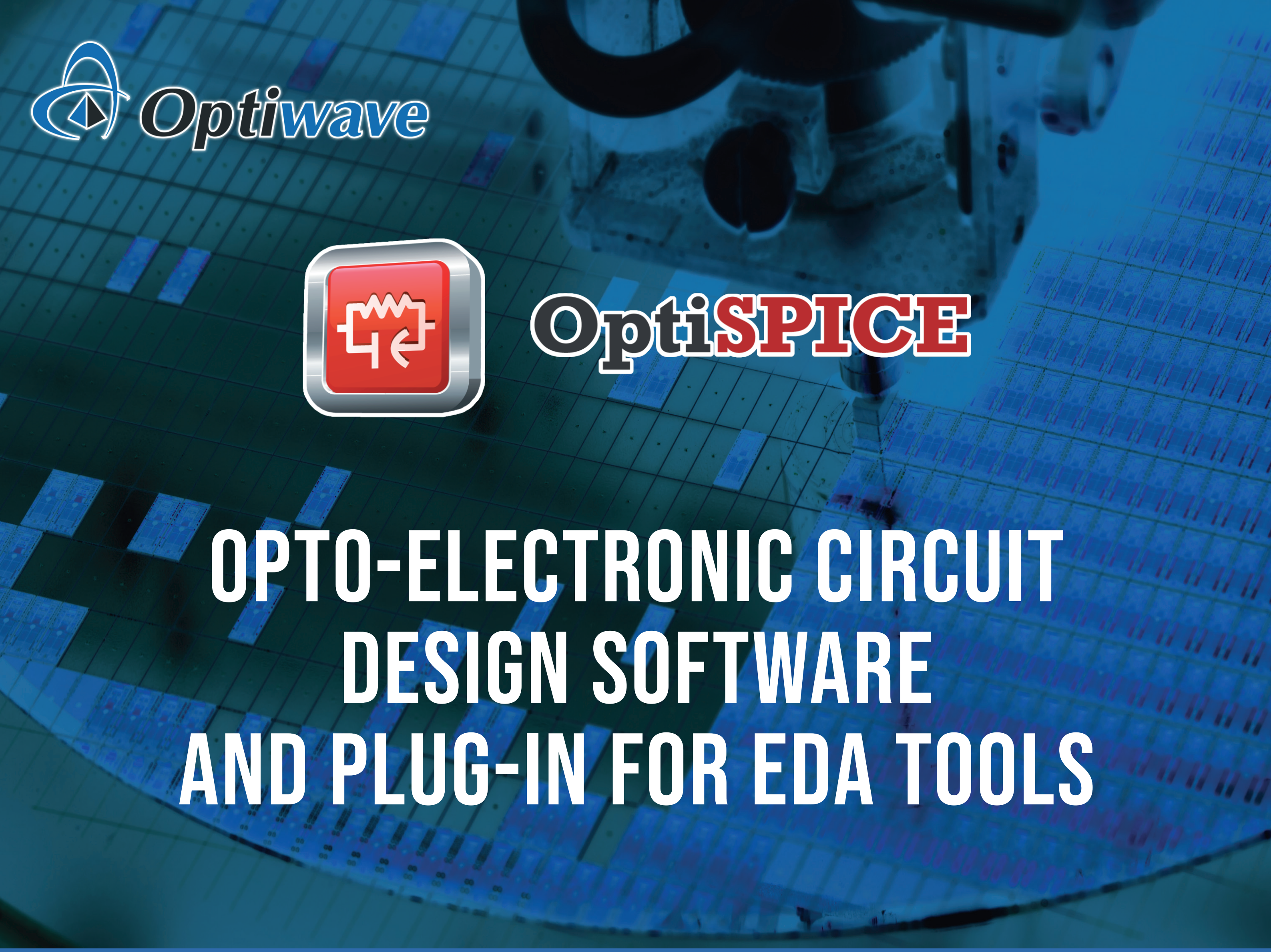
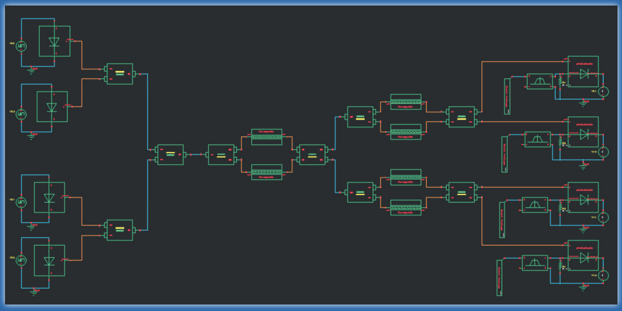
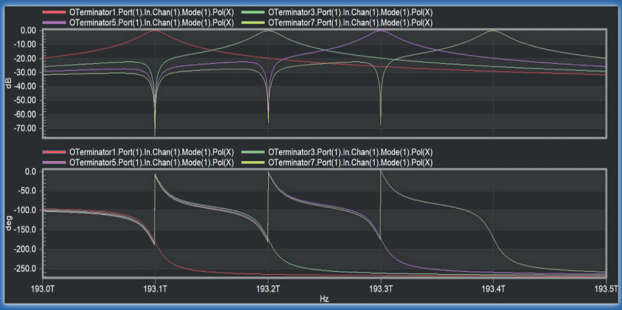


Figure 3. III-V laser integration on the monolithic SiPh platform. (a)-(d) 3D perspective views of various PICs with different SSCs formed on Si or SiN layer. (e)-(f) Optical image and SEM of laser cavities with and without flip-chip-bonded laser. (g)-(j) Light-current curve, RIN, spectral characterization and SMSR performance. (k)-(l) Wafer-level accelerated reliability test results



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in Fig.3 (a). By switching to a stacked Si-SiN SSC design (Fig. 3(b)), over 20 mW output was measured at the WG. The pure-SiN-based alternative SSC options illustrated in Figs.3(c)-(d) are currently being evaluated for high power applications and the results will be reported in the near future.

Fig.3 (h) depicts the measured relative intensity noise (RIN) power spectral density as a function of the frequency for various externally added back-reflections (BRs). The stable laser performance at low levels of BRs and relaxation oscillations observed when power exceeds the laser BR tolerance clearly indicate that components in the optical path within the PIC did not negatively impact the RIN performance of the laser.

The spectral characterization result in Fig. 3 (i) shows the peak wavelength of the laser as a function of the bias current from a mode-hop-free module, indicating no evidence of any wavelength discontinuity. We also confirmed that no mode competition was occurring during the laser operation by monitoring the side-mode suppression ratio (SMSR), which remains above 50 dB in the operating range as illustrated in Fig. 3 (j).

Finally, we performed a series of reliability assessments on laser-attached Si submounts and SiPh cavity test vehicles to understand the long-term performance stability of the PIC [10]. The reliability results shown in Figs.3 (k)-(l) reveals stable performance throughout the stress testing, which further confirms the robustness of the laser integration on the monolithic SiPh platform.

> We performed a series of reliability assessments on laser-attached Si submounts and SiPh cavity test vehicles to understand the long-term performance stability of the PIC

Summary

In this article, we have provided a brief overview of the recent progress that was made in high performance edge coupling solutions on our monolithic SiPh platform, including V-groove-based self-aligned fiber attach leveraging Si and SiN SSCs, and hybrid integration of III-V lasers. The I/O techniques presented here can be readily scalable to an optical source array with high fiber or laser counts as well as fine pitches. Their full compatibility with automated high-throughput microelectronic packaging tools renders themselves as highly attractive candidates for complex photonic systems and co-packaged optical modules.

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Commercialization accelerates for POET Technologies' platform technology

POET Technologies has spent five years striving to deliver a game-changing platform technology to the market. Now, the POET Optical Interposer is gaining adoption as ADVA and others utilize it to improve their own product offerings. Here's why they are convinced of POET's advantages.

BY POET TECHNOLOGIES

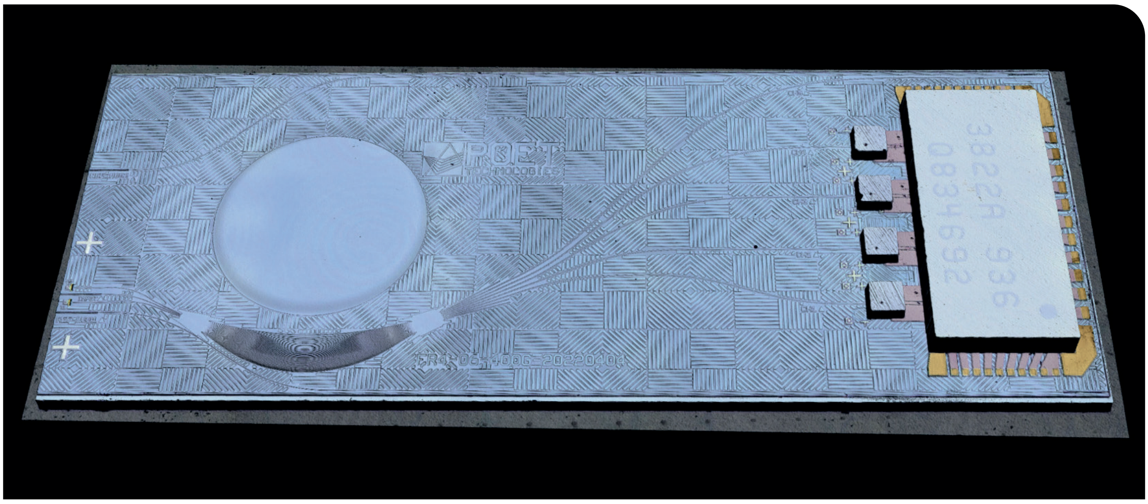
AT POET TECHNOLOGIES, we have been a company of "-ization". We had a goal for the "legitimization" of photonics in the semiconductor industry and built a hybrid-integration solution to deliver on the "optimization" of products built with the proprietary POET Optical Interposer. We have touted "miniaturization" of photonic solutions using wafer-scale assembly as critical to gaining industry attention and the "semiconductorization" of photonics as a description of what our seamless integration of photonics and electronics achieves.

Now, we bring the most exciting suffix of all to the top line of our story: commercialization.

Momentum has steadily grown for our products, which are currently being sampled by customers in data centers, telecommunications, and AI. They're attracted to the POET optical interposer-based solutions that eliminate costly components and labor-intensive assembly, alignment, and testing methods. Those earliest adopters of the technology include:

- **ADVA:** The European network equipment provider (recently merged with AdTran, Inc.) has collaborated with POET on an innovative set of optical engines to extend the life of legacy data center infrastructure while enabling simple migration to next generation speeds.
- **LuxshareTech:** POET's 400G and 800G optical engines will help this global datacom company offer its end customers high-speed transceiver modules.
- **Celestial AI:** The high-powered, well-funded Silicon Valley startup is scheduled to receive alpha samples of POET's C-band Light Engines for high-speed chip-to-chip communications in the first quarter of 2023. Purchase orders are expected later in the year.
- **FiberTop Technology:** The transceiver company plans to leap over its competition with the help of POET's 100G and 200G optical engines in its pluggable transceivers.

What these companies — and others whose names remain shrouded by confidentiality agreements — have realized is that the POET Optical Interposer



➤ The POET Optical Interposer™ is built to scale and to lower costs thanks to its unique chip-on-board packaging solution.

provides market differentiation in four key areas and that gives its suite of products advantages over alternative technologies.

1. Ease of Integration

The capital costs of replacing old equipment to accommodate new technology is always a challenge for companies. Whenever a solution emerges that can extend the life of existing infrastructure, executives are sure to consider the opportunity. That's what happened more than two years ago when POET and ADVA began discussing how to get the most out of 100G ports (which are currently prolific in data centers) and how best to transition the industry to 400G.

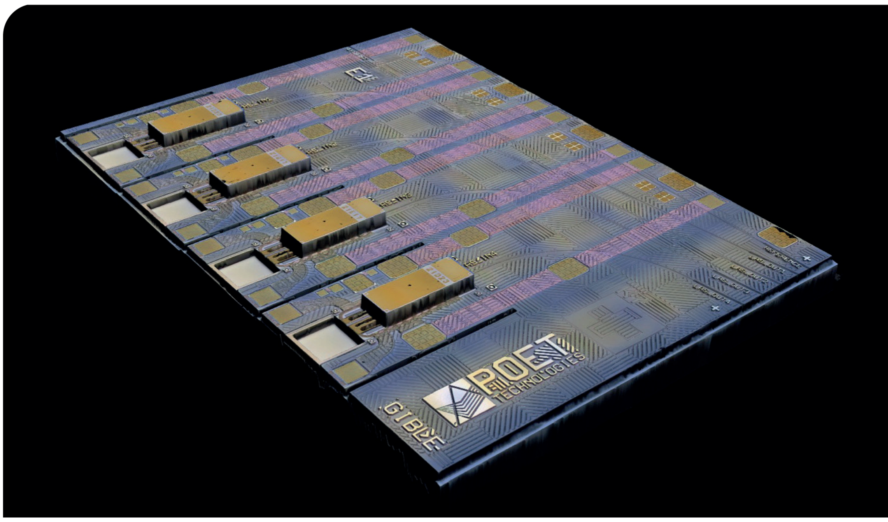
On January 18, POET and ADVA announced a strategic collaboration for optical engines that represent a life extension for a significant number of legacy 100G ports. POET has developed a multi-engine 100G CWDM4 and 100G LR4 optical engine that ADVA will use in its pluggable transceiver solution of four independent 100Gbit/s interfaces into a single 400G transceiver in a QSFP-DD housing.

ADVA's MicroMux Quattro has individual 100G ports in a QSFP-DD package that plugs into a 400G port. Along with fitting into standard sockets, it fans out 4x100GbE, maximizing the use of existing hardware in data centers. The solution creates compatibility to the legacy 100G links without the need for retrofits in network design or the use of additional hardware.

Also, the MicroMux Quattro becomes the industry's smallest pluggable transceiver to pack the functionality of four individual 100G LR4 or CWDM4 optical engines into a single module.
"ADVA's MicroMux Quattro brings the industry's smallest aggregation technology all the way to the network core. Engineered as a standard-compliant plug in a QSFP-DD form factor, it fits into a 400Gbit/s socket, enabling it to meet legacy needs.

This innovative pluggable solution packs the functionality of four independent 100Gbit/s interfaces or two independent 200Gbit/s interfaces into a single QSFP-DD housing," said Ross Saunders, GM of Optical Engines, ADVA, in a press release. "POET's unique design of its optical engines with hybrid integration of optical chips and monolithically integrated MUX and DMUX enables us to deliver industry-leading products in a small form factor that is scalable to high volume production as well as to higher data rates, such as 1.6Tbit/s and 3.2Tbit/s, thereby enabling much higher bandwidth in a pluggable form factor."

It's the most public example of the ease with which POET's products integrate with current systems and equipment, though much of the excitement building for interposer-based optical engines has to do with inherently lower capital and assembly costs — especially at a time when many companies are coming off of a difficult two years.

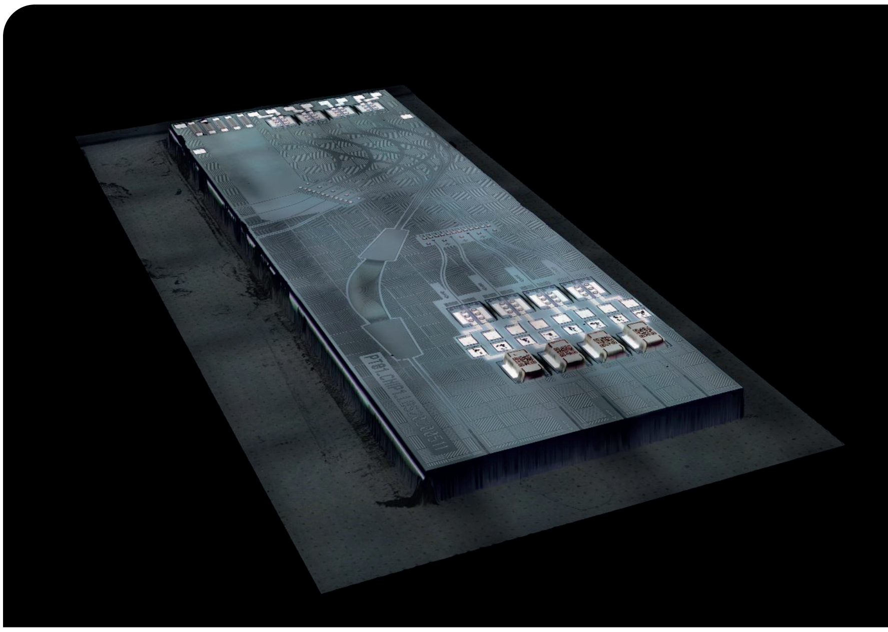


The O-Band LightBar™ by POET Technologies features high-power CW lasers for co-packaged optics and AI-ML GPUs. Celestial AI is POET's lead customer for AI products.

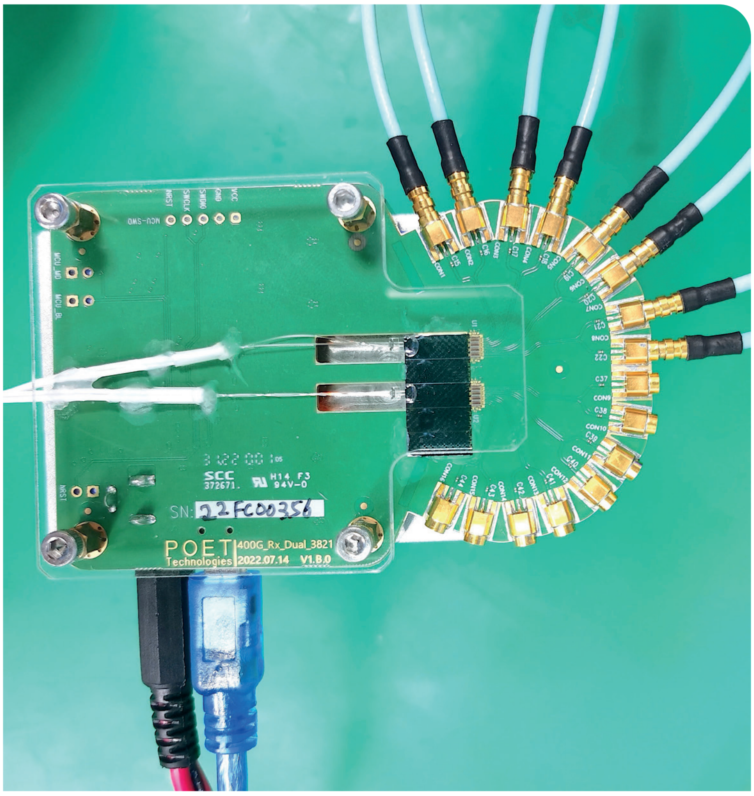
2. Scalability

Among POET's hallmarks is the ability to scale to high volume while avoiding high capital and operating expenses associated with conventional assembly of transceiver modules. By procuring optical engines from POET, our customers benefit from a steep reduction in the bill of materials, which results in a dramatic drop in module assembly costs. The company estimates its technology lowers industry assembly costs by as much as 70% from current solutions, by reducing the number of components and eliminating active alignments.

The smaller form factor (6mm x 9mm for an optical engine) and wafer-level manufacturing is critical to its scalability – increasing volume while driving down size, cost, and energy consumption. Even more importantly, wafer-level packaging is considered the only means available to meet the scalability demands of the future.



Early adopters of products built on the POET Optical Interposer include data center network operators who want to reduce cost and energy usage.

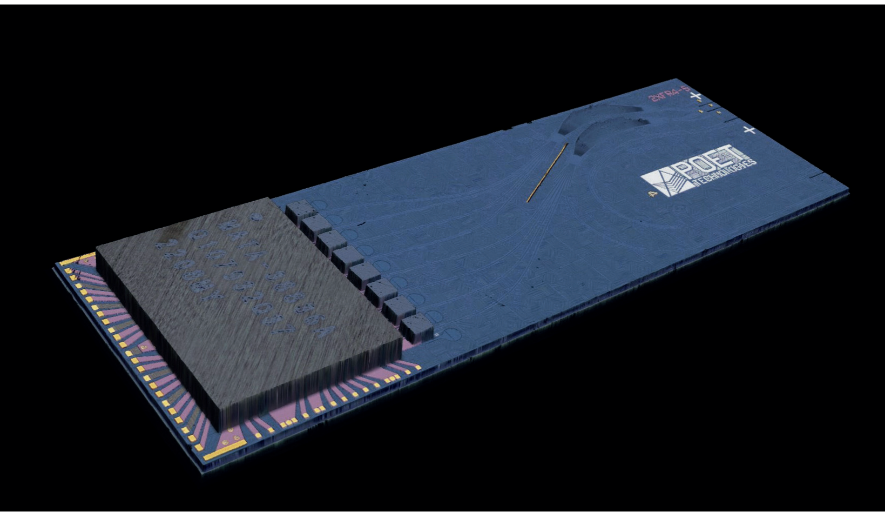


➤ POET Technologies has shipped samples of its 1.6Tbps receive optical engine.

3. Versatility

The POET Optical Interposer design allows engineers to layer components on top of each other and to achieve unique architecture to solve problems at chip level. For example, ADVA asked POET's team to tweak the design of the engines in order to maximize the routing within the module.

POET pulled wire bonds (which are typically on the side of an engine) to the front to accommodate other components in the tight space. Such clever adjustments were done to deliver a customized solution.



➤ POET Technologies is scheduled to unveil an 800G transceiver solution in the first half of 2023. In the meantime, it has completed its 800G 2xFR4 Receive Optical Engine with trans-impedance amplifier (TIA) and photodiodes assembled.

On top of that, POET uses known-good components that have been selected for their appropriateness to specific applications. Last year, the company announced the addition to its product designs of high-speed directly modulated lasers (DMLs) from Lumentum. It also uses continuous-wave (CW) lasers from Broadcom, adding to the best-of-breed components in its designs.

Produced solely with CMOS-compatible wafer fabrication methods, the POET Optical Interposer uses a standard high-resistivity silicon substrate to enable high-speed communications among all the components on a single chip.

A wide variety of components (e.g., lasers, detectors, modulators, photodiodes, drivers, etc.) are flip-chipped and bonded onto the optical interposer, creating an "optical engine" on a single chip. That simplicity allows engineers to imagine how to develop more innovations and to do it with a platform technology created to be used with diverse material systems and for generations of products to come.

4. Future Deployments

Speaking of the future, POET is already building toward it with partners and customers.

An industry that has struggled to find a reliable and cost-efficient solution to achieving higher speeds of data transfer can soon adopt POET's technology to architect 400G, 800G, 1.6Tbps and 3.2Tbps pluggable transceivers.

By using POET's optical engine "chiplets", module designers can easily scale simply by multiplying the number of them in a single package. A 400G chiplet, when multiplied by two, becomes an 800G solution, all within the same housing and without taking up any more space in a module.

The flexibility of the POET Optical Interposer extends to the materials it can use. POET is working with Liobate Technologies, an inventive company that specializes in Thin Film Lithium Niobate (TFLN), known as a stable and reliable material with promise of delivering higher speeds and reducing insertion loss. POET is using TFLN initially as a modulator solution for the commercialization of its 400G and 800G transmit and receive optical engines. It is on track to have a 400G transmit solution — which can easily scale to 800G and 1.6Tbps — ready for sampling in the first half of this year.

It's these building-block advancements that are proving that POET's goal for capitalization in a market of need is taking shape. While it's novel now, the use of the POET Optical Interposer appears to be lining up for wide-scale utilization and, perhaps eventually, normalization as the go-to technology for wafer-level, chip-scale engineering.

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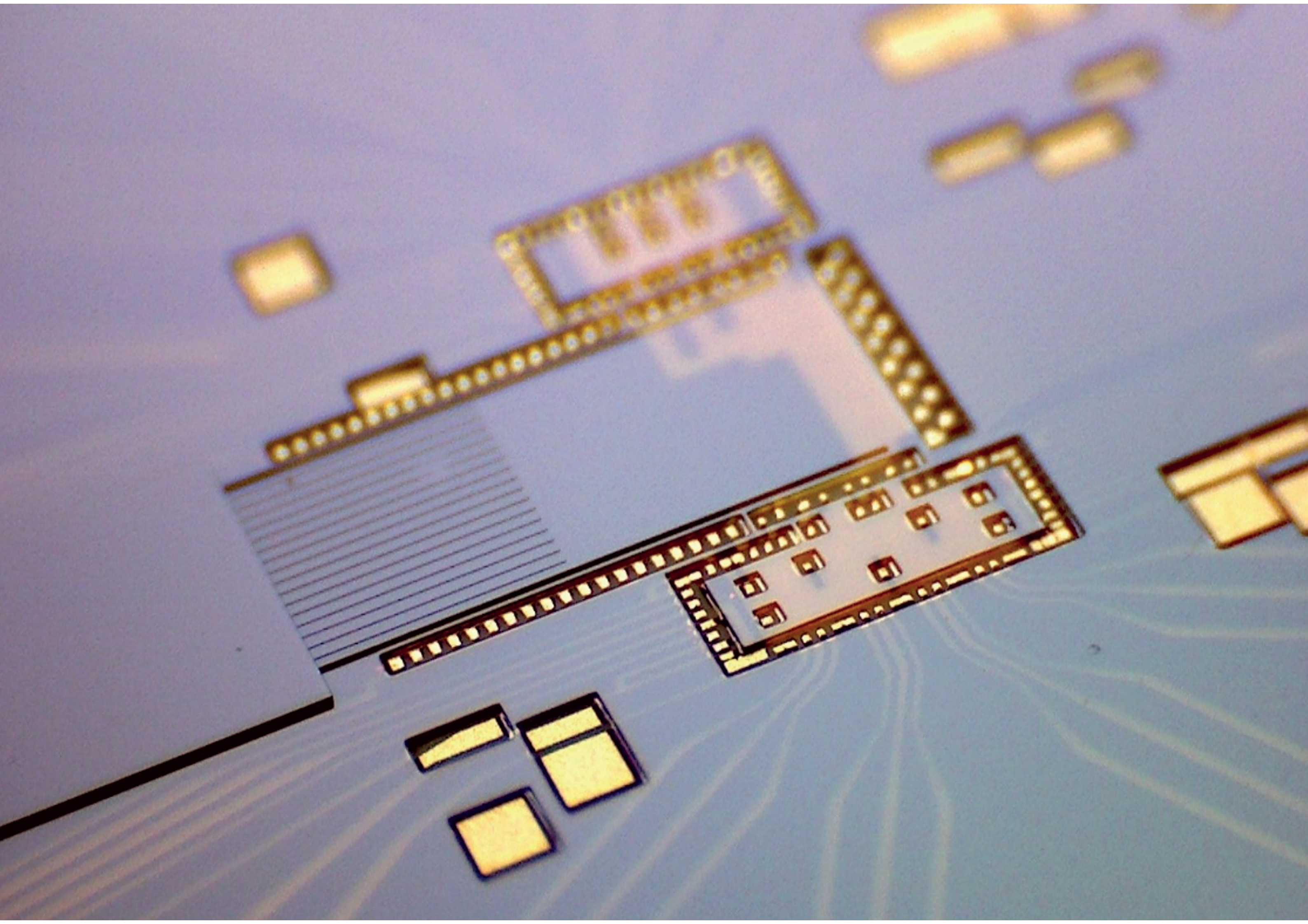


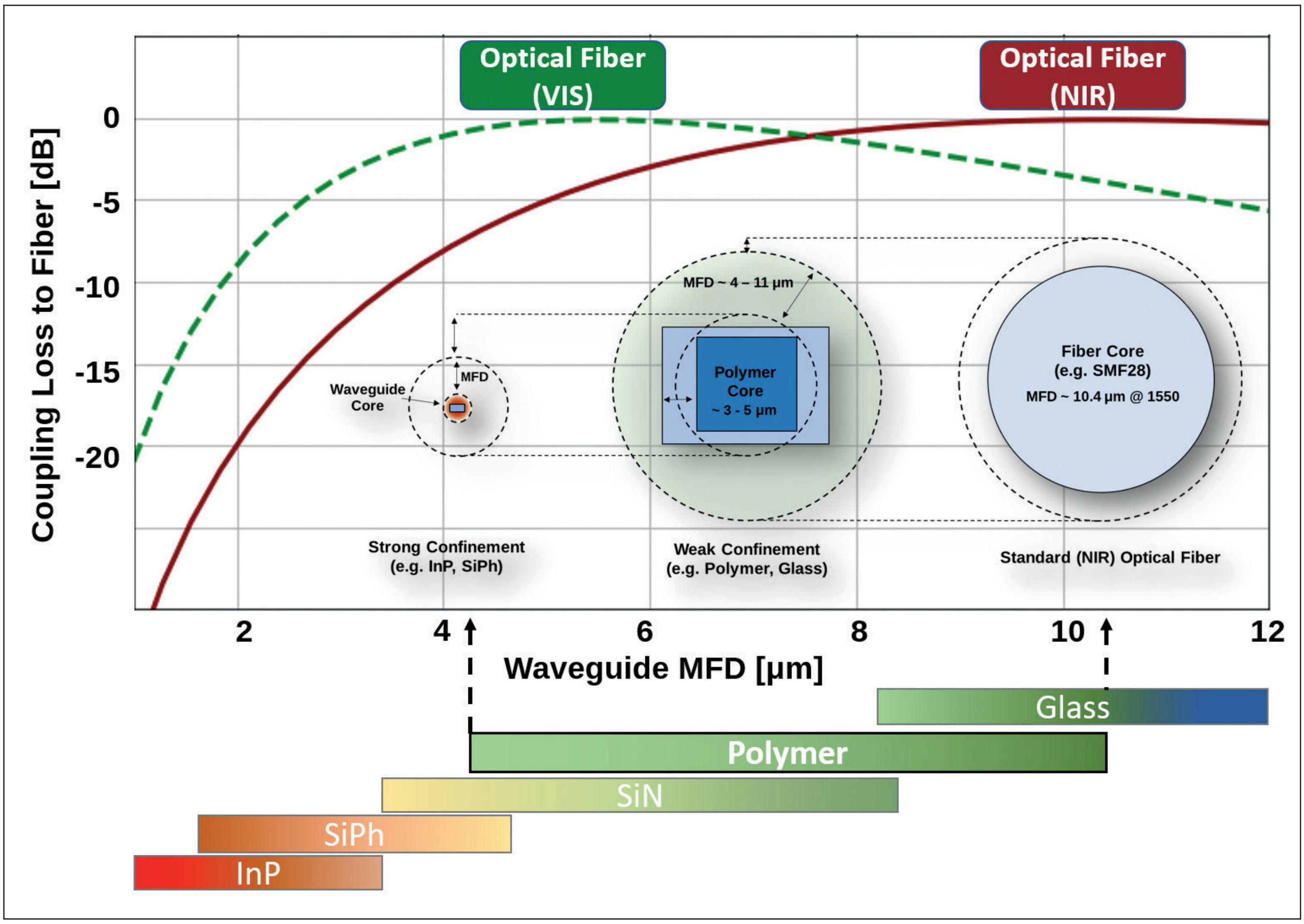
On-board photonics closing the gap between PICs and glass fibers

The growing demand for higher data-rates and lower power consumption is driving the development of many photonic integrated circuit (PIC) technologies. But it is the use of on-board photonics – PCB-embedded planar waveguides - which allows getting access to the benefits of these PICs.

BY NIKOLAUS FLÖRY FROM VARIO-OPTICS AG

Photonic integrated circuits (PICs) have matured tremendously over the last decade and are being employed in a variety of use-cases nowadays. As the range of applications is expanding, more effort is put into the seamless integration of PICs within complex electro-optical modules to create all-optical system architectures. These are required to fulfill the promises of photonic systems – i.e. lower power consumption at higher bandwidth in telecom, and utilizing novel functionalities for optical sensor devices.

However, this is where most photonic chips face a big challenge: while PICs are typically tightly confined, miniaturized chips, the typical module size of a complete package includes driver electronics,



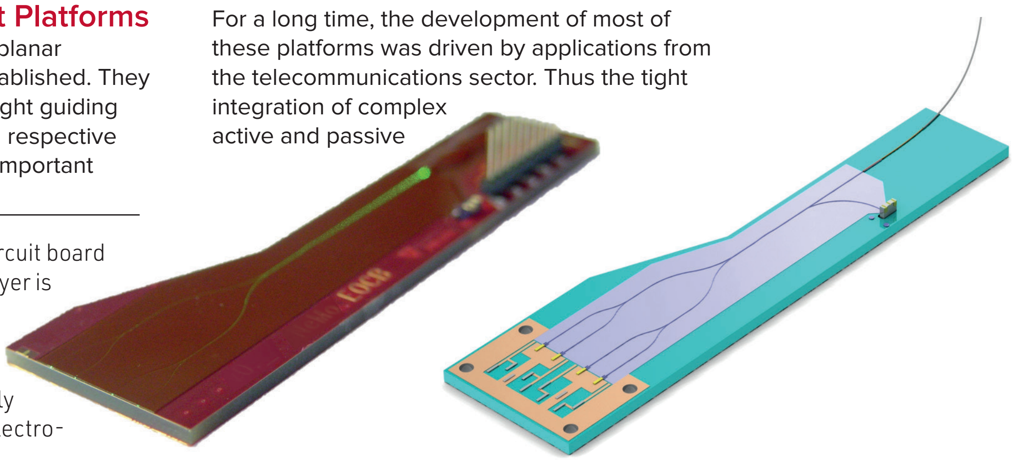
➤ The coupling loss to standard optical fibers as a function of waveguide modefield diameter (MFD). Several PIC platforms have emerged over the last decade, from strongly confined chips with large coupling loss to weaker confined platforms such as polymer or glass, with good overlap to optical fiber modefields.

fiber interfaces and other components. In the electrical world, PCBs act as the motherboard, hosting mutliple ICs and eventually being connected by wires. Analogous, in the field of photonics, Innovative solutions such as on-board optics, i.e. embedding planar waveguides made of polymer or glass material into printed circuit boards are necessary to bridge this missing gap between photonic chips and existing glass fiber networks.

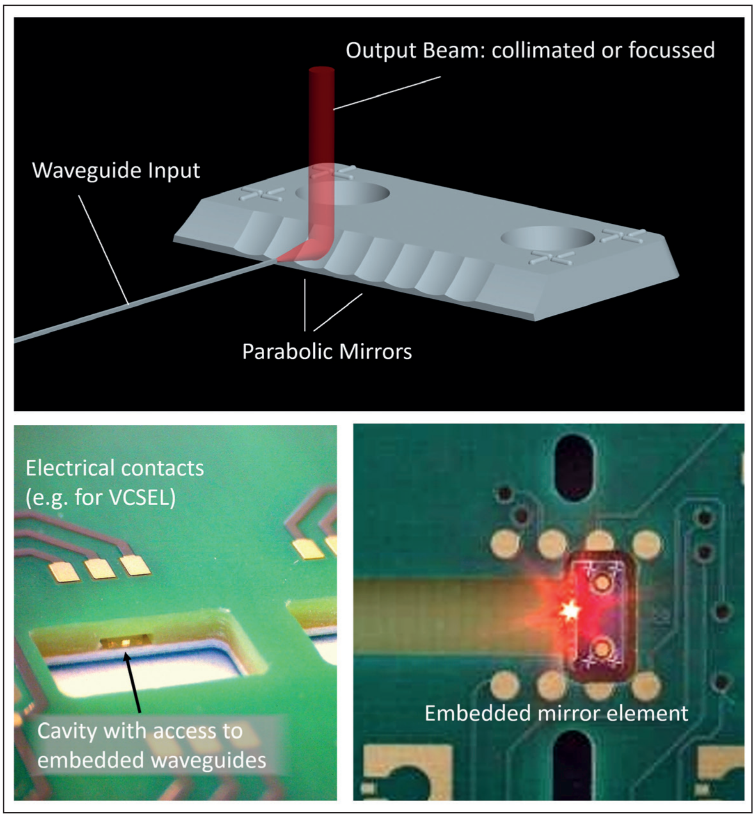
Photonic Integrated Circuit Platforms

Within the last 10 years, a variety of planar waveguide platforms have been established. They differ by the used materials for the light guiding cores and surrounding cladding and respective optical properties. One of the most important material parameters is their refractive index (RI) - specifically the RI-contrast between core and cladding, as this number, among others, dictates the typical waveguides dimensions of each platform. The range spans from highly integrated silicon photonics (SiPh) or silicon nitride (SiN) platforms over lithium niobate (LiNbO) to the slightly larger glass and polymer waveguides, which exhibit dimensions similar to optical glass fibers.

For a long time, the development of most of these platforms was driven by applications from the telecommunications sector. Thus the tight integration of complex active and passive



➤ An example of an electro-optical circuit board for a sensor application. A photonic layer is used on top of a PCB to combine light of edge-coupled laser diodes. Such a combination of planar waveguides and PCB technology reduces assembly efforts and enables fully integrated electro-optical systems.



➤ Vertical coupling to embedded waveguides can be achieved using parabolic micromirror arrays, which are integrated into PCBs. This patented technology from vario-optics allows efficient coupling of e.g. VCSELS into planar waveguide routing on-board. The micromirrors can be used for collimated or focused output and are optimized for waveguide dimensions of 50 µm.

device functionalities such as AWGs and modulators at the smallest possible size on the chip level was the prime goal. SiPh as well as InP have proven to be excellent platforms for these kind of use-cases. However, as the use of photonics is expanding the board-level, the manufacturing costs of these platforms are too high to be used for (multiple-) centimeter sized boards. Moreover, while the small waveguide cores (typically below 1 µm for SiPh or InP) have their own advantages, their associated small modefield diameters (MFDs) offer a substantial barrier when trying to couple to optical fibers.

This opens the field for less confined waveguide platforms, such as polymer or glass based photonic circuits, which can be efficiently coupled with existing optical fiber connections and manufactured at the board level.

In recent years, polymer photonics has gained tremendous attention as a result of its manufacturing simplicity. Polymer optical lenses, for example, are employed in modern smartphone cameras due to the easier fabrication, their robustness and lower costs. Similarly, polymer waveguides are an attractive alternative to other highly integrated PIC platforms such as SiPh or InP. In contrast to many other PIC platforms, polymer waveguides exhibit roughly the same dimensions and optical properties (e.g. RI) as standard optical glass fibers, which makes the combination with commonly used pigtailed laser sources or detector modules straightforward.

Similar to optical fibers, polymer waveguides can either be used in multimode (larger core dimension, typically 30 – 500 µm) or singlemode (2-5 µm core size) operation. In both cases, they are compatible with the according fiber type.

For example, the mode field diameter of singlemode optical fibers can be matched by polymer waveguides in different wavelength ranges, e.g. 4-6 µm in the visible (VIS) and 9-10 µm in the near infrared (NIR), allowing for efficient fiber-chip coupling.

Electro-Optical circuit boards

While typical PIC chips have dimensions of just a few mm each side and are processed on fixed wafers sizes, polymer waveguides can be manufactured in sizeable quantities on large panel sizes by means of UV photolithography. Making use of the tooling and standards from the printed circuit board industry provides an easier, more common process flow, and cuts down the production costs.

This allows their employment in electro-optical circuit boards (EOCBs), which, simply put, is a board featuring both an electric interface (PCB) as well as on-board optical connections (waveguides). This renders EOCBs a prime technology platform for hybrid integration and board-level photonics.

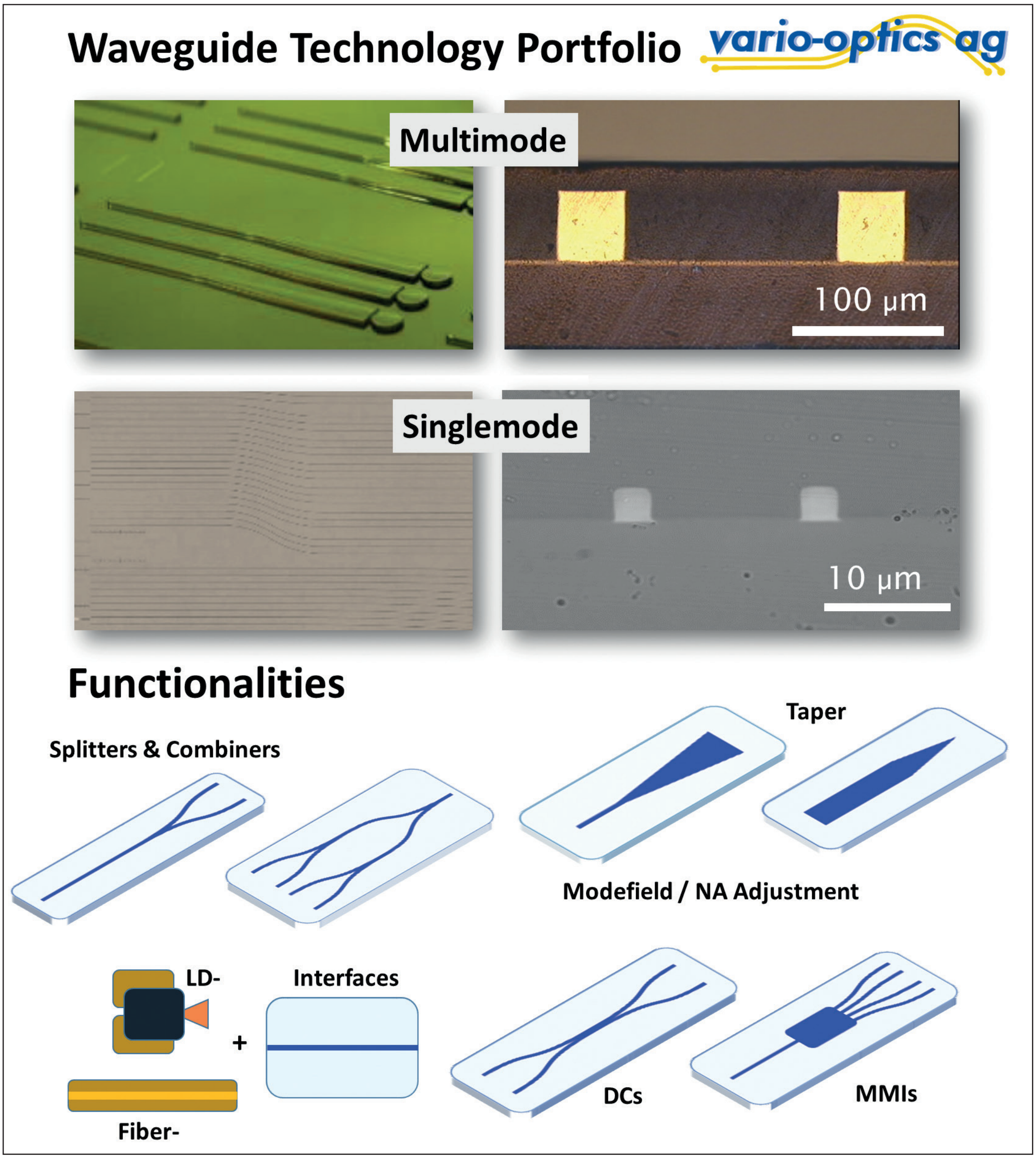
While typical PIC chips have dimensions of just a few mm each side and are processed on fixed wafers sizes, polymer waveguides can be manufactured in sizeable quantities on large panel sizes by means of UV photolithography. Making use of the tooling and standards from the printed circuit board industry provides an easier, more common process flow, and cuts down the production cost

Electrical circuits on an EOCB are manufactured by standard PCB technology, allowing to include features such as high-speed RF interfaces, (glass) interposers, thermal dissipation layers and vias. Optical on-board connections are created by including polymer based planar waveguides to the board. Depending on the application, these can be either directly manufactured on-board, using the PCB or glass as a substrate.

As polymer waveguides have advanced, they can now be operated in singlemode at most common (telecommunication) wavelength and moreover provide solid environmental stability and high power thresholds. The dimensions of the cores can be freely adapted and optimized. This way, many passive in-plane device functionalities such as splitters, directional couplers or multimode-interference couplers can be realized. As a result of the rectangular cross-section, polymer waveguides are also polarization maintaining.

The possibility of having one common host board for both the electrical and optical interface is a significant advantage over other integration methods, however often not considered enough. Most PIC packaging efforts only focus on an efficient optical coupling interface. While this is of course a central motivation and requirement in a majority of use-cases, thermomechanical and electrical requirements are often hard to meet this way.

The operation of high-power laser chips and high-speed modulators, for example, make it necessary to handle the heat as well as to provide RF above > 100 GHz. EOCBs can be designed precisely for the specific equirements of a photonic application, taking into account electrical, optical and thermal



Glass-Integration into PCB

APART from its use as an interposer, glass can also be employed as the waveguiding layer itself. Through a process based on ion-exchange, developed by Fraunhofer IZM, gradient index waveguides are created in thin glass.

These embedded waveguides exhibit low-loss singlemode operation and can be manufactured on large panel sizes of up to 457 mm x 303 mm [6].

Together with its partner Varioprint, an advanced PCB manufacturing company, vario-optics has developed a lamination process to integrate such glass panels into electrical PCBs, similar to what can be achieved with polymer waveguides in optical backplanes.

Optical interfaces to the glass layer are made by cut-outs in the PCB and CO_2 laser cutting of the glass. Laser-structuring of the panels also allows to create trough-glass vias or mechanical features for embedding optoelectronic components.

Overall, due to the low propagation loss at telecommunication wavelengths (< 0.06 dB/cm @ 1550 nm [7]), the addition of glass waveguides into large EOCBs is a promising technology for next generation photonic integration.

considerations, before being equipped with PICs as well as purely electronic components.

Coupling to EOCBs

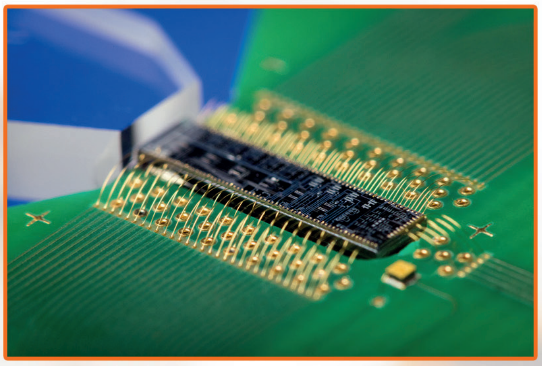
Optical coupling to an EOCB can be done both in-plane or vertical out-of-plane. In-plane coupling typically relies on butt-coupling, i.e. precise facet-to-facet placement of the optical component to the waveguide core.

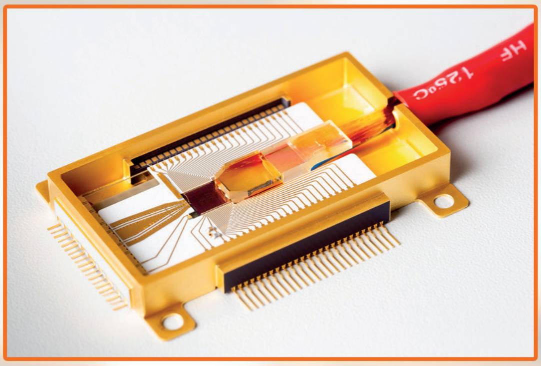
The efficiency of such an interface depends on the NA-match (multimode) and modefield overlap (singlemode), respectively. Thanks to the tenability of the geometry of polymer waveguide cores, their MFDs can be optimized for both coupling to a highly confined PIC, as well as to standard optical fibers. While there is the possibility to make use of precise on-board alignment features, which allow for passive placement of components, active alignment processes are becoming easier (and cheaper) over time as well and are capable to provide sub-micron assembly accuracy. An attractive alternative is vertical out-of-plane coupling. This can be achieved in multimode EOCBs by including miniaturized parabolic mirror elements into cavities inside the EOCBs. These can be positioned with high accuracy and allows to make use of VCSEL sources at very high efficiencies.

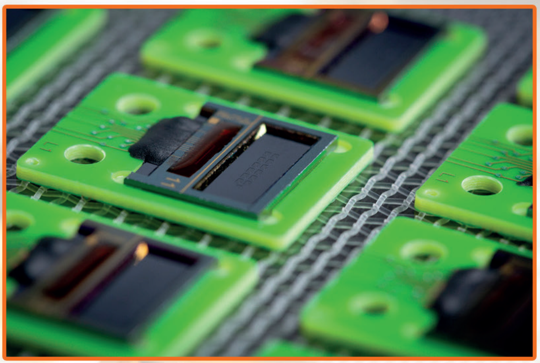
Another alternative approach to the assembly is to rely on an adiabatic, evanescent coupling interface. In this coupling scheme, inverse-tapered waveguides on the PIC are used to couple light to exposed polymer waveguide cores, and vice versa. In contrast to grating couplers, this approach provides not only relaxed lateral assembly tolerances (approximately +/- 2 µm), but also efficient coupling over a broad wavelength range for both TE and TM polarization.

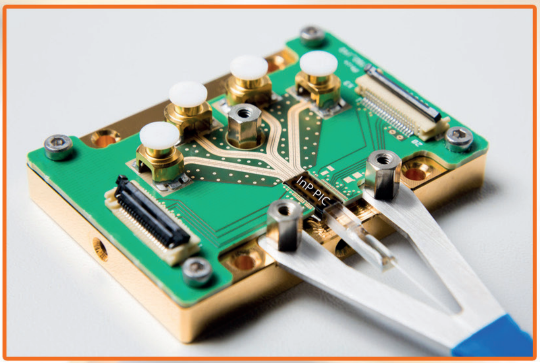
Summary

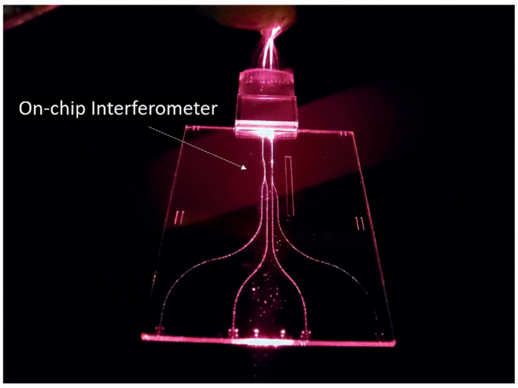
On-board photonic solutions are required to utilize the full potential of integrated photonic technologies. The rise of planar waveguides based on polymer or glass is a key step towards the development of devices and applications with



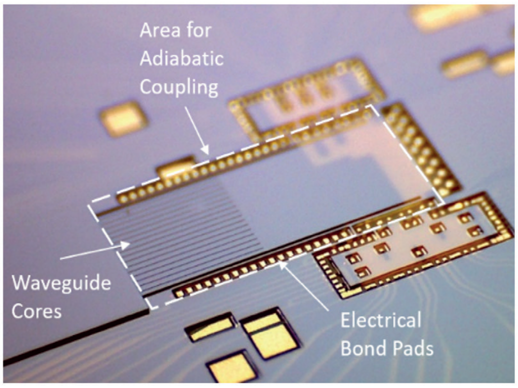




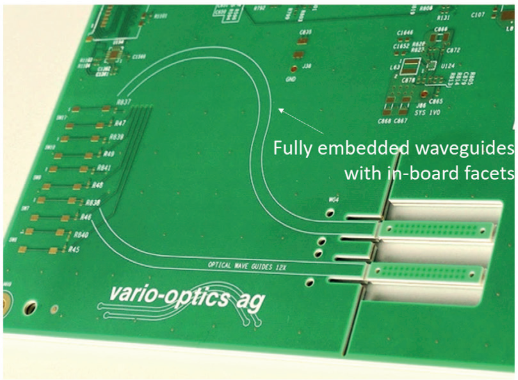

InP PIC



Photonic boards based on planar waveguides can also be employed for advanced functionalities such as on-chip interferometry, which helps to drastically reduce the footprint of industrial or environmental sensor systems [1].



When manufactured on top of a PCB substrate, polymer waveguides can be used for simultaneous electrical- and optical coupling to a PIC (e.g. SiPh, InP) [2].



Fully embedding polymer waveguides into complex PCBs enables true on-board optical systems [3,4]. By bringing the optical signal closer to the chip, such systems provide tremendous advantages in terms of low power consumption and allow to reduce the amount of disturbing glass fibers inside a package [5].

electro-optical functionalities, high integration density and competitive costs as compare to existing solutions. Electro-optical circuit boards, as manufactured by vario-optics ag, represent a key technological building block for such all-optical systems.

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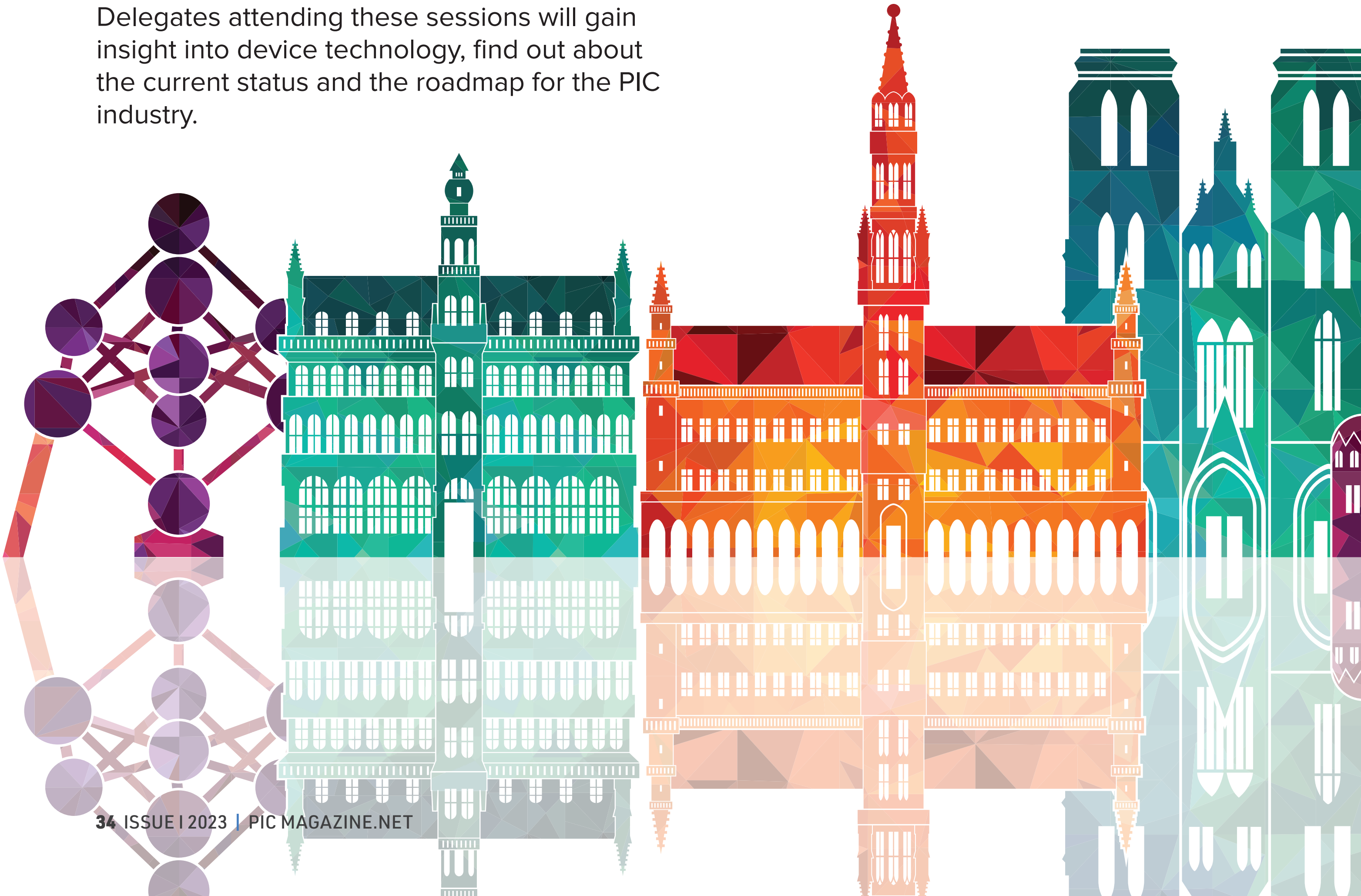

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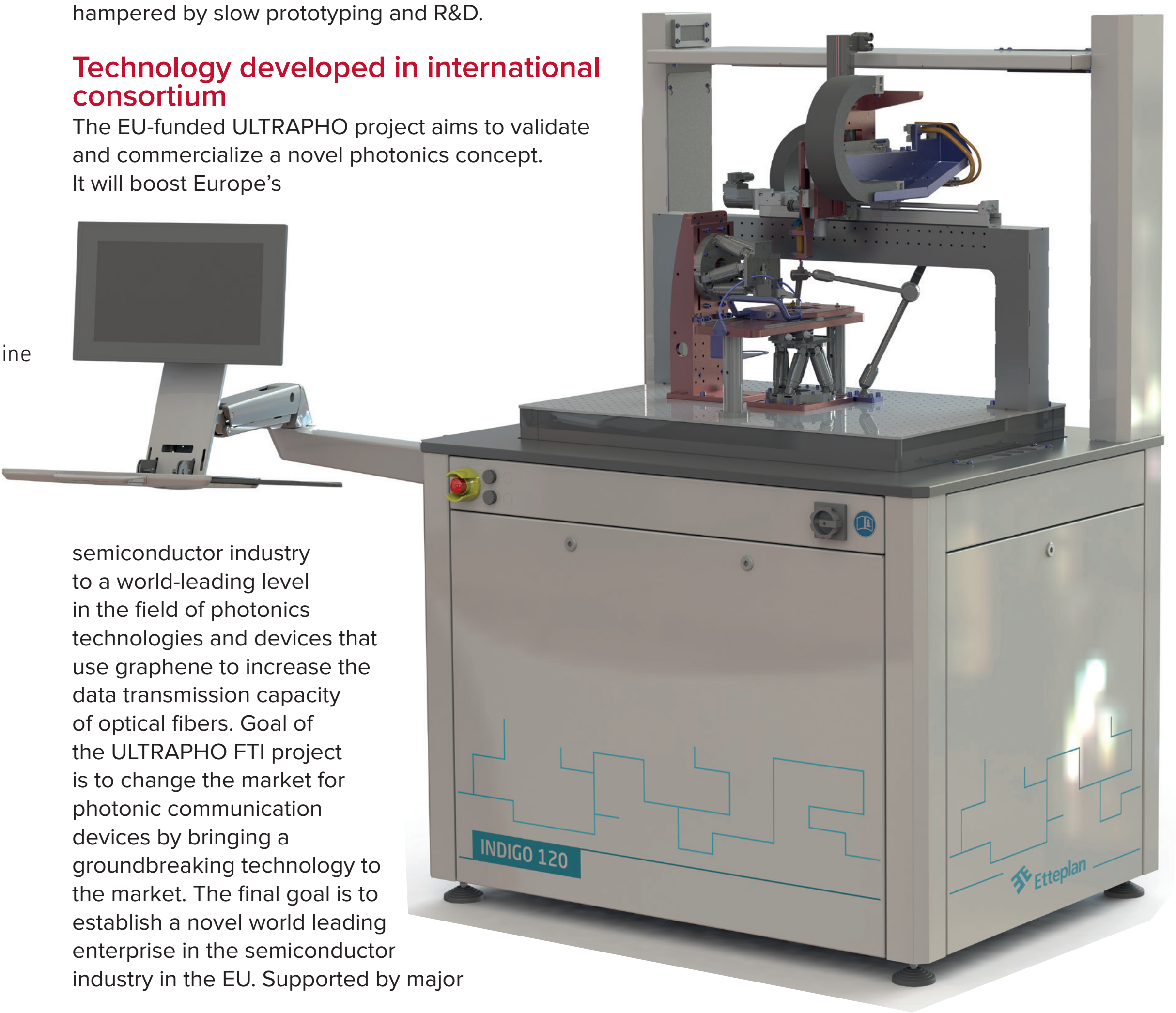
Accelerating the photonics transition with much shorter R&D

To accelerate the transition from electronic to photonic integrated circuits (PICs), a breakthrough in cost and cycle time of the manufacturing process is needed. Etteplan developed an R&D solution which accelerates the process. The solution uses a simple and efficient block-based programming interface via a standard web browser to enable users to program the production sequences themselves.

COMPANIES in the photonic industry, developing new products or products novelties, that are transitioning from startup to scale up and are working on the first prototypes, are seeking ways to quickly and reliably align photonic components and validate their product development. Despite all the developments, growth of integrated photonics is hampered by slow prototyping and R&D.

Technology developed in international consortium

The EU-funded ULTRAPHO project aims to validate and commercialize a novel photonics concept. It will boost Europe's semiconductor industry to a world-leading level in the field of photonics technologies and devices that use graphene to increase the data transmission capacity of optical fibers. Goal of the ULTRAPHO FTI project is to change the market for photonic communication devices by bringing a groundbreaking technology to the market. The final goal is to establish a novel world leading enterprise in the semiconductor industry in the EU. Supported by major players like Nokia, Sony, and GlobalFoundries, the consortium members will become worldwide leaders in the emerging field of photonic technologies and devices. The fundamentally new high-speed photonic devices use graphene to increase data transmission capacity of optical fibers. Together



➤ Etteplan Indigo machine platform.

AMO's packaged graphene photodetector. Image credit: AMO.

with novel fabrication and characterization tools and technology developed and marketed by the consortium the whole value chain from fabrication to the final product is covered.

The consortium markets an ultrafast and broadband graphene photodetector which is of increasing importance for datacenters or 5G infrastructure.

A solution to accelerate photonic R&D

To help accelerate the photonic transition, Etteplan developed 'Etteplan Indigo'. A modular machine platform for the assembly of a wide range of micro-optical elements, such as the graphene photodetector by Black Semiconductor and Graphenea. "Black Semiconductor and Grahenea are developing a photodector with graphene, capable of converting optical signals to RF and vice versa", tells Niels Jansen, manager Engineering at Etteplan. "They have asked Etteplan to help find solutions for the back-end assembly of this product.

As this product was still in development, flexibility in the production sequence of the packaging solution became a crucial element. Typically it takes days of work to adjust the machine platform from product X to do a test with product Y. As a general rule, the machine supplier has to be called in to convert machine settings. If for a product change one would have to move the gantry to a different position, choose a different alignment route, this takes a lot of time with a PLC control.

You have to create it, test it offline, track software changes and someone has to come on site to adjust settings, test and validate. This quickly adds up to six to eight charged hours, provided a programmer is readily available to make these changes.
By changing production parameters or complete sequences in a simple manner, multiple variations in the product design can be tested and validated quickly and comfortably, in the end enabling the development of the product to achieve quality results and limited lead time. Etteplan developed a solution that enabled just that.

Based on the open source platform Blockly, the solution combines a simple and efficient block-based programming interface via a standard web browser to enable users to program the production sequences themselves."

Make the changeover yourself

'Etteplan Indigo' has a short cycle time and enables a faster time-to-market for automatic and precise alignment systems, while increasing throughput tenfold with respect to currently available solutions. "But, most importantly, the flexible production solution (FPS) enables you to program the changes to package the next prototype yourself," tells Niels Jansen, manager Engineering at Etteplan.

"Visually programmable software controls the PLC, without the need for programming by the machine manufacturer. The representation of modules in visual blocks makes it 'child's play' to follow and adjust the steps in packaging. You don't need a PhD for it so you can also quickly and easily bring

> Flexibility in the production sequence of the packaging solution became a crucial element

➤ Etteplan's Flexible production solution (FPS), visually programmable software controlling the PLC.

Ready for sequence
Start your sequence
Ok

relatively untrained people into production. We have taken away the complexity and dependency, and that adds a lot of speed."

Etteplan's visually programmable software.

"Our modular machine is also financially attractive in terms of investment and the machine has a smaller footprint," states Niels Jansen. "There are no three or four machines next to each other working on different products. There is only one machine. Moreover, the reproducibility of the configured, programmed run is a big plus. The system allows you to store the programmed production sequence and configured parameters for retrieval and reuse at a later date. We therefore dare to call 'Etteplan Indigo' a 'photonic breakthrough' for good reason."

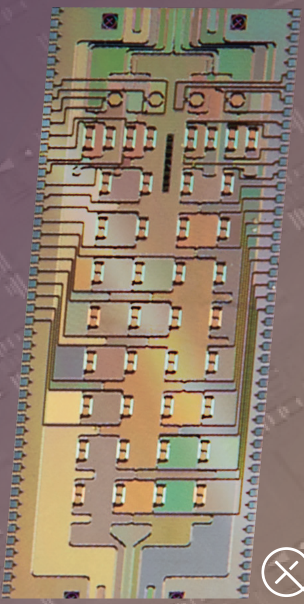
Another benefit: shorter changeover times in higher production volumes

The machine platform meets the specific needs for usage in R&D (start-up) and scale-ups environments, enabling accurate assembly of optical elements at relative low investment cost.

"If your production volume increases, you can reconfigure the system by simply adding modules to create a fully automated assembly solution", tells Niels Jansen. "The modular approach allows for a machine that is customized to your current demands while leaving plenty of room for the customization of different components and upgrades, and to integrate the machine into an assembly line."

"Besides the benefit for R&D and scale-ups of faster changeovers, we also see companies with a great need for quick and easy changeover of the packaging machine in order to meet production demands," tells Niels Jansen.

"A good example are foundries that are not yet running huge volumes with a photonic product and are creating low volumes of different products. They need a smart way to make their assembly


XANADU

> “The solution combines a simple and efficient block-based programming interface via a standard web browser to enable users to program the production sequences themselves”

production suitable for other and new products. Crucial to foundries is changeover time. Foundries active in photonics want to set up their production line in a way they can assemble product X one day and product Y the next.

The faster you can make that switch, the more you can produce and the faster you can meet your customers’ demands. You want to focus on improving and making the final product, not spend your time on the machines making them. This innovative software will drastically reduce changeover times.”

“I am convinced that we can significantly accelerate your R&D process with our software solution. The Etteplan Indigo Photonic Assembly Platform will also reduce your packaging cost and thus the cost price of your photonic devices.”

As Engineering Manager, Niels Jansen is responsible for the Engineering department at Etteplan Engineering Solutions in the Netherlands, including mechanical, electrical, software and process engineering. In his role, he is also responsible for the development of the machine platform and manufacturing production solutions, as well as the technology roadmap. Niels is member of the Management Team (MT) of Etteplan NL. Niels received his Master’s degree in Systems and Control from the Eindhoven University of Technology with the classification with great appreciation. Since then he worked for several companies in the industrial automation in the Netherlands, where he gained positions as group leader and manager for engineering teams, responsible for the development and implementation of industrial automation solutions. Contact via: **niels.jansen@etteplan.com**

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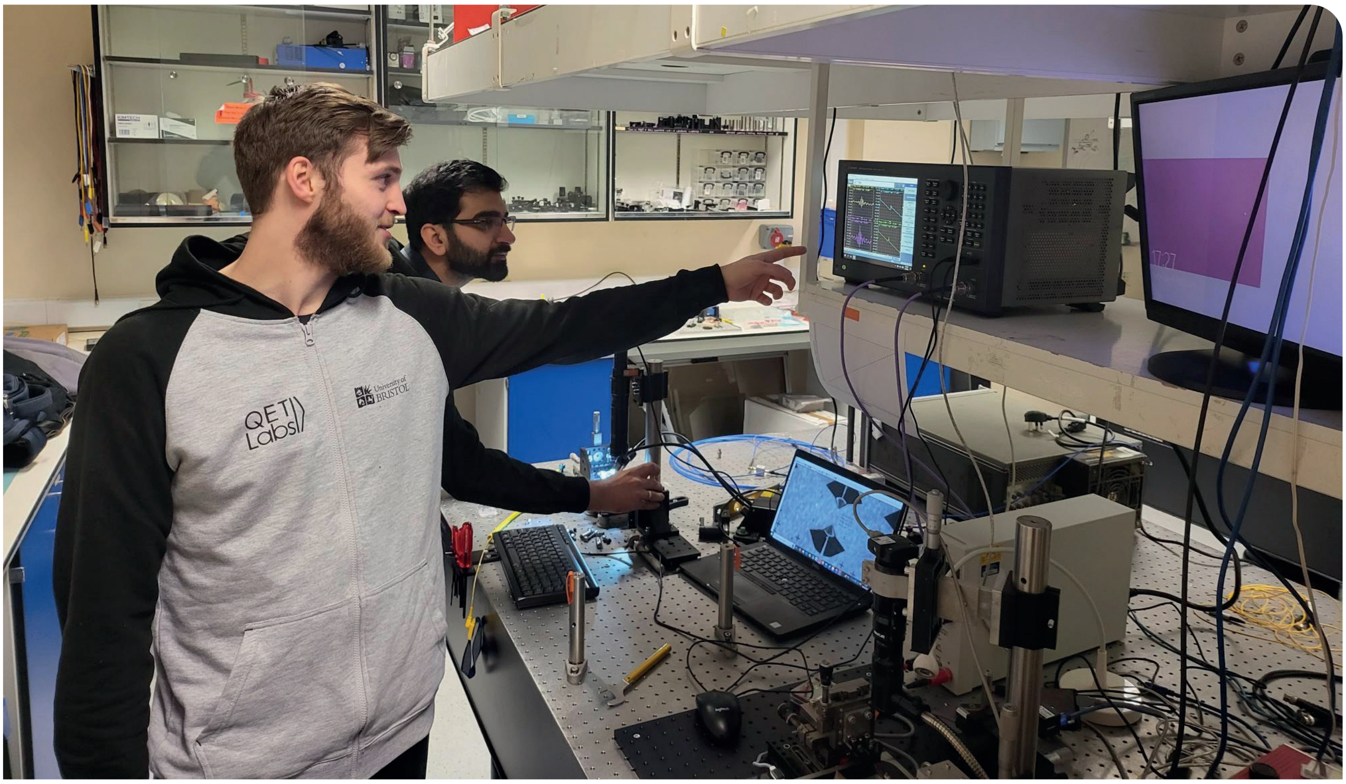
Building phononic integrated circuits with GaN

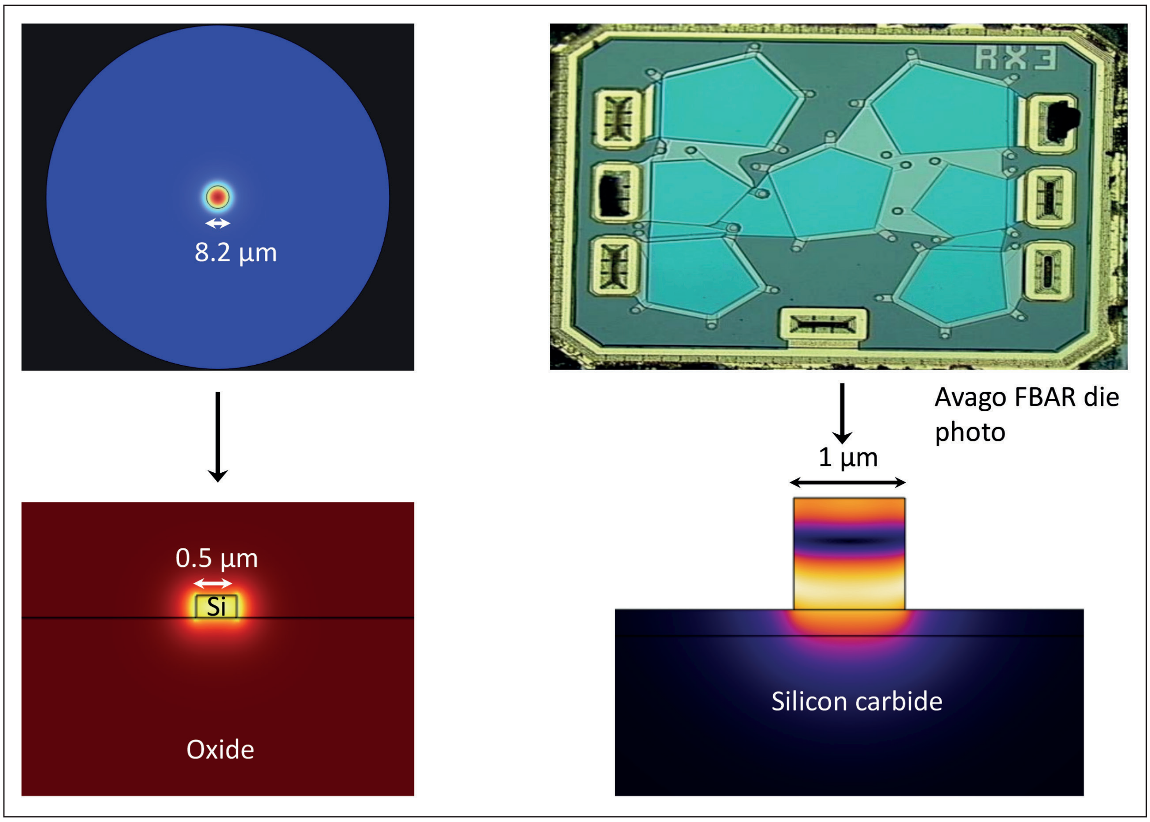
The ability to guide high-frequency sound around a semiconducting chip positions GaN as a promising platform for producing compact, high-performance acoustic wave devices

BY MAHMUT BICER, STEFANO VALLE, JACOB BROWN, MARTIN KUBALL AND KRISHNA C. BALRAM FROM THE UNIVERSITY OF BRISTOL

A long-standing theme of engineering research is exploring and exploiting the similarities between different wave phenomena. Their similarities, such as reflection, superposition and the creation of standing waves, has been appreciated for decades, thanks in part to excellent demonstrations by the late John Shive, who worked at Bell Labs. Back in 1959 Shive gave a lucid, insightful lecture on this topic that can still be enjoyed via Youtube. In that talk, standing as one of the earliest examples of recognizing the unifying nature of the underlying physics and illustrating how to translate ideas from one field to another, Shive demonstrated his wave generator, a great contribution to teaching this topic.

One modern iteration of exploiting wave phenomena is an extension of silicon integrated photonics, with chips designed to control the propagation of sound waves with frequencies in the gigahertz domain. Such efforts build on progress in silicon photonics over the last decade that spawned a revolution in optical telecommunication, with CMOS foundries now used to build photonic chips. The underlying physics behind this development is the high refractive index contrast provided by a silicon-on-insulator platform – this enables tight confinement of propagating light in wavelength-scale waveguides. For instance, the standard waveguides used to route optical telecommunication signals with wavelengths of





➤ Figure 1. Analogy between photonics and phononics. A strong geometric index contrast leads to an increase in confinement and a reduction in the waveguide cross-section. The rise of silicon photonics is a case in point, with telecom-wavelength silicon waveguides (bottom left) having sub-micron dimensions compared with optical fibres (top left). Bringing these ideas to high-frequency acoustic waves (top right) can lead to the development of compact passive acoustic devices and the prospect of tight active-passive integration on-chip with a view towards integrated RF front-ends. The image of the FBAR Avago die is taken from R. Ruby, "A decade of FBAR success and what is needed for another successful decade," 2011 Symposium on Piezoelectricity, Acoustic Waves and Device Applications (SPAWDA), Shenzhen, China, 2011, pp. 365-369.

around 1550 nm have a cross-section of around just 220 nm by 550 nm. That's substantial miniaturisation compared with an optical fibre: it has a typical core size of 8.2 µm and a cladding diameter of 125 µm, due to its far weaker refractive index contrast.

There are many benefits associated with the extreme confinement that enables compact devices. One great attribute is that a single chip can accommodate various passive and active functions, such as splitting signals, combining them, mode transformation modulation and detection. In addition, there is a low propagation loss that accompanies the strong confinement, resulting in high electric field strengths and associated non-linearities. These properties may be harnessed to implement a variety of functions for quantum information processing, such as single-photon generation using spontaneous four-wave mixing.

As the wavelength of sound waves in the gigahertz range is similar to that of the light used for telecommunication, it is natural to ask how far these ideas from integrated photonics can be extended to gigahertz frequency acoustic waves. One may also wonder what new device paradigms might be enabled. It should be noted that the idea of guiding sound in waveguides is not new – this had been discussed from the very early days of waveguide research. However, this interest has evolved, and is now motivated by considerations related to the acoustic waves that underlie all the filtering in modern smartphones. Today's state-of-the-art smartphones are packed with between 30 and 50 acoustic wave filters, with their number increasing with each successive generation. It is an ever-increasing challenge to accommodate this increasing number of discrete filters into a given area, along with the associated switches, amplifiers and other signal processing circuitry. Current devices are a packaging tour-de-force, but we cannot expect these methods to work well into the future.

The tremendous successes that have come from microelectronics, and more recently silicon photonics, indicate that monolithic integration could be the best solution to this growing problem. Success hinges on figuring out a way to trim the size of traditional acoustic wave devices, and how to implement tight integration between active and passive components on the same die. Much effort has already been directed at accomplishing this, with approaches relying on methods that employ a CMOS process to integrate existing acoustic-wave devices, such as FBAR and SAW filters, which rely on quasi plane-wave resonators. But at the University of Bristol we are taking a different path, investigating whether acoustic-wave devices can be redesigned around phononic integrated circuits (PnIC), featuring strong geometrical confinement of sound. We are keen to explore the benefits and challenges of this approach.

Computational challenges

Another driver behind the development of PnICs, coming from a very different direction, is the rise of superconducting qubit-based quantum processors – that includes the demonstration of computational quantum supremacy by Google using this platform. A logical next step, following the development of classical information processing technologies, is the development of small quantum networks around these superconducting qubit processors.

This is challenging task, because qubits usually work in a dilution fridge environment that is just a few millikelvin above absolute zero. In addition to this temperature restriction, another issue is that the microwave quantum states cannot be sent over any significant distance, due to loss in the microwave cables.

Alternative approaches may offer a better chance of success. One promising pathway is to switch to optical photons, which have been employed in quantum communication from near-earth satellites. This scheme requires quantum transducers, which convert microwave quantum states to light and back with high efficiency. To build such a device, engineers must overcome a massive wavelength mismatch between the fields in the microwave and optical domain. Fortunately, acoustic waves provide a natural way to bridge this, having wavelengths of microns at gigahertz frequencies.

We are pursuing piezoelectric optomechanical platforms that support light and sound propagation on these wavelength scales, and foster strong acousto-optic interactions between resonant optical and mechanical modes. Such piezoelectric optomechanical devices offer one of the most promising routes towards building quantum transducers, with state-of-the-art devices achieving photon transduction efficiencies of around 5 percent.

When developing a PnIC platform, deciding on the material platform is the first and possibly the most critical choice. There's a need for a slow-on-fast platform – in other words, a platform where the acoustic velocity in the waveguiding device layer is far lower than in the substrate – because this offers total internal reflection of sound and the prospect of waveguiding. It's important to satisfy the guiding condition for all potential leakage modes in the substrate, and for all propagation directions simultaneously. The good news is that in practice, this condition is relatively easy to satisfy. There are a wide range of substrate velocities available in different material platforms, and many material platforms are currently being explored, ranging from lithium niobate on sapphire to GaN-on-SiC.

Going with GaN-on-SiC

Out of the many options, which all offer unique advantages and disadvantages, we have selected GaN-on-SiC. Our primary reason for this is that GaN is a moderate piezoelectric semiconductor with a built-in foundry infrastructure that can potentially enable monolithic integration between active and passive components on the same die. By exploiting acousto-electric (electron-phonon) interactions in this platform, it is possible to develop non-reciprocal microwave devices that provide new degrees of freedom to manipulate RF signals on a chip. With alternative, existing technologies, this is only accomplished with the addition of magnetic materials.

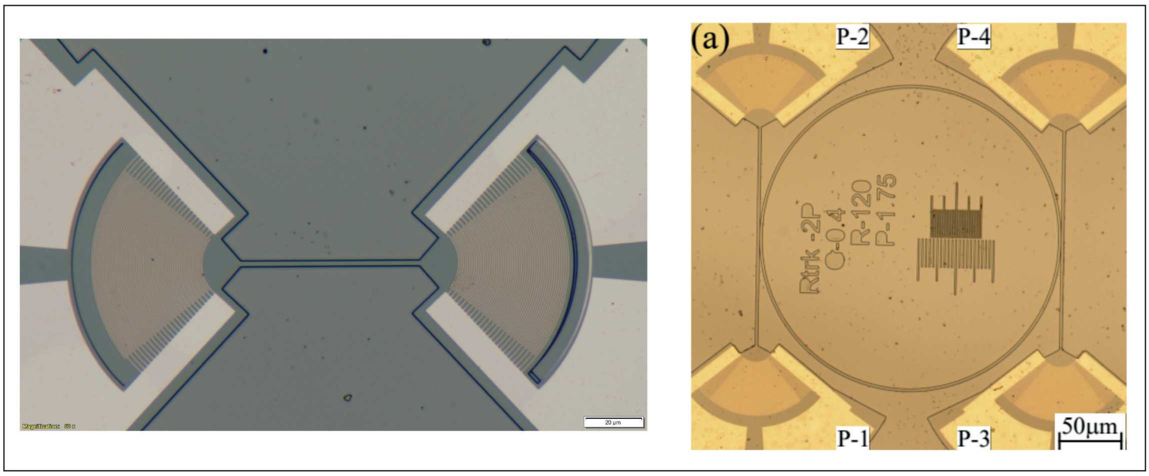


Figure 2. Optical microscope images of representative PnIC devices fabricated at the University of Bristol in a GaN-on-SiC platform. The acoustic waves are generated from applied RF signals using interdigitated transducers, whose fingers are curved to focus the sound into the acoustic waveguides. The waves are then routed on-chip using waveguides with cross-sectional dimensions of the order of a wavelength, and high-Q whispering gallery modes in ring resonators, which can be used for resonant devices.

Our PnICs feature an interdigitated transducer, which converts input microwave signals to sound waves (see Figure 2 for an optical microscope image of our device). The periodicity of our interdigitated transducer has been selected to match the acoustic (Lamb) wave frequency in the material. This ensures a periodic perturbation on the surface, due to the piezoelectric effect, and efficient conversion of microwave energy into propagating sound waves. By shaping our electrodes, we can focus sound waves efficiently into wavelength-scale waveguides that have a cross-sectional area of several square microns. Once sound is launched into these waveguides, it can be routed over the surface in an arbitrary fashion, while maintaining tight lateral confinement.

As well as producing straight waveguides, we have the opportunity to construct micro-ring resonators that exploit high-quality-factor, whispering-gallery modes of sound as the resonant building block for filters. Given that whispering-gallery modes rely on the total internal reflection of sound, which is theoretically lossless at a given frequency, resonators based on this technology should demonstrate higher quality factors than traditional SAW and FBAR devices – those incumbents rely on either metal gratings or metal contacts (hard boundaries) for reflection that's always accompanied by excess dissipation and scattering. If we are able to experimentally verify the promise of this micro-ring resonator technology, it would show that in addition to providing compact devices, the PnIC approach can deliver devices with a higher performance than those made with traditional approaches.

The real advantage of the PnIC lies in the realisation that since sound is generated from an RF signal, its manipulation on a chip ultimately provides new degrees of freedom to manipulate RF signals. For instance, if the designer of a PnIC decides to include spiral waveguides with an on-chip footprint of less than 0.25 mm^2, this allows RF signal delays of more than 2 μs, corresponding to electromagnetic delays of at least 600 m.

While our PnIC platform has shown promising initial results, there are a few important problems that we still need to address before our exciting device demonstrations can impact future RF systems. One essential area to work on is the reduction of the overall insertion loss in these platforms. Acoustic waves suffer negligible excess dissipation and scattering once inside the waveguide, but a significant insertion loss at the entrance and exit, coming from the transducer and the transducer-waveguide interface. It is a challenge to develop efficient transducers that are impedance-matched to 50 Ω and mode-matched to wavelength-scale waveguides.

Another issue arises because acoustic platforms are intrinsically multi-moded systems. There's a need to carefully control mode propagation so that sound is efficiently focused into the waveguides without deleterious mode conversion at the interfaces. Note that in this instance the analogy with optics breaks down. For integrated photonics the corresponding problem is much simpler, due to both single-mode operation and the nature of the refractive index profile, which keeps light near the waveguide centre. With sound, especially surface waves, there is a preference for intensity to peak beside the edges of the waveguide.

A second thrust for our research roadmap is to push the PnIC beyond purely passive devices and exert active control on the acoustic waves propagating in these wavelength-scale devices. We would like to move towards tuneable PnICs, engineering acoustoelectric interactions in our GaN platform to provide controllable gain and non-reciprocity. Success on this front will provide new degrees of freedom to the PnIC toolkit from an RF systems perspective. Finally, it goes without saying that there's a need to translate all these research advances to a commercial GaN foundry platform, to enable a full realisation of the system-level benefits.

We are in no doubt that by guiding and manipulating sound on the surface of a chip, wavelength-scale PnICs are providing a promising avenue to re-think passive acoustic devices from an RF systems perspective. As well as trimming the on-chip footprint, building around a waveguide geometry allows natural avenues to route and actively manipulate sound – and by extension the associated RF signal – on a chip in ways that open up new architectures for systems integration and signal processing. To realise the full benefits of this platform in the near-term there's a need to cut insertion loss to levels comparable to current systems and produce devices with a commercial foundry process.

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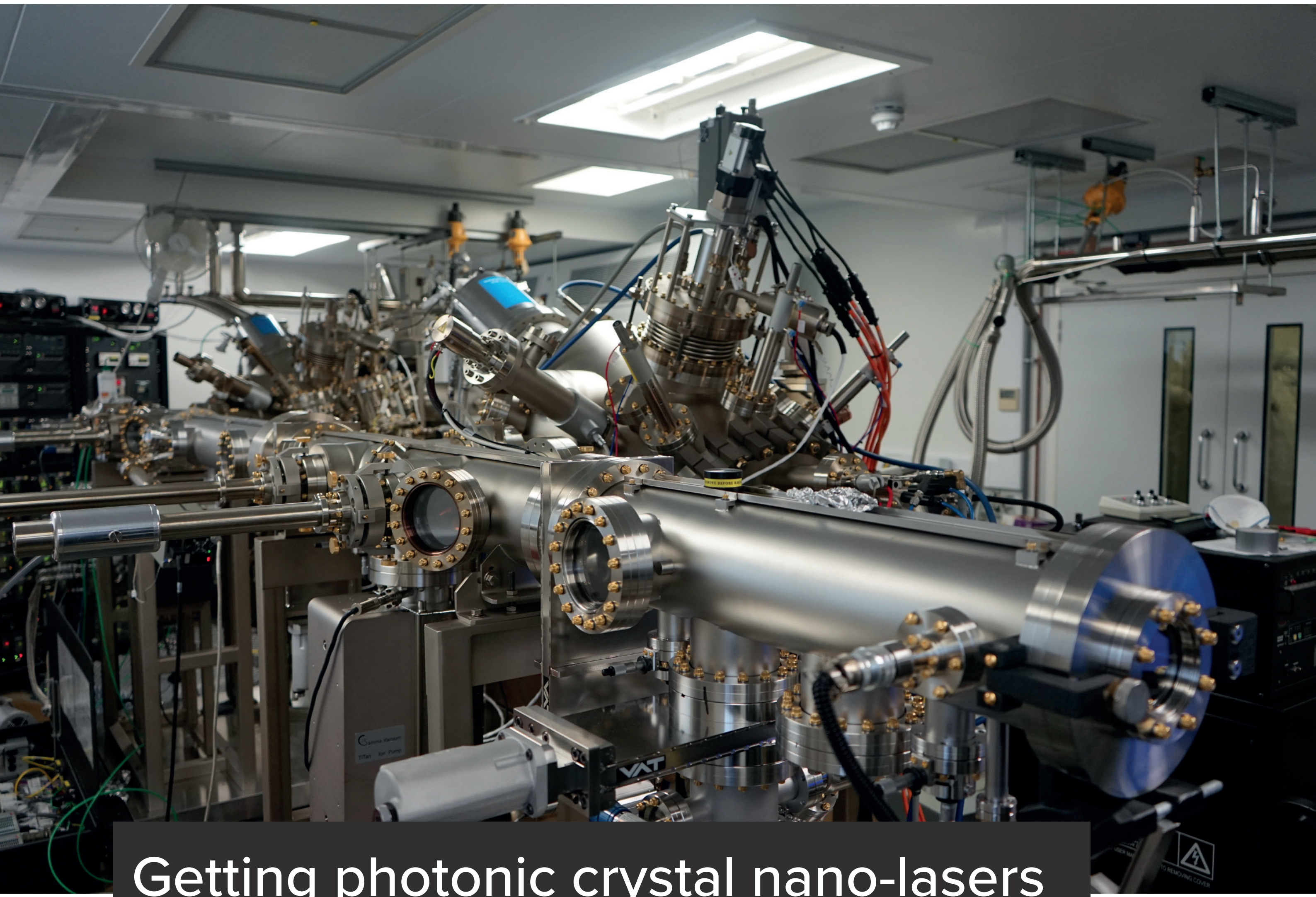


Getting photonic crystal nano-lasers on silicon

Recent demonstrations of photonic crystal lasers on a silicon platform highlight the tremendous potential of these devices for providing efficient light sources for silicon nanophotonic integrated circuits

BY MINGCHU TANG FROM UNIVERSITY COLLEGE LONDON

SEMICONDUCTOR LASERS have come an awfully long way since they emerged from a number of industrial labs in the US in 1962. To realise lasing in those first homostructure devices, the chips would be cooled by liquid nitrogen and electrically pumped with incredibly short, high-current pulses. Fortunately, rapid progress followed the invention of this device, with the introduction of double heterostructures and refinements to the active region improving key characteristics and enabling the production of a practical device.

These advances have spurred the commercialisation of the semiconductor laser and its widespread deployment. Significant successes include miniature sources for reading optical discs, the key technology for CD and DVD players, and the manufacture of countless light engines for various optical networks that underpin communication and the internet.

Now there is much interest in using III-V lasers for silicon photonics. Producing integrated circuits that route light through waveguides and a number of on-chip devices enables energy savings in many different applications requiring data transfer, such as high-performance computing and data centres, as well as opening up many new markets, including those in healthcare, where miniaturisation is highly valued.

A significant challenge with any silicon photonic integrated circuit is how to incorporate the III-V laser onto the chip. One option is bonding, using the likes of benzocyclobutene (BCB) or oxygen atoms to form a bonding interface. Intel has successfully commercialised this integration method, employing it for the production of silicon optical transceivers operating at 100 Gbit/s. However, the price of these components is at odds with the needs of silicon photonics, which requires a low-cost, high-yield, CMOS-compatible optical communication platform.

A more attractive alternative for bringing laser light to the silicon photonic chip is direct epitaxy. MBE and MOCVD have been used to grow III-Vs on silicon platforms. Recently, this has been shown to be an efficient way to fabricate silicon-based III-V lasers, due to the merits of low cost and large scale. However, despite significant demonstration of conventional Fabry-Pérot and distributed feedback lasers on III-V and silicon platforms, there is still the need for microscale and nanoscale laser devices with far lower energy consumption and optical mode control for silicon-based nanophotonic integrated circuits. Such circuits are promising candidates for next-generation quantum computing and optical microprocessors, and could be used to make microelectronic components for optical/photonic microprocessors.

Helping to lay the foundations for the development of miniature laser sources are the microdisk lasers, a triumph of the 1990s. At the heart of these devices are micro-resonators, a few micrometres in diameter. These structures support whispering-gallery modes, instrumental to single-mode lasing and low operating powers.

Photonic crystal cavities

Building on this concept – and shrinking the footprint of the laser while maintaining its excellent performance – are designs employing a photonic crystal cavity. Thanks to an enhanced light-matter interaction within the photonic cavity, the photonic crystal laser not only benefits from a smaller footprint that is nanoscale in size, but strong optical confinement that comes from the designed photonic bandgap (the primary strengths of the photonic crystal laser, compared with its edge-emitting variant, are listed in Table 1).

One option for integrating a photonic crystal laser with a silicon platform is to bond the light source to a silicon or silicon-on-insulator substrate. Several groups have done just that, including those at the University of Tokyo and the University of Paris-Saclay (see Figure 1 (a)). The greatest advantage of this technique is that it has the potential to couple laser emission to a waveguide, thereby creating a platform for nanophotonic integrated circuits along with other photonic components. However, yields can be very low, hampered by ultra-high requirements for alignment – a challenge that is magnified with micro and nanoscale fabrication.

Our team at UCL is pioneering a more straight-forward approach to fabricating silicon-based photonic crystal lasers, based on the use of direct epitaxy to deposit high-quality III-V materials on silicon (see Figure 1 (b)). This method promises to enable the simultaneous fabrication of many photonic crystal lasers, which significantly increases yield and makes massive production possible.

We have demonstrated the feasibility of massive production of photonic crystal lasers on silicon with our direct growth method by fabricating a nanobeam (one-dimensional photonic crystal) laser array (see Figure 2). Working in partnership with scientists from the Chinese University of Hong Kong and Grenoble Alpes University, we have broken new ground by developing the first III-V two-dimensional and one-dimensional photonic crystal lasers that are directly grown on silicon substrates.

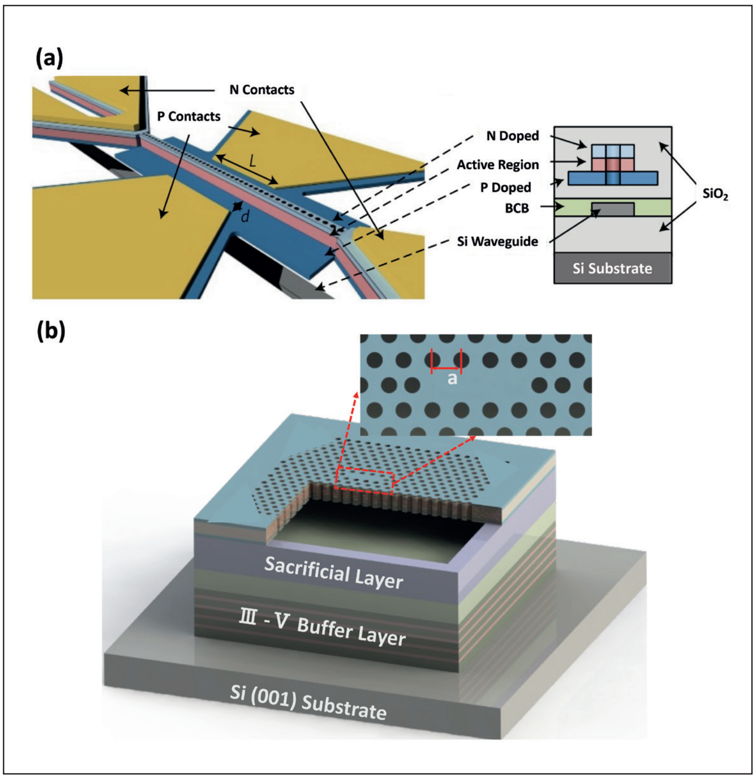
Growing on silicon

It is far from easy to grow high-quality III-V layers on silicon. Barriers to success include dissimilarities in material properties, such as differences in lattice constant, polarity and thermal expansion coefficient. These differences give rise to a high density of crystal defects, which trap numerous carriers, causing additional heating to the chip. Thus, it is crucial to epitaxially grow high-quality III-V materials on a silicon platform, because this is key to realising high-performance III-V lasers on silicon. We have excelled in this regard, growing III-V materials on silicon that have a crystal quality that is very close to that of the III-V native substrate.

To ensure high-crystal-quality III-V materials on silicon, we use a specially designed epitaxial buffer

	Edge-emitting laser	Photonic crystal laser
Footprint	Large	Small
Operating power	Low	Ultra-low
Output power	High	From Low to High
Fabrication cost	Low	Low-medium

Table 1. Comparison of the edge-emitting laser and the photonic crystal laser.



➤ Figure 1. Two different integration methods for photonic crystal lasers on silicon: (a) bonding a III-V nanobeam laser on silicon-on-insulator substrate via BCB material; (b) and direct growth of a III-V photonic crystal laser on a silicon substrate.

layer to prevent: a one-dimensional defect, namely threading dislocations; and a two-dimensional defect, antiphase boundaries. Working with our collaborators at Grenoble Alpes University, we have employed MOCVD to create double silicon atomic steps on the silicon (100) on-axis substrate to avoid formation of antiphase boundaries. The two-dimensional defects, antiphase boundaries, degrade device performance by splitting materials into different domains.

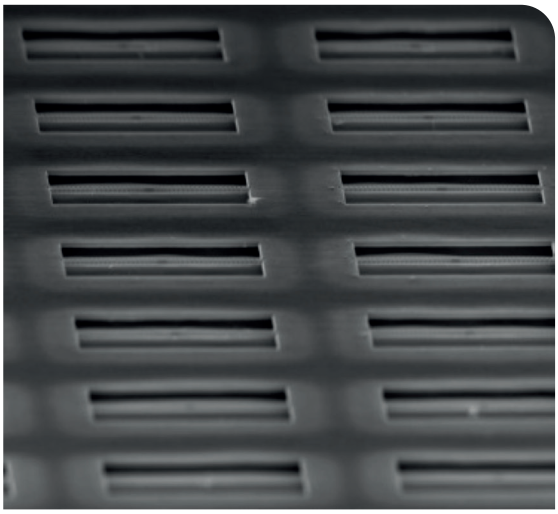
There's a need for this innovation, because prior to treatment, the silicon on-axis (001) surface is covered by single atomic steps. These single steps are to blame for forming antiphase boundaries, which arise when polar III-V materials are directly grown on the non-polar silicon surface.

By switching to a double atomic step, we avoid the formation of antiphase boundary. Evidence of this is provided by the use of hydrogen atoms to destroy the atomic bond between Si-Si atoms under high temperature. Thanks to these double atomic steps, we have grown on silicon a III-V, GaAs, that is free from antiphase boundary defects and has low roughness. Our approach has been widely used with 300 mm silicon substrates, highlighting its potential to slash fabrication costs compared with growth on III-V substrates, as well as the promise of processing our material with state-of-art CMOS fabrication equipment.

Another challenge of growing III-Vs on silicon is accommodating the large lattice mismatch that threatens to introduce a high density of threading dislocations – they could be in the region of 10^{10} cm^{-2} at the interface of III-Vs and silicon. The mismatch is significant: there's a difference of 4 percent between GaAs and silicon, and 7 percent between InP and silicon. Part of the solution is to introduce strained-layer superlattices, which have repeated layers of both tensile and compressive strain. When this is added, threading dislocation density fall to a practicable level for making a device of less than 10^{7} cm^{-2}. This is realised by pushing and pulling the propagation of threading dislocations into the horizontal direction, so they no longer impact the gain materials grown on top.

Additional improvement comes from a high-temperature annealing process, which encourages threading dislocations to move, encounter one another and merge. When annealing is combined with strained-layer superlattices and double atomic steps on silicon, the epitaxial quality of our photonic crystal lasers that are grown on silicon is comparable to heterostructures formed on native III-V substrates.

As well as a high crystal quality, our photonic-crystal lasers need a suitable active region. Over many years, quantum wells have provided gain material in various types of laser, due to their high output power and tremendous optical gain. But they are not ideal in our case, because residual threading dislocations are present in III-V materials grown on a silicon platform, even after careful design of the III-V buffer layer – and as the device operates, the number of threading dislocations grow, degrading device performance. The long-term impact is significant, including diminished output power, a shortened device lifetime and a hike in temperature instability.



➤ Figure 2. A scanning electron microscope image of a fabricated one-dimensional photonic crystal laser array.


Webinar

Drawing on dots

We have found that a far better alternative for providing gain is the self-assembled quantum dot. When dots are deployed in the active region, they have a high tolerance to threading dislocations – this could lead to threading dislocations forming closed loops, which reduce the extent of device degradation.

Employing the techniques mentioned above, we have produced optically pumped III-V quantum dot lasers on silicon that feature a photonic crystal cavity. These nanobeam lasers have many promising characteristics, including: an ultra-low threshold, with a pumping power below 1 μW; a nanoscale footprint of around 8 μm by 0.53 μm by 0.36 μm, for a one-dimensional photonic crystal cavity; and a high-temperature performance, exceeding 60 °C. These characteristics show that our nanobeam lasers could serve in silicon-based nanophotonic integrated circuits.

Our next challenge is to realise electrical operation with our photonic-crystal laser on a silicon platform. This can be accomplished by using ion implantation to introduce different *n*-type and *p*-type contact layers on the planar photonic crystal cavity.

It is worth noting that we have the opportunity to turn to some advance types of photonic-crystal cavity. They include the photonic crystal surface emitting laser (PCSEL), which combines the VCSEL's advantages of round beam shape and a high output power of more than 1 W with the high speed and low cost of the edge-emitting laser. Compared with the VCSEL, the PCSEL offers a simpler fabrication process, by using a photonic-crystal cavity to confine light horizontally. This approach avoids the process of oxidation in confining layers.

Another drawback of the VCSEL is that it requires a very high thickness of DBR, so growth of this class of laser on silicon would lead to a large volume of micro cracks, due to incompatible thermal expansion coefficients for the III-Vs and silicon. Turning to PCSELs-on-silicon would offer us a solution for realising high performance III-V surface-emitting lasers on a silicon platform.

When making any semiconductor laser, there are imperfections associated with light scattering at the non-smooth surface. This issue is more severe when using a nanofabrication process, and increases the difficulties of fabricating photonic crystal lasers.

A promising alternative is the topological laser, inspired by the topological insulator in electronics. Topological lasers are capable of guiding light within the designed photonic crystal pattern, and can avoid light scattering associated with imperfections in nanofabrication. Recently, working with colleagues at Grenoble Alpes University and The Chinese University of Hong Kong, we have demonstrated a topological laser with a photonic crystal cavity that's grown on the silicon substrate, thereby showing that this is a robust nanoscale light source for silicon photonics. Even though integrating the photonic crystal laser on a silicon platform is still at an the early stage, we are convinced that this source of light is destined to play a significant role in next-generation, silicon-based nanophotonic integrated circuits.

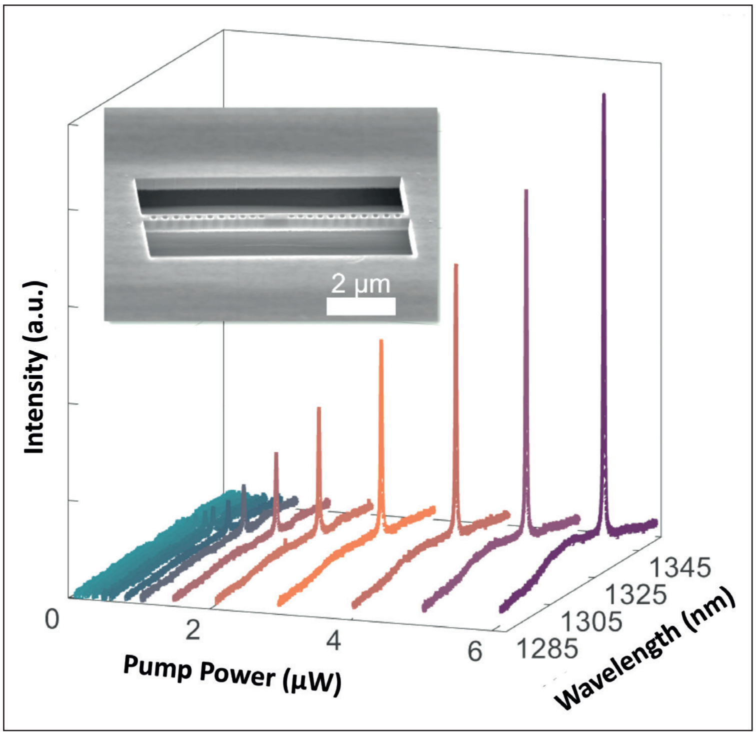


Figure 3. A nanobeam laser directly grown on silicon substrate with a nanoscale footprint and ultra-low threshold.

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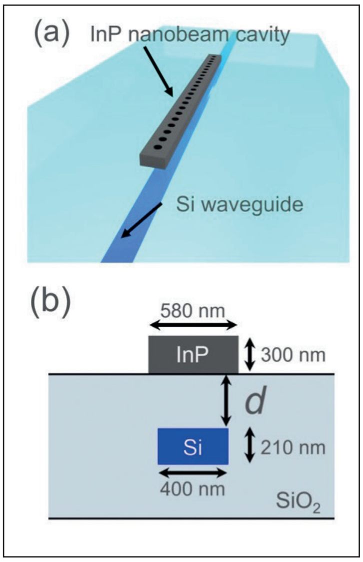
ANGEL EVENTS

Advancing quantum photonics with transfer printing

Transfer printing produces CMOS-compatible integration of a silicon platform with quantum-dot single-photon sources

A COLLABORATION between researchers in Japan and Germany is claiming to have broken new ground in the integration of single-photon sources and silicon photonic integrated circuits. According to the team, they are the first to unveil hybrid integration of quantum-dot single-photon sources in the telecom band with silicon photonic integrated circuits made in silicon foundries.



➤ (a) InP nanobeam cavities are positioned below the silicon waveguide by transfer printing. (b) Evanescent interaction ensures coupling between the waveguide and the cavity. Calculations indicate a quantum-dot-to-waveguide coupling efficiency of 99.4 percent for a value of *d* of 450 nm.

This advance by engineers from a number of institutions – Toyohashi University of Technology, The University of Tokyo, Keio University, The University of Electro-Communications and the University of Kassel – promises to aid the construction of large-scale quantum photonic integrated circuits. Such circuits could be used for quantum simulation, quantum communication and quantum machine learning.

Options for providing single-photon sources for quantum circuits include III-V quantum dots, colour centres in diamond and SiC, and defects in two-dimensional materials. Of these, there's much merit in InAs/InP quantum dots, according to team spokesman Ryota Katsumi, who is affiliated to Toyohashi University of Technology and The University of Tokyo.

Katsumi told *Compound Semiconductor* that quantum dots are ideal for meeting the requirements for single-photon sources, which include bright single-photon emission, high purity, deterministic operation and high indistinguishability. "It is difficult for other single-photon sources to perform all of these requirements at once."

The team's latest triumph builds on previous successes, including using transfer printing to realise the hybrid integration of InAs/GaAs quantum-dot single-photon sources on a CMOS-processed chip. For that work, the sources produced emission outside conventional communication bands. By now moving to the O and L bands via the switch from dots on GaAs to those on InP, the researchers are benefitting from low loss and low dispersion propagation through optical fibre – this is advantageous for long distance and secure quantum networks.

The latest work began with the growth of InAs quantum dots on an InP substrate via MBE. Using the addition of a hard mask, electron-beam lithography and dry and wet etch etching, photonic-crystal nanobeam cavities were formed from the epiwafers. Transfer printing re-located this structure to a silicon waveguide cladded with glass (see Figure).

Micro-photoluminescence measurements at 13K, using optical excitation from a 785 nm laser, produced a strong quantum-dot emission peak at 1436.9 nm and a fundamental cavity mode at 1436.2 nm. The single-photon coupling efficiency from the dots to the waveguide is 82 percent.

In the nanobeam cavities produced by the team around 10 quantum dots couple to the cavity. Some of these dots are outside the cavity's resonance, leading to background emission and a degradation of a key figure of merit known as g(2), which is a measure of the degree of second-order coherence.

"For purer single-photon emission, it is necessary to employ a single quantum dot," remarked Katsumi, who added that an attractive way to realise this is to produce epiwafers with a much lower quantum-dot density.

As well as improved purity of emission, integrated quantum photonic circuits need single-photon sources that are electrically driven, rather than optically pumped. According to Katsumi, the team's technology offers a way to do this. "Transfer printing could even be used for the implementation of the electrodes for electrical pumping on silicon."

To realise practical quantum photonic information processing, there needs to be efficient, plug-and-play coupling between single photons and fibre – this will ensure long-distance quantum networks. Katsumi and co-workers are targeting this, with efforts directed at making modularize solid-state single-photon sources by transfer printing. "This will enable the efficient and stable supply of single photons for future quantum applications."

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Enabling hydrogen purification for process equipment

BY ARM PURIFICATION

HYDROGEN is used in many processes in the semiconductor industry, such as annealing, epitaxial growth, lithography, and as a carrier gas for hydride dopants. The use of hydrogen gas in the semiconductor industry is increasing, and along with that increase come constraints on supply chains and markets. Hydrogen generation is becoming more prevalent, as well, in order to mitigate traditional supply chain issues such as trucking, plant shut downs, and more.

It's critical to utilize the right gas purifier when working with hydrogen. Applied Energy Systems (AES), the leading provider of high and ultra-high purity gas delivery systems, is focused on offering gas purification solutions for complex and myriad applications. AES's ARM Purification division recently introduced the redesigned APS60 series of purifiers, including the APS60-CXXX series of hydrogen purifiers (XXX is the flow in Nm3/hr). For any process, ARM Purification is equipped to handle hydrogen purification; traditionally utilizing H2 from liquid, tube trailers, and other sources and purifying it to 8N or 9N outlet quality.

Challenges with Traditional Heated Media-Based Purification Technology

While bulk purifiers have traditionally been utilized on systems providing fairly constant flow requirements, ARM Purification has introduced the ability to provide purified UHP 9N hydrogen gas in a process environment that demands high flow rate variations and fast response times for the success of the process. These systems are sized up to 300 Nm3/Hr and are fully PLC controlled with hydrogen safety features built into the unit.

Using traditional heated media-based purification technology for hydrogen purification is somewhat difficult in applications that require high flow rate variations, such as EPI, due to the construct of the material's reaction towards hydrogen. The traditional purification media, often a metal getter, reacts with hydrogen in a reversible manner, giving the ability to increase purifier vessel pressures and temperatures quickly upon flow demand through the unit. This is because the hydrogen can react exothermically with the media, and constitutes a reversible reaction in the media that is both temperature and pressure dependent.

Unlike oxygenated species and hydrocarbons, which are chemically bonded to the material upon reaction, the hydrogen goes into solid solution and is a reversible reaction. Therefore, under high flow requirements, the temperature increase needed to optimize purification efficiency must be monitored in real time, along with the pressure, in order to control the potential for increases in both, without the pressure loss associated with membrane H2 purifier technology.

Stringent Safety Considerations for Hydrogen Systems

The safety considerations of hydrogen systems are stringent – but with a solution like ARM's updated APS60 platform of purifiers, there exists the ability to automatically purge the purifier system with Argon gas, and provide for a safe system shut down in case of emergency. This shut down is then followed by an automatic process to re-introduce H2 into the media, thus providing a hydrogen compatible media to resume the purification of the hydrogen gas quickly and safely. All of these processes are PLC controlled and have been fine-tuned based on system user input and design engineering parameters, include HAZOPS analysis and best practices followed from AES' SEMI-GAS line of gas cabinet equipment, and SEMI guidelines. Some of the safety features considered standard are exhausted cabinets, Z-purge electronics, hydrogen gas sensors, and safety interlocks all designed for safe and efficient operation.

The challenges of taking a heated, getter-style hydrogen purifier from idle to full process flow conditions have been met by a combination of tight process controls which allow for temperature and flow changes quickly and effectively, and the possibility of user adjustment through the HMI within the process parameters set forth at the factory.

Solutions for Complex Challenges Made Possible with the Right Partner

ARM Purification is committed to delivering solutions for the semiconductor industry's various challenges. ARM includes Ethernet as a standard offering, and users now have the opportunity to provide UHP H2 and real time monitoring for process hydrogen in variable flow rates for processes that require it in the most demanding of semiconductor processes. The purifier system can be tied in to SCADA or process control systems for full visibility, and comes standard with sub-micron particle filtration, and the availability of industry leading 1.5 nm filtration. If you have a hydrogen delivery application that could benefit from 9N hydrogen, but the flow variations in the process, or the high pressure loss of membrane purification technology have kept you from considering purification; ARM Purification has the product that excels under these delivery system constraints.

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E: shehzad.munshi@angelbc.com
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