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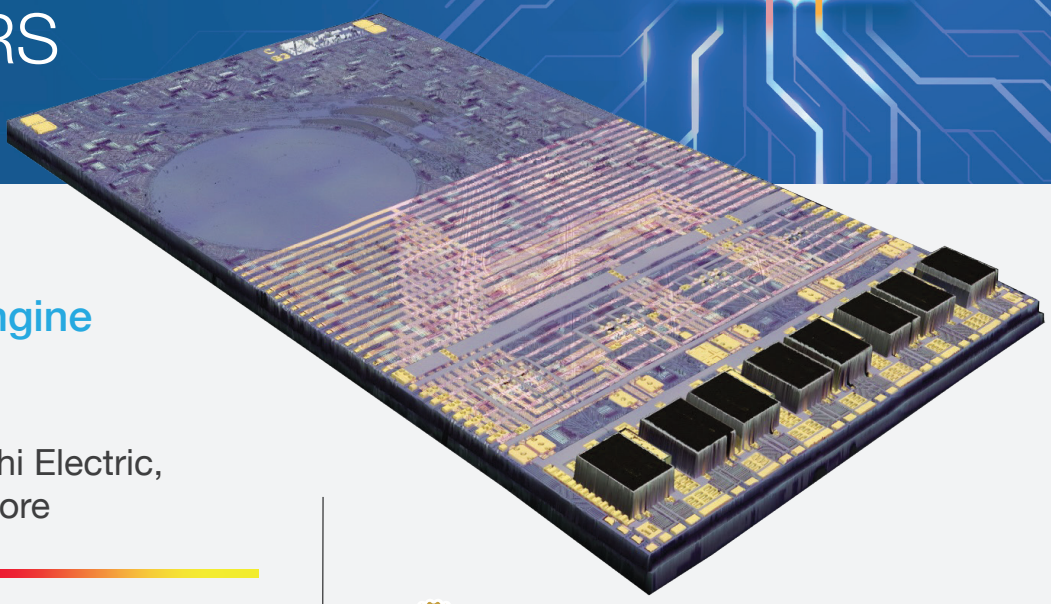

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VIEWPOINT

BY LAURA HISCOTT, EDITOR

To disrupt or not to disrupt

ACROSS THE tech industry, new innovations are often hailed as being disruptive, conjuring a vision of the latest products rapidly displacing incumbent solutions and heralding a step change in technological possibilities.

Yet, at the same time, companies often take care to emphasise that their new products will enable better performance without being too disruptive – reassuring customers that they conform to existing frameworks and can be swapped in with minimal hassle.

This apparent contradiction came up in a recent roundtable on PICs for enabling datacentres. After all, this is the sector that must adapt to keep up with skyrocketing data needs, but it also has a large and complex network of existing infrastructure; if possible, operators would rather avoid more extensive modifications, and the costs and downtime they might incur.

Perhaps this is an advantage for PIC products targeting other applications, like navigation or biomedical devices, which operate more independently and may therefore be freer to adopt the optimal design without needing to fit seamlessly into a large existing system. Yet these products are also under pressure to be compatible with established fabrication processes, particularly as they move from prototype to mass manufacturing.

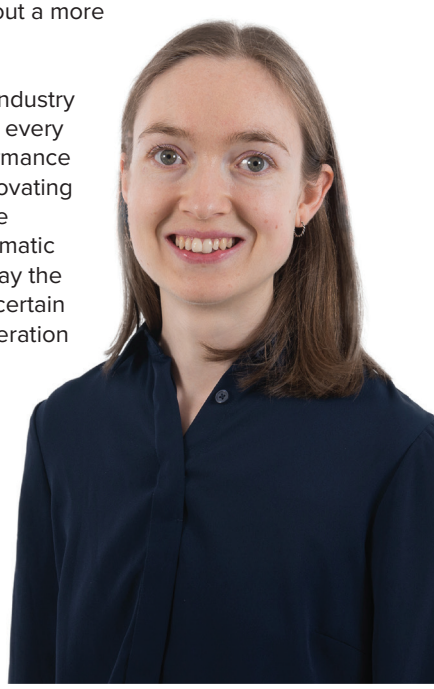
So, for all kinds of products, there are incentives in both directions. On the one hand, if we opt for less disruption, we might wonder if we are missing an opportunity for a larger leap in favour of smaller improvements. On the other hand, maybe a bird in the hand is worth two in the bush; perhaps it is better to have a product that offers a significant performance increase and can be readily manufactured at scale, than to chase the highest possible theoretical performance even if that solution is less feasible to ramp up.

Is it possible to get the best of both worlds? And if not, what should we prioritise? The answers to these

questions most likely change as time goes on. There are certainly products and processes being developed that promise to offer disruptive performance while fitting in smoothly with the surrounding ecosystem, whether at the point of fabrication or deployment.

But sometimes, the world evolves so much that nothing short of a complete overhaul will suffice. Maybe the continued rise of AI will eventually bring the datacentre industry to a tipping point, where data demands overcome the inertia of incremental, minimally disruptive improvements, and bring about a more sudden, large-scale change.

Fortunately, the diverse PIC industry is coming up with answers at every level, already realising performance improvements while also innovating novel approaches that can be ready to step in if a more dramatic shift is needed. Whichever way the landscape unfolds, PICs are certain to be at the core of next-generation technologies.



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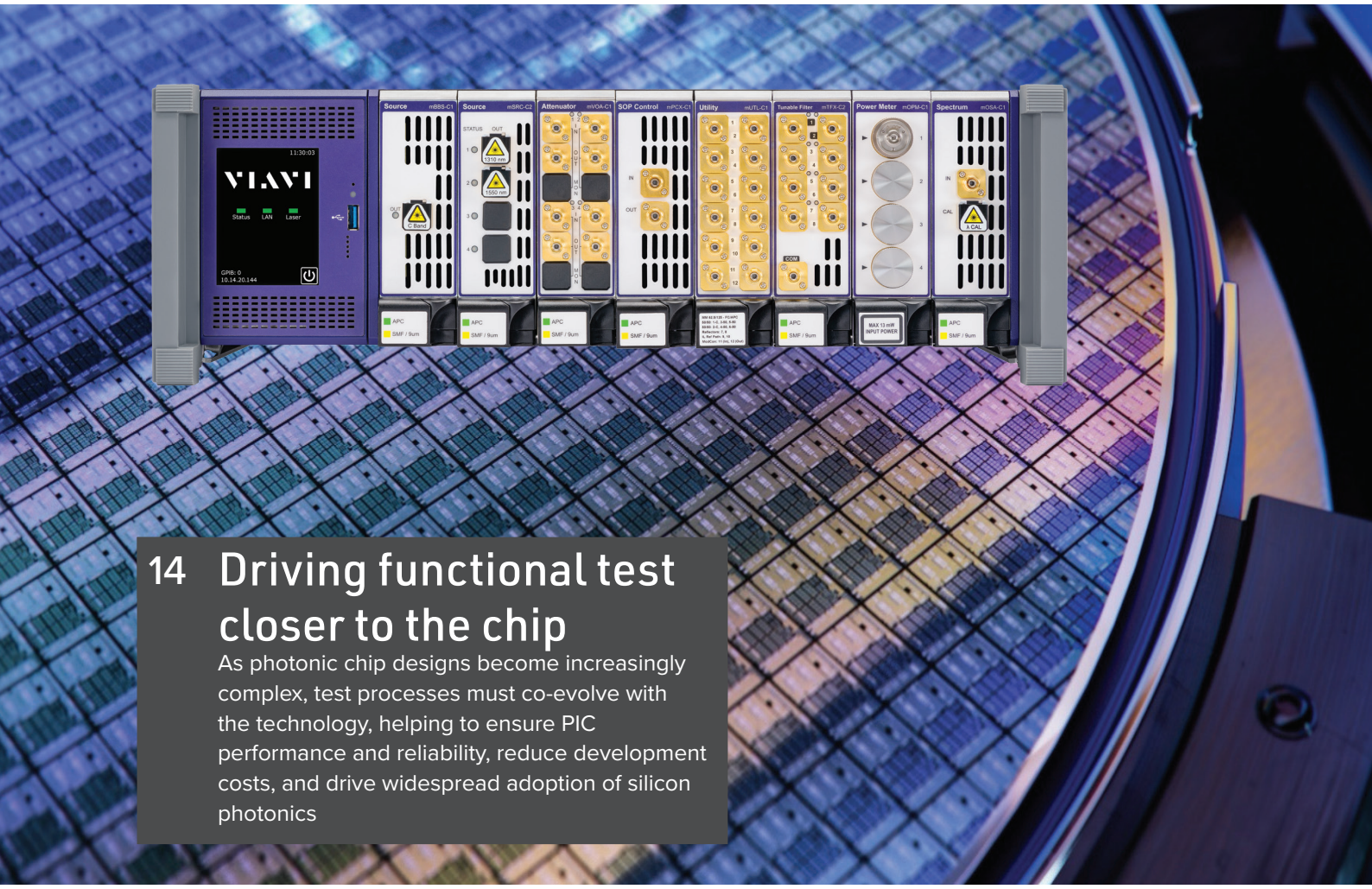


14 Driving functional test closer to the chip

As photonic chip designs become increasingly complex, test processes must co-evolve with the technology, helping to ensure PIC performance and reliability, reduce development costs, and drive widespread adoption of silicon photonics

18 Revolutionising telecoms with the world's smallest fully optical amplifier

A compact erbium-doped waveguide amplifier achieves record-breaking performance, heralding a new era for integrated photonics in data communication, sensing, and beyond

24 Propelling PICs from idea to MVP in under 12 months

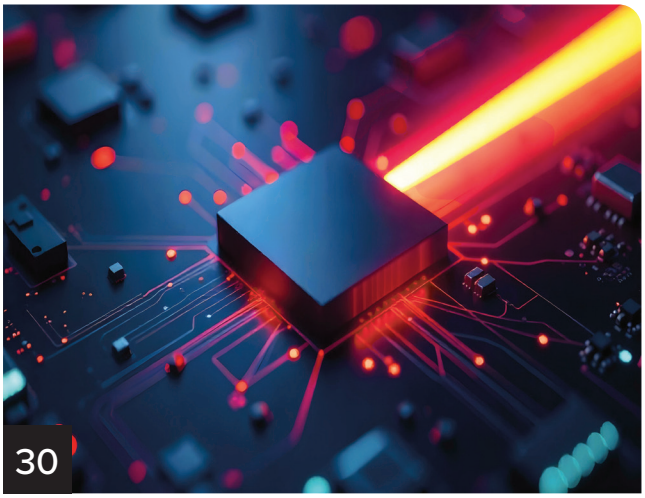
Light Trace Photonics has developed a cutting-edge pipeline for developing new integrated photonic products quickly and effectively, supporting companies with technical feasibility studies, proven component IP, and circuit-on-a-chip evaluation modules

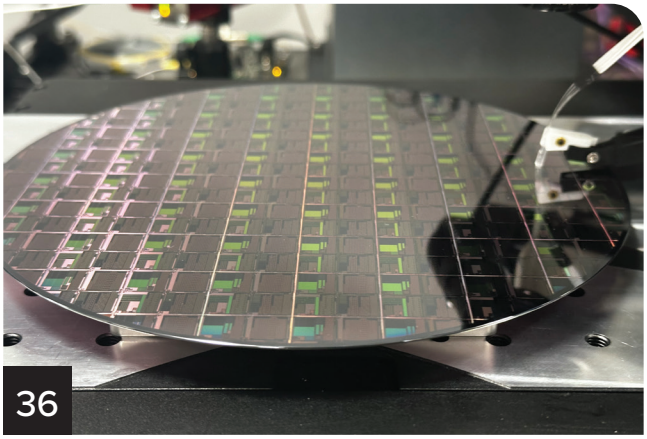
30 A PIC laser designed for reliability and volume production

In the era of massive AI data compute and transmission demand, optical chip innovations must look beyond basic performance metrics with designs that accelerate PIC manufacturability

36 Driving the next high-volume sensor revolution

Zero Point Motion is pioneering photonically enhanced inertial sensors, revealing how silicon photonics can break free from datacentres and become ubiquitous in everyday devices, but this transformation will require industry-wide cooperation





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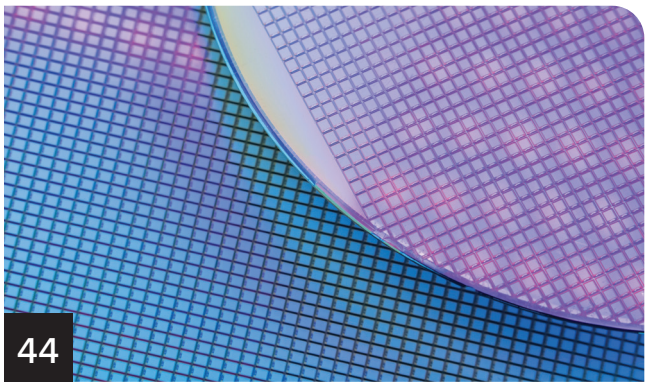
40 An outlook on the evolution of PICs for future interconnects

Optical transceivers' capacity has historically grown by 1 dB per year. AI now requires more rapid advances towards 100T or beyond over the next decade. Numerous promising technologies could overcome current bottlenecks

44 200G+ per lane: powering the next-gen data deluge

Integrated photonics is pushing the boundaries of data transmission, enabling speeds of 200G per lane and beyond. This leap forward promises to revolutionise datacentres and telecommunications, addressing the ever-growing demand for bandwidth driven by the proliferation of AI/ML



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South Devon College upgrades training programme with LightPort:Edu

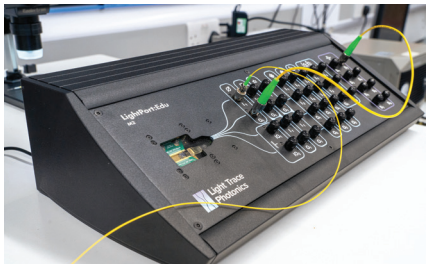
The college's PIC Packaging Academy (PICPAC) initiative delivers bespoke courses to address critical skills shortages in the optoelectronics and photonics industry

SOUTH DEVON COLLEGE has secured its position as a leader in photonics training, having recently taken delivery of a cutting-edge new piece of kit, which will offer more opportunities for its students and delegates to develop hands-on practical skills.

Home to the Torbay Hi-Tech Cluster, which brings together a growing number of innovative technology companies, the South Devon region is a specialist hub for photonics and microelectronics. The Paignton-based college and the University Centre South Devon have played a pivotal role in the growth of this sector, particularly through their innovative PIC Packaging ACademy (PICPAC) project.

This pioneering initiative, coordinated in collaboration with photonics specialists Bay Photonics and Davies & Bell, sees South Devon College become the first further education college to partner on a winning Innovate UK bid, delivering bespoke courses on Design for Manufacture, Photonic Systems, Photonic Wafer Fabrication, PIC Packaging, and PIC Assembly and Testing, to attendees from across the UK. These programmes address some of the key skills shortages currently facing the microelectronics, optoelectronics, and photonics engineering sectors.

Further enhancing these activities, the college has now invested in and installed a LightPort:Edu box from Light Trace Photonics in its £17 million Hi-Tech & Digital Centre. This makes South Devon College the only education provider in the UK to currently have this equipment, aside from the University of Bristol, creating further training opportunities and transforming the institute into a national centre for semiconductor photonic packaging



training. The college plans to use the new kit across its curriculum and industrial classes, adding to its growing face-to-face training capabilities.

As a skills provider, South Devon College is acutely aware of the challenges with traditional didactic lecturing in highly technical subjects. The LightPort:Edu box, together with all the college's other hands-on practical skills kit in the Kao Hockham training suite, is a fantastic opportunity for students to get direct, tangible experience with photonics and microelectronics packaging equipment and processes. By correlating theory with practice, this equipment improves and enhances the learning experience and journey for students, delegates, and all learners.

Offering options to manipulate light in several different ways, the new hardware is designed to mimic real telecoms and datacoms network challenges. For example, students can stress the fibre and change the polarity of light, or manipulate the light's amplitude and polarity by altering distinct functions built into the PIC structure itself, before finally receiving the light into the port of eight photodiodes.

The equipment contains phase shifters, tuneable delays, variable reflectors, variable attenuators, variable beam splitters, polarisation beam splitters, and wavelength multiplexers. Together with the accompanying integrated software, it provides at least 20 different lesson plans and training modules, programmed with Python coding, which will also benefit digital skills and coding students.

By giving a huge boost to practical, hands-on training, the LightPort:Edu will help South Devon College deliver its successful PICPAC courses alongside its photonics training more broadly.

And, being a portable piece of kit, it can be taken out on the road, travelling to businesses around the country for in-house training after completion of the college's theoretical online courses.

The college's suite of bespoke online and in-person short courses on microelectronics and photonics, some of which are a result of investment by the UK Shared Prosperity Fund provision, focus on developing manufacturing skills. Delivered by industry experts and highly qualified specialist teaching staff, these training resources put the college in a dominant position to provide the training and upskilling required to foster the booming photonics industry.

The college has developed new partnerships with specialist businesses including PandA Europe, Tribus-D, Micro Engineering Consultancy Ltd, and Light Trace Photonics, to help develop and deliver the courses.

In recognition of its industry standing, South Devon College recently hosted POP4, the fourth edition of the prestigious International Conference and Exhibition on Photonics and Opto-Electronics Packaging, in partnership with IMAPS-UK and the Torbay Hi-Tech Cluster, with visiting international delegates.

Q.ANT and IMS CHIPS launch production line for photonic chips for AI

The company is repurposing the existing facility at the Institute of Microelectronics Stuttgart to produce high-performance, energy-efficient TFLN-based photonic processors, marking a significant semiconductor manufacturing milestone

Q.ANT, a company focusing on photonic processing for AI, has announced the launch of a dedicated production line for its high-performance photonic AI chips at the Institute of Microelectronics Stuttgart (IMS CHIPS). By integrating Q.ANT's patented photonic chip technology on the base of thin-film lithium niobate (TFLN) and upcycling the existing CMOS production facility, Q.ANT and IMS CHIPS say they have established a first-of-its-kind manufacturing line to accelerate the production of energy-efficient, high-performance processors for AI applications. Q.ANT has invested €14 million in machinery and equipment to complement the new line.

According to the company, this manufacturing approach delivers faster, more energy-efficient processors to meet the growing computational demands of AI and high-performance computing (HPC), while also establishing a blueprint for cost-effectively modernising chip production worldwide, and for democratising production capacity. It aims to enable countries to attain greater semiconductor manufacturing resilience, reduce dependency on global supply chains, and accelerate the development of critical technologies that drive innovation across datacentres, research institutions, and advanced industries.

The official launch event, attended by leading industry figures and German officials, underscored the project's significance in driving innovation within the European and global semiconductor ecosystem. By modernising existing chip production capabilities, Q.ANT and IMS CHIPS say they have pioneered a scalable approach to bringing energy-efficient AI processors to the market at a faster pace, more cost-effectively, and more sustainably.

Q.ANT's photonic chips – which compute using light instead of electricity – deliver a 30-fold increase in energy efficiency and a 50-fold boost in computing speed, offering transformative potential for AI-driven datacentres and HPC environments, the company says. The pilot line is specifically designed for production using TFLN, the optimal material for photonic computing and critical to the success of the technology.

TFLN enables ultra-fast optical signal manipulation at several GHz without the need for heat to modulate the light on the photonic circuit. This advantage leads to more precise and energy-efficient control of the light, resulting in a significant increase in computing power and energy efficiency compared to traditional silicon.

"This approach establishes a new benchmark for AI chip manufacturing, providing a path towards greater self-sufficiency and more energy-efficient chip solutions," says Michael Förtsch, CEO of Q.ANT. "As AI and data-intensive applications push conventional semiconductor technology to its limits, we need to rethink the way we approach computing at the core. Q.ANT is driving this shift with photonic computing to achieve unprecedented energy efficiency and computational density.

"With this pilot line, we are accelerating time to market and laying the foundation for photonic processors to become standard coprocessors in high-performance computing. This milestone marks a major step toward the future of sustainable AI chip technology, engineered and produced in Germany for a rapidly evolving global market. By 2030, we aim to make our photonic processors a scalable, energy-efficient cornerstone of AI infrastructure."

Image credit: Q.ANT

Jens Anders, director and CEO of IMS CHIPS, said: "This pilot line at IMS CHIPS demonstrates how transformative technologies can thrive on existing infrastructure, setting a blueprint for energy-efficient next-generation computing. This comes at a critical time for the computing industry, as the exponential growth of AI and data-intensive applications will soon overwhelm the current datacentre infrastructure. By partnering with Q.ANT, we are leveraging our semiconductor manufacturing expertise to accelerate the industrialisation of photonic processors and establish a scalable model for energy-efficient computing – a crucial step for the future of AI."

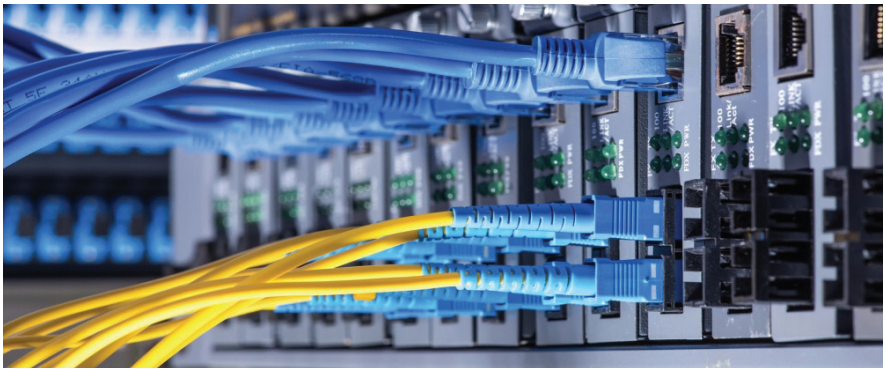
Capable of producing up to 1000 wafers per year, Q.ANT says the pilot line enables it to refine its chip architecture to meet evolving market requirements. It also serves as the R&D basis for the company's photonic Native Processing Units and Native Processing Server (NPS) solutions designed to power high-performance computing datacentres.

Q.ANT has demonstrated the potential of its technology in cloud-accessible AI inference demos. With PCIe integration, the company says its Native Processing Servers can seamlessly integrate into existing HPC servers, accelerating adoption across industries.

STMicroelectronics announces silicon photonics for datacentres and AI

In partnership with Amazon Web Services, the company has developed a new silicon photonics chip combined with BiCMOS technology, which it says will enable higher-performance, energy-efficient optical interconnects

STMICROELECTRONICS is unveiling its next generation of proprietary technologies for higher-performing optical interconnects in datacentres and AI clusters. With the exponential growth of AI computing needs, challenges arise in performance and energy efficiency across computing, memory, power supply, and the interconnections linking them. The company says it is helping hyperscalers, and the leading optical module provider, overcome those challenges with new silicon photonics and next-generation BiCMOS technologies, scheduled to ramp up from the second half of 2025 for 800G and 1.6T optical modules.



At the heart of interconnections in a datacentre are thousands, or even hundreds of thousands, of optical transceivers. These devices convert optical into electrical signals and vice versa to allow data flow between graphics processing unit (GPU) computing resources, switches, and storage. Inside these transceivers, ST says its new, proprietary silicon photonics technology will bring customers the ability to integrate multiple complex components into one single chip, while the company's next-generation, proprietary BiCMOS technology brings ultra-high-speed and low-power optical connectivity – key to sustaining AI growth.

"AI demand is accelerating the adoption of high-speed communication technology within the datacentre ecosystem. This is the right time for ST to introduce new power-efficient silicon photonics technology and complementing it with a new generation of BiCMOS for our customers to design the next wave of optical interconnect products, which will enable 800G/1.6T solutions for the hyperscalers," said Remi El-Ouazzane, president of the microcontrollers, digital ICs and RF products group at STMicroelectronics. "Both technologies will be manufactured on 300 mm processes in Europe, bringing customers an independent high-volume supply for two key components of their optical module development strategy.

"Today's announcement represents the first step for our PIC product-family and, thanks to close collaboration with key partners across the entire value chain, our ambition is to become a key supplier of silicon photonics and BiCMOS wafers for the datacentre and AI cluster market, be it pluggable optics today or optical I/O tomorrow."

AI demand is accelerating the adoption of high-speed communication technology within the datacentre ecosystem. This is the right time for ST to introduce new power-efficient silicon photonics technology and complementing it with a new generation of BiCMOS for our customers to design the next wave of optical interconnect products

Nafea Bshara, vice president and distinguished engineer at Amazon Web Services, said: "AWS is pleased to collaborate with STMicroelectronics to develop a new silicon photonics technology, PIC100, that will enable interconnection between any workload including AI. AWS is working with STMicroelectronics based on their demonstrated capability to make PIC100 a leading silicon photonics technology for the optical and AI market. We are enthusiastic about the potential innovations this will unlock for silicon photonics."

Vladimir Kozlov, CEO and chief analyst at LightCounting, commented: "The pluggable optics for datacentre market is experiencing significant growth, valued at $7 billion in 2024. This market is expected to grow at a compound annual growth rate (CAGR) of 23 percent during 2025-2030 to exceed $24 billion at the end of this period. Market share of transceivers based on silicon photonics modulators will increase from 30 percent in 2024 to 60 percent by 2030."

Lumotive raises $45 million for programmable optical semiconductors

The company says it will use the investment to expand its operations and sales of its chip-level beam steering technology worldwide, as well as accelerating growth in the areas of datacentre AI infrastructure and defence and aerospace

LUMOTIVE, a company focusing on programmable optical semiconductor products, has announced it has closed a $45 million Series B funding round to accelerate sales growth of its Light Control Metasurface (LCM) technology. The oversubscribed round included new investors Swisscom Ventures, East Bridge, EDOM, Grazia, Hokuyo Inc. and TSVC, as well as support from existing investors such as Gates Frontier, MetaVC Partners, Quan Funds, USAA, and HiMax Inc.

"This funding marks a pivotal moment in the evolution of programmable optics," said Sam Heidari, CEO of Lumotive. "Our LCM technology has already driven innovation across autonomous vehicles, advanced robotics, and industrial applications. With this new investment, we will accelerate sales in other new markets, particularly in AI datacentres and satellite communications."

Lumotive plans to use the new funding to scale its operations worldwide to meet growing demand from customers and partners in critical industries. By strengthening its international presence, the company says it will provide responsive, localised support and customised solutions tailored to specific technical and business needs.

Another strategic area Lumotive aims to accelerate growth in is datacentre AI infrastructure; by advancing high-performance optical switching solutions, the company says it is reshaping datacentre architectures. According to Lumotive, its two-dimensional LCM beam steering technology enables ultra-reliable optical circuit switches with thousands of ports and rapid switching speeds, addressing the demands of hyperscale and AI-driven networks. This technology is being deployed to support AI model training, real-time analytics, and energy-efficient hyperscale infrastructure management.

Additionally, the company says that the new investment will help it to continue advancing next-generation optical semiconductors for defence and aerospace applications, enhancing secure communications, advanced sensing, and mission-critical precision.

"Lumotive's unique technology represents a fundamental advance in optical semiconductors," said Pär Lange, investment partner at Swisscom Ventures. "Their proven success in automotive and industrial markets, combined with their ability to precisely control light at the chip level, enables applications that were previously impossible."

Conrad Burke, managing partner at MetaVC Partners, added: "Having supported Lumotive since its earliest days, we've witnessed the rapid evolution of the company's core technology and its expansion into diverse global markets. This new funding round marks an exciting milestone in the company's growth."

Photonic announces breakthrough in quantum error correction

The Canada-based start-up has published a paper demonstrating a technique that could enable quantum algorithms to run on up to 20x fewer physical qubits than in traditional error-correction techniques, accelerating the timeline to useful quantum computing

QUANTUM computing start-up Photonic has announced breakthrough results in error correction, which it describes as an industry first that will accelerate the timeline to useful quantum computing. The company has introduced a new, low-overhead family of Quantum Low-Density Parity Check (QLDPC) codes, which it says can efficiently perform both quantum computation and error correction, using materially fewer quantum bits (qubits) than traditional surface code approaches.

"Unlocking the quantum logic of high-performance QLDPC codes has been the holy grail of quantum error correction R&D for decades, and one of the obstacles to cost-effective quantum computing at scale," said Stephanie Simmons, chief quantum officer at Photonic.

"Today we're announcing that we have cracked these codes. Today we're launching fast and lean QLDPC codes, called SHYPS codes, that can run all quantum algorithms using up to 20x fewer physical qubits compared to the traditional approaches to error correction. We're excited to share these milestone results which have moved the goalposts for useful quantum computing 20x closer."

Quantum computers require error correction to realise the promised exponential speedups over known classical approaches for key computational challenges. Using surface code for error-correction introduces enormous overhead requirements for systems at scale – millions of physical qubits are needed to collectively act as the thousands of logical qubits required for impactful applications. These assumptions have contributed to 30+ year projections of when quantum will become "real" in the market.

According to Photonic, QLDPC codes were introduced 20 years ago and provide a promising alternative to reduce overheads by 10-100x.

However, there was one catch; the ability to perform quantum logic using QLDPC codes first had to be unlocked, a challenge that researchers have spent over a decade tackling.
Photonic says its new paper, "Computing Efficiently in QLDPC Codes," is the first to demonstrate how to compute using SHYPS QLDPC codes. This breakthrough simultaneously delivers the efficiency gains promised by QLDPC codes and removes a key barrier to commercially useful quantum applications.

According to Photonic, this fast and lean, patent-pending QLDPC code family has specific hardware requirements for implementation that not every approach to quantum computing can deliver. The start-up says its Entanglement First architecture provides the high levels of connectivity needed to realise the benefits of QLDPC codes.

These codes have been stress tested in the most complete simulations known to date, demonstrating that the logic works in practice, not just in theory, and the approach is implementable on distributed systems, working both within and between modules, the company adds.

Pixel Photonics wins €1 million for multi-mode single-photon detectors

PIXEL PHOTONICS has announced it has received a grant of €1 million from the German Federal Agency for Breakthrough Innovation (SPRIND) to further develop its waveguide-integrated superconducting nanowire single-photon detectors (WI-SNSPDs) for multi-mode detection. The company says this development represents a technological breakthrough in ultra-precise photon detection and enables new applications in fields such as microscopy, diagnostics, and laser communication.

Light is the central information carrier in numerous high-tech applications, from microscopy and telecommunications to quantum computing.

Highly sensitive detectors are essential for reliably detecting even the lowest signal strengths, with SNSPDs currently being the detectors of choice.

Pixel Photonics says it has already set milestones in scalability and sensitivity with the integration of SNSPDs with photonic waveguides.

However, existing highly efficient detector solutions, especially in the near-infrared spectral range, are often limited to light in a single optical mode, making interfacing with many applications challenging, especially in life sciences, microscopy, diagnostics and LiDAR, which typically work with multimodal light. This is where Pixel Photonics aims to help; with the new support from SPRIND, the start-up plans to advance a multi-mode adaptation of its detection technology.

CORNERSTONE Photonics Innovation Centre launches at House of Lords

The C-PIC aims to accelerate the commercialisation of silicon photonics technologies through rapid prototyping services and an innovation network, and has opened its first call for industry-driven projects that solve real-world problems

ON WEDNESDAY 12 February, the UK photonics community gathered at the House of Lords in London to celebrate the official launch of the CORNERSTONE Photonics Innovation Centre (C-PIC). As the UK's primary technology hub for silicon photonics, the C-PIC is designed to accelerate the commercialisation of innovations through state-of-the-art prototyping and an array of other services intended to foster a flourishing ecosystem.

CORNERSTONE was originally established in 2014 as a rapid prototyping foundry to support academic research in silicon photonics. Based in Southampton, it is affiliated with the University of Southampton and the University of Glasgow, as well as the UK government's Science and Technology Facilities Council (STFC), and was launched with a grant from the Engineering and Physical Sciences Research Council (EPSRC).

In 2023 the number of CORNERSTONE's industrial partners overtook the number of its academic partners for the first time, reflecting the growing number of start-ups translating silicon photonics innovations from the lab into products for the market. Last year, CORNERSTONE won £11 million in funding from the EPSRC and Innovate UK to build on its existing achievements and create the C-PIC, with the goal of catalysing the commercialisation of silicon photonics technologies.

Opening the launch event, Lord Sewell of Sanderstead spoke about the opportunities for the UK to take the lead in many emerging sectors within the rapidly growing photonics industry.

Graham Reed, a professor at the University of Southampton and principal investigator at the C-PIC, described CORNERSTONE's journey so far, as well as highlighting the strength of the wider photonics industry across the UK. Pointing out that the sector contributed an output of £15.2 billion to the UK economy in 2023, he emphasised that it is on a steep upwards trajectory, with a projected compound annual growth rate of 20-25 percent.

Dave Smith, the UK National Technology Advisor, reiterated the economic importance of the photonics industry and described the diverse applications, from AI and autonomous vehicles to improved biomedical devices and quantum technologies.

In addition to offering flexible prototyping and creating an effective pipeline capable of driving the development and large-scale adoption of silicon photonics technologies, the C-PIC plans to nurture the growing community comprehensively by establishing a network for innovation, supporting cross-sector engagement, and promoting the integration of research and business interests.

"The launch of the CORNERSTONE Photonics Innovation Centre marks a significant milestone in furthering the UK's position as a global leader in silicon photonics innovation," said Graham Reed. "By fostering a collaborative environment between academia and industry, we will accelerate the translation of cutting-edge research into transformative commercial technologies. This initiative will not only enhance our high-tech economy but also pave the way for advancements in critical sectors such as telecommunications, healthcare, and environmental monitoring."

CORNERSTONE currently has 70 UK-based partners and more than 100 in total. Last year, it was also announced that the C-PIC will be one of two UK institutes to participate in the PIXEurope consortium, a collaboration of organisations across Europe that has been selected by the European Commission and the Chips Joint Undertaking to develop a pilot line for photonic chips, to support the goal of European technological sovereignty.

The C-PIC has already opened its first call for industry-driven, academic-led photonics projects focused on solving real-world problems. Out of a £2 million innovation funding launch, the centre has up to £500 000 available to support the first round of selected projects. The deadline for submissions is 9 April 2025.

Salience Labs raises $30 million Series A

The company, which is developing optical switches for connectivity between AI clusters, has also announced the appointment of a new board member and a new chief financial officer

SALIENCE LABS, a company focusing on photonic solutions targeting connectivity for AI datacentre infrastructure, has announced the successful close of $30 million in Series A financing led by ICM HPQC Fund and Applied Ventures, LLC, the venture capital arm of Applied Materials, Inc., to further the development of its optical switches for large-scale AI connectivity.

Applied Ventures and ICM HPQC Fund are joined by Strategic Investment Fund, Braavos, and continued participation from existing investors Oxford Sciences Enterprises, Cambridge Innovation Capital, and leaders from the global semiconductor industry including Silicon Catalyst and Jalal Bagherli.

"What our customers want is a photonic switch to connect their AI clusters that is compatible with existing infrastructure while delivering high bandwidth, low latency and significant power savings. The completion of this round will further our development and help us bring our product to customers to enable not just the savings, but large cluster connectivity," said Vaysh Kewada, co-founder and CEO of Salience Labs. "We are also excited to be working closely with our strategic investors who are industry leaders to advance our go-to market schedule."

Anand Kamannavar, VP and global head of Applied Ventures, said: "Silicon photonics is a promising technology to deliver significant advancements in energy-efficient performance for AI datacentres. Salience's optical switch solution has the potential to enable a new generation of interconnect network architectures for faster and more efficient AI systems."

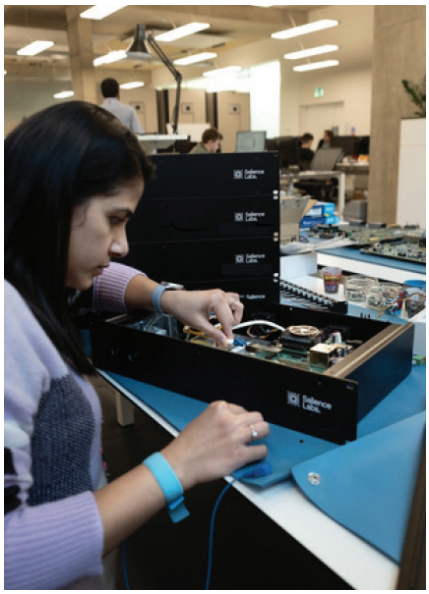


Image credit: Shabbir Bashar

In conjunction with the closing of the Series A financing, Salience Labs is appointing William Jeffrey to the board of directors. Jeffrey is an astronomer whose career has included working in the Executive Office of the President of the United States, leading HRL Laboratories, directing the National Institute of Standards and Technology, and serving as CEO of SRI International.

Salience Labs is also announcing its appointment of Bonnie Tomei, a certified public accountant located in Silicon Valley, California, as chief financial officer.

"With over 20 years of experience including initial public offerings, de-SPAC and a strong business operations background, Ms. Tomei will be a key member of the executive team to realise our strategic and operational objectives, including expanding to the US to serve our key customers," said Kewada.

PhotonFirst and Superlight Photonics extend collaboration

PHOTONFIRST has announced it is strengthening its collaboration with Superlight Photonics, a developer of supercontinuum generation lasers. Together, the companies aim to push the boundaries of photonics innovation, combining their expertise to accelerate the development of cutting-edge laser solutions.

Within this partnership, PhotonFirst and Superlight Photonics are working side by side on PIC packaging process development, with a particular focus on critical elements such as fibre-to-chip coupling.

According to PhotonFirst, the added value of this collaboration lies in its expertise in fibre-to-chip coupling, ensuring efficient and reliable connections, and in its proven product and PIC packaging process development, bringing almost 20 years of success in designing scalable, reliable solutions. The company adds that its team is committed to delivering fast, flexible, and innovative support tailored to Superlight Photonics' needs.

This collaboration underscores PhotonFirst's dedication to enabling the next generation of photonics applications, empowering its partners to lead in their fields. Together with Superlight Photonics, the company aims to pave the way for breakthroughs in laser technology.

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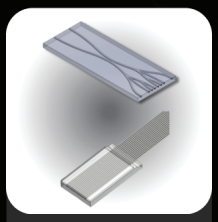
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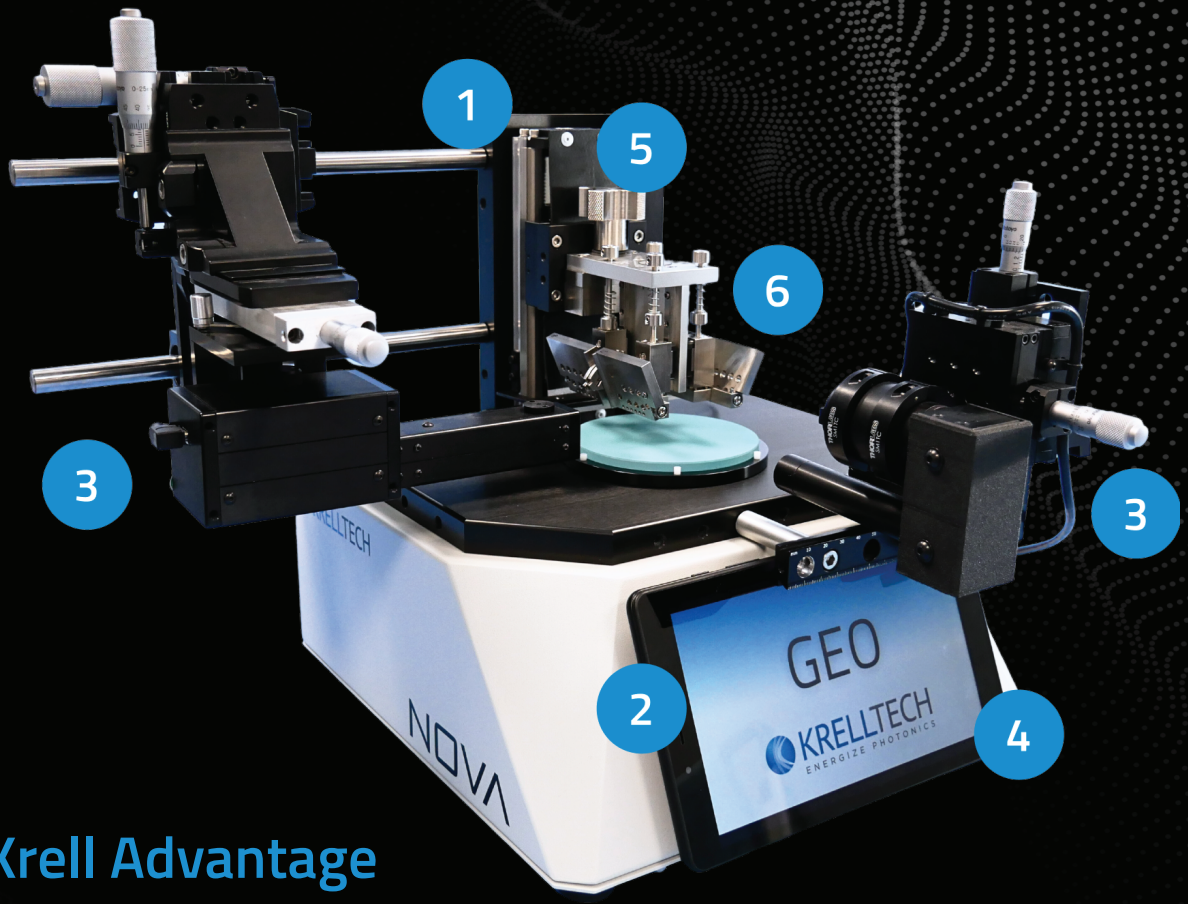

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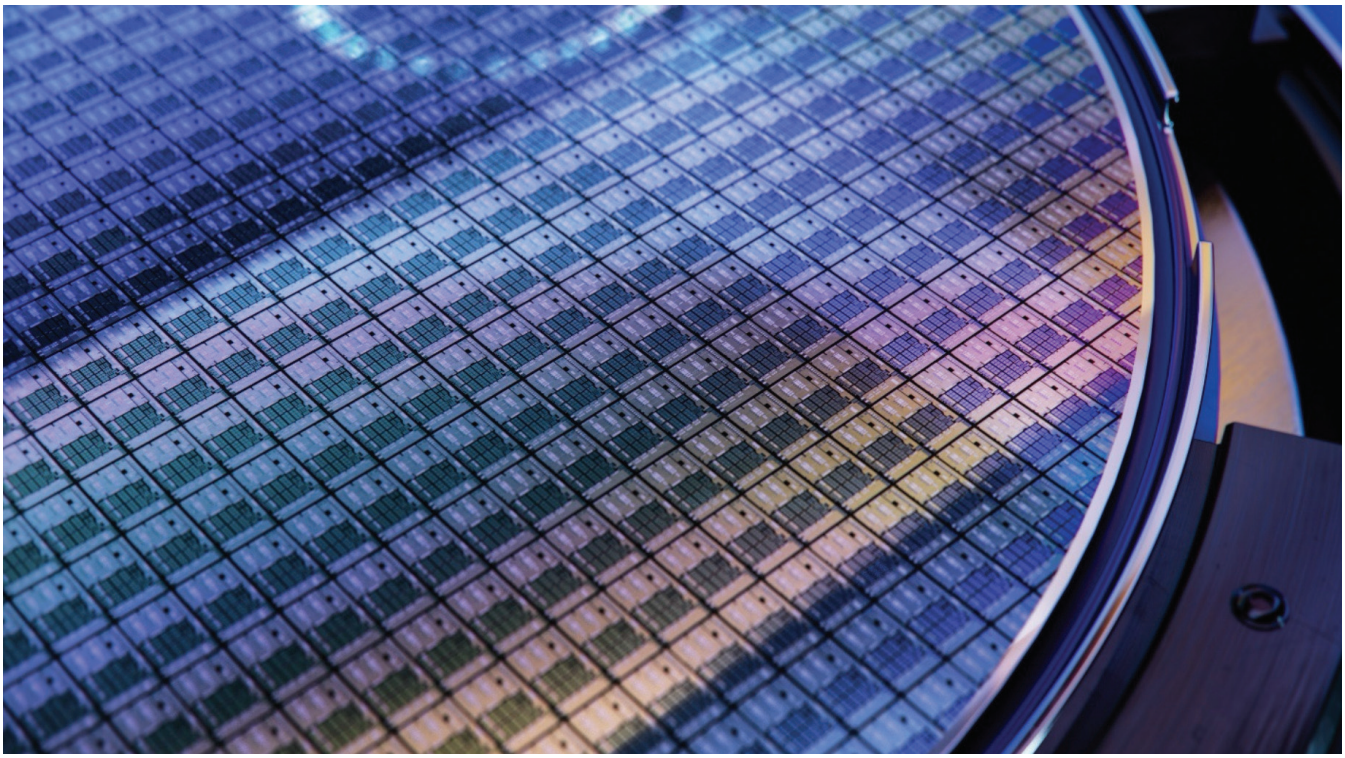


Driving functional test closer to the chip

As photonic chip designs become increasingly complex, test processes must co-evolve with the technology, helping to ensure PIC performance and reliability, reduce development costs, and drive widespread adoption of silicon photonics.

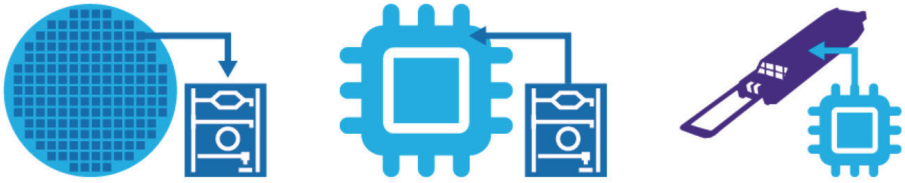
BY R. MATTHEW ADAMS, SENIOR PRODUCT MANAGER, PHOTONIC AND FIBRE OPTIC TEST SOLUTIONS, LAB & MANUFACTURING APPLICATIONS, VIAVI SOLUTIONS

SILICON PHOTONICS is a core technology enabling next-generation communication ecosystems. Recent advances in the area have been critical to delivering the 800G and 1.6T modules that underpin today's AI infrastructure, datacentres, and coherent transport. Yet as process technologies mature, expectations grow, leading to a plethora of new technical challenges.

For instance, the increasing functional integration and the hybrid integration of new materials as a path to reduced power consumption both require improvements to process and device yields, which in turn enable the number and types of devices per chip. Hurdles also remain with cost-effective "fibre-attach" processes for high-fibre-count applications, such as co-packaged optics (CPO) devices.

Meanwhile, rising baud rates and symbol rates will require tighter performance tolerances. In many cases the need to "trim" or calibrate chip-level characteristics will become increasingly important to improve yield and performance. Additionally, data management processes for integrating values into the digital signal processors (DSPs) controlling the target modules will need to become more and more efficient.

In the face of this dynamic ecosystem with its various obstacles, optical testing will also need to change and evolve, capitalising on the opportunity to bring application-level testing or functional test closer to the chip as functional integration increases and fabrication processes mature. To understand



	WAFER LEVEL TEST	PACKED DEVICE	MODULE
Test Target	Pre-singulated chip	Singulated chip-on-carrier	DSP integrated module/system
Optical Process	Fabrication, Test fiber alignment	Fiber attach, Hybrid material integration, Wire bonding	External connectors, splicing, power test, signal continuity
Parametric Test	Waveguide response, E/O response, Spectrum	Fiber attach IL/RL	
Functional Test		TX Power & Spectrum, RX loss, Signal continuity	BER, OSNR, TDECQ, Telemetry cal. TX Power & Spectrum

➤ Table 1. Optical tests occur at different stages along the transformation chain, traditionally grouped into three key phases: wafer level, packaged device level, and integrated modules like the OSFP or QSFP. Each phase has unique requirements for both optical test function and test system architecture.

how the industry can achieve this, we first need to look at the different kinds of tests routinely performed throughout product development, and what their purposes are.

Test engineers often divide test types into two categories: parametric and functional. For silicon photonics, a parametric test refers to a set of measurements taken on a photonic device to characterise its key optical properties. These include insertion loss, polarisation-dependent loss, bandwidth, and responsivity, with tests typically performed at the wafer level during the manufacturing process to identify potential issues early on.

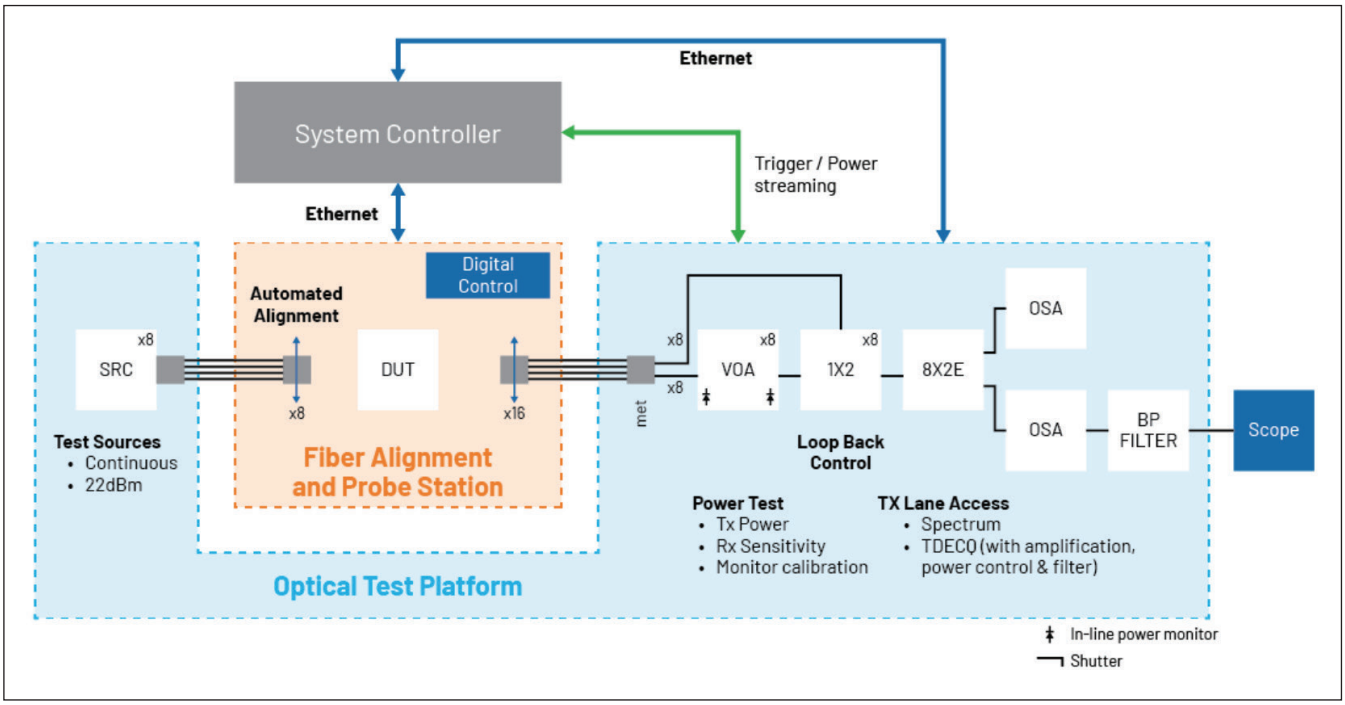
A functional test, on the other hand, refers to a set of measurements conducted on a fabricated PIC to verify that it operates as intended, assessing its overall performance by evaluating parameters driven by the final application. This kind of evaluation determines whether the device meets its design specifications and will function properly within a system.

These tests can also be distinguished by purpose; parametric tests focus on the physical properties of a device, and are predominantly indicative of device geometry and material quality. They can be important in the early stages of a chip's development and for tracking processing variation and, in many cases, they help take the chip from the lab to early manufacturing. However, as designs and processes mature, engineers may consider removing or reducing test coverage in these areas.

By comparison, device-level functional tests treat the chip as a system, measuring higher-level values. Testing here is much more focused and tends to occur at the intended operational wavelength and at a specified data rate, with tests such as bit error rate (BER) and transmitter dispersion eye closure quaternary (TDECQ) being used.

These tests are closely connected to final user specifications and include a range of transmitter powers (overload test). Results may look at the combined data from multiple structures and can be

➤ Figure 1. Modular platforms can be flexibly configured to deliver test coverage tailored to the needs of different optical functionality.



➤ Figure 2. Enabling triggering and real-time data streaming from the power meters in the VOA can dramatically simplify the provision of alignment feedback. When this action is complete, the VOA can be deployed for receiver sensitivity testing.

used to calibrate chip performance characteristics, such as optical losses impacting photodiode quantum efficiency, or the performance of polarisation beam splitting functions in coherent receivers.

Testing along the integration path

Optical tests occur at all phases of the transformation chain. A traditional segmentation would be to group them in the following three phases: wafer, package, and module, as summarised in Table 1. Each phase has unique requirements for both optical test function and test system architecture.

Traditionally, lower-level tests of basic optical performance have had to be undertaken at the chip level, with higher-level tests deployed as technologies are integrated.

As chip complexity grows and processes mature, moving these functional tests closer to the silicon offers significant advantages, including a reduction in the number of test steps from the wafer through to the module. It also allows the yielding of chips before costly integration steps, and the simplification of final module tests through the reduction of testing overlap.

Migrating tests to earlier manufacturing phases or closer to the chip presents several challenges, including differences in the requirements for test equipment format, measurement speed, and automation control interfaces. It also shifts test equipment packaging from standalone “rack & stack” solutions to designs that can be integrated with probe or fibre-attach stations. This demands fast, low-latency APIs, as well as simple, fast, and secure remote access, remote triggering and buffer capture operations, plus parallel multi-user support for multi-threaded automation.

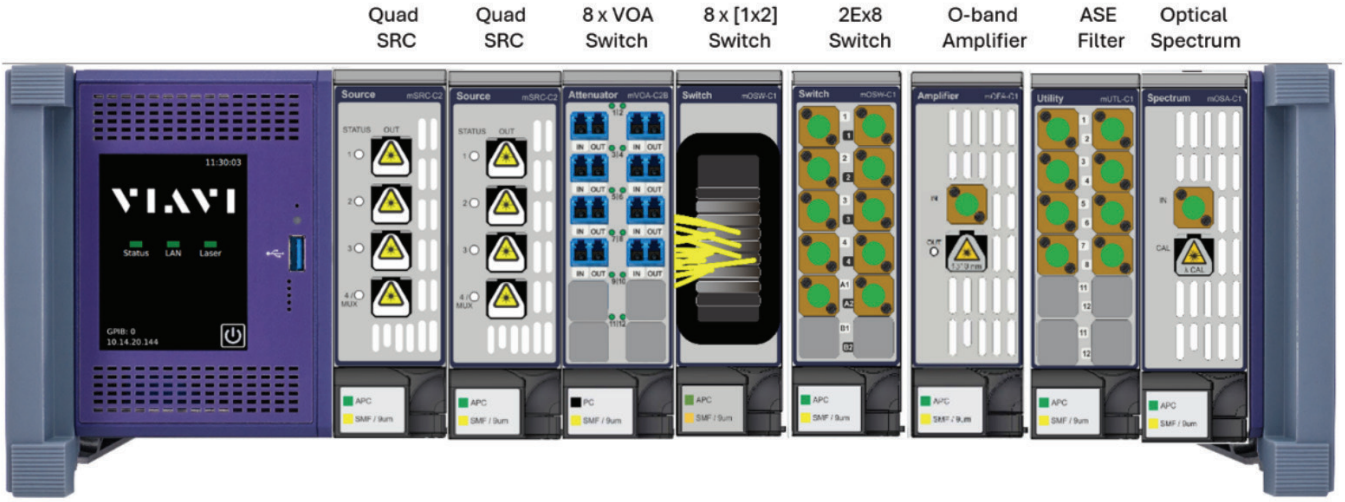
Optical requirements can also change. Working at the chip level often necessitates different test interfaces and the creation of test devices that can be used for both process and metrology steps.

Getting closer to the chip will require the use of polarisation-maintaining fibre switching, high-power sources for alignment processes, and the design of test devices that are both fast and accurate. In this evolution, it will be critical to move beyond designs that give simple pass/fail results to more sophisticated test processes that capture and deliver data to upstream operations.

A further complexity is the use of test equipment for both fibre alignment operations and for precision metrology, with particular focus on optical power meters. In these contexts, it is essential to use hybrid designs, which enable the measurement precision required, but which also have the bandwidth and interfaces required for alignment feedback. And as multifibre designs become more popular, these solutions need to be scalable.

While these challenges are far from trivial, overcoming them will be well worth the effort, paving the way for a valuable reduction in test equipment capital and operation expenses. However, not all tests can be migrated, and not all overlap optimised.

The handling and integration process will always require final performance tests at the module level, with tasks at this stage including DSP integration, validating fibre handling impact, and ensuring customer test reporting requirements are met.



➤ Figure 3. A single 3U solution that can accommodate an eight-lane functional test with the bandwidth required to accommodate fibre alignment and attach operation.

A consequence of bringing functional test close to the chip is that test systems need to be aligned with the specific requirements of the design. By their nature, parametric tests are generally standardised, whereas a functional test must be narrowly tailored to the architecture of the chip in question.

The availability of easily adjustable, rapidly adaptable modular test platforms, such as the VIAVI solution shown in Figure 1, will thus become increasingly vital to support PIC development.

Example functional test system

The schematic in Figure 2 outlines an example functional test solution for an eight-lane chip with integrated transmit and receive function. This solution integrates the required optical test modules for both alignment and functional test in a single system. The reference continuous-wave (CW) light sources enable output alignment and also have the optical properties (linewidth and power) required for the system-level test.

For CPO architectures, the external sources are critical as no source is integrated directly with the chip. In the case of an IEEE DR8-type device, these external sources may be temporary until the module source lasers can be integrated.

Enabling triggering and real-time data streaming from the power meters in the variable optical attenuator (VOA) can dramatically simplify the provision of alignment feedback. When this action is complete, the VOA can be deployed for receiver sensitivity testing. Options to add amplification in the test signal path offer flexibility to perform TDECQ measurements at relatively low powers. This facilitates early screening of the parameter prior to completing the full fibre alignment.

However, even in this relatively simple case of an eight-lane device, it is critical to use a compact, flexible modular platform, to ensure the manufacturing station size is compact and can be easily integrated into a standard probe or alignment station.

This single mainframe solution approach also significantly simplifies the number of IP addresses to be managed, while multi-threaded automation architectures allow all modules to be controlled in parallel. Additionally, the solution features duplex optical switching, which is a cost-effective tool to enable both optical spectrum and TDECQ measurements to happen in parallel.

This test could be flexibly deployed at the wafer level but is more likely to be integrated at the packaging phase. At the module level, most of these tests could be dramatically scaled back. Figure 3 shows a VIAVI solution capable of conducting the test depicted in Figure 2.

This setup is just one example of how VIAVI is innovating to ensure its test and measurement solutions co-evolve with silicon photonics technologies. The integration of the latter with existing semiconductor fabrication techniques allows for the cost-effective mass production of photonic devices, making the technology more accessible and scalable.

This is a vital step to meet the soaring demand for high-speed, energy-efficient data transfer, and is helping to advance datacentre interconnects, AI, long-haul telecommunications, and high-performance computing.

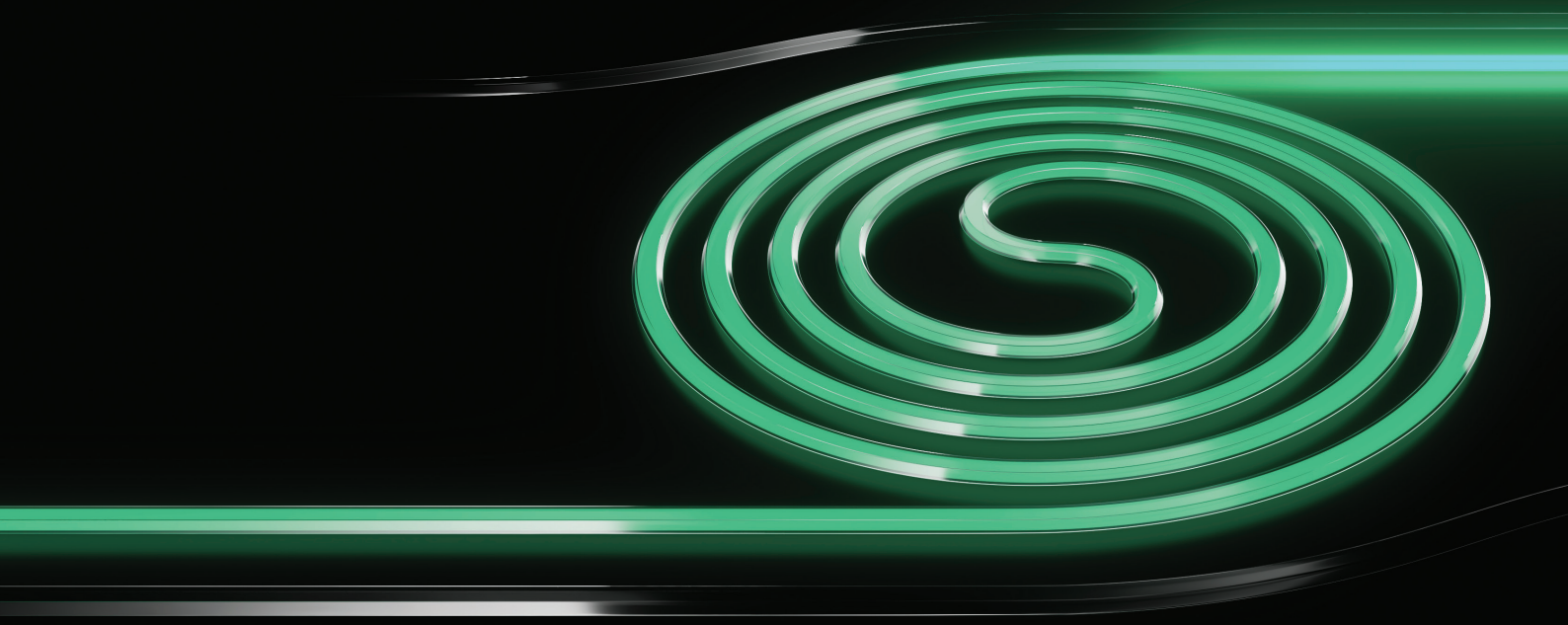
The ability to perform functional tests closer to the silicon will be critical in ensuring the reliability and performance of these advanced PICs, ultimately driving the adoption of silicon photonics across a wide range of applications.

Moving functional tests closer to the silicon also streamlines the testing process, reduces costs, and improves efficiency, thus supporting the PIC industry in tackling key challenges as it continues to grow.

Revolutionising telecoms with the world's smallest fully optical amplifier

A compact erbium-doped waveguide amplifier achieves record-breaking performance, heralding a new era for integrated photonics in data communication, sensing, and beyond.

BY PARSA KHORASANI, PHOTONICS ENGINEER, EDWATEC



IN TODAY'S digital age, where information flows faster and in higher volumes than ever before, optical amplification has become essential to global communication infrastructure. Whether streaming high-definition content or transferring terabytes of data within or between datacentres or across continents, activities of modern telecommunication networks would not be possible without the ability to amplify light signals with minimal noise.

Central to this capability are erbium-doped fibre amplifiers (EDFAs). Since their invention in the 1980s, EDFAs have revolutionised the telecoms industry by effectively boosting signals travelling through optical fibres, enabling seamless, long-distance data transmission across vast networks, including across the Atlantic Ocean.

Erbium's remarkable success lies in its unique ability to amplify light in the 1.55 µm wavelength range, which coincides with the region of lowest transmission loss in silica fibres, making it the ideal choice for optical communications.

Erbium ions have a distinctive electron configuration and exhibit long-lived excited states when embedded in host materials such as glass or silica.

This property allows them to act as highly efficient gain media, simultaneously amplifying multiple optical channels with exceptional stability, low noise figure, and without crosstalk. Over the decades, EDFAs have expanded their reach far beyond telecoms, finding critical applications in lasers, precision sensing, and even atomic clocks.

However, as the demand for data grows exponentially, driven by AI, cloud computing, video streaming, and the proliferation of IoT devices, traditional EDFAs are reaching their limits. This is particularly evident in datacentre interconnects, where data rates have surged beyond 400G, necessitating new solutions that align with the miniaturisation and integration requirements of modern photonic systems. While EDFAs continue to be reliable workhorses, their high cost, bulky fibre-based architecture, and large form factor are increasingly at odds with the demands for compactness and integration into next-generation photonic technologies. The need for efficient, scalable, small-form-factor amplification solutions has never been more urgent.

But replicating the success of EDFAs in a compact, chip-scale format has been a longstanding challenge. As early as the 1990s, institutions like Bell Labs embarked on efforts to develop erbium-doped waveguide amplifiers (EDWAs), aiming to capture the same amplification properties of erbium within a scalable, integrated waveguide structure that could be incorporated into photonic chips.

However, these and other early attempts were met with significant obstacles such as high waveguide losses, stemming from imperfections in the fabrication processes. These losses severely limited the length of useable waveguides, thereby restricting the amplification potential and significantly reducing the achievable gain. Additionally, the phenomenon of cooperative upconversion or pair-induced quenching—where energy is lost due to interactions between densely packed erbium ions—further reduced efficiency and limited the achievable gain.

Despite significant advancements in photonic integration technologies, all attempts to create integrated erbium-doped amplifiers had, until recently, struggled to exceed output power levels beyond a milliwatt, falling well short of the performance achieved by their fibre-based counterparts.

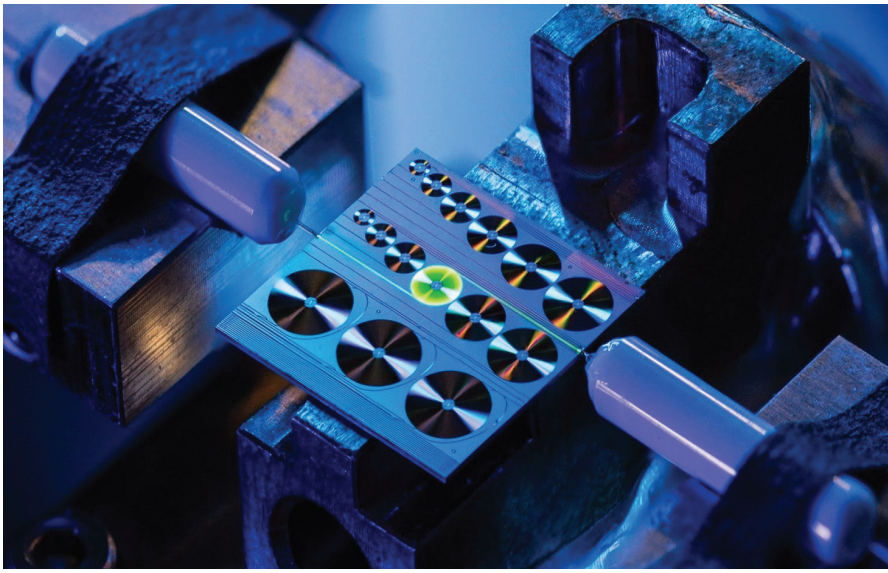
Founding EDWATEC on a technological breakthrough

Decades after the first attempts to develop EDWAs, a groundbreaking advancement at the Laboratory of Photonics and Quantum Measurements (LPQM), led by Tobias Kippenberg, a professor at EPFL, has led to a dramatic shift in the field. By integrating ultra-low-loss silicon nitride waveguides with precise ion implantation techniques, the LPQM team achieved an erbium-doped waveguide amplifier with an extraordinary output power of 200 mW.

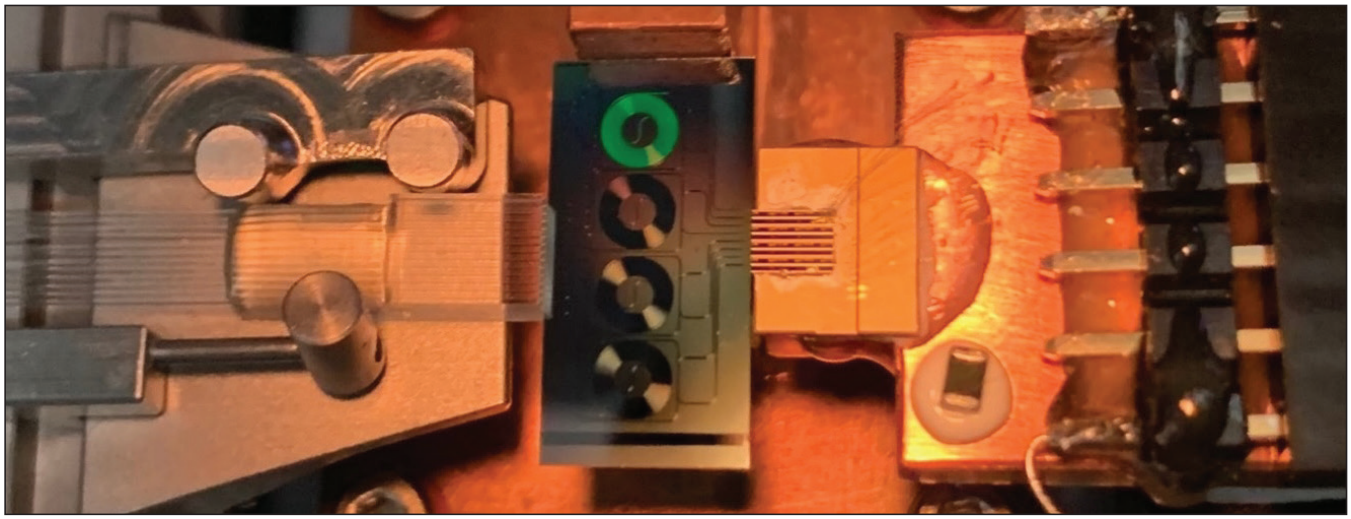
With a small-signal gain exceeding 30 dB, this results in more than 1000-fold signal amplification—all on a chip measuring below 5 mm^2 in footprint, making it the world's smallest fully optical amplifier. This EDWA provides stable gain with a low noise figure, while remaining resilient to crosstalk, non-linearities, and temperature fluctuations.
The innovation lies in the meticulous engineering of the silicon nitride waveguides and the ion implantation. By reducing background losses, the researchers have demonstrated designs featuring up to 50 cm of waveguide length in a compact spiral configuration, maximising the interaction length between light and the erbium-doped material.
This novel integration strategy allowed the team to overcome decades-old barriers, setting a new benchmark for chip-scale optical amplifiers, and paving the way for the founding of EDWATEC, a company that is now commercialising this cutting-edge technology.

One of the primary industries set to benefit from EDWAs' versatility is the growing market for coherent transceivers, especially for datacentre interconnects (DCIs). As data traffic between hyperscale datacentres surges, driven by AI workloads and massive data analytics, the demand for high-capacity, low-latency optical links has intensified. DCIs, typically spanning distances of 10-120 km, now require transmission rates that have skyrocketed from tens to hundreds of gigabytes and beyond in the span of just a few years. With the emergence of new terabyte communication systems, the critical role of advanced optical amplifiers becomes even more pronounced.

Traditional amplification technologies, such as EDFAs, face considerable challenges in this evolving landscape. Their fibre-based design limits scalability and integration within modern photonic platforms, while their high production costs present significant barriers to widespread adoption. EDWAs offer a transformative alternative; their compact form



➤ Figure 1. A 1 cm × 1 cm chip hosts multiple erbium-doped waveguide amplifiers (EDWAs), each featuring a spiral waveguide design tailored to specific performance characteristics. The visible green emission highlights the optically excited erbium ions, showcasing the active amplifier within the chip.



➤ Figure 2. Experimental setup of a multi-lane erbium-doped waveguide amplifier (EDWA) featuring an on-chip signal and pump mixing unit (WDM) and an edge-coupled pump laser. This design enables massive parallelisation of data transmission, a feat unattainable with traditional EDFAs due to their large footprint or conventional OSAs due to high channel crosstalk.

factor, compatibility with silicon photonics, and wafer-scale manufacturability enable the integration of multi-lane amplification on a single die. This breakthrough addresses a critical bottleneck in high-bandwidth, dense network environments, offering unprecedented scalability and efficiency for coherent transceivers and unlocking new capabilities for DCIs.

Deep-sea cables to satellite networks

DCIs are not the only application that EDWAs have the potential to transform in the coming years. Their compact size, high power output, and ability to operate efficiently in extreme environments position them as a key enabler of next-generation technologies across several critical domains, including communication, sensing, and mapping.

From deep-sea fibre optic networks to satellites orbiting Earth, EDWAs represent a versatile and scalable solution to the diverse amplification challenges faced in modern photonics.

In undersea optical communication networks, where amplification units are typically spaced every 80 km within tightly constrained repeater stations, EDWAs' minimal footprint provides a significant advantage. Traditional EDFAs face physical scaling limitations as the number of fibres in a single cable increases.

In contrast, EDWAs offer high-power amplification in a fraction of the space, enabling the integration of multi-channel amplification within a single module. EDWAs are also well suited for optical links in free-space satellite communications; their compact size and lightweight design make them ideal for systems where minimising payload weight and maximising available space are essential to reduce launch costs and optimise functionality. EDWAs' small footprint enables higher integration densities, allowing multiple amplifiers to be incorporated into limited satellite space. Additionally, silicon nitride-based EDWAs demonstrate exceptional resistance to radiation and environmental stresses, ensuring reliable operation in the harsh conditions of outer space.

LiDAR (light detection and ranging) systems are yet another area that stand to benefit from EDWAs. These systems are critical for applications ranging from autonomous vehicles and precision mapping to meteorological surveillance and forecasting. Once more, the high gain and compact design of EDWAs enable them to amplify low-power laser signals to the required levels for long-range sensing. Besides the direct advantages of EDWAs, their development has also driven more general advancements in erbium-doped PICs. An exciting by-product of this research is the invention of a

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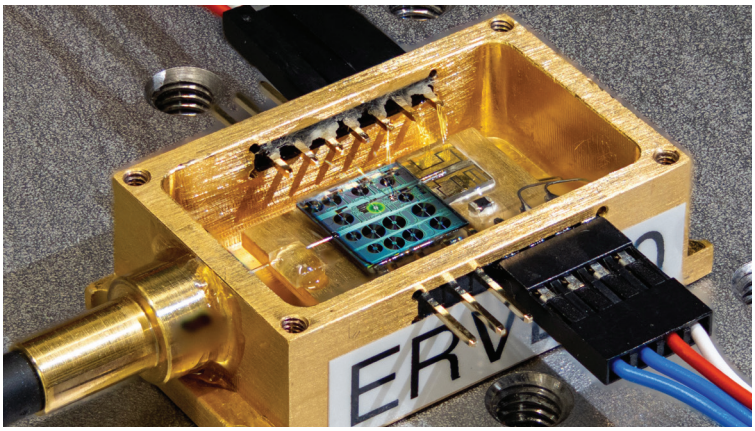

➤ Figure 3. Fully hybrid in-house packaged integrated external cavity erbium laser, featuring an edge-coupled pump diode and broad wavelength tuneability.

new type of laser: integrated external cavity erbium lasers. These devices are distinguished by their ultra-narrow linewidth, which reaches as low as 50 Hz, ensuring the high spectral purity that is critical for precision applications in optical communication, sensing, and beyond. Additionally, they demonstrate remarkable stability, with temperature insensitivity enabling consistent performance across a wide range of environmental conditions.

Another standout feature of these lasers is their ability to lase across the C-band and L-band – spectral regions that are vital for modern optical networks. EDWATEC achieves this broad tuneability using thermo-optic effects, enabling precise wavelength selection and allowing these devices to support a diverse array of applications.

With their compact form factor and ability to achieve low noise, high output power, and wide wavelength tuneability, integrated external cavity erbium lasers bridge the gap between traditional fibre-based systems and state-of-the-art semiconductor lasers. Their reliability and exceptional performance characteristics make them an indispensable tool for applications, notably in fibre sensing, spectroscopy, LiDAR, and communications.

Silicon photonics integration and scaling EDWAs

The next phase in EDWA development focuses on seamlessly integrating them into silicon photonics platforms to meet the demands of diverse communication systems. EDWATEC is exploring two primary approaches: heterogeneous integration, which incorporates EDWAs into existing platforms via hybrid techniques, and monolithic integration, which takes advantage of the amplifiers' compatibility with silicon photonics to embed them directly onto the photonic chip, ensuring a streamlined and homogeneous process flow. Successful integration requires precise alignment with the specific fabrication workflows and application requirements of each customer.

EDWATEC therefore tailors its integration strategies to ensure optimal performance in diverse real-world scenarios, including high-speed datacentres, telecommunication networks, and undersea communication systems.

The company also provides custom-designed EDWAs, meticulously optimised to meet the unique specifications of each application. This involves addressing the nuanced challenges posed by various deployment environments, ensuring that each solution delivers reliable and high-performance amplification. Looking ahead, EDWATEC aims to accelerate the commercialisation of EDWA technology through collaboration and supply agreements. This will enable clients to fabricate and integrate amplifiers within their own facilities, reducing production costs and lead times while granting full control over the integration process. This strategy marks a significant milestone in establishing EDWAs as a scalable, industry-standard solution for next-generation photonics. To enable large-scale production of EDWAs, the fabrication process is transferred to silicon photonics foundries, ensuring consistent quality and uniformity across high-volume manufacturing. EDWATEC collaborates closely with foundries to refine and optimise processes, adhering to stringent quality standards.

Additionally, applications such as deep-sea fibre optic links present unique challenges, requiring robust packaging solutions to withstand extreme conditions like high pressure, moisture, and mechanical stress. Scaling these packaging solutions for mass production is vital for deploying EDWAs in critical global infrastructure projects. EDWATEC is addressing these technical and logistical challenges, with the aim of establishing EDWAs as a scalable and reliable solution for demanding applications worldwide.

By enabling seamless integration within silicon photonics platforms where other functional components are already on-chip, EDWAs eliminate the need for bulky and costly fibre-based amplification, unlocking new possibilities for compact, high-performance transceivers that are not only more cost-effective, but also better suited for next-generation integrated solutions. From high-bandwidth datacentres to undersea communication cables and satellite communication systems, EDWATEC is dedicated to advancing the production, integration, and deployment of EDWAs to meet the ever-growing demand for faster, more energy-efficient, and reliable optical networks.

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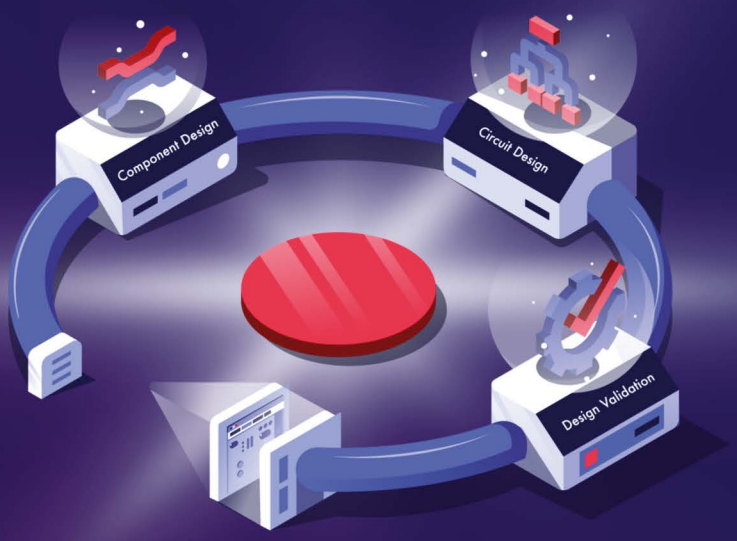

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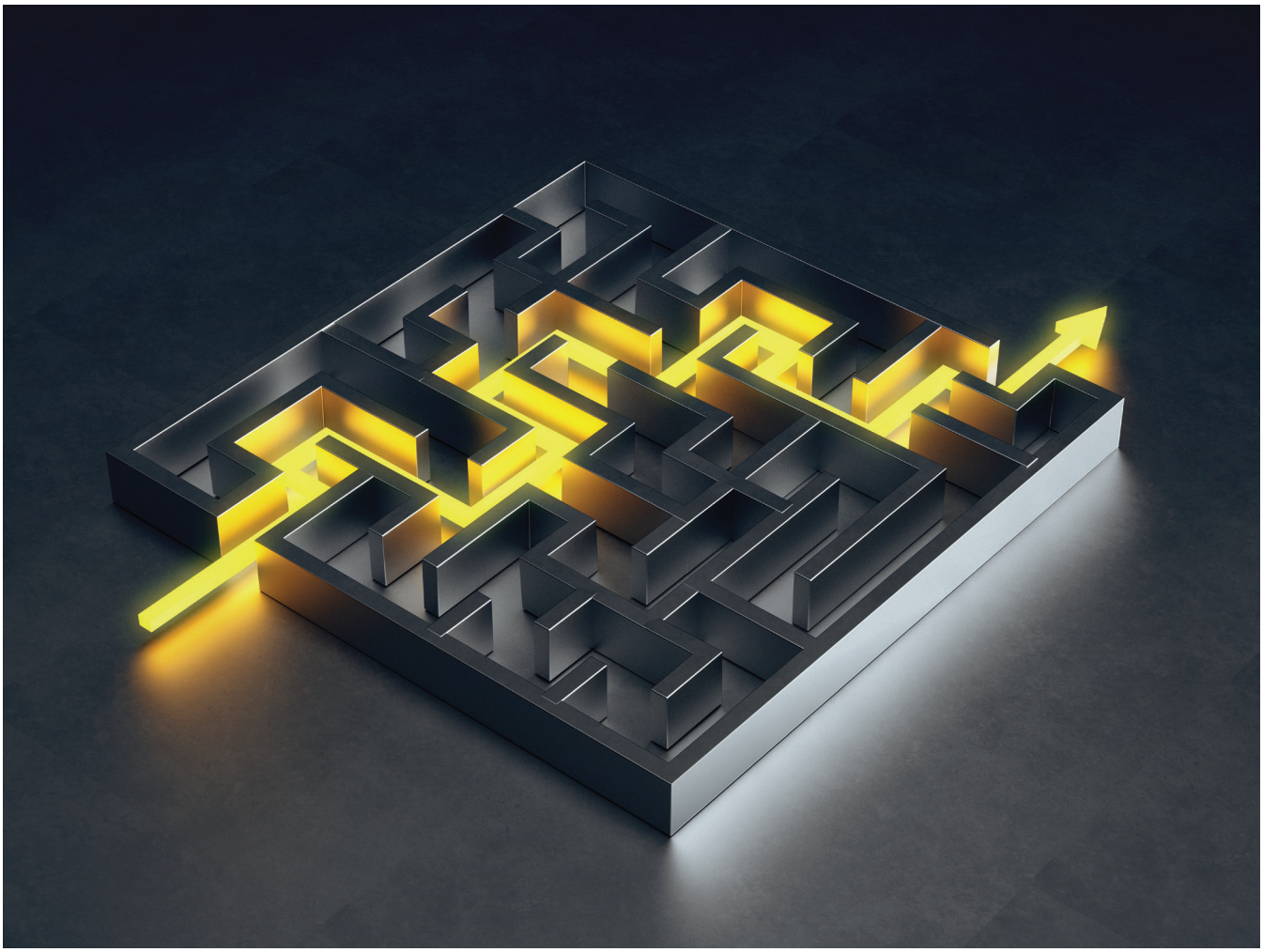


Propelling PICs from idea to MVP in under 12 months

Light Trace Photonics has developed a cutting-edge pipeline for developing new integrated photonic products quickly and effectively, supporting companies with technical feasibility studies, proven component IP, and circuit-on-a-chip evaluation modules.

BY JAKE BIELE, CEO, AND DOMINIC A. SULWAY, CTO, LIGHT TRACE PHOTONICS

THE WORLD is entering a new era of technological innovation, where light is poised to revolutionise the way we compute, communicate, and sense our environment. PICs are at the forefront of this transformation, offering unparalleled speed, efficiency, and scalability compared to traditional electronic chips. Yet, despite their immense potential, bringing a photonic chip from concept to reality remains a complex, high-risk endeavour.

For start-ups and established companies alike, the road to a successful PIC product is fraught with challenges – lengthy design cycles, costly fabrication runs, and the need for deep interdisciplinary expertise. With a rapidly evolving ecosystem and a lack of standardised components and skilled engineers, even the most promising ideas can stall before reaching a functional prototype, let alone a fully-fledged product. The question remains: how can companies navigate these challenges and accelerate their time to market?

At Light Trace Photonics, we provide a solution. Our cutting-edge development pipeline is designed to take companies from initial concept to a minimum viable product (MVP) in under 12 months. Our approach is simple: minimise risk and

maximise results during this early stage of product development.

By leveraging advanced proven photonic chip component IP, state-of-the-art design methodologies, and zero-barrier circuit-on-a-chip evaluation, we help our customers reduce risk, maximise results, and ultimately bring photonic innovations to life faster than ever before.

Our pipeline supports companies through four key stages to MVP. First, we help customers establish a strong foundation through expert-led training and technical feasibility studies. Next, using proven component IP and expert guidance, we maximise the probability of achieving first-time-right circuit design. Then, we support clients to make confident decisions with rigorous post-fabrication in-house test and measurement. And finally, we accelerate early commercial success with a seamless, zero-barrier circuit-on-a-chip evaluation module, the LightPort:Pro.

We understand the challenges involved in this journey because we've faced and overcome them firsthand, during the development and launch of the LightPort – a cutting-edge module that enables engineers to get hands-on experience using and programming a PIC outside the lab (see Figure 2).

The challenges: Why getting to MVP is so difficult

The world of integrated photonics is defined by extraordinary diversity – spanning multiple material platforms, wavelengths, and packaging options – standing in stark contrast to the more uniform landscape of microelectronics. This diversity is a testament to photonics' vast potential and a formidable challenge. Unlike microelectronics, where established development pipelines provide a degree of standardisation, the rapid evolution of photonic technologies means that staying up to date with this evolving ecosystem is no small feat.

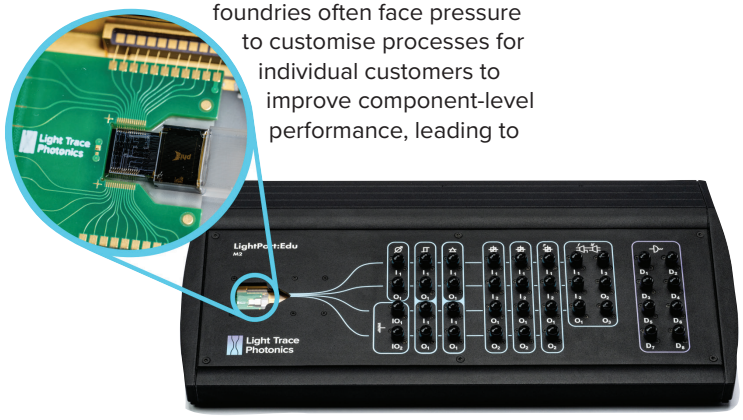
For companies developing PIC-based products, the challenge isn't just understanding today's capabilities – it's anticipating what will become viable in the next two to five years. Choosing the right technology now requires foresight, as the wrong decision could leave a development eclipsed by emerging innovations before it even reaches the market. Navigating this dynamic ecosystem demands a strategic approach, one that balances near-term feasibility with long-term competitiveness, ensuring that today's choices remain relevant among tomorrow's advancements.

One area of particular interest is thin-film lithium niobate (TFLN), which has rapidly emerged as a potential frontrunner in next-generation photonics [1]. Long valued in bulk crystals for its exceptional electro-optic properties, lithium niobate waveguides have historically been constrained by fabrication challenges and limited integration with other platforms. However, the advent of thin-film processing is beginning to unlock its full potential, enabling ultra-high-speed modulators, low-loss waveguides, and compact, power-efficient photonic circuits.

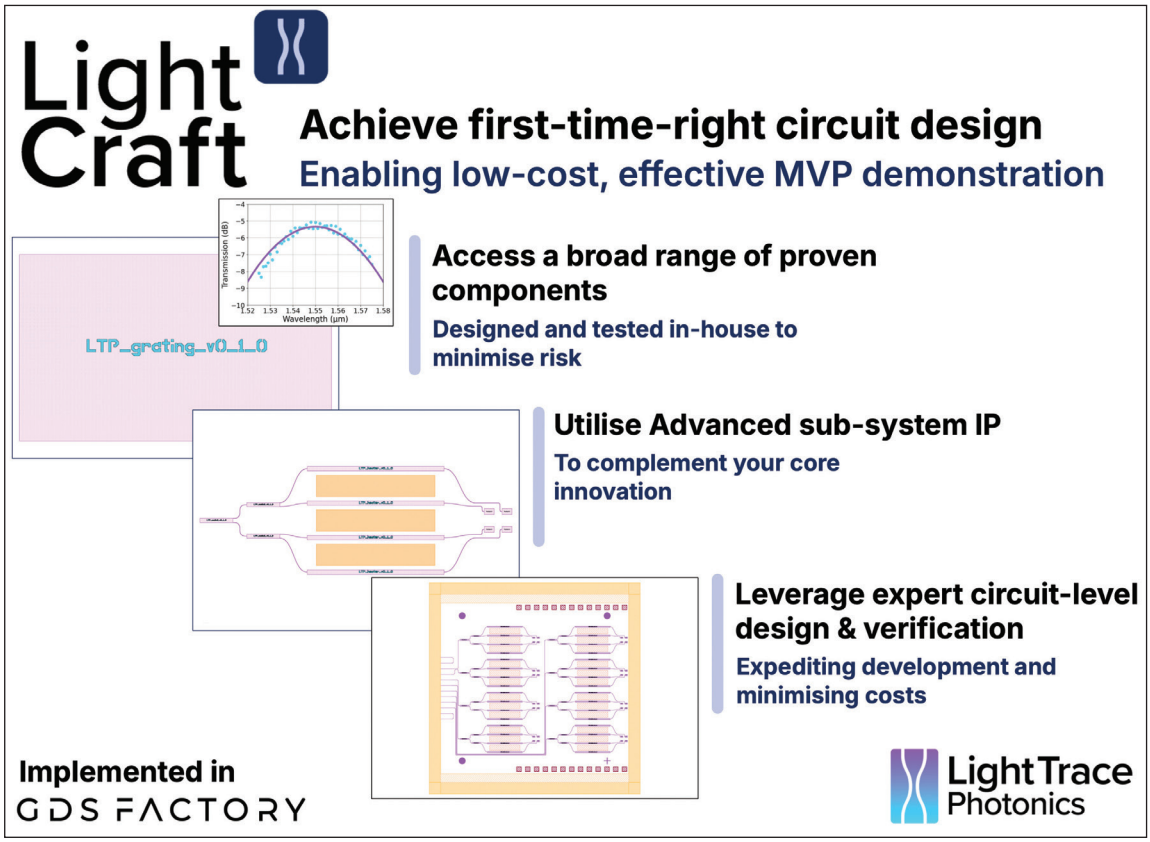
➤ Figure 1. The Light Trace team: (l-r) Harry Alexander, James Blatcher, Dominic Sulway, Quinn Palmer, Jake Biele, Steve Kitson, and Mike Ward.

With its combination of high bandwidth, low power consumption, and the establishment of commercial foundry offerings, TFLN is poised to play a transformative role in optical communications, quantum technologies, and microwave photonics. As fabrication techniques mature, and as these commercial foundries expand access, we see TFLN as a technology to watch – one that could redefine the landscape of integrated photonics in the coming years.

Besides this rapidly evolving and diverse ecosystem, another challenge that PIC entrepreneurs must navigate is a lack of access to proven IP. On this front, the PIC industry operates in a far less standardised environment than microelectronics. While increasing component density in photonics can enhance functionality and performance, it does not necessarily drive costs down in the same way as CMOS scaling. The analogue nature of many photonics circuits naturally results in a broader range of component types and designs to select from. In addition, photonic foundries often face pressure to customise processes for individual customers to improve component-level performance, leading to



➤ Figure 2. The LightPort training module helps upskill engineering teams.



➤ Figure 3. LightCraft's proven component IP, made available via PDKs, will help you accelerate your product development.

high R&D costs, lower yields, and manufacturing challenges.

This has resulted in an IP landscape that remains highly fragmented, with multiple companies reinventing fundamental components rather than leveraging standardised, proven building blocks. This limited standardisation makes component design selection a critical yet risky decision, as choices made early in development can have lasting consequences for manufacturability, scalability, and long-term competitiveness.

A third obstacle to overcome on the way to a successful integrated photonics product is the lengthy, costly fabrication processes involved. Bringing a PIC product to market typically requires multiple fabrication cycles, progressing from component-level validation to circuit integration and, ultimately, full system development. While early-stage development can leverage MPW (multi-project wafer) runs to reduce initial R&D costs, these still require significant investment – often tens of thousands of pounds per design – while iteration cycles average 5-8 months. Without a strong grasp of design best practices, many companies face repeated failed runs before achieving a functional prototype, significantly extending timelines and costs.

A critical challenge in early-stage circuit development is identifying and mitigating technical risks. While process design kits (PDKs) offer valuable design support, their effectiveness depends on a deep understanding of the underlying fabrication processes. Without this insight, even seemingly minor design choices can lead to costly setbacks on the road to product launch. Success in PIC development can hinge not only on leveraging standardised design tools but also on mastering the nuances of manufacturing constraints to ensure first-time-right fabrication.

Our solution: A streamlined pipeline for MVP success

Successful PIC development begins with a solid, up-to-date foundation of knowledge. At Light Trace, we bridge the skills gap with cutting-edge training and technical feasibility study services, ensuring in-house engineers gain the expertise needed to navigate the complexities of photonic integration. Our LightPort module is a game-changing tool designed to upskill engineers, demystify PIC technology, and align innovation with business objectives. Featuring a silicon nitride chip with a suite of programmable components – ranging from basic thermo-optic phase shifters through to complex wavelength demultiplexion schemes – the LightPort removes traditional barriers to hands-on learning, allowing all levels of engineer to experiment with photonic chips outside the lab.

In a rapidly evolving field, staying ahead requires both technical insight and strategic foresight. Our training programmes provide practical, hands-on experience while tailoring content to industry-specific challenges and applications. By equipping engineers with up-to-date knowledge and real-world

design experience, we help de-risk development, accelerate innovation, and enable informed technology choices.

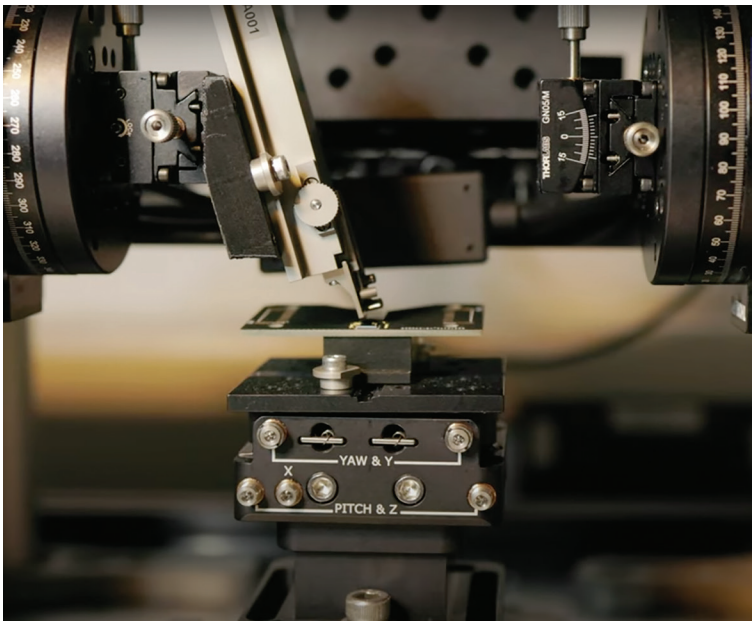
Once a team has a strong foundation in integrated photonics and a clear understanding of how it aligns with the company's technology roadmap, the next critical step is to carry out technical feasibility studies to help roadmap development. This process is essential for ensuring the MVP maximises impact while laying the groundwork for future innovation and growth. At Light Trace, we work closely with engineers to craft a detailed, actionable plan that minimises risks, avoids costly detours, and accelerates the development timeline.

Key considerations include selecting the right platform and materials to ensure technological feasibility, financial viability, and scalability. We help define critical components and their specifications to increase confidence, performance, and reliability.

Our team also focuses on optimising packaging solutions to integrate photonic chips seamlessly into the wider product, factoring in cost projections, end market requirements, and volume production challenges. Finally, we assist with budgeting and timeline planning, ensuring that both the MVP and full-scale launch are achievable within set financial and time constraints. With our roadmap, innovators have a clear path forward, reducing uncertainty and driving their product to market with confidence.

With a clear roadmap in hand, the next phase is to design and fabricate a photonic chip that brings the MVP to life, minimising the number of fabrication runs needed to reach MVP. Achieving a first-time-right design requires precision, expertise, and access to proven IP, all of which help avoid budget overruns and development delays. While no MVP is flawless, it's essential to identify the key value it must demonstrate to move to the next phase. Mapping this value to the technological risks in chip design and layout can be the crucial factor in determining success or failure at this stage.

Our LightCraft platform provides access to proven IP that has been rigorously tested in-house by the Light Trace team. This often allows our customers to bypass early design risks associated with key components and move quickly into circuit-level development. For teams without in-house chip design capabilities, LightCraft also offers expert support for system design and layout, ensuring that every aspect of the chip is optimised for success.



➤ Figure 4. Automated die-level testing of components helps ensure informed decision making.

Key challenges in this phase include design optimisation for packaging – such as fibre I/O, laser integration, and thermal/electrical management – leveraging proven designs to minimise design risks and ensuring compliance with foundry processes. Our expertise extends to navigating supply chain relations to guarantee smooth transitions from design to fabrication.

Once the photonic chip is fabricated, the third stage involves testing, packaging, and demonstration. The goal here is to quickly and reliably assess component-level performance, enable engineers to evaluate circuit-level functionality, and demonstrate the MVP outside of a controlled lab environment to showcase its capabilities in real-world settings.

Component-level testing is crucial before moving on to circuit-level characterisation. Even if individual components have been proven in other fabrication runs, validating their performance within each new chip design helps uncover any potential fabrication errors and provides a solid foundation. At Light Trace, we've developed bespoke automated testing capabilities that efficiently generate performance reports for each component in the circuit, including DC and RF characterisation data, offering reliable insights and clarity as companies move forwards with integration.

This streamlined process ensures that our customers can assess and optimise the performance of both individual components and the overall circuit

With a clear roadmap in hand, the next phase is to design and fabricate a photonic chip that brings the MVP to life, minimising the number of fabrication runs needed to reach MVP

➤ Figure 5. The LightPort: Pro packaging system makes demonstrating MVPs easier and more effective.

quickly, helping them demonstrate the MVP's value and accelerate its deployment in the field.

After component-level performance has been validated, the next step is packaging and circuit characterisation. At Light Trace, we understand that our clients' engineers, with their deep knowledge of their specific product lines, are most likely best equipped to carry out system-level characterisation. However, characterising a photonic chip at the circuit level can present new challenges related to electronic interfacing, optical interfacing, and temperature stability.

Unpackaged chips often require expensive, additional hardware for effective circuit interfacing, while custom software is often needed to programme and enable demonstrations. To simplify initial demonstration and chip interfacing, we integrate each customer's chip circuit into the LightPort:Pro, a circuit-on-a-chip evaluation module we have developed to address these key challenges.

FURTHER READING / REFERENCE

➤ https://www.ltphotonics.co.uk/news/an-intro-to-integrated-photonic-material-platforms

LightPort:Pro features up to 32 channels of optical fibre input/output to the chip, as well as up to 32 DC channels for programming it, with inbuilt 0-12 V precision voltage setting via interfacing with the Python programming language. Additionally, there are up to 8 GSG RF channels for applying/extracting signals to active components such as modulators and detectors, as well as 8 inbuilt (off-chip) photodiodes for easy debugging and live readout.

We use a Python-based scripting language for chip circuit control and programming in the LightPort:Pro, while ensuring temperature stabilisation for optimal demonstration of the chip. With this solution, engineers can focus on system characterisation and programming without the need for additional chip interfacing training or infrastructure, ensuring a smooth and efficient workflow towards MVP demonstration.

Driving the future of photonic integration

Our mission is to make photonic chips as ubiquitous as electronic ICs. With over 15 years of combined expertise in integrated quantum photonics and an extensive supply-chain and industry network, Light Trace Photonics is committed to helping companies turn ideas into market-ready solutions. The journey from concept to MVP doesn't have to be daunting. We help PIC pioneers navigate the complexities of photonic integration and bring their vision to life.

Partner with Light Trace Photonics to access a best-in-class development pipeline, expert guidance, and the tools needed for success. Together, we can drive the adoption of photonic chips and unlock new possibilities in computing, communications, and sensing. The future of technology is photonic – let's build it together.

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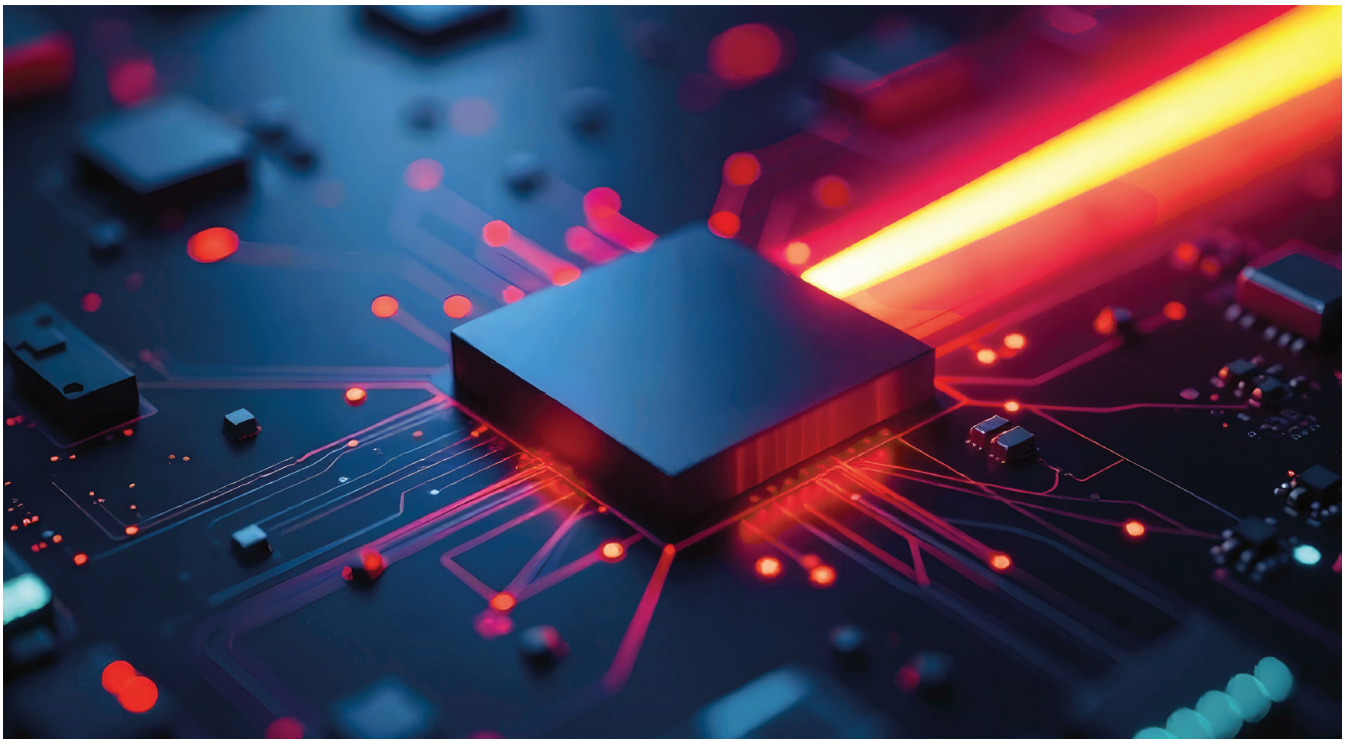


A PIC laser designed for reliability and volume production

In the era of massive AI data compute and transmission demand, optical chip innovations must look beyond basic performance metrics with designs that accelerate PIC manufacturability.

BY YOSEF BEN EZRA, CTO, NEWPHOTONICS

AS AI APPLICATIONS continue to reshape our daily lives, we are witnessing a real-time pivot by hyperscalers and datacentres to meet the technology's unique cluster compute and connectivity needs. Hyperscalers owned by giants like Google and Microsoft are building new configurations based on silicon photonics, which has been shown to improve energy efficiency and bandwidth benchmarks while reducing latency. Yet, while the technology advantages are known, these datacentres are now relying on the photonics and microelectronics ecosystem to demonstrate that silicon photonics manufacturing can be scaled to mass production.

While silicon photonics hold immense potential, one of the main challenges that remains is the integration of lasers.

There are various approaches to laser integration on silicon substrate that target improved laser coupling efficiencies, reliability, and testability. However, some techniques come at the cost of performance trade-offs, and few offer meaningful gains further along the design value chain.

In contrast to microelectronics' marriage to silicon, optical functionalities are inherently dependent on a variety of materials, and this presents a substantial scalability roadblock for PICs. Additionally, since optical interconnects are now sustaining exponential traffic growth, microelectronics and photonics technologies are tightly intertwined. Under urgent market pressures to fulfil the rapidly rising demand for energy efficiency and speed at minimal cost, photonics must quickly adopt an integration approach that meets both technical and business expectations.

This year, NewPhotonics has answered that call with its NPG102 family of on-chip silicon PIC transmitter solutions. At the core of these products is a novel approach to heterogeneously integrating lasers at the wafer level. This development fast-tracks the paradigm shift in system design to enhance module yield maturity and reliability, boosting both efficiency and efficacy. By eliminating process steps

in assembly and testing, this new technique reduces failure risks and enables output scaling, thus offering a solution to critical manufacturing and performance questions for transceiver module design.

Demonstrating greater than 90 percent efficiency (< 0.5 dB loss) in laser coupling alone, this innovation supports OEMs and system integrators to overcome current barriers and deliver what datacentres and hyperscalers are eager to implement. This article will examine the challenges associated with laser integration and packaging options, focusing on external coupling and discrete components, while also exploring how a shift towards scalable technologies can accelerate the adoption of silicon PIC solutions in datacentres. A comparison of various laser integration technologies is provided in Table 1.

Transitioning to heterogeneous integration

A growing number of methods for integrating PICs with lasers in transceiver module designs focus on gradually improving attachments to external components. However, while sourcing, aligning, testing, and managing lasers in new ways may achieve incremental gains, few options deliver significant leaps in performance and reliability, or offer greater manufacturability.

The challenge of coupling the laser energy output into a waveguide is ultimately solved by designing an optical mode-matching solution that promotes low-loss power transfer between the two elements. Precise physical alignment between the laser output and the waveguide is necessary but not sufficient; without careful three-dimensional design to accommodate the optical mode, the power transfer will not be optimised and coupling losses will increase. Attempting to couple discrete components is therefore limited by the lack of customised mode-matching design, meaning that more intimate integration between the laser and waveguide is a necessity for energy-efficient silicon PIC solutions in the datacentre and for scalable manufacturing.

Applying a more tightly aligned integration approach using wafer bonding to integrate III-V materials such as indium phosphide (InP) onto silicon substrates enables laser fabrication directly on silicon photonic platforms. This integration improves precision, density, and manufacturing efficiency. The transition between III-V laser structures and silicon waveguides is achieved through optimised bonding techniques and the design of rib or ridge waveguides to confine light effectively.

Direct wafer bonding generally involves three steps: surface treatment, room temperature bonding, and thermal treatment for bonding energy enhancement. The smooth, clean surfaces ensure efficient optical coupling and minimise losses. Some techniques involve deposition of self-assembled monolayers (SAMs) of an organic material and provide flexibility so that the surface chemistry can be adjusted to accommodate a variety of materials. Wafer bonding is crucial for creating silicon-on-insulator (SOI) substrates and enabling compact photonic devices, such as integrated waveguides and coupling mechanisms.

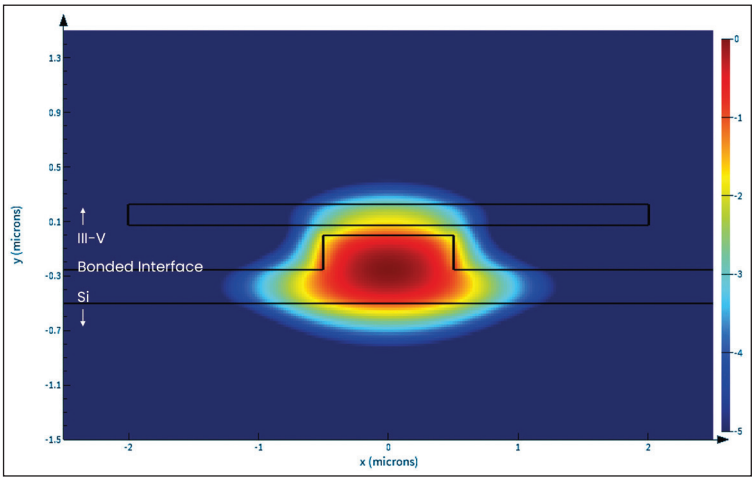
Manufacturers can create high-quality InP layers on silicon through methods like Epitaxial Lateral Overgrowth (ELOG) and Selective Area Growth (SAG). These InP layers serve as active gain mediums for the different kinds of lasers that can be formed, such as Fabry-Perot, Distributed-feedback (DFB), Distributed Bragg reflector (DBR) and ring resonator lasers. To achieve good coupling between the laser and waveguide on the chip, fabrication techniques must overcome challenges including lattice mismatch, thermal expansion differences, and defects such as stacking faults.

The silicon confinement factor – a measure of how much light remains trapped inside the silicon core of a photonic device, such as a waveguide – is an important parameter in determining coupling efficiency when a laser device is integrated with silicon passive devices. In silicon photonics, high confinement is typically desired because it allows the device to efficiently guide light within the silicon core, improving performance and minimising signal loss. The silicon confinement factor depends on the geometry of the waveguide and the refractive index contrast between silicon and the surrounding materials. Typically, the III-V mesa – a structure designed to guide the laser light – is wider than the silicon waveguide. This means that the confinement of the transverse mode is determined by the SOI waveguide and not the III-V mesa. This eliminates any issues with alignment of the III-V etch to the SOI etch. Figure 1 shows an optimised mode matching for efficient coupling between the III-V laser and silicon waveguide.

Eliminating failure points with laser on silicon

The drive to ‘illuminate silicon’ and close the gap between the photonics and microelectronics industries is no longer merely an attractive prospect—it is now an essential goal. However, to turn this vision into a commercially viable reality, the industry must overcome silicon’s inherent material limitations: its indirect bandgap and the lack of a linear electro-optic (Pockels) effect, both of which

The challenge of coupling the laser energy output into a waveguide is ultimately solved by designing an optical mode-matching solution that promotes low-loss power transfer between the two elements



➤ Figure 1. Optimised mode matching for efficient coupling between III-V laser and silicon waveguide.

make it challenging for silicon to emit or manipulate light. Leveraging mature CMOS infrastructure, the NewPhotonics design addresses this challenge by creating a 'shortcut' for photonics and eliminating the deficiency in integration technology.

Compared with the tricky alignment of a laser diode to a silicon photonic chip in the final stage of packaging, the integration of III-V on silicon represents a major technological breakthrough. Central to the NPG102 design are thin films of InP integrated through wafer bonding in a process similar to epitaxial growth of optical gain materials on large-scale silicon wafers. This platform also enables multiple technical merits favourable to laser design, operation, and integration of active and passive components.

From a fabrication perspective, this integration shifts laser functionality from being the last manual chip-level production stage to an earlier and automatic CMOS-like manufacturing stage. Since the active alignment and accuracy requirements for external lasers place a substantial burden on manufacturability and scaling, the move to integrated lasers represents a profound improvement in terms of fabrication precision, integration density, production volume, and efficiency. By reducing the need for added components, we also eliminate the points of failure caused by issues in coupling that could otherwise impact signal quality.

The financial advantages of integrating lasers are also clear. Discrete components demand added equipment and assembly steps when laser integration is external to the PIC. Eliminating engineering resources and instruments for laser-lens attachment, wire-bonding, and auto-alignment significantly reduces costs and speeds up production schedules, accelerating yield maturity rates and time to market, often by several months.

Significant logistics overhead may also be reduced without the need for separate device procurement, reliability, and vendor management. Historically the slow and labour-intensive packaging of discrete components in optical transceiver products has traditionally resulted in low-volume and expensive technology, with packaging typically contributing up to 80 percent of the total cost. Approximately half of this packaging expense is due to external laser integration, demonstrating an opportunity for considerable cost savings with integrated lasers.

On the performance side, this integrated design vitally enhances the coveted property of laser reliability to the extent that integrated lasers have become the technology of preference for leading hyperscalers. The most common fault in transceivers is laser failure, but photonic devices with integrated lasers are less susceptible to environmentally triggered failures due to the encapsulation of the silicon-based process, as well as having fewer discrete parts. There are also no etched and coated facets that risk catastrophic optical mirror damage. This means that employing CMOS-like technologies for InP laser integration is the key to advancing dependable and consistent photonic integration and performance, impacting reliability and yield at the level of both the device and transceiver module.

In the ramping stage of a new transceiver integration line, using "Known Good Die" has huge advantages in shortening the time to yield maturity. Equally advantageous is the lack of laser coupling and integration and the associated learning curve in the production line. Moreover, we have witnessed impressive zero failure rate metrics in NPG102 chips over an extended test period, accentuating the enhancements in reliability and longevity that extend both the life of the laser and the opportunity to scale.

Mode matching for integrated coupling

When external lasers are used in transceivers, the optical coupling loss reaches approximately 2.5 dB, due largely to the mismatch between the non-optimal, asymmetric mode of a DFB laser and the symmetric edge coupler input mode. Challenges with mechanical alignment require micron-level accuracy achieved through time-consuming active alignment techniques. Furthermore, reflections at the chip interfaces limit spectral flatness.

Integrated laser-to-waveguide coupling is a key element in heterogeneous photonic systems. There are several techniques for efficient coupling, including adiabatic, evanescent, and tapered coupling, among others. Table 1 summarises these methods and their advantages and disadvantages. Adiabatic coupling entails gradual transformation of the optical mode between the III-V laser and the silicon waveguide over a longer coupling region. Both materials have tapered waveguides that gradually merge, allowing efficient energy transfer. This offers low insertion loss due to the adiabatic nature of the transition, as well as better mode matching and higher bandwidth compared to abrupt coupling schemes.

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In evanescent coupling systems, the laser output couples to the silicon waveguide through an overlapping evanescent field. The III-V gain region is bonded onto a silicon photonics platform, and a shared evanescent field region enables gradual energy transfer between the laser and the waveguide. This technique has higher fabrication tolerance, and better integration density and scalability, but it requires highly precise engineering of the bonding interface for refractive index matching. A silicon-on-insulator (SOI) platform is often used to enhance the optical confinement.

Tapered coupling, meanwhile, allows the gradual transfer of the optical mode from a III-V laser into a silicon waveguide. The III-V laser facet is tapered down, matching the size of the silicon waveguide mode, and mode size transformation minimises coupling losses. This approach is widely used in high-speed optical transceivers to ensure efficient coupling. However, precise, high-quality tapering requires advanced lithography and etching processes, increasing fabrication complexity.

The NewPhotonics approach overcomes the limitations and compromises of external coupling and instead establishes an environment where internal coupling options may be optimised or customised for better overall chip performance. By adopting advanced wafer-bonding techniques with a laser-integrated design, we diminish the complexities that negatively impact efficiency, reliability, and density, reducing both time and cost to transceiver delivery.

This novel approach to wafer-level heterogenous integrated lasers for silicon PIC-based interconnect modules represents a transformative shift in optical transceiver technology. The heterogenous laser integration achieves outstanding coupling efficiency that optimises laser efficacy with higher reliability in terms of both performance and manufacturability.

With the NPG102 we have jumped beyond the incremental attempts to integrate lasers with discrete component designs to address critical market and sustainability concerns. This process leapfrogs traditional external laser coupling methods, reducing optical losses, and improving overall reliability. Furthermore, this advancement simplifies datacentre infrastructure — accelerating the pivot to rack designs that use optics-driven interconnects with optimised power efficiency and signal quality.

This novel strategy for integrated lasers offers increased production yield metrics, improved reliability, and shortened time to market. In the highly competitive datacom transceiver market these differentiators combine for clear cost and efficiency advantages. The shift to heterogenous laser integration in silicon will bridge the module supply gap for high-capacity, low-latency, and power-efficient data networks, helping datacentres to meet the growing demands placed on network and compute volume by AI. This evolution is set to redefine datacentre performance and efficiency, making it an indispensable technology for the future of digital communications.

➤ Table 1. A comparison of various laser integration techniques, their advantages, challenges, and coupling efficiencies.

Coupling Method	Advantages	Challenges	Efficiency
External Laser Coupling	• Simpler initial implementation	• High optical coupling loss (~2.5 dB) • Requires time-consuming alignment • Expensive due to added assembly steps • Contributes significantly to packaging cost	**Baseline**
Evanescent Coupling	• High fabrication tolerance • Better integration density • Scalability	• Requires precise bonding interface • Refractive index matching is critical	**Good**
Adiabatic Coupling	• Low insertion loss • Better mode matching • Higher bandwidth	• Requires precise design • Increased length adds to device footprint	**Better**
Tapered Coupling	• Efficient mode transformation • Common in high-speed optical transceivers	• Increased fabrication complexity • Advanced lithography and etching processes needed	**Better**

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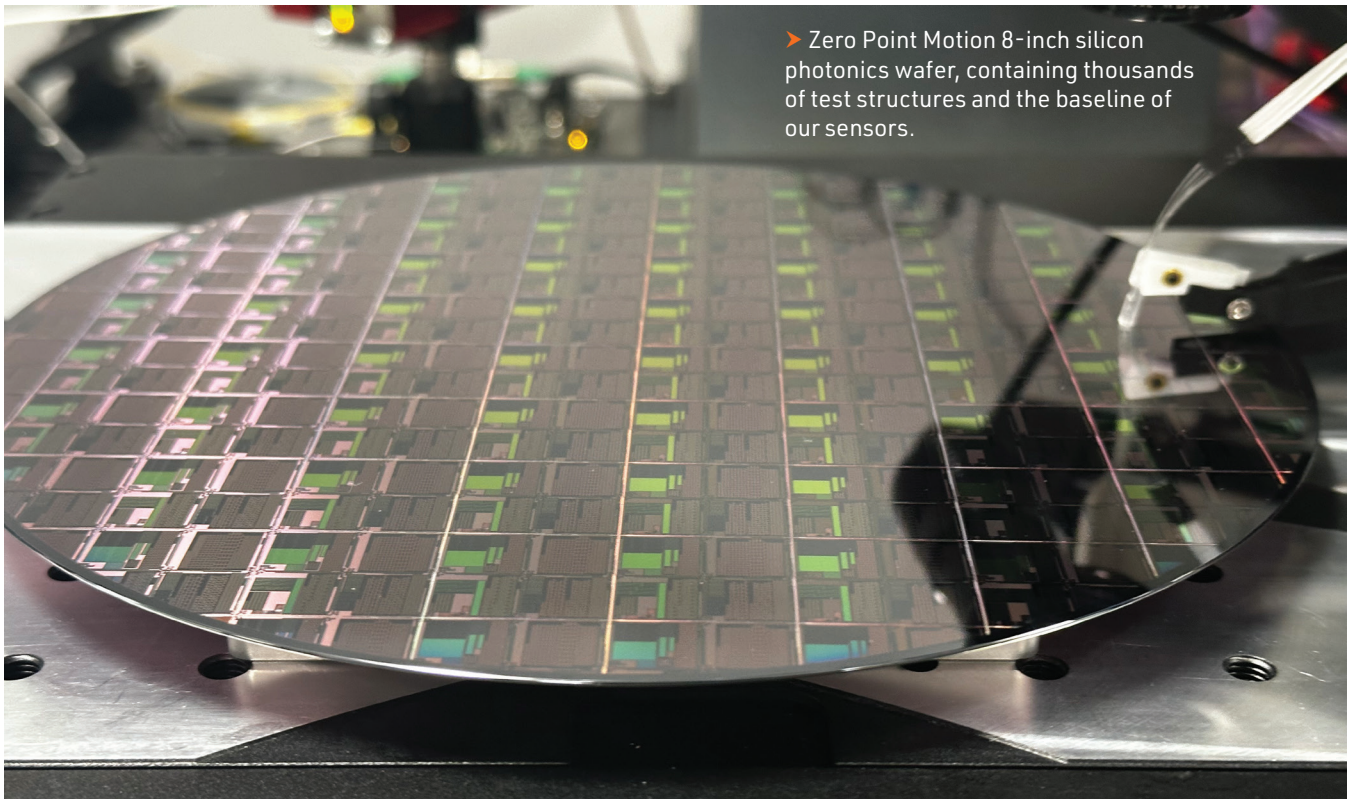


➤ Zero Point Motion 8-inch silicon photonics wafer, containing thousands of test structures and the baseline of our sensors.

Driving the next high-volume sensor revolution

Zero Point Motion is pioneering photonically enhanced inertial sensors, revealing how silicon photonics can break free from datacentres and become ubiquitous in everyday devices, but this transformation will require industry-wide cooperation.

BY LIA LI, CEO AND FOUNDER, ZERO POINT MOTION

THERE IS NO DOUBT that photonics is poised to transform the future, by enhancing existing technologies and enabling entirely new applications. My mission, and the reason I founded Zero Point Motion, is to answer one question: how do we bring photonics into everyday life?

Today, datacentres dominate high-volume photonics. They are massive, well funded, and rely on optical interconnects to power cloud computing and AI. This is "high volume but hidden away" – a market few consumers ever see directly.

Yet there's another high-volume future awaiting silicon photonics – one where photonic components reach the hands of the public in everyday environments. Imagine optical technology in smartphones, automobiles, VR headsets, or even home appliances. If these use cases truly take off, photonics could become as ubiquitous as electronics, bridging the gap between specialised labs and the mass market.

From my vantage point, the hold-up isn't a lack of ideas or even demand. Organisations are diving into photonic research for everything from quantum computing and telecoms to LiDAR and non-invasive biosensing. The real problem lies in scalability, standardisation, and packaging.

These hurdles were echoed at the Málaga Global Photonics Economic Forum in October 2024, where panellists discussing the question "Is photonics a semiconductor technology?" noted that a "lack of standardisation is due to companies not wanting to give up their IP," and that "the photonics industry has an emotional attachment to very small performance gains, even when it makes the technology non-manufacturable" [1]. This highlights a cultural challenge within photonics: the drive for incremental improvements can overshadow the need to build reproducible, scalable solutions.

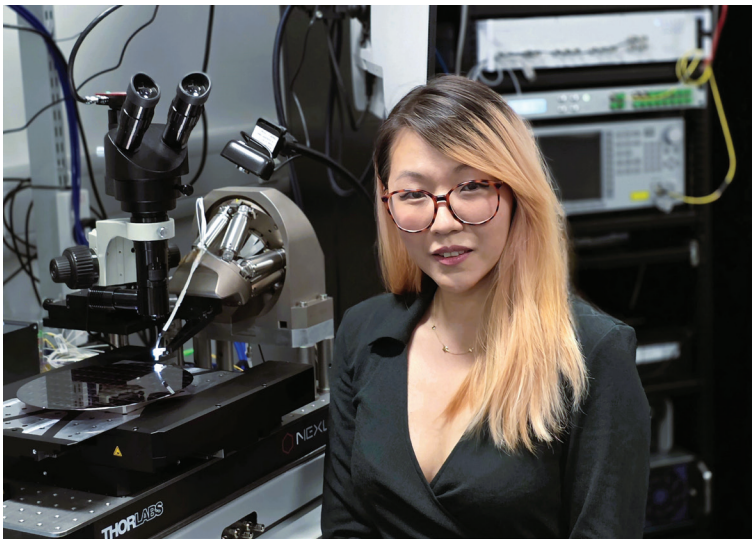
Interestingly, there's a parallel to draw with the world of micro-electro-mechanical systems (MEMS).

Unlike silicon photonics – which at least has process design kits (PDKs) to guide design and fabrication – MEMS manufacturing is notoriously custom and lacks an equivalent degree of standardisation. Yet MEMS has grown into a multi-billion-dollar industry, with some reports estimating its global value at around $16 billion. How did it get there? By thriving in diverse, high-impact applications, from automotive airbags to smartphone accelerometers to microphones, and overcoming its customisation challenges with robust foundry support, co-integration with CMOS, economies of scale for mass adoption, and relentless demand for miniaturised sensors.

In many ways, MEMS succeeded because of its customisation, not despite it. Being able to tailor designs for specific automotive, industrial, and consumer needs has delivered high-value products that competing sensor technologies have struggled to match at volume. Over time, specialised design tools, improved packaging, and greater supply-chain maturity made large-scale manufacturing more predictable. The lesson for photonics is clear: if we can leverage existing foundry processes, invest in packaging research, and tap into strong market needs, then high-volume silicon photonics can follow a similar trajectory.

Inertial sensing as a beachhead

At Zero Point Motion, we use photonics to build precise inertial sensors that track movement by measuring how a small silicon structure inside the sensor shifts in response to applied motion – just as you feel yourself sway when a car speeds up or turns. Inertial sensing is an area where existing low-cost solutions often reach performance ceilings, meaning that photonics can deliver a decisive improvement in accuracy. By replacing capacitive readout with optical sensing, we aim to achieve higher sensitivity, lower drift, and better robustness – key factors for applications ranging from industrial automation to robotics and augmented reality. Imagine a drone mapping a subterranean tunnel, a robot navigating a city's high-rises to deliver goods, or a vehicle finding its way through an underground car park. These are all scenarios where signals from global navigation satellite systems (GNSS) drop out or become unreliable due to multipath errors, whereby signals are reflected off obstacles in the surroundings, taking longer to be received. A more stable inertial measurement system can step in to maintain accurate positioning when GNSS is temporarily weakened or unavailable. If photonic inertial sensors offer superior drift performance, we can push the boundaries of autonomy, especially when combined with advanced sensor fusion and AI navigation algorithms.



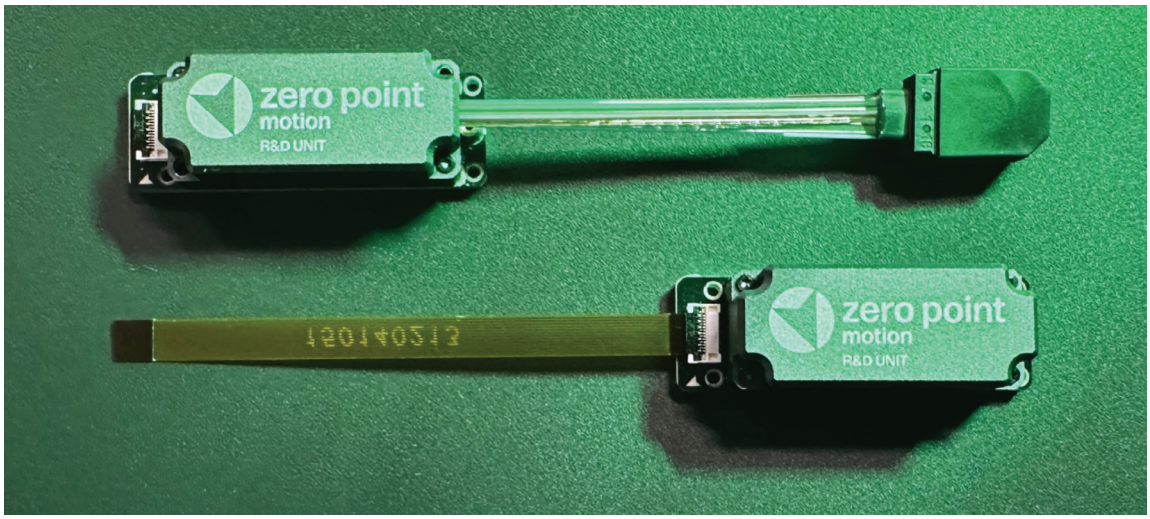
➤ Lia next to the ZPM semi-automated wafer prober which combines industry-grade equipment but with custom automation protocols and image recognition.

Crucially, to build the chips that underpin these sensors, we're not demanding exotic foundry setups; we're leveraging the same standard PIC processes already available in commercial fabs. Our goal is to show that photonic inertial sensors can be mass-produced on existing lines with minimal disruption to match the volumes of MEMS sensors shipped today.

Our sensors at ZPM harness the best of both worlds: MEMS for the large-mass mechanical response to a device's motion, and silicon photonics for ultra-sensitive optical readout. This approach represents the next step in the evolution of inertial sensing – akin to how companies like InvenSense once took a bold wafer-scale risk, stacking different semiconductor processes atop each other to revolutionise MEMS fabrication and integration with application-specific integrated circuits (ASICs).

By integrating optical waveguides with MEMS structures, we can eliminate many limitations of traditional inertial measurement units (IMUs), drastically reducing signal noise and drift while unlocking new possibilities in sensor design and signal processing. Specifically, we leverage the evanescent field of photonic waveguides and ring resonators to couple properties of light – like resonance features – with the motion of MEMS structures. As the MEMS moves within that evanescent field, subtle shifts in position alter the effective refractive index around the waveguide,

By integrating optical waveguides with MEMS structures, we can eliminate many limitations of traditional inertial measurement units, drastically reducing signal noise and drift while unlocking new possibilities in sensor design and signal processing



➤ Early prototypes showing both fibre-pigtailed and fully integrated devices.

changing the resonant frequencies of the optical cavity. This enables ultra-precise motion detection without the drawbacks of electrical noise or external interference. There's also a dissipative effect that broadens the resonance, increasing sensitivity and resolution even further.

A call for standardisation and industry cooperation

As exciting as photonic IMUs are, we face a harsh reality: without industry standardisation, start-ups can find themselves waiting months for a tape-out, then facing equally lengthy delays for packaging and integration. That's a timeline many start-ups cannot survive in.

At Zero Point Motion, we've chosen to take on a lot of these processes in house. We perform our own automated wafer-scale probing, fibre-array attach, photodetector attach, laser-on-submount integration, and packaging – compressing the time from design to prototypes. By removing multiple handoffs and dependencies, we can iterate more quickly – up to two months faster – to refine our designs and reach working prototypes in a fraction of the time that a fragmented supply chain would impose.

Yet no single company can do this alone, and we certainly cannot get to production this way. We need industry-wide alignment on a few fronts. Many ecosystem players remain hesitant to share IP or adopt universal design kits and standards, slowing innovation and adoption. While foundry PDKs are an essential first step, a key takeaway from the 2024 PIC International Conference was that 80 percent of photonic value lies in packaging. To accelerate progress, the industry must advance proven equipment, standardised processes, and accessible entry points for new players. Establishing these will build confidence, reduce prototyping time, and speed up market entry.

Photonics for AI gets plenty of headlines, but other promising applications, like sensing, can also drive the volumes necessary to make photonics mainstream. The industry as a whole stands to gain from championing multiple high-volume use cases, not just one. By building more predictable supply chains, smaller packaging solutions, and open standards, we can unlock an ecosystem that scales photonics as easily as we now scale MEMS or CMOS-based processes.

The sensor revolution is at a crossroads. Photonics can remain a niche technology, confined to specialised or high-end datacentre applications, or it can leap into everyday devices, treading the path MEMS sensors have taken over the past few decades. From my perspective, the choice is clear: we have to go big. By integrating photonic and MEMS platforms in ways that leverage existing foundries and packaging lines, we can unlock that next wave of scalable, high-performance sensors. From medical monitoring and automotive LiDAR to AR/VR motion sensing and robotics, there's no shortage of markets eager for greater precision and reliability.

However, we won't get there by inching forward with incremental improvements and proprietary processes. We need a unified push – from conferences to consortia – to standardise what we can, invest in robust packaging solutions, and open up to collaborative, cross-company efforts. If we do that, I believe that the next decade will see photonic sensors reach ubiquity, becoming woven seamlessly into consumer and industrial devices worldwide.

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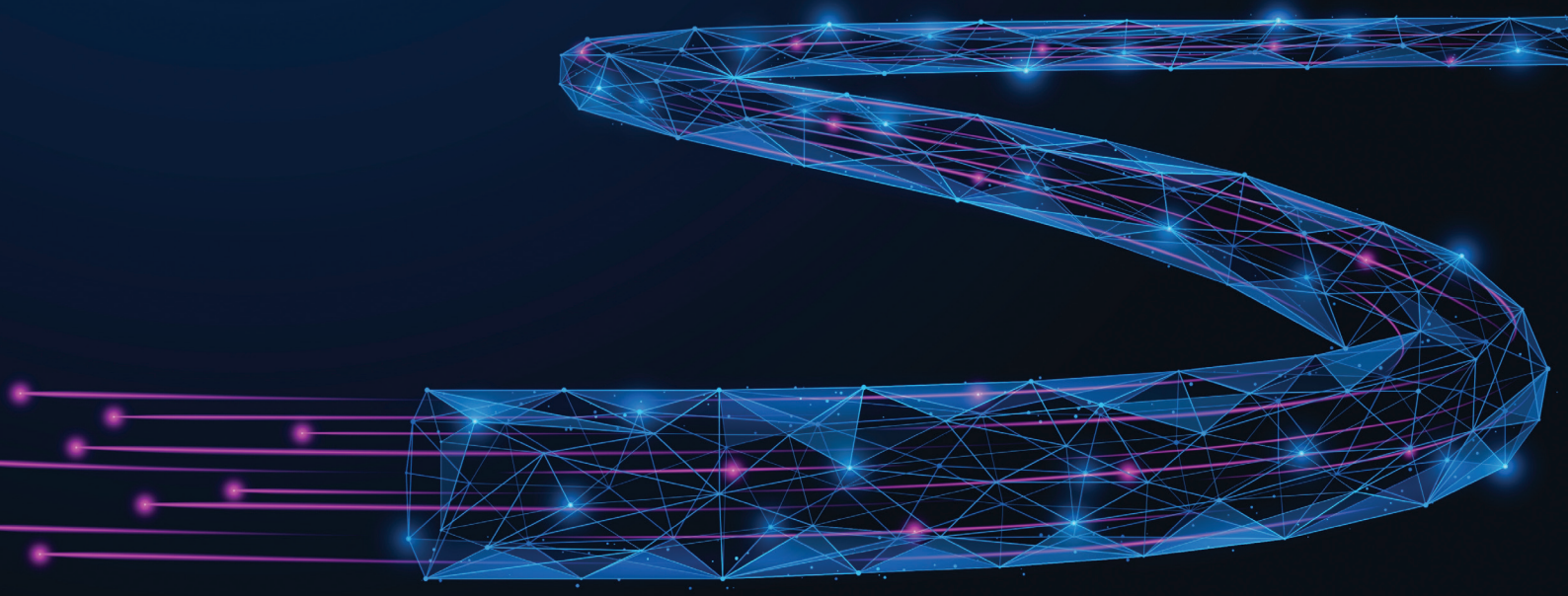


An outlook on the evolution of PICs for future interconnects

Optical transceivers' capacity has historically grown by 1 dB per year. AI now requires more rapid advances towards 100T or beyond over the next decade. Numerous promising technologies could overcome current bottlenecks.

BY YIKAI SU, FULL PROFESSOR IN ELECTRICAL ENGINEERING, SHANGHAI JIAO TONG UNIVERSITY

In today's complex global networks, where vast amounts of data must be processed, stored, located, and transmitted, a breakthrough in a single component is not always enough to drive progress at a macroscopic scale. Rather, such advancements can facilitate greater capacity, but only if they can be incorporated into the whole system, and if there are not bottlenecks elsewhere.

Yet there has historically been a mismatch in the growth rates of computational and data transmission technologies. The speed of computing hardware such as CPUs and GPUs has increased at an exponential annual growth rate of 73.8 percent, or 2.4 dB per year. Meanwhile, the interconnect technologies, both electrical and optical, have lagged behind; over the past decade or so, the data rates for electrical connects between electronic chips grew at 0.73 dB per year [1], while optical interconnects improved modestly more quickly at 1 dB per year [2].

Now, the emergence and rapid proliferation of AI applications has tremendously boosted demand for higher data capacities to an unprecedented rate of approximately 10 dB per year [3]. This number has two implications. First, more computing racks and clusters are needed to compensate for the gap between the required AI datacentre capacity growth (10 dB per year) and computing hardware development (2.4 dB per year). This has led datacentres to explore scale-up and scale-out approaches.

The second result is that the industry urgently needs significant innovations in interconnect technologies to keep up with the advances in computing hardware and overall AI datacentre expansion.

Even with optical interconnects, the gain of 1 dB per year for a module is much slower than that of computing electronics, and may eventually become a bottleneck in AI clusters.

We can estimate a baseline for the future capacity growth of optical interconnects, assuming that future development is unlikely to be slower than the past rate of 1 dB per year. Figure 1 shows this lower bound for the projected capacity growth of interconnect PICs, starting at 1.6T for existing products [3], and at 4T for chips demonstrated in research labs [4]. Following the trend, the capacities rise to 16T for commercial products and 40T for lab advancements in the next 10 years. These predictions offer bottom-line targets, because new technologies are likely to appear and considerably accelerate progress in R&D and commercialisation.

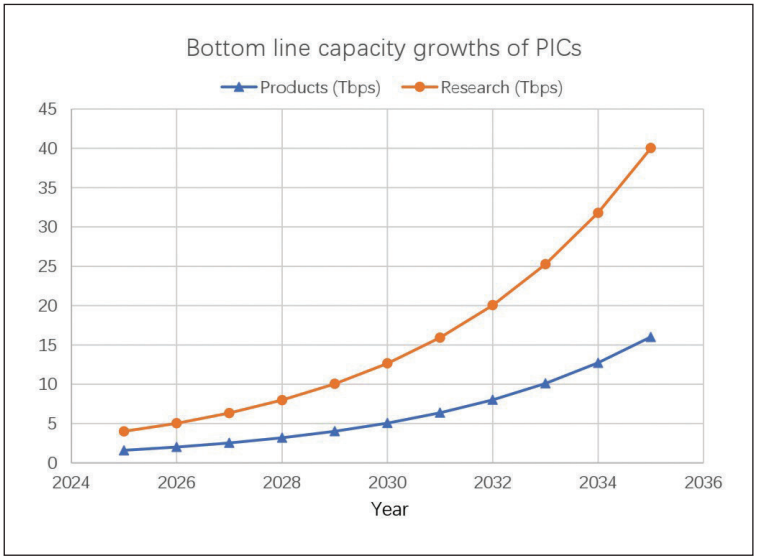
On the other hand, we can also calculate an aspirational target for the development of optical interconnects in a hypothetical scenario where it keeps up with computing electronics. This high rate of 73.8 percent (2.4 dB per year) is ambitious but may not be impossible for PICs to achieve. Looking inside a CPU or GPU, the clock rate has remained almost the same for years, but computing power has continued to grow, thanks to the massively parallel processing of data streams. Optical interconnects may take a similar technological path, with massively parallel channels integrated on a PIC. If optical input/output were to catch up and keep pace with the development of computing and switching chips, the extrapolated capacities would reach unprecedented levels of 100T or even achieve rates on the order of Petabits per second (Pbps), as Figure 2 illustrates.

The goal of realising a 100T-class PIC or beyond presents significant challenges for incumbent technologies, as some of them may come up against theoretical limits. Silicon modulators based on the carrier dispersion effect, for example, have a theoretical maximum bandwidth of approximately 100 GHz. Even using Nyquist shaping and PAM-4 to increase data rates, the modulator's single-polarisation limit may be 400G.

Required performances and associated challenges

The single-channel data rate for current PICs is 100G, and engineers are targeting 200G and beyond for next-generation PICs. If we take 256G as the raw data rate for a single channel, we would need a total of 4096 channels to accommodate 1 Pbps. Even with a dense channel spacing of 50 GHz, one waveband cannot support the required capacity for this goal. Designs will therefore need multiple fibres and multi-wavelength channels. Specifically, we can calculate that 64 fibres and 32 wavelengths would be required [5].

Bandwidth scaling of electronics can help to increase the single-channel data rate and thus reduce the number of channels. However, this is likely to happen at a slower pace than the rising demand for data, due to intrinsic limitations set by materials and device operation principles. Even with huge strides in the single-channel data rate approaching 1T, 1000 channels would still be needed to achieve the Pbps capacity. It is therefore likely that dense integration of massively parallel channels will be essential.

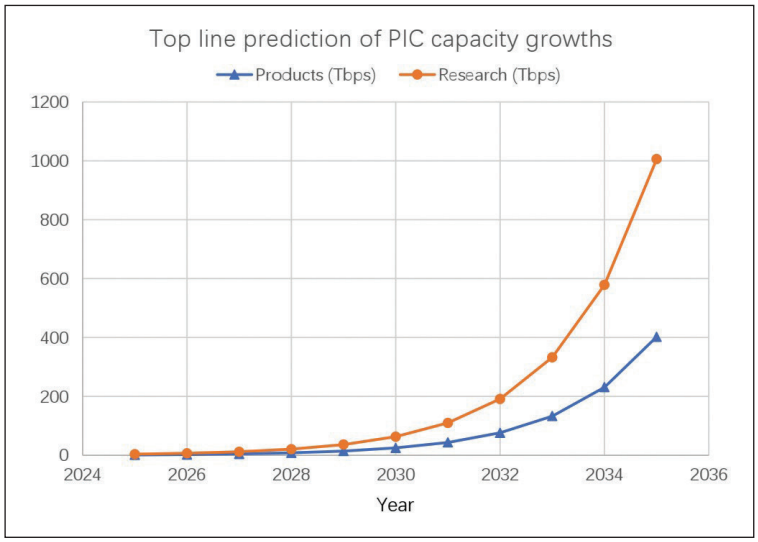


➤ Figure 1. Predicted capacity growth for PICs. The current year of 2025 starts with 1.6T for optical transceiver modules in production, while lab prototypes have demonstrated 4T PICs. Using the annual growth rate of 1 dB per year for optical modules based on historical data, the PIC capacities for products and lab demonstrations will very likely to increase to at least 16T and 40T, respectively, in 10 years. New technologies are expected to speed up the process driven by the recent emergence of AI with R&D funding support from industry and academia.

Each channel typically consists of a laser source, a modulation device, a (de)multiplexer, a photo detector (PD), and analogue electronics. Practically implementing such a high channel count on a large-capacity PIC poses many engineering challenges, including accommodating high integration density while avoiding crosstalk and maintaining high yield, as well as developing feasible high-speed dense packaging.

Summing up the footprints of these components, the minimum chip size is 462 mm^2 [5], and the resulting bandwidth density is 2.16T per mm^2. However, this calculation allowed for no margin, so the practical chip size would be much larger than the ideal case. This large footprint presents fabrication issues, such as uniformity across the wafer and stitching errors, as well as the problem of higher propagation loss on a wafer-scale chip.

Another challenge lies in the chip's power efficiency and total power consumption. Assuming the modulators, PDs, and peripheral analogue electronics each consume 100 fJ per bit, the power



➤ Figure 2. The projected upper bound capacities are calculated assuming technological breakthroughs in photonics enable the same rate of growth as that of computing hardware (GPUs, CPUs), which may be feasible through dense integration of massively parallel channels on a PIC. However 100T or Pbps-class PICs will encounter significant challenges and some fundamental limitations.

consumption is 300 W for these components. By adding 192 W power from the distributed-feedback Bragg-grating (DFB) laser array, the total power consumption for a PIC is 592 W, which may exceed the capability of conventional thermal management systems.

Table 1 summarises the required performances for a 1 Pbps PIC and the associated challenges [5]. There are three major bottlenecks: integration and packaging of massively parallel channels on the order of thousands; a large, potentially wafer-scale PIC footprint; and high power consumption of a few hundred watts, requiring active components to have ultra-high power efficiencies better than 100 fJ per bit. The parameters listed in the table are close to the ideal cases calculated from the best reported or projected results. Real implementations may face significant engineering challenges to achieve unprecedented performances while simultaneously ensuring that the Pbps PIC is functional under practical conditions.

➤ Table 1. Top-line requirements for a 1 Pbps PIC and the associated challenges.

Performance	Top-line requirement (10 years)	Challenges
Capacity	1000T (1 Pbps)	
Channel count	4096 (256G per channel)	Integration and packaging bottleneck
Chip size	462 mm^2	Footprint bottleneck
Bandwidth density	2.16T per mm^2	
Power efficiency	100 fJ per bit each for modulators, PDs, and analogue electronics	Power bottleneck (300 W power wall for thermal management)
Total power	592 W (including 192 W for DFB laser array)	

Breakthroughs to overcome bottlenecks

While the challenges outlined in Table 1 currently present significant obstacles to achieving Pbps-class PICs, they also offer opportunities for huge performance improvements, should they be overcome. The expanding field of PIC research across a wide range of optical components offers numerous routes to potential breakthroughs.

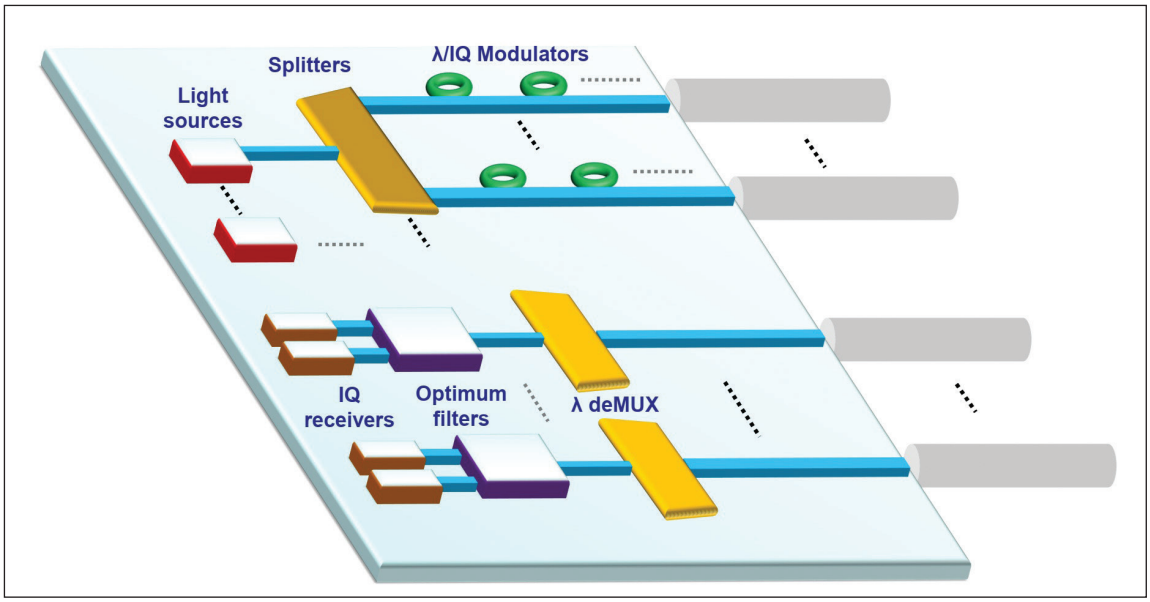
Since lasers account for a large portion of the footprint and power consumption of PICs, progress in laser integration may significantly improve PIC performance. A conventional DFB laser with power split may provide 8-16 channel outputs, but multi-wavelength lasers could allow for more. Various types of comb lasers have attracted tremendous interest in academia, including silicon nitride frequency combs and quantum dot (QD) mode locked lasers (MLLs), among others.

Comb lasers can substantially reduce insertion losses originating from fibre coupling and packaging. Due to the large number of wavelengths they generate, comb lasers offer advantages in terms of compactness and integration density. In particular, III-V QD MLLs exhibit high efficiencies with inherent defect and temperature insensitivity. Silicon nitride frequency combs also provide multi-wavelength outputs based on Kerr nonlinearity and dispersion management. Both schemes offer broadband multi-wavelength outputs, reduced footprints, and reduced number of lasers employed. For large-scale integration, however, additional on-chip optical amplification of the laser output may be required.

Advanced modulators are another component with potential to overcome current performance barriers. Conventional Mach-Zehnder silicon modulators occupy large footprints due to the weak electro-optic (EO) effect based on carrier induced dispersion. Resonator modulators, such as micro-ring resonators (MRR), Bragg gratings, and nanobeam resonators, can significantly shrink the footprints. Higher-speed ultra-compact modulators will be key to reducing the number of channels and the PIC footprint.

As previously mentioned, silicon modulators may approach their bandwidth limit, but new EO materials with high EO coefficients are emerging for heterogeneous integration, such as ferroelectric materials including lithium niobate and barium titanate, and high-reliability EO polymer materials. Other desirable features for next-generation modulators include intensity/quadrature (IQ) modulation, athermal operation, driver-less or capacitive-driven modulation, high process tolerance, and ultra-low power consumption heaters.

Improvements in MUX/DEMUX devices could also offer an opportunity for progress. Arrayed waveguide gratings (AWG) and cascaded MRRs are two devices typically used for wavelength (de)multiplexing. MRRs



➤ Figure 3. A conceptual illustration of possible techniques integrated on a PIC. In the transmitter component, power splitting and wavelength demultiplexing may be employed to construct thousands of data channels. Ultra-compact and high-speed modulators modulate the data on the optical carriers. At the receiver side, IQ DD receivers may double the capacity. 2.5D or 3D co-integration of electronics can be implemented with the PIC (not shown in the figure). High channel number, footprint and power consumption will be the bottlenecks to overcome.

have a larger footprint relative to AWGs if the channel count is high. Innovations in this area may include sub-wavelength engineering and inverse design. Currently it is still challenging to simultaneously optimise characteristics including loss, passband, crosstalk, channel number, and fabrication-error tolerance. Technological advances are needed in terms of design and fabrication methodologies.

When it comes to photodetectors and receivers, speed and efficiency are two key factors to consider. New materials may be explored, with one exciting area of development being the co-integration of PDs and electronic amplifiers using 2.5D or 3D integration techniques, allowing for reduced footprints and power consumptions. Another research direction focuses on improving the electrical spectral efficiency and thus the data rate of a direct detection receiver close to that of a coherent receiver by using full-field recovery technology – directly detecting the phase component of a complex signal in addition to its amplitude information without the need for coherent detection. In this case, optimised filters are crucial in the receiver design.

Finally, high-density packaging and thermal management on a PIC with thousands of high-speed electric contacts is a focus area with promising approaches for progress. By using nanophotonic interposers and automated assembly techniques with nanometre-level precision, for example, researchers can improve packaging efficiency and alignment accuracy. On the thermal management side, advanced cooling solutions such as microfluidic cooling through microfluidic channels, can manage heat effectively.

Figure 3 illustrates a vision of how some of the techniques described above might be integrated on a PIC. These are just some of the research areas that could unlock the next step change in performance in integrated photonics. New innovations will always arise, and it is possible that advancements other than those outlined here may change the path of PIC development, overcoming bottlenecks and accelerating the realisation of Pbps-level PICs.

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200G+ per lane: powering the next-gen data deluge

Integrated photonics is pushing the boundaries of data transmission, enabling speeds of 200G per lane and beyond. This leap forward promises to revolutionise datacentres and telecommunications, addressing the ever-growing demand for bandwidth driven by the proliferation of AI/ML.

BY ADAM CARTER, CEO, OPENLIGHT

GLOBAL DATA TRAFFIC is growing exponentially, with a huge increase in the amount of information created, consumed, and stored worldwide driven by trends like video streaming, the internet of things (IoT), and most significantly the rise of artificial intelligence and machine learning (AI/ML). As AI models grow in complexity and capability, the need for robust datacentre infrastructure is becoming more pressing than ever before.

Industry projections from JLL estimate that global datacentre storage capacity will soar from 10.1 zettabytes (ZB) in 2023 to a staggering 21.0 ZB by 2027, reflecting an annual growth rate of 18.5 percent. This demand requires network infrastructure capable of handling vastly higher data rates, pushing the boundaries of incumbent technologies. Current optical and electrical systems are struggling to keep pace, facing limitations in power efficiency, thermal management, and scalability.

A target in this evolution is PICs that can achieve 200G per lane, a milestone representing a significant leap forward in data transmission speeds. But scaling to 200G and beyond presents numerous challenges, including thermal management, power efficiency, signal integrity, and manufacturing scalability. Moreover, these hurdles are compounded by the increasing complexity of chip designs, the need for new materials and interconnect technologies, and the ever-present pressure to reduce costs. Utilising a heterogeneous PIC offers a 50 percent cost saving by leveraging the economies of scale of a commercial silicon foundry process versus the conventional manufacturing process for a transmitter optical sub-assembly.

While photonic technologies typically generate less heat per bit than electronic ICs, rising data rates mean that PICs, too, must incorporate effective thermal management strategies to ensure reliability and performance. Some high-speed solutions require thermoelectric coolers (TECs), but these have the drawback of increased power consumption. OpenLight's solutions, meanwhile, can avoid TECs altogether, thus offering better power efficiency.

Photonics also offers inherent energy advantages over traditional electronics, but maintaining low power consumption at ultra-high speeds remains a hurdle due to the energy needed to operate active components such as lasers and modulators,

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The EAM technology that OpenLight employs is particularly noteworthy, offering high-speed operation proven to over 65 GHz and targeting 100 GHz+ for 400G-per-lane support

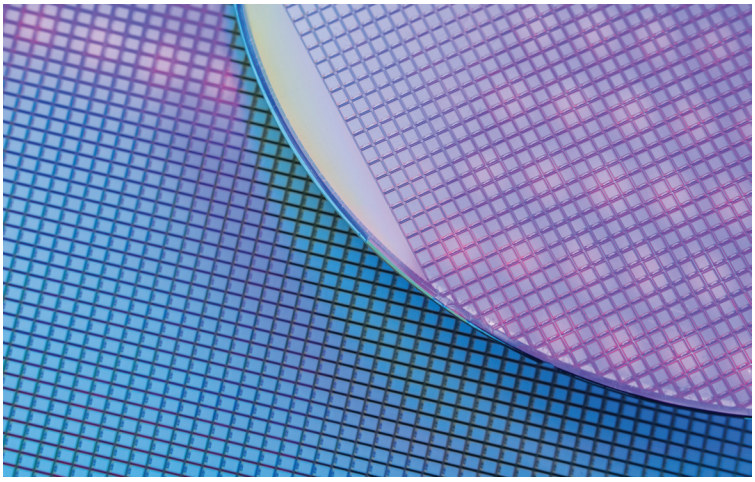
which are necessary for manipulating light signals effectively. This technology achieves over 40 percent power savings compared to traditional methods. By leveraging heterogeneous integration for superior waveguide coupling, this method significantly reduces the drive voltage needed for the desired output power. Furthermore, InP modulators require lower drive voltages than silicon modulators at 200G per channel, further contributing to energy efficiency.

When it comes to signal integrity, preserving quality over long distances and at such high speeds requires innovative design approaches, including advanced modulation formats and robust error-correction mechanisms. Traditional PICs, relying on external components, also face limitations in size, cost, and manufacturability, making them unsuitable for widespread deployment at higher speeds.

The OpenLight 1.6T DR8 PIC

To meet the demands of next-generation datacentres and AI infrastructure, OpenLight is developing the 1.6T DR8 PIC, which supports 200G-per-lane architectures. Currently at the alpha sampling stage, it represents remarkable progress in heterogeneously integrated silicon photonics and incorporates several features designed to address the critical challenges of high-speed data transmission.

To achieve high-performance 1.6T DR8 PICs, two key technologies are essential: distributed feedback lasers (DFBs) and electro-absorption modulators (EAMs). DFBs are used for their ability to provide a stable and precise light source, crucial for high-quality signal generation. EAMs, meanwhile, are used to modulate the light signal, encoding data onto it at incredibly high speeds.



OpenLight's 1.6T design includes both of these core enabling elements. Power-efficient DFBs serve as the PIC's light source, with integrated semiconductor optical amplifiers mitigating optical losses at 200G. This not only enables unprecedented data rates but also lays the foundation for future 3.2T infrastructure running at 400G per lane, a critical requirement for the continued growth of AI networks.

The EAM technology that OpenLight employs is particularly noteworthy, offering high-speed operation proven to over 65 GHz and targeting 100 GHz+ for 400G-per-lane support. At the same time, the PIC is small in size to allow for tight integration, temperature independent to eliminate the need for external cooling, and can be driven with differential or single-ended drives at low voltage. The 1.6T DR8 PIC achieves all this in a compact 37 mm^2 form factor and consumes a maximum of just 2.2 W, demonstrating exceptional energy efficiency.

The OpenLight platform: empowering innovation

Beyond developing our own technology, we are also acting on our commitment to an open platform and this is changing the game for the photonics industry. By providing Process Design Kits (PDKs) to foster a collaborative ecosystem, we are empowering companies to develop their own custom PIC solutions. Partnering with key players like Tower Semiconductor, Synopsys, and others will further strengthen this ecosystem to provide designers with the tools they need to succeed.

The future of data transmission hinges on the ability to move information at ever-increasing speeds. Breaking the 200G barrier represents a leap towards that future. As data demands continue to grow rapidly, innovations like heterogeneously integrated silicon photonics with DFBs and high-speed EAMs will be essential to driving progress. The continuous evolution of the PIC market fuelled by advancements in integrated photonics will open new opportunities in applications like 5G/6G networks, quantum computing, autonomous systems, and medical diagnostics. At the same time, industry-wide adoption of heterogeneously integrated PICs will drive standardisation and reduce fragmentation in the photonics ecosystem, creating a more streamlined approach to designing and manufacturing photonic systems.

OpenLight's technology promises to reshape datacentres, power the next generation of AI, and impact a wide range of fields, while our open platform is helping to cultivate a thriving industry that will be ready to meet the data needs of tomorrow.

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