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VIEWPOINT

BY SARAB CHOPRA
EDITOR

Advancing Photonics Innovation

The pace of innovation in photonics is accelerating, and 2026 is shaping up to be a pivotal year for the field. From AI data centres and quantum computing to human-safe pathogen control, photonics is redefining performance, efficiency, and scalability.

At the heart of this progress is the convergence of hybrid integration, chiplet architectures, and photonic integrated circuits, providing solutions to challenges that have long constrained computing and semiconductor systems.

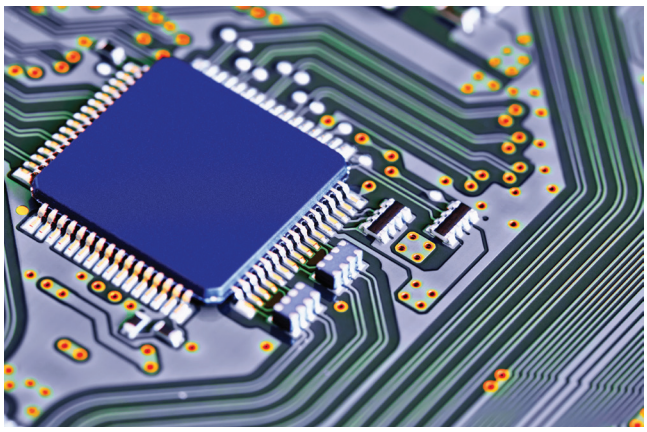
In AI computing, copper interconnects are increasingly a bottleneck. Traditional electrical pathways struggle to deliver the bandwidth, energy efficiency, and low latency needed for large-scale AI models. Co-packaged optics, hybrid integration, and optical engines offer a solution.

By embedding optical components directly with processors, these approaches shorten interconnect paths, reduce power consumption, and allow unprecedented bandwidth density. The result is AI infrastructure capable of scaling to meet the demands of multimodal processing and massive parallelism.

Hybrid integration is particularly transformative. By combining diverse materials and components in a single package, chiplet-based architectures improve yield, accelerate development, and reduce cost per bit.

Breaking monolithic chips into smaller, tested dies that can be assembled at wafer scale lowers energy per bit, reduces latency, and increases bandwidth density. Optical engines, integrating lasers, modulators, detectors, and waveguides into single chiplets, bridge electronics and optical signalling, enabling high-speed, scalable solutions for AI clusters. Photonics is also advancing quantum-enhanced computing. Hybrid photonic-electronic platforms show that light can tackle complex optimisation problems with efficiency beyond conventional computing.

Using entropy computing, single-photon counting, and electro-optic feedback, these systems handle non-convex and combinatorial challenges, including NP-hard tasks. Integrating such systems onto photonic circuits promises

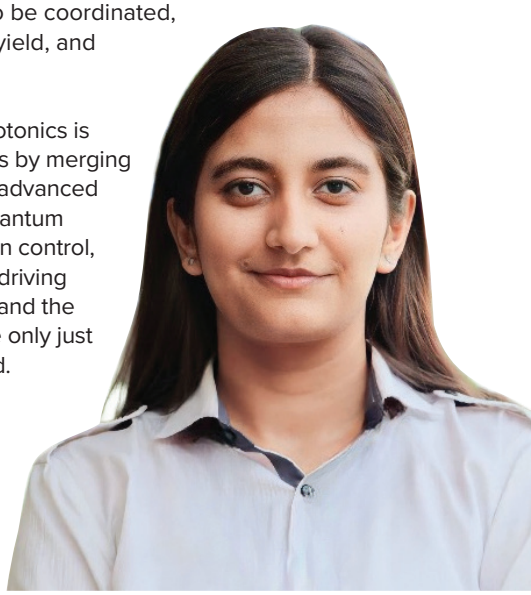


compact, scalable, room-temperature-compatible quantum solutions.

Beyond computing, photonics is making an impact on public health. Far-UVC photonic chips deliver pathogen-lethal light safely and efficiently in air, on surfaces, and in water. By generating spectrally pure far-UVC light on-chip, these devices overcome the limitations of traditional ultraviolet sources, offering a scalable and practical solution for continuous disinfection.

Testing and validation are evolving alongside these technologies. Narrow-linewidth lasers, precise polarisation control, and synchronised high-density test architectures are now essential. Modular platforms allow multiple sources, switches, and metres to be coordinated, improving throughput, yield, and reliability.

Across applications, photonics is enabling new paradigms by merging optics, electronics, and advanced materials. From AI to quantum optimisation to pathogen control, these technologies are driving transformative change, and the opportunities ahead are only just beginning to be realised.



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UK's CORNERSTONE to boost silicon photonics

CORNERSTONE Photonics Innovation Centre to accelerate silicon photonics prototyping, collaboration, and commercialisation, boosting its global competitiveness.

THE UK'S silicon photonics (SiPh) ecosystem is set for a major step forward with the launch of the CORNERSTONE Photonics Innovation Centre (C-PIC), designed to act as the national hub for research-to-market innovation.

Building on decades of academic excellence and open-access fabrication initiatives, C-PIC aims to accelerate prototyping, foster cross-industry collaboration, and strengthen the UK's position in the global SiPh supply chain.

SiPh, already transformative in data centres and telecoms, is now poised for emerging applications in quantum computing, LiDAR, biosensing, and AI acceleration.

Adoption, however, is challenged by integration costs, toolchain maturity, and fragmented collaboration. C-PIC addresses these hurdles by combining industry-aligned fabrication, open-access design enablement, and early engagement with investors and application specialists.

Its state-of-the-art facilities, including JEOL electron beam lithography systems, allow researchers and start-ups to prototype designs aligned with real-world system requirements.

The UK already benefits from world-class research at the University of Southampton's Optoelectronics Research Centre, a growing base of photonics SMEs, and support from initiatives like ChipStart UK, which has helped companies raise over £25 million since 2023.

Government-backed programmes through UKRI, EPSRC, and Innovate UK, alongside international engagement such as Taiwan's ITRI opening a London office, further strengthen the UK's global standing.

With SiPh projected to grow at 26–30% CAGR to 2030, C-PIC's coordinated approach aims to turn research strength into market-ready solutions, giving the UK a competitive edge in integrated photonics innovation.

Accelerating MEMS and photonics scaling

ADVANCES IN 300-mm wafer manufacturing are helping to close long-standing production gaps in MEMS and photonic integrated circuits (PICs), paving the way for broader commercial adoption and tighter integration with the semiconductor ecosystem.

Over the past two decades, PICs and MEMS technologieWs have transitioned from research-focused development to product-driven engineering, with growing demand from AI, data centers, sensing, and communications markets.

As applications scale, the emphasis has shifted from proving device feasibility to delivering high-volume, semiconductor-grade manufacturing with consistent yield and reliability.

A key enabler of this transition is the move toward 300-mm wafer platforms. While logic and memory manufacturing standardised on 300-mm production years ago, much of the MEMS and photonics industry continues to rely on smaller wafers and legacy tools.

Access to advanced 300-mm equipment improves film uniformity, etch precision, and process control factors critical to reducing optical loss, managing mechanical stress, and improving yield.

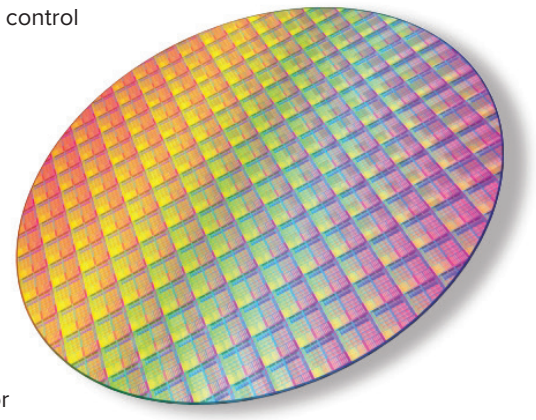
Both MEMS and photonics depend on high-quality thin films, precise etching, and advanced packaging.

Silicon nitride and oxide films underpin low-loss waveguides and MEMS structures alike, while increasingly complex etch processes must maintain tight dimensional and surface control across entire wafers.

Packaging remains another shared bottleneck, as optical alignment, wafer-level bonding, and thermal stability drive cost and scalability challenges.

Industry momentum is building around shared manufacturing platforms, particularly silicon-on-insulator substrates and wafer-level integration techniques.
As MEMS and photonics workflows continue to converge, improved process discipline and access to mature semiconductor infrastructure are expected to accelerate the path from prototype to high-volume production.

The shift toward scalable manufacturing marks a critical step in enabling the next generation of photonic and MEMS-based systems for sensing, communication, and computing.



DARPA launches $35M program to scale photonic circuits for AI computing

DARPA invests $35M in PICASSO to scale photonic circuits for AI, tackling system-level limits to unlock high-speed, energy-efficient computing.

DARPA has launched a new research initiative aimed at overcoming the fundamental physical limits that have so far prevented photonic integrated circuits from delivering large-scale computing advantages for artificial intelligence and other data-intensive workloads.

The program, titled Photonic Integrated Circuit Architectures for Scalable System Objectives (PICASSO), will distribute around $35 million in funding across multiple awards to develop photonic circuits capable of predictable, scalable system-level performance. Proposals are due by March 6, with the program expected to begin in July 2026.

While photonic circuits are already widely used for optical communication, DARPA argues that their role in computation remains constrained.

Current photonic computing demonstrations are typically limited to shallow circuit depths and simple linear operations, forcing frequent conversions between optical and electronic domains.

These conversions introduce latency and power penalties that negate many of photonics' inherent advantages in bandwidth, energy efficiency, and speed.

According to DARPA, the core challenge lies not in the lack of components, but in circuit-level architectural limitations rooted in the physics of light.

Optical attenuation and noise accumulation restrict signal fidelity as circuits scale, while spurious interference effects such as scattering, coupling, back reflections, and unwanted resonances become increasingly difficult to control across large, complex photonic systems.

PICASSO seeks to address these challenges by applying innovative circuit-level design strategies, rather than relying on new materials or devices.

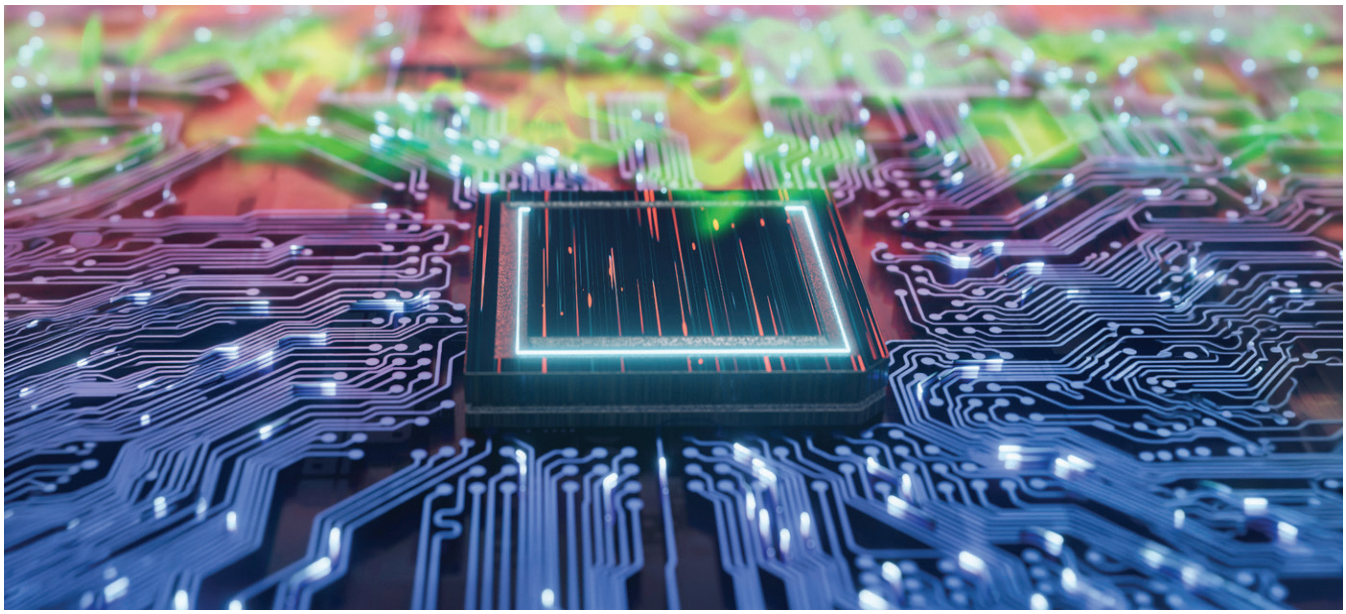
Drawing parallels with electronic circuit design, where architectural techniques compensate for transistor-level limitations, DARPA aims to demonstrate that today's photonic components can be assembled into far more capable and stable systems.

By the end of Phase 1, which runs for 18 months, program participants are expected to demonstrate photonic circuits with predictable performance at scale.

Phase 2, extending the program by a further 18 months, will focus on achieving generalised circuit functionality suitable for real computing workloads, including AI.

The initiative reflects growing interest in photonic computing as the semiconductor industry confronts power, bandwidth, and scaling constraints in electronic systems.

If successful, PICASSO could mark a significant step toward photonic architectures that move beyond niche applications and into mainstream computing platforms.



UC Davis develops AI spectrometer chip

UC Davis develops AI-powered spectrometer-on-a-chip, delivering lab-grade optical sensing in a sub-millimetre photonic device.

RESEARCHERS AT the University of California, Davis have demonstrated a spectrometer-on-a-chip that shrinks laboratory-grade optical sensing to a footprint smaller than a grain of sand.

The device combines nanostructured silicon photodetectors with artificial intelligence, eliminating the need for bulky optical components traditionally required for spectral analysis.

Instead of separating light using prisms or gratings, the chip employs 16 silicon photodetectors, each engineered with photon-trapping surface nanostructures that respond differently to incoming light.

These engineered surfaces extend silicon's sensitivity into the near-infrared, a spectral region that is typically challenging for standard silicon photodiodes.

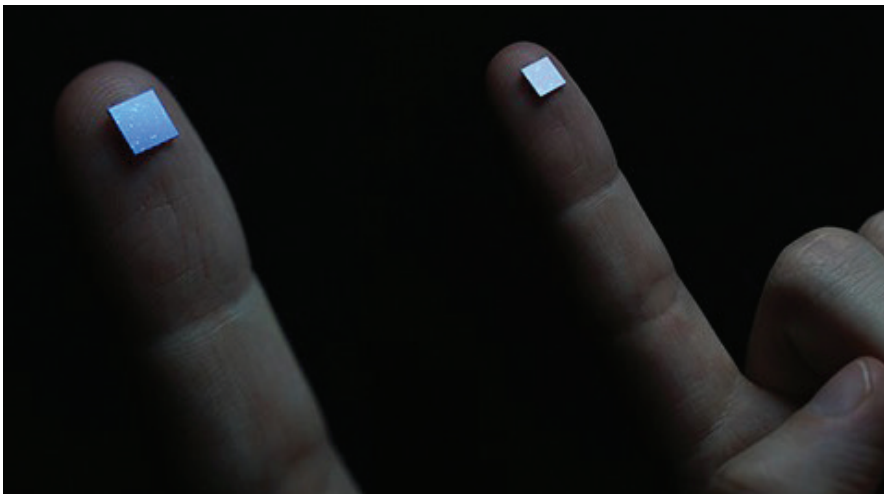
A fully connected neural network reconstructs the incoming light spectrum by learning the relationship between the detectors' encoded signals and the original spectrum.

The AI-based approach solves the inverse problem of spectral reconstruction, achieving approximately 8 nm resolution while maintaining high noise tolerance.

The chip occupies just 0.4 mm^2 and integrates high-speed sensing capabilities that also enable ultra-fast measurements of photon lifetime.

According to the researchers, the compact, low-power platform could enable real-time hyperspectral sensing in portable devices.

Led by postdoctoral researcher Ahasan Ahamed in the lab of Saif Islam, professor and chair of the Electrical and Computer Engineering department at UC Davis, the work points toward future photonic integrated circuits that combine nanophotonic structures with machine learning for applications ranging from medical diagnostics to environmental sensing.



Europe to secure lead in photonic chips

EUROPE CURRENTLY holds a leading position in photonic chip technology, a key enabler of energy-efficient digital infrastructure, advanced medical solutions, and sustainable innovation across mobility, agriculture, and communication systems.

However, industry leaders warn that without decisive investment and policy action, the EU risks losing its advantage as competition from the US and Asia intensifies.

A coalition of eight European CEOs, representing over 80 organisations in the photonic chip ecosystem and supported by PhotonDelta, is calling for targeted measures in the upcoming revision of the EU Chips Act.

Recommendations include accelerating industrial-scale production through open-access foundries, fostering public-private partnerships, simplifying regulations, and supporting talent development to strengthen Europe's innovation and investment climate.

Photonic chips, or Photonic Integrated Circuits (PICs), process information using light rather than electricity, offering higher speeds, lower energy consumption, and minimal heat generation.

This technology is crucial for AI, quantum computing, robotics, and sensing applications, making it a strategic asset for Europe's competitiveness and technological autonomy.

Industry leaders emphasise that urgent action is needed to move beyond pilot projects and ensure Europe remains at the forefront of the global photonic chip market.

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Dual function found in photonic component

Columbia researchers show that on-chip heaters in photonic circuits can double as precise temperature sensors, enabling real-time stabilisation without extra hardware.

RESEARCHERS AT Columbia University have demonstrated that a standard component already widely used in photonic integrated circuits can serve a second, critical function, offering a simple and scalable solution to one of integrated photonics' most persistent challenges: temperature control.

The team showed that thin-film metallic resistors, commonly used as on-chip heaters to tune photonic devices, can also act as accurate, real-time temperature sensors.

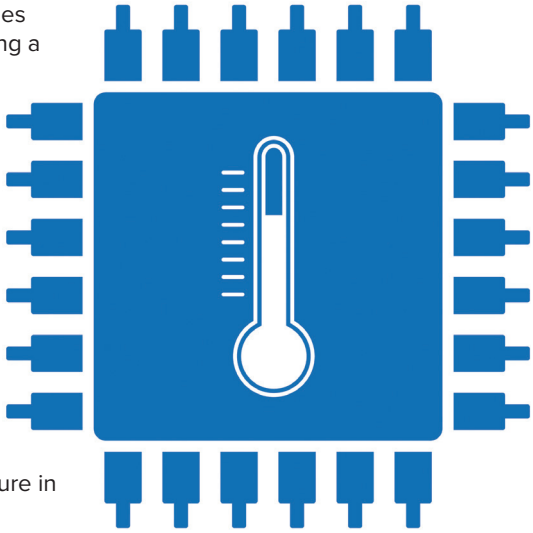
Photonic devices are highly sensitive to temperature fluctuations, with even small changes capable of shifting resonance frequencies and degrading performance.

Until now, monitoring chip temperature has typically required external sensors and additional hardware, creating obstacles for further miniaturisation and large-scale integration.

The Columbia researchers found that the thin-film platinum resistors already integrated into many photonic chips exhibit a strong temperature-dependent resistance, enabling them to function as on-chip resistance thermometers without adding new materials or fabrication steps.

The discovery emerged when the team observed large resistance changes in platinum heaters after modifying a chip's heat source.

Further investigation revealed non-Ohmic behaviour in the thin-film metal, similar to that seen in tungsten filaments, indicating a strong link between resistance and temperature.



By placing the resistor directly above a high-quality microcavity, the researchers were able to directly measure and stabilise the cavity temperature in real time.

Using this integrated thermometer, the team demonstrated long-term stabilisation of a photonic cavity by frequency-locking a commercial distributed feedback laser, maintaining wavelength stability within a picometer for more than two days.

Such performance is critical for optical communication systems and could be achieved without additional photodetectors or external sensing hardware.

The approach is platform-agnostic and compatible with existing foundry processes, making it applicable to a wide range of photonic devices, including silicon ring modulators already used in commercial data-centre applications.

The researchers also note potential benefits for emerging quantum photonic systems, where precise temperature control is essential and integrated sensing could help reduce system size and complexity.

The work represents a practical step toward more stable, scalable, and commercially viable photonic integrated circuits operating in real-world environments.

Caltech achieves ultralow loss photonic chips

RESEARCHERS AT Caltech, led by Kerry Vahala, Ted and Ginger Jenkins Professor of Information Science and Technology and Applied Physics, have demonstrated a photonic chip platform with ultralow optical loss approaching that of optical fibre, including at visible wavelengths.

The results, published in Nature, address a major limitation in photonic integrated circuits (PICs).

The work, led by postdoctoral scholar Hao-Jing Chen and graduate student Kellan Colburn, uses lithographically fabricated germano-silicate waveguides, the same glass material used in optical fibre, on standard silicon wafers.

A thermal reflow process smooths the waveguides to near-atomic roughness, significantly reducing scattering loss.

Devices fabricated on the platform match state-of-the-art silicon nitride PICs at near-infrared wavelengths and exceed previous visible-wavelength loss records by up to 20×.

Lasers demonstrated more than a 100-fold improvement in optical coherence.

The advance could enable ultra-coherent PICs for optical clocks, atomic sensors, quantum systems, and energy-efficient AI data-centre communications.

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Atomic layer processing advances silicon carbide quantum photonic circuits

Researchers advance silicon carbide quantum photonic circuits using atomic layer processing, paving the way for low-loss, scalable chip-based quantum technologies.

RESEARCHERS FROM the Max Planck Institute for the Science of Light and the Fraunhofer Institute for Integrated Systems and Device Technology IISB are advancing silicon carbide as a key material platform for next-generation photonic integrated circuits through the ALP-4-SiC project.

The initiative focuses on applying atomic layer processing techniques to improve the optical performance of silicon carbide-based microphotonic devices, supporting the development of scalable quantum photonic circuits.

Silicon carbide is gaining attention as a promising platform for photonics and quantum technologies due to its wide bandgap, compatibility with CMOS processes, and ability to host optically active colour centres that can operate at room temperature.

Within the project, researchers are using atomic layer etching to reduce surface roughness in silicon carbide waveguides and ring resonators, a critical step in minimising optical losses and enabling high-quality photonic components for integrated quantum systems.

The research addresses a major challenge in quantum photonics, translating complex laboratory optoelectronic systems into compact and manufacturable chips.

By improving photon confinement and reducing scattering losses, the work supports advanced functionalities such as nonlinear optical effects, optical frequency comb generation, and chip-scale photonic switches, which are essential building blocks for future quantum communication and computing platforms.

The ALP-4-SiC project combines the Max Planck Institute's expertise in photonic design and characterisation with Fraunhofer IISB's strengths in silicon carbide semiconductor technology and atomic layer processing.

Fully funded by the German Federal Ministry of Research, Technology, and Space under the WiVoPro programme, the initiative aims to bridge basic research and industrial process development, laying the groundwork for silicon carbide-based quantum photonic integrated circuits.

Global PIC market set to more than double by 2030

THE GLOBAL photonic integrated circuit (PIC) market is poised for rapid expansion, with its value expected to grow from $18.73 billion in 2026 to $42.21 billion by 2030, according to the Photonic Integrated Circuit Market Report 2026 released by Research and Markets.

The market is forecast to maintain a strong compound annual growth rate (CAGR) of 22.5%, driven by rising demand for high-speed data transmission and advances in semiconductor manufacturing.

Growth is being fuelled by the continued expansion of data centres, cloud computing, and optical fibre networks, alongside emerging applications in quantum computing.

Increasing adoption of energy-efficient photonic technologies in healthcare and life sciences, as well as the push toward autonomous and smart vehicles, is further accelerating market momentum.

High-speed internet deployment remains a key catalyst for PIC adoption. National broadband initiatives, such as Canada's target to achieve 98% high-speed internet coverage by 2026, highlight the growing reliance on photonic integrated circuits to support faster, more efficient data transmission using light rather than electrical signals.

Innovation and strategic activity are shaping the competitive landscape. Companies such as Keysight Technologies are introducing advanced design tools to streamline PIC development, while mergers and acquisitions continue to strengthen capabilities in next-generation computing.

In June 2025, Pasqal's acquisition of Aeponyx underscored the increasing role of PICs in enabling scalable and fault-tolerant quantum computing systems.

Major industry players, including Huawei Technologies, Intel, IBM, Cisco, and Fujitsu, are leading the market while navigating challenges such as tariffs and supply-chain pressures, particularly across Asia-Pacific and North America.

As demand accelerates across telecommunications, data centres, healthcare, automotive, and defence sectors, photonic integrated circuits are set to play a central role in the future of high-performance and energy-efficient digital infrastructure.

Perceptra secures €1.2m funding from PhotonDelta

MIT spin-off and winner of the Global Photonics Engineering Contest to relocate R&D to the Netherlands to develop PIC-based Raman sensors.

PERCEPTRA, the MIT spin-off pioneering photonic chip-based AI-enabled Raman sensors for chemical monitoring, has secured a €1.2m investment from PhotonDelta, the Dutch photonic chip industry accelerator.

The funding will accelerate the development and commercialisation of the company's next-generation photonic chip-based Raman sensors, based on a hybrid Silicon Nitride (SiN) and GaAs PIC platform.

Rather than relying on traditional dispersive spectrometers, the company deploys on-chip tuneable lasers to perform swept-source Raman spectroscopy. This architecture allows them to eliminate bulky dispersive spectrometers, drastically reduce system size, and enable high-sensitivity molecular analysis directly on the chip.

The ultra-compact design reduces system size 1,000× compared to traditional systems, and the low-cost architecture is claimed to be 100× cheaper to produce and deploy.

The €1.2m funding with a loan marks the next stage in the collaboration between Perceptra and PhotonDelta, following the startup's victory in the 2025 Global Photonics Engineering Contest for Raman sensor for real-time molecular monitoring in biomanufacturing.

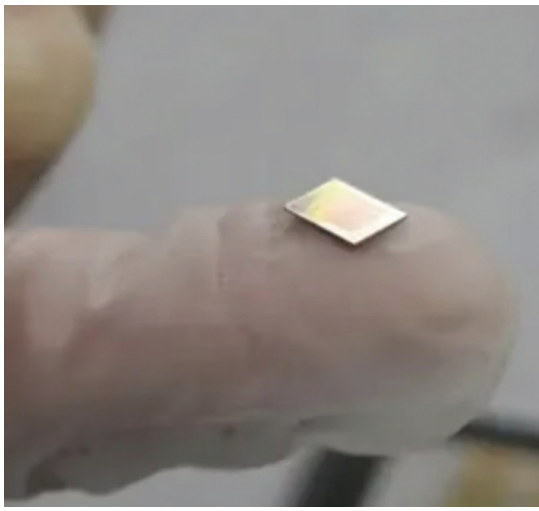
Perceptra is focused on developing its Raman sensor for real-time molecular monitoring. Having demonstrated proof-of-concept, Perceptra will use the funding to develop a first PIC-based version of the system.

Launching its innovative solution at the PIC Summit Europe 2025 in October, Perceptra took to the stage to share its journey from early-stage concept to ecosystem-backed venture, and outline the next stage of its technology roadmap. They also demonstrated a working prototype on the show floor developed in collaboration with PhiX Photonics Assembly and LioniX International.

The startup is relocating its integrated photonic R&D to the Netherlands to join the vibrant PhotonDelta ecosystem. This will facilitate access to a world-leading infrastructure, research networks, and a large engineering talent pool, enabling Perceptra to advance its technology and scale its business in Europe.

Amir Atabaki, CEO and co-founder of Perceptra, said: "PhotonDelta's funding marks a milestone moment in turning our research into a scalable venture. Integrated photonics is redefining what's possible in molecular sensing, and by joining the PhotonDelta ecosystem in the Netherlands, we will be able to accelerate development, access world-class fabrication, and bring our first photonic sensing products to market."

Laurens Weers, executive director and CFO at PhotonDelta, said: "Perceptra's announcement at PIC Summit Europe showcases the major strides the integrated photonics space is taking. It represents the kind of breakthrough thinking that integrated photonics enables. Their work at the intersection of photonic chip technology and AI is an example of how this technology can transform entire industries. We are excited to support Perceptra as they expand to the Netherlands and bring their vision to market."



MIT boosts quantum cooling with photonic chip

MIT RESEARCHERS have developed a photonic chip capable of cooling trapped ions in quantum computers to temperatures nearly ten times lower than standard laser cooling limits.

The breakthrough promises more compact and scalable chip-based quantum systems.

The chip integrates nanoscale antennas and waveguides to precisely control intersecting light beams, creating a rotating vortex that efficiently reduces ion vibrations.

By eliminating bulky external lasers and stabilising optical routing on-chip, the design overcomes major obstacles in traditional trapped-ion systems.

This advancement not only enhances cooling performance but also improves ion control precision, paving the way for scalable quantum computing with thousands of interconnected ions on a single chip.

Researchers say this integrated photonics approach could be a key step toward more stable, efficient, and miniaturised quantum computers.

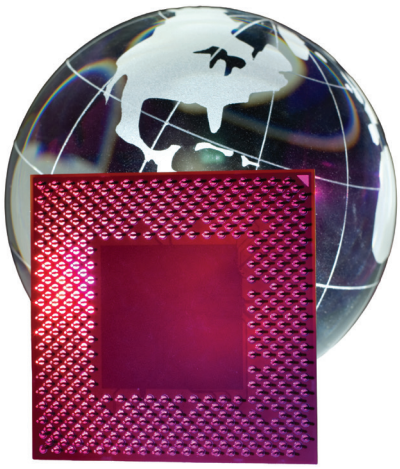
Global PIC market to reach US$31.7 billion by 2031

The global PIC market is forecast to surge to US$31.7 billion by 2031, driven by accelerating demand from data centres, AI, 5G, and high-performance computing.

THE GLOBAL PHOTONIC integrated circuit (PIC) market is projected to grow from US$3.2 billion in 2023 to US$31.7 billion by 2031, expanding at a CAGR of 33.2%, according to DataM Intelligence.

Growth is being driven by rising demand for high-speed data transmission, the expansion of optical communication networks, and increasing adoption of photonics in data centres, AI, 5G infrastructure and high-performance computing.

PICs enable faster processing and lower power consumption by integrating multiple photonic functions onto a single chip.



North America leads the market with around 40% share, supported by strong data centre investment and major players such as Intel and Cisco driving silicon photonics innovation.

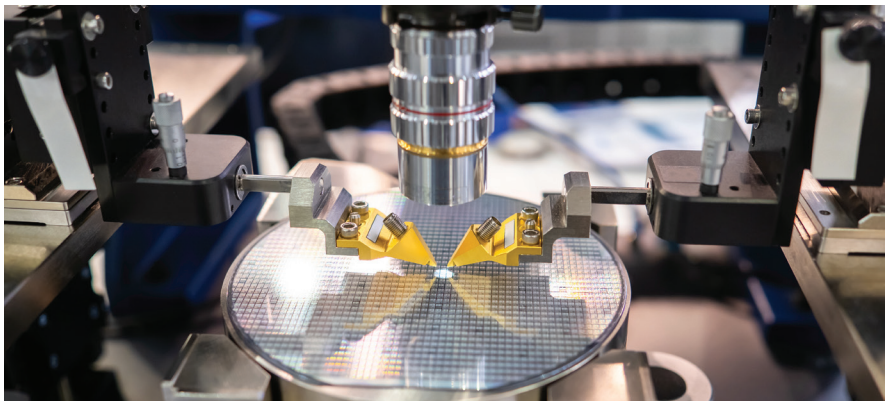
Ateneo expands PIC research collaboration

ATENEO DE MANILA University is strengthening international cooperation in photonics research through its Research on Optical and Electronic Systems Laboratory (ROSES Lab), the country's first facility dedicated to designing Photonic Integrated Circuits (PICs) and training local PIC engineers.

Founded in 2017 by physicist Benjamin B. Dingel, the laboratory has evolved into a national centre for optical sciences and photonics engineering, supporting the Philippines' efforts to build capabilities in light-based electronics and next-generation communication technologies.

The lab recently hosted the Workshop on Advanced Photonics Technologies for Emerging ICT and Sensing Applications at Ateneo's Loyola Heights campus, bringing together researchers from Japan, Thailand, Taiwan, and the Philippines under international research initiatives, including the e-Asia Joint Research Program and ASEAN collaborative projects.

Participating institutions included Waseda University, the National Institute of Information and Communications Technology, and Chiang Mai University, alongside regional industry partners.



With more than 85 scientific publications and support from national research agencies, the ROSES Lab aims to position the Philippines as an emerging contributor to global PIC design and photonics innovation.

The initiative focuses on advancing hybrid electronic-photonic systems for applications spanning telecommunications, computing, medical devices, and sensing technologies.

According to Dingel, expanding international collaboration remains central to accelerating local innovation and enabling the country to participate more actively in the global photonics ecosystem.

The development highlights growing efforts across Southeast Asia to strengthen PIC design expertise and photonics research infrastructure amid rising global demand for optical technologies.

POET

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Key features of our Optical Interposer-based technology:

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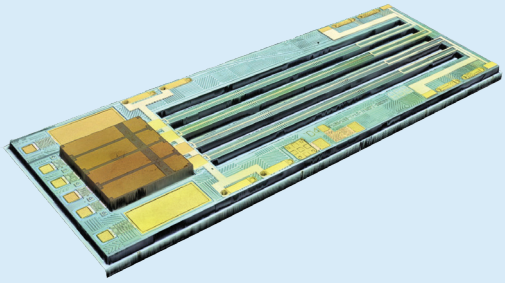
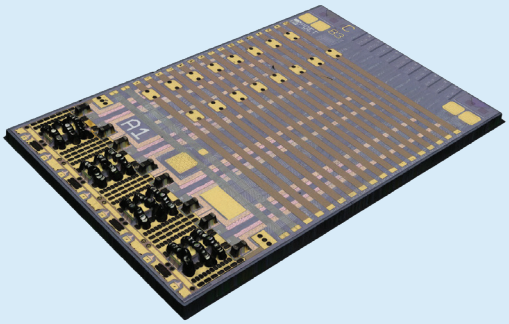
- Enabling next-generation interconnect solutions for 1.6T and above data rates
- Wafer-level chip-scale packaging (no wire bonds and no active alignments)

Our revolutionary products include:



POET Blazar
A high-power, multi-channel External Light Source. Designed to power both AI Scale-up and Scale-out Networks, including co-packaged optics.



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How co-packaged optics (CPO) is changing the game in optical testing

BY MATTHEW ADAMS, DIRECTOR OF PRODUCT LINE MANAGEMENT, VIAVI SOLUTIONS

Executive summary

CO-PACKAGED OPTIC (CPO) based designs promise dramatic gains in bandwidth density and power efficiency for next-generation switching by moving optical engines adjacent to the switch ASIC. This well-known architectural shift reduces high speed electrical trace lengths and board-level electrical losses, but it also reshapes test and measurement from the optical silicon on out: lasers move out of the PIC into external, field-replaceable modules, light is split across many channels, and the bar rises for source power, linewidth stability, and parametric test rigor.

The Optical Internetworking Forum's External Laser Small Form-Factor Pluggable (ELSFP) implementation agreement standardizes this model and enables high-power, multi-channel CW delivery inside the chassis via blind-mate optics—fundamentally altering how designers and manufacturing lines emulate and validate light sources and scale out test to manage the number of parallel optical paths. Both deeply impact on how CPO engines are tested.

The CPO impact on test and measurement

CPO integrates silicon-photonics (SiPh) optical engines next to the switch ASIC, replacing long, lossy electrical traces with short connections that mitigate channel loss and power-hungry equalization. As lane counts and radix grow to meet AI fabrics, CPO introduces new test surfaces and denser optical interfaces compared to pluggable modules: Silicon photonic optical interfaces, ultra-high density fibre management, and board-level laser distribution and control. For SiPh, CPO is a natural evolution—modulators, filters, and monitors are densely integrated on wafer, and on-package placement tightens control of coupling, thermal behavior, and telemetry—yet it elevates requirements for external laser quality during both characterization and production test along with the number of transmit and receiver ports to be characterized.

The external laser and the OIF ELSFP

The OIF ELSFP Implementation Agreement defines a faceplate-pluggable, blind-mate module that delivers continuous-wave (CW) laser power into a CPO system for distribution to multiple on-package optical engines. By locating the high-power lasers behind a blind-mate optical interface within the chassis, the ELSFP approach supports field-replaceability while addressing eye-safety and thermal isolation from the hot ASIC region. Public product announcements highlight the scale now expected per channel: for example, 16-channel ELSFP devices around the 100 mW per-channel level and modules specifying up to ~20 dBm per channel, illustrating the order of magnitude required so that downstream splitters, taps, and PIC insertion losses still leave sufficient margin for modulation and monitoring.

Given these specific design and deployment factors, it is critical to select the appropriate source for on-chip testing.

CPO PIC Testing: Start with the right photonic source

When lasers live outside the PIC, their output must be split and routed to multiple engines, modulators, and monitor taps. Each 1×2 split costs roughly 3 dB ideally, and real systems accrue additional

connectors, waveguide, and coupler losses, plus monitor taps for control loops. In practice, an adequate margin at each branch requires high initial launch power.

First, multi-channel distribution means the source must feed four, eight, or sixteen channels. After splitting the subdivided CW signal propagates within engines to serve both the modulation path and taps. Second, silicon-photonics elements (modulators, MUX/DEMUX, couplers) add several dB of insertion loss; as channel counts and monitor density grow, these losses multiply. Third, test itself requires headroom: thermal corners, VOA-emulated link budgets, alignment offsets, and loop dynamics all demand power surplus so the test bench can drive, perturb, and measure the DUT with confidence.

The ELSFP model's blind-mate, in-chassis interface simplifies delivering such high powers safely and serviceably compared with fully exposed faceplate optics, but we must also consider how to deliver this functionality during PIC testing. The source must not only have the power required, but additional properties that ensure we are validating the PIC performance and not simply testing the stability of the source.

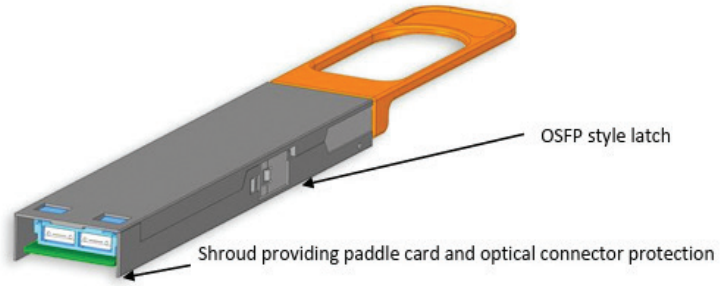
Why laser linewidth Is equally critical

Even though today's CPO fabrics for AI switching typically rely on direct-detect links (e.g., DR-class PAM4), linewidth and phase noise materially affect both functional and parametric outcomes. Narrower, stable linewidths reduce measurement error when characterizing ring resonators, AWGs, and edge-coupled structures whose responses are frequency-dependent; broader or drifting linewidths inflate apparent insertion loss or passband ripple and confound extinction-ratio measurements.

Source linewidth and design also influence RIN and low-frequency noise. In the CPO model—where every lane is illuminated by the same external source tree—any excess noise or wander is injected into every optical engine, biasing BER, eye opening, and sensitivity measurements. Because one module can feed dozens of lanes through splitters and taps, vendors emphasise narrow-linewidth DFB arrays at high per-channel power to preserve SNR after splitting.

In a traditional pluggable optic, the intended CW light source has already been integrated, and therefore, functional testing of the integrated part is very clear. This is never the case for CPO – not in deployment and certainly not during tests. This new pressure on CW test light sources comes from the disaggregated design – the CPO architecture light is always coming from elsewhere.

From a PIC perspective, CPO chiplets are deeply complex, and testing them parametrically is increasingly expensive. The solution is to move silicon tests that are more functional in nature, and this, in turn, changes the types of source properties we are looking for in a typical PIC environment.



➤External Laser Small Form Factor Pluggable (ELSFP) defined by the OIF-ELSFP-02.0

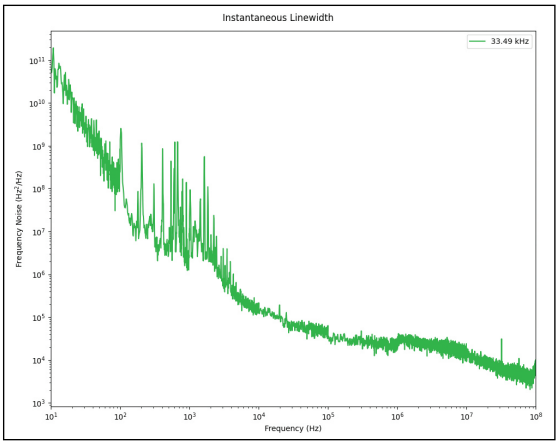
Types of optical sources for photonic testing

CPO and silicon-photonics test environments rely on a range of optical sources. Understanding differences between ASE, SLED, TLS, and DFB lasers can help engineers choose the right tool for alignment, spectral analysis, functional testing, and parametric characterization. Table 1 provides a simple definition and comparison.

Alignment dominates early PIC tests, and often production throughput is driven by pairing basic sources with fast power meters and low-latency alignment stages. Most PIC's have an inherent polarisation dependence. The ELSFP definition works to simplify the situation by providing polarisation-maintaining (PM) fibre interfaces. While PM fibres can simplify testing, they are not a cure-all and come with their own complexity. Polarisation alignment drift can masquerade as coupling variation. There are two paths to manage. One is to use a source which is naturally fully depolarised and ignore the initial polarisation challenge, or two add polarisation management with polarisation maintaining fibre or controllers. In many cases, using a depolarised source will simplify and improve alignment; it cannot be used for additional functional testing.

Scaling up channel counts at the chip

CPO for AI fabrics implies many lanes per device (for example, DR8 per port scaled across high-radix systems). Optical switches route dozens of PIC ports to shared meters, TLS, and attenuators



➤ Example frequency noise spectrum for a narrow band DFB laser at 1311nm

➤ Table 1: Simple comparison of key source types used in PIC testing of CPO switches

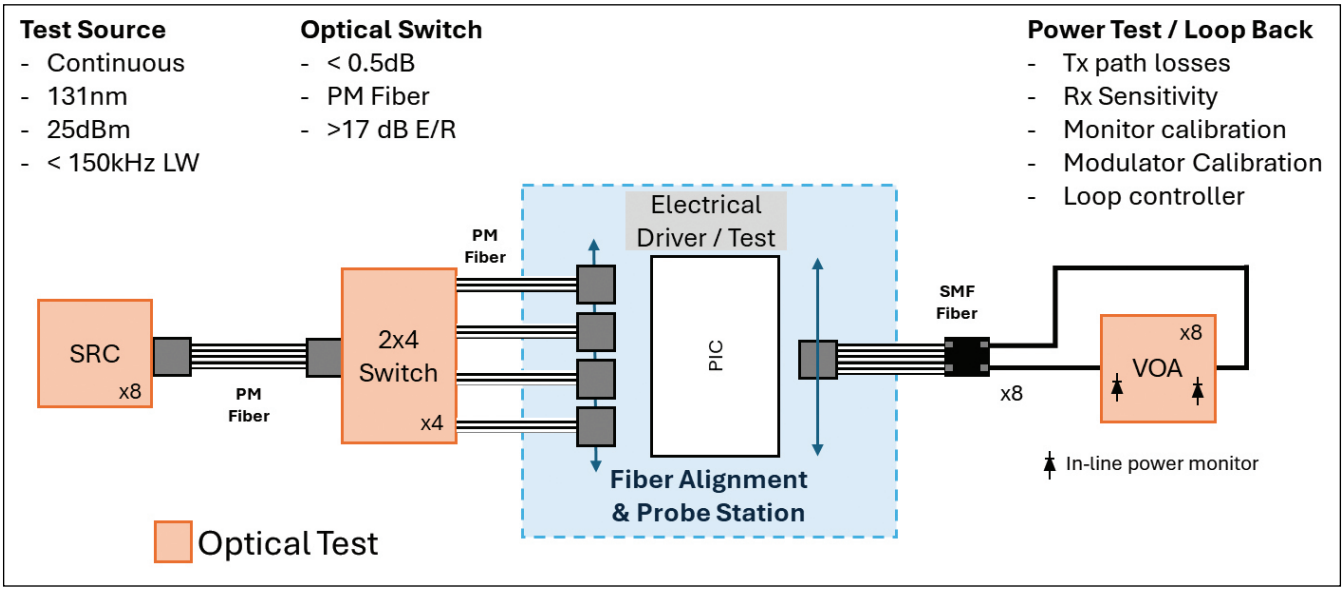
Source Type	Relative Power	Spectrum	Linewidth	Polarization	Parametric Test / Alignment	Functional Test
S-LED (Super Luminescent Diode)	Medium	**Broadband** (10–50 nm)	**N/A** (Incoherent Broadband Emitter)	**Partially polarized**	**Yes (with Power Meter)**	**No**
ASE Source (Amplified Spontaneous Emission)	Medium / High	**Very broad** (10–40+ nm)	**N/A** (Incoherent Broadband Emitter)	**Unpolarized**	**Yes (with Power Meter or Spectrum Analyzer)**	**No**
Basic DFB Laser (Distributed Feedback Laser)	Medium	**Narrowband** (Fixed Wavelength +/- 5nm)	**Very narrow linewidth** (MHz class)	**Stable polarization** (often PM coupled for test)	**Yes (with Power Meter)**	**No**
Performance DFB Laser	High	**Narrowband** (Fixed Wavelength) (Temperature tuning +/-1nm)	**Very narrow linewidth** (kHz class)	**Stable polarization** (often PM coupled for test)	**Yes (with Power Meter)**	**ELSFP Emulator**
TLS (Tuneable Laser)	Medium /High	**Narrowband** (Wavelength Tuneable > 50nm)	**Very narrow linewidth** (MHz class)	**Stable polarization** (often PM coupled for test)	**Yes (with Power Meter)**	**ELSFP Emulator**

and offer a path to high density high throughput test architectures. Scripted sequencing sweeps wavelength across N ports, applies attenuation, log power and/or BER, and coordinates scope triggers. Synchronised optical buffer capture around events (wavelength steps, polarisation changes) provides the transient context needed for root-cause analysis.

CPO will put a strong premium on measurements in parallel and creating test sequences where maxims equipment utilisation will alternate paths are aligned.

Synchronising optical events (wavelength steps, VOA changes) with electrical captures enables isolation of transient-induced penalties and confirms control loop stability. Despite best efforts, source differences can sway BER and eye metrics, so inline optical monitoring helps separate PIC issues from source artefacts. Once initial validation is complete, additional checkpoints include link bring-up at the target baud rate, BER under FEC, lane margining, power-budget validation, and control/telemetry checks.

Across R&D and manufacturing, solutions converge on similar building blocks: sources (CW DFBs and TLS with precise power and wavelength control and narrow linewidth), conditioning (VOAs, polarisation controllers/scramblers), routing (optical switches), sensing (high-accuracy power meters and taps), and control/automation (deterministic sequencing, triggers, data capture). A modular platform such



➤ Leveraging a modular platform, 8 or 16 high power DFB lasers can be fed through PM fibre switching to enable fibre alignment and testing of the CPO PIC. High density power meter and VOA arrays are used to execute functional testing and tuning of the modulators

as MAP-300 assembles these elements within one chassis and API, enabling repeatable wavelength sweeps synchronised with power logging, closed-loop alignment using fast meters and VOAs, scalable multiplexing via switch modules, and lifecycle consistency from NPI to volume manufacturing. This orchestration complements best-of-breed scopes, BERTs, and OSAs.

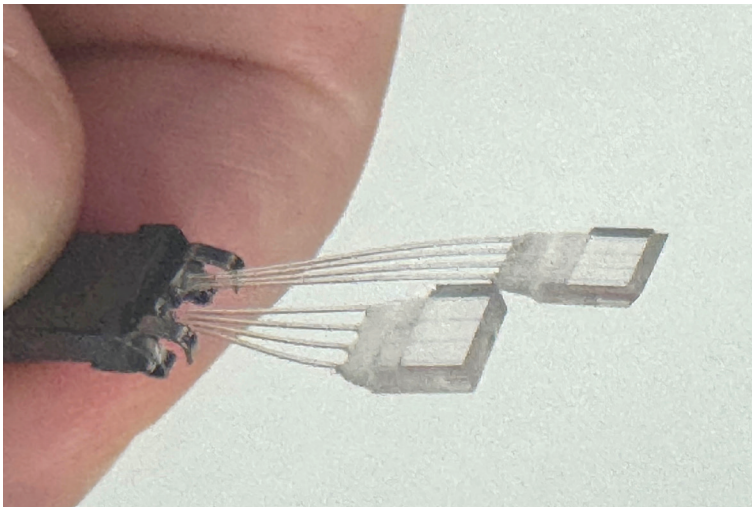
Complimentary tools

The sheer volume of the number of connection points, coupled with powers potentially greater than 24dBm, forces intense focus on interface cleanliness – both at the PIC and at the test rack. Contamination on fibre-array connectors, ribbons, and lensed facets remains a top yield killer. Bake inspection checkpoints into the automated flow (pre- and post-key steps), standardize cleaning recipes (dry/wet, force control), and log images and outcomes to correlate with parametric anomalies. This alone can collapse retest time and recover yield.

Lensed outputs (on-chip or attached micro-lenses) improve coupling but shrink depth of focus and raise angular sensitivity. Contamination near the apex degrades coupling and back-reflection; the apparent 'best power' point can shift with SOP or source linewidth, so stabilized polarization and clean, narrow-linewidth sources are essential during seek and verify.

Summary

Early planning of the light-source strategy for CPO-based PIC testing is critical. The following recommendations can save time and improve yield. If lasers are external (ELSFP), emulate their multi-channel power, linewidth, and stability characteristics on the test bench. Instrument for scale—expect rising lane counts; prioritise switching, multiport metrology and tight synchronisation. Automate tunability and alignment; deterministic sequencing and fast feedback loops save the most time in production. Bake inspection into the test and treat it as a yield lever. Correlate lab-to-line using a modular platform (e.g., MAP-300) to keep sources, VOAs, switches, and meters on a common control plane and calibration chain for easier change control and faster yield ramp.



➤ Inspection of fibre arrays (FAU) is critical to ensuring optical coupling interfaces are clean and do not impact PIC testing results

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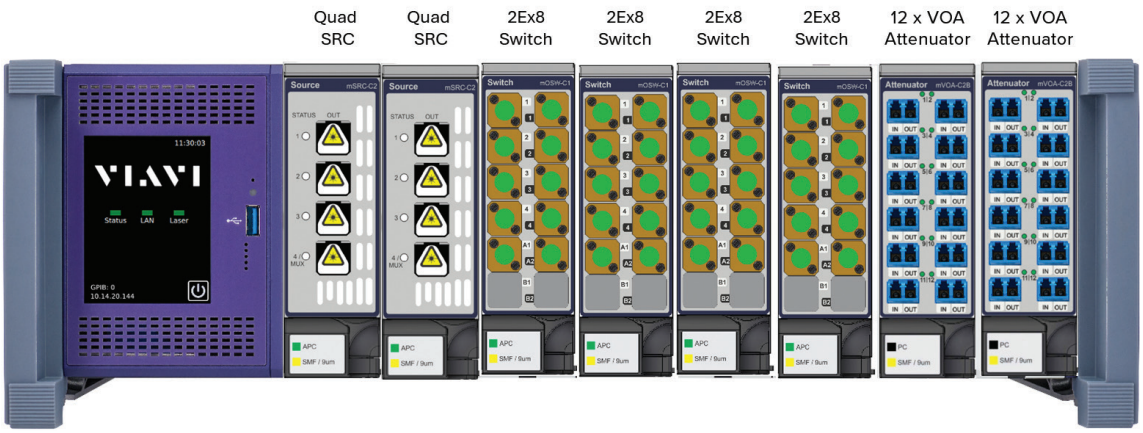
➤ [1] OIF, External Laser Small Form-Factor Pluggable (ELSFP) Implementation Agreement, OIF-ELSFP-02.0.



➤ Example layout of the PIC test station with high power reference sources along with switch and fast VOA / OPM modules with high-speed triggering

POET explains hybrid integration, optical engines and chiplet-based PIC development in the AI era

As AI workloads strain copper interconnects, hybrid integration, optical engines, and chiplet-based PICs are emerging as scalable, energy-efficient solutions to power next-generation data centre and hyperscale infrastructure

BY DR SURESH VENKATESAN, EXECUTIVE CHAIRMAN AND CEO, POET TECHNOLOGIES

AS ARTIFICIAL intelligence systems advance toward ever more demanding workloads and sprawling data centre fabrics, the semiconductor industry faces a looming bottleneck in data transfer. Traditional copper interconnects, long in the backbone of server, switch, and GPU communication, are nearing their physical limits for speed, power, and scalability. To sustain the next wave of AI models and hyperscale networking, the industry is pivoting toward photonics.

The ability of light-based signaling to carry vast amounts of data at high speed with far lower energy than electron-based copper traces is pivotal as the AI era accelerates. At the heart of the transformation to increased photonics use are innovative approaches like hybrid integration, optical engines, and chiplet-based photonic integrated circuits (PICs).

How CPO can solve the data transfer bottleneck in the AI revolution

For decades, scaling semiconductor performance relied on Moore's law — shrinking transistors to pack more gates into a silicon die every two years or less. But as we push into an era of AI accelerators, GPUs, and massive model parallelism, a new constraint has emerged: interconnect bottlenecks. This means that even when individual processing units are powerful, the speed, energy cost, and latency of moving data between them (or memory and other systems) can throttle overall performance.

AI workloads, especially large language models (LLMs) and multimodal systems, are becoming heavier as they are tasked with moving massive amounts of data. Training and inference require constant exchange of information across processors, memory modules, accelerators, and networking stacks. The result? Traditional interconnects begin to falter.

"Though conductive copper interconnect is well understood, it presents fundamental limitations when transmitting data signals at the high frequencies required for modern XPUs in the age of AI," states PhotonDelta. "In-package and chip-to-chip optical interconnect not only promise to support the computational bandwidth that AI data centres demand, but they can also reduce latency, heat generation, power consumption, and signal degradation."

Industry voices have emphasized that data transfer bandwidth and energy efficiency are now the key system bottlenecks in AI infrastructure, outpacing even compute core

performance. As a result, momentum has been built toward co-packaged optics.

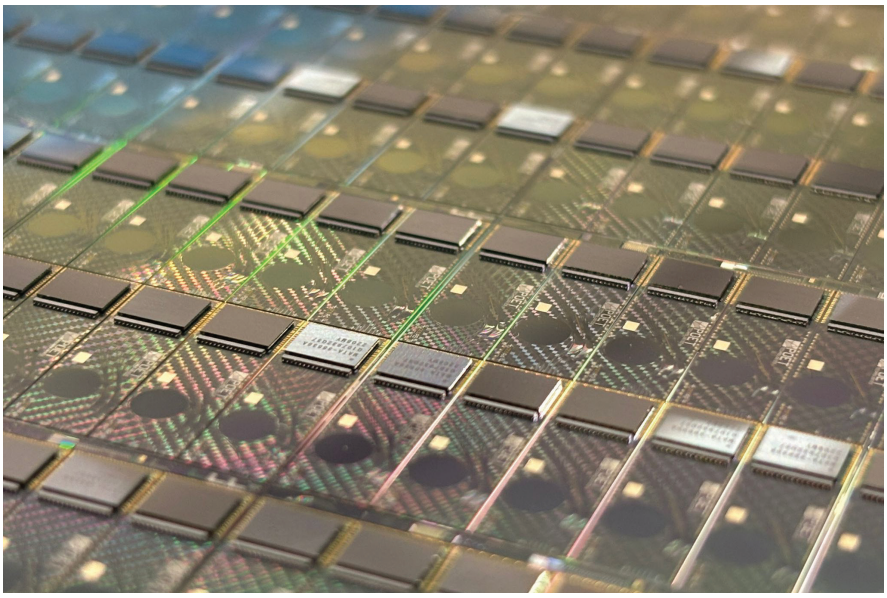
"As hyperscale computing grows and data centre infrastructure evolves, switch designs are shifting toward co-packaged optics (CPO), which embed optical chiplets in the same package as the ASICs (application-specific integrated circuit). CPO approach shortens interconnect lengths, thereby reducing power consumption, while simultaneously enabling a more compact footprint and higher bandwidth density," writes Pingfan Wu, Senior Technical Director at Futurewei Technologies, in ComSoc Technology News.

Optical links and photonic techniques offer orders of magnitude higher data densities and dramatically lower energy per bit than traditional solutions. For example, PICs are gaining traction because of their promise to replace problematic electrical interconnects with optical links, delivering high bandwidth with low latency and power. But traditional silicon photonic devices require complex fabrication and expensive packaging, which has limited the adoption of PICs. And while optical signaling is inherently superior at scale, getting photonics integrated with existing electronic workflows — at volume and low cost — has been one of the industry's largest hurdles this decade.

Cost and performance advantages of hybrid integration

Now, hybrid integration has matured. It represents a structural shift in how photonic systems are built and scaled. At its core, hybrid integration brings together components made from different materials into a single package. This design typically enables automated wafer-scale assembly (rather than manual alignment of discrete parts), and chiplet-level packaging where photonics and electronics operate in concert in one high-speed subsystem.

Hybrid integration allows for flexibility in design and manufacturing. Large monolithic dies suffer disproportionately from defects, where a single flaw can render an entire chip unusable. But chiplet-based hybrid integration mitigates that risk by breaking functionality into smaller, known-good



dies that can be tested independently before assembly. According to a 2024 McKinsey analysis on advanced packaging, chiplet-based architectures can improve effective yield by more than 30% while simultaneously shortening development cycles. The yield advantage directly translates into lower cost per bit— a critical metric for AI networking infrastructure.

Hybrid integration also reduces cost by simplifying packaging and assembly. Conventional photonic modules often require active alignment, manual fibre attachment, and labour-intensive testing. Wafer-scale hybrid integration enables passive alignment and parallel assembly, dramatically reducing manufacturing time and capital expenditure.

On the performance side, hybrid integration shortens electrical interconnect lengths and enables tighter coupling between photonics and electronics. By placing drivers, modulators, and detectors within the same package, signal integrity improves while power consumption drops. The result is lower energy per bit, higher bandwidth density, and reduced latency—key requirements for AI training clusters where microseconds of delay can cascade into significant efficiency losses at scale.

With added efficiency, hybrid integration also accelerates time-to-market, which is essential in an AI landscape where network speeds are advancing from 400G to 800G to 1.6T in rapid succession. As LightCounting has observed, "The economics of optical networking increasingly favor platforms that can scale bandwidth without scaling complexity."

For hyperscalers and AI system architects under pressure to deploy ever-higher bandwidth at sustainable cost and power levels; hybrid integration is not merely an incremental improvement—it is a foundational enabler of next-generation AI infrastructure.

Why chiplets have risen to the forefront of photonics design

Getting to this point in the evolution of hybrid integration has not been simple. Breakthroughs in photonic integration have taken place because increased research and development has led to an understanding of why light performs so well at higher speeds. The challenge recently has been to harness its abilities. Photons travel with no resistive loss (a difference from electrons, which do have resistive loss when moving through copper); optical waveguides and fibers enable bandwidth densities unachievable with metal traces; and optical signaling reduces heat and cross-talk.

As the industry unlocks more potential from hybrid integration, chiplet design has emerged as a leading option to solve the data-transfer bottleneck. Increasingly employed to mix best-of-breed components in photonics, chiplets enable yield improvements because they have smaller dies than large monolithic chips and more flexibility. Chiplets can be configured in various combinations for targeted

applications, and they can also use a range of materials.

The deployment of optical engines, which are a commercially viable form of chiplets, has been one of the first moves by the industry to usher hybrid-integrated subsystems into the marketplace. Optical engines generally combine electrical drivers, high-speed modulators, lasers, photodetectors, waveguides, and other components. These engines act as the bridge between electrical processing and optical signaling, converting high-speed electronic data into light and back.

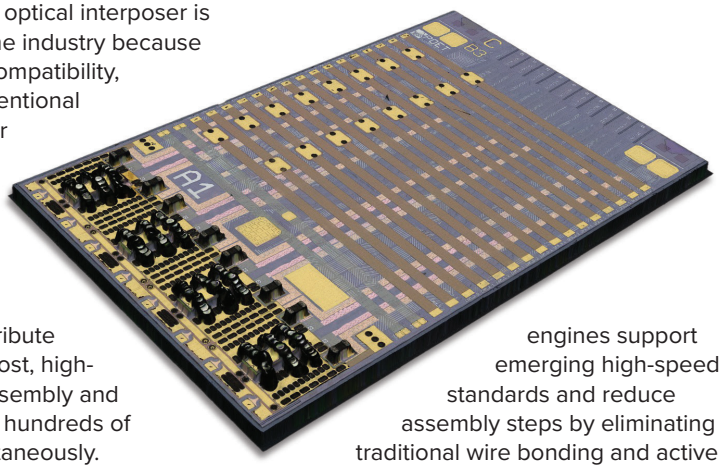
Optical engines deliver advantages including:

- High data rates — optical channels can scale beyond terabits per second per module.
- Lower energy per bit — light propagation in waveguides incurs minimal loss and heat to deliver this crucial metric for AI hardware manufacturers.
- Reduced latency — light travels faster with fewer intermediate conversions.
- Scalability — optical links extend over meters or kilometers with low signal degradation.

These capabilities make optical engines ideal for AI cluster and ultra-fast networking, where massive amounts of data move continuously and unpredictably.

Optical interposer technology is a key solution for the AI era

Among the leading technologies used in the design and assembly of optical engines is the optical interposer. An optical interposer is attractive to the industry because of its CMOS compatibility, allowing conventional semiconductor fabrication processes to be used in building photonic systems at scale. This attribute enables low-cost, high-throughput assembly and testing across hundreds of devices simultaneously.

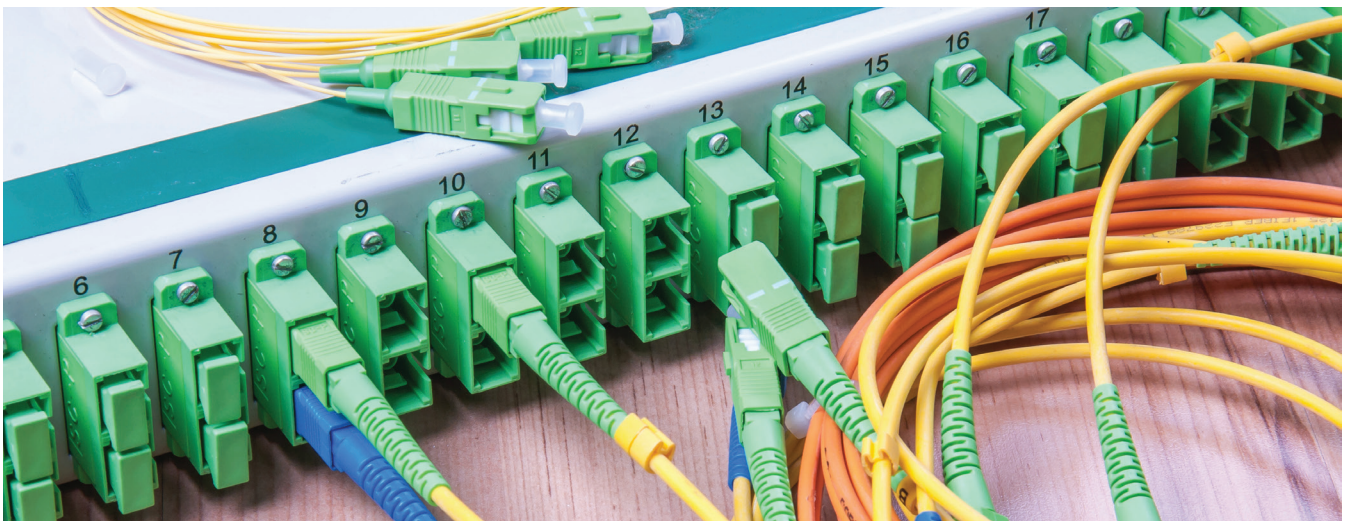


POET Technologies' Optical Interposer™ was created to be a platform technology that can power the next generation of compute devices. Using a "semiconductorization of photonics" approach that combines electronics and photonics at a wafer scale, POET's optical interposer dramatically reduces assembly complexity and cost. By embedding low-loss optical waveguides into a silicon interposer with integrated electrical traces, the platform enables seamless integration of diverse components — lasers, detectors, modulators, and driver electronics — into fully realized optical engines.

In 2025, POET proved the commercial credibility of the platform as its partnerships with a number of industry leaders matured. Among its core products is POET Teralight™, a line of 1.6 Tbps transmit and receive optical engines that illustrate scalability to next-generation speeds and longer reaches suitable for AI systems networks and hyperscale data centers. The Teralight engines support emerging high-speed standards and reduce assembly steps by eliminating traditional wire bonding and active alignment. The Teralight engines have garnered industry recognition, winning multiple competitions, including most recently at China's Infostone (ICCSZ) Awards, where it was named Product Innovation of the Year during a ceremony on January 16, 2026.

By merging hybrid integration with chiplet-scale design, POET's approach addresses key industry pain points — cost, scalability, and performance, enabling optical interconnect architectures ready for the AI era.

Together, hybrid integration, optical engines, and chiplet-based PICs deliver a reliable path forward for photonic interconnects that sidestep the power-heavy limitations of copper — enabling AI data applications to grow without being choked by electrical bottlenecks. How to effectively power the AI revolution has been a conundrum for the industry in recent years, but viable solutions have appeared and, bit by bit, are becoming the foundation of exciting new system designs and light-based interconnect solutions.



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What it would take: The rise of barium titanate

As a photonic material, lithium niobate is "old reliable." But as the photonics landscape evolves, can barium titanate become a challenger? What would it take for this newcomer to equal, or even surpass, lithium niobate?

BY ALEX DEMKOV, LA LUCE CRISTALLINA

Challenges of integrated silicon photonics

IN THE last forty years [1], integrated Si photonics (SiPh) has reached the level of "very large scale of integration" with approximately ten thousand elements per photonic integrated circuit (PIC) [2]. SiPh's rise was fueled by explosive speed and bandwidth demands in optical communication networks across short (datacom) and long (telecom) distances. The adoption of 400G and 800G transceivers is common across data centers, telecommunication and enterprise networks. More recently, photonic AI poses unprecedented data rate and optical network density requirements [3].

These developments spur an urgent need for a compact, fast and energy-efficient coherent transceiver. Integrated SiPh can no longer rely on Si alone. Other materials must be considered to satisfy the insatiable market appetite for bandwidth and speed while significantly reducing power consumption. Another aspect, particularly for AI applications, is the co-packaging of optical and electronic devices on the same die. This has implications for optimal wafer size choice and the requirement that all materials are compatible with stringent Si fabrication facility protocols. There are three groups of materials that can realistically challenge silicon dominance over the active integrated photonic devices: III-V semiconductors, electro-optic polymers and ferroelectrics. Before discussing these, let's explore what makes a coherent transceiver special and the optical modulation schemes needed for very high data rates.

Data modulation

Non-coherent transceivers typically use intensity-modulated direct detection (IM-DD) technology; they are simple and work well with single-mode fiber. They were perfect for applications when transmission distance wasn't too long, and the data rate wasn't too high.

However, when the distance measures hundreds or even thousands of kilometers (long fiber links) or the data rate becomes very high (high-speed networks and AI), a more sophisticated modulation format (typically a combination of phase shift keying (PSK) and amplitude modulation (AM)) is needed. This scheme usually requires a reference signal and, therefore, a coherent transceiver and phase modulation.

In optical systems, techniques like quadrature amplitude modulation (QAM) and QPSK enhance data transmission rates and spectral efficiency. These methods enable the encoding of data into the phase of the optical signal, facilitating high-speed and high-capacity communication systems.

Hardware and processing needs

To make use of electro-optic (EO) modulation, we need an EO material, like a material exhibiting a linear electro-optic effect (Pockels effect) to change refractive index with an electric field. We can use materials such as EO

polymers, Lithium Niobate ($LiNbO_3$), or Barium Titanate ($BaTiO_3$).

We also need integrated optical waveguides to guide light, and metal electrodes patterned around them to apply voltage. These can be fabricated in the EO material itself (monolithic approach) or in an adjacent Si or SiN layer (hybrid approach). This requires fabrication facilities and processes that can handle all the materials involved.

Finally, we need a phase shifter or an IQ Modulator. A Mach-Zehnder Interferometer (MZI) that can control phase and amplitude independently for in-phase (I) and quadrature (Q) is an option.

Operational MZI requirements are as follows: to reduce power consumption, low drive voltage is required. To support multi-gigabit data rates (e.g., 320+ Gbps), we need high bandwidth. For signal integrity and low distortion, low optical loss and chirp are a must. For integration and manufacturing scalability, a compact footprint is desirable.

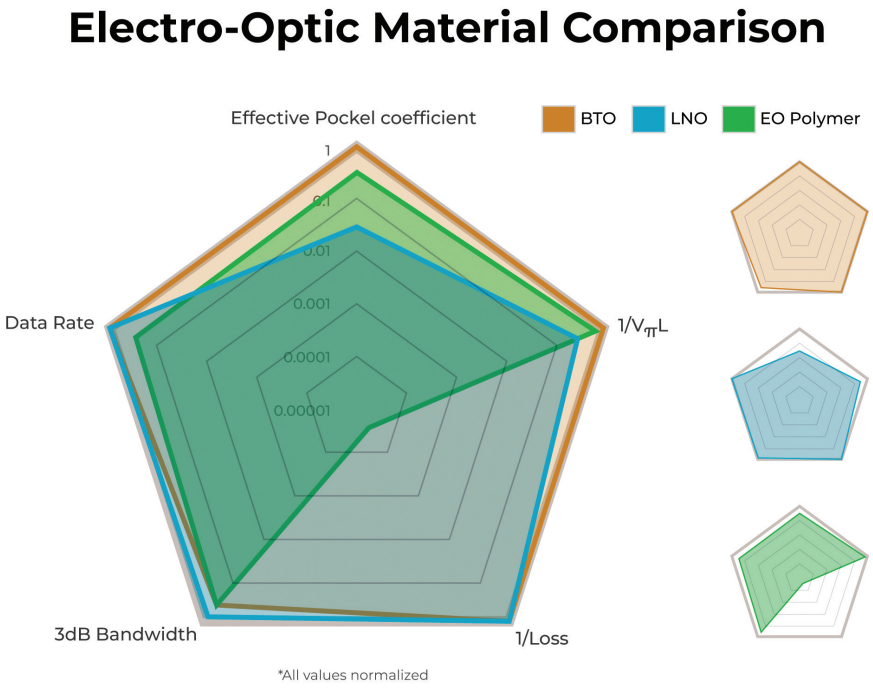
From the system point-of-view, we need a high-speed driver to amplify electrical signals to drive the electrodes. For modulation (QPSK, QAM) and error correction, a digital signal processing unit (DSP) is needed. Ideally, control electronics should be included in the package calling for co-packaged optics or CPO, which will require advanced in-line processes like lithography and etching. Because the lithium oxide component of lithium niobate is relatively volatile, and lithium is a contaminant in Si fabrication, it is not practical to use lithium niobate in applications requiring CPO. There is, hence, a bifurcation from the integration and fabrication point-of-view, resulting in a binary platform choice for on-chip integration between either SiPh or Thin-Film Lithium Niobate (TFLN). Fortunately, it doesn't have to be.

Why $BaTiO_3$?

Over the past decade, Si-integrated single crystal thin film $BaTiO_3$ (BTO) has emerged as a promising material platform for a new generation of electro-optic devices in SiPh. The key attributes of BTO technology are a very low V_{π}·L, high bandwidth and linear frequency response, low insertion loss, low power operation and high-speed data transfer. These, combined with novel integration concepts, open exciting applications in high-speed communication, optical computing (quantum and neuromorphic) and sensing/ranging [4].

BTO is a ferroelectric with similarities to $LiNbO_3$ (LN). Modulation is achieved using the Pockels effect, and a typical device is based on a wave guide phase shifter. However, unlike LN, BTO is a soft ferroelectric with a relatively low Curie temperature, high dielectric constant and giant Pockels effect; the r_{42} component of the Pockels tensor is 1,300 pm/V and is one of the largest known. It's a dielectric material from the near ultraviolet to the mid-infrared part of the spectrum with low optical losses and relatively high refractive index (n_o=2.304; n_e=2.267 at 1550 nm). These properties enable fabrication of extremely small (~100 µm), low loss (0.14 dB/cm), fast (~ps) and broadband (>70 GHz) modulators and high Q ($1.4x10^6$) resonators. The material also maintains strong electro-optic response to cryogenic temperatures, which is important for quantum computing applications.

BTO is also compatible with CMOS manufacturing. BTO can be grown on Si wafers up to 300 mm in diameter [5] and can serve as a standalone photonic platform or be used with existing silicon or SiN platforms via direct wafer-to-wafer or die-to-wafer bonding. A qualitative diagram comparing key metrics of EO ferroelectric materials is shown in Fig. 1.

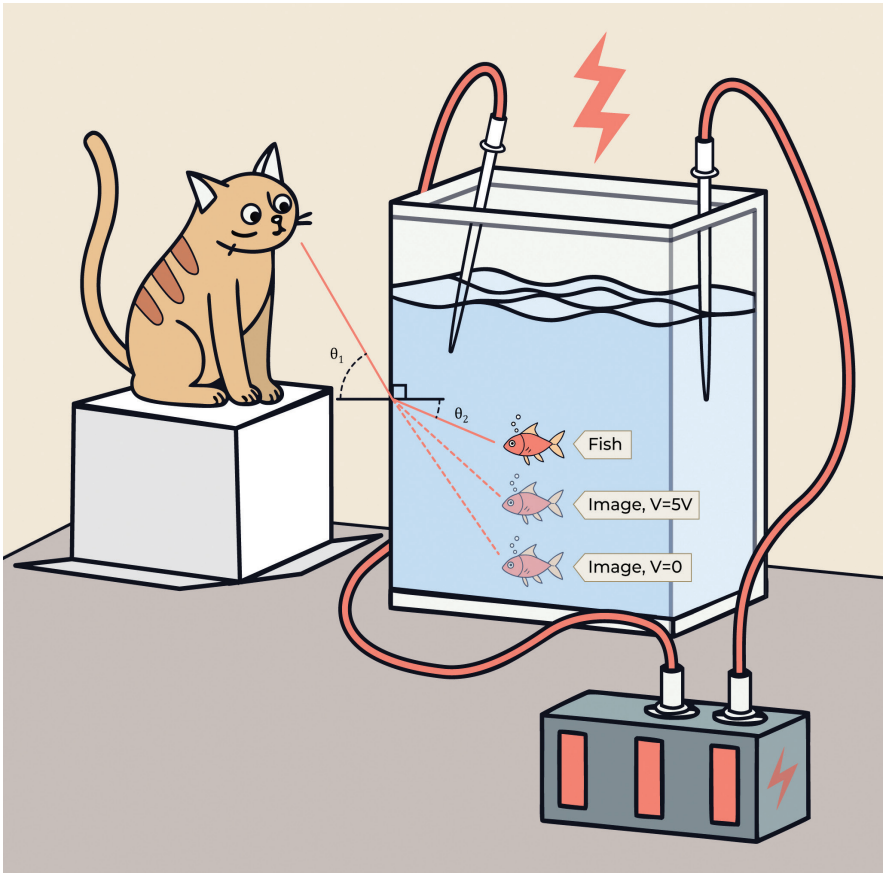


➤ Fig 1. Ferroelectric electrooptic materials performance and benchmark comparison.

State-of-the-art and current research efforts

BTO boasts one of the largest known Pockels coefficients. The Pockels coefficient relates the change in the index of refraction (ratio of the speed of light in vacuum to that inside the material) to an applied electric field as $n(E)=n_0-1/2\ r n_0^3\ E$, where n_0 is the index of refraction under zero field. Refractive index is known from the Snell's law (see Fig. 2 for a simple description of refraction and how it changes with the EO effect). It is worth noting that the integrated SiPh is only possible due to the total internal reflection in a waveguide, a condition when the refracted beam can't leave the higher refractive index medium (water in the case of the water/air interface or Si for an Si/SiO_2 waveguide).

In a ferroelectric crystal, a modulating electric field can couple directly to the electrons, to the lattice vibrations (optical phonons) or can cause a strain modulation via the converse



➤ **Fig 2.** Refraction is a familiar phenomenon caused by the change of the speed of light when crossing from one medium into another. The fish appears at a shallower location than it actually is as the beam of light bends crossing from water into air. Waveguiding is based on the total internal reflection inside the waveguide. If water were an EO material, one could have manipulated the perceived position by applying an electric field across the water tank.

piezoelectric effect (all ferroelectrics are also piezoelectrics). We illustrate the contributions to the EO or Pockels coefficient r (describing the change of the refractive index in response to an external field) in Fig. 3 following Ref. [6].

In BTO, the electronic ($\chi^{(2)}$) contribution to the r_{42} tensor component (the largest component) is insignificant, while the Raman and converse piezo effect contribute to approximately equal measure on the order of 650 pm/V each. This implies that, though the EO response will diminish at very high frequencies (above the acoustic resonances), it should still outperform LN. It also suggests that if the tetragonal phase is stabilized by suppressing the phase transition e.g., by epitaxial strain, the material should maintain a sizable EO response at low temperature when the optical phonons are "frozen out" [7].

The second term is the so-called ionic or optical phonon contribution related to the Raman effect, surviving up to THz. The last term is the converse piezoelectric effect. The strain is caused by the applied field. This contribution is present only at low modulating frequencies (<1 GHz); it can be neglected at high modulating frequencies, but it dominates at low temperatures.

Manufacturing infrastructure

By using an epitaxial buffer of $SrTiO_3$, single-crystal BTO thin films can be easily integrated on Si by direct deposition, unlike LN where crystal slicing and wafer bonding processes are necessary. A variety of deposition techniques such as chemical vapor deposition, molecular beam epitaxy (MBE), sputtering or pulsed laser deposition can support this purpose. Integration of BTO into existing Si-photonics (SiPh) foundry infrastructure requires access to large production-scale wafers. Among the deposition techniques, off-axis RF magnetron sputtering (with its stoichiometric transfer of source composition to the substrate) may be most suitable for volume production. Pulsed laser deposition tends to scale poorly for larger areas, while chemical vapor deposition relies heavily on hydrogen-containing precursors that create absorption centers for light at telecom wavelengths. MBE is generally too slow but could be ramped up if stoichiometry can be automatically controlled.

Although BTO on 300-mm wafers have already been demonstrated with 3σ thickness uniformity of <3% and a Pockels coefficient of >1000 pm/V [8], there are few commercial suppliers. Among them, start-ups such as Lumiphase in Europe (200- and 300-mm wafers) [9] and La Luce Cristallina in the US (200-mm wafers) [10] have established the infrastructure for medium-scale volume production of BTO wafers for photonic devices.

PsiQuantum also produces BTO photonic components in a 300-mm wafer scale, facilitating the construction of their photonic quantum computer [5].

Performance of state-of-the-art building blocks

BTO-based passive and active electro-optic photonic devices have demonstrated remarkable performance in terms of propagation loss and low-power operation. Micro-racetrack-resonators fabricated with monolithic BTO-on-insulator have demonstrated high intrinsic quality factors of 5×10^5 with a record-low straight (bent) waveguide loss of 0.15 dB/cm (1.5 dB/cm) [12]. Continuous improvements in high-quality material growth, patterning and etching techniques have significantly improved the performance of BTO-based modulators and waveguides.

As a result, an improved quality factor exceeding 1×10^6 with straight (bent) waveguide loss of 0.32 dB/cm (0.48 dB/cm) has been achieved [13]. Mach-Zehnder modulators (MZM), with arm length of 3.75 mm fabricated with the same material, have demonstrated $V_\pi \cdot L$ of 0.54 V·cm. Recent IBM studies report propagation loss of 0.11 dB/cm and large Kerr non-linear refractive index of 1.8×10^{-18} m^2/W in BTO ridge resonators, indicating that the PICs based on BTO may achieve state-of-the-art efficiency

beyond what has been demonstrated today [14]. Ultra-fast switching networks, one of the key components required for photonic quantum computers, is achieved by incorporating low-loss BTO phase shifters into the 300-mm photonic stack developed by PsiQuantum. Fabricated devices include a 2-mm phase shift length with propagation loss of 0.55 dB/cm and FOM V_{π}·L of 0.62 V·cm in a 2mm×2mm footprint enabling large high-speed switching networks [5].

Current wafer-level integration

Until recently, most work on BTO-based modulators focused on hybrid technology where the waveguide was fabricated in Si or SiN deposited on, or bonded to, BTO [15]. Ultra-low power refractive index tuning with a power consumption of 106 nW/FSR (free spectral range) has been achieved in a hybrid BTO-SiN platform integrated on Si. Hybrid integration of BTO on SOI waveguides using a special layer transfer technique exhibited high-performance EO modulation with V_{π}·L of 1.67 V·cm, enhancing the EO properties of Si photonics [16]. The monolithic approach is gaining popularity, along with the introduction of commercial 200-mm and 300-mm BTO-on Si or SOI wafers allowing the fabrication of all PIC components on a single chip.

BTO films can be integrated on Si with both in-plane (a-oriented films) and out-of-plane (c-oriented films) ferroelectric polarization. The combination of these options creates a rich space for possible device architectures. In addition, plasmonic devices using Si-integrated BTO have also been explored. Overall, modulators look promising; the losses are moderate - on the order of 0.1 dB/cm; V_{π}·L as low as 0.23 V·cm has been demonstrated (0.014 V·cm in plasmonic devices); the bandwidth is close to 100 GHz; and data rates above 250 Gb/s have been achieved. In addition, Si-integrated BTO-based devices have shown robust cryogenic performance. Importantly, BTO is fully compatible with CMOS manufacturing with large area wafers, making it suitable for low-cost, large-volume manufacturing.

Future performance evolution and industrialization outlook

As Si-integrated BTO quality rapidly improves and processing capabilities are established at Si photonic foundries, we expect the unique properties of this material to be gradually embraced by more of the integrated silicon photonics community.

> This implies that, though the EO response will diminish at very high frequencies, it should still outperform LN

The Pockels effect allows for a pure phase modulation mechanism with low power, fast response, low insertion loss and minimal crosstalk. BTO photonic devices have already demonstrated the ability to operate at low voltage and low power consumption. Its main strength, though, is beyond stand-alone high-speed modulators.

Co-packaged optics (CPO) is an area where compatibility with CMOS processing is essential. As AI processing demands increase, CPO will be necessary to address this bandwidth, latency and power requirement. Switching from pure silicon to a material that can be made into compact modulators with high modulation efficiency at very high switching speed and low power will become necessary.

Simultaneously, material compatibility with CMOS foundries is essential. For CPO, InP-based materials, and BTO are the only practical solutions for modulators.

So, as AI spurs optical engine demand, wider industrial acceptance of BTO may follow. It is expected that silicon photonics foundries will begin developing processes for BTO on Si in the next 1-2 years and offer PDKs involving BTO soon after. It will initially be die-to-wafer bonding on existing Si or SiN architecture but will eventually add monolithic BTO processing.

The ability to make Mach-Zehnder modulators ten times shorter in BTO than those based on LN, while operating at the same voltage, makes

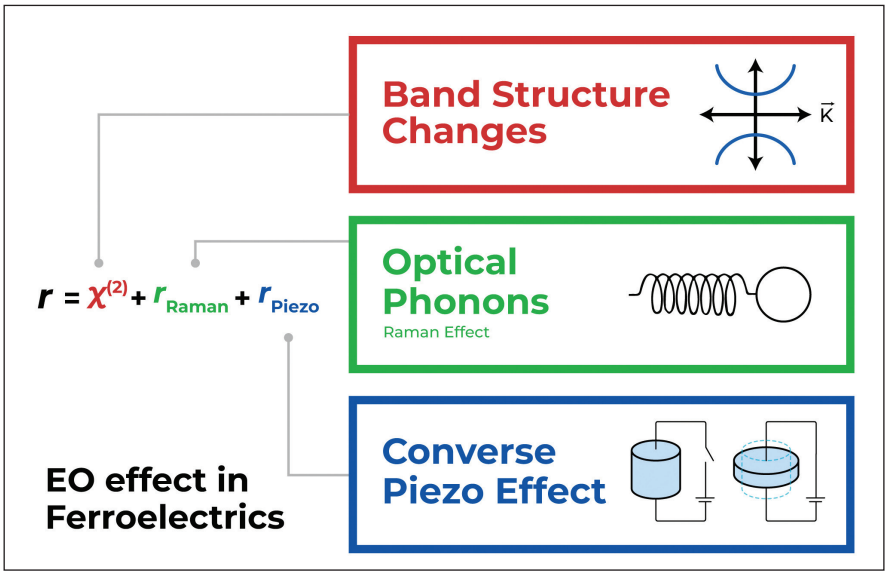


Fig 3. In a ferroelectric, there are three contributions to the effect. The first term describes the direct effect of the applied field on the polarizability (non-linear optical susceptibility), and only electrons can respond at optical probing frequencies; this is second harmonic generation ($x^{(2)}$). The second term is the so-called ionic or optical phonon contribution related to the Raman effect, surviving up to THz. The last term is the converse piezoelectric effect. The strain is caused by the applied field. This contribution is present only at low modulating frequencies (<1 GHz); it can be neglected at high modulating frequencies, but it dominates at low temperatures.

BTO a natural platform for building general purpose photonic processors (GPPPs). GPPPs consist of a mesh of waveguides, couplers and Mach-Zehnder interferometers. Similarly, BTO has a strong potential for use as reconfigurable weight elements in photonic neural networks, as demonstrated by a recent publication by Ligentec and Lumiphase using a BTO-SiN hybrid platform [16].

BTO on SiN is also the materials platform of choice implemented by PsiQuantum for their photonic quantum computing system. This demonstration shows that BTO can be made very low loss and can modulate well even at cryogenic temperatures (0.33 dB-V for $V_{\pi}L\alpha$) [5]. This proves that BTO retains its strong Pockels response at low temperature [20] due to the strong contribution of the piezoelectric effect on the electro-optic response [7].

While BTO is not yet well-known in nonlinear optics, the physics of BTO is essentially the same as LN, and it is expected that this will change with BTO wafers availability. In fact, the Kerr nonlinearity of BTO is about ten times larger than LN [14]. Thus, BTO will be the material of choice for monolithically integrated devices requiring both a large Pockels effect and a large Kerr nonlinearity.

Such devices could be used for high-precision optical clocks, parallelized coherent data communication using solitons or high-resolution dual-comb spectroscopy. BTO-based integrated electro-optic modulators have seen great advances in technological readiness in the last decade, demonstrating that they can overcome the bandwidth limitations and power consumption issues of SiPh plasma-dispersion and thermo-optic modulators.

These advances strongly position BTO SiPh technology to be the next generation of electro-optic modulators for data center and optical interconnect applications, including co-packaged optics, non-volatile optical memory, on-chip photon sources and optical-RF converters, as well as for future optical quantum and neuromorphic computing platforms.

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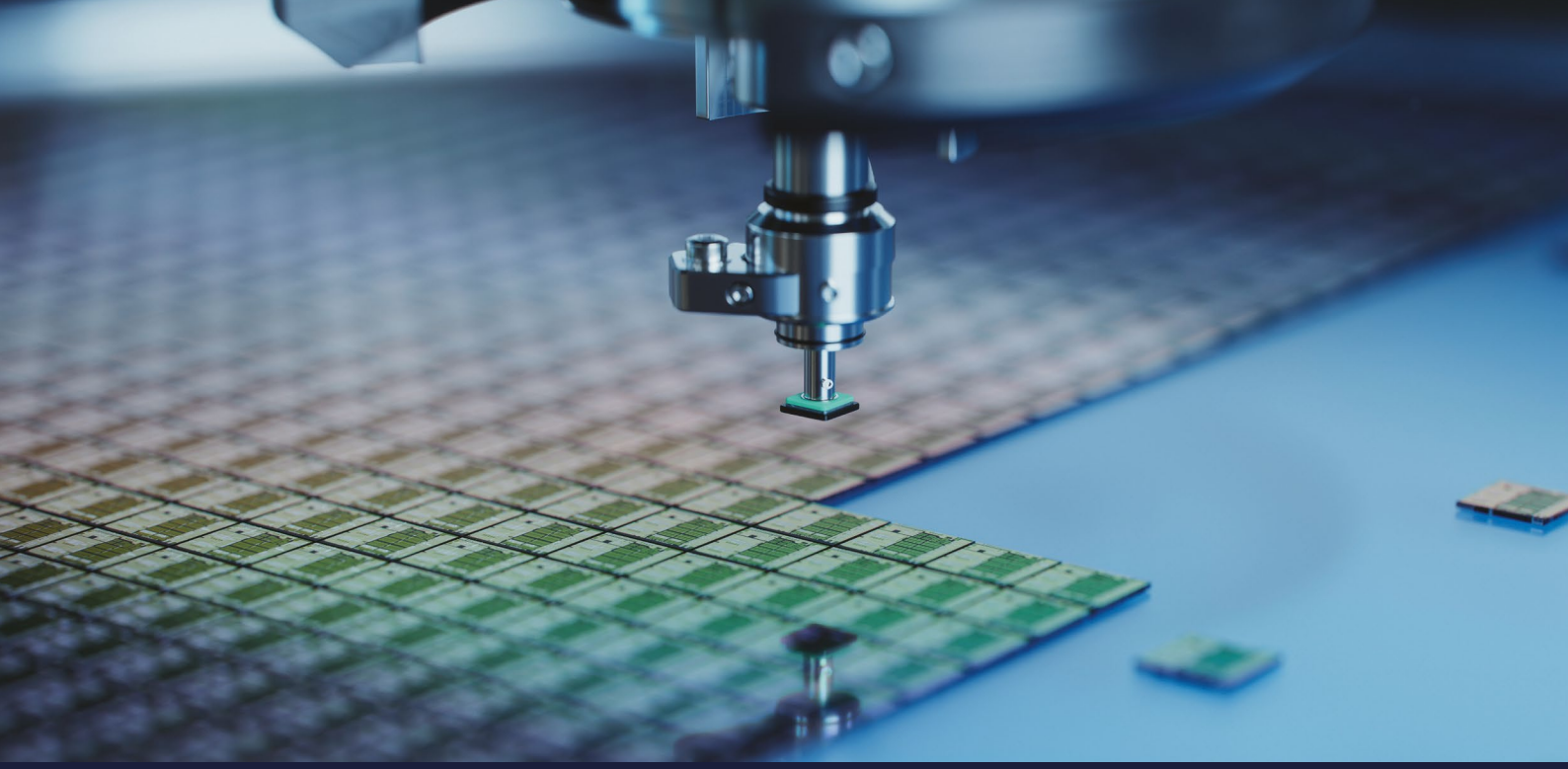

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Data communications networks face numerous challenges, including soaring AI-driven demands, high energy consumption, and the possibility of future quantum technologies breaking current encryption methods. How can PICs help to solve these issues and underpin the high-speed, energy-efficient, quantum-secure networks of the future?

Emerging applications: photonics for sensing, imaging and beyond
Integrated photonics has a wide range of potential applications. From self-driving cars to miniaturised molecular sensors and non-invasive healthcare, how are PICs making these possibilities a reality?

Future computing: PICs for photonic processing, quantum computers, and neural networks
Computing power is integral to the modern world, but established technologies have limits, and novel systems could herald more powerful devices. From fully photonic processing to photonics for neuromorphic and quantum computing, how are PICs transforming the way we process data?

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PICs enter bioreactors: what it takes to monitor cell growth in real-time

InSpek's PIC sensors enable real-time bioprocess monitoring on a scale previously unachievable. But pharmaceutical manufacturing demands completely novel engineering solutions in photonic integration

BY IVAN-LAZAR BUNDALO, CTO INSPEK

EVERY DAY at pharmaceutical facilities worldwide, a scientist samples a 1-litre glass bioreactor containing brownish liquid. Inside: valuable microorganisms or cells and their entire microbiome. The sample goes to an analytical lab. Then comes the wait: 4 to 24 hours for results.

Meanwhile, life in the original container continues. If culture conditions drift, that fact remains unknown. Contamination, stress, oxygen deprivation - all stay undetected until the run fails or a scientist acts in time. Each failed batch can cost millions of euros. For vaccines and cancer treatments, failures delay patient access by months. Regulatory approval can slip by years.

The irony is stark. Modern medicine can fend off pandemics and fight many cancers. Yet the factories making these drugs operate with primitive tools, unable to see inside bioreactors in real time – a remarkable feat in itself. Think of it like this: running a bioprocess is like driving a car through a city but seeing your speed and position only every 10 seconds, with the newest data already 10 seconds old.

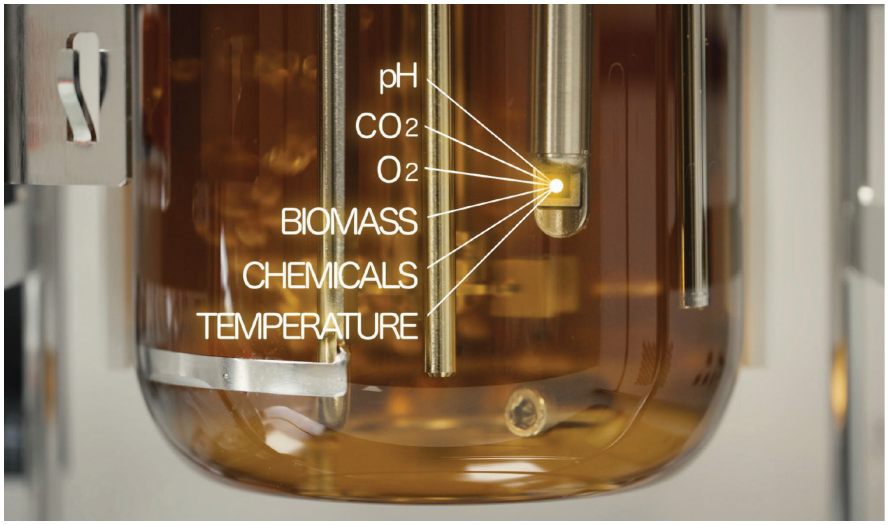
If this problem gets solved, the impact extends beyond factory floors. Faster process optimisation could shorten drug development timelines by months. Higher yields would reduce manufacturing costs. More immediately, reducing batch failures means fewer drug shortages, a chronic problem in biopharmaceuticals where supply barely meets demand.

InSpek, a Parisian startup, is miniaturising optical spectroscopic methods onto a photonic chip. Real-time multiparameter sensing at this scale changes bioprocessing economics. These are multibillion-euro industries where even small optimisations are worth millions. The challenge is that pharmaceutical manufacturing demands solving problems telecommunications photonics never faced.

A patent for seeing the invisible

InSpek was founded by Jérôme Michon, who brought the technology from his MIT PhD back to Paris. The company has 14 full-time staff, including 6 PhDs specialised in optics, biotech and AI. Unusually for a French startup, it has more foreigners than French people. The company raised €3.5m in seed funding two years ago and is preparing for a Series A round this year. It has backing from the European Union via the EIC Accelerator, the world's biggest and most prestigious startup grant.

Why is InSpek first in this domain? Sensing weak optical signals on a chip generates lots of background noise. InSpek started with a patent to clear that noise, becoming the first company able to detect these faint scattering signals in a photonic integrated circuit, in possibly the most complicated spectroscopic method called Raman. Incumbents in the bulk optics sensor business are usually unaware of integrated photonics. Though both involve optics, integrated photonics operates on very different physics, not easily translatable from bench-scale instruments to chips.



➤ Monitoring bioprocesses requires many sensors on a small probe - something only integrated photonics enables.

Driving blind through the bioprocess

The problem InSpek is tackling runs deep. Two out of three biopharmaceutical processes fail during scale-up. Nine out of ten non-pharmaceutical bioprocesses fail for the same reason. Complexity increases with volume.

Current sensors are inadequate. Electrochemical sensors measure only one analyte and drift over time, giving unreliable readings. Established optical sensing methods use bulk optics, which makes them bulky and expensive. They quickly occupy scarce bioreactor ports and represent a massive cumulative cost when multiple parameters need monitoring.

There is also a contamination paradox. Each time something enters a bioprocess, failure risk increases. The biopharmaceutical industry is terrified of contamination and often prefers slow, blind processes over having multiple sensors with attendant risk.

What's needed to start with is a pen-sized probe measuring multiple analytes simultaneously through a single standard port. PICs make this possible because they are tiny and cheap at scale. They also enable something the industry increasingly wants: single-use technologies. Counterintuitively, sterilising reusable sensors multiple times has a bigger carbon footprint than sterilising disposable sensors once, and using more of them. Only PICs make single-use sensors economically viable.

Silicon nitride for a broad spectrum

Most photonic chips since 1985 were optimised for one goal: transmit data through fibre-optic cables at 1550 nanometres, cheaply and over long distances. Silicon photonics excels at that wavelength, so the industry evolved there.

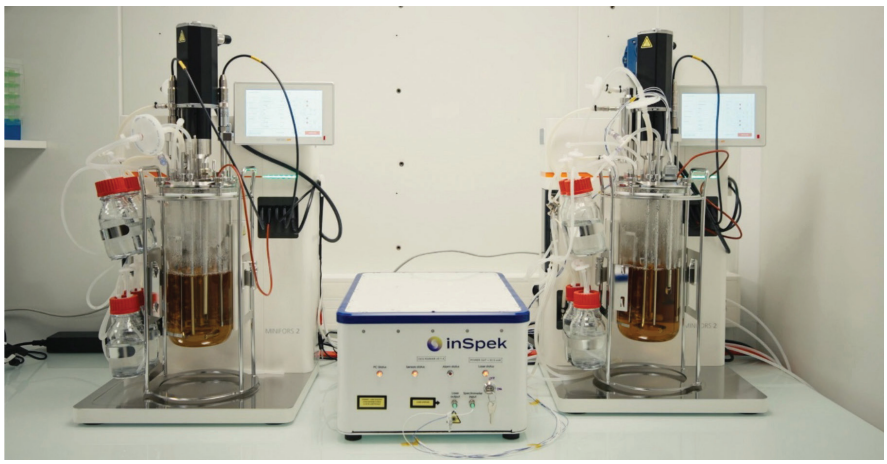
Bioprocess spectroscopy demands something different: wavelengths from 400 to 1000 nanometres. Raman scattering spans 800 to 1000nm. Fluorescence-based pH and oxygen sensing sits near 400nm. Temperature and biomass measurements fall in between. Silicon photonics fails below 800nm, as the material becomes opaque.

InSpek is based in Paris and is run by an international team of PhDs and engineers in Optics, Bioprocessing and AI.

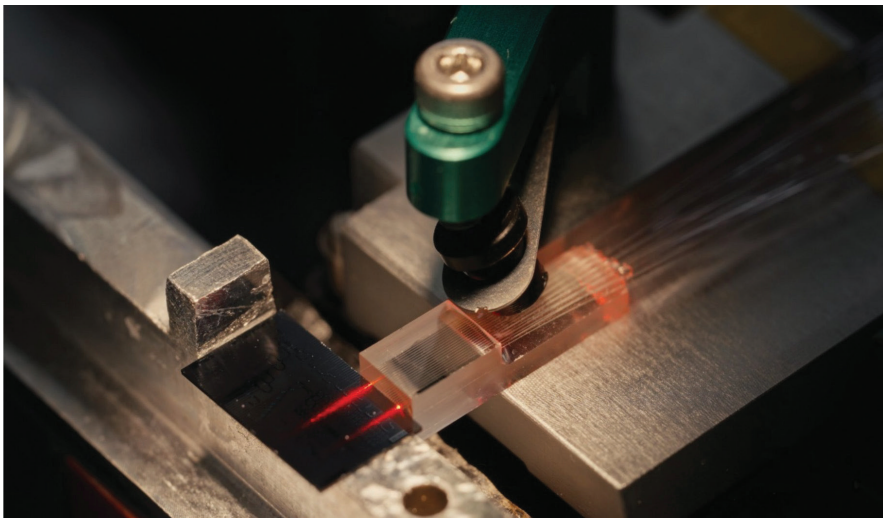
Remaining platform options include silicon nitride, aluminium oxide and lithium niobate. InSpek works with multiple, driven by mature ecosystem, favourable competitive landscape and growing potential of platforms.

The company's chips are passive. External lasers and spectrometers do the active work. This decision brings several benefits. As laser and spectrometer technology improves, InSpek's sensors improve too. Problems are decoupled. Packaging becomes simpler. The alternative, integrating multiple wavelength sources onto one active chip, would be extremely difficult.

The challenge is nonetheless impressive. Integrated photonics is difficult even in its "home territory" of telecommunications. InSpek is attempting to drag it into bioprocessing for the first time. Whether a technology optimised for data transmission cables can survive radiation, heat, chemicals and biofilm remains to be answered. Yet InSpek's bet is that the timing has never been better. The company is piggybacking on decades of telecom



InSpek's technology grows with market, as the best lasers, spectrometers and other components are decoupled from chip-based sensing technology. One Optical Control Unit (OCU - box in the centre) can monitor multiple probes in different bioreactors.



Packaging for bioprocess monitoring requires tolerating radiation, high temperature steam and harsh chemicals.

photonics development. Silicon nitride foundries matured only in the past decade. Supply chains that didn't exist 10 years ago are now established. Edge couplers, packaging techniques, design tools exist because telecom companies spent billions perfecting them. InSpek need not invent photonic integration from scratch; they must adapt it. The advantages, they claim, are worth the difficulty.

Packaging takes centre stage

A known problem in the PIC industry is that chip-making represents 40% of the challenge, packaging the other 60%. This is where the team's difficulties become uniquely severe. Some wonder whether photonics, optimised for telecom over decades, is mature enough to be bent to bioprocessing's messy demands. Standard approach: plug a fibre array onto the chip using epoxy. It works and survives industrial conditions. Companies have done this for 30 years in telecommunications. InSpek's packaging requirements are driven by three factors: broadband coupling, packaging losses and sterilisation resistance.

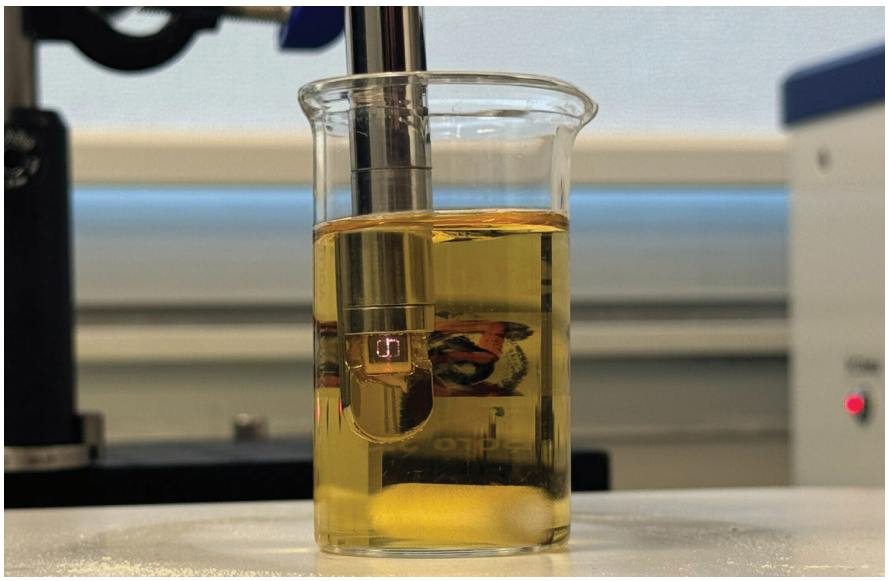
Broadband coupling creates the first headache. As InSpek's wavelength requirements span visible to near-infrared, edge couplers work best. Standard adhesives for optical packaging require low shrinkage and thermal post-cure to ensure shaded areas cure properly. Most epoxies are not transparent down to 400nm. Amongst the few that are, most suffer rapid photodegradation. The effect, often seen as yellowing and darkening, can appear even after short exposure.

The team explored alternatives such as epoxy-free packaging. Each approach involves trade-offs. Some are expensive, some fragile, some introduce new problems hard to assess. Looking back, it is difficult to see shortcuts that could have been taken when the requirements list is so exhaustive. This explains why InSpek has been accumulating knowledge through multiple packaging projects. Sterilisation survival presents a different taste of tough challenge. Before a bioreactor probe is used, it must be sterilised. Industry standard for single-use applications is gamma ray irradiation at 25 to 55 kilograys. Some multi-use facilities use autoclaving instead: 140°C steam under high pressure for 15 to 20 minutes. Chemical Clean-In-Place (CIP) sterilisation using diluted sodium hydroxide is also used.

All three methods are destructive to many materials. Radiation damages polymer molecules, creating free radicals that break chemical bonds. Material darkens, refractive index shifts, and adhesive becomes brittle. Heat creates a thermal expansion mismatch between dissimilar materials and breaks polymer bonds. Chemical sterilisation eats into materials. Repeated cycles cause microscopic cracking and delamination. Dosing variability, especially with gamma irradiation, makes validation harder still.

Biofouling adds a third dimension. Once a fully operational sensing probe sits inside a bioprocess for the typical two weeks (some run longer), biofilm forms. This combination of dead and live cells creates a slimy layer on everything, including sensors.

The layer can block sensors from seeing what happens in the bioreactor. Combinations of coatings, electrical and mechanical tools mitigate the process and extend sensor lifetime. InSpek's packaging solutions address these challenges through material selection, smart design and protective coatings.



Having multiple sensors on one chip demands visible to IR spectra handling on one PIC, and one probe.

➤ Company's value was recognised and supported by multiple investors, as well as European Union. Pictured Jerome Michon, CEO (left), and Ivan-Lazar Bundalo, CTO (right).

Rhythm of 3 tape-outs per year

Startups face a dilemma. They must iterate quickly to reach market, but in deep-tech integrated photonics entrepreneurship, each chip run costs hundreds of thousands of euros. InSpek's rhythm: 3 runs per year in 4-month cycles. Design in month one. Fabricate in months two and three. Test, package and analyse in month four, then restart.

This pace is fast compared to typical PIC startups but slow compared to established semiconductor companies doing multiple iterations at a massive scale. These four-month deadlines set the tempo for everything else. Coordination must be excellent; otherwise, the data needed for the next iteration fails to reach designers. An extremely costly mistake.

One sign of startup maturity is logistics diversification. For InSpek this came as a requirement from investors. At least one backup foundry, one backup packaging partner, one backup contract manufacturing organization for whatever work happens externally. Because packaging is so critical, InSpek works with no less than 4 different partners, in addition to their own in-house packaging abilities.

Early customers and disruption

InSpek is not launching a finished, perfect product. Instead, the company pursues early deployments in academic labs and smaller facilities - customers willing to tolerate maturing early versions in exchange for being the first to use novel technology.

Real-world data shapes the product faster than internal R&D alone. One concrete example: collaboration with URD ABI showed a 2x yield improvement with InSpek's technology in production of p-coumaric acid, an important biochemical for the cosmetics industry. Partnerships with some of the biggest companies in the biotech field signal serious interest.

The economics are compelling. The bioprocessing equipment market is massive. Production costs for InSpek's chips plus packaging rival bulk optics at low scales, coming in at a few hundred euros. At higher volumes, costs drop significantly by leveraging microelectronics-scale economics. The target: below €100 at scale.

The business model focuses on three segments: reusable sensors for multi-use facilities, single-use sensors for disposable bioreactors, and AI data modelling and optimisation services.

Incumbent sensor makers, accustomed to selling expensive bulk optics probes, face disruption. Integrated photonics operates on physics unfamiliar to traditional optics engineers, creating barriers to entry. This is an advantage, as by the time bulk optics companies recognise the potential, InSpek may have an insurmountable lead in chip-based sensing.

Regulatory hurdles exist but are manageable. The pathway is cytotoxicity-based, less stringent than medical device regulation but tough, nonetheless. The bigger challenge is industry reluctance to adopt new technologies, driven by quality requirements and high safety standards. This will not happen overnight, InSpek is in for the long term.

As for most PIC technologies, the central risk remains packaging. If costs stay high or sterilisation proves unreliable at scale, the economics could collapse. Everything else looks promising. InSpek's vision extends beyond just sensing bioprocesses. Chemistry is a massive market, but there's something even bigger out there. With unprecedented data volumes, the company wants to enable tight process control using AI. Current focus is on yeast-based fermentation. The future target: monoclonal antibodies for treating major diseases, and advanced AI helper for whatever biotechnological process imaginable.

The bioprocessing equipment market is worth billions. Optimisations are worth millions. InSpek's knowledge in adapting photonics to bioprocessing's brutal conditions - radiation, heat, chemicals, biofilm - may prove its deepest competitive advantage. Perhaps one day, bioreactor operators will monitor their drug factories with the same precision we now track the pandemics those factories help fight. The primitive tools won't stay primitive for long.

➤ InSpek's multiparameter chips enable AI-driven real-time bioprocess optimization

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With profit margins shrinking, makers of SiC devices cannot rest on their laurels. But what are the key innovations to ensure success, in terms of production processes, fab operations and new device architectures?

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A new class of photonic chip for human-safe pathogen control

The world's first solid-state photonic chip that delivers human-safe, pathogen-lethal far-UVC light to rapidly eliminate viruses, bacteria, fungi and mold spores in air, surface, and water

BY SCOTT BURROUGHS, CEO, UVIQUITY

ULTRAVIOLET light has long been recognised for its germicidal properties, yet its use has historically been constrained by safety, scalability, and system-level complexity. In recent years, far-UVC light, typically defined as wavelengths between 200 and 230 nm, has emerged as a promising solution for continuous pathogen inactivation in occupied environments. Experimental and clinical studies have shown that far-UVC can inactivate a broad spectrum of viruses, bacteria, fungi, and spores while remaining safe for human exposure within established regulatory limits.

Despite this demonstrated potential, far-UVC adoption remains limited. The challenge has not been efficacy, but rather the lack of a scalable, efficient, and manufacturable light source. Today's far-UVC systems rely almost exclusively on excimer lamps, which impose fundamental constraints on cost, lifetime, form factor, and system integration.

Uviquity is addressing these challenges by developing the first solid-state far-UVC photonic integrated circuit (PIC), delivering chip-scale generation of spectrally pure far-UVC light using established semiconductor manufacturing processes. The company's approach supports compact, efficient, and scalable light engines that can be deployed wherever pathogens exist in air, on surfaces, and in water without the operational constraints of legacy ultraviolet systems.

The germicidal power of light

Ultraviolet (UV) light spans wavelengths from approximately 100 nm to 400 nm and has been used for disinfection for more than a century. Within this range, UVC light (200–280 nm) is particularly effective because it is strongly absorbed by nucleic acids and proteins, damaging the DNA, RNA, and structural components of microorganisms and rendering them nonviable.

Traditional germicidal UVC systems typically operate near 254 nm and rely on mercury vapor lamps or, more recently, UVC LEDs. While effective against pathogens, radiation at these wavelengths penetrates living tissue, requiring strict controls to prevent eye and skin injury. As a result, conventional UVC systems must be shielded, interlocked, or used only in unoccupied spaces, limiting their utility for continuous disinfection.

Far-UVC light, generally defined as wavelengths between 200 nm and 230 nm, behaves differently.

At these shorter wavelengths, photons are strongly absorbed by the outermost layers of human skin and the superficial corneal epithelium of the eye, limiting penetration into deeper, living tissue. Microorganisms, which lack these protective barriers, remain highly susceptible. This unique interaction enables far-UVC light to inactivate pathogens in occupied environments when delivered within established exposure guidelines.

Proven safety and efficacy—with a scaling challenge

Over the past decade, a growing body of peer-reviewed research has demonstrated both the germicidal efficacy and the safety profile of far-UVC light. These efforts accelerated during the COVID-19 pandemic, as researchers and standards bodies worked to evaluate far-UVC for real-time air and surface disinfection.

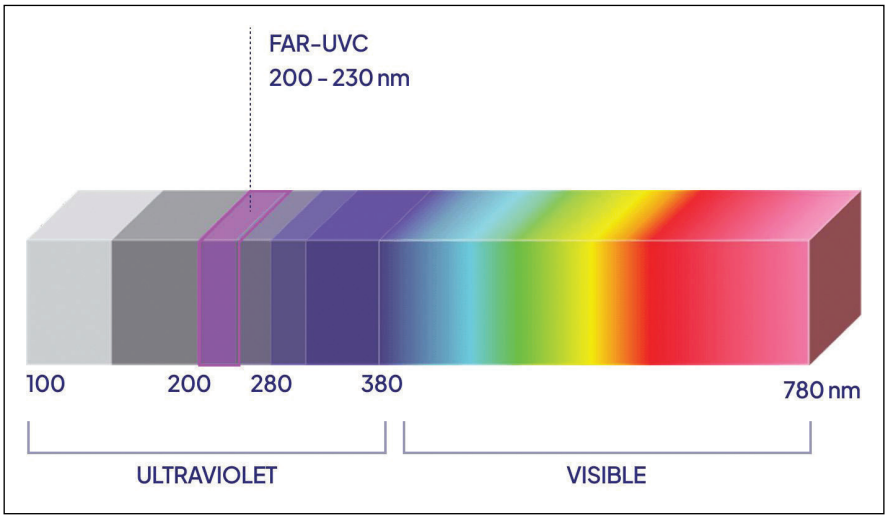
Early commercial deployments of far-UVC have relied primarily on krypton-chloride (KrCl) excimer lamps emitting near 222 nm. These gas-discharge sources in sealed quartz bulbs played an important role in validating the efficacy and safety of far-UVC in practical settings, but their physical operating principles impose significant limitations. Excimer lamps typically exhibit low wall-plug efficiency, high cost per milliwatt, limited operating lifetime, and bulky form factors. They also require optical filtering to remove unwanted wavelengths outside the human-safe band, adding complexity, and further reducing usable output. High operating voltages and fragile bulbs introduce additional barriers to broad adoption.

As a result, the use of far-UVC light for disinfection has been proven in principle—but not yet delivered in a form factor or cost structure suitable for mass deployment.

Engineering far-UVC on a single chip

Uviquity addresses this challenge by generating far-UVC light directly on a semiconductor photonic integrated circuit.

The company's platform is based on aluminum nitride (AlN), a material particularly well suited for deep- and far-UV photonics due to its wide bandgap, high damage threshold, and strong second-order nonlinear coefficient. Importantly, AlN is transparent deep into the far-UVC spectrum, enabling low-loss waveguiding at wavelengths inaccessible to many other integrated photonic materials.



Electromagnetic spectrum showing the wavelength ranges of visible, ultraviolet, and far-UVC light.

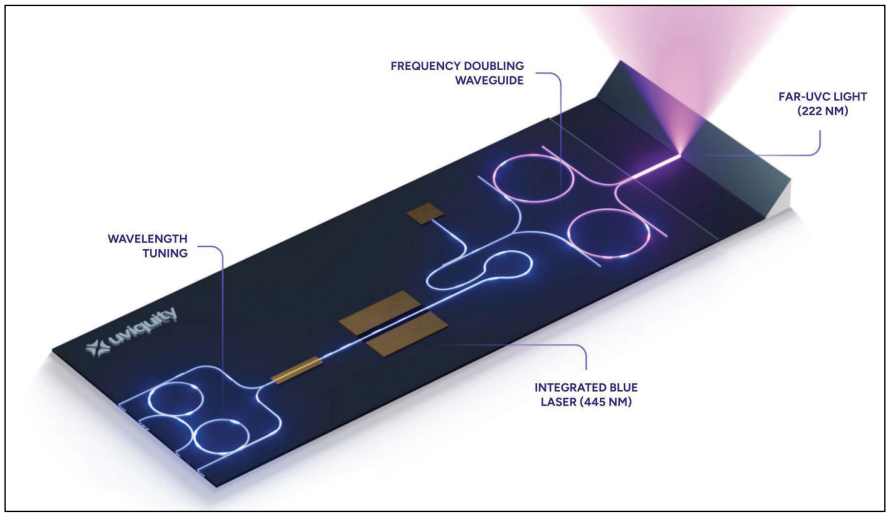
At the core of the device is an integrated blue gallium-nitride laser operating near 445 nm. Light from this laser is routed through precisely engineered AlN waveguides, where it undergoes second harmonic generation (SHG). This nonlinear optical process doubles the fundamental frequency of the input light, producing a narrow-linewidth output near 222 nm, squarely within the human-safe far-UVC band. Because frequency conversion occurs within a phase-matched waveguide, the emitted light is intrinsically narrowband, eliminating the need for external filtering, resonators or bulk nonlinear crystals. The result is efficient frequency doubling in a compact, solid-state far-UVC light engine that integrates into standard photonic packages without the bulk, high voltages, or fragile components associated with lamp-based sources.

Semiconductor manufacturing and materials platform enable scale

Uviquity's AlN PIC platform is fabricated using wafer-scale semiconductor processes. Wafer-scale fabrication enables large numbers of identical devices to be produced using standard semiconductor processes, supporting improvements in uniformity, reproducibility, and manufacturing scalability. This wafer-scale approach contrasts sharply with lamp-based technologies, where each source is fabricated and assembled individually.

Importantly, the company's platform leverages the broader III-nitride semiconductor ecosystem that underpins today's blue LED and laser industries. This provides access to mature supply chains, established fabrication infrastructure, and decades of

Uviquity's second harmonic generation (SHG) aluminum nitride (AlN) chip integrates into standard photonics packages. The chip is shown above, held by tweezers.



➤ Uviquity's technology platform enables the heterogeneous integration of a blue laser with AlN waveguides on a single semiconductor chip to generate far-UVC light using second harmonic generation.

manufacturing know-how. As a result, the technology will follow a cost and performance trajectory akin to that of LEDs, where dramatic reductions in cost and increases in efficiency were achieved through materials optimization and volume production.

Beyond cost, solid-state integration delivers additional benefits: longer operating lifetimes, lower maintenance requirements, improved reliability, and the ability to engineer and tightly control optical properties such as power, beam shape, and spectral width.

Applications enabled by chip-scale far-UVC

Because its optical characteristics can be engineered at the chip level, Uviquity's PIC platform supports a wide range of applications.

Air disinfection and allergen control

In enclosed spaces, airborne pathogens are a primary driver of disease transmission. Far-UVC light can continuously inactivate viruses, bacteria, and spores as they circulate through a room, reducing transmission risk in real time. Studies have demonstrated rapid reductions in airborne pathogen concentrations, even under conditions where new pathogens are continuously introduced. Additionally, far-UVC light has been shown to rapidly reduce airborne allergens like dust mites, pet dander, mold and pollen. This combination of pathogen and allergen control highlights the potential for significant improvement in indoor air quality and comfort.

Unlike HVAC-based interventions, which require high airflow rates and significant energy consumption to achieve comparable air-change equivalents, far-UVC light sources operate locally within occupied spaces. Chip-scale emitters make it practical to integrate far-UVC sources into overhead lighting fixtures, transportation cabins, air purifiers, and other distributed systems, bringing disinfection and allergen inactivation directly to the point of highest risk rather than relying solely on centralised filtration.

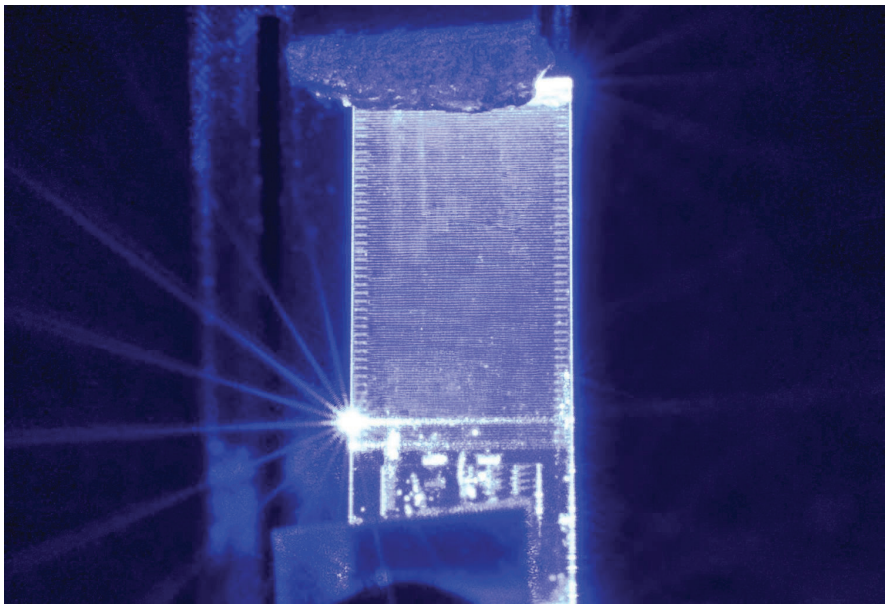
Surface disinfection

High-touch surfaces play a critical role in pathogen spread, particularly in healthcare and food-handling environments. Far-UVC light disrupts both nucleic acids and protein structures, enabling rapid inactivation of a broad range of microorganisms, including drug-resistant bacteria.

Because far-UVC light can be used safely in occupied spaces, it enables frequent or continuous surface decontamination without interrupting normal operations. This opens new possibilities for reducing healthcare-associated infections, improving food safety, and extending shelf life across the food supply chain while reducing reliance on chemical disinfectants and addressing fungicide-resistant crops. Pathogens treated with far-UVC light are also less susceptible to photoreactivation than those dosed with 254 nm UVC, making it well-suited for use in crop protection during daylight hours and in the presence of people.

Water treatment

Far-UVC light is also effective in aqueous environments, where its higher photon energy can improve inactivation efficiency for certain pathogens compared to conventional 254 nm UVC. The shorter wavelength increases absorption in microorganisms and can reduce the required dose for specific targets, including viruses, bacteria, protozoa, and other waterborne microorganisms. Uviquity's solid-



➤ Uviquity's AlN photonic chip converts 445 nm blue laser light into 222 nm far-UVC light.

state emitters provide a mercury-free alternative with dramatically smaller form factors, longer operating lifetimes, and reduced maintenance. These attributes enable compact point-of-use and point-of-entry systems, as well as modular integration into industrial and municipal water-treatment infrastructure.

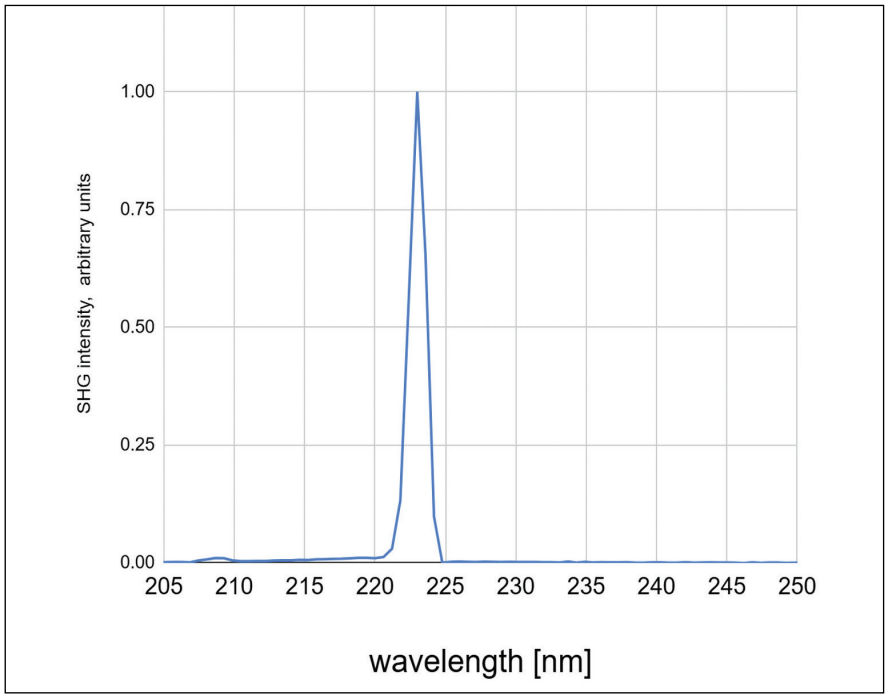
Optical sensing and analytical instrumentation

Beyond disinfection, far-UVC wavelengths are highly valuable for analytical instruments, including absorbance and fluorescence spectroscopy, and deep-UV Raman techniques. Uviquity's PIC provides a narrow linewidth, collimated far-UVC light source with precise wavelength control to improve signal-to-noise ratios, while enabling more compact instrument designs.

These attributes are beneficial to existing analytical instruments and potentially disposable analytical instruments and sensors for environmental monitoring, life science, defense and semiconductor metrology applications.

Chemical destruction

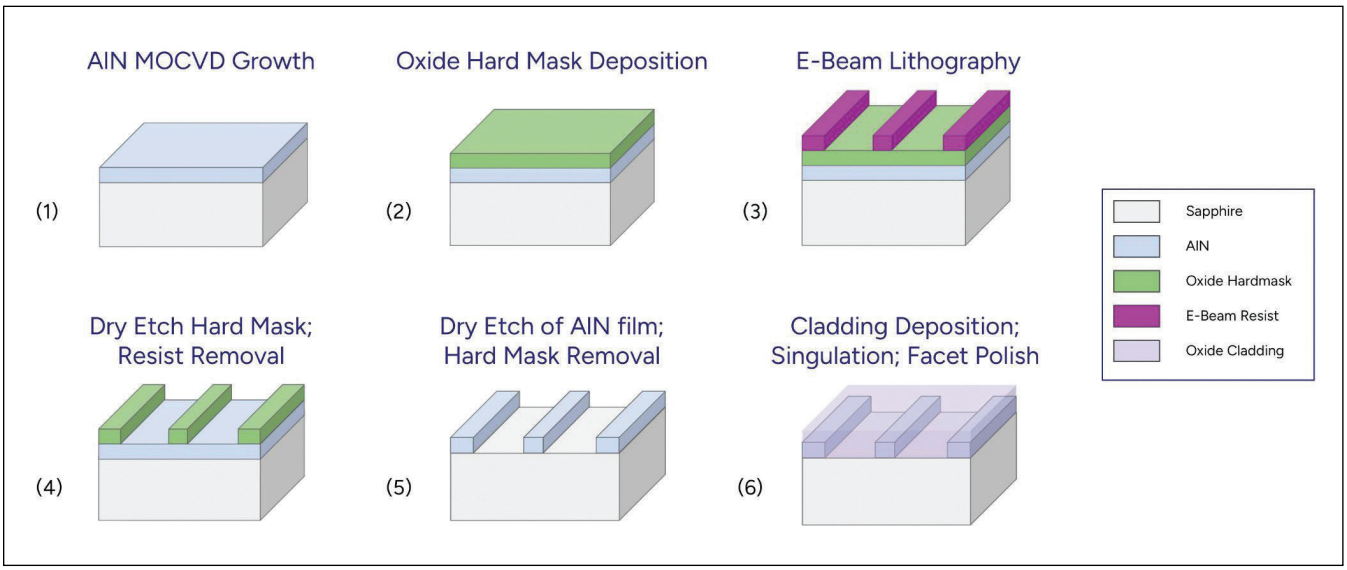
High-energy far-UVC photons can drive direct photolytic chemical destruction by breaking strong molecular bonds that resist longer-wavelength UV light. Unlike advanced oxidation processes (AOPs), which depend on added reagents and radical chemistry, far-UVC photolysis enables direct bond cleavage under controlled conditions. This approach is well suited to treating persistent contaminants such as chloramines, selected pharmaceuticals, and certain per- and polyfluoroalkyl substances (PFAS) and related so-called "forever chemicals," where direct photolytic bond cleavage is required. Uviquity's chip-scale, spectrally pure emitters support precise process control and scalable deployment in advanced water-treatment applications.



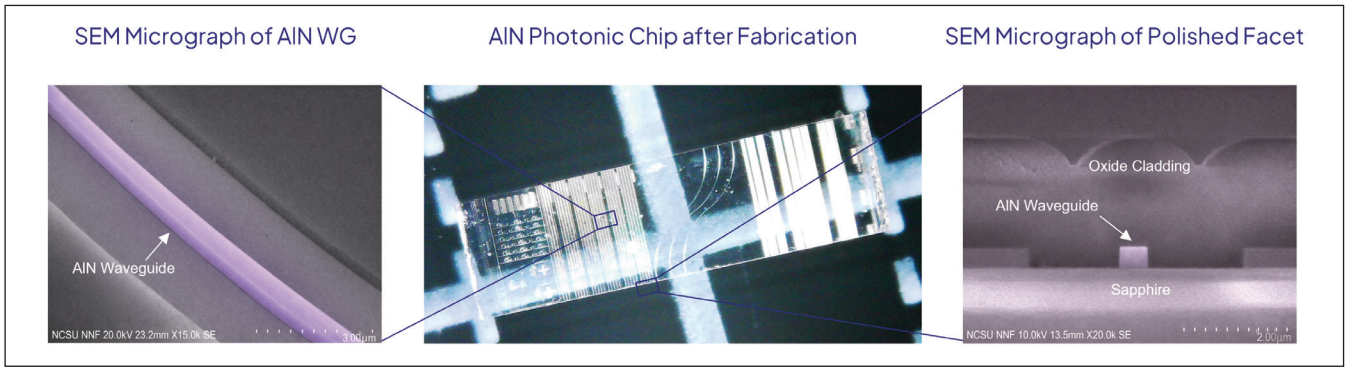
Uviquity's far-UVC light emitter generates a narrow linewidth output with a peak wavelength at 222 nm.

Extending the platform: quantum photonics

Uviquity's aluminum nitride PIC platform also supports emerging quantum photonic applications. AlN's strong nonlinear optical properties enable low-noise frequency conversion across ultraviolet, visible, and telecom wavelengths on a single chip.



Uviquity has developed a proprietary process to fabricate its far-UVC chips. Beginning with an MOCVD-grown AlN epitaxial wafer, high quality waveguides are fabricated with very smooth sidewalls subsequent to the cladding deposition.



➤ (Center) Uviquity's AlN R&D test chip after fabrication. The features on the chip are the waveguides through which light passes. (Left) Magnified area of the chip to show a single AlN waveguide. (Right) Cross section of the chip identifying the AlN waveguide between a bottom sapphire substrate and a top oxide cladding. Waveguides color-enhanced for emphasis.

This capability allows quantum information carried by photons to be translated between otherwise incompatible systems, such as atomic, ionic, solid-state, and fibre-based platforms, using wafer-scale semiconductor manufacturing.

By supporting both up- and down-conversion with high fidelity, the platform has the potential to serve as a foundational optical interconnect layer as quantum systems scale and become increasingly networked.

Advancing toward commercial deployment

With far-UVC light generation demonstrated using an integrated AlN photonic platform, Uviquity is now focused on commercialization.

Near-term efforts center on completing the company's first product designs and engaging partners for characterization and application testing. Uviquity is working with partners across multiple industries to bring this technology into real-world systems.

At the same time, the technology's roadmap targets continued improvements in nonlinear conversion efficiency, output power, and packaging flexibility advances that will further expand the range of applications.

➤ Uviquity's PIC technology enables compact far-UVC light engines that integrate seamlessly into standard photonic packages.

A solid-state foundation for ubiquitous far-UVC light

By shrinking far-UVC light generation into a solid-state PIC platform, Uviquity enables a new class of disinfection, optical sensing, and photonic systems.

The combination of human safety, germicidal efficacy, spectral purity, precision beam control, compactness, and semiconductor scalability positions the company's chip-scale far-UVC light emitters as a powerful tool for improving global health, food security, and environmental sustainability.

With far-UVC light generation demonstrated using an integrated AlN photonic platform, Uviquity is now focused on commercialization. Near-term efforts center on completing the company's first product designs and engaging partners for characterization and application testing.

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Entropy Computing: A photonics-enabled quantum computing solution for optimization

QCi's Dirac-3 hybrid photonic system uses entropy computing to tackle complex NP-hard optimization problems, demonstrating rapid convergence, global minimum detection, and scalable performance beyond conventional classical approaches

BY JENN ROBINSON, LAC NGUYEN, POUYA DIANAT, AND YONG MENG SUA, QCI

ADVANCED computational problems underlie some of the most seemingly-mundane problems in our lives. The quintessential logistics problem – the traveling salesman problem, which aims at finding the best route for a traveling salesman to take for his sales – is also a classic example of an NP-hard problem.

While mathematically interesting, it is more important that these problems also represent critical issues in everyday life. Optimization problems inform everyday processes like GPS routing, shipping logistics, and process development in manufacturing, and making the solution of these problems more efficient could have profound effects on everyday applications.

Quantum and quantum-inspired computation is one way in which advanced tech can make these problems more easily solved in the real world. While large-scale, fault-tolerant entangled-gate quantum computers are still years away, intermediate machines based on advanced photonics, such as the Dirac-3 system from Quantum Computing Inc. (QCi), can be designed to enhance the efficiency of solving NP-hard optimization problems.

In their recent paper, QCi describes using their hybrid photonic-electronic computer in a paradigm called entropy computing to solve a sample non-convex optimization problem, which can also demonstrate how the calculations will scale as problems become more complex.

Dirac-3 and entropy quantum computing

The Dirac-3 is a hybrid photonic-electronic computing system that leverages an entropy quantum computing paradigm to solve large-scale optimization problems. The system uses time-correlated single photon counting and electro-optic feedback. A future version could also operate in an all-optical configuration.

The Hamiltonian is encoded into the amplitude of an electrical signal, which is then used to modulate an electro-optic modulator (EOM). A continuous-wave laser that has been passed through a variable optical attenuator to produce a weak coherent state is then passed through the EOM that is modulated by the Hamiltonian-encoded signal. This light is combined with unmodulated light and fed into a periodically-poled lithium niobate (PPLN) nonlinear crystal, which combines the two light beams using sum-frequency conversion, where the resulting light's frequency is the sum of the two combined beams.

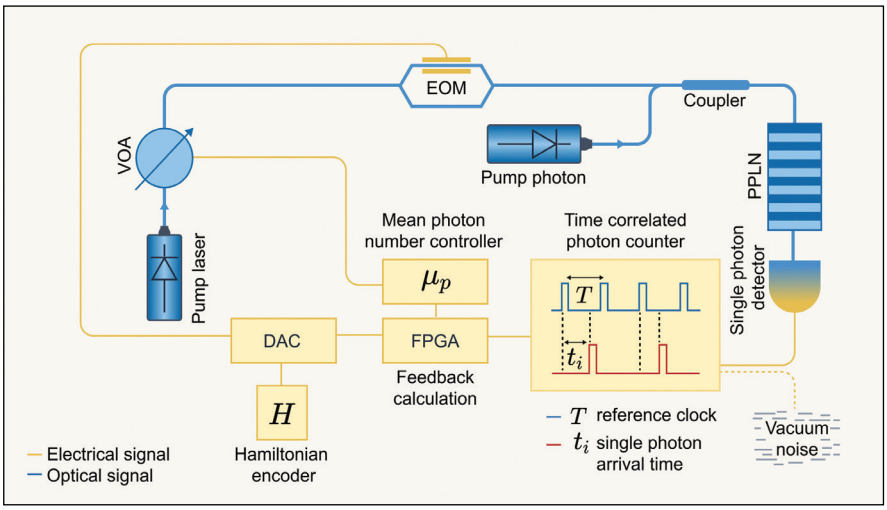
The output of this process is collected using time-correlated single photon counting and processed using a field-programmable gate array. This is then fed back to the EOM.

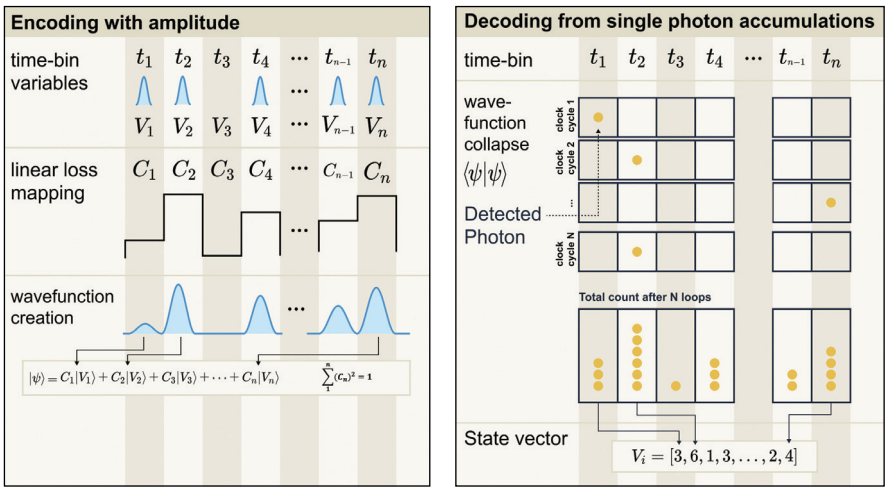
After several feedback iterations, the time-binned accumulated photons represent the internal state vector of the Hamiltonian.

Unlike quantum annealers, the Dirac-3 system does not just approximate Boltzmann sampling, but directly minimizes the encoded Hamiltonian. A key feature of the system is the ability to handle a large dynamic range without losing fidelity and compromising solution quality.

A simple two-variable non-convex quadratic optimization problem can be used to demonstrate how this system can solve an optimization problem. The sample function is a quadratic function with three local minima and a global minimum. Not only does Dirac-3 converge rapidly to a solution within a few iterations, but it also shows the ability to avoid the local minima and converge on the global minimum, even in cases where the starting point for the problem was near a local minimum. Beyond this simple implementation, the system has been benchmarked using a 50-variable non-convex quadratic problem that is hard enough that a conventional gradient descent program often becomes stuck in a local minimum point.

➤ The Dirac-3 high-performance photonic-enabled hybrid quantum computing system.





➤ The schematic for the entropy computing system using time-energy modes and a measurement-feedback system. The system is a hybrid electro-optic system that encodes the Hamiltonian into an optical signal.

Dirac-3 not only is able to converge to a solution nearly 80% of the time, it also shows the same avoidance of non-optimal minima that was seen in the smaller problem.

This successful benchmarking led QCi researchers to then implement a true NP-hard problem on Dirac-3. The maximum cut, or max-cut, problem, describes the partitioning of the vertices of a graph such that the number of edges is maximized. A 30-node unweighted graph was considered, which was then cut into a varying number of subsets. Dirac-3 was able to outperform Semi-Definite Programming (SDP), a standard current way of solving the problem, for two, three, and four cuts.The Dirac-3 has been successfully demonstrated in non-convex and combinatorial optimization programs, with a particular advantage in problems that demonstrate the same sum constraint present in the current version of Dirac. Similar problems have applications to portfolio optimization and resource allocation problems as well as problems involving elections and voting systems, among others.

Dirac-3 also simplifies the implementation of higher-order interactions in many problems by directly mapping high-order optimization problems. This provides an increase in solution quality and precision while requiring fewer resources to run. This successful benchmarking of Dirac-3 for solving optimization problems shows that further studies are necessary to explore its full capabilities.

Photonics enabled quantum progress

The Dirac-3 is a system that is fundamentally enabled by advanced photonics. While the current incarnation is a hybrid photonic-electronic system, an all-optical implementation of the system is possible.

Currently, Dirac-3 relies on the speed of high-performance single photon detectors for accurate operation, and couples them with PPLN waveguides to ensure a compact and stable system by maintaining high efficiency and low dark counts. The integration of lithium niobate elements into the system also opens up the possibility of integrating Dirac-3's operation protocol onto a nonlinear photonic integrated circuit (PIC).

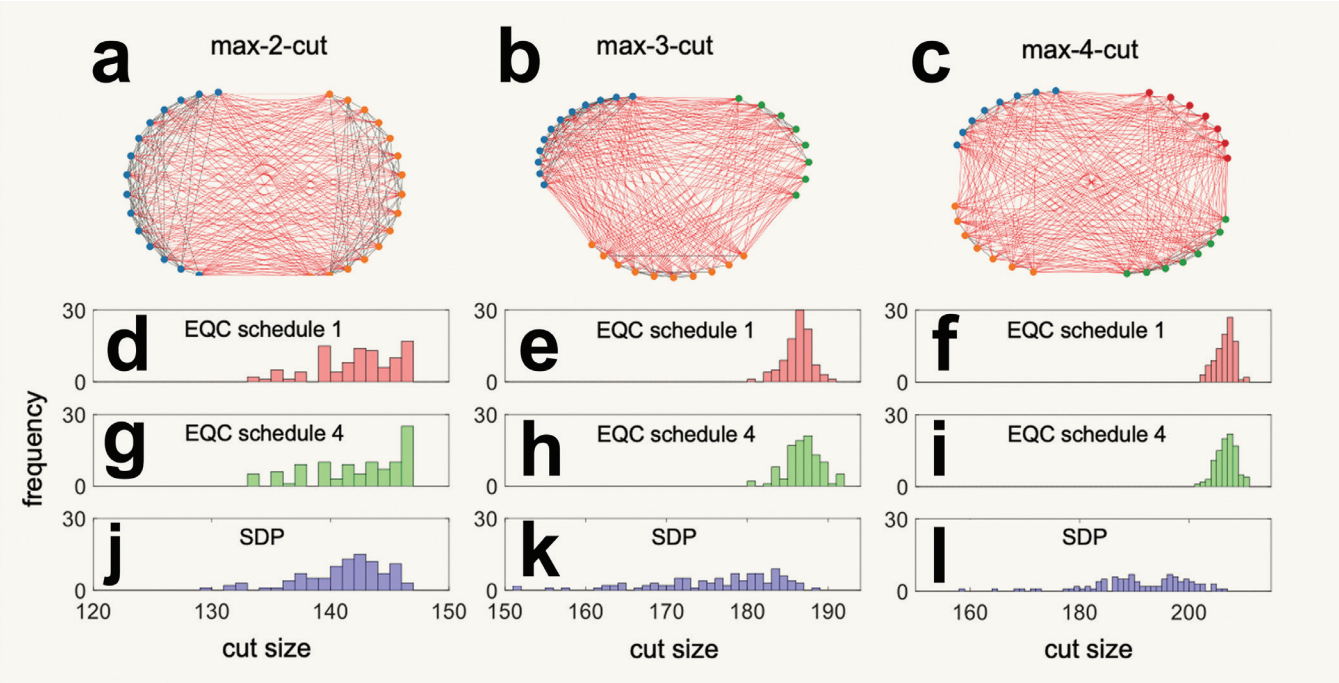
The ultimate goal of an all-optical entropy quantum computing system would be a system that can be integrated on a photonic chip. Such a system would be compact and efficient, and, coupled with the room-temperature operation of a photonic open quantum system, would represent an accessible form factor for quantum-enhanced calculations. Systems using PICs would be scalable for production at a higher volume.

As the limitations of conventional classical computing systems become apparent for solving these NP-hard optimization problems, advances in photonics, particularly efficiency and speed of single photon detectors and the quality of optical modulators and mixers, will enable the new generation of quantum-enhanced calculations.

The benchmarking of the Dirac-3 not only shows how incorporating photonic elements into a hybrid computing system can provide near-term benefit in computing, but also hints at how next-generation photonic quantum entropy computing could represent a further advance in solving optimization problems.

QCi foundry and the quantum supply chain of the future

QCi aims to position itself not just as a vendor of high-performance quantum-enabled solutions to the technological problems of today's world, but also as a key element in the future quantum industrial ecosystem. The lack of a robust supply chain for critical high-performance components for quantum technology remains a key stumbling block in scaling the manufacture of quantum tech.



➤ The results for solving max-cut problems on Dirac-3. These are the results of optimizing the problem for a max-2-cut, a max-3-cut, and a max-4-cut for a generalized 30-node graph, which is generated randomly with a 0.5 probability of connectivity between each two nodes.

The QCi Foundry is QCi's answer to the problems of smaller companies that cannot develop in-house manufacturing but have outgrown university fabs and whose devices are more advanced than is produced in traditional semiconductor facilities.

The QCi Foundry focuses on thin-film lithium niobate, which combines manufacturing convenience with high performance as a nonlinear optical medium to be an ideal candidate for next-generation high-performance integrated photonics.

The Dirac-3 is QCi's flagship advanced computing system and represents the advantage that photonics-enabled machines will have in tackling the optimization problems of the future. By continuing to explore improvements to this technology and by building up their own in-house photonics capabilities, QCi is bringing the quantum future into the present by putting photons to work.

REFERENCE

➤ Lac Nguyen, et al. "Entropy Computing, a Paradigm for Optimization in Open Quantum Systems." Communications Physics, 8, 411 (2025)

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