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Beyond Communication, Silicon Photonics is Penetrating Consumer and Automotive Applications

STRATEGY ANALYTICS

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INSIDE

EUROPE PILOTS PIC PRODUCTION

Producing PICs at industrial scale is a growing capability across the EU thanks to multiple EC-funded programme ecosystem within Europe's borders

HYBRID INTEGRATION

Hybrid integration methods are gaining attention as PIC technologies are requiring sophisticated solutions

GETTING PICS OFF THE GROUND

PICs based on InP and GaAs prepare to slash the size, weight and power of systems to be deployed in space and on-board aircraft for a variety of sensing applications

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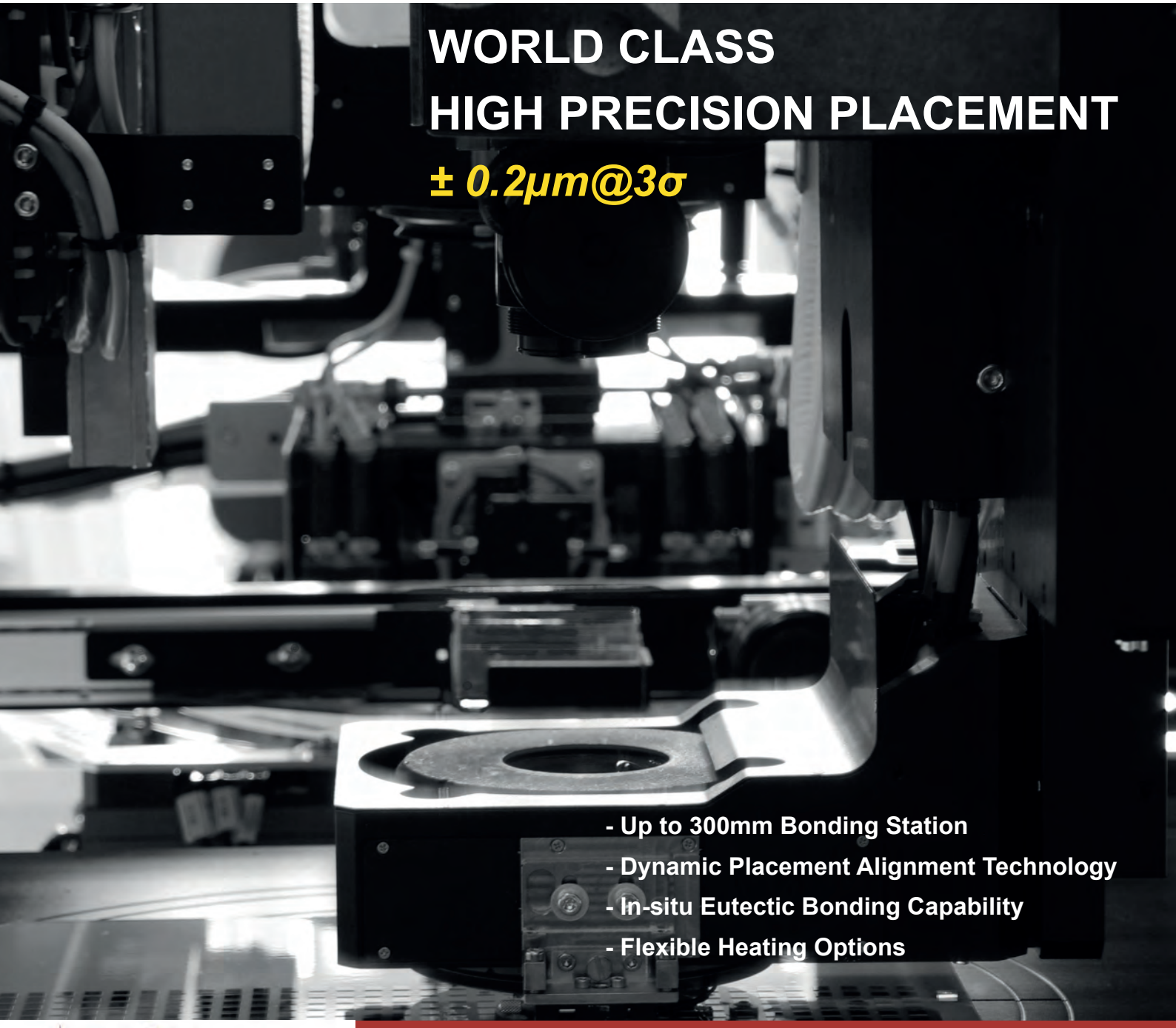

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VIEWPOINT

By Mark Andrews Technical Editor

angel tech
PIC INTERNATIONAL CONFERENCE

Get ready for AngelTech and PIC International 2022

AS THIS EDITION of PIC Magazine readies for publication, we are mere weeks away from AngelTech 2022 and PIC International, one of the three-in-one conference events that make AngelTech unique in its scope. Hear the latest developments from industry leaders and what new innovations can mean for your business, all in one convenient location.

One topic sure to be discussed at this year's PIC International is the announcement in April by Synopsis and Juniper Networks that the two industry leaders plan to create a to-be-named company that will focus on Silicon Photonics (SiP). Synopsis and Juniper say its priority is to bring a new, integrated Indium Phosphide (InP) laser, plus optical amplifiers and other key PIC building blocks, directly onto a silicon wafer via Tower Semiconductor's PH18DA process tech. The companies say they expect their initial multi-project wafers will be taped out later in 2Q.

2022's PIC International will bring together representatives of leading companies from across the photonics ecosystem. Attendees will also hear from noteworthy industry analysts who will offer keen insights into how advances and opportunities within PIC design, development and manufacture are changing and growing in the post-pandemic world. More than 30 speakers addressing wide-ranging PIC topics will share useful and actionable insights designed around maximizing attendee opportunities for business success.

In this edition of PIC Magazine we explore the unique device optimization possibilities enabled by the code-driven design process called IPKISS developed by Luceda Photonics. Utilizing code instead of GUI-based EDA software offers better version control and change traceability, according to co-founder Martin Fiers, as well as other benefits unique to their 'code-first' approach.

We also explore ongoing research from Samsung's Advanced Institute of Technology in developing PICs for LiDAR applications and seamless PIC testing designed to move devices from lab to fab courtesy of EXFO. We hear from EPIC as the European consortium
details what InPULSE—an Indium Phosphide pilot line – is doing to enable a self-sustaining PIC ecosystem. The EPIC article dovetails nicely with the organization's Pilot Line programme scheduled for 27th June, the day before AngelTech PIC International opens on the 28th.

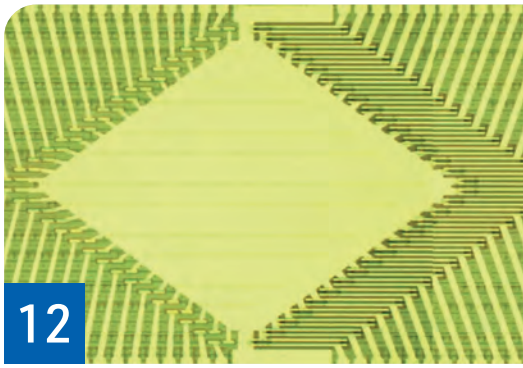
See you in Brussels!

PIC PHOTONIC INTEGRATED CIRCUITS

28

BEYOND COMMUNICATION, SILICON PHOTONICS IS PENETRATING CONSUMER AND AUTOMOTIVE APPLICATIONS

LiDAR in automotive applications is becoming one of the more exciting adjacent applications for photonics as that industry evolves toward more autonomous content and capability



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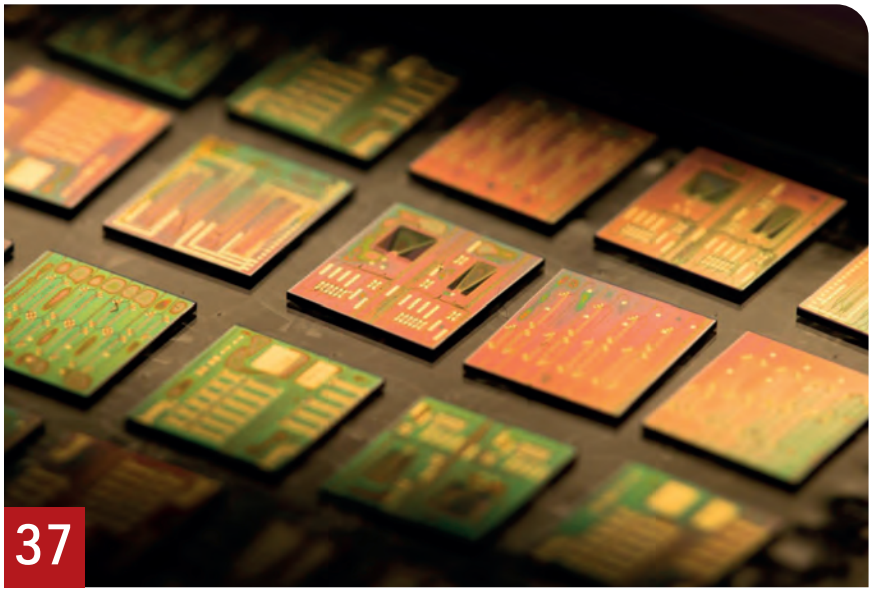

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Angel BUSINESS COMMUNICATIONS

Cognifiber downsizes system for edge computing with breakthrough glass processors

Cognifiber, a deep technology company focusing on revolutionizing photonic computing, announced the development of a glass-based photonic chip that will bring its technology one step closer to revolutionizing edge computing

BEING THE FIRST OF ITS KIND, this glass-based chip reduces power consumption and takes a fraction of the size of previous designs in CogniFiber's solutions.

Edge devices, including smart meters, smart home assistants, connected vehicles, and other IoT devices, rely primarily on cloud computing to rapidly recognize patterns and act in a seamless manner. Today, due to the edge devices' size and power limitations, they require a constant uplink with data centers, which face their own problems surrounding capacity and power consumption. Existing edge solutions may include low-power chips; however, these may limit speed, model size, and accuracy. To address this problem, Cognifiber is developing glass-based photonic chips that reduce its data center rack-size systems to a mere 4U server (~18cm high), making it deployable in any office. "The downsizing potential using glass-based photonic chips in conjunction with our proprietary fibers promises to bring superb-performance servers to the edge, removing many existing bottlenecks while dramatically reducing power consumption," said Dr. Eyal Cohen, Co-founder & CEO of Cognifiber. "Anything that generates vast amounts of data every second, such as connected vehicles, automated trains, or fleet management of large shipment drones can respond in real-time to events without reliance on data centers."

Cognifiber has already set the stage for reimagining Moore's Law. Replacing legacy silicon-based semiconductors, they are already in the advanced stages of developing in-fiber processing that minimizes the reliance on chips altogether by conducting complex computations within specialty optical fiber. "The future of computing demands a whole new way of transferring and processing vast amounts of data," said Professor Ze'ev Zalevsky, Co-founder & CTO of Cognifiber. "Combining photonic glass chips promotes our edge solution to bring rapid AI and Machine Learning locally to edge devices, which are limited in their capacity and power allowance."

Even with in-fiber processing, which can deliver a 100-fold boost in computing capabilities, there is still a reliance on semiconductors to conduct various operations of control and training. Future glass photonic chips, beyond downsizing, may provide a replacement for today's silicon ones, while reducing manufacturing costs, power consumption, and the removal of bandwidth bottlenecks.

This giant leap for the photonics industry creates the foundation for future capabilities while companies rely on edge devices to make increasingly complex autonomous decisions. "Devices will react faster and more reliably with our expected edge computing capacity," said Cohen.

LIGENTEC opens R&D centre in France

LIGENTEC SA, supplier of high performance, low loss, silicon nitride Photonic Integrated Circuits has established a R&D Centre in France. Photonic integrated circuits (PICs) are ready to repeat the success story of electronic integrated circuits (ICs)

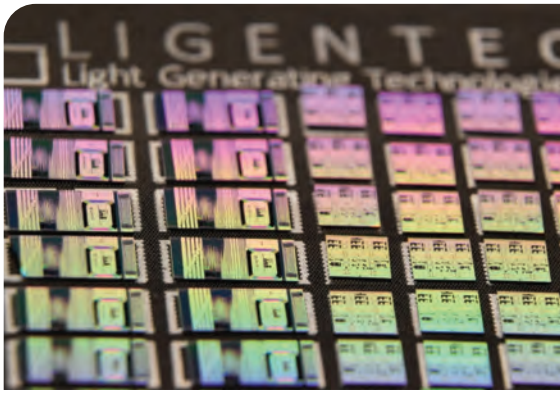
PICs work with light instead of electrons and will play a key role in tomorrow's crucial infrastructure in communication, sensing, transportation, and quantum computing.

LIGENTEC, originating from western Switzerland, has established its first foreign subsidiary in Corbeil- Essonnes near Paris. The newly formed company, LIGENTEC France SAS, will primarily act as a R&D centre to advance the LIGENTEC base technology as well as to expand it with new functionalities. The centre's expertise will cover the whole chain in PIC development, from design, wafer processing to characterization and is equipped with state-of-the-art equipment.

The centre is located in a new development area in Corbeil-Essonnes south of Paris, hosting a range of highly innovative high tech semiconductor companies. This local density of semiconductor technology, the great support by the tenant and the flexible options for expansion were key criteria for the location selection.

"This centre allows us to perform research and development very close to our strategic partner and will increase our efficiency," says LIGENTEC's co-founder Michalis Zervas, President of the new entity. "Furthermore, we benefit from the ideal boundary conditions for innovation given by the European Union, the French Government, the Region and the great talent pool in the metropolitan Paris region."

The newly formed company has already built a core team in Corbeil-Essonnes and plans to expand further in the next months.
"LIGENTEC is a fantastic company achieving key breakthroughs in the



PIC domain which we love at Jolt Capital. I am therefore delighted to advise Michael (founder and chairman) and Thomas (CEO), to share our network and our know how with them" commented Antoine Trannoy, Managing Partner at Jolt Capital, who recently joined LIGENTEC's board to support the management team in the scaling phase of the company and in the setup of its French subsidiary.

POET joins Singapore Photonics Centre as founding member

POET Technologies, designer and developer of the POET Optical Interposer and Photonic Integrated Circuits (PICs) for data centre and telecommunication markets, has announced that it has joined the Singapore Hybrid-Integrated Next Generation micro-Electronics (SHINE) Centre located in the College of Design and Engineering at the National University of Singapore (NUS).

The mission of the SHINE Centre is to address fundamental issues arising in IoT microelectronics and to engage industry players during the development cycle, to eventually translate the technology to industry. A strong team formed by professors across the world from NUS, NTU, University of California Berkeley and Northeastern University, A*STAR Institute of Microelectronics (IME) and DSO National Laboratories (DSO) will be actively involved as research participants.

"The vision for SHINE comes from Professor Aaron Thean, Dean of the College of Design and Engineering, with whom POET has worked for a number of years on certain engineering challenges, and more recently Professor Lim Yeow Kheng, who joined the faculty about two years ago from STATS ChipPAC Pte. Ltd.," said Suresh Venkatesan, chairman and CEO of POET Technologies.

He added: "We are delighted to be a founding member of SHINE, as it brings together equipment and expertise that NUS and companies in the consortium may use, independently and confidentially, to develop advanced processes and manufacturing techniques for hybrid integration of photonics devices. The systems, scientific instruments and engineering staff at NUS complements well our existing operation in Singapore, especially in the area of 2.5D and 3D semiconductor manufacturing. We plan to use the SHINE Center to design and manufacture Optical Interposer-based solutions for several new vertical markets, consistent with the mission of SHINE, including applications in sensing and the Internet of Things (IoT)."

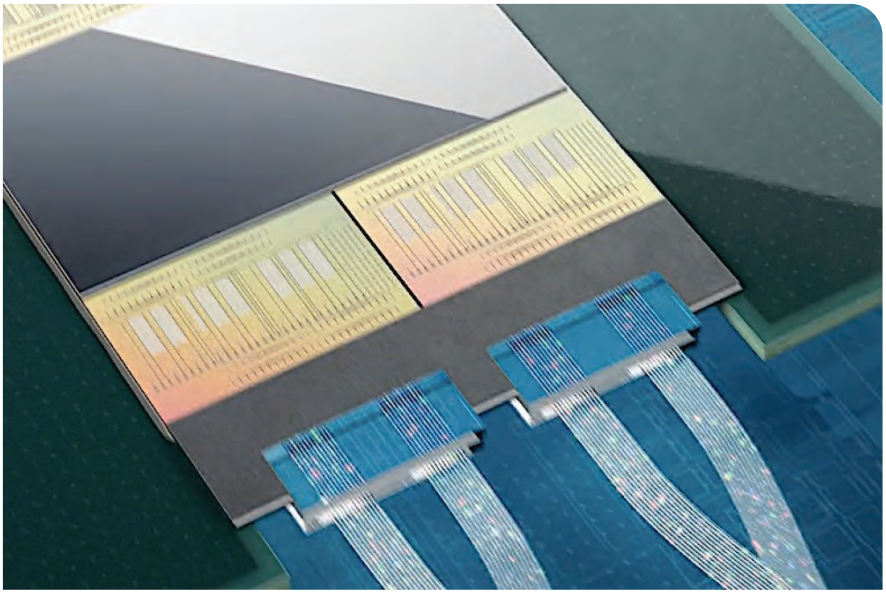
Ayar Labs raises $130M in Series C funding

Boardman Bay Capital Management leads round joined by Hewlett Packard Enterprise and NVIDIA to drive commercialisation of Ayar's optical I/O

AYAR LABS has secured $130 million in additional financing led by Boardman Bay Capital Management. The funding is to drive the commercialisation of Ayar's optical I/O solution, which is based on a patented approach using industry standard silicon processing techniques to develop optical interconnect "chiplets" and lasers to replace traditional electrical-based I/O.

Hewlett Packard Enterprise (HPE) and NVIDIA entered this investment round, joining existing strategic investors Applied Ventures LLC, GlobalFoundries, Intel Capital, and Lockheed Martin Ventures. Other new strategic and financial investors participating in the round include Agave SPV, Atreides Capital, Berkeley Frontier Fund, IAG Capital Partners, Infinitum Capital, Nautilus Venture Partners, and Tyche Partners. They join existing investors such as BlueSky Capital, Founders Fund, Playground Global, and TechU Venture Partners.

"As a successful technology-focused crossover fund operating for over a decade, Ayar Labs represents our largest private investment to date," said Will Graves, CIO at Boardman Bay Capital Management. "We believe that silicon photonics-based optical interconnects in the data center and telecommunications markets represent a massive new opportunity and that Ayar Labs is the leader in this emerging space with proven technology, a fantastic team, and the right ecosystem partners and strategy."



Optical connectivity will be important to scale accelerated computing clusters to meet the fast-growing demands of AI and HPC workloads

"Optical connectivity will be important to scale accelerated computing clusters to meet the fast-growing demands of AI and HPC workloads," said Bill Dally, chief scientist and SVP of Research at NVIDIA. "Ayar Labs has unique optical I/O technology that meets the needs of scaling next-generation silicon photonics-based architectures for AI."

Ayar Labs is ramping production and securing supply chain partners, as signaled by previously announced multi-year strategic collaborations with Lumentum and Macom, both leaders in optical and photonic products, as well as GlobalFoundries on its new GF Fotonix platform.

"Ayar Labs' highly differentiated technology is crucial to supporting the high-performance computing architectures of the future," said Paul Glaser, VP and head of Hewlett Packard Pathfinder, HPE's venture arm. "Ayar Labs represents a strategic investment opportunity for HPE to help our customers more efficiently derive greater insights and value from their data."

"The overall financing is much larger than we originally targeted, underscoring the market opportunity for optical I/O and Ayar Labs' leadership position in silicon photonics-based interconnect solutions," said Charles Wuischpard, CEO of Ayar Labs. "This financing allows us to fully qualify our solution against industry standards for quality and reliability and scale production starting this year."

Ayar Labs also announced that it made its first volume commercial shipments under contract and expects to ship thousands of units of its in-package optical interconnect by end of year.

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Fraunhofer IPMS consortium partner in research on photonic quantum chips

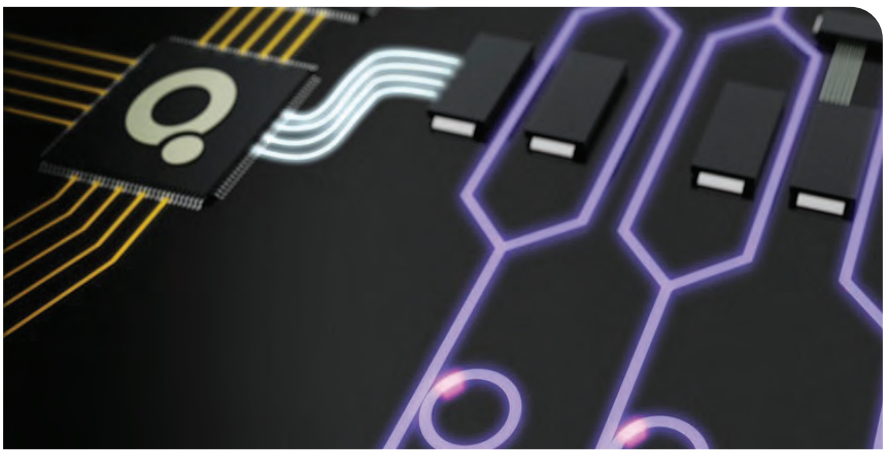
Everyone is talking about quantum computers. With the help of high interconnection of as many qubits (two-state quantum systems) as possible, massive amounts of data are to be processed more easily, quickly and securely in the future

IN THE PhoQuant project, a consortium led by the quantum start-up Q.ANT is now researching photonic quantum computer chips - made in Germany - which can also be operated at room temperature. One of the 14 consortium partners is the Dresden-based Fraunhofer Institute for Photonic Microsystems IPMS.

In the project “PhoQuant” many years of experience in cutting-edge research and business come together to bring quantum technology to industry. Many quantum computers still operate at extremely low temperatures close to absolute zero (- 273.15 °C). Cooling requirements are correspondingly high, and direct on-chip coupling with classical computer architectures is not possible. In order to ensure a symbiosis of quantum computer chips and conventional mainframe computers, the new photonic chip process is being applied in the “PhoQuant” research project.

The “PhoQuant” project is being funded with around 50 million euros. Of this, around 42 million euros will come from the German Federal Ministry of Education and Research (BMBF), while the consortium partners will contribute around 8 million euros. The funding will be used to build a demonstration and test facility for photonic quantum computer chips and other quantum computing components. In the project, the consortium will develop algorithms and technologies for photonic quantum computing and prepare for industrial deployment. The functions required for computing operations can be fabricated on a single chip using sophisticated semiconductor manufacturing processes. By depositing highly specialized light channels on silicon wafers, quantum states can be manipulated, controlled and monitored in the so-called “photonic integrated circuits” with almost no loss, even at room temperature. In the future, this will make it possible to use the chips to supplement conventional mainframe computers.

“The funding is an important signal for Germany as a location for innovation. We are at the dawn of the quantum computing age and the global race for market share of this future technology has begun. The funds now provided for this research alliance are an important building block for a quantum computer made in Germany,” says Michael Förtsch, CEO of Q.ANT. During the 5 years of the project, the goal is to provide an advantage for the computation of industry-relevant applications. A first example is the real-time optimization of schedules at airports in case of unforeseen delays.



For this purpose, the consortium is developing a new photonic computing architecture that will enable a quantum computer with up to 100 qubits during the course of the project. Tailored to this new architecture, optimized algorithms for special problems as well as algorithms for universal quantum computing will be developed during the project and made available to the public via cloud connection.

“In this project, Fraunhofer IPMS is developing FPGA and ASIC architectures with active interfaces for high-precision control and evaluation of functionalities of the photonic quantum computer chip. In addition to know-how in photonics, competences in mixed-signal control design for FPGA and ASICs are particularly necessary for this. These are competences that we can contribute in order to realize a common goal together with the consortium partners. Namely, to realize a high-performance photonic quantum computer,” explains Marcus Pietzsch, head of the PhoQuant project at IPMS.

In two and a half years, the project partners want to present a first prototype, and in five years at the latest, a quantum computer chip capable of performing large-scale calculations should be developed. Experts currently see the use of computers with quantum chips in sectors such as the chemical industry, biomedicine and materials science.

PhotonDelta ecosystem lands €1.1 Billion funding

Capital from the Netherlands government will be used to build 200 photonic startups and scale production

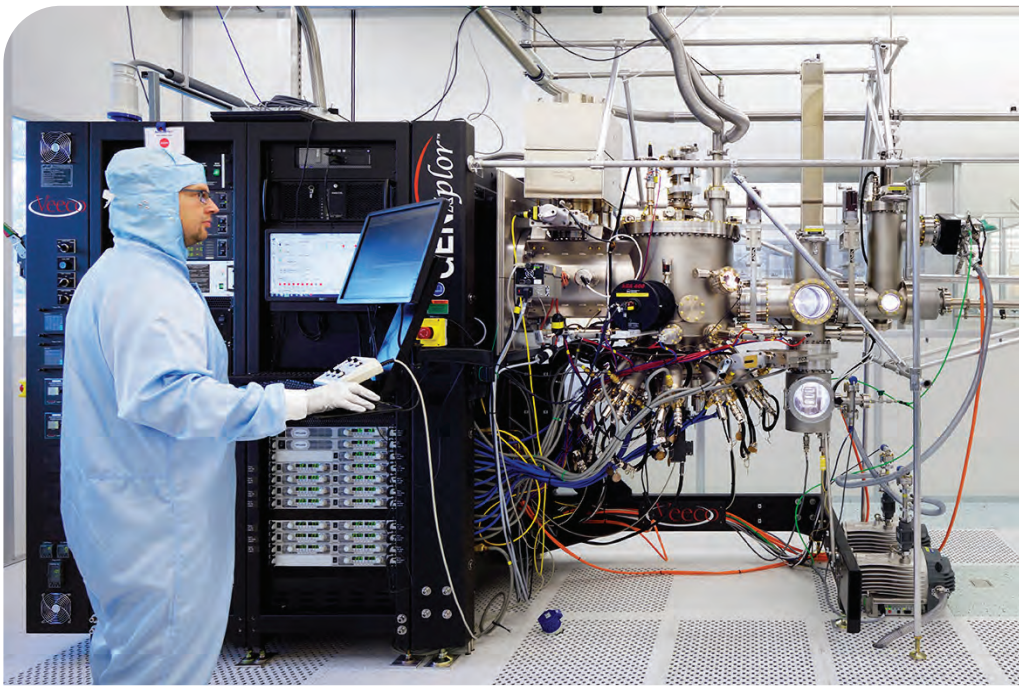
PHOTONDELTA, a cross-border ecosystem of photonic chip technology organisations, has secured €1.1 billion in public and private investment to transform the Netherlands into the leader of the next generation of semiconductors. The investment includes €470 million of funding obtained through the National Growth Fund (Nationaal Groeifonds), while the rest is co-invested by various partners and stakeholders. It is part of the Dutch Government's national plan to cement and expand the country's position as a world leader in integrated photonics.

The programme will run for six years and will enable PhotonDelta and its partners to further invest in photonic startups and scaleups, expand production and research facilities, attract and train talent, drive adoption, and develop a world-class design library. By 2030, PhotonDelta aims to have created an ecosystem with hundreds of companies, serving customers worldwide and a wafer production capacity of 100,000+ per year. Photonics uses photons (light) to transfer information. Photonic chips, also called photonic integrated circuits (PICs), integrate photonic functions into microchips to create smaller, faster and more energy-efficient devices. PICs can process and transmit data much more effectively than their electronic counterparts. Just like with traditional chips, the production process is carried out using automatic wafer-scale technology. This allows the chips to be mass-produced, reducing costs.

Crucially, PICs can overcome the expected limit to Moore's Law and will also help tackle energy sustainability issues. PICs are currently used in the data and telecom industry to reduce the energy consumption per bit and increase speeds. With data and internet use expected to be around 10% of global electricity consumption by 2027, PICs provide a powerful way to limit the impact on the climate. Photonic circuits will also soon play an important role for innovative sensors that can be mass-produced, leading to earlier diagnostics of diseases, safe autonomous vehicles and infrastructure, and more efficient food production. Ewit Roos, CEO at PhotonDelta, said: "This investment is a game-changer. It will make the Netherlands the home of the next generation of semiconductors which will have a profound impact on the whole European tech industry.

"The ongoing chip shortage highlights the pressing need for Europe to create its own production capabilities for strategic technologies. We will now be able to support hundreds of startups, researchers, producers and innovators to boost this industry that will be as impactful as the introduction of microelectronics a few decades ago. "The Netherlands is considered a pioneer in the development of PIC technology, and thanks to the continuous support from the Dutch government, we have been able to build a full supply-chain around it that is globally recognised as a hotspot for photonic integration. "Photonic chips are one of the most important technological breakthroughs of the last decade. Not only do they allow for the creation of devices that are faster, cheaper, more powerful and greener - they also enable radical new innovations like affordable point-of-care diagnostics or quantum computing to become a reality."

The PhotonDelta proposal has been submitted by the Dutch Ministry of Economic Affairs & Climate Policy in close collaboration with Eindhoven University of Technology (TU/e), University of Twente (UT), Delft University of Technology (TUD), Holst Centre, TNO, IMEC, PITC, CITC, Holst Centre, OnePlanet, Smart Photonics,Lionix International, Effect Photonics, MantiSpectra, PhotonFirst, Phix, and Bright Photonics.



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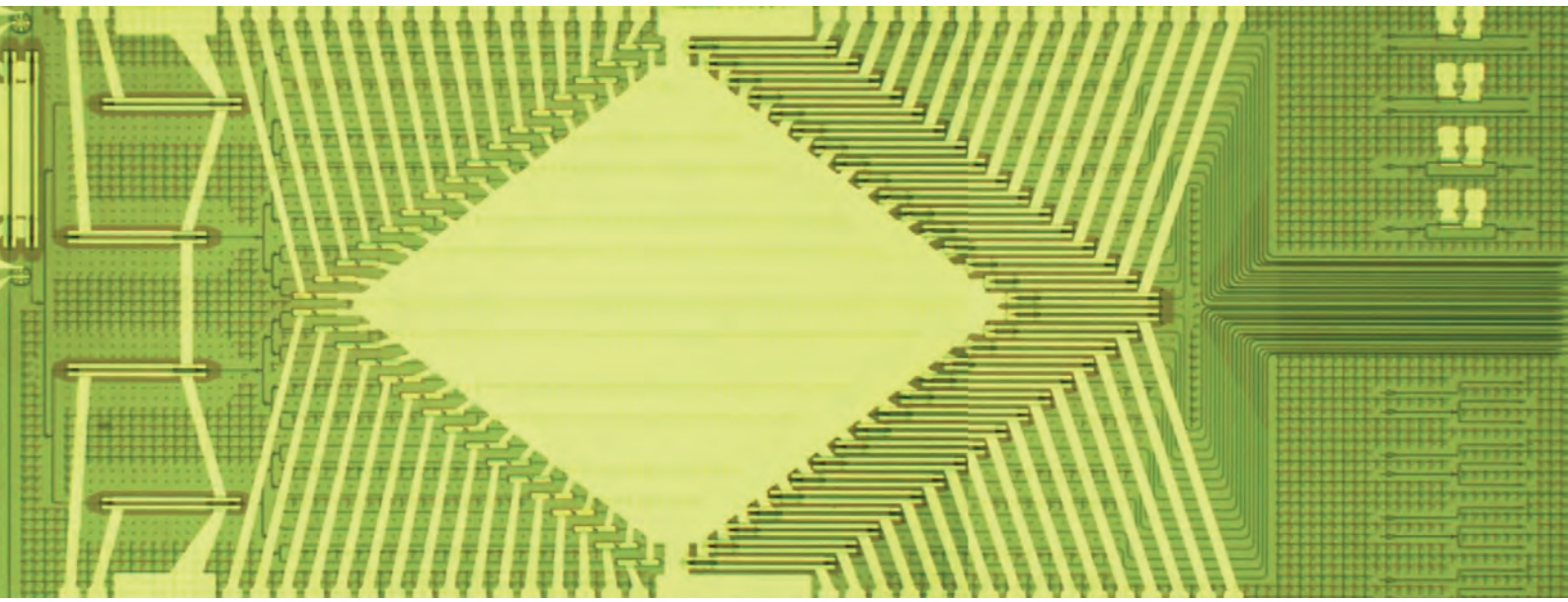


Samsung progresses in developing PICs for LiDAR

Microelectronics has truly revolutionized almost every aspect of life. Efforts to incorporate photonic integrated circuits (PICs) into advanced CMOS ICs today often center around fulfilling needs that II-VI or III-V based technologies cannot meet by themselves. Computing, automotive, wellness and myriad other applications will or are already benefitting from integrated photonic solutions. LiDAR is at an inflection point where further advances to reduce size and increase performance will likely hinge on incorporating new approaches such as those envisioned by researchers at Samsung Advanced Institute of Technology who report on recent advances in the quest to build a better PIC for LiDAR.

BY DONGJAE SHIN, KYOUNGHO HA, AND HYUCK CHOO, SAMSUNG ADVANCED INSTITUTE OF TECHNOLOGY

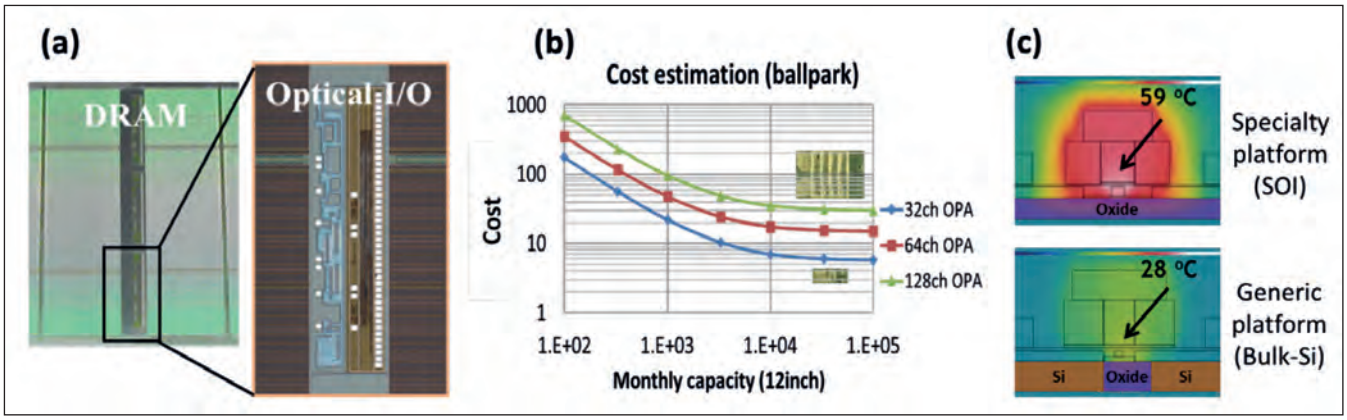
MODERN ELECTRONICS and photonics began around the middle of the 20th century with the inventions of the transistor and laser, respectively. Thanks to the continued evolution of complementary-metal-oxide-semiconductor (CMOS) technology that revolutionized transistors, microelectronics has for decades been a foundation for creating today's communications and computing systems and countless other innovations [1].

On the other hand, photonics is evolving at a relatively slower pace and is still confined, compared to microelectronics, to diverse but relatively smaller niche fields. Silicon Photonics (SiP) was born under this circumstance. Interest continues to grow as to whether Silicon Photonics can reduce the gap between the two technologies and achieve the commoditization of photonic devices by grafting the productivity of CMOS to photonics [2].

As the CMOS industry has given more technical attention to SiP, it is important to find 'killer applications' that can bridge the gap between technologies that can become profitable business opportunities since without a profit potential any technology will not see rapid development. This article introduces recent research by the Samsung Advanced Institute of Technology (SAIT) in support of photonic integrated circuits designed for light detection and ranging (LiDAR) sensors.

Why LiDAR?

In order to explain why LiDAR presents one of the best opportunities for photonic integration among



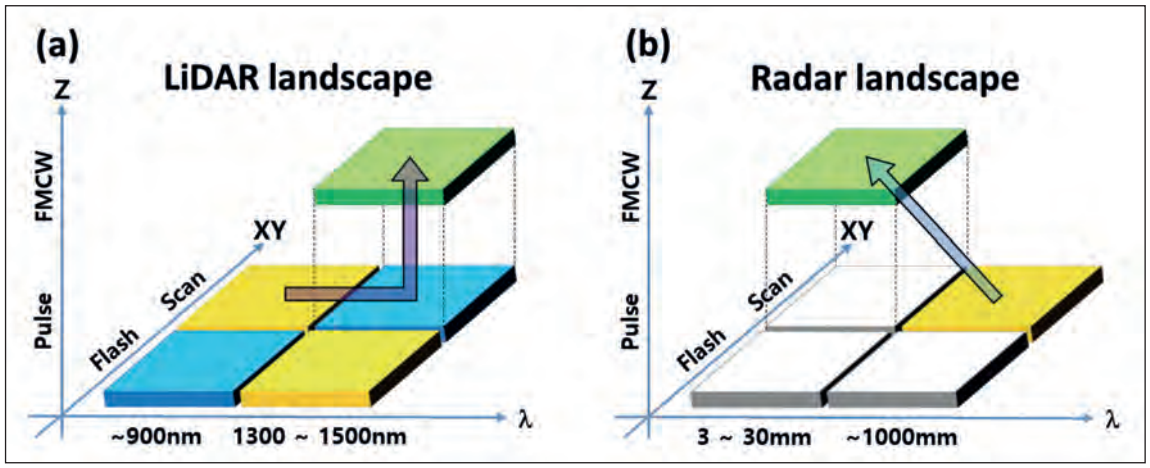
➤ Figure 1. (a) PIC embedded in 65nm DRAM. (b) Estimated volume-cost curve for LiDAR. (c) Thermal advantage of generic platform.

numerous applications, a glimpse into the product development history at Samsung is helpful. One of the most representative missions of SiP has been to resolve the DRAM-CPU interconnect bottleneck, the well-known Achilles heel of classical von Neumann computing architectures. Attempts were actively made by Samsung around 2010. Considering the cost limit of DRAM, photonic interconnect feasibility between DRAM and CPU was demonstrated by directly integrating a PIC into a DRAM chip as shown in Fig. 1(a) [3][4]. Despite such a significant achievement, these attempts also revealed the huge difference in technological maturity between CMOS and photonics, and did not lead to subsequent full-scale development. One of the lessons learned from this experience was that it is very difficult to apply emerging PIC technology directly to legacy applications that have matured for a long time. Samsung therefore believes that PIC technology is most suitable for emerging applications in many instances.

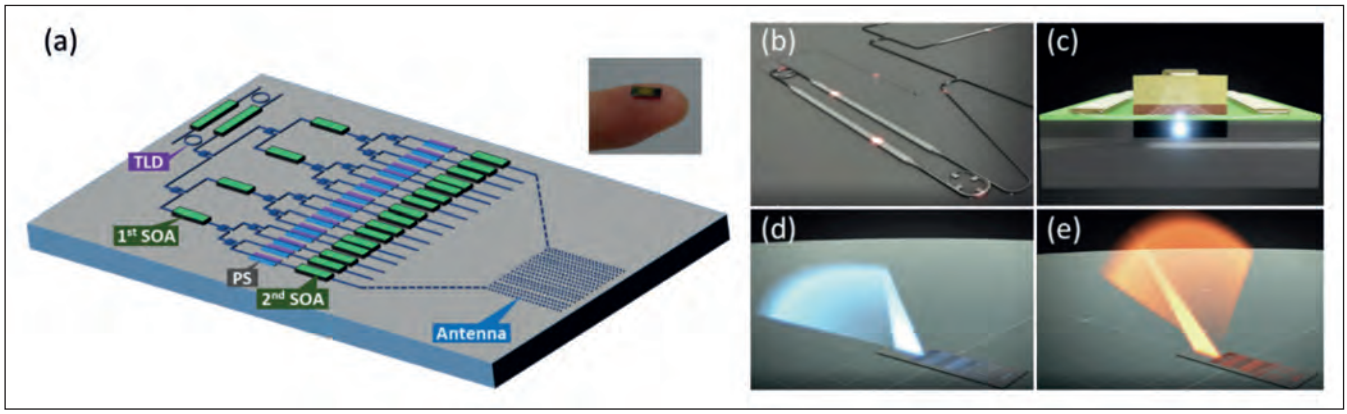
Among numerous emerging applications considered, LiDAR was chosen for three main reasons. The first reason is its possibility of high volume. Since LiDAR is (or will be) in high demand from various applications such as autonomous vehicles, robots, and smart devices, it is likely to achieve the high volume that can justify CMOS scale production. The second reason is its good timing from the perspective of CMOS evolution as characterized by Moore's Law and its relentless march towards smaller, faster devices that use less power and cost less to fabricate. Wide deployment of LiDAR has been delayed due to its high cost, so the virtuous cycle of volume and cost reduction from CMOS-like production processes has been an urgent goal for LiDAR development as shown in Fig. 1(b). The third reason is LiDAR's good match-up with Samsung's PIC platform. While most of the Silicon Photonics industry has been developing PICs on various specialty substrate-based platforms such as SOI, Samsung has developed PICs on a generic substrate-based platform for legacy applications as shown in Fig. 1(c) [5]. Thanks to ~100X higher thermal conductivity of silicon compared to oxide, Samsung's platform provides better heat dissipation, making it well-suited for heat-sensitive laser or amplifier arrays needed for LiDAR applications. This generic platform, however, is on hold for now, and the specialty platform is used for research purposes.

Technologies best suited for LiDAR

In LiDAR, various technology schemes are competing in terms of performance and cost, and the market winner is still uncertain at this point, especially for low-end applications. The rough consensus about LiDAR architectures is that solid-state solutions are most likely to win rather than mechanical systems with moving parts. Integration



➤ Figure 2. Technology landscapes of LiDAR(a) and RADAR(b).



➤ Figure 3. (a) LiDAR chip integrating TLD, SOA, PS, and antenna array. (b) TLD planar structure. (c) SOA vertical structure. (d) Horizontal beam scan in lower elevation angle with short wavelength. (e) Horizontal beam scan in higher elevation angle with long wavelength.

rather than assembly of disparate technologies will have an advantage in competition; comparative discussions are actively underway from various viewpoints.

The road to an optimized LiDAR solution typically considers three most important viewpoints: planar (XY) illumination, axial (Z) ranging, and wavelength as shown in the Fig. 2. Illumination typically employs the flash scheme, with simultaneous illumination of the entire field of view (FOV) while the scanning scheme employs sequential illumination in each direction comprising the FOV. The flash scheme has already been commercialized for short-range applications by utilizing the existing CMOS ecosystem, and the scanning scheme has been proven for a long time in long-range radio detection and ranging (RADAR) applications.

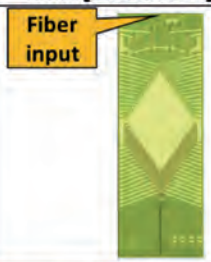
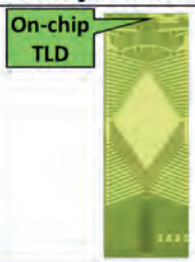
Ranging could involve various approaches such as the time of flight (TOF) scheme that transmits short light pulses while the frequency modulated continuous wave (FMCW) scheme transmits frequency modulated light. Considering that RADAR evolved from TOF to FMCW, it is believed that a similar evolution is likely to occur in LiDAR.

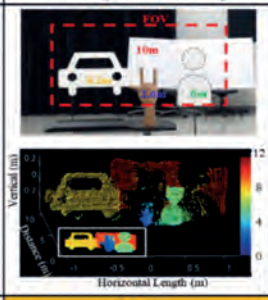
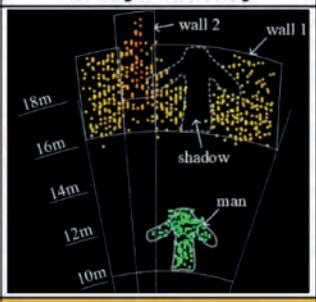
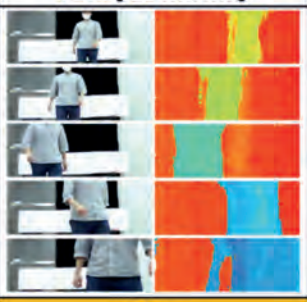
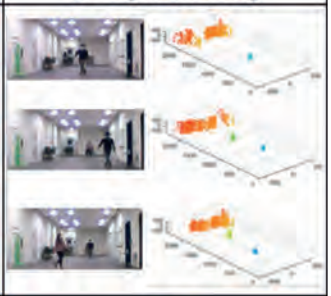
In wavelength, there is the silicon-compatible ~900nm band and the III/V-based 1.3~1.5um band. The ~900nm band is advantageous from the perspective of the existing industry ecosystem, but the 1.3~1.5um band is advantageous from the perspective of eye safety and resistance to ambient light noise. SAIT has been adopting the scanning scheme and the 1.3um band with more focus on long-range applications; it is preparing to evolve from TOF to FMCW.

PICs for LiDAR

As is appreciated in many photonics applications, to maximize the volume-cost virtuous cycle, it is necessary to integrate all photonic devices on a single chip. Until now, photonic devices for a LiDAR transmitter (Tx) have been integrated into a single chip first, with receiver (Rx) photonic devices integrated after clearing architectural uncertainties. The LiDAR Tx is an optical phased array (OPA) that corresponds to a photonic version of the RF phased antenna array used for RADAR. Figure 3 conceptually illustrates the OPA chip and main photonic devices such as tunable laser diode (TLD),

➤ Figure 4. LiDAR device integration progress.

	PoC1[CLEO2021]	PoC2[CLEO2020]	PoC3[IEDM2020]	PoC4[IEDM2021]	PoC5
Chip					
Platform	Si	III/V on Si	III/V on Si	III/V on Si	III/V on Si
Ch#/size	128ch, 5.7 x 5mm	32ch, 7.5 x 3mm	32ch, 7.5 x 3mm	32ch, 8.7 x 3mm	TBA
OPA	Integrated	Integrated	Integrated	Integrated	Integrated
SOA	Assembly	Integrated	Integrated	Integrated	Integrated
TLD	Assembly	Assembly	Integrated	Integrated	Integrated
PD	Assembly	Assembly	Assembly	Assembly	Integrated

	PoC1[CLEO2021]	PoC2[CLEO2020]	PoC3[IEDM2020]	PoC4[IEDM2021]
Real-time 3D data				
Range	~10m	~20m	~10m	~20m
FOV	50 x 7°	12 x 3.2°	15 x 3.5°	20 x 3.5°
Res.(H x V)	100 x 36	40 x 21	120 x 20	120 x 20
Frame rate	slow	2 fps	20 fps	20 fps

➤ Figure 5. LiDAR performance progress.

semiconductor optical amplifier (SOA), phase shifter (PS), and antenna array. The OPA amplifies the 32-way split outputs of the TLD by a total of 36 SOAs and controls the phases with 32 phase shifters, thereby reducing the diffusion angle of the optical beam from the antenna array. The optical beam is then scanned by the phase shifters in the horizontal direction and by the TLD in the vertical direction as shown in Fig. 3(d) and (e). The TLD controls the lasing wavelength by the heaters in the two ring resonators shown in Fig. 3(b).

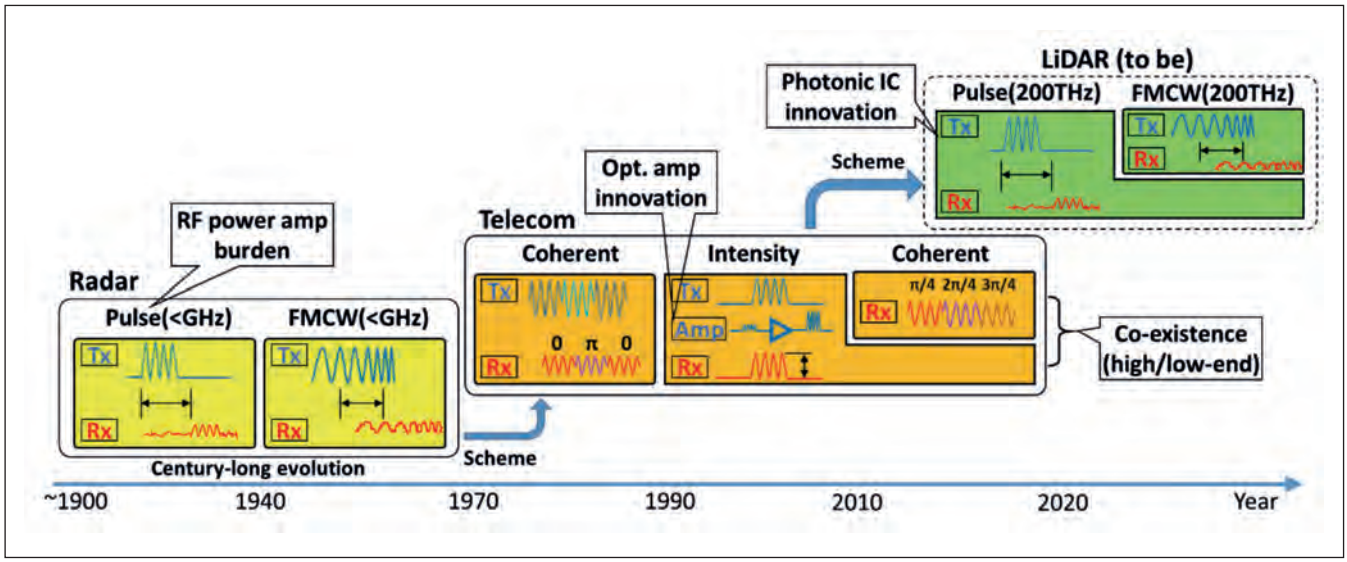
When fabricating the OPA, silicon processes were followed by III-V on silicon bonding and III-V processes. This III-V on silicon heterogeneous integration is advantageous for low-cost manufacturing since it simplifies subsequent packaging. The III-V material used for this work is combination of four elements in the group III and V of the periodic table such as Aluminum, Gallium, Indium, and Arsenic, grown on InP substrates.

LiDAR developmental status

In moving toward single-chip integration, the progress of device integration so far is summarized in Fig. 4. From the PoC1 in which only the phase shifter and antenna array were integrated with a silicon-only process, to the PoC2 with additional integration of the SOA, to the PoC3 and the PoC4 groups with additional integration of TLD. These were fabricated through III-V on silicon process [6] [7]. From the PoC3 to the PoC4, the circuit layout was improved to reduce on-chip losses and thermal effects [8][9]. The PoC5 with integrated photodiodes (PDs) is also under consideration, but its integration is still ongoing due to delays related to some LiDAR architectural issues. In the PoC1, using a relatively simple silicon-only processes, an OPA with 128 antennas was fabricated, and from the PoC2 with higher III-V on silicon process challenges, OPAs with 32 antennas were fabricated due to lower device yields. The optimal antenna count is determined as part of a performance-cost trade-off, and is expected to vary according to the detection distance required for various applications.

The success of various technology combinations designed to achieve optimal LiDAR performance is summarized in Figure 5. While the PoC1 group had decent resolution with 128 antennas, a very slow frame rate was unavoidable due to low OPA output power and slow external TLD. In the PoC2 testing, because the OPA output power was improved through the SOA integration, video recording at 2 frames per second became possible, but the resolution was lowered due to the decrease in the antenna count. In the PoC3 tests, a 20 frames per second video recording was achieved thanks to the additional integration of TLD, and the resolution was also improved by digital signal processing (DSP) and image signal processing (ISP). In the PoC4 tests, the detection range and FOV were

When fabricating the OPA, silicon processes were followed by III-V on silicon bonding and III-V processes. This III-V on silicon heterogeneous integration is advantageous for low-cost manufacturing since it simplifies subsequent packaging. The III-V material used for this work is combination of four elements in the group III and V of the periodic table such as Aluminum, Gallium, Indium, and Arsenic, grown on InP substrates.



➤ Figure 6. Insights from RADAR and Telecom evolution.

improved as the output power increased by the optical and thermal improvement of the OPA. Efforts to optimize performance are currently underway to reach the performance levels demanded by the market. In particular, improving the FOV is the most urgent issue as indicated in Fig. 5.

Since the FOV and range are interrelated, improvements to the FOV should be accompanied by improved range. While a TOF approach is likely to be sufficient for short-range applications, long-range utility is likely to necessitate using a FMCW approach. Therefore, it is believed that the lower cost of the relatively complex FMCW and the higher performance of the relatively simple TOF would be important to the initial segmentation of the LiDAR market.

Future outlooks

In order to anticipate the future technology evolution of LiDAR, it is necessary to look into relevant prior technologies such as those pivotal to the development of RADAR and telecommunications (Telecoms) applications. Radar has almost the same purpose as LiDAR, and has undergone technological evolution over 100 years. Telecom also uses optical devices and module technology that are common to LiDAR, and has undergone evolution over 50 years. Fig. 6 concisely summarizes the major evolutionary paths of RADAR and Telecom. RADAR started in the early 20th century using a TOF approach, and has evolved into utilizing a FMCW scheme because of the challenges of high-power RF amplifiers. FMCW RADAR influenced the development of Telecom technologies in the 1970s; interest in a FMCW-like coherent scheme was high.

However, due to the emergence of optoelectronic based systems and well-known optical fiber amplifiers, the telecommunications market has been dominated by TOF-like intensity schemes since the 1990s. Beginning in the 2010s when more performance improvement was needed, a coherent scheme was revisited for telecom/datacom applications, and now it coexists with the intensity scheme. One important implication of this evolutionary history is that the amplifier technology has had a significant impact on the evolutionary direction of these devices and timing for development leading to market introduction, which is likely to repeat in the evolution of LiDAR technologies. That is, the timing of the TOF-FMCW transition might be determined according to the degree of success of the SOA-based distributed optical amplification technology as described in this article.

Attention is focused on how this technological uncertainty will affect the commercialization of LiDAR technology in the coming years.

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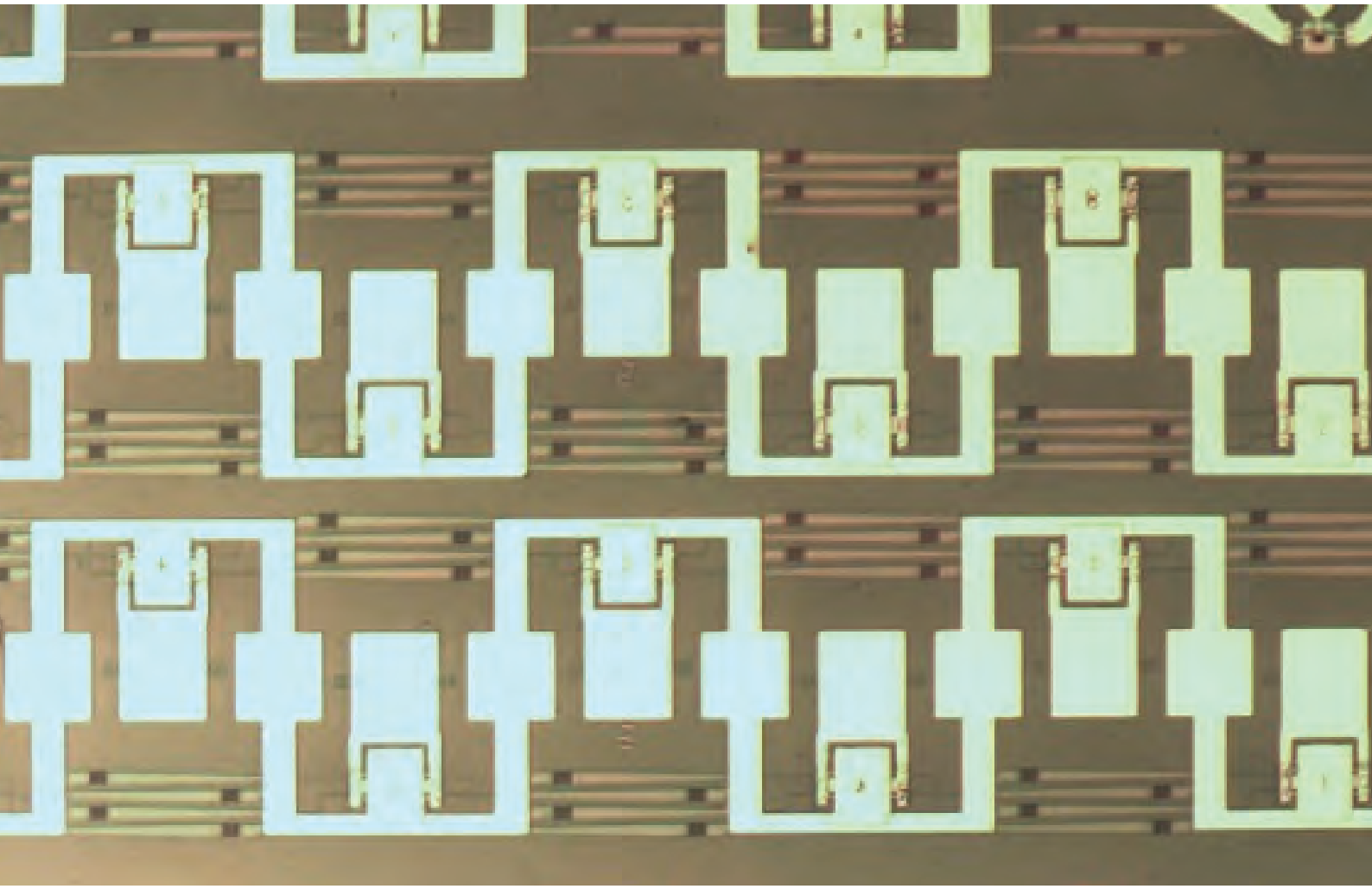


Integrated photonics design success is built on a software foundation

PIC MAGAZINE SPOKE WITH LUCEDA PHOTONICS to explore what sets the company's approach to design automation apart from other software being used to create next-generation photonic integrated circuits (PICs). What began as a collaborative effort between Ghent University and imec researchers to support the design of large IC masks in 2002 has expanded to become a global system to speed PIC design cycle times, eliminate errors and simulate performance without costly prototyping.

PHOTONIC INTEGRATION is already bringing the benefits of light-speed data transfer to industries such as datacom and telecom, with new generations of PICs being created for applications that run the gamut from automotive to biomedical to quantum computing and AI.

While electronic design automation (EDA) today speeds PIC design, available programmes differ greatly in power and scope; platform choices often come down to designer preference or a company-wide commitment to particular software platforms.

Luceda Photonics developed an environment called IPKISS that allows companies and researchers to use software-development best practices in photonics circuit design. This approach is seen as a means to improve design flows, allow for more automation, engender better teamwork and save companies and researchers from needless time-crunches right before a deadline.

While all designers appreciate that 'EDA' stands for electronic design automation, in practice the automation part of the acronym is often forgotten, remarked Luceda Photonics co-founder, Martin Fiers. Working with a global customer base has shown Fiers that at many companies, manual processes still dominate photonic design workflows, and coordination within teams can be a challenge. This is why Luceda Photonics first built its IPKISS software 15 years ago, a system today that is used by research groups and universities globally as well as manufacturers and fabless photonic design companies of all sizes.

An essential quality that distinguishes IPKISS from other design software suites is that users build circuits in a code-based environment instead of a graphical interface based approach favored by others that typically rely on linking blocks to manually construct circuit layouts. Using IPKISS, designers instead write scripts that generate designs of photonic integrated circuits. IPKISS essentially replaces point-and-click software with lines of code. This process allows designers to take best practices and techniques from software development, such as version control, continuous integration and continuous delivery (CI/CD), and apply them to photonics. "We use code as a source of truth instead of binary data which is typically done today in CAD/EDA environments. Binary data is hard to manage since large file sizes make it difficult to share and as design versions and iterations grow, the data is hard to compare and store. On the other hand, code is human readable, easy to compare and is easier to collaborate on and share," stated Fiers.

As Fiers further explained, the use of code became the company's 'go-to' solution since it was based on the time-tested engineering concept that duplicating information in the design process is dangerous to achieving the goal of an error-free design because at some point a designer will make an error, such as copy-pasting the wrong component, or forgetting to modify a parameter in one place. But in IPKISS, the designer can define parametric cells (PCells) where all design information is integrated into one place. IPKISS then handles the transition between the different steps within a design flow, making sure that the necessary information is available and correct.

Advantages of code-driven design

- **Version control:** better knowledge sharing, teamwork and product quality.
- **Practical automation:** remove all manual steps in a design workflow that can be error-prone and time-consuming to reproduce manually.
- **Continuous integration / Continuous delivery (CI/CD):** better time management and predictability

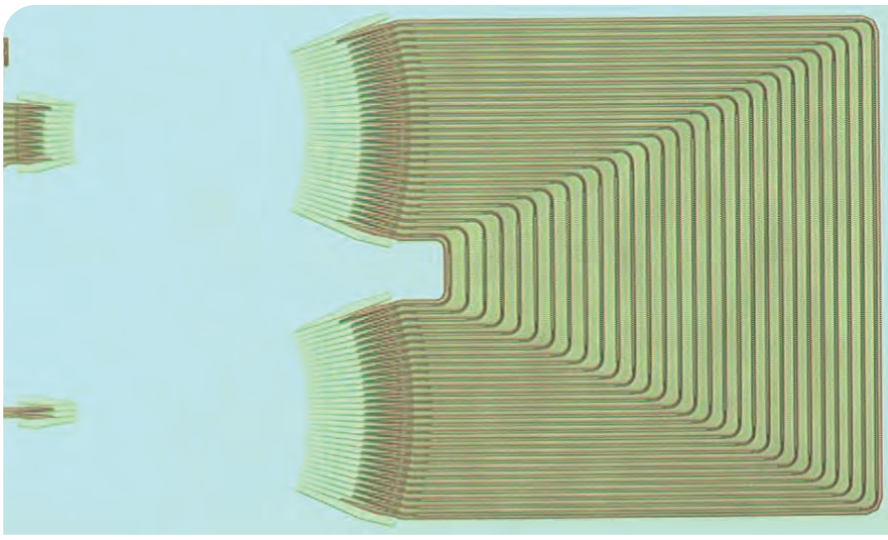
Version control & teamwork

Luceda Photonics believes its code-based approach also has advantages in terms of teamwork; primarily in that code allows circuit design to benefit from version-control systems typically used in software-development. The most commonly used system is called 'Git,' which is accessed through collaboration platforms such as GitHub, GitLab or Bitbucket. Git provides version control and an efficient approach to branching and merging histories of changes. A collaboration platform adds key features: issues tracking, pull requests (code review before merging), release management and automation (CI/CD). Together they enable teamwork.

Issue tracking is used to communicate about tasks to be done. Each designer has her/his own Git repository to work with. The designer makes changes to the code base, committing each of them to a branch. When ready, the designer opens a pull request on the collaboration platform. In a pull review, participants can then read the proposed changes, verify them, propose corrections and enhancements. This process spreads knowledge and promotes strong interactions within the team. "People can learn from others and show what they are doing", says Sébastien Lardenois, Team Lead, imec Silicon Photonics Devices. "It brings teamwork into the design phase. Instead of just sharing workspace with design team members, you really work and collaborate on the same project. At the same time, you're building re-usable knowledge. Code from previous projects can be used as starting point for a new one. It's also a great tool for training new team-members."

Lardenois explained some additional advantages of a code based approach include reducing the time to go through a design cycle since repeating tasks are easier to capture, and that redoing a design becomes a matter of changing a value within the code, which is as easy as pressing a button.

"The idea is to reduce errors, improve reproducibility and avoid expensive re-spins," he said. "Imagine having a system in which you can change the



position of a device on a chip, rebuild sections or rebuild an entire mask that needs to be taped-out and also check for DRC errors, rerun circuit simulations, change the geometry of a device and then rerun the full physical simulation. The designer can also rebuild compact models based on the resulting data and validate new models. All this is possible using a code-driven design flow," Lardenois said.

Isn't using a GUI easier than coding?

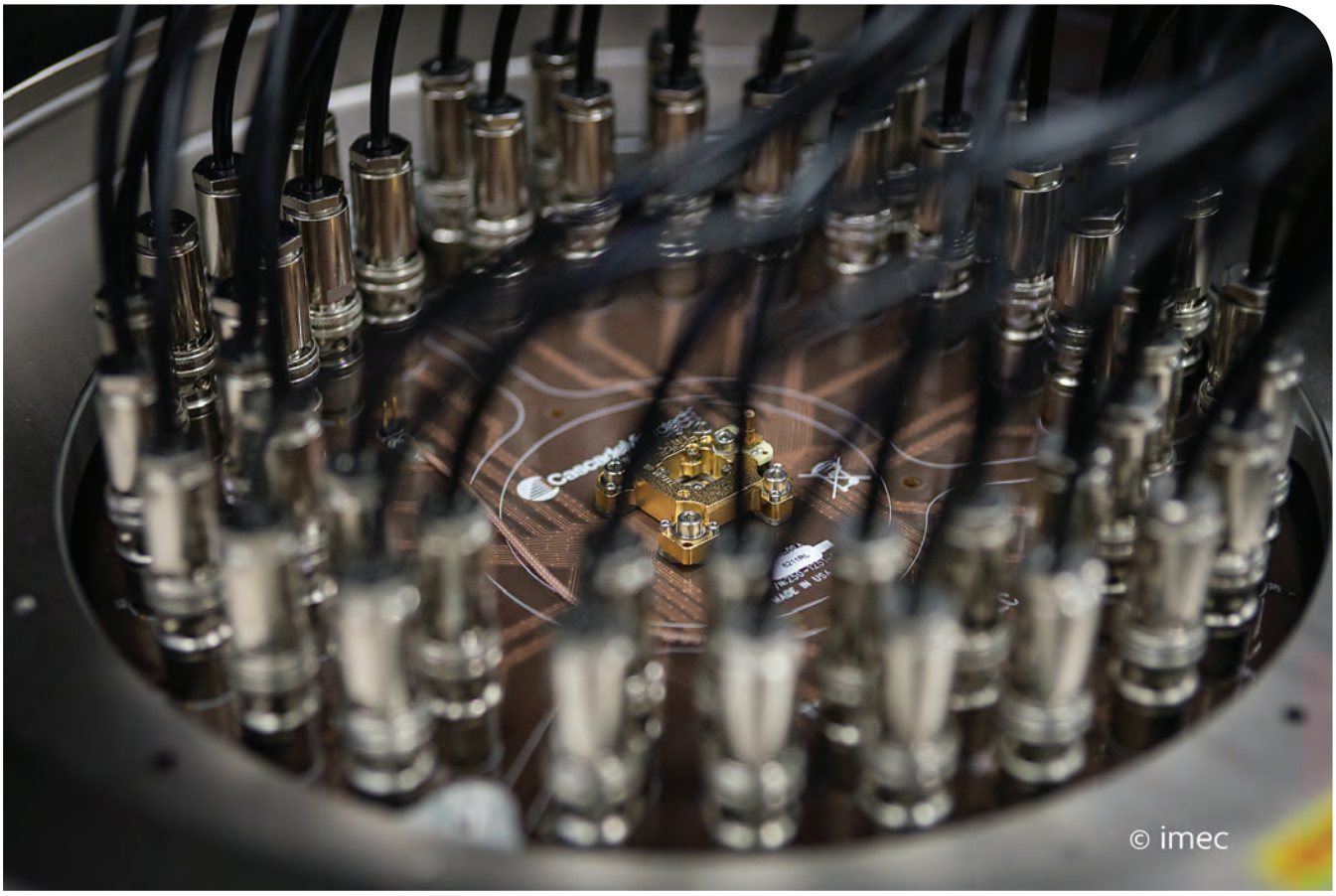
Using a visual approach is easier to a degree, but it also has downsides, remarked Fiers, offering a common issue they see in different approaches to EDA as an example. "GUI based design makes it harder to reuse parts of the drawing and keep track of why designers made certain choices. In a code-first approach, on the other hand, designers can easily re-use elements from previous design runs and automate sub-tasks by scripting. This can lead to large productivity boosts," Fiers said. Coding enables designs from previous projects to serve as the building blocks of subsequent projects. Designs that are common to multiple projects can be stored into separate libraries, which are also version controlled. This library-centric approach, where designs are reused throughout different projects, is a key component of IPKISS. "Knowledge that is built up in one design project easily propagates to other projects through the use of design libraries, including improvements and bug fixes," Fiers said.

Once version-controlled libraries and designs are in place within IPKISS, users can start to automate the design process, which saves time, creates efficiencies and reduces errors.

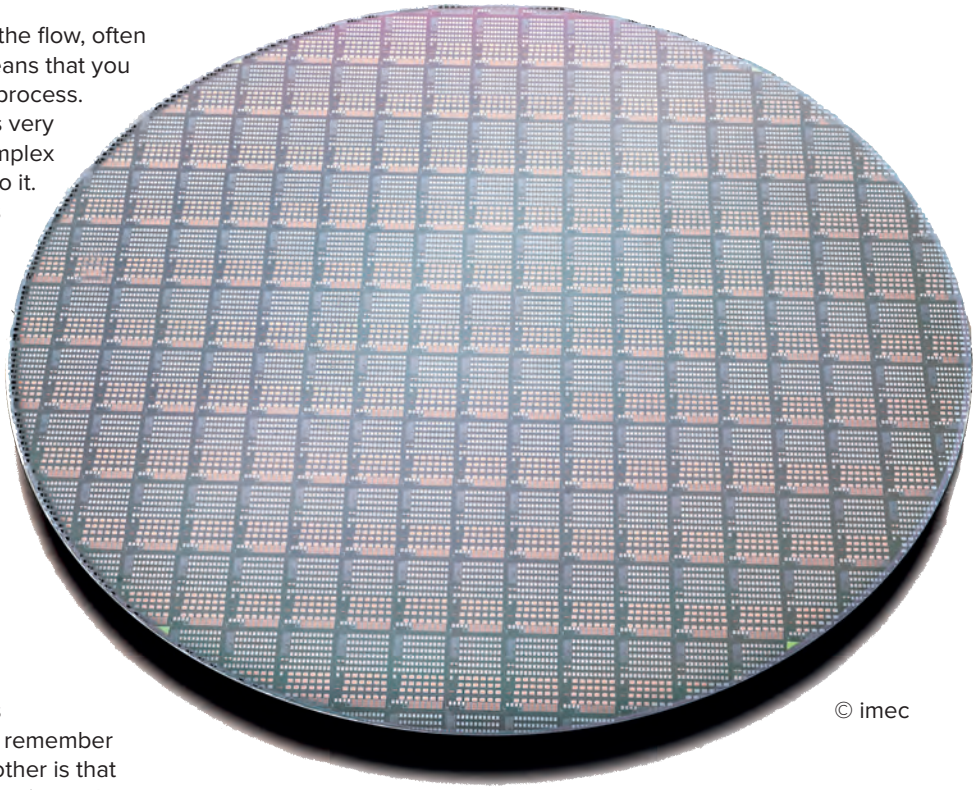
Practical automation

In a typical design project, there are many subtasks that can be automated. Instead of manually repeating certain steps over and over again, automation scripts help to improve reproducibility, save time, and internalize the knowledge of the design. IPKISS is written in Python, the programming language of choice across engineering and scientific communities that makes it relatively easy to create scripts designed to automate certain subtasks. Another benefit of programming based design is a quality common to software development: continuous integration / continuous delivery (CI/CD). In the context of PIC design, this means to continuously and automatically verifying designs. This includes very basic checks, like seeing whether the syntax of the code is correct. But it also means that the circuits themselves can be regularly verified. The physical verification, like DRC and LVS, can happen every time a change is made.

The CI/CD advantage is an important key for imec. "By placing the verification early in the flow you flatten the effort needed for a release," said Lardenois. "You avoid a peak at the end of a project. If you need to do verification manually, you typically



defer the verification to the end of the flow, often at the moment of tape-out. This means that you only see problems very late in the process. But at that point making changes is very expensive because you have a complex object to modify and little time to do it. Continuous verification also carries project management advantages. "You know where you are in the design process," said Lardenois, "Your project is in a known state, which facilitates predictions of when you will be ready."



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Learning curve

Any new type of work process has its challenges. Fiers acknowledged that switching to a script-based design flow has a steeper learning curve, and teams will need to adopt skills like coding and using Git.

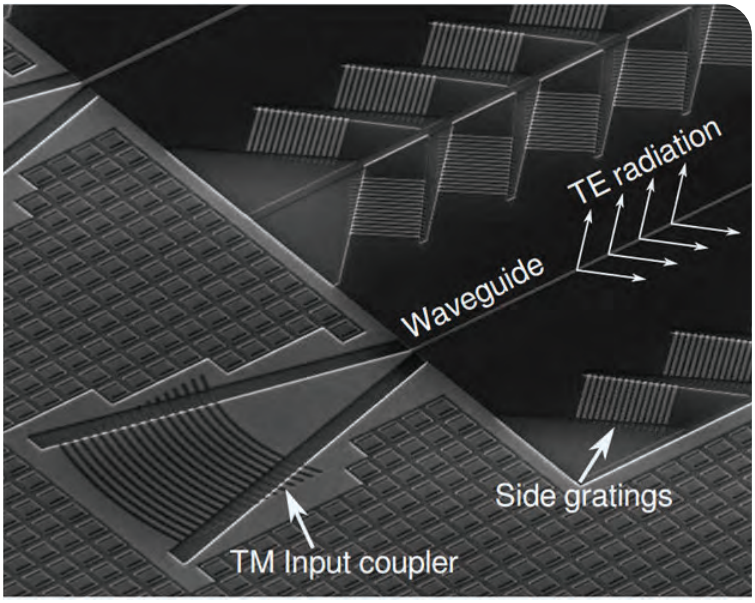
"This seems like a big step, but it is manageable. An important thing to remember if switching from one system to another is that you can do this step-by-step. You don't need to implement a full flow before you see benefits. You can start small, for example by introducing a version-control system and start using code-review between team members. Over time, based on your learnings, you can then introduce new concepts such as automated tests, mask post-processing, and verification, all the way until a real tape-out."

An important aspect of choosing Luceda Photonics is the company's concerted dedication to working with customers to achieve full value from their design investment.

"Customers of Luceda Photonics are never alone in transitioning to our software; we work with our customers to improve their user experience. We provide guidance in many ways. For customers entering the world of photonics, some of whom may be coming from free-space optics, they come to us seeking guidance to navigate the photonics world. We help them get to know all the aspects of IPKISS including setting up their design projects in the best way possible. We provide onboarding trainings for free to every customer. In addition we often have extra support meetings or training meetings with customers when a need arises. Our support channel is complimentary with the software license and we are very proud to provide continuous support to our customers," Fiers remarked.

Productivity and predictability

When correctly implemented, a software-based approach for designing PICs saves large amounts of time and resources. The photonics industry is undeniably maturing. This means that while time-to-market remains important, PIC design managers also need to consider time-to-market-share, which is getting more important. While a design team's genius and innovative capacities may bring a product first to market, it is the design flow that will make any design sustainable with results that are also readily repeatable. Design platforms like Luceda's IPKISS enable knowledge sharing, team learning, and automation through the use of validated building blocks. The design flow is kept transparent through continuous integration and delivery, qualities that can help guarantee long-term design success.



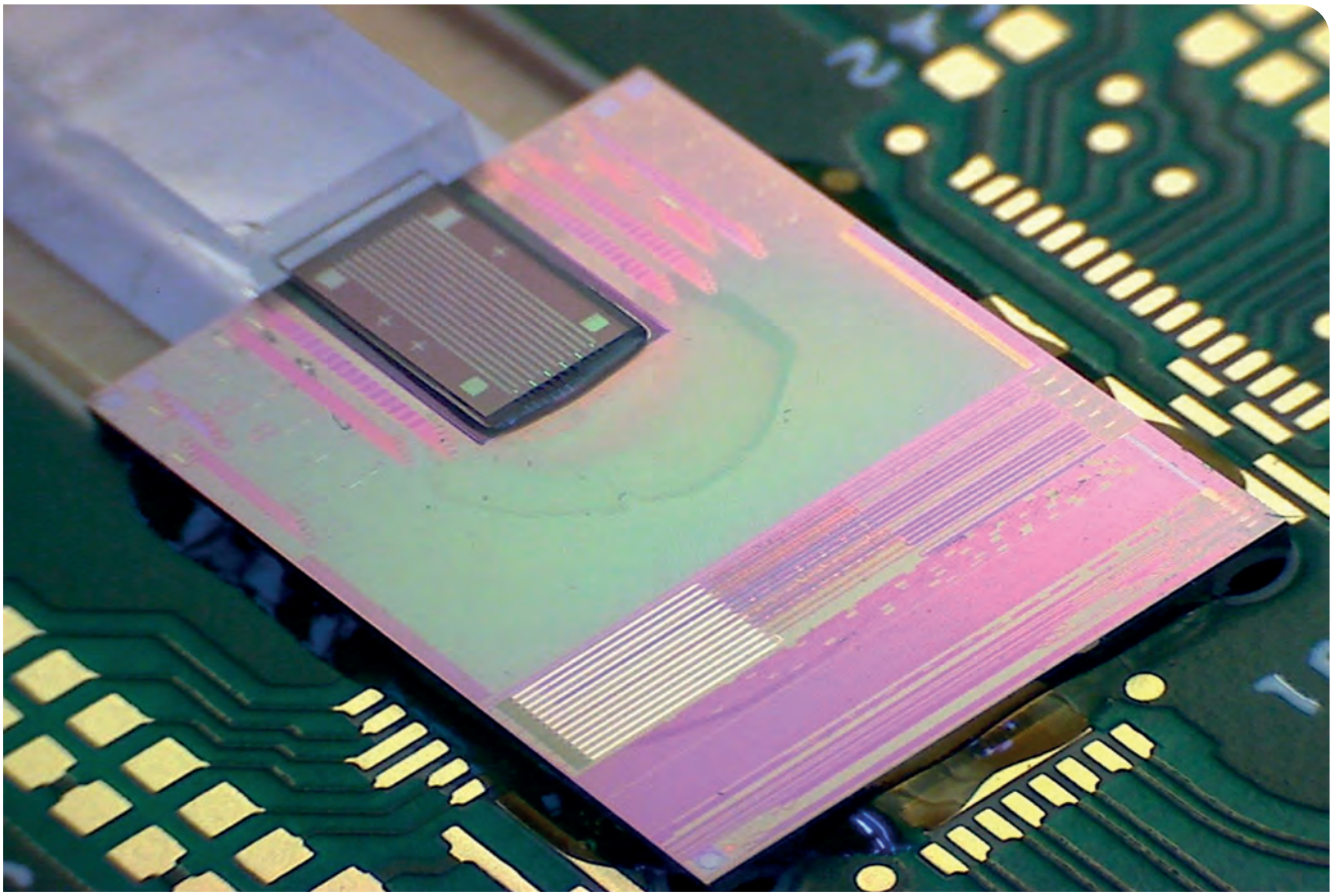
Hybrid integration using electro-optical circuit boards

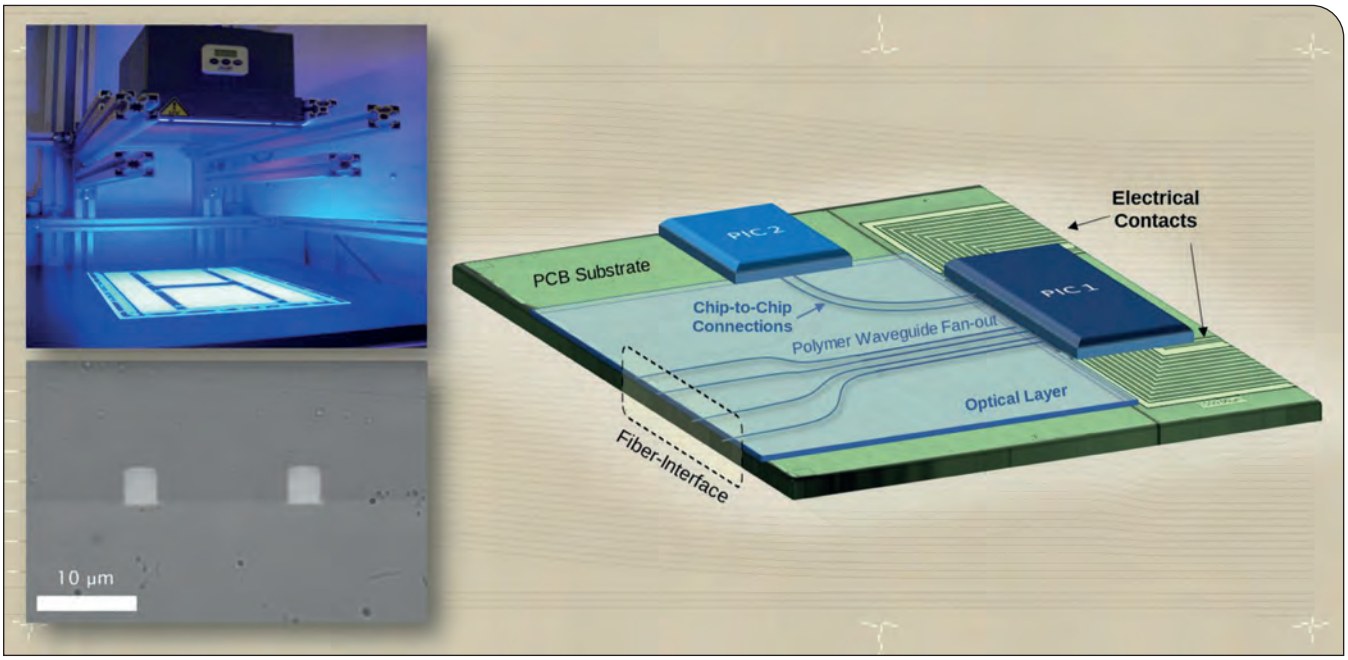
Hybrid integration methods are gaining attention as PIC technologies are advancing and requiring sophisticated packaging solutions. Electro-optical circuit boards, developed by vario-optics ag, represent a promising platform able to overcome the limitations of traditional packaging approaches.

BY NIKOLAUS FLÖRY FROM VARIO-OPTICS AG

PHOTONIC INTEGRATED CIRCUITS (PICs) have tremendously matured over the last decade and found use in a multitude of devices. Photonic chips based on silicon photonic technologies, for example, have expanded their use-case from being employed in transceivers to several other applications, such as photonic computing, optical interconnects and even consumer applications, according to the latest market reports *(www.yole.fr/Silicon_Photonics_Market_Update_2021.aspx)*.

These advancements are not only spurred by extensive research efforts and the addition of new functionalities to the major platforms themselves - silicon-on-insulator (SOI), silicon nitride (SiN) and indium phosphide (InP) - but also by developments





➤ Electro-optical circuit board platform based on polymer photonics. Optical layers containing planar singlemode waveguides are processed via UV-photolithography and integrated with standard PCB technology. The EOCB platform provides solutions for (electrical & optical) PIC-coupling, fan-outs to standard fiber-interfaces as well as on-board PIC-to-PIC connections.

on other material platforms and technologies, such as thin film lithium niobate on insulator (LNOI), polymer photonics and plasmonics.

Still, to date, no single platform alone provides all components and functionalities, which are necessary in a typical PIC application such as a complete high-speed transceiver module. SiN exhibits low propagation loss and allows wafer level packaging, but lacks any intrinsic active device functions – such as modulators, photodetectors and most importantly lasers, which is also the major missing building block on the SOI platform.

InP on the other hand is an excellent material for integrating laser sources on-chip, but exhibits larger propagation loss and is thus not too suitable for passive devices and large-scale integration.

As a consequence, extensive efforts have been made on developing scalable integration technologies, which enables leveraging the benefits of multiple platforms, combined and tightly packaged together in one module.

The importance of integration platforms

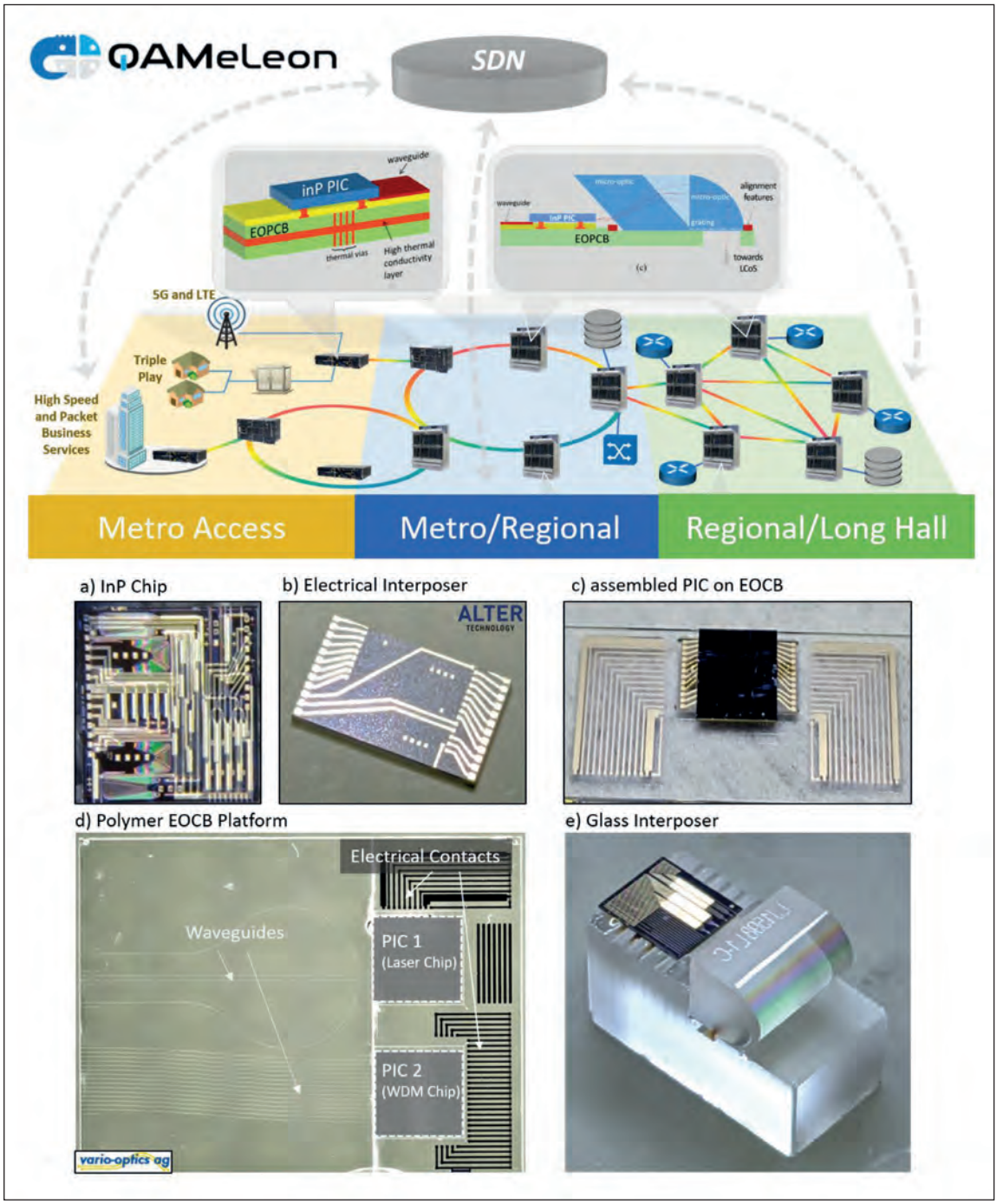
The technologies and methods for the combined integration of different PICs can be roughly divided into two branches. On the one hand, additional efforts in the front- and back-end (e.g. micro-transfer printing, direct epitaxial growth) lead to heterogeneously integrated chips. On the other hand, advanced packaging methods such as micro-packaging or on-board co-integration of different chips results in hybrid integrated modules and chiplets.

While the former wafer-scale integration methods hold great promises for low-cost, efficient integration of several chips, the resulting heterogeneous PIC still needs to be packaged – an issue, which has risen in awareness over the last couple of years. As of now, the efficient packaging of PICs still resembles a bottleneck in many applications and has thus become an integral part in any system development involving PICs. This holds true in particular as the complexity of chips is advancing, the number of optical I/Os is increasing and the electrical requirements are getting tighter as well (e.g. high-speed RF interfaces or high-density electrical traces.)

In order to overcome the challenges associated with the packaging of PICs, hybrid integration methods are offering significant advantages. They not only allow to combine and connect different PICs together in one module, but at the same time already tackle the issue of packaging, thereby solving two problems at a time. In the following, electro-optical circuit boards (EOCBs) are introduced as an attractive solution to hybrid integration and several technological features relevant for advanced PIC packaging are discussed.

Electro-Optical circuit boards

An EOCB, simply put, is a board featuring both an electric interface (PCB) as well as on-board optical connections (waveguides), which renders it a prime platform for hybrid integration [1].



➤ The Horizon 2020 funded QAMeleon project aims on developing novel scalable transceiver and switches based on a common EOCB platform. a) InP chips and b) electrical interposer used to mounting on a c) glass host-board. d) The EOCB integration approach allows to assemble several chips on one common EOCB, as well as to add micro-optical components (e). The assembly was performed by Alter Technology TÜV NORD UK Ltd

As for the electrical part, standard PCB technology is used, which allows including features such as high-speed RF interfaces, (glass) interposers, thermal dissipation layers and vias. Optical on-board connections are created by including polymer or glass based planar waveguides to the board. In the case of polymer, they can be directly manufactured on-board, using the PCB or glass as a substrate. As polymer waveguides have advanced, they can now be operated in singlemode at most common (telecommunication) wavelengths and moreover provide solid environmental stability and high power thresholds. Since the dimensions of the cores can be freely adapted and optimized, any passive in-plane device functionality is possible, such as directional couplers or multimode-interference couplers, and as a result of the rectangular cross-section, polymer waveguides maintain polarization.

In the case of glass waveguides, the photonic layers can be fabricated separately and laminated with the PCB later on. In both cases, the resulting EOCBs can be designed precisely for the specific requirements of a photonic application, taking into account electrical, optical and thermal considerations, before being equipped with PICs as well as purely electronic components.

The possibility of having one common host board for both the electrical and optical interface is a

significant advantage over other integration methods; however, they are often not considered. Most PIC packaging efforts only focus on an efficient optical coupling interface. While this is of course a central motivation and requirement in a majority of use-cases, thermomechanical and electrical requirements are often hard to meet this way. The operation of high-power laser chips and high-speed modulators, for example, make it necessary to handle the heat as well as to provide RF above 100 GHz. EOCBs can handle and fulfill both these needs.

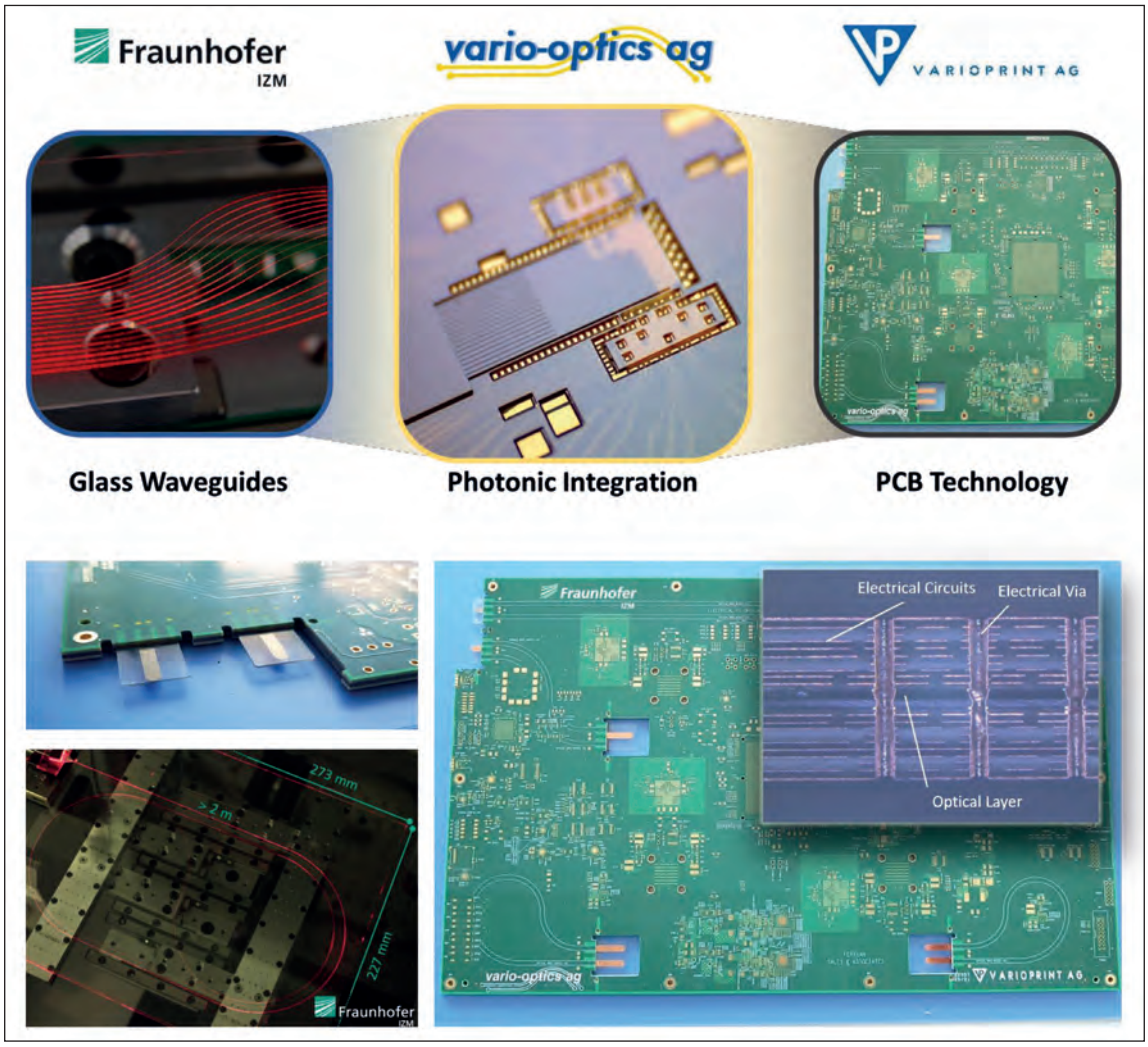
Novel transceiver architectures – QAMeleon project

A perfect example of using this technology for the development of novel transceiver architectures is the Horizon2020 funded project "QAMeleon" [2]. Within this R&D project, novel transceivers and wavelength-selective switch devices are developed, based on InP components and free-space micro-optical elements. The scalability of transceiver and switching technologies plays a key role in the development of future architectures for data-center interconnects (DCIs), as data centers are pushed to their limits due to the ever-increasing demand for bandwidth. Thus, the components developed within QAMeleon are combined and integrated on an EOCB, which is based on a glass substrate featuring metallizations as well as mechanical features for the alignment of the optical and electrical components. Planar polymer waveguides in the top layer of the board are used to couple light in and out of the InP laser and WDM chips. In contrast to bulky fiber-coupling arrangements, the EOCB platform easily allows the scale-up to many parallel optical channels - 18 inputs/outputs (I/Os) - and to match the narrow pitch of the optical I/Os on InP (e.g. ~30 µm), a key-requirement for multi-port chips.

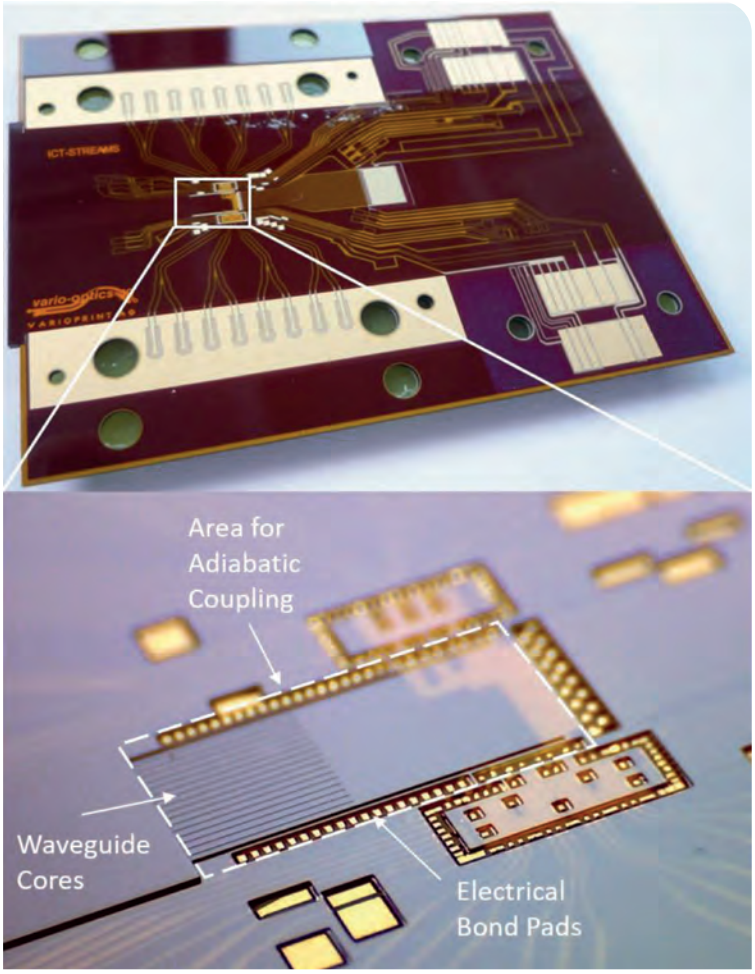
Glass-Integration into PCB

Apart from its use as an interposer, glass can also be employed as the waveguiding layer itself [3]. Through a process based on ion-exchange, developed by Fraunhofer IZM, gradient index waveguides are created in thin glass. These embedded waveguides exhibit low-loss singlemode operation and can be manufactured on large panel sizes of up to 457 mm x 303 mm.

Together with its partner Varioprint, an advanced PCB manufacturing company, vario-optics has developed a lamination process to integrate such



➤ Glass-based EOCBs. Together with Fraunhofer IZM and Varioprint AG, vario-optics has developed an integration process to embedd glass waveguide panels into a PCB.



➤ Fig5: Adiabatic coupling interface on an EOCB. Singlemode polymer waveguides and electrical bond pads are manufactured close by to allow simultaneous electrical and optical coupling via a flip-chip bonding process.

FURTHER READING

➤ [1] N. Flöry et al., "Highly reliable polymer waveguide platform for multi-port photonic chip-packaging," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 1689-1694, doi: 10.1109/ECTC32696.2021.00267.

➤ [2] C. Zervos et al., "A new generation of high-speed electro-optical transceivers and flexible bandwidth wavelength selective switches for coherent DCI: the QAMeleon project approach," Proc. SPIE 10924, Optical Interconnects XIX, 109240E, 2019; https://doi.org/10.1117/12.2509454

➤ [3] H. Schröder et al., «Low-loss optical single-mode waveguide platform in thin glass with wide spectral range», Proc. SPIE 12007, Optical Interconnects XXII, 120070D, 2022; https://doi.org/10.1117/12.2611775

➤ [4] T. Lamprecht, et al., "Electronic-photonic board as an integration platform for Tb/s multi-chip optical communication." IET Optoelectronics, 2021, 15: 92-101. https://doi.org/10.1049/ote2.12017

glass panels into electrical PCBs, similar to what has been achieved with polymer waveguides in optical backplanes. The reliability of the glass lamination process is verified by copper metallizations on the glass layer, which can be used for conductance measurements after the integration, thus facilitating the process control. Optical interfaces to the glass layer are made by cut-outs in the PCB and CO_2 laser cutting of the glass. Laser-structuring of the panels also allows the creation of trough-glass vias or mechanical features for embedding optoelectronic components. Overall, due to the low propagation loss at telecommunication wavelengths (< 0.1 dB/cm @ 1550 nm), the addition of glass waveguides into large EOCBs is a promising technology for next generation photonic integration.

PIC coupling to EOCBs

One of the biggest challenges in assembling PICs is their typically small mode field diameter in the range of only roughly 1 µm. Even though the optical properties of polymer waveguides can be adjusted to achieve small mode fields of down to 4 µm, the remaining mismatch makes it favorable to use spot-size converters on the PIC side as well. Nevertheless, the assembly process of a PIC relying on conventional butt-coupling requires sub-micron precision accuracy.

While active alignment processes become easier (and cheaper) over time, this is still a limiting factor in the high-volume production of PIC devices. EOCB offer the additional possibility of including precise mechanical alignment structures (e.g. in glass) on the host board, which can drastically facilitate the assembly process.

Another alternative approach to the assembly is to rely on an adiabatic, evanescent coupling interface. In this coupling scheme, inverse-tapered waveguides on the PIC are used to couple light to exposed polymer waveguide cores, and vice versa. In contrast to grating couplers, this approach provides not only relaxed lateral assembly tolerances (approximately +/- 2 µm), but also efficient coupling over a broad wavelength range for both TE and TM polarization [4].

Outlook

As PIC technologies are advancing, the focus is shifting from device-performance only to complete system aspects. Hybrid integration plays a key role in this development, and it is about time that additional efforts are put into the packaging aspects of PIC technologies by academic institutions but also industrial players.

In the end, what is true for the individual PIC platforms themselves also holds for the various integration options: as of now, each approach offers certain benefits and lacks some features, so most probably we will see a combination of them in future applications.

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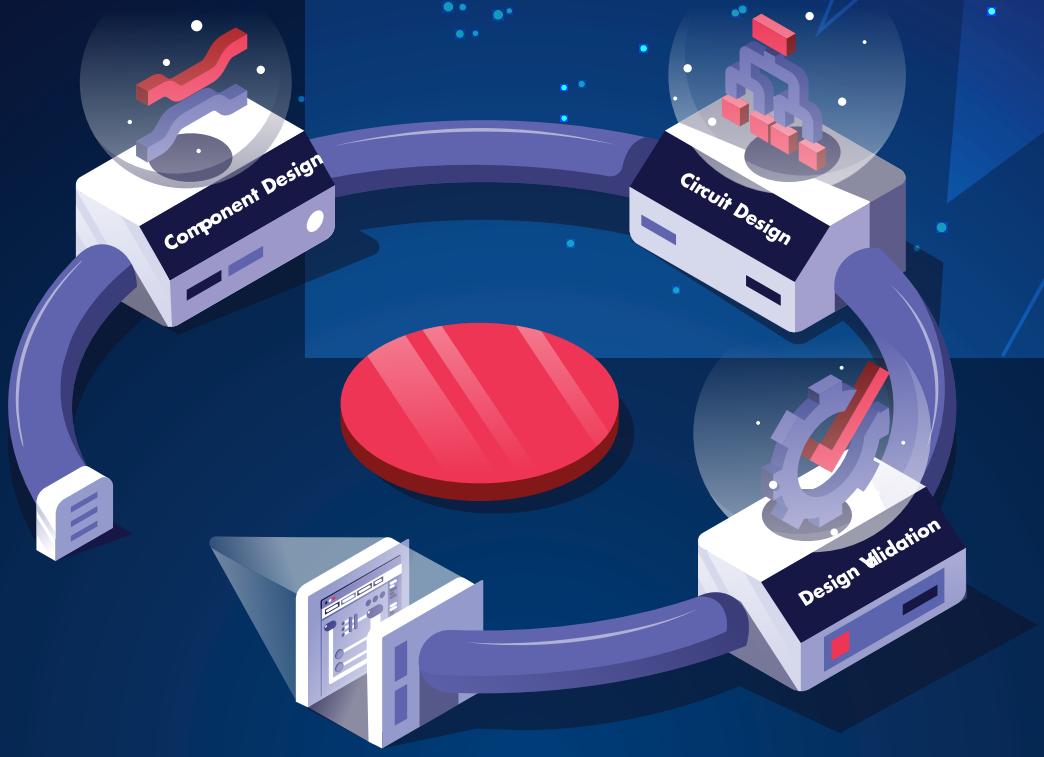

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Beyond communication, silicon photonics is penetrating consumer and automotive applications

The strong pull from communications opportunities has allowed the photonics industry to look at adjacent applications that will benefit from the advantages of silicon photonics and photonic integrated circuits. LiDAR in automotive applications is becoming one of the more exciting adjacent applications for photonics as that industry evolves toward more autonomous content and capability.

BY ERIC HIGHAM, DIRECTOR – ADVANCED SEMICONDUCTOR APPLICATIONS/ADVANCED DEFENSE APPLICATIONS, STRATEGY ANALYTICS

AS GLOBAL ECONOMIES continue to recover from COVID and the pace of events around the world quickens, the importance of broadband connectivity is clear. Countries are expanding their broadband footprints and users are clamoring for higher data rates to accommodate their growing video and application appetites. The result has been an explosion of data traffic over the past decade. The curves in Figure 1 show an extrapolation of Cisco network data for the next decade and the conclusion is inescapable; data traffic is large and growing quickly.

The red curve shows IP (Internet Protocol) data traffic and this represents any bit of transmitted data, whether that data is on a wireless or wireline network. This data extrapolation predicts traffic to increase by a factor of 125 times over the forecast period. Even more impressive is the magnitude of data shown by the blue line. This curve represents expected data traffic in data centers. This short-

reach data traffic runs between five and six times the magnitude of the IP data and it reflects the increasing importance of data communications as we have become more comfortable with the cloud and the home becomes the center of many of our interactions with the world.

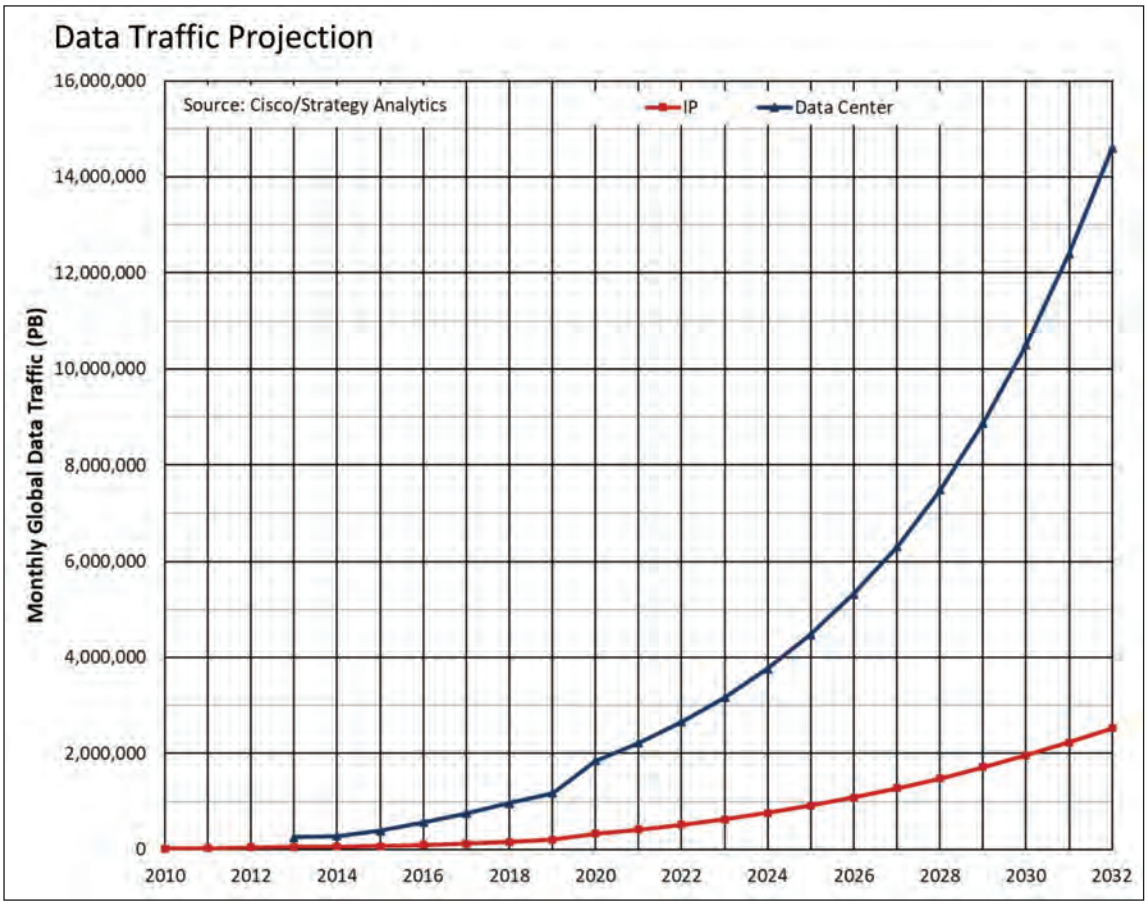
The magnitude of this communications activity is becoming clearer. The emerging 5G wireless standard will drive the entire electronics market with cellular terminals exceeding 1 billion units. There are reports of total optical transceiver shipments reaching 1 billion in the next 5 years and yearly data center port shipments exceeding 60 million in the next couple of years.

This communications opportunity, along with the technical requirements have been instrumental in the development and maturation of silicon photonics and the broader photonics integrated circuits (PIC) ecosystem. While communications opportunities currently drive the optical market, the industry is looking at other fast growth, high volume applications that could benefit from more optical content in devices and networks.

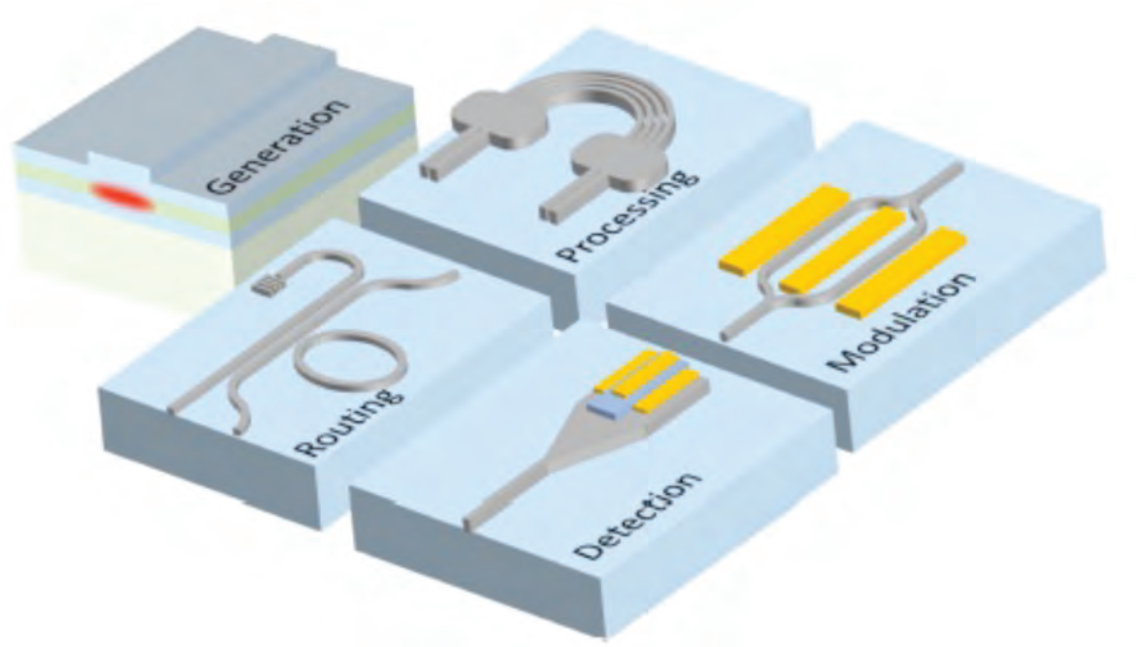
Silicon Photonics

Photonics devices face the same pressures as electronic devices to be smaller and less expensive, with better performance to enable more capabilities. The response to these challenges from optical component manufactures has been more integration. Photonic integrated circuit design and manufacturing techniques have gained traction as the component roadmap evolves to include more electrical and optical functions in an optical module. These modules are a mix of direct and coherent detection schemes and that means a variety of compound semiconductors to optimize the linear functions, along with an increasing amount of digital silicon to increase performance characteristics.

Figure 2 shows a conceptual block diagram of the functions that a photonic integrated circuit must address. As digital processing and control capabilities become more important in optical applications, silicon becomes the natural choice for an integration medium. This allows for relatively low volume opportunities to take advantage of the massive processing and manufacturing infrastructure in place for silicon technologies. Manufacturers are using existing silicon CMOS-based processes for all the functions shown in Figure 2, except for the generation function. Silicon is an indirect bandgap material, so it will not emit photons meaning that the generation function requires another technology. The silicon photonics device becomes a subset of a photonics integrated circuit, with a silicon integrated circuit accomplishing all the required functions except for the laser.



➤ Figure 1: Data Traffic Projection



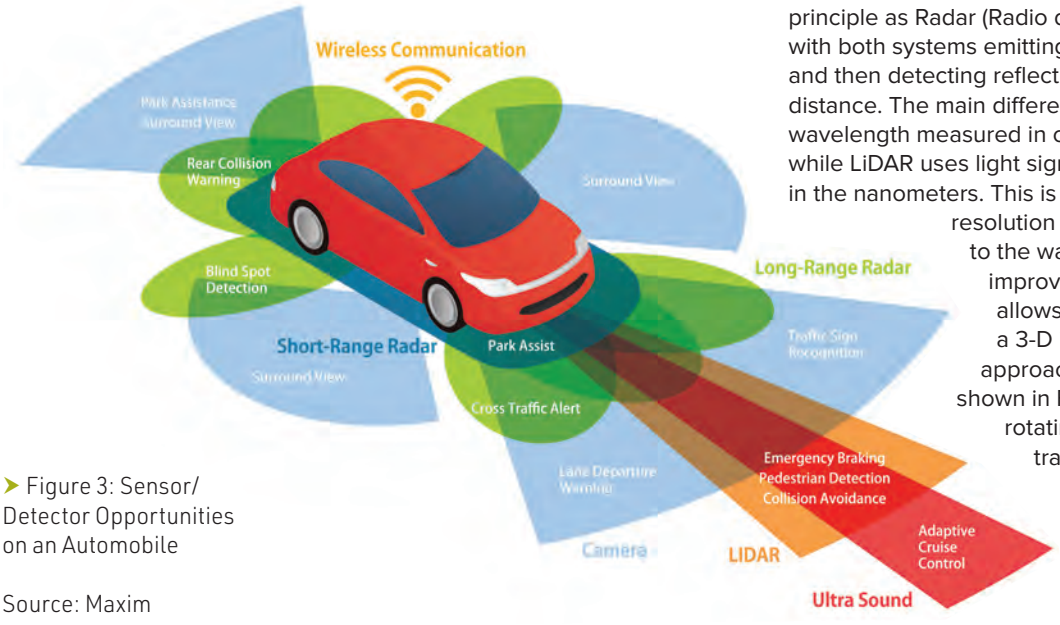
➤ Figure 2: Photonic Integrated Circuit Conceptual Block Diagram

Source: S. Y. Siew, et al, Review of Silicon Photonics Technology and Platform Development, Journal of Lightwave Technology, 2021

New Market Applications

Broadly, the optical industry is becoming extremely excited about the potential in sensing applications. Automotive platforms are generating significant interest as that industry evolves toward more electric vehicles, more sophisticated ADAS (Advanced Driver Assistance Systems) capabilities and full autonomation. After being hard hit by COVID, the automotive industry is trending toward global sales of 100 million vehicles per year and as Figure 3 shows, sensing and detection opportunities in automobiles are increasing and becoming very sophisticated. Vehicle platforms of assorted sizes and purposes are becoming webs of sensor inputs.

The term “sensor” encompasses many distinct functions and technologies. Sensors became increasingly important in automotive applications as vehicles began to incorporate more computerized functions. As semiconductor detection and processing capabilities have improved, the scope of driver assistance has increased. A thorough discussion of the full range of sensor applications and technologies is outside the scope of this discussion, but most vehicles sold today use a combination of cameras, ultrasonic sensors and radar at different frequencies to enable features like adaptive cruise control, parking assistance, automatic emergency braking, and blind spot monitoring. These technologies have advantages and disadvantages and the photonics industry is particularly interested in building on early successes with LiDAR systems to help enable the automotive industry’s evolution to full automation.



➤ Figure 3: Sensor/ Detector Opportunities on an Automobile

Source: Maxim

LiDAR (Light Detection And Ranging) uses the same principle as Radar (Radio detection and ranging), with both systems emitting an electronic signal and then detecting reflections from objects in the distance. The main difference is a radar signal has a wavelength measured in centimeters, or millimeters, while LiDAR uses light signals with wavelengths in the nanometers. This is important because the resolution of either system is related to the wavelength. The resulting improvement in resolution allows LiDAR systems to map a 3-D image that begins to approach the actual image as shown in Figure 4. By using a rotating transceiver, or multiple transceivers strategically located, the system can create a 360-degree, 3-D image of the vehicle’s surroundings. Of course, there are

challenges to LiDAR technology and this is where the silicon photonics industry believes it can add value.

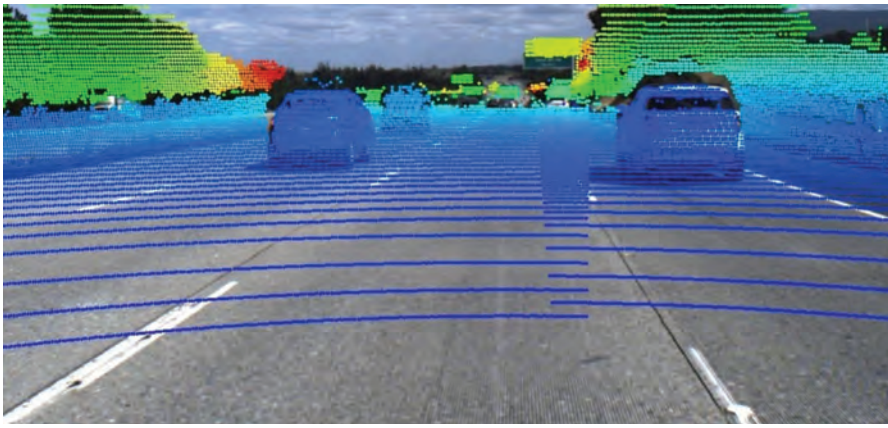
The first challenge is the appropriate system wavelength. The reflected photons received by the LiDAR system must compete with the ambient lighting to be identified as a signal. Solar irradiance in the 850nm-940nm wavelength range is about three times higher than levels at 1500nm, another popular wavelength. This added solar irradiance translates to system noise, but there is substantial development activity at 850nm and this starts to give us insight into the advantage and opportunity for silicon photonics.

The ability to detect that reflected signal depends on the material characteristics of the sensor. Silicon is responsive at wavelengths up to about 1000nm, but detection at longer wavelengths requires a compound semiconductor material. Detectors for LiDAR systems have evolved from PIN diodes to avalanche photodiodes to single photon avalanche diodes (SPAD) and silicon photomultipliers (SiPM), with the latter two methods capable of being fabricated into arrays with more capabilities. Despite the challenge posed by higher solar irradiance, wavelengths that can be detected and processed by silicon semiconductors provide cost and performance advantages.

Earlier, we mentioned achieving 360-degree coverage by rotating a LiDAR system and while early versions use this approach, the goal of LiDAR manufacturers is to develop an array approach to steer light beams in azimuth and elevation. MEMS and mirrors, along with liquid crystal metasurfaces, are array components under development, but the photonics industry is trying to develop an optical phased array (OPA). Like its RF counterparts, the OPA requires a transmit path that includes a chirped or pulsed laser source, isolators, amplifiers, modulators and splitters, along with a receive path including combiners and a detector. Both paths would also need transmission, filtering and other passive structures and that detected signal would undergo substantial processing to generate a detailed rendering like we see in Figure 4.

Except for the laser, all the necessary functional building blocks exist in process design kits (PDK) at silicon foundries currently doing optical work. The need for a discrete laser using a non-silicon technology is a challenge, but emerging silicon photonics opportunities are already embracing and optimizing this impediment. It represents an acceptable concession to access the large and well-capitalized silicon foundry and packaging industry.

Some observers believe that LiDAR deployment has been slowed by technology limitations. Words like clunky and costly are used to explain this slower than hoped adoption. The solution



➤ Figure 4: LiDAR-Generated Point Cloud Representation. Source: JD Power

to these challenges is miniaturizing circuits and footprints through integration and tapping into more cost-effective fabrication and manufacturing technologies. The emerging silicon photonics components industry is addressing all these issues as the ecosystem matures and grows. Those features, coupled with more digital processing power in shrinking silicon nodes makes silicon the likely technology choice to unlock the potential of LiDAR in automotive applications.

LiDAR has also found its way into other commercial applications. Apple includes this feature on a range of its latest devices. The LiDAR feature improves resolution and depth for more lifelike pictures. The capability is becoming important as augmented and virtual reality devices become more popular. LiDAR

MEMs and mirrors, along with liquid crystal metasurfaces are in systems being deployed in systems, but the photonics industry is trying to develop an optical phased array (OPA). Like its RF counterparts, the OPA requires a transmit path that includes a chirped or pulsed laser source, isolators, amplifiers, modulators and splitters, along with a receive path including combiners and a detector

allows spaces to be mapped before 3-D elements are overlaid. Drones and robots use the technology for more accurate mapping and positioning.

On a broader scale, the ability of silicon to detect at wavelengths less than 1000nm (visible and near-infrared spectrum) makes this an excellent choice for biosensors. This opens a whole host of health applications such as glucose monitoring, early detection of cancer or other infectious diseases, with companies currently developing PIC-based biosensors to develop rapid testing for COVID-19. There is discussion of incorporating these capabilities into smart watches to provide medical telemetry data on a real-time basis. Other applications of the biosensor technology include detecting pollutants in the environment and chemical residues and infectious diseases in the food industry.

Conclusions

As consumers and businesses embrace more sophisticated digital capabilities, data traffic is increasing dramatically. Enabling the magnitude of this traffic explosion means that networks and devices are increasingly turning to optical transmission with that technology's enormous bandwidth capability. Like any electronics capability, as quantity and capabilities grow, size, weight, cost and performance become increasingly important.

For the optical market, this has meant a growing dependence on photonic integrated circuits that use multiple technologies and a hybrid assembly approach, along with emerging silicon photonics devices that integrate all the required functions except the laser into silicon CMOS technology. The silicon photonics ecosystem is relatively new, but it is maturing quickly and it taps into the large, established CMOS manufacturing infrastructure. While the silicon photonics solution is new, the communications and connectivity applications are not and the size of these market opportunities is a big growth engine for silicon photonics revenue.

The strong pull from communications opportunities has allowed the photonics industry to look at adjacent applications that will benefit from the advantages of silicon photonics and photonic integrated circuits. LiDAR in automotive applications is becoming one of the more exciting adjacent applications for photonics as that industry evolves toward more autonomous content and capability. Automotive volume is large and while there are still challenges to address, the silicon photonics ecosystem is interested and they are developing compelling solutions to these challenges. This combination of a strong growth engine, along with new and emerging automotive and sensor opportunities underpins our bullish outlook for the photonics market.

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Seamlessly move PIC testing from lab to fab

Automating PIC manufacturing processes including test, assembly and packaging (TAP) are key to increasing product quality as well as dramatically reducing overall production costs. The experts at EXFO detail ways that automation continues to accelerate time to market for PICs while helping reassure customers of consistent quality.

BY FRANÇOIS COUNY, PHD, SENIOR PRODUCT LINE MANAGER AT EXFO

MASS PRODUCTION of photonic components requires fast, flexible, and integrated testing and characterization. And testing constitutes a big chunk of component manufacturers' investment given that an estimated 30 percent of the total cost of photonic chip production is driven by testing.

Recent Photonic Integrated Circuits (PIC) testing advances have helped reduce operating expenses via increased speed, reliability, and scalability. PIC measurement can now be optimized using turn-key solutions – delivered through vendor collaborations -- to perform multiple tasks efficiently with easy reconfiguration. And new technologies are on the horizon to provide even more opportunities to reduce component manufacturing costs.

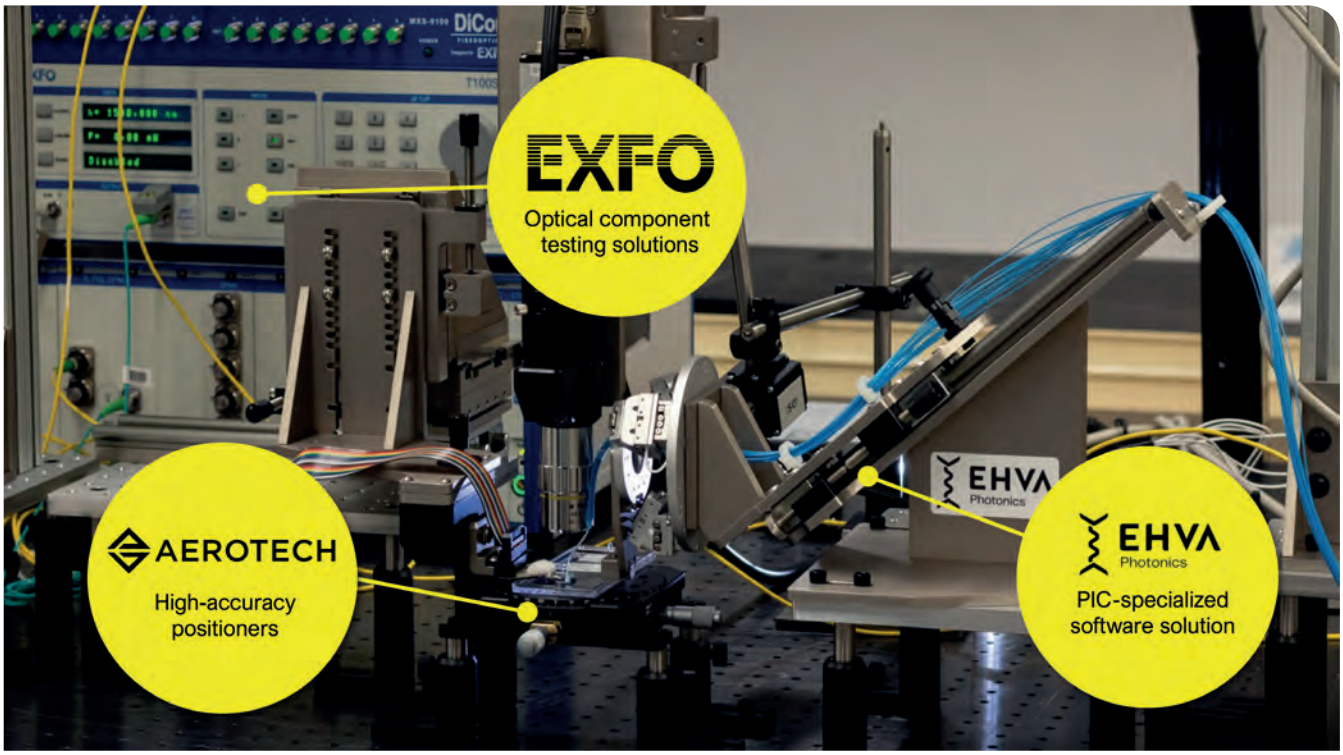
This article looks at the current state of PIC testing, progress made in seamlessly moving PIC testing from the lab to fabrication, and the advancements in laser technology that will reduce the cost and time of testing while maintaining reliability.

Streamlining the PIC testing process

Testing PICs has always been a big challenge over the decades of development in the cleanroom. Often researchers would put together some test instruments and perform the characterization by hand or even design their own dedicated instrument that could also include post-processing and analysis of the results. Over the past few years, test instruments designer EXFO has worked closely with these researchers to create instruments that are fine-tuned to the technical requirements of PIC optical testing.

Moving PIC-based passive component testing into production is often challenging due to the high port count of some components like arrayed waveguide grating (AWG) or the sheer number of components to test on a single die. Since testing requirements are very similar in the lab and in production of these specialized devices, component manufacturers can now use the same component test platforms they used during the development of the product in the factory. The test solution serves as a multiport detection system that operates in conjunction with a continuously tunable laser to measure optical insertion loss, return loss, and polarization-dependent loss across the laser's spectral range. This cost-effective method yields optical spectrum quickly and with a high wavelength resolution down to a picometer level.

➤ EXFO's CTP10 component testing platform can be configured for spectral testing of insertion loss, return loss, or polarization-dependent loss, of optical components such as ring resonators.



One further paradigm when considering testing in production is the need to reduce testing costs and hence reduce testing time. In the case of spectral measurement, the test consists of a laser performing a wavelength sweep and in synchronous detection of optical power onto one or several detectors. How much can be gained in speed comes down to how fast the laser can sweep, how quickly the detector can react to the change in optical power, and how long it takes for the data to become available to the operator.

EXFO's CTP10 is a modular component test platform that characterizes the spectral properties of high port count devices in one single scan with picometer resolution and a 70 dB dynamic range, even at high laser sweep speeds. The CTP10 operates from 1240 to 1680 nm and covers a wide range of test applications, including telecom, waveguide technology and coupling, sensing, and LIDAR.

The CPT10's electronics and internal processor streamline data transfer as well as providing a suite of analysis tools, hence offering a solution that is fast in all aspects of the testing phase. Indeed, precious seconds per die can be gained by using such an integrated solution. On a wafer with several hundreds of dies, that is hours of testing that can be saved by using the CTP10.

The component testing platform can be controlled remotely using SCPI commands, enabling integration as part of an automated PIC testing setup, increasing PIC testing throughput while reducing test time. This is a key solution to measure optical components quickly, reliably, and accurately.

Automation to enable mass component production

When testing hundreds or even thousands of components on a single wafer, optimizing the automation process quickly becomes essential.

This is particularly true because optical functionalities to be tested may vary from device to device or from die to die. As a result, PIC test solutions need to address fast reconfiguration of both software and hardware through the use of optical switches. Additionally, faster single-wavelength tests may also be beneficial at some points in the production process such as fiber alignment or after dicing. These simpler tests also help the overall speed of the test and measurement (T&M) process.

EXFO has addressed these challenges with a two-pronged approach. First, the FTBx series of modules provide the optical testing building blocks for a simple laser + power meter test configuration, with

➤ The CTP10 system can also be used with a matrix switch MXS-9100 for easy reconfiguration of PIC die-level testing as in this demonstration from Aerotech, EHVA, and EXFO

The CPT10's electronics and internal processor streamline data transfer as well as providing a suite of analysis tools, hence offering a solution that is fast in all aspects of the testing phase

➤ EXFO's CTP10 system can be used with the wafer-level probe station from MPI Corporation

ample possibilities for adding attenuators, switches, or different types of optical sources. Second, the MXS matrix switch addresses the need for quick but repeatable reconfiguration, switching in a fraction of a second to a new configuration.

Supporting process design kits (PDKs)

Design and manufacturing of PIC dies is maturing fast, with photonic wafers now containing thousands of components made available by foundries through process design kits (PDKs). To create and update these PDKs, wafer manufacturers require reliable testing solutions to optimize the different parameters of interest for a given optical component. Ring resonators have attracted a lot of attention in recent years and are commonly found in PIC designs to create extremely narrow peaks/troughs that can be used, for instance, as modulators; however, they are notoriously difficult to characterize spectrally.

Testing is a crucial step after design and manufacturing to provide feedback to the design tools and help optimize them. It is also needed for process control, to ensure that devices operate as expected throughout the assembly and packaging of the PIC chips. The PIC devices are usually tested at the wafer level prior to dicing so as to detect defects as early as possible and to avoid packaging defective dies. The ultimate goal of these PDKs is to allow the complete simulation of optical properties of a PIC design even before it is produced. However, 'real' testing will still remain in place in the lab for development of new components as well as in production to verify the specifications of the finished product.

Multi-vendor collaboration to deliver optimized solutions

It's notable that when thinking about test solutions for PIC production, one should not limit the discussion to the testing itself. Indeed, light first needs to be coupled in and out of each device and that operation also needs to be as fast as possible. For that purpose, PIC wafer probe stations include specially-designed optical fiber hardware and high-precision alignment software. It is also possible to couple several components simultaneously using a fiber array. Precision alignment and speed allow coupling optimization within a fraction of a second. Once the light is coupled into the wafer, the optical characteristics of the device under test can be measured.

To create customized solutions supporting specific production requirements, EXFO is involved in key collaborations with industry leaders in the PIC ecosystem to validate hardware and software interoperability. Collaborating with major suppliers of high-accuracy wafer positioners such as MPI Corporation, Aerotech, and FormFactor ensures optimal performance of the overall test solution.

A recent example is the collaboration between Aerotech, EHVA and EXFO in demonstrating an automated integrated photonic test solution that accelerates the lab to production timeline. Photonics testing software seamlessly integrates with EXFO's CTP10 and Aerotech's ultra-high precision photonics aligners, delivering optimum reliability and efficiency EXFO's PIC testing solutions can be fully automated and operated with third-party software integrators such as EHVA, OptiInstrument, and Maple Leaf Photonics (MLP) to provide turnkey solutions.

Next steps in PIC testing from lab to production

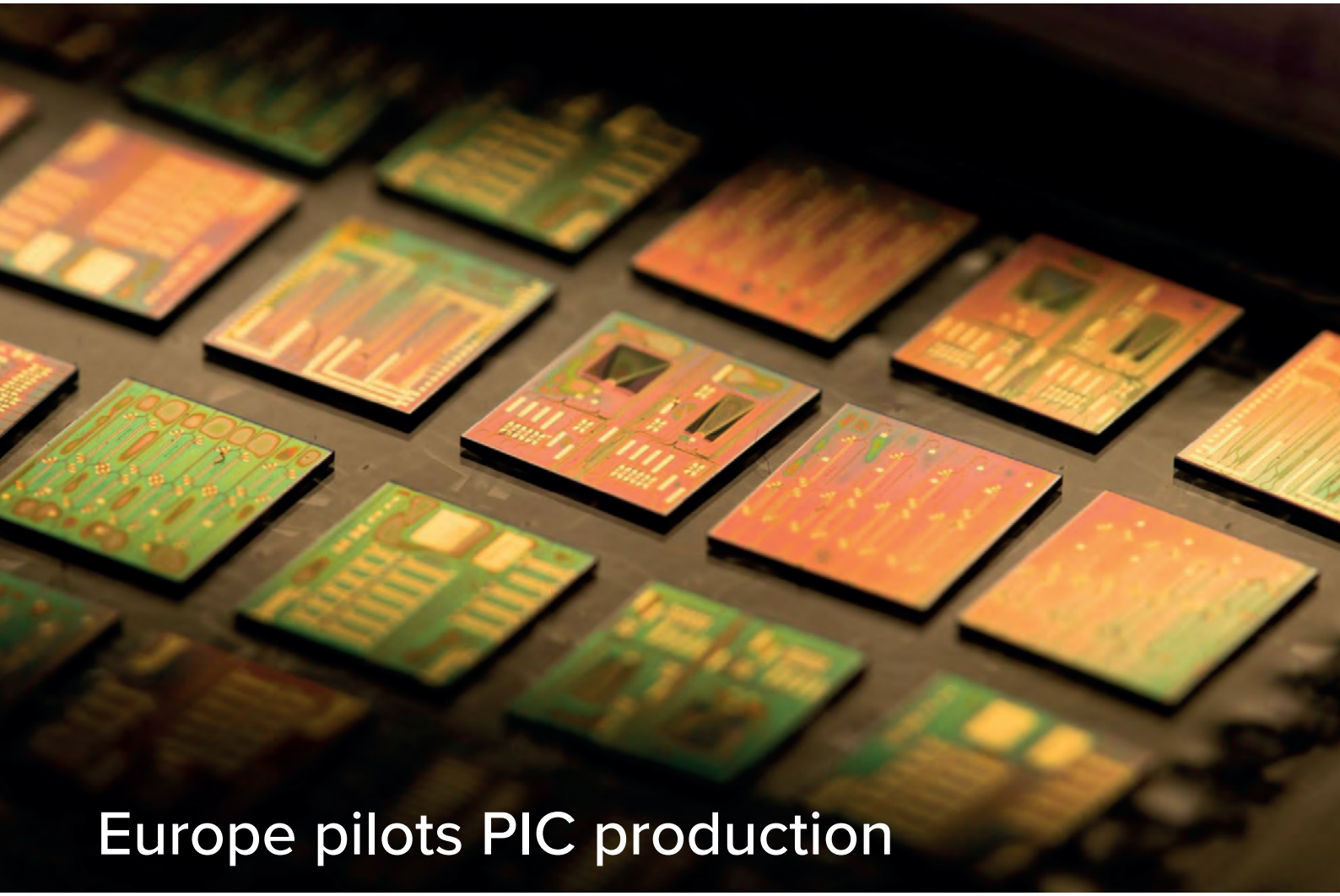
Clearly, several avenues can be investigated to ensure PIC component manufacturers are well equipped for mass production.

First, testing speed needs to be pushed to the limit. Twice the scanning speed on the tunable laser, coupled with suitable detecting speeds, can reduce the overall test process by a factor of 2 if the data post-processing is also optimized.

Second, rational testing needs to be implemented when possible, using reconfigurable hardware and software or even using PDKs to achieve "by-design" specifications.

Lastly, the handling of data and results as proposed by companies such as EHVA will also become a key component of optical testing.

What is certain is that the optical testing of PICs is set to evolve faster in the next few years than it has over the past decade, making 'lab to fab' a more seamless transition.



Europe pilots PIC production

Producing photonic integrated circuits (PICs) at industrial scale is a growing capability across the EU thanks to multiple EC-funded programmes that seek to create a complete PIC ecosystem within Europe's borders. Taking a new product to the pilot line stage is one of the last major steps toward commercialization. EPIC details recent advances and the important role Indium Phosphide technologies will play in this growing industry.

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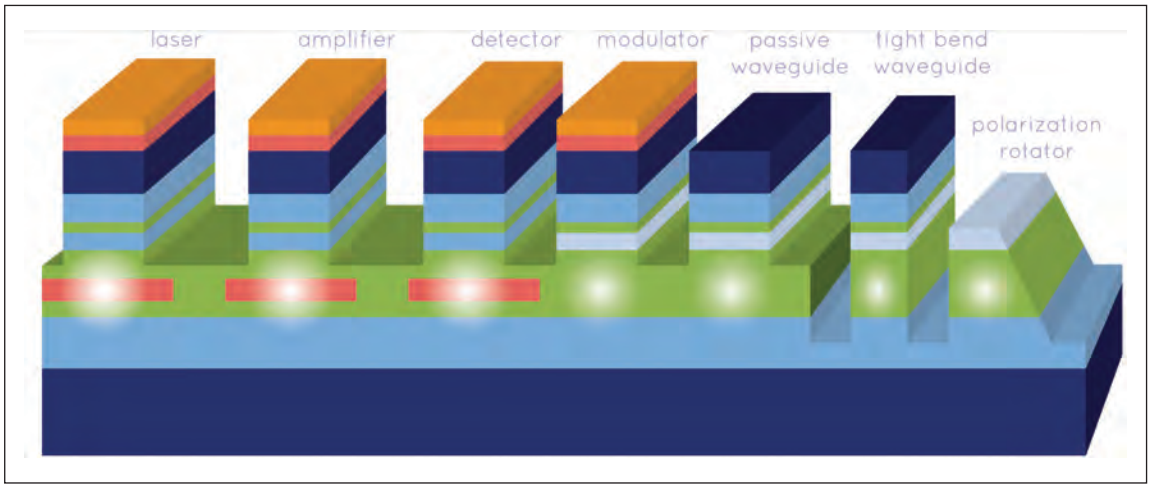
PHOTONIC INTEGRATED CIRCUITS (PICs) can be built on several material platforms that are complementary in many ways, but are also currently competing. The InP platform is very promising as it allows the integration of active photonic components on the chip, but until recently, European SMEs have been hampered in developing PIC-enabled technologies due to the lack of access to a mature, fast-turnaround, predictable, high-performance production infrastructure. Over the last six years, Europe has created several pilot line projects to empower users to scale up their photonic integrated circuit ideas and validate them for commercial production to meet these challenges.

The market of photonic integrated circuits (PICs) is facing exponential growth. Several material platforms are being developed in parallel to serve all the needs in photonic integration: silica, silicon nitride (SiN), silicon-on-insulator, and indium phosphide (InP). None of these platforms can serve all market needs on their own. They can serve as standalone platforms for some purposes, but they should be seen as complementary in the overall photonics landscape. The limitations of each material platform are well-known: lack of



➤ Figure 1: Active photonic components available in the InP material platform

active elements, such as lasers, in both Si-based technologies; the absence of low-loss passive components in the InP platform; and the challenges of integrating active photonic devices in mainstream electronics. Hybridization of all three technologies is often deployed to overcome the limitations of each of them. Another method is heterogeneous integration by bonding III-V materials on top of silicon, industrialized at Intel. Finally, there is hetero-epitaxy: the monolithic integration of III-V on silicon offering an exciting perspective for producing InP devices on 8-inch wafers.

The indium phosphide platform offers game-changing performance capabilities for photonic integrated circuits. InP allows for amplification and laser sources that are monolithically integrated into the chip without complex assembly steps. Additionally, InP offers efficient modulators and detectors as well as a broad range of passive waveguide structures and devices, such as waveguides and polarization rotators. Despite these advantages, InP-based PICs have so far been restricted to a small number of vertically integrated technology businesses. And although Europe boasts tens of innovative enterprises positioned to develop PIC-enabled technologies, progress in this direction has hitherto been limited by a lack of access to a mature, fast-turnaround, high-performance production infrastructure that delivers predictable results.

European efforts in promoting photonic integration started with the foundation of ePIXfab in 2006. The EU had a mission to build a future for integrated photonics in Europe by developing a fabless model for the fabrication of photonic circuits relying on European know-how. The idea was to promote photonics through advocacy of the latest developments in the field through training, road-mapped research, and reducing barriers to technology access. Over the last six years, Europe has created four pilot line projects that focus on scaling up PICs production on various material platforms that include the following:

- PIX4Life (2016 –2020) - a pilot line that focuses on state-of-the-art SiN photonic integrated circuit technology for health applications in the visible wavelength domain (400-700nm);
- PIXAPP (2017-2021) - the world's first open-access photonic integrated circuit (PIC) assembly and packaging pilot line;
- OIP4NWE (2018-2022) – an open-innovation pilot-production line for shared use by European SMEs through innovations in manufacturing equipment, focusing on reducing the defect rate, variability in production, and shortening throughput time;
- JePPIX (2016-2022) - the manufacturing pilot line for InP PICs with the mission to broaden access and transform the PIC industry through the introduction of a fabless manufacturing model from a vertically integrated model with all skills in-house within a small number of specialized businesses, to an open-access horizontal model accessible to all European innovators [1].

JePPIX is the Joint European Platform for Photonic Integrated Components and Circuits – a long-established community that includes many researchers and innovators spread across process

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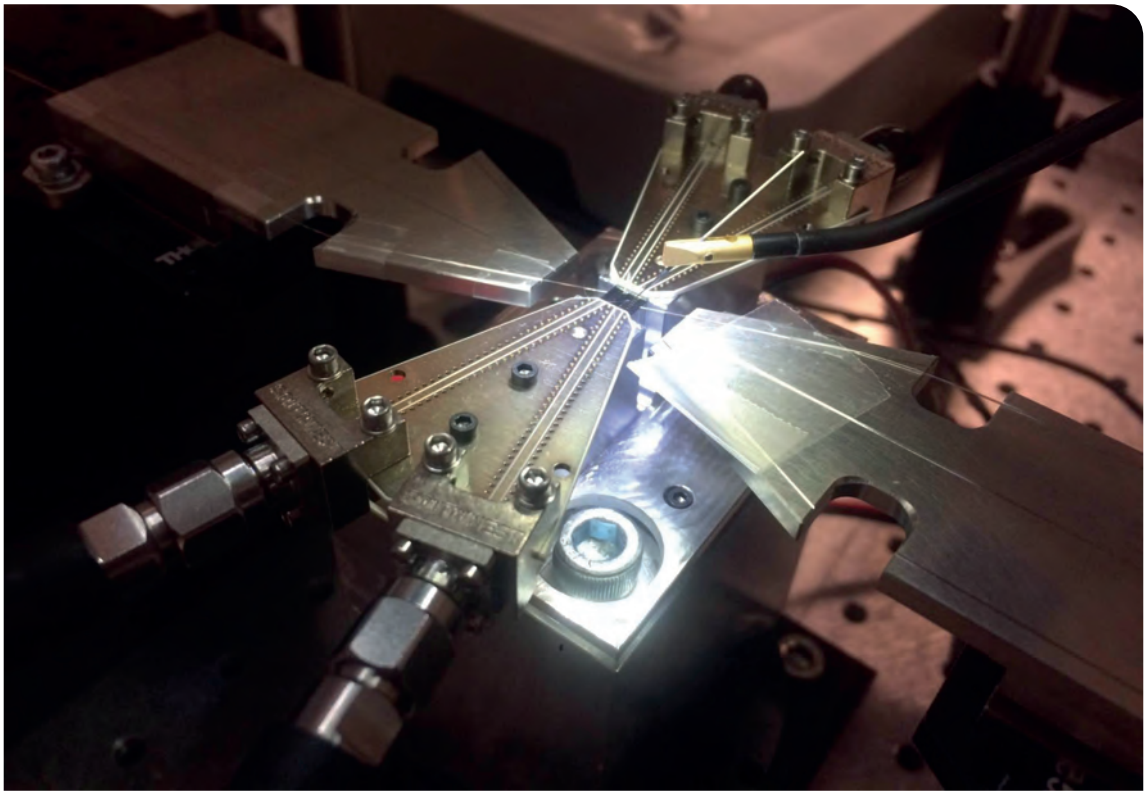
development, chip fabrication, packaging, software development, design, and training and which has several hundred users and members. JePPIX is active in multiple photonic integration research projects, and the R&D outlined in the JePPIX roadmap provides a route to sustained areal reductions and performance enhancement through energy efficiencies, speed, and precision. Initially, JePPIX offered access to the production of InP-based chips via multi-project wafer (MPW) services, and with the Pilot Line capability, this allows developers to transition seamlessly to scale-up and manufacturing. There are three InP manufacturing platforms in the JePPIX Pilot Line:

- Fraunhofer HHI provides a transmitter/receiver platform with passive elements, MMIs, AWGs, SOAs, DFB lasers, DBR gratings, 40G pin detectors, spot size converter, and thermo-optic phase shifters.
- Smart Photonics runs a 10G Transmitter/Receiver platform with passives, MMIs, AWGs, SOAs, pin detectors, electro-optical phase shifters, and metal interconnects.
- LioniX International, with its TriPleX technology platform, offers ultra-low-loss passives like straight waveguides, bends, S-bends, offsets, splitters, spot-size converters, lateral tapers, and thermo-optic phase shifters.

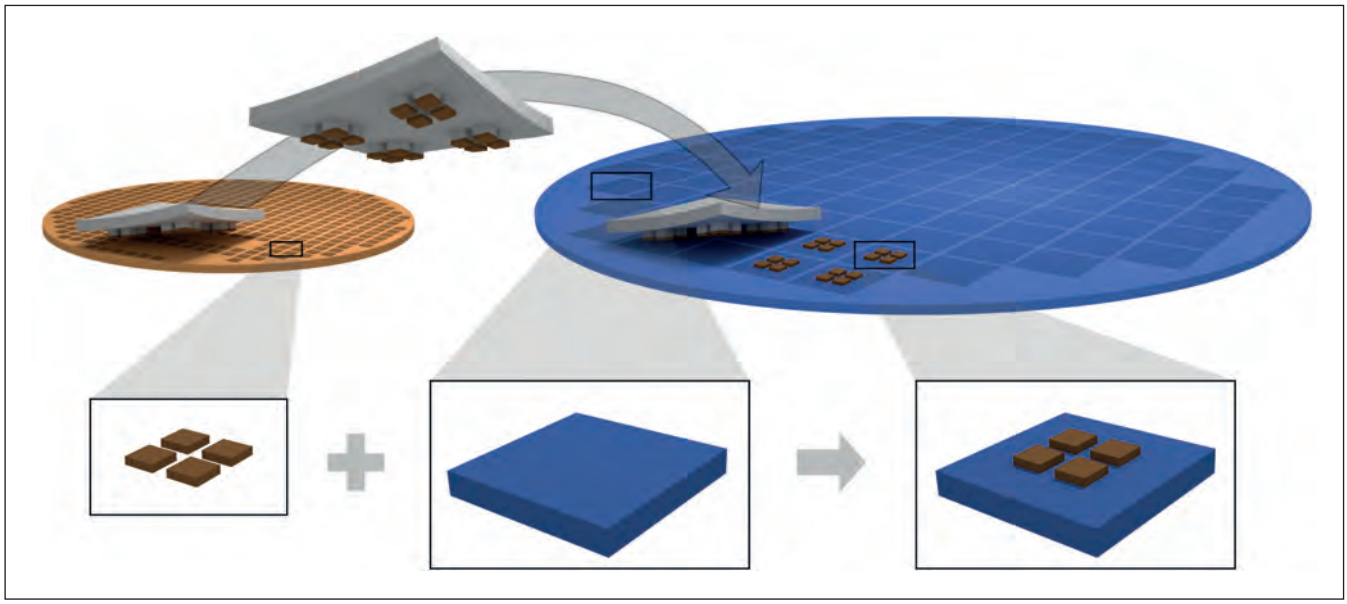
JePPIX facilitates the monolithic integration of best-in-class InP laser, modulator, amplifiers, and detectors with a comprehensive library of passive components. This monolithic approach provides a route to simplifying packaging and lowering costs. Specifically, JePPIX provides the technological and operational processes to accelerate the uptake of PIC technology in new markets - enabling SMEs to create products in markets where PICs have not been used before. It allows sustainable production in Europe by creating aligned, scalable, and inter-locking services and value chains that accelerates time to market from years to under 24 months with predictive design for fewer and faster product development cycles; qualify foundry processes, to TRL7, sharing process optimization across products.

The JePPIX pilot line for InP photonics is enabled by 12 partners, including leading photonics foundries (Smart Photonics, Fraunhofer HHI, III-V lab); design houses (Bright Photonics, VLC Photonics); packaging specialists (Tyndall National Institute); software specialists (VPI Photonics, Synopsys, Photon Design). The project is coordinated by TU Eindhoven and is validated by Nvidia, PhotonFirst, and promoted by the EPIC organization.

With EU support, the JePPIX pilot line will be able to co-finance European scale-up projects through to 2023. The pilot line is designed to be commercially viable beyond the enabling InPulse project. This enables businesses to continue past the prototype phase through industrial scale-up, design validation, yield learning, qualification, and ultimately acceptance for volume production on the same platform using the same design and test automation environments. It will also continue to offer monolithic indium phosphide integration using wafer batch processing to enable volume-cost scaling. The InP industry is using 3-inch and 4-inch wafers, enabling product shipments of millions per year.



➤ Figure 2: Photonic Integrated Circuit (PIC) under test.



➤ Figure 3: Schematic representation of the micro-transfer printing process proposed in the INSPIRE project.

According to Prof. Martin Schell from Fraunhofer HHI, InP photonics also has the potential to make a breakthrough in microelectronics and consumer markets: “Typical silicon fabs have several hundreds of thousands of wafer starts per year and lot sizes of twenty-five 8-inch wafers. These volumes may be required when photonics enters microelectronics, e.g., for intra-chip or chip-to-chip connections or consumer markets. For classical telecom, Datacom, and sensing markets, InP with its capability to both manufacture 40,000 lasers on a single 3-inch wafer and to efficiently handle smaller wafer volumes is the preferred technology.”

Several JePPIX project partners are already thinking ahead to the next challenges in systems integration. One such example could be the incorporation of micro-transfer printing, which is a method to print active elements such as InP circuits on a wafer-scale by transferring them with a stamp. Using a relatively large area stamp allows simultaneously aligning and bonding multiple devices to a carrier wafer containing passive circuitry like silicon or silicon technology.

The current challenge is to enable high-density arrays and functional circuits within the printed stamp, designing for high yield and low assembly variability. To address this and other challenges, the INSPIRE project was created in 2021 with EU funding of €4.9 million to bring transfer printing to a higher maturity level and industrialization. This project, by 2024, aims to achieve TRL 4 and is ideal for applications requiring very low noise lasers, such as fiber sensing or microwave photonics. If successful, it will become the first platform to combine the strengths of InP and SiN photonics and create best-in-class PIC manufacturing.

Furthermore, INSPIRE will strengthen the European manufacturing base by developing and implementing processing steps that are key to removing expensive assembly steps in PIC-based product realization. Initially, the methods will be developed for silicon nitride – indium phosphide integration. Later the developed technology can be further ported to silicon CMOS photonics as well, as the optical coupling happens through an intermediate silicon layer. INSPIRE will connect state-of-the-art manufacturing capability to leading-edge applications and industry clusters through JePPIX, ePIXfab, and the EC manufacturing pilot lines.

In conclusion, the European leadership in foundry technologies for photonic integration is now transitioning to a robust industrial manufacturing capability. The most recent efforts were dedicated to Indium phosphide integration that allows native lasers and modulators to be connected monolithically with a broad range of low-loss devices to simplify assembly and module integration. In perspective it will also provide a route to integration with premium silicon nitride passive components and 8-inch wafer production on silicon CMOS.

Europe’s flagship PIC pilot line, JePPIX, facilitates the uptake of InP PIC technology in new markets, and with the introduction of micro-transfer printing via the INSPIRE project, there is great promise for greater scalability of PIC technology. Eventually, the combination of performance requirements, market size, and cost requirements will determine what kind of integration technique becomes the preferred technology, and the EU´s pilot line efforts will pave the way for expanding European industry standards for photonic integration.

FURTHER READING

➤ [1] https://www.jeppix.eu/jeppix-pilot-line-in-a-nutshell/

New Industry Roadmap Released

Integrated Photonics for Data and Telecom

As the world becomes increasingly connected via the Internet, the demand for data continues to rise. Alongside increased usage, the digital population also continues to grow, with current estimates close to 5 billion users worldwide. So how will the data and telecom industry meet this exponential growth in demand?

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