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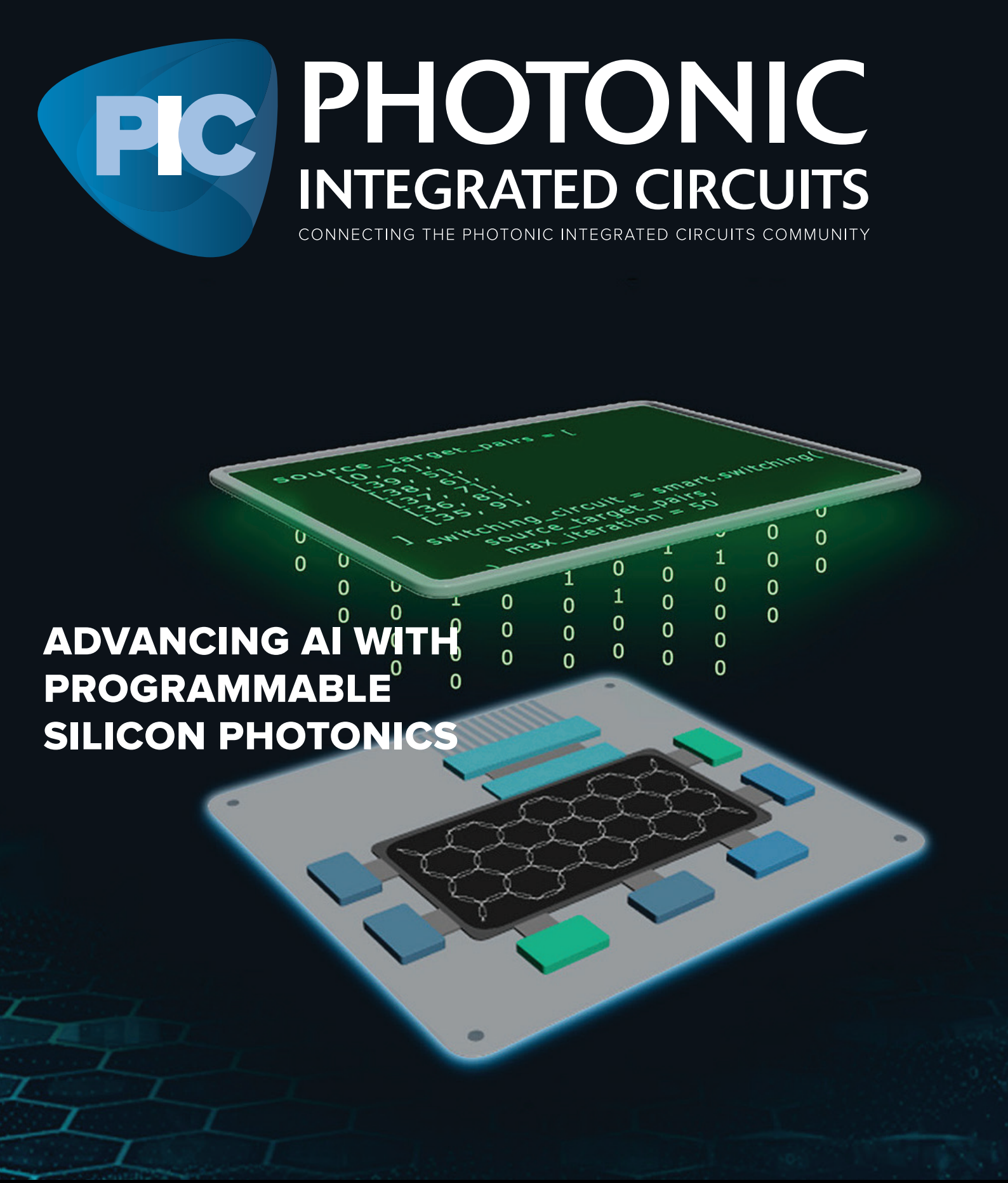

ADVANCING AI WITH PROGRAMMABLE SILICON PHOTONICS

ISSUE II 2024
AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION
PICMAGAZINE.NET

INSIDE

A bright future for the global PIC market

The latest report from IDTechEx predicts that the global PIC market will see robust growth , reaching $22 billion by 2034

People, planet, profits: sustainable ways forward for all

While pushing the boundaries of technology, businesses face a critical workforce shortage and environmental responsibilities

Efficient light emission and detection

Monolithic integration of in-plane III-V lasers and photodetectors on SOI is an approach for addressing the communications bottleneck

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VIEWPOINT

By Laura Hiscott, Editor

The industry in harmony

BACK IN APRIL, at the ninth PIC International conference, a delegate I was speaking to likened the industry to an orchestra; everyone is focusing on a different job but in combination they create something coherent and valuable. Who, then, I wondered, is the conductor?

It occurred to me that there isn't one. As the conference illustrated, the PIC industry is a dynamic system in which innovation and product development happen through knowledge exchange and partnerships. Lots of bridges are needed between all the different activities, from academic research and design expertise to manufacturing methods and testing capabilities.

The more than 40 talks at the meeting showcased how companies and research institutes are constantly trying new approaches and improving in every single one of these areas. Many speakers also highlighted their collaborations with partners, bringing their technologies together to create a more comprehensive solution.

With this magazine we also strive to capture a snapshot of these endeavours and to represent the progress being made in all facets of the ecosystem. In this issue, Ana González from iPronics explains the company's programmable silicon photonics technology and how it can advance computing infrastructure to meet the ever-growing demands of AI.

Meanwhile, Paul Momtahan from Infinera gives an overview of the many emerging uses of indium phosphide PICs, and James Falkiner from IDTechEx looks at the market forecast for several application areas. An interesting finding is that, although it is unlikely that a quantum computer will be fully commercialised within the next decade, it is expected to be a noticeable market for PICs by 2034.

In the context of this growth of quantum PICs, Ansys share how their new software can help designers to simulate quantum PICs accurately and realistically with allowances for fabrication imperfections, thus enabling engineers to create PIC designs without needing a deep understanding of quantum mechanics.

On the academic side, Ying Xue and Kei May Lau from the Hong Kong University of Science and Technology (HKUST) outline a new technique for integrating in-plane III-V lasers and photodetectors monolithically with silicon, to address the long-standing challenge of reducing loss.

Of course, the PIC industry does not exist in a vacuum, but is integrated within global social, economic and environmental structures. On this note, we also have a Q&A with Anuradha Agarwal from MIT, discussing how an NSF-funded project is building a skilled workforce and promoting sustainable practices within microchip manufacturing.

As all these efforts come together, the industry certainly seems to be in harmony.

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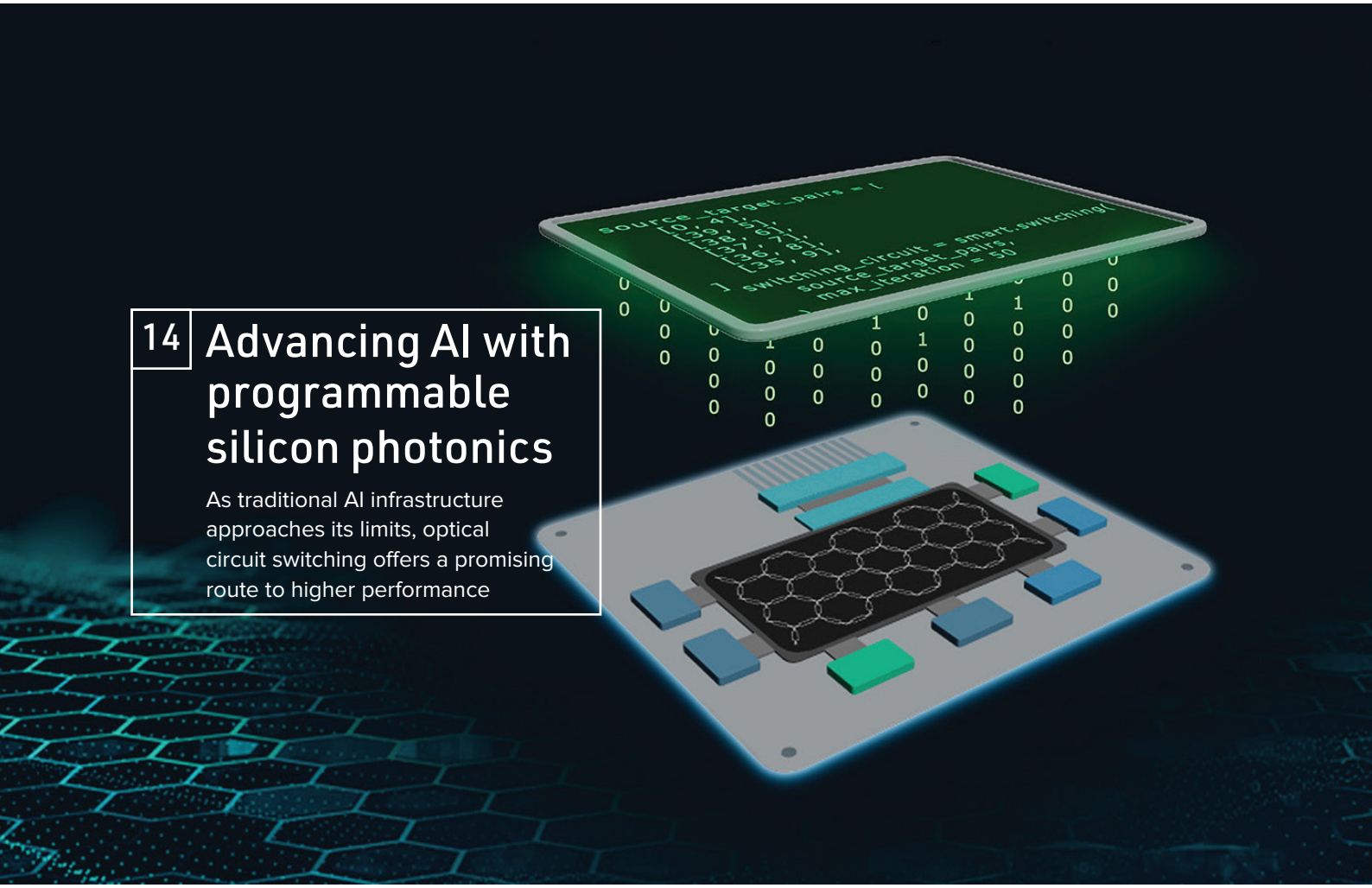

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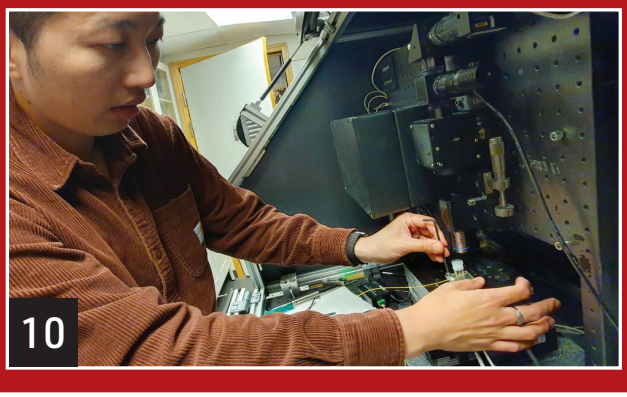

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Angel BUSINESS COMMUNICATIONS

PIC Magazine is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.US mailing information: Pic Magazine, ISSN 1096-598X, is published 4 times a year, March, May, August and December by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. The 2024 US annual subscription price is $198. Airfreight and mailing in the USA by agent named Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Periodicals post-age paid at Jamaica NY 11431. US Postmaster: Send address changes to Pic Magazine, Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Printed by: The Manson Group.

Optiwave Systems and CPFC partner on simulation for custom III-V devices

With the OptiSystem simulation framework, the organisations aim to address the lack of a supporting simulation ecosystem associated with pure-play foundries, enabling clients to tighten design cycles and reduce time to market

OPTIWAVE SYSTEMS and the National Research Council of Canada's Canadian Photonics Fabrication Centre (CPFC) are collaborating to deliver a design-to-manufacturing workflow that enables fabrication-aware simulation of custom III-V devices while protecting both epitaxial and layout design IP.

The advancement in heterogeneous PICs has evolved to a level that requires a unified simulation environment that enables pre-manufacturability evaluation. A high-fidelity simulation environment offers a distinct competitive advantage by drastically reducing a product's time to market and enhancing product quality through low-cost parameter exploration, thus improving overall cost-effectiveness and competitiveness.

Optiwave Systems offers a comprehensive solution for designing PICs from schematic design to system characterisation. The company says its monolithic simulation platform includes SPICE and System software that seamlessly integrates with third-party software for loading process design kits (PDKs) from photonic fabrication facilities. Compact device models (CDMs) of commercial PDKs can be generated using Optiwave's OptiFDTD and OptiMode software, then applied to the OptiSPICE engine called by layout tools. The company adds that OptiSystem also enables the characterisation of a PIC's performance within a system comprising devices, optical wires or wireless channels.

The CPFC is a commercial pure-play indium phosphide (InP) photonics foundry that specialises in volume manufacturing of custom high-performance devices, such as buried heterostructure lasers and optical amplifiers.

In a design-assisted III-V foundry model, a foundry provides a set of reference designs, or PDKs, to allow clients to rapidly construct photonic circuits. In contrast, with the pure-play III-V foundry model, clients specify both component geometries and epitaxial compositions. The resulting photonic devices fabricated at pure-play foundries are thus fully customised and capable of achieving best-in-class performance tailored for specific applications.

One challenge in the pure-play foundry model arising from the lack of III-V component standardisation is the absence of a supporting simulation ecosystem for custom photonic devices. Optiwave Systems and the CPFC are aiming to address this challenge, by delivering a design-to-manufacturing workflow that enables fabrication-aware simulation of custom III-V devices while protecting both epitaxial and layout design IP.

The organisations say that clients working with both Optiwave Systems and the CPFC can leverage this workflow to fabricate custom III-V devices with the CPFC and emulate their performance in system-level and link-level deployments with OptiSystem's suite of over 600 components, including realistic fibre models, DSP components, and advanced visualisers.

Moreover, the heterogeneous integration of III-V materials onto silicon platforms has attracted significant attention in the past year. According to Optiwave, its complementary suite of simulation tools allows users to evaluate custom III-V components fabricated at the CPFC with various silicon photonics technologies, such as those accessible in PDK form at various silicon foundries.

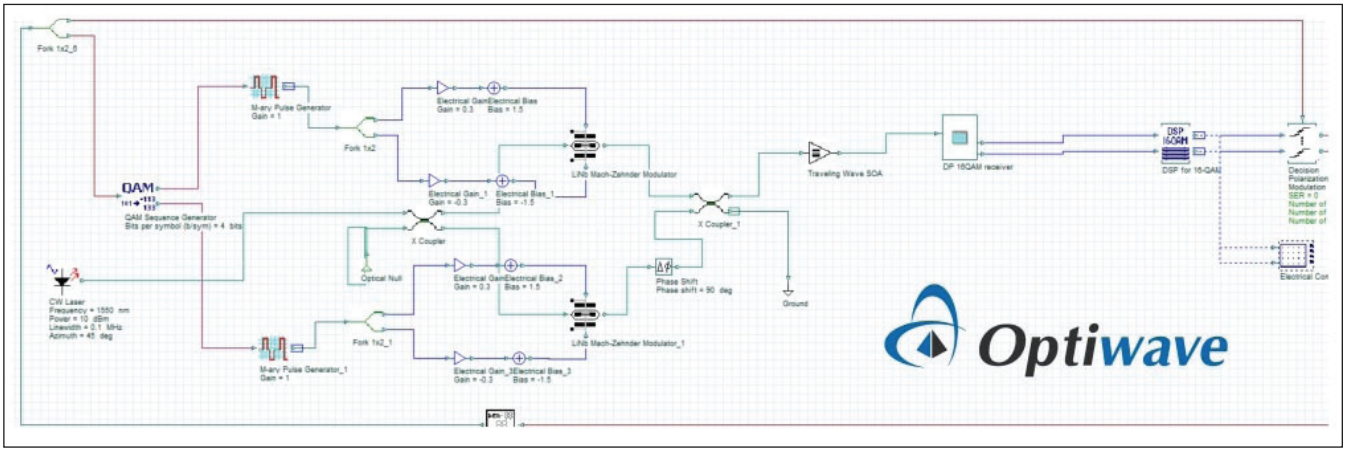

Image credit: Optiwave Systems Inc.

One Silicon Chip Photonics and Thales partner on autonomous rail

The Canada-based company says its optical inertial navigation system is 10 times more accurate than commercial-grade MEMS-based navigation devices, and can be used in a wide range of applications from drones and autonomous transport to agriculture and survey work

THE MARKET for commercial drones is growing dramatically – from an estimated $19.9 billion in 2022 to a projected $57 billion in 2030. Meanwhile, the autonomous vehicle (AV) market is projected to grow to more than $13 trillion by 2030. But one of the key challenges for drone and AV manufacturers continues to be finding higher-accuracy and lower-cost navigational sensors that are essential to enabling this growth.

Drones and AVs rely on sensor technology to navigate. Until recently, much of the technical work on AV navigation has focused on a blend of sensors that have critical limiting factors. Camera, radar, and LiDAR sensors are all limited by advancements in computer perception, with a huge need for redundancy due to environmental conditions – such as the risk of fog or dirt covering one or more sensors.

Another technical challenge is that many types of drones and AVs must operate in demanding and/or hostile environments where GPS is denied and extreme accuracy is essential.

To address these challenges, One Silicon Chip Photonics (OSCP), a Montreal-based company, has developed an inertial optical system which it says matches the accuracy of navigational sensors used in the aerospace industry at a fraction of the cost. According to the company, because these chips do not have any moving parts, they are 10 times more accurate than commercial-grade micro-electro-mechanical systems inertial measurement units (MEMS IMUs) and they enable highly accurate navigation even when GPS signals are not available.

OSCP has partnered with French multinational company Thales, which is developing autonomous rail systems and has been testing OSCP's prototype in the field. Using sensors like OSCP's in rail transport will increase vehicle autonomy which – along with moving block signalling – has the potential to increase rail capacity by up to 50 percent and cut energy consumption by 15 percent, according to Thales.

In addition to rail transport and military applications, drones and AVs are also increasingly being used in agriculture, mining, mapping and survey work, as well as in trucking, delivery and other transport industries.

OSCP has recently secured $1.2 million in seed funding from 7percent Ventures and 2050 Capital, which it says will allow it to accelerate its growth. This funding supplements earlier grants to OSCP totalling $4.2 million. The company says that its technology's potential to reduce greenhouse gas emissions in autonomous transport as compared with conventional technologies has been central to its funding.

"This $5.4 million in total funding will allow us to expand our sales and development team and expedite the commercialisation of our sensors," said Kazem Zandi, OSCP's founder & CEO. Harry Morgan of 7percent Ventures said: "The enabling technologies for AVs – sensors, chips, and other hardware – are often overlooked when it comes to investment and innovation. We believe that the technology that Kazem and OSCP have developed will be vital in facilitating and accelerating the rate at which autonomous systems, across transport and mobility, can realise their potential."

Cornel Chiriac, founding partner of 2050 Capital, added: "The road to full autonomy requires fundamental innovation in navigation, not more sensors and workarounds. OSCP delivers a blend of precision, reliability, and cost-effectiveness in an integrated photonic chip. OSCP technology paves the way for mass adoption of autonomous systems and unlocks innovation across both existing enterprises and ambitious startups that need these crucial building blocks for their own visions of autonomy."

Photonic demonstrates distributed quantum entanglement between modules

The company says its architecture optically entangles and performs distributed computing between remote T centre spins using telecom photons, marking a milestone towards scalable, commercially relevant quantum systems

THE CANADA-BASED COMPANY Photonic, which focuses on distributed quantum computing in silicon, has announced the demonstration of entanglement between modules – as opposed to entanglement within modules, which has been achieved in many existing quantum architectures.

The company says this shows that its architecture provides a unique solution to one of the primary challenges on the road to large-scale quantum adoption – scalable entanglement distribution – and literally goes "outside the box" to open avenues for transformative applications in fields such as materials science and drug discovery.

"The crucial role that entanglement distribution will play in unlocking the commercial promise of quantum computing cannot be overstated," said Stephanie Simmons, founder and chief quantum officer at Photonic.

"Large-scale quantum algorithms running across multiple quantum computers require enormous amounts of distributed entanglement to work well. These demonstrations highlight the promise of our distinctive architectural approach to solve the challenge of scaling beyond single nodes. While there is still much work ahead, it's important to acknowledge the pivotal role that entanglement distribution must play in shaping quantum system designs."

Krysta Svore, distinguished engineer and vice president of Advanced Quantum Development at Microsoft, added: "Last November, we announced a strategic collaboration with Photonic to co-innovate on quantum technologies to accelerate scientific discovery.

"These recent developments showcase a fundamental capability: entanglement distribution over long distances. With these advancements, we're progressing toward the next stages of networked quantum computing."

According to Photonic, its approach is based on optically-linked silicon spin qubits with a native telecom networking interface, meaning that it can integrate with the infrastructure, platforms, and scale of today's global telecommunications networks, including the Microsoft Azure cloud.

The company says that three demonstrations, culminating in the teleported CNOT gate sequence, established and consumed distributed quantum entanglement – entanglement between qubits not adjacent to one another or even in the same cryostat.

Global Quantum Intelligence's March 2024 Scalable Quantum Hardware report confirmed "the necessity for a modular approach to scaling in nearly all proposed quantum computing architectures. This modular approach, which emphasises distributed rather than monolithic quantum computing stacks, offers not only scalability but also flexibility, maintainability, and redundancy."

Quandela announces manufacturing site

The company says its new pilot line for high-performance photonic qubit devices will improve manufacturability of the quantum technology and propel it into the industrialisation phase

QUANDELA, a European quantum computing company, has announced the inauguration of its first manufacturing pilot line for high-performance photonic qubit devices, aiming to accelerate the deployment of error-corrected quantum computers. Following the opening of the company's first quantum computer factory in June 2023, which it says has enabled the delivery of two quantum computers to industrial customers, this new production site underscores Quandela's commitment to industrial scaling and innovation in the quantum computing sector.

Quandela's approach to building quantum computers at scale combines integrated photonics technology with semiconductor quantum dot-based devices, serving as both spin qubits and photon generators. The company says this technology is rooted in 20 years of top-class scientific research conducted within French telecom laboratories and the French National Research Institute CNRS. The know-how was transferred to Quandela in 2017, and packaged devices have been commercialised since 2018.

According to the company, the new manufacturing plant combines this extensive know-how with industrial machines and processes to boost the manufacturability and performance of the qubit devices. It is located at The Photovoltaic Institute of Île-de-France (IPVF).

Quandela says that this site is the first manufacturing plant entirely dedicated to such technology worldwide, marking a key milestone in the continued development of its technology. The company adds that the pilot line effectively opens a new phase that will propel this quantum technology into the industrialisation phase and expand its integration into quantum systems for computing, networking, and communication.

For the upcoming two years, Quandela expects the pilot line to produce more than 2000 devices per year. At full capacity, it is projected to reach 10,000 devices per year, with qubit device density increasing to hundreds of devices per mm^2.

Quandela also highlights its Qubits Identification Tool, a machine which it says permits testing of qubit properties, such as coherence time, at cryogenic temperatures in just a few minutes, selecting the most performant qubits for further processing.

By probing the quantum properties of hundreds of nanometre-sized structures and collecting high-volume data while mapping uniformity, this method aims to provide fast feedback to optimise the fabrication process and lead to high yield (from 40 percent to over 70 percent) and low process variation (increased uniformity over thousands of devices on a cm^2 area).

Lightwave Logic and AMF partner on advanced modulators

LIGHTWAVE LOGIC, a technology platform company leveraging its proprietary electro-optic (EO) polymers to transmit data at higher speeds with less power in a small form factor, has announced that it is collaborating with Advanced Micro Foundry (AMF), a silicon photonics volume foundry, to develop state-of-the-art polymer slot modulators utilising AMF's silicon photonics platform.

According to Lightwave Logic, these modulators have been shown to achieve a record low drive voltage below 1 V and data rates of 200G PAM-4. The company says this performance will enable a new generation of 800G and 1.6T pluggable transceivers to address fast-growing requirements for optical connectivity for large generative AI computing clusters.

Lightwave Logic and AMF have collaborated over the past year to develop the electro-optic polymer slot modulators utilising AMF's standard manufacturing process flow on 200 mm wafers. The companies say that this successful demonstration marks a significant milestone in integrated photonics, blending silicon photonics with polymer materials.

Building on this demonstration, both parties are aiming to enhance the modulators to ensure these advanced components are readily accessible to companies on a manufacturing scale.

"AMF is truly a world-class facility with their silicon photonics maturity, and capacity for volume manufacturing," said Michael Lebby, chairman and CEO of Lightwave Logic. "Working with AMF, we not only increased our wafer size to 200 mm, but we also turbo-boosted silicon photonics with our polymer slot modulators to achieve world-class performance. Engineers from both sides have worked hard to achieve a silicon photonics design that integrates smoothly with polymer – a process that would have been much more challenging if other next-generation modulator materials had been utilised. This accomplishment puts our company in a very strong position to ramp volume both for our polymers as well as 200 mm silicon wafer volume with AMF."

Silica glass micro-optics 3D printed on optical fibre tips

Researchers say that this achievement is a first for communications and bridges the gap between 3D printing and photonics, with a wide range of potential applications including sensors and quantum communication

RESEARCHERS in Sweden 3D printed silica glass micro-optics on the tips of optical fibres – surfaces as small as the cross section of a human hair. The achievement, which the team says is a first for communications, could enable faster internet and improved connectivity, as well as innovations like smaller sensors and imaging systems.

Reporting in the journal *ACS Nano,* researchers at KTH Royal Institute of Technology in Stockholm say integrating silica glass optical devices with optical fibres enables multiple innovations, including more powerful remote sensors for environmental and healthcare applications. They add that their printing techniques could also prove valuable in the production of pharmaceuticals and chemicals.

According to KTH Professor Kristinn Gylfason, the method overcomes long-standing limitations in structuring optical fibre tips with silica glass, which often require high-temperature treatments that compromise the integrity of temperature-sensitive fibre coatings.

In contrast to other methods, the process begins with a base material that doesn't contain carbon, meaning that high temperatures are not needed to drive out carbon in order to make the glass structure transparent. The authors have filed a patent application for the technique.

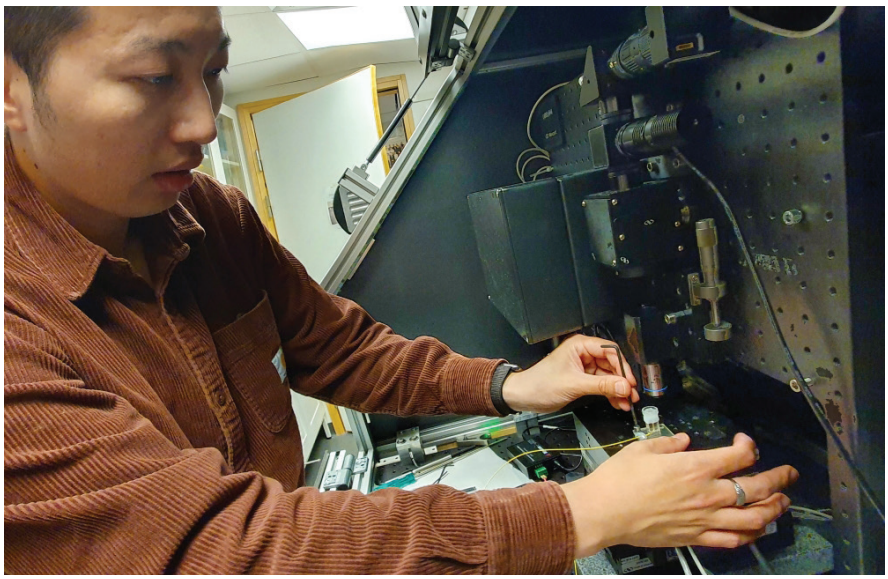

Image credit: David Callahan

More resilient sensors

The study's lead author, Lee-Lun Lai, says the researchers printed a silica glass sensor that proved more resilient than a standard plastic-based sensor after multiple measurements.

"We demonstrated a glass refractive index sensor integrated onto the fibre tip that allowed us to measure the concentration of organic solvents," said Lai. "This measurement is challenging for polymer-based sensors due to the corrosiveness of the solvents."

A co-author of the study, Po-Han Huang, added: "These structures are so small you could fit 1000 of them on the surface of a grain of sand, which is about the size of sensors being used today."

The researchers also demonstrated a technique for printing nanogratings, ultra-small patterns etched onto surfaces at the nanometre scale. These are used to manipulate light in precise ways and have potential applications in quantum communication.

Gylfason says the ability to 3D print arbitrary glass structures directly on fibre tip opens new frontiers in photonics. "By bridging the gap between 3D printing and photonics, the implications of this research are far-reaching, with potential applications in microfluidic devices, MEMS accelerometers and fibre-integrated quantum emitters."

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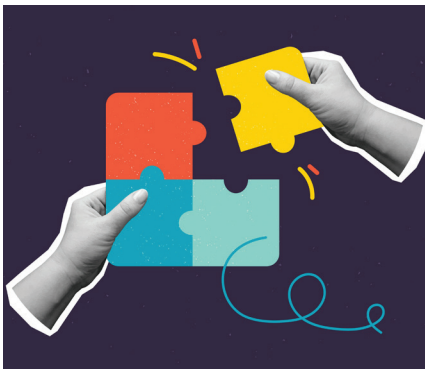
POET and Foxconn collaborate on 800G and 1.6T optical transceivers

Foxconn has selected POET to supply silicon PIC optical engines for use in high-speed pluggable transceivers, which are intended to address growing demand from AI and datacentre applications

POET TECHNOLOGIES has announced that Foxconn Interconnect Technology (FIT), a provider of interconnect solutions for communication infrastructure and several other large, high-growth markets, has selected POET's optical engines, which are silicon PICs, for its 800G and 1.6T optical transceiver modules.

POET and FIT have entered into a collaboration to develop 800G and 1.6T pluggable optical transceiver modules using POET optical engines with an aim to address the growth in demand from cutting-edge AI applications and high-speed datacentre networks. As part of the collaboration, POET will develop and supply its silicon PIC optical engines based on the patented POET Optical Interposer technology, while FIT will design and supply the high-speed pluggable optical transceivers for delivery to some of the largest end customers in the world.

"The growth in demand from emerging applications such as artificial intelligence and machine learning requires continuous innovation to keep pace with power and cost



requirements," said Joseph Wang, CTO at FIT. "We are excited to partner with POET on this development. POET's hybrid-integration platform technology will enable us to use best-of-breed components and ramp to high volume at a much faster pace and in a cost-efficient manner."

Suresh Venkatesan, chairman and CEO of POET, said: "POET's vision is to 'semiconductorise' photonics by integrating electronic and photonic components on the interposer to enable wafer-scale assembly. We are honoured to work with an industry leader like FIT, capable of ramping to high volume production with its expertise in transceiver design and manufacturing. We look forward to expanding our collaboration to future projects once this initial project is complete."

POET's transmit optical engines integrate externally modulated lasers (EMLs), EML drivers, monitor photodiodes, optical waveguides, thermistors and an optical multiplexer, where applicable, onto an optical interposer-based PIC. The receive optical engines integrate high-speed photodiodes, transimpedance amplifiers, optical waveguides and optical demultiplexers, where applicable. All components are passively assembled on the interposer at wafer scale using standard pick-and-place semiconductor equipment. Passive alignment of the photonic elements and use of high-speed RF traces between the electronic and photonic components to avoid wire-bonds are two hallmarks of the technology. POET expects to complete the design of the optical engines for FIT by Q3 2024 and start optical engine production at its joint venture, Super Photonics Xiamen, by Q4 2024.

Imec and Sarcura introduce scalable on-chip cell detection

The organisations say that this proof of concept, which uses integrated photonics and is fabricated on imec's 200 mm CMOS pilot line, paves the way for high-throughput cell analysis

THE BELGIAN research institute imec and Austrian technology startup Sarcura have presented their proof-of-concept on-chip flow cytometer using integrated photonics. Published in *Scientific Reports,* part of the Nature Publishing Group, the organisations say this innovation offers a unique platform for the detection and discrimination of human leukocytes (white blood cells) and marks a significant stride towards cost-effective, scalable, and highly parallelised cell analysis.

Accurate identification of human cells is a key operation in modern medicine, pivotal for understanding disease mechanisms and advancing targeted and personalised treatments. With the advent of cell manufacturing, living cells can now be engineered to function as treatments, notably in groundbreaking therapies like CAR-T immune cell therapy for cancer. The ability to identify these therapeutic cells in complex cell products at high throughput is crucial, and often time sensitive.

The method of choice today is flow cytometry, which enables characterisation of cell populations based on the physical and chemical characteristics of individual cells as they flow past a laser. However, the current implementation includes bulky instrumentation, complex and manual workflows (posing contamination risks), and high operational costs. These challenges hinder widespread availability and adoption of cell therapies in decentralised settings.

To address these limitations, imec is harnessing its expertise in CMOS technology, photonics, and fluidics with the aim of automating, miniaturising and parallelising flow cytometry. In a study published in *Scientific Reports,* imec, together with Sarcura, has unveiled an on-chip flow cytometer using integrated photonics. Fabricated on imec's 200 mm CMOS pilot line, the organisations describe the opto-fluidic chip as featuring a pioneering material stack facilitating both cell illumination and capturing of scattered light through waveguide optics, and precise cell delivery to the detection points using microfluidic channels.

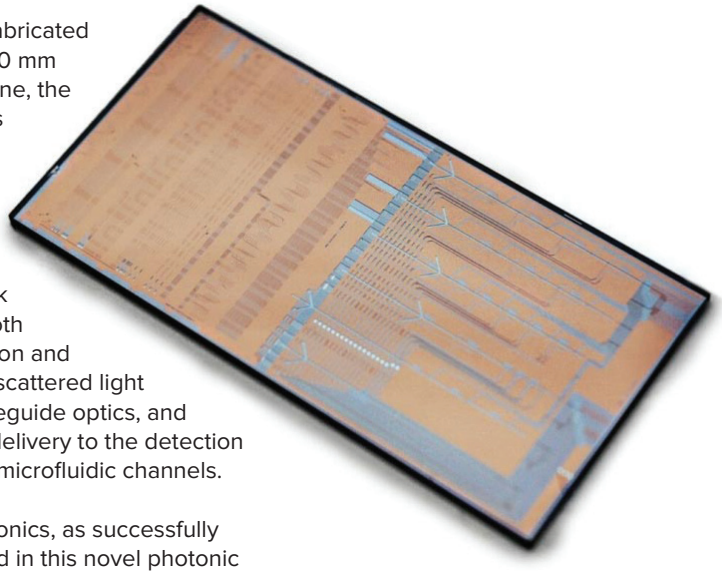


Image credit: imec

"Silicon photonics, as successfully demonstrated in this novel photonic chip, is the revolutionary and essential building block that merges single-cell detection capabilities with massive parallelisation on a dramatically miniaturised footprint," said Daniela Buchmayr, CEO and cofounder of Sarcura. "This breakthrough opens new possibilities for addressing previously unsolved challenges in applications such as cell therapy manufacturing."

Niels Verellen, scientific director at imec, added: "We have demonstrated, for the first time, that a monolithically integrated biophotonic chip can be used to collect optical scattering signals that allow the discrimination of lymphocytes and monocytes from a patient's blood sample, rivalling the performance of commercial cytometers. The main advantage lies in the potential for dense parallelisation of multiple flow channels to boost the system throughput."

In a next phase, imec and Sarcura say the compact, alignment-free design should enable billions of cells to be identified within a limited amount of time.

Crucially, according to the organisations, the chip architecture seamlessly integrates with imec's previously developed bubble jet cell sorting module, compatible with wafer-scale fabrication, and the photonic components and layout can be tailored to suit specific applications. Therefore, they add, this proof-of-concept marks a substantial leap towards cost-effective, scalable, and highly parallelised cell sorting platforms.

To address these limitations, imec is harnessing its expertise in CMOS technology, photonics, and fluidics with the aim of automating, miniaturising and parallelising flow cytometry

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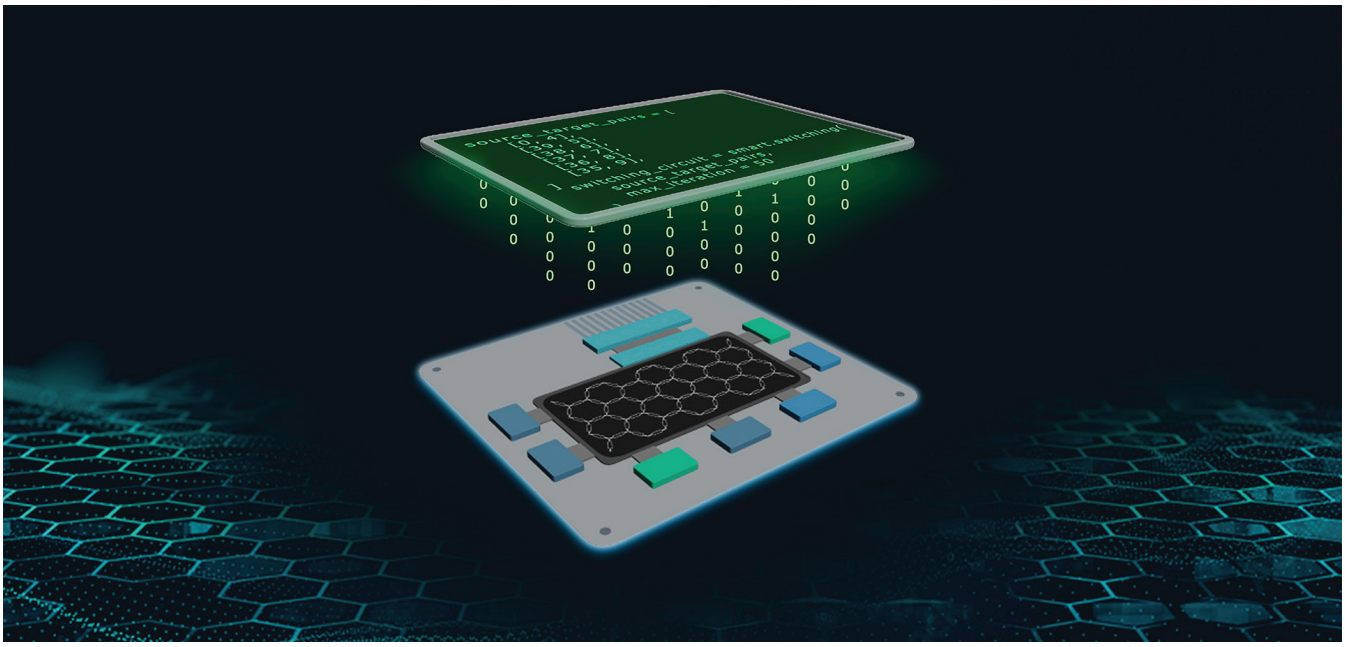


Advancing AI with **programmable silicon photonics**

As traditional AI infrastructure approaches its limits, optical circuit switching offers a promising route to higher performance. iPronics' software-defined silicon photonics engine can deliver the low latency, high speed, and flexibility to support the next generation of AI clusters.

BY ANA GONZÁLEZ, VICE PRESIDENT OF BUSINESS DEVELOPMENT, IPRONICS

THE AI REVOLUTION unfolding today promises to open new frontiers in wide-ranging fields, from designing more targeted drugs in medicine to achieving real-time augmented reality. These exciting machine learning (ML) applications have highlighted the importance of large-scale compute capabilities, and the growing demand for powerful ML models has driven an increase in the size of deep neural networks, as well as the datasets used to train them.

As this technology reshapes our world, it is having a profound impact on the landscape of the datacentre industry, demanding more robust, efficient, and scalable solutions. Training large language models (LLMs) involves complex and power-intensive computational tasks, with higher requirements of network bandwidth, latency, and advanced network management systems. All of this creates a pressing need for entirely new ways to build interconnects for distributed ML systems. When AI leaders were recently asked about the key considerations for expanding their AI compute infrastructure in 2024, they reported that flexibility and speed are the top drivers, with 65 percent and 55 percent of respondents citing these factors, respectively. Optimising GPU utilisation is another major concern for 2024-2025, with the majority of GPUs currently underutilised during peak times [1].

As the demands of AI compute infrastructure grow, traditional electronic solutions are reaching their limits in terms of flexibility and rapid scaling. To take AI to the next level, the field of photonics offers a promising path forward, with optical circuit switching (OCS) emerging as a key technology for dynamic network reconfiguration and efficient data flow.

In this article, we present the limitations of current infrastructure for AI clusters, and how OCS technology – particularly software-defined silicon photonics engines – can overcome them.

Fibre links and network topologies

Hyperscale datacentres usually use a folded Clos topology, also called a spine-leaf architecture. In this configuration, servers in the rack are connected to the top-of-rack (ToR) switches with short copper cables that are 1-2 m long and carry 25G or 50G signalling. The ToR is then connected through a

fibre cable to a leaf switch at the end of the row or in another room. All the leaf switches in a datacentre connect to all the spine switches.

AI clusters, on the other hand, require much more connectivity between GPU servers, but have fewer servers per rack (due to heat constraints). Each GPU server is connected to a switch within the row or room. These links require 100G to 400G over distances that cannot be supported by copper. NVIDIA's GPU server DGX H100 has 4 x 800G ports to switches (operated as 8 x 400GE), 4 x 400GE ports to storage, and 1GE and 10GE ports for management. A DGX SuperPOD can contain 32 of these GPU servers connected to 18 switches in a single row. This represents a remarkable increase in the number of fibre links in the data hall, indicating a potential need for alternative network topologies and technologies that can overcome the scaling challenge.

Optical circuit switching (OCS) technologies offer benefits compared with electronic packet switches (EPS), including low latency, energy efficiency, and data rate and wavelength agnosticism. OCS is agnostic to bit rate, protocol, framing, line coding, and modulation formats. Leveraging OCS is equivalent to physical re-cabling of the fibre links, without requiring any actual re-cabling, to adapt the system configuration to match workload placement.

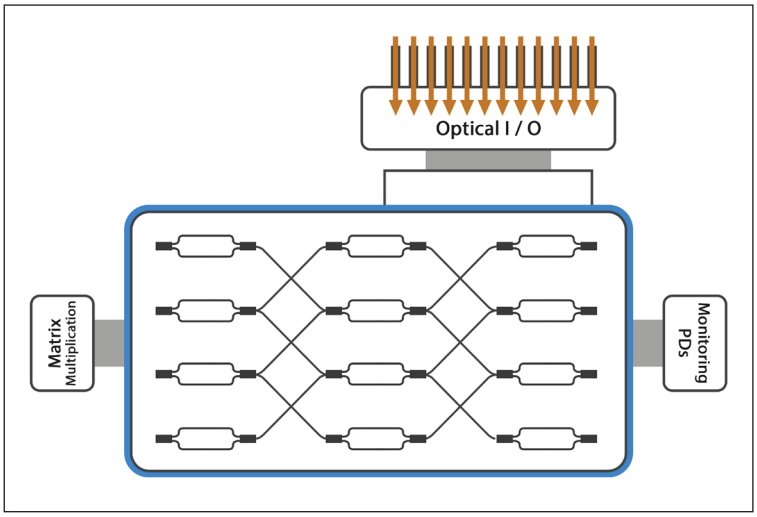
Among the main benefits of OCS technology in datacentres is its flexibility, since it can support different network topologies that can adapt to the communication patterns of individual services. Additionally, optical switching can replace subsets of electronic switches within static topologies, reducing power, latency, and cost. Moreover, the cost of OCS systems does not grow with increasing data rates.

Google has been the first hyperscaler to deploy OCS on a large scale for datacentre networking; by employing circulators to realise bidirectional links through the OCS, the company has effectively doubled the OCS radix [2]. Google implemented a datacentre interconnection layer employing micro-electro-mechanical systems (MEMs)-based OCS to enable dynamic topology reconfiguration, centralised software-defined networking (SDN) control for traffic engineering, and automated network operations for incremental capacity delivery and topology engineering [3].

In AI clusters, OCS technology can also be highly valuable for bandwidth-intensive and latency-sensitive applications such as ML training. Optical switches that are commercially available today have a reconfiguration latency of around 10 ms, which makes them suitable for circuits that last through the entire training process.

Flexibility for network adaptations

In most datacentres, there are two levels of network adaptations that can save capex and opex: traffic engineering and topology engineering. These two levels operate on distinct timescales.



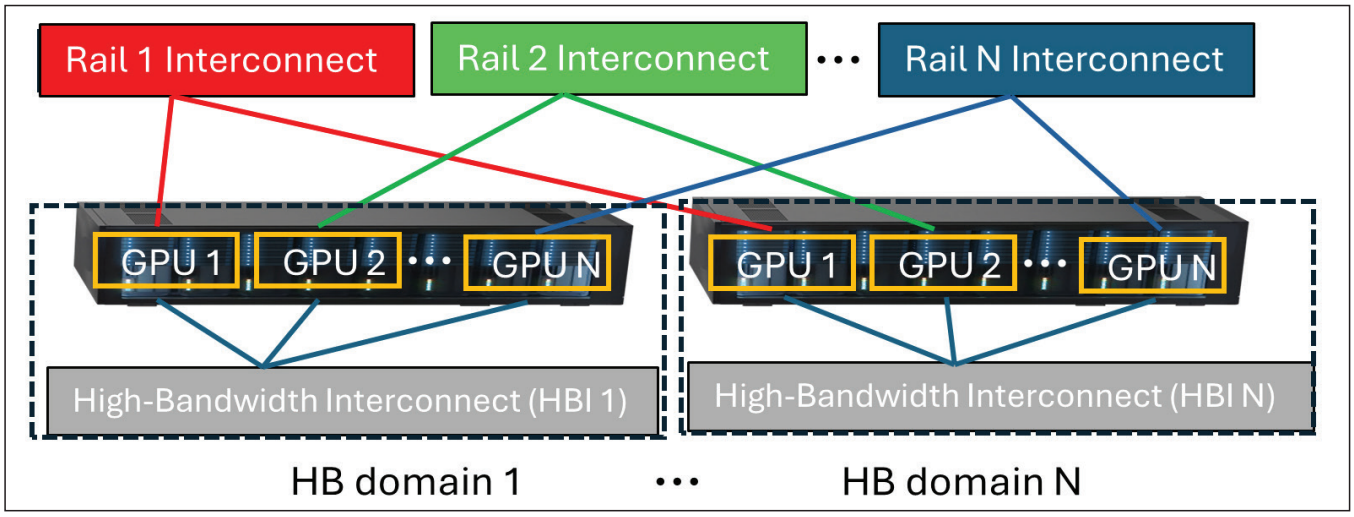
➤ Figure 1. Sketch of the chip under development at iPronics for AI clusters and datacentre applications.

The first level, traffic engineering, operates on top of the logical topology, and aims to optimise traffic forwarding across different paths, based on the real-time demand matrix representing communication patterns. Traffic engineering is the inner control loop that responds to topology and traffic changes at a granularity of seconds to minutes, depending on the urgency of the change. In this context, OCS technology allows for traffic-aware topology that can accommodate a particular load and avoid indirect paths.

The second level, topology engineering, adapts the topology itself to increase bandwidth efficiency. In a datacentre, the varying demand matrix needs to be satisfied, while also leaving enough headroom to accommodate traffic bursts, network failures, and maintenance. In datacentres, generating short-term traffic predictions is challenging, so topology engineering is much slower than traffic engineering.

However, large-scale ML requires more frequent topology reconfiguration, with its high bandwidth requirements and relative predictability of traffic patterns, which shift intensive communication among changing subsets of computation and accelerator nodes. Large-scale AI clusters simultaneously manage multiple jobs with varying communication needs.

If a job requires a large amount of inter-group traffic, unrestricted routing can allow data to travel freely across the network. However, it also introduces competition between unrelated jobs, causing unpredictable performance. Furthermore, indirect routing consumes more capacity and increases round-trip time, impacting flow completion time, particularly for small flows.



➤ Figure 2. New network infrastructure for AI clusters, called rail-only, where the spine switches are removed and all the uplinks connecting rail switches to the spine are repurposed as down-links to GPUs.

OCS technology can address this challenge in AI clusters by leveraging topology engineering. In particular, optical switching can be used to effectively "re-cable" all the links of the groups at job launch time, to provide increased bandwidth between the groups involved in that job.

This higher bandwidth reduces the need for indirect routing, thereby potentially reducing latency and increasing delivered end-to-end bandwidth. OCS can also eliminate all network interference between unrelated jobs, while supporting a range of novel network topologies, meaning that the topology can be tailored to suit the communication patterns of individual services [4].

Reducing transmission latency

Some of the most exciting emerging ML applications include mobile Augmented Reality (mobile AR) and Internet of Things (IoT) analytics. However, a major challenge of realising these technologies is that data needs to be processed with tight latency constraints. Network latency during data communication comprises two components: static latency and dynamic latency. Static latency refers to delays associated with data serialisation, device forwarding, and electro-optical transmission. It is determined by the capabilities of the forwarding chip and transmission distance, and has a constant value when the network topology and communication data volume are fixed. Conversely, dynamic latency encompasses delays due to queuing within switches and due to packet loss and retransmission, often caused by network congestion. This component can significantly affect network performance.

Addressing these problems is critical for latency-sensitive ML applications, and OCS technology can eliminate some sources of delay. For instance, optical switches do not entail any per-packet processing, as they allow a shift from traditional optical-electrical-optical (OEO) to all-optical (OOO) interconnects. Latency is therefore set by the speed-of-light propagation delay – 5 ns/m in optical fibre, and 3.3 ns/m in free space. By comparison, an equivalent EPS would add on the order of 10-100 ns of delay per network hop. Additionally, as mentioned above, OCS-enabled topology engineering can rewire fibre links to avoid the use of indirect, higher-latency paths.

Overcoming challenges with software-defined silicon photonics

In light of the challenges outlined above, software-defined photonics emerges as a transformative solution, especially in the context of AI infrastructures. The technology provides greater benefits than MEMs-based optical switching, such as faster reconfiguration time.

Current OCS equipment is limited to coarse-grained reconfigurations, because the switching times exceed milliseconds, limiting its applicability to relatively long-lived applications such as backups and virtual machine migration. This might represent an opportunity for faster switching speed and/or smaller radix, and lower-cost OCS in lower layers of the datacentre network for shorter or more

bursty traffic flows (i.e. ToR to AB traffic) or flexible bandwidth provisioning.

Figure 1 shows a sketch of a software-defined silicon photonics chip that iPronics is developing for interconnect applications. This chip is based on programmable silicon photonics technology [5] and consists of tuneable elements in a mesh architecture that can be controlled by software. Other building blocks can be incorporated to add functionalities including monitoring photodetectors and matrix multiplication.

The system contains a software framework and control system that includes an electronic processing unit (PU), multi-channel electronic driver array (MEDA), and multi-channel electronic monitor array (MEMA) for precise actuation and real-time optimisation.

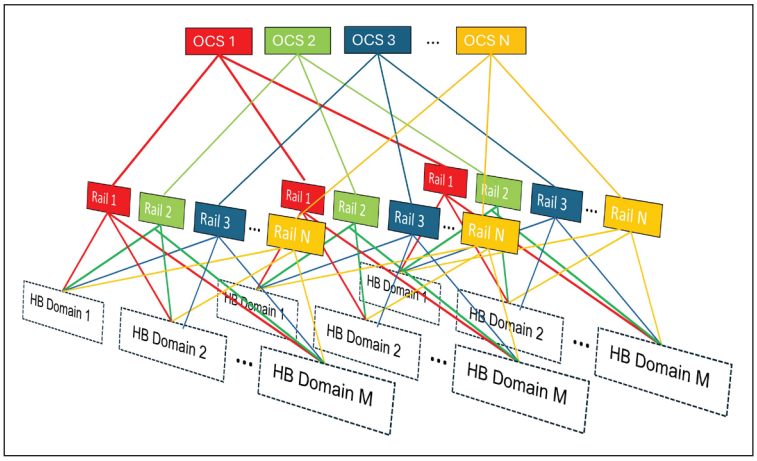
To ensure seamless integration and flexibility, the software layer incorporates application programming interfaces (APIs), enabling interaction between the software and its underlying photonic hardware components. This allows various levels of user interaction, from manual adjustments to fully autonomous configurations, such as integration with software-defined networking (SDN) for advanced network management, optimisation, and automation.

Future AI clusters for heavy ML workloads

The rise of network-heavy ML workloads has led to the dominance of GPU-centric clusters that typically employ two types of connections: (i) a few GPUs residing within a high-bandwidth (HB) domain through a short-range interconnection, and (ii) any-to-any GPU communication using remote direct memory access (RDMA)-enabled network interface cards (NICs) connected in a variant of a Clos network.

However, recent research has demonstrated that network cost can be reduced by up to 75 percent by following a “rail-only” connection. In this new architecture, outlined in Figure 2, LLM training traffic does not require any-to-any connectivity across all GPUs in the network. Instead, it only requires high-bandwidth any-to-any connectivity within small subsets of GPUs, and each subset fits within a HB domain [6].

We therefore suggest using reconfigurable optical switches to provide greater flexibility for interconnections across HB domains even in different racks (see Figure 3). Such a design also allows for the reconfiguration of some connections across rails for forthcoming workloads that behave differently from LLMs. Previous research has shown that µs reconfiguration latency is close to optimal for ML [7]. Software-defined silicon photonics engines offer a µs reconfiguration time, making them particularly suitable for use in optical interconnects for distributed ML training clusters. Building on this, it seems that fast reconfigurable switches are going to be essential in elastic scenarios where the cluster is shared across multiple jobs, with servers joining and leaving different jobs unexpectedly, or when large, high-degree communication dominates the workload.



➤ Figure 3. OCS replacing spine switches, providing high bandwidth and reconfigurability in connecting high-bandwidth domains in different racks.

Our vision at iPronics is that software-defined silicon photonics engines will play a key role in evolving the next generation of AI clusters to optimise dynamic traffic engineering and topology engineering. Offering low transmission latency and a µs reconfiguration time, this OCS technology can fulfil the requirements of new, more cost-efficient AI infrastructures for reconfigurable and flexible optical switches to connect HB domains that can be in distant racks. As AI increasingly reshapes our world, software-defined photonics can support it in realising its transformative potential.

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Quantum PICs: Empowering designers with accurate simulations

Integrated photonics is an exciting potential route to quantum computation and communication. The Ansys Lumerical qINTERCONNECT solver can precisely simulate quantum PICs, enabling engineers to design these circuits without needing extensive quantum mechanics knowledge.

BY SEBASTIAN GITT, RUOSHI XU, AND AHSAN ALAM, R&D ENGINEERS AT ANSYS

OF THE MANY PROMISES of the quantum revolution, two of the most exciting are powerful quantum computing and secure quantum communication channels impervious to tampering. Researchers are making rapid progress in exploring integrated photonics as a potential route to both of these. However, crafting photonic circuits for these applications often demands a profound grasp of quantum mechanics and the nuanced behaviour of qubits – the elemental units of quantum information.

To expedite the advancement of this technology, there is therefore a pressing industry demand for a commercially accessible tool that can empower engineers who have limited quantum mechanics expertise to design and refine these circuits. Furthermore, as these quantum PICs grow larger and more sophisticated, it is increasingly critical to suppress errors due to circuit imperfections, which impede their reliability and scalability.

These flaws include manufacturing variances in circuit components, photons that are not perfectly indistinguishable, and losses in the circuit. Consequently, there is a growing need for simulation tools that can also model realistic quantum PICs. For purely classical photonic chips, the simulation can be performed by commercially available tools like Ansys Lumerical INTERCONNECT, which can accurately model the evolution of a single photon in any PIC by calculating the S-parameter. However, for scenarios with more than one photon, non-classical interference between photons must be accounted for.

Enter the Lumerical qINTERCONNECT solver by Ansys, a cutting-edge solution poised to address this need. By facilitating precise simulation of quantum PICs, compatible with Process Design Kits (PDKs) from photonic foundries, qINTERCONNECT streamlines the design and simulation process for engineers, supporting them to navigate this intricate domain with confidence and ease.

The qINTERCONNECT solver uses the classical scattering matrix from INTERCONNECT to generate a quantum scattering matrix, which can then be used to calculate the evolution of a quantum state in a PIC [1]. By using the quantum state in the Fock (number) basis as input to the solver,

qINTERCONNECT returns the output of the PIC as a density matrix. Additionally, the solver can report the fidelity of the final state with respect to an expected final state and the probability of success for measuring a given output.

Since qINTERCONNECT uses INTERCONNECT as a starting point to simulate the PIC, it benefits from the advanced features of INTERCONNECT. These include the ability to design with PDKs from different photonic foundries, to account for manufacturing variability in photonic components by using statistically enabled compact models, and advanced nonlinear model support for elements like nonlinear optical fibres.

While qINTERCONNECT works in the Fock basis, it supports more exotic inputs in terms of Fock states. Users can encode logical qubit states in terms of physical Fock states, as well as coherent states and squeezed states. Additionally, the output from non-classical photon sources, such as physics-based simulations of optical nonlinearities, can be used as inputs.

Two areas that have recently attracted increased interest are programmable unitary matrices, which have uses across many different areas within quantum photonics, and continuous-variable quantum key distribution (CV-QKD) for secure data communication. qINTERCONNECT, as we will demonstrate, can be used in both of these contexts.

Generating and simulating programmable unitary matrix circuits

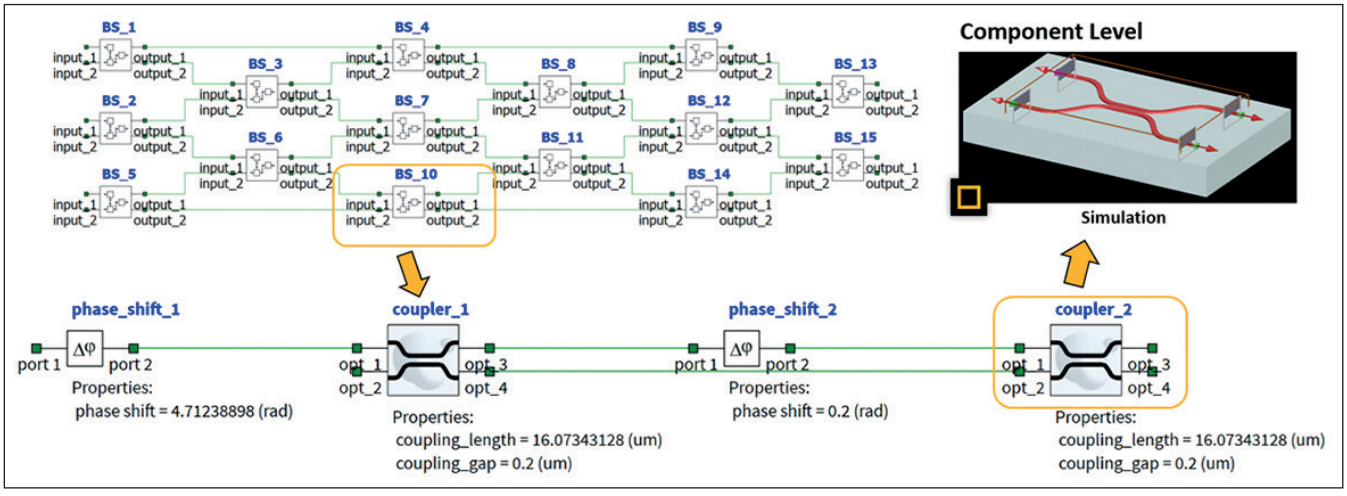
Unitary operations are fundamental building blocks in both classical and quantum linear systems, since any linear operator can be decomposed into a product of unitary and diagonal operators [2]. In classical systems, they are commonly used in applications related to matrix multiplication and neural networks, whereas in quantum systems they can be used for boson sampling, graph similarity algorithms, and the simulation of quantum systems [3-5].

The main principle behind constructing a programmable unitary matrix lies in the fact that an N-dimensional unitary can be factorised into a product of 2-dimensional unitary matrices [6]. Hence, a collection of programmable 2-dimensional unitary matrices can be used to construct a programmable unitary matrix of any size.

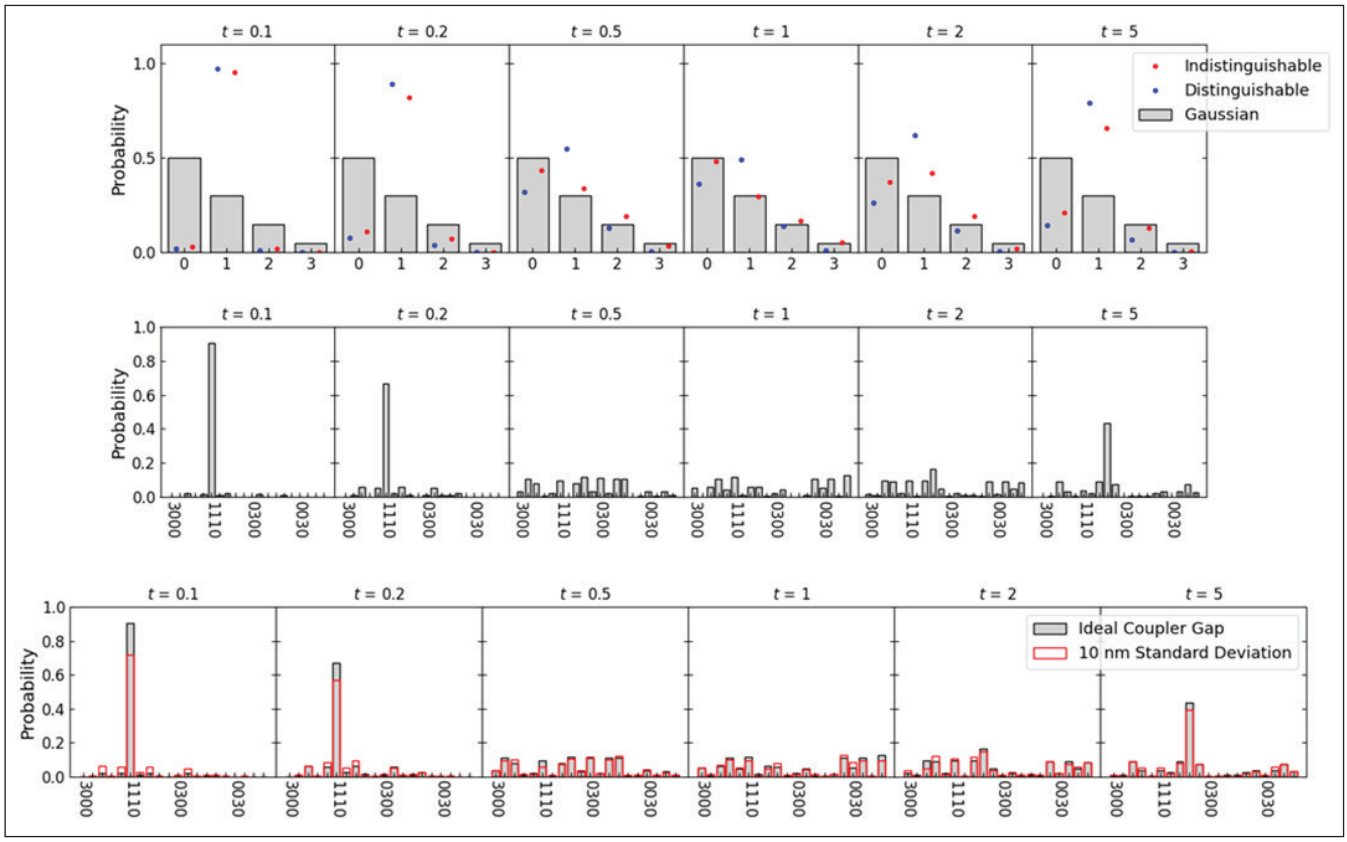
Since Mach-Zehnder interferometers (MZIs) can be used for these 2-dimensional unitary matrices, integrated photonics is a particularly convenient platform for implementing programmable unitary matrices. A common implementation is the so-called Clements decomposition, which improves upon the design of the earlier proposed Reck decomposition by using a symmetrical design that reduces the optical depth of the circuit and is more robust to losses [7].

With Ansys Lumerical qINTERCONNECT, users can construct a PIC in INTERCONNECT representing their own user-defined unitary matrix of arbitrary size. Furthermore, custom circuit elements can be used in the construction of each MZI. This enables workflows where the designer starts with component design with Multiphysics tools like Ansys Lumerical FDTD, CHARGE, or MODE, then generates an accurate, statistically enabled compact model of the optimised element using CML Compiler, and finally creates the PIC in INTERCONNECT to simulate how quantum states will evolve through it.

Furthermore, the user has the option of using more complex MZIs as the fundamental building block in the unitary circuit, which can provide a greater robustness against manufacturing imperfections and losses, at the cost of increased circuit complexity [8]. Figure 1 depicts an overview of how the user constructs the unitary matrix circuit, as well as each hierarchical level of the circuit.



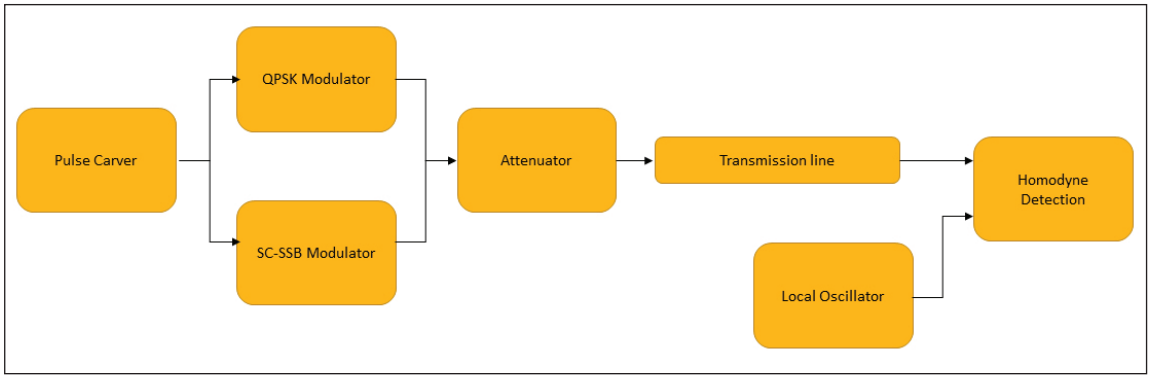
➤ Figure 1. A circuit for a user-defined unitary matrix of any size can be constructed using Ansys Lumerical qINTERCONNECT. Using the Clements decomposition method, the circuit consists of a square mesh of beamsplitters, which in turn can be customised by the user to contain custom components or to be a different geometry altogether.



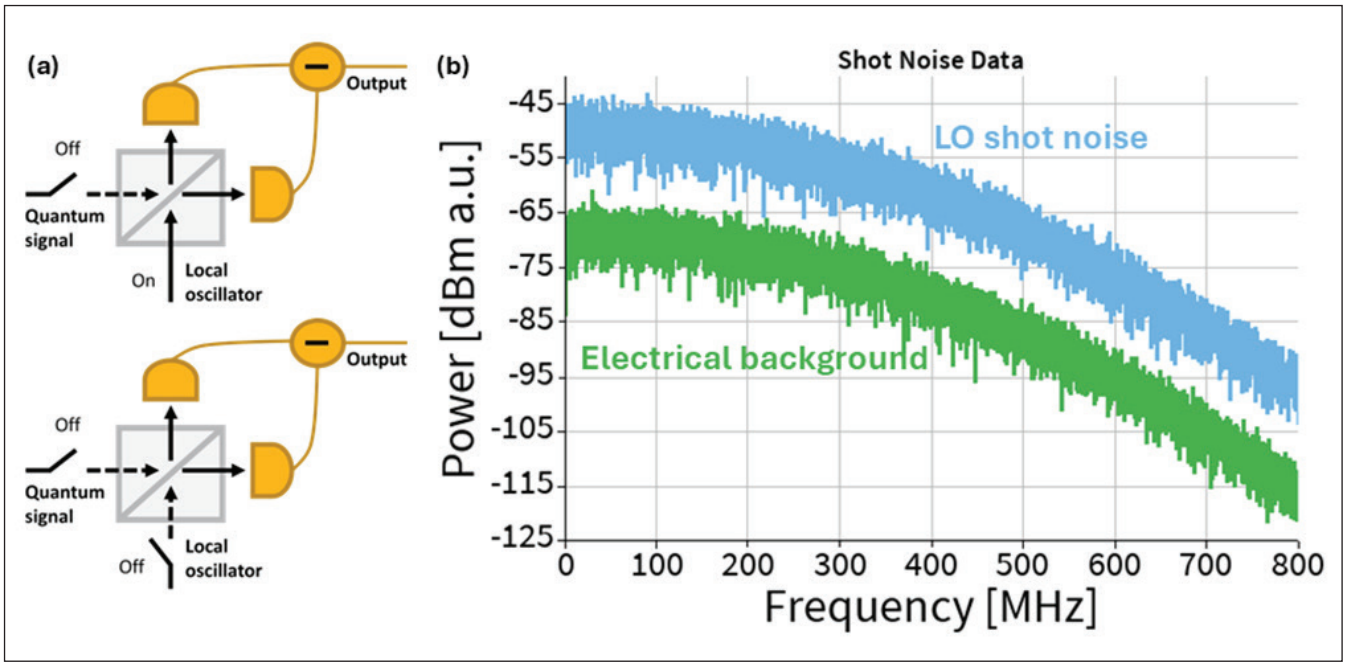
➤ Figure 2. (a) The probabilities of measuring up to three photons in the first channel of the output of the unitary matrix circuit for an input state of indistinguishable photons |1,1,1,0⟩ (red) and a state of distinguishable photons (blue) at six different interaction strengths, represented different times, as in [7]. (b) The probabilities of measuring any given output state across all four channels at the output of the unitary matrix circuit for the same indistinguishable state as in (a). (c) Same as (b) but coupling gap values are taken from a normal distribution with a mean value equal to the ideal coupling gap value of 200 nm and with a standard deviation of 10 nm.

Once the INTERCONNECT project file containing the programmable unitary matrix circuit has been generated, it is ready for simulation in qINTERCONNECT, a quantum circuit solver that can calculate the frequency domain response of a PIC in the Fock, or photon number, basis. The solver takes the classical S-parameters given by INTERCONNECT and uses them to calculate a quantum S-matrix (QS-matrix), which relates input and output states defined in a Fock basis prescribed by the number of channels and a maximum total number of photons.

The QS-matrix specifies the quantum mechanical state of light exiting the circuit in terms of the non-classical input state. Consequently, the qINTERCONNECT solver enables users to specify an input state in the Fock basis, either as a state in bra-ket notation or a density matrix, and the solver will yield the output state in terms of probability amplitudes for measuring discrete photon detection patterns in the output channels. Furthermore, if a target output state is supplied, the solver can also calculate the fidelity.



➤ Figure 3. An overview of the pilot-assisted CV-QKD circuit, from transmitter to receiver, being simulated in INTER-CONNECT.



➤ Figure 4. (a) Calibration of the shot noise variance is accomplished by measuring the shot noise from the detector when the signal is disconnected and the LO is connected, and the electronic noise from when both the signal and LO are disconnected. (b) The power spectra for the shot noise and electronic noise.

As an example, the qINTERCONNECT solver can be used to construct a photonic circuit to model the unitary evolution of a non-interacting Bose-Hubbard model, or "hopping" Hamiltonian with four sites. It can then simulate the probabilities of success for various measurement outcomes for three-photon input states of both distinguishable and indistinguishable photons.

A simulation was performed using an input state of |1,1,1,0>, corresponding to one photon in each of the first three channels and no photon in the final channel. Figure 2a and 2b show the measurement results for the output of the first channel using both distinguishable and indistinguishable photons, as well as the results for measuring all four channels using an input state consisting of indistinguishable photons, which agree with established results [5]. Using this workflow, it is possible to characterise the impact of manufacturing uncertainty on these measurement outcomes. For example, users can vary the coupler gap spacing in the directional coupler elements that make up each MZI in the unitary circuit, and then repeat the simulations, as illustrated in Figure 2c. Here, the coupling gap values are drawn from a distribution with a standard deviation of 10 nm, modelling the effects of fabrication variance. The impact this has on the measured probabilities of detecting various output states is clearly demonstrated.

Continuous-variable quantum key distribution

Ansys Lumerical tools can also be used to model circuits for continuous-variable quantum key distribution (CV-QKD). In these applications, keys are encoded in the quadrature components of strongly attenuated coherent states using quadrature phase shift keying (QPSK). Since the information in the quadrature components can be read out using homodyne detection, CV-QKD can be fully implemented using well-established telecom technology. This stands in contrast with discrete-variable QKD, which requires single-photon sources and detectors.

An eavesdropper intercepting the quantum signal will necessarily introduce additional noise into a CV-QKD system, which can be detected by the receiving party. If the noise level inherent in the system is minimised, the additional noise introduced due to the eavesdropper can be detected, and the protocol can be aborted until the channel is determined to be secure. Since the amount of

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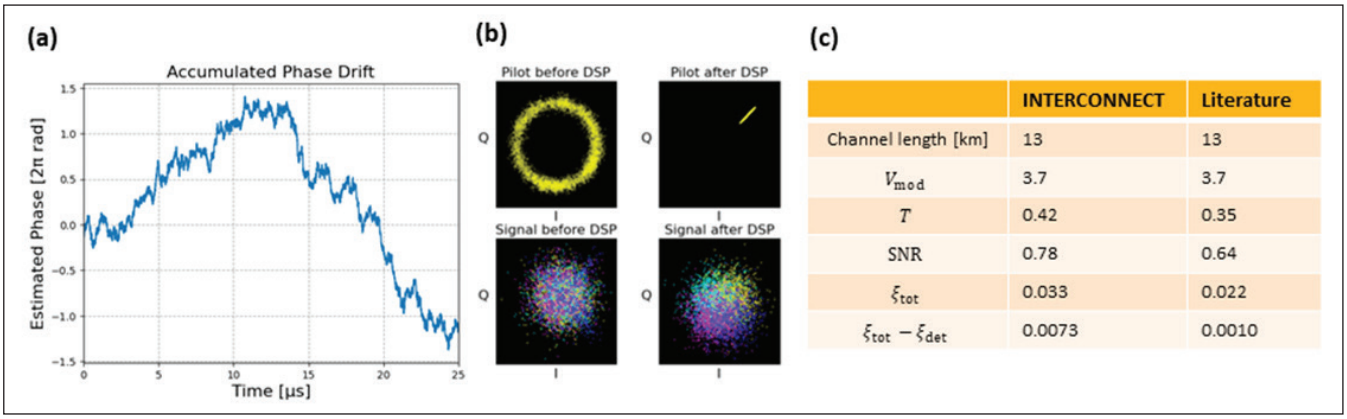

	INTERCONNECT	Literature
Channel length [km]	13	13
V_{mod}	3.7	3.7
T	0.42	0.35
SNR	0.78	0.64
ξ_{tot}	0.033	0.022
$\xi_{tot} - \xi_{det}$	0.0073	0.0010

➤ Figure 5. (a) Accumulated phase drift over time between the pilot and the LO. (b) Digital signal processing (DSP) is performed using the measured quadrature values of the pilot tone to correct to the phase of the quantum signal. (c) Comparison of simulated parameters in INTERCONNECT against experimentally determined values [9].

noise tolerated in the system before the protocol is aborted is so low, it is important to be able to simulate the noise in the system accurately.

Given that the coherent states are weak, they cannot be used as an accurate phase reference to recover the encoded keys. However, a stronger pilot reference can be transmitted alongside the quantum signal for phase correction at the receiver side. To avoid crosstalk between the pilot and the signal, the pilot can be first shifted to a different frequency using suppressed carrier single-sideband modulation (SC-SSB), and then rotated to an orthogonal polarisation [9]. In addition, a pulse carver can be used to reduce the information that can be obtained from monitoring the transition between symbols. Figure 3 depicts an overview of the full CV-QKD circuit.

The most important figure of merit for a QKD system is the secure key rate, which, in general, is improved by minimising noise and losses in the system. Consequently, the goal of the simulation is to determine the transmittivity and total excess loss, the latter of which is attributable to the eavesdropper and must therefore be kept as low as possible.

Since the transmittivity and excess noise must be given in shot noise units, the first step is to perform a shot noise unit calibration, which consists of two simulations. First, the transmission line is disconnected from the receiver and a simulation is performed with only the local oscillator (LO) connected to the homodyne detectors to measure shot noise plus noise intrinsic to the detector. Next, a second simulation, with the LO disconnected, measures detector noise. The variances of both measured voltage values are subtracted to obtain the shot noise variance. These two steps are then repeated eight times to obtain an averaged value for the shot noise calibration. Figure 4 shows the power spectra for the shot noise and electrical background noise.

After the shot noise calibration is complete, a simulation is performed with the transmitter connected to the receiver and the measured quadrature values are normalised by the previously measured shot noise variance, which is necessary to relate the measured results to the language of Gaussian information [10]. As before, the results are averaged over eight simulations. Then, the pilot tone is used to correct the phase drift between the LO and the signal.

Next, a fraction of the key information is disclosed between the sender and the receiver, which allows the receiver to calculate the transmittivity and the total noise in the link. If the receiver is inaccessible to an eavesdropper, the receiver noise can, under a relaxed security assumption, be treated as trusted noise, and is no longer attributed to the eavesdropper. In this case, the total noise minus detector noise will be another important figure of merit (ξ_{tot} - ξ_{det}). Comparing the simulated parameters to those obtained experimentally and reported in the literature, we can see consistent results in the transmittivity (T), signal-to-noise ratio (SNR), and total noise (ξ_{tot}), as shown in Figure 5.

Since the transmittivity is affected not only by the transmission channel losses but also by detector losses and any coupling losses between the transmission channel and the detector, its value will be strongly dependent on the details of any given experimental implementation. Then, assuming a reconciliation efficiency value of $\beta = 0.97$, a frame-error rate of FER = 0.05, and a fraction disclosed for parameter estimation of $\nu = 0.25$, and using the parameters in Figure 5, the secret key rate is found to be 38.0 Mbit/s over 13 km [9].

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A versatile tool for designing and refining quantum PICs

Thanks to Ansys Lumerical qINTERCONNECT, you no longer need to be an expert in quantum mechanics to design a functional and effective integrated quantum photonic circuit. By leveraging foundry PDKs and advanced statistical and nonlinear compact models for different building blocks in their PICs, designers can account for issues originating from fabrication variations, propagation losses, and indistinguishable photons.

Designers can investigate the evolution of quantum states propagating through their quantum PICs using various types of sources ranging from physical Fock states to logical qubit states, such as coherent states or squeezed states to even non-classical photon sources. This makes qINTERCONNECT a versatile tool for the design and evaluation of integrated quantum photonic circuits.

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A bright future for the global PIC market

The latest report from IDTechEx predicts that the global PIC market will see robust growth, reaching $22 billion by 2034. But which applications are likely to grow the most? And what commercialisation challenges do PICs still face?

BY JAMES FALKINER, TECHNOLOGY ANALYST AT IDTECHEX

FROM SENDING and receiving billions of bits of information in a package the size of a candy bar to detecting different molecules in the air with remarkable sensitivity, PICs are a powerful technology that can be adapted for a wide range of uses. These tiny optical systems, made of materials such as silica (glass), silicon, and indium phosphide (InP), have already experienced commercial success in telecoms and datacoms, and show plenty of promise for future growth.

By leveraging the billions of dollars of investment in CMOS chips, for instance, PICs can unlock new potential for scaling information processing beyond Moore's law.

However, there remain significant challenges for the PIC market, such as material limitations, integration complexity, and cost management. Large demand volumes are required to offset the high initial costs of designing and manufacturing PICs, while production lead times can take months.

IDTechEx's new PIC report thoroughly investigates the market for this technology and identifies photonic transceivers for AI as an emerging segment that will soon be the largest source of demand for photonic chips. This is because PICs can overcome some of the challenges faced by traditional optical transceivers, including data limitations associated with bandwidth, modulation speeds, and noise. PIC-based transceivers can thus send more data in a similar form factor.

Figure 1 shows a traditional pluggable optical transceiver on the left with large independent transmitter optical sub-assembly (TOSA) and receiver optical sub-assembly (ROSA) circled in orange. On the right is a PIC-based transceiver of a similar size, but which offers 10 times the performance thanks to the large PIC-based TOSA under a heatsink. Under that heatsink is a PIC that controls the transmitting laser (bonded to the PIC), modulator systems, and passive optical components used for wavelength-division multiplexing (WDM), a method used to increase the data rate.

Materials on the horizon

Although silicon photonics has generally been the most widespread platform for commercial PIC devices, researchers in both academia and industry are investigating alternative materials for various applications.

As part of our analysis of the PIC market, IDTechEx has evaluated some emerging and popular materials. We compare important performance metrics, such as cost, scalability, losses (power lost per metre), and modulation performance. The latter is defined as how quickly a material changes when exposed to an electric field, and is a critical factor for high-performance transceivers.

Although most of the current market uses silicon- and silica-based PICs for light propagation, silicon, as an indirect semiconductor, is not an efficient light source or photodetector. Therefore, it is usually combined with III-V materials, like InP, for photon emission and photodetection functionalities.

Silicon's market dominance looks set to continue. However, thin-film lithium niobate (TFLN), with its moderate Pockels effect and low material loss, is emerging as a strong contender for applications that require high-performance modulation, such as quantum systems and potentially also future high-performance transceivers. Monolithic InP continues to be a major player due to its light detection and emission abilities. Additionally, innovative materials like barium titanate (BTO), electro-optical polymers, and rare-earth metals are being explored for their potential in quantum computing and other cutting-edge applications.

AI impacts

The rise of artificial intelligence (AI) has spurred an unprecedented demand for high-performance transceivers capable of supporting the massive data rates required by AI accelerators and datacentres. Silicon photonics and PIC technologies are at the forefront of this revolution, with their ability to transmit data at speeds of 1.6T and beyond.
As shown by Nvidia's latest Blackwell CPUs, which, according to our research, require approximately two 800G transceivers per GPU, the need for efficient, high-bandwidth communication is becoming more critical for AI, positioning silicon photonics and PICs in general as essential components in the AI-driven future. Indeed, the biggest driver of PIC-based transceiver development is AI, since higher-performance AI accelerators will require higher-performance transceivers, with 3.2T transceivers expected to arrive by 2026, as indicated in Figure 2. Based on past trends, we forecast that future AI accelerators will require two optical transceivers per accelerator on average on launch, with in-generation transceiver improvements resulting in a lower transceiver per accelerator ratio throughout the estimated eight-year lifespan of an accelerator.

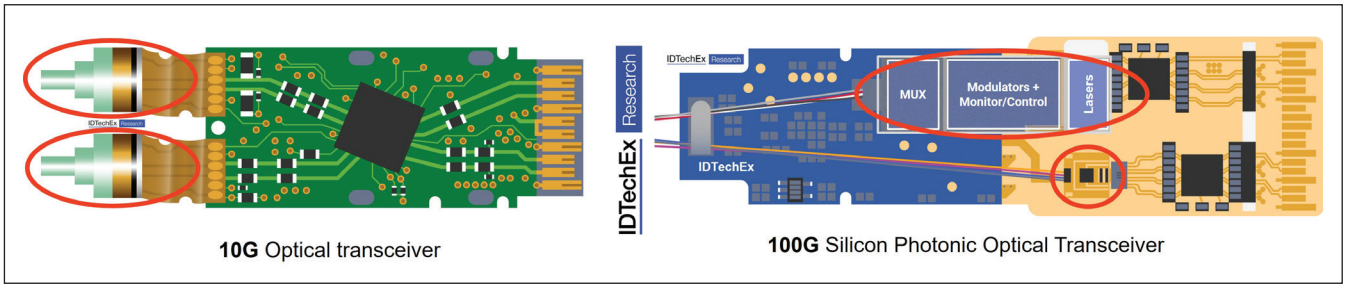
The AI accelerator market is set to see significant short-term growth with the H100 and B100 GPUs, alongside Google, Microsoft, and Amazon's upcoming dedicated products. Beyond 2026, IDTechEx forecasts that the market will not see the same level of demand that we see in 2024, due to a slowdown in datacentre growth, and satisfaction with and consolidation of the current emerging AI and large language model (LLM) market.

In the short term, we expect to see rapid growth in global datacentre numbers. However, datacentre spending is set to slow beyond 2026 as datacentres start to satisfy global AI demand. Beyond 2030, datacentre performance and capability will be improved through the renovation and refitting of existing datacentres with faster AI accelerators, satisfying AI demand and leading to reduced numbers of new datacentres.

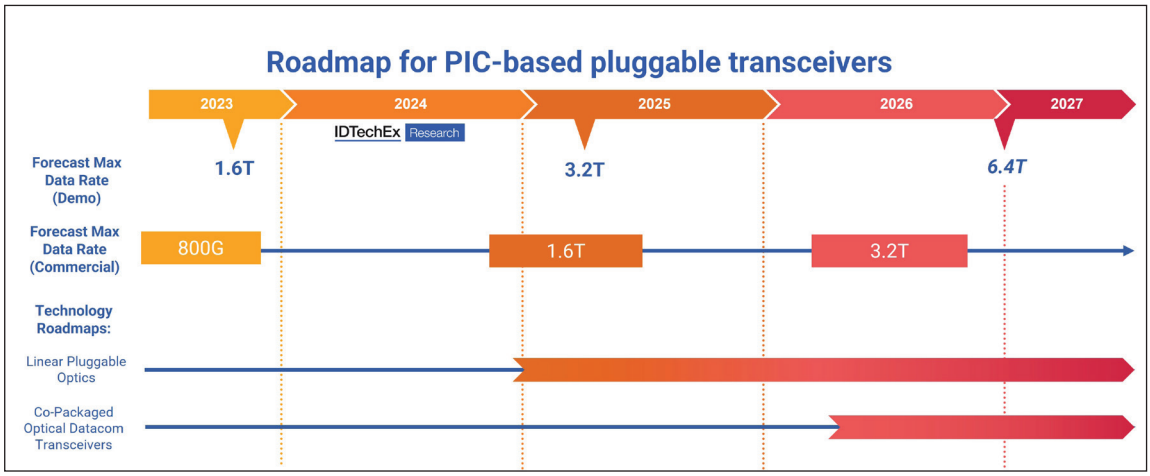
According to our analysis, datacentres already use about 1 percent of the world's energy, so there is a limit to how much they can grow before they start running into wider electrical infrastructure limitations. Datacentre growth is likely to have a significant impact on the PIC market, as PIC-based transceivers are a critical component for transferring data to, from, and within this infrastructure. IDTechEx forecasts that by 2034, there will be over 15 000 datacentres globally.

Emerging applications

Silicon photonics and other kinds of PICs are being used to innovate new solutions in a wide range



➤ Figure 1: A traditional pluggable optical transceiver (left) compared with a PIC-based transceiver (right). The PIC-based transceiver offers around 10 times the performance of the traditional transceiver, despite being a similar size, thanks to a transmitter optical sub-assembly (TOSA), which is situated under a heatsink and contains passive optical elements that increase the data rate through wavelength-division multiplexing.



➤ Figure 2: A roadmap for PIC-based pluggable transceivers. 3.2T transceivers are expected to arrive by 2026.

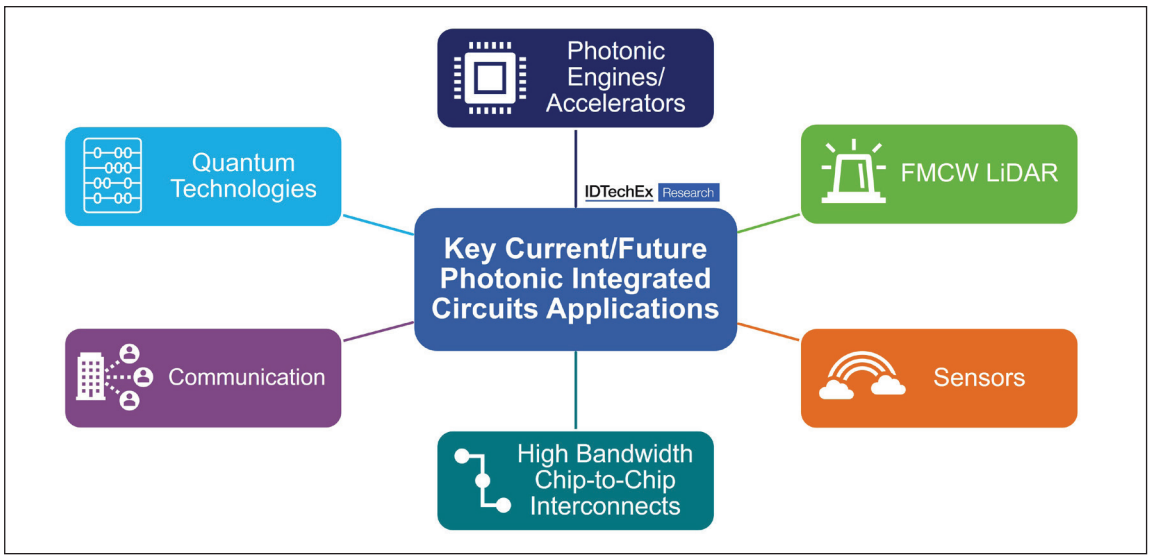
of fields, as illustrated in Figure 3. IDTechEx has explored several of the most prominent applications and the advantages they can offer within their respective industries.

First, within the area of photonic engines and accelerators, photonic components such as Mach-Zehnder Interferometers and low-loss waveguides can be used to design and manufacture high-performance photonic processors and programmable PIC devices. This could unlock higher performance than is possible with electronic accelerators alone. These photonic accelerators can perform certain mathematical functions extremely quickly, potentially having applications in machine learning and AI matrix operation.

In the sensor market, PIC materials, such as silicon nitride, can enable a range of different technologies, from gas sensors to "artificial noses." The healthcare sensor industry may be able to take advantage of the miniaturisation of optical components into PIC devices, which could see applications in point-of-care diagnostics or wearable tech. Meanwhile, PIC-based frequency-mode continuous-wave (FMCW) LiDAR has the potential to transform the automotive and agricultural industries, with applications in drones and autonomous vehicles. As the quantum revolution continues to unfold, companies investing in quantum computing based on trapped ions and photonic qubits are looking to PICs for more stable and scalable quantum systems. PICs are used in photonic quantum systems to achieve the precise control of photons necessary for quantum computation.

Another promising application area for PICs is in high-bandwidth chip-to-chip interconnects. By taking advantage of co-packaged optics (CPO) and external lasers, PICs can be used to replace copper interconnects within AI accelerator systems, offering greater bandwidth and better power efficiency at high data rates. IDTechEx expects to see significant adoption of CPO in 2026/2027.

Finally, the industries in which integrated photonics is already most established are telecoms and datacoms, both of which employ PIC-based transceivers. The volume of units associated with the telecoms (long-distance data transmission) market is smaller than that associated with the datacoms market. However, the cost per transceiver is much higher in telecoms, often 10 times the price, making this market relatively lucrative.



➤ Figure 3: PICs have a wide range of applications, some of which they are already well established in, and others which are still on the path to commercialisation.

In telecoms, PIC-based dense-wavelength division multiplexing (DWDM) transceivers are critical for aggregating the signals from 5G base stations to distribute to the wider network. DWDM transceivers can combine the data of several 5G base stations within a backhaul connection. IDTechEx forecasts strong growth in the 5G market, with 5G PIC transceivers set to benefit.

The rest of the telecoms market is set to slow, growing at a 1 percent CAGR. Pluggable PIC telecom transceivers are used to send data hundreds of kilometres at high data rates, taking advantage of WDM to maximise the data rate sent through one optical cable. As discussed previously, datacoms (short-distance data transmission) is a fast-growing market due to AI-driven datacentre growth.

Market forecast

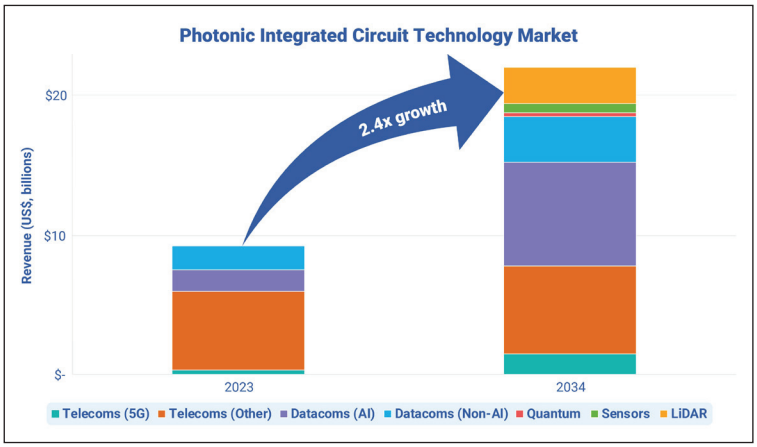
The overall PIC market is set to grow to over $22 billion by 2034, with a CAGR of 9.1 percent. As shown in Figure 4, we expect this growth to be primarily due to AI-associated demand for datacom transceivers. PIC-based LiDAR is expected to benefit from growth in the autonomous vehicle market, as well as having applications in agricultural and aerospace markets.

PIC-based sensors for wearables, point-of-care, and gas detection will likely each take a small percentage of their respective markets, although they are unlikely to dominate them. A quantum computer is unlikely to be fully commercialised by 2034 but will still represent a noticeable market size. Quantum systems will probably be a significant application for PICs by 2044.

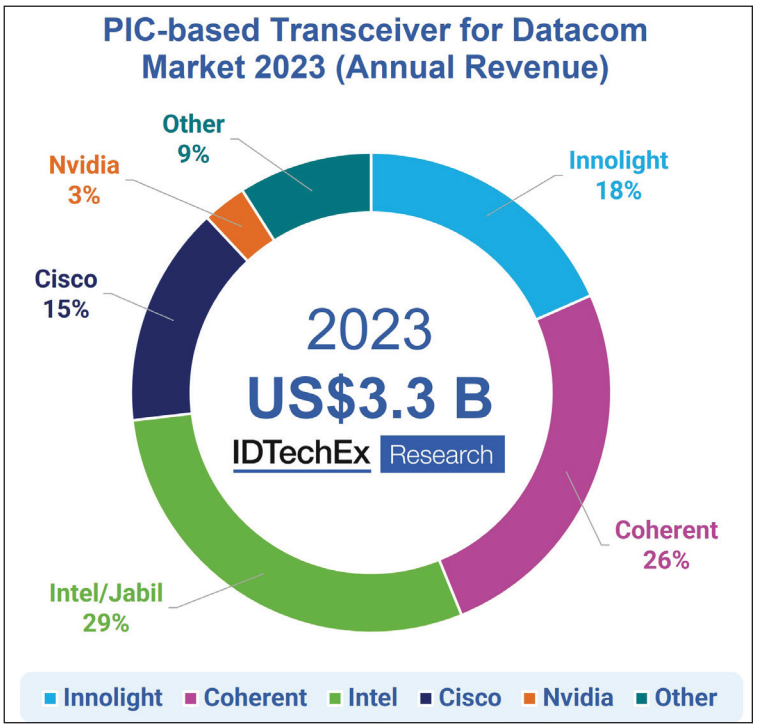
Overall, the market for silicon photonics and PICs is experiencing robust growth, driven by the surge in AI and datacom transceiver demand. Key players in the industry, such as Intel/Jabil, Coherent, and Infinera, are actively using PICs within their transceivers. Figure 4 shows the market share of these and other major firms in the PIC-based datacoms transceivers space in 2023.

Innolight, a China-based transceiver company, hit 1.6T of transfer speed in their most recent products in late 2023, which are due to start shipping for datacentre applications in 2024. Coherent, which has its own InP wafer fab facilities, is also developing higher-performance transceivers for 1.6T+ applications.

According to our analysis, Intel Silicon Photonics, which is potentially going to be acquired by manufacturing firm Jabil, sold about 1.7 million PICs in 2023, and is continuing to develop datacom and telecom transceivers. IDTechEx forecasts that PIC technology will continue to dominate the high-performance transceiver market, further solidifying its position as a critical component in the modern technological landscape.



➤ Figure 4: The global PIC market is forecast to grow by a factor of 2.4 to a value of $22 billion over the next decade. Datacom transceivers needed to satisfy the demand for AI are expected to be the biggest driver of this growth.



➤ Figure 5: The major players in PIC-based transceivers for datacoms and their market shares in 2023.

FURTHER READING

- IDTechEx market report: “Silicon Photonics and Photonic Integrated Circuits 2024-2034: Market, Technologies, and Forecasts” www.IDTechEx.com/SemiPIC
- IDTechEx webinar: “Photonic Integrated Circuits: Materials, Forecasts, and How AI Accelerator Demand Is Affecting the PIC Market”

Harnessing InP for applications beyond optical communications

Photonic chips are well established in optical communications markets. However, InP PICs are now proving versatile, as they are increasingly adapted to unlock other applications, from AI and neuromorphic computing to quantum technology and sensing.

BY PAUL MOMTAHAN, DIRECTOR OF SOLUTION MARKETING, INFINERA

SINCE ITS INCEPTION several decades ago, photonic integration technology has delivered a plethora of benefits, which have so far been reaped largely by the telecom industry. Fundamentally, PICs perform multiple photonic functions on a single chip, as outlined in Figure 1. As is the case with conventional electronics, manufacturing one high-function chip is far more cost-effective than manufacturing lots of individual optical components and then integrating and packaging them.

Additionally, by enabling device miniaturisation, photonic integration can dramatically reduce footprint, exemplified by the evolution from large coherent transponder modules to compact digital coherent pluggables in a wide range of small form factors. PICs also offer reduced power consumption, as well as improved performance due to minimised coupling losses when connecting photonic functions with waveguides inside the PIC, as opposed to coupling optics between discrete components. Since these external coupling losses are eliminated as a source of failure, equipment failures, too, are less frequent.

Having proven their value in the telecom industry, PICs are now also being explored as a potential enabling technology in a wide range of other

fields. From AI and neuromorphic computing to quantum technology and sensing, integrated photonics – and the indium phosphide platform in particular – is a versatile tool that could supercharge the development of numerous transformative applications.

A brief history of PICs

The concept of combining multiple optical components in a single circuit has been around for 55 years, since Stewart Miller of Bell Labs published a paper called "Integrated optics: An introduction" in 1969 [1]. This paper proposed a PIC consisting of a single integrated laser and modulator and suggested that savings would result from the use of photonic integration.

Then, in 1987 two papers further described integrating a laser and a modulator, one by researchers at KDD Research & Development Laboratories in Japan [2], and the other by a team at NTT Electrical Communication Laboratories [3]. The latter demonstrated an electro-absorption-modulated laser (EML) in a monolithic indium phosphide (InP) PIC, though these were only successfully commercially deployed later, in 1995.

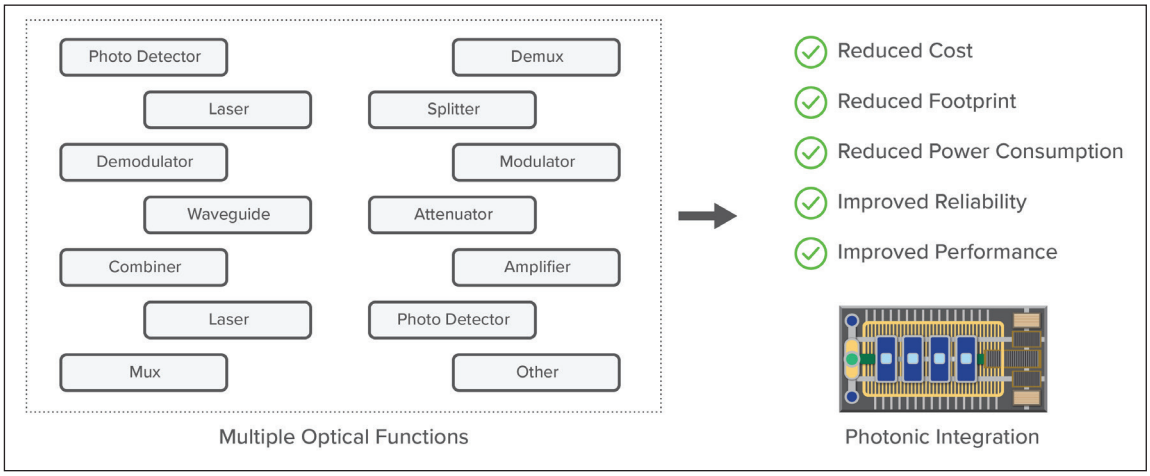
In 1988, Bookham Technologies, now part of Lumentum, was founded in the UK and went on to become the first company to make optical components that could be incorporated into silicon integrated circuits. In the early 1990s, Meint Smit at Delft University of Technology started pioneering in the field of integrated photonics and is credited with inventing the arrayed waveguide grating (AWG). In 1986, Richard Soref and Joseph Lorenzo published their seminal paper: "All-silicon active and passive guided-wave components for λ = 1.3 and 1.6 μm" [4]. Infinera, founded in 2000 as Zepton Networks, released its first products leveraging the industry's first large-scale monolithic PICs in 2004. These PICs, one for transmit and one for receive, integrated all the components for the transmitter and receiver respectively for 10 x 10G direct-detect wavelengths in a single monolithic device. Combined with Infinera's optical transport network (OTN) switching technology in the delay-tolerant networking (DTN) product, these PICs transformed the economics of long-haul transport by addressing the challenge of expensive optical-electrical-optical (OEO) conversion and regeneration.

Infinera selected InP as the material for its PICs because it can support a wide range of functions, including laser and optical amplification at dense wavelength-division multiplexing (DWDM) wavelengths, i.e. the C-band (1529-1567 nm) and the L-band (1569-1610 nm). An additional advantage that has become increasingly important is its inherently superior modulation effect compared to silicon [5], which is especially valuable for the highest-performance segment of the DWDM transceiver market as baud rates evolve to 200 GBaud and beyond.

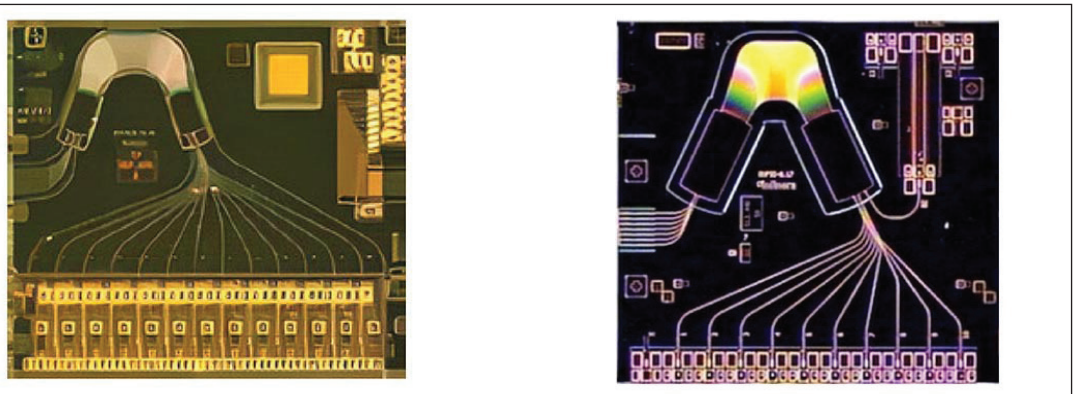
Metro, long-haul, and submarine

Photonic technology plays a critical role in optical communications, supporting the transmission of tens of terabits per second over the submarine and long-haul terrestrial fibres that form the backbone of the internet, while also facilitating high-speed metro, mobile backhaul, and broadband access networks. Specifically, these metro, long-haul, and submarine networks are powered by coherent optical engines, which incorporate multiple components and functions, including the digital application-specific integrated circuit (ASIC), often referred to simply as the digital signal processor (DSP), an analogue ASIC that integrates multiple drivers and transimpedance amplifiers (TIAs), and the photonics.

The photonic components in the coherent optical engines include the laser that generates light with the desired wavelength and a modulator that takes the light from the laser and encodes the data by changing the phase and amplitude. The coherent modulator itself encompasses four individual Mach-Zehnder modulators (MZMs), as well as beam splitters, combiners, phase shifters, a polarisation rotator, and a polarisation beam combiner. The receive side, meanwhile, has photodetectors and passive photonics, including a polarisation beam



➤ Figure 1: Benefits of photonic integration for optical communications.



➤ Figure 2: Infinera's first large-scale monolithic PICs, released in 2024. 10 x 10G transmitter PIC (left) and 10 x 10G receiver PIC (right).

splitter and 90 degree hybrid coupler. Infinera's coherent InP PICs integrate all the transmit and receive photonic functions for one, two, or even six wavelengths on a single PIC.

The PICs that are indispensable in today's communications networks show that integrated photonics has come a long way in the decades since it was first conceived. But the telecoms industry is only the start; this sophisticated technology can be adapted for use in a wide array of other systems, potentially helping to realise game-changing new applications and accelerate them to market.

AI datacentres and neuromorphic computing

Generative artificial intelligence (AI) is having a huge impact on the world, not only in terms of how people are using it in their daily lives, but also in terms of the demands placed on the datacentres that provide access to it. There is currently a mismatch between the growth rate of generative AI models and that of the infrastructure they require. In two years, the number of parameters in these models scales by a factor of 100, and the GPUs they run on increase their performance by a factor of 3.3. Meanwhile, in the same two-year period, interconnect bandwidth increases by a factor of just 1.4. In other words, the growth of AI models is currently outpacing the growth of data transfer capacity it requires.

GPU clusters for generative AI are currently scaling by a factor of 10 every three years, with the present state of the art being 32,000 GPUs in a cluster. These clusters will require massive amounts of optical interconnects, with low power and low latency both being critical. Leveraging the low power requirements of InP modulators, low loss of InP, and ability to integrate gain functions including lasers and semiconductor optical amplifiers (SOAs), monolithic InP PICs provide an ideal-material platform for high-speed intra-datacentre optics.

PICs such as Infinera's newly announced ICE-D products can integrate optical functions including distributed feedback (DFB) lasers and arrays, ultra-low-voltage MZMs, low-switching-voltage electro-absorption modulators, and photodiode arrays, making them a compelling option for scaling intra-datacentre optics to 1.6T, 3.2T, and beyond.

Furthermore, these versatile InP PICs can be used with a variety of different optical setups. For example, they are compatible with today's retimed pluggable optics (RPO), which have DSP functions for transmit and receive, as well as new industry initiatives such as linear-drive pluggable optics (LPO), which remove the DSP from the pluggable optics. They can also be used with pluggables that that have a DSP function only for transmit, referred to as linear receive optics (LRO) or half-retimed linear optics (HALO), and co-packaged optics (CPO), which replace pluggable optics with optics packaged with the switching silicon.

Another way in which InP PICs could advance AI and machine learning (ML) is through the field of neuromorphic computing. This area of research seeks to build computer chips with neural networks embedded in the hardware itself, as opposed to running neural network software on conventional processors.

Internally, these chips require massively parallel interconnections, making InP PICs a strong candidate, with optical waveguides replacing the metallic interconnects in an electronic integrated circuit. Eindhoven University of Technology demonstrated this type of device in 2020 with an InP PIC as shown in Figure 2 [6]. As the field evolves, photonic neuromorphic processors could become a key enabling technology to harness the power of AI/ML for wide-ranging applications, including high-energy particle physics, fusion reactor control, and nonlinear optimisation for robotics and autonomous vehicles.

Quantum tech and photonic sensing

Another area getting a lot of attention and investment is the field of quantum technology. Since InP's properties enable quantum effects at the individual photon level, PICs based on this material could be a key technology in achieving the exciting goals of the quantum revolution. For example,

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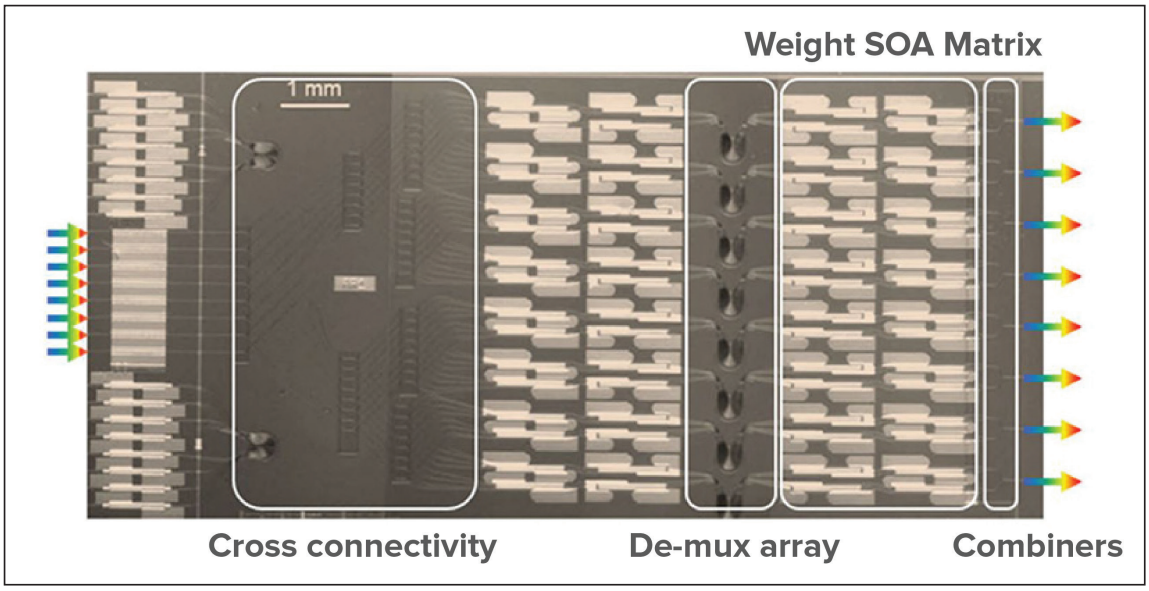

➤ Figure 3: InP PIC for photonic neuromorphic computing (Eindhoven University of Technology, 2020)

InP colloidal quantum dots could be a less toxic alternative to today's cadmium-based quantum dots for use as single-photon sources.

Meanwhile, researchers are also investigating the material's potential for use in quantum-safe cryptography. Quside, a startup based in Barcelona, Spain, has developed a high-performance random number generator based on an InP PIC that has tremendous potential as an enabler for quantum-safe encryption. This random number generator could also facilitate faster and more energy-efficient simulations, which are needed to produce, for example, weather forecasts and risk analyses in the financial sector.

Yet another key emerging application for InP PICs is sensing. The material is already used for short-wave infrared (SWIR) sensors and edge-emitting laser (EEL) proximity sensors; the third generation of Apple AirPods were the first device to leverage InP SWIRs in 2021, while the iPhone 14 Pro was the first to use an InP EEL. 3D sensing in smartphones and tablets, which is used for applications including facial recognition, currently uses gallium arsenide (GaAs) vertical-cavity surface-emitting laser (VCSEL) arrays. However, this is also expected to evolve to InP, as the notch in the phone shrinks to a dot. This is because InP-generated light at 1310 nm can pass through the OLED screen transparently, unlike GaAs-generated light, which is in the range of 780-980 nm.

In the area of automotive LiDAR, moving to InP offers another advantage over today's GaAs-based solutions; since InP-generated light can operate in the mid-infrared range, it can offer higher laser power without posing a risk to pedestrian eye safety, unlike the near-infrared range of incumbent GaAs-based LiDAR. The material can thus facilitate longer ranges of more than 200 m. Moreover, InP LiDAR can leverage frequency-modulated continuous wave (FMCW), rather than today's time-of-flight (TOF) techniques. Whereas the latter measures only the distance and direction of detected objects, the former also measures their velocity, enhancing accuracy and safety.

Finally, the mid-infrared frequency range can also be applied to medical use cases. For instance, it could expand the monitoring capabilities of wearables like smart watches to include blood markers such as glucose, lactate, and alcohol.

All these examples offer a glimpse into the myriad fields that InP PICs are now flourishing in. Although they have so far primarily been developed for telecoms, underpinning the coherent transceivers used in communications networks, their potential is increasingly being tapped for diverse and potentially world-changing technologies. As we strive towards a future with larger generative AI datacentres, new computing paradigms, quantum cryptography, safe autonomous vehicles, and non-invasive medical monitoring, InP PICs may be an essential part of helping us get there.

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- [3] "Monolithic integration of a DFB laser and an MQW optical modulator in the 1.5 μm wavelength range" by a team at NTT Electrical Communication Laboratories
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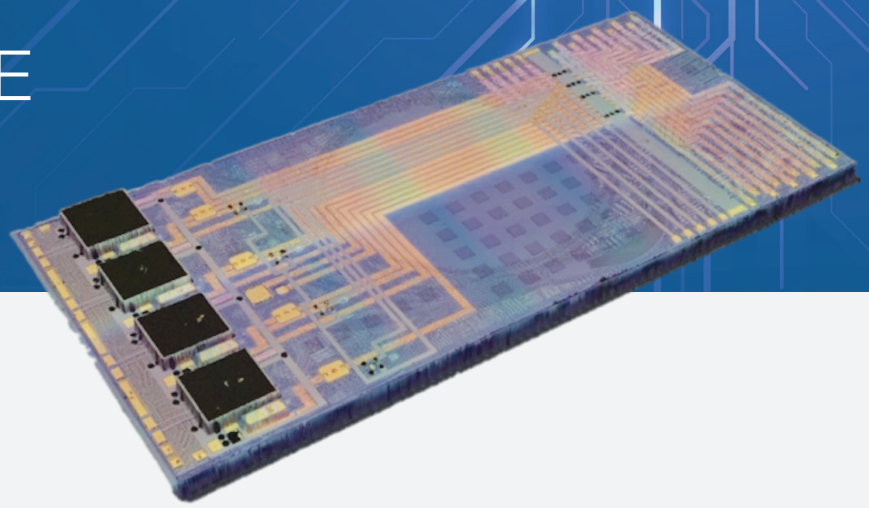

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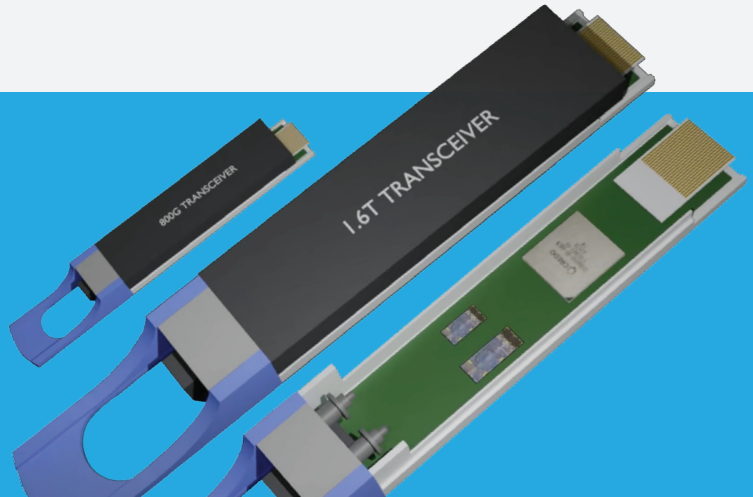

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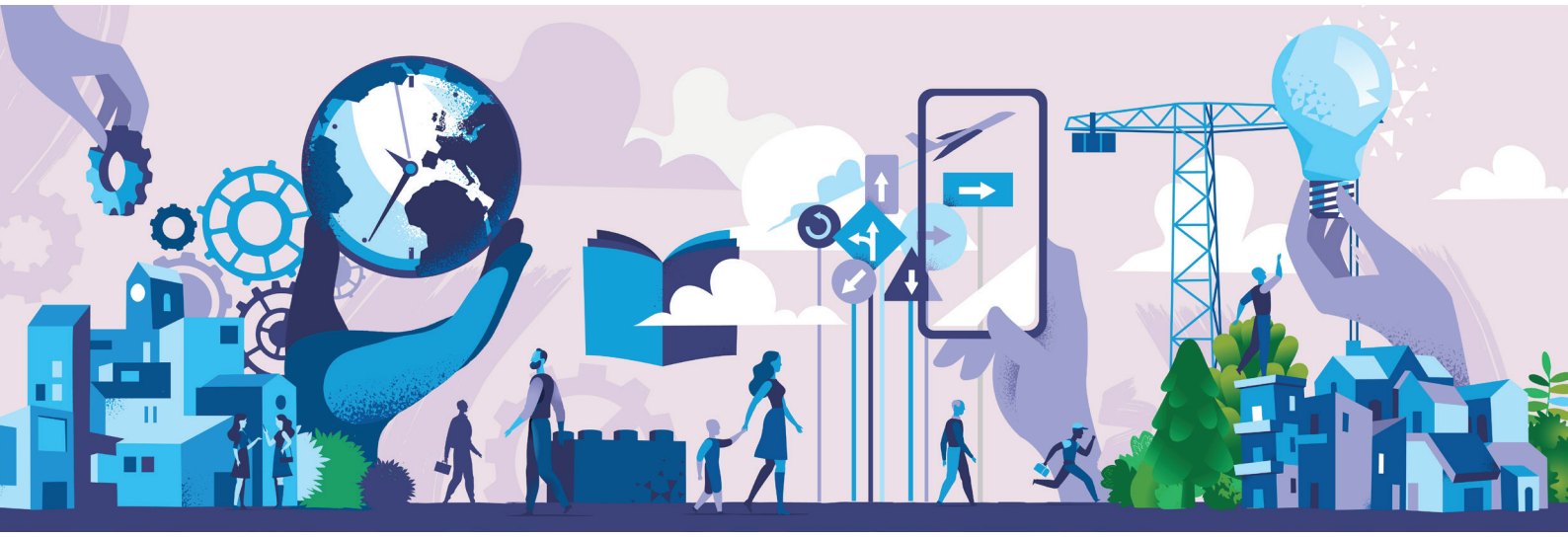


People, planet, profits: a sustainable way forward for all

While pushing the boundaries of technology, businesses increasingly face a critical workforce shortage and pressing environmental responsibilities. A project run by MIT has recently won NSF funding to address these challenges to build a more sustainable future for microchip manufacturing.

AN INTERVIEW WITH ANU AGARWAL, PRINCIPAL INVESTIGATOR ON THE PROJECT AND PRINCIPAL RESEARCH SCIENTIST AT THE MICROPHOTONICS CENTER AND MATERIALS RESEARCH LABORATORY OF THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY (MIT)

LH: *Could you tell me a bit about FUTUR-IC? How did the project start and what is its vision?*

AA: The project is on microchip manufacturing and sustainability, and we started it when we were funded by Dr. Linda Molnar, Program Director of Track I: Sustainable Materials for Global Challenges. This funding came through the National Science Foundation (NSF) Convergence Accelerator's Directorate for Technology, Innovation and Partnerships (TIP) in December 2022. As we started to think about sustainable microchip manufacturing, we realised that it is not a simple problem. It's not just one size fits all. Instead, it's multiple problems rolled in together. While we were brainstorming and wondering how the future of integrated circuit (IC) manufacturing should look, we realised there were three main branches to think about: technology, ecology, and workforce.

These three dimensions, as we call them, need to be simultaneously optimised. What that means is, we need to enhance microchip performance to meet the future needs for, say, AI, LiDAR, self-driving cars, and quantum applications, but we must think about doing it in an environmentally sustainable fashion. We must educate our workforce so they can meet the STEM performance challenges with sustainability top of mind.

FUTUR-IC will enable the coexistence and co-optimisation of people, which is workforce, planet, which is ecology, and profits, which is technology. But we cannot do it alone within academia. We must be rooted with industry associations, companies, universities, governments, and policymakers. This is the only way we can build a sustainable microchip supply chain for the future of our planet.

LH: *After running FUTUR-IC for a year with Phase 1 funding from the NSF, you have now received a Phase 2 Award, which is a clear signal of its value. Did the NSF outline in their decision what they find most important about the project?*

AA: The NSF Convergence Accelerator TIP Directorate has always been very clear that a positive impact to society is what they care about. That is important to us as well. Based on that, we conducted stakeholder interviews with at least

100-150 people in different walks of life, including people in companies, consumers of electronics, equipment vendors for the electronics industry, materials vendors, people who design the devices, and people in academia who are innovating in electronics. We interviewed people across the spectrum. We also talked to people in the government and in companies that make defence-related electronics.

Based on this use-inspired research, which we learned during NSF Phase 1, the feedback that we got showed the benefit of FUTUR-IC's work to people/workforce, planet/ecology, and profits/technology, and could have played a part in NSF's decision. For example, we didn't just pull three dimensions out of a hat. They were pointedly given to us by all our interviewees saying: "Yes, it's important to make technology with the highest performance, but at the same time, looking at what impact it has on the environment while ensuring that the future workforce is trained to design sustainably."

We learned from companies that they don't have a large enough pool of STEM-trained workforce to innovate new technology. Today we have about 2 million in this industry's workforce. By 2030, we need to climb to 3 million, and they must be trained not only in STEM but also in semiconductors and green literacy.

LH: *You have previously mentioned that the microchip industry has the potential to be a leader in environmental sustainability. Could you expand on this?*

AA: Several industries must consider sustainability during their process and design phases if we are to save our planet. One would think: why worry about the microchip manufacturing industry alone? But if you think harder about this microchip industry, it's made up of chemists, biologists, physicists, engineers, and computer scientists, with everybody working together in an interdisciplinary fashion driving exponential growth. If we can bring that interdisciplinary expertise to solving sustainability problems, think how wonderful that would be. We could transfer what we learn in the microchip industry to adjacent industries. Why not plant that seed of innovation in the microchip manufacturing industry, and perhaps other industries can also enjoy the fruits?

Another important factor is that the microchip industry is not limited to our cell phones and computers anymore. It is everywhere. It is ubiquitous in home appliances, like washers, dryers, toasters, cookers, and cars. Everything has electronics now. For the Internet of things (IoT) to work, so you can remotely access everything, we need microchips. So chips are expanding their scope and footprint in the world tremendously.

FUTUR-IC
Sustainable Microchip Manufacturing

There is another reason why this industry should take a leadership role. Everyone's trying to use ChatGPT with AI chips, which are known to cause overheating problems in datacentres. If we don't come up with sustainable solutions now, 10 years down the road we'll be in deep trouble in terms of energy consumption, heat generation, and electronic and chemical wastage. These are problems that we cannot tackle overnight; we must plan solutions early.

LH: *You have spoken about creating sustainable electronic-photonic packaging by being strategic about how we approach different tasks, such as computation and communication. Could you elaborate on this?*

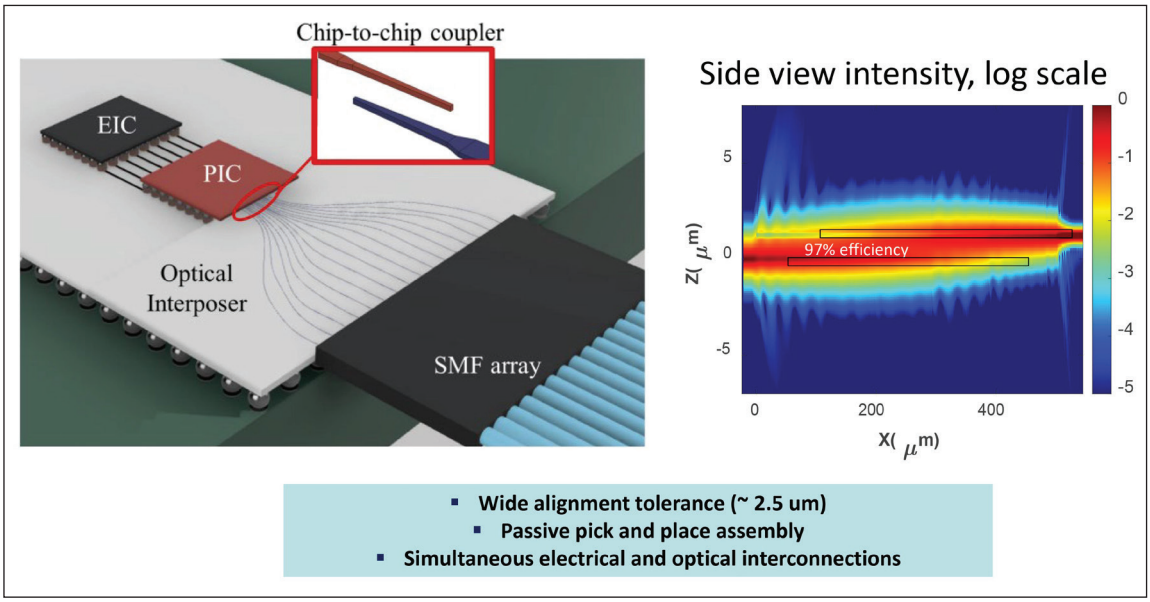
AA: It is about managing trade-offs between performance and cost. Following the prediction based on Moore's law the semiconductor industry has been driven towards smaller transistor dimensions. One reason for shrinking the size is that you can get more chips for a given area, leading to increased revenue, if you can hold down the cost of manufacturing. Also, the shrinking dimension has historically yielded enhanced performance, which is typically measured in the telecommunications industry as an increased bandwidth density with significantly lower power consumption.

To continue along the prediction offered by Moore's Law, some manufacturers are moving towards 3 nm and smaller process nodes. We may be able to push this dimensional shrink of transistors for another decade or so, but we're soon reaching the physical size limit. So, what's next?

Why don't we think about putting more chips in a package to increase bandwidth? Although more chips per package enables the use of shorter copper traces and lowers heat generation, a trade-off is that it also crowds the copper traces closer together, which can make it harder to dissipate the heat generated. So, we need new packaging designs, materials, and processes.

One way out is electronic-photonic integration through smart packaging. We can use electronics for data computation and photonics for data communication. Photonics, because it offers the possibility of high-speed and large-bandwidth data transmission through low-loss optical waveguides, leading to lower energy use, rather than through lossy long-reach copper traces.

➤ FUTUR-IC is advancing sustainable microchip manufacturing through three dimensions – technology/profits, ecology/planet, and workforce/people. The project has won Phase 2 funding from the National Science Foundation (NSF) Convergence Accelerator's Directorate for Technology, Innovation and Partnerships (TIP)



➤ FUTUR-IC is promoting electronic-photonic packaging, standardisation, and modularity, as practices that can make the microchip manufacturing industry more sustainable. Adapted with permission from Drew Weninger et al., "High density vertical optical interconnects for passive assembly," Opt. Express 31, 2816-2832 (2023) © Optica Publishing Group

A second benefit of electronic-photonic packaging is that for manufacturing photonic devices you can use mature and more environmentally sustainable process nodes, while maintaining high performance. The leading process nodes can be reserved only for manufacturing electronic devices, because that is a requirement for high-performance computation.
A third benefit is modularity. We can make a modular electronic-photonic package where we have photonic chips and electronic chips, each manufactured with different process nodes, maybe even in different foundries, placed next to each other on a common interposer or substrate. This idea is not new. In fact, in August 2023, at the Hot Chips conference, several large companies, including AMD, Intel, TSMC, and Samsung, decided that manufacturers need to start standardising the package to reduce costs.

We can combine these two ideas to get photonics for communication within a standardised electronic chiplet platform. Large companies have already begun using this combined idea. FUTUR-IC is pushing these ideas forward saying: "let's get on this standardisation bandwagon where we all use electronics for computation and photonics for communication," which makes microchip manufacturing more sustainable in terms of materials, processes, and energy.

Another benefit of using photonics for communication is that you can design for chips to be further apart from each other. Spatially separated chips in a package can be disassembled for repair or into separate waste streams at the end of life and recycled more readily for easier material recovery, improving sustainability. This might go against your instinct if you are trying to minimise the size of the overall package, but that is an engineering trade-off between size and modularity.

LH: *It sounds like this can help with several aspects of sustainability?*

AA: Yes, photonics helps with sustainability in multiple ways: energy consumption reduction, so less heating of datacentres; more chips per package instead of solely shrinking transistors, so bringing about "More than Moore"; and then this concept of disassembly for repair and into different waste streams. Since we're in this new era of packaging, why don't we start with training the workforce to design for sustainability and repair of microchip-containing systems, and to think about this ahead of time, rather than finding out at the end-of-life that repair is too costly or not feasible?

There are several electronic-photonic design automation (EPDA) vendors working on this. For example, Ansys offers software called Granta, which has a sustainable materials database. If I'm designing on Granta, it can tell me: "Hey, I notice that you're using this particular polymer. Have you considered this other polymer that has the same properties you're looking for, but is easier to recycle at end-of-life?" Upfront, it's giving engineers a sustainable alternative. There are other software packages that offer such "Design for Sustainability" options.

FUTUR-IC is introducing lifecycle assessment models for processes across three areas of microchip manufacturing: production, distribution, and use. We are calculating carbon footprints and handprints. Handprinting is the inclusion of the impact of positive environmental actions into lifecycle assessment models. Can we design and make cradle-to-cradle products?

FUTUR-IC has been promoting something called design for repair and upgrade. We all know of the three 'R's: reduce, reuse, recycle. But we're adding another 'R', for repair, and a 'U', which is upgrade. Let us try to repair our electronics. Let us try to upgrade our devices by just replacing one chip as opposed to throwing the entire device or appliance away.

LH: *You mentioned that several companies at Hot Chips 2023 highlighted the importance of standardisation. What needs to happen for the industry to collectively move in this direction?*

AA: Everybody must get on board. There must be a movement. Standardisation happens when everyone agrees that there should be standards. For example, if people decide that there should be a standard universal charger for cell phones, no matter the company, make, or model, it will happen.

Other standardisation approaches relate to what I was saying about packaging. Let's say I need a way to put together an AI accelerator chip, a memory chip, and another chip that does my specialised custom function. How can I put it all together without having to redesign a package from scratch for each product? And it's not only good for the environment, but also good for the companies, as it becomes easier and less expensive for them to source components with a mix-and-match approach.

We've interviewed about 140 companies, and what they said to us is that technology drives the business, but ecology maintains business continuity, because, for example, if the planet runs out of lithium there can be no business. And finally, workforce grows the business. Without a well-educated workforce, not just in STEM (science, technology, engineering, and mathematics), but also in sustainability, we cannot grow in the right direction. So that's why we need to co-optimise the technology, ecology, and workforce dimensions. There are lots of companies and groups doing one or another. But FUTUR-IC works on them simultaneously.

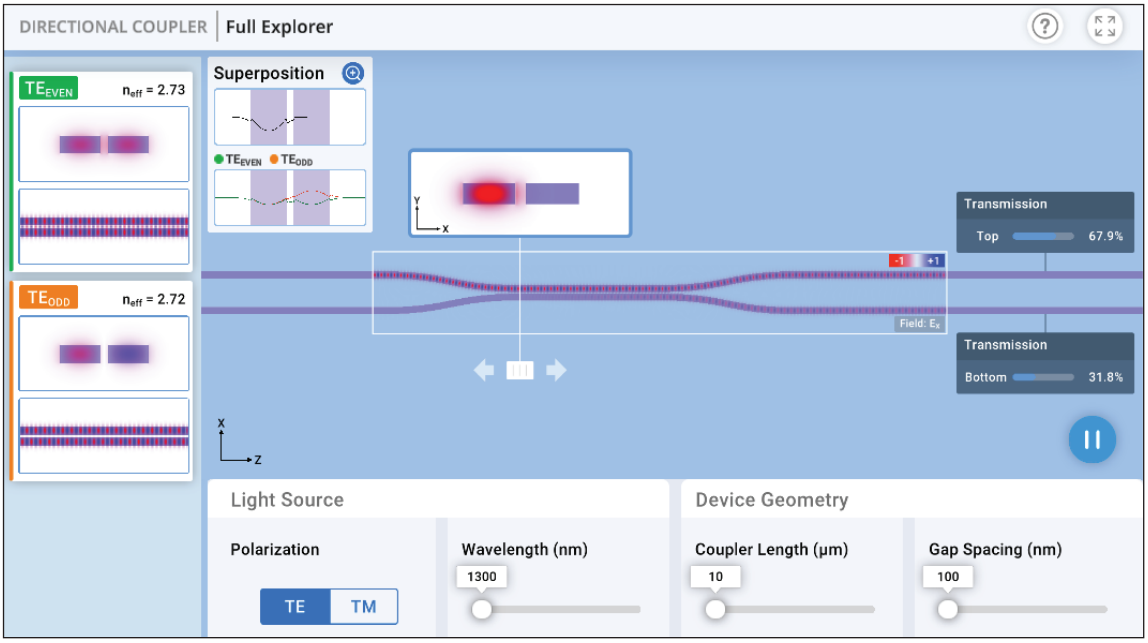
LH: *You mentioned that tech companies are facing a shortage of people with the appropriate technical skills. How is MIT working to address this issue?*

AA: There is a huge workforce shortage, not just in the US, but globally. Anecdotally, people have been saying that students used to come to their professors as they were getting close to graduation, asking for recommendation letters for jobs. Now, students are coming in and saying: "I have five job offers and I just have to pick one – no thank you, I don't need a recommendation letter!"

At MIT, our team is building a roadmap for microchip technology as well as for the semiconductor workforce. Through a different programme, members on our team are creating a Workforce Readiness Level (WRL) categorisation, just like we have the Manufacturing Readiness Level (MRL). Our philosophy at MIT has been agile continuous education using a three-legged stool approach. The first leg is lectures, or some kind of pedagogical teaching, with which we are all very familiar. The second leg is Virtual Reality (VR) simulations to build intuition. And finally, the third leg is hands-on training in labs, for which the Commonwealth of Massachusetts has invested about $18 million into five LEAPs (Lab for Education and Application Prototypes) across the state (cam.masstech.org/cam-programs/lab-education-application-prototype-leap).

In terms of traditional education, we have teaching packages, short courses, and a summer academy. We also have several online electronics, photonics, and sustainability courses available.

We have a virtual lab photonic device simulation library which you can find on the website of our partner AIM Photonics (www.aimphotonics.com/simulation-library), with simulations of photonic device components, such as a Y-branch splitter, Mach-Zehnder interferometer, ring resonator and others. One simulation, for example, shows you how light bends at corners. You can see that there's loss



➤ FUTUR-IC is working on many educational initiatives for workforce training and development, including a library of simulations that build intuition around how light behaves within various photonic components.

at an edge with a sharp bend, and if you change the radius of curvature to be less sharp, there's less loss. This is what I mean by building intuition.

The simulation for a directional coupler shows you what happens when you bring two waveguides close to each other, or if you change the length of the coupling region. If you look at the output, you can see whether the modes couple from one waveguide to the other, depending on the coupler length and the wavelength. We've created these browser simulations based on solutions to Maxwell's equations.

A learner may ask: what happens if I change the radius of my device? What happens if I change the gap between these waveguides? What happens if I move from one wavelength to another? The VR simulations provide them with an immediate intuitive understanding of the behaviour of light in on-chip devices.

For practical training, we have hands-on bootcamps that we offer at MIT and with Professor Samuel Serna at Bridgewater State University, which is a four-year college in Massachusetts. Through an NSF-ATE programme led by Suny-Poly in New York and MassBay Community College in Massachusetts, we offer bootcamps to students in community colleges and help to place them in company internships following the training. With bootcamps, apprenticeships and internships, we bring people into labs, and we teach them how to perform hands-on testing. We are hoping that this successful three-legged stool education model can be replicated across the country.

We have an education team at MIT within the Initiative for Knowledge and Innovation in Manufacturing (IKIM), and you can see all our educational offerings at ikim.mit.edu. Our education director is Dr. Sajan Saini, and Professor Lionel Kimerling leads IKIM. Due to this IKIM team effort in education and workforce development over the last five years, we stand where we are today.

LH: *The Phase 1 Award was for a year, but the Phase 2 Award is for three years. Will this enable the FUTUR-IC team to do anything qualitatively different, or is the main outcome the further continuation of the research?*

AA: The longevity helps in goal setting. We know what we want to accomplish in the long term – a sustainable microchip industry. In the short term, we're working with low-volume foundries, and eventually we'll go to higher-volume foundries, packaging houses, and design vendors. Now the fact that we have two and a half to three years to work it out means we can start to build our relationships with the various stakeholders, gather the data that is required, and then build technology, ecology, and workforce products, and co-optimise them simultaneously. It gives us some more flexibility because it's over a longer period and we have time to course correct whenever necessary.

The result should be the same, which is sustainable microchip manufacturing across the supply chain. But how we apportion the tasks that we're doing, our deliverables, is different. They are broken down according to what should be done in year one in order to build for year two and year three.

LH: *The MIT Microphotonics Center is also co-leading the Integrated Photonics Systems Roadmap-International (IPSR-I), together with PhotonDelta from the Netherlands. How can companies and research institutes get involved?*

AA: The IPSR-I started out as a communications technology roadmapping initiative, and it's now an international project. We have partnerships from Japan and Europe, and we have partnership requests coming in from South America as well.

We have two meetings a year. One is in June at MIT, and one is in autumn in Eindhoven. There's a lot of interest in the technology roadmap. Anyone interested in joining is welcome to reach out to us (at anu@mit.edu) or go to our website, ikim.mit.edu, and ask what they can do to move the sustainability needle in the right direction by simultaneously benefiting people, planet and profits.

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Enabling efficient light **emission and detection**

Efficient monolithic integration of in-plane III-V lasers and photodetectors on SOI is a promising approach for addressing the communications bottleneck.

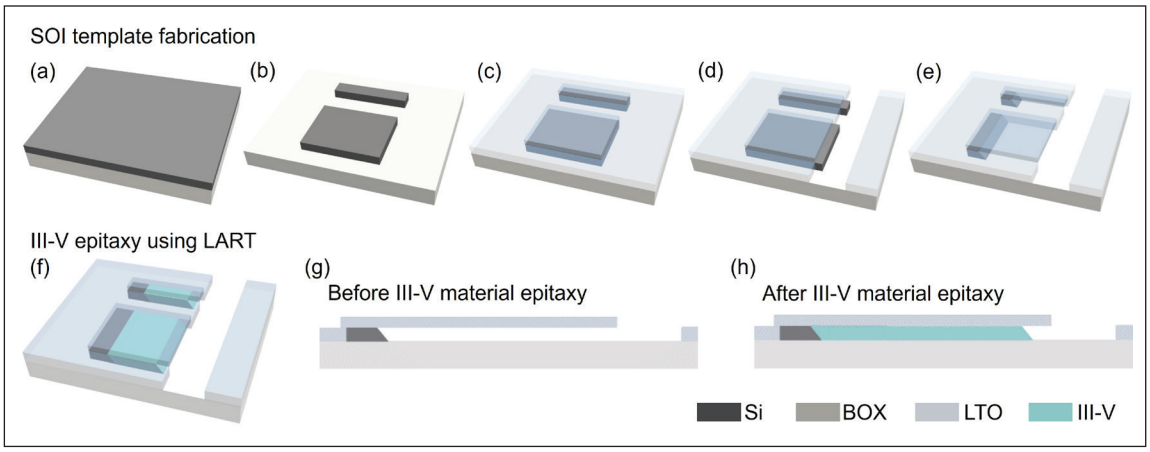
BY YING XUE AND KEI MAY LAU, HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

IN RECENT YEARS, internet traffic has soared, growing at around 27 percent per year. About three quarters of this traffic occurs within datacentres, where high speed, large bandwidth, low cost, and low power consumption are vital. This surge in demand is pushing current electrical interconnects to their limits, prompting the need for optical interconnects, which are fast, efficient, scalable, and eco-friendly.

Integrated silicon photonics is leading the way, since it can leverage mature CMOS technologies, and is well equipped with various photonic functions, mainly established by highly integrated passive circuits. Yet, since silicon and germanium have an indirect bandgap, realising on-chip light sources – the heart of integrated photonics – requires the integration of high-quality III-V gain materials onto the existing silicon photonic platforms.

Much effort has been devoted to realising the monolithic integration of III-V light sources onto silicon. However, efficient strategies that yield both a high-performance device and low-loss interfacing with existing passive photonic integration platforms have remained elusive.

To solve this dilemma, our team at Hong Kong University of Science and Technology (HKUST) recently developed a novel integration method named lateral aspect ratio trapping (LART) [1-3]. We tackle the integration challenge from two perspectives: device performance and interfacing efficiency. This allows for the close integration of high-quality III-V with silicon in the same plane. The high-quality III-V – essential for high-performance III-V active devices including lasers, photodetectors and modulators – is enabled by the unique defect necking effect using the LART method.



➤ Figure 1. (a)-(e) SOI template fabrication for lateral selective epitaxy including silicon patterning, oxide encapsulation and opening definition. (f) 3D architecture of the III-V on SOI platform after lateral epitaxy. (g)-(h) Cross section of the lateral trench before and after III-V epitaxy.

Our in-plane configuration with silicon results in low-loss interfacing between building blocks constructed from different materials, especially between III-V light sources and silicon waveguides, the key bridge for PICs. Leveraging the LART technique, we have developed various critical photonic devices including micro-lasers, distributed feedback lasers, distributed Bragg reflector lasers, photodetectors, and modulators. Furthermore, we have demonstrated efficient coupling between III-V and silicon using a butt-coupling strategy.

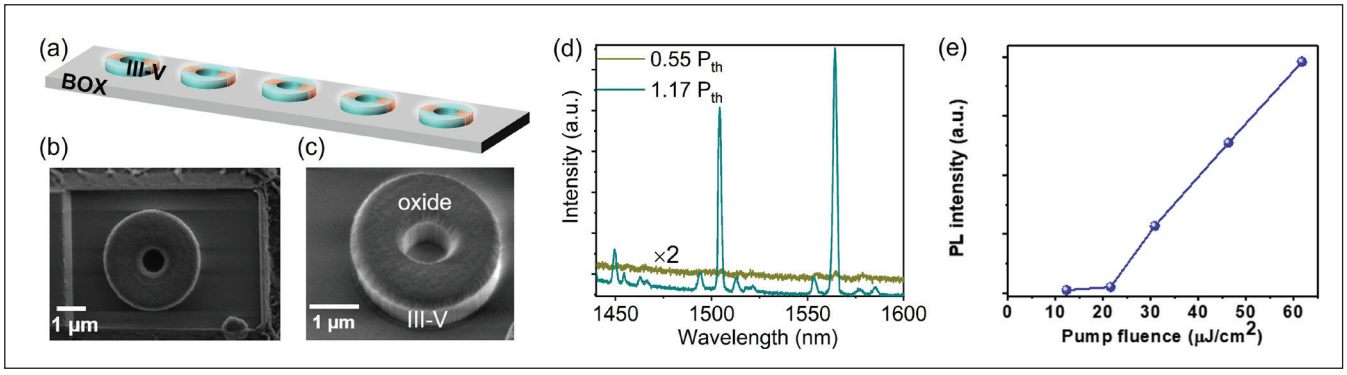
The LART fabrication technique

All selective epitaxy processes require a growth template with pre-patterned trenches or pockets to guide the epitaxy. For our LART method, we designed a growth template with pre-patterned lateral trenches of various lengths to provide confinement and guidance for the lateral III-V epitaxy. Figure 1(a)-(e) schematically depicts the fabrication process of the growth template [3] for lateral selective epitaxy. Starting from 8-inch silicon-on-insulator (SOI) wafers, we patterned the silicon device layer with a thickness of 500 nm or 800 nm into silicon segments with identical widths and different lengths, spanning hundreds of nanometres to hundreds of micrometres. The process involved using i-line lithography and a subsequent silicon dry etch. Since the sidewall of the growth pockets guides the growth of III-V materials, we carefully optimised it to be vertical and smooth.

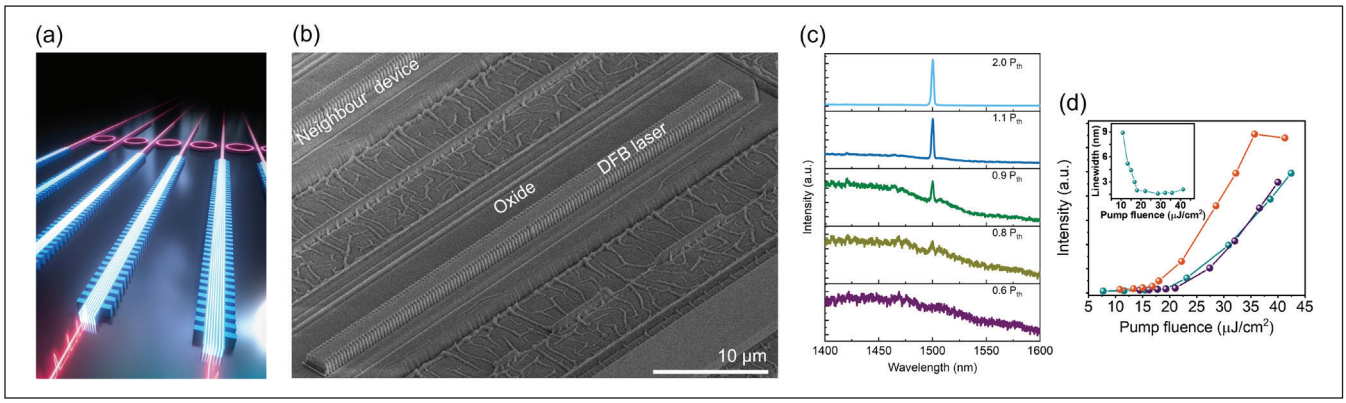
Next, to achieve dense oxide coverage, we encapsulated the silicon segments in a thin layer of low-temperature oxide (LTO) and annealed them in a nitrogen atmosphere. Using dry etching, we defined the openings and undercut the silicon deeply into the trenches, to enable the diffusion of precursors for the epitaxy of III-V materials. The fabrication of the growth template on SOI is compatible with that of passive PICs and can be finished in a CMOS line, therefore allowing for high integration density and low cost.

The III-V lateral epitaxy step was performed using a metal-organic chemical vapour deposition (MOCVD) system (Figure 1(f)-(h)). With optimised growth conditions, we have produced high-quality and large-volume III-V crystals laterally grown on SOI. Due to the effective defect engineering of LART, the defects generated by the large mismatch between III-V and silicon are accommodated at the interface between the materials. Most of the III-V segments for device fabrication are therefore free of most defects that would severely degrade device performance [2].

The resulting monolithic III-V on SOI platform is a promising way of achieving various active devices including lasers, photodetectors, and modulators, as well as their efficient interfacing with passive photonic circuits [1]. Furthermore, the platform can act as a regrowth template to provide a solution for



➤ Figure 2. (a) 3D schematic of the micro-laser array on SOI. (b)-(c) SEM images of the fabricated micro-laser. (d) Lasing spectra of the micro-laser below and above threshold. (e) Extracted L-L curve of one micro-laser on SOI.



➤ Figure 3. (a) 3D schematic of the DFB laser array on SOI. (b) SEM images of the fabricated micro-laser. (c) Lasing spectra of the DFB laser at progressively increased power. (d) Extracted L-L curve of DFB lasers on SOI. Inset: Linewidth evolution showing the lasing behaviour.

the integration of indium phosphide (InP) photonic circuits and passive silicon photonics on SOI.

Building lasers and photodetectors

Using our monolithic III-V on SOI platform, we first demonstrated micro-laser arrays in the telecom band with small footprints and low power consumption [4]. The micro-lasers generated feature a III-V-on-insulator structure for superior optical confinement as illustrated in Figure 2(a).

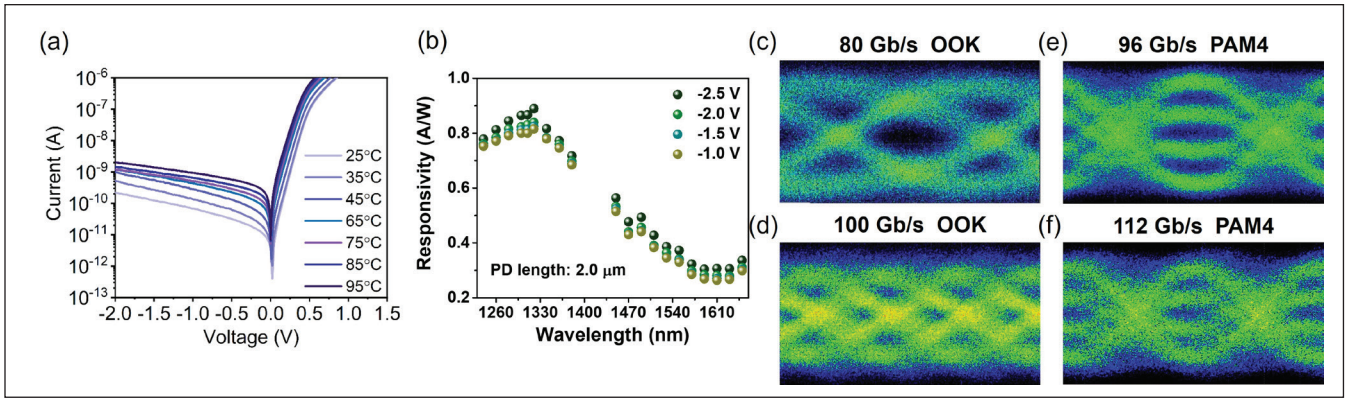
The top-view and tilted-view scanning electron microscopy (SEM) images in Figure 2(b) and (c) show the good circularity and smooth sidewall of the defined cavity. The micro-lasers demonstrated multimode lasing w ith thresholds of around 20 μJ/cm². Figure 2(d) plots the lasing spectra below and above the lasing threshold showing the lasing wavelength in the 1.5 μm band. The extracted light-light (L-L) curve is displayed in Figure 2(e).

To realise single-mode lasing and demonstrate the viability of the monolithic III-V on SOI platform with a larger III-V volume, we further designed and fabricated 1.5 μm in-plane III-V distributed feedback (DFB) lasers on commercial (001) SOI wafer using LART, as illustrated in Figure 3(a).

Although DFB lasers with vertically stacking quantum wells (QWs) have been widely reported, DFB lasers with laterally stacking QWs are novel and remain to be explored. We defined unique gratings with minimised non-radiative recombination and undemanding fabrication processes for the DFB lasers on SOI. We demonstrated lasers with a short cavity length, low lasing thresholds, and excellent mechanical stability exhibit stable single-mode lasing in the 1.5 μm telecom band [5]. Furthermore, the in-plane structure allows for efficient coupling with the passive components.

The SEM image in Figure 3(b) depicts the well-fabricated DFB lasers on SOI. Figure 3(c) shows the room-temperature emission spectrum of the DFB lasers on SOI at various pumping powers.

We measured a side-mode-suppression-ratio (SMSR) exceeding 35 dB. Figure 3(d) presents representative L-L curves in linear scale measured from the DFB lasers on SOI with an extracted threshold of around 17 μJ/cm². The measured



➤ Figure 4. (a) Temperature-dependent dark current of the PD from 25 degrees Celsius to 95 degrees Celsius. (b) Responsivity at different wavelengths from 1240 nm to 1650 nm. (c)-(d) 80G and 100G OOK eye diagram under -2 V bias. (e)-(f) 96G and 112G PAM-4 eye diagram measured at -2 V.

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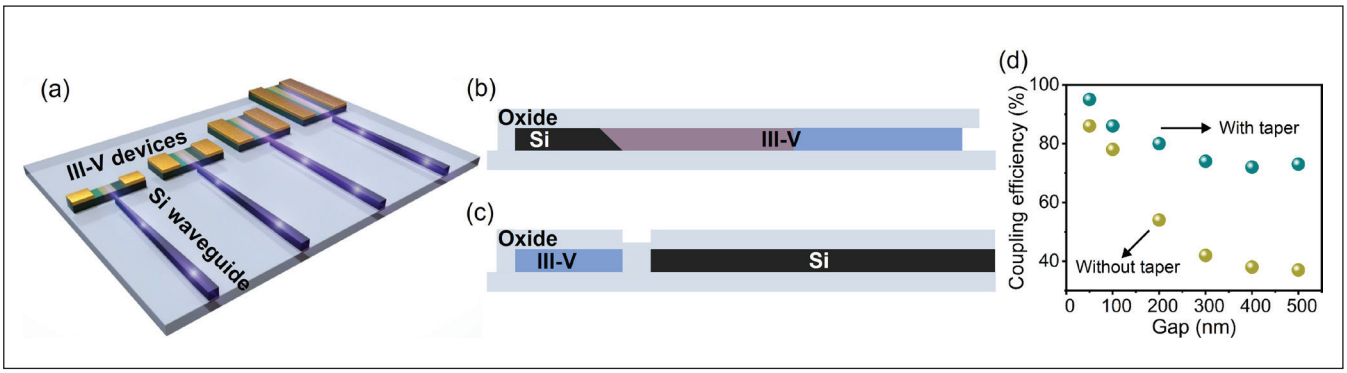

➤ Figure 5. (a) 3D schematic of the silicon-waveguide-coupled III-V PD on SOI with various dimensions. (b) Cross-sectional view schematic of III-V laterally grown on SOI. (c) Cross-sectional view schematic illustrating the placement of III-V absorption layer and silicon waveguide perpendicular to the growth direction. (d) Coupling efficiency between the silicon waveguide and III-V photodetector for the designed coupling scheme with and without a silicon inverse taper.

linewidth as a function of pump fluence is plotted in the inset of Figure 3(d).

Our demonstration of lasers represents a highly scalable monolithic solution to integrated laser sources on silicon, thus providing an elegant approach for fully integrated silicon photonics with both conventional electronics and photonics. Besides lasers, high-performance photodetectors (PDs) are crucial optical building blocks in silicon PICs, and should have the following characteristics: high responsivity, low dark current, large bandwidth, operation over a wide wavelength band, efficient light coupling with silicon waveguides, and CMOS compatibility. To fulfil these criteria, we used LART to develop high-performance III-V PDs on commercial (001) SOI.

The resulting PDs manifest a low dark current of 60 pA as shown in Figure 4(a), a large photocurrent exceeding 1 mA, responsivities of 0.3 A/W at 1550 nm and 0.8 A/W at 1310 nm (see Figure 4(b)), and a large detection wavelength range over the entire telecom band [3]. High-speed measurements reveal a 3 dB bandwidth over 52 GHz and a data communication rate of 112G with four-level pulse amplitude modulation and 100G with on-off keying (Figure 4(c)-(f)). The photocurrents can be adjusted for various applications by altering the length of the PDs.

Efficient waveguide coupling

After growing III-V lasers and PDs on silicon, and focusing on improving the performance of these stand-alone devices, we explored light interfacing strategies between the III-V devices and silicon waveguides. We did this by demonstrating III-V PDs grown on (001) SOI wafers efficiently butt-coupled with silicon waveguides [6], as illustrated by the schematics in Figure 5(a)-(c).

The coupling efficiency between III-V and silicon can be enhanced by designing inverse tapers as plotted in Figure 5(d). We achieve efficient light interfacing between III-V PDs and silicon waveguides through the in-plane placement of the epitaxial III-V material with the silicon-device layer and the design of advanced couplers.
The waveguide-coupled III-V PDs show a superior device performance compared with the stand-alone III-V PDs on SOI. These waveguide-coupled III-V PDs have potential to advance the state of the art of future PICs that can be manufactured with seamless monolithic integration of III-V lasers and detectors on the common silicon photonics platform.

To build further on this research, we are currently working on electrically pumped lasers and focusing on how they can be efficiently coupled and integrated with passive components for various applications in communications.

In future work, we will also investigate the characteristics of the novel lateral laser structures and advanced coupling techniques. We believe that the LART technique and the developments it paves the way for will play an important role in fulfilling the potential of integrated photonics for communications and other emerging applications.

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