PICMAGAZINE

CONNECTING THE PHOTONIC INTEGRATED CIRCUITS COMMUNITY

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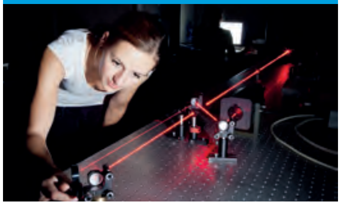
Membranes light up silicon photonics

Indispensable indium

PICs for Sensing Applications

PhotonDelta is investing in PHIX

Cambridge Nu Quantum raises £2.1m



Tiny PICs have huge impact on optical wafer testing

EXFO

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Contact: Jackie cannon
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Viewpoint

By Mark Andrews, Technical Editor

Continuing advances in photonic technology spur market growth

AS THIS EDITION of PIC Magazine nears publication, the AngelTech Virtual Live II event is only a few days away. Photonic integration continues to evolve, creating greater opportunities in datacom and emerging new markets built around versatile, light-speed technologies.

Photonic integrated circuits are strengthening as an industry, expanding their reach while sales of broad market photonic components recovered strongly in second quarter after a 1Q contraction during initial COVID-19 outbreaks. Analysts report that optical markets grew by mid-year, but the latest viral resurgence points to a possible fall-off during 2H 2020. In a year like none other, PIC developers and manufacturers continue to show resilience and innovation, fueling expectations for growth once vaccines and treatments begin distribution in late 2020 or early 2021.

Throughout the pandemic, the photonics community has again demonstrated its ability to meet customer needs even as many amongst us continue to face steep personal challenges and loss. In this PIC Magazine we explore the ever-expanding photonics ecosystem and ways that different supply chain members contribute to applications as familiar as datacom as well as emerging healthcare applications, automotive sensory systems, biotech, Industry 4.0, and many others.

R&D Manager for EPIC, Ana Gonzalez, examines ways that PICs play essential roles as new biosensors. In her pre-AngelTech Virtual Live video interview she discusses the expansion of pilot line programmes across the EU. Experts from Synopsys delve into PIC-based PAM-4 designs, demonstrating once again that the move to integrated photonics is indeed creating new opportunities. The test and measurement experts at EXFO, Hewlett Packard Enterprise and MPI explore ways that the three companies brought their own unique perspectives and expertise to a new integrated PIC testing solution.

VPIphotonics and Luceda Photonics detail the power of their ongoing partnership to offer highly advanced PIC design tools and simulation modeling that is faster, more efficient, repeatable and reliable, thus mitigating bottlenecks that can slow time to market or increase costs.

Enjoy this edition of PIC Magazine and look for a recap of the AngelTech Virtual Live II Summit in future editions along with an in-depth look at PIC pilot lines across Europe.

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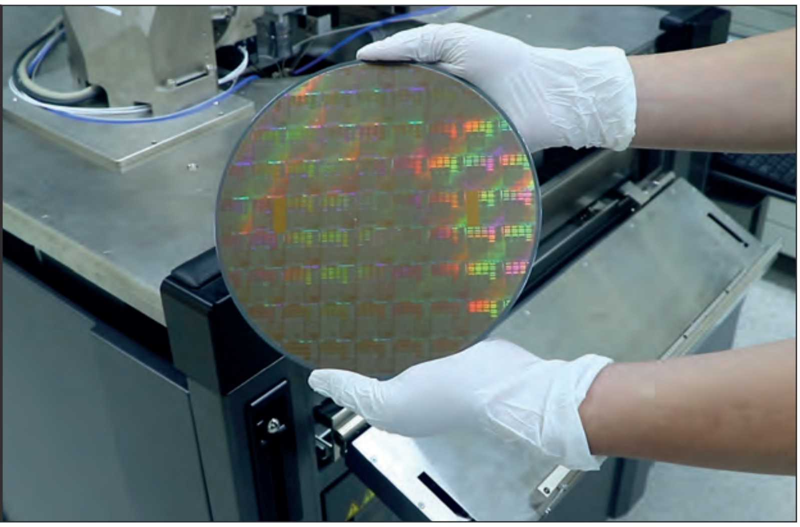
ISSUE III 2020

CONTENTS

12 COVER STORY

Tiny PICs have huge impact on optical wafer testing

Given the out-sized role silicon wafers play in creating photonic integrated circuits (PICs), non-automated/non-integrated testing setups impede optimization



18 Photonic Integrated Circuits for sensing applications

Companies developing products for optical ommunications, 3D sensing, biosensing, or spectroscopy are increasingly incorporating photonic integrated circuits (PICs) because they offer economic and functional advantages.

24 PAM-4 transmitter design using segmented-electrode modulators

Photonic integrated circuits (PICs) are rapidly bringing their size, performance and energy saving advantages to data centre operations.

32 Membranes light up silicon photonics

Epitaxial growth on wafer-bonded InP templates enables the integration of high-performance lasers and Mach-Zehnder modulators with silicon waveguides.

38 Indispensable indium

From flat panel displays to semiconductor wafers, the use of indium in electronics continues to grow.

42 Seamless integration of photonic circuit simulation and design

VPIphotonics and Luceda Photonics have combined their considerable design software expertise to offer the integrated photonics industry a powerful suite of tools created around the idea of speeding the design process while enabling the simulation of a new circuit's performance in real-world conditions.

news

UK start-up AegiQ secures £1.4m to develop secure quantum communications

AEGIQ, the UK quantum photonics start-up, has announced that it has secured a total of £1.4 million in funding from Innovate UK to develop secure quantum communications for fibre-optic and satellite based applications.

AegiQ will join a global pilot project to provide scalable, high-performing semiconductor technology for next generation telecoms.

AegiQ has been awarded Innovate UK funding as part of a consortium of companies. It will build communication infrastructure resistant to hacking by new quantum methods.

The start-up is also championing the use and development of quantum photonic technologies. Led by CEO and co-founder Dr. Max Sich, AegiQ is a spin-out of the University of Sheffield and part of the UK government's £70m funding initiative to secure the UK's position as a world-leader in quantum technology.

Quantum cryptography is viewed as the key to future-proofing security by the telecoms industry, by addressing advances in quantum computing which make traditional messaging encryption methods vulnerable to attacks. The UK National Quantum Technologies Programme expects "Quantum technologies to lead to major advances in [...] the finance, defence, aerospace, energy, infrastructure and telecommunications sectors."

AegiQ is the leading company developing III-V semiconductor-based quantum photonics (manufacturing chips using elements such as Gallium, Indium and Arsenic rather than traditional Silicon), which is accepted as a far superior method in terms of reliability and security, and leverages existing industrial processing techniques.

The company, which is part of this year's Creative Destruction Lab's Quantum Stream cohort, has also been named one of the Quantum Computing Hardware Companies Building the Future.

"Existing software-based encryption of telecom networks is vulnerable to quantum attack," commented Scott Dufferwiel, AegiQ's CTO. "The risks are losing control of our communications and being faced with massively compromised security from quantum hackers. With the rise of quantum computing, standard encryption methods are no longer fit for purpose. A wide range of industries will require these quantum solutions in the near term."

Dr. Max Sich added: "Thousands of AegiQ systems will be required in each data centre around the world, as they transition to using quantum technologies for communication and cloud computing.

Deploying our scalable technology with mass production capabilities into initiatives like this project will position the UK as a world-leader in manufacturing quantum communications."

AegiQ is currently raising its seed round of investment. The Innovate UK funding will also enable AegiQ to invest in the further R&D and production of its technology, which underpin technology used in areas such as quantum communications, quantum sensing and information processing.

Korean team makes 2D light-emitting FETs

2D TRANSITION metal dichalcogenides (TMDs) are promising materials for next-generation optoelectronic devices. They can emit strong light due to the large binding energies of excitons (quasiparticles composed of electron-hole pair) as well as an atomically thin nature.

In existing 2D light emitting devices, however, the simultaneous injection of electrons and holes into 2D materials has been challenging, which results in low light emission efficiency.

To overcome these problems, Gwan-Hyoung Lee's group in Seoul National University and Chul-Ho Lee's group in Korea University demonstrated all-2D light-emitting field-effect transistors (LEFETs) by staking 2D materials. They chose graphene and monolayer WSe2 as contact electrode and an ambipolar channel, respectively.

Typically, a junction between metal and semiconductor has a large energy barrier. It is the same at a junction of graphene and WSe2. However, Lee group used the barrier-tuneable graphene electrode as a key for the selective injection of electrons and holes. Since the work function of graphene can be tuned by an external electric field, the contact barrier height can be modulated in the graphene-contacted WSe2 transistor, enabling selective injection of electrons and holes at each graphene contact.

By controlling the densities of injected electrons and holes, the high efficiency of electroluminescence as high as 6 percent was achieved at room temperature.

In addition, the researchers showed that, by modulating the contacts and channel with separate three gates, the polarity and light emission of LEFETs can be controlled, showing great promises of the all-2D LEFETs in multi-digit logic devices and highly integrated optoelectronic circuitry.

'Multioperation mode light-emitting field-effect transistors based on van der Waals heterostructure' by Junyoung Koon et al; Advanced Materials, September 2020.

Sheffield University spin-out to build III-V semiconductor platform for quantum cryptography

AEGIQ, a UK quantum photonics start-up, has secured a total of £1.4 million in funding from Innovate UK to develop secure quantum communications for fibre-optic and satellite based applications. AegiQ will join a global pilot project to provide scalable, high-performing semiconductor technology for next generation telecoms.

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"Deploying our scalable technology with mass production capabilities into initiatives like this project will position the UK as a world-leader in manufacturing quantum communications."

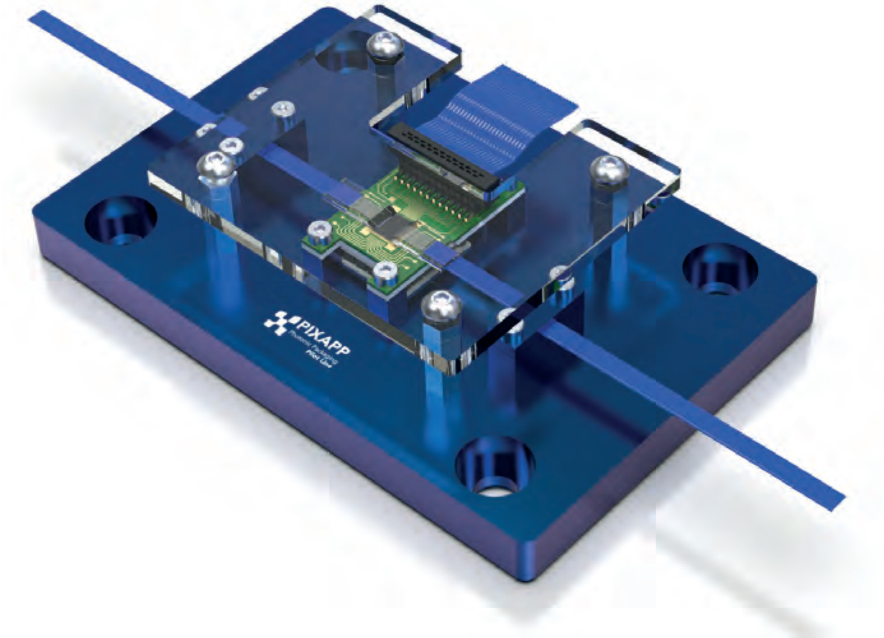
KT chooses Infinera for backbone network

Infinera has announced that KT Corporation (KT), South Korea's largest telecommunications company and formerly Korea Telecom, deployed the Infinera 7300 Series Multi-haul Transport Platform in its national backbone network to support a nationwide rollout of 5G services. KT selected the 7300 platform to provide a scalable core network solution optimised for the performance requirements of bandwidth-intensive end-user services such as 5G.

KT offers high-bandwidth services and 5G technology. KT deployed the first phase of its 5G network in late 2018, launching new services in the greater Seoul metropolitan area. KT plans to expand its 5G network nationwide this year to include 24 major cities, as well as key transport routes such as expressways, subways, high-speed railways, large universities, and neighbourhood shopping areas. Infinera's solution for KT includes support for secure and reliable 200G transmission across KT's nationwide core infrastructure. The 7300 coherent packet optical transport system offers a compelling pay-as-you-grow approach to network scaling. This model benefits KT by lowering initial costs, reducing equipment sparing costs, and providing the foundation for cost-effective scalability.

"Infinera's advanced optical solutions enable KT to efficiently use its fibre and optimise the transmission of optical channels, lowering the total cost of network ownership, and helps KT maintain its global leadership in 5G," said Nick Walden, SVP, worldwide sales at Infinera. "With Infinera's innovative solutions, operators like KT pave the way for an agile and scalable infrastructure to support significant increases in bandwidth. We are greatly honoured to be appointed to deliver Infinera's cutting-edge and robust solution to support KT's national backbone network to support 5G," said Choi Yong Seok, CEO & Chairman of Daesung Infotech.

PIXAPP launches new prototype packaging platforms



PIXAPP, the world's first open-access Photonic Integrated Circuit (PIC) Assembly and Packaging Pilot line, today announced the introduction of two new prototype packaging platforms to enable the early-stage testing and evaluation of integrated photonic devices.

The PIXAPP Grating Coupler Based Generic Packages (PIXAPP-GCP-10 and PIXAPP-GCP-100) are now available to users that need fast and cost-effective PIC packages with 10s to 100s of electrical connections. "Off-the-shelf" designs are available in volumes from 5 to 1000 units for rapid prototyping using the PIXAPP-GCP-10 design. For PICs with larger electrical and optical connections, the more flexible PIXAPP-GCP-100 design is available.

These prototype packages add to PIXAPP's established advanced photonic packaging services, helping users speed-up the development of their new photonic-based products. The prototype packages offered are based on PIXAPP's standardised packaging building blocks, including standardised optical and electrical interconnects, thermal and mechanical components.

Since 2017, PIXAPP has led and coordinated efforts with Europe's leading photonics research institutes and companies to standardise advanced packaging processes and coordinate the manufacturing supply chain, working with design houses, device foundries, companies providing packaging components and services, and manufacturers of automated packaging equipment. "We are excited about the launch of these new standard prototype packages that support companies in the early stage of product development and evaluation.

"We believe these packages will benefit users across many application areas, including optical communications, medical devices and other emerging industrial markets" said Peter O'Brien, director of the PIXAPP Pilot Line.

POET signs deal with european optical systems company

POET Technologies, a developer of Photonic Integrated Circuits (PICs) for data centres and telecoms, has signed a development and supply agreement with a European optical systems company for a 400G data centre application.

The contract includes a nominal amount of Non-Recurring Engineering (NRE) funding to design optical engines based on the POET Optical Interposer for a 400G application, along with a Purchase Order for initial production units.

The design and development stage is expected to extend through March 2021, with production planned for June 2021, consistent with the company's recently updated roadmap presented at its shareholder meeting held on August 26, 2020. The customer is a provider of optical networking systems for data centre and enterprise applications. However, due to confidentiality, the name of the customer and the specifics of the end application cannot be disclosed.

"The agreement is further evidence of the expanding customer interest in POET's optical engines and the pace at which our product development is progressing," said Vivek Rajgarhia, POET's president and general manager.

"Over the next several months, we expect demand from additional customers will increase further as we continue to demonstrate the full capabilities of the Optical Interposer. Our platform utilises a novel approach to integrating key electronic, photonic and optical components into a full transmit and receive optical engine, broadly applicable to data centre and telecommunications products."

PhotonDelta is investing in PHIX

WITH THE ADDITION of PhotonDelta as a shareholder, PHIX further secures its position as a leading packaging and assembly foundry within the European integrated photonics ecosystem.

PhotonDelta also provides PHIX with long term financing for equipment purchases necessary to ramp up production of optoelectronic modules. This is made possible by PhotonDelta's funding partners: Brainport Development and The Province of Overijssel.

PhotonDelta is a growth accelerator for the Dutch integrated photonics industry. Their team of experts actively supports its partners by providing them with access to funding, knowledge, and a wide network of companies and knowledge institutions. Their objective is to promote the development and commercialization of integrated photonics, in order to reduce time-to-market and accelerate the adoption of the technology by the industries.

Over the years, they have developed a strong ecosystem with major players in the supply-chain. A number of start-ups have transformedinto mature companies, each with their own distinctive technological propositions, setting the foundation of a strong Dutch supply chain that is able to design, manufacture, package and test high quality integrated photonic solutions based on InP as well as TriPleX (SiN) technology.

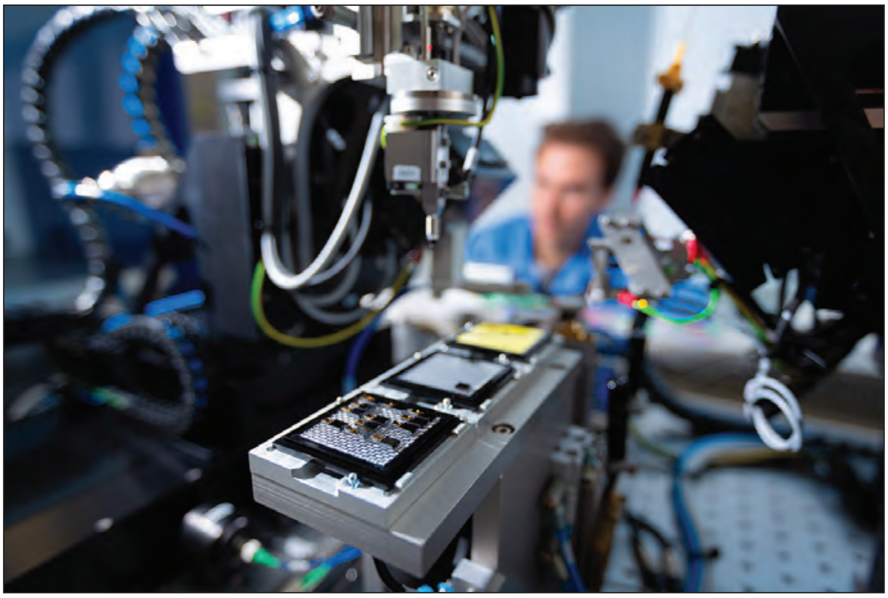
The partners are encouraged to collaborate and share knowledge and experience. An example of this is the Flagship project, in which many PhotonDelta partners including PHIX are participating.

Furthermore, PhotonDelta acts as a worldwide ambassador for its partners. This opens new market opportunities for PHIX as a specialist in packaging and assembly of photonic integrated circuits (PICs) in scalable volumes.

As disruptive PIC-enabled technologies are becoming more and more commercialized, PHIX is accelerating its growth to facilitate its customers' production scale-up. CEO Albert Hasper comments,

"This loan from PhotonDelta enables us to expand the equipment infrastructure towards volume production to facilitate our growing customer base."Ewit Roos, CEO of PhotonDelta says "Over the recent years, PHIX has demonstrated their ability of driving a business towards success.

"Their activity is essential for the mass adoption of integrated photonics in general and provides the Dutch ecosystem with an important supplier for the packaging and assembly of Photonic Integrated Chips. That is why we are delighted to contribute to PHIX's next growth phase."



OFC San Francisco rescheduled for June 2021

OFC 2021, a key industry event in telecom and data centre optics, will now take place 6 – 10, June 2021, at the Moscone Center, San Francisco, California, USA. Considered the foremost gathering of leaders in academia, engineering and industry, OFC represents the entire optical communications ecosystem from research to the marketplace, from components to systems and networks, technical sessions and an interactive exhibition.

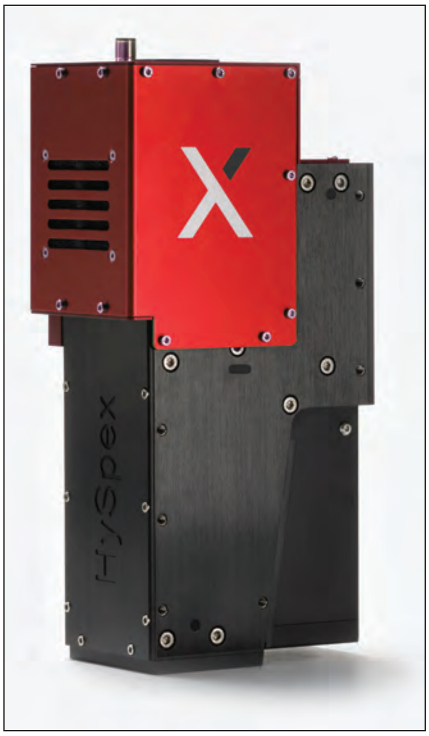
"Since the 2020 conference and exhibition occurred, OFC's co-sponsors, Steering Committee and Program Chairs have been meeting regularly to ascertain the likely impact of the current pandemic on the event," said OFC 2021 Steering Committee Chair, Seb Savory, IEEE/ Photonics Society, and University of Cambridge, UK.

"After careful consideration, having consulted various stakeholders, it became clear that the best solution at this point in time, was to shift the timing of OFC, from March to June. By moving the event to these new dates, we not only increase the likelihood that we will be able meet together in person and so able to enjoy both the usual onsite programming and exhibits, but it also better aligns the timing of OFC with other major conferences that have shifted their timing in response to the pandemic."

OFC 2021 will introduce a blended in-person and virtual format to provide attendees the greatest opportunity to reach customers, reconnect with colleagues and demonstrate innovative solutions to this community. The high-caliber plenary program will include live onsite presentations from three distinguished speakers on the latest research and applications in optical fiber communication.

The OFC 2021 technical program will continue to explore the latest in optical communications innovation, data-center connectivity, machine learning/artificial intelligence (AI), applications of optical networks in 5G and cloud computing.

HySpex launches SWIR-640 camera with sharper optics



HYPERSPECTRAL IMAGING is one of the most talked about technologies these days, mainly due to the wide range of problems it can solve, but not all hyperspectral imaging systems are created equally. HySpex, the leading brand in hyperspectral imaging, has been forging a path forward in the industry with optimal performance at the forefront.

The new HySpex SWIR-640 is no exception, offering 640 spatial pixels and 360 spectral bands, while maintaining the spectral fidelity and optical quality for which HySpex is renowned, yet at an attractive price.

A common problem faced by many users of hyperspectral imagers is aspects of optical systems propagate errors into data which can affect its interpretation. The state-of-the-art SWIR-640 camera, with its sharper optics and PSF (Point Spread Function) of 1.2 pixels in the field of view and for all wavelengths, reduces spatial and spectral misregistration to less than 10%.

This is crucial considering any errors over 10% of a pixel negatively affect material discrimination and pixel classification due to nonlinear contributions from neighboring pixels. Additionally, because errors from other systems can be up to or exceeding 50% of a pixel, the user must have more pixels covering the target of interest and even so, are still affected by contributions of neighboring pixels making these systems neither stable, nor repeatable.

Low error results in more effective pixels and far greater accuracy in detection, making the SWIR-640 the most exciting hyperspectral camera on the market today – at a lower price per effective pixel. The SWIR-640 can be used in all field, lab, and airborne applications. It is ideal for high-end researchers and commercial operations working in geology, vegetation, military, mining, food-quality and other fields where the accuracy and reliability of imaging data is crucial.

CompoundTek announces R&D collaboration for SiPh laser source

(Pictured above are KS Ang (left), COO of CompoundTek and Professor Wang (right), NTU pictured together with a prototype of the packaged tuneable laser.)

COMPOUNDTEK PTE LTD, a Singapore-based foundry services provider in emerging Silicon Photonics (SiPh) solutions, is working with Nanyang Technological University, Singapore on a three-year joint R&D collaboration for 'O, C, L-band Silicon Photonics tuneable Lasers for Communications and Other Emerging Applications'.

One of the primary objectives is to develop a high-performance tuneable laser that has a compact footprint and is scalable, high-yield and suited for low-cost manufacturing. By replacing the commonly used array of single wavelength lasers with a single wavelength tuneable laser, this much-simplified design architecture reduces existing complexities of optical Wavelength Division Multiplexing (WDM) systems, and will additionally lower wavelength contention and inventory costs for commercial products.

The SiPh platform today offers scalability, cost-effectiveness and manufacturability of the matured Si CMOS process.

However, one of the key disadvantages of SiPh is the non-availability of highly-efficient silicon laser integrated with SiPh circuits.

Hybrid SiPh, integrating SiPh devices with III-V compound semiconductor optical amplifier (SOA), offers the best of both worlds – enabling low propagation loss and high integration densities while providing efficient optical gain and flexibility for spectral engineering. This integration is one of the key research areas at NTU's The Photonics Institute.

Cambridge spin-off Nu Quantum raises £2.1m

BRITISH QUANTUM photonics start-up Nu Quantum has raised £2.1 million in Seed funding in a round led by Amadeus Capital Partners.

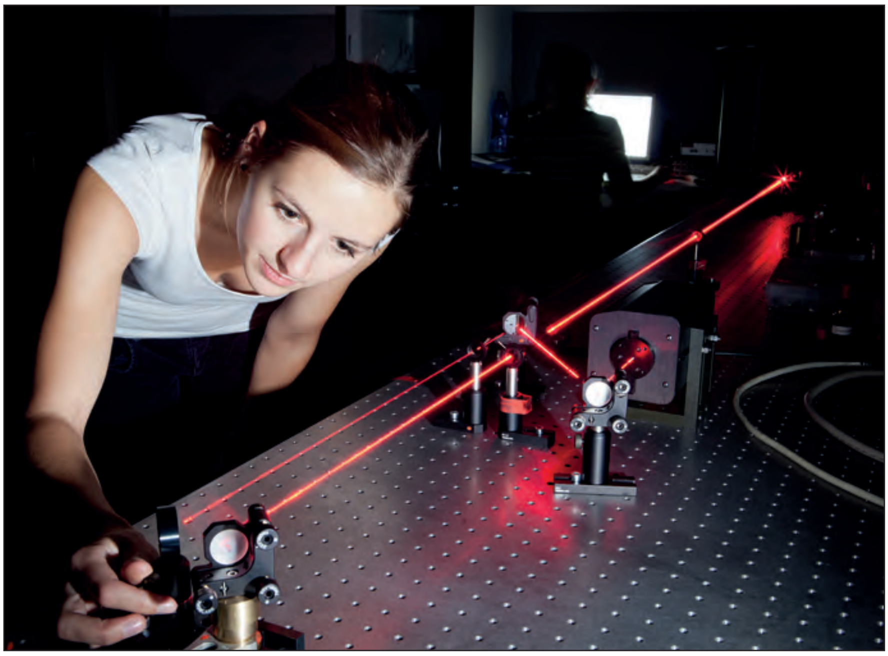
Ahren Innovation Capital, IQ Capital, Cambridge Enterprise and Martlet Capital have also followed-on from the company's pre-Seed investment round last September, with Seraphim Capital joining as a new investor.

The funding will go towards a state-of-the-art photonics lab in Cambridge and a major recruitment ive for scientists, product team members and business functions as the company approaches the launch of its first commercial technology demonstration.

Nu Quantum brings together a portfolio of intellectual property combining quantum optics, semiconductor photonics, and information theory, spun out of the University of Cambridge after eight years of research at the Cavendish Laboratory carried out by the two co-founders Matthew Applegate and Carmen Palacios-Berraquero.

The company is developing high-performance light-emitting and light-detecting components, which operate at the single-photon level and at ambient temperature. Nu Quantum is one of a handful of companies in the world developing this kind of technology. The components could become an integral part of larger quantum photonics systems – which will employ this kind of technology in the thousands – enabling applications such as quantum cryptography and simulation.

The company's first commercial deliverable will use quantum photonic technology and proprietary algorithms to generate random numbers extracted from quantum-level effects, giving the highest confidence in the quality of these numbers which are ubiquitously used as cryptographic keys to secure data. Nu Quantum is a partner in the consortium led by the National Physical Laboratory, developing the UK standard for quantum random number generation, a project which was awarded £2.8m from the UK government's Industrial Strategy Challenge Fund.



Carmen Palacios-Berraquero, CEO, Nu Quantum, commented: "Our aim is to enable the potential of quantum mechanics using quantum photonics hardware.

This funding will allow us to do just that – a world-class multidisciplinary team and our new laboratories will give Nu Quantum the ability to deliver meaningful demonstrations of our technology into the hands of customers and partners for the first time."

Peter Knight, chair of the UK Quantum Technology Initiative Strategy Advisory Board and former chief scientific adviser at the UK National Physical Laboratory added:"I'm delighted to see Nu Quantum, one of the UK's leading quantum photonics companies, achieve this investment milestone to enable the translation of its founders' world-class academic research into the commercial world. This is further validation of the quality of the UK capability in this critical area of technological innovation."

Alex van Someren, managing partner, Amadeus Capital Partners, said: "Quantum photonics has the potential to transform cyber security through digital cryptography. We're making another investment in Nu Quantum because we believe in the team and its ability to take its solutions to market. Cambridge is leading the world on developing and commercialising quantum computing hardware and applications, and Amadeus is excited to be backing great entrepreneurs here."

Alice Newcombe-Ellis, founding and managing partner, Ahren Innovation Capital said:"We are proud to have backed Carmen, Matthew and their team since the formative idea stage of Nu Quantum. We invest in exceptional founders with big visions, applying deep tech in highly disruptive technologies and Nu Quantum is a great example of this, applying fundamental properties of physics to enable secure communication in a quantum future."

Ed Stacey, managing partner at IQ Capital said:"Nu Quantum is one of the foremost companies in the world developing quantum photonics technology and is playing a major role in iving the UK's capabilities in quantum computing. We are proud to invest in this team once again as the company undertakes significant growth and begins to demonstrate the real-world applications of the technology it has developed. The proprietary technology it has created, and the vision and expertise of the team, give Nu Quantum the potential to ive quantum computing on a national and international level."

Tiny PICs have huge impact on optical wafer testing

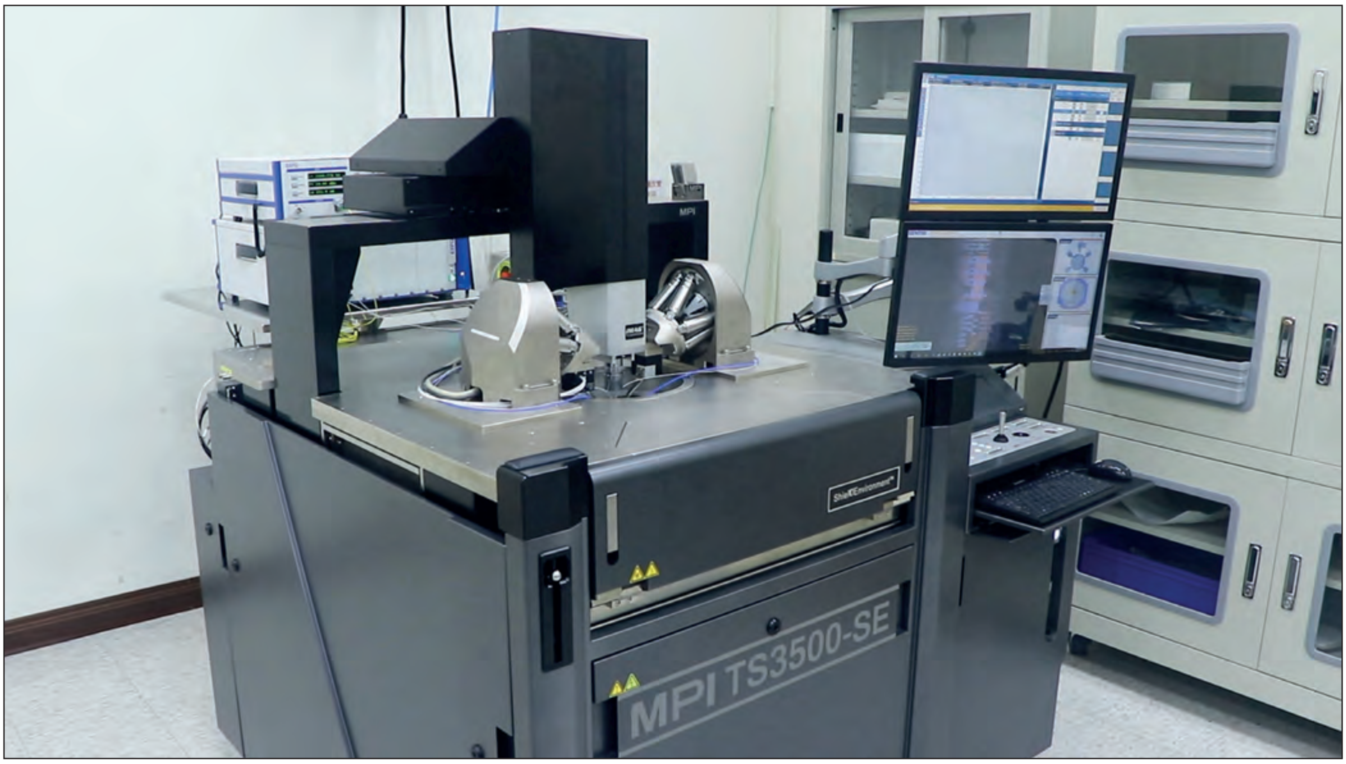
Given the out-sized role silicon wafers play in creating photonic integrated circuits (PICs), non-automated/non-integrated testing setups impede optimization. Testing needs to be automated to ensure high quality, fast throughput for applications including high-speed data centers and 5G networks. A unique partnership is working to automate and optimize testing solutions.

BY LAWRENCE VAN DER VEGT, SUBJECT MATTER EXPERT, EXFO, WITH CONTRIBUTIONS FROM ASHKAN SEYEDI, SENIOR RESEARCH SCIENTIST, HEWLETT-PACKARD ENTERPRISE, AND SEBASTIAN GIESSMANN, PRODUCT MARKETING MANAGER, MPI

Testing photonic integrated circuits for next-generation networks

Optical testing presents a major bottleneck in PIC component manufacturing due to tight tolerances in optical wafer testing compared to electrical testing. In fact, based on statistics driven by data from foundries and design houses, EXFO estimates that optical testing and component assembly currently comprise 80 percent of test and assembly cost of the final product.

Three industry innovators – EXFO, Hewlett Packard Enterprise (HPE), and MPI Corporation – have addressed the challenges posed by wafer level



EXFO/HPE/MPI integrated test solutions for PICs at the wafer level

optical testing with their advanced, interoperable measurement solutions which are now commercially available.

The three companies recently presented a webinar produced in association with PIC Magazine, sharing the strategies and technologies that deliver on the promise of integrated testing. The collaborative solution makes automated wafer level testing of PICs faster, more reliable, and scalable.

Joining forces to improve optical testing

EXFO, HPE, and MPI were familiar with each others' capabilities in their respective areas of expertise. The companies decided to combine resources to deliver integrated test and measurement solutions that would operate quickly and accurately.

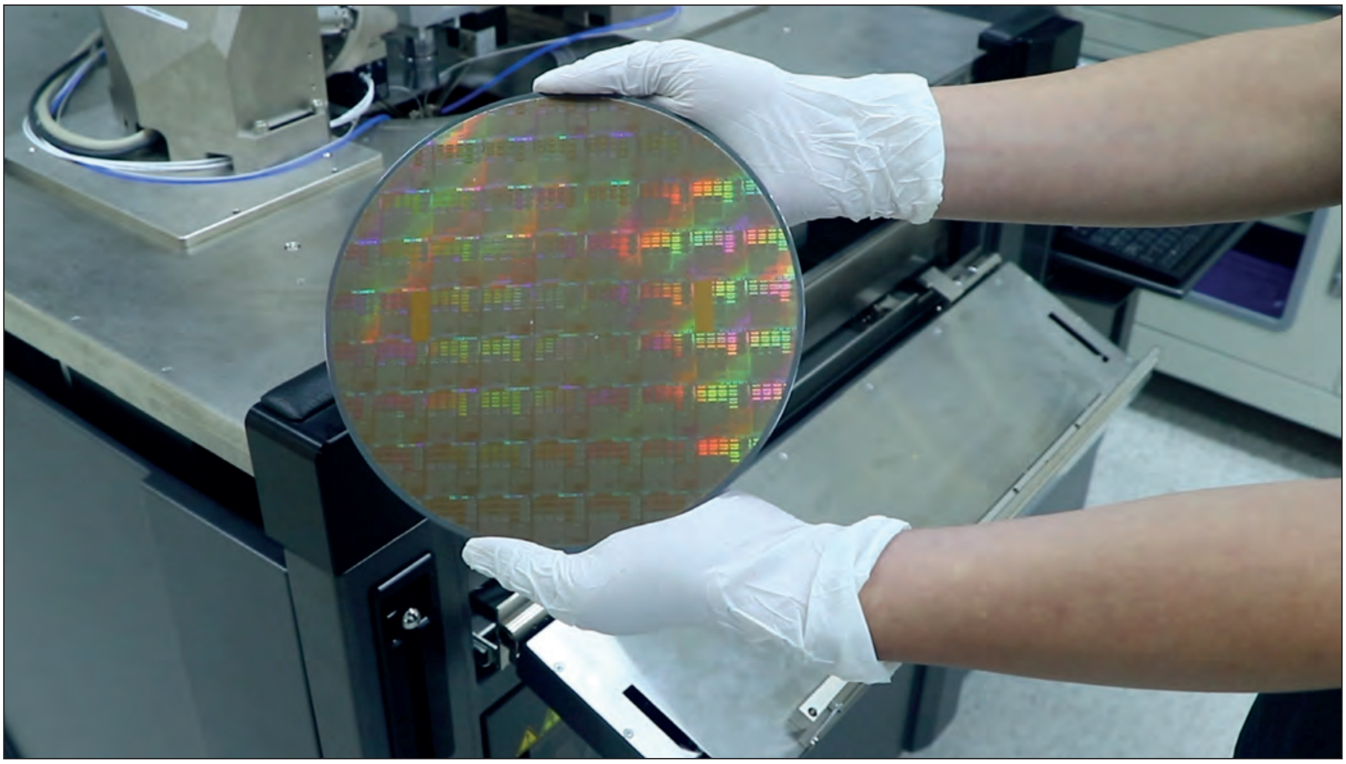
The main objective of the initiative was to provide solutions rather than just test instrumentation. Wafer discs are provided by HPE; wafer handling and probe alignment is addressed by MPI; optical test and measurement is made available by EXFO. The integrated approach makes it possible to provide turnkey solutions based on customer needs. The testing solutions resulting from the collaboration are described as "Tiny PICs – Huge Impact" because they bring a new level of reliability and automated testing to PIC manufacturing.

By creating a system that is scalable and agnostic, these PIC testing solutions can be used at any stage within the PIC ecosystem: during research and development, at the foundry, or on the assembly line. And because results are reliable and consistent, a common set of data can be cross-referenced among all users. Here is a snapshot of what each company contributes to the integrated solution:

EXFO provides test solutions at the component and sub-component level, as well as the system and network levels. In this instance, test & measurement of componentry is the focus. EXFO's CTP10 passive optical component tester with T100S-HP high-dynamic range tunable laser enables swept laser testing of passive optical components at picometer resolution and at high speeds, even under the most stringent conditions. The auto-alignment capability of the CTP10 enables finding the optimum optical in- and output connections of the PIC on the wafer disc in the fastest time possible.

HPE's overall goal is accelerating business outcomes with comprehensive solutions from the edge to the cloud. That includes providing better computer hardware components to handle the data deluge experienced by network operators. Improvement starts at the wafer level where HPE relies on customer co-design/optimization using HPE's Silicon Photonics (SiPh). HPE's wafer technology is at the heart of the EXFO, HPE, and MPI collaborative solution.

MPI's Advanced Semiconductor Test division concentrates on various applications for high frequency device modeling, wafer level reliability, and high power. PIC-specialized wafer probe stations enable precision optical component alignment, and other dedicated functionality within the unique SENTIO® software. This advanced software provides highly intuitive prober control.



HPE wafer technology

Industry realities and HPE's contribution

Ashkan Seyedi, Senior Research Scientist at HPE, is well aware of challenges in the industry regarding adoption of automated wafer testing processes. Manufacturing of electronic components is long established, including automated testing capability. However there is limited foundry availability for photonics, with only approximately 10 such foundries worldwide.

Photonic testing is primarily manual, using electronic tools that have been adapted to support emerging requirements.

"As the pluggable silicon photonics starts to ramp up, some assembly houses are learning how to do semi-automated testing, but it's still not anywhere near where it needs to be to hit mass volume," Seyedi said. Market excellence relies on fulfilling the end-to-end experience from design to assembly and testing, to producing the final product, he adds. Automated wafer-level testing of silicon photonic wafers is critical at the foundry and testing stages.

"In an ideal world, it needs to be fully automated so that you can basically load the wafer, load the test program, do some alignment and setup, press play, and just walk away and know that you get your either pass or fail, essentially," said Ashkan.

Testing must be fast and reliable and fully scalable to accommodate additional testing capability that ties in with design generation via electronic design automation (EDA) tools. HPE's wafer technology is an active contributor to the complete EXFO/HPE/MPI solution based on data derived at the PDK (Product Development Kit) level and HPE's customer co-designed and optimized Silicon Photonics (SiPh).

Project goals and MPI's solutions

For the integrated EXFO/HPE/MPI project, goals established at the outset included the most common criteria for testing photonic integrated circuits:

- **Speed:** keeping total wafer testing time to a minimum
- **T&M response time:** faster than the PIC under test
- **Accuracy:** traceable and without assumptions
- **Repeatability:** a one-time measurement should be conclusive
- **Flexibility and scalability:** ability to add functions and features over time
- **CAPEX savings:** reduce costs with optimized investments

A key part of delivering on these goals is precise optical measurement. Sebastian Giessmann, Product Marketing Manager at MPI, says MPI's contribution is the integration of the silicon photonics test requirements into the wafer probe station environment.

To accommodate photonic testing, modifications were made to MPI's standard semi-automatic probe stations. MPI's extra-stable probe platen provides a vibration-free platform for the photonics alignment positioner. All the wafer loading can be done automatically using a robot and testing can continue 24/7 on high quantities of wafers. PIC devices can be tested on wafers up to 300 mm in size with single fibers and fiber arrays.

> After completion of the measurement, the CTP10 automatically provides the data analysis of the PIC measured, bringing the total alignment to measurement time to an impressive 5.5 seconds. With regard to wavelength, the accuracy is within +-5 picometres with options available to reduce this into the sub-picometer accuracy range typically required for ring resonator testing

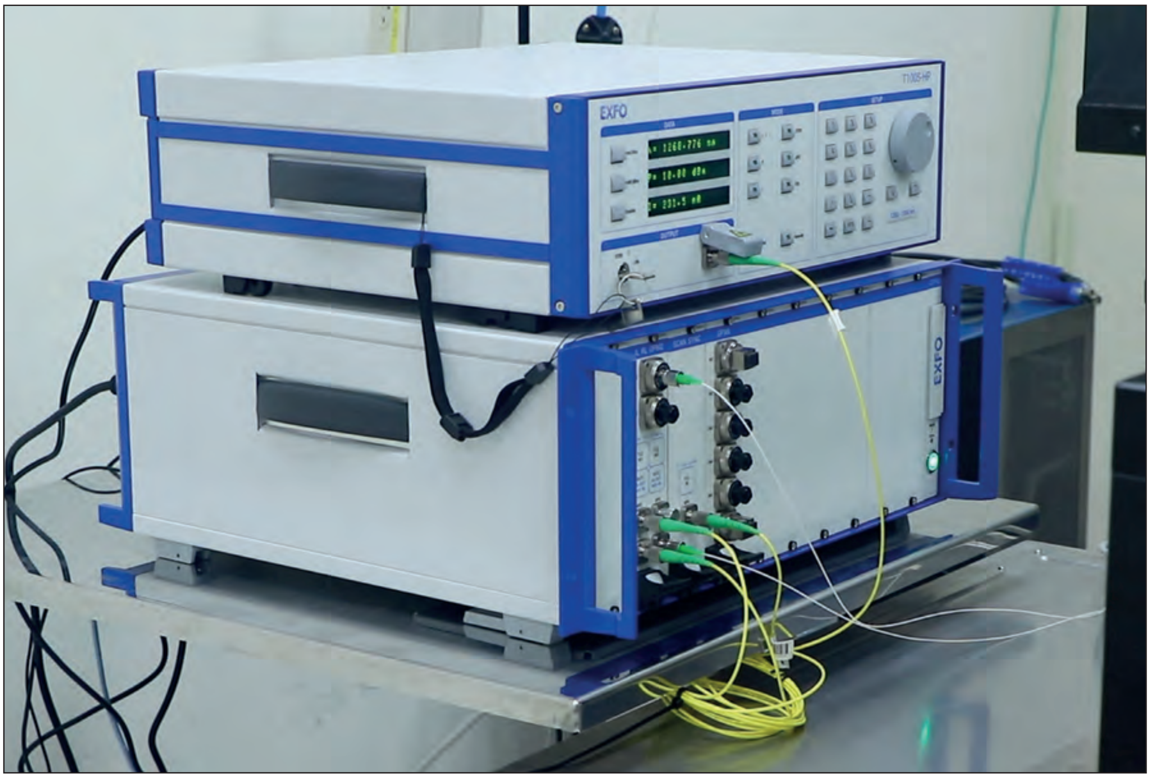
The PIC-specialized wafer probe stations enable precision optical component alignment, and additional dedicated functionality. Safety is addressed by providing collision prevention between fibers and the wafer. "To set it up in previous systems can take very long times," Sebastian said. "In our case it's done within seconds and stepping to the next die is a very precise functionality with this probe station. Testing a full wafer is much easier with this kind of automated solution." The unique SENTIO® software is an intuitive prober control software that enables easy navigation and test setup, he added.

EXFO's test and measurement stage offering

With industry-leading wafer technology and precision alignment, testing moves forward with EXFO technology.

The test and measurement setup includes a CTP10 passive optical component tester with two tunable laser sources and a PDL controller for testing passive PIC components. As outlined above, auto-alignment of fiber probes onto the PIC is optimized using the MPI probe station for faster wafer alignment. This enables EXFO's CTP10 to find the best optical in- and output connections of the PIC on wafer in the shortest time possible. Data is processed, and the CTP10 moves to the next position or PIC device. That process then repeats.

After completion of the measurement, the CTP10 automatically provides the data analysis of the PIC measured, bringing the total alignment to measurement time to an impressive 5.5 seconds. With regard to wavelength, the accuracy is within +-5 picometres with options available to reduce this into



MPI probe station for fast wafer alignment the sub-picometer accuracy range typically required for ring resonator testing. Because of the speed, accuracy, and reliability of the end-to-end system, data collected from testing is consistent and can be compared across the industry by users as needed.

EXFO CTP10 for fast swept optical measurement

The future looks bright

One of the key takeaways from the collaboration according to HPE's Ashkan Seyedi is to not think about layout, fabrication, and testing as three independent entities. Ideally, test solutions would be informed at the design time, "so that when you're designing something, you're doing your floor planning, you're doing your layout. You keep your testing solution in mind. Because sometimes what we've done in the past, what we've realized the problems are, are artificial problems." Or put another way: "If I knew how I was going to test it, maybe I would have designed it a little bit better," Ashkan quips.

With 5G networking rolling out and high-speed data centers moving data at unprecedented speeds, it is imperative that the foundation of the network be solid. This starts at the wafer level and relies on accurate, fast, and scalable automated testing for photonic components. EXFO, HPE, and MPI have collaborated to help meet that need by delivering an integrated optical wafer testing solution specifically designed for photonics.

Instead of relying on manual or semi-automated solutions derived from existing electronic test formats, the industry now has a better solution.

The bottleneck in component manufacturing has been unblocked and the industry is benefiting from process and CAPEX improvements. Tiny PICs are indeed having a huge impact on optical wafer testing.

About the authors:

Lawrence van der Vegt, Subject Matter Expert, EXFO

Lawrence is an optics veteran; he earned his Bachelor's degree in Electrical and Computer Engineering in the Netherlands and has held various key directorial positions at optical T&M companies in the Netherlands and the U.S.A. He is currently active as a Subject Matter Expert on behalf of EXFO, involved in passive and active component testing driven by PIC technologies.

Ashkan Seyedi, Research Scientist, Hewlett-Packard Enterprise (HPE)

Ashkan received a dual Bachelor's degree in Electrical and Computer Engineering from the University of Missouri-Columbia and a Ph.D. from the University of Southern California working on photonic crystal devices, high-speed nanowire photodetectors, efficient white LEDs and solar cells. While at Hewlett Packard Enterprise as a research scientist, he has been working on developing high-bandwidth, efficient optical interconnects for exascale and high performance computing applications.

Sebastian Giessmann, Product Marketing Manager, MPI Corporation

Sebastian received his degree in Electrical Engineering from the Dresden University of Applied Science. He has held various positions in R&D, application support and product management in the semiconductor test industry. Currently he is responsible for probe systems product marketing at MPI Corporation and with specialization in silicon photonics testing.

For more information

To learn more please visit:

EXFO PIC testing solutions:
https://www.exfo.com/en/solutions/academic-research-institutions/pic-testing
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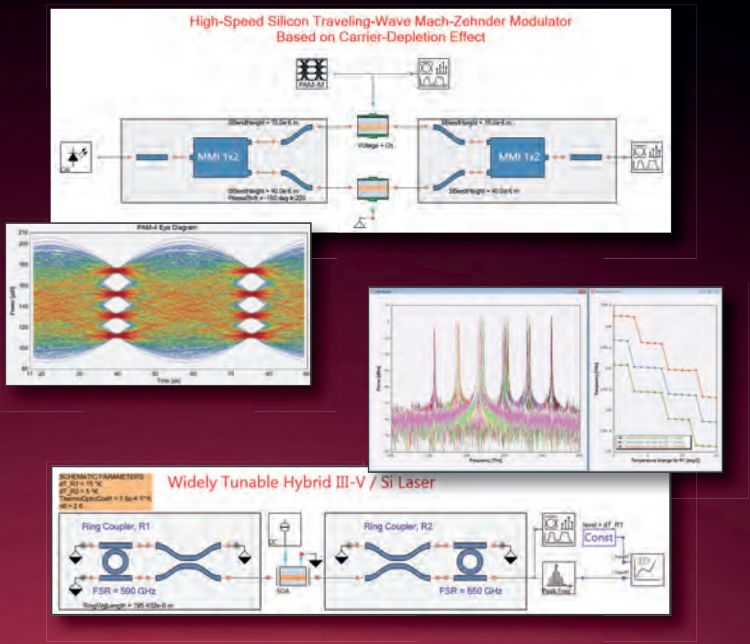
MPI Corporation silicon photonics website:
https://www.mpi-corporation.com/ast/engineering-probe-systems/mpi-automated-systems/siph-upgrade/
Contact: Sebastian Giessmann:
sebastian.giessmann@mpi-corporation.com

HPE follow-up:
Contact Ashkan Seyedi:
ashkan.seyedi@hpe.com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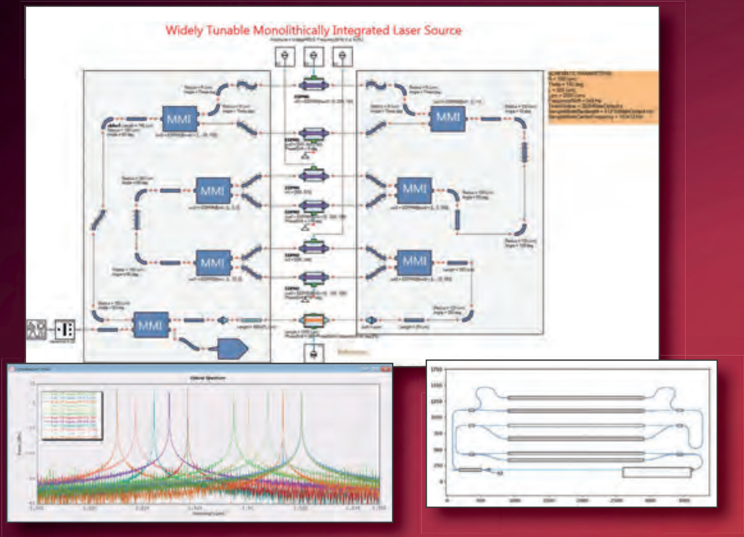
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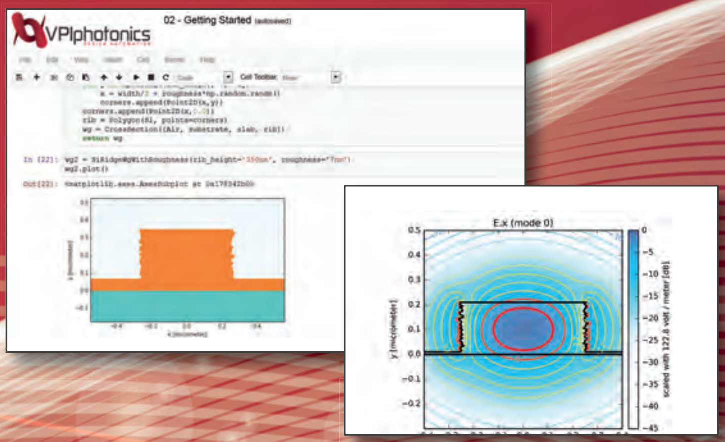
VPIphotonics
02 - Getting Started
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Photonic Integrated Circuits for **sensing applications**

Companies developing products for optical communications, 3D sensing, biosensing, or spectroscopy are increasingly incorporating photonic integrated circuits (PICs) because they offer economic and functional advantages. PICs offer smaller size, higher data rates, lower power consumption, and steadily improving reliability paired with ever-increasing cost advantages, making PICs an ideal solution for many applications.

BY ANA GONZALEZ, R&D MANAGER AT EPIC

IN THE LAST FEW YEARS, PICs have demonstrated their potential for a range of sensing devices such as LiDAR, biosensing, Optical Coherent Tomography (OCT) and spectrometry, which are different from PIC optical communications applications. In this article, we look at the opportunities for PICs in these new application fields and review the role of pilot lines in this active photonic ecosystem.

Introduction

PICs are usually fabricated with a wafer-scale technology to produce a substrate (chip) on which many functionalities can be integrated in a single production process. Substrate material varies according the functions to be integrated.

For instance, silicon photonics and Si_3N_4 (silicon nitride) have desirable properties for passive components like Arrayed Waveguide Gratings (AWGs); the fabrication technology is very mature while GaAs or InP allow direct integration of active components, i.e. light sources, detectors and other building blocks providing the same functionality while achieving lighter devices that are often cheaper and have no moving parts; compared to microelectronics they are not as susceptible to vibration and are more mechanically stable.

3D sensing

The main driver for PIC-based LiDARs is the automotive industry, which is developing LiDAR-based innovations in the field of safety systems such as ADAS, in-dash controls, and telematics. Original equipment manufacturers (OEMs) and component suppliers have been actively investing to reduce the cost and size of these components and systems for mass and mid-segment vehicles; therefore, PIC-based solutions are particularly attractive for automotive applications. The global automotive ADAS market was valued at $37.33 billion in 2019 according to market analysts and is expected to grow to $94.84 billion by 2024. For market players, this will create an incremental growth opportunity worth $57.51 billion by 2024, which translates to around 154 percent of the market size in 2019 (see Figure 1).

A conventional LiDAR device generally consists of two basic components: the transceiver and the receiver, which include a light source (laser, LED or VCSEL diode); scanner and optics (e.g. an oscillating mirror to omit light and/or an aspherical lens), a photodetector and electronics.

PICs can be used to replace these components with miniaturized versions to produce a more compact and lighter final device, e.g. the beam-steering part of the LiDAR can be replaced with optical phased arrays that are able to shape the laser beam and rapidly steer it for video-rate three-dimensional imaging.
PICs offer other advantages including immunity to electromagnetic interference and can easily handle the high volumes of data produced through LiDAR. Also, in comparison with RADAR systems, which rely on radio-waves, LiDAR uses visible to near infrared light to provide distance measurements with higher resolution; the light spectra ranges from 250 nanometres (ultraviolet) to 10 micrometres (infrared) wavelengths.

Companies interested in developing new PIC-based LiDAR systems can take advantage of initiatives launched by the European Union’s Horizon 2020 research and innovation programme in Public-Private Partnership with Photonics 21 (www.photonics21.org) such as the JePPIX pilot line and PIXAPP. JePPIX enables high TRL development in a scalable, design kit driven process, driving open access InP PICs from proof of concept to industrial prototyping and pre-production. PIXAPP offers services for packaging and assembly of these chips using standardized building blocks. PIXAPP building blocks are compatible with chips from MPW runs and Package Design Kits are available at different European foundries such as Fraunhofer HHI, III-V labs, Smart Photonics, Imec, CEA-Leti and LioniX International.

Another 3D sensing technique in which PIC technologies have a big potential is optical coherence tomography (OCT,) an imaging technique that uses low-coherence light to capture micrometre-resolution, two- and three-dimensional images from within optical scattering media (e.g., biological tissue). It is used for medical imaging and industrial non-destructive testing. OCT is based on low-coherence interferometry, typically employing near-infrared light. The use of relatively long wavelength light allows it to penetrate the scattering medium. In the case of spectral-domain OCT (SD-OCT) most of today’s systems rely on CCD detectors, which cannot scale arbitrarily without sacrificing performance.

Figure 1. Global Automotive ADAS market size and forecast 2019-2024 ($ billions). Courtesy of Technavio (market report available for EPIC Members).

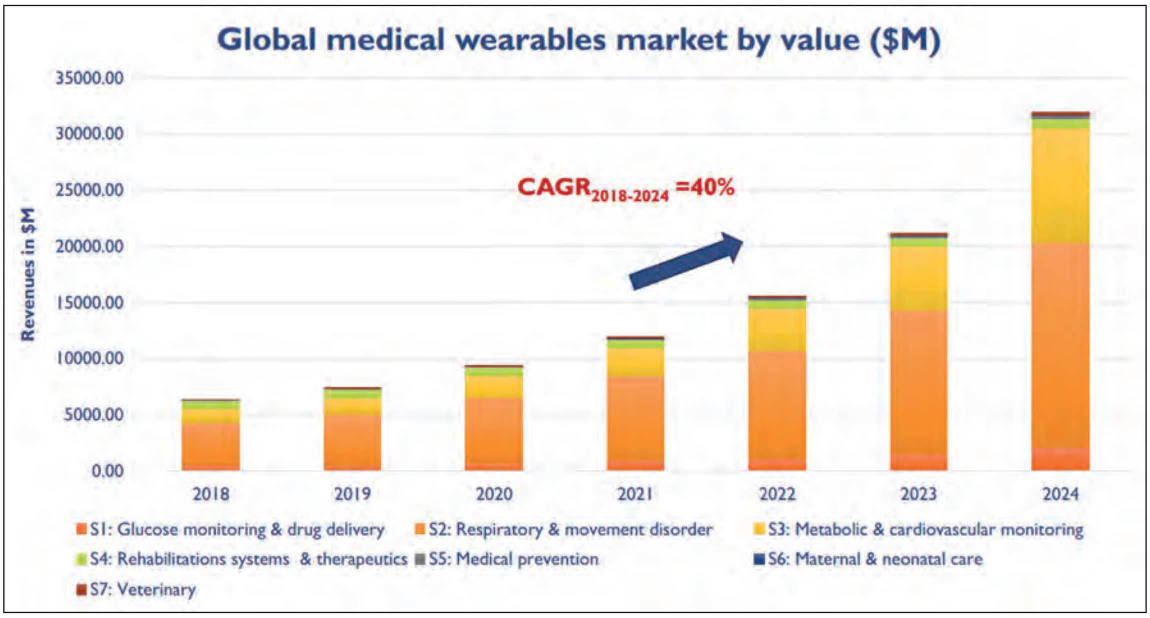

Figure 2. Market forecast for the global medical wearables market. Courtesy of Yole Development (market report available for EPIC Members).

The advantage of PIC waveguide integrated photodetectors in OCT systems is that they can be used to form a complete spectrometer in a footprint smaller than 1 cm^2. Semiconductor photodiodes are also much faster than CCDs, allowing for the OCT scan rate to scale.

Regarding swept-source OCT (SS-OCT), PICs can be used to provide the laser source, which can deliver better coherence lengths with tuning ranges of up to 80 nm in monolithic InP devices. With the use of electro-optic tuning, PICs have the potential to unlock scan rates well into tens of gigahertz with existing technology. In addition, the size reduction made possible by PIC technology can enable handheld OCT devices, possibly even disposable products, without sacrificing performance.

Biosensing and wearable sensors

Reliability, reproducibility, and accuracy are key parameters in the diagnosis field for clinical applications, which so far has only been achieved with sensing systems that are big and costly. Moreover, such systems frequently require pre-treatment steps by skilled personnel before the sample can be introduced into the machine, which increases the overall time and cost of the assay.

The advantage of PIC-based biosensors is that they allow the detection of a specific biomarker in a complex sample in a direct way, without the need of pre-treatments nor operation by skilled personnel. In this kind of device, selectivity is provided by attaching a specific biomolecule, a bioreceptor, to the sensing PIC.

The bioreceptor will react specifically with the biomolecule to detect affecting the light confined in the PIC. Microfluidic technology will be also required, with special attention to prevent the formation of bubbles and irreproducible turbulences. Also, biochemistry plays a dominant role in these kind of devices as biomolecules must be attached on a solid surface which could force proteins in the bioreceptors to unfold and to lose their functionality.

Biosensing is a very transversal field involving semiconductor development, optical engineering, mechanical packaging, biochemistry optimization and polymer technology, which needs the right level of development in all the different technologies related to reach the intended point-of-care application. The PIXAPP pilot line has finalized the optimization of the different building blocks required for the packaging of a biosensor chip for point-of-care applications. These building blocks include the SiN-PIC chip, polymer microfluidics, spring-loaded DC contacts, lensed fibre array and a LIFT microlense system.

The medical wearables market is expected to reach more than $31.9 billion in 2024, growing at a rate of up to 40 percent (see Figure 2). Sensor manufacturers for wearables are becoming interested in developing new PIC based platforms to meet the challenges of high level integration of electronics, low power consumption, format and conformability. Extremely novel wearable sensors are being developed in this context, including smart watches for heart rate monitoring, patches for sleep apnea and wearable oxygen diffusion sensors for tracking wound healing, etc.

Despite the potential of PIC technologies for wearable devices, many companies developing current healthcare devices lack the knowledge and expertise required for the design of PIC based systems for medical wearables. To overcome these challenges, the new MedPhab pilot line offers the services and expertise for developing medical devices for in-vivo and in-vitro diagnostics, including hospital use, home care devices and equipment for molecular diagnosis.

Optical spectrometry

Optical emission spectroscopy has wide application in several industries, particularly for the detection and sensing of gases, e.g. for monitoring chemical processes, to identify environmental climate-relevant gases CO_2, methane and ammonia as well as monitoring other harmful emissions. Other applications include monitoring the manufacture of food and beverages, the growth of crops and the identification of pathogens and biological screening, e.g., to identify cancerous cells.

Conventional optical spectrometers are capable of outstanding sensitivity, selectivity, and longevity, but are held back by their high costs. PICs are well placed to help overcome this hurdle because they combine several functionalities on a substrate, e.g. lasers, modulators, detectors and amplifiers; they can thus build on the strengths of optical detectors and potentially reduce their price, size and footprint.

In the case of gas detection, there are two fundamental direct absorption measurement techniques for PICs. The first approach is to use a tuneable, single-mode laser and a broadband photodetector to target narrow absorption lines as typically present in gases. The second approach is to use a broadband light source and spectrometer, which, depending on the type of spectrometer, can measure the whole spectrum simultaneously.

PICs can also be used for indirect measurements, such as opto-chemical detection schemes, where a chemical reaction is optically probed to obtain a gas concentration, e.g., fluorescence measurements MIRPHAB is a European funded pilot line for prototyping and producing spectroscopy devices based on Mid-IR technologies that are able to operate in both gas and liquid mediums. MIRPHAB provides an innovative technology for miniaturized chemical sensors by using PIC technology able to transmit in the Mid-IR region.

Conclusion

PIC-based technology has enormous potential for improving the functionality and decreasing the size, cost, and weight for various sensing applications. In the case of 3D sensing, there is the exciting possibility that because of the inherent advantages of PIC-based systems LiDAR technology may be able to break into mass and mid-segment vehicle sectors.

For medical wearables, PIC systems will improve utility, expand the market and ultimately improve long-term health monitoring both inside and outside of clinics and hospitals. PICs also have the potential to greatly enhance OCT systems as they can address issues around scalability and miniaturization. For optical spectroscopy, PICs can build on the strengths of optical detectors and potentially reduce their price, size, and footprint.

Across the supply chain, European photonics pilot lines are moving fast to address two main challenges: accelerating the technological and manufacturing readiness needed for enabling mass-volume production while also moving to foster a strong, unified ecosystem to ensure the adoption of design and manufacturing standards that will be required to ramp up volumes.

Dr. Ana González is currently R&D Manager at EPIC (European Photonics Industry Consortium). Her role is to understand the technology developed by EPIC members and to identify potential collaboration between them. She also participates in different EC initiatives such the Pilot Lines in Photonics in which she is involved in business development and marketing strategy. Her expertise lies in the development of optical systems and the investigation of applications such as Sensing and Datacom. She received her bachelor's degree in Chemistry from the University Autonomous of Barcelona (UAB) and her PhD degree from the Catalan Institute of Nanoscience and Nanotechnology (ICN2).

EPIC is the European industry association that promotes the sustainable development of organizations working in the field of photonics. Our members encompass the entire value chain from LED lighting, PV solar energy, Silicon photonics, Optical components, Lasers, Sensors, Displays, Projectors, Optic fiber, and other photonic related technologies. We foster a vibrant photonics ecosystem by maintaining a strong network and acting as a catalyst and facilitator for technological and commercial advancement. EPIC works closely with related industries, universities, and public authorities to build a more competitive photonics industrial sector, capable of both economic and technological growth in a highly competitive world-wide marketplace. www.epic-assoc.com

EPIC Partners

PIXAPP is the world's first open-access Photonic Integrated Circuit (PIC) Assembly and Packaging Pilot Line. Developing multiple standardized packaging and packaging building blocks, the PIXAPP pilot line aims to help leading companies and SMEs to exploit PIC technologies for improving their current products and/or to transfer their PIC-related research(es) into PIC-based products. PIXAPP has received funding from the European Union's Horizon 2020 research and innovation programme under Grant Agreement N° 731954 (www.pixapp.eu)

JePPIX Pilot Line democratizes access to industrial prototyping and pre-production of high-performance InP photonic integrated circuits (PIC). InPulse has the ambition to transform business practices from vertical integration – where design, fabrication and product development are all in-house and inaccessible to new entrants, to horizontal where fabless and lab less businesses share the same manufacturing infrastructure. InPulse provides a low entry barrier access to low and medium production volumes of InP PICs. InPulse has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement n°824980 (www.inpulse.jeppix.eu)

MIRPHAB is a Pilot Line for prototyping and production of Mid-IR chemical sensing devices able to operate in both gas and liquid mediums. MIRPHAB provides a platform to ensure the bridging between technology and component development and the commercial availability of such component avoiding the risks associated with the introduction of new disruptive technologies.

The aim of MIRPHAB is to become a commercially available prototyping line in 2020. The focus of the Pilot Line is to deploy your Mid-IR prototype swiftly in the market at a minimum of capital investment. MIRPHAB has received funding from the European Union's Horizon 2020 research and innovation programme under Grant Agreement N° 688265. (https://mirphab.eu/)

MedPhab is Europe's first Pilot Line dedicated to manufacturing, testing, validation, and up-scaling of new photonics technologies for medical applications ranging from diagnostics to surgical tools and therapeutics. The purpose of the MedPhab pilot production line is to accelerate the commercialisation of diagnostic devices and instruments for treatments based on photonics, and simultaneously reduce the R&D costs. The chosen areas are devices intended for hospital use (assist doctors), home care devices (monitoring patient) and equipment for chemical diagnostics (based on use of serum, saliva, or urine sample).

MedPhab will also provide seamless transition from pilot line production to up-scaled production without a need for changing service providers. Use-case companies have been selected for the validation of the pilot line services covering both in-vivo and in-vitro domains. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 871345.

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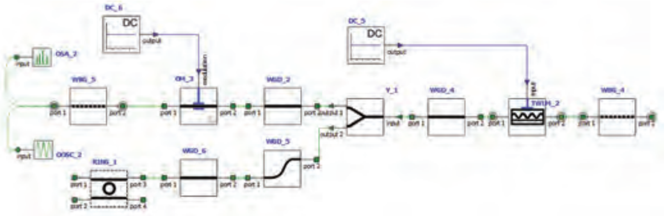
www.photonics21.org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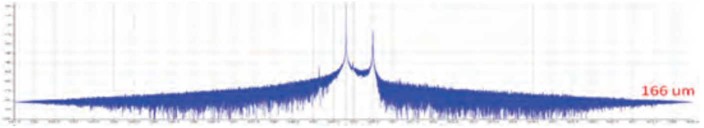
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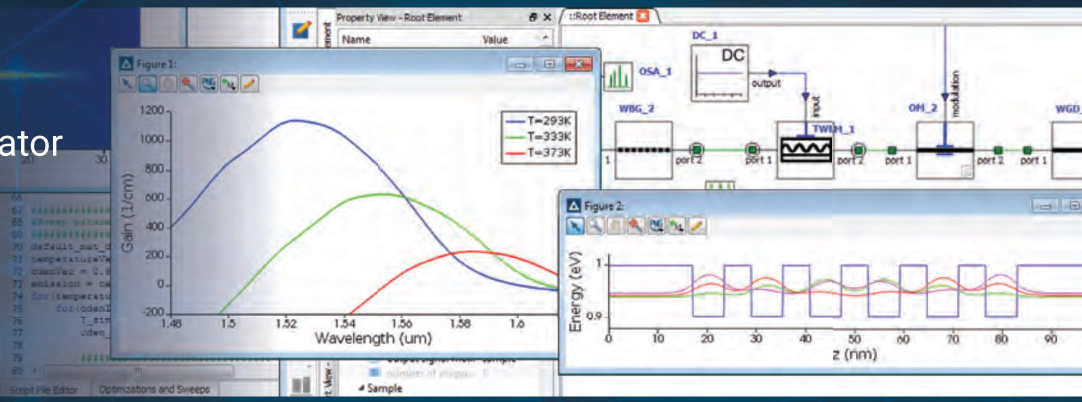
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PAM-4 transmitter PIC design using segmented-electrode mach-zehnder modulators

Photonic integrated circuits (PPIC) are rapidly bringing their size, performance and energy saving advantages to data centre operations. PIC Magazine invited the experts at SYNOPSYS to share their insights into designing PIC based PAM-4 modulators that reduce bandwidth requirements while also helping to reduce electricity consumption.

BY JIGESH K. PATEL, PRODUCT MANAGER AND DR. PABLO V. MENA, SENIOR R&D ENGINEER

IN DATA CENTRE OPTIPIC, 4-level Pulse Amplitude Modulation (PAM-4) signalling is gradually overtaking Non-Return to Zero (NRZ) signalling. [1-3]

Although both signalling schemes use intensity modulation and direct detection, PAM-4 encodes 2 bits into four intensity levels, reducing bandwidth requirements for a given data rate by half. In other words, with PAM-4 signalling, transmission of 40Gbps data rate requires components with 20GHz bandwidth (corresponding to 20GBdps symbol rate).

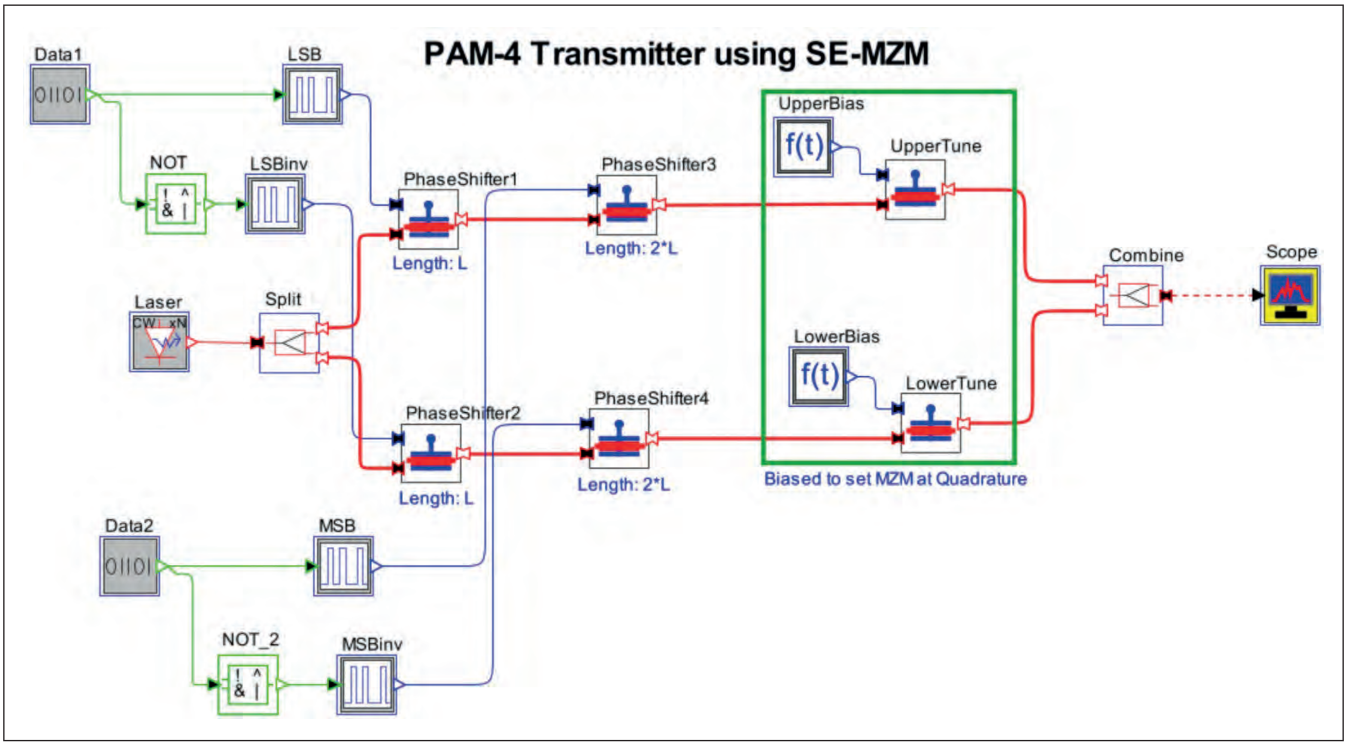


Figure 1 shows an OptSim Circuit schematic of a PAM-4 transmitter using an SE-MZM made from discrete PIC elements.

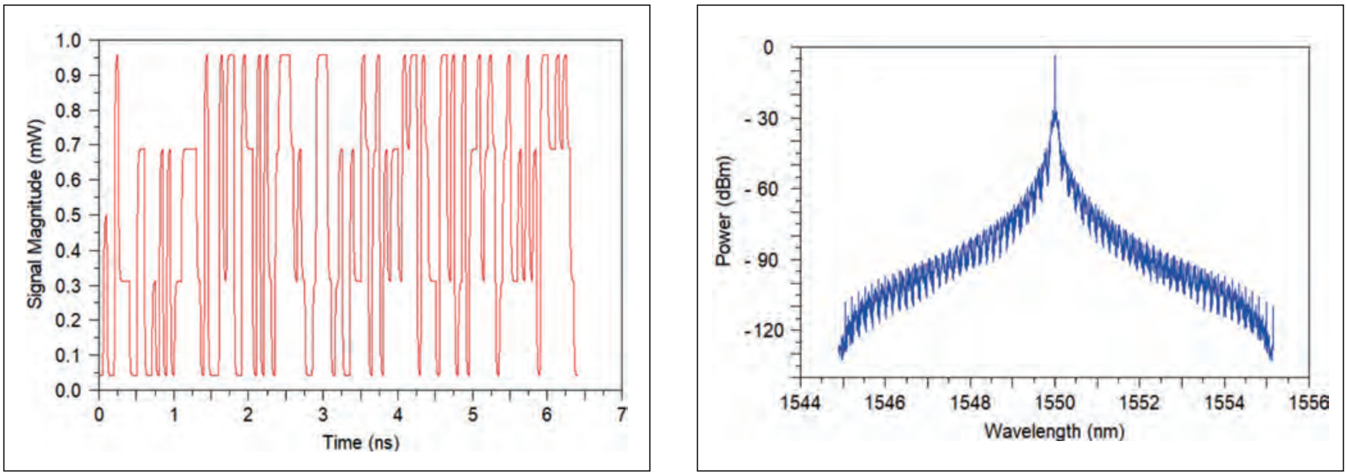


Figure 2 shows the PAM-4 modulated optical signal (left) and its spectrum (right).

This paper describes how to design a PAM-4 transmitter photonic integrated circuit (PIC) using a Segmented-Electrode Mach-Zehnder Modulator (SE-MZM), and how to study the impact of manufacturing and packaging variations on overall PIC performance.

SE-MZM-Based PAM-4 Transmitter PIC

Traditionally, in photonic PAM-4 transmitters, an MZM is driven by an electrical digital-to-analogue converter (DAC) with an electrical driver, which requires energy-inefficient electroniPIC. Implementations with nested modulators and drivers also exist, but they typically have larger footprints.

As an alternative, we can accomplish a DAC-less design using inherent DAC capabilities of segmented phase-shifters [4]. The longer interaction length in conventional traveling-wave MZMs (TW-MZMs) helps reduce drive voltage due to technology-dependent VϖL. However, longer electrodes result in higher RF losses and mismatch in group velocities between RF and optical signals, which in turn impact modulation bandwidth [5].

The segmented approach offers the advantage of longer interaction lengths without increased loss by shifting the velocity matching to electronic timing circuits to control timing of applied electrical signals to match the optical delay between segments [6].

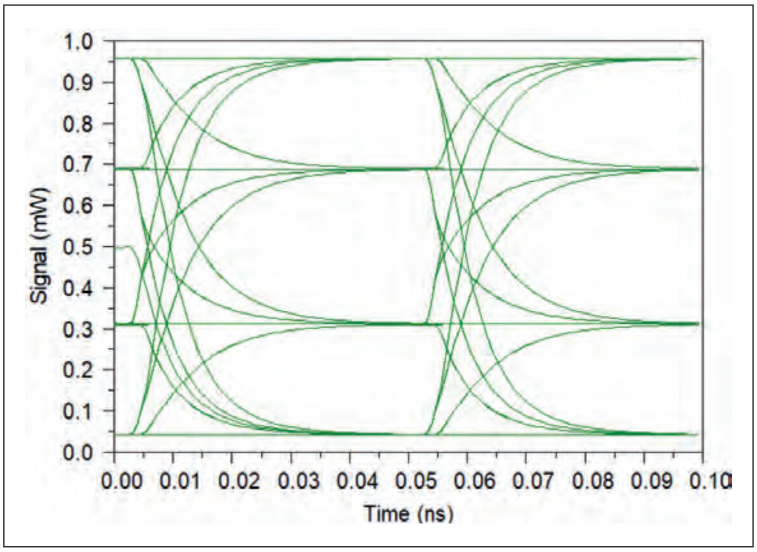
The topology comprises bidirectional PIC elements such as an optical splitter 1x2 and combiner 2x1 with user-defined power ratio, and two pairs of traveling wave optical phase shifters. The phase shifters are used to implement the segmented MZM. The lengths of the phase-shifter are binary-weighted so that each binary word can be applied directly and the number of segments is minimized, which helps with integration.

The first segment's length corresponds to one third of the total MZM length; the second segment corresponds to two thirds of the total MZM length. The 20Gbps bit sequence has already been split into separate bit patterns corresponding to the most- and least-significant bits (MSB and LSB, respectively), with the top driver modulating the first MZM segment using the LSB pattern, and the bottom driver modulating the second MZM segment using the MSB pattern.

Each traveling wave phase shifter has an optical waveguide and a surrounding electrical transmission line that introduces change in the waveguide's refractive index and propagation loss. The interaction between the electrical and optical signals is distributed along the propagation direction. The waveguide's thermal behaviour (and hence modulator) is modelled with the derivative of effective index, parameter VϖL, and propagation loss as functions of temperature [7].

Each MZM arm also has a phase tuner near the combiner, which sets the modulator at quadrature. A simple 90-degree phase shifter model from OptSim Circuit in one of the arms could have also accomplished the same, though in a packaged product; external controls for tuning are preferred to account for additional need for tuning due to, for example, factors related to ambient or manufacturing tolerances.

Figure 3 shows a 4-level PAM-4 optical eye diagram at the output of the transmitter.



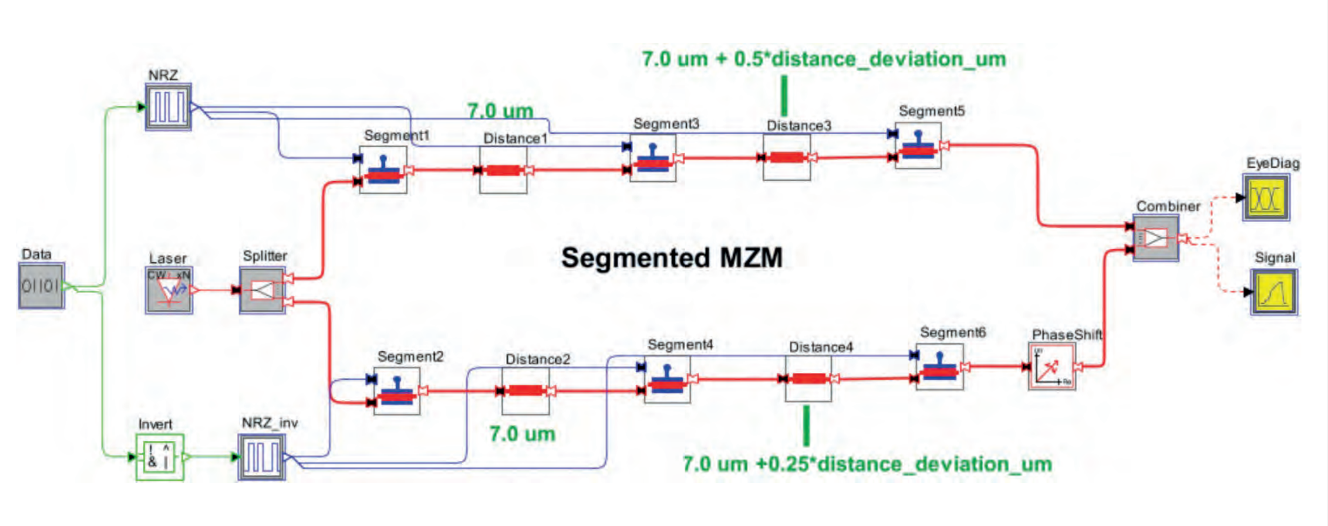


Figure 4: Scematic of a PAM-2 transmitter using SE-MZM

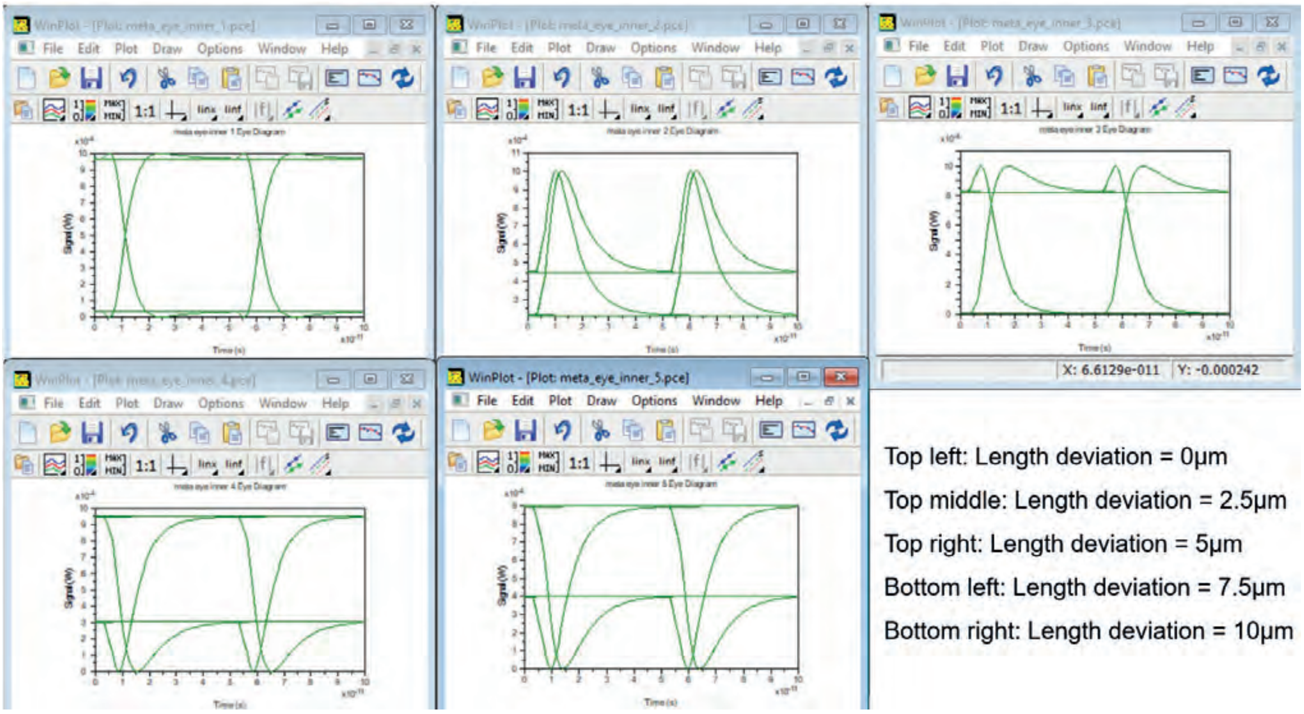
The CW light is modulated by an electrical signal derived from PRBS data followed by an electrical driver. The inverter model provides push-pull electrical bias to one of the electrodes compared to the other. At the output of the SE-MZM PIC, a scope is connected to observe transmitter output.

Now that we understand the design motives and operation of a DAC-less optical PAM-4 transmitter using SE-MZM, we will next use this segmented design concept to build a PAM-2 transmitter to analyse performance with respect to the deviations in segment-to-segment distance, driver time-delay and response time – all of which have direct impact on overall yield of SE-MZM-based high speed transmitter PIPIC.

Impact of Inter-Segment Distance Deviations

In the previous section, we designed an optical PAM-4 transmitter PIC using SE-MZM. In SE-MZM, electrodes are split in segments of specific lengths to achieve desired level of amplitude modulation.

Whether the phase shifter lengths are binary weighted or thermometer coded [8], the manufacturing process variations can result in deviations in the inter-electrodes, thereby affecting the MZM's bias and



Top left: Length deviation = 0µm

Top middle: Length deviation = 2.5µm

Top right: Length deviation = 5µm

Bottom left: Length deviation = 7.5µm

Bottom right: Length deviation = 10µm

Figure 5 shows the PAM-2 modulated optical eye diagrams.

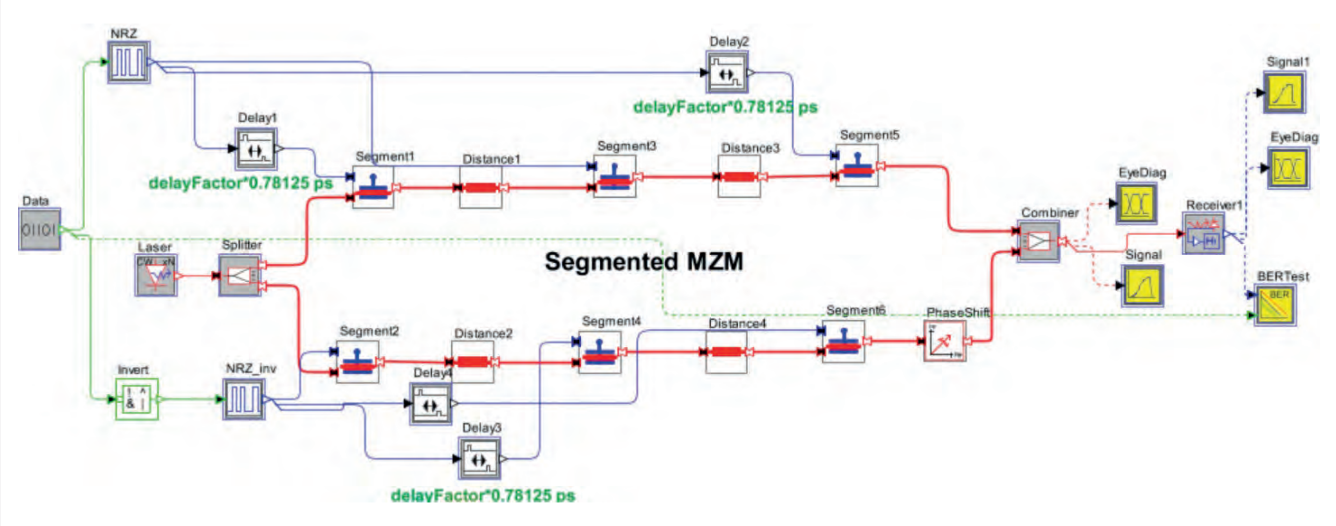


Figure 6: Schematic of a PAM-2 transmitter using SE-MZM

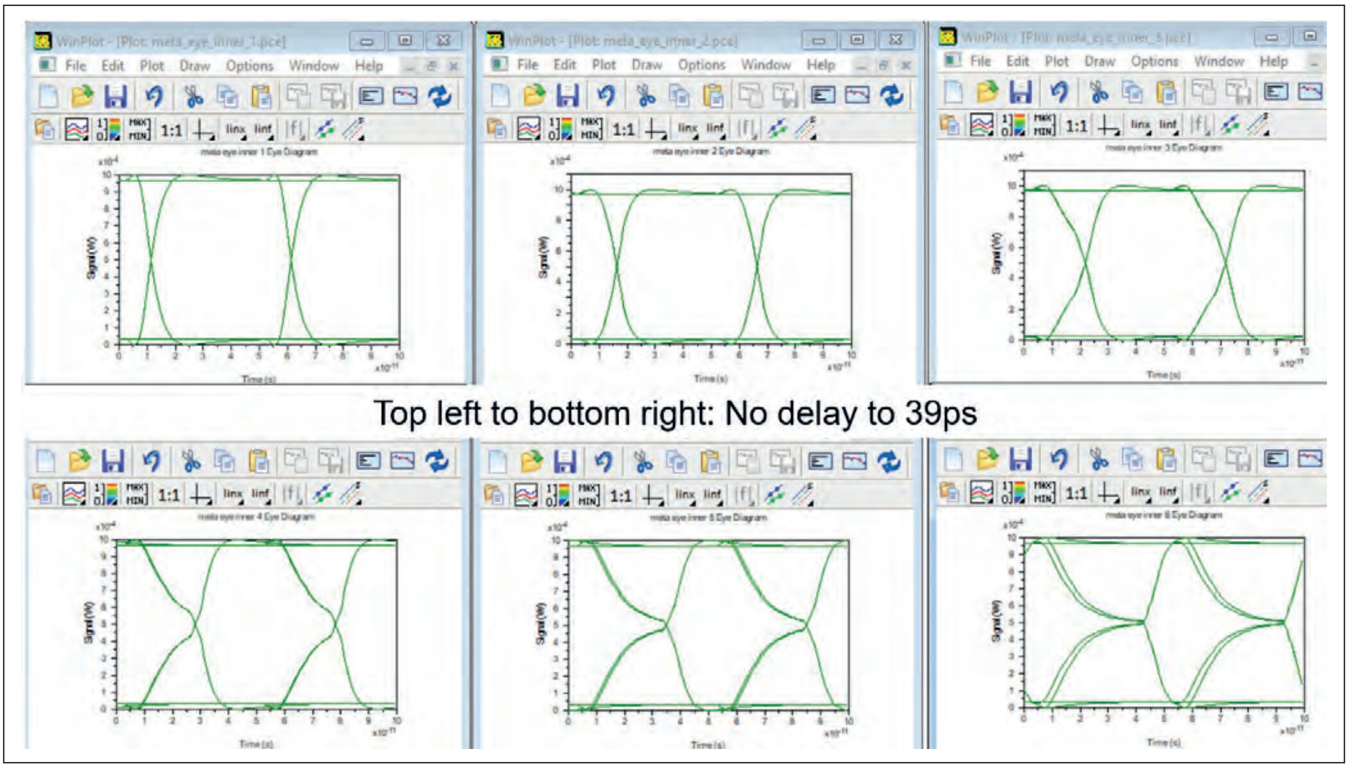
bandwidth. OptSim is an excellent platform for Monte Carlo analyses to achieve design for manufacturing (DFM) [9].

In this section, we study the impact of inter-segment deviations in a PAM-2 transmitter using an SE-MZM made from discrete PIC elements in OptSim Circuit. The schematic is shown in Figure 4. The topology comprises bidirectional PIC elements such as optical splitter 1x2 and combiner 2x1 with user-defined power ratio, and pairs of traveling-wave optical phase shifters.

The phase shifters are used to implement the segmented MZM. OptSim Circuit's bidirectional waveguide model connects phase shifters and implements deviations in separations between the segmented electrodes. A parameter scan is set for distances between the electrode segments.

The bandwidth narrowing due to deviations in inter-electrode distances is obvious: the higher the deviation, the worse the eye opening.

In the next several sections, we extend this study to analyse performance with respect to the deviations in driver time-delay and response time, both of which have a direct impact on the performance of SE-MZM-based high-speed transmitter PIPIC.



Top left to bottom right: No delay to 39ps

Figure 7 shows PAM-2 modulated optical eye diagrams with different values of drive delays.

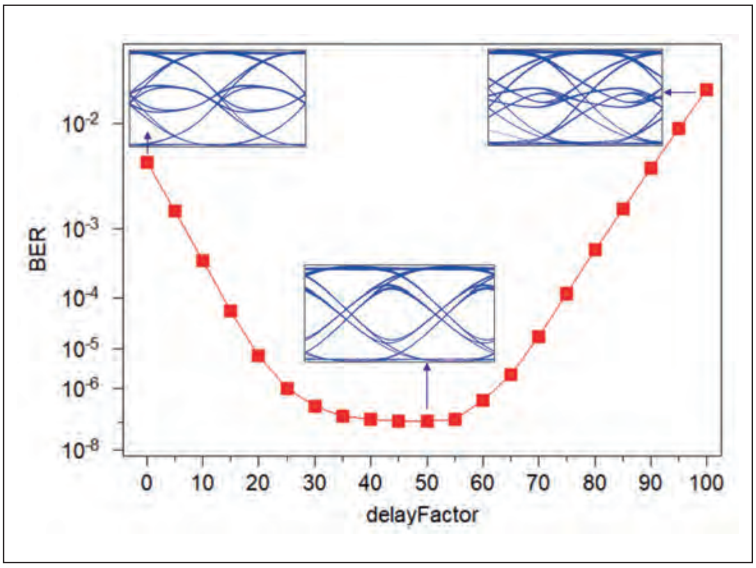


Figure 8: BER as a function of driving time delay

Impact of Driver Time-Delay Deviations

In the previous section, we studied the impact of deviations in the inter-electrode distances on the transmitter bandwidth. In SE-MZM transmitters, phase shifters are driven by electrical driving circuits. The manufacturing process variations and packaging constraints (such as different lengths of copper traces to electrical pads due to chip placement in a die) can result in electrical timing deviations in driving electrodes, thereby affecting mismatch in RF and optical group velocities and ultimately the bandwidth of the transmitter PIC.

In this section, we study the impact of driver time-delay deviations for an SE-MZM PAM-2 transmitter. The OptSim Circuit schematic is shown in Figure 6.

The topology comprises bidirectional PIC elements such as optical splitter 1x2 and combiner 2x1 with user-defined power ratio, and pairs of traveling-wave optical phase shifters. The phase shifters are used to implement the segmented MZM. OptSim Circuit's bidirectional waveguide model connects phase-shifters and implements separations between the segmented electrodes.

The electrical time delay block models driver timing delay deviations as integer multiples of sampling interval, which for the design under study is 0.78125ps corresponding to data rate of 20GBd/s sampled at 64 samples per symbol. The lower arm of the MZM uses a discrete 90-degree phase shifter model from OptSim Circuit to bias the MZM at quadrature.

The CW light is modulated by an electrical signal derived from PRBS data followed by an electrical driver. The inverter model provides push-pull electrical bias to one of the electrodes compared to the other. At the output of the SE-MZM PIC, an eye diagram analyser and a signal analyser are connected to observe transmitter outputs.

A back-to-back receiver at the SE-MZM PIC's output detects received signal, and the bit error rate (BER) tester is used to estimate driver timing-delay-induced penalties on the BER. A parameter scan is set for driving delays at segment electrodes as integer multiples of the sampling interval.

The resulting bandwidth penalties can also be visualized as back-to-back BER at the transmitter chip as shown in Figure 8. Optimal performance is achieved when optical and RF group velocities match.

The preceding study demonstrated the impact of timing delay deviations due to fabrication tolerances of electrical driver circuitry, as well as different electrode-to-pad RF trace lengths arising from the packaging constraints. This analysis helps designers find optimal trace-lengths to obtain performance within acceptable bounds. In the next section, we analyse PIC performance with respect to the deviation in electrode response time, which is an important design consideration in SE-MZM-based high-speed transmitter PIPIC.

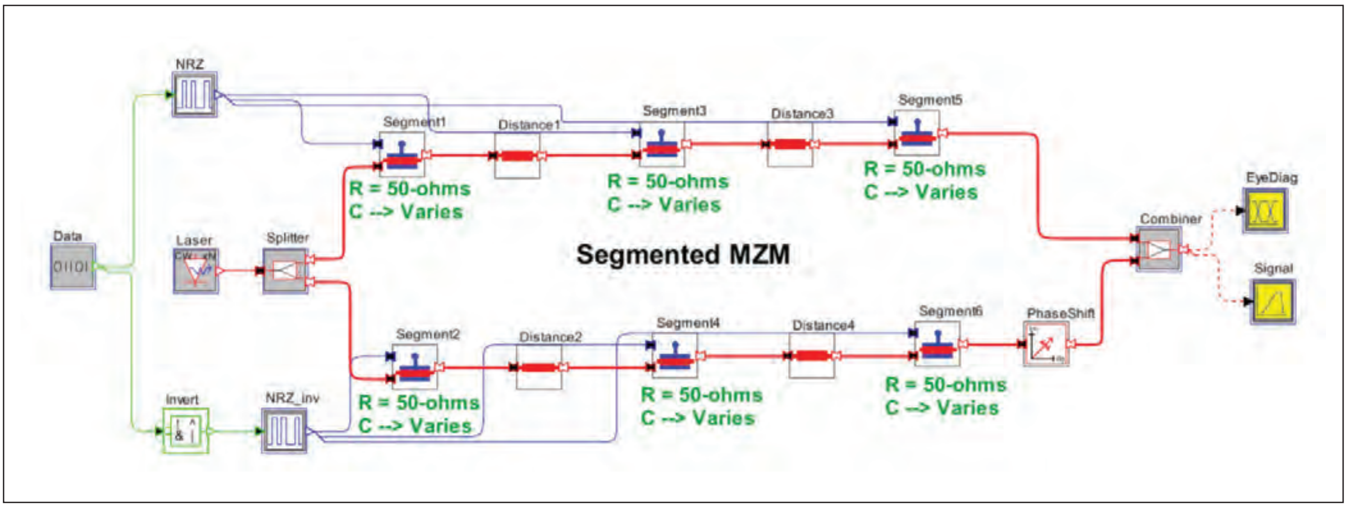
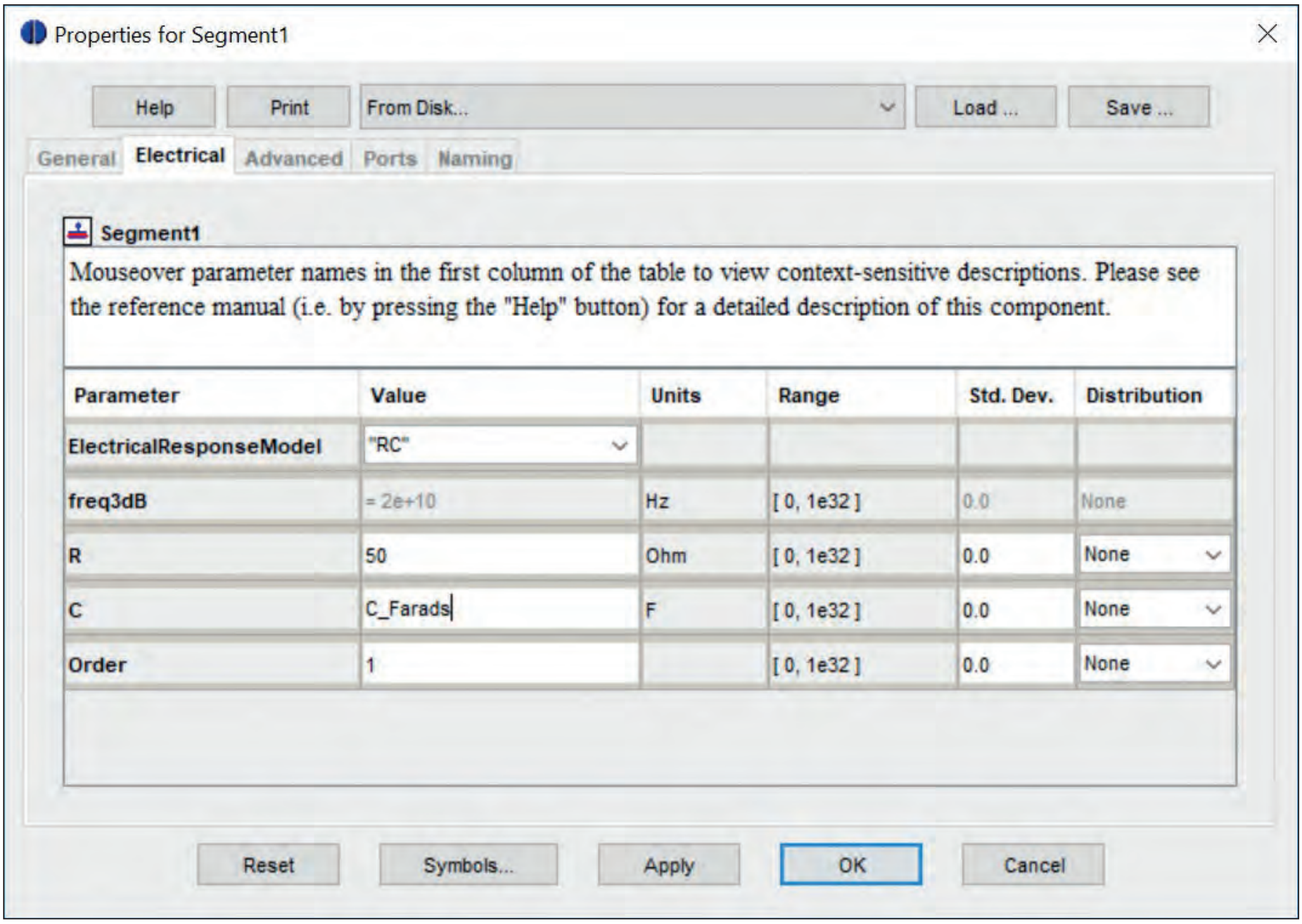


Figure 9: OptSim circuit scematic of a PAM-2 transmitter using SE-MZM



Segment1

Mouseover parameter names in the first column of the table to view context-sensitive descriptions. Please see the reference manual (i.e. by pressing the "Help" button) for a detailed description of this component.

Parameter	Value	Units	Range	Std. Dev.	Distribution
ElectricalResponseModel	"RC"				
freq3dB	= 2e+10	Hz	[0, 1e32]	0.0	None
R	50	Ohm	[0, 1e32]	0.0	None
C	C_Farads	F	[0, 1e32]	0.0	None
Order	1		[0, 1e32]	0.0	None

Figure 10: Choice of electrical response model via the parameter window of the phase shifter model

Impact of capacitive charge and R-C response times

Previously, we studied the impact of deviations in the inter-electrode distances and driver circuit's time variations on the bandwidth of an SE-MZM transmitter. In SE-MZMs, the R-C time response of phase shifter electrodes directly impacts bandwidth of the transmitter PIC.

The junction capacitance of the *p-n* diode and parasitiPIC from packaging both contribute to the capacitive charge and R-C time limitations in a phase shifter. In our study, we lump both effects into the overall R-C response time of the phase shifter. The schematic is shown in Figure 9. The topology comprises bidirectional PIC elements such as optical splitter 1x2 and combiner 2x1 with user-defined power ratio, and pairs of traveling-wave optical phase shifters. As shown in Figure 10, the electrical response model of the phase shifter is set to "RC."

A parameter scan is set for capacitance to model different amounts of capacitive charge and R-C times. Figure 11 shows PAM-2 modulated optical eye

Previously, we studied the impact of deviations in the inter-electrode distances and driver circuit's time variations on the bandwidth of an SE-MZM transmitter. In SE-MZMs, the R-C time response of phase shifter electrodes directly impacts bandwidth of the transmitter PIC

> We designed a PAM-4 transmitter for data centre interconnect applications in OptSim Circuit and analysed impairments due to deviations in some of the key design parameters arising from packaging, technology, and manufacturing process variations. OptSim Circuit, an advanced photonic circuit simulation tool, is part of the SYNOPSYS PIC Design Suite

diagrams with different values of R-C response.

The effect of R-C time variations due to the capacitive charging at the p-n junction and the packaging parasitiPIC can be seen in Figure 11. As expected, a higher response time adversely affects modulation speed.

Summary

This paper presents design considerations for SE-MZM based transmitters commonly used for DAC-less, multi-level optical modulation formats.
We designed a PAM-4 transmitter for data centre interconnect applications in OptSim Circuit and analysed impairments due to deviations in some of the key design parameters arising from packaging, technology, and manufacturing process variations.
OptSim Circuit, an advanced photonic circuit simulation tool, is part of the SYNOPSYS PIC Design Suite. The PIC Design Suite offers photonic-aware physical layout capabilities enabled by support for foundry-specific PDKs. [10]

Contact us at:
photoniPIC@SYNOPSYS.com to request more information and a 30-day evaluation of our software solutions.

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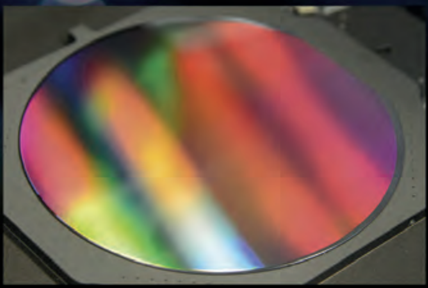

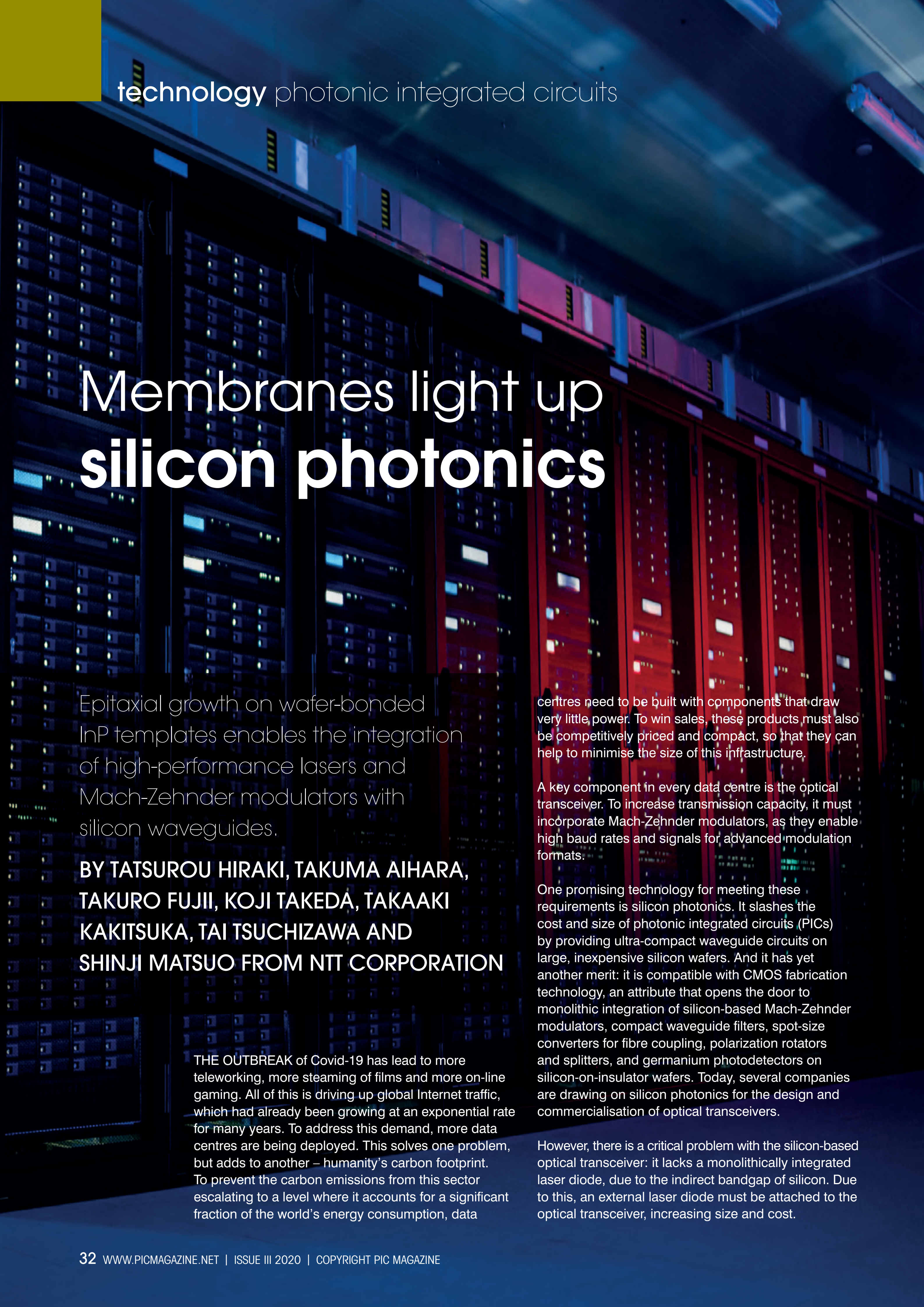

Membranes light up **silicon photonics**

Epitaxial growth on wafer-bonded InP templates enables the integration of high-performance lasers and Mach-Zehnder modulators with silicon waveguides.

BY TATSUROU HIRAKI, TAKUMA AIHARA, TAKURO FUJII, KOJI TAKEDA, TAKAAKI KAKITSUKA, TAI TSUCHIZAWA AND SHINJI MATSUO FROM NTT CORPORATION

THE OUTBREAK of Covid-19 has lead to more teleworking, more steaming of films and more on-line gaming. All of this is driving up global Internet traffic, which had already been growing at an exponential rate for many years. To address this demand, more data centres are being deployed. This solves one problem, but adds to another – humanity's carbon footprint. To prevent the carbon emissions from this sector escalating to a level where it accounts for a significant fraction of the world's energy consumption, data centres need to be built with components that draw very little power. To win sales, these products must also be competitively priced and compact, so that they can help to minimise the size of this infrastructure.

A key component in every data centre is the optical transceiver. To increase transmission capacity, it must incorporate Mach-Zehnder modulators, as they enable high baud rates and signals for advanced modulation formats.

One promising technology for meeting these requirements is silicon photonics. It slashes the cost and size of photonic integrated circuits (PICs) by providing ultra-compact waveguide circuits on large, inexpensive silicon wafers. And it has yet another merit: it is compatible with CMOS fabrication technology, an attribute that opens the door to monolithic integration of silicon-based Mach-Zehnder modulators, compact waveguide filters, spot-size converters for fibre coupling, polarization rotators and splitters, and germanium photodetectors on silicon-on-insulator wafers. Today, several companies are drawing on silicon photonics for the design and commercialisation of optical transceivers.

However, there is a critical problem with the silicon-based optical transceiver: it lacks a monolithically integrated laser diode, due to the indirect bandgap of silicon. Due to this, an external laser diode must be attached to the optical transceiver, increasing size and cost.

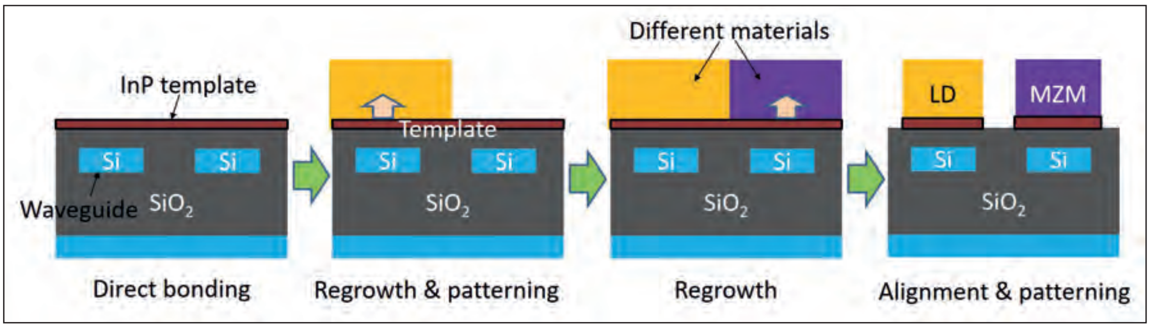

Figure 1. Procedure for integrating III-V semiconductor devices with different bandgaps by direct bonding and epitaxial growth.

There is also another issue with the silicon-based Mach-Zehnder modulator. It has a poor modulation efficiency, because silicon is only able to exploit the inefficient carrier-plasma effect. For this class of modulator, a key figure of merit, known as the half-wave-voltage-length product ($V_\pi L$), is typically larger than 1 V cm. This high value hampers efforts to trim the size and the power consumption of silicon-based optical transceivers.

An attractive solution to these issues is to heterogeneously integrate III-V semiconductors on a silicon platform. A good choice for this is the InP-based family of materials, which is an established, mature technology for making lasers for telecommunication applications. Another attribute of InP-based materials is that they have a much larger refractive-index change than silicon, thanks to their strong carrier-plasma, band-filling, and Franz-Keldysh effects. These phenomena assist the fabrication of high-efficiency phase shifters for Mach-Zehnder modulators with a small $V_\pi L$.

To produce transceivers with this technology requires the integration of laser diodes and Mach-Zehnder modulators with a silicon platform. One way to do this is to bond different devices to a silicon waveguide circuit. With this approach, the laser diode and Mach-Zehnder modulators are fabricated on different III-V semiconductor wafers, before each is bonded to a silicon waveguide circuit, using precise alignment. A downside of this approach is that it is challenging to realise the high throughput needed to integrate a large number of components. Alternatively, monolithic integration can be realised through epitaxial growth of different III-Vs on silicon. This has the potential to provide low-cost, wafer-level integration, as lithography techniques allow patterning and aligning of all devices. But success is not assured, because it is difficult to obtain high-quality layers of crystalline III-Vs, due to their lattice mismatch with silicon. So, whatever approach is adopted, it is far from easy to integrate simultaneously laser diodes and Mach-Zehnder III-V modulators on a silicon platform.

A hybrid solution

At the NTT Device Technology Labs in Kanagawa, Japan, our team is developing a novel fabrication method that addresses these issues. Our technology combines direct bonding and epitaxial growth to integrate various III-V devices with different bandgaps on silicon waveguide circuits (see Figure 1).

Fabrication begins by bonding a III-V template to a SOI wafer, and then re-growing different materials on the lattice-matched template, which could be a thin film of InP on SiO_2/silicon. Our next step is to use lithographic processes to align and pattern all the III-V devices on the silicon waveguide circuits. With this approach, as well as using epitaxial growth on the lattice-matched template, we can integrate a variety of high-quality materials with different bandgaps. It is this high degree of flexibility that allows us to integrate many high-performance III-V devices.

When applying this technique, we had to consider the critical thickness of the epitaxial layers on the bonded template. This thickness is determined by the difference between the thermal expansion coefficient of the bonded III-V layer and the silicon substrate. For example, for the epitaxial growth of an InP layer on a silicon substrate at 600 °C, the critical thickness is 430 nm. That is concerning, since the typical thickness of both a conventional semiconductor laser diode and a Mach-Zehnder III-V modulator are 2 μm to 3 μm. As these devices are much thicker than the critical thickness, it makes it very difficult to integrate conventional III-V semiconductor devices on a silicon

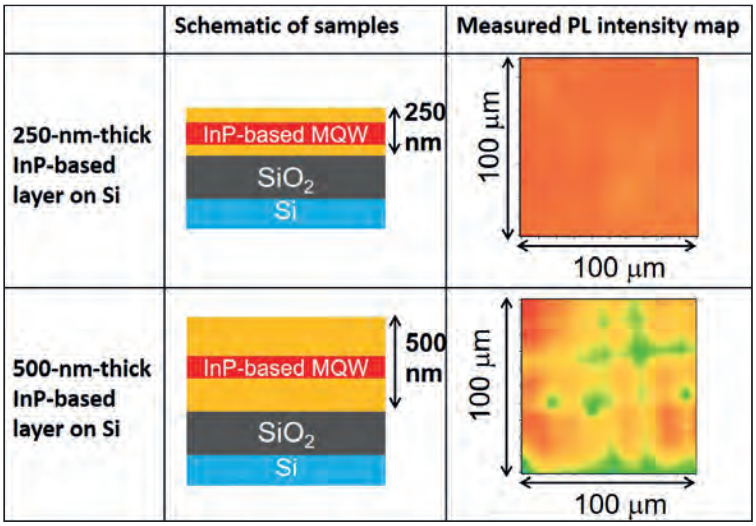

Figure 2. Measured photoluminescence intensity distributions of InP-based layers bonded onto SiO_2/silicon substrates and annealed at 610 °C for 30 minutes.

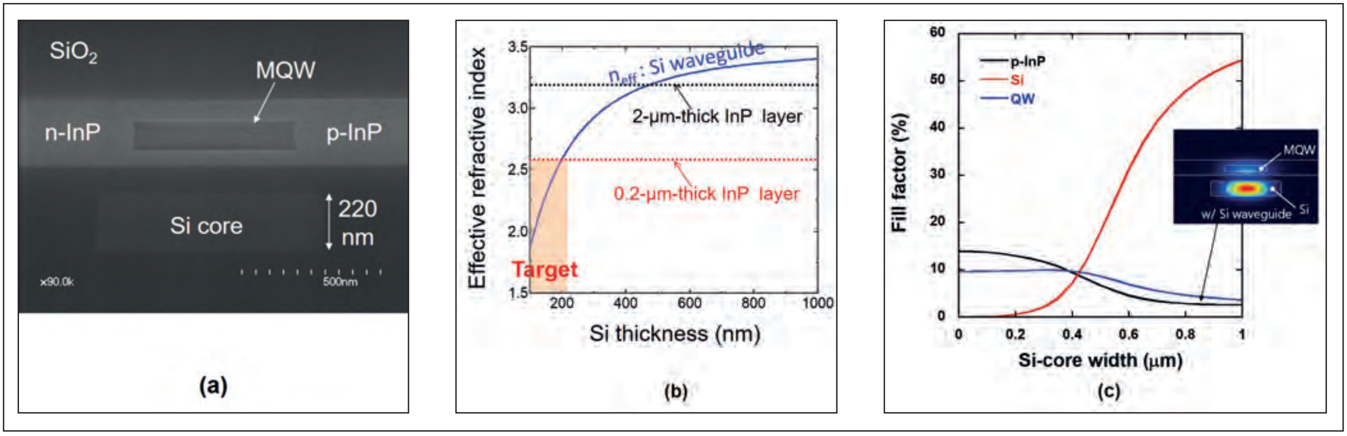

Figure 3. (a) Cross-sectional, scanning-electron microscopy of a membrane laser diode. (b) Calculated effective refractive index of silicon waveguides and InP layers. (c) Calculated fill factors in the multi-quantum well, *p*-type InP, and silicon cores. The area of the multi-quantum well core is set to 0.6 x 0.1 μm^2.

platform with an epitaxial growth process.

Membrane devices

Our solution is to trim the thickness of the III-V layers, as this reduce thermal strain during the epitaxial growth process. The success of this approach is illustrated in measurements of photoluminescence intensity (see Figure 2). They reveal that there is very little strain in the InP-based layers that are bonded to SiO_2/silicon substrates, prior to annealing for 30 minutes in an MOCVD chamber, using the following conditions: 610°C, a PH_3 atmosphere and a pressure of 30 Torr. While photoluminescence measurements on structures with 500 nm-thick InP-based layers that include 150 nm-thick multi-quantum-well layers have dark lines, due to exceeding the critical thickness, those that are 250 nm-thick and feature an identical active region are free from degradation, due to the lower thermal strain. These results highlight the necessity of using a membrane structure for epitaxial growth on the silicon substrate.

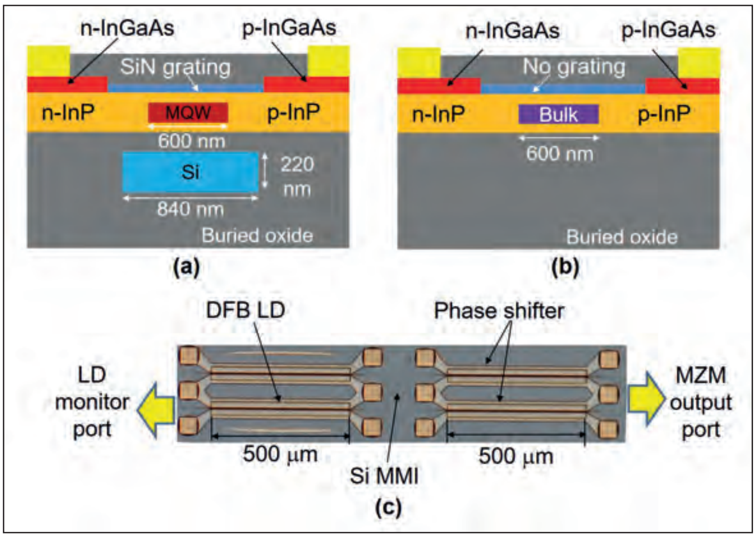

Figure 4. Cross sections of (a) laser diode and (b) phase shifter. (c) Microscopy image of a fabricated laser diode and Mach-Zehnder modulator device.

Based on these findings, we have developed membrane buried-heterostructure lateral *p-i-n* and *p-n* diodes for lasers, optical amplifiers, and Mach-Zehnder modulators on a silicon platform. Note that the buried heterostructure is a valuable feature, enabling efficient confinement of both carriers and photons. To integrate the various lateral diode devices, we use silicon ion implantation and zinc thermal diffusion processes to form the donor and acceptor regions, respectively. Using these techniques, we define donor and acceptor regions with photolithography processes, and thus obtain different carrier profiles for the laser diode and the Mach-Zehnder modulator. This is critical to integrating laser diodes and Mach-Zehnder modulators on a silicon platform.

Using this method, we have fabricated a lateral-current-injection *p-i-n* diode for the laser diode (see Figure 3(a)). At its heart is a multi-quantum-well core, buried in the 230 nm-thick InP layer and precisely aligned to the silicon waveguide core. This membrane buried heterostructure overcomes another issue facing typical InP-based vertical diodes on a silicon platform – it provides effective refractive-index matching between the III-V and silicon layers.

For optical coupling between the InP and silicon layer, calculations indicate that a typical vertical diode requires a silicon-waveguide layer with a thickness between 400 nm and 500 nm. However, the silicon waveguides widely developed for low-loss and compact channel-waveguide circuits have a thickness of only 220 nm (see Figure 3(b)). In other words, a typical vertical InP-based device is not compatible with these thin silicon waveguide circuits. Fortunately, that's not the case for our membrane InP-based layer, which is much thinner than the conventional 2 μm-thick InP layer, and comparable to that of the widely used 220 nm-thick silicon waveguide layers. This means that thanks to effective index matching, it is easy to couple our InP-based membrane devices to mature silicon waveguide circuits.

Efficient optical coupling between the multi-quantum well core and low-loss silicon waveguide holds the key to reducing the internal optical loss of the laser diode. Calculations of fill factors in the multi-quantum well core, *p*-type InP, and silicon cores indicate that thanks to index matching, we can control the fill factors by changing the width of the silicon core (see Figure 3(c)). As a result, overlap with the large-loss, *p*-type InP region can be reduced by increasing the overlap with the low-loss 220 nm-thick silicon core. Making good use of this, we set the silicon core width to 840 nm to provide a fill factor of around 4 percent in the multi-quantum well. We can change the fill factors of our membrane structure while maintaining the small multi-quantum-well area, enabling us to reduce the threshold current. The upshot of all of this flexibility is that by using the membrane structure, we can obtain high-performance laser diodes on widely developed, 220 nm-thick silicon waveguide circuits.

Integrating laser diodes and modulators

Drawing on the insights provided by our calculations, we have integrated a membrane laser diode with an InP-based Mach-Zehnder modulator on a silicon platform (cross-sections of our membrane laser diode and phase shifter for the Mach-Zehnder modulator are shown in Figures 4(a) and 4(b), respectively). For this particular design, we use a 500 μm-long distributed-feedback laser with a SiN grating on the top of the InP layer. To ensure operation in the C-band, we set the photoluminescence peak wavelengths for the multi-quantum-well core of the laser diode to 1.52 μm, and that for the *n*-type InGaAsP-bulk core of the phase shifter to 1.3 μm. As both the laser diode and phase shifter are formed in 230 nm-thick InP-based layers, they can be integrated using the epitaxial growth process on a silicon platform.

We designed the phase shifter for a high-efficiency, carrier-depletion, Mach-Zehnder modulator. As shown in Figure 4(b), the buried InGaAsP-bulk core of the phase shifter does not couple to the silicon waveguide. With this design, there is a large fill factor of around 30 percent in the *n*-type InGaAsP core – it exceeds the values associated with conventional III-V semiconductor phase shifters with thicknesses of 1 μm to 2 μm. By applying reverse bias to the *n*-type InGaAsP core, we can efficiently modulate the optical phase using a combination of the carrier-plasma effect, the band-filling effect, and the Franz-Keldysh effect. This type of membrane phase shifter has a typical $V_\pi L$ of around 0.4 V cm, a figure far lower than that for a typical silicon carrier-depletion Mach-Zehnder modulator, which has a $V_\pi L$ higher than 1 V cm. Another attribute of the membrane structure is its low capacitance, which is useful for reducing the capacitance-resistance time constant of the phase shifter.

Building on this success we have united components, with a 500 μm-long DFB laser diode integrated on the silicon waveguide and connected to the Mach-Zehnder modulator (see the microscopy image, shown in Figure 4(c)). The modulator has silicon multimode interferometers and 500 μm-long membrane phase shifters. At the chip facet there is a silica-based (SiO_x) core with an area of 3 x 3 μm², designed for low-loss fibre coupling. The role of the narrow inverse silicon taper is to convert the optical mode field diameter from the nanowire silicon waveguide to the SiO_x waveguide. The SiO_x core provides easy butt-coupling to the optical fibre, realising low loss and low reflection.

Our narrow inverse InP tapers are designed to transfer the optical mode fields between the laser diode or phase shifter and the single-mode silicon waveguide. The inverse taper, 50 μm in length and with a cross-sectional area of 0.1 x 0.23 μm², launches light into the single-mode silicon waveguide that has a cross-sectional area of 0.44 x 0.22 μm². As the aspect ratio of the taper tip is much lower than that of conventional InP devices, it is relatively easy to fabricate this narrow membrane taper using a mature process. Using this mode converter, we integrate the membrane laser diode and phase shifters with silicon waveguides, realised with low loss and low reflection.

> Efficient optical coupling between the multi-quantum well core and low-loss silicon waveguide holds the key to reducing the internal optical loss of the laser diode

To realise wafer-level integration of both laser diodes and Mach-Zehnder modulators on a silicon platform, we pattern silicon waveguides on a SOI wafer, before burying them in a SiO_2 cladding film. Chemical-mechanical polishing of this cladding flattens its surface and reduces its thickness on the silicon waveguide to 100 nm. After this, we remove the InP substrate. The whole multi-quantum well layer is taken away, except for the laser diode region, to leave a 50 nm-thick InP template on the entire wafer. An *n*-type InGaAsP-bulk layer is then regrown for the phase shifter, before the cores for the laser diode and phase shifter are patterned by lithography. The next steps are: the re-growth of an InP layer to form a buried heterostructure; re-growth of an InGaAs contact layer; and patterning donor and acceptor regions by lithography, followed by their formation with silicon ion implantation and zinc thermal diffusion. The latter step enables us to obtain different carrier profiles for the laser diode and phase shifter on the entire wafer. Completion of the fabrication process involves patterning the InGaAs contact layer and InP mesa and tapers, before turning to a backend process, used to

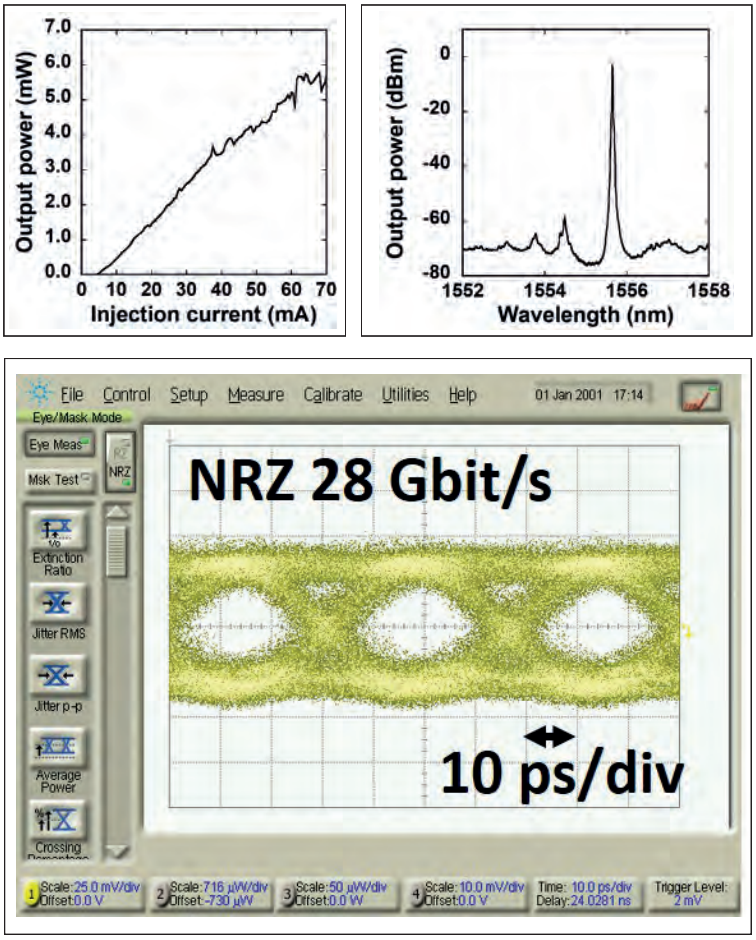

Figure 5. (a) Measured light-output curve from the laser diode port of the laser. The chip facet faced air in this experiment, creating a power fluctuation, due to optical reflection at the facet. (b) Measured output spectrum from the modulator, using a laser diode current of 50 mA and a Mach-Zehnder modulator DC voltage of 4.5 V. A refractive-index-matching oil is inserted between the high-numerical-aperture fibre and the silica core to reduce the reflection at the chip facet. (c) Measured eye diagram for NRZ 28 Gbit/s signal.

add electrodes and produce a large silica-based core for fibre coupling. By forming the large silica core at a temperature below 200 °C, we avoid damage to the III-V devices.

Proven success

Measurements of output power from the laser diode port, made with a photodetector directly facing a chip facet that detects the total output power coming from it, reveal that the threshold current is only 4.5 mA (see Figure 5(a)). This low value, given the 500 µm active length of the laser diode, is attributed to the small active area. Increasing the injection current to 70 mA propels the output power to around 5.5 mW. This figure indicates that we prevented fatal damage to the active layer during the regrowth processes, and highlights that the membrane InP-based layer is beneficial for reducing thermal strain during the epitaxial growth process.

To evaluate the output power from the Mach-Zehnder modulator's output port, we aligned a high-numerical-aperture fibre with the silica core at the chip facet. The fibre-coupled output power hits 2.9 mW when driving the laser diode at 70 mA, with tuning of the DC bias of the phase shifter maximising the output power from the measured port. We attribute this high output power to efficient light emission from the membrane laser and to low losses of the Mach-Zehnder modulator and spot-size converter.

Additional measurements reveal that the half-wave voltage (V_π) of the Mach-Zehnder modulator is around 7.5 V. It follows that $V_\pi L$ is around 0.4 V cm, a value more than three times smaller than that of a typical silicon carrier-depletion Mach-Zehnder modulator. These results show that we have succeeded in integrating a high-efficiency InP-based Mach-Zehnder modulator on a silicon platform.

We have also demonstrated dynamic modulation of our laser diode and Mach-Zehnder modulator integrated device. Using a DC bias of 4.5 V for the Mach-Zehnder modulator, to ensure modulation of non-return-to-zero signals, we have investigated the output spectrum at different drive currents for the laser diode. These measurements, made without an RF input to the phase shifter, show single-mode lasing with a side-mode suppression ratio of around 55 dB, for a drive current of 50 mA (see Figure 5(b)).

To evaluate the modulation capability of our design, we have applied RF input signals from a pulse pattern generator to one of the phase shifters in the Mach-Zehnder modulator. This produced a clear eye opening using the following conditions: a laser diode current of 42 mA; a non-return-to-zero 28-Gbit/s signal; without 50 Ω termination at the Mach-Zehnder modulator.

Our next goal is to use our technology to integrate narrow-linewidth laser diodes and in-phase and quadrature modulators for optical transceivers in telecommunication systems. Further ahead, the uses of our platform will expand, as it is not limited to integrating laser diodes and Mach-Zehnder modulators, but can be used to construct other III-V devices with different bandgaps on a silicon platform. This virtue makes our technology ideal for constructing low-cost, large-scale, high-performance PICs with high functionality for various applications.

Further reading

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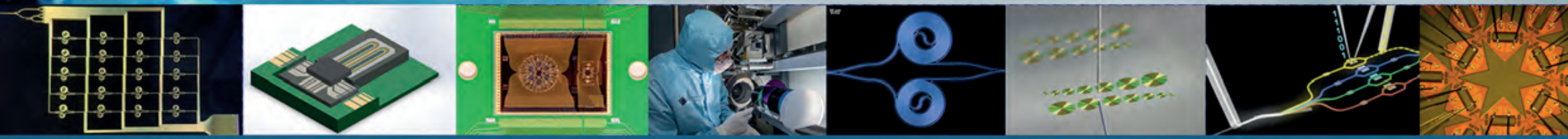

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Indispensable indium

From flat panel displays to semiconductor wafers, the use of indium in electronics continues to grow.

BY ROBERT PLOESSL, INDIUM CORPORATION

THE ELEMENT with atomic number 49 – indium – is central to modern life. Just consider a typical day: often we will spend hours staring at a flat panel display containing hundreds of thousands of pixels, each turned on and off by thin-film transistors and illuminated by some form of LED. While these transistors and LEDs might contain indium, there is no doubt that this element is encountered by the light traversing the display stack, as it will pass through indium-tin oxide (ITO) electrodes. This oxide combines transparency with conductivity, making it a great material for the display industry. In some of the latest high-colour-gamut TVs, indium crops up again, appearing in the display's InP quantum dot layer of the colour filter that yields brilliant reds and greens. This makes five potential encounters between photons and indium-based materials before the light hits our retina. And there may be even more. If we watch content stored remotely, such as streaming video, it will reach us through a network of optical fibres, transmitting infrared light generated by an InP-based laser.

For those of us that are reading this on an electronic screen, the chances are that most of the above applies – there is no doubt that indium seems to be everywhere. Yet, despite its ubiquity, the economics of indium are poorly understood. That's because most of the building blocks of modern technology emerge from supply chains that are rarely discussed, even in the technical press. To put it frankly, most of us don't have much of a clue where indium comes from.

Let's go back to the beginning. Like all heavy elements, indium was created during supernovas as planets condensed and formed. Due to its geochemical properties, indium appears in sphalerite, the most common ore of zinc, where its concentration can be as high as 100 parts per million. Another common carrier element for indium is lead. Deposits containing relatively high concentrations of indium are found all over the world. According to an exhaustive survey detailed by Ulrich Schwarz-Schampera and Peter Hertzig in *Indium: Geology, Mineralogy, and Economics*, a large number of indium-bearing deposits have been found around the Pacific Rim and in many other sites in Europe, Africa, and central Asia.

It comes as a shock to many, including quite a few working within the semiconductor industry that there

One of the first successful applications of indium began in the 1940s when engineers diffused this metal into the surface layer of the bearings in aircraft engine pistons. Indium provided lubrication on the atomic scale, reducing wear and tear on the engine and increasing fuel efficiency – a prime example of our strongly held belief at Indium Corporation that materials science changes the world.

are no indium mines anywhere. Element 49 is almost always co-mined with zinc. That's not actually too surprising, as there are only a few carrier elements that have their own corresponding production infrastructure, such as copper, iron, and aluminium. When demand swings for most co-mined elements, such as indium, supply at the carrier infrastructure is often relatively inelastic. The real supply for indium is actually set downstream from the mines at the refiners where material is processed to produce an indium content up to 4N (99.99 percent). Indium ore is found all over the globe but refiners are heavily concentrated in China.

The overall global abundance of indium is in the range of 5-7 parts per million. That may not seem like a lot, but it is almost exactly the same value as that for silver. However, unlike that precious metal, which has been in use since ancient times, indium only started its commercial life in the twentieth century and was initially explored for its mechanical properties. One of the first successful applications of indium began in the 1940s when engineers diffused this metal into the surface layer of the bearings in aircraft engine pistons. Indium provided lubrication on the atomic scale, reducing wear and tear on the engine and increasing fuel efficiency – a prime example of our strongly held belief at Indium Corporation that materials science changes the world.

Fast forward to the age of electronics and high-speed communication when InP semiconductor crystals came to the fore, thanks to a bandgap that matches the transmission window of optical fibre. With a light source and a lossless technology for transmitting information, the groundwork was laid for the Internet and the connection of computers. It is a success story that we all know.

The InP-based lasers in optical networks are built on wafers sliced from monocrystalline boules, which are grown using techniques such as vertical freeze gradient and the Czochralski method – both requiring high-purity indium ingots as the starting ingredient. It is not sufficient to use standard commercial indium metal, which has a purity that starts at a 4N. That purity is suitable for making inorganic compounds and ITO sputter targets, but is not nearly enough for the production of compound semiconductors, which require a purity at least 500 times higher, typically 6N5. Indium with purity this high is produced in a cleanroom-like environment using a proprietary manufacturing process. The metal is cast into moulds with a wide variety of shapes and sizes. Ingots can be long cylinders, small 50-gram blocks or large rectangular shapes – anything that aids the downstream process for customers. It is critical to reduce trace elements, as they threaten to form energy states in the band gap of the InP semiconductor that degrade electronic and optical properties. Unwanted consequences of undesirable states include a lowering of electron mobility, a decrease in photoluminescence efficiency, and the creation of carrier recombination pathways.

What happens to the InP crystals and wafers that are left over from their respective manufacturing process? What about the sustainability of the indium value chain?

From the start, the ITO and flat panel display industry have been reclaiming indium and the compound semiconductor industry is now following suit. This is

Indium phosphide crystal pieces from wafer boule manufacturing – the raw material for reclaiming indium from InP.

to be expected, as every mature, high-value-added materials-using industry should have a recycling loop for its valuable input materials. At Indium Corporation we have added this reclaim capability, initially for InP crystals and wafers, and we plan to add capabilities for InSb in the near future.

There is no doubt that it makes sense to do this at the industrial level with end-of-life wafers and unused crystal material. It is harder to accomplish this with packaged electronic InP devices or end-of-life consumer products – this probably explains why we are not aware of any companies doing so. However, if our society is to be a responsible steward of our planet, this is an important objective.

Polycrystalline InP wafers form part of the input stream for indium reclaim.

As of today, we are concentrating on output from crystal growers, InP wafer makers, and output from fab and epi-wafer fabs. If you are using InP wafers in a fab and have any recycling needs, we certainly would like to hear from you.

So, what does the InP-consuming industry landscape currently look like and how has it evolved? 25 years ago, this magazine reported that global InP wafer consumption totalled 58,000 wafers, equating to a surface area of 183,000-square inches. Back then, Japan led the world and was responsible for 56 percent of wafer consumption. Today, according to a recent report from SEMI, 64 fabs are capable of processing InP wafers – 40 percent are found in North America, 31 percent in Europe, and the balance in Asia. This report claims that the capacity figure of all these InP fabs, based on 200 mm equivalent wafers, totals 667,000. That's a figure that equates to just over 11 times that of global consumption in 1995. So, it is clear that there has been an astonishing growth of InP, even with the caveat that the SEMI figures are capacities, rather than actual output. They are total fab capacities; that is, the InP output is in the mix but not the total number.

Up until now, we haven't discussed other semiconductor wafers that incorporate indium – InSb and InAs. Due to their narrow bandgaps, these wafers are used primarily for the manufacture of infrared sensors and detectors. Reliable market figures are sparse. However, this could change very soon with the adoption of gas sensors and infrared imaging devices in, for example, the automotive sector.

Another use of indium is, of course, in indium-containing epilayers. They are grown epitaxially, often by MOCVD, using the metal-organic trimethyl-indium. This source is made from high-purity indium trichloride, available as an anhydrous salt. The density of this salt may be tailored to the process of our customers.

When engineers use trimethyl-indium to grow heterostructures by MOCVD, they control the flow of this source of indium. With this lever, they tune the band structure and shift the emission or absorption wavelength of a device. An exciting new development over the last few years is the development of hybrid integration, a technology that allows compound semiconductor layers to be constructed directly on a silicon substrate.

As this technology is still in its infancy, outside the display market the growth of indium consumption is largely driven by data centres. They are the workhorses for the cloud, which has become both the storage and the processor of internet core computing. The cloud holds messages, photos, videos; it hosts entire web sites; and it runs software algorithms like machine learning. And if you are reading this online, the article will be stored there and brought to you via InP lasers to a screen coated in ITO, probably backlit with InGaN-based LEDs.

Further reading

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Achieve seamless integration of photonic circuit simulation and layout design

VPIphotonics and Luceda Photonics have combined their considerable design software expertise to offer the integrated photonics industry a powerful suite of tools created around the idea of speeding the design process while enabling the simulation of a new circuit's performance in real-world conditions. PIC Magazine asked the two companies to explore the advantages of their combined resources created to support key PIC technologies.

BY EUGENE SOKOLOV, SENIOR APPLICATIONS ENGINEER, VPIPHOTONICS;
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VPIPHOTONICS and Luceda Photonics are leading suppliers of design software for the integrated photonics industry. Following the needs of design teams they have combined both a system and layout driven design flow to assure that any layout changes are reflected in simulations and vice-versa.

This approach began several years ago when the companies began aligning common foundry-validated Process Design Kits (PDKs) for their design tools. Designers benefit from a process flow that starts from a graphical photonic integrated circuit (PIC) design and system simulation environment, which seamlessly couples to Python scripted layout and design capabilities for tape-out. Supporting this process, the companies distribute building block (BB) libraries for foundry-specific PDKs that contain validated circuit simulation models linked to corresponding layout data. With PDKs from LIGENTEC, SMART Photonics and, recently, Fraunhofer HHI, both Silicon Photonics (SiP) and Indium Phosphide (InP) based fabrication technologies are covered.

The Platforms

Luceda's IPKISS Design Platform combines circuit level design and simulation, layout and device CAD all based on Python scripting. Luceda also allows designers to tape out to the foundries by means of foundry validated PDKs. Support of Python makes its usage accessible for customers and automatically gives access to the rich set of open-source libraries written in Python including those for scientific and technical computing.

VPIcomponentMaker Photonic Circuits is a professional simulation and design environment for large-scale photonic integrated circuits, which offers a mix of general-purpose photonic, electrical and optoelectronic device models. Dedicated VPItoolkit PDK extensions (for example, VPItoolkit PDK SMART or VPItoolkit PDK LIGENTEC), enable a layout-aware schematic-driven PIC design workflow and provide access to a broad set of available standard building blocks of the specific foundry PDK.

Features and Benefits

- Use VPIcomponentMaker Photonic Circuits and PDK extensions to design and simulate the PIC within a complete optical or opto-electrical system employing a library of active and passive PDK BBs with realistic foundry-specific simulation models.
- Seamlessly generate the Python based layout of a circuit within the IPKISS Design Platform using the foundry PDK and improve the yield and reliability of the PIC design flow.
- Combine graphical schematic capture and automated waveguide routing employing the layout-aware schematic-driven PIC design methodology [1, 2]. This approach is delivered by:
  - the seamless integration of circuit and layout tools via smart elastic optical connectors
  - the capability to specify exact physical locations and orientations of PDK BBs on the final layout while performing graphical schematic capture.

The circuit simulator invokes the layout design tool (automatically and invisibly for users) to determine the actual physical lengths and shapes of automatically routed elastic connectors. It also constructs compact simulation models for them, and after that the program initiates circuit simulations as schematically described in Fig. 1.

Refer to the application example in Fig. 2 to see how the port locations are specified and the elastic connectors are used on the schematic. Note that absolute, relative, and parameterized locations are supported.

- Sweep and optimize the values of one or more schematic parameters, including the parameters which affect the circuit layout, for achieving a desired circuit behavior.
- The list of PDK BBs can be extended by users with custom components not covered by the list of foundry-certified PDK BBs. Importantly, all such custom PDK BBs will support the layout-aware schematic-driven design capabilities and the export of their layout to Luceda’s IPKISS Design Platform (Fig. 3).
- Leverage support of multilevel hierarchical designs and reuse subcircuits (if desired) as compound BBs in other designs, thus conveniently handling design complexity of large-scale PICs.
- Quickly generate a GDS mask of the designed circuit directly from a customer’s circuit schematic view in VPIcomponentMaker Photonic Circuits via IPKISS, called in background. The GDS mask can be additionally opened and shown by other tools such as KLayout for immediate verification.
- Investigate and validate PIC functionality in the system application of interest employing the seamless interface with VPItransmissionMaker Optical Systems.

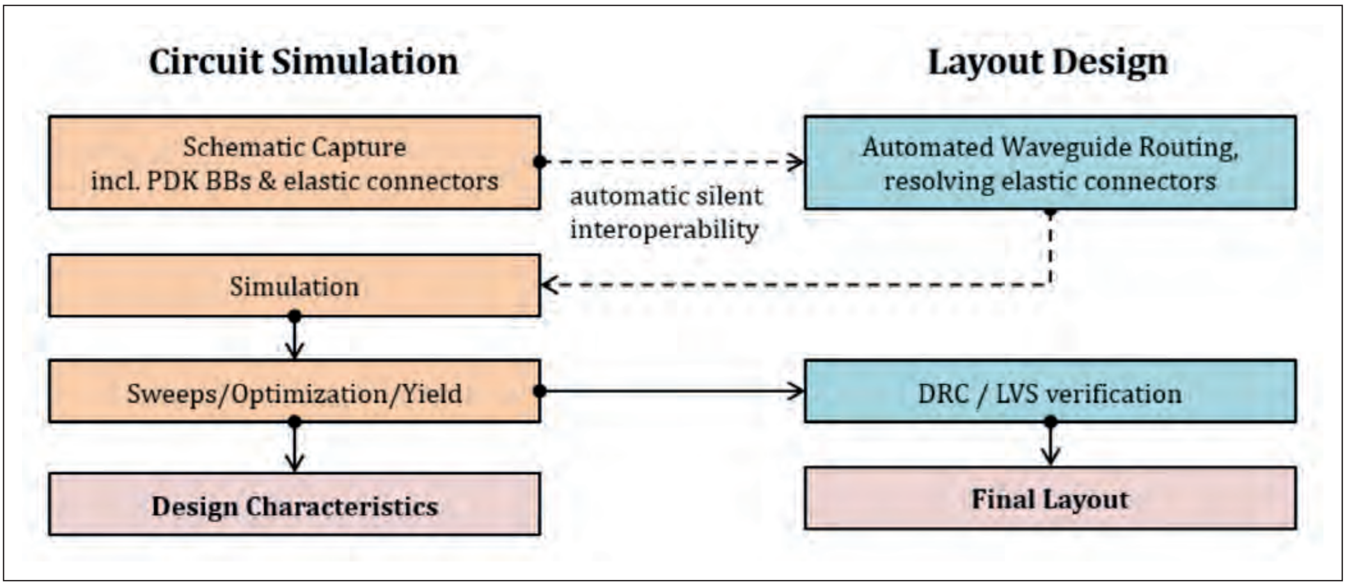


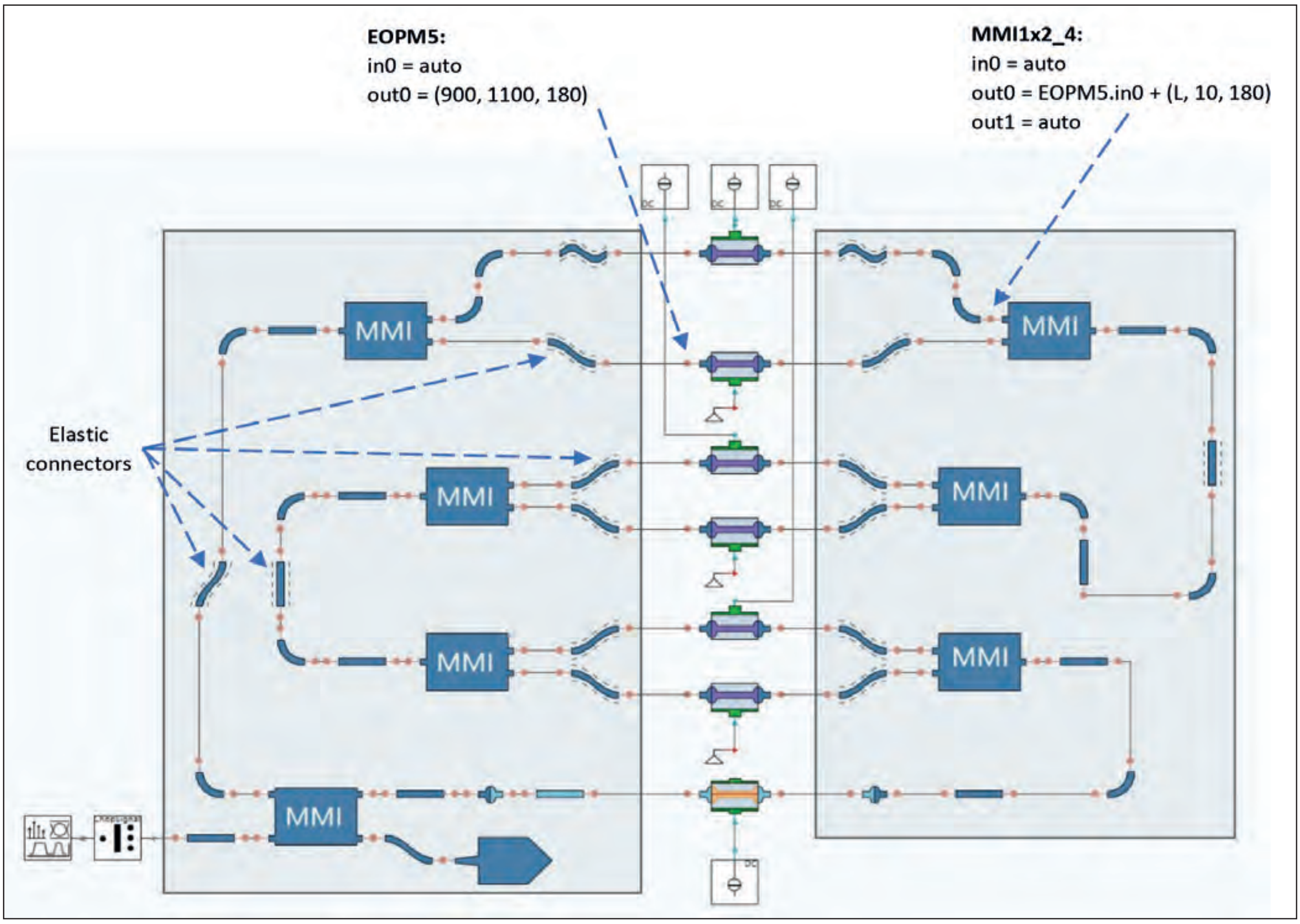
Figure 1. Sketch of layout-aware schematic-driven design methodology

Please refer to the design examples in Fig. 2 and 3, for which the schematic representation in VPIphotonics Design Suite, the corresponding layout in Luceda's IPKISS Design Platform and exemplary simulation results are shown.

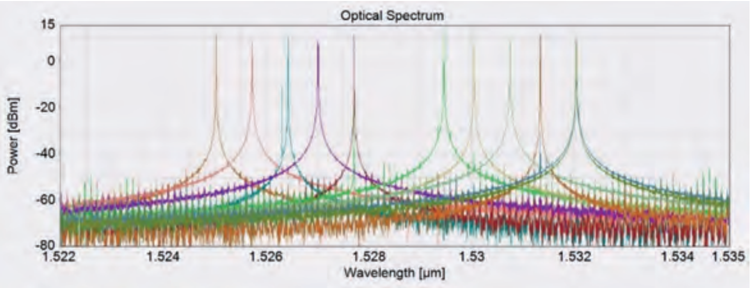
Design Examples using PDK Libraries

Widely Tunable Laser

Figure 2 (with three component images) shows a design example of a widely tunable laser based on the PDK for an InP-based PIC foundry process by SMART Photonics [3]. Both VPIcomponentMaker and IPKISS provide PDKs for this process:



Above: 2a) Simulation schematic created in VPIcomponentMaker Photonic Circuits using BBs of VPItoolkit PDK SMART, including elastic connectors, and examples of port locations



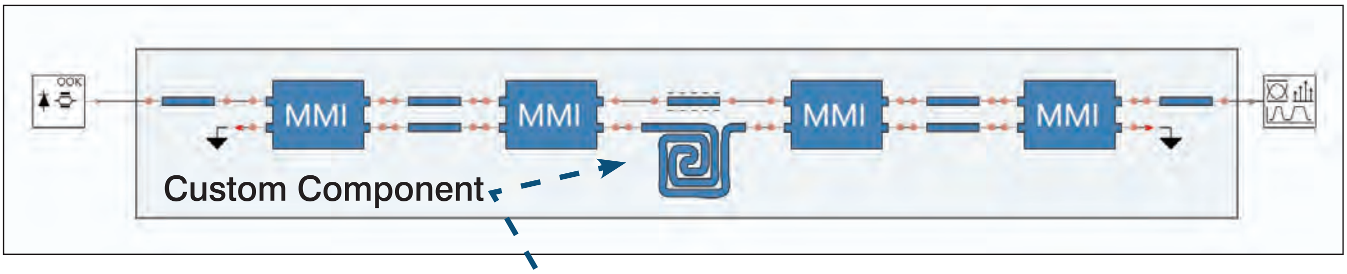
Right: 2b. Exemplary simulation results demonstrating the laser tuning characteristics

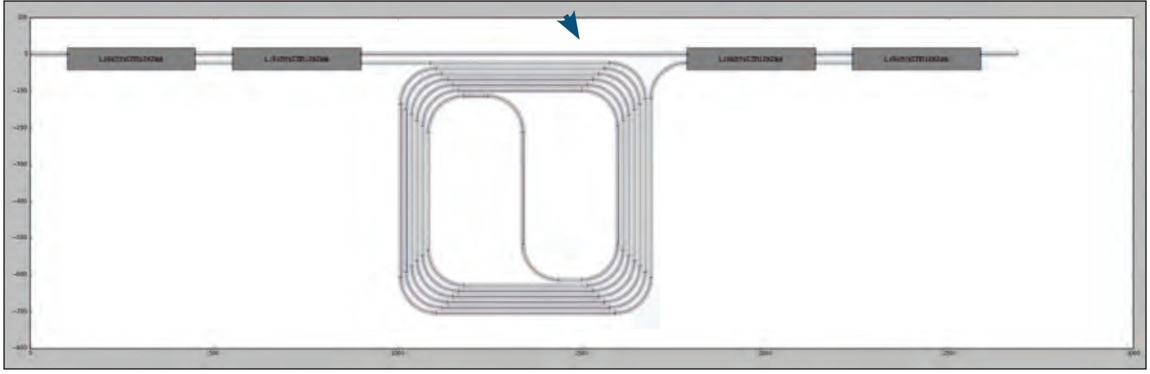
2c. The corresponding automatically exported mask layout in Luceda's IPKISS Design Platform

Integrated Optical Buffer

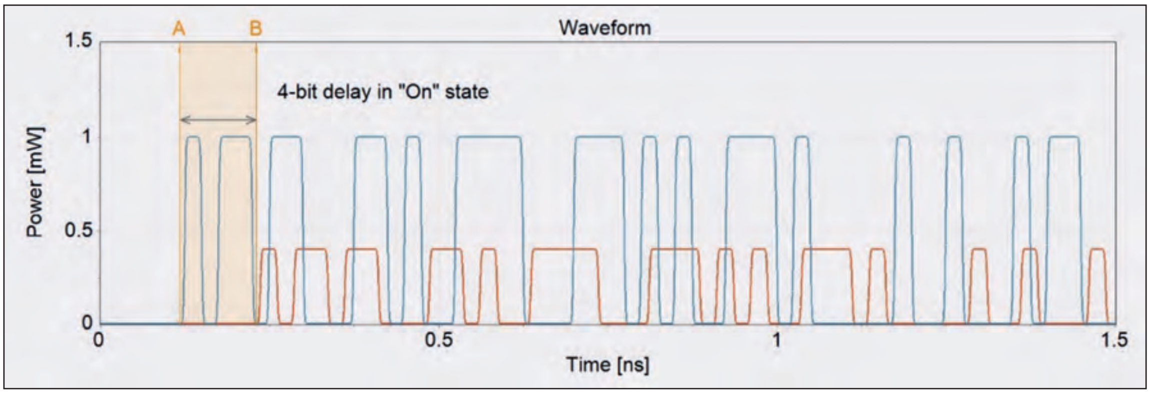
Figure 3 (with three component images) shows a design example of an integrated optical buffer based on the PDK for a SiN-based PIC foundry process by LIGENTEC [4] Both VPIcomponentMaker Photonic Circuits and IPKISS provide PDKs for this process:

3a. Simulation schematic created in VPIcomponentMaker Photonic Circuits using BBs of VPItoolkit PDK LIGENTEC, including elastic connectors, and a custom component for waveguide delay line





3b. The corresponding automatically exported mask layout in Luceda's IPKISS Design Platform



3c. Exemplary simulation results of a 4-bit delay for the output signal introduced by the optical buffer in "switched-on" state

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[1] S. F. Mingaleev, S. G. Savitski, E. S. Sokolov, I. G. Koltchanov, and A. Richter, Layout-Aware Schematic-Driven Design Methodology for Photonic Integrated Circuits, European Conference on Integrated Optics, p-21 (2016).

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[3] SMART Photonics, https://smartphotonics.nl/ (accessed 20 June 2020)

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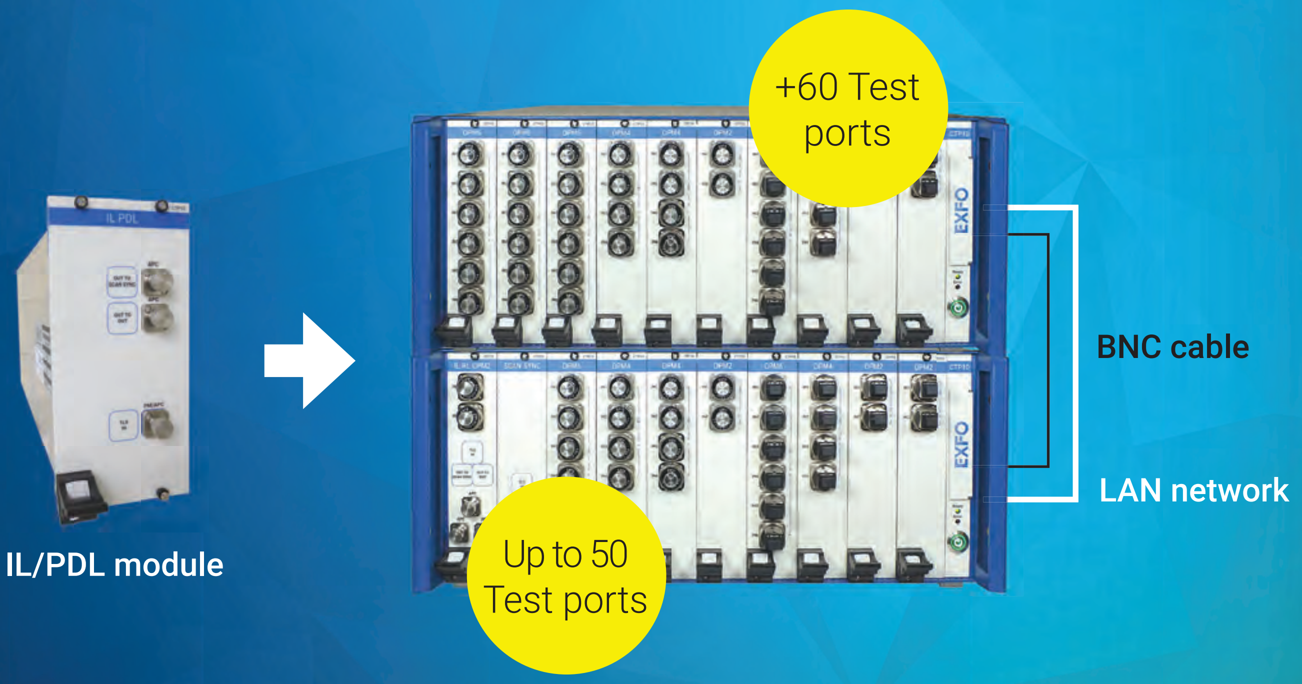
For further information, visit us at www.VPIphotonics.com and www.LucedaPhotonics.com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