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OPTICAL COMMUNICATION WITH INP PICS

Combining InP PICs with state-of-the-art silicon CMOC process nodes creates an efficient coherent technology

RISKS BURSTING THE QUANTUM BUBBLE

The arrival of quantum technologies, and the demanding compound semiconductor devices

PHOTONIC INTEGRATED CIRCUIT PACKAGING

Using standardized components and automated assembly processes in the testing and development stages can significantly reduce costs

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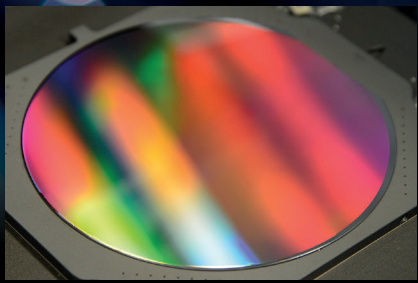

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VIEWPOINT

By Laura Hiscott, Editor

Looking ahead to ECOC

WELCOME TO this edition of PIC Magazine – my first issue since taking over as editor. It's an exciting time to be joining, with many innovations from the lab edging to application in real-world settings.

I am looking forward to watching the industry flourish and seeing the many possibilities offered by this technology come to fruition. I will ensure PIC Magazine continues to serve its readership as this industry grows and matures.

As products evolve from prototyping to high volume manufacturing, some critical challenges are integration and packaging. As intricate as the PICs themselves are, the surrounding module can be just as tricky, representing a significant fraction of the cost, particularly if it is being altered at every iteration in the design process.

Fortunately, many companies are working on solutions. In this issue Vanguard Automation describes how photonic wire bonding and facet-attached micro-optical components, both created with 3D nano-printing, can offer a scalable packaging process.
In a similar vein, PHIX Photonics Assembly share its approach to keeping costs down during the development phase by using standard components and automated assembly processes. For example, using bond pad pitches compatible with standard printed circuit boards can reduce costs during design iterations, until the finalised PIC is ready for custom packaging.

This edition also includes an interview with Eléonore Hardy, who co-chaired a dedicated photonics workshop at the CEA Leti Innovation Days. The workshop involved talks and panel sessions on the latest developments in photonics and a wide range of applications, including inspiring biomedical devices that promise to dramatically improve people's lives.

The next big event that will bring the community together is the European Conference on Optical Communication (ECOC), taking place from 1-5 October in Glasgow. This conference and exhibition is Europe's largest in the field, showcasing the latest advancements and fostering collaborations across the industry.

I look forward to seeing you there.

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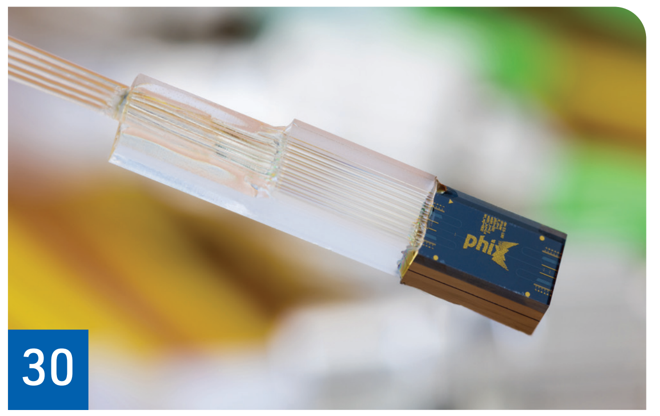

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Vector Photonics and Sivers collaborate

Companies to evaluate new material for next-generation lasers

SIVERS PHOTONICS has received an initial order from Vector Photonics for the evaluation of epitaxial material for a new, next-generation surface coupling laser project.

The order, which includes laser fabrication and life testing, will be the first time both Glasgow-based companies have worked together on a project. It will be manufactured on the Sivers InP100 platform at their Glasgow foundry.

Euan Livingston, sales and marketing director at Vector Photonics, explained: “Vector Photonics operates a ‘fabless’ business model, outsourcing wafer fabrication to semiconductor foundry partners around the world. Sivers Photonics is an ideal fabrication partner for Vector Photonics in every aspect. Furthermore, the proximate location of the businesses supports a particularly close working relationship, with clear benefits to in-depth development and R&D working”.

Livingston added: “The order with Sivers Photonics helps to establish the required quality and life testing of our laser materials and is a significant part of our ongoing commercialisation of surface coupling laser devices.”

Andy McKee, CTO and interim managing director at Sivers Photonics, said: “We are delighted to partner with Vector Photonics on this project, using our expertise to support the commercialisation of next generation surface coupling lasers whilst also continuing to strengthen Scotland’s strong position as a global leader in photonics. Following the successful wafer fabrication and testing phases and utilising our proven foundry capabilities, we will enable Vector Photonics to deliver to their customers at scale.”

“Surface coupling laser offer great performance by reducing power consumption, latency, size and costs and will be a great solution for the data centre market. Sivers likes to support innovation which makes this new partnership with Vector Photonics a great match,” said Anders Storm, CEO of Sivers Semiconductors.

PhotonVentures raises €60 million to supercharge photonics startups

PHOTONVENTURES has launched a venture capital fund aimed at early-stage photonic chip startups and scale-ups. €60 million was raised in its first financing round with PhotonDelta as the lead investor alongside numerous private investors.

PhotonVentures plans to raise a total of €100 million to €150 million, with its final close set for the start of 2024. It will prioritise Series A rounds, with the aim of providing investments between €1 million and €2.5 million. PhotonVentures’ investment strategy leverages the Dutch PhotonDelta ecosystem to accelerate European startups and scale-ups.

PhotonVentures is an independent deep-tech venture capital firm that has emerged from PhotonDelta, a hub of the Dutch integrated photonics ecosystem. The two organisations are strategic partners with the aim of supporting the rapid growth of Europe’s photonics industry. Photonic chips are critical in a range of applications like quantum computing, robotics, sustainable agriculture, and autonomous vehicles. The fund is planning to initially invest in 15 European deep-tech companies that have potential to grow into international winners in their sectors. The startups should have an integrated photonics-based MVP connected to the European ecosystem.

Founded in 2014, PhotonDelta has made significant investments in photonics companies and R&D over the last five years. In backing the fund, PhotonDelta seeks to progress its goal of building a world-leading industry for integrated photonics in the Netherlands and Europe. Last year, PhotonDelta secured €1.1 billion in public and private investment to scale up production, build 200 startups, create new applications for photonic chips and develop infrastructure and talent. PhotonDelta is a lead investor in the fund via the transfer of its portfolio to PhotonVentures. The PhotonVentures board consists of Joachim de Sterke, Pieter Klinkert and Rijkman Groenink. Joachim de Sterke has a financial, legal and technical background with long-term investment experience, and is co-founder and CFO of PhotonDelta. Pieter Klinkert joined PhotonDelta in 2021 and previously was investment manager at OostNL and held positions in financing and corporate investment at various banks. Rijkman Groenink is a former banker with experience in the financial sector.

Joachim de Sterke, General Partner at PhotonVentures, said: “There are hundreds of incredibly promising startups and scale-ups driving development and application of photonic chips that need investment and support to take the next step on their journey. PhotonVentures fulfils this need, it is the only fund geared directly towards photonic chip startups and scale-ups. Our aim is to play an instrumental role in making Europe a global leader in integrated photonics. We will continue to expand our fund to enable us to invest in scores of startups over the next few years.”

Marvell announces new 800 Gbps coherent DSP

Data infrastructure company Marvell has announced a new coherent digital signal processor (DSP) called Orion.

THE FIRM says Orion is the industry's first 800 Gbps coherent DSP for pluggable modules, and is intended to change the economics and performance of the transport networks connecting carrier and cloud assets over extended geographic areas.

Marvell has stated that Orion delivers twice the maximum bandwidth over today's solutions while staying within the stringent thermal and electrical limits of pluggable modules. This gives carriers and cloud service providers the opportunity to shift from building transport networks with traditional optical transport networking transmission equipment to designing networks around streamlined, scalable architectures built on merchant routers, integrated optical modules and other technologies for a lower total cost of ownership.

Orion-based pluggable modules are expected to deliver up to 75% in capex and opex savings over traditional transport equipment for popular carrier use cases such as metro networks. Orion-based modules are also expected to provide 30% lower cost and power per bit compared to currently available pluggable modules.

By spanning a wider range of transport lengths and bandwidth capacities, Orion aims to increase the performance of pluggable modules across multiple use cases, including metro network connections, 600 Gbps regional network connections, 400 Gbps long-haul connections, and 800 Gbps data centre interconnects.

"Orion represents a tipping point for optical transport technology," said Achyut Shah, Senior Vice President and General Manager of the Connectivity Business Group at Marvell. "With Orion, pluggable modules will be able to be deployed across these complex, high-performance networks while delivering substantial reductions in cost and power. Orion-based modules will also deliver the bandwidth needed for data centre interconnects to meet the exploding demand for AI. Fuelled by the innovation of our partners, pluggable modules based on Orion will become the leading choice for carriers and clouds."

Produced on 5nm technology, Orion is the fifth generation coherent DSP from Marvell and offers twice the bandwidth in the same small module form factors as Deneb and Canopus, Marvell's 400 Gbps coherent DSPs that have been widely adopted by carriers and clouds.

Orion is a coherent DSP supporting standards-based pluggable form factors at symbol rates in excess of 130+ GBaud, which allows Orion-based modules to transfer data at a faster rate and across longer distances than current modules. Orion incorporates Marvell's 112 Gbps SerDes developed as part of Marvell's technology platform for 5nm devices.

Orion complies with OIF, OpenZR+, OpenROADM, and IEEE standards and can be used in the QSFP-DD, OSFP, and CFP2 form factors, to support widespread transition into coherent pluggable-enabled architectures.

Orion-based modules could also pave the way for greater adoption of IPoDWDM. Many carriers are in the midst of once-in-a-decade upgrade of their core network routers—which can cost hundreds of thousands of dollars and occupy multiple racks—from 100 Gbps to 400 Gbps. Coupled with Orion-based modules, 400 Gbps IPoDWDM routers could match the performance of existing transport equipment at a far lower cost.

Lightwave Logic expands its Colorado operations

LIGHTWAVE LOGIC has announced the completion of new laboratory production facilities, expanding the corporate facility in Englewood, Colorado by nearly 10,000 square feet for a total of approximately 23,500 square feet to support new commercial activity.

The technology platform company focuses on leveraging its proprietary electro-optic polymers to transmit data at higher speeds with less power in a small form factor to improve the efficiency of internet infrastructure. According to the Computing Technology Industry Association, Colorado's tech industry has an economic impact of $52.6 billion, or 12.2% of the state's economy, fifth highest among all states.

The renovations and installation of new laboratory and engineering facilities expands the size of the Lightwave Logic's Englewood facility by over 65%, enabling commercial device testing and evaluation, production reliability testing, laser characterization, SEM analysis and the expansion of the company's chemical synthesis production line. The facility will support the company's recently added employees, including organic chemists as well as photonics, packaging and reliability engineers who will bring the company's team to 33 members.

"As we enter into this exciting new phase of advancing our commercial business plans, we believe that we now have the team and the facilities in place to make our electro-optic polymers ubiquitous," said Dr. Michael Lebby, Chairman and Chief Executive Officer of Lightwave Logic.

Sandia Labs announces method to integrate microscale optical devices on silicon microchips

Sandia National Laboratories has been awarded a patent for developing a novel method of integrating microscale optical devices onto silicon

USING THIS TECHNIQUE, the R&D centre, which is based in Albuquerque, New Mexico, created a microscale laser embedded in silicon. While similar lasers have been built before, the company says this is the first time that such a device could function within photonic integrated circuits. This technology could be applied to make self-driving cars safer, data centers more efficient, biochemical sensors more portable and radars and other defense technologies more versatile.

While silicon is the mainstay of the semiconductor and computer chip industries, it is not a good material for making lasers. This poses challenges for the development of microscale optical devices for use in these technologies. One approach to tackling this obstacle is to design a way for optical components made from a variety of materials to coexist on a silicon microchip.

However, these kinds of materials can't just be glued into place. Instead, Sandia research scientist Ashok Kodigala, a co-inventor of the new technique, fused them to silicon in complex layers, a process also called heterogeneous integration.

The Sandia team successfully demonstrated heterogenous integration techniques to create hybrid silicon devices: hybrid lasers and amplifiers made from both indium phosphide and silicon, and similarly modulators made of both lithium-niobate and silicon, which encode information in light generated from the lasers. Moreover, high-power and high-speed germanium detectors were developed to keep up with the lasers and modulators under the same platform.

With this method, Sandia can build many critical components for high-power optical systems, including build

high-bandwidth, high-speed optical devices, including indium phosphide lasers, lithium niobate modulators, germanium detectors and low-loss acousto-optic isolators.

Other organizations, including the University of California, Santa Barbara, and Intel Corp., have built similar lasers, but Sandia has broadened the class of devices that can be integrated. For the first time, these devices could work together on optical microchips, also called photonic integrated circuits.

Semiconductor fabs could use Sandia technique/US leadership
Sandia built its chip-scale lasers with a goal of transferring the technology to industry, and stated that the achievement could strengthen America's leadership in semiconductor technology. The team used many of the same tools found at commercial semiconductor plants, and the lasers generate light in wavelengths commonly used in the telecommunications industry, called the C-band and the O-band.

"Once we demonstrate this photonic platform at a national lab, we can then pass this technology to U.S. companies, where they can focus on even larger-scale production for commercial and U.S. government applications," Kodigala said.

"This allows the U.S. to lead and have less dependency on foreign manufacturing capabilities," said Patrick Chu, who co-leads the National Security Photonics Center, a group of more than 60 photonics scientists and engineers at Sandia's

Microsystems Engineering, Science and Applications complex.
The new technique was conceived with funding from Sandia's Laboratory Directed Research and Development program and developed it under a Defense Advanced Research Projects Agency program called Lasers for Universal Microscale Optical Systems.

Photonic semiconductors support CHIPS and Science Act
President Biden made headlines in 2022 when he signed the CHIPS and Science Act, a nonpartisan, $52.7 billion boost for the semiconductor industry. While the legislation is expected to increase production of American-made computer chips, it also directs funding for photonic semiconductors.
Sandia is also investing in optical microchips because they transmit more information than conventional ones. But manufacturing challenges have prevented their widespread adoption, Chu said. Even though the technology is well known in scientific circles, on most microchips, he said, electronic technologies still reign supreme.

With a working platform to build photonic circuits, Sandia has positioned itself to support industry and other institutions performing photonics research and development in the coming years. Sandia research is not currently funded by the CHIPS Act.

"We know our process is scalable, so that's one way we're supporting the CHIPS Act mission," Chu said. "Sandia is eager to collaborate with others and start building new technologies together."

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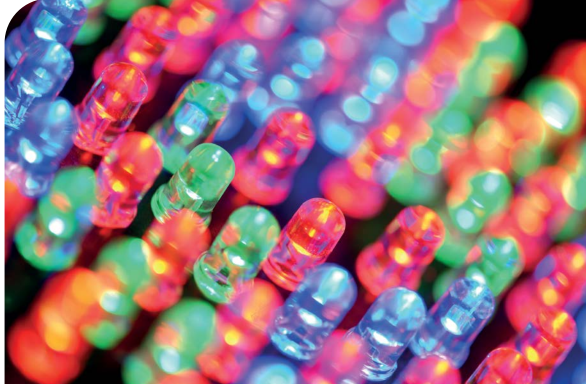
— Dr. Suresh Venkatesan, POET Technologies Chairman & CEO

Advanced Micro Foundry and Ascenta Technologies launch MPW runs

Advanced Micro Foundry (AMF) and Ascenta Technologies (Ascenta) have announced a new milestone in their collaboration: The AMF Visible + Infrared (IR) multi-project wafer (MPW) series



AMF is a Silicon Photonics foundry, while Ascenta is a spin-off led by researchers from the Max Planck Institute of Microstructure Physics and the University of Toronto. With this project, the two companies aim to bring a versatile and functional Visible + IR platform to the photonics community.

The visible platform was built using AMF's expertise in low-loss SiN platform technology, leveraging a multi-layer silicon nitride and silicon stack. AMF says that this platform enables the creation of high-and low-confinement single-mode waveguides, effectively spanning a wavelength spectrum of 400 nm to 1600 nm, as well as active functionalities including photodetectors and highly efficient phase shifters.

> The visible platform was built using AMF's expertise in low-loss SiN platform technology, using a multi-layer silicon nitride and silicon stack

AMF partnered with Ascenta to develop a library of Visible and IR photonic components on AMF's silicon nitride technology platform. The library includes a suite of devices such as low-loss waveguides, fiber-to-chip couplers, photodetectors, thermo-optic phase shifters, MEMS structures, and modulators. This collaborative offering seeks to empower optical designers with the necessary tools to design complex PICs with confidence, paving the way for further innovation.

Both companies are actively aggregating users for MPW runs in 2024. The AMF Visible MPW offering aims to advance visible product development in fields ranging from LiDAR, optical computing, health, and augmented reality.

AMF CTO, Dr. Patrick Lo remarked "I am very excited to see the interest from the community to utilise the wide space of visible applications. AMF is very proud to partner with Prof. Joyce Poon & Ascenta to provide access to this platform via MPW to support the community and grow the market".

Ascenta CEO, Mr. Ilan Almog added "The Ascenta team is grateful for our partnership with AMF and thrilled to share the VIS+IR silicon photonics platform with MPW participants. The platform is the same fundamental technology Ascenta is using to develop its products, in the 3D sensing space and beyond. We are excited to enable the wide range of applications brought forth by the creativity of the community, leveraging the capabilities in the platform".

Coherent has shipped over 200 billion VCSELs

OPTOELECTRONICS firm Coherent has announced that is has shipped more than 200 billion VCSEL emitters to date for sensing applications.

"In 2013, we began working on two-dimensional VCSEL arrays for 3D sensing in smart phones," said Giovanni Barbarossa, Coherent chief strategy officer and president of the materials segment. "We scaled our production capabilities from 3-inch to 6-inch wafers in 2017, just in time to help enable the market launch of the first smartphones with facial biometrics."

Barbarossa adds that the company believes semiconductor laser-based sensing applications will continue to expand into new applications such as in smart watches for health monitoring and in smart glasses for extended reality. VCSELs will also continue to enable a growing market for in-cabin sensing and LiDAR in automotive.

The company recently announced a new VCSEL module technology that enables ultracompact pattern projectors, flood illuminators, and tightly integrated sensing subsystems. This patented module technology relies on an flip-chip assembly of backside-emitting VCSEL arrays on application-specific integrated circuits and supports the integration of photodetector arrays.

UK consortium to address skills shortages

Bay Photonics, Phlux Technology and the University of Sheffield win £400k Innovate UK funded grant

BAY PHOTONICS and Phlux Technology are part of a consortium to have been awarded an Innovate UK funded grant (~£400k), to address the semiconductor skills shortage in the UK. The project is led by the department of electronic and Eeectrical Engineering and the department of multidisciplinary engineering education at the University of Sheffield.

Phlux, a spin-out of the University of Sheffield, designs high-performance infrared sensors using AlGaAsSb for sensing and communication systems. Bay Photonics is a UK-based design facility that focuses on photonic chip assembly and packaging for optoelectronic component manufacturers. The project is called ASISST (Addressing Shortages in Semiconductor Skills Training) and will see the partners producing accessible, relevant semiconductor training courses to meet the specific requirements of employers in the semiconductor sector in order to increase the flow of talented people into the industry.

Ben White CEO and founder of Phlux Technology said: " The UK has a wealth of game changing ideas, but a chronic shortage of the people with the skills needed to turn these ideas into companies. We are pleased to help inspire the next generation of STEM innovators who fulfil their potential and bring a step change in the development of tech companies across the UK.

We at Phlux hope to benefit from this work by being able to hire the next generation of innovators to advance our technology in Sheffield. Andrew Robertson, CTO of Bay Photonics commented: “This project is in complete alignment with the recent UK National Semiconductor Strategy. We are focused on providing semiconductor training skills that the UK semiconductor industry is crying out for to ensure we remain competitive in this strategically important and rapidly growing market.”

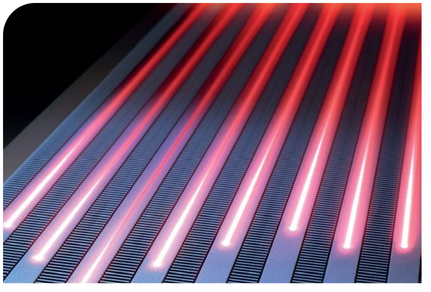
KAIST research team unveils new path for dense photonic integration

KAIST (President Kwang-Hyung Lee) announced on the that a research team led by Professor Sangsik Kim of the Department of Electrical and Electronic Engineering discovered a new optical coupling mechanism that can increase the degree of integration of optical semiconductor devices by more than 100 times.

The degree of the number of elements that can be configured per chip is called the degree of integration. However, it is very difficult to increase the degree of integration of optical semiconductor devices, because crosstalk occurs between photons between adjacent devices due to the wave nature of light.

In previous studies, it was possible to reduce crosstalk of light only in specific polarizations, but in this study, the research team developed a method to increase the degree of integration even under polarization conditions, which were previously considered impossible, by discovering a new light coupling mechanism. This study, led by Professor Sangsik Kim as a corresponding author and conducted with students he taught at Texas Tech University, was published in the international journal 'Light: Science & Applications' [IF=20.257] on June 2nd. done. (Paper title: Anisotropic leaky-like perturbation with subwavelength gratings enables zero crosstalk). Professor Sangsik Kim said, "The interesting thing about this study is that it paradoxically eliminated the confusion through leaky waves (light tends to spread sideways), which was previously thought to increase the crosstalk." He went on to add, "If the optical coupling method using the leaky wave revealed in this study is applied, it will be possible to develop various optical semiconductor devices that are smaller and that has less noise."

Professor Sangsik Kim is a researcher recognized for his expertise and research in optical semiconductor integration. Through his previous research, he developed an all-dielectric metamaterial that can control the degree of light spreading laterally by patterning a semiconductor structure at a size smaller than the wavelength, and proved this through experiments to improve the degree of integration of optical semiconductors. These studies were reported in 'Nature



Communications' (Vol. 9, Article 1893, 2018) and 'Optica' (Vol. 7, pp. 881-887, 2020). In recognition of these achievements, Professor Kim has received the NSF Career Award from the National Science Foundation (NSF) and the Young Scientist Award from the Association of Korean-American Scientists and Engineers.

Meanwhile, this research was carried out with the support from the New Research Project of Excellence of the National Research Foundation of Korea and and the National Science Foundation of the US.

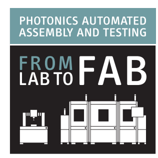
Luceda Photonics and Aluvia Photonics release new process design platform

LUCEDA PHOTONICS has announced a collaboration with Aluvia Photonics, the world's first Al_2O_3 foundry for integrated photonics applications. This collaboration offers designers an advanced Process Design Kit (PDK) within the Luceda Photonics Design Platform, enabling access to the upcoming Multi-Project Wafer (MPW) runs at Aluvia Photonics.

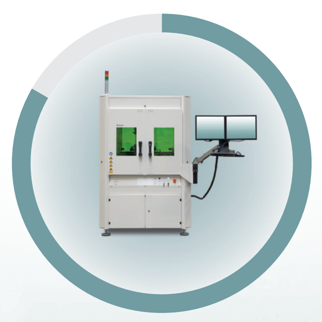
Integrated photonics has been revolutionizing various industries, and aluminium oxide (Al_2O_3) has emerged as a promising material to further expand the possibilities in this field. With properties including a broad transparency window down to the ultraviolet and low propagation losses, aluminium oxide opens up new application possibilities, such as on-chip ion trapping.

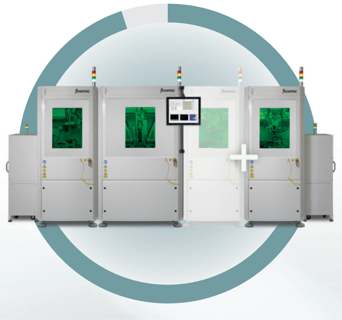
The partnership between Luceda Photonics and Aluvia Photonics aims to provide designers and researchers with access to Aluvia's Al_2O_3-based photonic technology, empowering them to pursue innovative photonic designs. By accessing a comprehensive PDK in the Luceda Photonics Design Platform, customers can leverage Luceda's design tools to design their integrated photonic circuits and also take advantage of Aluvia Photonics' upcoming MPW runs.

"We are excited to partner with Aluvia Photonics to offer a comprehensive Photonic Design Kit for alumina-based integrated photonics," said Pieter Dumon, CTO of Luceda Photonics. "This collaboration enables our customers to access and leverage this new technology, offering a broad wavelength range and unlocking a whole world of new applications."



Automation Solutions for Photonics Packaging and Testing





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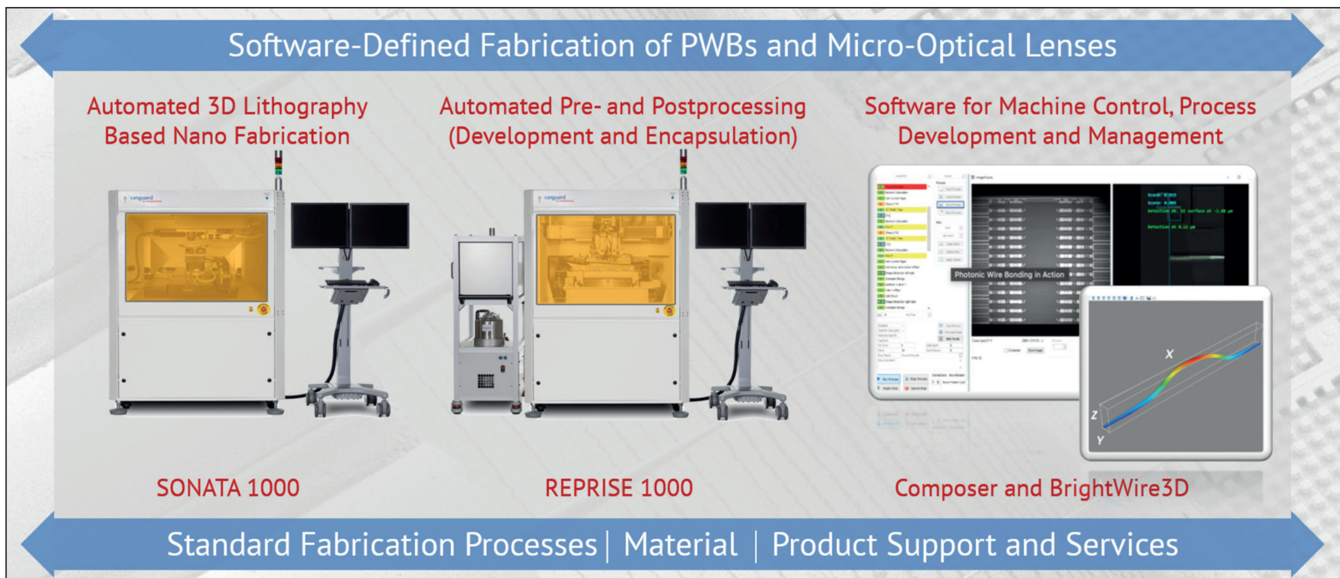
Photonic integration and packaging with Photonic Wire Bonding and facet-attached micro-optical elements

Fully automated solutions for seamless transitioning from prototyping to high-volume production

BY SEBASTIAN SKACEL, LAURA HORAN AND CALIN HRELESCU, VANGUARD AUTOMATION

THE RAPID GROWTH of photonic integrated circuits is driving the need for fast innovation, and this is made possible by the development of Photonic Wire Bonding (PWB), which creates low-loss, 3D free-form connections between optical components. Just as electrical integrated circuits have benefitted from electronic wire bonding, photonics innovations will now advance on a faster trajectory thanks to PWB.

Built on advanced 3D nano-printing technology, PWB is inherently a fully automated process and provides a high degree of design flexibility. Additionally, 3D nano-printing has been used for several years to fabricate facet-attached micro-optical elements on optical chips and fibres, enabling low-loss coupling with relaxed alignment tolerances and wafer-level probing of optical devices. With both PWB and facet-attached micro-optical elements in their technology portfolio, Vanguard Automation's mission is to advance photonic packaging and assembly by providing scalable 3D nano-fabrication solutions, allowing seamless transitions from prototyping to industrial high-volume production.



➤ Figure 1: Vanguard Symphony, Vanguard Automation's fully automated photonic integration and packaging solution comprising the automated 3D lithography-based nano fabrication unit Sonata 1000 and the automated pre- and postprocessing unit Reprise 1000. The systems are equipped with Vanguard's BrightWire3D software, enabling highly precise detection and on-the-fly trajectory calculations. Vanguard's own photoresists (Vanguard VanCore series), standard process development, as well as product support and engineering services complete Vanguard's solution from prototyping to high-volume production.

Figure 2: List of Vanguard Automation's technology users and ecosystem partners which can be disclosed at the time of publication.

Today's packaging and assembly challenges arise from the need to integrate various optical components from different material platforms. Take, for example, a hybrid module, comprising indium phosphite-based active devices such as lasers or semiconductor optical amplifiers, passive devices made from silicon, silicon nitride or lithium niobate, as well as photodiodes and single-mode or polarization-maintaining fibres. Packaging such a module entails an integration challenge due to the very specific optical properties of each component. To be viable for industrial mass production, packaging and integration solutions must address and solve the challenges that these specific optical properties present.

To reduce coupling loss when combining different photonic devices, the specific mode field profiles have to be matched and the devices have to be aligned very precisely. In industrial mass production, processes such as mode matching and alignment must be fast and reproducible since speed and yield determine the cost of the product. Additionally, the packaged assemblies need to be reliable under various environmental conditions which are specific to their applications.

Although the application-specific conditions, such as the environmental conditions that the packaged assemblies must withstand, may vary considerably, the fundamental requirements of efficient and reliable packaging hold true for a large range of application areas such as telecommunications and datacom, 3D sensing, LiDAR and quantum applications. Hence, even though photonic devices used for such specific applications are made with sophisticated processes from sometimes exotic material platforms, the optical packaging

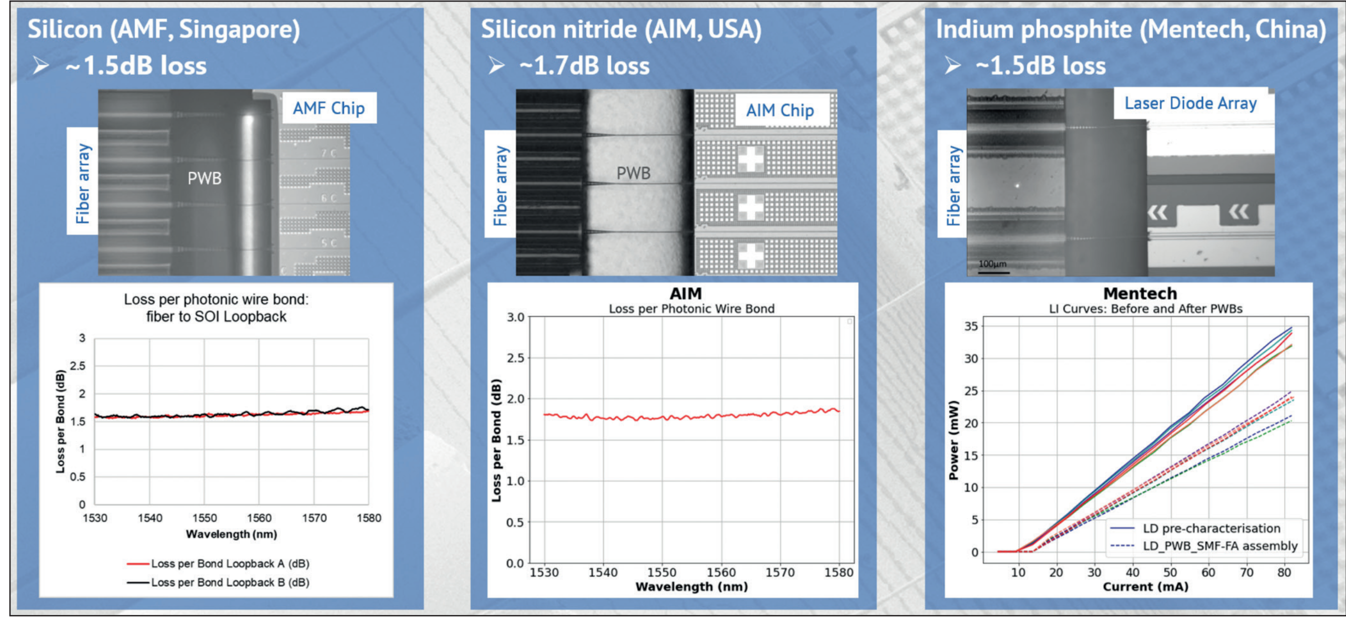


Figure 3: Examples of photonic wire bonds (PWBs) demonstrating low loss connectivity solutions for active and passive devices from various foundries. (left) AMF (Si) chip with 1.5dB loss and (centre) AIM (SiN) chip with 1.7dB loss per PWB. (right) Mentech (InP) laser diode array with 1.5dB loss per PWB.

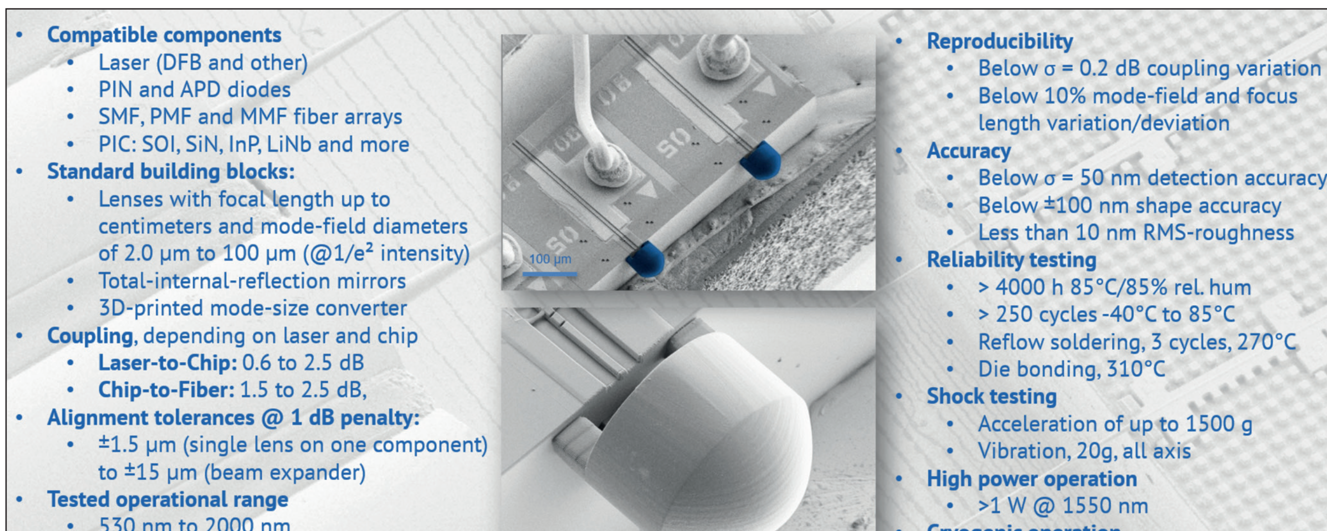


Figure 4: Vanguard Automation's industrial grade facet-attached micro-optical elements technology compatible with a large variety of applications and widely tested under industry standards.

or integration process remains in most cases the biggest cost driver.

Vanguard Automation aims to solve these challenges with its fully automated solution portfolio: the Vanguard Symphony comprising two systems, one for the fabrication of PWB as well as facet-attached micro-optical elements (Vanguard Sonata 1000), and one for postprocessing of connected optical assemblies completing the fully automated packaging process (Vanguard Reprise 1000). This solution includes Vanguard's Brightwire3D software for automated, highly precise (accuracy < 100 nm) interface detection as well as on-the-fly calculation of optimal PWB trajectories, and dedicated photoresists tailored to meet strict industrial reliability requirements (Vanguard VanCore series). Vanguard Automation also provides standard processes as well as engineering service and support to enable customers to advance quickly from prototyping phases to high-volume production (see Fig. 1).

Over the past years, the number of Vanguard technology adopters and ecosystem partners has rapidly increased (see Fig. 2). Our customers and partners have used Vanguard's PWB and facet-attached micro-optical elements technology in many applications solving the various challenges of hybrid module packaging and integration.

In the data centre, telecommunication, and artificial intelligence markets Vanguard's customers [1] have utilized innovative PWB processes working on various material platforms, such as silicon, silicon nitride, indium phosphite, and lithium niobate to advance the concept of hybrid integration [1] (see Fig. 3). Offering the unique advantage of using only one coupling Process Design Kit (PDK) to couple to other types of optical components, Vanguard's technology portfolio is compatible with all academic and commercial foundries. Consequently, foundries can avoid having to create complex spot size converters. [2]

Since the Vanguard technology can work with simple inverse tapered edge couplers realised by stepper lithography, the chip real estate used for sophisticated couplers can be reduced substantially, paving the way towards a novel and more universal standard for optical coupling. PWB has been utilized for self-injection-locked Kerr soliton microcombs and lasers with sub-100Hz linewidth. [3, 4] In the field of quantum applications, PWB has been successfully tested in ultra-low-temperature experiments. [5]

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Furthermore, Vanguard Automation's facet-attached micro-optical elements have demonstrated improved efficiencies for High-Bandwidth Coherent Driver Modulators (HB-CDM) [2]. Vanguard's dedicated photoresists series VanCore, tailored to meet strict industrial reliability requirements, is proven to be reliable under the harshest environmental conditions [2]. (see Fig. 4). The facet-attached micro-optical elements have created

a powerful platform for electro-optical engines for transceivers, co-packaged optics, light engines, and sensing devices [6].

Incorporating Vanguard's technology improves the coupling efficiency of light as it passes from one photonic device to another, which in turn reduces the power consumption of the combined solution (see Fig. 3 & 4). The precise alignment and printing of the facet-attached micro-optical elements at the wafer level enables significant scalability and enhances the ability to address new applications [6, 7, 8, 9]. Vanguard's facet-attached micro-optical elements technology has already been successfully used in LiDAR applications for beam shaping elements [10] and in quantum applications to increase the effective collection area of superconducting nanowire single-photon detectors (SNSPD), thereby overcoming a fundamental design conflict of such devices [11].

Due to its complementary technology portfolio combining PWB and facet-attached micro-optical elements, Vanguard Automation offers volume production customers a simplified path for incorporating the Vanguard technology into their production chain. In the first instance, Vanguard technology can be included in hybrid approaches together with conventional technologies such as active alignment [2] to improve coupling efficiencies and yield. This approach does not imply any major changes to the chain of process steps in production. Secondly, beam-expanding micro-lenses can be implemented in products to ease the positioning tolerance of PICs and other optical components such as InP-lasers and fibres, thus relaxing alignment tolerances to such a degree that passive assembly becomes a viable process [9]. Finally, the full disruptive potential for photonic integration and packaging can be introduced by incorporating PWB into the product design. This supports a shift towards standard pick and placing of all components of a hybrid multi-chip assembly with very relaxed placement tolerances, while simultaneously ensuring high coupling efficiency and high yields, as well as fast manufacturing and high package density.

In summary, Vanguard's PWB technology enables the combination of the complementary strengths of different optical integration platforms in advanced photonic multi-chip modules leading to compactness with high performance and design flexibility. Vanguard's photonic integration solution portfolio is completed with facet-attached micro-optical elements on optical chips and fibres, allowing for low-loss coupling with high alignment tolerances and for wafer-level probing of optical devices. The fully automated, highly reproducible, and reliable Vanguard Symphony solution is already being used by research and industry customers targeting next-generation photonic integration and packaging.

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Enabling coherent optical communication with InP PICs

Combining InP PICs with state-of-the-art silicon CMOS process nodes creates an incredibly efficient coherent technology with exceptional date rates

BY PAUL MOMTAHAN FROM INFINERA

EMERGING in the late 2000s, coherent optical technology has revolutionised optical transport over long-haul, submarine, data centre interconnect and metro networks. Prior to the introduction of this technology, optical communication had a more primitive format, involving simply on/off modulation. Commonly referred to as intensity-modulation direct detection, this previous standard involved transmitting one bit per symbol for each wavelength, initially at 2.5 Gbit/s and then 10 Gbit/s.

The migration to coherent modulation has underpinned tremendous increases in wavelength speed, spectral efficiency and fibre capacity. Wavelength speed shot up from 10 Gbit/s to 100 Gbit/s, then to 200 Gbit/s, 400 Gbit/s, 600 Gbit/s, and most recently 800 Gb/s. And that's certainly not the end of the line, with even higher-speed coherent engines poised to hit the market, including the 1.2 Tbit/s ICE7 from our company, Infinera.

Fibre capacity is benefitting from the increase in wavelength speed. For the extended C-band, having a bandwidth of 4.8 THz, fibre capacity has evolved from 960 Gbit/s (e.g., 96 x 10 Gbit/s) to 9.6 Tbit/s (e.g., 96 x 100 Gbit/s) and most recently to more than 40 Tbit/s (e.g., 53 x 800 Gbit/s).

There are also other advantages that come from the introduction of coherent technology. One is a simpler optical infrastructure, as there is no longer a need for a carefully planned dispersion compensation module placement. Another is that coherent technology can now provide data rates of 400 Gbit/s in compact pluggable form factors, such as QSFP-DD, that can be plugged directly into non-transport host devices, such as routers. What's more, power consumption is lower than ever – it fell from approximately 5 W/G with 10 Gbit/s to around 2 W/G with the first generation of 100 Gbit/s coherent, and is now around just 0.05 W/G with today's 400 Gbit/s pluggables. So how do these miraculous devices work, and what role does InP play in them?

Inside a coherent optical engine

To understand the role of InP, one must understand the building blocks and functions inside a coherent optical engine (see Figure 1). In these engines there are three basic, high-level building blocks: a digital ASIC/DSP, analogue electronics, and photonics. Often the analogue electronics and photonics are packaged together as a transmit-receive optical sub-assembly. Together with the RF interconnects and packaging, these three basic building blocks constitute a coherent optical engine. Note, though, that each of these blocks actually consists of multiple functions.

Leveraging state-of-the-art silicon CMOS process nodes – such as 7 nm, but evolving to 5 nm, then 3 nm and beyond – in the digital ASIC, often referred to as simply 'the DSP', there are digital signal processing (DSP) functions for the receive and transmit directions and the digital-to-analogue converter (DAC) and the analogue-to-digital converter (ADC). In addition, digital ASICs tend to incorporate other functions, such as forward-error correction, framing, multiplexing, encryption and performance monitoring.

In the transmit direction, drivers take the low voltages from the DAC and convert them to higher voltages required by the modulator. Meanwhile, in the receive direction, the transimpedance amplifiers take the currents from the photodetectors and convert them to the voltages required by the ADC.

The analogue electronics building block, typically packaged as a single ASIC, is made from a material other than the CMOS silicon used for the digital ASIC. For example, in Infinera's coherent engines, analogue ASICs are made from SiGe.

Inside the photonics

For the third building block, which provides photonics, the key transmit functions include the laser and the modulator. Generating light with the required frequency, the laser is always made from InP. Its emission is coupled into the modulator, which encodes data by changing the phase and amplitude of the light, using an electric field to alter the refractive index of the material the light passes through.

A coherent modulator leverages four Mach-Zehnder modulators. Each splits the light into two arms, with phase changes either taking place in one arm, or more typically both arms. When the light is subsequently combined, interference controls the resulting amplitude. As a pair of phase-shifted Mach-Zehnder modulators are needed to control amplitude and phase, four are required for coherent transmission, due to the two polarisations.

There are a number of other components inside a coherent modulator. They include splitters, combiners, phase shifters, a polarisation rotator and a polarisation beam combiner. In addition, some coherent engines include an amplifier in the transmit direction to boost the wavelength power. Depending on the type of amplifier, a tuneable optical filter might also be included, to minimise this amplifier's out-of-band noise.

The receive direction contains passive photonics and photodetectors. The passives include: a polarisation beam splitter, which separates the two polarisations of the coherent signal; and a pair of 90° hybrids, which extract the phase and amplitude from each polarisation, in the form of the in-phase and quadrature components. The role of

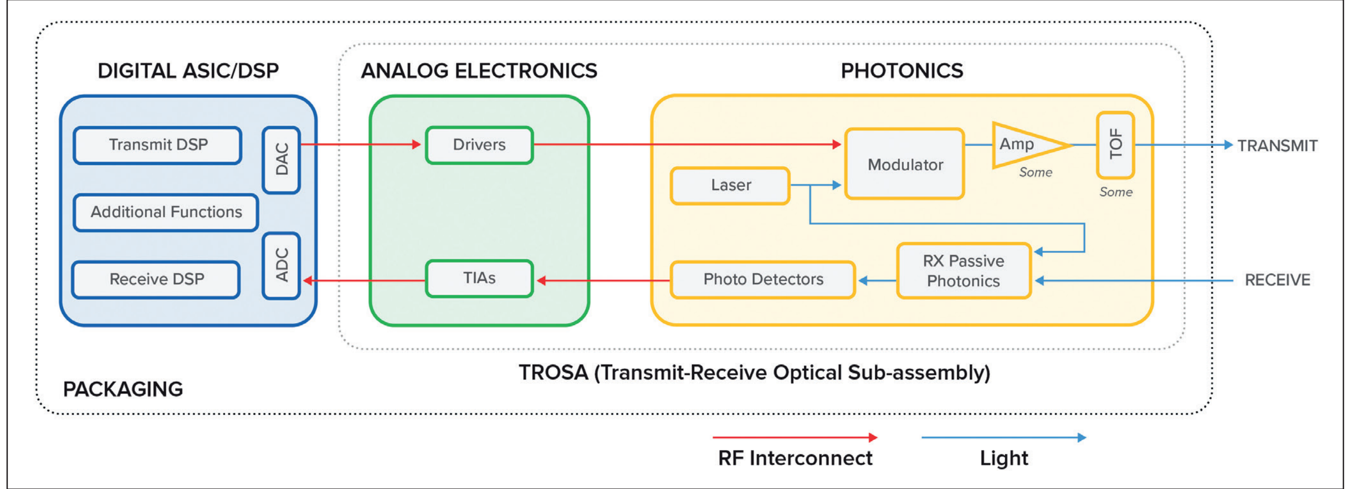


Figure 1: Coherent optical engine high-level building blocks

the photodetectors is to detect light and convert it to electrical current. There is also a laser in this part of the photonics building block, employed to help extract phase information from the received modulated wavelength. In many devices, this laser is also used in the transmit section. However, in devices such as Infinera's ICE6, separate lasers are deployed for transmit and receive.

Photonic integrated circuits

When coherent optical engines were in their infancy, their photonics building blocks were constructed from hundreds of discrete components, connected with coupling optics. But this design is certainly not ideal. It led to bulky, expensive devices with a less than optimal mean time between failure. Pioneered by our company, originally for pre-coherent optical communication with the first 10 x 10 Gbit/s PICs in 2005, this issue can be addressed through photonic integration of hundreds of previously discrete photonic components into a single chip (see Figure 2).

Mirroring the factors at play with conventional electronics, the use of advanced fabrication and integration capabilities enables the manufacture of one PIC to be far more cost-effective than that associated with making many individual optical components, prior to the integration and packaging of them. PICs also have the upper hand on many other fronts, with strengths that include a far smaller footprint, enabling the miniaturisation of optical devices, and lower power consumption. Another asset is minimised optical coupling losses, reduced by replacing coupling optics with discrete components with waveguides that connect the optical functions inside the PIC. Using waveguides for coupling also ensures fewer equipment failures, because this eliminates coupling optics as a source of failure.

Benefits of InP

Manufacturers of communications components and equipment have two material options for their PICs: InP and silicon. Deciding between them requires a weighing up of various pros and cons. The only candidate for providing the laser and optical amplification functions at DWDM frequencies is InP, so some of this material will always be present in coherent optical engines. Silicon falls short in this regard, due to its indirect bandgap that causes excited electrons to generate heat rather than light. Consequently, silicon photonics tends to be used with external DWDM lasers and amplifiers.

One promising approach to overcoming this drawback that has attracted substantial research and development is the heterogeneous integration of light-emitting materials, such as InP, into silicon PICs. However, this form of integration requires a specialised silicon foundry line. Due to this, heterogeneous integration is not currently supported as a standard offering by silicon foundries.

As well as its excellent light-generating characteristics, InP has an inherently superior modulation effect. This is a major asset for the highest-performance embedded segment of the coherent optical engine market. In addition, InP can detect DWDM light. That's not the case for silicon photonics, which leverages the integration of germanium for this function.

Today, several silicon foundries are enabling silicon photonics to be manufactured on legacy CMOS production lines, with the resulting chips using external light sources and amplifiers. This service lowers the barriers to entry for vendors that want to manufacture PICs but lack the necessary manufacturing expertise and facilities. For simpler applications, access to these foundries allows companies to produce products based on silicon photonics that have a cost advantage in very high volumes, such as millions of units per year.

Due to the evolution of CMOS process nodes and diversifying market requirements, the coherent optical engine market is bifurcating into two distinct segments: high-performance embedded optical engines and compact coherent pluggables.

High-performance engines draw on larger, more powerful and more power-hungry digital ASICs to deliver the highest possible baud rates and advanced features that maximise wavelength capacity-reach and spectral efficiency. Embedded in transponders,

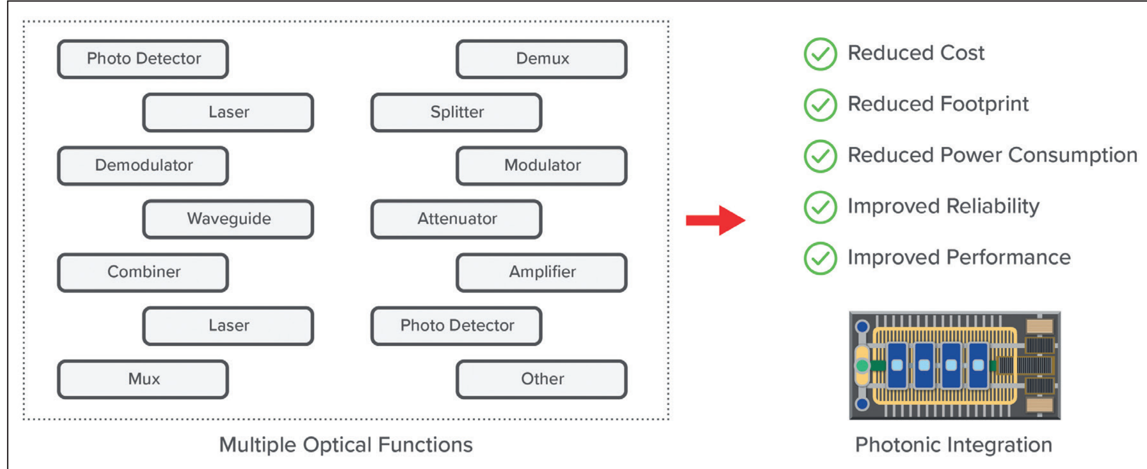
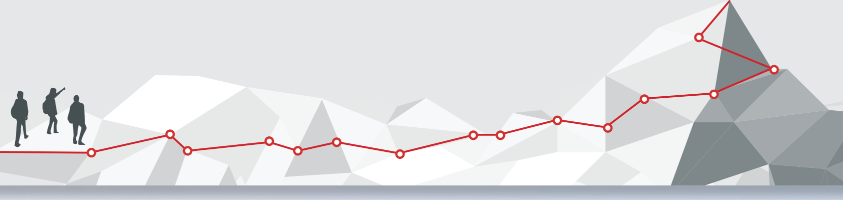


Figure 2: Photonic integration benefits



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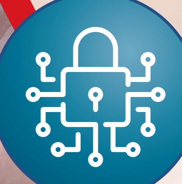

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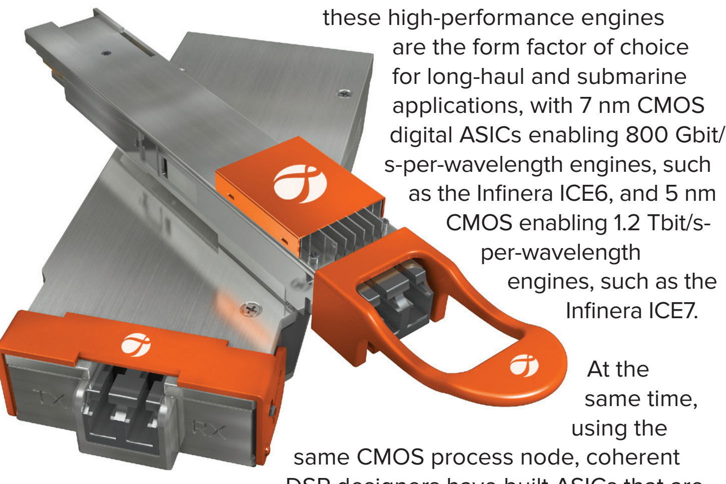

these high-performance engines are the form factor of choice for long-haul and submarine applications, with 7 nm CMOS digital ASICs enabling 800 Gbit/s-per-wavelength engines, such as the Infinera ICE6, and 5 nm CMOS enabling 1.2 Tbit/s-per-wavelength engines, such as the Infinera ICE7.

At the same time, using the same CMOS process node, coherent DSP designers have built ASICs that are more optimised for low power consumption and a small footprint. This focus has enabled 400 Gbit/s in QSFP-DD, OSFP, and CFP2 pluggable form factors. The 400 Gbit/s pluggables produced with 7 nm CMOS digital ASICs are available in a variety of flavours: 400ZR for point-to-point data centre interconnects up to 120 km; ZR+ as an umbrella term for 400 Gbit/s pluggables with enhanced performance; and XR optics, which also provides a transformative point-to-multi-point option.

As well as the generic advantages already discussed, InP PICs provide specific advantages for both types of optical engine. In the high-performance embedded segment, the electro-optic modulator effect in InP is inherently superior to silicon's plasma dispersion effect, enabling a phase change that's up to ten times higher for a given unit length and voltage. Thanks to this, InP enables more compact, power-efficient modulators that ensure lower loss, superior linearity, a larger modulation voltage for a higher transmitter signal-to-noise ratio, and thus a greater reach.

For compact pluggables, a key advantage of InP is associated with the integrated amplification required for a high transmit power. Coherent pluggables incorporating silicon photonics tend to have a low transmit power, typically around just -10 dBm, which is well short of that required by existing optical line systems – they need a transmit power of around 0 dBm. An imperfect solution is to integrate silicon photonics with an erbium-doped fibre amplifier, and add a tuneable optical filter to block out-of-band noise that's introduced with the additional amplification. But there's a price to pay, as the introduction of these additional components increases cost and power consumption. A far better option is InP-based pluggables. They include the Infinera ICE-X, which delivers a high transmit power by integrating a semiconductor optical amplifier into the PIC.

What's next?

In the high-performance embedded segment, evolution vectors include: higher baud rates; improved spectral efficiency and fibre capacity; advanced features related to nonlinear compensation, advanced modulation, forward-error correction, monitoring and automation; support for space-division multiplexing; and novel fibre types, such as multi-core fibres, multi-mode fibres and hollow-core fibres. However, as this sector starts encroaching spectral efficiency limits, there is much discussion over whether it makes sense to have one very high-speed interface (i.e., 3.2 Tbit/s) or multiple lower-speed interfaces (i.e., 2 x 1.6 Gbit /s). InP PICs have a strong role to play in both scenarios, with a proven path to 200+ Gbaud and the ability to integrate transmit and receive for multiple wavelengths into a single PIC. Demonstrating this capability are the latest coherent optical engines produced by Infinera, such as the ICE6 (2 x 800 Gbit/s) and the ICE4 (6 x 200 Gbit/s).

In the pluggable segment, likely introductions include low-power 100 Gbit/s for the metro edge, higher speeds (800 Gbit/s, 1.6 Tbit/s) for metro and data-centre interconnects, and longer reach enabling long-haul use cases. Undergoing debate is the role of coherent technologies inside the data centre, with some vendors targeting campus data centre interconnect applications with simplified 800 Gbit/s coherent engines, such as 800LR. Due to the need to reduce data-centre power consumption – a growing concern as artificial intelligence clusters and workloads are sure to scale – huge strain is being applied to data-centre power and cooling infrastructure. A strong contender to help to relieve this strain are InP modulators. Operating at low voltages and powers, these components are compelling candidates even in non-coherent intensity-modulated direct-detect transceivers that dominate today's data centres.

Beyond optical communications, InP PICs are a promising technology for a wide range of emerging and potential applications. These include defence, automotive lidar, 3D sensing for wearables and smartphones, solar cells, and medical sensing. This class of PICs could also have a role to play in quantum computing and in neuromorphic computing for AI and machine learning.

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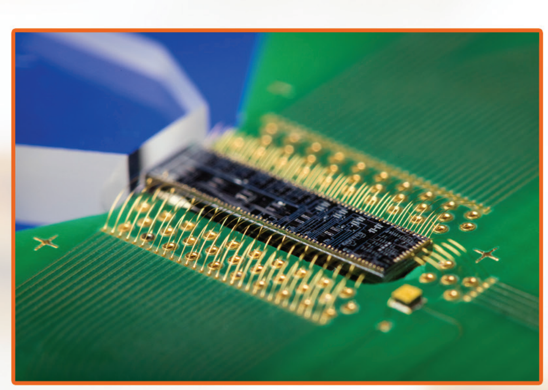

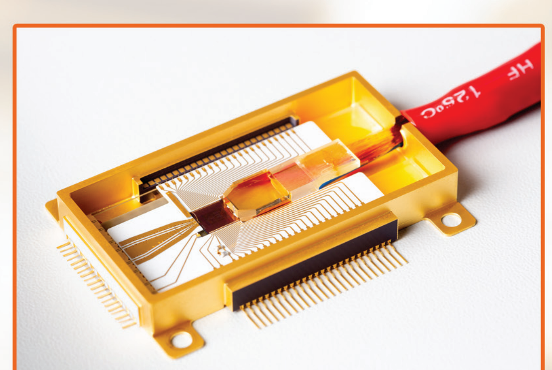

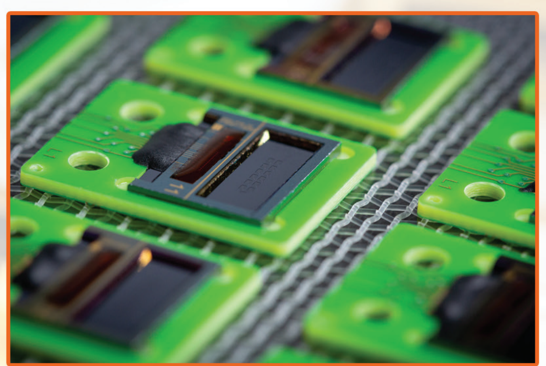

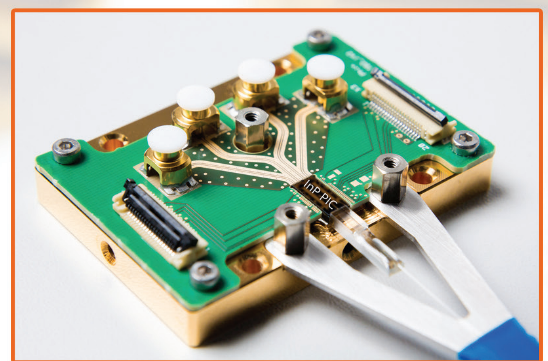

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Component viability risks bursting the quantum bubble

To speed the arrival of quantum technologies, the incredibly demanding compound semiconductor devices that lie at the heart of them need to be produced on high-volume platforms

BY DENISE POWELL AND WYN MEREDITH FROM THE COMPOUND SEMICONDUCTOR CENTRE, SAMUEL SHUTTS FROM CARDIFF UNIVERSITY, MOHAMED MISSOUS FROM THE INTEGRATED COMPOUND SEMICONDUCTORS, MOHSIN HAJI FROM THE NATIONAL PHYSICAL LABORATORY AND CHRIS MEADOWS FROM CSCONNECTED

THERE IS no doubt that quantum technologies have the potential to revolutionise every sector we can think of. Their impact will include: highly accurate navigation, enabled by quantum gyroscopes; GNSS-free communications, underpinned by atomic clocks; ultra-secure communications, via quantum key distribution; improved manufacturing control and timely maintenance on infrastructure; the detection of anomalies in organs such as the brain and heart, through quantum magnetometers, alongside rapid drug and materials discovery; and financial modelling, enabled by quantum computers.

The possibilities for quantum technologies are so vast that this revolution is anticipated to be on a par with that of AI, in terms of scale. In fact, these two headline-grabbing technologies are complementary, with the true magic underway when quantum systems are enabled by AI. This is not just fantasy:

AI is already applied to data from quantum systems at the UK's National Physical Laboratory to ensure rapid analysis.

Unfortunately, for any nascent technology, promise is no guarantee of success. History attests that when a technology with great potential delivers encouraging results, substantial investment follows – but this optimism may well be short lived, with the bubbles breaking to induce a widespread cull that leaves those hanging under the spotlight having trying to salvage a future for their revolutionary technology. Today some firms are still recovering from the lidar aftermath, and reports suggest AI is next for re-evaluation.

And what of quantum? Why aren't we seeing widespread deployment of this technology, on the back of investment totalling hundreds of millions of dollars? You might be thinking that the humble laser draws on quantum effects, so quantum is already well-embedded in our lives. That's somewhat true, but misses the point that here we are considering what most refer to as 'Quantum 2.0' – that is, technologies that utilise superposition or entanglement, or as Einstein famously said, "spooky action at a distance".

To delve deeper into the future of quantum, it's helpful to consider an example. One highly successful Quantum 2.0 product is the world's first commercially available chip-scale atomic clock, Microchip's Microsemi SA.45s CSAC. According to the National Institute of Standards (NIST), this triumph is the culmination of more than 10 years of extensive R&D, costing several tens of millions of dollars, with support from both the Defence Advanced Research Project Agency (DARPA) and NIST. John Kitching, a key researcher at NIST involved in this development, rightly suggests that given that the market for chip-scale atomic clocks is worth around $200 million per annum, it's difficult for industry to invest the amount needed for fundamental R&D in this area.

VCSELs: a hero in the making

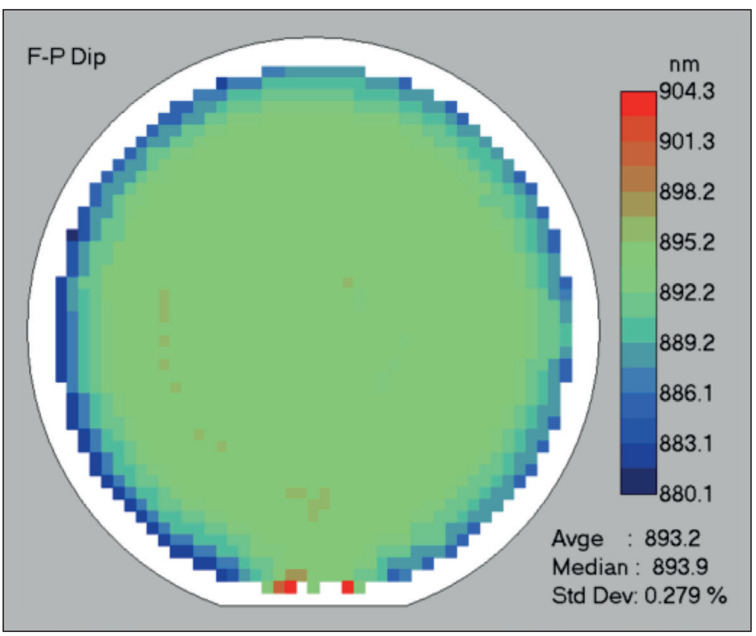
A key component in miniature atomic clocks, as well as other quantum systems based on alkali metal vapour, is the VCSEL. Renowned for its low power operation, circular beam profile and intrinsic reliability characteristics, this class of laser is ideal for interrogating the alkali metal atomic species, typically rubidium or caesium, that are contained in a small cell within the atomic clock. As the clock's principle of operation is coherent population trapping, the VCSEL must emit at highly precise wavelengths corresponding to atomic energy transitions. For example, the emission must coincide with D1 transitions at elevated temperatures, which occur at 795 nm and 894.6 nm for rubidium and caesium, respectively.

In addition to these highly stringent wavelength requirements, there are many other specifications that must be met, including single-mode operation with a narrow linewidth and high mode stability. Fulfilling them all is not easy, as in some cases adhering to one narrow tolerance makes it harder to meet the demands of another. Given this state of affairs, it's no surprise that it's not a stroll in the park to realise the high levels of epitaxial material design, growth and fabrication demanded for VCSELs deployed in quantum technologies.

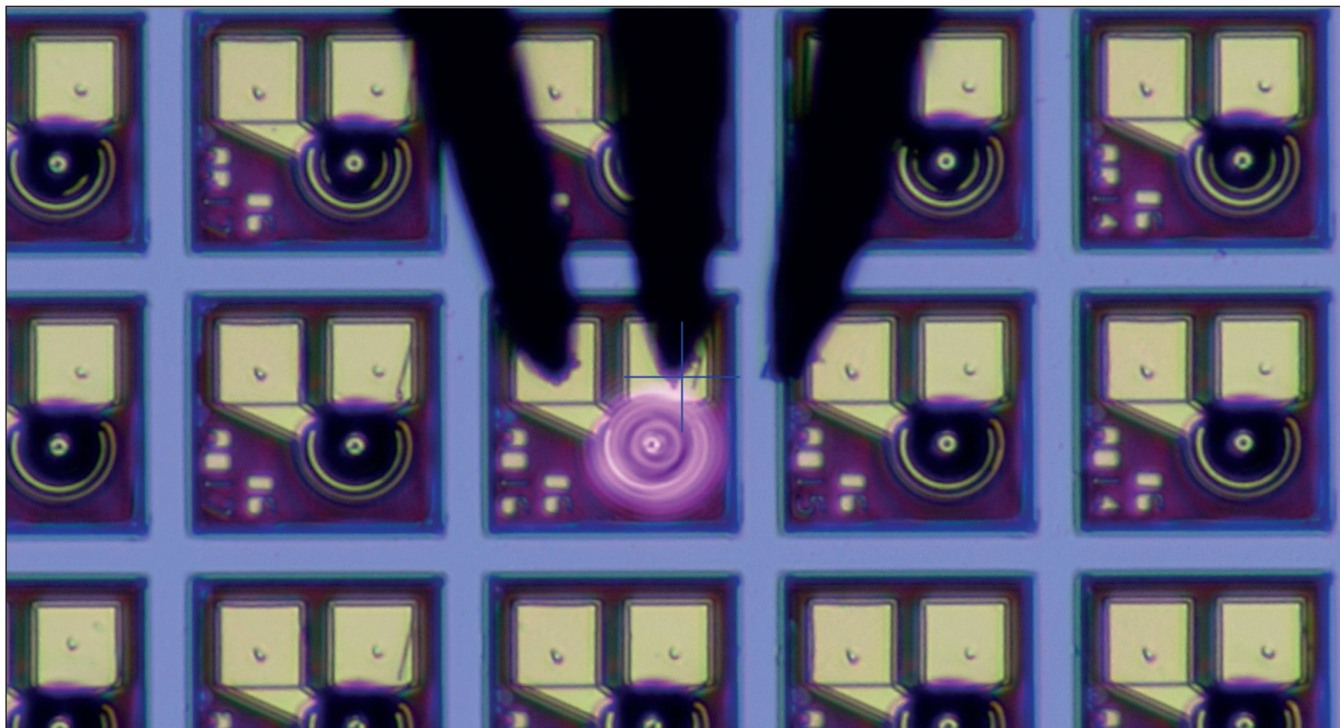
To illustrate this point, when VCSELs serve in quantum technologies, the ideal uniformity for the Fabry-Pérot dip across a wafer is below 1 nm, with the precise figure depending on the current tuning capability. In stark contrast, telecommunications applications can tolerate a non-uniformity of this parameter of several nanometres across a wafer.

There is significant effort in the UK to develop VCSEL technology that is customised to the stringent needs of quantum applications. The Compound Semiconductor Centre (CSC), a joint venture between IQE Plc and Cardiff University, has worked extensively on improving the centre-uniformity profile for 100 mm epiwafers produced with Aixtron series G3/4 MOCVD tools. This is the preferred substrate size for the VCSEL design, fabrication and test partner Integrated Compound Semiconductors, of Manchester, UK.

Fabrication is equally challenging, demanding tight control of the oxidation processes to ensure single-mode operation at the required optical output power. Naturally, these process challenges impact yield. Whilst standard VCSEL platforms boast yields typically in excess of 90 percent, those developed specifically for quantum applications are far lower, due to the cumulative effects of stringent specifications.



➤ The Fabry-Pérot profile across a 894.6 nm VCSEL structure grown on a 100 mm GaAs substrate using Aixtron G3 series MOCVD system.

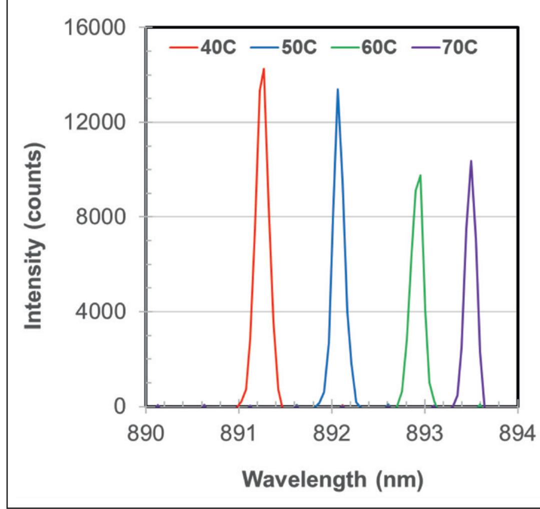


Fabricated VCSEL devices at ICS, Manchester

The hefty price tag on Quantum 2.0

Product pricing depends heavily on manufacturing yields. For VCSELs for consumer applications, many thousands of lasers can come from a 150 mm wafer, with yields typically allowing for a fully processed device to cost up to $5. That's not a feasible price-point for highly customised VCSELs for quantum applications.

VCSELs can also serve in other alkali metal vapour-based quantum systems, such as quantum magnetometers and gyroscopes, where they are again used for coherent population trapping. In all these products, other custom components are also required, such as: wafer cells to contain the alkali metal species; niche optics; crystal oscillators, in the case of atomic clocks; and shielding and/or coils, when fabricating gyroscopes and magnetometers.



Optical spectra of a single mode VCSEL fabricated at ICS, Manchester

Progress is being made on all these fronts. For example, MEMS wafer cell technologies are emerging. However, in addition to efforts at improving yield, a lot of fundamental research and development still needs to be undertaken to understand the effect of process and cell parameters on application performance.

One crucial question plaguing the quantum sector is this: What level of product mark-up is tolerable for end-users, so they don't stick to other, perhaps more proven technologies? And related to this is the question of what is the price-point at which the advantage of Quantum 2.0 is too expensive to justify? It's an unspoken reality that quantum systems will not be widely deployed until critical components are manufactured at accessible costs, unless value at the system level far outweighs the cost. You'll not be surprised to hear that defence and security are often the early adopters for emerging technologies, enabling low-volume production that provides a pipe cleaner step for a subsequent volume ramp.

Upscaling an existing asset base

The issue of manufacturability for quantum is not limited to VCSELs. There are applications requiring single-photon light sources or detectors. Producing these devices is even more challenging than VCSELs, because they are at a lower technology readiness level, having not benefited from years of volume production for non-quantum applications. Viewed in that light, it's not that surprising that miniaturised atomic clocks are one of the first quantum systems to be commercialised. The lack of maturity in the production of some types of devices, along with their high

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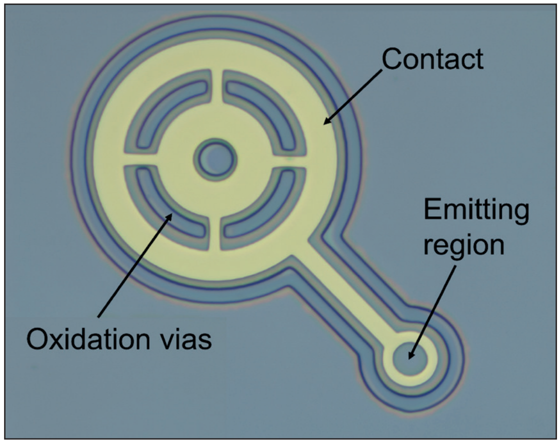

A Quick Fabrication VCSEL structure produced at Cardiff University.

manufacturing costs, creates a substantial barrier for many quantum industries, including quantum key distribution, quantum sensing and quantum computing. The solution is to manufacture quantum devices alongside other semiconductor processes, and leverage existing assets and infrastructure.

Helping to bridge that gap is a three year, £5.8 million project, part-funded by the UK Quantum Technologies Challenge under UK Research & Innovation (UKRI), that draws on existing assets and infrastructure across 12 partners in the UK.

This venture, the QFoundry project, is establishing a foundry for quantum photonic components and is focused on upscaling manufacturability of these devices and understanding drivers of yield, reproducibility and reliability. Another contributor to the progress made by CSC is through the CSconnected compound semiconductor cluster in South Wales, that is supported under UKRI Strength in Places programme and is actively involved in establishing UK supply chains for a range of quantum technologies. CSC, which has access to volume MOCVD reactors through IQE, works closely with Cardiff University who have developed a novel Quick Fabrication (QF) VCSEL process to determine the impact of material design changes or growth parameters in less than half the time it would normally take to fabricate full devices.

Those that have read Move Over MOCVD (Compound Semiconductor issue V, p. 20, 2022) Some may wonder why MBE is not the growth method of choice, given its capability to deliver superior uniformity. However, the reason is simple: MBE would cast an additional financial burden on the already high cost for custom design and fabrication of VCSELs for quantum technologies. To ensure the success of quantum, its devices must be made alongside volume platforms and create additional market opportunities for the same wafer platform.

Underscoring the importance of running quantum fabrication alongside standard volume semiconductor processes is the approach taken by the leading developer of quantum computers, PsiQuantum, which has partnered with Global Foundries. According to PsiQuantum, the only path to creating a commercially viable quantum computer is the one that leverages the trillions of dollars invested in the semiconductor industry, which now dates back more than half a century. Through collaboration with Global Foundries, PsiQuantum gains access to high-precision lithography and other high-end toolsets, as well as running design-of-experiments at volume to accelerate development.

It's a sure bet that one day quantum will be a natural part of everyday life. However, getting there involves tackling fabrication challenges, and taking sensible pathways to commercialisation and eventual volume deployment.

FURTHER READING

- C. Hentschel *et al.* "Gain measurements on VCSEL material using segmented contact technique." J. Phys. D. **56** 74003 (2023)
- J. Baker *et al.* "VCSEL quick fabrication of 894.6 nm wavelength epi-material for miniature atomic clock applications." IET Optoelectron. **17** 24 (2022)
- J. Baker *et al.* "VCSEL quick fabrication for assessment of large diameter epitaxial wafers." IEEE Photonics J. **14** 1530110 (2022)

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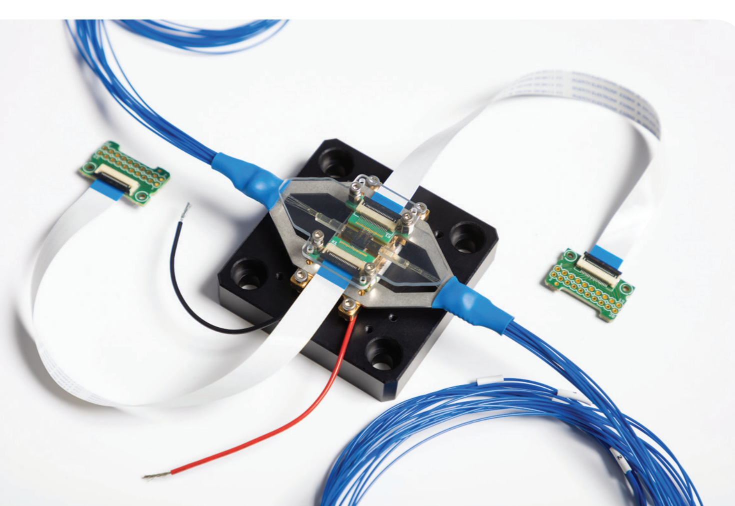
Photonic integrated circuit packaging, from prototype to production scale-up

Packaging photonic integrated circuits (PICs) can be complicated and expensive, but using standardized components and automated assembly processes in the testing and development stages can significantly reduce costs and improve the final product

BY GIJS VAN OUWERKERK, MARKETING AND COMMUNICATION SPECIALIST, PHIX PHOTONICS ASSEMBLY

PACKAGING photonic integrated circuits (PICs) into functional optoelectronic devices is often complex and costly. Bringing together optical and electrical interfacing, thermal management, mechanical support and sometimes even chemical sealing, PIC packaging requires a multi-disciplinary team of experts. On top of that, standardization within the industry is lacking at the front-end, where many different PIC material platforms exist that often need to be co-packaged to combine their strengths.

These factors mean that packaging can swallow a large share of the total costs of PIC-based optoelectronic module development. But there is also an opportunity here: cost savings in this area will have a large positive effect on total expenses. This article will discuss an approach to PIC packaging that minimizes costs and maximizes performance of the end product by considering product design, manufacturing equipment sourcing and process development in parallel and at a system design level.



PIC characterization package with fibre arrays, electrical fan-outs and a thermoelectric cooling solution.

As the PIC-based optoelectronic device matures from its prototyping phase towards a product manufactured in volume, it is inevitable that the design of the PIC and its surrounding module will go through a series of transformations. Paradoxically, the article will show that designing effectively for volume production actually means starting with a prototype package. Even when manufacturing volumes are low at first, automated assembly can play a key role in keeping the cost down.

The need for prototype packaging

The first step in the development of a PIC-based device is to perform characterization of the first manufactured chips, often produced on multi-project wafers (MPWs). The designer could be interested in measuring variations between dies, fine-tuning waveguide tapers, or comparing different chip designs with each other. Although this can be done by connecting electrical and optical probes to the bare die, there are severe downsides to this. First, the temporary optical interfaces obtained in this way are not stable, so the data about the performance of the chip is polluted by the fluctuating performance of the interface. Secondly, environmental temperature changes also affect the chip's properties and introduce additional performance fluctuations.

To drastically reduce these variations, using a simple open architecture prototype package makes a lot of sense. Here, the electrical connections are wire bonded out to simple printed circuit boards (PCBs), the optical signals are coupled to fibre arrays secured with index matching epoxy and stress reliefs, and a thermal management system is installed.

Temperature management can be passive, with a large copper mount acting as a heatsink, or active, by using a thermoelectric cooler (TEC) in combination with a TEC controller and thermistor

fitted inside the copper mount. This module is suitable not only for PIC characterization, but also for device characterization and system integration, enabling demonstrations outside of a laboratory environment. Since the device prototyping phase usually involves multiple design iterations of the chip and/or module, each requiring new packaging, it's important to keep packaging costs and turnaround times as low as possible.

The way to do this is to work with standardized off-the-shelf packaging building blocks and standardized automated assembly processes as much as possible. This avoids custom package design, parts, equipment, tooling and (manual) processes. Custom packaging of small series is difficult to automate, expensive, time-consuming, carries more risk, and may involve parts for which there is a minimum order quantity (MOQ). It should be put off for as long as possible, until the PIC design is ready for assembly into qualification modules in higher volumes.

How to minimize prototyping time and costs

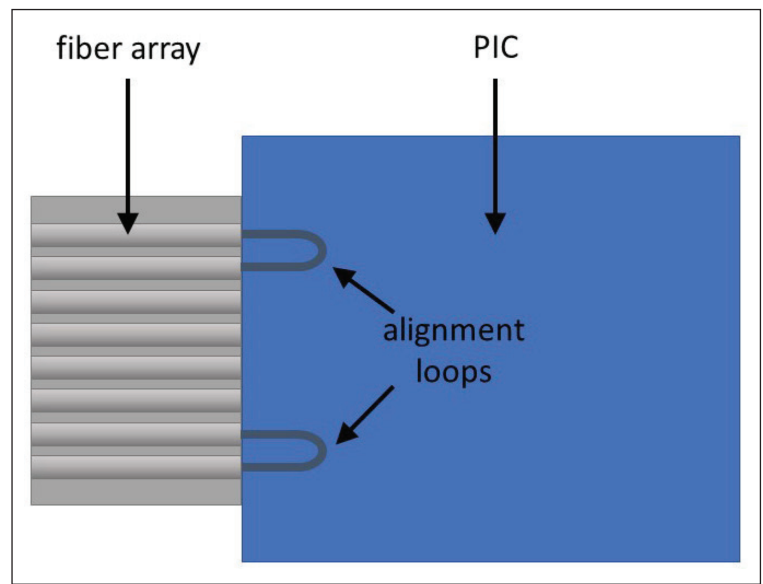
There are several ways to design the PIC to work with standardized building blocks and production processes for easy prototyping. For example, PHIX has developed prototype packaging solutions that use waveguide alignment loops, electrical bond pad pitches compatible with standard PCBs, and the packaging foundry's standard housings and accessories.

Waveguide alignment loops

Waveguide alignment loops are extra waveguides, not used as part of the functional structures on the PIC, that enable active alignment during the assembly of the optical interface, particularly the attachment of fibre arrays. Active alignment achieves the best possible coupling efficiency for optical assembly processes in prototype PIC packaging. Crucially, the presence of waveguide alignment loops allows the packaging foundry to use standardized and automated alignment routines involving calibrated light sources and detectors.

Performing active alignment without these loops would mean using probes to activate the functionality of the PIC, for example, by driving gain elements and measuring photodiode currents. These probes are chip-specific and therefore would need to be custom-designed and manufactured for each project, requiring non-recurring engineering (NRE) with added development time and cost. Furthermore, using the functional structures on the PIC as part of alignment routines pollutes the assembly performance data with the product performance data, making this method of process control monitoring less reliable.

Although waveguide alignment loops occupy some space on the PIC and require additional fibres, they compensate for this added cost by making the manufacturing process during the prototyping packaging phase much more affordable and reliable.

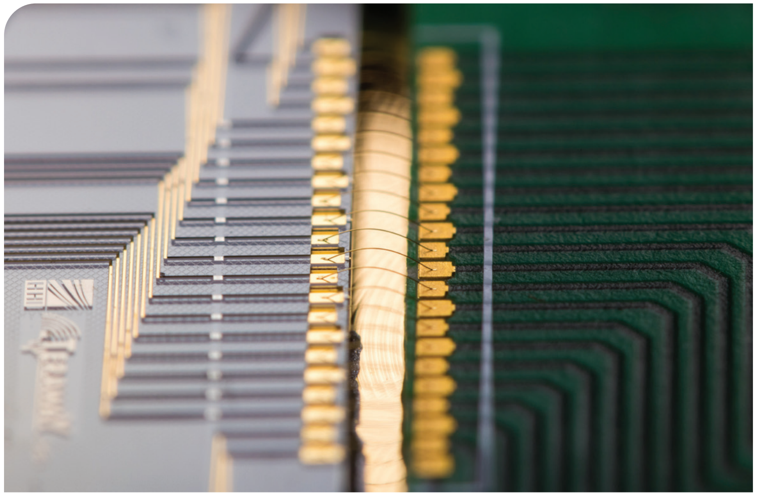


Waveguide alignment loops in a PIC to aid edge coupling of a fibre array.

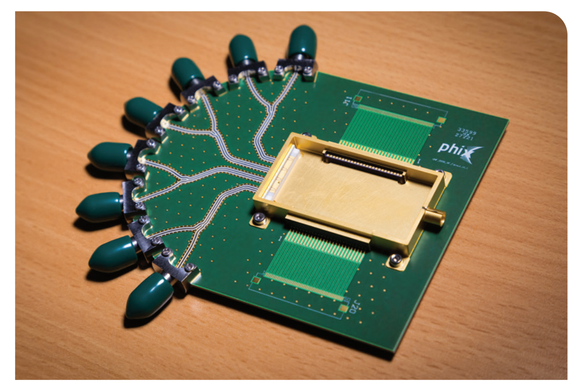
Bond pad pitches compatible with standard PCBs

In PIC prototype packaging, where making flip chip electrical connections using redistribution layers and land or ball grid arrays (LGAs or BGAs) is not yet feasible, it's common to place direct current (DC) bond pads near the edges of the PIC and wire bond out to the neighbouring PCB or housing. Due to the high accuracy of the lithographic etching processes of PIC foundries and the desire to make PICs as small as possible, there is a tendency to place these bond pads very close to each other on the PIC surface. Such small bond pad pitches, however, can be detrimental to achieving low costs and short lead times in prototype packaging.

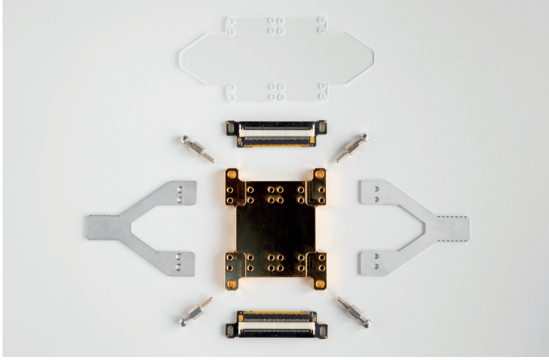
The reason for this is incompatibility between the PICs and standard PCBs. To prevent wire bonds from shorting or sagging, they need to be as short and as parallel as possible. Ideally, they should cross



Wire bonds crossing over straight and parallel from a PIC to a PCB.



A standard fan-out solution for a large area goldbox module, providing DC and RF connections.



4) Building blocks of a standard PIC packaging housing, with copper mount, fibre array strain reliefs, and standard PCBs.

straight over from the PIC to the PCB, so the bond pad pitch on the PIC needs to match that on the PCB. But, since most standard PCB suppliers only support pitches down to 200 µm, while pitches on PICs are sometimes chosen to be as small as 70 µm, there can be problematic mismatches.

A packaging foundry can deal with small bond pad pitches on the PIC by choosing thin film ceramic or organic interposers from specialized suppliers, or by using staggered vias for distributing the signals to different layers of the PCB. However, these solutions are very costly due to the NRE and expensive components they require. Furthermore, they make process automation much more difficult. Instead, choosing a sufficiently large bond pad pitch on the PIC during the packaging prototyping phase can ensure compatibility with standard low-cost PCBs, significantly reducing the cost and lead time of the prototype packages.

Using standard packaging solutions

Another way to reduce the level of customization involved in creating a PIC package is to make use of standardized packaging solutions. PHIX offers solutions that consist of standard off-the-shelf building blocks, but still provide flexibility and design freedom. This approach allows the packaging foundry to leverage previous engineering efforts and keep standard parts in stock, thus eliminating the problem of minimum order quantities. This method also allows for the use of standardized (semi-)automated assembly processes, ensuring a cost-effective prototyping phase with short lead times.

Butterfly and goldbox housings have many of the same advantages, but they require custom interiors. They are worth considering if radio frequency (RF) electrical signals are used. Besides prototyping they are also suitable for qualification packages in higher production volumes. Standard electrical fan-out solutions offered by packaging foundries allow convenient connectivity for device characterization and system integration tests.

Design at system level

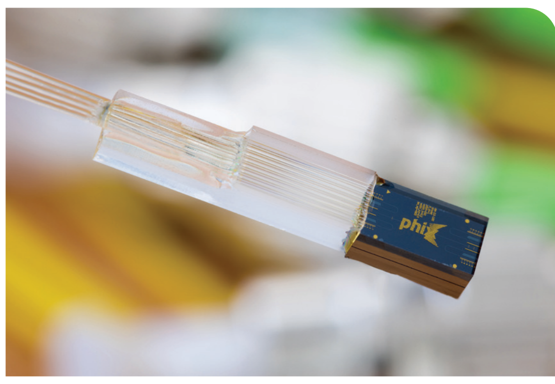
Designing a PIC based optoelectronic module is a multidisciplinary activity where PIC and module design must be in harmony with process development and manufacturing equipment. PIC packaging therefore needs to be approached with an eagle eye view of the system, where product performance is weighed with cost and ease of scale-up.

The use of waveguide alignment loops and the choice of a DC bond pad pitch compatible with wire bonding to standard PCBs are good examples of this system-level approach. Some other areas of PIC design that require attention in this regard include mode field matching and power budget.

Mode field matching

Significant optical losses can be caused by mode field mismatches between optical components being assembled. This is of particular concern when edge coupling fibre arrays (with typical mode fields of 10 µm) to PIC waveguides (with mode fields that can be as low as 1 µm). The best coupling performance is obtained if the mode fields of the two components match as closely as possible at the interface. In addition, the mode fields at the interface should be as large as possible, to reduce the influence of manufacturing tolerances on the coupling losses.

Traditional solutions for mode field matching between optical fibres and PICs involve lensed or tapered fibres with high numerical apertures. This approach works well for single fibre attachments but, when applied to multichannel fibre arrays, it poses significant alignment challenges and makes the assembly process difficult to automate. As dense PICs with high channel counts become the norm, these individual fibre treatments are quickly becoming obsolete for mode field matching.



Multi-channel spot size converter attached to a fibre array.

Spot size converters (SSCs), on the other hand, are mode field matching solutions that scale well with channel count. They are waveguide tapers that resize and/or reshape the mode field near the optical coupling interface. SSCs perform best and are most cost-effective when they are a functional building block on the PIC itself. The availability of on-chip SSCs depends on the PIC platform and whether or not the PIC foundry supports it. If an on-chip SSC is not available or if it does not eliminate the entire mode field mismatch, then the packaging foundry may offer other solutions, such as off-chip SSCs pre-attached to a fibre array. These are typically made from ion-exchanged glass or silicon nitride and have lithographically defined tapered waveguides. They can be attached to fibre arrays using automated active alignment processes, even in small volumes.

Power budgeting

Another example of good system-level design is to consider the power budget for each component or interface in the package. It's very difficult to avoid introducing small losses in many places in the design, starting at the optical structures on the chip and moving through all the components and interfaces. These losses should be considered in the context of the whole system, in order to choose the right components and assembly processes needed for the desired functionality and performance.

Packaging foundries are capable of assembling components at high accuracies and with minimal losses, but the engineering, processes and equipment this requires come at a cost and may be difficult to scale to volume production. For certain PIC applications, such as in quantum or astrophotonics markets, where every decibel of loss matters and manufacturing volumes are relatively low, the higher costs of top-quality interfaces may be acceptable.

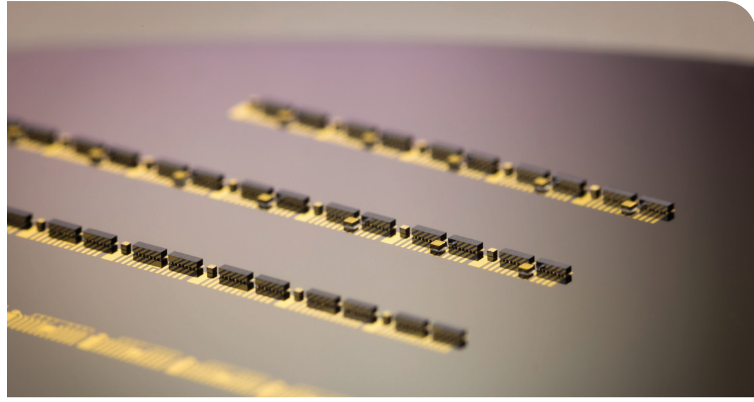
However, if the device is intended to scale to high volumes, it is important to add some margin to the power budget in order to relax assembly constraints and allow a more affordable and scalable automated manufacturing process. A sufficient power margin gives the packaging foundry some freedom to design for manufacturability and cost-effectiveness, rather than having to focus purely on achieving maximum performance.
The PIC designer should be aware that, besides mode field matching and power budgeting, there are many other recommended design practices that favour manufacturability and cost-effective scaling. It is recommended that designers get in touch with a packaging foundry early and benefit from their experience.

The road to volume production

The previous sections described a cost-effective iterative prototyping phase for the PIC and the device, with fast turnaround times. Having approached the design of the PIC-based module at system level, the full playing field of design parameters has come into view.

The next phase in the volume scale-up is to develop a qualification package that is optimized for consistent performance and low cost per unit. At this stage it starts to make sense for the packaging foundry to make investments in custom parts, tooling, processes, and perhaps even equipment. Since the structures on the PIC now have a stable and well-known performance, they can be used for active alignment routines that no longer require waveguide alignment loops and extra fibres.
Flip chip assembly of electrical components may become a feasible alternative to wire bonding, because it will become possible at wafer level instead of at chip level. These considerations can now lead to a minimization of chip area without compromising the assembly processes or performance.

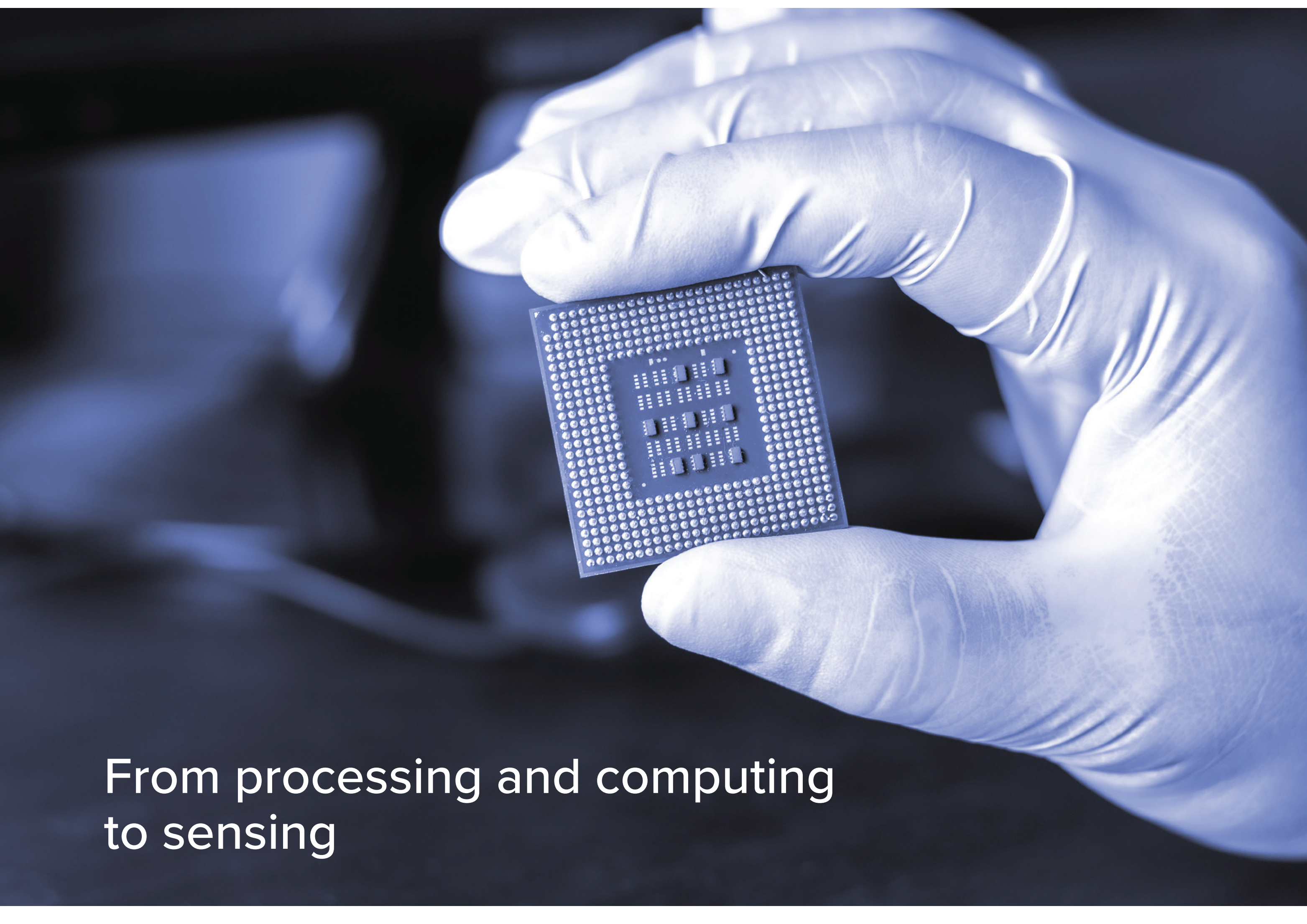
The qualification package and its contents may require sealing and be subject to reliability testing and yield optimization. Once the PIC design is frozen, the final volume package can be defined. Then, if the manufacturing volumes are sufficiently high, the packaging foundry can transition from batch level automation to the deployment of a dedicated, fully automated production line for the product.



➤ Flip chip assembly of electronic components onto silicon nitride at wafer level.

Conclusion

Navigating towards volume packaging of an optoelectronic device in the quickest and most cost-effective way revolves around two main principles. Firstly, the PIC design should be approached at a system level, considering all aspects of the optoelectronic module and its manufacturing. Secondly, the PIC design and its packaging should be adapted to the state of maturity of the product, putting off the use of customized design, components, and processes for as long as possible. This approach requires the PIC designer and the packaging foundry to work closely together. The PIC designer should seek out this collaboration as early as possible in the design process. It's the responsibility of the foundry, on the other hand, to offer multidisciplinary engineering support to promote PIC designs that are optimized for cost-effective packaging, and to assist in a smooth scale-up from prototype to automated volume manufacturing.



From processing and computing to sensing

The recent CEA-Leti Innovation Days provided a great opportunity to learn about some of the very latest developments and research being undertaken in the semiconductor industry, covering such topics as quantum computing, sustainable electronics, cybersecurity and memory for edge computing. There was a dedicated session on Photonics: Data and Sensing, which looked at photonics for computing and communications as well as integrated photonics for biomedical and chemical sensing applications.

ELÉONORE HARDY, BUSINESS DEVELOPER AT CEA-LETI, co-chaired the workshop and here she provides an overview of the topics and technologies discussed, in conversation with Philip Alsop, contributing editor to PIC Magazine.

FROM 27 -29 June, the French technology research institute CEA-Leti held its Innovation Days – an annual three-day conference that brings together technology leaders from around the world to share their latest and most exciting developments. This year's event hosted a dedicated photonics workshop called "From Processing and Computing to Sensing

PA: *At the recent CEA-Leti Innovation Days, there was a workshop on photonics, which you co-chaired. Could you tell me a bit about how the day went?*

EH: This workshop went really smoothly. I was particularly happy with the attendance. In the morning, we had a session dedicated to communications and computing applications for photonics, and in the afternoon, we were really focusing on sensing applications. We could not cover everything in one day, but we had very interesting talks with people from both industry and research. What I found really nice about this session was seeing the different points of view of our different speakers. Some speakers, like STMicroelectronics (ST), were giving foundry

perspectives, and Hewlett Packard Enterprise (HPE), for example, was giving a system perspective on photonics, so it was a very rich discussion. We also had panel discussions at the end of each session to have questions from the audience to our speakers.

PA: *The headline talk was "Photonics 2.0 and Applications." I'm sure that is quite a big topic, but can you give us some flavour of that high level overview of photonics? What did you cover?*

EH: The aim was to start the session with a really broad overview of photonics and its applications. We gave the mic to Frederic Boeuf, who is the technical director of technology R&D for photonics at ST. He gave a vision of the possibilities given by silicon photonics platforms for different applications. He covered, of course, datacom applications, because this is really what we are facing today: a big amount of silicon photonics really going into all parts of the data centres, not only for interconnects between servers, but also between data centres, and now coming closer and closer to the chip. He talked about the applications for quantum communications and quantum computing, biosensing, LiDAR chips for the automotive industry, high performance computing (HPC) and also depth sensing. These can all really be pushed forward thanks to silicon photonics. Then he also gave an overview of what ST's photonics platform can do for those applications, in particular for communications, the advantages of this platform and also what would be the next step for it.

At the end, he reviewed one very interesting point, which is the need for more advanced modulators for HPC, for communication, and for many applications. He compared different versions of modulators we can see today in papers, from very classical ones to more advanced ones. He also discussed at the very end how to integrate new materials in this platform, because we know silicon is not enough. We also need to have other materials brought into the platform, like III-V materials, of course, for lasers. But there are other integrations that are really interesting, like InGaAsP materials, and also BTO and lithium niobate. So it was a very good start for the morning.

PA: *Just to pick up on something, it's been suggested that photonics has quite an exciting future, particularly when it comes to energy efficiency. Was there any discussion during the day of how much of an impact photonics can make when it comes to energy efficiency?*

EH: During the Innovation Days, we had a very specific session on sustainability. Energy consumption is in everyone's mind, and in photonics, as well, we have this in mind. It's important to find a way to decrease the consumption of data centres, and yes, photonics can help greatly in this change. But also looking at computing, when you talk about AI and all the needs for these new AI systems, you see that the energy consumption is incredibly high. We had a talk from Thomas Van Vaerenbergh from HPE about how photonics can help, from the interconnects to the core of the computing processors. He gave a view of the energy consumption of those processors and how photonics could really help decrease the consumption of those new computing architectures.

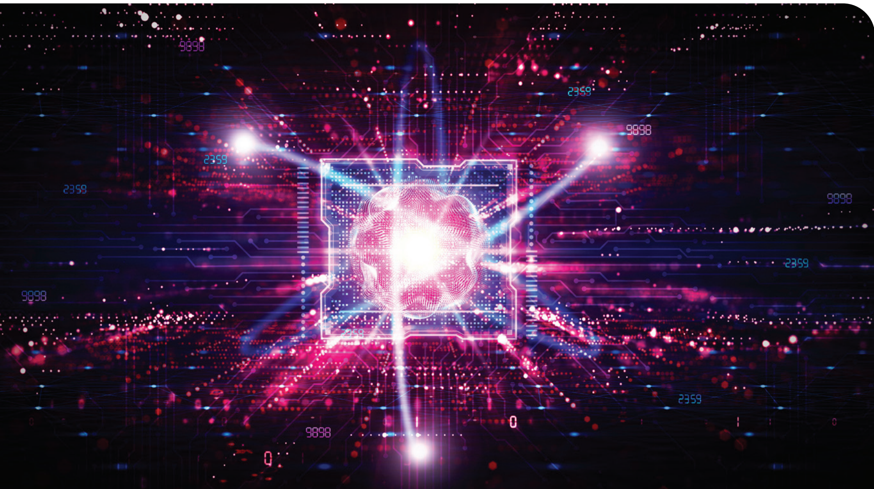
PA: *The next presentation was to do with interposer optical communications. Could you give us a flavour of what was covered?*

EH: This talk was given by Yvain Thonnart from CEA-List, who has been working on computing architectures for years. He's one of our best experts in the field, and so he really showed us how there is a big need for interposers, for HPC in particular, and why basic silicon interposers will not be enough for many reasons, like latency and energy consumption. He showed us how we could move from silicon interposers to active silicon photonics interposers that could really help in reducing the latency and the energy consumption of those architectures, by having denser on-chip interconnects with lower latency routing.

What he wanted to show is that photonics really can help scale out the interposers, allowing a routing with very low latency and low power. We have made a proof of concept of this at CEA-Leti. We are doing the tests currently, which shows this is something we can do for real and we can scale into production in the coming years.

PA: *The next topic for discussion was photonic neuromorphic accelerators. Could you tell us a bit about that presentation?*

EH: This presentation was made by Thomas van Vaerenbergh from HPE, who has been working on photonics for years, but also electronics. He worked on a road for optical HPC interconnects, but also on new architectures based on neuromorphic accelerators. This is a very different way to think about the next generation of accelerators.



Nowadays we are focusing more on digital computing, but analogue computing is also a very interesting possibility for the future, to reduce once again the energy consumption. Thomas gave us a flavour of what photonics can do for digital computing, and also for analogue computing. He showed us the great performances that can allow photonics for machine learning accelerators.

The maturity level is still very low today for that, but we are talking about what could be next in ten years from now. And we need to prepare it today, so it was very exciting from this point of view. Thomas also tried to highlight the need for a better structure for the photonics community, to have people really able to understand each other and to have a full supply chain ready to scale up this technology.

PA: *Next there was a talk about CEA-Leti's own silicon photonics platform, so it would be good to understand what that is and where that fits within the photonics landscape?*

EH: We have had a silicon photonics platform at CEA-Leti for nearly 20 years now, so we started very early in those developments. For years we worked on an 8" silicon photonics platform, which was standard. But a few years ago we moved to a 12" silicon photonics platform for many reasons, because we saw that big foundries like ST, for example, are in 12". We need to be compatible with those very performant platforms to bring the technology for those 12" volume foundries. Also, in 12" usually you have better silicon-on-insulator (SOI) uniformity, so a better yield at the end. And you can also take advantage of immersion lithography in 12", meaning that you can go to smaller feature sizes. The smallest feature size we usually do in 12" is around 40-60 nm for our projects. That is much better than what you can get with an 8" platform. So we developed a standard silicon photonics platform that is aimed at developing new technologies for photonics, bringing in new materials, like III-V, of course. We have worked on collective die-to-wafer bonding of III-V materials for lasers and semiconductor optical amplifiers (SOAs) for years. We launched a startup company a few years ago, Scintil Photonics. And we also work on new materials like NbN, which is a superconductive material, which is very useful when you look at SNSPDs, or single-photon detectors needed for quantum applications. We also integrate lithium niobates nowadays by bonding, and we also work on BTO integration with Lumiphase in Switzerland. So we have a very versatile platform. This is a good field for us to work on new materials and new integrations, to find the perfect new components for the future, to then transfer them to volume foundries.

PA: *Picking up on that point, the morning ended with a panel discussion about the likely or the predicted impact of photonics. Everyone will have their own view as to where and how and when, but can you give us a flavour of that discussion and maybe even your own thoughts as to where it's going to show the most or the quickest return, or just how the landscape might be developing?*

EH: We had a very fruitful panel discussion. I would say what remains very important is datacom is still mainstream today for photonics, no question about it. But we have been seeing, of course, for years, a big trend to explore new applications. When you work on a photonics platform, usually you can cover more than one application with the same platform, so the versatility of silicon photonics is interesting for exploring new applications.

The morning was really focused on the advantages for computing. A highlight in the panel session was that photonics is getting closer to the cores. That's a reality because of low latency and low power consumption again. But there is also a need to really look at photonics for a new style, a new way of computing, which Thomas from HPE spoke about in his talk on analogue computing and Benoît Charbonnier, researcher at CEA-Leti, in his talk on Neuromorphic photonics for tomorrow's AI. For sure, photonics is also a big enabler for AI for the future, so that was a perspective we had during this panel session.

Also, when looking at material integration and foundry perspectives, working only with silicon or silicon nitride is not enough. All foundries need to look at the best integrations of materials like lithium niobate, BTO, III-V materials. This is a big challenge for future developments.

PA: *The afternoon moved more to the sensors side of things. One of the first talks was about miniaturisation of mid-IR sensors. Could you talk through what happened there?*

EH: This talk was given by Badhise Ben Bakir, a research engineer at CEA-Leti and he focused on quantum cascade lasers and the miniaturisation of mid-IR sensors. We have demonstrated very nice sensors in the past, and we are working on the next

generations, integrating even further those sensors. The talk gave a flavour of how we work on the integration of III-V on silicon for quantum cascade lasers, especially for multigas sensors based on different technologies, such as photoacoustic detections, but also photonic integrated circuits and the QCL quantum cascade lasers integration, so Badhise talked about chemical sensing. What is really nice with photonics is that you can miniaturise the devices, but you can also target very performant devices, so this is perfect for the next generation of gas sensors. At the end he gave a view of the possibilities in mid-IR for other applications as well. He showed how we can handle the integration of III-V on silicon and the results of our quantum cascade lasers.

He also talked about the work we do in the IRT Nanoelec Consortium, which is a French consortium. We have a photonics programme with Siemens, STMicroelectronics, Almae and CNRS, so he talked about this consortium and how we developed the hybridization of III-V and silicon for new functionalities.

PA: *The next talk was to do with wearables, like non-invasive biomolecule sensors. I'm intrigued about what's going on with that these days?*

EH: We were very lucky to have Hélène Lefebvre, CEO of the startup ECLYPIA. ECLYPIA was in stealth mode for two years, and last May they decided to share their developments during Medi'nov, a conference and show in Lyon about medical developments. ECLYPIA is a startup company bringing a new generation of non-invasive continuous glucose monitoring. The developments they are making are really going to change the lives of people with diabetes. Hélène presented their latest developments and we were very lucky to have them for this session.

PA: *Am I right in thinking Admir is another startup company that shared what they're doing technology-wise?*

EH: Admir is a young startup spinoff of CEA-Leti and Laurent Duraffourg, the CEO, came to present their multispectral spectroscopic lensless imaging system. This is a brilliant system they are developing and once again it is very useful for people's health because it's a system that you can use for ultrafast cancer diagnostics. Laurent introduced the concept of how the technology

works, not only for the detection of cancer, but also for microbiology applications like the analysis of water or food to detect bacteria, and also the detection of microplastics in water. So these are very important topics as well for our future. The talk introduced the technology, the possibilities for those different applications and how they are developing this, thanks to the collaboration of doctors they are working with. Once again, it was a mid-IR photonic platform that is used for those developments. This is really the link between all the talks we had in the afternoon: how those mid-IR photonic platforms can help for medical applications.

PA: *The final technical presentation before the panel discussion was to do with Mach-Zehnder interferometers. Please tell us what that was all about.*

EH: This presentation was by Loïc Laplatine, who is a researcher at CEA-Leti. We have this very nice silicon nitride platform we have been developing for years, and based on that there were developments based on Mach-Zehnder interferometers for biosensing and olfactometry. In fact, we have a startup company called Aryballe that was mentioned during this talk. Loïc showed the results of Aryballe's NeOse products for odour analysis. This is quite incredible, but thanks to a photonic chip, you can have analysis of the odours around you and you can find applications for this in many different areas. It can be, of course, for the perfume industry, but also for the food industry and even the automotive industry. When you rent cars, you need to make sure that the car you are renting will have a nice odour in it. So we had this presentation from Loïc to show how it works, how we make those chips and the functionalisation of those chips. He showed how we work with the microfluidic integration as well,

Once again, it was a mid-IR photonic platform that is used for those developments. This is really the link between all the talks we had in the afternoon: how those mid-IR photonic platforms can help for medical applications

because the chip itself is not enough; once you have your photonic chip, you also need to have the electronics and the microfluidic system to have the flow of gas going around. At the end, Loïc showed the applications for biosensing based on photonic integrated circuits with VCSELs as the light source. It could also be used in environmental sensing and monitoring, to detect bacteria in rivers, for example.

PA: *From what you've said, it sounds as if there's plenty of work already going on in sensing applications, but it can be a time consuming process meeting regulatory requirements and/or to gain the trust of the users?*

EH: This is a big challenge for biomedical applications, because you need to take the time to go through all the regulations and this is a long process. Those startup companies are really doing a great job in this industry, but you need to also be patient to go through all the steps to qualify. You also need to go through some steps to convince end users that the new devices are reliable, and to show patients and doctors that the equipment is bringing a plus to their life. So, yes, they discussed the challenges faced by startups for biomedical applications.

PA: *If you had to choose one or two things to take away from the day, anything that brought you up short and made you feel "wow, that's amazing," or "I didn't know that," what would they be?*

EH: That's a very tough question. I would say from the morning session, my takeaway is that we are getting more and more mature silicon photonics platforms, which is very good news, because now more and more companies can start really to put their hands on those platforms, to develop new circuits and new solutions. But there are still lots of challenges for new material integration, which is good news. We still have work to do.

My takeaway from the afternoon would be: "wow, how fantastic our world can be thanks to photonics for medical applications." I saw in the presentation from Admir how much time you can save for cancer diagnostics, and in the presentation from Hélène from ECLYPIA how you can really change the life of millions, billions of people on Earth, thanks to nice, accurate sensors that you can handle discreetly in your watch, for example. We are bringing huge contributions to our future, so this is very exciting for people working in photonics to see we are doing something very useful.

It's been pleasure to chat to you and thank you so much for bringing alive the workshop in the way you have.

My pleasure. Thank you and see you next year at the next Leti Innovation Days.

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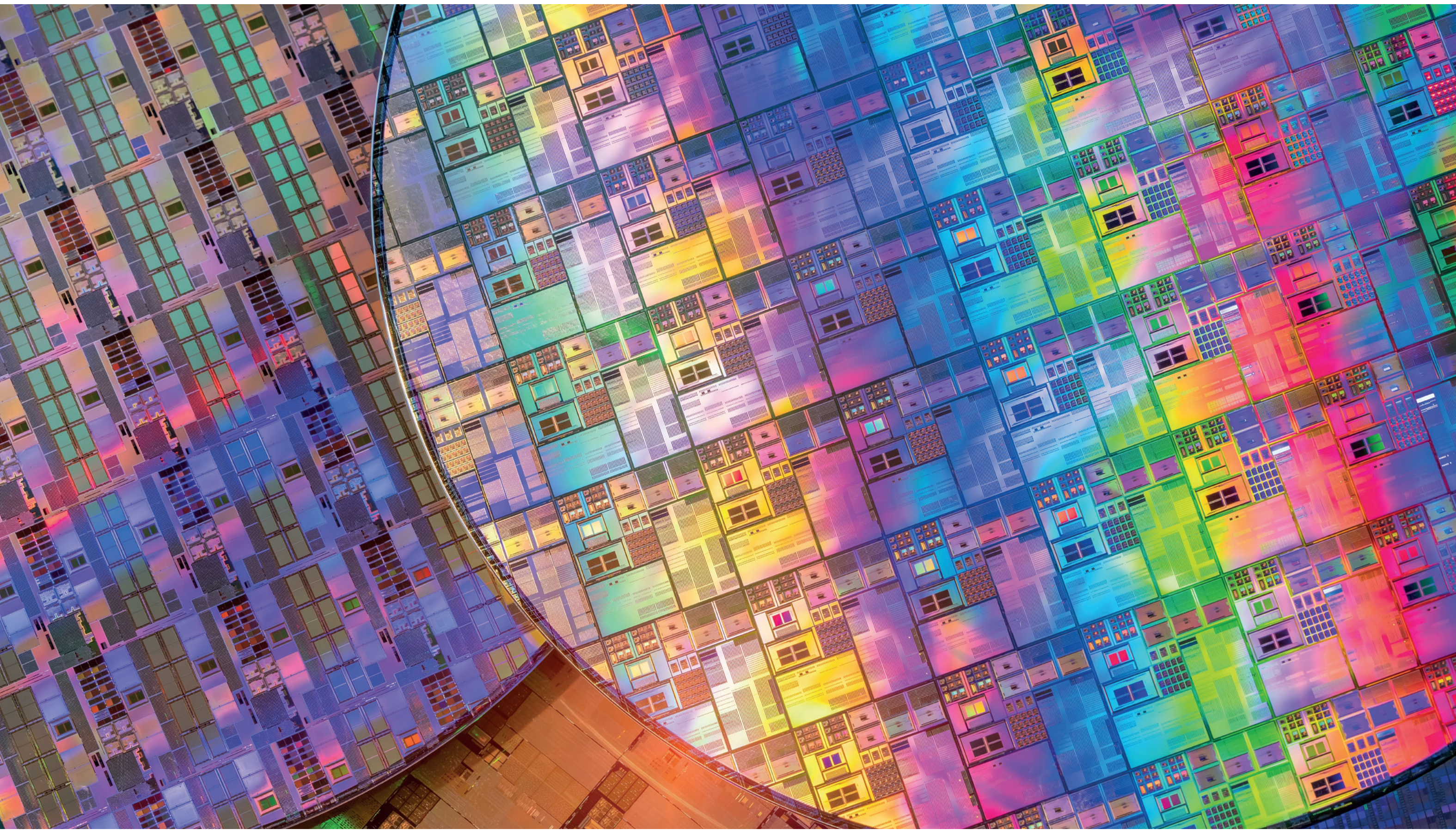

Broadband PICs with 3 µm SOI technology

Micrometer-scale silicon waveguides enable ultra-broadband PICs with low coupling losses

BY TIMO AALTO, VTT TECHNICAL RESEARCH CENTRE OF FINLAND

BASED ON PHOTONICS TEXTBOOKS, many would say that an optical waveguide with 3 µm thick silicon core is highly multi-moded, requires >>1 mm bending radius and suffers from strong back-reflections at input/output facets. In other words, such micrometer-scale silicon waveguides would not be suitable for making dense photonic integrated circuits (PICs). By thinking beyond the obvious, all these assumptions have been proven wrong, and the 3 µm thick silicon-on-insulator (SOI) waveguide technology has been used to demonstrate compact PICs with ultra-broadband, polarization independent low-loss operation (Figure. 1).

The development and commercialization of silicon photonics has taken huge steps in the past 10 years. Most of the work has been done with sub-micrometer waveguides, typically 220-300 nm thick, which can be processed in CMOS foundries that have been built for the production of electronic integrated circuits (EICs). This enables easy scaling to large-volume production without the need to invest into new foundries. Another advantage of the "thin-SOI" waveguides is that they comply with the photonics textbooks in terms of single-mode (SM) operation and small bending radii. Grating couplers and inverse tapers also allow to couple light in/out without significant back-reflections. The term "high-confinement" is often used to describe the ability to confine light into small mode-field areas with the help of the large refractive index contrast between silicon and silicon dioxide.

However, for a single-mode 220 nm SOI waveguide, the relative confinement of the fundamental mode's optical power into the Si core is approximately the same as in a standard single mode fiber (SMF). This is because the design of a SM waveguide is normally based on adjusting the size of the rectangular core to achieve SM operation with the used refractive index contrast. For a 220 x 500 nm SOI waveguide the confinement at

1550 nm wavelength is ~76 % for the horizontal (TE) polarization and ~43 % for the vertical (TM) polarization, while it is ~73% for a SMF. Because of the large geometrical birefringence, the thin SOI waveguides are typically used with one polarization only.

In a 3 µm thick SOI waveguide the cross-section area of the fundamental mode is naturally larger, but the relative confinement of the mode inside the waveguide core is much higher (99.96% for both TE and TM). This ultra-high mode confinement leads to many exceptional waveguide properties.

Firstly, the 3 µm SOI waveguides become quite insensitive to variations in the waveguide dimensions and wavelength. The effective index of the fundamental mode remains very close to the refractive index of bulk silicon even if the waveguide width or height is changed by a few %. This leads to small phase errors in the PICs and allows to realize e.g. optical phased arrays (OPAs) and cascaded interferometers without phase modulators and complex electrical control circuits.

The mode confinement remains high even if the wavelength is doubled (Figure. 2). This means that the same 3 µm SOI waveguide works well from 1.2 µm (lower limit from the energy gap of Si) to >3 µm wavelength where the absorption of the silicon dioxide cladding starts to become a limitation. High confinement actually helps to push further the upper wavelength limit since only a small fraction of the light propagates in the absorbing SiO_2 cladding even at 3 µm wavelength. By replacing SiO_2 with some other cladding material it is possible to further extend the wavelength range to ~6 µm where multi-phonon absorption starts to become a limiting factor.

Secondly, ultra-high mode confinement enables polarization-independent operation (Figure. 2). With an approximately square waveguide cross-section it is possible to have exactly zero-birefringence operation, and the birefringence remains small for other waveguide shapes as well. This opens up the possibility to make polarization independent and dual-polarization PICs with 3 µm SOI waveguides.

Thirdly, the ultra-high mode confinement leads to very low propagation losses. Between 1.2 and 3 µm wavelengths, the waveguide absorption is negligible and the propagation loss comes from mode field scattering at the dry-etched waveguide side-walls. This scattering loss depends on the overlap of the mode field with the roughness on the waveguide side-wall, which is extremely small in the 3 µm SOI waveguides. By replacing thermal oxidation with hydrogen annealing (Figure. 3), the side-wall roughness has been reduced to a few nm, which leads to a few dB propagation loss per meter. In meter-long waveguide spirals the propagation loss has been demonstrated to be ~4 dB/m, which includes the bending losses. In race-track ring resonators the intrinsic quality (Q) factors have reached >10 million, which corresponds to propagation losses <3 dB/m inside the ring [1]

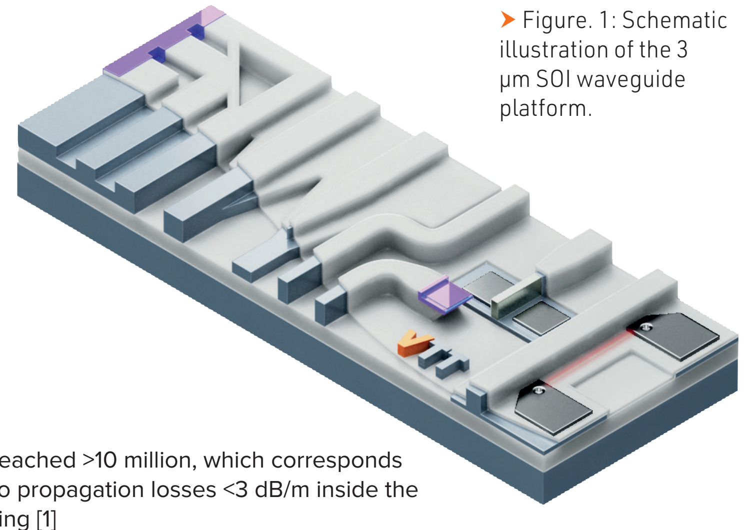

Figure. 1: Schematic illustration of the 3 µm SOI waveguide platform.

The fourth advantage of the ultra-high mode confinement is the ability for ultra-dense integration (Figure. 4). Historically, the micron-scale waveguides required bending radii of millimeters or even centimeters. This limitation was first eliminated with total-internal reflection mirrors, which had an effective bending radius smaller than the width of the waveguide. They are still the preferred approach for extremely dense integration, although they have an insertion loss of ~0.1 dB/90° for turning the light. Waveguides with lower confinement can't reach as low loss because the light propagating in the cladding doesn't get reflected by the mirror. A practically lossless approach then appeared in the form of an Euler bend that has negligible (<0.001 dB/90°) loss, as long as the bending radius is at least a few µm [2]. In addition to small bends and mirrors, the high confinement allows the realization of trivial waveguide crossings where light barely sees an intersecting waveguide.

The apparent challenge in 3 µm thick SOI waveguides is their highly multi-moded operation. With very careful design and with the support of low propagation losses, it is possible to keep light in the fundamental mode of through-etched strip waveguides. But their rectangular cross-section supports tens of propagating waveguide modes and it is difficult to launch light only to the fundamental light and to completely avoid the

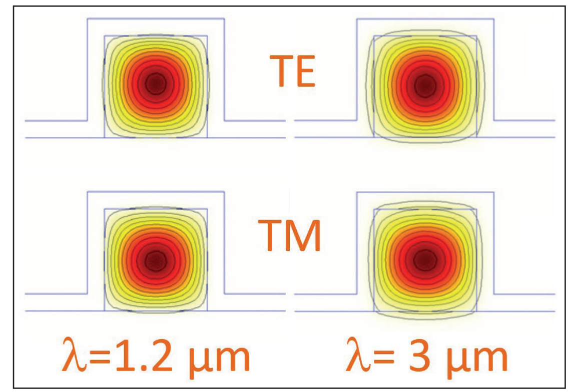

Figure. 2: Simulated mode fields of square-shaped 3 µm SOI waveguides at 1.2 and 3 µm wavelength, and at both polarizations.

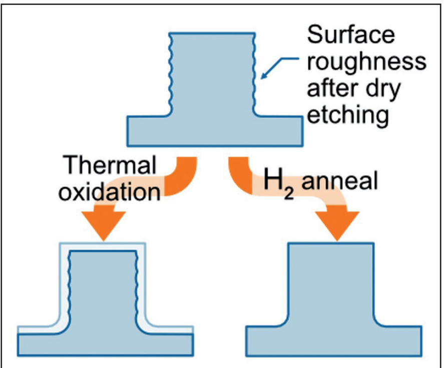

Figure. 3: The propagation losses of the 3 µm SOI waveguides are reduced to a few dB per meter by using hydrogen annealing to smoothen the waveguide side-walls.

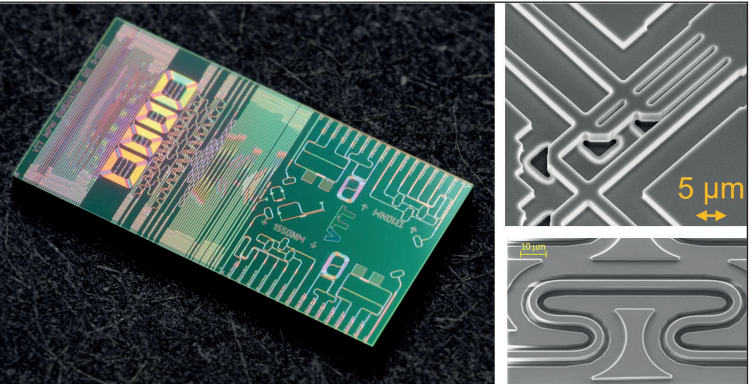

Figure 4: 5x10 mm test chip (left), crossings and TIR-mirrors at the output of a multi-mode interference (MMI) coupler (top right), and Euler bends (bottom right).

excitation of higher order modes. The solution to this problem was invented already in the 80's when partly-etched rib waveguides were demonstrated to offer single mode operation in almost arbitrarily thick waveguides. Only the fundamental mode can propagate along the rib waveguide, while any other light coupled to the waveguide radiates away into the surrounding Si slab. When combined with an adiabatic rib-strip converter (Figure. 1), this allows to keep light in the fundamental mode, to filter out any unwanted power in the higher-order modes and to make the PICs effectively single-moded.

A particularly attractive property of the rib waveguides is that their SM-condition doesn't depend on the wavelength, so that the PICs can be made to have SM operation and low-loss over an extremely wide wavelength range. Some simple waveguide components, such as waveguide spirals, mirrors, bends and wavelength (de)multiplexers have been demonstrated to operate with low loss from 1.2 to >2.4 µm wavelength.

Numerous passive and active waveguide components have been developed and monolithically integrated on the 3 µm SOI platform. These include multi-mode interference couplers arrayed waveguide gratings (AWGs), echelle gratings, thermo-optic and plasma dispersion modulators, and Ge photodetectors, just to name a few. Instead of describing them in detail, we focus here on the broadband and polarization independent operation of the platform and its input/output interfaces. As was explained above, the ultra-high mode confinement allows the waveguides and many waveguide components to operate over ultra-wide wavelength ranges. Bends, mirrors, crossings, directional couplers, AWGs and echelle gratings can have >1 µm bandwidth.

The last three on this list are interferometric components that have natural wavelength dependency that is used to make e.g. wavelength filtering or (de)multiplexing, but their insertion loss remains small over this ultra-wide bandwidth. In contrast to those, the widely used multi-mode interference (MMI) couplers have a finite bandwidth of ~100 nm, which must be taken into account.

Light can be coupled into (or from) the 3 µm SOI waveguides either horizontally or vertically. The former is achieved by simply leaving an etched waveguide facet at the edge of the chip and coating it with an anti-reflection coating (ARC) to reduce back-reflections. A lensed fiber with ~3 µm spot size can be used to couple light to the 3 µm SOI waveguides with very repeatable ~0.5 dB coupling

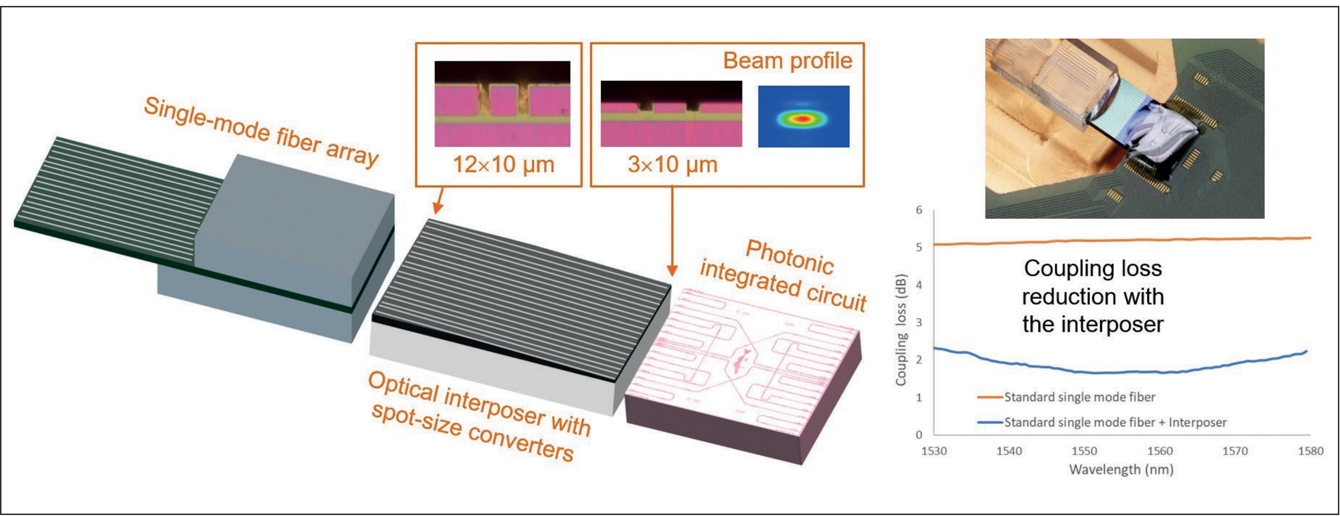

Figure. 5: Horizontal fiber-coupling concept using a polished 12 µm SOI interposer.

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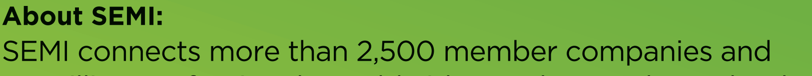

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loss. The bandwidth of the fiber-coupling is mainly limited by the fiber itself and the ARC. With a single-layer ARC the low-loss coupling bandwidth is ~100 nm and it can be extended beyond 300 nm by using a multi-layer ARC. Permanent coupling to a standard single-mode fiber array (SSMF) can be achieved with a polished interposer made from 12 µm SOI waveguides (Figure. 5). It connects the SSMF array to a 12 µm thick SOI waveguide array, gradually reduces the thickness of the waveguides down to 3 µm and then couples the light to the 3 µm thick SOI waveguides on the actual PIC chip. Horizontal coupling has also been used to hybrid integrate semiconductor optical amplifiers (SOAs), lasers and modulators on SOI using flip-chip bonding.

Vertical I/O coupling is possible with so-called up-reflecting mirrors (URMs). Those have a wet-etched negative 45° TIR mirror that reflects light up/down through an ARC that is deposited on top of the URM. This has been demonstrated to have as low coupling loss as the horizontal coupling [3]. Vertical coupling can be used for wafer-level testing (WLT), permanent fiber coupling (with suitable fiber arrays or down-reflecting coupling blocks) and hybrid integration. In particular, photodetectors (PDs) and vertical-cavity surface-emitting lasers (VCSELs) have been successfully integrated on 3 µm SOI using URMs.

In conclusion, 3 µm SOI waveguide PICs feature ultra-high mode confinement into the Si core, which enables ultra-broadband, low-loss and polarization-independent operation, as well as dense integration. This makes the technology particularly useful for applications like lidars, spectroscopy and broadband communication.

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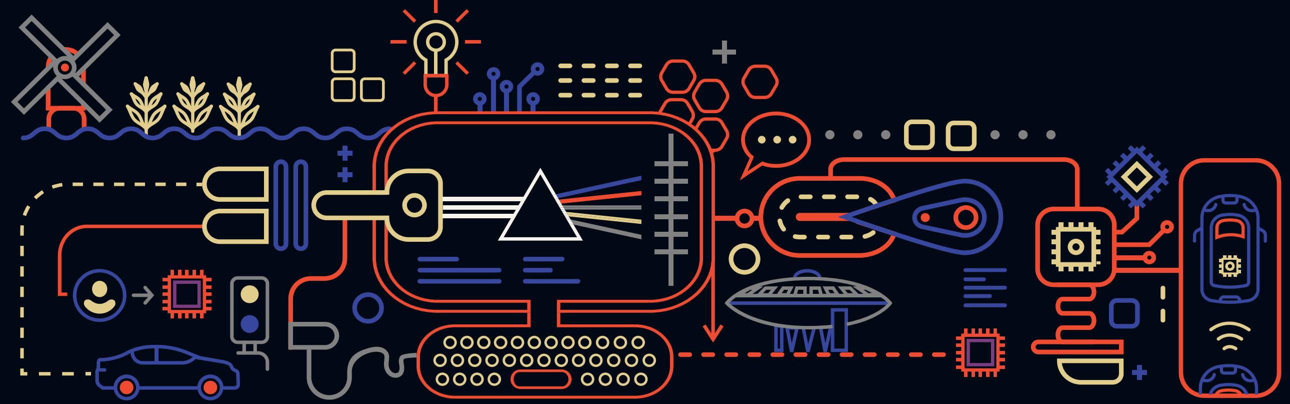

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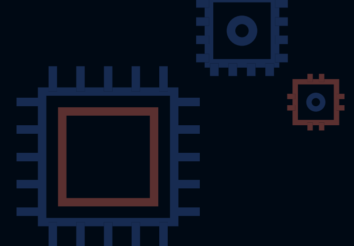

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InP-based lasers surpass 2.2 µm

Thanks to the antimonide surfactant effect, strained InP lasers are delivering milliwatt emission at almost 2.3 µm

ENGINEERS from NTT, Japan, are claiming to have enhanced the capability of InP-based lasers by smashing through the 2.2 µm barrier. The team's InP ridge-waveguide lasers, featuring strained InGaAsSb multi-quantum wells, are capable of emitting output powers of several milliwatts at wavelengths up to 2.278 µm.

This breakthrough increases the attractiveness of the InP laser as an alternative to the lattice-matched GaSb-based laser in a number of applications requiring sources in the 2.1 µm to 2.3 µm range. While GaSb-based lasers in this spectral domain can be used for gaseous sensors, biomedical sensors and car exhaust analysers, processing technologies for this material system are not as mature as those for InP, which has been the key material for telecommunications for many decades.

➤ The team from NCT employed a combination of metal-organic MBE and MOCVD for growth of their hetero-structures.

Extending the wavelength of the InP-based laser is far from easy. To reach beyond 2.1 µm with an active region that employs InGaAs quantum wells, strain in this material system must exceed + 1.8 percent. The growth of such structures is challenging, requiring growth temperatures below 500 °C, alongside just a few quantum wells and layers less than 6 nm-thick. Of most concern are defects induced by large strain – they threaten to quash laser emission.

To avoid these issues, the team from NCT has turned to InGaAsSb quantum wells, supressing defect formation with surfactant mediated growth. These engineers are not the first to introduce antimony, which acts as a surfactant during the growth of strained InGaAs wells, but they have stretched the emission further than their peers by cranking up the concentration of this element.

Record-breaking lasers have been realised with a two-step epitaxial process, beginning with the growth of a four-period multi-quantum well active region sandwich by InGaAsP and InP, all grown by metal-organic MBE. After the team studied these structures, they turned to re-growth by MOCVD to add Zn-doped InP and InGaAs layers, prior to the formation of ridge-waveguide lasers. According to team spokesman Manabu Mitsuhara, the strained InGaAsSb lasers produced by NCT, could also be formed by other growth methods, such as MBE and MOCVD, which are capable of growing active regions with sharp interfaces.

Mitsuhara and co-workers studied a pair of samples grown by metal-organic MBE, featuring active regions with different thicknesses. X-ray diffraction determined that both heterostructures have smooth interfaces between the wells and barriers, while simulations of the well-defined satellite peaks suggest that the quantum wells have a strain of +2.3 percent and thicknesses of 6.4 nm in one sample and 8.4 nm in the other. Both samples have 20.6 nm-thick barriers with a strain of -0.23 percent.

Calculations based on the model-solid theory, drawing on photoluminescence measurements and strain value obtained from X-ray diffraction, suggest compositions for the well and barrier of $In_{0.82}Ga_{0.18}As_{0.95}Sb_{0.05}$ and $In_{0.45}Ga_{0.55}As_{0.95}Sb_{0.05}$, respectively.

Using standard processes for making InP telecom lasers, Mitsuhara and co-workers have fabricated ridge-waveguide lasers with a cavity length of 600 µm and a stripe width of 2.5 µm. These lasers, with quantum well thicknesses of 6.4 nm and 8.4 nm, produced several Fabry-Perot modes and had peak wavelengths of 2.190 µm and 2.278 µm, respectively, at 15 °C. Driven at 100 mA, the output power per facet of the longer-wavelength source fell from 5.9 mW to 2.4 mW when its operating temperature increased from 15 °C to 55 °C.

Mitsuhara claims that it should be easy to apply their lasers to absorption spectroscopy, which requires a tunable light source with single-mode operation and an output power of several milliwatts.

REFERENCE

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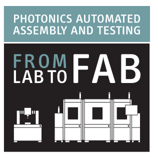

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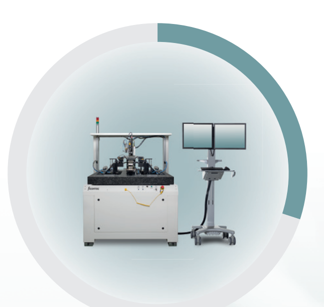

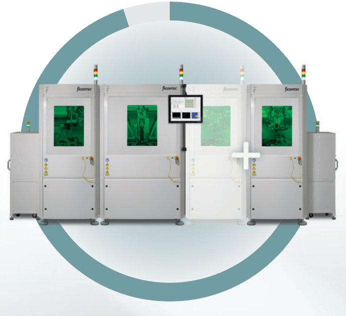

Semi Automated
Production Systems

Automated
Production Cells

Fully Automated
Manufacturing Lines

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