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VIEWPOINT

BY LAURA HISCOTT
EDITOR

Fabrication fragmentation

PICS are often compared and contrasted with their traditional electronic counterparts, and for good reason. There's much to learn from the success of the established semiconductor industry and how it might be replicated with photonic chips, while also identifying the physical differences that present unique manufacturing challenges.

But the PIC industry's evolution – and its potential divergence from the path that its electronic predecessors have taken – may be influenced by more than just intrinsic technical details. After all, this industry is maturing in a notably different geopolitical atmosphere from the one in which semiconductors originally flourished.

The consolidation of manufacturing in a handful of countries occurred in a time of relative peace and liberal trade. And perhaps it was not yet clear just how vital these chips would prove to be. Now, amidst raised and rising global tensions, countries are under no illusions about how essential a resource they are, both for domestic infrastructure and for economic relevance on the world stage.

PICs, despite being in an earlier phase of development, are already recognised as part of this critical sector. And they have not been left out of the drive to build up domestic supply chains – a trend which has continued this year. In June, for instance, GlobalFoundries announced its "re-shoring" investment of $16 billion in US semiconductor production, with focus areas including silicon photonics.

But while countries seek to loosen their reliance on global supply chains for silicon, novel PIC platforms may offer an opportunity to establish a better level of independence from the get-go. For example, this year has seen major announcements from three foundries producing TFLN PICs

– which are rapidly gaining traction – on three different continents. In May, QCi officially opened a new TFLN facility in Arizona, US. The same month, CSEM announced that it had launched the spin-off CCRAFT in Switzerland, describing it as the first production-ready pure-play TFLN foundry. In June, reports emerged that CHIPX in Shanghai had officially begun producing TFLN chips, in China's first PIC pilot line.

While some consolidation may happen at a company level, we might not see a replay of the geographical concentration of manufacturing that took place with silicon. Is this a good thing for the industry? Efficiency and resilience are often conflicting imperatives. It was economic efficiency, after all, that drove the current geographical imbalance in manufacturing. But then, perhaps the added level of competition will drive innovation. It will be interesting to see how the PIC production landscape unfolds over the coming years, and how it reflects the era in which the industry grew.

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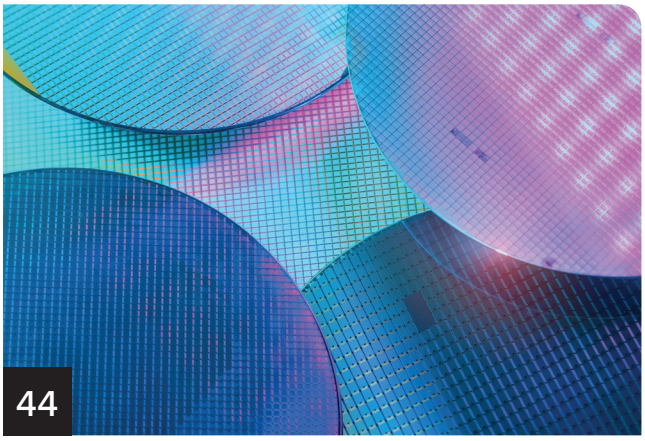
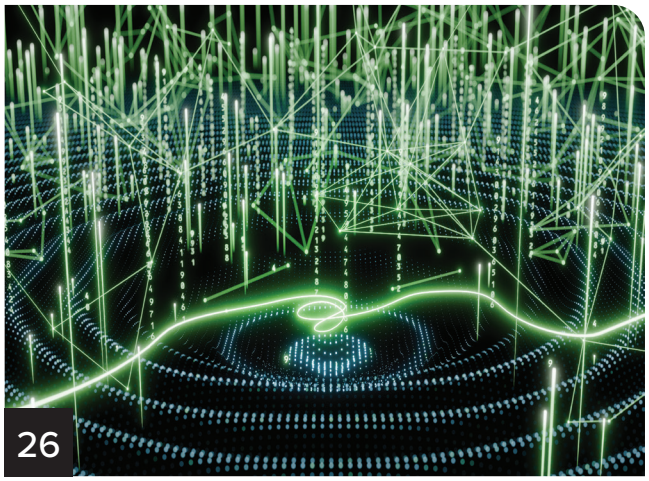
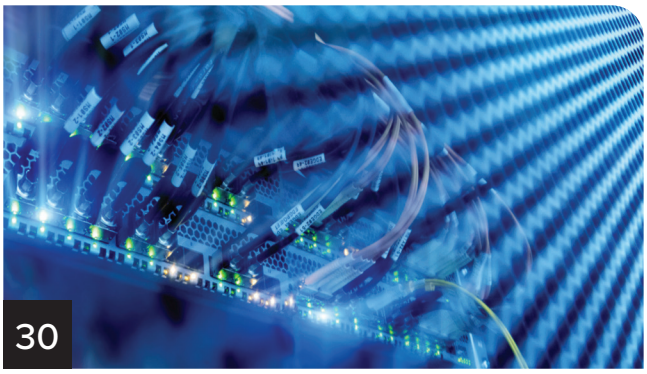
COVER STORY

The essential link in next-generation optical connectivity

With industry-ready 3D nano-printing solutions, Vanguard Automation is lighting the path to scalable and reliable processes for integrating active components to PICs







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Terakraft and Neurophos collaborate on sustainable AI

The companies plan to run a pilot in 2027, offering early access to Neurophos' ultra-efficient optical chips for AI inference hosted in Terakraft's fully renewables-powered datacentre

AI DATACENTRE operator Terakraft and AI chip company Neurophos have announced that they are collaborating to provide sustainable, high performance, and energy efficient AI infrastructure.

As the AI-driven surge in demand for data continues, a major challenge is the enormous amounts of energy required to power and cool computing infrastructure. Terakraft and Neurophos seek to demonstrate that a combination of green datacentres and breakthrough hardware can meet these needs in a sustainable way.

Terakraft, which is based in Norway, says its infrastructure is fully powered by renewable hydropower and cooled with natural lake water, achieving a power usage effectiveness (PUE) below 1.1, which it says is among the best metrics in the industry. The company is repurposing an existing hydropower plant built with reinforced concrete, with the goal of avoiding additional embodied carbon and setting a new benchmark for low-emission operations.

Meanwhile, Neurophos has developed AI hardware with proprietary optical processing units which it says are 100x more energy efficient than leading GPUs for the same workload.

The company says it has successfully fabricated, demonstrated, and characterised its miniaturisation of optical modulators by a factor of 10,000x, enabling future optical processing units to deliver the compute power of 100 GPUs while consuming the equivalent of 1 percent of the energy, validated by end-to-end simulation results. According to Neurophos, its compute-in-memory architecture, which is inspired by the human brain's efficiency, allows for unprecedented processing speeds and density, making ultra-efficient, large-scale AI inference practical and scalable.

The companies plan to host a pilot as part of a commercial early access programme in 2027 for Neurophos' accelerated AI inference platform – a project that aims to provide a real-world proving ground for sustainable, ultra-efficient compute.

"By hosting Neurophos' ultra-efficient optical chips in our green datacentre for select enterprise clients, we not only reduce our carbon footprint but also raise the bar for energy-efficient AI infrastructure," said Giorgio Sbriglia, chairman of the board of Terakraft. "Our mission has always been to power the future responsibly, and this collaboration brings that vision to life."

Patrick Bowen, CEO and founder of Neurophos, added: "Terakraft's commitment to renewable energy and innovative technologies aligns perfectly with our mission to democratise high-performance AI. By deploying our 100x more efficient inference chips in Terakraft's green datacentre we're proving that AI's exponential growth can be achieved sustainably, together."

OpenLight closes $34 million Series A funding round

The company plans to use the new investment to expand its PDK library, which is based on the heterogeneous integration of indium phosphide and silicon photonics, and scale its team to support customers as they transition to volume production

OPENLIGHT, a company focusing on custom photonic application-specific integrated circuit (PASIC) chip design and manufacturing based on heterogeneous integration, has announced that it has closed its oversubscribed $34 million Series A funding round.

The round is co-led by Xora Innovation and Capricorn Investment Group. Other participants include Mayfield; Juniper Networks, now part of HPE; Lam Capital, the corporate venture arm of Lam Research Corporation; New Legacy Ventures; and K2 Access.

OpenLight says that this round of financing completes its transition from a Synopsys subsidiary to a high-velocity, venture-backed company positioned to address the growing demand for faster and more energy-efficient data movement in AI datacentre networks.

As the shift from electrical to optical interconnects accelerates to support AI-scale workloads, integrated photonics is emerging as a core enabler of next-generation datacentre infrastructure. Additional applications for OpenLight's technology include telecom, automotive and industrial sensing, IoT sensing, healthcare and quantum computing.

OpenLight has developed a Process Design Kit (PDK), based on the heterogeneous integration of indium phosphide and silicon photonics, which aims to give customers access to a library of passive and active components covering integrated lasers, modulators, amplifiers and detectors.

The company says its PDK has been validated at the leading photonics foundry Tower Semiconductor, ensuring designs are production-ready from day one.

According to OpenLight, this enables customers to create custom PASICs using proven building blocks, simplifying advanced chip development and accelerating time to market.

The company adds that it currently holds more than 360 patents covering its PDK and the manufacturing of heterogeneously integrated III-V photonics, and that its PDK is already being used by over 20 companies to design and fabricate PASICs across a wide spectrum of applications.

With the new capital injection, OpenLight plans to expand its PDK library of active and passive photonics components, including its 400G modulator and indium phosphide heterogeneously integrated on-chip laser technology. The company also aims to ramp up its standard-based reference PICs at 1.6T and 3.2T to provide customers with the most flexible and leading-edge component design library available in the market. In addition, OpenLight says it will scale its team to support customers as they transition to volume production over the next 12 months.

"As we enter this next phase of our company's growth, we are excited to be adding such strong investors with deep roots and expertise in the semiconductor and photonics industry," said Adam Carter, CEO of OpenLight. "With this strong syndicate of investors, we can push the boundaries of innovation and deliver transformative solutions to our customers. This funding will allow us to scale our operations, deepen our R&D efforts and bring our groundbreaking products to market faster. We believe heterogeneous integrated silicon photonics will transform the way data is processed and transmitted, and we're excited to be at the forefront of this revolution."

Phil Inagaki, managing partner and chief investment officer at Xora, commented: "Xora has conviction that the field of photonics is going to see exponential growth in the coming years, and III-V heterogeneous integration is one of the foundational capabilities that will enable this growth."

"We see OpenLight not only as a technology leader in this field, but also as a company positioned to quickly scale manufacturing with foundry partners. One of the critical challenges for the photonics industry in the back half of this decade will be achieving scale, and we see OpenLight's PDK as an important part of the solution."

Dipender Saluja, managing partner at Capricorn's Technology Impact Funds, added: "Optical connectivity in datacentres has become critical for next-generation scale-up and scale-out AI architectures. OpenLight's heterogeneous integration delivers on all three axes of performance, reliability and cost, which will enable the explosive growth of optical IO. With the industry's leading team, open PDKs, strong foundry and customer relationships, OpenLight is best positioned to meet the scale of demand that is needed for next-generation AI hardware."

Lightmatter achieves 16-wavelength bidirectional link on standard optical fibre

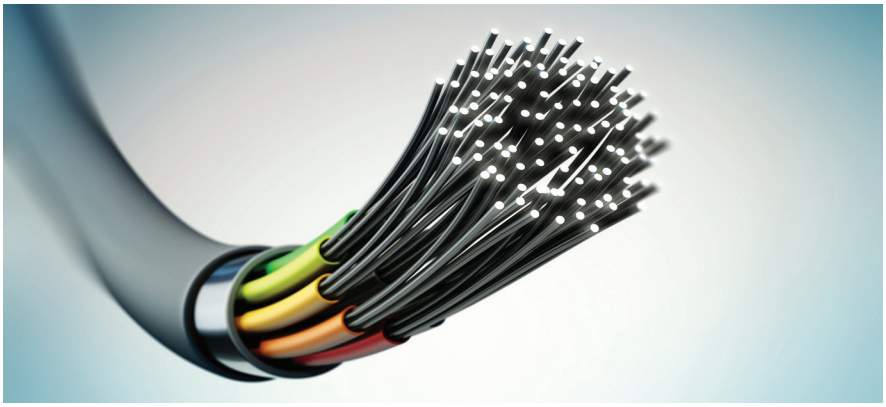
The company says this breakthrough advances chip I/O design by increasing bandwidth per fibre compared to existing co-packaged optics solutions, and enables more powerful, efficient, and scalable datacentres

LIGHTMATTER, a company focusing on photonic supercomputing, has announced it has developed a 16-wavelength bidirectional dense wavelength division multiplexing (DWDM) optical link operating on one strand of standard single-mode (SM) fibre. Powered by Lightmatter's Passage interconnect and Guide laser technologies, the company says this achievement shatters previous limitations in fibre bandwidth density and spectral utilisation, setting a new benchmark for high-performance, resilient datacentre interconnects.

With the rise of complex trillion-parameter "mixture of experts" models, scaling AI workloads is increasingly bottlenecked by bandwidth and radix (I/O port count) limitations in datacentre infrastructure. Lightmatter says its Passage technology delivers an unprecedented 800G bidirectional bandwidth (400G transmit and 400G receive) per single-mode fibre for distances of several hundred metres or more. This achievement advances chip I/O design by simultaneously increasing both radix and bandwidth per fibre compared to existing co-packaged optics (CPO) solutions, the company adds.

While commercial bidirectional transmission on a single fibre has been limited mainly to two wavelengths, achieving 16 wavelengths (also referred to as "lambdas") has historically required multiple or specialised fibres.

According to Lightmatter, this milestone addresses significant technical challenges related to managing complex wavelength-dependent propagation characteristics, power budget constraints, optical nonlinearity, and mitigating crosstalk and backscattering in a single fibre.



Such innovations could pave the way for the next major advances in AI model development, which demand more extensive and efficient high-bandwidth networking than exists today.

"Datacentres are the new unit of compute in the AI era, with the next 1000X performance gain coming largely from ultra-fast photonic interconnects," said Nicholas Harris, founder and CEO of Lightmatter. "Our 16-lambda bidirectional link is an architectural leap forward. Hyperscalers can achieve significantly higher bandwidth density with standard single-mode fibre, reducing both capital expenditure and operational complexity, while enabling higher 'radix' – more connections per XPU or switch."

Alan Weckel, co-founder and analyst at 650 Group, added: "Lightmatter's innovation arrives at a pivotal moment for hyperscale AI infrastructure. The ability to dramatically increase bandwidth density on existing single-mode fibre, coupled with the technology's robust thermal performance, is a game-changer for datacentre scalability and efficiency. This solves one of the most pressing challenges in AI development and brings advanced CPO a giant step closer to market."

According to Lightmatter, the new breakthrough incorporates a proprietary closed-loop digital stabilisation system that actively compensates for thermal drift, ensuring continuous, low-error transmission over wide temperature fluctuations. In addition, architectural innovations aim to make the Passage 3D CPO platform inherently polarisation-insensitive, maintaining robust performance even when the fibres are being handled or subject to mechanical stress.
Standard SM fibre, while offering immense bandwidth potential, does not inherently maintain light's polarisation state, unlike specialised and more costly polarisation-maintaining fibre. By achieving polarisation insensitivity, Lightmatter says it enables the use of cost-effective SM fibre for its bidirectional DWDM technology.

This combination of fibre bandwidth density, efficient spectral utilisation, and robust performance makes Lightmatter's Passage technology foundational for the industry's transition from electrical to optical interconnects in AI datacentres, the company concludes. It aims to empower customers to accelerate development of larger and more capable AI models with more powerful, efficient, and scalable datacentres.

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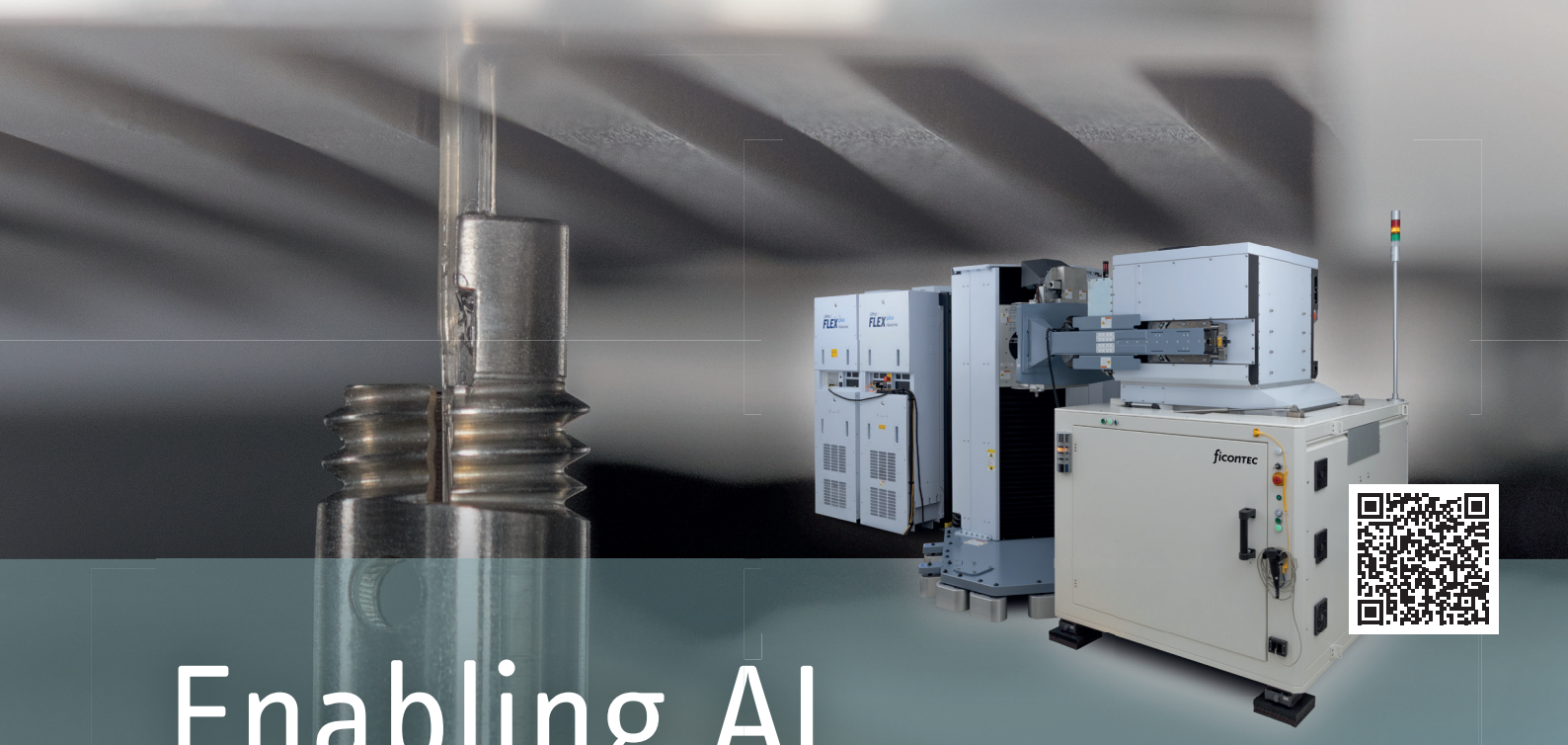

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- Compatibility with wafer autoloader

Lightium, MPI Corporation and Axiomatic AI partner on PIC testing

The companies say their AI-driven solution sets a new industry benchmark for efficiency, precision, and scalability, lowering the total cost of testing and accelerating time-to-market for next-generation PIC devices

LIGHTIUM AG, MPI Corporation, and Axiomatic_AI Inc. have announced they have entered into a memorandum of understanding (MoU) to jointly develop a platform that they describe as the world's first Intelligent, Autonomous, and Integrated Test Solution (IAITS) for photonic devices.

This strategic collaboration aims to revolutionise the testing and qualification processes of PIC devices by uniting state-of-the-art AI, next-generation hardware, and deep domain expertise.

The companies say the IAITS platform will deliver breakthrough performance in testing workflows, enabling unmatched efficiency, precision, and scalability to meet the ever-evolving demands of the photonics industry.

According to the companies, this partnership is motivated by a shared commitment to deliver groundbreaking AI-driven and self-optimising solutions to the photonics industry. By combining Axiomatic_AI's reasoning-based AI with MPI's wafer probing systems and automation software, and leveraging Lightium's testing infrastructure and expertise in ultra-high-speed photonic device measurements, the collaboration aims to bring fully integrated, intelligent PIC test solutions to market.

Together, the three companies plan to create a unified AI platform that addresses the growing complexity and performance demands of characterising PICs – unlocking new levels of automation, precision, and scalability for next-generation applications.

The Intelligent, Autonomous, and Integrated Test Solution (IAITS) aims to introduce a new paradigm in PIC testing, delivering transformative value across both technology infrastructure and human capital.

By automating complex test routines, minimising downtime, and optimising measurement system utilisation, the companies say IAITS significantly accelerates test cycles and reduces iteration times, increasing throughput. Another key benefit that IAITS aims to offer is enhanced human efficiency, achieved by reducing reliance on manual operation, programming, and debugging – freeing skilled personnel to focus on high-value engineering and strategic innovation tasks.

Designed to support both R&D and high-volume production environments, IAITS will be commercially available as an advanced software add-on package for MPI Corporation's wafer probing systems.

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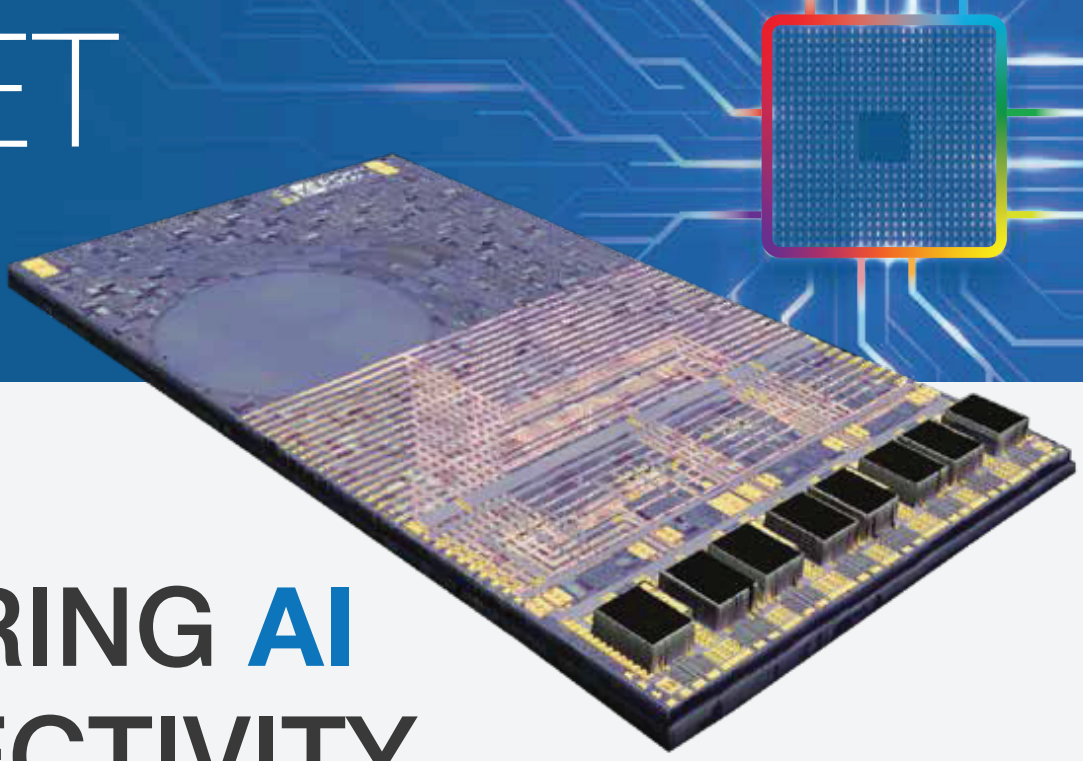

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Chief Revenue Officer

- Panelist on Market Potential for CPO
- Product Focus Presentation on POET's 1.6T Optical Engines

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Those attending these sessions will gain greater insight into device technologies while learning of the latest opportunities and trends within the PIC industry. Delegates will also discover significant advances in tools and processes that deliver enhanced yield and throughput.

Attendees at this two-day conference will also meet a wide variety of key players within the community, from investors and analysts to fab engineers and managers.

PIC International is part of AngelTech, which delivers a portfolio of insightful, informative, highly valued chip-level conferences. Bringing together an Innovate Summit and four conferences with more than 120 presentations, more than 700 delegates and over 80 exhibitors,

AngelTech is the premier global event covering compound semiconductors, photonic integrated circuits, power electronic technologies and advanced packaging.

With a significant overlap between the four conferences, attendees and exhibitors are exposed to the full relevant supply chains and customer and supplier bases.

Key Themes for 2026

Foundations of PIC design: materials, devices and processes
While PICs are well established, they still face technological limitations. How can new materials and devices improve their performance and expand their range of functionalities, and how can we accelerate these innovations to market?

Connectivity and scalability for secure, high-speed data networks
Data communications networks face numerous challenges, including soaring AI-driven demands, high energy consumption, and the possibility of future quantum technologies breaking current encryption methods. How can PICs help to solve these issues and underpin the high-speed, energy-efficient, quantum-secure networks of the future?

Emerging applications: photonics for sensing, imaging and beyond
Integrated photonics has a wide range of potential applications. From self-driving cars to miniaturised molecular sensors and non-invasive healthcare, how are PICs making these possibilities a reality?

Future computing: PICs for photonic processing, quantum computers, and neural networks
Computing power is integral to the modern world, but established technologies have limits, and novel systems could herald more powerful devices. From fully photonic processing to photonics for neuromorphic and quantum computing, how are PICs transforming the way we process data?

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The essential link in next-generation optical connectivity

With industry-ready 3D nano-printing solutions, Vanguard Automation is lighting the path to scalable and reliable processes for integrating active components to PICs

BY LAURA HORAN AND MO LU, VANGUARD AUTOMATION GMBH

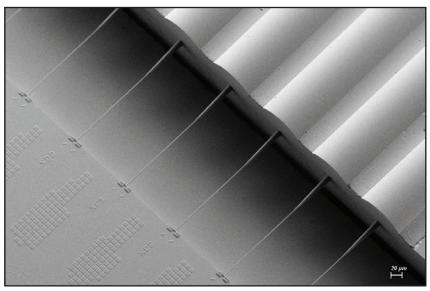
DEMAND is surging for high-performance optics and PICs, driven by AI, datacom, and quantum technologies. LightCounting's recent report on *Optics for AI Clusters* forecasts that the market for optical transceivers used in AI clusters will double from $5 billion in 2024 to over $10 billion by 2026 [1]. This underscores how the AI megatrend is reshaping traditional manufacturing, placing pressure on the industry to deliver optical assemblies that ensure precision, reliability, and cost-efficiency at scale.

But there's a major complication in meeting these needs: next-generation designs for photonic products often combine active and passive components in hybrid systems, fabricated on diverse material platforms such as indium phosphide (InP), silicon nitride, silicon, and thin-film lithium niobate (TFLN). Each of these materials has distinct mode-field characteristics and packaging requirements, and integrating active components like edge-emitting lasers into passive PIC materials for hybrid photonics remains a challenge for the industry.

Traditional active alignment techniques enable accuracy down to sub-micron precision, meeting the stringent requirements for mode-field matching and alignment tolerances that are needed to ensure highly efficient signal transmission. But these methods are labour-intensive and difficult to scale from single to multi-channel arrays. This means that packaging costs can amount to up to 80 percent of the cost of the final product, representing a significant barrier to manufacturing.

At Vanguard Automation, we take a different approach; by combining passive alignment techniques and machine vision with high-precision and fully automated 3D nano-printing, we develop scalable and high-throughput manufacturing solutions for hybrid photonic integration. Headquartered in Karlsruhe, Germany, and now a part of Mycronic, a global supplier of high-precision manufacturing tools, Vanguard Automation is uniquely positioned to deliver advanced manufacturing tools to the market.

Across datacentre, telecommunication, and AI applications, a range of users [2] working on various material platforms have proven that Vanguard Automation's novel processes can deliver the innovation and scalability needed to unlock the full potential of hybrid photonic integration [3].

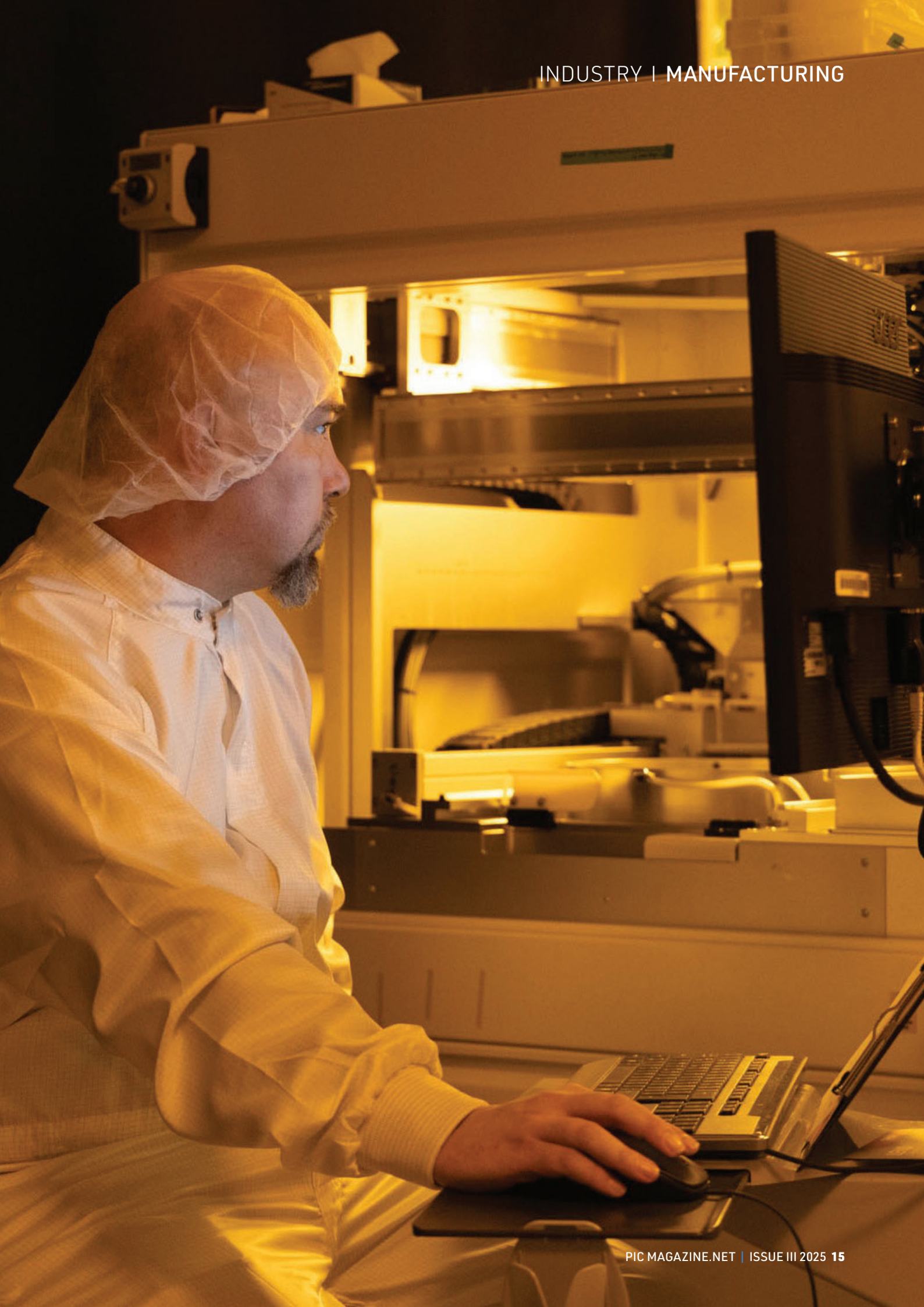


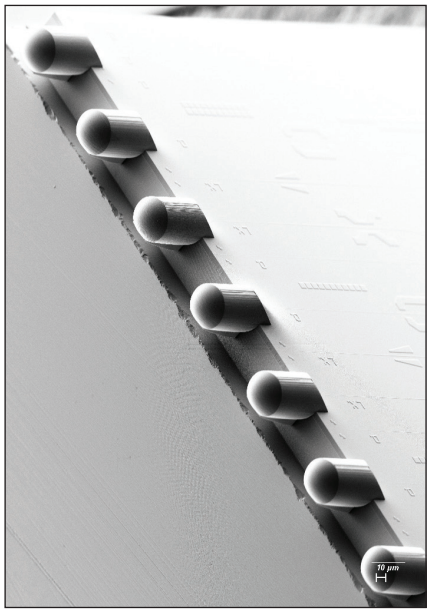
➤ Figure 1. SEM image of a single-mode fibre (SMF) array aligned to an AMF chip and integrated using Photonic Wire Bonds. This assembly type has demonstrated 100 percent yield across 180 connections, with insertion losses consistently below 2 dB and an average of 1.4 dB–highlighting the reliability of passive photonic integration packaging.

Automated nano fabrication

Vanguard's solution uses highly precise direct-write 3D laser lithography to print 3D freeform optics in-situ at the chip level, eliminating the need for active alignment and enabling passive pick-and-place assembly. The printed optics allow for mode-field matching between dissimilar materials and components, as well as compensating for manufacturing variations by relaxing alignment tolerances. Vanguard Automation offers a robust portfolio of photonic interconnect structures – most notably Photonic Wire Bonds and facet-attached micro-lenses – engineered to support versatile and scalable photonic integration across a wide range of packaging scenarios. This empowers photonic product designers and manufacturing teams to fully leverage efficient assembly build-up in volume manufacturing.

Photonic Wire Bonds (PWBs), shown in Figure 1, are single-mode freeform optical waveguides printed between two photonic components, that compensate for misalignment of up to ±20 µm. This ensures optimal coupling between dissimilar photonic components and enables passive alignment during assembly. PWBs are increasingly recognised as the preferred solution for hybrid integration of active devices such as III-V lasers, quantum-dot lasers, and amplifiers onto passive PIC material platforms [4-6].





➤ Figure 2. SEM image showing facet-attached micro-lenses precisely 3D-printed onto the edge of an AMF chip, demonstrating in-situ fabrication for compact, alignment-tolerant photonic integration.

In recent demonstrations, PWBs achieved insertion losses as low as 1 dB per interface and supported stable, mode-hop-free laser operation exceeding 58 hours.

Even more impressively, the Vanguard system can complete fibre-to-chip-to-laser integration in a single fabrication step. To achieve this, the system uses machine vision to detect the individual waveguide positions, and automatically calculates the optimal low-loss PWB interconnect trajectory, including mode-field matching.

Meanwhile, facet-attached micro-lenses (FaMLs) can perform spot size conversion and beam expansion, relaxing alignment tolerances up to ±15 µm, and beam shaping reduces sensitivity to lateral and angular misalignment. This eliminates the need for bulk optics, reducing system footprint and cost while overcoming optical and mechanical challenges in hybrid photonic packaging.

FaMLs are a key component for integration in electro-optical engines that underpin transceivers, co-packaged optics, light engines, and sensing devices. A stand-out example is POET Technologies, which collaborates with Vanguard Automation to integrate 3D printed micro-lenses onto its optical interposers. This collaboration enhances coupling efficiency while preserving POET's signature wafer-level passive assembly process [7].

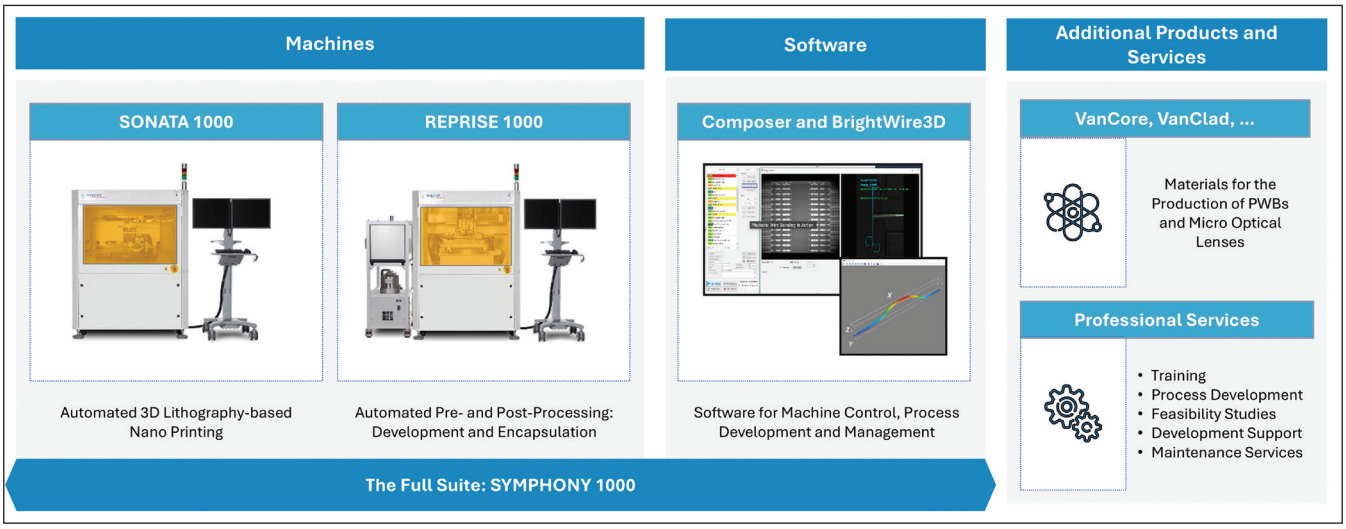
With its complementary technology portfolio, Vanguard Automation provides a scalable path for volume-production customers to incorporate 3D-printed optics into their production chain. Starting with hybrid approaches using 3D-printed optical elements and active alignment, the product design can evolve to leverage the full potential for photonic integration. Ultimately, customers can benefit from incorporating PWBs with standard pick-and-placing of components with very relaxed tolerances, while simultaneously ensuring high coupling efficiency, high yields, and high package density.

And there are advantages for foundries too; since PWBs and FaMLs can work with simple inverse taper edge couplers realised by stepper lithography, the chip real estate used for sophisticated couplers can be reduced substantially, paving the way towards a novel and more universal standard for optical coupling [8]. Furthermore, the benefits of PWBs and FaMLs can be combined to form a unique offering to correct highly elliptical laser outputs [9].

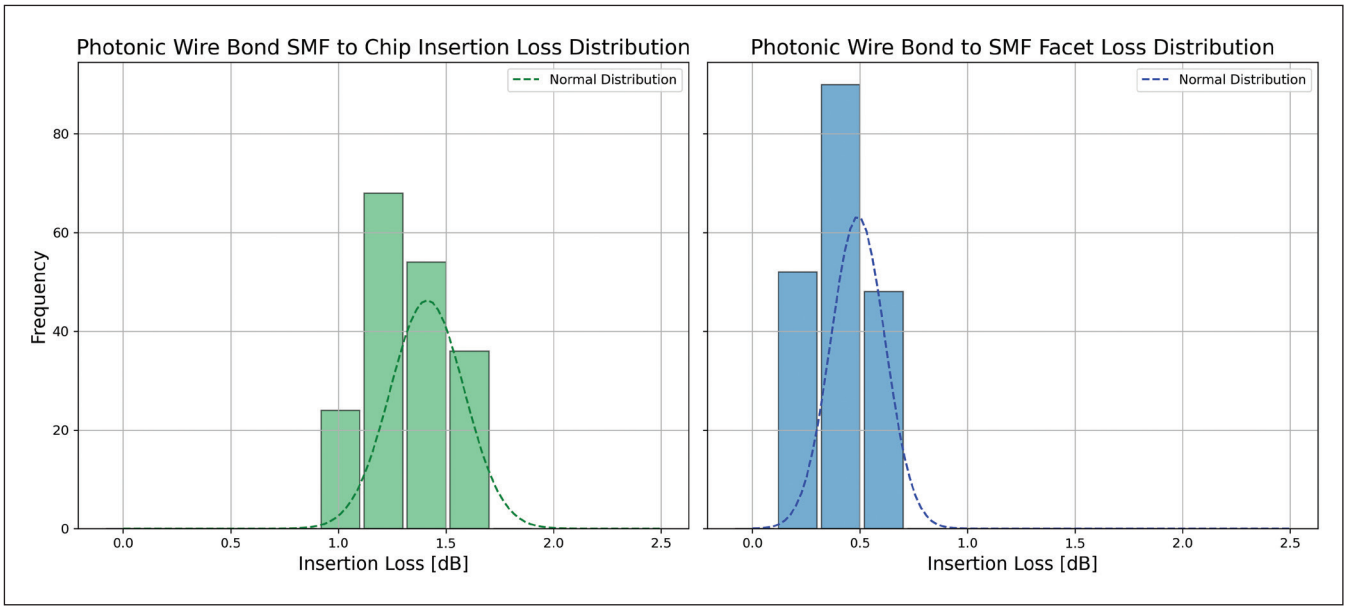
This convergence of compact design, relaxed alignment tolerances, and platform versatility positions PWBs and FaMLs as foundational building blocks for scalable, cost-efficient photonic manufacturing, enabling streamlined integration and expanded design flexibility across platforms.

Flexible, reliable and robust

Vanguard offers a fully automated solution, the vanguard SYMPHONY, which comprises two systems: one for the fabrication of PWBs and FaMLs (vanguard SONATA 1000), and one for postprocessing of optical assemblies to complete the fully automated packaging process (vanguard REPRISE 1000). Alongside the machines, vanguard SYMPHONY incorporates Vanguard's Brightwire3D software for automated, highly precise interface detection (accurate to < 50 nm) as well as on-the-fly calculation of optimal PWB trajectories.



➤ Figure 3. Vanguard SYMPHONY: Vanguard Automation's fully automated photonic integration and packaging platform, featuring BrightWire3D software for precision interface detection and VanCore photoresists engineered for industrial reliability.



➤ Figure 4. Statistical overview of insertion loss performance for fibre-to-silicon PIC and SMF facet coupling using Photonic Wire Bonds, demonstrating consistent low-loss results across multiple assemblies.

Additionally, the solution includes dedicated photoresists tailored to meet strict industrial reliability requirements (vanguard VanCore series), and standard fabrication processes. Finally, customers can also take advantage of engineering services and support to advance quickly from prototyping to production, as seen in Figure 3.

Whereas traditional volume manufacturing relies on product-specific physical tooling, 3D printing operates on a software-defined model, enabling the complete removal of long lead times and expenses associated with tooling preparation. This significantly accelerates the development and production cycle of complex freeform optical components and waveguides for hybrid photonic integration.

Vanguard's solution thus enables seamless transition from prototyping to volume production, including batch and wafer-level processing with industrial-grade reliability. Designed to be flexible, the Vanguard Automation SYMPHONY systems can be easily adapted to different product requirements and production lines.

While delivering flexibility and automation for scalability, Vanguard's photonic packaging technology does not compromise on yield; indeed, it consistently delivers high yield across a range of integration scenarios and has undergone rigorous testing to validate its performance and reliability. Figure 4 highlights the high yield performance of two common assembly types used in photonic integration: SMF fibre-to-silicon PIC and SMF fibre-to-fibre.

In the case of SMF fibre-to-silicon PIC assemblies, Vanguard's PWB achieves 100 percent yield with insertion losses below 2 dB across 180 connections, with a mean of 1.4 dB. For SMF fibre-to-fibre assemblies, the technology maintains 100 percent yield with insertion losses under 0.75 dB per facet across 190 PWB to SMF facet interfaces, with a mean of 0.49 dB [3]. Even with lateral misalignments exceeding 20 µm and vertical offsets exceeding 40 µm, insertion loss remains stable — demonstrating that PWBs work reliably with passive alignment at production scale.

In high-precision photonic manufacturing, consistent insertion loss performance for back-end photonic integration is critical to ensuring high yield, process control, and quality assurance. Reliable manufacturing of photonic interconnects ensures that performance metrics remain within acceptable limits across production batches. Vanguard's consistent insertion loss results highlight the robustness and repeatability of its 3D printing technologies, making them highly suitable for industrial-scale deployment. Industry users have reported a 99 percent reproducible yield in laser-to-silicon nitride assemblies, with coupling losses below 2.3 dB and a mean of just 1.7 dB, further validating the reliability of PWBs for hybrid integration.

PWBs and FaMLs have also demonstrated exceptional reliability under rigorous environmental testing [3]. Assemblies with 3D-printed optics have been subjected to thermal cycling, mechanical stress, and Telcordia damp heat conditions (85 degrees C, 85 percent relative humidity), with insertion loss variation remaining within 0.5 dB

By combining fully automated system tools, Telcordia-qualified materials, and 3D-printed freeform optics, Vanguard Automation's photonic integration solution portfolio delivers industry-grade performance from prototyping to volume manufacturing

over 2000 hours, as demonstrated in Figure 5. In further testing, no degradation was observed under mechanical shock or vibration, and FaMLs maintained stable performance during high-power operation at 200 mW for over 5000 hours, showing no signs of delamination or structural failure. These results confirm the robustness of Vanguard's photonic packaging technologies for demanding industrial applications.

Crucially, 3D-printed structures retain optical integrity after 260 degrees C solder reflow, ensuring compatibility with thermally demanding back-end processes. This makes the technology an ideal fit for integration into standard semiconductor workflows.

When FaMLs are printed in situ to InP modulator chips and sealed in industry-standard hermetic "gold-box" packages, they maintain stable performance – even after 500 thermal cycles, mechanical shock, vibration, and die bonding at 320 degrees C [3].

In non-hermetic applications, such as coupling silicon nitride PICs to polarisation-maintaining fibre arrays, FaMLs have demonstrated robust thermal stability, with less than 0.1 dB variation after reflow soldering [10]. This level of thermal and mechanical resilience makes FaMLs a viable solution for co-packaged optics (CPO), which demands compact, reflow-tolerant, and detachable fibre-to-chip coupling.

A bright future

As we look ahead to ECOC 2025 and beyond, the message is clear: Vanguard Automation's Photonic Wire Bonds and facet-attached micro-lenses offer a scalable and reliable solution to one of the photonic industry's most pressing challenges – integrating active components to PICs.

By combining fully automated system tools, Telcordia-qualified materials, and 3D-printed freeform optics, Vanguard Automation's photonic integration solution portfolio delivers industry-grade performance from prototyping to volume manufacturing.

The platform-agnostic solution enables passive assembly alignment, batch and wafer-level processing, and software-defined fabrication, eliminating the bottlenecks of traditional tooling and accelerating development cycles.

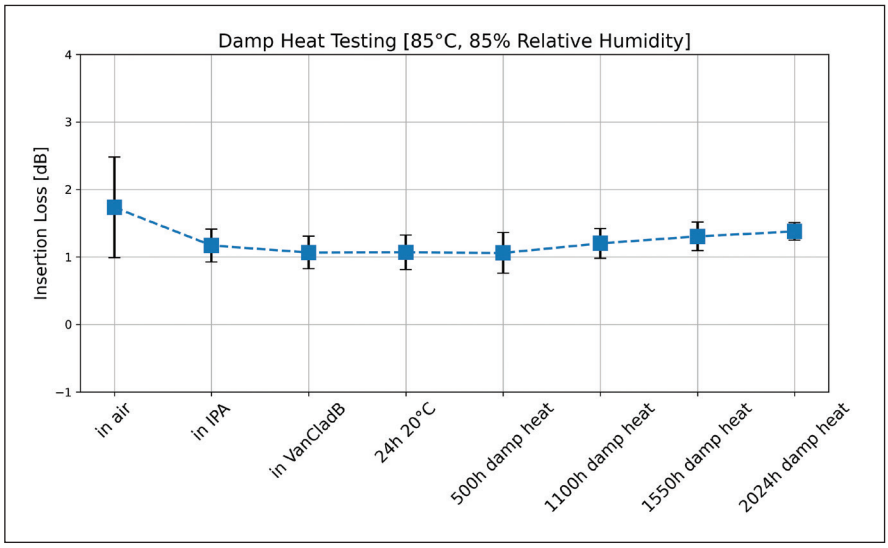


Figure 5. Telcordia damp heat test results for SMF fibre-to-fibre connections using Photonic Wire Bonds, monitored over 2000 hours at 85 degrees C and 85 percent relative humidity. Each data point represents the average performance of 10 PWBs, demonstrating long-term environmental stability.

This approach is already empowering customers in both research and industry to develop next-generation photonic integration and packaging that combine the strengths of diverse photonic platforms into compact, high-density multi-chip modules. 3D-printed freeform optics is more than just a packaging solution; it's a platform for innovation.

With proven yield, low-loss performance, and design flexibility, Vanguard Automation is not just solving today's integration challenges, but shaping the future of photonic manufacturing.

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A seamless PIC design workflow for datacentre interconnects

VPIphotonics' universal design automation framework empowers design teams to model and optimise PIC-based optical datacentre interconnects at every level, from submicron integrated devices to kilometre-scale fibre links. The framework features customisable, secure, and multi-platform PDK support.

BY EUGENE SOKOLOV, ANDRZEJ POLATYNSKI, NEBRAS DEB, HANNES LÜDER, CHRIS MALONEY, AND ANDRÉ RICHTER, VPIPHOTONICS

FROM pluggable transceivers to advanced co-packaged optics, PICs are already powering next-generation datacentre interconnects. By offering compact, low-power, and high-bandwidth solutions for wavelength-division multiplexing (WDM) and high-speed links between multiple processing units, they enhance data throughput and scalability [1], addressing an unprecedented demand for computing power in datacentres. As such, they are an indispensable technology for AI and the digital transformation.

However, photonic chips are complex devices, and performance bottlenecks often emerge late in the design cycle [2]. System-level modelling of PICs is essential to optimise optical links and meet strict network specifications. This increasingly involves hybrid PIC platforms, combining diverse materials and integration strategies, which require optimisation of basic sub-components, such as modulators, splitters, and combiners. Although Process Design Kits (PDKs) with building block libraries simplify design, there is growing demand for customisation without compromising IP security [3].

This is where VPIphotonics' advanced Photonic Design Automation (PDA) framework excels, unifying PIC and optical system simulation in one environment.

This solution enables accurate modelling of photonic devices and components considering full-system behaviour – from submicron integrated devices to kilometre-scale fibre links – while supporting customisable, multi-platform PDK development. The framework supports collaboration between designers working on different aspects of the system. Designing PIC-based systems often involves separate teams; photonic engineers focus on designing PICs and optimising components such as modulators and filters, while system engineers are responsible for the overall system architecture and performance, whether for transmitters, receivers, fibre links, or digital signal processing (DSP). While this division of expertise is necessary for such a complex, multi-stage process, it can also lead to fragmented

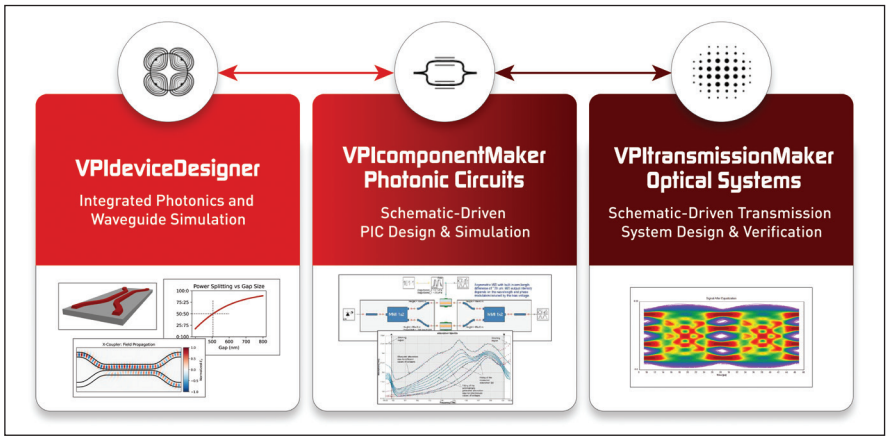
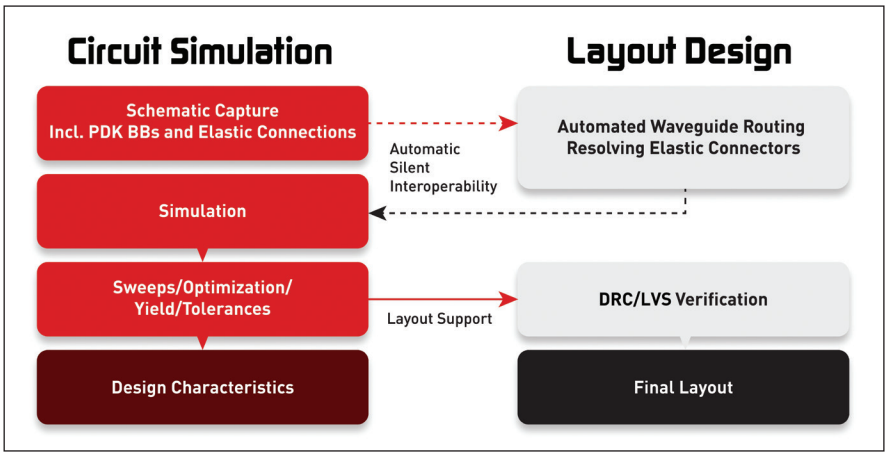


Figure 1. Block description of the cross-layer photonic design framework.

workflows, relying on manual file transfers, custom scripts, and repeated tuning cycles [1].

To address this, a unified simulation framework brings together VPIphotonics Design Suite [4] and VPIdeviceDesigner [5] as presented in Figure 1. It combines device design and optimisation with flexible import and export of the component GDS, custom PDK creation, and circuit design with full optical system simulation, and export of the final circuit layout. This shared design environment facilitates seamless collaboration, allowing teams to co-simulate and optimise PICs in system-level contexts, while tailoring models to specific foundry processes.



➤ Figure 2. Block description of the layout-aware schematic-driven design methodology [7].

Device modelling

The first layer of the PDA framework focuses on the level of individual devices. Here, optimising building blocks for foundry-specific, PIC-dedicated applications requires both adequate simulation models and the ability to import and export the equivalent layout of the building blocks. While working with foundry-specific elements, the design process typically follows layout-driven workflows. This involves importing an existing initial design as a GDS file, adding or removing fabrication-aware corrections, generating the 3D device, and optimising its simulation and geometry. On the other hand, to develop new, custom individual PIC building blocks, designers require a flexible process for creating 2D waveguide cross-sections and 3D devices.

In both scenarios, the simulation requires a combination of powerful mode solvers, which calculate light's behaviour in the device, and an efficient 3D simulation technique to optimise its geometry. A few of the most common techniques are finite difference time domain (FDTD), 3D beam propagation (BPM), and eigenmode expansion (EME) methods.

While FDTD provides the most accurate simulation results, this method has high computational and memory costs, making it unusable for larger components and more complex optimisation processes. In many cases, BPM and EME provide great alternatives with satisfying accuracy and reasonable simulation time for optimising integrated photonic devices. That, together with easy-to-use postprocessing capabilities, makes VPIdeviceDesigner a practical tool for analysing integrated dielectric and plasmonic waveguides, optical fibres, and passive integrated components such as multi-mode interferometers, directional couplers, edge couplers, and photonic lanterns. VPIdeviceDesigner is natively integrated in Python, offering complete flexibility in the simulation workflow and seamless integration with other Python libraries.

Additionally, users can export the performance data in a suitable format for VPIcomponentMaker Photonic Circuits [4] – the second layer of our design framework – ready to be included in the circuit-level PIC simulation. Furthermore, it is easy to systematically vary the dimensions of GDS-imported layouts, enabling geometry optimisations and parameter sweeps. Designers can then export the resulting optimised layout back to the layout tool, or write it directly into the PDK file structure. Since VPIdeviceDesigner is fully integrated into Python, all these steps can be fully automated, version-controlled, and organised as reproducible simulation recipes.

PICs and PDKs

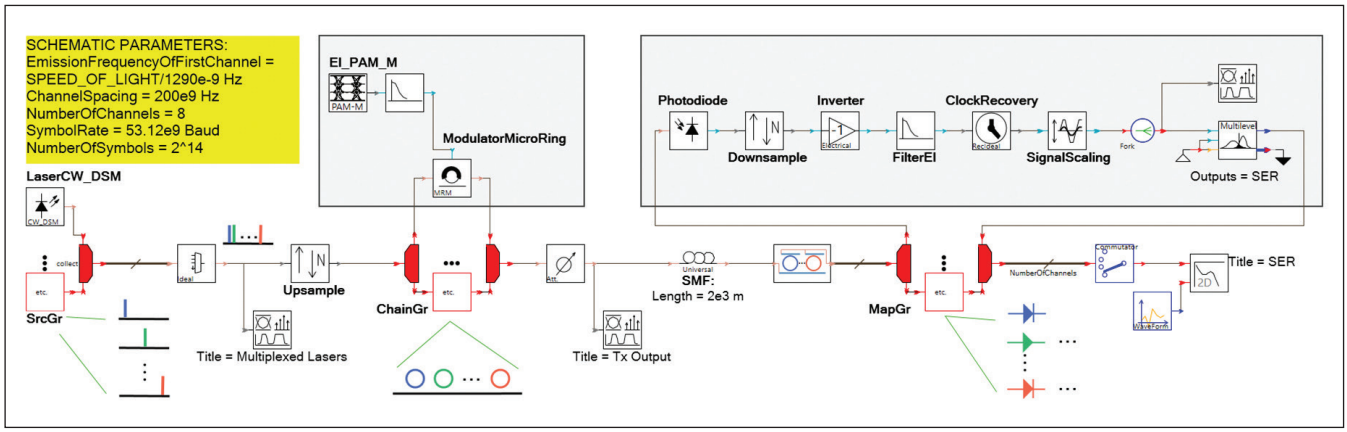
Moving from individual devices to circuit design represents a new level of complexity, with modern PICs containing dozens of components and hundreds of devices on just a single chip. A large-scale passive PIC – which does not include any light sources or detectors – can be efficiently simulated at different frequencies as a single assembled S-matrix, which is calculated from the schematic on the fly and fully describes transmitted and reflected signals [6]. Since these models represent steady-state behaviour without transient effects, the duration of the signal data block, or time window, can remain short; the lower limit is defined mainly by the desired frequency resolution, which is improved by a longer time window.

However, validating system performance metrics, such as symbol error rate (SER), may require the simulation of millions of symbols and thus a long time window. This means the S-matrix must be calculated at many more frequency points, making its assembly significantly more complex.

To address this, a faster, memory-efficient implementation calculates the S-matrix for a smaller number of frequency points and then interpolates the values between them. This maintains a high accuracy while significantly reducing the computation resources required.

While simulating passive linear circuits is relatively straightforward, accurately modelling active and electro-optic elements such as lasers, amplifiers, and modulators requires sophisticated circuit-level models operating in the time domain that capture nonlinear effects, bidirectional propagation, and dynamic carrier density behaviour [6].

VPIcomponentMaker Photonic Circuits addresses these requirements with its transmission-line laser model (TLM).



➤ Figure 3. 800G DWDM PAM-4 system schematic.

To further manage the complexity of large-scale circuits, circuit-level tools support hierarchical designs for block reuse, graphical structuring of serial/parallel layouts, and Python/MATLAB co-simulation for creating custom components or technologies.

Besides the many different components that make up PICs, a further complexity in simulation arises from the many photonic platforms available, including silicon, indium phosphide, lithium niobate and more. Designing high-performance PICs for optical systems often involves combining these different materials, each of which has unique advantages and integration approaches, increasing the need for customisation. While foundry-provided PDKs accelerate development by using libraries of pre-characterised building blocks, designers often face two key limitations: the difficulty of creating new building blocks and the challenge of customising existing ones without compromising foundry and company IP [3].

To address these challenges, VPI Design Suite provides a framework for the flexible development of new PDKs and seamless integration of novel components into existing libraries. This gives designers the freedom to enrich commercial PDKs or build entirely new libraries for emerging PIC technologies, enabling innovative applications and empowering fabless companies to develop secure, IP-protected internal PDKs.

The custom PDK library is automatically created from a template and includes all necessary features of a standard PDK, including design automation macros, schematic-to-layout conversion tools [7], and fabrication tolerance analysis capabilities [8]. Custom user interface toolbars allow for streamlined usability, while building block templates with links to their corresponding layout descriptions enable the layout-aware, schematic-driven design methodology (see Figure 2). Users can further customise this process to adapt the template models to their requirements.

System design

Today's datacentres communicate information across multiple scales – from intra-rack and intra-campus links to inter-campus connections spanning hundreds of kilometres [9]. Each tier demands unique optical interconnect solutions, such as coherent optical interconnects with advanced modulation formats (QPSK, 16QAM) and intensity-modulated direct-detection systems utilising PAM-M. Supporting such a wide range of applications requires powerful system-level simulation tools that must include models for transmitters, receivers, fibres, modulation and coding schemes, DSP elements, and dispersion mitigation techniques. Additionally, they should enable virtual testing environments that comply with industry standards and evaluate key performance metrics such as SER, bit error ratio, optical signal-to-noise ratio, Q-factor, and others.

VPItransmissionMaker Optical Systems [4] – the third pillar of our design framework – delivers a robust solution, offering an integrated simulation environment for diverse use cases, ranging from short-reach optical interconnects to metro/core networks, free-space optics, microwave photonics, and more. Supported by comprehensive model and application example libraries as well as advanced analysis capabilities, engineers can move confidently from concept to system validation in today's dynamic datacentre landscape.

Together, VPIdeviceDesigner, VPIcomponentMaker Photonic Circuits, and VPItransmissionMaker Optical Systems offer a complete design workflow. Historically, PIC research has focused primarily on individual device or circuit optimisation. Now, with the growing adoption of PICs in commercial applications, engineers are increasingly adopting a system-level approach, starting from high-level performance targets and deriving component requirements based on the overall application. Factors like required data

Unlike simplified datasheet models, advanced architectures demand physical-level simulations. The MRM response depends on resonant wavelength, free spectral range, extinction ratio, and tuning conditions – all affected by device geometry and material properties

rate, transmission distance, and channel spacing define parameters such as desired modulator bandwidth, Q-factor, and noise tolerance. However, due to the different nature and scale of the device, circuit, and system levels, it is challenging to combine simulations for them.

Optimising device geometry is a complex task that cannot always be done by modelling the behaviours of electromagnetic fields rigorously, due to the high computational and memory demands of these methods. But neither can the problem be solved in isolation from the target circuit performance.
To overcome these challenges, PIC design teams need a flexible equivalent compact model for accurate circuit-level simulation. VPIdeviceDesigner provides exactly this, by offering an automated transfer of the device simulation data into VPI Design Suite circuit-level analytical models and parametrised S-matrix representations.
The shared simulation environment also addresses the challenges that arise between the circuit and system levels.

Optical fibre models, for example, implement computationally efficient methods in the frequency domain, that only support periodic boundary conditions, where the signals display repeating patterns and the end of one segment smoothly joins up to the start of the next. However, modelling PICs often requires more complex time-domain simulations with aperiodic boundary conditions, meaning that the signal cannot be broken into a pattern of repeating segments.

To model long signal streams, as needed for system performance validation, engineers can use multi-run periodic simulations, breaking the stream into different chunks.

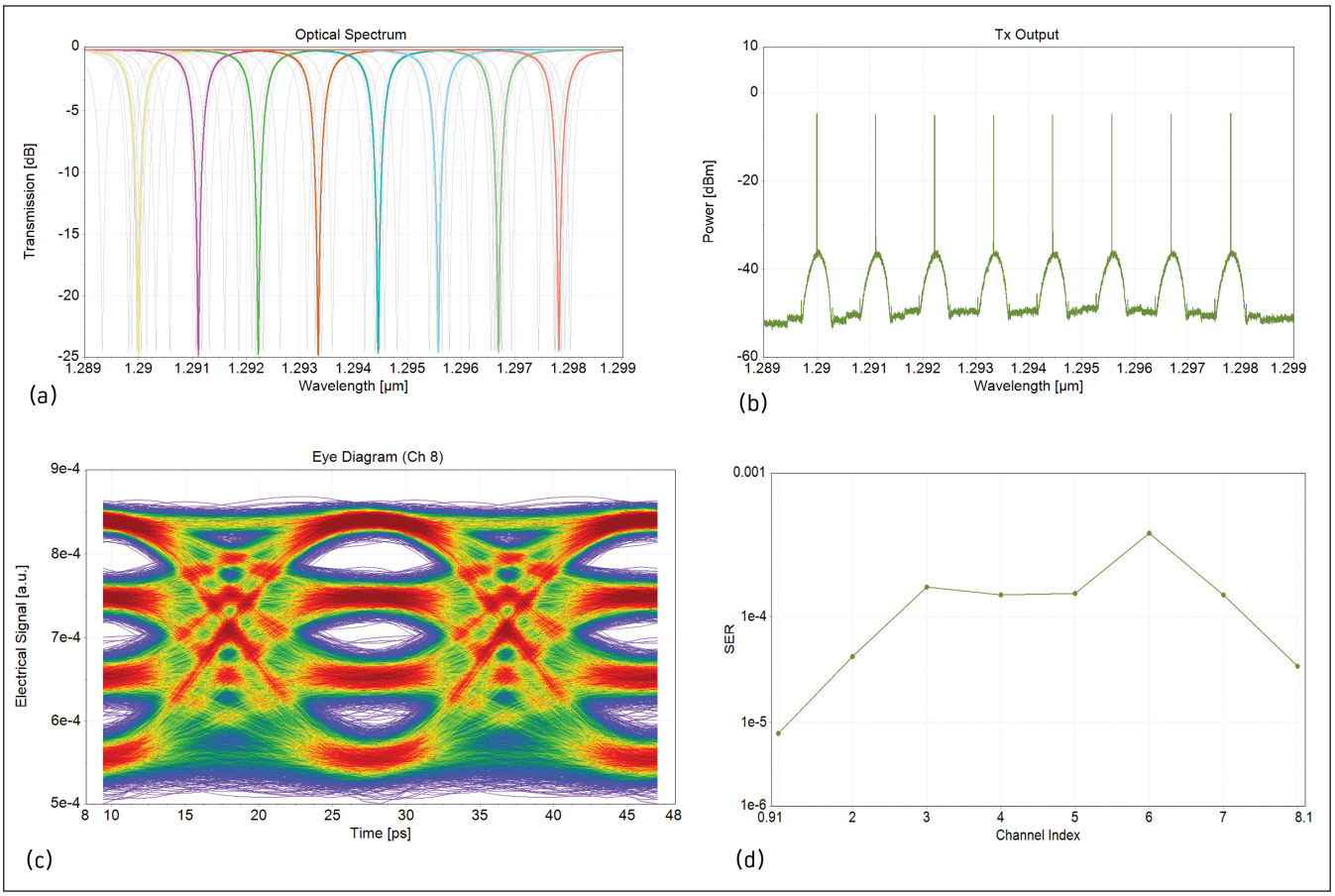
However, this approach can create artificial signal discontinuities at the break between one chunk and the next, due to the above-mentioned inherent aperiodicity of some of the circuit-level simulations. These discontinuities do not occur in the real data stream and can falsely deteriorate the assessed performance metrics, such as the SER.

To mitigate such numerical effects, the VPI Design Suite environment provides techniques for smoothing discontinuities, such as windowing, stitching, and the overlap-save method. It also offers signal conversion functionalities like resampling. These modules are important tools that are essential to the simulation setup, but they do not have physical counterparts in an actual PIC or system.

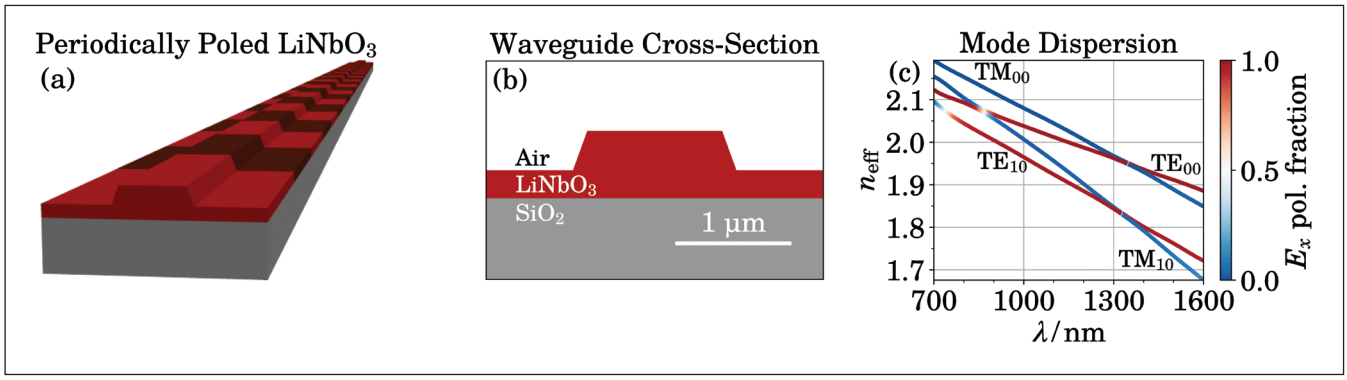
Finally, supporting faster and more memory-efficient algorithms for S-matrix assembly and dedicated time-and-frequency domain simulations [7] with a flexible frequency grid and advanced interpolation enables the simulation of large-scale PICs in complete system scenarios.

Application examples

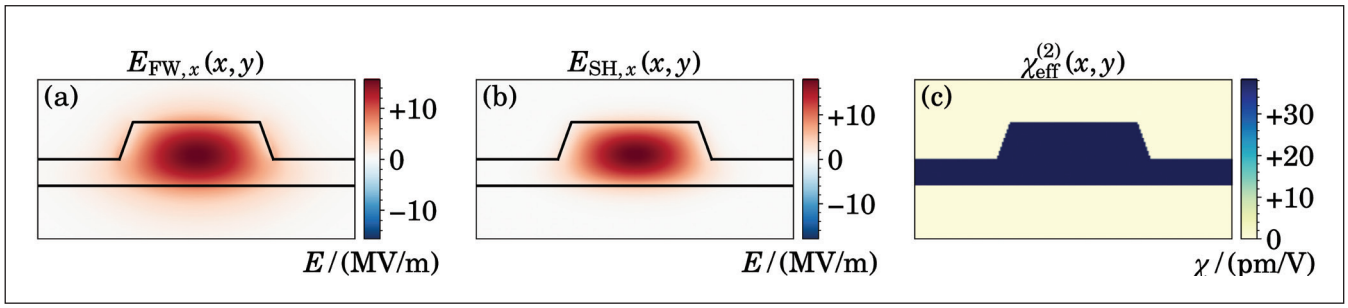
A powerful example of advanced system-level simulation is an 800G DWDM PAM-4 optical link leveraging silicon microring modulators (MRMs) and third-order microring resonator filters (MRRs) [1]. The system uses up to 8 laser channels at 200 GHz spacing,



➤ Figure 4. 8-channel DWDM PAM-4 transmission system simulation results: static MRM transfer functions including intermediate plots for the automated phase tuning (a), modulated optical spectrum at the transmitter output (b), eye diagram at the receiver for channel #8 (c), SER performance for all 8 channels (d).



➤ Figure 5. 3D impression of a PPLN waveguide (a), investigated lithium niobate waveguide cross-section (b), and waveguide mode dispersion (c).



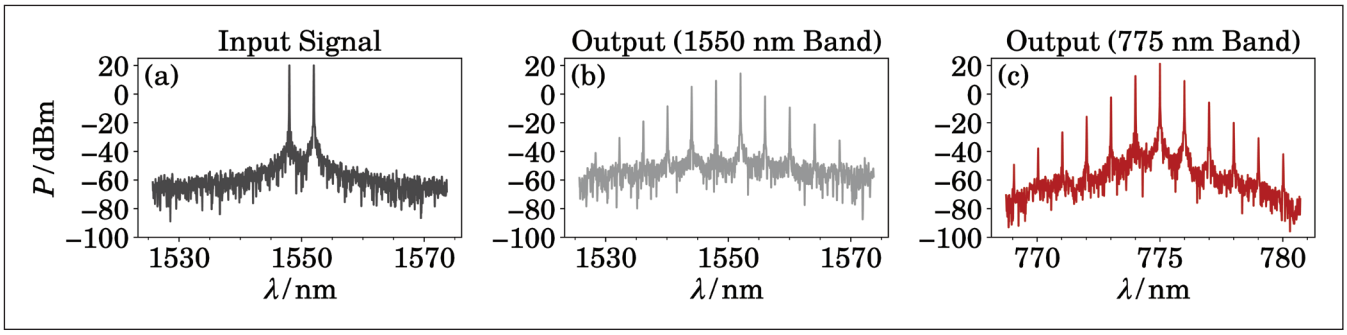
➤ Figure 6. Mode profile of the fundamental TE mode at 1550 nm (a), mode profile of the fundamental TE mode at 775 nm (b), and spatial distribution of the nonlinearity (c).

modulated by cascaded MRMs, transmitted over 2 km of single-mode fibre (SMF), and demultiplexed via MRRs before signal detection and SER estimation (Figure 3).

The design employs higher-order-function modules for scalable schematic generation, enabling quick reconfiguration (such as increasing channel count) without redrawing the circuit. Modules like SrcGr, ChainGr, and MapGr automate channel-wise source generation, modulation, and detection setup.

Unlike simplified datasheet models, advanced architectures demand physical-level simulations. The MRM response depends on resonant wavelength, free spectral range, extinction ratio, and tuning conditions – all affected by device geometry and material properties. To streamline tuning, dedicated test benches automate characterisation, optimising parameters such as microring radius, attenuation, coupling coefficients, and phase alignment.

The simulation, conducted in VPIphotonics Design Suite, integrates VPIcomponentMaker Photonic Circuits and VPItransmissionMaker Optical Systems, completing a full-system simulation run in about 32 seconds on



➤ Figure 7. Spectra of the optical signal in the simulation. In addition to the sum frequency at 775 nm and the two second harmonics, a few more lines appear due to the mutual interaction of the signals in the PPLN.

a standard desktop. Results include automatically tuned transfer spectra, eye diagrams, and SER across channels, offering insights into system performance under realistic conditions (Figure 4).

Another promising technology for datacentre interconnects is thin-film lithium niobate (TFLN). This material enables ultra-high-speed modulation with travelling-wave Mach-Zehnder modulators (MZMs), paving the way for data transmission beyond 1 Tbps.

We previously validated this through the simulation of a 2 Tbps single-polarisation DWDM 32 QAM coherent optical system for mid- and long-reach datacentre interconnects using TFLN MZMs in the IQ modulator [1]. TFLN is also an attractive platform for nonlinear conversion processes such as second-harmonic generation due to its strong second-order nonlinear coefficient.

Developing the corresponding TFLN-based PDK library requires the combination of accurate device-level and circuit-level simulations. As an example, we have modelled a periodically poled lithium niobate (PPLN) waveguide (Figures 5a-b). While the local conversion efficiency is determined by waveguide mode overlap integrals, which must be calculated on the level of Maxwell's equation, the propagation along the PPLN waveguide can span more than several millimetres and can involve broadband signals, requiring coupled-mode or split-step methods in circuit-level models.

VPIdeviceDesigner calculates the conversion efficiency in a single line of Python code (Figure 6), utilising the fact that calculated modes are feature-rich Python objects in VPIdeviceDesigner. The wavelength-dependent effective mode indices (Figure 5c) and conversion efficiency can be easily exported to VPIcomponentMaker Photonic Circuits.

In our simulation, the PPLN waveguide is excited with two laser lines spaced at 0.5 THz, which induce second-harmonic generation, sum frequency generation, and difference frequency generation in the PPLN. These effects are calculated using a multi-wavelength coupled-mode approach, as shown in Figure 7. This device-level data is then loaded into the circuit-level PPLN model for further use.

These are just two examples of how VPIphotonics' versatile platform can support designers in simulating and optimising various optical systems.

As the optical interconnect industry increasingly turns to heterogeneous fabrication platforms and hybrid integration technologies to meet the growing demand for high-speed components, system design is becoming increasingly complex.

There is now a critical need for integrated system and circuit co-design, in particular for scalable WDM architectures and advanced modulation schemes. By providing a complete solution for efficient device and circuit simulation, seamlessly moving from the smallest individual devices to the entire functional system, VPIphotonics is empowering designers to realise the future of optical communications.

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Image credit: Long Hua Dao

Harnessing sound waves for photonic neuromorphic computing

Optical neural networks could bring about sustainable, energy-efficient AI, but fulfilling this vision requires further advances in scalability and reconfigurability. Using sound waves in optical fibres and PICs offers one path to flexible, configurable, photonic deep learning units.

BY BY BIRGIT STILLER, PROFESSOR AT LEIBNIZ UNIVERSITY AND GROUP LEADER AT THE MAX PLANCK INSTITUTE FOR THE SCIENCE OF LIGHT

LAST YEAR, Microsoft made headlines when it signed a deal to buy energy from Three Mile Island, a nuclear power plant infamous for the accident that took place there in 1979. And Microsoft is not the only tech company seeking new ways to fulfil its soaring energy needs. Google and Meta have also been making deals to purchase power from nuclear facilities, while Google and Microsoft have even signed long-term agreements with nuclear fusion start-ups to secure future fusion-generated electricity.

These actions underscore just how much energy these companies are expecting to need for their power-hungry datacentres and AI applications. Large language models such as ChatGPT have already proven extremely useful across numerous industries and in our daily lives. A technology that might have seemed far-fetched just a few years ago has been adopted remarkably quickly, and the demand for AI services will only continue to grow. But providing access to them will require new technologies that speed up data processing and reduce energy consumption.

One potential solution arises from using optical devices, such as PICs or hybrid photonic-electronic chips, as the basis for new computing architectures. By using light instead of electrical

signals to represent data, optical neural networks could handle large volumes of information at high speeds and with great energy efficiency, forming the backbone of future AI systems.

Electrical signals travel comparatively quickly over short distances, meaning that the speed of light itself does not necessarily offer a huge advantage for computing. A more significant gain comes from the fact that light has many more parameters that can encode information; frequency, spatial modes, optical phase, and polarisation can all carry data simultaneously – an advantage that is already being harnessed in optical communications.

To date many of the experimental approaches to implementing optical neural networks have relied on fixed components and devices configured to manipulate light in specific ways.

These components may include resonator structures on a chip, huge interferometric networks made of photonic waveguides, arrangements of diffractive phase plates, or even metamaterials. It is possible to tune and train these elements, but for many of these setups, once a structure or device is fabricated there is limited room for reconfiguration. This lack of flexibility means that some devices can usually perform the task they were designed for and cannot be adapted for broader functions – an essential feature of the most useful AI models.

Now, let's take a break from photonics and think about sound: about acoustic waves. Acoustic waves have a completely different nature from optical signals, which are electromagnetic waves. Optical waves travel at high speed through materials and also through vacuums like outer space. Acoustic waves, on the other hand, travel a million times more slowly than light in air, and they do not travel through a vacuum at all; they need a material to propagate through. Optical and sound waves also have very different frequency ranges, with the former generally oscillating millions of times more per second than the latter.

Given all these dissimilarities, it may seem unlikely that pristine optical information could be captured in such a bulky, macroscopic thing as an acoustic wave. Yet the two forms of energy can in fact interact very efficiently via the refractive index of a material.

For example, in an acousto-optic modulator, sound waves periodically distort the material and change its refractive index, scattering incoming optical waves. Additionally, in certain materials, light waves can cause charged particles in the structure to move (a physical effect called electrostriction), and the resulting deformation can produce acoustic waves. These interactions offer an opportunity to modulate and control optical signals with sound.

Sound as memory

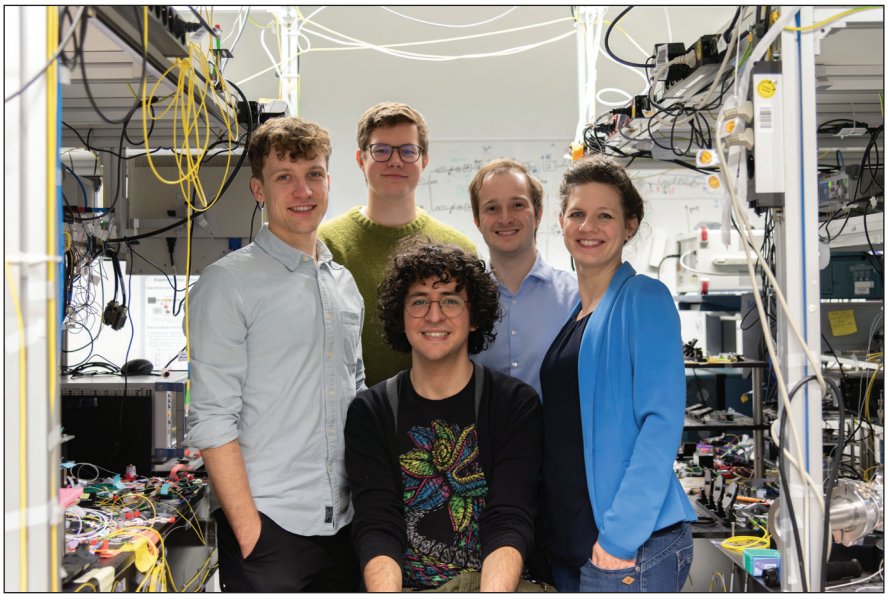
In our research on neuromorphic computing at the Leibniz University Hannover and Max Planck Institute for the Science of Light, our vision is to create neuromorphic hardware based on optical fibres and photonic chips that can be built and reconfigured by acoustic waves. To this end, we use stimulated Brillouin scattering – a phenomenon by which light and sound waves affect one another via the refractive index of a material.

By bringing the waves into interaction, we have found a way to build reconfigurable building blocks based on sound waves for photonic machine learning. With optical control pulses, we can generate coherent acoustic waves, which can then be used for various functions.

For example, they can be used to store information, serving as a temporary memory, to amplify certain signals, or to enable other functionalities such as recurrency and nonlinearity. These building blocks can be implemented in hair-thin optical fibres, already used globally for fast internet connections, or in photonic chips for potential hybrid integration with electronics.

The optoacoustic memory uses the fact that acoustic waves are slow and can therefore act like a parking slot for optical information. Additionally, these waves fulfil several other key requirements for an optical high-performance random-access memory: they are coherent, they are compatible with photonic chips, they can be tuned to different frequencies, and they have a high bandwidth.

The mechanism for transferring information from light waves to sound waves involves an optical data stream being sent into the optical fibre or photonic chip, while a second optical control pulse is sent from the other side. When these two counterpropagating waves collide, they create an acoustic wave that encodes the information from the data stream. This information is preserved in the acoustic domain until a second optical control pulse enters the medium and "reads" the sound wave, creating a corresponding optical wave again.



➤ Figure 1. Part of Birgit Stiller's research group, from left to right: Steven Becker, Niklas Braband, Jesus Humberto Marines Cabello, Andreas Geilen, Birgit Stiller. Photo: Susanne Viezens.

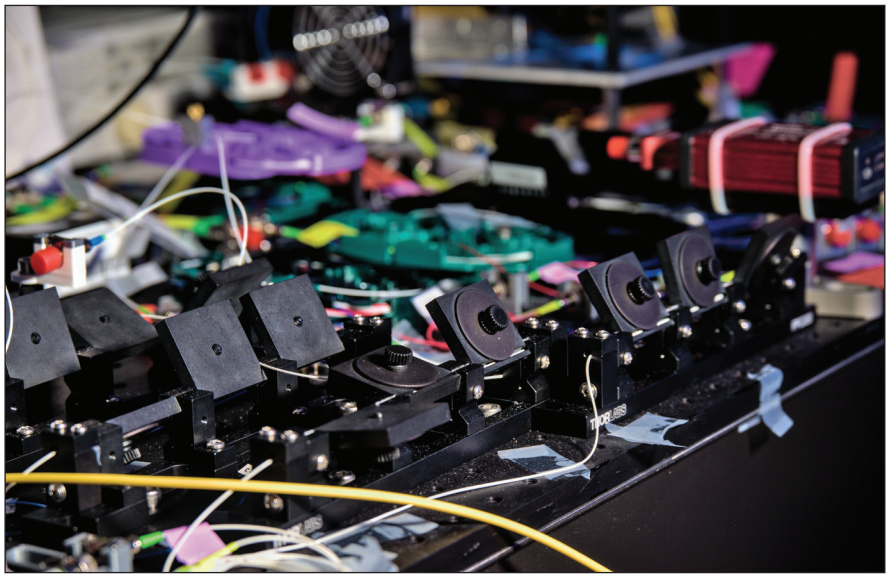


Photo credit: Max Gmelch.

➤ Figure 2. In photonic systems, sound waves can serve several different purposes, such as storing data in a temporary memory, amplifying certain signals, or introducing functions like recurrency and nonlinearity.

We have demonstrated that this memory is coherent in amplitude and phase, meaning that the data does not get lost or scrambled, and provides a high bandwidth up to the GHz range. The memory can also be accessed at high speed and be operated at different frequency channels at the same time with negligible crosstalk.

Because the acoustic waves only travel in one specific direction, this type of photonic memory is nonreciprocal, meaning that it is unaffected by counterpropagating signals and only interacts with the optical control pulse intended to read it. This property also allows for the nonreciprocal manipulation and potentially storage of specific types of light beams called orbital angular momentum modes, which can carry more information than standard light signals.

Recurrency and nonlinearity

Being so slow, acoustic waves remain in the medium much longer than optical waves, which makes them perfect candidates for recurrent neural networks – a type of architecture that is designed to process sequential data, in which the order of the data is important. For example, in human language, the order of words in a sentence affects its meaning. The two sentences "The cat hunts the mouse" and "The mouse hunts the cat" consist of the same words but have different meanings, indicated by the word orders.

A traditional fully connected neural network on a computer faces difficulties capturing this context because it requires access to memory. But recurrent operators feed the output of one calculation back as an additional input for the next, linking a series of computational steps and thus providing context for each single calculation performed. By equipping neural networks with recurrent operations, we can give systems internal memory and enable them to capture contextual information, overcoming the challenges associated with processing sequential data.

We have now used sound waves to implement such a recurrent operator.

Our Optoacoustic REcurrent Operator (OREO) harnesses the intrinsic properties of optical waveguides, meaning we can enable recurrent operations in the existing physical structures, without needing to add an artificial reservoir or any additional components. Unique to OREO is the advantage of being entirely controlled by light, making the optoacoustic computer programmable on a pulse-by-pulse basis, and eliminating the need for complicated structures or transducers to convert between signal types.

Another key ingredient of neural networks is an activation function – a nonlinear mathematical operation that takes the inputs to a particular neuron and determines its output. Examples of activation functions include ReLU, sigmoid, or tanh functions, which are commonly used to transform the weighted sum of inputs in an artificial neural network. Crucially, these functions introduce nonlinearity into the neuromorphic structure, which is essential for deep learning models to learn complex relationships between data and to be able to perform complex tasks.

In optical neural networks, nonlinear activation functions should ideally be implemented in the photonic domain, to avoid the typical conversion between optics and electronics, which would limit the benefits of using photonic hardware in the first place. When it comes to building larger optical neural networks, it might prove especially beneficial to have an all-optical activation function

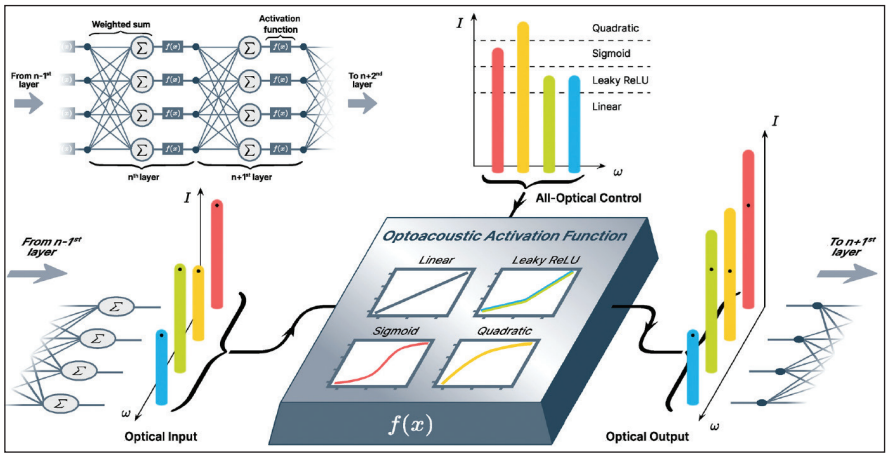


Image credit: Grigorii Slinkov.

➤ Figure 3. Nonlinear activation functions are essential for neural networks to learn complex patterns in data and to perform complex tasks. Acoustic waves can effectively mediate these types of functions in photonic architectures through their nonlinear interactions with light waves.

which can also be controlled all-optically, making the system more efficient and easier to scale.

For linear operations such as the weighted sum – a matrix operator – a plethora of photonic techniques already exist. But this is not the case for nonlinear activation functions, for which few approaches have been demonstrated experimentally. Here, acoustic waves could become an enabler because the effect is intrinsically nonlinear. Indeed, we have demonstrated that sound waves can be the mediator for an effective photonic activation function.

Once again, stimulated Brillouin scattering is the key; optical input information interacts with sound waves and undergoes a nonlinear change depending on the level of optical intensity. In this mechanism, the information does not have to leave the optical domain and is directly processed in optical fibres or photonic waveguides.

Besides avoiding electro-optic conversion and any associated loss or latency, including a photonic activation function in an optical neural network also preserves the bandwidth of the optical data and maintains the coherence of the signal. The versatile control of the nonlinear activation function with the help of sound waves allows the implementation of this process in existing optical fibre systems as well as photonic chips.

Future directions

With our recent European Research Council (ERC) Consolidator funding, we hope to scale up our approach and to achieve complete, reconfigurable computing architectures that might lead to fabrication-less AI. But, while AI may be our primary focus, it is not the only promising application of optoacoustics. Another research direction that the Stiller Lab is actively investigating is the quantum domain; here too, sound waves in optical waveguides could enable technological progress.

For instance, optically controlled acoustic waves could serve as a quantum memory for quantum information processing, as well as for quantum repeaters, which enable long-distance transmission of quantum information despite signal degradation.

We have now used sound waves to implement such a recurrent operator. Our Optoacoustic REcurrent Operator (OREO) harnesses the intrinsic properties of optical waveguides, meaning we can enable recurrent operations in the existing physical structures, without needing to add an artificial reservoir or any additional components

Interactions between light and sound waves could also generate the entanglement necessary for quantum communications.

In the first experimental demonstration of its kind, we have already proven that we can achieve strong coupling between optical and acoustic waves in waveguides – a prerequisite for quantum information processing.

Additionally, we have shown that our system exhibits high cooling rates, meaning it can cool down very quickly between operations, suppressing thermal noise that could interfere with quantum states. These experiments will ultimately enable optoacoustic memory for quantum states and entanglement between photons and phonons – "quanta" of vibrational energy that can be thought of as the sound-wave counterparts of photons.

Looking ahead, we believe that using acoustic waves for optical neural networks has great potential to unlock a new class of photonic neuromorphic computing which can be reconfigured spontaneously. On-chip implementations of optical neural networks can also benefit from this approach without additional electronic controls. Further down the line, combining both research avenues – quantum interactions and neuromorphic architectures – could create a powerful toolbox for quantum neuromorphic computing, helping to realise neural networks in photonic quantum hardware based on optical fibres or PICs.

As both the AI and quantum industries incorporate more photonics, adding in sound can help these transformative technologies to flourish in a sustainable way.

Photo credit: Stephan Spangenberg

➤ Figure 4. As well as enabling new architectures for AI, the optoacoustic phenomena being investigated by Stiller's research group could one day be used for quantum communication and quantum information processing.

Unlocking 3D-CPO: The industry's first double-sided electro-optical wafer tester

As the telecom industry adopts co-packaged optics at scale, ficonTEC has developed a product strategy that enables volume testing of next-generation optical engines for high-performance computing in datacentres

BY SUNG-HOON IM, PRODUCT MANAGEMENT DIRECTOR FOR PHOTONICS TEST, FICONTEC

AMID the continuing surge in data demands, co-packaged optics (CPO) has emerged as a game-changing solution to overcome the speed and power limitations of incumbent networking technologies.

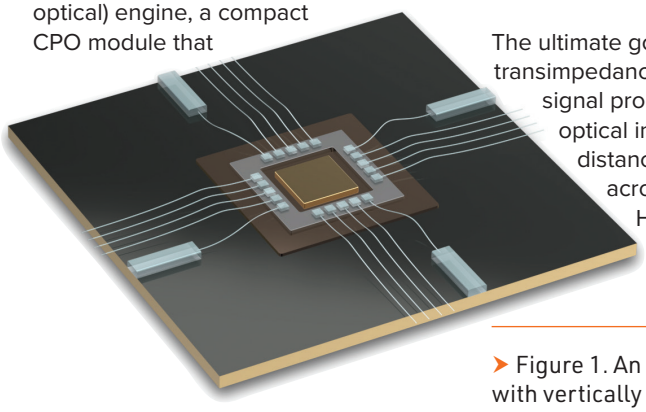
By moving optical transmission closer to the xPUs, CPO technology contributes significantly to improved operational latency and thermal efficiency compared with traditional chip-to-chip interconnects and high-performance switches. Moreover, this approach simultaneously reduces chip footprint and power demand, making datacentre infrastructure both more sustainable and scalable.

As the telecommunications industry races to make the most of these benefits by adopting more integrated solutions at scale, chip designers together with traditional foundries are increasingly exploring vertically stacked photonic and electronic dies.

Here, diverse second-generation "on-board optics" philosophies are already giving way to next-level CPO.

Central to this shift is the photonic (or optical) engine, a compact CPO module that vertically integrates photonic and electronic components. A prime example is TSMC's compact universal photonic engine, or COUPE wafer design and reconstituted wafers on PIC substrates, which integrate a PIC with one or more electronic ICs using 3D heterogeneous stacking or polymer overmolding.

The ultimate goal is to bring drivers, transimpedance amplifiers and digital signal processors closer to the optical interface, reducing link distances and power loss across the device (Figure 1). However, there are many potential pathways to reaching that goal.



➤ Figure 1. An illustration of 3D CPO with vertically stacked optical engines.

➤ Figure 2. ficonTEC's WLT-D2 double-sided wafer prober (lower right) integrated with a commercially available ATE. The wafer is located at the interface between the two systems.

In a departure from conventional single-sided chip designs, some innovative architectures require a wafer hybridisation approach that places optical and electrical functionality onto opposite sides of the wafer, yielding a so-called double-sided electro-optical wafer.

Yet as the level of integration increases, novel technologies like these introduce new complexities for the device-evaluation stage; testing both electrical and optical functionality with the required throughput becomes a formidable technical challenge.

For the double-sided wafers in particular, the obligatory test before device singulation requires a test solution capable of characterising optical and electrical performance simultaneously on the opposing sides of a wafer. Until recently, no existing tool had such capabilities. But now, ficonTEC has developed a test system that addresses exactly this need.

Double-sided wafer testing

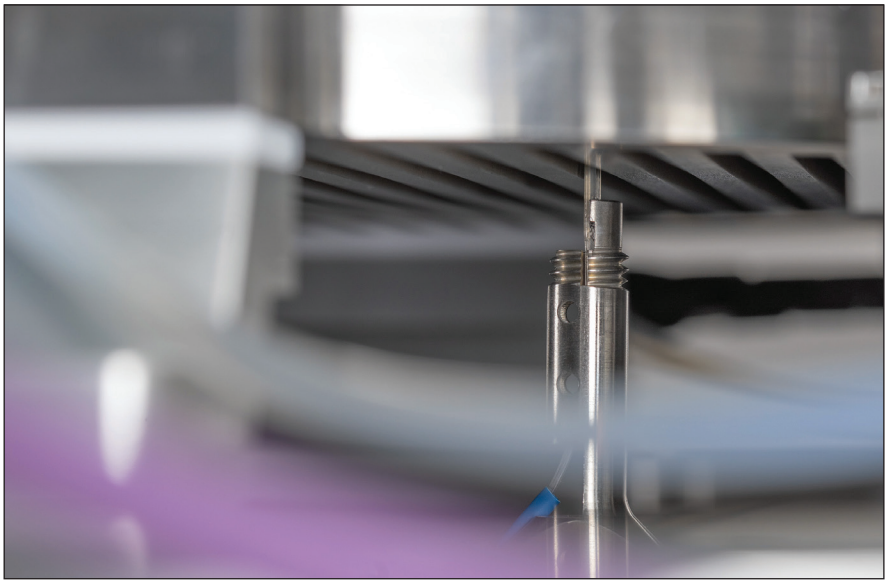
ficonTEC is the market leader in high-precision alignment and photonic device assembly automation, celebrating nearly 25 years of designing and manufacturing custom "align-&-attach" as well as "test-&-qualify" production solutions for R&D, new product introduction, and volume manufacturing. Within the last five years, ficonTEC has additionally gained valuable expertise with wafer-level test systems that have been successfully implemented in R&D settings, as well as by PIC development service providers such as VLC Photonics.

More recently, the demand for PIC device hybridisation and device test has been rapidly expanding to include true volume applications. This includes mainstream sectors such as sensors for automotive, for example, but so too in particular for telecommunications applications. For the latter, silicon photonics marks the convergence of PIC applications with established semiconductor technology, both in terms of application and manufacture.

To be adopted at scale in this context, the corresponding optical chip assembly and test production solutions must now be "industry ready". In other words, they must exhibit top-level reliability and be fully capable within a highly demanding foundry environment. This is a key condition that ficonTEC keeps in mind when designing its test solutions.

By leveraging its own extensive background in sub-micron optical alignment and drawing on the more recent expertise gained in wafer-level test systems, ficonTEC has developed a groundbreaking test system tool designed to enable probing both sides of a wafer simultaneously.

At the heart of this innovation is a newly designed prober platform that enables seamless integration with standard automated test equipment (ATE) as used in the semiconductor industry; while the ATE performs conventional electrical probing on one side of the wafer, the ficonTEC system



➤ Figure 3. Optical probe aligning to the bottom of the wafer through the slotted chuck.

ficonTEC's double-sided fully automated wafer prober marks a major milestone in enabling scalable CPO deployment. Further, it is a critical component of the company's larger vision to enable the future of a CPO manufacturing and test ecosystem

supports additional, high-precision, multi-channel optical probing on the other (Figure 2).

Designed for the fab

To support high-volume manufacturing and be "foundry capable", any solution must fully integrate on both a hardware and software level with existing, commercially available ATE setups. ATEs typically operate from the top of a prober for electrical-only testing.

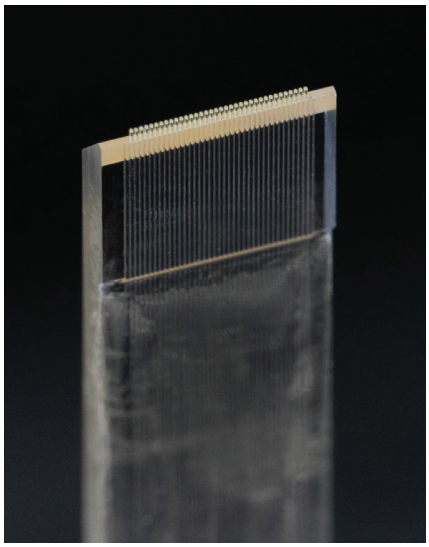
In order to enable simultaneous electro-optical probing with an ATE, the ficonTEC system offers up a custom wafer chuck to the ATE via a 4-axis motion system. This motion system provides the necessary control and precision for positioning the heavy chuck system complete with the sensitive wafer up against the ATE's fixed electrical probe.

To then successively access each individual device under test (DUT) across the wafer, the wafer chuck assembly is repeatedly traversed.

The system performs optical probing from below via slots in the wafer chuck whose pitch matches the optical I/O placement locations across the wafer. Beneath the chuck, a precision 6-axis alignment module holds a vertically oriented fibre array unit (FAU), which is then positioned to access the corresponding optical I/O location for the current DUT (Figure 3).

During this entire process the ATE remains the master, making the necessary calls to the ficonTEC system to move to the next DUT and to subsequently perform a synchronised electro-optical test, then repeating this process until the entire wafer has been verified.

The system operator must choose the optical coupling configuration – edge or grating couplers – to match the current DUT, and ficonTEC has developed a range of custom FAUs featuring micro-lens tips accordingly



➤ Figure 4. Custom designed multi-channel FAU with 3D printed micro-lens for beam steering and focusing.

(Figure 4). These micro-lenses, fabricated via high-precision 3D printing of organic polymers, refract the beam at the correct angles (usually between 5-23 degrees) while maintaining the alignment accuracy required for optical coupling.

A CPO test ecosystem

Beyond its optical and mechanical ingenuity, ficonTEC's double-sided prober was built for the rigours of high-throughput semiconductor fabs. It supports direct integration with leading ATE systems, ensuring customers can incorporate it while maintaining their existing test infrastructure. Auxiliary features such as probe tip inspection, FAU end-face inspection, automated tip cleaning, optical/electrical calibration, and wafer autoloaders further ensure manufacturing consistency.

Another critical component of wafer-level optical testing, and even semiconductor electrical testing, is cleanliness. Microscopic debris, in particular on an optical I/O, can degrade coupling efficiency, severely compromising the test procedure and ultimately directly impacting effective yield across the wafer.

To address diverse contamination issues, ficonTEC also offers a dry laser spot cleaning module using a 2.8 µm wavelength high-power pulsed laser from Femtum. As the silicon substrate is transparent at this wavelength, only contaminants absorb the laser energy and can therefore be selectively ablated.

ficonTEC's double-sided fully automated wafer prober marks a major milestone in enabling scalable CPO deployment. Further, it is a critical component of the company's larger vision to enable the future of a CPO manufacturing and test ecosystem. ficonTEC now offers a suite of test solutions spanning single-sided and double-sided wafer-level testing, as well as singulated die-level testing.

Looking toward the future, the company is currently developing a module-level test platform. Together with ficonTEC's other solutions, this platform will pave the way for a unified and streamlined test flow, supporting the entire product manufacturing cycle for high-performance optical engines.

As the industry continues its march toward 3D integration and CPO adoption, ficonTEC's innovations are setting the foundation to enable the high-yield, high-performance computing systems of tomorrow.

FURTHER READING / REFERENCE

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Accelerating toward the future of connectivity with photonic integration

The AI-driven surge in data traffic and disaggregated computing demand more integrated optical networking technologies. With expertise spanning photonics, packaging and testing, PICadvanced is uniquely positioned to create customised solutions and accelerate them from design to final product.

BY ANTÓNIO TEIXEIRA, CO-FOUNDER AND CSTO, PICADVANCED

IN A WORLD where digital transformation increasingly depends on the speed and efficiency of data movement, the pressure on telecom and datacom infrastructure has never been greater. The shift toward distributed computing systems and the race to support connectivity for growing AI usage demand not only more bandwidth, but also smarter, more integrated photonic solutions, such as co-packaged optics.

At the heart of this transformation is PICadvanced, a company that is redefining how optical systems are conceived, designed, and deployed.

Founded in 2014 and headquartered in the PCI – Creative Science Park in Ílhavo, Portugal, PICadvanced was born from a vision to revolutionise the future of telecommunications with PICs. What began as a bold idea quickly transformed into a reality, driven by a multidisciplinary team of more than 50 engineers dedicated to innovation in photonics, electronics, packaging, and system-level design and integration.

An early turning point in the company's journey came with the appearance in 2015 of the NG-PON2 standard, a crucial development in the evolution of passive optical networks (PON).

NG-PON2 represented a leap in bandwidth capabilities, supporting up to 4 x 10G symmetrical channels. This gave operators more flexibility to enable "pay as you grow", adding capacity as needed, to offer more services, and to provide a better quality of service for end users. To support this development, PICadvanced specifically created a unique set of end-user transceivers based on advanced components and assembled in traditional sub-mounts. These products combined compact form factors, energy efficiency, and cost-effective performance.

This was where the company's trajectory took off, but from the start we had our sights set on a broader goal: following the path toward more integrated solutions and building a sustainable future by further minimising footprint, power consumption, and cost. Pursuing this mission, the company has leveraged photonic integration to further reduce the number of discrete components in its transceivers, thus lowering insertion loss.

Another key milestone was the development of PICadvanced's multi-standard "combo" transceivers, capable of supporting various standards, including GPON (2.5G), XGS-PON (10G), and 50G-PON simultaneously. This versatility allows operators to upgrade more gradually, future-proofing their networks while ensuring co-existence of older and newer technologies to avoid

disruptions to service.
These innovations enabled PICadvanced to enter into a competitive market dominated by large-scale transceiver vendors. Rather than compete on scale, PICadvanced differentiates itself through customisation, speed of development, and tight integration between photonics, advanced packaging, electronics, and testing. To this end, the company has been developing the necessary tools to position itself as vertically integrated, conducting the process from design to final product, apart from the PIC fabrication stage itself. In this way, it acts as an accelerator between the fabs and the outsourced semiconductor assembly and test companies (OSATs) at a smaller scale.

Now, drawing on more than a decade of experience, PICadvanced is well positioned to enable the rapid transformation happening in the telecommunications industry today. As carriers deploy fibre deeper into networks and transition toward 50G-PON and beyond, having access to flexible, scalable, and energy-efficient optical transceivers is becoming mission-critical. At the same time, datacentres are moving toward disaggregated infrastructure, such as edge computing, and adopting terabit-scale optical interconnects to keep up with the explosive growth in AI workloads and high-performance computing.

Yet, while these changes are motivated by a need to increase data rates, achieving them requires developments in numerous other aspects of the technology. They demand integrated solutions that can meet stringent requirements not only for transmission speeds, but also for form factor, thermal management, signal fidelity, and cost. This is where PICadvanced stands out, bringing deep photonic design expertise, rapid prototyping, and scalable advanced packaging to meet the complex demands of next-generation infrastructure.

Tailored solutions

Dominated by several key players with global supply chains, the optoelectronic transceiver market requires continuous innovation as well as competitive pricing and ever-increasing performance to meet the demands of

Figure 1. PICadvanced cleanroom view: advanced packaging and testing at scale.

telecom operators and system vendors. PICadvanced's approach has been to position itself not as a transceiver manufacturer, but as a design and integration company with deep and advanced photonic capabilities.

By investing in proprietary IP, including photonic chip design, packaging platforms, and thermal management techniques, the company has been delivering flexible, high-performance solutions tailored to specific operator needs. As the underlying foundation of its work, the company has built a platform robust and adaptable enough to solve most of the electro-optic challenges found in today's high-speed PONs and datacentres.

In an industry where development cycles are critical, the ability to go from concept to prototype gives PICadvanced a distinct edge. Whether adapting a design for a specific optical architecture, or optimising packaging for thermal dissipation in dense environments, the company delivers with agility and flexibility. Unlike many players in the field, PICadvanced does not just assemble components; it builds solutions from the ground up. The company's fabless yet vertically integrated model enables it to innovate

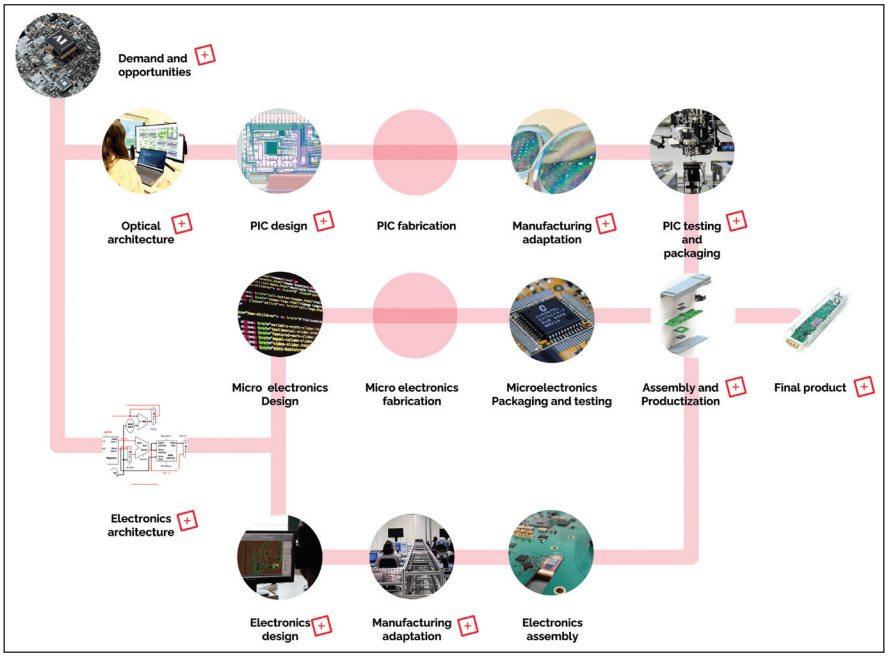
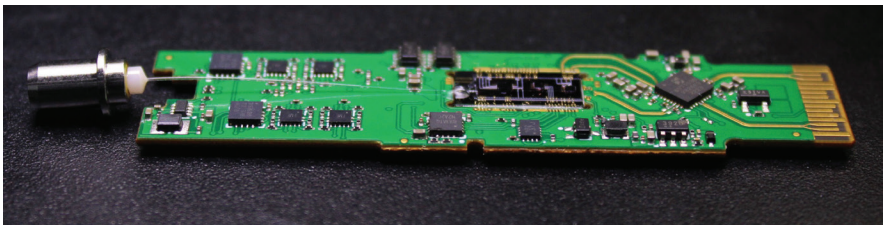


Figure 2. PICadvanced value chain: from optics, electronics and packaging to a product.



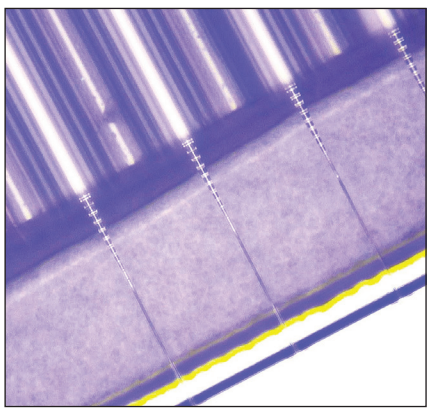
➤ Figure 3. Accelerator and aggregator: photonic-based optical transceiver for access networks.

across the value chain depicted in Figure 2.

This positioning allows PICadvanced to offer vertically integrated, rapid-turnaround development and customisation, with a feedback loop between design, fabrication, packaging, and testing. Such an integrated process ensures higher performance, lower cost for smaller productions, and faster time to market – all essential ingredients for competitiveness in both telecom and datacom applications.

Today, PICadvanced employs a team of around 50 highly skilled engineers and scientists, operating in one of the most complete PIC development pipelines in Europe. From design and simulation of photonic structures to full packaging and testing, the company serves as a cornerstone of the hybrid integration ecosystem.

A key enabler of this integration is PICadvanced's proprietary silicon-based packaging platform, which allows co-packaging and interoperability of photonic and electronic chips with high-density electrical interconnects, optical interfaces with multiple I/Os, and thermal control and management. The platform is supported by several methods and tools that have been developed in-house, as well as industry-grade equipment, ensuring high-precision die bonding on different platforms and materials, automated and low-loss fibre alignment, and pre- and post-assembly inspection covering 2.5D and 3D die alignment, and optical/electrical performance.



➤ Figure 4. Advanced packaging: photonic wire bonding towards a hybrid advanced packaging solution.

Complementing this is an internal suite of design and simulation tools spanning photonic, electronic, and thermal domains. These tools allow PICadvanced to simulate performance under real-world conditions and optimise across multiple variables – from bandwidth and power consumption to mechanical reliability and signal integrity. Additionally, the company's facilities also include an ISO7 cleanroom, and assembly and alignment labs with automated optical and electrical testing stations. This equipment provides accurate, high-resolution measurements and advanced packaging capabilities for creating prototypes and pre-series production lines.

Collaborative innovation

While NG-PON2 is now being deployed, PICadvanced is already focused on the next step in the progression of telecommunications networks and datacentres. As the industry moves toward 50G-PON, the company is at the forefront of developing compatible solutions that not only meet the necessary performance standards but go further by supporting combo transceivers – capable of handling multiple PON technologies within the same module. These products offer operators a flexible solution in managing upgrades alongside legacy compatibility, while minimising capital expenditure.

The datacentre space is entering a new era defined by optical switching, high-density interposers, and co-packaged optics. With bandwidth demands doubling every 18 months – fuelled by generative AI and edge workloads – optical integration must evolve in step.

PICadvanced is responding to these needs by contributing to the development of multiple new innovations, including optical interposers for Tbps optical links, advanced hybrid packaging for dense environments, and multi-domain simulations covering photonic, electronic, thermal, and mechanical dynamics. These technologies are being designed to support 200G data rates and beyond for short-reach interconnects, high-throughput switching platforms, and chiplet-based architectures. Through these projects, PICadvanced is becoming not just a supplier, but an innovation partner for hyperscale datacentres and AI infrastructure developers.

With more than 80 percent of its products and services exported to Europe and the US, PICadvanced is already a global player. Last year, the company opened its first international office in the US to support growing partnerships and gain closer proximity to some of the world's largest telecom and datacentre operators.

In an industry where performance, cost, and time to market often pull in opposite directions, PICadvanced has found a way to merge and optimise all three. The company's structure, expertise, and vertically integrated capabilities make it uniquely positioned to serve evolving telecom and datacom markets – from chip to product. By continuing to invest in its design, packaging, and integration capabilities – and by aiming for leadership in fast-growing areas – PICadvanced is not only transforming itself, but also helping to shape the broader communications industry and state-of-the-art networking technologies.

FURTHER READING / REFERENCE

➤ https://www.picadvanced.com

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Achieving precision for photonics with multi-chip bonding

With a focus on upcoming trends in advanced packaging, the new multi-chip bonding platform, MEGA, is the latest example of how ASMPT Semiconductor Solutions is pushing the boundaries of precision and speed in semiconductor manufacturing.

BY DAVID FELICETTI, PRODUCT MARKETING MANAGER, ASMPT

WE are currently witnessing a global transformation towards a world where machines autonomously interpret data, learn, and act, enabled by advanced technologies such as AI and the Internet of Things (IoT). This intelligence revolution, unfolding before our eyes, depends crucially on invisible connections between chips, between systems, and between technologies. As the semiconductor industry shifts its focus from simple transistor scaling to sophisticated system integration, ASMPT Semiconductor Solutions' comprehensive packaging portfolio stands at the centre of this evolution.

From automotive applications to datacentres, and from consumer devices to industrial systems, ASMPT's forward-looking solutions for advanced packaging and semiconductor assembly make it an enabler of the precise and reliable integration of diverse components into unified systems. These technologies form the foundation for the next generation of intelligent applications – especially in key areas such as AI, smart mobility, and hyperconnectivity.

AI is a good example of how applications are driving developments in chip design; as AI workloads grow increasingly complex, the connections between processing and memory elements are becoming critical bottlenecks.

To address this challenge ASMPT SEMI advanced packaging first-level interconnect solutions leverage technologies including mass reflow bonders, thermo-compression bonders with active oxide removal, and high-performance hybrid bonders that ensure maximum precision and reliability.

These solutions enable the creation of chip-on-wafer-on-substrate (CoWoS) packages that integrate AI logic processors with high-bandwidth memory, creating the high-speed, high-density connections that generative AI systems require. The advanced packaging techniques represent a fundamental shift in how computing systems are designed, moving beyond traditional planar architectures to three-dimensional structures that maximise both performance and efficiency.

Besides AI, advanced semiconductor packaging technologies also form the foundation of hyperconnectivity, enabling ultra-fast, reliable, and energy-efficient data transfers across IoT, 5G/6G telecommunications networks, datacentres, and vehicle-to-everything (V2X) communications that define the connected world. In these applications, where speed and bandwidth are key,

silicon photonics represents one of the most promising frontiers, using optical pulses instead of electrical signals to transmit data at unprecedented rates. Die-attach solutions for silicon photonics and co-packaged optics enable this revolution by providing the nanometre-precision connections these systems require.

Higher transmission speeds are not the only imperative that is driving advances in packaging technologies for photonics. Take, for example, the development from MEMS LiDAR to flash LiDAR. Whereas the former uses tiny mirrors to mechanically scan a laser beam across its surroundings, the latter illuminates its entire field of view at once with a flash of light and then captures the reflected signals simultaneously with a 2D array of detectors.

Creating flash LiDAR requires the manufacture of arrays of vertical cavity surface-emitting lasers (VCSELs) and single-photon avalanche diodes (SPADs). Both the transmitter array and the receiver silicon photomultiplier made from SPADs put the highest demands on placement accuracy and chip handling. Additionally, this application relies on highly precise alignment of lenses. These stringent requirements for photonics devices are challenging packaging engineers to push their technologies to the next level.

A versatile platform

A wide range of packaging innovations are available to realise high-performance integrated photonics devices, including wafer-level packaging, flip-chip bonding, through-silicon vias (TSVs), 2.5D/3D integration, system-in-package, and fan-out packaging. Machines such as those from ASMPT are available for all of these advanced packaging technologies and the associated work steps, and production lines can be set up to produce the chips.

ASMPT Semiconductor Solutions has set its sights on reducing the high space and energy requirements of such lines by using multi-chip module (MCM) type machines. While ASMPT may not be the only manufacturer with this goal, the MEGA MCM bonder achieves more in many respects than other solutions available to date.

The MEGA chip bonder platform is characterised by high flexibility, a modular design, and minimal space requirements (2550 × 2085 × 1970 mm). Two basic versions are available. The MEGA-G (where G stands for “general”) is designed for maximum speed, processing 12,000 units per hour with an accuracy of ±10 µm at a confidence level of 3σ. The more specialised MEGA-P (where P stands for “photonics”) achieves a reduced speed of 8,000 units per hour, but offers unparalleled precision of ± 2 µm and rotational accuracy of ± 0.1 degrees, both at a confidence level of 3σ. As the name suggests, ASMPT SEMI is targeting photonic manufacturers in particular with the latter device.

Even in the slower, photonics-focused version, MEGA has a higher throughput than competing machines for both die placement and flip chip. With automatic bond tool change, up to 10 bond tool buffers, and five ejector tools, this exceptionally versatile machine adapts quickly to new tasks. The MEGA platform offers various epoxy dispensers and stamp options, the ability to use multiple adhesives in parallel, and automatic switching between application variants.

For direct application, users can choose between dual dispensing, whereby adhesive deposits are applied line by line at high speed, and highly flexible all-in-one dispensing, whereby any epoxy pattern can be applied, for example for multi-chip applications. In addition, micro-jetting is available for applying low-viscosity epoxy resin, such as that mixed with phosphorus platelets, which is used in LED production.

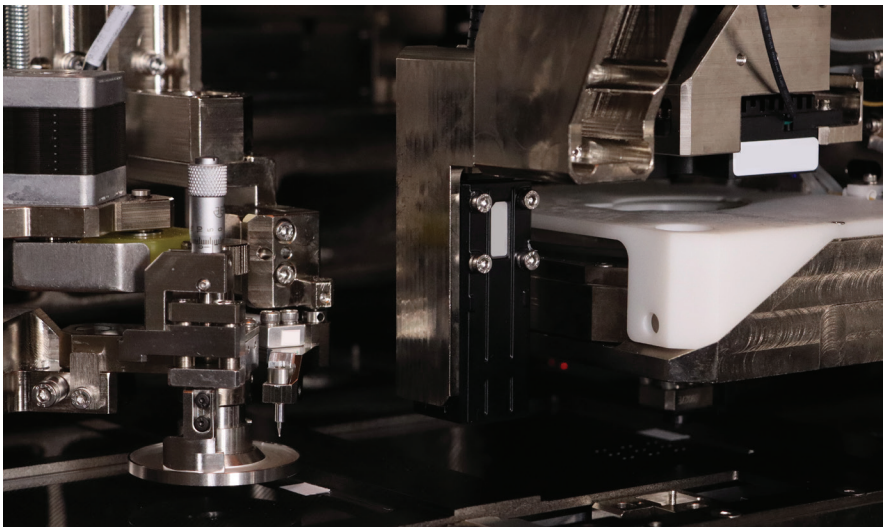
A special feature is the new 3D inspection of the epoxy application, which measures not only the height, but also the entire profile of the adhesive deposits. This is important, for instance, in high-precision applications where even the smallest changes in process parameters can lead to changes in adhesive behaviour and thus affect the bonding result. Another new feature is the optional instant epoxy stamping unit, which is located directly next to the bond head rather than on the other dispensers. This instant unit provides immediate fixation through UV curing – a major advantage when placing the above-mentioned lenses on optoelectronic multi-chip modules, for example.

Precision and flexibility

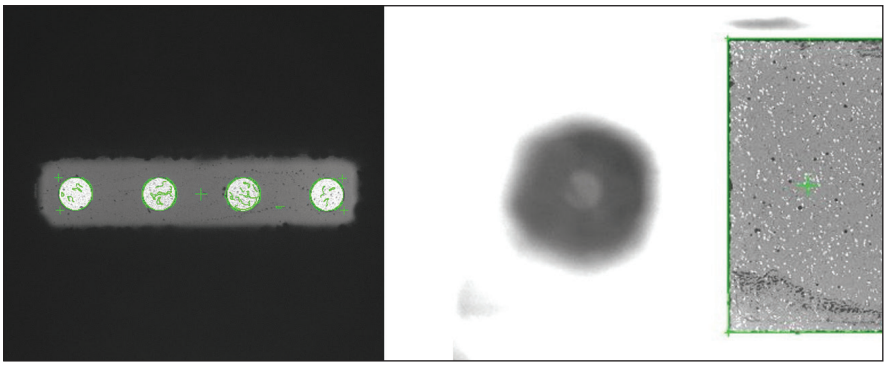
The MEGA-P achieves its high accuracy of ± 2 µm with its patented High Precision Bond Head. The look-through bond head allows visual inspection during the process, with pattern-recognition vision systems using the visible edges of the die to determine whether it is being applied correctly. The automatic theta correction and inline quality control ultimately ensure that the machine can achieve a rotational alignment accuracy of ± 0.1 degrees at 3σ. Another detail that increases accuracy is a counterweight that moves back and forth to compensate for vibrations that could otherwise occur due to the rapid movements of the bond head in the machine.

An important design principle of the ASMPT machine is the division of movements and tasks to increase flexibility and shorten distances travelled. The bond track and dispense

➤ Figure 1. ASMPT’s multi-chip module die-bonder platform, MEGA.



➤ Figure 2. MEGA's all-in-one dispense and stamping tool (left) and look-through bond head (right).



➤ Figure 3. ASMPT's look-through bond head is capable of looking at die edges or at fiducials on the component surface to improve angular and placement accuracy.

track move independently of each other, not only in a linear fashion as is usually the case, but also in the x and y directions. The machine can perform dispensing and bonding in parallel without the processes interfering with each other.

This also shortens the distances travelled by the bond head and thus also the travel times.

The decoupling of the chip pickup from the wafer and its placement is highly important too. The picking and bonding arms work independently of each other, allowing space for a flip-pick arm and a rotation unit between them. The rotation unit is used for angle correction and makes a significant contribution to precise alignment. Since even a slight rotation can lead to incorrect positions in the outer areas, this angular correction increases precision, especially for elongated chips.

MEGA also demonstrates flexibility in wafer feeding and die and substrate handling. For example, dies can be fed using waffle packs, gel packs, or an optional tape feeder station. The multi-chip bonder processes wafers up to 12 inches and dies from 0.15 × 0.15 mm to 10 × 10 mm, as well as substrates up to 130 × 300 mm.

Moreover, the machine's customisable options meet the packaging requirements of demanding multi-chip components, making the bonder the first choice for optical transceivers, photonics, sensors, and many other forward-looking applications.

"The MEGA multi-chip bonder performs tasks in a single machine that previously required an entire line of machines," explains Johann Weinhändler, regional head of ASMPT Semiconductor Solutions Europe and managing director of ASMPT AMICRA in Regensburg, Germany.

"We have made sure that chip manufacturers still retain maximum flexibility. The modular design also allows for customised equipment, so that no one has to buy functions they don't need."

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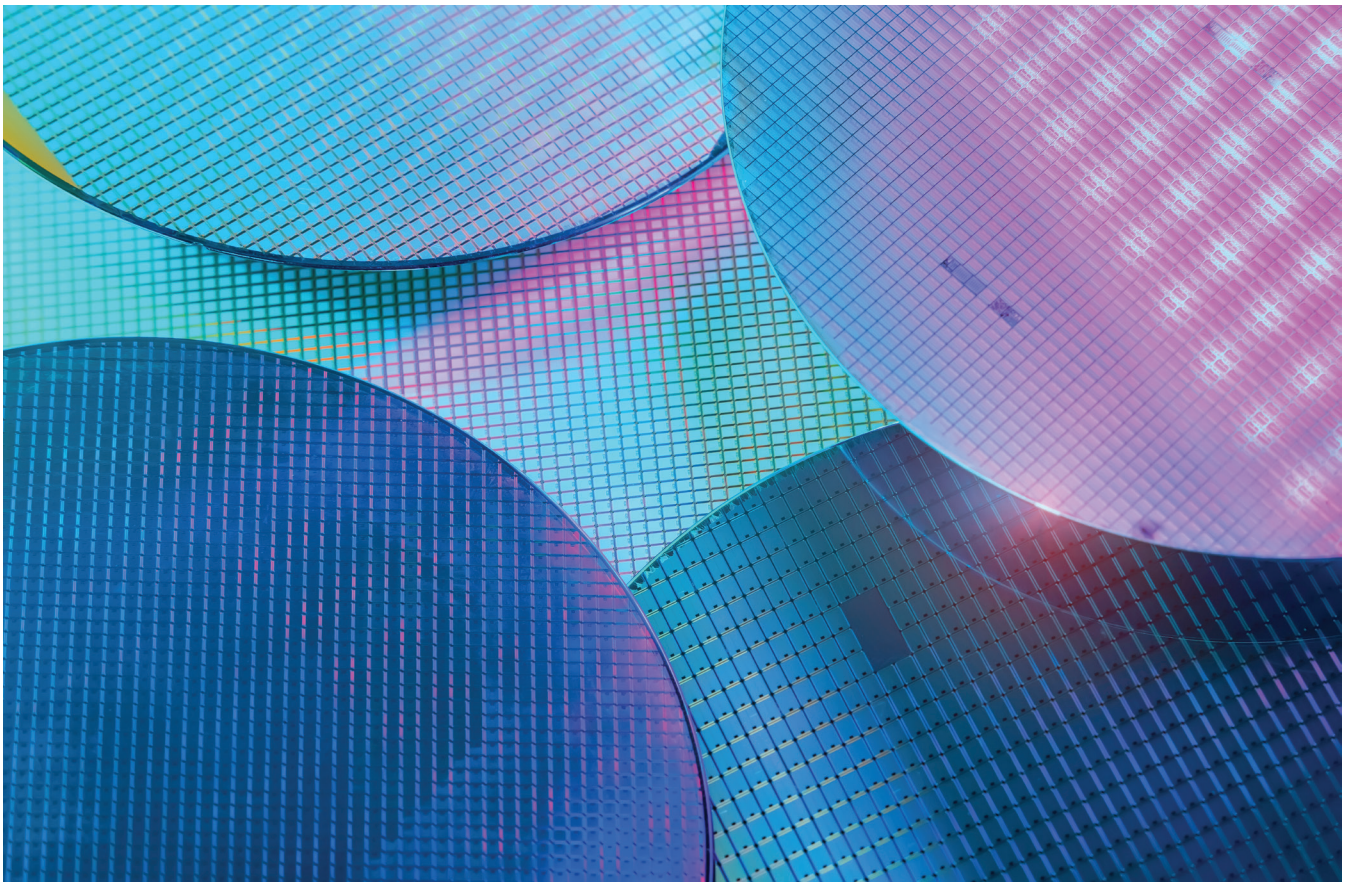


Shaping the future of cloud AI with silicon photonics

Silicon photonics is transforming Cloud AI with high-speed, energy-efficient data movement. Soitec's Photonics-SOI engineered substrates are key enablers, enhancing performance, scalability, and integration for next-gen AI infrastructures.

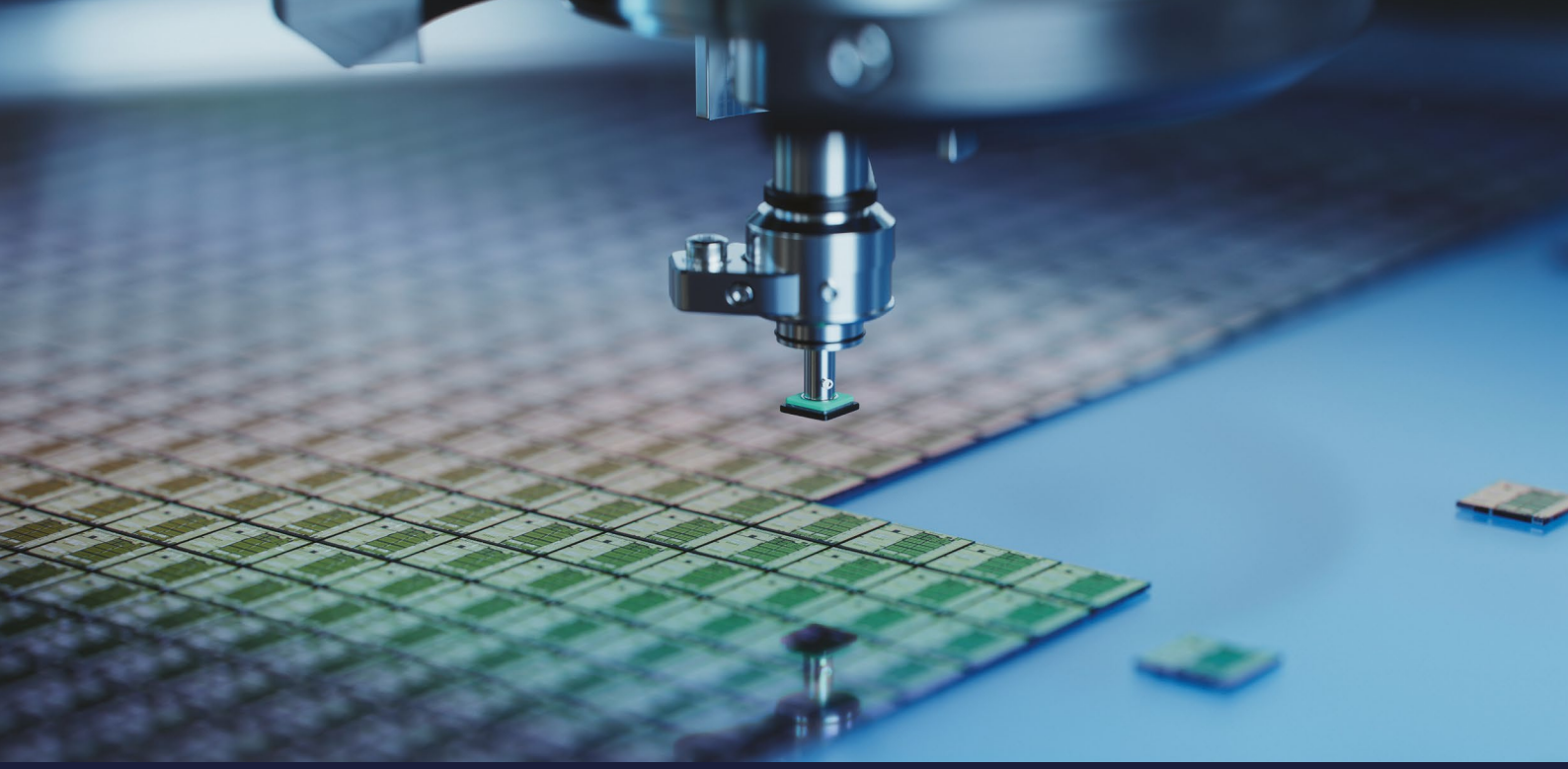
BY RENÉ JONKER, EXECUTIVE VICE PRESIDENT OF EDGE & CLOUD AI DIVISION, SOITEC

CLOUD-BASED AI has become a cornerstone of digital transformation. From natural language processing to computer vision, large-scale AI models hosted in hyperscale datacentres are delivering unprecedented value across a wide array of industries. However, as these models grow in complexity and size, the infrastructure supporting them is approaching critical bottlenecks.

Two dominant challenges define the current landscape: bandwidth limitations and excessive power consumption. Training and deploying AI models involves massive data exchange between GPUs, CPUs, memory, and storage. Traditional electrical interconnects are struggling to scale bandwidth to the necessary levels to support frontier models without increasing latency.

Those same interconnects in modern AI datacentres currently consume over 30 percent of total system power. As AI usage continues to grow, this number is projected to rise, threatening sustainability goals as well as the economic viability of operating AI models. Table 1 shows the energy consumption of large language models like ChatGPT based on carbon emissions associated with electricity production. This emission is equivalent to driving an average passenger vehicle for approximately 2,190,000 km (GPT-3), 3,650,000 km (GPT-4), or 7,300,000 km (GPT-5), using the EPA's estimate of 0.25 kg CO_2 per km.

These challenges underscore an urgent need for a new paradigm in data movement – one that combines speed, energy efficiency, and scalability. And this is where silicon photonics comes in, moving data at high speeds within and between chips, using silicon as the optical medium. Compared with traditional copper-based electrical connections, photonic interconnects



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Calculation	Value (GPT-3)	Value (GPT-4)	Value (GPT-5)
Total Annual Energy Consumption	1,095,000 kWh	1,825,000 kWh	3,650,000 kWh
Carbon Intensity (Averaged)	0.5 kg CO_2 / kWh	0.5 kg CO_2 / kWh	0.5 kg CO_2 / kWh
Annual Carbon Emissions	547,500 kg CO_2	912,500 kg CO_2	1,825,000 kg CO_2

➤ Table 1. Comparison of energy consumption of AI models (Source: Baeldung).

can transmit data with significantly less energy loss and higher bandwidth, all while leveraging the mature silicon CMOS fabrication ecosystem.

Current pluggable optics achieve data rates exceeding 800G for scale-out networking, with roadmap projections reaching several terabits per second in the coming years. Such pluggable optics consume roughly 15-20 pJ/bit. As the compute and data rate requirements grow along with the ever-increasing model sizes, new architectures will be required to further improve the energy efficiency of just moving data within the compute clusters.

This is where co-packaged optics (CPO) comes in. This technology integrates optical engines close to, or alongside, the ASIC within the same package. This shortens the length of high-speed electrical traces and thus reduces power loss and signal degradation. Such implementations reduce energy consumed to 5-7 pJ/bit, while future advancements in semiconductor packaging technology will likely bring further improvements to cross the sub-1 pJ/bit barrier.

From a system point of view, bringing the optics closer to the ASIC – as represented in Figure 2 - helps to shrink the system footprint, offering higher bandwidth density and enabling scalable designs for larger AI clusters. Additionally, even if the optics in CPO devices are within the same module as the electronics, they are not fully integrated on the same silicon die. This means there is still an element of modularity, facilitating easier future upgrades without requiring an entire system redesign.

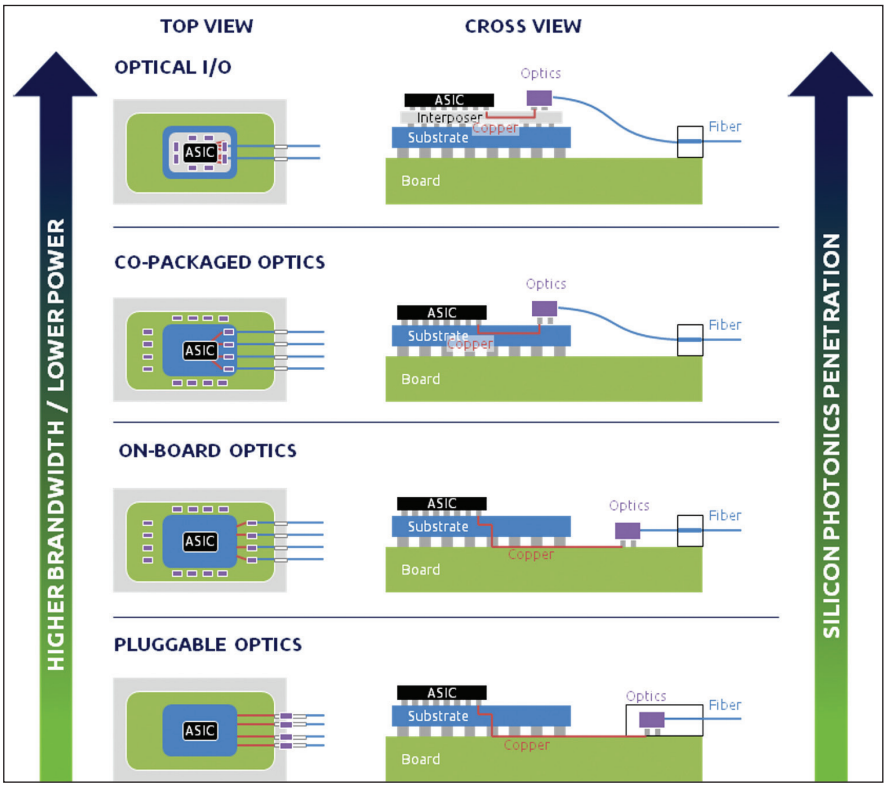


Figure 1. From pluggable optics to CPOs & OIOs.

Soitec's role in the ecosystem

The success of silicon photonics in cloud AI does not rest on a single player, but rather on a collaborative ecosystem, connected by strategic partnerships across the value chain. The key players at the design and fabrication stage include foundries for scalable chip production as well as design houses and research and technology organisations for innovative optical IP blocks. Once the chip is made, it requires packaging experts for high-precision alignment and thermal management, and system integrators for AI-scale deployment.

Soitec's substrates are at the heart of this ecosystem, enabling wafer-level integration and performance consistency across global photonics fabs, and thus facilitating the large-scale adoption of silicon photonics. In particular, the Smart Cut technology pioneered by Soitec and CEA-Leti offers an unmatched method for producing substrates of exceptionally high quality.

Smart Cut is Soitec's proprietary wafer bonding and layer transfer technology used to produce engineered substrates like SOI (silicon-on-insulator). It works by implanting hydrogen ions into a donor wafer, bonding it to a handle wafer, and then splitting off a thin active layer. The remaining donor wafer can be reused, enhancing cost efficiency. This enables precise control of layer thickness and uniformity, critical when designing and producing waveguides for photonics applications, with high performance and yield at scale.

Soitec's Photonics-SOI substrates are specifically engineered with a top mono-crystalline silicon layer ("device layer") with precise thickness control, commonly about 220 nm or 340 nm.

Below this top layer, the substrates have a buried oxide layer (“BOX”) of optimised thickness (typically 2–3 µm) critical for optimal fibre edge coupling, and a low-defect and high-uniformity silicon base wafer. This layered structure, illustrated in Figure 3, is critical for defining single-mode waveguides with high precision, essential for dense, low-crosstalk optical routing.

Additionally, the large refractive index contrast between top silicon (typically about 3.48) and silicon dioxide “BOX” (typically about 1.44) in the SOI stack provides strong optical confinement. This minimises mode spreading, enables small bending radii, supporting compact layouts, and facilitates high-density photonic integration (critical in transceivers, switches, and CPO architectures).

Finally, low optical propagation loss is ensured thanks to ultra-smooth silicon surfaces and interfaces. This is essential for minimising scattering loss in waveguides, ensuring <1 dB/cm propagation losses in optimised designs, and supporting high-Q resonators and interferometers with minimal insertion loss.

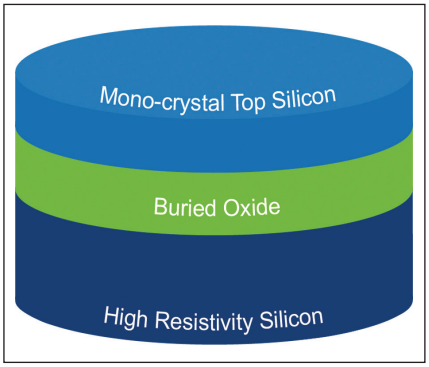
Thanks to the advantages outlined above, Soitec’s substrates are used by leading integrated photonics designers and system providers, bridging semiconductor and photonic ecosystems. This in turn underpins the adoption of silicon photonics in real-world applications, which is already happening in AI supercomputing clusters and optical I/O for accelerators.

Vision for the future

The exponential growth of AI, particularly in the cloud, demands an equally transformative shift in how data moves. This will only be compounded as AI evolves toward real-time reasoning, edge-to-cloud learning loops, and trillion-parameter models. Providing the essential ingredients of speed, efficiency, and integration, silicon photonics will become a non-negotiable foundation for performance and sustainability, overcoming the limitations of electrical interconnects.

In the coming years, we expect to see the mass adoption of CPO in hyperscale environments, new hybrid compute-photonic architectures, and photonic AI chips using light for both communication and computation. Soitec’s contributions at the materials level are pivotal. By providing substrates optimised for optical performance and semiconductor integration, Soitec ensures that the promise of silicon photonics can scale globally and reliably.

Adding to this roadmap, Soitec is preparing to launch lithium niobate on insulator (also called LNOI and TFLN) – a new engineered substrate platform aimed at unlocking ultra-fast, low-loss electro-optic modulation and nonlinear photonic functions. LNOI will be targeting high-speed modulators starting at 1.6T (200G per lane) with main adoption planned for 3.2T (400G per lane), driven by superior modulation bandwidth and ultra-low drive voltage compared to incumbent technologies. The possibility of hybrid and heterogenous integrations with silicon photonics will make Soitec’s LNOI platform a real boon to integrated photonics adoption.



➤ Figure 2. Layered structure of a photonics-SOI substrate.

This innovation signals an even broader vision: a heterogeneous photonics future where multiple materials and functions are integrated at the wafer level to meet the demands of AI, quantum computing, and next-generation communications. With its growing portfolio of advanced materials, Soitec is not just supporting the evolution of silicon photonics but actively shaping the future of optical technologies. The future of cloud AI is bright – literally – and it’s being realised, in part, by the photons travelling through Soitec’s engineered substrates!

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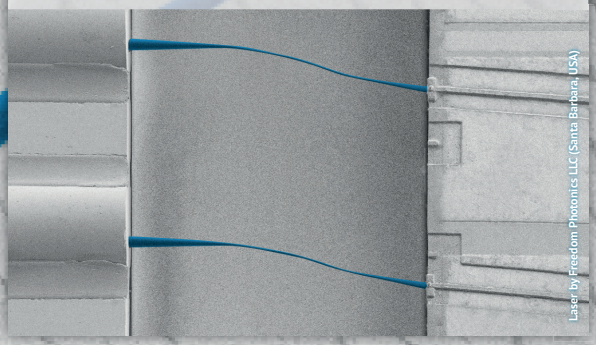
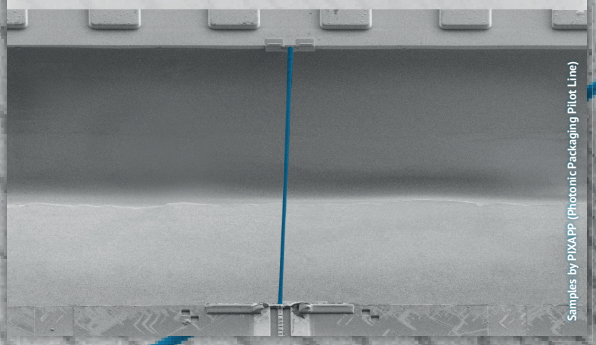


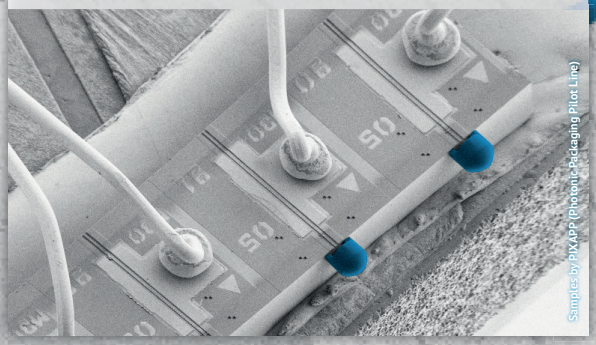
Laser by Freedom Photonics LLC (Santa Barbara, USA)

Laser to SOI chip



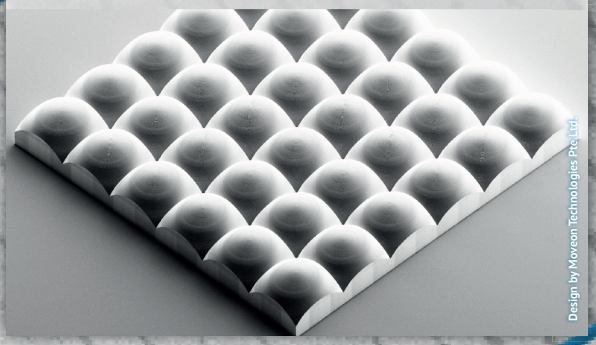
Samples by PIXAPP (Photonic Packaging Pilot Line)

Lens on laser



Samples by PIXAPP (Photonic Packaging Pilot Line)

Large scale micro-optics



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