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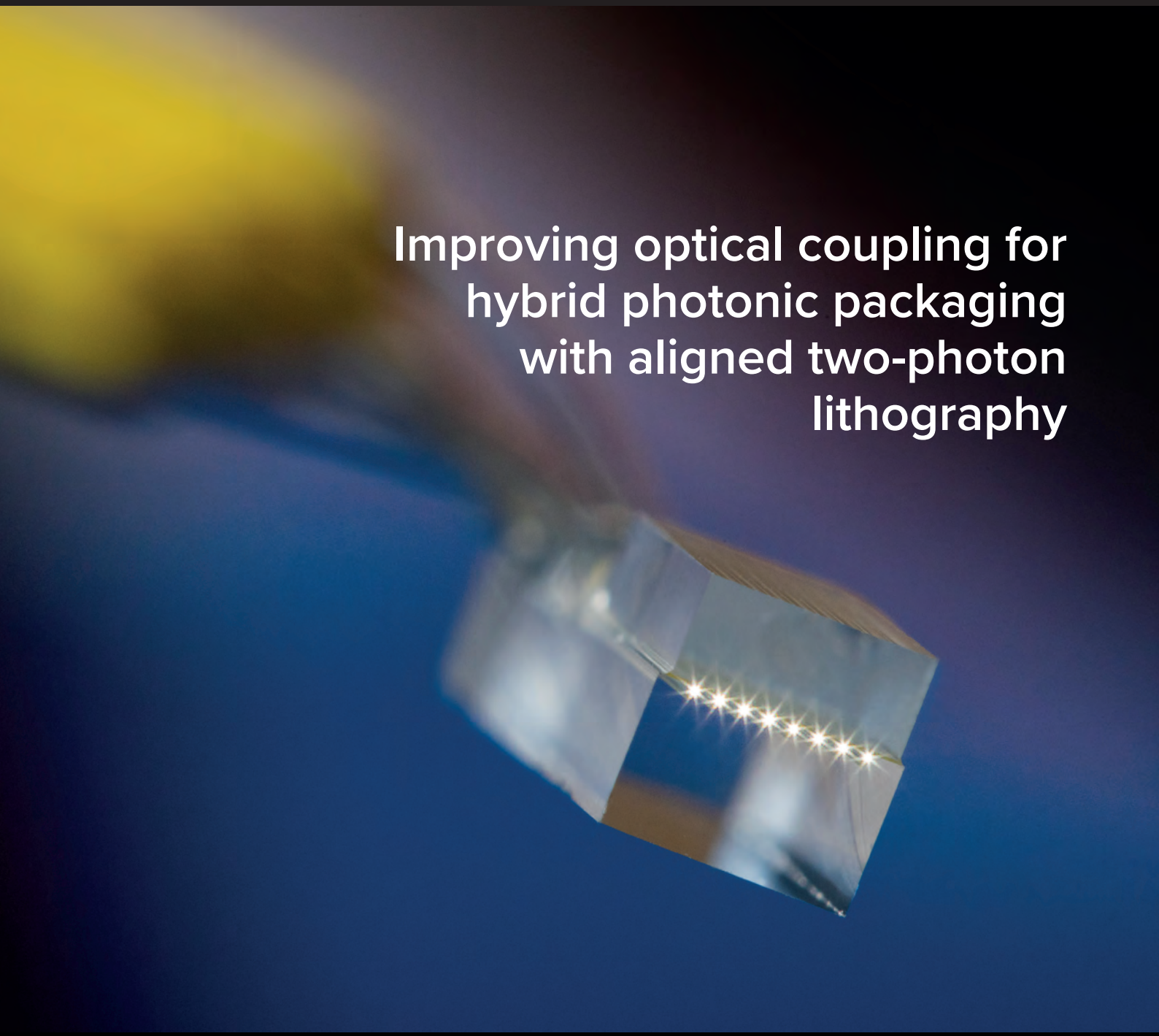

Improving optical coupling for hybrid photonic packaging with aligned two-photon lithography

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VIEWPOINT

By Mark Andrews Technical Editor

Photonic integration & packaging are key to next-gen PICs

WITH THE ECOC CONFERENCE behind us, industry innovators are again focused on seeing that PICs and SiP devices form the fastest growing, most exciting sectors within advanced technology. In this PIC Magazine we focus on packaging, integration, component coupling and strategies for incorporating photonic devices into more applications.

While photonic components including PICs offer many advantages, they also present challenges. The photonics ecosystem began evolving in the 1980s while SiP devices and PICs are 21st century products. Microelectronics began evolving 20 years earlier than the oldest photonic devices, meaning that IC makers have had ample time to develop the standards, practices and processes that have made microelectronics so successful. And while photonic device makers are building on the successes of their microelectronic cousins, the unique packaging, test and assembly requirements within photonics leads the list of 'must-have' solutions.

Nanoscribe and its 3D polymer microfabrication system offers unique solutions to vexing integration issues including optical coupling and packaging for hybrid integrated components. Nanoscribe believes any technology that eases or eliminates coupling complaints is a big step towards making PICs practical for high volume manufacturing (HVM) applications. By leveraging its expertise in two-photon polymerization, Nanoscribe can provide coupling functionality at extreme precision yet without the costly active alignment techniques others utilize.

Also in this edition we hear from EV Group's Andrea Kneidinger who discusses work that her company undertook with Teramount to develop microstructures for faster and easier fiber-to-chip assembly. The EV Group/Teramount team went on to develop microstructures using a simple, reliable and cost-effective wafer-level replication process that enables full production and the scaling needed for HVM.

We also look at the work Vanguard Automation GmbH has done in creating new types of photonic component coupling. Vanguard's new program leverages wire bonding tech – the same 'family' of bonding processes used to connect legacy microelectronic die within modules. The Vanguard approach utilizes nano-printed polymer waveguides to create what it calls Photonic Wire Bonds (PWBs). Using lasers to polymerize photoresist, Vanguard's system can build a connection between any two target points, eliminating the need to physically align fibers with device inputs and outputs.

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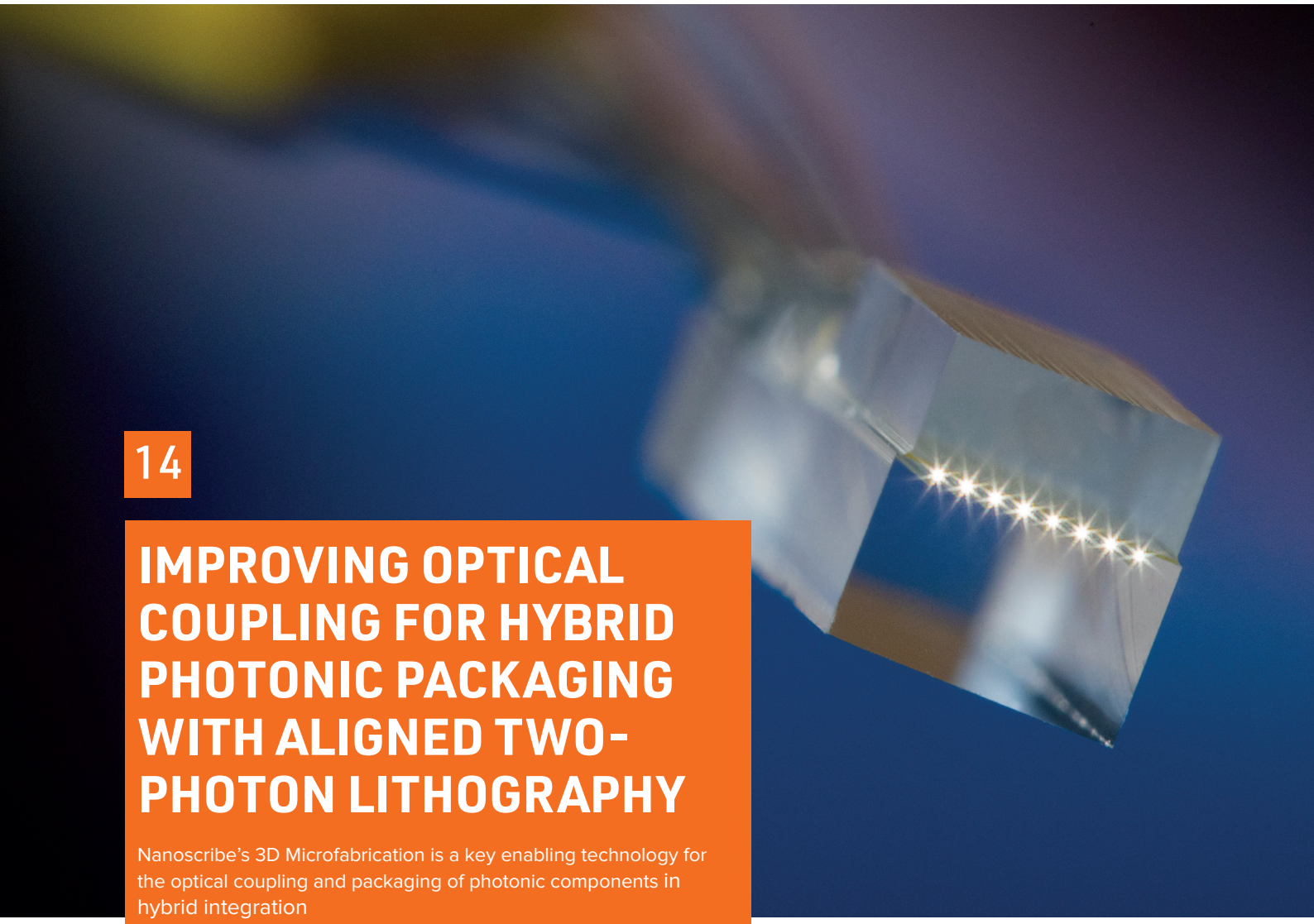

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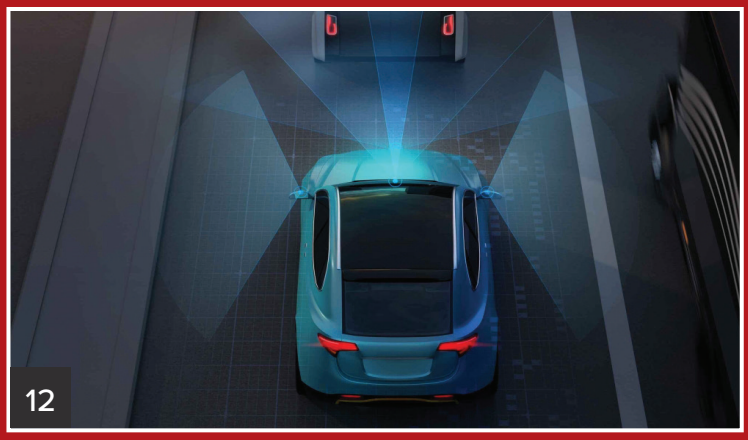

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Angel BUSINESS COMMUNICATIONS

POET announces 800G and 1.6T optical engines

Company announces Optical Engines with high-speed DMLs and photodiodes

Photonics firm POET Technologies has announced that it will use Directly Modulated Lasers (DMLs) in its optical engines for 800G and 1.6T pluggable transceivers for hyperscale data centres.

The DMLs will be combined with integrated drivers in POET's transmit optical engines. High-speed photodiodes and integrated Transimpedance Amplifiers (TIAs) will be used in its receive optical engines. The approach will enable low power, cost-efficient and highly scalable 800G and 1.6T pluggable transceivers for hyperscale data centres, according to the company.

POET's optical engines will be the industry's first implementation of DMLs at these data rates. The company will use the DMLs for its modulator-free design of the POET 400G transmit engine. It says the small size and chip-on-board design will allow 800G and 1.6T designs to easily fit in an industry-standard 1.6T OSFP-XD form factor.

DML technology has a proven track record of enabling high volume transceiver deployments at every

generation of speeds in hyperscale data centres. The 100G PAM4 DML passively integrated on the POET Optical Engine not only addresses current 400G solutions at mass volume but also enables future intra-data centre interconnects as the industry moves to higher speeds.

"POET's Optical Engines are 'photonic chiplets,' unique to POET, which enable a scalable, elegant solution to module design that can extend the use of pluggable transceivers in data centres to 1.6T and even 3.2T, " said Suresh Venkatesan, chairman & CEO of POET. " Extending pluggables to these speeds with industry-standard form factors was previously thought to be impossible, but because of the small size and extent of integration of devices in our Optical Engines, data centre customers will have more flexibility in network design than ever before."

POET says that pluggable transceiver customers will benefit from the optical engine platform with chip-scale assembly, monolithically integrated multiplexer/demultiplexer and passive alignments for use in 400G, 800G and 1.6T FR4 modules. The Optical Engine solutions will simplify the transceiver design and eliminate the need for cumbersome and costly active alignments.

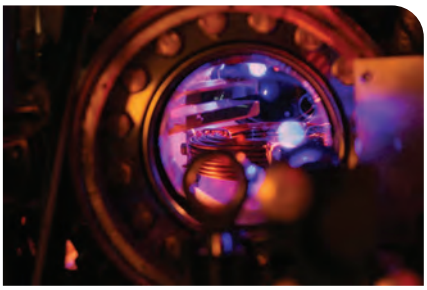
POET expects to start sampling 800G/1.6T Optical Engines in the first half of 2023.

DigiQuant project aims to shrink laser diodes

AMS OSRAM, Fraunhofer IIS, and Toptica have announced a joint project called DigiQuant for digitalisation and miniaturisation of laser diode technology for quantum and terahertz applications.

Within the project, Ams Osram will develop new laser diodes suitable for hybrid integration of photonic waveguides and digital control electronics at Toptica.

In parallel, Fraunhofer Institute for Integrated Circuits IIS and Toptica



will investigate the miniaturisation of electronics in integrated circuits for digitised operation of any material class laser diodes from diverse manufacturers.

The resultant subsystem will be tested in two different applications: a quantum computer application and in an industrial application to readout a digital code with a hand-held scanner.

The hope is that these combined developments will enable the implementation of complex laboratory technology in portable and robust devices with high wall plug efficiency for industrial use and help to scale up quantum computers and take them from the basic research stage to market maturity.

ITRI and Ganvix extend GaN VCSEL venture

Next phase will focus on expanding wavelength range from blue to green, testing and packaging

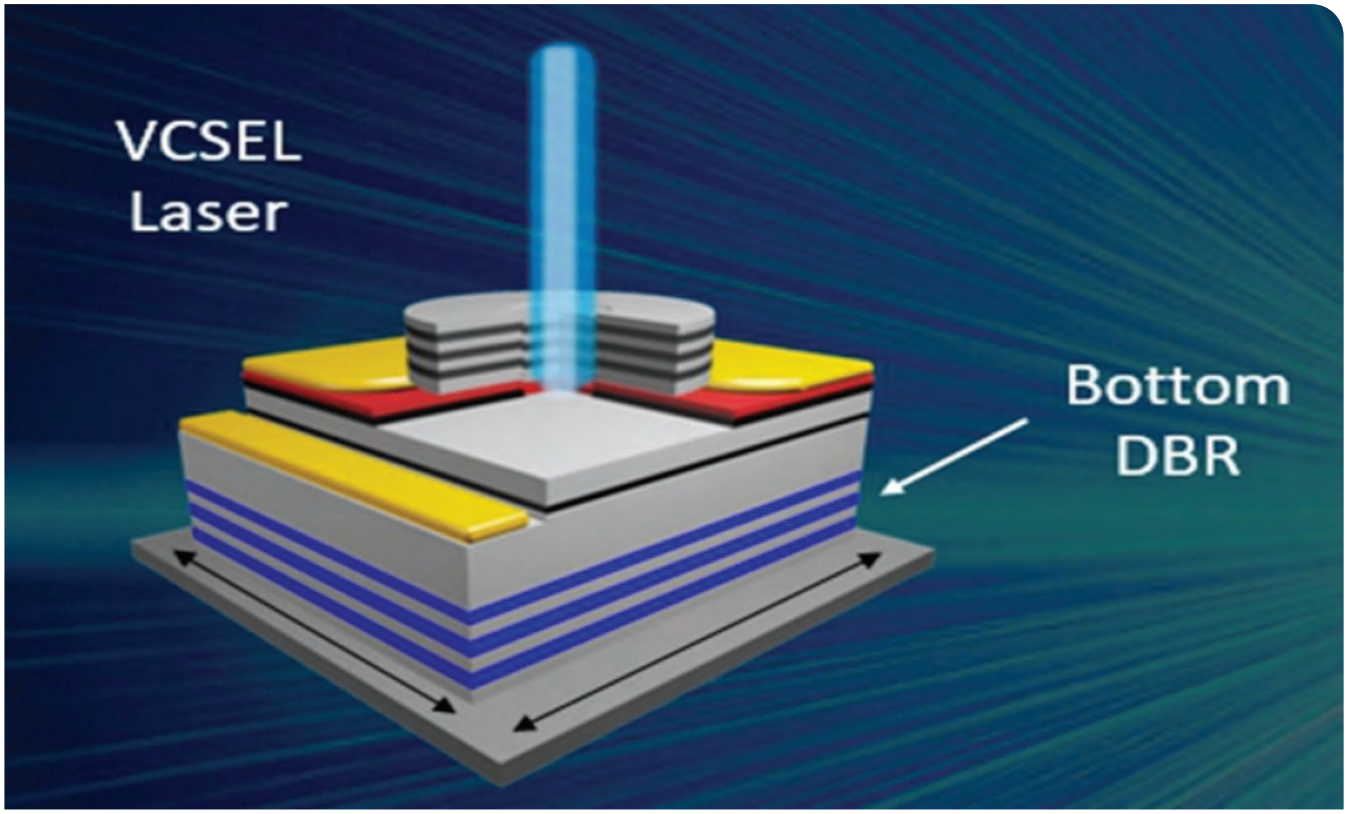
ITRI has announced a continued partnership with Ganvix, a company developing GaN VCSELs on laser technology advancements. The two parties completed the development of the first blue GaN lasers and signed a phase II agreement to extend their joint venture.

GaN VCSELS operating in the blue wavelength range has been demonstrated successfully based on the close collaboration between Ganvix's design and ITRI manufacturability. The next phase of development under the agreement will include expanding the wavelength range from blue to green; qualification testing; and packaging of discrete lasers and laser arrays.

Ganvix uses nano-porous technology to deliver compact, lightweight blue/green/UV VCSEL lasers that produce superior wavelength control, smaller spot size, and array architectures, allowing substantial innovation across a wide range of applications. ITRI will continue to apply its substantial capability and infrastructure for the manufacture of electro-optic devices to accelerate Ganvix's time to market. The resulting products will address the nascent opportunity for high-performance and low-cost GaN VCSELs in the billion-dollar global markets.

GaAs VCSELs that operate in the infrared spectrum are one of the fastest-growing technologies in electro-optics today. However, GaAs cannot emit light in the ultraviolet or visible (blue and green) wavelengths. For these applications, GaN is required, but there has been no commercially viable solution to form the laser cavity mirrors required until now. Ganvix has solved this problem using nano-porous technology to engineer the optical properties of GaN.

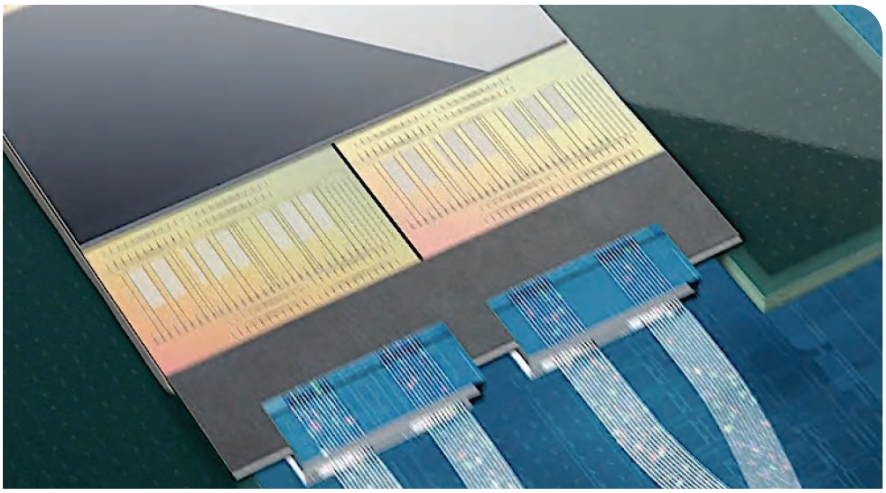
"For future metaverse application, the three-primary-colour VCSELs will play a key role," commented Shih-Chieh Chang, general director of ITRI's Electronic and Optoelectronic System Research Laboratories. "We are very happy to continue to deepen the cooperation with Ganvix and launch commercialised products, which can also drive Taiwan's industries to enter the metaverse market," he said. "We are excited to announce the successful demonstration of blue VCSEL lasers using our proprietary nano porous GaN fabricated in collaboration with ITRI," said John Fijol, CEO of Ganvix. "This marks a critical achievement enabling commercialisation of these new laser devices. We look forward to the next phase of our relationship working with ITRI to bring these devices to market."



Lockheed Martin and Ayar Labs Partner on optical I/O

Companies to develop new generation of defence platforms with optical I/O

LOCKHEED MARTIN and Ayar Labs have entered into a collaboration to develop future sensory platforms that use Ayar Labs' optical I/O microchips to transfer data faster, at a lower latency, and at a fraction of the power of existing electrical I/O solutions. The new platforms could be used across Department of Defense (DoD) applications to capture, digitise, transport, and process spectral information.



"As the complexity and amount of data grows on the battlefield, faster decision-making is essential. New innovative system architectures, coupled with AI and machine learning techniques, are needed for our customers' mission success," said Steve Walker, chief technology officer and vice president, Engineering & Technology at Lockheed Martin.

"Ayar Labs' optical interconnect solution provides the necessary technology to process spectral information with greater speed and lower latency for next-generation system designs."

Lockheed Martin is partnering with Ayar Labs in developing multi-chip package (MCP) solutions which place high-density, high-efficiency optical I/O chiplets in the same microelectronics package as the radio frequency processing devices. The development and integration of Ayar Labs' TeraPHY optical I/O chiplets and SuperNova light source represent a faster, more efficient, and more reliable transfer of data throughout the platform. This is important for next-generation architectures that will use phased array apertures to connect systems and people to make smarter, faster decisions.

"Our advances in interconnect density, latency, reach and power efficiency represent a significant advantage for extreme-edge sensing applications, which is critical for enabling next-generation architectures and systems," said Charles Wuischpard, CEO of Ayar Labs. "For example, our optical I/O solution will provide a 5x power reduction and 12x size reduction versus a representative mid-board optical solution."

Lockheed Martin and Ayar Labs's co-authored paper '*Converged RF Phased Arrays enabled by Silicon Photonics*' was presented at the IEEE International Symposium on Phased Array Systems and Technology earlier this month.

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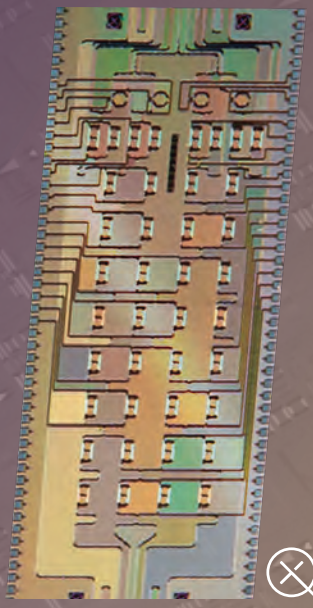

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Next stop for InP: consumer applications?

2022 marks the beginning of a shift into smartphones and beyond

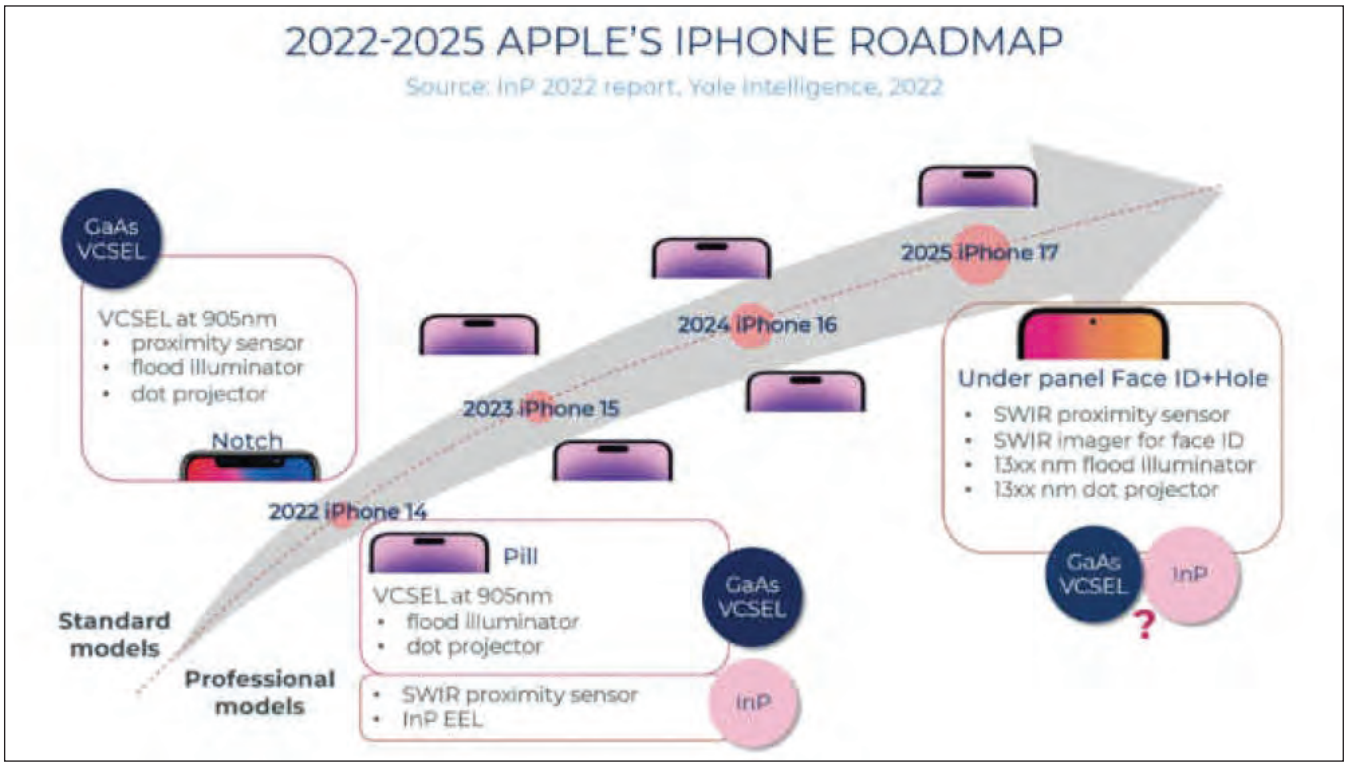
The InP market has long been dominated by datacom and telecom applications, and as such is expected grow from $2.5 billion in 2021 to around $5.6 billion in 2027 driven by high-data-rate modules, above 400G, by big cloud services and national telecom operators requiring increased fibre-optic network capacity.

But, according to Yole Intelligence, consumer applications will be the next showcase for the InP industry, with a 37 percent CAGR between 2021 and 2027. “There has been a lot of speculation on the penetration of InP in consumer applications. The year 2022 marks the beginning of this adoption. For smartphones, OLED displays are transparent at wavelengths ranging from around 13xx to 15xxnm, ” said Ali Jaffal, technology and market analyst at Yole Intelligence. OEMs are interested in removing the camera notch on mobile phone screens and integrating these 3D-sensing modules underneath the OLED displays. In this context, they are considering moving to InP EELs to replace the current GaAs VCSELs .However, such a move is not straightforward from cost and supply perspectives.

Yole Intelligence noted the first penetration of InP into wearable earbuds in 2021.Apple was the first OEM to deploy InP SWIR proximity sensors in its AirPods 3 family to help differentiate between skin and other surfaces. This has been extended to the iPhone 14 Pro family. The leading smartphone player has also changed the aesthetics of its premium range of smartphones, the iPhone 14 Pro family, reducing the size of the notch at the top of the screen to a pill shape.
To achieve this new front camera arrangement, some other sensors, such as the proximity sensor, had to be placed under the display.

Will InP penetration continue in other 3D sensing modules, such as dot projectors and flood illuminators? Or could GaAs technology come back again with a different solution for long-wavelength lasers?

The impact of an innovative company like Apple adding such a differentiator to its product significantly affects companies in its supply chain, and vice versa. Traditional GaAs suppliers for Apple’s proximity sensors could switch from GaAs to InP platforms since both materials could share similar front-end processing tools. Yole Intelligence certainly expects to see new players entering the InP business as the consumer market represents high volume potential. In addition, Apple’s move could trigger the penetration of InP into other consumer applications, such as smartwatches and automotive LiDAR with silicon photonics platforms.



EVG unveils EVG150 resist processing system

Redesigned 200-mm platform increases module capacity for higher throughput

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment, has unveiled the next-generation 200-mm version of its EVG150 automated resist processing system.

The redesigned EVG150 platform includes advanced features and enhancements that provide greater throughput (by up to 80 percent) and versatility, as well as smaller tool footprint (by nearly 50 percent), compared to the previous-generation platform.

The EVG150 is said to provides reliable and high-quality coating and developing processes in a universal platform that supports a variety of devices and applications, including advanced packaging, MEMS, radio frequency (RF), 3D sensing, power electronics, and photonics.

Silicon Austria Labs, a research centre, is the first customer to receive the next-generation EVG150 system. “Through our cooperative research with leading manufacturers, we develop key technologies that build the foundation for Industry 4.0, IoT, autonomous driving, cyber-physical systems (CPS), AI, smart cities, smart energy, and smart health long before they reach the market,” stated Dr. Mohssen Moridi, Head of Research Division Microsystems of Silicon Austria Labs.

“The high flexibility of EVG’s next-generation EVG150 resist processing system helps pave the way for high-volume implementation of new processes and products with our development customers that fuel EBS innovation.”

Company executives will be available to discuss the EVG150 resist processing system at SEMICON Europa, taking place next week at the Messe München in Munich, Germany, from November 15-18 (co-located with Electronica).

Multi-junction VCSELs save power and space

Trumpf expands VCSEL array portfolio with multi-junction featureTrumpf expands VCSEL array portfolio with multi-junction feature

TRUMPF PHOTONIC COMPONENTS has expanded its VCSEL array portfolio with multi-junction devices. The company's tunnel function technology is said to offer a highly efficient solution for the demanding trend towards miniaturisation.

With tunnel functions, the performance of a single VCSEL is increased, as multiple active zones are put into series in the same VCSEL component. Up to three times the output can be generated out of the same VCSEL device. Most illumination applications benefit from higher efficiency and increase in output power with the same VCSEL light source.

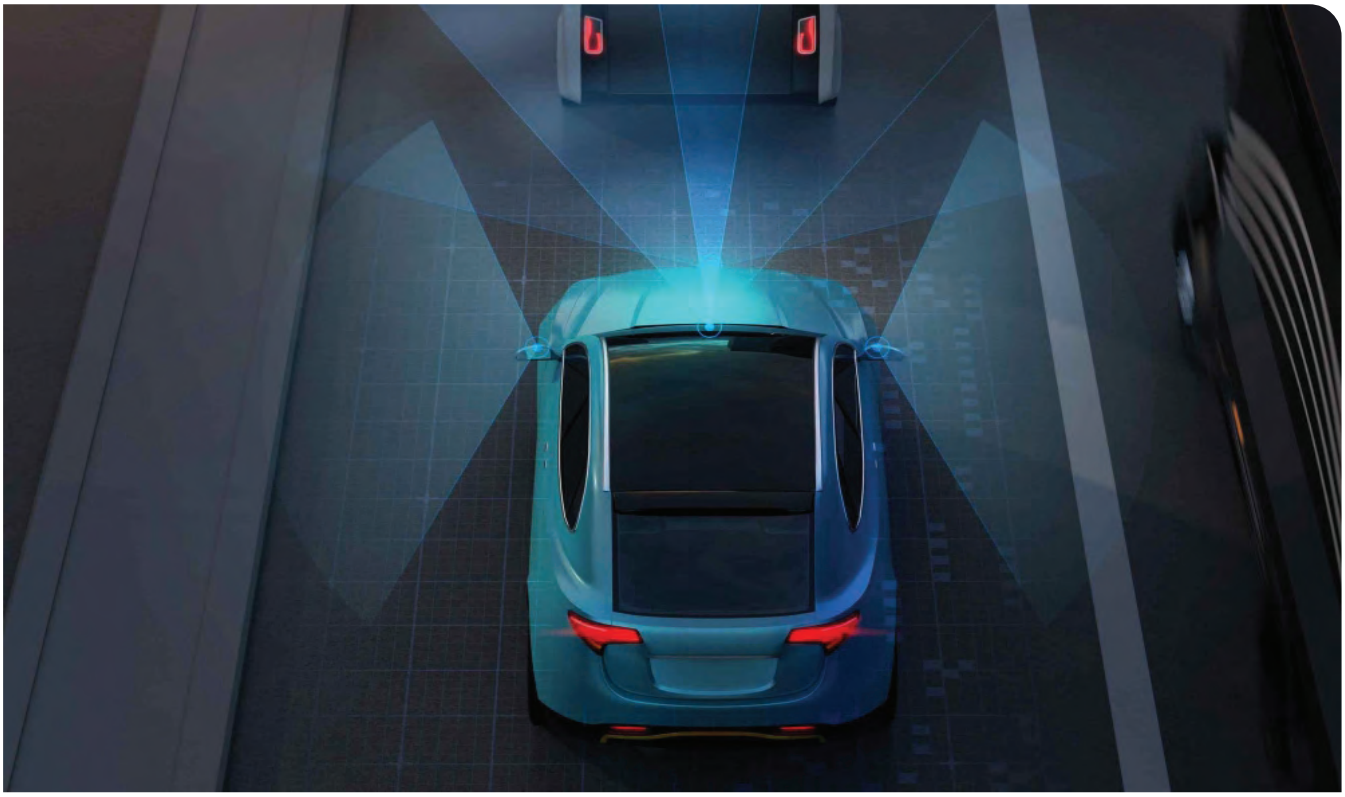
"Our customers also benefit from an increase in flexibility. Based on their application needs, they can configure their VCSEL components with a single, double, or triple junction", says Alexander Weigl, head of product management at Trumpf Photonic Components.

The multi-junction technology supports applications such as LiDAR, as this application in the automotive branch requires high-output power within limited space for the short and long-range identification of objects.

"We even combine the multi-junction technology with our ViBO technology platform. Due to our integration approach to make our VCSELs smarter, this unique VCSEL comes with integrated backside optics and is already up to five to ten times smaller compared to other VCSELs", explains Weigl. "This is a big step towards miniaturisation, while increasing output power and reliability of the VCSEL components", Weigl adds. VCSEL technology will remain a main light source for applications in smartphones, consumer electronics and automotive applications, as they are highly efficient and boast a long service life.

Based on the application requirements, Trumpf offers options with highly integrated optical structures for the best fit.

Therefore, along with the multi-junction option and monolithically integrated optics, VCSELs can offer polarisation control for improved illumination quality, or integrated photodiodes to enable the further processing of light signals. To offer robust VCSEL devices with high performance, Trumpf covers the whole process chain, from the developing and designing right to its manufacturing of their VCSELs solutions.



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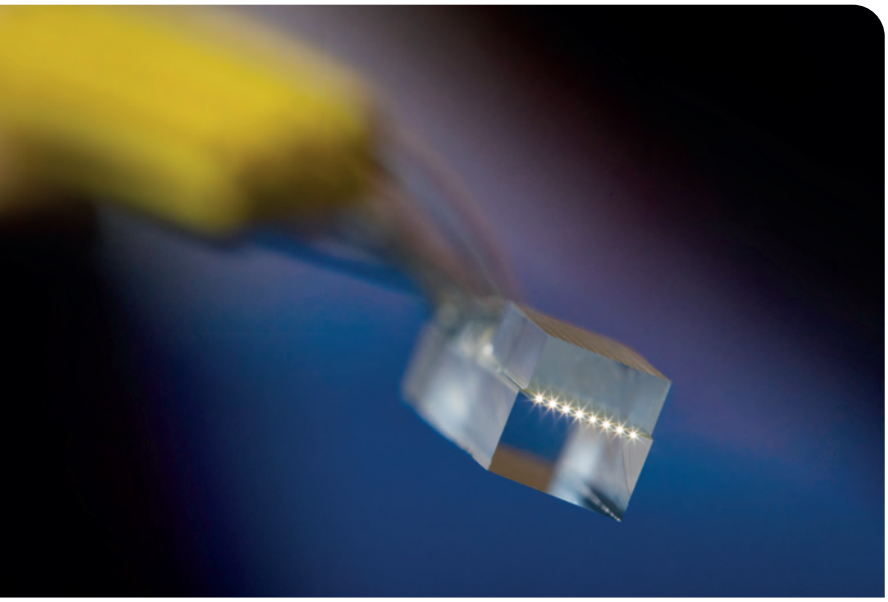
Improving optical coupling for hybrid photonic packaging with aligned two-photon lithography

Nanoscribe's 3D Microfabrication is a key enabling technology for the optical coupling and packaging of photonic components in hybrid integration to enable the penetration of photonic integrated circuits (PIC) in industrial high-volume manufacturing

BY JÖRG SMOLENSKI AND SOFÍA RODRÍGUEZ, NANOSCRIBE

Photonic data processing and photonic quantum computing have a great potential to exploit the concept of computing at the speed of light. For example, artificial intelligence (AI) applications demand high computing power and storage capacity. But electronic technologies currently struggle with the processing power needed in AI. New methods are under investigation by moving away from electronic towards photonic approaches for ultrafast information processing. Moreover, photonic integrated circuits extend also to application fields such as frequency-modulated continuous wave (FMCW) LiDAR, wearables, or medical and environmental sensors or data and telecom applications.



➤ Figure 1: This image shows a lensed fiber array (LFA). Nanoscribe's Two-Photon Polymerization is used to print Free Space Microoptical Coupling (FSMOC) elements directly on fiber arrays. Image: © PHIX Photonics Assembly

The challenge of hybrid integration in photonic packaging

Photonic packaging means integrating photonic integrated circuits (PIC) with a wide range of active and passive optical components into a compact module but with the key challenge to couple the light between each of them. The buildup is not monolithic as in electronics packaging but rather heterogenous with active alignment of the different components to each other. Next to the PIC itself, these components include lasers, photodiodes, waveguides, optical sensors, fibers and other optical modules. To integrate the different components, photonic packaging requires specialized microoptical structures as highly efficient optical coupling elements. These elements can couple light between various optical components and platforms, facilitating hybrid integration.

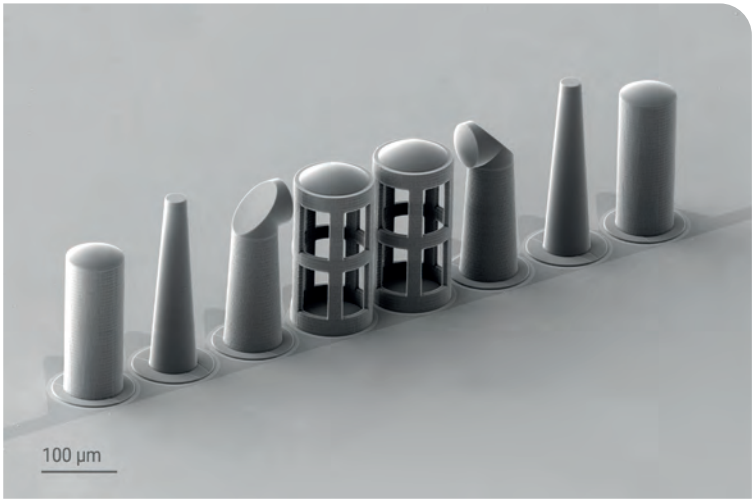
Nanoscribe's additive manufacturing technology of Two-Photon Polymerization (2PP) offers a unique microfabrication approach to tackle the issue of hybrid integration. The core capability of this technology is to 3D print finest miniature structures of virtually any shape. Its versatile capability to fabricate high-precision 3D structures on the nano- and microscale is an asset for developing microoptical coupling elements with specific designs. In 2PP technology, a pulsed laser is used to cure a photopolymer resin to create shapes with submicron resolution [1]. The technology enables the fabrication of free space microoptical couplers (FSMOC) with complex 3D geometries. Using

2PP's 3D design freedom, FSMOC designs can be adapted to fit in with a variety of photonic packaging systems. The 3D printing capability of 2PP enables challenging microfabrication tasks for highly efficient light coupling onto different photonic platforms.

Relaxed alignment tolerances by 3D microfabrication

The different photonic components usually have different optical coupling interfaces (e.g beam diameter, numerical aperture, etc.) and also require different coupling strategies: the coupling between single components either occurs through the edge of the die (edge coupling) or through the surface (surface coupling). The most common technique for edge coupling is either with a lensed fiber or butt coupling. In the second, a fiber is directly positioned on the facet of the edge coupler. Lensed fibers enable simple mode field adaptation but are not usable for high volume production due to the optical lens design limitations (e.g. for elliptical mode fields).

Not only the variety of optical coupling interfaces require specifically designed microoptical couplers, also, another challenge of photonic integrated circuits in photonic packaging is to precisely align passively these optical components instead of the costly active alignment that has been the traditional approach. The challenge is relaxing alignment tolerances for packaging to several micrometers instead of hundreds of nanometers. Efficient optical coupling with active alignment is a time-consuming process. The 2PP technology is therefore a decisive microfabrication strategy that enables passive packaging (pick & place) by the use of non-contact FSMOC, allowing tolerances of a few micrometers for the final components. The difficulty of precise alignment in photonic packaging is transferred from the packaging process to the printing technology.

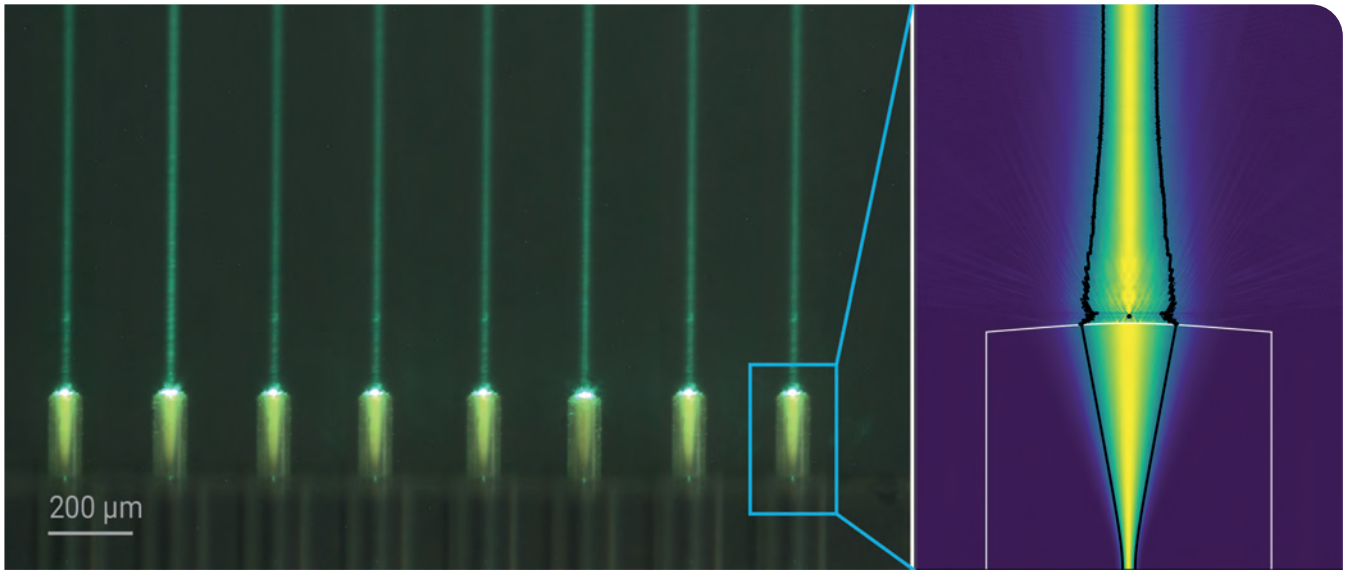


➤ Figure 2: SEM image of different optical designs printed precisely aligned to the fiber core in a v-groove fiber array. Image: © Nanoscribe

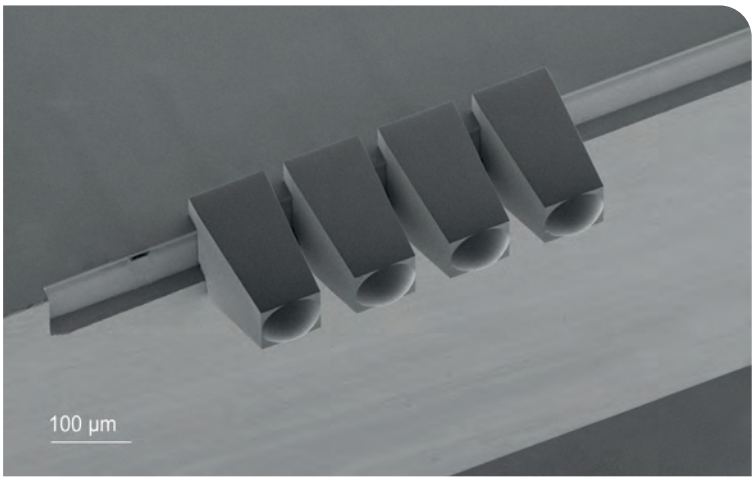
2PP has demonstrated to tackle these difficulties by printing microoptical coupling elements in place with an automatic alignment system with nanometer precision. The microoptical elements are directly printed on the optical interface of chips or fibers with a precision of down to 200 nm. The low alignment tolerances between optical elements mentioned above are achieved by simply tailoring the beam shapes and by making mode field adjustments. The design of FSMOC can be easily and quickly adapted to new requirements and applications. This flexibility takes into consideration the different types of microoptical fiber-to-chip couplers needed, for example for lensed fiber-to-chip, lensed chip-to-fiber and lensed fiber-to-lensed chip.

Aligned printing of microoptical couplers on fibers

Freeform microoptics can be 3D printed on fiber tips for imaging and beam shaping tasks, including challenging applications such as periscopic



➤ Figure 3: Free Space Microoptical Couplers are used for collimating light beams with relaxed alignment tolerances, achieving coupling losses of below 1 dB. Optical micrograph of the FSMOC on fiber array (left) and simulated beam expansion (right). Source: Sample from research project MiLiQuant © Nanoscribe



➤ Figure 4: The SEM shows an example of beam shaping optics printed on a photonic chip. Source: Sample from research project HandheldOCT © Nanoscribe

lenses used for wafer-level testing. There are different options to couple a fiber to other optical components, depending on the application. Using free space microoptical coupling (FSMOC) is a viable route to implement freeform optics for shaping light beams and coupling light from one to another optical component. Many applications require to steer and form beams from small to large or from large to small mode field diameters. The beams need to follow a path in different directions from a planar, to an inclined or even vertical direction.

FSMOC on fibers are used to tailor beams with beam expanders. For this purpose, freeform microlenses are 3D printed onto fibers using 2PP. One application example for printing onto fibers using 2PP is the case of a beam expander for a 25 µm mode field diameter. A fiber array with 460 HP single mode optical fibers is the starting optical platform. The camera-based detection is used to precisely detect the fiber core position before the printing within a ring down to 500 nm around the core. Then, the beam expanders are printed with automatic alignment to produce a lensed fiber array (LFA). To prove the performance of the microoptical couplers, the beam propagation is measured for 532 nm wavelength with a metrology setup. The measured beam coincides with the simulated expanded beam. The beam allows single mode fiber array to fiber array coupling over 1.2 mm. A 25 µm beam expander for 532 nm wavelength achieves ± 2.5 µm for 1 dB lateral alignment tolerance. This result demonstrates the precise performance of the camera-based alignment process for printing freeform microoptics to the core of the fibers, opening the way as a viable tool for research and industrial applications.

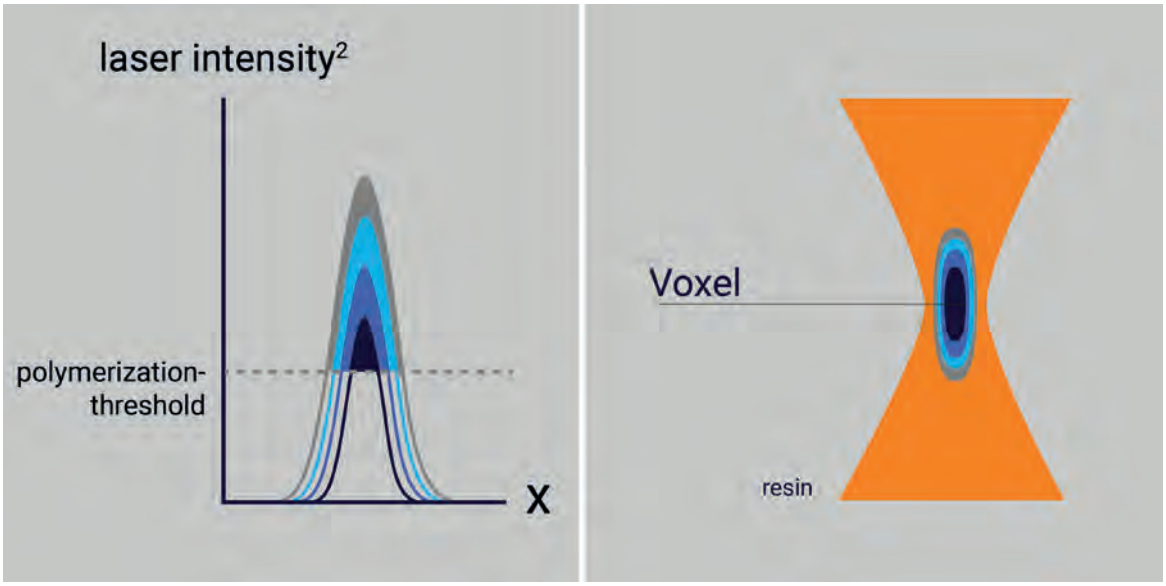
Moreover, the use of focusing lenses on fibers can generate a small beam output from a SMF fiber (e.g. fiber mode field diameter of 10 µm at 1550 nm). In this case the printed microlenses onto the fiber are focusing lenses that can achieve direct coupling to tapered waveguides with low coupling losses. A lens focusing to a mode field diameter of 3.6 µm achieves a loss of -1.7 dB per coupling interface on SMF28 fibers for 1550 nm for coupling to SOI tapered edge coupled waveguides.

Aligned printing of microoptical couplers on chips

To fabricate optical couplers for edge coupling from a photonic chip to another die or towards a fiber, the spatial orientation of the fiber cores and photonic chips have to be detected. For this, 2PP-based 3D printers implement another automated method for aligned printing on chips: integrated confocal 3D mapping. The inline confocal imaging module provides a 3D mapping of the substrate topography. This enables precise lateral alignment, down to 200 nm, and precise 3D alignment to predefined markers or waveguides. Optical interfaces on photonic chips or fiber cores and their spatial orientation are automatically detected, and predefined freeform microoptics are printed directly in place. Thus, 2PP-based microfabrication reduces the complexity of the process chain, and assembly tolerances are relaxed while enabling even more compact devices. The often costly active alignment process is no longer necessary. Moreover, there is a strong need to reduce coupling losses between fibers, edge couplers, grating couplers, emitting facets, and especially between different material platforms. 2PP-printed microoptical couplers achieve lateral excess coupling losses down to 1 dB or below.

Quantum X align, Nanoscribe's 2PP-based printer for photonic packaging is combining all the above mentioned features such as alignment with nanoprecision and novel printing processes for precisely aligned 3D printing on optical fibers and photonic chips. The system uses automatic detection of the printing base to measure the spatial orientation of the fiber cores or photonic chips. Using this detection system, the printer manufactures freeform microoptical components directly in place, facilitating optimized optical coupling on photonic platforms.

To fabricate optical couplers for edge coupling from a photonic chip to another die or towards a fiber, the spatial orientation of the fiber cores and photonic chips have to be detected. For this, Nanoscribe's 2PP-based 3D printers implement another automated method for aligned printing on chips: integrated confocal 3D mapping



➤ Figure 5: In Two-Photon Polymerization, a sharp polymerization threshold separates the polymerized from the unpolymerized areas within the photoresin. Outside the focal volume, the intensity falls below the polymerization threshold and thus the photoresin remains liquid. The size of the polymerized voxel can be tuned with varying laser intensity, which is the core capability of Two-Photon Grayscale Lithography (2GL®) [2]. © Nanoscribe

Additively manufactured freeform microoptics

Additive manufacturing by Two-Photon Polymerization allows to go beyond classical optical designs on the microscale. Nearly any three-dimensional shape, be it spherical, aspherical, sharply edgy, freeform, and even compound 3D microoptics composed by a stack of various lenses can be materialized with 2PP-based 3D printing. This capability circumvents limitations imposed by mechanical tools and geometrical and process design constraints known from subtractive techniques.

When printing 3D microstructures, the 3D objects are printed line by line to form one layer, and layer by layer to build the 3D shape. To achieve this discretization, the structure design is sliced in layers with a defined slicing distance using the print preparation software. Each microstructure can combine different elements, for example, one supporting base and a functional lens can be printed combined in one design and one pass. To reduce print time and reach best optical quality, each element is printed using different printing parameters. Thus, the supporting base will be printed with a coarse slicing setting while the lens structure will be printed with a much finer slicing.

This advanced printing strategy, called smart slicing, allows to reduce print time and achieve optically smooth surfaces. The resulting 2PP-printed microoptics have surfaces roughness R_a that reach down to less than 10 nm. Moreover the designs printed with this technology achieve a shape accuracy in the range of 200 nm or less.

Novel 3D microfabrication opportunities

2PP has been used for years mostly at universities and research organizations. Nanoscribe's new industrial 3D printers make novel and advanced microfabrication capabilities such as 3D-aligned printing particularly attractive to the photonic packaging industry. With its versatility, the 2PP-based printers can overcome light transmission challenges in photonic packaging by adapting the mode field diameter from one material platform to another while optimizing coupling efficiency by reducing coupling losses.

The 2PP technology allows for fast photonic packaging by relaxed alignment tolerances between the optical components. In this respect, 3D-aligned additive manufacturing of microoptical elements is crucial for the penetration of photonic integrated circuits in high-volume industrial manufacturing. The explained advances will also have effects in diverse applications such as photonic computing and data processing for AI, sensing and imaging applications needed in automotive and medical fields.

REFERENCES

➤ [1] Additive manufacturing based on Two-Photon Polymerization. A key enabling technology for high-precision 3D printing. https://www.nanoscribe.com/en/whitepaper/

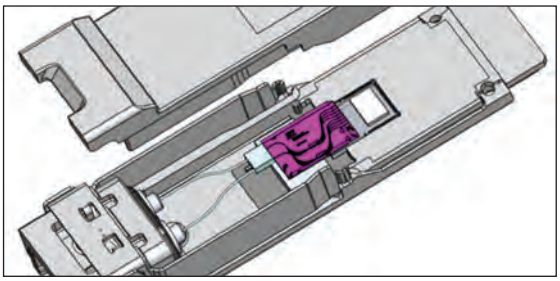
➤ [2] Introducing Two-Photon Grayscale Lithography. Outstanding performance of a new maskless lithography technology. https://www.nanoscribe.com/en/whitepaper/

Yield improvement techniques in the manufacturing of AWG (Cascade) PLC

The AWG Cascade chip offers a step improvement over the conventional AWG. In this article Broadex Technologies discusses how the AWG Cascade chip works, where it will be deployed and how it can be manufactured with a good yield.

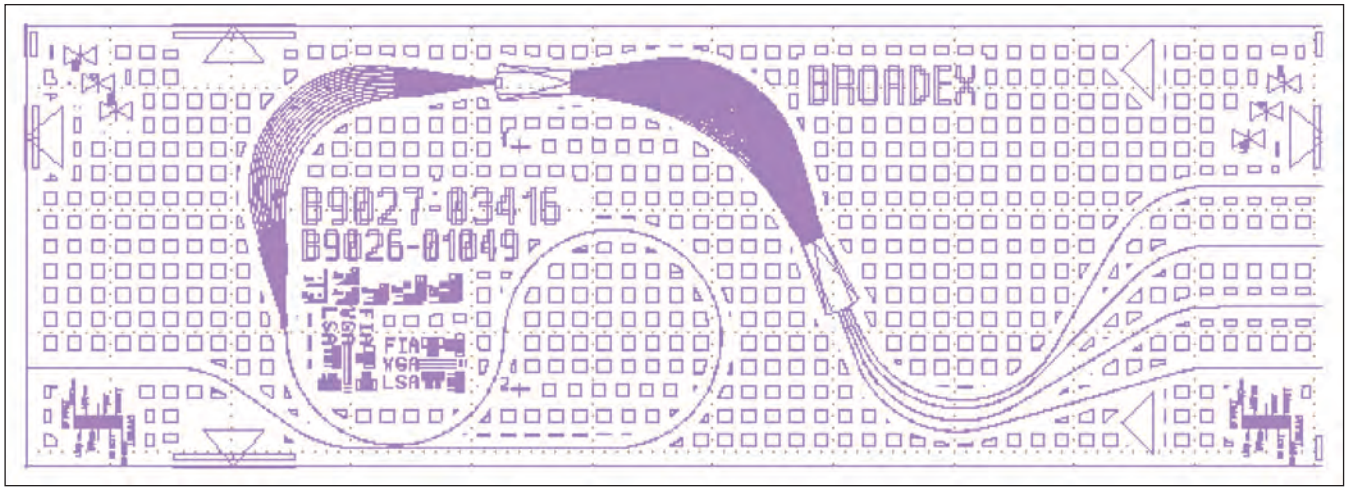
BY HENK BULTHUIS, BROADEX TECHNOLOGIES UK

AWG Cascade products consist of two synchronized Silica-on-Silicon Array Waveguided Gratings (AWGs), arranged in series on a single chip. Arrayed Waveguide Gratings are working as a prism that disperse the light coming into the device when coupled to an input fiber. For AWG Cascade (CAWG) chips the dispersion of the two AWGs are synchronized which gives a theoretical zero loss over a wide passband. The small footprint allows the chip to be integrated in small form factor transceivers which make up the workforce of datacenters for data transport, internal between the racks, from rack to rack and even from datacenter to datacenter.

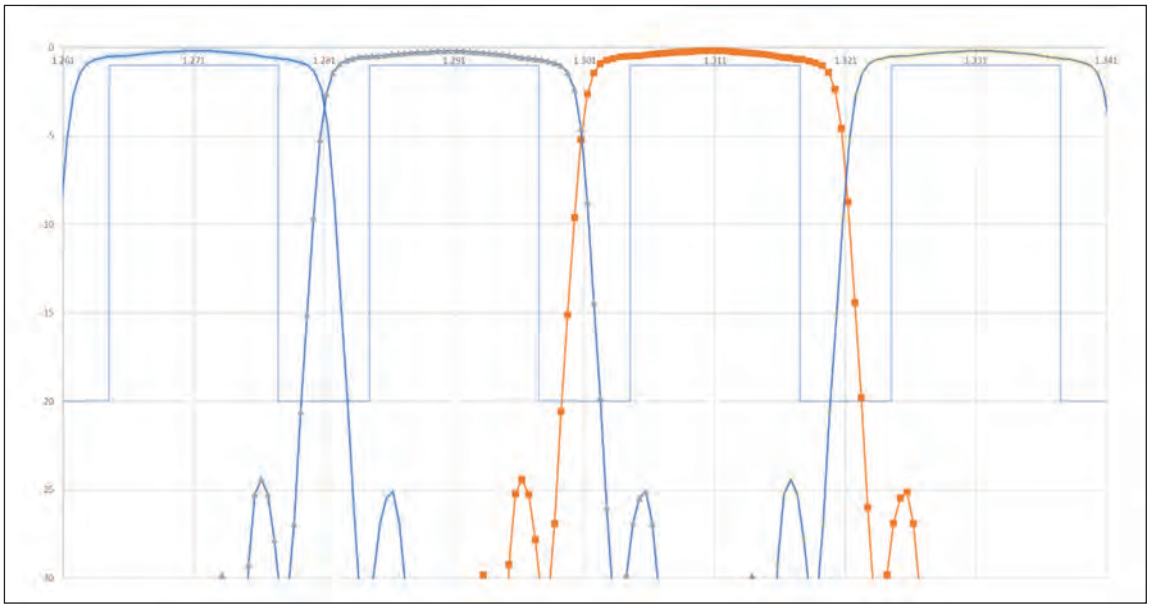


➤ AWG Cascade or CAWG chip in transceiver package

In the illustration below, light enters the chip from a fiber to the input waveguide on the left-hand side. The four receiver channels on the right side of the chip connect to high-speed photodetectors and each photodetector captures a different slice of the optical spectrum. This way the chip is used to demultiplex the 4 channels from the input fiber, each channel carrying its own portion of data. The slicing action of the spectrum for each of the 4 receive channels is displayed in the transmission spectrum. The fiber can now carry 4 times more information compared to using only a single frequency of light. AWGs and CAWGS can be designed to Multiplex and or Demultiplex anywhere between 4 and 96 channels, thus multiplying the capacity of a fiber connection by a factor 4x to 96x respectively without need to grow the fiber plant. Compared to regular AWG, the AWG Cascade produces ultra-



➤ Layout of an approximately 10 mm long AWG cascade chip for CWDM4 transceiver.



➤ Figure, simulated transmission spectrum of Cascade AWG.

low insertion loss, flat-top bandpass shape while maintaining a single mode output. The single mode output allows for efficient coupling to ever increasing high-speed photodetectors which have ever decreasing active area sizes as the speed of switches, or baud rate, increases. Suitable for WDM applications, they can be used as both a MUX, to combine say the light of 4 lasers on a single fiber, or DEMUX, to separate the light from a single fiber to 4 individual detectors.

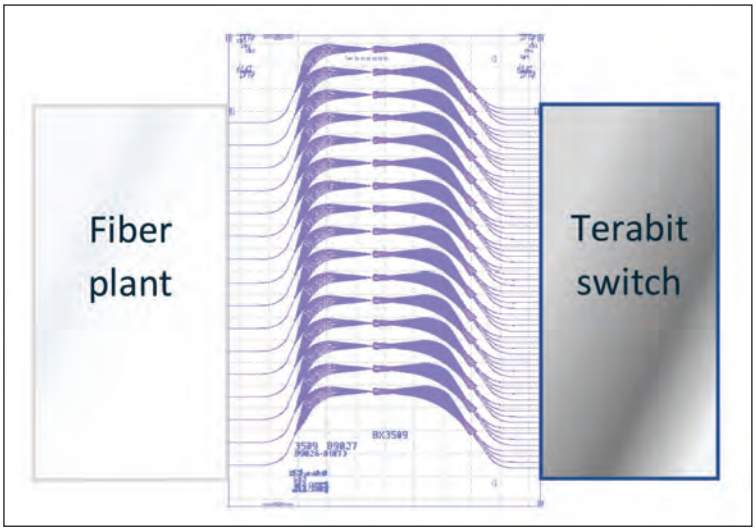
The curved AWG Cascade structure can also be laid out very efficiently to provide up to 16 individual AWG Cascade structures on a single chip, see figure, which is of a similar size (10x20mm) as a typical fiber block array that is conventionally used to couple light from chip to fiber. This dense footprint and the flexibility to adjust the mode field diameter, minimizing coupling loss, is ideal for Co-Packaged Optics (CPO) used in next generation multi-Terabit applications.

Yield improvement for AWG Cascade manufacturing: Even though semiconductor processes are used for manufacturing of PLC (Planar Lightwave Circuits) the yield is not just limited by defects. The wave-type nature of the photons that travel the channels on the chip means that the function of the chip is very sensitive to the exact pathlength that photons travel. When the photons are separated and combined they need to arrive exactly in phase. If the light path traveled by photons in one channel is off by a femtosecond this will already cause destructive interference of the photons causing the chip to fail specification.

During etching of the waveguides the width of the waveguides may vary due to local varying etch chemistry. Other nonuniformities may arise from imaging errors due to photo, wafer bow, resist spin, refractive index and thickness variation during deposition of the layers.

All these variations impact the transit time, or phase, of the photons on the chip. These phase errors are equivalent to imaging errors which are the main cause of failing chips. Defects cause amplitude errors which are sporadic compared to phase errors. In the figure we show a typical sickle-shaped phase error across the branches that make up the array section of an AWG.

Very similar to the imaging errors when fabricating discrete lenses, you can have parabolic phase errors that cause a defocus or blurring of the image. One can also have third order phase errors, or COMA, that cause a ghost image slightly displaced relative to the main image. In practice, in order to make a yielding chip one should eliminate at least the first, second and third order imaging errors. At Broadex Technologies we have developed an industrial approach to testing and eliminating these phase errors in order to improve the yield.



➤ An array of 16 individual AWG Cascade structures for next generation multi-Terabit applications using Co-Packaged Optics (CPO).

A typical sickle-shaped phase error across the branches of the AWG

We use a tuneable laser scan to the transfer function of the chip at test. Fourier transform of the transfer function gives time response. The time response gives delay errors which are the equivalent of the phase errors causing the aberrations in the function of the AWG. Correction and monitor of phase errors are subsequently automated for our AWG chips in order to get good yield for volume products.

The UV Trimming system is based around a high power UV laser and PC controlled stages. Before trimming the chips are saturated with hydrogen.

During the trim, the laser causes the hydrogen to react within the Germanium doped waveguiding glass, modifying the refractive index of the material by about 4e-3, which is enough to allow for the order of femtosecond delay corrections by writing arbitrary shapes of the order of 100um using a programmable stage.

The alignment and setup is manual while trim design and implementation is automated. It is also possible to make the phase corrections for each of the two orthogonal polarization states of light. In the future these corrections can be made using wafer level testing and wafer level trimming.

Due to routine testing of all chips that run in the operations we frequently find that depending on the location on the wafer, and depending on the design, systematic phase errors are created that are signature of the specific combination of channel density and processing equipment.

These systematic phase errors are not eliminated by UV trimming but by design. Even though we can make every chip work by UV trimming, provided there are no defects on the channels where the photons travel, it is still economical to eliminate the systematic phase errors beforehand. Using the data from the phase measurements, routine adjustments in the design are made during the exposure of the photoresist for each individual chip depending on location. It is shown here how we correct for a systematic phase error on one particular device.

In the fabrication of AWG Cascade chip it is important that the dispersion of the first and second AWG of the Cascade are perfectly synchronized. If

Testing of the phase error.

that is not the case the transmission passband will suffer high insertion loss. Again using the UV trimming procedure outlined in this article we can repair the passband by UV trimming. Such a correction, and how the passband recovers is illustrated in the following figure.

Conclusion

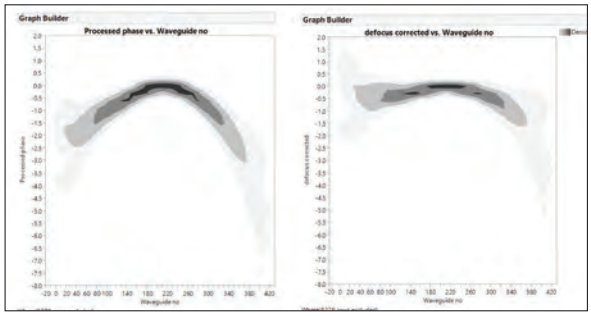
We have discussed the manufacturing of AWG Cascade chips for Multiplexing and Demultiplexing function. It is demonstrated that the chip possesses a passband that is wide, has low loss and works for single mode transmission.

Distributions in performance of these chips, and other types of AWG chips, are observed from the process variation inherent in the manufacturing methods used in the chip manufacturing process.

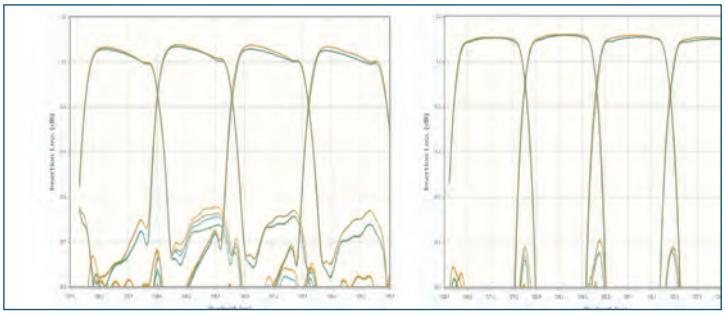
Such variation, whether within wafer or wafer to wafer can be addressed through modification of the manufacturing process to remove systematic phase errors, or by laser trimming the chips to eliminate the remaining phase errors in the chips one by one.

The testing and trimming of phase errors has been automated in order to essentially allow all defect-free chips to pass specification.

➤ Correction of the phase error.



➤ Figure, left the distribution of phase versus channel number before, and right after correction.



➤ Figure, CAWG response before (left) and after (right) aligning the two AWGs in the Cascade.

Wafer-level Nanoimprint Technology for Innovative Packaging of Photonic Integrated Circuits

The need for high-speed data transfers with low-power consumption and low latency in data centers, telecom networks, sensors and emerging applications in advanced computing for artificial intelligence (AI) is growing exponentially. More than ever, we rely on these applications to ensure a safer and more productive world. All across these markets, silicon photonics (SiPh) play a key role in enabling ultra-high bandwidth performance. As a result, it is more important than ever to develop solutions that can cost-effectively scale up the production of silicon photonics.

BY ANDREA KNEIDINGER, EV GROUP

WHILE THE WAFER manufacturing capabilities for SiPh have matured through the use of standard semiconductor mass production processes and existing infrastructure, packaging solutions for SiPh remain a key bottleneck to mass commercialization.

Production capabilities for SiPh are still behind and lack scalability compared to wafer fabrication. The main limiting factor is the fiber to chip assembly, where companies today often rely on very complex solutions; for example, direct fiber bonding on chip with adhesive through active alignment or high-precision tools.

These factors limit the wider deployment of SiPh. To solve this challenge, EV Group (EVG) teamed up with Teramount to develop optical microstructures using a simple, reliable and cost-effective wafer-level replication process that enables the production and scaling up of complex structures to high volumes.

This replication process, known as nanoimprint lithography (NIL), helps to simplify, miniaturize and standardize the optical interface to bridge the gap in SiPh packaging toward wafer-level high-volume manufacturing (HVM).

NIL overview

NIL is a precise replication technique that has shown to be ideally suited to facilitate the patterning of microstructures with challenging geometries, required for emerging devices and applications across the photonics market. This technology is very flexible and can produce a wide range of shapes and structures, such as mirrors, prisms, spheric and aspheric lenses, micro lens arrays as well as various types of diffractive structures. Supported dimensions can be freeform and range from single nanometer resolution up to millimeter lateral extent. These 3D structures are replicated in a single step, which is ideally suited for the photonics industry, where light matter interaction relies largely on shape and geometry.

A further key asset of NIL is the straightforward transfer of these complex and high-precision structures to HVM as hundreds or thousands of structures can be replicated with high fidelity over a large area in a single step. Overall, wafer-level NIL represents an efficient and low-cost non-conventional lithography method capable of replicating complex micro- and nano-scale structures, particularly wafer-level optics (WLO).

Step and Repeat Mastering: scaling NIL from single die to fully populated master

Step-and-repeat (S&R) NIL is a key enabling technique for manufacturing wafer-level micro- or nanostructures because it bridges a crucial gap between die-level designs and wafer-level production. In particular, it allows the scaling of structures that were previously prototyped on areas measuring in the square-millimeter range to fill full 200-mm or 300-mm wafers. The main challenge with S&R NIL is that the quality of the initial master stamp defines the success of subsequent production, so the quality of the single-die master must be preserved. Therefore, it is necessary to take a master mold of a single die — written with either an electron beam, direct laser writing, or two-photon polymerization — and replicate it exactly hundreds or even thousands of times to produce full-area masters for 200-mm or even 300-mm wafer production lines (see Figure 1).

To address this need, EVG has developed the EVG770 S&R NIL system, which enables precise replication of micro- and nano-patterns for large-area master stamp fabrication used in HVM. It dispenses the resist, aligns the structures, imprints accordingly and demolds in a fully automated procedure. To support the most advanced mastering requirements, the S&R system includes full process control, with precision alignment within 250 nm, and is capable of positioning every structure next to alignment patterns. All process steps — from dispensing, imprint, curing, and demolding — must also be performed precisely and monitored within a single environment to allow optimal feedback control.

This not only avoids the impact of external sources such as airborne particles or temperature changes that can lead to imperfections, but it also enables the creation of both a wafer-level master with optimal quality and exact replicas of every single die that can then be applied to wafer-level manufacturing.

With every replication step — from single die to S&R master to working stamp and final imprint — some changes in pattern dimensions are inevitable, due to shrinkage of the polymers caused by crosslinking during the UV curing process. These changes are predictable, some steps can even compensate for each other, and the deviations from the original

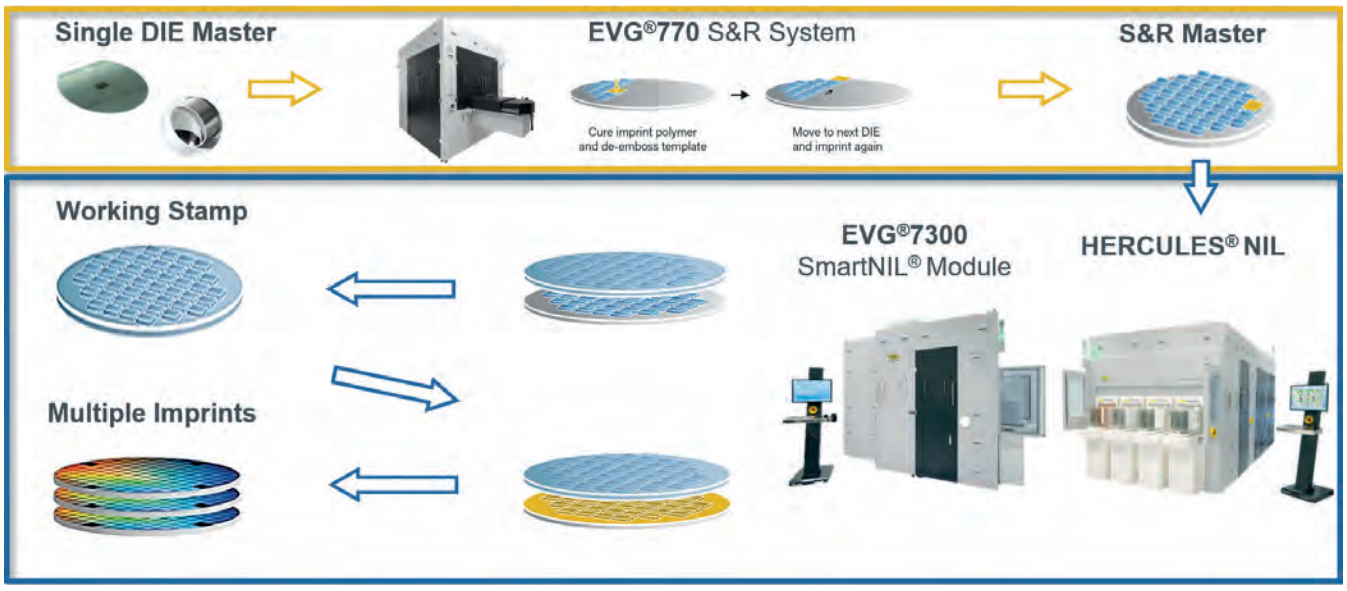
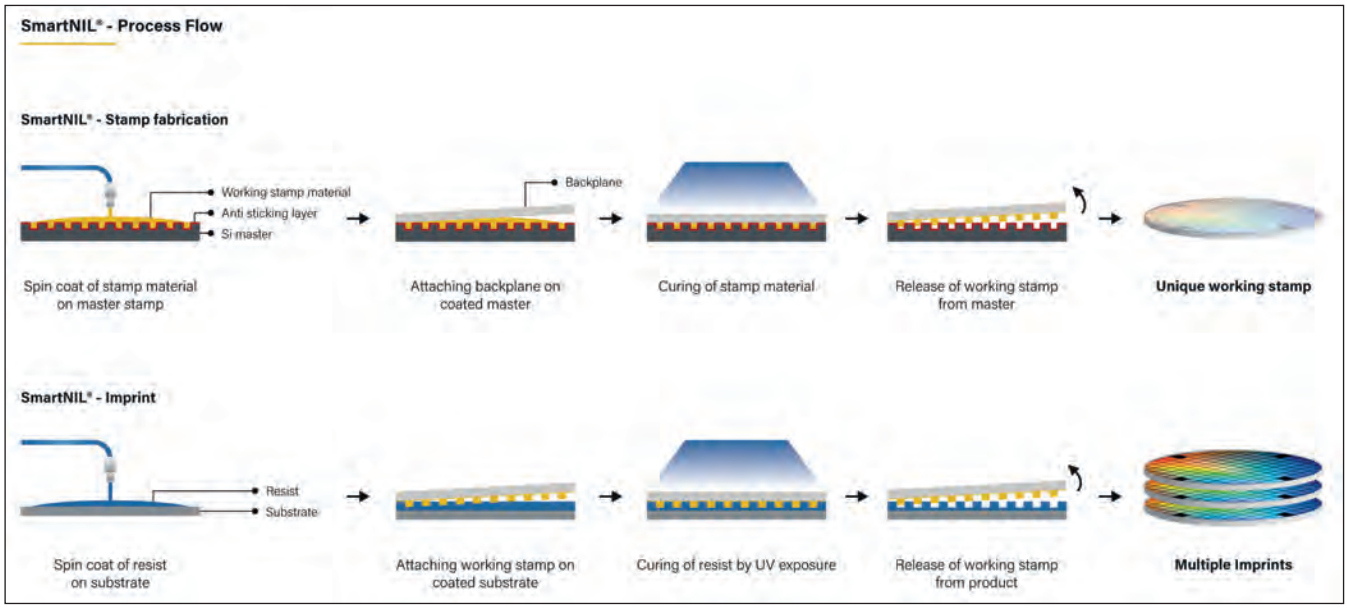


Figure 1: EVG's NIL process and scaling know how: from single die, via Step and Repeat (S&R), to fully populated master and high-volume manufacturing.



➤ Figure 2: Schematic of a NIL process, consisting of two steps: working stamp fabrication and imprint. Both steps are carried out in the same tool.

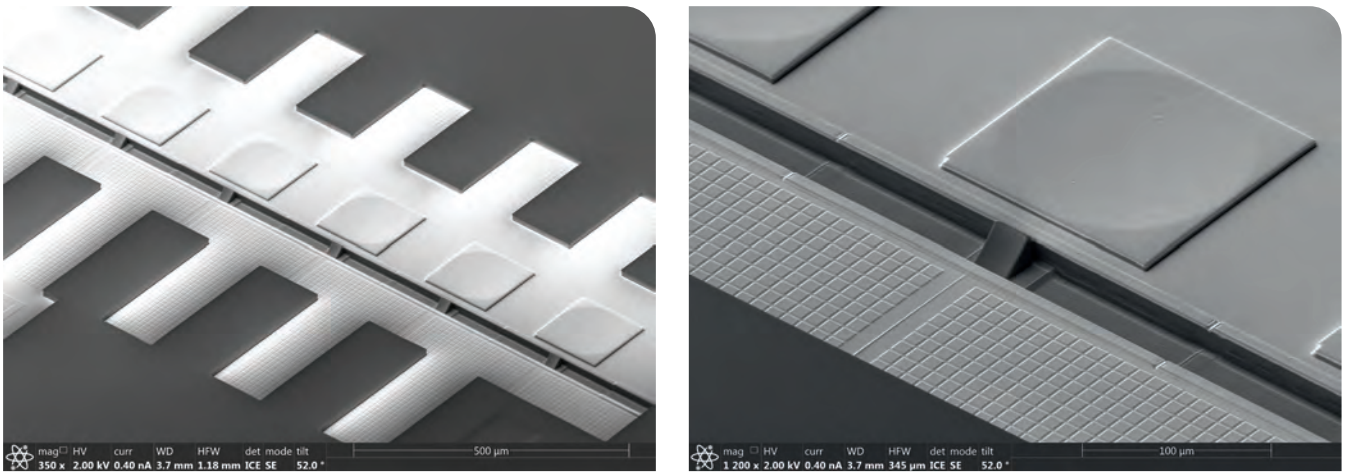
design are very repeatable for a given set of materials. Thus, compensation can be calculated into the master design. Flexible fabrication methods, such as 2GL (two photon greyscale lithography) or e-beam, support such design changes as well as short iteration times.

Wafer-level NIL for high-volume manufacturing

The S&R mastering process is followed by wafer-level NIL replication, which is performed on the EVG7300. This process consists of two steps, both of which are carried out on the same system (Figure 2). First, the S&R master is replicated to fabricate a working stamp. This step is particularly useful because it minimizes wear of the expensive masters and reduces the risk of introducing defects. Defective working stamps can be replaced quickly and at low cost, which can be particularly advantageous during high-volume production runs. To ensure defect-free working stamp fabrication, the initial master is coated with an anti-sticking layer applied by spin coating. Next, the working stamp material is coated directly on the master, also by a spin coating process, using an EVG120 spin/spray coating system. Next, the transparent backplane is attached on the coated master. The working stamp polymer is then cured using an UV LED light source, and finally demolded from the master.

After the working stamp is produced, the actual imprinting process on the device substrate is performed. This involves applying a dedicated material on the substrate using the same spin coating process used for the working stamp fabrication.

Next, the working stamp and the substrate with the dispensed material are brought into contact with each other. As was the case with the working stamp fabrication process, this step is followed by UV curing and demolding, resulting in multiple imprints with the final devices on the substrate. The working stamp can then be reused for multiple imprints,



➤ Figure 3: a) PhotonicBump NIL imprint on a SiPh wafer next to multi-channel photonic integrated circuit waveguides; b) Close-up image shows PhotonicBump elements including beam deflection and beam expansion mirrors.

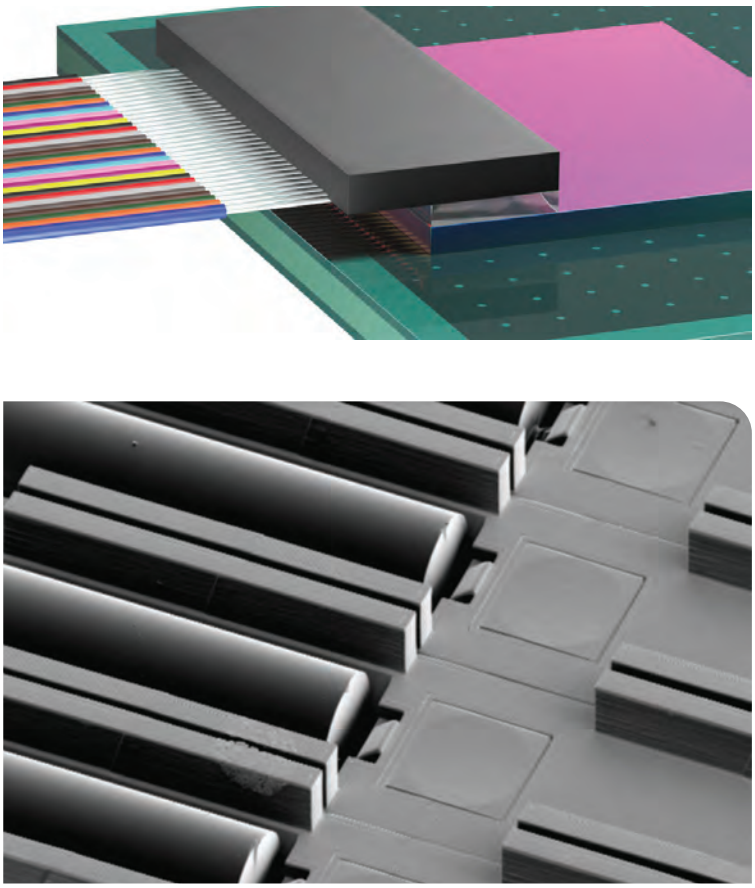
increasing NIL process efficiency. This method of reusing working stamps has been proven already for HVM applications.

The NIL process has long proven its high repeatability in high-volume production for optical sensors and is now being leveraged for replicating complex optical structures for silicon photonic packaging. It offers significant yield and cost advantages for these structures compared to conventional manufacturing methods, such as diamond drilling, laser direct writing and electron-beam writing, which are difficult to scale up to larger substrates and limited in their throughput. Incorporating the NIL process enables the use of best-performing dies and the ability to efficiently bring these high-quality patterns into production lines. In particular, the precise alignment to the underneath optical structures on the photonic chip is crucial for the excellent coupling performance needed within the SiPh packaging devices. NIL can also produce complex structures, which typically are not possible to produce through standard CMOS processes, such as optical coupling elements of mirrors and lenses with sharp edges, curved surfaces or structures with high and low aspects ratios. The ability of NIL to provide high pattern fidelity, repeatability and accurate placement of optical elements on SiPh wafers plays a key role in shifting the typical fiber packaging complexity from the assembly domain to the wafer manufacturing domain.

Teramount collaboration

EVG's collaboration with Teramount illustrates how NIL can help enable a paradigm shift in SiPh packaging. Teramount implements its PhotonicPlug and PhotonicBump wafer-level optical elements through the use of NIL – aligning photonic packaging with standard semiconductor manufacturing and packaging flow. NIL provides an ideal platform for post-processing of silicon photonic wafers for the photonic "bumping" process to be performed either at semiconductor foundries or at outsourced semiconductor assembly and test (OSAT) facilities.

NIL has been used to imprint PhotonicBumps on eight-inch SiPh wafers for performing wafer-level optical coupling elements from and to waveguides of photonic integrated circuits. Figure 3a shows PhotonicBumps imprinted next to a multi-channel SiPh chip, and Figure 3b shows a close-up of a PhotonicBump imprinted in close proximity to a single waveguide channel. PhotonicBump incorporates a deflector mirror imprinted inside a 20-micron cavity depth and a second element of lensed mirror. The deflector mirror performs vertical beam deflection to enable wide-band surface coupling as a replacement for the complicated side-coupling geometry, which is typically used in silicon photonics packaging. The lensed mirror is used for beam expansion for establishing a self-aligning optical scheme[1] and for generating large assembly

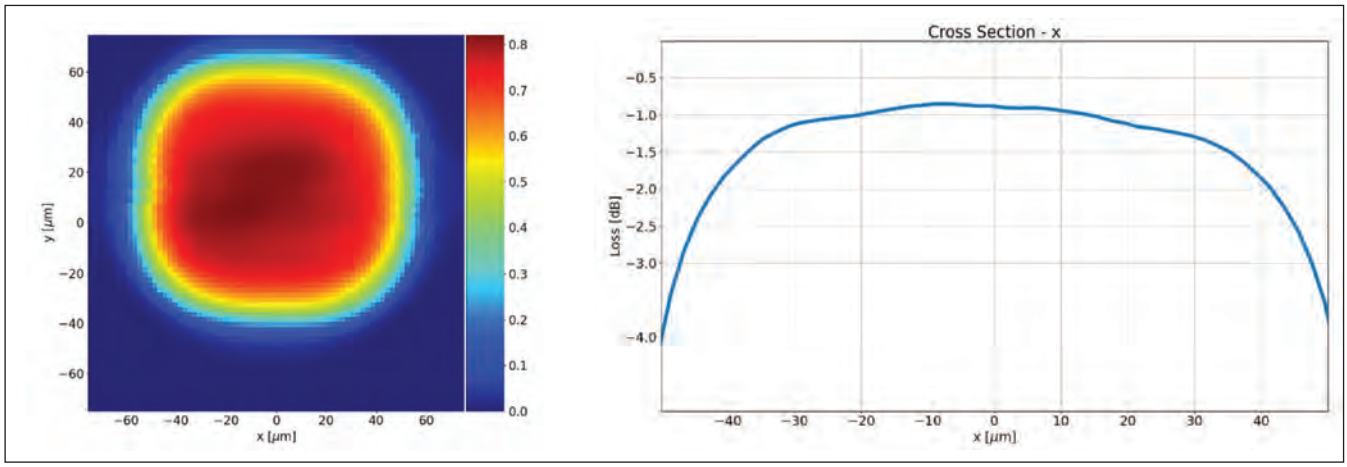


➤ Figure 4: Top) a diagram of PhotonicPlug fiber connector assembled on a "bumped" SiPh chip; above) PhotonicPlug optical elements including single-mode fibers, deflector mirror and beam expansion mirror. PhotonicPlug optics form a self-aligning optical scheme when combined with PhotonicBump optics.

tolerances when combined with PhotonicPlug fiber connectors shown in Figure 4.

Figure 5 shows the optical coupling performance of PhotonicPlug when packaged with a bumped SiPh chip. Figure 5a shows XY tolerance map and Figure 5b shows x-cross section with a large assembly tolerance of >±30µm/0.5dB and a total insertion loss of 1dB from fiber to waveguide. Such superior performance demonstrates PhotonicPlug and PhotonicBump capabilities as well as the advantages of NIL technology to perform accurate placement of wafer-level optical elements.

Working in conjunction with Teramount's PhotonicBump packaging technology, NIL is making wafer-scale packaging possible in the photonics industry, which could have a profound impact on lowering packaging and overall product costs. Whereas packaging is still a relatively small (but growing) share of overall CMOS production costs, it presents the majority of overall cost in photonics manufacturing, which still relies on single device packaging schemes. Wafer-level integrated



➤ Figure 5: a) Measured XY map of PhotonicPlug assembly tolerances when coupling to SiPh chip; b) X-cross section of PhotonicPlug assembly tolerance presenting >±30µm/0.5dB and a total insertion loss of 1dB from fiber to waveguide.

photonics, enabled by NIL and PhotonicBump packaging, has the potential to flip this equation. Through this combination of NIL process and innovative optical elements, the bottleneck in SiPh packaging is being shifted to the optical design rather than fiber assembly tolerance.

NILPhotonics Competence Center: A flexible cooperation mode

As part of the joint-collaboration between EVG and Teramount, EVG provided NIL process development and prototyping services through its NILPhotonics Competence Center, as well as expertise in both CMOS and photonics manufacturing, to assist Teramount in accelerating the development and productization of its PhotonicPlug technology.

EVG's NILPhotonics Competence Center provides an open access innovation incubator for customers and partners across the NIL supply chain to collaborate to shorten development cycles and time to market for innovative photonic devices and applications.

The center is highly flexible and adapts to the varied needs of customers while ensuring the highest level of IP protection for every aspect of development. The cleanroom is designed to meet the most stringent customer requirements and allows for virtual line concepts where wafers are reintroduced into customer fabs for further processing.

ACKNOWLEDGEMENT & REFERENCES

➤ The author wishes to thank Hesham Taha of Teramount for his assistance with the development of this article.

➤ [1] "Photonic plug for scalable silicon photonics packaging", A. Israel et al. Proc. SPIE 11286, Optical Interconnects XX, 1128607 (28 February 2020); doi: 10.1117/12.2543490

Optiwave

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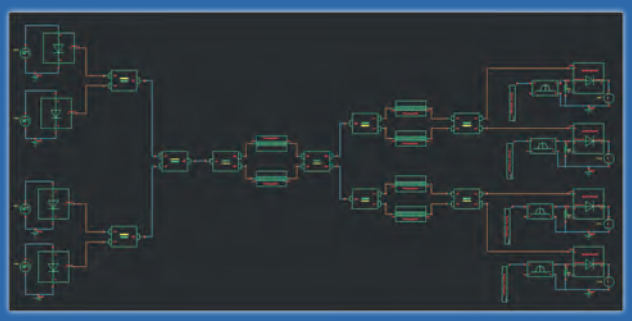

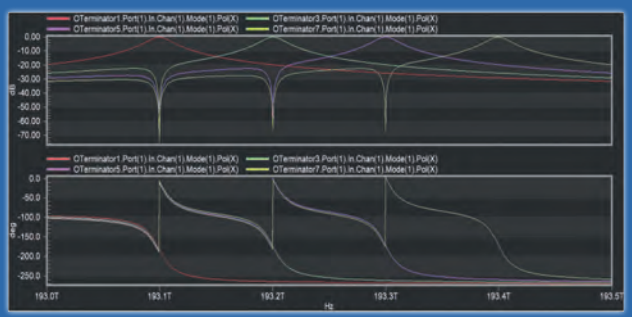

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The Best of Both Worlds: Mature hybrid integration & its applications

The continuously widening application range of photonic chips requires a practical approach to getting the most out of the available toolkit. Hybrid integration of photonic platforms is a versatile way of scaling module production with optimal performance.

By LIONiX INTERNATIONAL

WITH THE commercial success of integrated photonics continuing apace, the industry continues to search for methods to streamline production while boosting its chips' unique advantages. One persistent source of inspiration for integrated photonics is integrated circuits. In the history of integrated circuit development, the use of a single chip to integrate many electronic functions was definitional in its success.

This monolithic integration is a much sought-after goal within integrated photonics. At the same time, this makes monolithic integration of photonic integrated circuits (PICs) a legacy ambition. It should seem odd that the future of a novel technology is envisioned in its ability to replicate the success of a former one, but the reasons are sound enough that this strangeness is overlooked. Monolithic integration would lower production costs of PICs and centralize many of its processes. As of now, it remains an ambition.

With the various advantages that different photonic platforms over each other, it seems unlikely that one platform will rule them all. The functions built into photonic modules need both active and passive platforms, often requiring different platforms of the same kind to achieve the best performance. Fusing the platforms together after initial processing to create a single block of functional materials became the surrogate goal. Heterogenous integration has advantages of its own, most clearly in terms of the total size of the devices.

However, it also has its own unique challenges: how do we engineer dependable paths past different materials reacting to various conditions differently? New attempts at answering this question are published in peer reviewed journals daily. Once those arrive at a consensus, new machines and processes that can replicate these methods at high volumes must be invented to make heterogenous integration cost effective. This was also the case with electric circuits- only at massive quantities did the margins on monolithic chips make business sense.

In the meantime, a more direct and ultimately practical approach to the incorporation of different platforms exists in hybrid integration. The difference is subtle: in hybrid integration, the different photonic platforms remain separate, but are connected to each other. There are various advantages to this approach.

To start with, hybrid integration techniques have ceased to be experimental years ago. In most cases, they are simple reapplications of CMOS techniques, with alterations to fit the light-based operations of PICs. The performance these techniques deliver is reproducible. The yields of the processes are known. They are also cheap, and many of the machines used for their automated execution are adapted from their CMOS counterparts. Active alignment machines are a prime example that keeps getting better.

Nonetheless, there are some affordances specific to the integrated photonic industry to consider. The simplest method to attach an optical fiber to a photonic chip, or to attach two photonic chips together, is to use an adhesive and stick them together. Butt-coupling of this kind requires very accurate alignment, as the slightest discrepancy can cause the light to be absorbed or reflected away.

The choice of adhesive is also critical, as organic glues can absorb light in the blue region of visible light. Another factor to consider is the mode field diameter of the light in waveguides of different

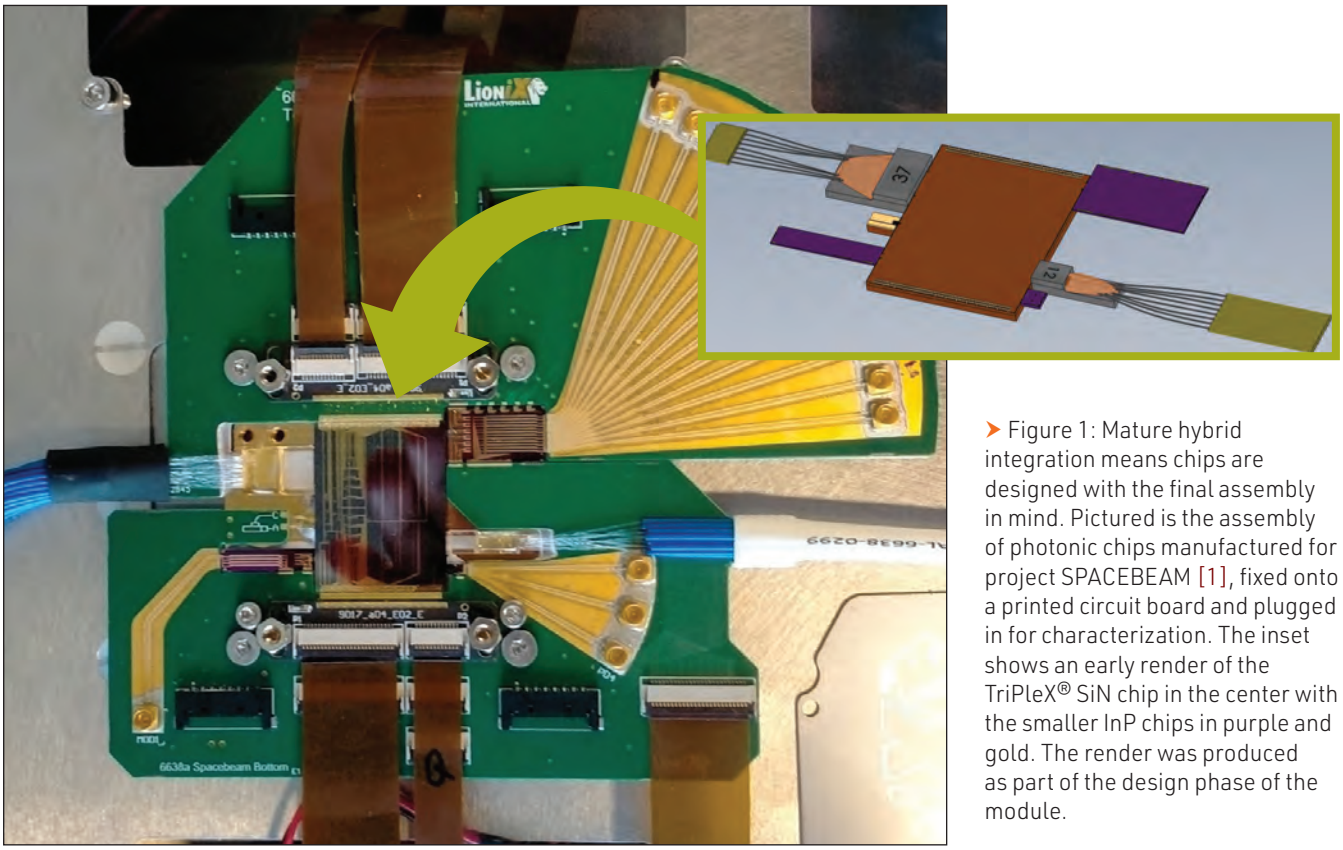


Figure 1: Mature hybrid integration means chips are designed with the final assembly in mind. Pictured is the assembly of photonic chips manufactured for project SPACEBEAM [1], fixed onto a printed circuit board and plugged in for characterization. The inset shows an early render of the TriPleX® SiN chip in the center with the smaller InP chips in purple and gold. The render was produced as part of the design phase of the module.

platforms. Without accounting for different diameters across platforms and fiber optics, there will always be signal losses at the periphery. Suffice to say that hybrid integration itself requires extensive engineering to ensure low optical losses. Such best practices are optimized over many iterations of hybrid assembly for different applications. Out of such cumulative experience, certain applications can be identified as commonplace archetypes of the potential in integrated photonics altogether. The following are such exemplary case studies from our work in LioniX International.

Mature integration processes cut on development time

Indium phosphide (InP) is one of the better-known waveguide platforms deployed in integrated photonics. Its key asset is its ability to generate light. This makes InP chips ideal as gain sections or amplifiers. However, the optical losses within InP make it less ideal for passive waveguides or delay lines. Silicon nitride (SiN) has very low optical losses, but is a passive material unable to generate or detect light. Our own TriPleX® technology is a SiN-based platform that further lowers the losses of standard SiN. TriPleX® makes for an excellent platform for optical modulators and filters, so combining it with InP became standard practice for our designers.

Using InP as a gain section and TriPleX® as a modulator, we fabricated a tunable laser with a miniscule form factor that produces 90 mW of power with a linewidth of less than 1 kHz and tunability over the entire c-band [2]. Using in-house design expertise and careful polishing of the interfaces, we were able to lower the optical loss across each interface to 1 dB, with only 3 dB loss from the bare InP chip.

The external cavity of the TriPleX® chip hosts a phase modulator, micro-ring resonators for wavelength modulation, and a power controller. Using SiN's broad transparency and these chip building blocks allowed the optimization of the laser to other wavelength ranges, such as near infrared (780 to 850 nm) and the visible (420 to 680nm) spectrum. This specialization of functions across the two photonic platforms granted the best of both worlds without cutting back on the advantages of integrated photonics.

Stuffing an antenna into a lunchbox

The first ever fully optical beamforming network (OBFN) was made by us in 2018. As neat as these assemblies looked, they came out of years of optimization work. In earlier days, chips were simply connected with wires, and the assembly process was anything but simple. Not only did these take a lot of time and effort to put together, they were also fragile products which had to be treated very gently during characterization. These were not ready for in-situ deployment.

By 2018, however, the picture had changed dramatically. By this stage, vertical integration was

part and parcel of our work. PICs were designed with final assembly in mind, and their electronics and packaging were co-designed at the same pre-production stages.

Modules for the transmission and reception of radio frequencies were designed and assembled, with the TriPleX chips fabricated in house. The modules included lasers, such that optical signal generation and processing was handled within the assembly. Those lasers followed the same principle as was described in the earlier section: InP gain sections butt-coupled to TriPleX.

However, the TriPleX chips in these modules did more than tune light into a target range. By integrating another InP chip, this one acting as a modulator, to the TriPleX chip, the TriPleX acted as a central hub for the translating of the radio frequency signal into an optical signal and vice versa.

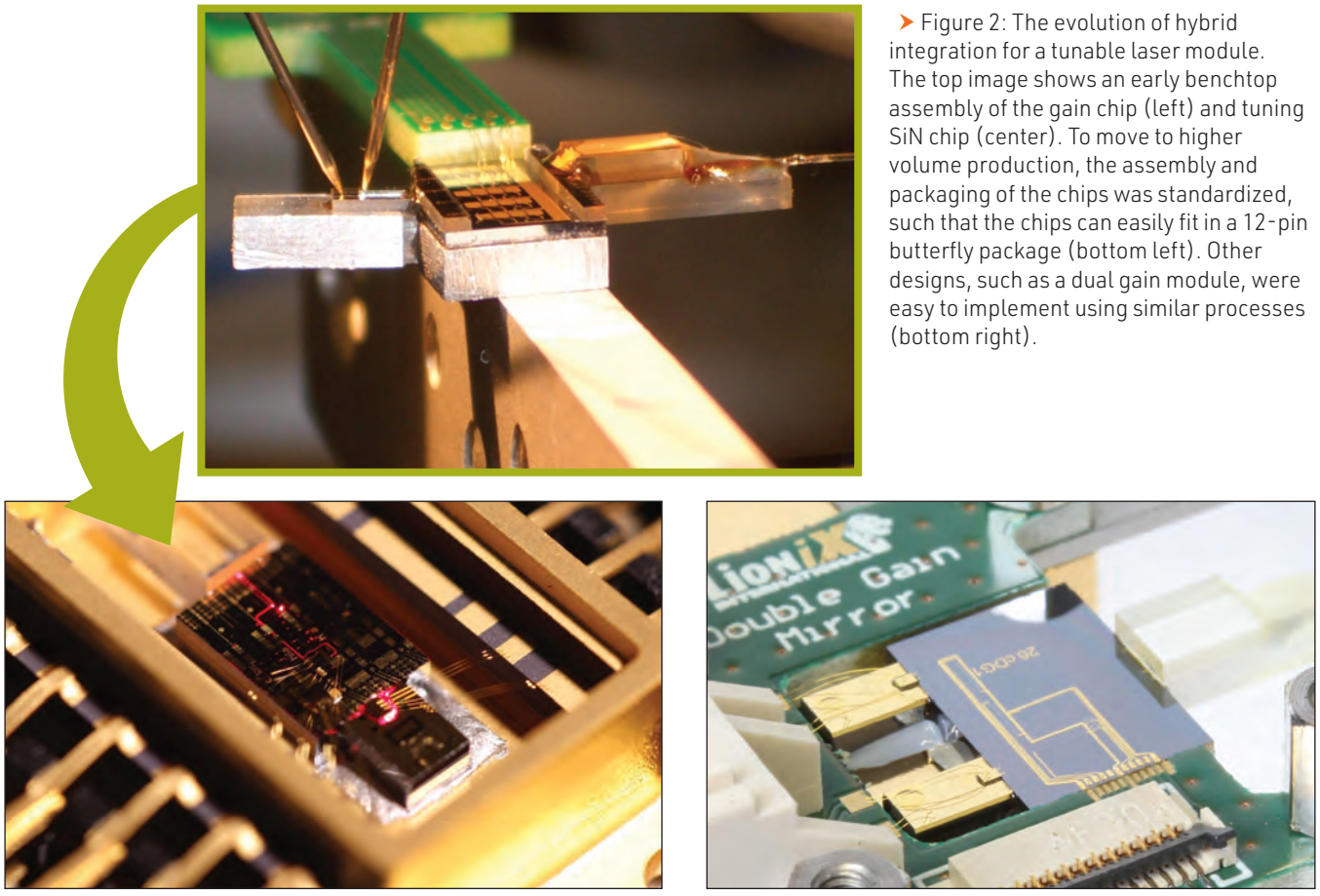
For transmission, a photodetector array was included to convert the optical signal into RF, and switch delays were used to collate the signal. For reception, microring resonators were used to apply continuous delay to the received signal, and photodetectors were not implemented to allow remoting. Fiber arrays were used as the optical interfaces for the assemblies. What was remarkable even then was that the chips used in these assemblies were all mass-producible. With only the assembly as a bottleneck, scalable volume production was possible.

Since then, the OBFN went through many iterations, especially as it was redesigned for different applications. The OBFN was deployed in the distribution of 5G signals in a wide area without the use of antennae, in groundstation technology for satellite communication as well as satellite-side and on airplanes. Photodetectors became standard in our OBFNs to ensure that they were RF-in, RF-out. They became smaller, cheaper, and more robust.

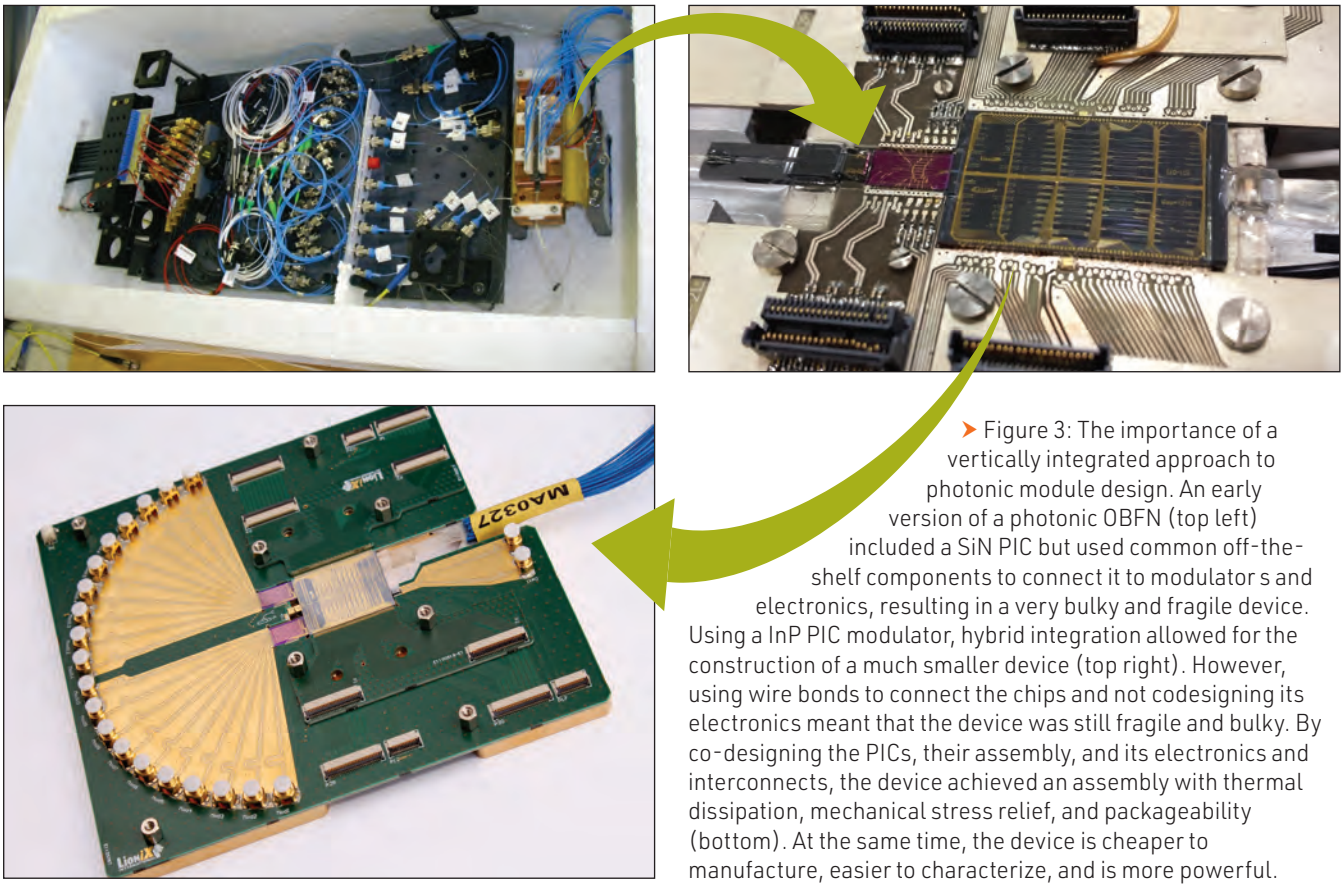
Scaling production for consumer markets

In the earlier examples, the low loss performance of the assembly is crucial to their function. The butt-coupling approach is favored in them for that reason, as active alignment can ensure the low losses necessary. Such markets can handle high end, medium volume applications.

To scale production to even higher volumes, new hybrid approaches are being developed. A common one is the etching of holes in the SiN wafers and then flip-chipping the semiconductor components into it [3]. This approach can be done at wafer scale through passive alignment. This enables its use for the high-volume quantities needed in telecommunications or consumer electronics applications. In the visible range, this process



➤ Figure 2: The evolution of hybrid integration for a tunable laser module. The top image shows an early benchtop assembly of the gain chip (left) and tuning SiN chip (center). To move to higher volume production, the assembly and packaging of the chips was standardized, such that the chips can easily fit in a 12-pin butterfly package (bottom left). Other designs, such as a dual gain module, were easy to implement using similar processes (bottom right).



➤ Figure 3: The importance of a vertically integrated approach to photonic module design. An early version of a photonic OBFN (top left) included a SiN PIC but used common off-the-shelf components to connect it to modulator s and electronics, resulting in a very bulky and fragile device. Using a InP PIC modulator, hybrid integration allowed for the construction of a much smaller device (top right). However, using wire bonds to connect the chips and not codesigning its electronics meant that the device was still fragile and bulky. By co-designing the PICs, their assembly, and its electronics and interconnects, the device achieved an assembly with thermal dissipation, mechanical stress relief, and packageability (bottom). At the same time, the device is cheaper to manufacture, easier to characterize, and is more powerful.

can be adapted for use in augmented reality (AR) glasses [4]. Red, green, and blue laser diodes can be flip-chipped onto the SiN wafer to make a light engine that combines the three laser modes into a single optimized one at the output. As no additional packaging is required, the light engine is very compact and manufacturable in high volumes.

Therefore, hybrid integration includes many more techniques than simple butt-coupling. Micromachined mirrors can be placed at 45° angles to waveguides, allowing for vertical out-coupling of the light. Grating couplers allow the same thing, with the possibility of splitting the light by wavelength. Free space out-coupling allows for light interference effect to be engineered into applications. Nonetheless, what is crucial about hybrid integration is that it is functional. For the PIC industry to have a felt impact in technological advancement, techniques must exit the laboratory and be implemented in consumer-grade products. With multiple waveguide platforms being necessary, and monolithic fabrication in early research stages, hybrid integration unites different material properties with market-ready processes. It is the best of both present worlds.

REFERENCES

- [1] Manuel Reza, Giovanni Serafino, Tobias Otto, Ahmad Mohammad, Hakimeh Mohammadhosseini, Leili Shiramin, Francesco Floris, Matthias Kolb, Dave Bail, Simone Gabrielli, Chris Roeloffzen, Paul van Dijk, Amin Abbasi, Bart Desoete, and Paolo Ghelfi, "Design and Performance Estimation of a Photonic Integrated Beamforming Receiver for Scan-on-Receive Synthetic Aperture Radar," J. Lightwave Technol. 39, 7588-7599 (2021)
- [2] Lin, Y., Browning, C., Timens, R. B., Geuzebroek, D., Roeloffzen, C. G. H., Hoekman, M., Geskus, D., Oldenbeuving, R. M., Heideman, R. G., Fan, Y., Boller, K., & Barry, L. P. (2018). "Characterization of Hybrid InP-TriPleX Photonic Integrated Tunable Lasers Based on Silicon Nitride (Si 3N4/SiO2) Microring Resonators for Optical Coherent System," in IEEE Photonics Journal, vol. 10, no. 3, pp. 1-8, June 2018, Art no. 1400108, doi: 10.1109/JPHOT.2018.2842026.
- [3] Michael Theurer, Martin Moehrle, Ariane Sigmund, Karl-Otto Velthaus, Ruud M. Oldenbeuving, Lennart Wevers, Ferry M. Postma, Richard Mateman, Frederik Schreuder, Dimitri Geskus, Kerstin Wörhoff, Ronald Dekker, Rene G. Heideman, and Martin Schell, "Flip-Chip Integration of InP to SiN Photonic Integrated Circuits," J. Lightwave Technol. 38, 2630-2636 (2020)
- [4] Brilliance. Retrieved October 14, 2022, from https://www.brilliancergb.com

Spain could prioritize PIC manufacturing to lead in EU photonics

Spain is working to create an infrastructure for semiconductor chip fabrication, but despite subsidies of just over €12 billion, Spain has found it challenging to attract manufacturers. The European Photonics Industry Consortium (EPIC) looks at the challenges involved and opportunities for alternative investment in Spain's vibrant Photonic Integrated Circuits (PICs) ecosystem.

BY DR. IVAN NIKITSKIY, PHOTONICS TECHNOLOGY MANAGER, EUROPEAN PHOTONICS INDUSTRY CONSORTIUM (EPIC)

The race for semiconductors

Semiconductor chips are essential for all electronic devices and subsystems ranging from TVs, computers, and laptops to smartphones, vehicles, and medical diagnostic equipment; demand is so great that microchips are seen as the "new oil" of the 21st century.

However, over the last two decades, the global electronics industry has become increasingly dependent on semiconductor manufacturers in Taiwan, South Korea, and China, who, in 2019, accounted for 78% of the world's semiconductor fabrication capacity. In light of the global semiconductor shortage that began in 2020, this dependency is now seen as a national security issue across both Europe and in the US. Accordingly, in February 2022, the US Congress approved the Chips and Science Act that allocated $52 billion to help US companies manufacture semiconductor chips with the aim of "re-establishing American leadership in the technology." The EU followed suit in February 2022 with their own Chips Act comprising a pledge of €43 billion to reduce "excessive dependencies on Taiwan, the United States, South Korea, Japan and China" by boosting

Europe's market share of chip production from around 9% in 2022 to 20% by 2030.

Spain's contribution to this target is its "Strategic Project for the Recovery and Economic Transformation of Microelectronics and Semiconductors", known as PERTE Chip. The aim is to invest €12.25 billion from an addendum to the country's post-Covid Recovery, Transformation, and Resilience Plan to bolster its semiconductor industry[1]. The plan is to be structured around four pillars:

1. Strengthen R&D on cutting-edge microprocessors, alternative architectures, integrated photonics, and quantum chips.
2. Foster the creation of fabless companies, test pilot lines, and semiconductor training networks.
3. Boost the European IT manufacturing industry with an incentive scheme to create a chip pool.
4. Install manufacturing plants in Spain with capacities above and below 5 nm.

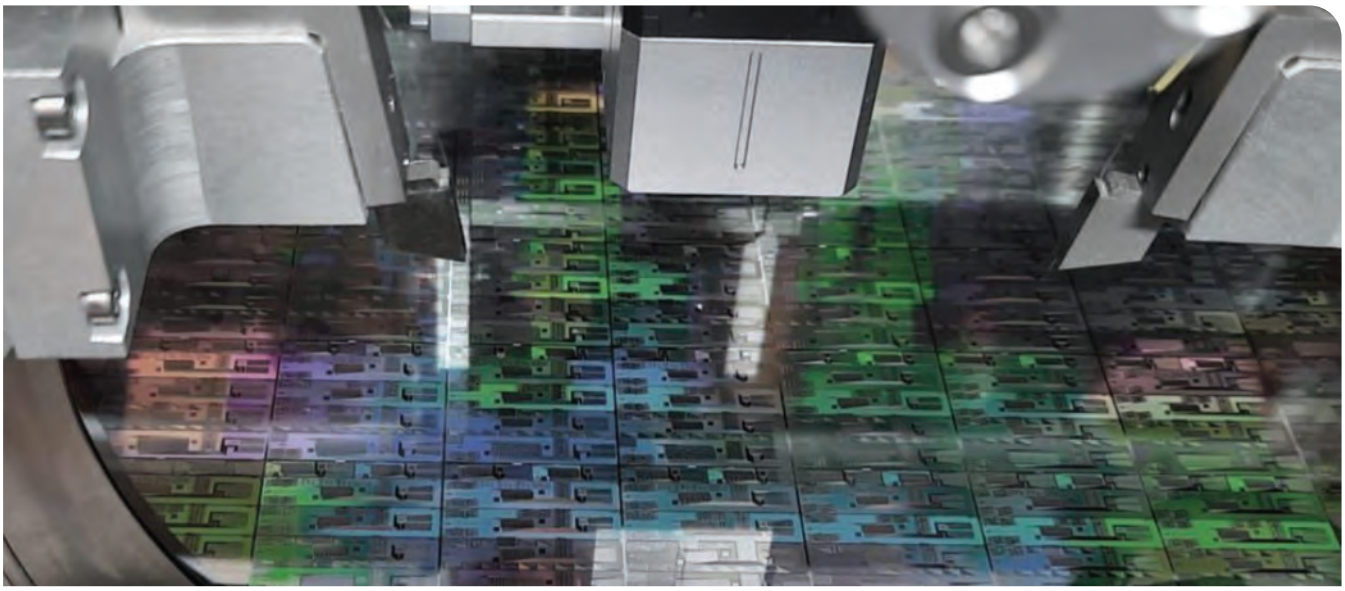
While the first three objectives appear feasible to many industry observers, many also believe that the aim to install manufacturing plants in Spain with capacities below 5nm is unrealistic[2]. Considering that the cost to build, equip and staff a state-of-the-art sub-5nm semiconductor fab is now estimated at $50 billion, the €12.25 billion investment planned so far would fall short of building even a single plant. Smaller device features at nanometre scale translates into a higher number of transistors that can be fitted into each finished chip, leading to potentially more powerful chips. The chips in Apple's latest iPhone, for example, are 5 nm, which are considered the leading edge for mass, in-production technologies even as TSMC readies its 3 nm process for widespread access. The idea for PERTE is to allocate €7.2 billion to 5 nm processes, with €2.1 billion going to manufacture less advanced architectures of between 14 and 28 nm, which are the most commonly used in the automotive industry. But given the cost of leading-edge semiconductor fabs, and the fact Spain has no semiconductor ecosystem on which to build, home-grown semiconductor manufacturing can only become a reality by convincing companies like America´s Intel, Taiwan's TSMC, or South Korea's Samsung to build factories in Spain and create an ecosystem from scratch. The first obstacle is that this will require an enormous investment in equipment. The machinery used to produce 170 nm circuits is around $1 million for each major process tool, and each manufacturing plant would need several of these machines. The lithography machines using EUV ultraviolet light made by ASML, such as those used by leading companies like TSMC and Samsung, are far more expensive, ranging from $150 - $300 million. For this reason, manufacturers tend to look for territories with an already established industry, and several European countries have a certain advantage over Spain. For example, Spain has tried to lure TSMC, but the company is expected to opt for Germany, where there is already a large chip ecosystem in the eastern state of Saxony. Similarly, France already has companies like Global Foundries Inc. and STMicroelectronics producing energy-efficient chips. A second obstacle is the amount of investment available. Even though PERTE Chip's €12.25 billion is the most significant investment project of its kind in Spain, it is far behind the other international efforts taken in the sector. In the case of Taiwan's TSMC, one of the industry leaders, its investment between 2021 and 2023 alone is €100 billion. In the same way, PERTE Chip's budget is lower than Germany's offer of €17 billion for American Intel Corp to build a macro-factory of microchips in Germany to start in the first half of 2023[3].

Perhaps the biggest obstacle for PERTE is the fact that following the recent global chip shortages, all regions are seeking to ramp up domestic production and have more control over the supply chains. For example, Japan and China are working hard towards chip self-sufficiency; Korea´s SK Hynix aims to become the world´s third-largest semiconductor company – an achievable goal according to most experts.

Spain's PIC industry

If the aim of setting up semiconductor manufacturing in Spain ultimately proves unfeasible, investment in Spain's photonics integrated circuits (PICs) industry would be a good alternative. In the last two decades, Spain has built up a vibrant photonics ecosystem, particularly in the field of photonic integrated circuits

➤ Figure 1. National Microelectronics Center (IMB-CNM) in Barcelona.



➤ Figure 2. Wafer-level PIC testing at VLC Photonics.

(PICs). Unlike conventional semiconductors that are based on the flow of electrons, PICs are based on the flow of light employing components such as laser diodes, waveguides, filters, and gain media. While microelectronic devices offer advantages in many different types of applications, PICs offer numerous advantages over conventional ICs in data and other communications applications such as higher speed, greater bandwidth, and lower energy loss. The main problem with photonics from a business and technology perspective is that while the semiconductor industry is mature, the photonics industry is still in development, finding applications in telecommunications, sensing, and defence. Compared to microelectronics, photonics has been considered a niche industry. Yet technology always moves forward and new photonic applications are being discovered every day. Technologies utilizing both photonic and microelectronic circuits are rapidly advancing; it is just a matter of time until PICs become a commonplace component in consumer technology.

For this reason, Spain would be wise to allocate a sizeable chunk of PERTE Chip's €12.25 billion to support the work of Spanish companies and organizations represented in every aspect of photonic integration:

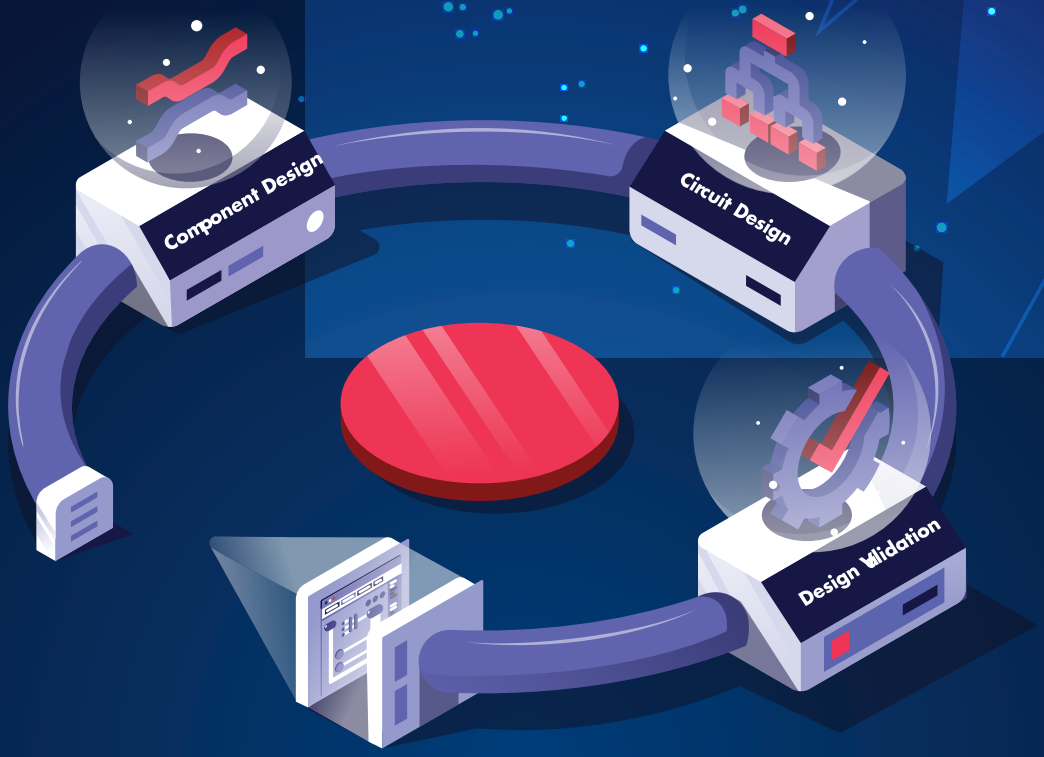
Research and Development:
Spain has several research and development centers working in the field of photonics and optical engineering. These include CD6 - Centre for Sensors, Instruments and Systems Development, a spin-off from the University Polytechnic of Catalunya which focuses on the areas of metrology, visual optics, optical design & simulation, and colour; and also FYLA, based in Valencia and Barcelona who make lasers and systems for a multitude of applications from hyperspectral imaging and metrology to optical communication and material processing. The two most important research organizations in photonics are the Institute of Optics in Madrid, part of the Spanish government's network of research centers, and the world-renown ICFO - The Institute of Photonic Sciences founded in 2002 in Catalunya.

Frontend Integration:
The Institute of Microelectronics of Barcelona (IMB-CNM) has developed a silicon nitride (SiN) Photonic Platform for PIC prototyping. Their mission is to carry out applied research based on micro and nanotechnologies, mainly focused on the development of components and micro and nano systems. The infrastructure and equipment allow for the development of processes for the realization and characterization of photonic and electronic: micro-nano devices, integrated circuits, and micro-nano systems intended for research, development, and technology transfer to industry.

Backend Integration:
UPVfab, located at the University Polytechnic of Valencia has a micro-fabrication R+D and pilot line cleanroom facility. Their mission is to perform transversal activities to serve and educate the academic and industry communities about micro- and nano-fabrication. UPVfab together with the IMB-CNM has developed a versatile, moderate confinement Silicon Nitride platform for photonic integrated applications, running under a Multi-Project Wafer scheme or dedicated runs. The facility comprises 500 m^2 cleanrooms ISO-7 (class 10.000) and positions with automation tools for the backend processing of semiconductor wafers.

Chip Design and Testing:
VLC Photonics is a world-leading engineering company offering a full range of services for the development of Photonic Integrated Circuits (PICs), with a focus on design in testing at both die and wafer levels. The current service portfolio includes techno-economic feasibility studies and consultancy, in-house PIC design, characterization and test, and full PIC prototyping through external manufacturing

LUCEDA PHOTONICS



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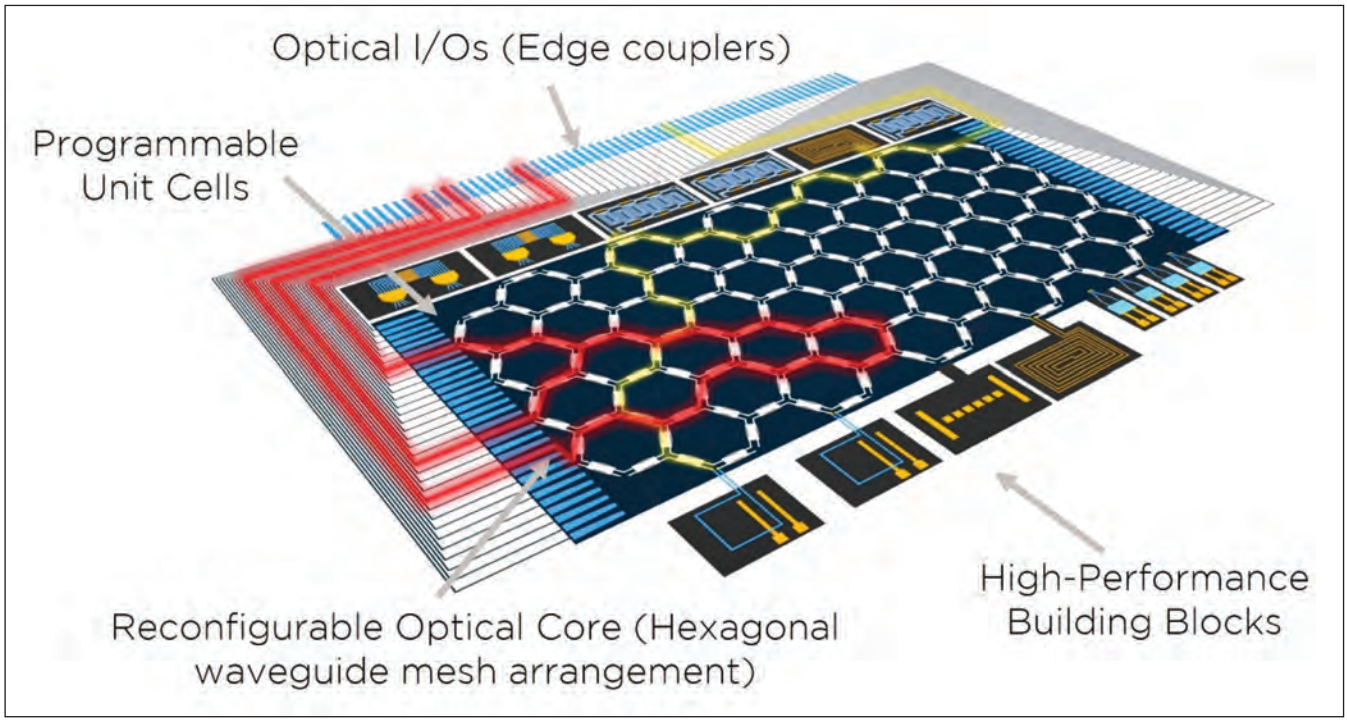

➤ Figure 3. Photonic layout of the iPronics´ SPPGA-based SmartLight Processor.

and packaging/assembly partners. VLC Photonics, as a pure-play fabless design house, works with multiple foundries and has expertise in all the main photonic integration technologies, including Silicon-on-insulator, PLC, SiN, InP, LNOI, and GaAs. VLC Photonics also works closely with foundries in the development of their Process Design Kits (PDKs), allowing external users to easily access their manufacturing capabilities. The organization has world-leading capabilities for RF testing up to 110 GHz and has also provided unique edge-coupling wafer-level testing since 2020. VLC Photonics is part of Hitachi, Ltd.

Field Programmable Photonic Gate Arrays: iPronics, a spinoff company from the University Polytechnic of Valencia, Spain is developing the innovative concept of Field Programmable Photonic Gate Arrays (FPPGAs), which are based on common optical hardware configurable through software to perform multiple functions. iPronics is working on the development of future information processing systems where electronics and photonics work cooperatively by synergistically exploiting the best capabilities of each technology. Applications include 5G and 6G telecommunications, data center interconnection, artificial intelligence, signal processing, sensing, and quantum information.
III-V semiconductors foundry: The city of Vigo in Spain will be the location of a new state-of-the-art foundry for III-V-Semiconductor-based photonics called SPARC. This new company will consist of a 1.600 m^2 cleanroom for wafer production and a research center that will assist customers in bringing fully-certified photonic products to the market. The foundry expects to be operational around late 2023 and SPARC aims to capitalize on the potential of III-V to accommodate the increasing number of markets and applications that rely heavily on light, photonics, and high-speed electronics. III-V Semiconductors are the only class of materials that can be used to realize very compact- and efficient light sources and detectors across a very wide wavelength range from the ultraviolet up to the mid-infrared.

Consequently, SPARC will have the capability and capacity to address a large customer base across a wide range of different markets, including optical communications, displays, lighting, aerospace, automotive, biomedical, sensing, and quantum technologies, as well as high-speed- and/or high-power electronic applications for which the III-V Semiconductor technology is equally well suited for. From this brief overview, it can be seen that while missing the capabilities in traditional chip manufacturing Spain has a well-established organic ecosystem in the production of photonic chips. With the right level of investment, and if the right decisions are taken – this country famous for its beautiful weather and cheerful people could also become the European reference in photonic integration.

FURTHER READING

[1] https://www.eetimes.eu/spain-approves-e12-25b-semiconductor-investment-plan/

[2] https://www.bloomberg.com/news/articles/2022-08-02/spain-short-on-takers-for-12-billion-in-semiconductor-subsidies

[3] https://www.euronews.com/next/2022/03/15/intel-set-to-build-a-new-17-billion-chip-manufacturing-hub-in-germany-as-it-pours-money-in

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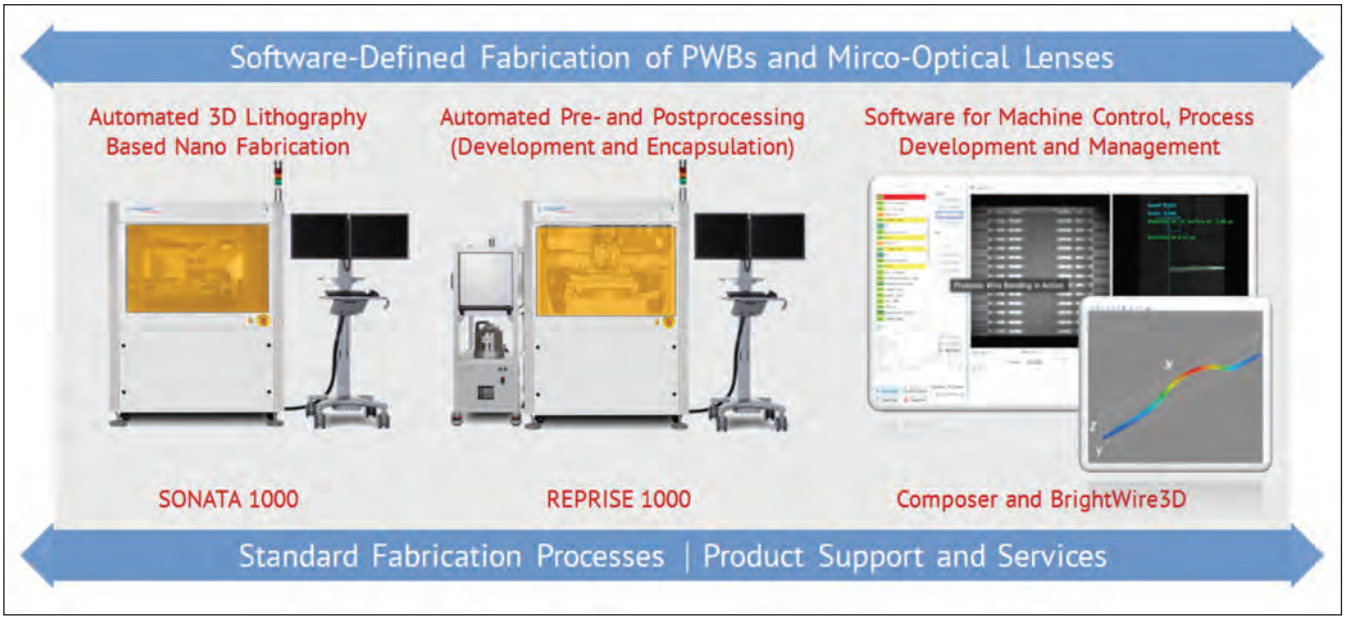
Enabling next generation photonic integration and packaging solutions with Photonic Wire Bonding (PWB) and Facet-Attached Micro-Lenses (FAML)

With the growth of photonic integrated circuits comes the need to innovate quickly. This innovation acceleration is made possible by the creation of Photonic Wire Bonding. Much as electrical integrated circuits have benefitted from electronic wire bonding, photonics innovations will now advance on a faster trajectory. By Vanguard Automation GmbH, Karlsruhe, Germany

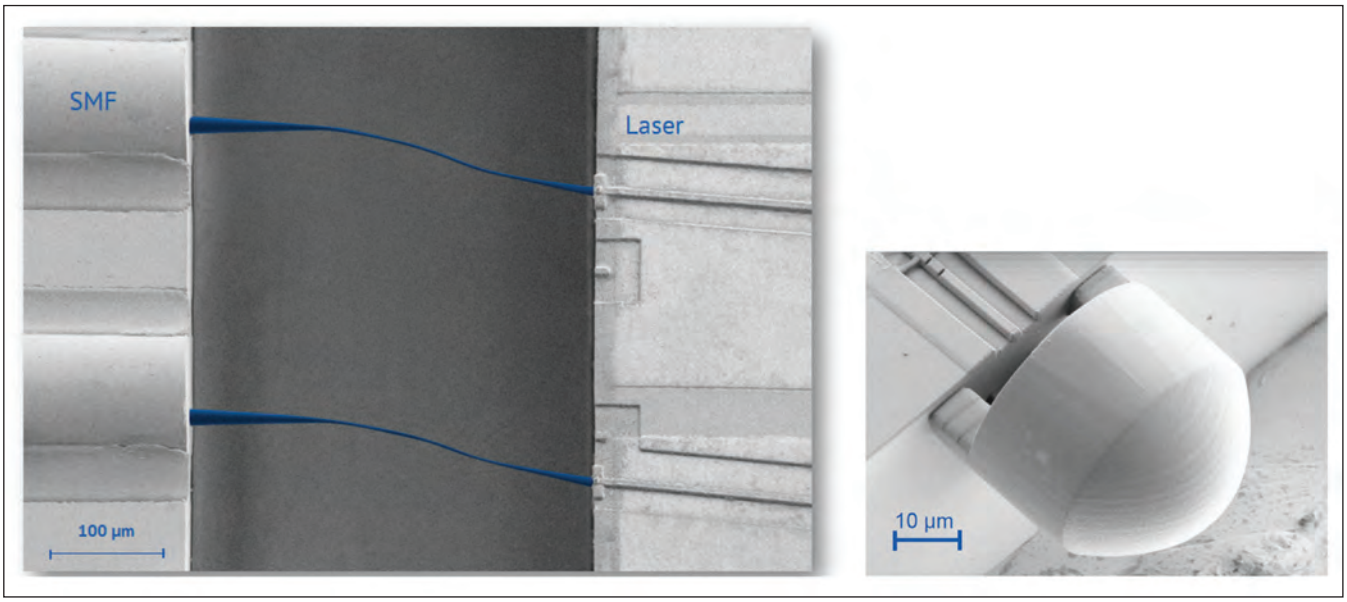
BY VANGUARD AUTOMATION GMBH, KARLSRUHE, GERMANY

ENABLING next Generation Photonic Integration and Packaging Solutions with Photonic Wire Bonding (PWB) and Facet-Attached Micro-Lenses (FAML).

With the growth of photonic integrated circuits comes the need to innovate quickly. This innovation acceleration is made possible by the creation of Photonic Wire Bonding. Much as electrical integrated circuits have benefitted from electronic wire bonding, photonics innovations will now advance on a faster trajectory. Photonic Wire Bonding creates low-loss, 3D free-form connections between optical components. Built on advanced nano-print technology, Photonic Wire Bonding is inherently automatable and provides a high degree of design flexibility. Additionally, 3D nano-printing can also be used to fabricate facet-attached



➤ Figure 1: Vanguard Automation's fully automated photonic integration and packaging solution vanguard SYMPHONY comprising the automated 3D lithography based nano fabrication unit SONATA 1000 and the automated pre- and postprocessing unit REPRISE 1000. The systems are equipped with Vanguard's BrightWire3D software enabling highly precise detection and on the fly trajectory calculation. Vanguard's own photoresists, standard process development as well as product support and services complete Vanguard's solution for prototyping and mass production.



➤ Figure 2: left Scanning electron beam microscope image of Photonic Wire Bonds connecting a single mode fiber array with an array of indium phosphite based lasers from Vanguard's partner FREEDOM PHOTONICS LLC (a Luminar company). It has to be noted that the sample is tilted in order to show the vertical offset between the components. right Scanning electron beam microscope image of a Facet-Attached Micro-Lens on an indium phosphite based laser.

micro-optical elements on optical chips and fibers, allowing for low-loss coupling with high alignment tolerances and for wafer-level probing of optical devices.

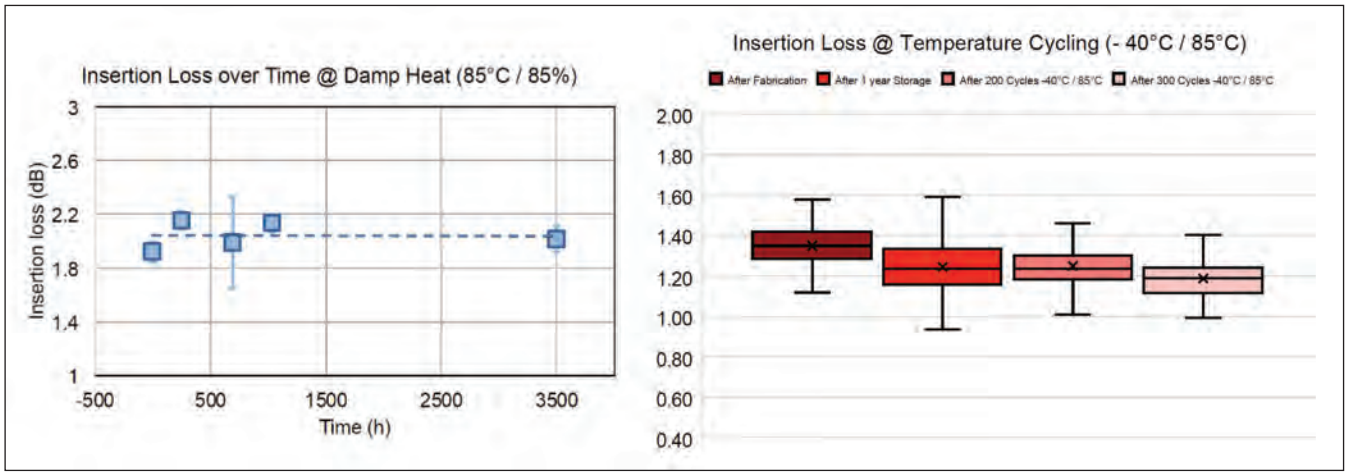
Today's packaging and assembly challenges arise from the necessity to integrate various optical components from different material platforms. A hybrid module comprising, e.g., indium phosphite based active devices such as lasers or semiconductor optical amplifiers, passive devices made from silicon, silicon nitride or lithium niobate as well as photo diodes, and single mode or polarization maintaining fibers imposes a challenge in terms of integration due to their very specific optical properties.

A packaging or integration solution which is viable in industrial mass production has to be able to address and solve challenges arising from these specific optical properties. In order to reduce coupling loss when combining different devices, the specific mode field profiles have to be matched and the devices have to be aligned very precisely. For an industrial mass production process such mode matching and alignment processes have to be very fast and reproducible since speed and yield determine the cost of the product.

Additionally, the packaged assemblies must be reliable under various environmental conditions specific to their applications. These fundamental conditions hold true for a large range of application areas such as tele and data communication, 3D sensing, e.g, lidar as well as quantum applications while the application specific conditions which the packaged assemblies have to meet may vary. Thus, even though devices which are used for such applications are made in sophisticated processes from sometimes exotic material platforms, the optical packaging or integration process represents the biggest cost driver in most cases.

In order to solve this commercial challenge for next generation hybrid multi-chip modules the aforementioned technical challenges have to be resolved. Vanguard Automation has set out to advance photonic packaging and assembly by providing scalable 3D nano-fabrication solutions for prototyping and industrial mass production. Vanguard Automation GmbH is headquartered in Karlsruhe, Germany which is also home to the Karlsruhe Institute of Technology (KIT) and a fast-growing start-up scene. Vanguard started operating in 2018 as a joint venture combing a decade worth of research in silicon photonics and integrated optics from the group of Professor Christian Koos at KIT with 20 years of experience in building industrial machinery for assembly of opto-electronic components and (hybrid) photonic devices contributed by ficonTEC Service GmbH in Achim, Germany. Inspired by electronic wire bonding with its benefits such as fast process times, tight packaging density and loop control Christian Koos and his team of talented engineers developed a method of 3D nano-printed polymer waveguides so-called Photonic Wire Bonds (PWB).

Vanguard Automation then developed the photonic wire bonding technology further into a fully automated solution portfolio comprising two systems for fabrication of PWBs and postprocessing



➤ Figure 3: left Telcordia damp heat test (85°C, 85% relative humidity) result over 3500 hours of Photonic Wire Bonds. Each square represents the average of several tens of PWB. right Telcordia thermal shock/cycling test (temperature cycles of -40 – 85°C) result over 300 cycles of Photonic Wire Bonds. Each block represents the average of several tens of PWB.

of connected optical assemblies, software for automated detection as well as calculation of optimal PWB trajectories, dedicated photoresists, standard processes as well as service and support (see Fig. 1) to enable customers to advance quickly.

In Vanguard's systems single multi-chip assemblies, a tray with many assemblies, or wafers up to 12 inch can be handled which makes them viable for high-throughput production. In Vanguard's SONATA 1000 systems the interfaces which have to be connected by PWBs are immersed in a special photoresist. Vanguard developed and tailored photoresists for specific requirements such as high resolution, strong adhesion on edge-facets and surfaces, and durability. In the SONATA 1000 the immersed devices are brought into contact with a high NA objective lens. This lens focuses a pulsed femtosecond laser into the resist.

First the laser is used to identify the interfaces as well as their orientations with an accuracy of sub 100 nm. Afterwards Vanguard's Bridgewire3D software calculates the PWB trajectory on the fly based on the detected positions and orientations of the interfaces. Then the laser polymerises the photoresist along this trajectory by two photon polymerisation forming the optical connection between the interfaces. Hence, no calibration between detection and printing mechanism is necessary. Such a process comprising detection, calculation, and printing of a PWB is fully automated, reproducible and fast, which makes it viable for industrial mass production. The REPRISE 1000 system removes the unexposed resin, cleans the assembly and encapsulates the PWBs. The packaged assembly can then undergo follow-on processing (e.g. electric wire bonding).

The encapsulation process, or cladding, is done by detecting the PWB area, dispensing a dam, filling in the cladding material, and completed by UV-curing, either locally or with its 12 inch UV flood exposure. Therewith, Vanguard's SYMPHONY comprising SONATA 1000 and REPRISE 1000 enables fully automated photonic packaging and integration of multi-chip assemblies or full wafers for industrial mass production using Photonic Wire Bonding or Facet-Attached Micro-Lenses or a combination of both. All processes on Vanguard's systems are software defined and can be adapted to customer specific requirements. Vanguard Automation, offers process development either directly or through eco system partners who offer development of Photonic Wire Bonding processes adapted to customer assemblies with their own Vanguard systems. In addition, customers can benefit from Vanguard's support and service contracts which, amongst other topics, provide access to PWB experts who assist with the adaption of fabrication processes to new devices.

Vanguard's PWB technology is capable of addressing the fundamental challenges of photonic integration of multi-chip assemblies (see Fig. 2 left). Highly precise alignment of components is no longer necessary due to the highly accurate detection methods and algorithms in Vanguard's systems. Additionally, vertical and/or lateral misalignments of up to +/- 20 µm of the optical interfaces are compensated by the s-shaped trajectories of PWBs (see Fig. 2 left). This allows for a fast pick and place process of components with relaxed placement tolerances rather than a more difficult and time consuming active-alignement process.

This also means that during the PWB writing process no active operation of devices is necessary. Mode-matching happens intrinsically in the process by free-form tapering of PWBs to adapt them to the device specific mode field profiles which can be round, elliptical or rectangular. As shown in Fig. 2

left, the PWB taper facing the single mode fiber (SMF) differs from the taper facing the indium phosphite based laser. Additionally, in case of angled facets or waveguides or rotated devices the PWB taper direction can be adjusted. In Fig. 2 left the PWB meets the laser facet under a specific angle determined by the different effective refractive indices of PWB and laser. Based on these properties PWBs connect various interfaces in multi-chip assemblies enabling a high degree of design flexibility for hybrid multi-chip integration. The software defined processes allow for a quick adaptation when devices have to be changed, e.g., for second sourcing or when devices are added to the product. Additionally, PWBs facilitate a high interconnect or package density due to their very compact size, which also lends itself to short fabrication times.

Vanguard's Facet-Attached Micro-Lenses (see Fig. 2 right) round off Vanguard's photonic integration and packaging solutions. They are a complementary approach to the Photonic Wire Bonds enabling free space optics over larger distances including low-loss coupling with high alignment tolerance. These lenses can be designed with a flexibility in shape including various lens surfaces and total internal reflective mirrors. They are precisely aligned and printed to the interface position and orientation using Vanguard's highly accurate detection mechanisms. For wafer-level probing of optical devices Vanguard's printed wafer-level probers are widely used in research and industry for several years. Hence, Vanguard's wafer-level probers are used by market-leaders in their modern wafer-level probing systems proving the maturity of Vanguard's technology portfolio for industrial applications.

Vanguard's Photonic Wire Bonds as well as Facet-Attached Micro-Lenses have been successfully tested in a wide variation of environmental conditions such as standard Telcordia damp-heat and temperature shock/cycling tests (see Fig. 3), vibration tests, mechanical shock tests as well as for high-power handling, reflow soldering and die bonding. With respect to quantum applications, they also have been tested in low and ultra-low temperature environments.

In summary, Vanguard's Photonic Wire Bonding technology allows to combine the complementary strengths of different optical integration platforms in advanced photonic multi-chip modules leading to compactness, high performance, and great design flexibility. Vanguard's portfolio is completed by Facet-Attached Micro-Lenses on optical chips and fibers, allowing for low-loss coupling with high alignment tolerance and for wafer-level probing of optical devices. All fabrication processes are fully-automated, highly reproducible as well as reliable and used by research and industry customers for next generation photonic integration and packaging.

Silicon photonics is driven by data center applications

Silicon photonic platform maturity and rapidly developing ecosystem will drive a $5.4B datacom market in 2027. And new applications in multiple markets could emerge as well in the future.

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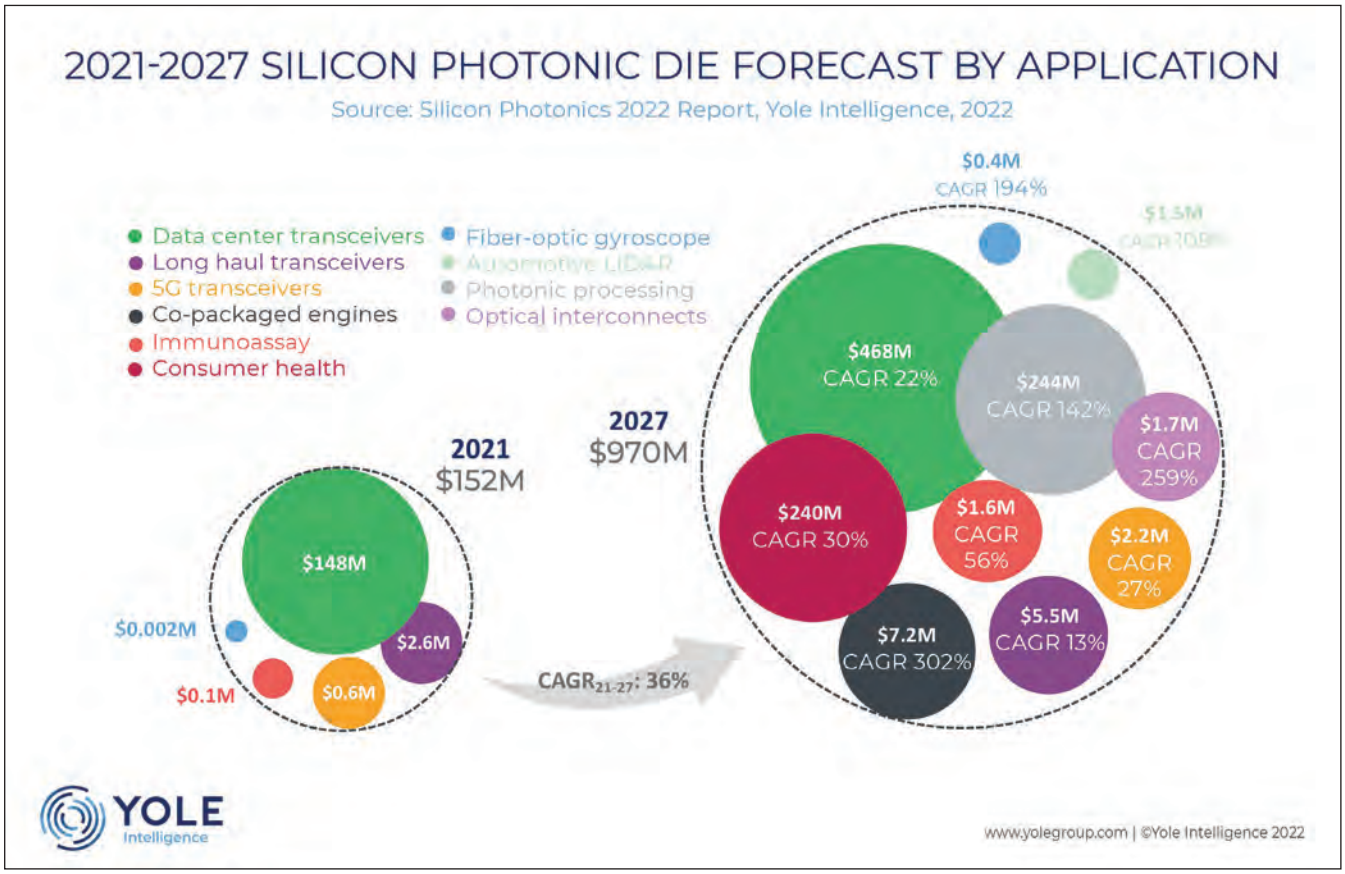
DATA CENTER NETWORKING is currently undergoing profound evolution. This evolution in architecture has, in turn, significant implications for the technologies at the transceiver and chip levels. Very-short-reach optical interconnects are coming for High Power Computing (HPC) and new disaggregated architectures where computing, memory, and storage components will be separated is a new trend.

The global optical transceiver industry remains very competitive, and competitors are racing to develop different techniques to overcome physical limits to achieve higher data rates. Two platforms are clearly emerging: InP and Silicon Photonics, which will coexist during the coming years.

Silicon photonics will be central in data center evolution in the short-term for 100 G (already well implemented in data centers) and then for 400 G and 800 G pluggables. It will also be an enabling technology for the disaggregation of data centers and a possible future CPO approach.

Although the Covid-19 pandemic and the Ukraine-Russia crisis have strongly impacted the semiconductor supply chain, the effect has been less in silicon photonics than in other semiconductor markets. Indeed, silicon photonics is a low-volume wafer and strategic technology, so allocated capacity does not affect the global fabs' capacity, which is generally much larger. So, silicon photonics continues to gain traction in the data center industry.

In the Silicon photonics 2022 report, we estimated that the value of the silicon photonics market was more than 20% of the optical transceivers market for datacom in 2021, which is still growing. It will be more than 30% in 2027. Silicon photonics is more used in short reach and is increasingly used for 500 m DR, but it is also more and more used with coherent technology entering datacom applications. There is also an increasing demand for 400ZR. It is interesting to see how telecom technologies (e.g. : coherent technology) are diffusing throughout the datacom industry today. And besides datacom,



other applications are promising in computing, interconnects in data centers, and sensing.

We forecast the silicon photonics market will be more than $1B (Si photonics units) in 2027, with 62 million devices. This will only require a modest number of wafers, estimated at about 70k 12'' eq. SOI wafers. Data center applications will have the largest share with $467M.

Optical interconnects will be $2M. Optical interconnects using silicon photonics will enable disaggregated data centers with more power available for high-performance computing (HPC) and data communications. This approach is pursued by AyarLabs, which is planning its first shipments in 2022. Applications will be HPC and data centers. Photonic computing, allowing for analog AI computations much faster than today's digital AI is developing and will soon hit the market.

The market ramp-up for CPO is still an open question, but it will co-exist with pluggable optics. So far, Google and Meta (Facebook) have been defining their pluggable optics requirements based on switch performance. With both optical engines and switches in the same package and in the hands of the same player, GAFAMs would be highly dependent on suppliers such as Broadcom. CPO will likely be used initially for niche applications (such as custom-built high-performing computers) before massive adoption in datacom in the longer term.

Consumer health will be worth $240M. Consumer health development continues, with Rockley announcing shipments of its Pro module (VitalSpexTM) for 2022/23. This would pave the way for future integration of silicon photonics-based biosensors in wearables from large OEMs like Apple or Huawei. However, this is a complex technology to implement, and it is difficult today to say whether this approach will be widely used. Other applications include sensors (immunoassays, gyroscopes, and lidars), 5G, optical processing, and CPO. Medical begins to hit the market, with Genalyte and many other startups using Si-integrated optics as a manufacturing platform. In the automotive domain, more and more manufacturers are integrating LiDAR into their products.

Player landscape

In recent years we saw strategic investments by both InP and Si photonics market leaders to strengthen their positions. The traditional InP-based players are strengthening their leading positions and are taking advantage of the platform for a new application – 3D sensing, and system vendors are betting on Silicon Photonics to enable scalable integration while eliminating the cost and complexity of the optical package.

In Si photonics, Intel is strengthening its market leadership with a 58% market share in units in 2021, followed by Cisco and other smaller companies (Marvell/Inphi, Sicoya, Acacia, and others) that, step by step, are gaining market share.

As integrated optics moves towards increased functionalities, the definition of Si photonics would broaden to incorporate other materials. Meanwhile, packaging and testing remain severe challenges for photonics

After decades of investments from Intel, the silicon photonics market is now the centerpiece of the evolution of the data center. Intel is now securing its access and manufacturing capabilities to leverage all its core competencies for the coming decades. From autonomous mobility to the data center and the future of cloud computing, Intel is now strengthening its position in the silicon photonics landscape with great recent results. From the decentralized on-the-edge central processing leader, Intel is transforming itself to be the centerpiece of the future of computing based on photonics and data centers.

The silicon photonics industrial landscape has remained very active. New potential applications of silicon photonics have resulted in the creation of various companies in the past three years. So, while some players are taking the opportunity to enter the optical transceiver market, others are looking for new applications: medical, sensors, interconnects, and computing. Co-packaged optics seem to require a large investment which is not achievable by any player yet, delaying its introduction.

Maximum shipments of optical transceivers will probably occur only after 2026. This will push players that cannot get into co-packaged optics to move to new applications in 5 - 10 years. We should, therefore, see a shift in applications in the coming years.

China continues to be very active in the development of silicon photonics, with many players involved. It has invested heavily in silicon photonics manufacturing platforms and InP. The China-US trade restrictions and ZTE's ban may prompt China to increase its support for high-speed optical chips, and domestic optical chip production is expected to accelerate further.

Many companies worldwide are offering foundry services. The acquisition of Tower by Intel could lead to the creation of a major silicon photonics player.

Technology landscape

Historically, integrated photonics has been developed on an SOI platform. The goal was to leverage wafer-scale manufacturing from the CMOS industry and use it for photonic chips. But SOI is expensive, and silicon is not the perfect material for all the different photonics functionalities.
Since the very start, the laser has been one of the greatest challenges for silicon photonics. The considerable development effort made by Intel for InP chiplet integration on SOI has been key to Intel's actual business success in silicon photonics.
More companies are now trying to duplicate this model to offer Si photonic wafers with integrated laser chips.

Today, as data rates increase, high-speed modulation using Mach-Zehnder on Si is becoming a bottleneck. There are numerous developments in new materials to overcome the current limitation (LNO thin films, InP, BTO, polymer, plasmons). For example, Arista has integrated thin film LNOs in modulators in an 800G transceiver prototype shown at OFC 2022.

This creates opportunities for companies focusing on materials for silicon photonics: Lumiphase and Polariton (created in Switzerland in 2019), Hyperlight and Liobate in China for thin film LNO, or Riber for BTO.

As integrated optics moves towards increased functionalities, the definition of Si photonics would broaden to incorporate other materials. Meanwhile, packaging and testing remain severe challenges for photonics. Current developments are being made to speed up testing time at the wafer level for Si photonic chips.

Conclusions

Silicon photonics as a platform is definitely a technology that will drive the datacom market in the coming years. It is also an enabling technology for co-packaged optics and possible new applications besides data centers. Silicon photonics is now a well-established technology and market, with more than 9 million silicon photonic transceivers shipped for data centers in 2021. In 2027,

it will be about 30% of the optical transceivers market in US$ value. Photonic processing could also be an important application of silicon photonics. Other applications include optical interconnects for disaggregated data centers. The industry is preparing for co-packaged optics (CPO), which is expected to arrive only after 2025.