PIC
PHOTONIC INTEGRATED CIRCUITS
CONNECTING THE PHOTONIC INTEGRATED CIRCUITS COMMUNITY

PIC platforms:
A question of choice
An interview with Julie Eng, CTO at Coherent

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INSIDE

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Toolbox for quantum computing

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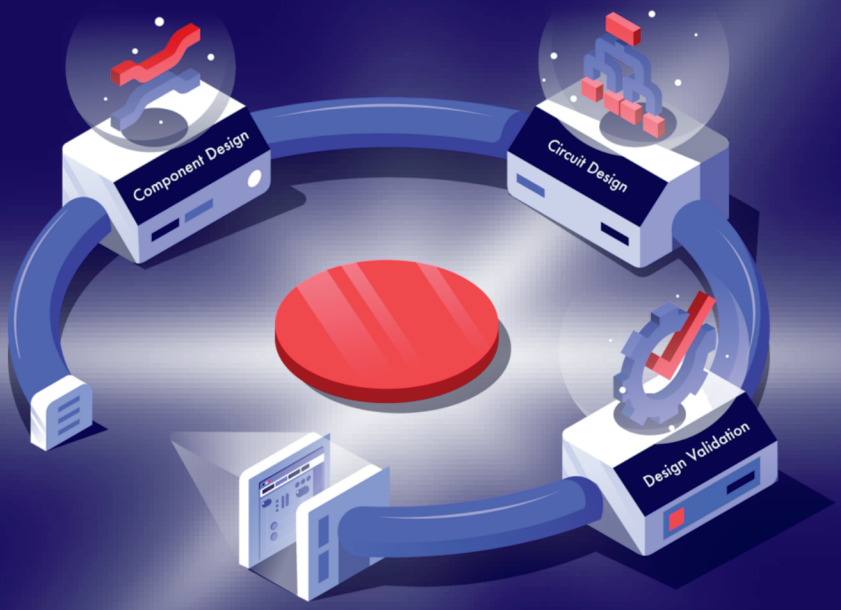
Luceda Photonics Design Platform



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VIEWPOINT

By Laura Hiscott, Editor

Photonics joins the quantum computing race

TECHNOLOGICAL progress often takes two broad forms: incremental improvements that push existing technologies to their limits, and revolutions that introduce novel approaches to accomplishing tasks, opening up a new range of possibilities. So-called quantum 2.0 promises to be the next big overhaul.

Indeed, it is already underway, and it turns out that PICs may be pivotal in achieving many of its goals. This was the topic of a special session on “PICs for Quantum” at the European Conference on Optical Communication (ECOC) in October (page 50).

The symposium covered a range of different quantum applications, whose timelines vary. Sensing and metrology, for instance, is generally considered to be nearer term than a useful quantum computer – the holy grail of this revolution.

There are multiple possible ways of building such a device. To date, the idea of using photonics has not been explored as extensively as other approaches. However, it now seems to be getting a lot of attention – and funding. In the weeks since ECOC, quantum computing company PASQAL announced a collaboration, named the PANDA consortium, to build the foundations of a photonic quantum computer; the R&D hub NY CREATES announced a partnership with PsiQuantum, a company also seeking to build a photonic quantum computer; and a startup called Photonic, which is using silicon photonics to tackle the challenge of scalable quantum computing, has received investment of $100 million.

Taking a deep dive into this topical theme, an article from imec on page 38 looks at the advantages that photonic qubits can offer over other types of qubits, and what challenges need to be solved to realise their potential.

Also in this issue, Yole Intelligence provides an overview (page 24) of the silicon photonics industry today, and how it is expected to evolve over the coming years, while on page 14 Julie Eng, CTO of Coherent, discusses InP and silicon photonics, and why there might be no definitive answer as to which one is better for making PICs.

Additionally, CEA-Leti reports developments in building an optical network-on-chip on a photonic interposer, Ansys describes their electronic-photonic design automation solution, and Luceda Photonics explains how their software can speed up PIC design cycles, accelerating the time to market.

It will be fascinating to watch how PICs progress in 2024.

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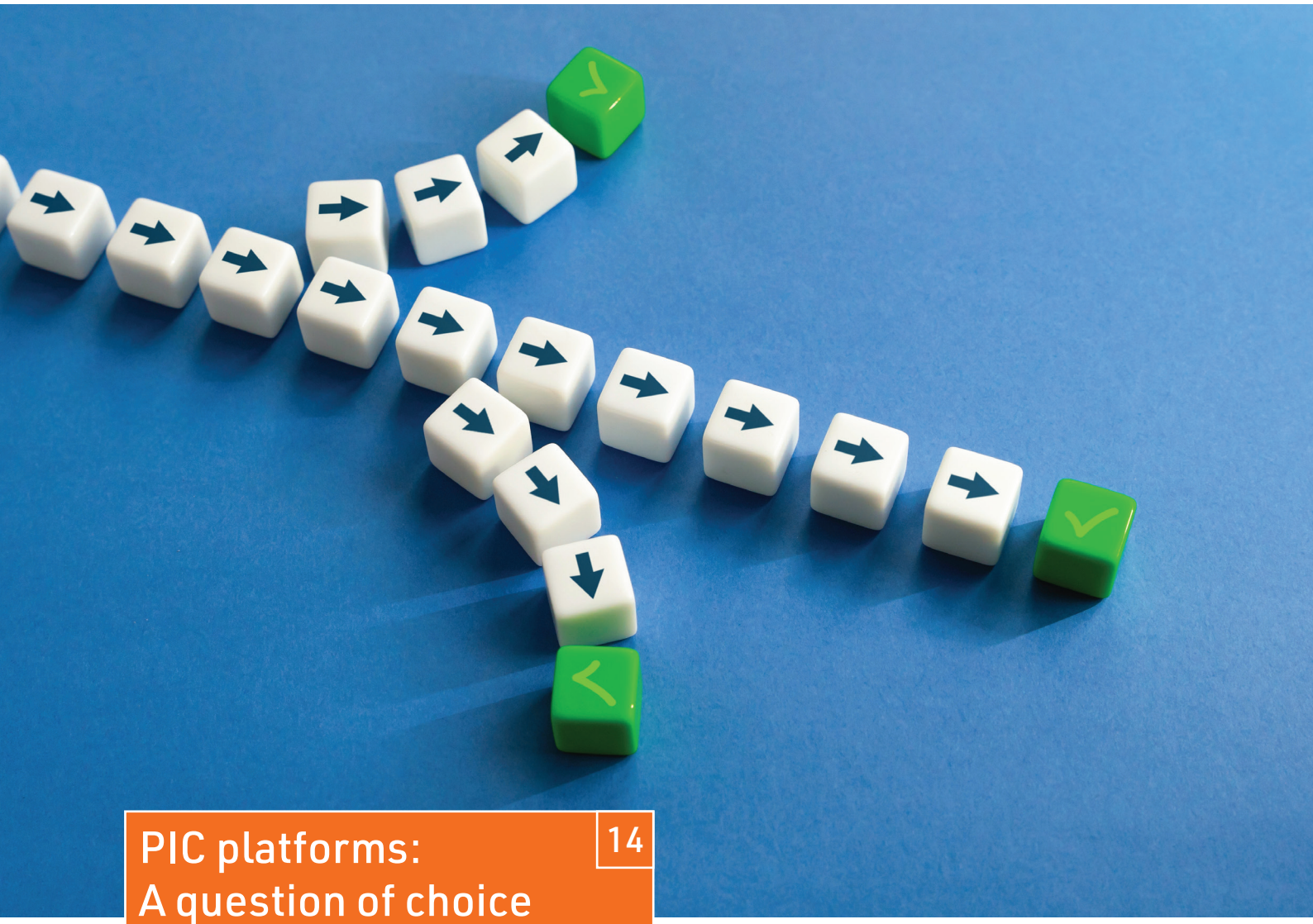

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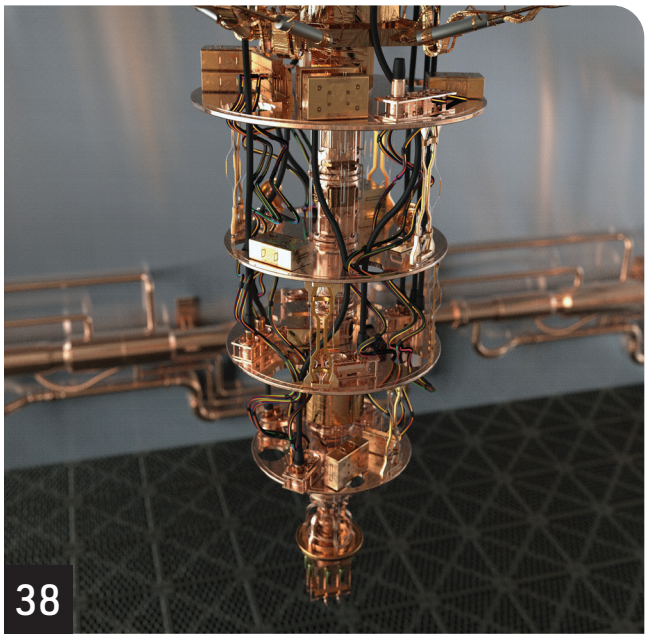

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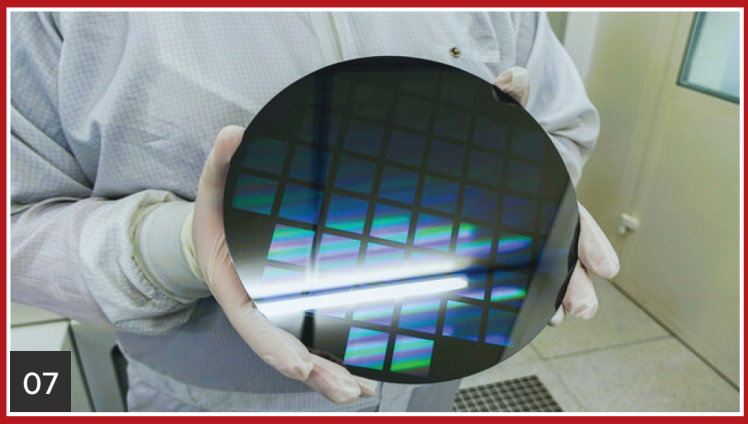

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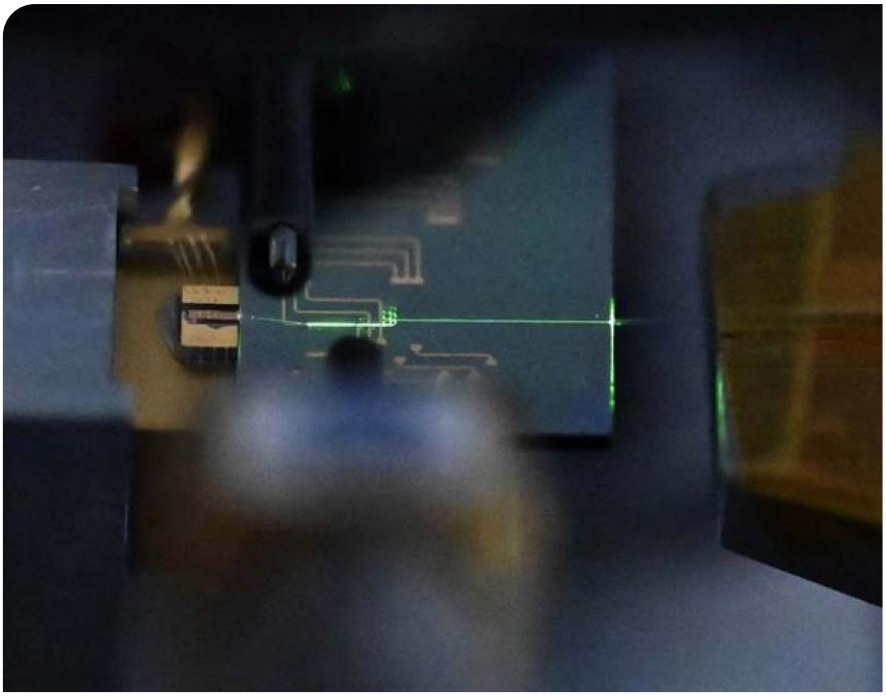
Researchers develop novel method for making chipscale mode-locked lasers

In a paper in the journal Science, researchers have described a new method for making a mode-locked laser on a photonic chip. The lasers are made using nanoscale components, allowing them to be integrated into light-based circuits similar to the electricity-based integrated circuits found in modern electronics

THE METHOD was developed by the lab of Alireza Marandi, an assistant professor of electrical engineering and applied physics at the California Institute of Technology (Caltech).

Mode-locked lasers are lasers that can emit extremely short pulses – on the order of one picosecond or shorter. Using lasers operating on such small timescales, researchers can study physical and chemical phenomena that occur extremely quickly – for example, the making or breaking of molecular bonds in a chemical reaction or the movement of electrons within materials. These ultrashort pulses are also extensively used for imaging applications because they can have extremely large peak intensities but low average power, so they avoid heating or even burning up samples such as biological tissues.



"We're not just interested in making mode-locked lasers more compact," says Marandi. "We are excited about making a well-performing mode-locked laser on a nanophotonic chip and combining it with other components. That's when we can build a complete ultrafast photonic system in an integrated circuit. This will bring the wealth of ultrafast science and technology, currently belonging to metre-scale experiments, to millimetre-scale chips."

Ultrafast lasers of this sort are so important to research, that this year's Nobel Prize in Physics was awarded to a trio of scientists for the development of lasers that produce attosecond pulses. Such lasers, however, are currently extremely expensive and bulky, says Marandi, adding that his research is exploring methods to achieve such timescales on chips that can be orders of magnitude cheaper and smaller, with the aim of developing affordable and deployable ultrafast photonic technologies.

"These attosecond experiments are done almost exclusively with ultrafast mode-locked lasers," he says. "And some of them can cost as much as $10 million, with a good chunk of that cost being the mode-locked laser. We are really excited to think about how we can replicate those experiments and functionalities in nanophotonics."

At the heart of the nanophotonic mode-locked laser developed by Marandi's lab is lithium niobate, a synthetic salt with unique optical and electrical properties that, in this case, allows the laser pulses to be controlled and shaped through the application of an external radio-frequency electrical signal. This approach is known as active mode-locking with intracavity phase modulation.

"About 50 years ago, researchers used intracavity phase modulation in tabletop experiments to make mode-locked lasers and decided that it was not a great fit compared to other techniques," says Qiushi Guo, the first author of the paper and a former postdoctoral scholar in Marandi's lab. "But we found it to be a great fit for our integrated platform. Beyond its compact size, our laser also exhibits a range of intriguing properties. For example, we can precisely tune the repetition frequency of the output pulses in a wide range. We can leverage this to develop chipscale stabilised frequency comb sources, which are vital for frequency metrology and precision sensing."

Silicon Austria Labs and EV Group strengthen collaboration

EV Group (EVG), a supplier of wafer bonding and lithography equipment, and Silicon Austria Labs (SAL), an Austrian research centre for electronic based systems (EBS), have strengthened their collaboration on heterogeneous integration

AS PART OF THIS cooperation, the organisations have announced that SAL has received and installed multiple EVG lithography and resist processing systems at its MicroFab R&D cleanroom facility in Villach, Austria. Together, the companies seek to accelerate the development and deployment of advanced optical technologies for heterogeneous integration applications, including wafer-level optics used for micro cameras and micromirrors, diffractive optics, and automotive optics used to enable autonomous driving and automotive lighting.

The newly installed EVG systems include the LITHOSCALE maskless exposure system, the EVG7300 automated SmartNIL nanoimprint and wafer-level optics system, as well as multiple complementary resist processing systems.

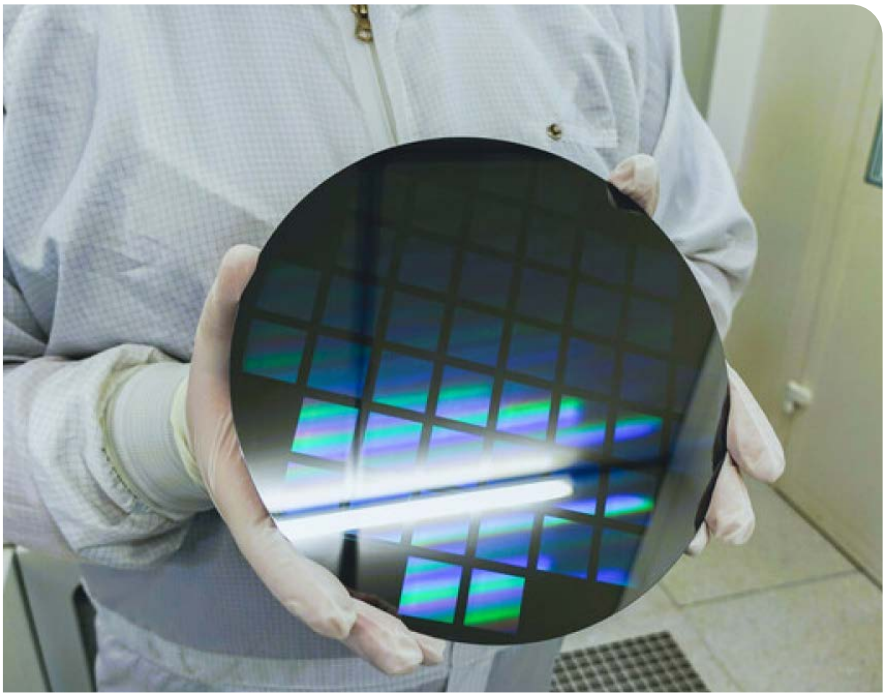
These systems join SAL's existing installed base of multiple EVG bonding, mask alignment and lithography systems, including the first installation of the next-generation 200 mm version of the EVG150 automated resist processing system. EVG says the latter provides significantly higher throughput, increased flexibility and smaller tool footprint compared to the previous-generation platform.

In addition, SAL has been working closely with the technology development and application engineering team at EVG's headquarters, including the NILPhotonics Competence Center, to leverage EVG's equipment and process knowhow and develop processes that are transferable and scalable to high-volume manufacturing.

Dr. Mohssen Moridi, head of the Microsystems Research Division at SAL, said: "We have recently been immersed in a range of cutting-edge R&D projects spanning meta-optics, integrated photonics, and MEMS, necessitating the use of advanced lithography and bonding tools. Through our valued partnership with EVG, we have gained access to tools of exceptional reliability and precision, paramount for successful R&D endeavours. Notably, the EVG7300 SmartNIL system has emerged as a pivotal tool, enabling the mass production of nanostructures for emerging photonics and MEMS devices. Its applications extend to diverse fields such as smart lighting systems, AR/VR, automotive optics, telecommunication, and quantum technology."

SAL was among the first customers to receive the new EVG7300 system, which EVG says is its most advanced solution combining multiple UV-based process capabilities, such as nanoimprint lithography (NIL), lens molding and lens stacking (UV bonding), in a single platform. The EVG7300 was developed with the intention of serving advanced R&D and production needs for a wide range of emerging applications involving micro- and nano-patterning as well as functional layer stacking.

Thomas Glinsner, corporate technology director at EV Group, added: "Silicon Austria Labs is a leading research centre for optical miniaturisation and heterogeneous integration, and is a strategic partner for EV Group. This latest shipment and installation of our advanced lithography and resist processing systems further strengthens our relationship and supports SAL's ability to develop future key technologies and apply our leading-edge solutions into real-world industrial applications."



Credit: Silicon Austria Labs

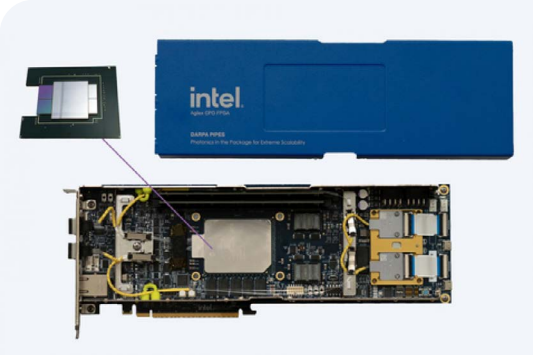
Ayar Labs showcases optically-enabled Intel FPGA

Ayar Labs, a company developing silicon photonics solutions for chip-to-chip connectivity, will showcased its in-package optical I/O solution integrated with Intel's Agilex field-programmable gate array (FPGA) technology

THE COMPANY says that the optical FPGA, which is packaged in a common PCIe card form factor, demonstrates 5x current industry bandwidth at 5x lower power and 20x lower latency. According to Ayar Labs, it therefore has the potential to transform the high performance computing (HPC) landscape for data-intensive workloads such as generative artificial intelligence (AI) and machine learning, and support novel disaggregated compute and memory architectures.

"We're on the cusp of a new era in high performance computing as optical I/O becomes a 'must have' building block for meeting the exponentially growing, data-intensive demands of emerging technologies like generative AI," said Charles Wuischpard, CEO of Ayar Labs. "Showcasing the integration of Ayar Labs' silicon photonics and Intel's cutting-edge FPGA technology at Supercomputing is a concrete demonstration that optical I/O has the maturity and manufacturability needed to meet these critical demands."

Ayar Labs describes the optical FPGA as consisting of two TeraPHY optical I/O chiplets that are each capable of 4 Tbps bi-directional bandwidth. These chiplets are connected to a 10 nm FPGA fabric die, the core fabric used in Intel's Agilex FPGAs. The optical communication is powered by two SuperNova light sources, supporting 64 optical channels of communication across eight fibres on each chiplet. The company says this configuration is capable of delivering 5x the bandwidth at a fraction of the power (<5 pJ/b) and latency (5 ns per chiplet + TOF) required by current industry solutions, all critical factors for the future of high performance compute fabrics and next-generation disaggregated architectures.



"At Intel, we pursue relentless innovation with our FPGA portfolio," said Venkat Yadavalli, VP and GM of Intel's Product Excellence Group. "With Ayar Labs' in-package optics coupled with our FPGA fabric die, we created I/O bandwidth over 4 Tbps — far greater than what is currently possible with electrical connections.

We're looking well beyond 400G Ethernet with this capability. Optical interfaces like these have the potential to unlock huge advancements in high performance computing, AI, data centres, sensing, communications, edge, and more. Imagine what you could do with an optical interface FPGA communicating at over 4 Tbps."

This development has utilised the emerging chiplet ecosystem, combining Ayar Labs' optical I/O chiplets developed on GlobalFoundries' Fotonix monolithic silicon photonics platform with Intel's FPGA and leading packaging process into a single package. Ayar Labs says that this co-packaged integration has delivered a step function in performance without changing the underlying compute silicon, illustrating the benefits of the chiplet ecosystem.

PI announces new alignment system for silicon photonics

PHYSIK INSTRUMENTE (PI), a precision motion control technology company, has announced it has expanded its family of photonics alignment automation systems, with a new air bearing-based multi-axis assembly and an EtherCat-based high-performance motion controller with embedded alignment algorithms. The company says the new system offers a unique combination of direct-drive maintenance-free air bearing alignment stages with sophisticated first light search and alignment routines, and could save a significant amount of time – a critical factor in silicon photonics alignment automation.

The F-143 alignment system is based on three A-143 air bearing stages in an XYZ configuration. According to PI, each axis provides a travel range of 25 mm, with a maximum velocity of 250 mm/s, and acceleration up to 10 m/s^2, while preloaded air bearings guarantee flatness and straightness of 0.25 µm and 0.05 µm, respectively. The company also says that the vertical axis stage is equipped with an adjustable counterbalance and brake mechanism to offset the force of gravity on the motor and prevent potential collisions with a SiPh wafer in the event of a power failure.

PI adds that a special, EtherCat-based motion controller with embedded photonics alignment algorithms and user-friendly software allows the system to perform alignments up to 100 times faster than conventional optical alignment engines. Finally, the use of friction-free, wear-free, and maintenance-free components along with the absence of lubricants seeks to make the air bearing automated alignment system ideally suited for silicon photonics wafer probing and other clean-room applications.

Photonic quantum computing company raises $100 million investment

Photonic, a quantum computing company, has announced that it has raised an investment round of $100 million

THE COMPANY seeks to build one of the world's first scalable, fault-tolerant, and unified quantum computing and networking platforms, based on photonically linked silicon spin qubits. The funds were raised from organisations including British Columbia Investment Management Corporation (BCI), Microsoft Corporation, the UK government's National Security Strategic Investment Fund (NSSIF), Inovia Capital, and Amadeus Capital Partners. This brings the company's total funding raised to date to $140 million.

Photonic aims to make fault-tolerant quantum technologies a reality with its silicon spin-photon interface, leveraging the memory and computing capabilities of spins and the connectivity of photonics to build a scalable, fault-tolerant, and networked quantum computer. The company has over 120 employees with a head office in Canada and has recently opened offices in the UK and the US.

"Photonic's game-changing approach to deliver on the decades-old promises of quantum computing continues to be fuelled by our committed investors and best-in-class employees," said Paul Terry, CEO of Photonic. "The support of such knowledgeable investors who believe in our work is a testament to our team, our technology, and the direction we're headed in."

Hermann Hauser, co-founder and venture partner at Amadeus Capital Partners, added: "Photonic is solving one of the central challenges for scalable quantum computing. By linking qubits with photons on a silicon-based architecture, the power of quantum processing can be unleashed across a distributed computing network with confidence that error correction is able to keep pace. This is an innovation with awesome potential."

Gordon J. Fyfe, CEO of BCI, said: "Since our initial investment in Photonic, the company has reached several major technical milestones related to developing secure quantum solutions, while establishing key commercial partnerships. As one of Photonic's largest shareholders, BCI is excited to partner with its management team with the goal of developing one of the first fault-tolerant quantum computers in the world."

NTT and Chunghwa Telecom cooperate on all-photonics network

Communications companies NTT Corporation and Chunghwa Telecom have signed an agreement to advance international network connectivity through the Innovative Optical and Wireless Network (IOWN), proposed by NTT

IN THE FUTURE, with IOWN's communication technology centred on the All-Photonics Network, the companies aim to realise international network connectivity between Japan and Taiwan and to collaborate in IOWN-related businesses and security.

NTT has proposed the IOWN concept, which is a network and information processing infrastructure that the company says can provide high-speed, high-capacity communications, and substantial computing resources by utilising innovative photonics technologies. NTT has established the Innovative Optical and Wireless Network (IOWN) Global Forum, in which Chunghwa Telecom participates, to promote the realisation of new communication infrastructure.

According to NTT's website, a major component of IOWN is an All-Photonics Network, which is intended to

reduce power consumption, improve transmission capacity, and reduce transmission delays. NTT says that photonic circuits are part of the key to achieving this network, with silicon photonics being one field of research that the company is engaged in.

Akira Shimada, President & CEO of NTT Corporation, said: "With outstanding technology and extensive global business experience, we expect that NTT and Chunghwa Telecom working together on IOWN's international communications will strongly accelerate IOWN's technology development and service deployment. Based on the achievements of NTT and Chunghwa Telecom, we hope to expand IOWN in various other countries."

"As Taiwan's leading telecommunications company, Chunghwa Telecom is pleased to sign the IOWN cooperation memorandum with NTT, Japan's leading telecommunications company," said Shui-Yi Kuo, Chairman & CEO of Chunghwa Telecom. "Chunghwa Telecom agrees with the vision of IOWN's innovative technologies, and will continue to uphold the brand spirit of "Always Ahead" and implement the corporate sustainability goals of ESG energy conservation, actively invest in innovative research and development, and bring people with more diversified and convenient network and services."

Jabil takes over Intel silicon photonics line

JABIL, a manufacturing solutions provider, has announced it will take over the manufacture and sale of Intel's current silicon photonics-based pluggable optical transceiver ("module") product lines and the development of future generations of such modules.

"This deal better positions Jabil to cater to the needs of our valued customers in the data centre industry, including hyperscale, next-wave clouds, and AI cloud data centres. These complex environments present unique challenges, and we are committed to tackling them head-on and delivering innovative solutions to support the evolving demands of the data centre ecosystem," stated Matt Crowley, senior vice president of Cloud and Enterprise Infrastructure at Jabil. "This deal enables Jabil to expand its presence in the data centre value chain."

Through its photonics business unit, Jabil seeks to empower organisations to reduce the complexities of developing and deploying enhanced optical networking solutions by offering complete photonics capabilities, including component design, system assembly, and streamlined supply chain management.

"We are pleased to reach this agreement with a world-class supplier like Jabil," said Safroadu Yeboah-Amankwah, senior vice president and chief strategy officer of Intel. "We look forward to working closely with Jabil, our customers, and our suppliers to enable a seamless transition as Intel shifts its focus to silicon photonics components for existing markets and emerging applications."

Crowley concluded: "Our Design-to-Dust capabilities continue to resonate with customers and we are investing in the areas of data centre infrastructure services, liquid cooling, and silicon photonics to help our customers solve their challenges. Jabil is extremely well positioned to support customers as they incorporate innovative technologies into their data centres to navigate the increasing requirements around power and cooling being driven by artificial intelligence."

Lumentum to acquire Cloud Light, expanding provision for data centres

Optics and photonics company Lumentum has announced it will acquire Cloud Light Technology, a manufacturer of optical modules for automotive sensors and data centre interconnects for approximately $750 million

THE TRANSACTION has been unanimously approved by the Boards of Directors of both companies and by Cloud Light's shareholders.

Lumentum expects its acquisition of Cloud Light to accelerate its push into the fastest growing segments of the multibillion-dollar opportunity for optical modules used in cloud computing data centre infrastructure. The company said that Cloud Light has a demonstrated track record of developing and manufacturing the highest-speed connectivity solutions at the leading edge of new and rapidly growing technology transitions. Nearly all of Cloud Light's more than $200 million revenue in the last 12 months was derived from 400G or higher-speed transceiver sales. In the most recent quarter, over half of Cloud Light's optical transceiver revenue was derived from 800G modules. With this acquisition, Lumentum is positioning itself to serve the growing needs of cloud and networking customers, particularly those focused on optimising their data centre infrastructure for the demands of AI/ML. The company is aiming to deliver immediate customer value with a more comprehensive product and technology portfolio, enabling customers to more effectively manage the escalating compute and interconnect requirements of AI workloads. Lumentum added that the combination also brings best-in-class design and assembly, test, and packaging capabilities together with its global scale and customer reach.

"With Cloud Light, we are making a strategic investment to significantly expand our opportunities in the cloud data centre and networking infrastructure space," said Alan Lowe, Lumentum president and CEO. "Cloud Light provides us with the highest-speed transceiver solutions at scale and complements our advanced component capabilities. This results in a broad product and technology portfolio that addresses a wide range of cloud operator needs."

Dr. Dennis Tong, Cloud Light founder and CEO, said that the announcement "is a pivotal milestone in the history of Cloud Light, and a testament to the hard work and dedication of our employees. We founded the company with a vision that our deep expertise in high-volume precision manufacturing would result in a superior value proposition for cloud data centre customers. Having worked closely with the technology teams within leading cloud operators, we believe we can build upon our success to date and further accelerate cloud data centre growth by combining Lumentum's advanced photonic integration and transmission technologies with our highly automated packaging and manufacturing processes. We look forward to joining the Lumentum team and beginning an exciting new chapter."

New consortium seeks to advance photonic quantum computing

QUANTUM computing company PASQAL has announced a collaboration to build the essential foundations for a photonic quantum computer powered by neutral atom technology. The collaboration, dubbed the PANDA consortium, working towards this goal comprises PASQAL; Sorbonne Université, France; Pixel Photonics (PIX), Germany; the Institute of Photonic Sciences (ICFO), Spain; and Institut d'Optique Théorique et Appliquée (IOTA), France. The project will be funded by a grant from the European Innovation Council Pathfinder Challenges programme of 2023.

Coordinated by the Laboratoire Kastler Brossel at Sorbonne Université, the collaboration seeks to use the power of neutral atoms to develop the foundations of a quantum processor that will use light as the carrier of quantum information, using an approach known as continuous variable quantum computing. This relies on the wave-like nature of light rather than discrete quantum bits associated with its particle-like behaviour.

Light has the intrinsic ability to carry large amounts of information over long distances with low loss rates, operating at room temperature. These properties make light a great candidate for scalable quantum computers. However, photons, the particles of light, do not interact with each other naturally, a feature that represents a big challenge to building quantum processing units, since interactions are required to carry out operations and create quantum circuits.

The PANDA consortium aims to build the foundations of a photonic quantum computer through interactions between quanta of light – or photons – with a specially ordered assembly of neutral atoms. PASQAL architecture uses highly focused lasers called optical tweezers to manipulate neutral atoms and arrange them in 2D and 3D arrays of any configuration.

"As leaders in neutral atoms quantum processing, we are excited to be part of this consortium," said Loïc Henriet, CTO of PASQAL. "Innovations to our technology will help push forward quantum computing, together with experts in photonics. We are convinced that our atoms, provided by nature, will be optimal in this undertaking."

Silicon photonics research centre established at Indian Institute of Technology Madras

A new Silicon Photonics Research Centre of Excellence has been launched at the Indian Institute of Technology Madras (IIT Madras) by the Ministry of Electronics and Information Technology (MeitY) Secretary, Shri S. Krishnan

WITHIN THE NEXT FIVE YEARS, the Silicon Photonics Centre of Excellence, Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) is targeting achieving self-sufficiency and driving product commercialisation through startups.

IIT Madras said the centre will provide essential training to bolster the future ecosystem of PIC manufacturing in India, and is actively developing indigenous PIC design rules and hardware infrastructure for precision packaging for system-level applications. Through these activities, the CPPICS is intended to play a major role in fulfilling the objectives of the India Semiconductor Mission of the Government of India.

The immediate focus of the CPPICS is to provide better solutions for microwave and quantum photonics applications such as advanced photonic processors to be used in high-performance RF transceivers, scalable linear optical quantum computing processors for next-generation qubit computation, and chip-level quantum key generation and distribution circuits, among others. The centre has a long-term mission of catering for R&D in programmable PICs and systems using CMOS-compatible silicon photonics technology for solving various levels of complex problems.

During the inauguration on 20 October, Shri S. Krishnan said: “Today, we are inaugurating yet another of MeiTY and Government of India’s initiatives in IIT Madras. Many of MeitY’s efforts with IIT Madras have been huge successes and I am sure this will also succeed. We have caught up (with rest of the world) and now we should leapfrog others.... This Centre of Excellence complements many things MeitY is trying to do.”

Shri S. Krishnan added: “The fact that there is an insistence and there is a rigour and discipline of bringing in industry participation is very significant. I would like to thank the industry partners, specifically Intel and Si2 Microsystems. This partnership will take us very far, both in terms of developing capacity and ensuring that all of us benefit from it. When we work together, there are larger benefits.”

Addressing students specifically, Shri S. Krishnan said, “What the Government encourages you to do is to be bolder and more courageous than the previous generation in taking up challenges. Societally and economically, the country has changed to enable you to not go for the safest choice and to make bold choices and go for entrepreneurial activities.”

Speaking about this Centre, Prof. V. Kamakoti, Director, IIT Madras, said, “As our country is moving towards building our own capability in semiconductor electronics, it is very heartening to see our Institute establish a Centre of Excellence in Silicon Photonics, which is an outcome of extensive R&D pursued over nearly two decades. The substantial seed funding for establishing this state-of-the-art Silicon Photonics CPPICS by MeitY has helped in consolidation of indigenously-developed silicon photonics technology at IIT Madras. I am confident that the centre is going to impact significantly, both in the domestic as well as global silicon photonics R&D market in the upcoming years.”

The centre has a long-term mission of catering for R&D in programmable PICs and systems using CMOS-compatible silicon photonics technology for solving various levels of complex problems

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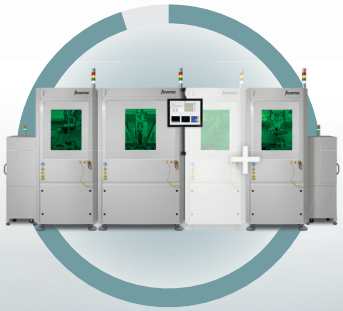

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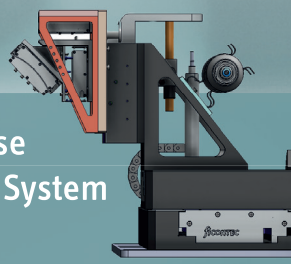

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PIC platforms: A question of choice

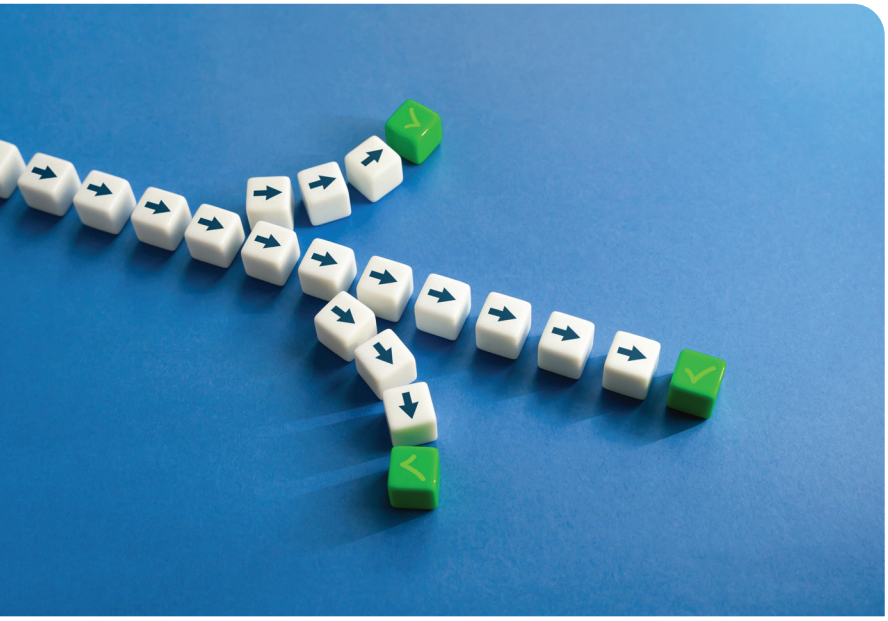
There are several different materials being used to make photonic integrated circuits, with two of the most common being silicon and indium phosphide. For companies designing PICs, therefore, a major question is: which material is better?

AN INTERVIEW WITH JULIE ENG, CHIEF TECHNOLOGY OFFICER AT COHERENT.

LH: ***Indium phosphide (InP) PICs have historically had concerns over yield. Is that still an issue?***

JE: In general, I would say that the III-V industry hasn't historically had the same level of investment in tools, wafer volume, and yield improvement as the silicon (Si) industry. However, the yields in III-V devices have definitely improved over time as the optics industry has matured. We've increased our wafer sizes and higher volumes have been shipped. We at Coherent recently had a public announcement that we've shipped over 200 billion gallium arsenide (GaAs) VCSELs. That's GaAs and not InP, but the reason I point to it is that it's III-V lasers and it's a public data point.

The total volume of InP is lower than GaAs, but still very significant and much higher than 10 years ago. So that gives us a lot of data and also a lot of motivation to improve yields. Overall, the yield of InP PICs has definitely improved over time in a way that can make those solutions viable in transceivers – that's why you see them in transceivers today.



LH: ***Is there a sweet spot for the level of integration of InP PICs? That is, if InP PICs are large and contain many components, is there a price to pay for their complexity?***

JE: To talk about the sweet spot for InP, it's important to look at the trade-off between InP and silicon photonics (SiPh). The main advantages of InP are, first, that the laser and the modulator are integrated; they're in the same die, so the coupling loss between them can be very low. Second, due to material properties, modulators in InP are more efficient than modulators in silicon. In InP PICs you can also integrate, if you choose to, semiconductor optical amplifiers (SOAs). So InP is generally a great fit for the applications that need high optical power – because you can have an integrated SOA – and also the most complex applications that really care about performance.

SiPh, on the other hand, has the advantage that the passive optical devices can generally be made smaller in size than in InP, again due to physical differences in the material properties. Additionally, silicon foundries are on larger wafer sizes, and generally have very high-yielding processes, and mature metrology and test. All of this should result in a lower die cost for some applications.

What I see as the sweet spot for InP PICs is primarily where key electro-optic performance parameters such as optical power and modulator efficiency are paramount and valued. In an application that might have a lot of passive optics in it, if the performance

of the SiPh die is good enough, then the die size might be smaller and the cost lower if you use a SiPh PIC. It's a case of looking at the detailed requirements of the application and choosing the best-performance, lowest-cost solution for the application.

LH: ***For silicon PICs, can the level of integration be higher?***

JE: The answer depends on how you define integration, and also to some extent on the application. Specifically, as I mentioned, passive optical devices can generally be smaller in silicon. If you're going down the path of having an InP PIC, you can have a laser, a modulator, and an optical amplifier integrated in the PIC. But, because the passive optics will be larger in an InP PIC, you might choose to do what we call free-space optics, where the passive optics are not part of the PIC, but are separate elements. If you did that, then you might say the InP solution is less integrated than the SiPh solution.

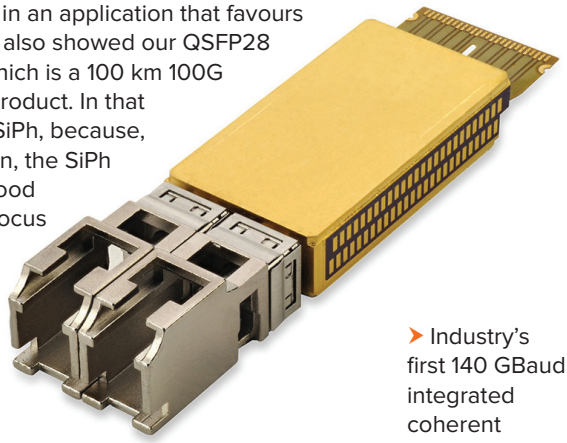
But on the other hand, silicon doesn't lase, so you always need an InP laser when you make a SiPh solution. In that case, you might say the SiPh PIC is less integrated. Another example is if you need amplification, the amplifier can be integrated in the InP solution. But in the silicon solution, in most cases, you'd have a separate amplifier, such as a micro EDFA (erbium-doped fibre amplifier). In this case, SiPh PIC would be a less integrated solution than the InP PIC.

So, again, it's this situation where you have to ask: what is the application? How am I defining the word integration? I think there are cases where a SiPh PIC will be more integrated and there are cases where you would say the InP PIC is more integrated.

LH: ***Some will argue for InP PICs and others for silicon, but you see a role for both. Why?***

JE: A lot of people want to make it an either/or. My view is it's an "and." I ran transceiver engineering for Finisar for almost two decades. We needed to innovate new technologies and design, qualify, and deliver optical transceiver products year after year, as data rates increased, as the customers and the specs and the applications changed over time. From that experience, I know that there's no one-size-fits-all technology for optics. To me, InP and SiPh are two tools in the toolbox. One thing that people sometimes forget is that every time someone says SiPh, there's always an InP laser in there anyway, so InP and SiPh are always together.

To be more specific, a great example is our own coherent optics transceiver product line. Within that one product line, we use both InP PICs and SiPh PICs, but we use them for different products. For instance, at ECOC 2023 we showed our 140GBaud IC-TROSA. For that, we use an InP PIC, because the transceiver is in an application that favours performance. We also showed our QSFP28 ZR transceiver, which is a 100 km 100G coherent optics product. In that product, we use SiPh, because, for that application, the SiPh performance is good enough and the focus is really on cost and size, so the integration of the passives really matters.



Industry's first 140 GBaud integrated coherent transmitter-receiver optical subassembly (IC-TROSA) from Coherent.

Of course, we make our decisions based on the tools in our toolbox. Every transceiver manufacturer might have different decision-making criteria, based on what they have in-house and what they don't. For a vendor who has an InP capability, but not a SiPh design team, it might make more sense to continue to use InP in products that I might choose to use SiPh in, just because they might not want to invest in the R&D to bring up a SiPh design capability. On the flip side, a transceiver manufacturer who has SiPh design capability but doesn't have in-house InP might be more inclined to choose SiPh for things I might choose InP for.

Our strategy at Coherent is to have all the capabilities, so we can objectively choose the right technology for a product on a product-by-product basis, because we're the number one maker of optical transceivers in the world, so we're going to make all the different types of transceivers.

LH: ***For those wishing to produce InP and silicon PICs, production can be done in partnership with foundries and via in-house manufacture. For both technologies, are there benefits to vertical integration? And does volume have an impact on the appropriate approach?***

JE: The silicon industry is primarily a foundry-based industry, and the majority of integrated circuit (IC) companies don't own fabs anymore. A few big ones still own fabs, but many huge IC companies are fabless, and rely on foundries for both the chip manufacturing and packaging. The reason is, of course, the fabs are very expensive to invest in, so it doesn't make sense anymore for most IC companies to own their own fabs. The volume is therefore aggregated in a few big foundries. SiPh follows that model; it's relatively straightforward to get access to very high quality and reasonably-priced SiPh PICs from tier-one silicon foundries, so, from my perspective, it doesn't make sense for us to own an in-house SiPh factory. A lot of people doing SiPh are using a foundry model, although a few people have something very specialised and they do that portion in house. For us, we're not a silicon foundry and we don't have any other silicon manufacturing, so it makes sense to utilise the foundries.

Coherent 100G QSFP28 0 dBm DCO transceiver for edge and aggregation networks.

On the InP side, there are InP foundries, but in general they're not as mature as the InP manufacturing capability that's inside the optical companies today. And the InP foundries are also generally not as mature as the silicon foundries in terms of maturity of PDKs (process design kits). This can be a challenge, particularly when you're considering making a device like a PIC, which is much more complex than a standalone laser. For us, since we already own multiple InP fabs, it makes sense for us to do that in house. And I think most of the people doing InP PICs are doing them in house.

In either of those situations, volume definitely matters. That's why a lot of people don't have in-house silicon fabs anymore – because the volume is so aggregated at a few fabs that, if you own your own, you're operating at a disadvantage. The same is true in InP; a fab that is not running fully utilised is never good. That adds to the cost of the die, because the fixed cost has to be amortised over the volume. This could change the economic part of the decision of InP versus SiPh for some vendors.

LH: ***SiPh requires the addition of a light source. How do you view the various approaches for incorporating a laser onto the silicon chip?***

Coherent 200G distributed feedback laser and Mach-Zehnder modulator won Most Innovative Photonics Component Award at ECOC 2023.

JE: There are two main approaches. The first is a totally hybrid approach, in which you have an InP laser that's a physically separate die from the SiPh die. The advantage of this is it's the most straightforward option. You don't have to have special processes in your SiPh foundry; you can either fabricate or buy the InP die and then separately either design a SiPh device yourself and buy it from a foundry, or buy it from one of the SiPh die vendors. Then, you integrate them together in the package. A positive side of that is, if you have a yield hit on your InP laser, it doesn't affect the PIC yield, and vice versa.

But the disadvantage is that the light from the InP device has to be coupled from the laser into the SiPh waveguide, for example through edge coupling or grating coupling, and there's loss associated with that, which impacts performance. There's also a financial cost to do that, as you have to physically align things. Several SiPh companies and foundries have now started to integrate III-V materials, specifically InP, into their SiPh process to provide the light generation. Depending on the process, there are different ways of integrating it. Some people use the III-V material only for the light generation, while others use III-V materials for modulators, or potentially even integrating amplifiers or photodiodes into the SiPh process.

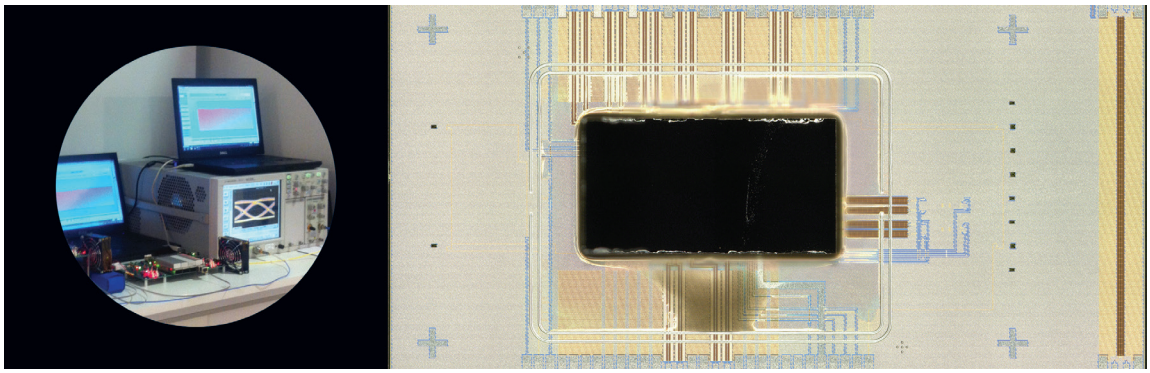
This approach holds the promise of using InP for what it's good at, and using silicon for what it's good at, but doing it in a single-die solution. That has a real allure to it; it eliminates the coupling loss and the cost of coupling. But the major downside is that this technique still somewhat new, and it's obviously more complex than SiPh without integrated III-V materials, so presumably it's higher cost. Also, only a few of the fabs offer this capability, so, because there's less competition, that could lead to higher pricing. And, the yield is going to be aggregated, so anytime a laser doesn't yield, you're going to throw away a SiPh PIC and vice versa, so there's an economic calculation there. The question is, in the end, is that approach less expensive than just having an InP CW laser separate from your SiPh PIC? The economics of that may be different for different companies and applications.

Finally, there are some research groups working to grow III-V materials directly on silicon, but I see that as much further out. The two primary approaches right now are either fully discrete or III-V integrated into the SiPh process, and you see different companies making different decisions.

LH: ***At Coherent, how have you evolved your PIC technologies?***

JE: We've had InP fabs for more than two decades. We started with Fabry-Perot lasers, which are simple, small lasers. Then went to directly modulated lasers, which are more complex, and photodetectors, and later we developed tunable lasers. As the data rates went up, we and the rest of the industry needed to start implementing coherent optics to get the fibre reaches needed in telecom. So we needed really complex InP devices, such as tunable lasers integrated with dual Mach-Zehnder modulators, with semiconductor optical amplifiers and photodiode arrays.

We started by showing each element could work on its own, because you need a device that works with good yield before you can integrate it with other devices. We wanted to build a platform that could support mixing and matching of the various components for different products. So we



First demonstration of a 50G NRZ end-to-end link with silicon photonics demonstrated by Coherent (former Finisar) at ECOC 2014.

developed that capability over time with a lot of effort, significant expertise in the personnel, and a lot of investment, and I'm super proud of our team and what they've achieved. One of our integrated InP PIC products, the 200G distributed-feedback laser with Mach-Zehnder modulator got the Innovation Award at ECOC 2023.

We started to invest in SiPh design capability as far back as 2010. From the beginning, we had an outsourced fab strategy for SiPh because we are not a silicon manufacturing company. But of course, we had GaAs VCSELs and InP directly modulated lasers and photodetectors in house. For each product, we would compare SiPh to the other technologies before designing them. For a long time, we didn't have SiPh in any of our production products, because the performance and economics of GaAs and InP worked for us. But we continued SiPh as a technology development effort and we had our first public demo at ECOC 2014. It was the industry's first 50G NRZ end-to-end link based on SiPh (this was before the industry transitioned to 50G PAM-4).

Over time, as the transceivers started to need multiple channels, as parallel single-mode fibre applications emerged, and as we started working on the coherent optical transceivers, for some products, the economic calculation started to favour SiPh. So we are shipping products with SiPh in production. On that side we're fabless, and we rely on the tier-one foundries for the SiPh manufacturing. Then we bring it in house for the assembly and integration into the module. So we have design capabilities in both areas, which gives us the freedom to choose the best technology for each application.

LH: ***How do you view the future of silicon and InP PICs?***

JE: As we've discussed already, I think InP and SiPh PICs will continue to coexist, with each technology being used for the applications for which it's best. As the industry transitions to higher and higher data-rate devices, with more channels and more complexity within each transceiver, I think the percentage of total transceivers using PICs, whether InP or SiPh, compared to discrete devices, will increase. Increasing data rate is getting tougher; 200G per lane is already really hard, and jumping to 400G per lane in optical is going to be that much harder. So what you see is people deploying many lanes. That is complicated, and PICs lend themselves to this, whether they're InP, or SiPh. A higher level of integration is needed for the functionality to just physically fit inside the box. I do think that the integration of III-V into the silicon foundries will continue to mature over time. And I would keep my eye on the researchers who are working to grow III-V directly on silicon. Today it's a research effort, but 20 years ago having InP in a SiPh fab was a research effort. So these things get better and better over time until at some point they can be commercialised.

Bringing photonic technology to 3D-stacked computing systems

Creating the low-latency “POPSTAR” optical network-on-chip through hetereogeneous integration on a photonic interposer

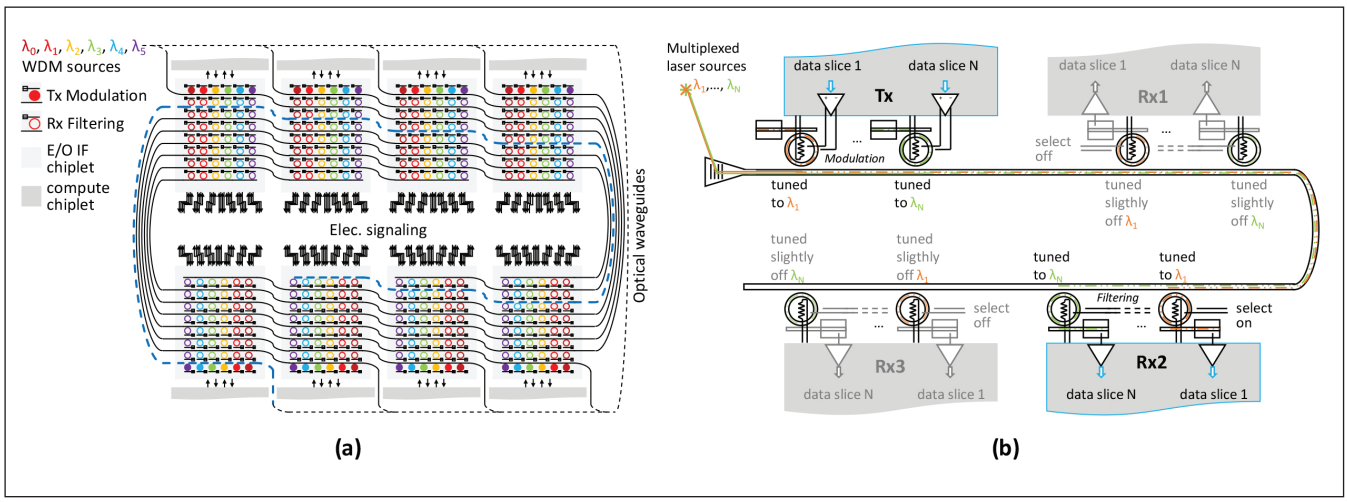
BY STÉPHANE MALHOUITRE, LEOPOLD VIROT, ANDRÉ MYKO, AND JEAN CHARBONNIER FROM UNIVERSITÉ GRENOBLE ALPES AND CEA-LETI, AND YVAIN THONNART FROM UNIVERSITÉ GRENOBLE ALPES AND CEA-LIST

OVER THE PAST FEW DECADES, optical devices have proven useful for high-throughput communication at multiple scales, from the Internet backbone to metre-range communication between compute nodes in datacentres and supercomputers. With ever-increasing baud rates, optical transceivers have demonstrated power efficiency at shorter scales down to board-level communication. Conversely, computing architectures stopped the gigahertz race more than 10 years ago in favour of greater emphasis on parallel execution. This shift requires increased communication between computing cores and memories, meaning that processor architectures have grown and core count has increased – in some cases up to the point where chip-level communication costs prohibit scaling.

Now, heterogeneity has become the buzzword for efficient computing architectures. Heterogeneous cores can be used for heterogeneous applications: following a trend from embedded systems-on-chip, it has become more efficient to have dedicated accelerators with specialised processing capabilities to perform distinct tasks, driving a shift from CPUs (central processing unit) to GPUs (graphical), NPUs (neural), and TPUs (tensor). Since packing all those accelerators and memories onto a single die rapidly becomes unfeasible, heterogeneous packaging solutions are needed to integrate multiple silicon dies implementing accelerators in modules stacked on an interposer. This approach benefits from 3D assembly technology involving multiple chiplets. It also allows the most appropriate technology node to be used for each chiplet to match the required performance, thus providing the highest energy efficiency.

The potential of interposer-based optical communication

To meet system performance requirements, communication between heterogeneous dies must sustain high-throughput at a low latency, while remaining within a low power budget. From this perspective, given its capacities at larger scales, optical communication is a promising option for



➤ Figure 1. (a) Optical network on silicon photonic interposer and (b) single-writer multiple-reader silicon photonic link.

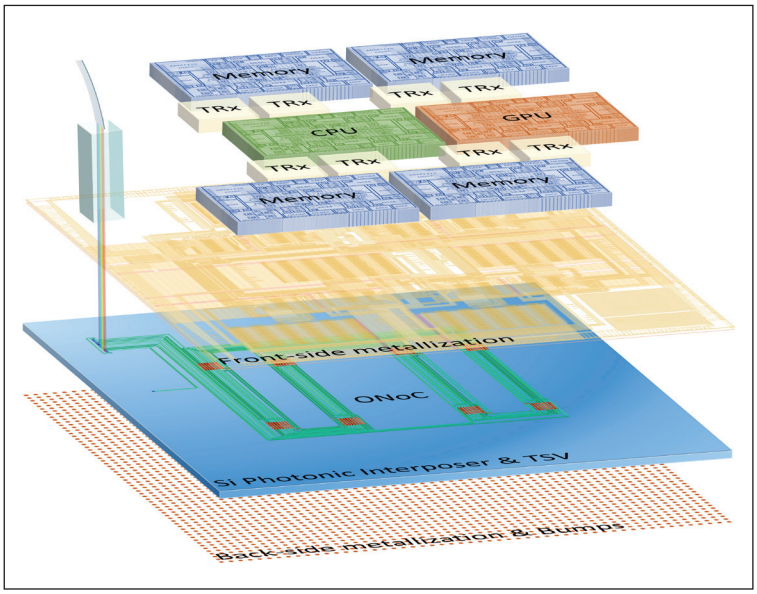
ultra-short-reach die-to-die links. However, system optimisation goes beyond high-speed transceivers and point-to-point links. Thus, latency and power in computing systems are not only linked to distance, but also to routing and queuing costs.

Consequently, if only nearest-neighbour communication is implemented, heterogeneous architectures will encounter huge queuing latencies at every die interface for longer communication paths. To overcome this, we suggest the use of stacked systems on a large photonic interposer. This interposer serves as a base die for all the heterogeneous chiplets and allows implementation of an overall optical communication architecture between chiplets. Indeed, optical routing on the interposer removes the need for additional queuing and electro-optical conversion at each crossing in the network.

The POPSTAR computing architecture on a photonic interposer

This architectural vision of an optical network on an interposer presents several challenges, from system requirements to implementation constraints:

- First, this interposer-borne optical network must be scalable according to the system requirements, with an appropriate interface between the chiplets and the network.
- Routing in the system should be decentralised to avoid the need for long-distance communication to a central scheduler for every data transfer.
- Unlike longer-distance transceivers, the associated interface must have a low footprint to create as little overhead as possible in the chiplets.
- Scalability and network topology must be considered in view of the optical power budget from the laser sources to the final opto-electrical conversion.
- As computing systems may have very unbalanced and variable activity ratios, power dissipation is not homogeneous, and temperatures can fluctuate by several tens of degrees during operation. These effects must not degrade communication within the optical network.
- Finally, the co-integration of multiple devices and process options must be possible without degrading individual device performances.

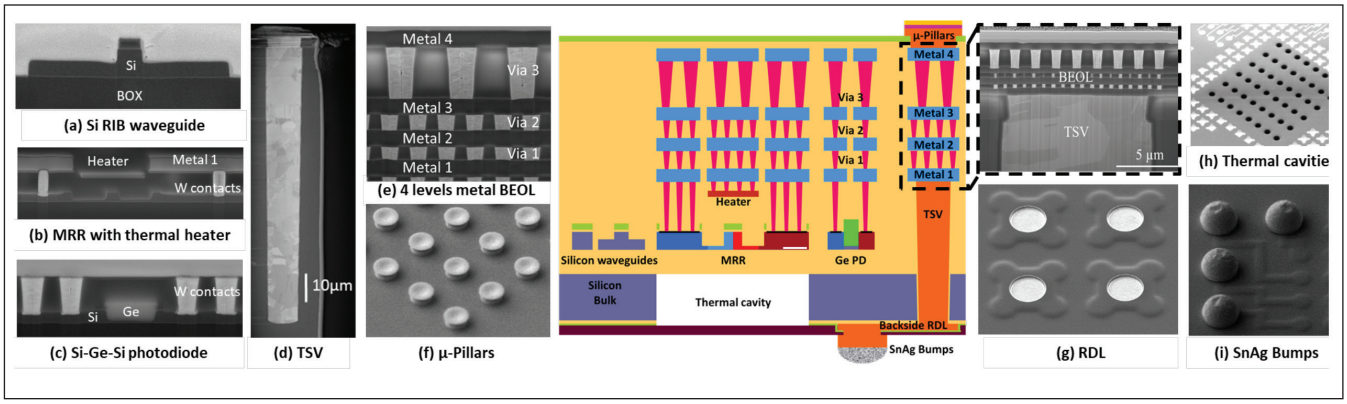


➤ Figure 2. POPSTAR optical network-on-chip (ONoC) architecture.

To address these challenges, we propose the POPSTAR optical network-on-chip (ONoC) architecture [1], with its ring topology of nested spiral single-writer multiple-reader (SWMR) optical links, as shown in Figure 1a. POPSTAR's ring-based topology allows easy scalability. The optical interface of each die is fully standard and includes decentralised destination-based routing without intermediate routers. This interface leverages low-footprint microring resonators as modulators, and filters on wavelength-division multiplexed (WDM) links.

The design includes a base SWMR link structure for each wavelength (Figure 1b), with a high-speed PN depletion-mode modulator on the transmission (Tx) side, and multiple low-loss PIN injection-mode filters on each potential receiver (Rx). Tuning these microring resonators involves thermal switching depending on the laser wavelength, which is enabled by closed-loop feedback and a dedicated remapping algorithm. This process makes it possible to lock close to the appropriate wavelengths while minimising the energy cost of tuning.

To route the optical data to its designated opto-electrical interface, during communication, only the Tx and relevant Rx adjust locking with voltage tuning of their filters to the laser wavelengths.



➤ Figure 3. Schematic cross-section of POPSTAR ONoC with associated SEM images of fabricated devices.

We have been working on creating a prototype of this architecture, connecting multiple 16-core computing chiplets with an optical network on an interposer. Each computing chiplet is associated with an electro-optical interface chiplet responsible for queuing, routing, and driving the optical network. Two additional electro-optical interfaces serve as primary inputs and outputs for the system, as shown in Figure 2. The computing chiplets were designed in a STMicroelectronics 28 nm fully depleted silicon on insulator support, whereas the photonic interposer is made using a dedicated process developed on an 8 inch silicon platform at CEA-Leti, combining silicon photonics and 3D integration.

Photonic and 3D process integration

The photonic IC for POPSTAR ONoC shown in Figure 3 is composed of RIB silicon waveguides (Figure 3a) and specific features like single polarisation grating couplers (SPGC) and splitters [2]. Propagation losses in RIB waveguides are measured at 0.3 dB/cm, and SPGC shows insertion losses at about 3.3 dB, in accordance with the standard specifications for silicon photonic circuits.

The ONoC architecture is based on matrices of microring resonators (MRR) (Figure 3b) with PN-junction microring modulators for data encoding, and PIN-junction microring filters for data switching and routing. MRRs are fabricated with three patterning levels – resulting in three silicon thicknesses (300 nm, 165 nm and 65 nm) – combined with six implantation levels.

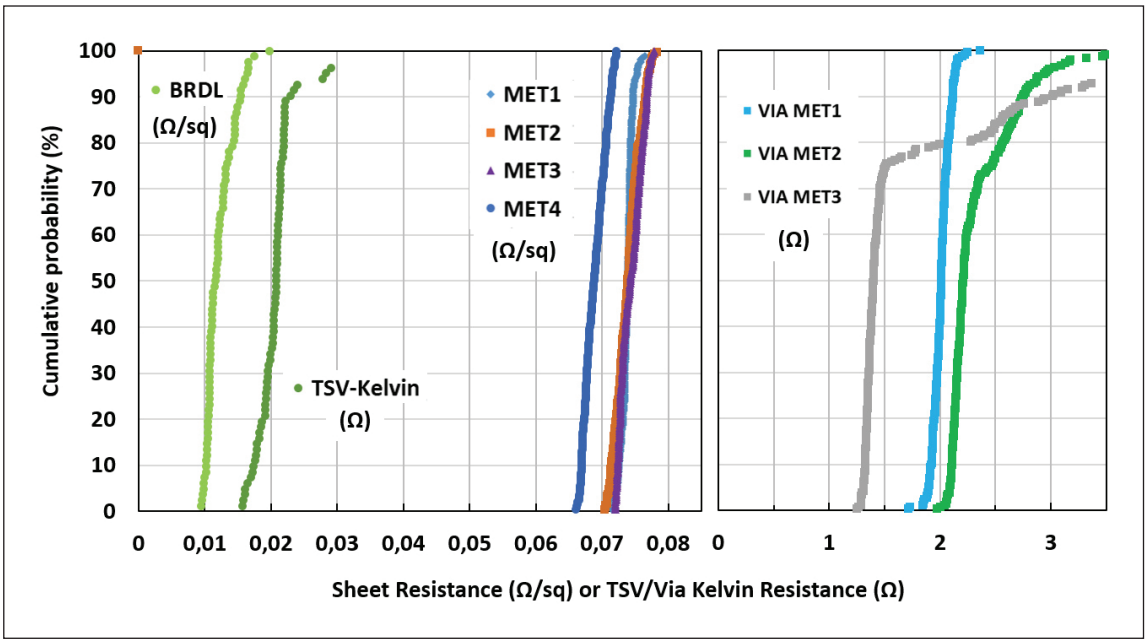
Lateral Si-Ge-Si heterojunction photodiodes monitor the readout of the optical signal (Figure 3c) with an intrinsic germanium area measuring 1 µm wide and 15 µm long. The germanium is epitaxially grown in a Si cavity. Photodiode responsivity exceeds 0.8 A/W at 1 V voltage bias, which is in line with the standard specifications for Ge photodiodes.

All silicon photonic devices are embedded in planarized silicon oxide. A standard CMOS process produces a silicide layer at the surface of contact areas on both the MRRs and photodiodes. This reduces the electrical contact resistance with back end of line (BEOL) levels. To optimise an MRR's efficiency, it is accurately tuned using a patterned Ti-TiN thermal heater embedded in silicon oxide and placed on top of the MRR. The different components – MRRs, Si-Ge-Si PDs, and thermal heaters – are electrically connected by W contacts. A SiN passivation layer caps the W contacts before through-silicon via (TSV) (Figure 3d) processing.

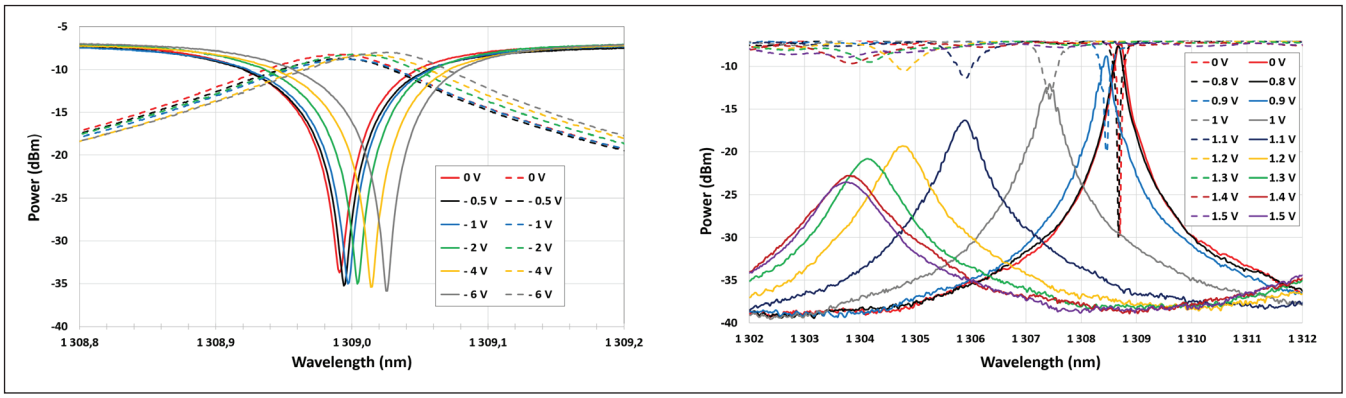
TSVs manage the frontside to backside interconnections. The POPSTAR interposer integrates 12 µm diameter and 100 µm thick TSV middle process successively formed by reactive ion etching (RIE) of the top dielectric photonic stack (SiN/SiO_2) and deep (DRIE) etching of the bulk silicon wafer.

A deposition of a dual silicon oxide layer (sub atmospheric chemical vapour deposition (SACVD) and plasma enhanced CVD (PECVD)) isolates the TSVs from the silicon bulk, followed by a Ti-TiN diffusion barrier deposition. Finally, a process of electroplating fills the TSVs with copper. A chemical mechanical polishing (CMP) step removes any excess copper and releases the W contacts of photonic active devices ready for BEOL processing.

A four-metal-layer BEOL (Figure 3e) is fabricated, on which active silicon photonic devices are contacted with top-stacked dies, and by TSV to the bottom substrate. The four metal layers consist of 540 nm thick AlCu. To match radio-frequency signal impedance, the inter-metal SiO_2 layer for the third via level is increased to 1.5 µm from the 540 nm used for the first and second via levels.



➤ Figure 4. Electrical resistances of routing levels and vias, alongside Kelvin structures for TSVs.



➤ Figure 5. (a) Through port (solid lines) and drop port (dashed lines) optical power for the PN MRR as a function of wavelength and reverse bias and (b) through port (solid lines) and drop port (dashed lines) optical power for the PIN MRR as a function of wavelength and forward bias.

A deposition of planarized SiO_2 and SiN layers passivate the fourth metal layer. To terminate the frontside process, Cu-Ni-Au micropillars (Figure 3f) with a pitch of 40 µm are processed to connect metal 4 to the top dies. The backside process starts with temporary bonding of bulk silicon carrier to the wafer's frontside using an adhesive polymer. We achieve thinning of the interposer wafer by coarse and fine grinding to a final thickness of about 110 µm.

Next, we perform electro-chemical deposition of a copper redistribution layer (RDL) (Figure 3g) with a minimum linewidth of 10 µm on the backside of the silicon photonic interposer. We pattern 40 µm diameter cavities (Figure 3h) in the silicon bulk, stopping at the buried oxide (BOX) underneath the MRR devices. For subsequent interposer mounting on a ball grid array substrate, we grow 80 µm pitch Cu-Ni-SnAg electroplated solder bumps (Figure 3i) on RDL after applying a thick organic coating to achieve passivation. The wafers are finally debonded on dicing tape and cleaned to remove adhesive residue in preparation for the packaging process.

Figure 4 shows results of in-line electrical testing of the interconnections' wafer level using an automatic prober. For the BEOL tests, we find a uniform distribution of resistance for all four metal layers, based on 2 µm wide – 2 µm spaced comb serpentines probing. Measurements revealed 2.2 Ω/via for via 1 and via 2, and 1.7 Ω/via for via 3 [2]. The Kelvin resistance value measured for the 12 µm diameter TSV is well centred on 21 ± 3 mΩ, and is in line with the expected theoretical value. We measure a high yield for the backside RDL, with a mean r-square of 12 ± 2 mΩ/sq.

MRR characterized at metal 1 level after TSV integration

The POPSTAR photonic circuit is designed to demonstrate the capacity of the ONoC architecture at moderate optical link speed (>10 Gb/s). We have verified the operation of the MRR for modulation and switching/routing several times during integration and fabrication, and have presented the results for the tests performed after metal 1 level and TSV integration. Figures 5a and 5b show representative electro-optical device responses for PN- and PIN-based MRR devices. For the PN MRR, which serves as a modulator, the modulation efficiency is around 10 pm/V, which, combined with the quality factor extracted from the through port measurement (solid lines in Figure 5a) of about ~10 200, leads to an optical bandwidth of 22 GHz. This bandwidth is sufficient for the speed targeted.

For the PIN-based MRR, which acts as a switch/router, speed is not a requirement, but it should nevertheless be compatible with efficient switching between the through port and the drop port with low insertion losses. Based on the data presented in Figure 5b, a high quality factor ensures negligible off-resonance losses in the through port, whereas the signal in the drop port shows negligible losses at resonance. Thus, for near-resonance tuning, we record a loss of about 12 dB under 0.9 V, rising to 22 dB under 1 V forward bias.

The four key challenges of POPSTAR interposer integration

Initially, we undertook dedicated studies to characterize the impact of TSVs on MRRs, depending on the separation distance. From these, we defined the TSV-MRR keep-out zone. Indeed, the presence of a large amount of copper and numerous stressed layers inside and on TSV sidewalls creates a strain field around each TSV, which can affect the waveguide and MRR. Since a mechanical constraint on the waveguide may affect its refractive index, it was essential to define the design rules governing co-integration of TSVs in photonic circuits. Experimental data indicate that integration did not modify the performance of MRRs, SPGCs or PDs, when TSVs are placed just 1 µm from the device [3]. This first result encouraged us to insert TSVs within functional MRR matrices with an optimised and compact footprint.

The second challenge was to integrate TSVs just after creating the contacts. During the CMP process, after isolating the TSVs and filling them with copper, several microns of copper and dielectric material had to be removed from the surface to land on W heater contacts with a final height of 300 nm. To ensure removal stopped at the appropriate point on these contacts, we inserted a SiN CMP stop layer before the TSV process, creating a uniform final position for the CMP at wafer level with careful measurement

of in-line ellipsometry thicknesses to avoid leaving contacts unrevealed or their complete removal. The third challenge related to the warp of the interposer during subsequent packing steps. Due to a thick (800 nm) BOX and several routing layers on the frontside, the unbalanced thermomechanical constraints of the system give the 110 µm interposer a convex curvature. To account for these frontside constraints, we studied a number of backside integration alternatives. By experimental design, we identified the effects linked to the introduction of dielectric stressed layers, copper thickness, density of the backside RDL, and passivation polymer thickness. Based on the results obtained, we defined an optimised integration flow, producing a final interposer bow compatible with packaging steps over a temperature range from ambient to 260 °C.

The final challenge, which is important to highlight, related to the solution for extending the range of MRR resonance frequency tuning at CMOS-compatible voltages. Thermal tuning of an MRR with heaters was limited due to heat dissipation in the silicon substrate. Previous reports indicated that removing the substrate beneath the MRR resulted in up to 70 percent power gain [4]. This approach could improve the thermal insulation of an MRR, and thus the efficiency of heat-induced tuning in the case of the photonic interposer. The interposer backside process flow already involves wafer bonding and substrate thinning, so processing cavities by DRIE adds few steps and is easy to implement.

Relevance of heterogeneous integration

A monolithic approach would require compromises that might be detrimental to overall system performance, as these technologies are not very compatible in a monolithic integration process. Heterogeneous systems allow co-optimisation of technology and design, using TSVs to create essential signal density. The heterogeneity of the system allows the use of advanced CMOS nodes such as FDSOI 28 nm chiplets for compute dies and electro-optical interface dies, whereas the photonic interposer benefits from the most advanced photonic technology with very low waveguide losses. Additionally, if we use a standard interface for microbumps, pitch, and communication IP blocks, we could envisage a versatile system that would be compatible with next-generation chiplets.

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From transceivers to speed-of-light AI

Since 1985, silicon photonics has progressed from the initial development of high confinement waveguides to strategically incorporate CMOS techniques, establishing its dominance in the transceiver space. In the coming years, it has the potential to expand to a wide range of innovative applications.

BY MARTIN VALLO, SENIOR ANALYST IN PHOTONICS AT YOLE

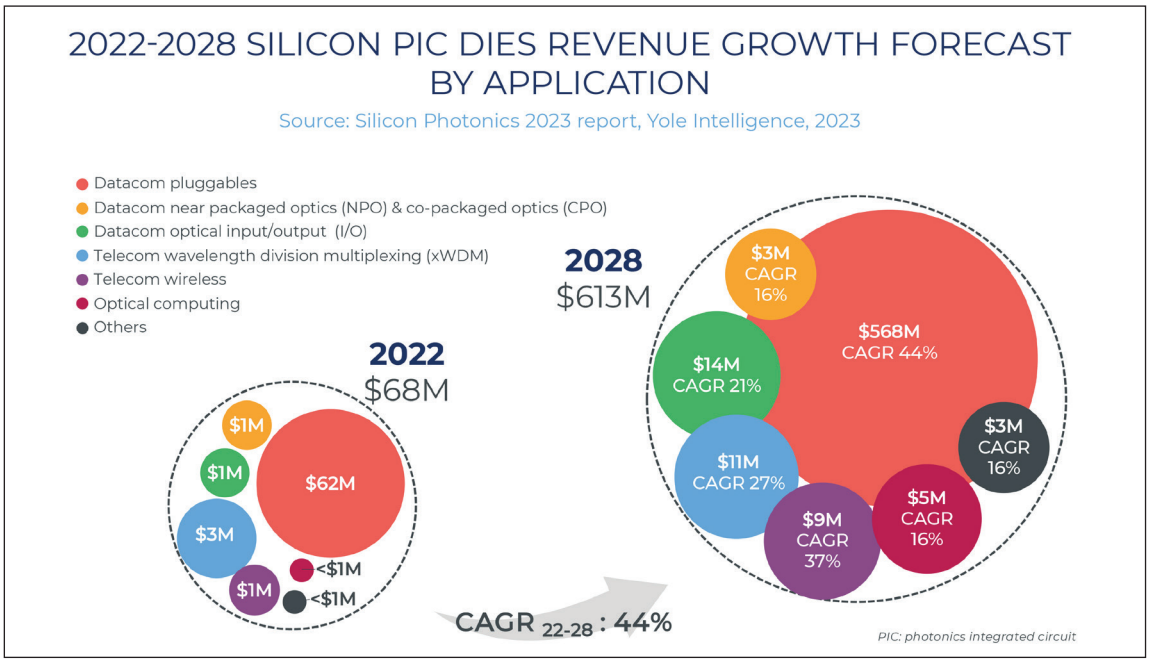
SINCE EARLY 2023, there has been a lot of hype around – and massive investments into – silicon photonics, especially optical computing, optical I/O, and diverse sensing applications. It seems logical that primary technologies in various applications will be replaced relatively quickly by optical-based designs and architectures. The giants forecast that optics will be necessary and become ubiquitous relatively soon, while startups are developing new applications through R&D. So, can we expect this prediction to be realised any time soon?

While there are many arguments about the necessity of photonics coupled with electronics, the largest silicon photonics market – datacom pluggables – generates only around 12 percent of datacom transceiver revenue (projected to reach 30 percent by 2028). The semiconductor market is suffering from an extended period of decline, leading to more pragmatic buying behaviour on the part of customers. DC operators prefer long-established and low-cost technology solutions. Yole Intelligence's market research shows that silicon photonics is not yet a primary technology, even for intra-data-centre interconnects with up to 500m reach.

In this context, silicon photonics remains a technology in active development, with a wide array of potential applications, hinting at promising opportunities on the horizon. In the coming decade, frontrunners will emerge, leading to industry consolidation. Nevertheless, the broad spectrum of applications will ensure abundant opportunities for the technology to expand and proliferate.

Yole Group, in its new Silicon Photonics 2023 report, estimated the silicon photonics PIC market was worth US$68 million in 2022 and is forecast to generate more than US$600 million in 2028 at a 44 percent Compound Annual Growth Rate for 2022-2028 (CAGR2022-2028). This growth will mainly be driven by 800G high-data-rate pluggable modules for increased fibre-optic network capacity. Additionally, projections of rapidly growing training dataset sizes show that data will need to use light to scale ML models using optical I/O in ML servers.

Substantial data centre requirements, particularly in the domains of artificial intelligence (AI) and machine learning (ML), are expected to fuel the ongoing



➤ Figure 1: Growth forecast for various silicon photonics applications. Credit: Yole Intelligence.

over the next decade. With the conventional processor-centric computing architecture and copper interconnects, the state-of-the-art chips based on 3nm technology are approaching their physical limitations, while the necessity for faster data transmission has surged. Silicon photonics, with its ability to facilitate high-speed communication, has therefore become a prime focus.

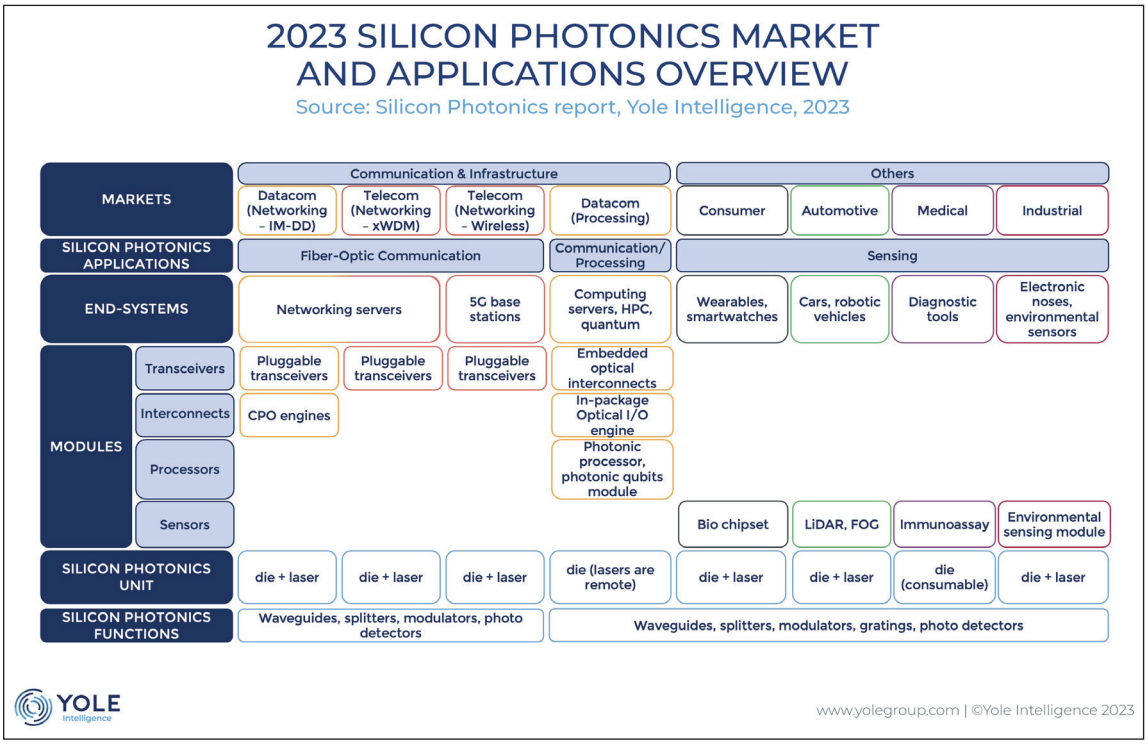
Architectures that include optical I/Os can take out streamline access between compute nodes and memory pools, harnessing the fan-out capabilities of optics to minimise the number of switching hops required to access resources. Broadcom's strategic plan outlines a trajectory for switching chips, projecting an increase from 51.2 Tb/s (5 nm process node) this year to 102.4 Tb/s (3 nm process node) in 2025, and an impressive 204.8 Tb/s (2 nm process node) by 2027. This exponential growth could serve as a significant catalyst for the advancement of silicon photonics in networking applications, paving the way for significantly enhanced data capacity in the future. Silicon photonics provides a versatile platform for applications with high-volume scalability demands.

The primary and most immediate domain for its application is data centres, where Intel holds a dominant position. A second major high-volume application is telecommunications, as exemplified by Acacia, benefiting from the consistent and superior performance of silicon processing. A third broad application area encompassing optical LiDAR systems has significant potential but faces cost and 2D beam-scanning challenges. 3D integration, housing both chips on the same silicon substrate, is vital for seamless control. Optical gyroscopes need sizeable chips for sensitive rotation sensors, benefiting from silicon substrates and SiN waveguides. Quantum computing is pivotal in the evolving AI and machine learning landscape. Optical computing, ideal for efficiency-focused tasks, garners industry attention and promises substantial impact.

Advanced photonic components and their integration for medical use can transform healthcare, enabling faster, more precise diagnostics, treatment, and patient monitoring. Overcoming regulatory and standardisation challenges may be necessary for clinical adoption. The outlook for silicon photonics-based medical applications is promising and holds significant potential for various healthcare and medical fields. Extending silicon photonics into the visible spectrum shows potential for future developments, offering a vast range of innovative applications.

The silicon photonics industrial landscape is forming around diverse players, including: major vertically integrated players (Intel, Cisco, Marvell, Broadcom, Nvidia, IBM, etc.); actively engaged in the silicon photonics industry; startups and design houses (AyarLabs, OpenLight, Lightmatter, Lightelligence); research institutions (UCSB, Columbia University, Stanford Engineering, MIT, etc.); foundries (GlobalFoundries, Tower Semiconductor, imec, TSMC, etc.); and equipment suppliers (Applied Materials, ASML, Aixtron, etc.). All these players contribute to significant growth and diversification.

Intel is a leader in this field, investing heavily in research and development. There are numerous startups focused on silicon photonics technology, aiming to bring innovation to the market. These startups often focus on specific applications or novel technologies, such as high-speed transceivers, optical interconnects, and LiDAR systems. Universities and research institutions play



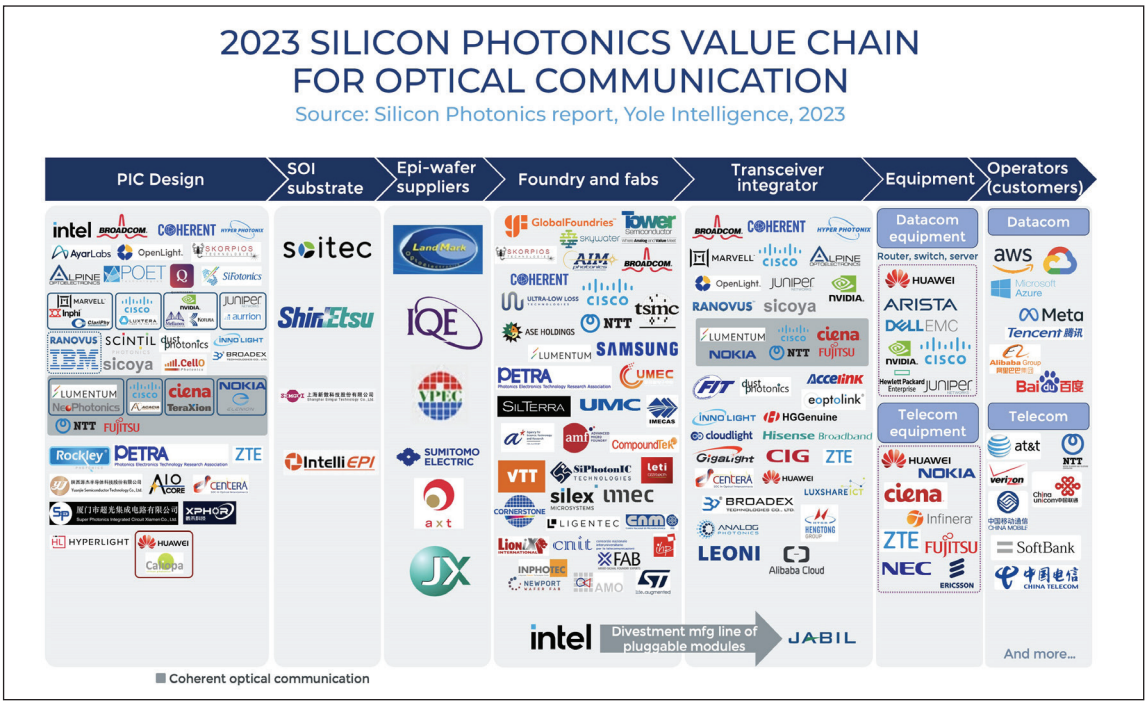
➤ Figure 2: A vast array of potential applications hinting at promising opportunities on the horizon. Credit: Yole Intelligence.

a crucial role in advancing silicon photonics, often collaborating with industry partners to develop cutting-edge technologies and share knowledge.

Foundries provide silicon photonics services, enabling other companies to manufacture their photonic chips. These foundries often use advanced manufacturing processes, such as CMOS (complementary metal-oxide-semiconductor) technology, to produce these chips. Equipment suppliers provide the tools necessary for manufacturing silicon photonic devices. The quality and precision of these tools are critical for producing high-performance photonic components.

The silicon photonics industry is marked by ongoing research and development, strategic partnerships, and collaboration between players to advance the technology. It is also becoming more accessible to a broader range of companies, thanks to silicon photonics foundries and growing expertise in the field. The technology's ability to improve data transfer speeds, reduce energy consumption, and enable various applications make it a promising area for industrial growth.

Intel remains the market leader in datacom, with



➤ Figure 3: Intel, Cisco, Marvell... The silicon photonics industry is confident of its future value. Credit: Yole Intelligence.

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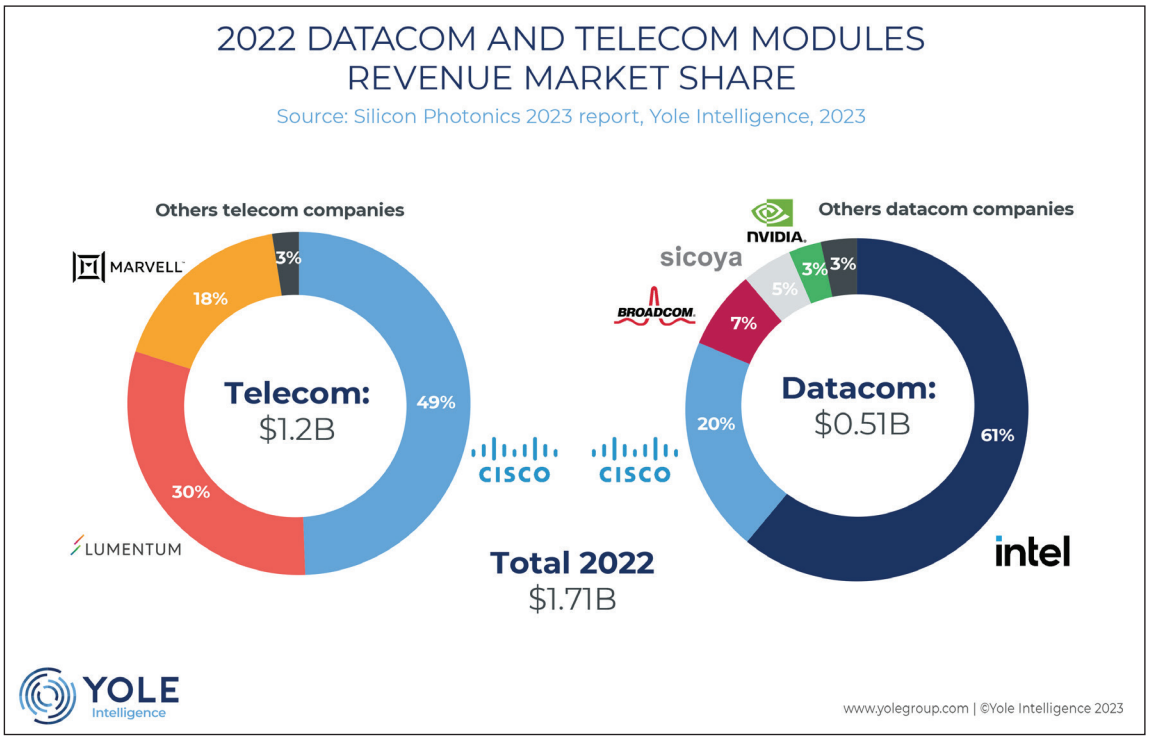


Figure 4: Revenue market shares for datacom and telecom modules in 2022. Credit: Yole Intelligence.

a 61 percent market share in both shipments and revenue, followed by Cisco, Broadcom, and other smaller companies.

With the recent strengthening of product portfolios and the commercialization of PICs by other players, Yole Intelligence expects that Intel will lose its dominant market share. In telecom, Cisco (Acacia) has almost 50 percent market share, followed by Lumentum (Neophotonics) and Marvell (Inphi). The telecom silicon photonics market is driven by coherent pluggable ZR/ZR+ modules.
Intel has recently muddied the water, failing to complete the acquisition of Tower as well as divesting its manufacturing line of silicon photonics-based pluggable modules to Jabil. Intel, which is struggling to regain the lead in chip production technology, hoped the merger with Tower would help accelerate a shift to become a major manufacturer for other chip designers. The failure to complete this acquisition will force it to focus its Intel Foundry Services (IFS) division business strategy solely on leading-edge process technologies. It could also send a further chill through American companies with deep ties in China, as technology is the prime battlefield in the tense economic relations

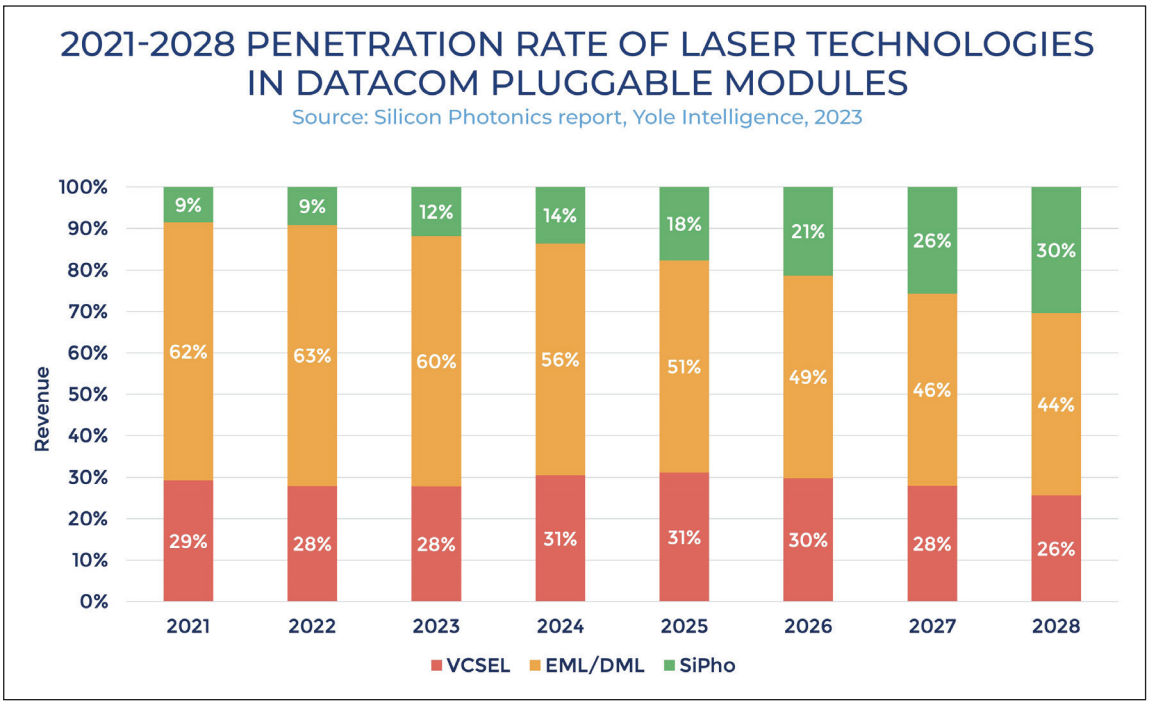
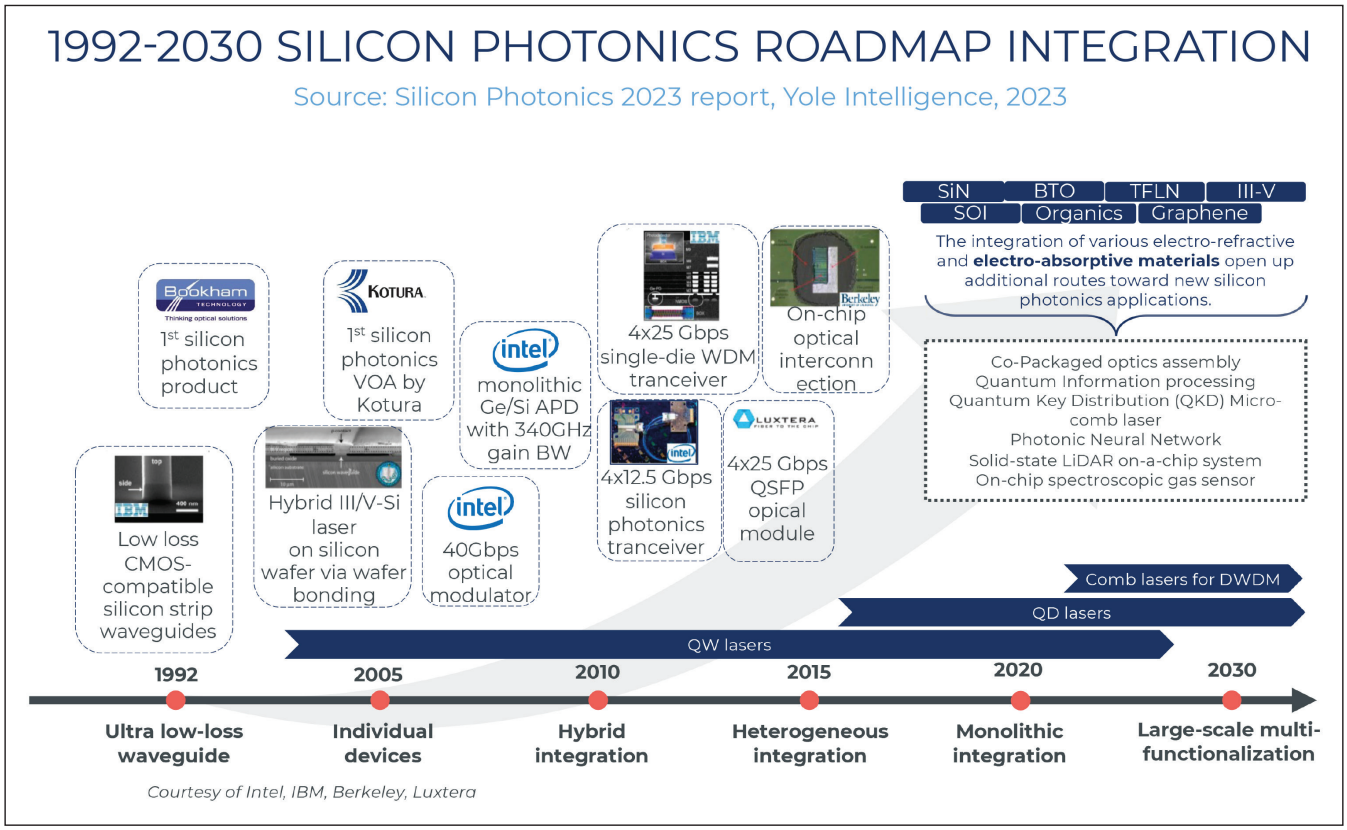


Figure 5: Penetration rate of laser technologies in datacom pluggable modules 2021-2028. Credit: Yole Intelligence.



➤ Figure 6: Roadmap of silicon photonics integration 1992-2030. Credit: Yole Intelligence.

between China and the United States. Intel's recent strategic decision to offload its manufacturing line to Jabil allows it to optimise its operational efficiency, reduce costs, and leverage Jabil's expertise to serve its customers better, remain competitive in the market, and boost profitability. Intel is shifting its focus towards the development and production of higher-value components, such as processors and compute platforms, which are integral to forthcoming optical interconnects designed for disaggregated data centres. The company is setting its priorities to concentrate on silicon photonics components that are crucial for emerging sensing applications, for example in the automotive industry or in medical uses.

Silicon photonics: what is happening in China?

Silicon photonics is an advanced technology requiring access to high-level manufacturing skills, which China still lacks. Chinese companies are at the prototyping or sampling level and rely on external partnerships to supply silicon photonics transceivers or optical engines in volume. Skorpios-Luxshare-Broadex and Sicoya-Broadex are good examples of collaborations in datacom. The Chinese telecom players Huawei and ZTE usually purchase PICs from Cisco or Nokia.

In 2014, Huawei and imec added silicon photonics to their joint research on optical data link technology. That followed Huawei's acquisition of Caliopa, a developer of silicon photonics optical transceivers spun out of imec and Ghent University. Ultimately, the Huawei-imec collaboration was terminated, and shipments of ASML's EUV lithography systems to China were banned in 2019.

After being put on the US Commerce Department's Entity List, Huawei has continued with its research, which is essential both for its telecom equipment business and its efforts to escape sanctions imposed by the US government. China has strong motivations to make substantial investments in silicon photonics. Huawei is trying to procure American equipment essential for chip production and other restricted materials and thus uses a covert strategy to circumvent international sanctions.

What is the technology pathway for silicon photonics?

Despite silicon's shortcomings as a light emitter, recent breakthroughs have introduced innovative approaches to creating active optical components on silicon and have achieved mass production in just a few years. It's worth noting that silicon's internal quantum efficiency is low, whereas direct bandgap III–V materials boast an efficiency close to 100 percent. After the success of bonded LEDs (GaAs on GaP) back in the 1990s in high-brightness LED applications, it was anticipated that bonding III–V materials to silicon would also prove highly effective.

A pivotal collaboration between the UCSB and Intel played a crucial role in resolving manufacturing issues and achieving high-volume production. The pathway for silicon photonics appears to be monolithic integration through quantum dots (QD). Conventional InP PICs require five or six regrowth

By utilising 3D bonding to connect the photonic integrated circuit (PIC) to electronics, which may operate at lithography of 3nm or beyond, we can harness the strengths of both worlds

steps, which are complex and expensive, and have limited yield. Heterogeneous integration offers the advantage of combining multiple materials, and bonding and processing simultaneously. With this approach, modulators, lasers, and detectors can be bonded side by side and processed together, offering inherent benefits. However, the cost of the substrate is not insignificant, as III–V substrates are considerably smaller than 300 mm, prompting a growing interest in monolithic integration. Therefore, the monolithic integration techniques of on-chip lasers offer a promising approach towards high-density and large-scale silicon photonic integration.

The choice between quantum wells (QW) and quantum dots in monolithic GaAs-on-silicon devices has been a critical issue. After four decades of research, QD lasers have demonstrated intrinsic parameters surpassing QW devices, providing a much longer lifetime. For example, the QD gain medium exhibits a large tolerance to material defects, allowing for the epitaxial integration of QD lasers on silicon, while its fast gain response makes it suitable for amplifying high-speed signals.

Additionally, the QD gain medium's stability at high temperatures enables uncooled operation, while narrow linewidth lasers, low threshold current density, internal loss, and confinement factor contribute to low noise figure operation. Significant improvements in III-V/silicon epitaxy have pushed QD technology to the frontiers of Si photonics and a wide range of applications. Still, much effort is needed to make this technology ubiquitous and affordable for high-volume, high-performance PICs.

The realm of silicon photonics is not confined to a single substrate or material. Various material platforms, such as thin film $LiNbO_3$ (TFLN), SiN, BTO, and GaAs, among others, have demonstrated their potential for photonic integration. Among these, TFLN on silicon has made rapid progress. With its tight mode confinement, TFLN has proven invaluable for creating high-speed modulators, comb generators, and a diverse array of devices. Notably, HyperLight has played a pivotal role in advancing this technology with remarkable success.

Waveguides extend beyond silicon and encompass a wide range of materials, including $LiNbO_3$ compound semiconductors, compound semiconductor on insulators (CSOI), SiN, and more. SiN waveguides, for instance, support 980 nm tuneable lasers operating at remarkable temperatures, presenting exceptional possibilities.

There is a significant disparity in scale when comparing silicon photonics, which operates at 45 nm, with silicon integrated circuits, which have scaled down to just a few nanometres. Remarkably, silicon photonics doesn't require 3 nm lithography, as the 45 nm technology is perfectly adequate for producing high-performance, high-quality silicon photonics devices. This is advantageous because employing older foundries with lower lithography levels is very cost-effective.

By utilising 3D bonding to connect the PIC to electronics, which may operate at lithography of 3 nm or beyond, we can harness the strengths of both worlds. Consequently, it doesn't appear rational to integrate photonics and electronics on the same wafer in the same process flow, as it would increase costs and production timelines. Instead, the more sensible approach is 3D integration, aligning the most advanced electronics with the most advanced photonics.

Silicon photonics has the potential to revolutionise the way data is transmitted and processed, offering benefits in terms of speed, power efficiency, and cost-effectiveness. The technology pathway involves a combination of material science, device engineering, and application development to realise this potential.

ABOUT THE AUTHOR

MARTIN VALLO, Ph.D., is a Senior Analyst, Photonics, specialized in optical communication and semiconductor lasers within the Photonics and Sensing division at Yole Intelligence, part of Yole Group. With 12 years of experience in semiconductor technology, Martin is currently involved in the development of technology & market reports and the production of custom consulting projects at Yole.

Prior to his mission at Yole, Martin worked at CEA (Grenoble, France), where he focused on the epitaxial growth of InGaN/GaN core-shell nanowire LEDs by MOCVD and their characterization for highly flexible photonic devices.

Martin graduated from the Academy of Sciences, Institute of Electrical Engineering (Slovakia) with an engineering degree in III-nitride semiconductors.

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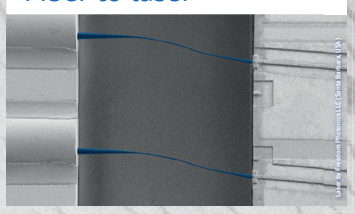
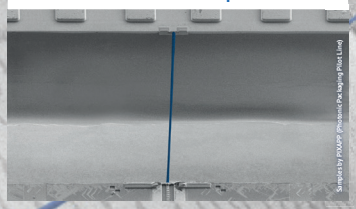
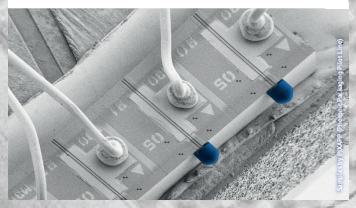


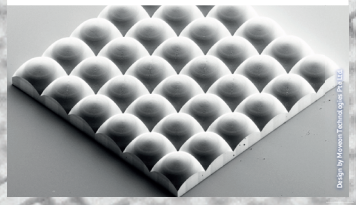
Laser to SOI chip



Lens on laser



Large scale micro-optics



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State-of-the-art electronic photonic design automation

Through partnerships with foundries and electronic design automation (EDA) tool providers, Ansys has created a comprehensive Electronic Photonic Design Automation (EPDA) solution, featuring the co-design and co-simulation of EICs and PICs.

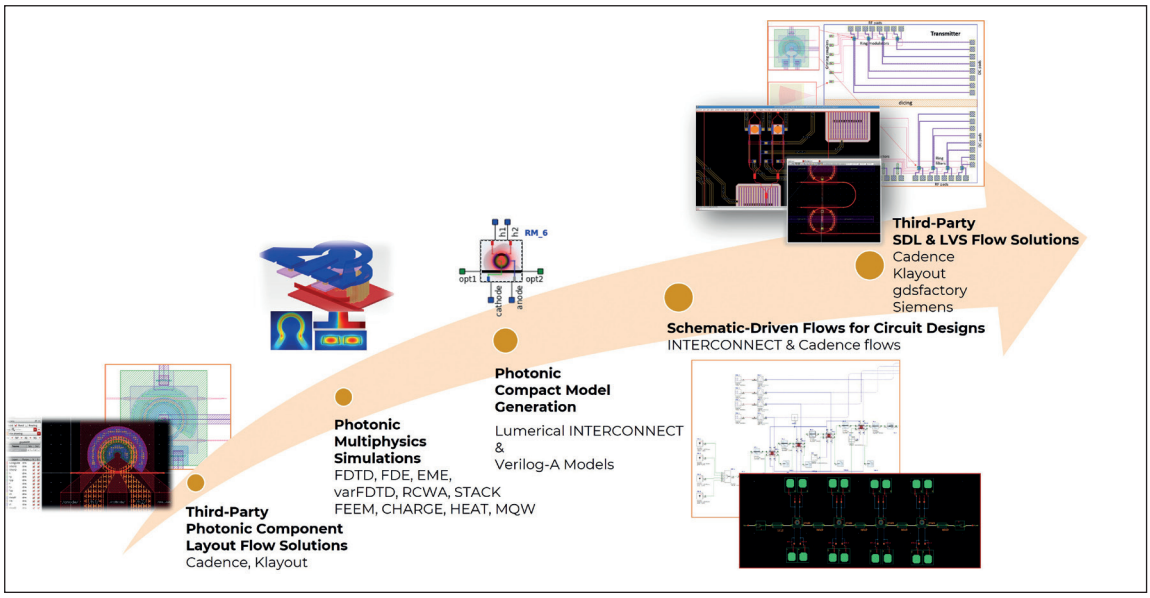
BY RAHA VAFAEI, ZEQIN LU, AHSAN ALAM, PARYA SAMADIAN, FEDERICO DUQUE GOMEZ AT ANSYS

IN RECENT YEARS, photonic integrated circuits have been on a trajectory of ever-increasing design complexity, driven primarily by the massive growth in data, and the growing demand for high performance, low power consumption, and low cost. To meet these demands, the PIC industry has evolved to emulate the world of electronics. In electronics, foundries can yield hundreds of chips on a single wafer, each one meticulously designed by engineers and incorporating billions of transistors, with each transistor about 1000 times smaller than what the human eye can perceive.

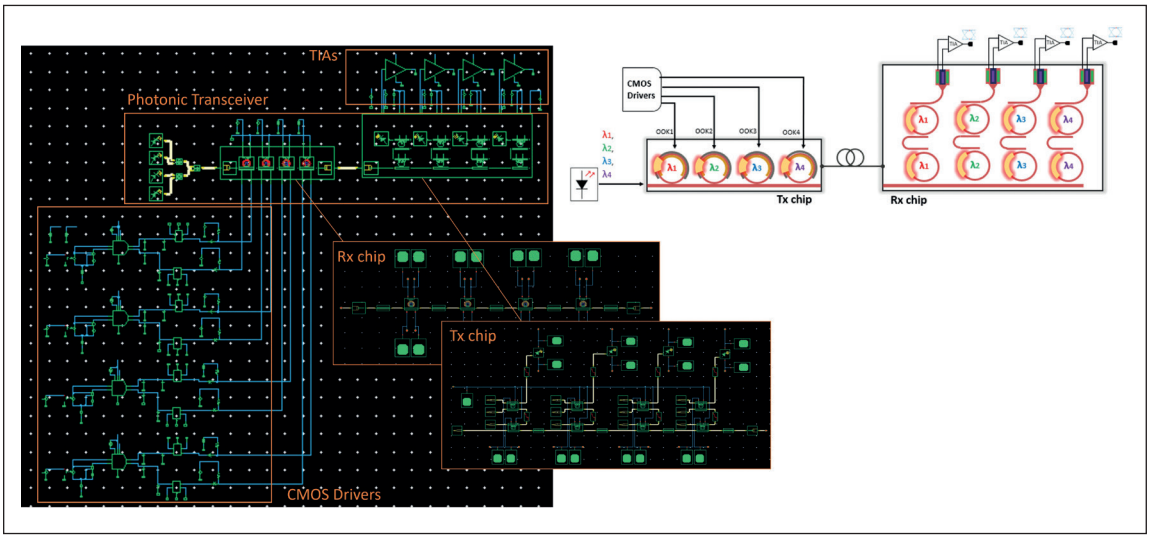
The electronic industry owes this incredible success largely to the maturity of the CMOS manufacturing facilities and the electronic design automation (EDA) tools and workflows. Similarly, to meet the growing demands for photonic solutions, the industry has responded with an orchestrated effort between foundries and design tool providers to create an electronic photonic design automation (EPDA) ecosystem. In collaboration with foundries and other EDA providers, Ansys has developed EPDA workflows built on best-in-class tools that meet photonic design requirements while embracing flexibility for designers to run on their preferred platforms. Figure 1 shows an overview of our multiplatform EPDA solution which enables designs from a component to a working chip.

Multiplatform photonic system design

Photonic integrated circuits are often controlled or driven by electronic integrated circuits (EICs). Ideally, EICs and PICs should be co-designed in a single schematic and be co-simulated to capture the tight interaction between the optical and electrical domains, such as photonic components' loading effects on the EICs and the electrical feedback loops between the two domains. This allows designers to analyse and optimise the overall performance. When it comes to simulating purely a photonic circuit, the simulation can be done entirely in Lumerical INTERCONNECT which provides a schematic design environment with a circuit simulator purpose-built for simulating complex photonic integrated circuits. To design a complex photonic chip with EIC controls, however, it is important to model the full electro-optical circuit. To this end, Ansys Lumerical and Cadence have partnered over the years to provide the industry's first and most mature EPDA environment. The integration between Cadence Virtuoso and



➤ Figure 1: In collaboration with third-party EDA and Layout tool providers, Ansys Lumerical enables scalable designs, from concept to a working chip.



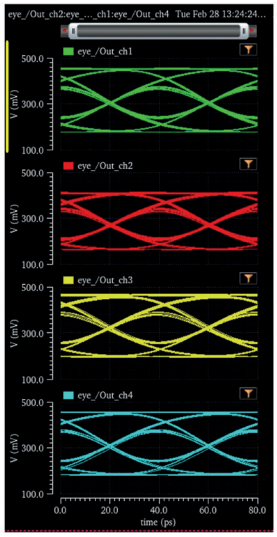
➤ Figure 2: The left-hand side of the figure shows the complete schematic capture in Cadence Virtuoso including the photonic transceiver, CMOS drivers, and TIAs. The right side shows the ring-based, 4-channel DWDM transceiver circuit.

Lumerical INTERCONNECT means users can take advantage of these two engines for the photonic and electronic parts of their system respectively. In this seamless integration, the Virtuoso schematic design environment is used for complete schematic capture of the system, including the photonic and electronic sub circuitries. Virtuoso ADE can co-simulate by simultaneously running Spectre and INTERCONNECT engines in the background and exchanging data to solve the full system.

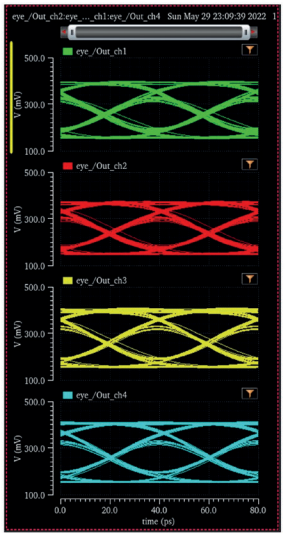
For simulating full electro-optical circuits, Ansys Lumerical also provides advanced photonic Verilog-A models: analogue behavioural models that can be solved by SPICE solvers and are commonly used in the electronics world. Photonic Verilog-A models describe the behaviour of photonic elements using the standard Verilog-A language, leveraging the maturity of the corresponding electrical methods. Hence these models are also ideal for full electro-optical system simulation in EDA platforms like Cadence Spectre. Using advanced photonic Verilog-A models from Ansys, Spectre can solve both electrical and optical parts of the circuit. All the above platform options for modelling PICs have been developed to meet the unique requirements of optical signals, taking into consideration amplitude, phase, multi-wavelength, bidirectional and multimodal behaviour. It is important to note that all these platforms deliver consistent results as the models have been thoroughly verified for the physics and workflows they support.

We will now consider the co-design and co-simulation of a 4-channel, dense-wavelength-division-multiplexing (DWDM) silicon photonic transceiver and its electrical drivers and receivers as shown in Figure 2. The design consists of continuous-wave (CW) laser sources, a photonic transmitter (Tx) chip, a photonic receiver (Rx) chip, high-speed CMOS drivers, and transimpedance amplifiers (TIAs). We leverage our Cadence schematic-driven flow to design the photonic circuits and the electronic circuits and compare the results of the co-simulation using INTERCONNECT

Spectre-INTERCONNECT flow models



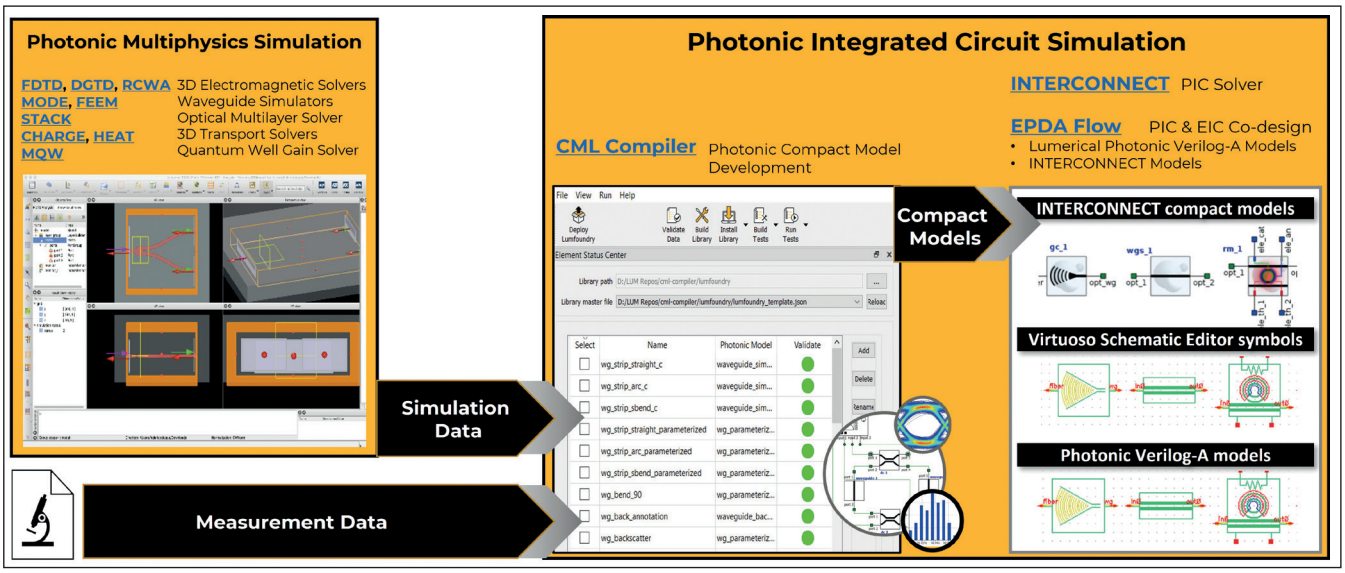
Photonic Verilog-A flow



Benchmark Results: Photonic Verilog-A Models vs. INTERCONNECT Models

	WDM Channel	INTERCONNECT-Spectre	Verilog-A
Rise Time (ps)	1	19.61	21.02
	2	19.52	21.08
	3	20.04	22.17
	4	20.37	22.40
Fall Time (ps)	1	19.15	20.40
	2	18.36	19.11
	3	19.36	20.72
	4	19.25	20.70
Max Eye Height (mV)	1	113.5	106.15
	2	102.67	106.28
	3	119.49	110.06
	4	115.35	116.74

➤ Figure 3: Simulations using the DWDM example demonstrate consistent simulation results between the Verilog-A models versus interconnect models.



➤ Figure 4: Automated photonic compact model generation with Ansys Lumerical CML Compiler. CML Compiler takes simulation data from the Ansys Lumerical Photonic Multiphysics Simulation Suite and measurement data as input to generate consistent photonic Verilog-A models and INTERCONNECT models.

models with the results of electro-optical simulations using the Verilog-A models. Figure 2 shows the complete schematic capture in Virtuoso including the photonic transceiver, CMOS drivers, and TIAs. Comparing the electronic-photonic co-simulation using INTERCONNECT models versus running Verilog-A models, we can see consistent results in key measures of performance, such as rise/fall time and eye-opening, as shown in Figure 3.

Multiplatform photonic PDK generation

The precision of a circuit's simulation results relies on the fidelity of the models employed in its building blocks. Accurate models are established through rigorous component-level simulations, measurements derived from device characterization, or a combination of both approaches. The complexity of multiphysics effects within these devices necessitates models that can capture their intricate interplay while accounting for fabrication realities. To account for these variations and ensure desired post-fabrication functionality, statistical models for yield analysis are essential.

Over the years, Ansys Lumerical foundry partners have leveraged the Lumerical CML Compiler to automatically generate thousands of calibrated photonic compact models. CML Compiler automates the process of generating compact model libraries as depicted in Figure 4, essentially bridging the gap between the world of component designers and circuit designers. It comes with purpose-built photonic models that can be customised with user data from various sources, such as experiments and simulations. While the Lumerical Multiphysics suite of tools has automated data-collection workflows to facilitate data collection for CML Compiler, users are not restricted to only using these workflows, but can potentially bring data from any simulation tools or measurements. Statistical data can also be provided to enable the models for corner and yield analysis. The same input data source is used to generate models for Lumerical INTERCONNECT and Cadence Virtuoso platforms, as well as photonic Verilog-A models for electro-optical simulation in Virtuoso. It can also generate Virtuoso symbols for co-simulation with INTERCONNECT. Additionally, it encrypts the models to ensure the security of the data and any IP contained in the models, and makes library maintenance fast and easy through automated quality assurance tests. Figure 5 depicts the described photonic compact model generation workflow, in four easy steps.

In an ideal photonic design flow, circuit designers would use off-the-shelf components from a foundry PDK. However, the photonics industry is still in the early stages of development, and custom components are often needed to meet specific design requirements. The Lumerical photonic component suite of solvers is equipped with a unique layer-builder object which facilitates a process-enabled custom design flow. The layer-builder object uses two key pieces of information to automatically generate foundry-compatible structures ready for simulation: the process file, and geometry information. The layer builder relies on a foundry process file to accurately define fabrication process layers, material properties, doping concentrations, and process variations.

Additionally, the layer-builder object reads layout geometry data for the device from a GDS file, or directly from KLayout or the Virtuoso Layout Suite database. This streamlined process ensures that the simulation environment is equipped with the necessary information for accurate multiphysics

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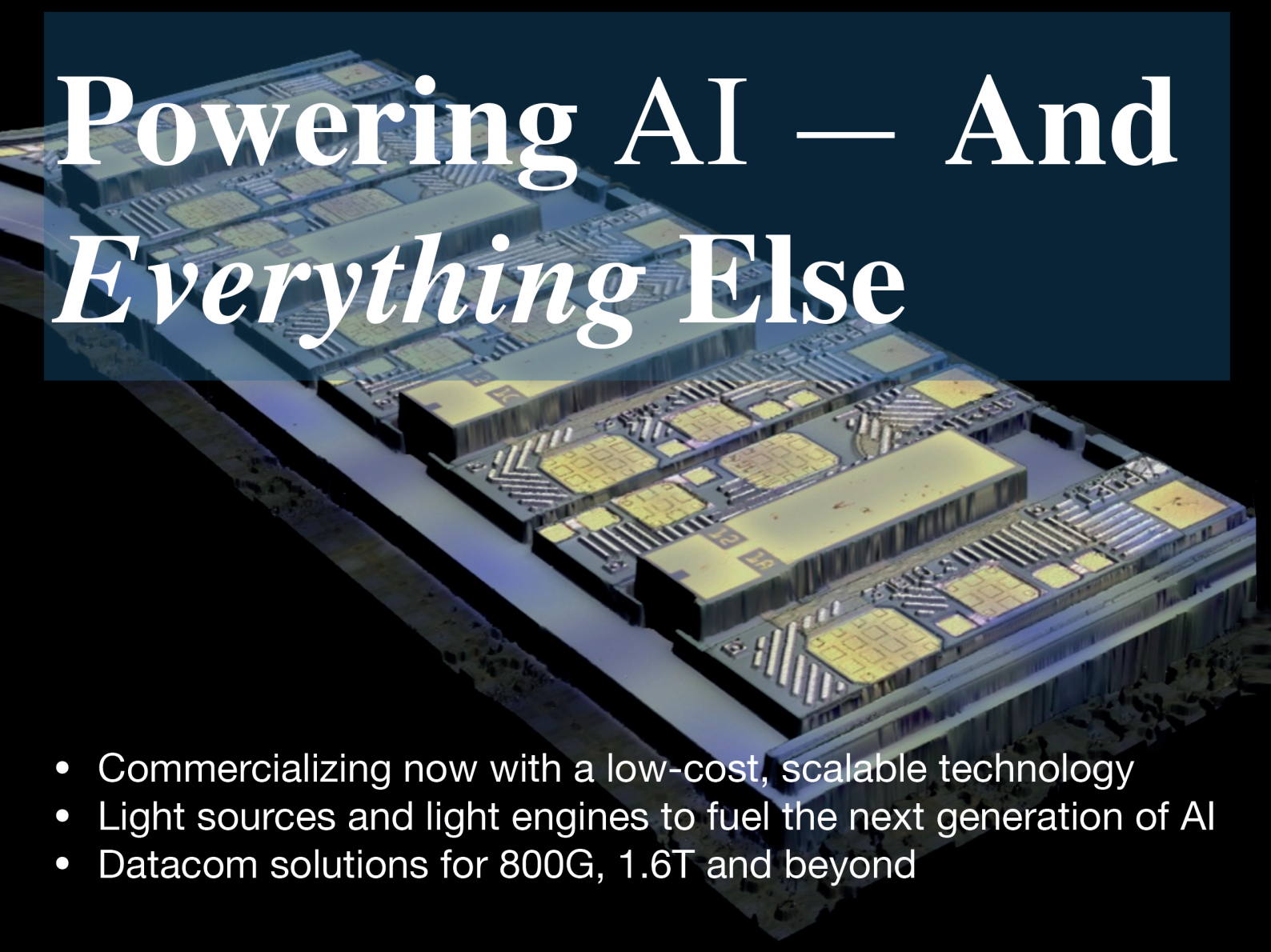

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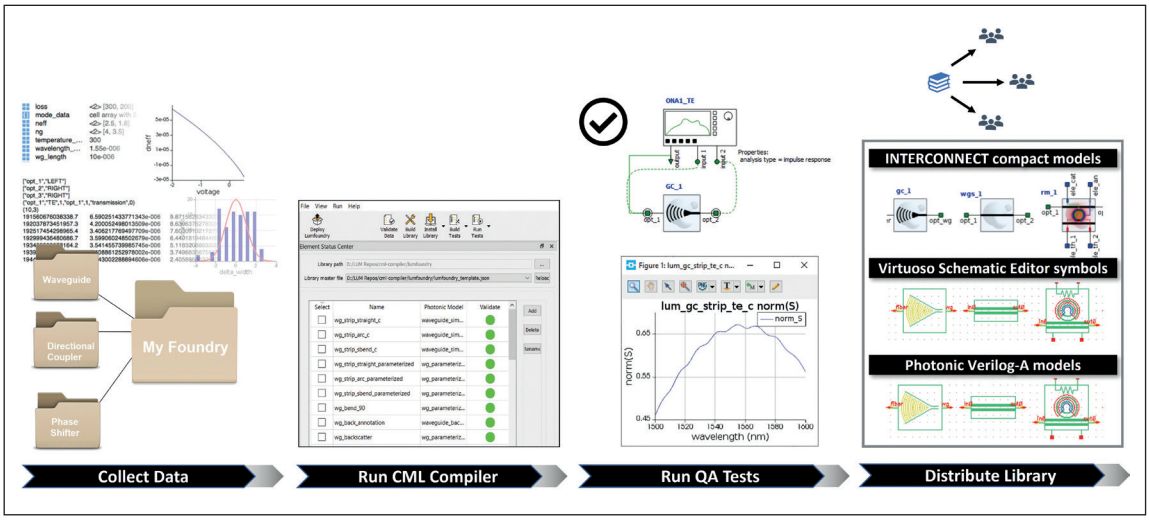


➤ Figure 5: Photonic compact model generation workflow.

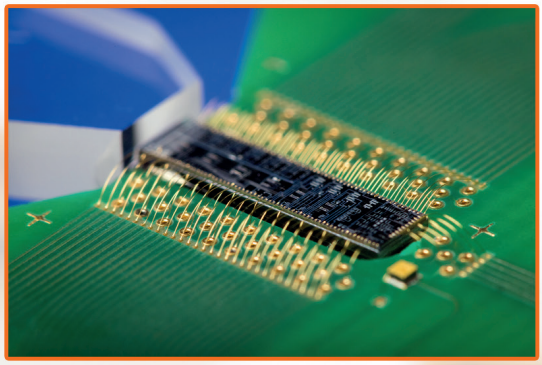
component modelling. Another significant challenge lies in layout generation and verification before tapeout, as designers must ensure that the layout aligns with the targeted performance requirements. When it comes to addressing challenges around finalising the layout for tapeout, Ansys Lumerical's multiplatform layout solutions include automated workflows that seamlessly enable the transfer of geometry information from various layout tools, including Cadence Virtuoso Layout Suite and KLayout, to and from Ansys Lumerical's suite of tools.

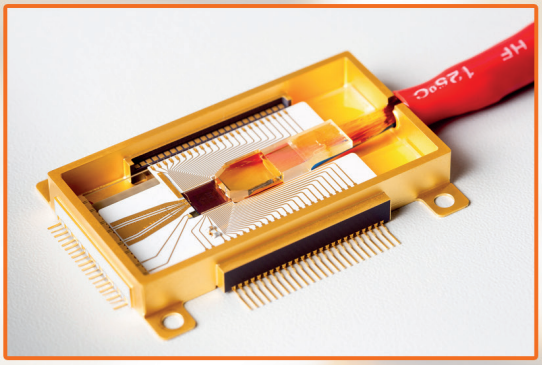
Summary and outlook

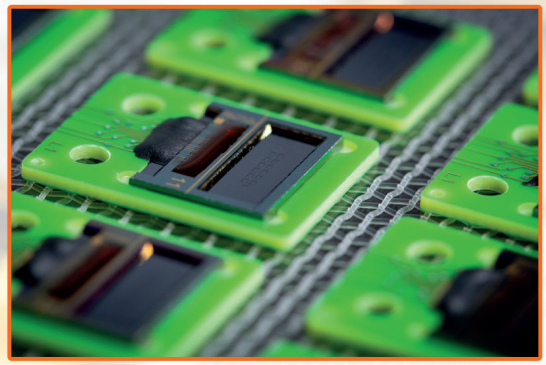
Ansys has partnered with multiple EDA vendors and foundries to enable the next generation of scalable photonic systems, offering multiplatform solutions for the co-design and co-simulation of EICs and PICs with photonic Verilog-A and INTERCONNECT models, and design workflows including schematic driven layout (SDL) and layout versus schematic (LVS). Introducing a consistent design tool chain facilitates the creation of foundry-compatible customised designs and automated generation of photonic compact model libraries in a streamlined manner across multiple system design platforms. We underscore the significance of EPDA- and foundry-compatible PDK-driven design in meeting the evolving demands of the photonic industry.

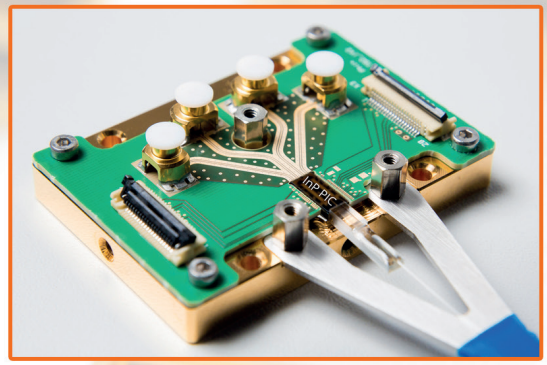
The component-level design process reported above can further leverage methods such as AI-powered parametric optimisation or photonic inverse design optimisation, and effortlessly scale design space exploration and tolerancing on HPC and cloud applications. Additionally, integrating Ansys Lumerical with the Ansys Optics, Electronics, Mechanical, and Semiconductor tools offers a route to tackling challenges such as thermal management, optical I/O, RF and signal integrity analysis for technologies such as co-packaged optics design.

Get your PICs packaged in scalable volumes









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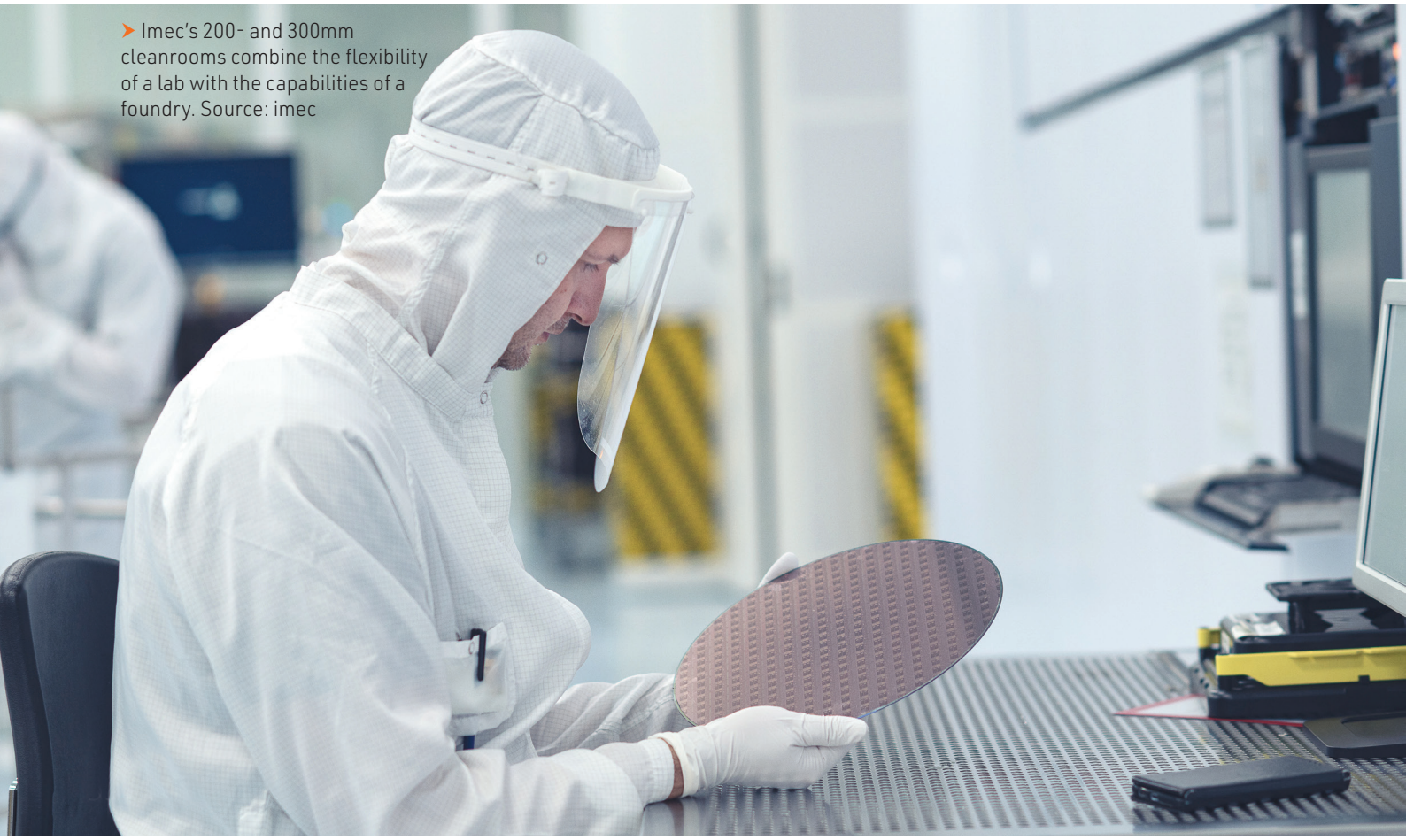


Imec's 200- and 300mm cleanrooms combine the flexibility of a lab with the capabilities of a foundry. Source: imec

A toolbox for photonic quantum computing

A mature integrated photonics platform is essential for building scalable photonic quantum devices. Quantum pioneers can access it by partnering with imec as a technology provider with a flexible CMOS fab.

BY AMIN ABBASI, SENIOR BUSINESS DEVELOPMENT MANAGER, IMEC

WILL WE HAVE a quantum computer one day? There has been a tremendous amount of progress over the last few years – with breakthroughs that were destined to make media headlines. Nevertheless, you'd be hard-pressed to find a quantum expert who's prepared to give you a 100 percent guarantee that practical quantum computing is already on the horizon.

The main hurdle is scalability. Although physical qubits are essential building blocks of future quantum computers, obtaining them is, more or less, the 'easy' part. The more significant challenge is making the necessary connections between thousands or even millions of them. That's why, in the debate on the preferred method for producing physical qubits, scalability is quickly becoming a decisive argument. It also goes a long way towards explaining why photonics-based quantum computing – a relative newcomer compared with well-established contenders such as superconducting- and semiconductor-based quantum computing – has been attracting much attention lately.

In this article, we look at what makes photonics such a promising match for quantum computing, and we'll enumerate the existing challenges and how they can be addressed. We also want to highlight imec's role, not only as an application company for quantum computing using integrated photonics, but also as a technology provider to its valued customers.

Harnessing the unshakeable power of photons

Qubits are the primary carriers of information in a quantum computer. In contrast with bits in classical

computing, which are constrained to ones or zeros, qubits can be in multiple states simultaneously (ones, zeros and combinations of ones and zeros). String them together, and they contain amounts of information that scale exponentially to astronomical proportions.

Despite this superpower, qubits in their physical form are incredibly delicate. Their decoherence time is very short, meaning that, when you put them in a quantum state, they quickly lose it again. This makes it difficult to do computation, and it can only be counteracted by cooling them to cryogenic temperatures, preventing interactions with their environment. That's why the quantum computer prototypes we know so well are surrounded by a roomful of cooling infrastructure, and it partly explains why the scaling challenge is so huge.

There are, however, certain kinds of qubits, such as physical qubits based on near-infrared optical photons, that are less dependent on cryogenic cooling to tens of millikelvins. This is because the energy of optical photons (~ 1 eV) is orders of magnitude larger than the thermal noise at room temperature (~23 meV).

Once you put these photons in a quantum state, they maintain it as long as they can travel freely, potentially making a room-temperature quantum computer more than just a fantasy. But before we can make it a reality, there are plenty of challenges left to solve.

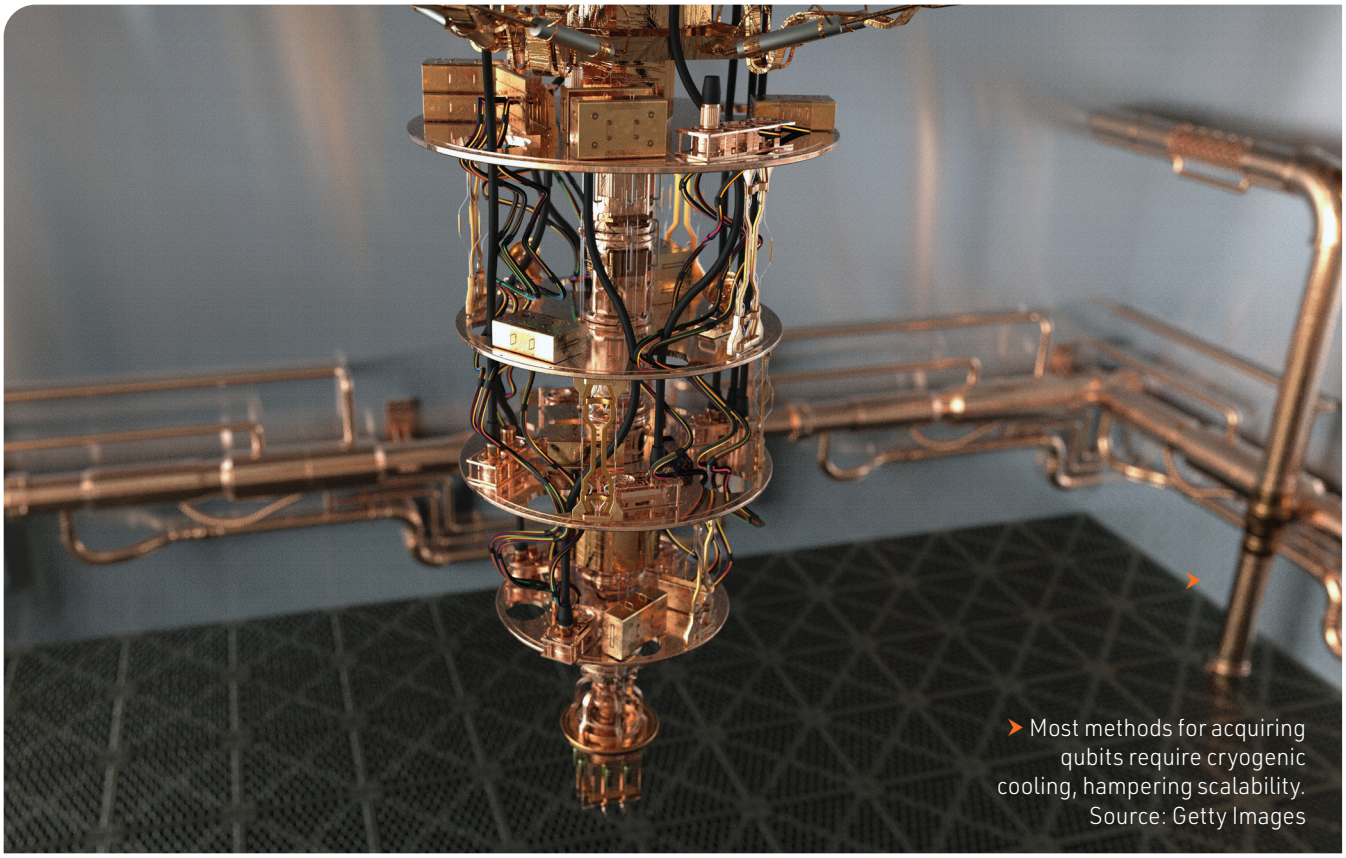
Every photon counts, so count every photon

What is the basic layout of a photonics-based quantum computer? An ideal light source produces single photons – a considerable challenge in itself. Then, linear optical elements such as beam splitters and phase shifters implement qubits and logic gates. Finally, photodetectors read out the final states by measuring the arrival of single photons.

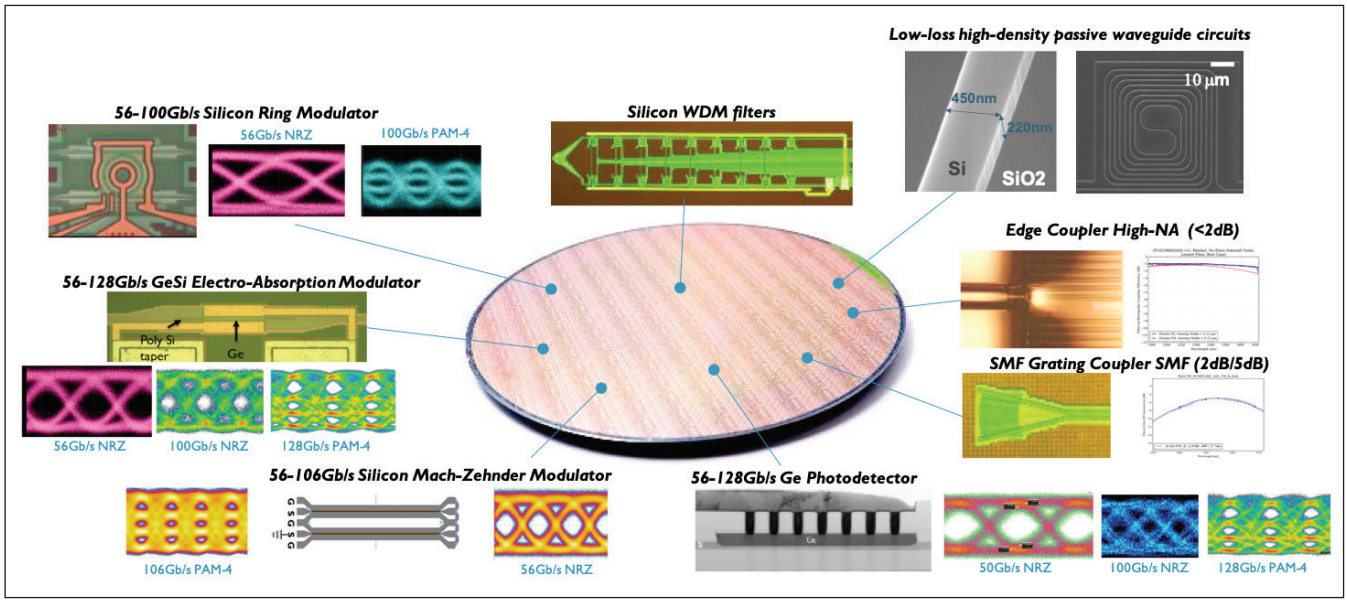
Such a system has been set up in free space for lab demonstration purposes, producing a handful of qubits. But setups like this have zero scaling potential. A true photonics-based quantum computer with thousands or even millions of qubits can only be achieved by bringing all components onto a highly integrated on-chip platform.

The good news is that quantum computing development can plug into a rapidly growing silicon photonics ecosystem that leverages the mature semiconductor manufacturing infrastructure to make photonic structures – from waveguides to phase shifters – on silicon chips. This considerably lowers the barrier for pioneering companies in the quantum photonics domain, as they don't need to start from a blank slate but can at least partly use existing modules.

Still, photonics for quantum is a different game than photonics for existing applications like telecommunications. By far the biggest challenge when designing photonic circuits for quantum is controlling loss; in the quantum space, every single



Most methods for acquiring qubits require cryogenic cooling, hampering scalability. Source: Getty Images



➤ Overview of imec's silicon photonics platform. Source: imec

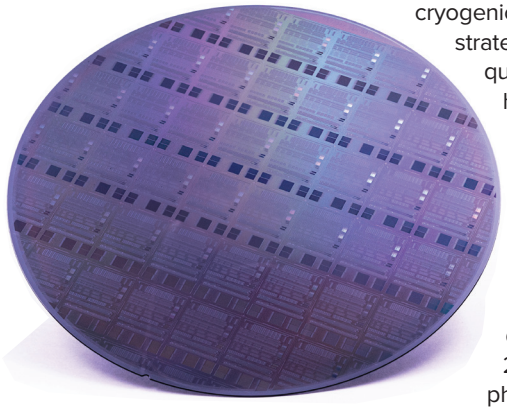
photon is a vessel for information that should not be lost. Imagine such a photon traveling through centimetres or even metres of waveguide with a propagation loss of 2 or 3 dB per centimetre. The chances are that it will not arrive at the end and will not get measured.

On top of this propagation loss, coupling loss is an equally pressing issue. Making a quantum computer with thousands or millions of qubits will require dozens of chips to be connected. The signal integrity at these interconnections has to be guaranteed for photonic quantum computing to stand a chance.

Such ultra-low-loss structures are not feasible using silicon photonics alone. Other materials, such as silicon nitride (SiN), will be needed – preferably while retaining tight integration with a silicon platform that is still required for other components, such as the driving electronics.

Bridging the gap between lab and fab

As a leading semiconductor R&D hub, imec took an early interest in quantum computing. We're conducting research into promising options for the development of physical qubits, such as spin qubits and superconducting qubits, as well as cryogenic 3D integration. Our strategy towards photonic quantum computing, however, is somewhat different.



➤ 200 mm SiN wafer processed at imec. Source: imec

While we are pursuing some fundamental research in the photonic quantum domain – such as 2D-based single photon emitters (with Ghent University and MIT) – we mainly aim to advance the field by sharing our infrastructure and expertise with our partners from the industry. The reason for this approach is that we see many companies, especially start-ups and scale-ups, struggling to bridge the divide between their idea or concept – even a first lab-developed prototype – and commercialisation.

We can consider that divide as stemming from the difference between an academic lab and a commercial foundry. University labs are where most start-ups originate. They offer the flexibility to explore different concepts and produce creative solutions. However, they lack advanced capabilities – including industry-grade tools – that allow the development of a manufacturable prototype, which is needed to convince investors once you want to scale up.

However, when companies turn to foundries to manufacture such a prototype or do a low-volume run, they often come up against a brick wall. Very few foundries have the flexibility to take on such small projects, being booked to the brim with profitable high-volume runs.

As a semiconductor R&D centre with strong ties to the industry, imec can bridge that gap by combining the flexibility of a lab with the capabilities of a foundry. In our 200 mm and 300 mm cleanrooms, partners can develop a process or a prototype that's guaranteed to be compatible with the standard industry tools. We can even handle low-volume runs of their product – up to a few hundred wafers per year – or transfer the technology to a customer-preferred CMOS foundry for high-volume production.

Considering the importance of scalability when it comes to quantum, that's a significant advantage for aspiring companies. One such company is Xanadu,

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Contact us at: www.photondelta.com/contact

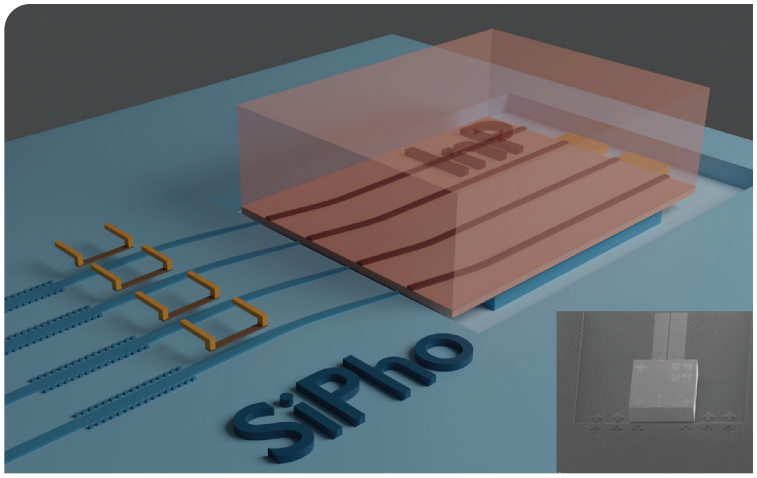
Our silicon nitride platform is ideal for non-communication applications such as sensing, biophotonics, and metrology. But silicon nitride also holds critical benefits for the development of quantum applications

which partnered with imec to develop photonic chips for fault-tolerant quantum computing. In the words of Zachary Vernon, head of Xanadu's hardware team, "one of the most critical challenges in building a photonic quantum computer is finding the right fabrication partner that can simultaneously deliver innovative process development and volume production of high-performing photonic chips. Imec is one of the few semiconductor R&D centres that does advanced technology R&D on advanced 200 mm and 300 mm lines, as well as volume manufacturing on their 200 mm line. The seamless transfer offered by imec of new processes to production is especially critical for the rapid scaling of our technology."

Photonic quantum computing toolbox

Let's now look at the toolbox that imec offers partners that want to push the boundaries of photonic quantum computing. The ultimate goal is clear: combine all quantum computing functions (sources, circuits and detectors) on one photonic integrated circuit, overcoming specific challenges, such as the need for ultra-low loss.

To reach this goal, we leverage our mature and versatile integrated photonics platform. We perform customisations and add new modules to meet our partners' needs. Imec has two integrated photonics platforms: silicon photonics, based on silicon-on-insulator (SOI), and silicon nitride photonics, based on thin-film SiN. Our silicon platform contains many high-speed active and passive modules. It's mainly geared towards datacom and telecom applications, but it also includes basic building blocks for quantum, such as a PIC-based quantum engine, high Q-ring resonators, and edge couplers.



➤ Artist's impression of an external-cavity diode laser (ECDL) array. Inset: scanning electron microscope (SEM) picture of a bonded DFB laser. Source: imec

Meanwhile, our silicon nitride platform is ideal for non-communication applications such as sensing, biophotonics, and metrology. But silicon nitride also holds critical benefits for the development of quantum applications. In particular, its extremely low propagation loss (0.2 dB/cm down to a couple of dB/m) and its high tolerance for thermal variations of the environment make it a good candidate for quantum.

Finally, multiple other materials with wide index variations can be integrated, such as titanium oxide, niobium oxide, aluminium oxide, and silicon oxide. Different substrates are also possible, such as doped glass and quartz.

This portfolio allows us to build solutions tailored to our partners' needs. New modules are constantly being developed, such as novel electro-optical modular integration, wafer-to-wafer bonding, and wafer-scale laser integration through an RSO/DFB flip-chip process.

Conclusion: a shortcut from idea to manufacturable quantum device

In the race towards a practical quantum computer, photonic quantum computing is a strong contender. Its presumed ability to function at room temperature makes the crucial issue of scaling somewhat easier. However, the challenge remains formidable, with the need to achieve ultra-low propagation loss and coupling loss as one of the main hurdles to overcome.

The good news is that years of experience with integrated photonics have resulted in mature platforms that support a lot of the building blocks needed for photonic quantum computing. What's more, these platforms leverage the existing mass manufacturing tools of the semiconductor industry, which ensures an effortless route to further scaling once the initial R&D obstacles are solved.

Due to its unique position in the semiconductor ecosystem, between academia and industry, imec can offer photonic quantum computing companies a flexible environment to do initial R&D and the opportunity to develop their solutions using industry-grade tools. That allows them to take a shortcut from concept to manufacturable device, inching us closer to a technology that promises to crack some of humankind's biggest problems.

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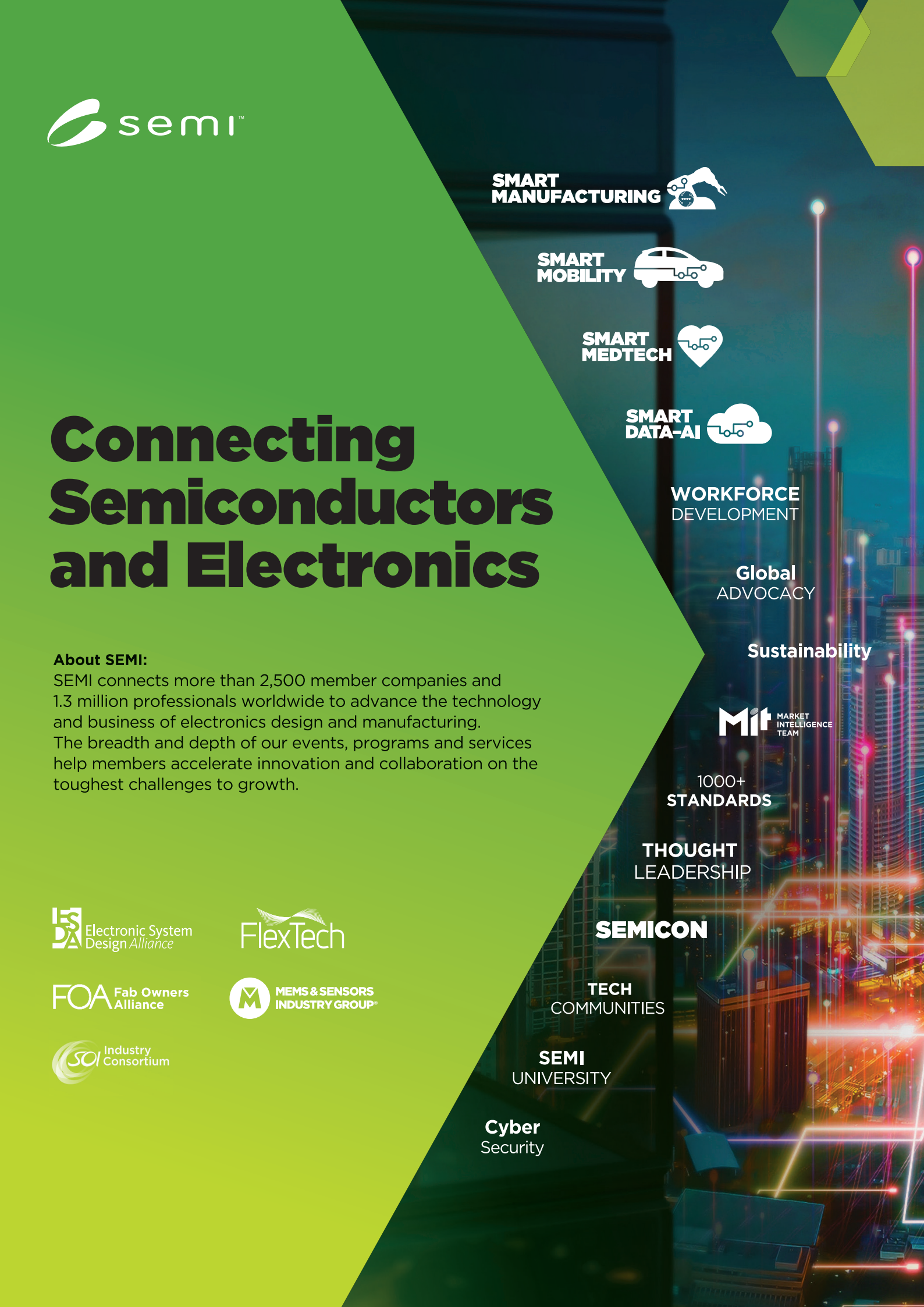


Supercharging PICs with advanced design

Design tools that combine flexibility and precision can speed up design cycles and reduce the number of iterations needed, accelerating PIC technologies to market.

BY MARTIN FIERS AND CHIARA ALESSANDRI FROM LUCEDA PHOTONICS

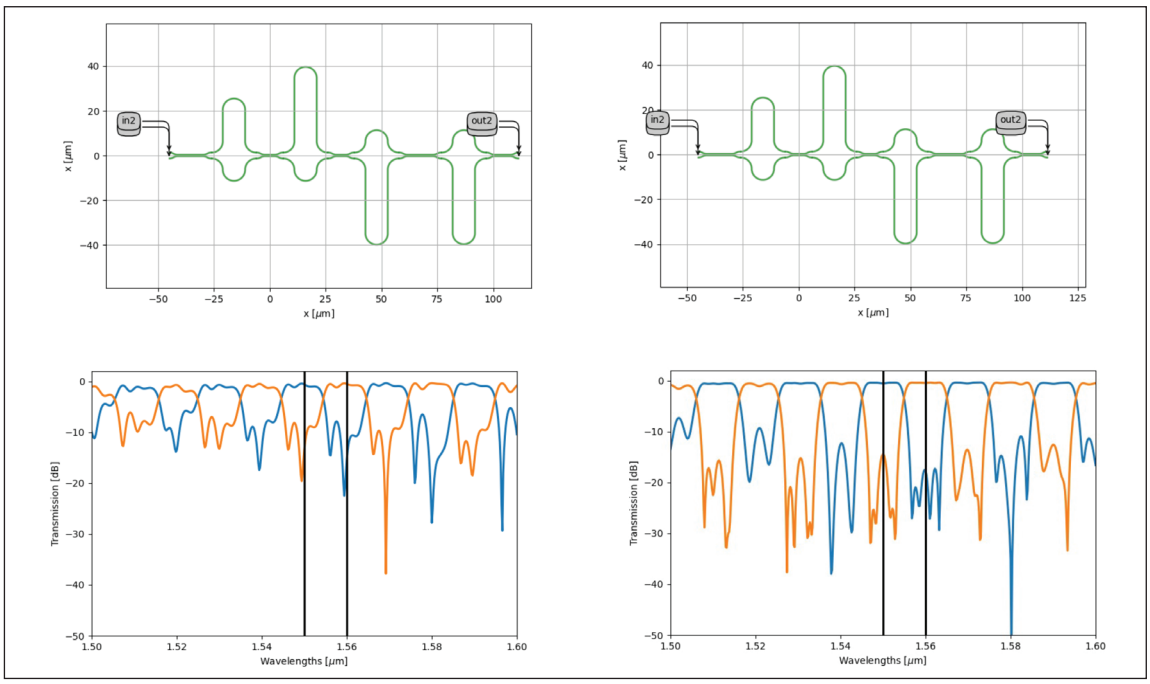
WHEN A PHOTONIC CIRCUIT DESIGNER sends a drawing to a foundry, they are making a significant commitment. Depending on various factors, such as the volume and whether the wafer run is shared or dedicated, they will typically have to pay somewhere between €10,000 - €1 million and wait 4-9 months to get the manufactured circuit back. If they find there is an error in the prototype, then it will be an extremely expensive one; they will have to correct their design and go through another iteration, incurring the same cost in time and money again.

And beyond the expense to the company, there is a broader cost to the PIC industry and society as a whole. From photonic biosensors for diagnostics to LiDAR for autonomous vehicles, we know that PICs could be instrumental in achieving multiple exciting technologies, with the potential to transform healthcare, transport, computing and more. Anything we can do to reduce the time to market brings us closer to realising these benefits in people's daily lives.

But these circuits are highly complicated devices, requiring extremely precise design and fabrication – even a seemingly tiny error in a circuit's physical layout can have a decisive impact on how the chip functions. To illustrate this point, Figure 1 shows an example of two real designs for a PIC wavelength demultiplexer. The designer initially sent the one on the left to the foundry, but when he received the chip back, he discovered its performance was significantly poorer than he expected.

It turned out that one of the waveguides in the drawing is just fractionally – about 200 nm – too long, and this is enough to lead to an extra π phase shift that significantly impairs the circuit's ability to separate the frequencies. The design on the right is correct and performs much better. Yet, to the human eye, they appear identical. This is just one example, but there are many different types of errors that are hard to spot, even after a careful design process.

So, rather than asking designers to pore even more painstakingly over the drawings, we could instead create tools that are specifically designed to make it much easier to generate the correct layouts, and which flag errors that have cropped up as automatically as possible. This is where the Luceda Photonics Design Platform comes in. With its flagship product IPKISS, the platform supports designers throughout the whole design flow, from the initial ideation phase, through component and circuit design, to functional validation and tape-out preparation.



➤ Figure 1. The two PICs might appear identical, but the one waveguide in the one on the left is about 200 nm too long. This significantly impairs its performance as a wavelength demultiplexer.

Flexible component design

We often draw comparisons between electronic circuits and photonic circuits, but, when it comes to design, there are some important differences. In electronics, designers can usually work with a set of standardised building blocks: transistors, resistors, and capacitors. In photonics, on the other hand, there is a much larger number of possible components – and more variations of each component – that designers can choose from.

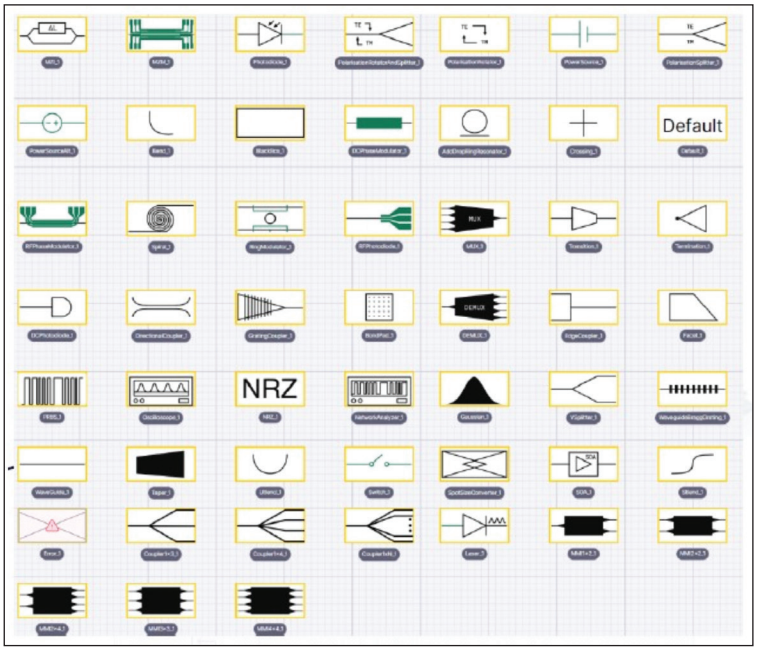
IPKISS has a library of many of the most commonly used elements for designers to quickly add to their circuits, some of which are shown in Figure 2. However, many PIC designers need to create custom components specifically tailored to their technology and use case. IPKISS therefore uses a flexible code-based approach, based on the Python programming language, which is more expressive than a graphical user interface. With IPKISS, designers create PIC devices and circuits by writing IPKISS code based on Python, from which the software can generate the layout. In addition, their custom building blocks become reusable IP blocks, that can be employed throughout the lifecycle of the product, or even be applied to different products and projects.

A major advantage of using Python in particular is that it has become widely adopted as the standard programming language in many science and engineering disciplines, and is being taught as part of many technical degrees. PIC designers are therefore likely to already have the coding knowledge needed, making it maximally accessible and convenient. It also comes with many libraries for visualisation, analysis, and integration.

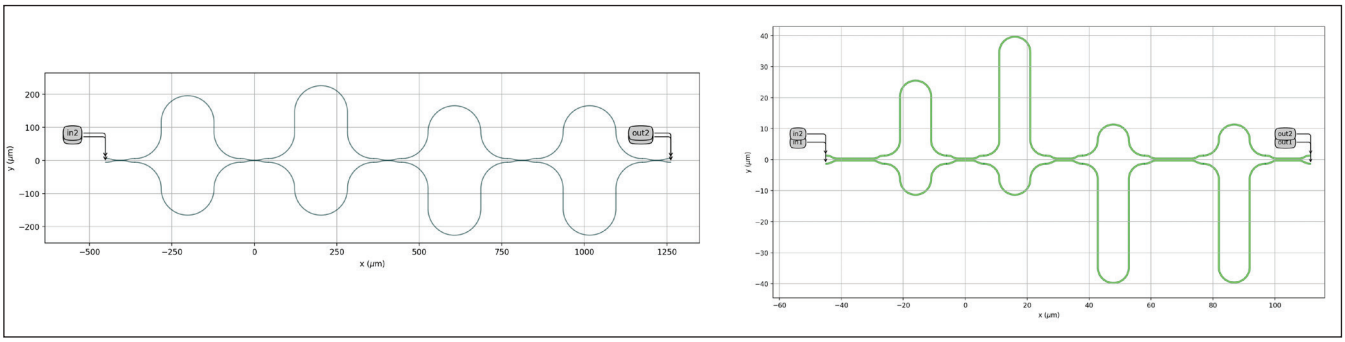
Additionally, Python is a superb language to automate the design flow, offering the possibility of fine-tuning and adjusting the code to each organisation's unique requirements, as well as giving the user control over the tiny details that can make or break a photonic device or circuit.

Precise circuit design

While offering a high level of flexibility, the code-based approach makes no sacrifices in terms of precision. Designers have full control over all aspects of the layout; they can specify exact quantities for various parameters within the Python script, and can also add formulas for many key characteristics of the circuit.



➤ Figure 2. IPKISS has a library of common PIC components. Users can also write code for custom components, which then become reusable IP blocks.



➤ Figure 3. PICs made in different materials will also need to have a different physical structure if they are to perform the same function. The circuit on the left is in SiN with a bend radius of 80 µm. The circuit on the right is in silicon with a bend radius of 5 µm.

Going back to the example of the error in the demultiplexer PIC, a designer could use IPKISS to avoid such a mistake by specifying in the code exactly how long each waveguide should be. The software can then create the correct waveguide layout and verify it afterwards.

If a designer wants a property, such as the Free Spectral Range (FSR), to have a specific value, they can add a formula to extract the correct layout parameters based on this property's value. Executing the IPKISS code will then generate an adjusted layout to yield the desired result. This avoids the need for designers to redo calculations, thereby reducing errors, and enabling them to quickly and conveniently adjust key characteristics if they need to .

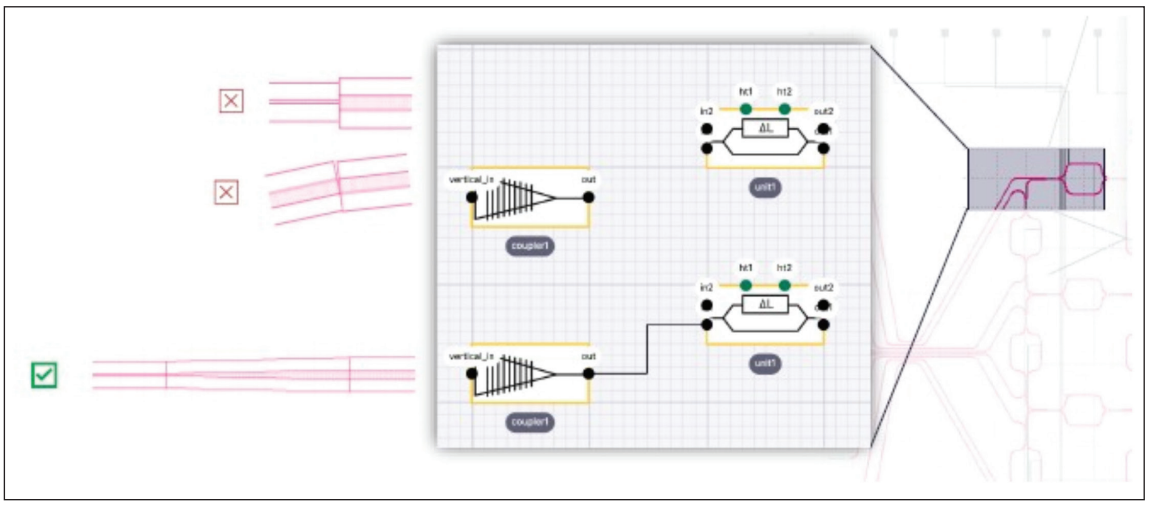
Another challenge that PIC designers face is that the correct drawing for a particular chip differs depending on the fabrication material and manufacturing methods of the specific foundry they are sending it to. For instance, the refractive index contrast is different for silicon (Si) than it is for silicon nitride SiN – two common PIC materials.

This means that, to manipulate light in the same way and get the same effect from chips made in these two materials, the physical size and structure of the circuits will in fact need to be different, as shown in Figure 3. To make it as quick and easy as possible for designers to navigate this, Luceda Photonics collaborates with multiple foundries to provide designers with the necessary design rules, geometries and building blocks associated with each one. Within the software, once a designer has the base code for their chip, they need only import the correct foundry and run the IPKISS script to generate the appropriate drawing.

An added benefit of this code-based approach to PIC design is that fabless companies have more flexibility about which foundry they work with, so they can compare the different technologies available and see which one fits their application best. Being able to easily switch between foundries also reduces supply chain risks, compared with relying on just one provider.

Simulation and functional verification with IPKISS Canvas

While the features described so far can help designers from the start of the design process, these circuits are incredibly detailed, so the layouts need to undergo a thorough design validation process once they have been generated. IPKISS can help at this stage too, with a feature, graphical user interface (GUI) called IPKISS Canvas, which generates schematic diagrams from a designer's Python script. These schematics are abstract



➤ Figure 4. IPKISS Canvas generates schematics that makes some common errors more visible. For example, the schematics here show whether there is a break or abrupt change in a waveguide – something which is difficult to spot by looking at the small segment of the layout on the right.

PIC ROUNDTABLE

Connecting The Photonic Integrated Circuits Community

Not every discussion is a **heated debate...**

- Based around a hot topic for your company, this 60-minute recorded, moderated ZOOM roundtable would be a platform for debate and discussion
- Moderated by an editor, Laura Hiscott, this can include 3 speakers
- Questions prepared and shared in advance
- There would be an opportunity to view and edit in advance

This event would be publicised for 4 weeks through all our mediums including:

- A banner on the PIC Magazine homepage for 8 weeks
- 4x weekly dedicated HTMLs
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- All registered attendees' details would be made available to you

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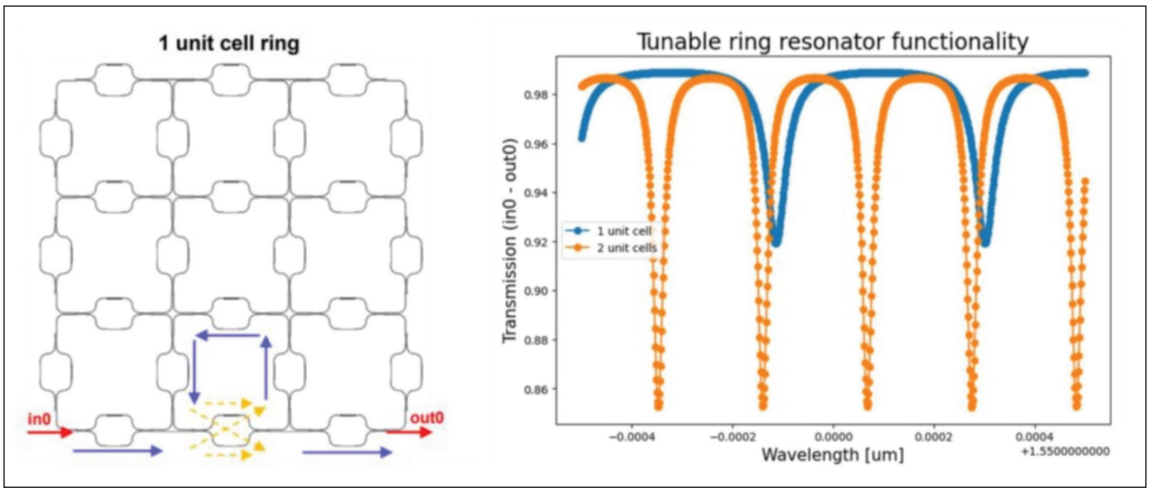
Contact: Jackie Cannon at jackie.cannon@angelbc.com

ANGEL EVENTS



➤ Figure 5. IPKISS can run simulations of how a circuit will perform after it has been physically implemented in the layout, indicating to designers whether the layout might need correcting.

representations that visualise the components in the circuit and how they are connected, making several types of errors much easier to catch.

For example, if there are any abrupt changes in the size of a waveguide in the circuit, or any breaks in its continuity, they might be almost invisible in the layout.

However, as shown in the Figure 4, the schematics make them more visible, so designers can spot and correct them without having to zoom in on every tiny part of the drawing. In this way, the schematics can help verify optical connectivity, ensuring smooth, tapered transitions and minimising loss. This feature can also help with checking electrical connectivity, showing where wires cross unintentionally and where they could short the electrical signal.

With IPKISS Canvas, users can annotate any crucial information from the layout on the schematic, such as path lengths of waveguides to compare path length differences. There are often specific requirements to match certain path lengths, and designers need exact control over the delays for light going through devices and circuits that are phase sensitive. These details are also included in the schematics, making it quicker to check whether the delays are what they should be.

> “Another crucial aspect of a PIC that IPKISS Canvas schematics can help designers check is the delay for light travelling along different parts of the circuit, also called path length difference”

Finally, in addition to circuit layouts and schematics, the IPKISS software can also run circuit simulations of how a PIC will function, putting virtual signals into the inputs and calculating the transmission it will produce, in both the frequency and time domain (see Figure 5). With this capability, designers can check that the output is what they are aiming for, flagging that they need to return to the PIC design to identify errors if it is not.

Future PIC design

Luceda’s long-term vision is to give photonics designers the same powers that electronics designers currently enjoy. We want to create a future in which PIC designers can depend on rapid design iterations, requiring only a minimal number of cycles to achieve the final, working device.

There are still challenges to overcome in making that vision a reality. Circuit models need to be standardised and calibrated for different devices, processes, and wavelength ranges, further improving the pre- and post-layout circuit simulations. As we continue to advance the IPKISS software, place and routing will further evolve to speed up the physical implementation, and additional verification at the functional level will give PIC designers more confidence that their intended design is properly captured and translated into the physical implementation.

The latest version of IPKISS is a major step towards the goal of reducing the time to market. By offering designers both flexibility and precision in the design process, and by helping them catch errors with extensive verification features, IPKISS improves designers’ confidence that the circuit they have generated matches the idea they had in mind. In this way, the software reduces the risk involved in sending a circuit off to be manufactured. Ultimately, a faster time to market will be valuable for everyone who can benefit from the applications of this exciting technology.

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ECOC 2023 explores the future of photonics

From artificial intelligence and machine learning to quantum 2.0, focused sessions discussed how PICs can be scaled and evolved to support exciting applications.

BY LAURA HISCOTT, EDITOR, PIC MAGAZINE

PHOTONIC INTEGRATED CIRCUITS were very much on the agenda at the 49th European Conference on Optical Communication (ECOC), which was held in Glasgow from 1-5 October.

On the first morning, a workshop on "Scaling Routes in Silicon Photonics" reflected on the growth that the sector has experienced in recent years, and explored potential strategies for boosting current volumes even further to establish a sustainable ecosystem. Thomas Liljeberg from Intel opened the session with a talk on heterogeneous integration, reporting on Intel's work integrating InP lasers onto silicon platforms.

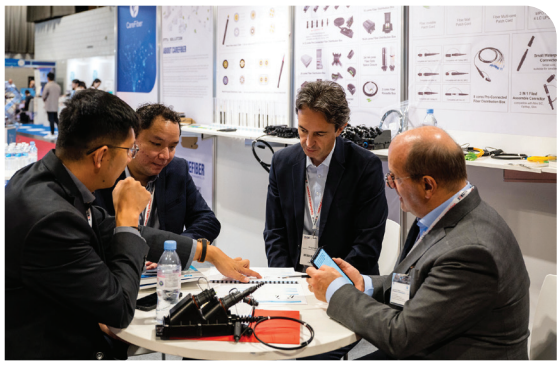

Image credit: Ian Arthur Photography

He emphasized how this can overcome the input/output costs, while taking advantage of the reliability of CMOS manufacturing. Focusing on the data-hungry application of AI, Liljeberg outlined how integrating multiple channels onto a chip can offer higher bandwidth, and how, for reliable fabrication processes, cost per channel drops as the channel number increases.

In the same workshop, Kamil Gradkowski from Tyndall National Institute addressed the need for faster, cheaper packaging processes, highlighting

that, together, assembly, packaging, and alignment can account for up to 80 percent of a device's total cost. To tackle this, he presented recent work on pluggable couplers that are designed with microlenses that can collimate the light between the chip and the fibre, expanding alignment tolerances. These pluggable couplers offer an opportunity for standardisation, since they should be compatible with any photonic chip, provided it has the correct microlenses attached to it. Gradkowski also described collaborative work with the packaging manufacturer ficonTEC, demonstrating that the process of attaching microlenses to a chip can be automated with the company's machines, offering another advantage for scalability.

While PICs are useful in optical communications in general, one session at ECOC focused in on how they could be particularly useful for quantum technologies. Introducing the symposium, "PICs for Quantum," John Marsh from the University of Glasgow spoke about the proposal of a National Institute for Quantum Integration (NiQi), a potential UK-wide programme to accelerate the commercialisation of quantum technology. A trial of the concept – the NiQi Pilot Accelerator – is currently underway in the form of a two-year Glasgow-based initiative that is supported by the Department of Science, Innovation & Technology, Innovate UK, and Glasgow City Region.

Image credit: Ian Arthur Photography

The session went on to cover a wide range of quantum applications of photonics. Andrew McKee from Sivers, a designer and manufacturer of lasers, spoke about the company's collaborative work to apply their technology to atomic clocks, quantum magnetometers, and LiDAR systems. Meanwhile, Jon Heffernan from the University of Sheffield presented developments in the fabrication of quantum dots as single-photon sources for quantum photonic circuits, and Jonathan Silver from NPL discussed how PICs could be used to miniaturise atomic clocks.

Describing why PICs are well suited to quantum applications, Peter Smith from the University of Southampton cited the value of being able to do wavelength conversion and generate entangled pairs of photons. He also highlighted that integration is key, given that quantum technology cannot

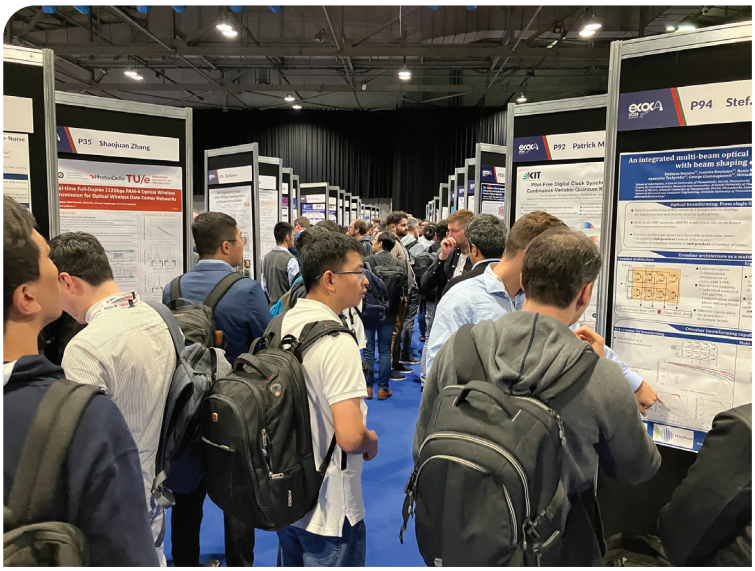

Image credit: Sarah Sennett

tolerate any loss of photons, unlike telecom, which can compensate for insertion loss by amplifying the signal. Smith also spoke about Covesion, a company he co-founded, which makes periodically poled lithium niobate (PPLN). He described how PPLN waveguides can perform efficient wavelength conversion and thus act as a narrow linewidth source of wavelengths corresponding to specific quantum transitions, such as those of rubidium atoms.

An interesting message from Smith's talk was that the community might benefit from being open-minded about the route to fully commercialised quantum applications and how long it might take. Contrasting photos of the Colossus computer, which was built in the 1940s, and the Apple M1 chip, released in 2020, Smith pointed out that it took over 70 years to get from the former to the latter, and that numerous technologies had to be developed to facilitate that transition. "In this quantum space there's a danger of thinking 'we need a mass-market solution now,'" he said, "and that might not be true because these two pictures are 76 years apart."

We don't know how long it will take to realise the promises of the quantum revolution, or all the intermediate technologies we might need to develop along the way, but fundamental research in this space is essential. It will be fascinating to see what progress has been made in a year's time, at ECOC 2024.

Image credit: Ian Arthur Photography

ANGELTECH

PIC INTERNATIONAL CONFERENCE

The 9th PIC International conference aims to connect, educate, and inspire the photonic integrated circuit (PIC) industry. With presentations covering seven sectors, attendees will gain insights into topics like Hybrid PICs: Pioneering New Frontiers in Photonic Integration; PIC Packaging: Securing Optimal Integration and Performance; Quantum Era: Unleashing PICs' Boundless Potential; Rapid Scaling: Foundries Fuelling PICs' Mass Production; Accelerating PIC Adoption in Established Markets; PIC Size and Simulation: Enhancing Design Efficiency, and Power Efficiency: Minimizing Consumption in PICs.

Attendees at this two-day conference will also meet a wide variety of key players within the community, from investors and analysts to fab engineers and managers.

SAVE THE DATE 16-17 APRIL 2024

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