PIC PHOTONIC INTEGRATED CIRCUITS

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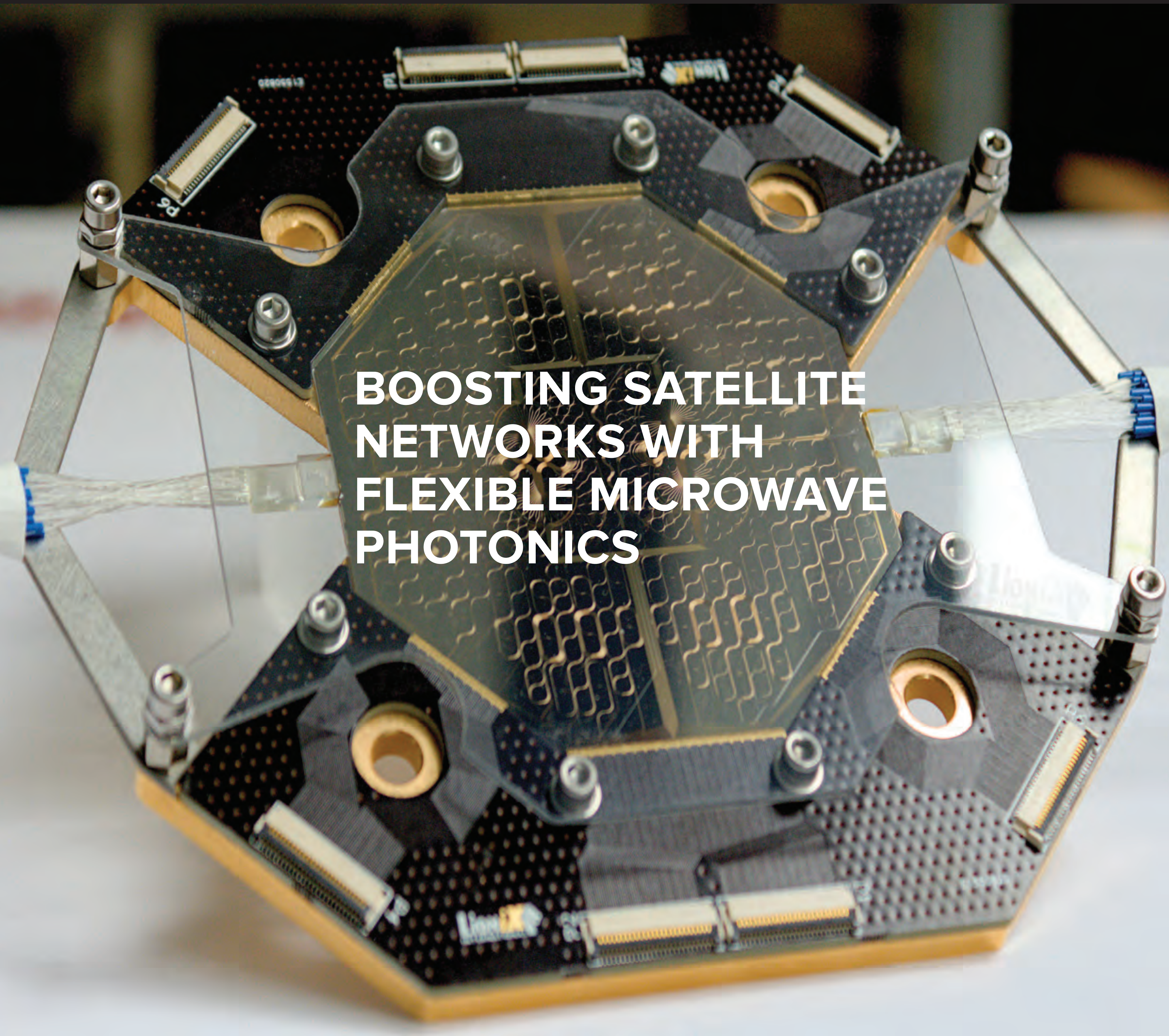

BOOSTING SATELLITE NETWORKS WITH FLEXIBLE MICROWAVE PHOTONICS

ISSUE IV 2024

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

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In the AI arms race between tech giants, there is more than one approach to using optics for efficient datacentres and AI clusters

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VIEWPOINT

By Laura Hiscott, Editor

Mobilising resources to support growth

WHAT CAME FIRST, the chicken or the egg? This well-worn paradox can be applied to any number of scenarios, and the tech sector is no exception. In this case, we might ask: what came first, the product or the funding? It's reasonable that funders will want to see some evidence of a technology's potential before investing in it, but start-up founders might well need funding before they can develop and provide such assurances.

In a plenary session at ECOC this year, PIC pioneer Roel Baets mentioned a striking fact: despite the large number of PIC start-ups pursuing various materials, technologies, and applications, he and his colleagues could only find six non-transceiver PIC products that have so far made it to market.

It's early days for the industry, of course, but Baets pointed out that, for start-ups and scale-ups, there is often a gap between the finances needed for non-recurring engineering (NRE) and the funds available for it. He therefore called for a mobilisation of resources to support PIC development and achieve its potential.

While the diversity of PIC technologies certainly makes it an exciting industry, I wonder whether it can sometimes be a mixed blessing. After all, each material platform needs its own supply chain, and perhaps there is less possibility – at least today – for mixing and matching components across different products. What's more, with a dizzying variety of potential products, who knows which one to back?

Yet these kinds of challenges are nothing new for a nascent industry, and there are plenty of reasons to

be hopeful that the integrated photonics sector will overcome them. Numerous PIC start-ups have secured substantial investments this year, and the Chips Joint Undertaking recently announced it has begun negotiations with a consortium to launch PIXEurope – an advanced PIC pilot line to be established in Europe.

The world is rarely as simple as the phrasing of the chicken-egg question might imply. Life evolved for aeons before the appearance of chickens and their eggs, trying out innovations and seeing which ones worked. Industry, too, charts a more circuitous path, growing step by step, rather than appearing fully formed. It might mean there are challenges on the journey, but it's the only way to beat the paradox.

We might not yet know which PIC products will take off, but hopefully it will be many of them.

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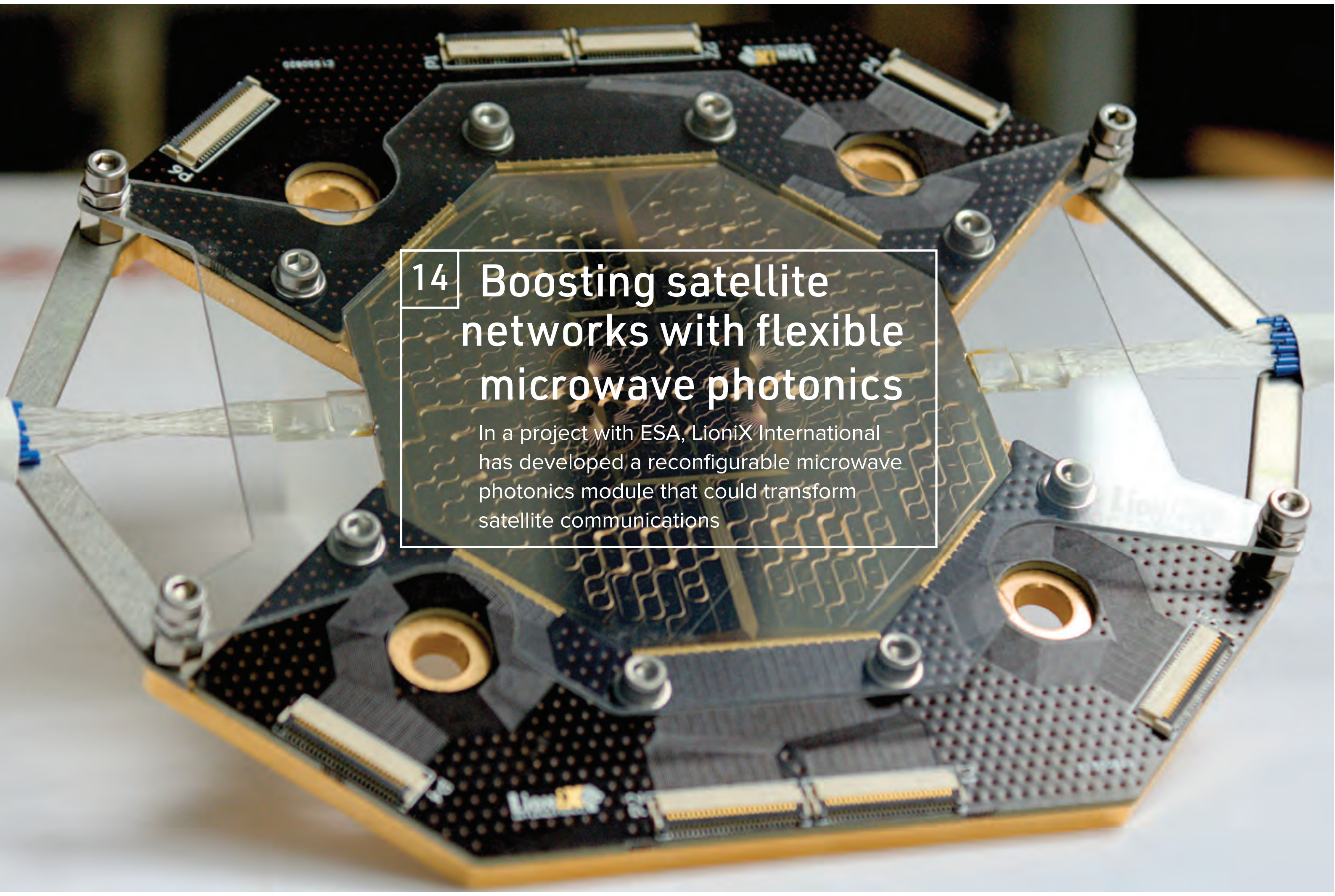

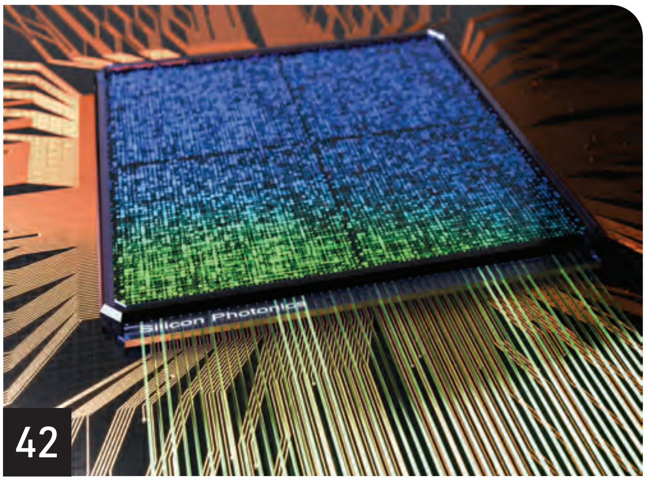

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NEWS

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TELUS and Photonic join forces to advance quantum internet

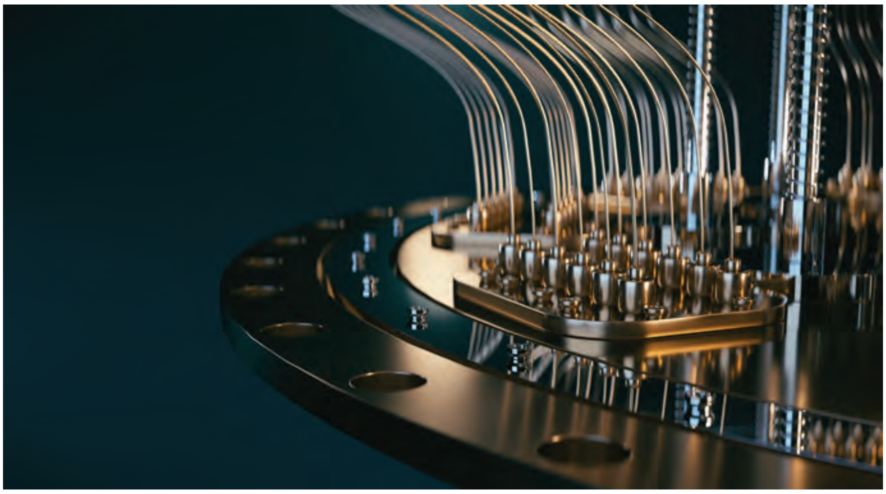
The Canadian communications company will offer the quantum computing start-up access to its PureFibre network to test and accelerate the commercialisation of quantum solutions and to prepare for a quantum-secure future

TELUS and Photonic Inc. have announced that they are collaborating to accelerate the development of next-generation quantum communications in Canada. TELUS will provide Photonic dedicated access to its advanced fibre-optic network, aiming to enable the testing of ground-breaking quantum technologies and emerging solutions that could reshape Canada's digital landscape, improve productivity and drive economic growth.

Over the past several years, quantum technology has moved beyond academic research and is now entering the commercial realm. The two companies say their collaboration provides a path for industries such as finance, security, and logistics to prepare for a quantum-secure future. With TELUS' infrastructure enabling the testing of real-world applications, Photonic aims to accelerate the commercialisation of quantum technologies, set to reshape how industries approach computing and secure communication, both in Canada and worldwide.

As part of this collaboration, TELUS is providing Photonic access to a 30-km dedicated fibre network in British Columbia – which the company says is configured to test increasingly complex quantum networking that leverages quantum encryption for ultra-secure, tamper-evident transfer of information over long distances.

According to Photonic, this infrastructure will enable it to advance critical capabilities in quantum computing, quantum networking, and quantum key distribution (using quantum signals to create secure encryption) – crucial technologies for the future of digital security and innovation.



The companies say this effort marks a major milestone for them both as they work to lay the foundation for a quantum internet. The dedicated fibre network is connected to TELUS' national infrastructure, which it says offers potential for broader, nationwide testing and marking the first time a Canadian start-up has been granted access to a major telecom operator's network for the purpose of developing quantum communication capabilities.

Photonic says this announcement follows milestones it has recently achieved, including a successful demonstration of entanglement distribution between independent systems in a commercial setting, an essential component of scaling quantum networks.

"This collaboration with TELUS allows us to move from the lab into real-world applications, showcasing the compatibility of our technology with existing infrastructure," said Stephanie Simmons, founder and chief quantum officer at Photonic. "It marks a significant step forward in building the foundation for a quantum-ready future that will revolutionise computing and digital communication across Canada and beyond."

Nazim Benhadid, chief technology officer at TELUS, said: "At TELUS we believe quantum computing is the next frontier in digital communications and I'm excited to see breakthroughs and innovations from Photonic. This collaboration is part of our broader commitment to investing in cutting-edge technologies that will support a secure and connected future in Canada. By building the quantum infrastructure today, we are helping unlock economic potential and empower industries to innovate and compete globally."

Quantum technology holds the potential to solve some of the world's most complex computation problems, ranging from materials development to climate-friendly catalyst development. However, it also presents new challenges, including the ability to break existing encryption methods within the next decade. This collaboration between TELUS and Photonic aims to position Canada as a global leader in the quantum race, ensuring everyday Canadians and businesses are prepared for a quantum-secure future.

QCi wins NASA contract for LiDAR to study atmosphere

The integrated photonics company says that the project aims to create quantum sensing solutions that will reduce the cost of LiDAR missions, facilitating a better understanding of the causes of climate change

QUANTUM COMPUTING INC. (QCi), an integrated photonics and quantum optics technology company, has announced that it has been awarded a fifth project from the National Aeronautics and Space Administration (NASA) to develop quantum remote sensing technology that would significantly lower the cost of spaceborne LiDAR imaging and advance scientific understanding of the mechanisms of climate change.

This is a continuation of a long-standing strategic partnership between NASA and QCi aimed at creating a radically different approach to LiDAR technology for atmospheric remote sensing measurements. According to QCi, the proposed approach, which it is currently developing, would significantly lower the cost of LiDAR missions, thereby allowing NASA to undertake more frequent flights to better understand the causes of climate change.

The company says that the recently awarded contract is an important milestone in further assessing the viability of its technology, as well as a pivotal step towards deploying its remote sensing technology on LiDAR flights, and further establishes the applicability of its quantum technology in diverse fields, such as civilian and military surveillance.

"QCi is honoured to support NASA in this critical mission dedicated to advancing remote sensing and climate change monitoring," said William McGann, CEO at QCi.

"This new technology aims to reduce the cost of LiDAR missions from billions to millions and ultimately will help us in understanding the root causes of climate change and contribute to NASA's efforts to protect the earth's environment. This partnership reinforces QCi's commitment to providing innovative, cost-effective solutions for various remote sensing applications and highlights the transformative potential of QCi's quantum remote sensing technology for climate research and environmental management strategies."

The company added that the contract announced today builds upon its work helping NASA denoise the sunlight in satellite LiDAR images by using QCi's latest entropy quantum optimisation machine, the Dirac-3, to simulate the background noise and turn the denoising problem into an optimisation problem.

Infinera to receive up to $93 million CHIPS Act funding

INFINERA and the U.S. Department of Commerce have signed a non-binding preliminary memorandum of terms for Infinera to receive up to $93 million in direct funding as part of the bipartisan CHIPS and Science Act. This proposed direct funding, when combined with investment tax credits available under the CHIPS and Science Act, could result in more than $200 million in total federal incentives as well as potential state and local incentives.

According to Infinera, this proposed funding would support the expansion and modernisation of both its semiconductor capabilities in Silicon Valley, California and its advanced test and packaging capabilities in Lehigh Valley, Pennsylvania, increasing the company's existing domestic manufacturing capacity by an estimated factor of ten. The company adds that combined proposed funding for these two projects could create up to 1,700 manufacturing and construction jobs while strengthening America's supply chain, economic, and national security.

"We are grateful for the bipartisan efforts under the CHIPS and Science Act to increase semiconductor fabrication and packaging in the U.S. and protect our national and economic security," said David Heard, Infinera CEO.

"The proposed CHIPS funding will enable us to better secure our supply chain and compete more effectively with foreign adversary nations. Our unique photonic semiconductors address the increased demand for bandwidth from consumers while opening new markets inside the datacentre driven by the explosive growth in AI workloads."

Celestial AI acquires Rockley Photonics IP

The company says that the silicon photonics IP aligns with its core technology roadmap and enhances its strategy for deployment and commercialisation of its Photonic Fabric platform

CELESTIAL AI has announced its acquisition of silicon photonics intellectual property from Rockley Photonics, including worldwide issued and pending patents. The company says that the combination of its own IP with that of Rockley results in one of the strongest IP portfolios in the field of silicon photonics for optical compute interconnect, bringing their total IP portfolio to more than 200 patents globally. The acquired patent portfolio is comprised of three main technology categories including optoelectronic systems-in-package, electro-absorption modulators (EAMs) and optical switch technology, relevant for multiple AI datacentre infrastructure applications.

Celestial AI is focused on delivering solutions to hyperscale datacentre customers, both directly and through their ecosystem partners, that enable transformational performance, scalability, and energy efficiency advantages at the forefront of next-generation AI compute and network connectivity.

Rockley has foundational IP in silicon photonics that dates back to 2014, predating the foundation of many market competitors. Celestial AI says the acquired IP directly aligns with its core technology roadmap and enhances the deployment and commercialisation strategy of the company's Photonic Fabric technology platform.

The company adds that this IP complements its existing portfolio, which it says has rapidly evolved into the industry-leading technology platform for optical interconnectivity.

"The addition of Rockley's IP into our technology platform further accelerates the growth of Celestial AI's highly valuable intellectual property portfolio and amplifies the strength of our position," said Dave Lazovsky, founder and CEO of Celestial AI. "These patents fit well into our expanding Photonic Fabric patent portfolio spanning advanced packaging, thermally stable silicon photonics, and system architectures for optical compute interconnect. This acquisition reflects Celestial AI's commitment to protecting Photonic Fabric-based solutions that are being implemented in our customers' AI datacentre infrastructure."

QLASS consortium wins €6 million for glass-based quantum PICs

THE QLASS project, which focuses on advancing Quantum Photonic Integrated Circuits (QPICs), has secured €6 million in funding from the European Commission. The initiative is led by a consortium coordinated by Politecnico di Milano, and includes the following partners: CNRS-Institut Charles Gerhardt Montpellier, Ephos, Fondazione Politecnico di Milano, Pixel Photonics, Quantum Lab in Sapienza Università di Roma, Schott AG, Unitary Fund France, and Université de Montpellier.

QPICs are specialised devices that leverage the properties of light and quantum mechanics to execute complex tasks in fields such as quantum computing, communication, and sensing.

By integrating multiple photonic components, such as waveguides, beam splitters and detectors, onto a single chip, QPICs offer a scalable solution for manipulating quantum states of light with high precision. These circuits hold the potential to significantly reduce the size, cost, and complexity of quantum systems, paving the way for real-world applications.

However, the development of QPICs is currently limited by challenges such as photon loss, scalability issues, fabrication complexity, and imperfect photon sources. The QLASS project aims to tackle these challenges head-on. To address the limitations of current QPIC technology, QLASS plans to employ femtosecond laser writing to fabricate 3D waveguides within glass specifically developed for optimal photonic performance, significantly reducing losses.

Additionally, the project intends to incorporate high-performance single-photon sources, superconducting nanowire single-photon detectors (SNSPDs), and advanced electronics capable of programming the whole system. Lastly, the team says they will develop software to compile quantum programmes onto the special QPIC processors.

A principal use case of the QLASS project is modelling complex systems and materials. According to QLASS, the project will pave the way to the design of new materials and technologies for lithium-ion batteries, aiming to improve their capacity, efficiency, and cyclability, which are crucial in meeting the European Union's technological and sustainability goals.

The project also aims to bring significant advancements to the development of QPIC technology and contribute to progress in glass development and novel SNSPD processes. It is hoped that these breakthroughs will benefit the broader quantum technology community and enable new quantum devices with performance levels far beyond the current platforms.

Lightmatter raises $400 million funding for datacentre photonics

The company plans to use the investment to prepare its product, Passage, which it describes as the first photonic engine to deliver I/O in 3D, for mass deployment in datacentres, enabling the scaling required for AI

The photonic supercomputing company Lightmatter has announced it has raised a $400 million Series D, valuing the company at $4.4 billion and bringing the total capital raised to date to $850 million. The round was led by new investors advised by T. Rowe Price Associates, Inc. with participation from existing investors, including Fidelity Management & Research Company and Google Ventures. With this financing, Lightmatter plans to ready its photonic engine, Passage, for mass deployment in partner datacentres, to enable the scaling required for sustained AI innovation.

"We're not just advancing AI infrastructure – we're reinventing it," said Lightmatter co-founder and CEO Nick Harris. "With Passage, the world's fastest photonic engine, we're setting a new standard for performance and breaking through the barriers that limit AI computing. This funding accelerates our ability to scale, delivering the supercomputers of tomorrow today."

As frontier AI models expand and training clusters surpass 100,000 XPUs, traditional electronic interconnects are becoming a critical bottleneck. These interconnects can't keep pace with the growing need for high-bandwidth, low-latency data movement, which is crucial for scaling AI workloads. Lightmatter says its Passage technology addresses this challenge by leveraging 3D-stacked photonic chips to move data. According to the company, this development dramatically increases AI cluster bandwidth and performance, while reducing power consumption.

Lightmatter describes Passage as the first photonic engine to deliver I/O in 3D, and says it frees XPU shoreline to support more memory, addressing another critical bottleneck for scaling AI performance. By transforming data movement across AI clusters, Lightmatter says it enables systems to scale efficiently, unlocking new levels of performance and preparing computing infrastructure for the demands of next-generation AI models.

"Lightmatter has the technology, leadership, and team to bring the industry the future of computing through photonics," said Tony Wang, portfolio manager of the T. Rowe Price Science & Technology Fund. "The demand for AI supercomputers that will power the next wave of frontier AI models is strong and growing. We're pleased to back Lightmatter on their mission to help power AI infrastructure."

IonQ and imec partner on quantum computing

THE COLLABORATION aims to develop integrated photonics systems to reduce the size and cost of quantum computing devices while increasing qubit count, reliability, and capabilities

Quantum computing company IonQ has announced that it is developing PICs and chip-scale ion trap technology for trapped ion quantum computing in partnership with R&D centre imec. By optimising the design, production, and integration of chip-scale photonic devices and ion traps for scalable and high-performance quantum computers, the developments aim to push the boundaries of quantum computing performance.

Traditional trapped ion quantum computing approaches rely on bulk optics for laser light modulation, delivery, and photon collection. By moving traditional bulk optical components into integrated photonic devices, IonQ aims to reduce overall hardware system size and cost, increase qubit count, and improve system performance and robustness. The company hopes that its tight integration with imec's trap manufacturing and packing will increase reliability, drive down cost and reduce time to market for new generations of quantum computers.

"Adding imec to IonQ's set of fabrication and technology partners will have a profound impact on our ability to increase the computational power of our quantum computers through the co-development of compact, high-performance electro-optical systems," said Dean Kassmann, IonQ's SVP of engineering and technology. "This partnership marks a significant milestone in IonQ's path to achieving commercial quantum advantage, demonstrating our commitment to combining technical performance improvements with scalability and enterprise-grade solutions."

Since 2021, IonQ and imec have worked to prototype and refine photonic and ion trap technologies critical to IonQ's quantum computing roadmap. This expanded engagement aims to develop advanced trap fabrication processes that will allow much richer trap and device functionality in the future.

Optalysys and Google HEIR collaborate on secure computing

The companies say that, by using optical computing, they could significantly boost the operational speed of fully homomorphic encryption, making the quantum-resilient cryptography method more commercially viable

Optalysys, a company focused on the future of secure computing, has partnered with Google HEIR to integrate its photonic processing technology into HEIR's compiler toolchain for fully homomorphic encryption (FHE). This integration aims to address the computational challenges of FHE, making it more commercially viable.

FHE is an advanced, quantum-resilient cryptography method that allows encrypted data to be processed without ever needing to be decrypted. It allows organisations to process data while maintaining privacy, opening up opportunities for secure data collaboration across industries, even in untrusted environments. However, the high processing demands of FHE, which are far greater than traditional computing, have posed a barrier to its widespread adoption and commercial viability.

HEIR, a compiler developed by Google, aims to provide an intermediate representation (IR) layer that allows FHE applications to run efficiently across various hardware platforms. HEIR does this by simplifying FHE integration, to make this cryptography method more accessible to developers, paving the way for new commercial applications.

Through the partnership, Optalysys plans to integrate its advanced photonic computing technology with HEIR's compiler, to enable HEIR-generated code to run FHE workloads on Optalysys' optical processing chips.

"Our partnership with Google HEIR is a milestone for both photonic computing and the FHE ecosystem," said Nick New, CEO of Optalysys. "This is the first time that photonic processing has been integrated into an FHE toolchain, and the results from our trial demonstrate significant improvements in performance. Optalysys' technology is uniquely positioned to address the demanding computational needs of FHE and this collaboration is a major step toward faster, more efficient, and accessible encryption."

Jeremy Kun, SWE, Google Security Research, said: "We are excited about the Optalysys and Google HEIR collaboration, a significant step forward towards practical FHE. This effort showcases how the interplay of sophisticated algorithms, groundbreaking hardware, and user-friendly tools is essential for bringing FHE into the mainstream.

HEIR simplifies FHE integration and empowers developers to build real-world, privacy-preserving applications without requiring deep cryptographic expertise. This type of focused investment, bridging the gap between advanced cryptographic research and practical application development, is precisely what's needed to unlock FHE's transformative potential for secure computation."

Jabil expands silicon photonics capabilities

JABIL has announced its continued investment in silicon photonics-based products and capabilities to support the increasing demands of hyperscalers and next-wave cloud and AI datacentre growth.

The company said it is set to roll out additional capabilities at its Ottawa, Canada, site in the fourth calendar-year quarter of 2024 to support customers' advanced photonics packaging new product introductions (NPIs).

According to Jabil, the NPI line will feature innovative capabilities designed to assist photonics customers to quickly scale from proof of concept to mass production, such as fluxless flip-chip, fibre attachment, precise die bonding, and wire bonding. The company says these advancements will support silicon photonics chip packaging, particularly in high-speed connectivity applications such as co-packaged optics (CPO) and high-speed on-board connections. Jabil adds that, by leveraging its expertise, customers can benefit from enhanced performance and reliability in their photonics solutions, ultimately driving agility and scalability in their operations.

"The expansion of our Ottawa site is a game-changer for Jabil," said Matt Crowley, executive vice president, Global Business Units. "This facility will enable us to meet the growing demands for advanced photonics solutions tailored to AI and next-generation datacentres. Through our NPI capabilities, we can assist customers in their own product development journeys, significantly reducing the need for costly trial and error in developing their own solutions from scratch."

Jabil says it continues to pioneer industry-first "silicon to solutions" manufacturing approaches that improve the scalability of current and next-generation photonics, including 800G and 1.6T. The company also continues to make investments in next-generation silicon photonic technologies beyond 800G and 1.6T, intending to support AI and cloud computing, and focusing on optimised performance and reduced power consumption for modern datacentres.

PhotonDelta announces €50,000 global photonics engineering contest

Submissions will be open until 3 March 2025 and the winner will receive €50,000 in services from the ecosystem to transform their idea into reality

PHOTONIC CHIP industry accelerator PhotonDelta has announced it is launching a global engineering contest in collaboration with Wevolver, a knowledge and community platform for engineers, to stimulate the creation of new applications for photonic chips that tackle global challenges.

PICs enable smaller, faster, and more energy-efficient devices by sensing, processing, and transmitting data far more effectively than traditional electronic chips. Crucially, they surpass the limits of Moore's Law and are used in semiconductors, telecom, agriculture, quantum computing, and automotive technologies.

The engineering contest is a global competition for innovative ideas for PIC-based solutions that address some of the world's most pressing societal and technical challenges, from combating climate change and advancing healthcare to addressing energy sustainability challenges. The competition invites engineers to use the characteristics of PICs to revolutionise fields like healthcare, autonomous vehicles, AI and agriculture by enabling advanced sensors for earlier diagnostics, safer infrastructure, or more efficient food production. The ultimate goal of the contest is to discover future applications in segments that are yet to be invented.

The contest is backed by a €60 million fund from PhotonDelta, set up to stimulate the creation of new startups and innovative applications in the PIC industry. By offering favourable loans to (pre-)seed companies, the fund seeks to support entrepreneurs and researchers in turning their ideas into viable businesses. This initiative aims to foster innovation at the earliest stages, encouraging the development of new technologies and applications that can shape the future of the PIC ecosystem.

The winner will receive €50,000 worth of services to bring their idea to life as well as global exposure at an industry event. On top of that, participating in this challenge will provide the unique opportunity to position the company for raising a favourable loan of up to €2 million by PhotonDelta. The contest is held in collaboration with Wevolver, and supported by imec, SMART Photonics, LioniX International, Bright Photonics, Epiphany and PHIX Photonics Assembly.

The Global Photonics Engineering Contest is open to startups, established companies, engineers, researchers, students, and academic organisations working on innovative photonic chip applications.

The contest was officially launched at PIC Summit 2024 in Eindhoven, the Netherlands on 15 October. Submissions will be open until 3 March 2025. Entries will be judged on the level of innovation, technical and commercial feasibility, and how effectively the design addresses current industry challenges. Participants are required to submit detailed descriptions of their projects, including team information and supporting visuals or videos. A jury panel of experts from the integrated photonics industry will review the submissions, with the winners announced on 2 April 2025.

HyperLight announces $37 million funding round

HYPERLIGHT CORPORATION, a provider of thin film lithium niobate (TFLN) PICs, has announced a $37 million Series B investment led by Summit Partners. The round includes participation from existing investors Xora Innovation, a deep tech venture fund backed by Temasek, and Foothill Ventures. Peter Chung, managing director and CEO of Summit Partners, will join HyperLight's board of directors.

The continuing need for more bandwidth and greater power efficiency, accelerated by AI, is driving the industry's transition to next-generation photonics technology. Current PICs have performance limitations due to their material properties and have become bottlenecks for high-performance optical communication.

According to HyperLight, its TFLN PICs deliver unmatched bandwidth and energy efficiency well-aligned with the current and future needs of AI/datacentre infrastructure, telecommunications optical networks, and high-performance computing. The company says that, since its founding in 2018, it has delivered industrial-scale TFLN PICs with a trusted supply chain.

With this new financing, HyperLight intends to accelerate product development and meet rapidly growing customer demand.

"We believe TFLN will be the photonics platform of the future and identified HyperLight as an emerging category leader," said Peter Chung of Summit Partners. "The HyperLight team has established an impressive track record of pioneering innovation and strong execution. In a short time, the company has evolved this critical technology into market-ready products with a production-ready supply chain."

X-Celeprint, Ligentec and X-FAB team up on heterogeneous integration

The three companies aim to create a fully integrated supply chain for hybrid PICs by combining X-Celeprint's micro transfer printing technology with Ligentec's silicon nitride platform and X-FAB's specialty foundry

X-Celeprint, Ligentec, and X-FAB have announced that they are aligning their efforts to simplify and enhance heterogeneous integration through micro transfer printing (MTP), with the goal of revolutionising PICs. The companies say their collaboration is set to close existing gaps in the value chain and offer a seamless journey from R&D to mass production.

In response to the global need for reducing power consumption, emissions, and material waste, advanced photonic integration and packaging technologies offer a route towards a greener future while delivering scalable, high-performance solutions for the industry. PICs are at the forefront of technological innovation, poised to enable breakthrough applications and overcome current technological barriers.

The future of PICs is moving towards chiplets, where the best materials and components are combined to create hybrid solutions. Today, achieving these hybrid chiplets is a complex and cumbersome process for customers, as no integrated supply chain exists to streamline the path from development to production.

To address this challenge, the partnership between X-Celeprint, Ligentec, and X-FAB is aimed at creating a fully integrated supply chain that simplifies the development and industrialisation of hybrid PICs.

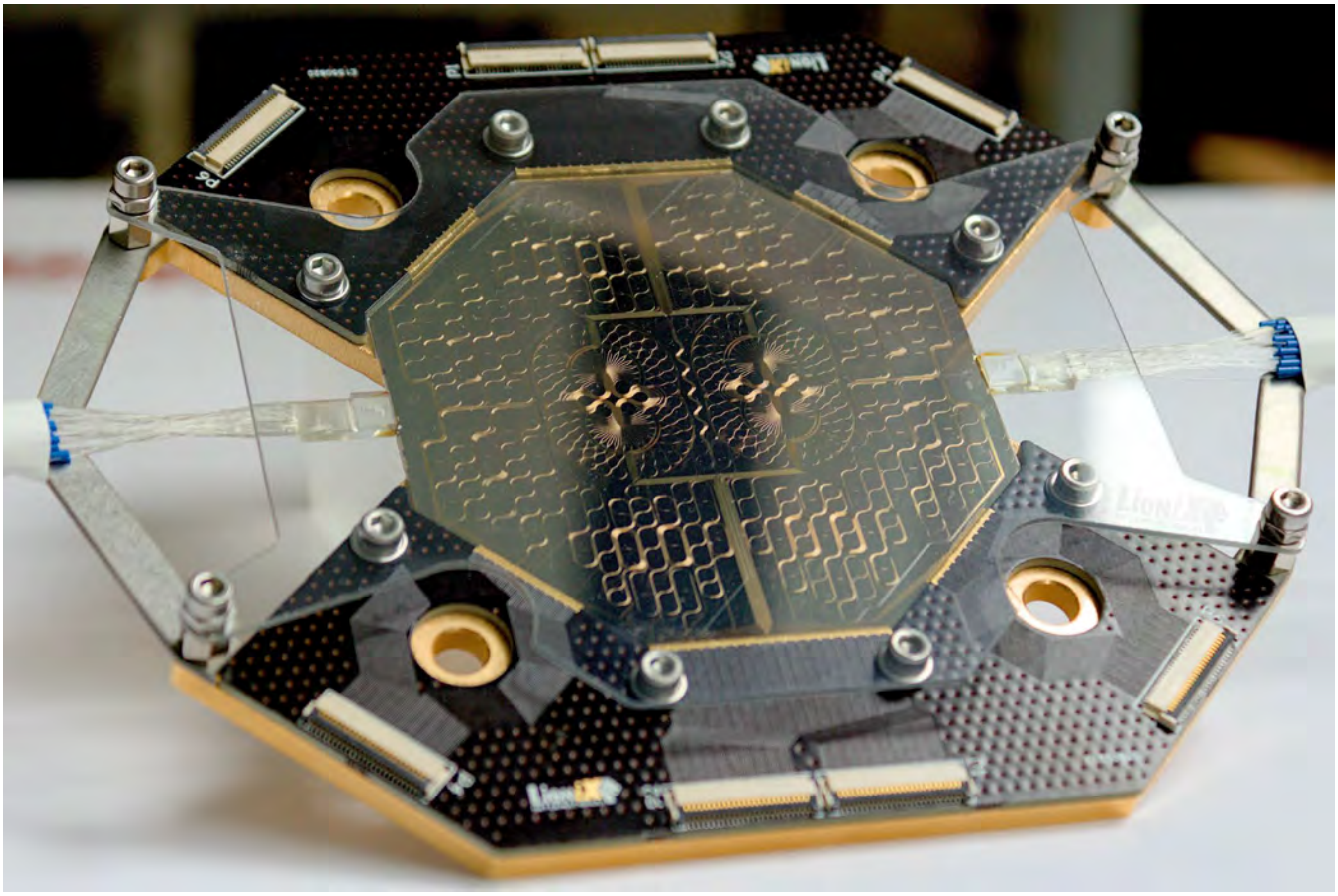
According to the companies, the collaboration combines Ligentec's low-loss silicon nitride PICs, X-Celeprint's MTP technology, bringing the capability to integrate diverse active materials on PIC platforms, and X-FAB's specialty foundry for feature-rich analogue mixed-signal ASICs, MEMS, microsystems and photonics, providing scaling-up and volume production capabilities. Together, the companies will be working towards offering customers a complete, seamless solution, covering all stages from early technology assessment and R&D, through design support, prototyping, and piloting, to full-scale production.

As the first step in this partnership, Ligentec plans to integrate photodetectors onto their low-loss silicon nitride platform using MTP technology. This will be offered as an additional module to their regular multi-project wafer runs, intending to provide an easy, low-barrier entry point for customers. X-Celeprint plans to contribute its expertise in process development, with X-FAB seeking to ensure a smooth scale-up from prototyping to volume production.

"After years of intensive R&D, we are seeing significant uptake and interest in MTP," said Kyle Benkendorfer, CEO of X-Celeprint. "The technology readiness level in photonics integration has reached the stage to bring it to the market, offering customers a powerful solution to overcome the challenges of hybrid PICs."

Thomas Hessler, CEO of LIGENTEC, said: "No single material system can meet the diverse requirements of photonics. Heterogeneous integration is essential, and with MTP, we have the ideal technology to combine the best active materials with our high-performance silicon nitride platform. This not only enhances functionality but also opens the door to new applications and innovations."

Volker Herbig, VP BU Microsystems of X-FAB, added: "We see MTP as a very promising technology with tremendous future potential. X-FAB is committed to supporting this collaboration, ensuring a smooth and efficient transition from prototyping to high-volume production." The companies say their combined offering covers the entire customer journey, providing clear and accessible pathways from R&D to high-volume production. They also plan to integrate more functionalities, such as light generation and modulation, in the next stages, further expanding the potential of this technology.



Boosting satellite networks with flexible microwave photonics

In a project with ESA, LioniX International has developed a reconfigurable microwave photonics module that could transform satellite communications. This innovation illustrates how far PIC technologies have come and how effectively they can now be adapted to serve a diverse range of industries.

BY SADOON AL-OBAIDI, MARKETING & COMMUNICATIONS DIRECTOR, CHAROULA MITSOLIDOU, SYSTEMS ENGINEER, AND IOANA MATECIUC, MARKETING ASSISTANT, LIONIX INTERNATIONAL

THE UBIQUITY of generative AI in today's world, both as a content-making tool and as a successful business case for PICs, has quickly become well-trodden ground. Of course, for industry insiders this is nothing new. Pluggable transceivers were already the biggest market for PICs before 2022, when popular software like DALL-E 2, Stable Diffusion, and ChatGPT were released for public use. For the PIC specialists, they are not where the intrigue lies. Instead, what everyone wants to know is: what will be next? Of all the possible applications of PIC technology, bursting with potential as it is, what device will combine the performance boost, market necessity, and ease of production to make the big time?

Will quantum computers finally take the crown from GPU computation? Is PIC-powered LiDAR on the verge of appearing in every car? How many disposable PIC sensors will personalised medicine need for rapid drug testing? Each of these applications requires entire ecosystems, with variations on product developers, design houses, chip foundries, assemblers, test labs, you name it. The technology is flourishing; if only we could know which of the many innovations will take off.

To be clear, we will not be consulting any oracles here. Aside from the Euro 2024 office pool, LioniX International is not in the betting business. But our module development work does make us regular optimists. We have seen design and processing principles, developed through more than 20 years of operation, prove capable of realising a range of disparate applications. We have converged on some basic rules to follow, like using each photonic integration platform for what it's good at, designing the whole device before designing the photonic circuit, and involving the application experts as much as possible.

The PIC ecosystem has been arriving at the same conclusions, too. We now see a thriving PIC field, with many new and established firms following the same principles to tackle a wide range of problems from different angles. So, we are in no rush to have a horse in the race. Instead, our vertically integrated structure allows us to see the potential of PICs actualised for different markets, in novel modular devices, time and time again. Which brings us to the subject of this article: a particularly exciting recent in-house development in the form of a fully adjustable satellite communications (satcom) channel selector, functional across three microwave bands (Ka, Q, and V), from 300 MHz to 300 GHz.

Microwave communications is its own highly sophisticated field, rivalling even quantum processing in complexity and technical considerations. Diving into this world, we will explore how the function, design, and production of microwave communications come together, and how this technology can revolutionise satellite communications. But this is just one compelling example of a broader take-home message: PICs have reached a level of maturity that lets us build high-performance, energy-efficient devices for virtually every industry.

The question isn't whether PICs can prove themselves again with a second killer app; the question is which market will be next to find its great leap forward with PICs.

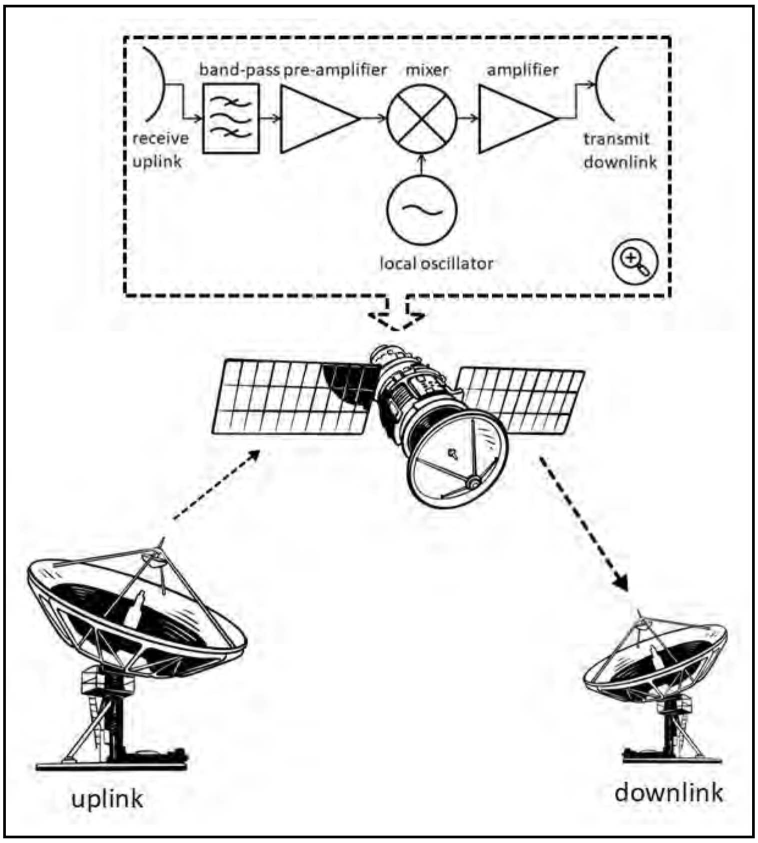
Crowded bandwidth, crowded orbit

The satcom industry faces an old monster in an evolved form. As telecom providers plan for bigger data rates through 6G networks and beyond, satcom must accommodate that need within a limited available bandwidth. There are a few options, but the industry has yet to converge on a solution for allocating the limited bandwidth where it is needed.

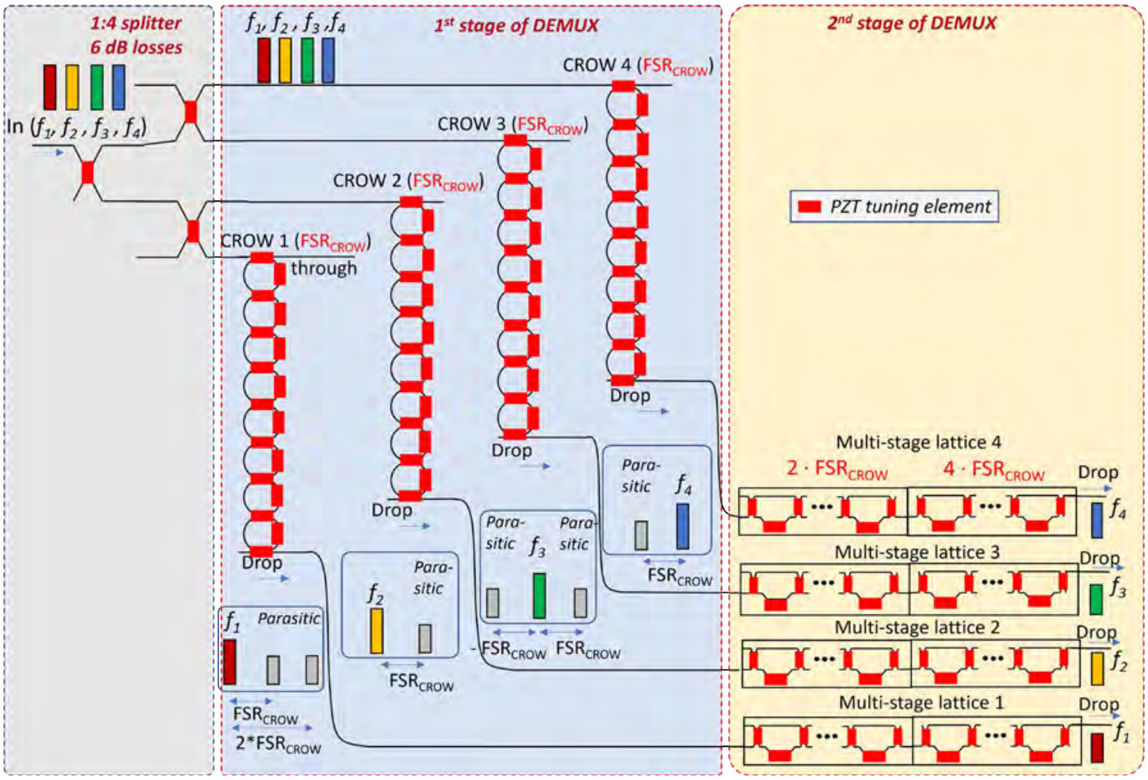
The status quo of satcom is that each conventional satellite is sent to orbit with a payload of electronics that processes signals in one specific way (Figure 1). They receive a low-power broadband signal from a ground station, which the satellite splits into different channels (demultiplexing, DEMUX). These component signals are frequency-shifted, filtered clean, then power-amplified separately, recombined into a single signal (multiplexing, MUX), and sent back to Earth.

This process of DEMUX, filtering, amplification, and MUX, is pre-programmed before the satellite is launched. The signal processing system is set, with no possibility of reconfiguring any of it once it is in orbit. If there is a signal that needs to be processed differently in some way, this can only happen if a different satellite equipped for the task is already launched into orbit.

One solution would be to populate space with as many satellites as necessary to handle the different processing routes. But there are many reasons why this would be far from ideal. Besides the high financial and material costs of launching so many satellites, this approach would clearly contribute to the serious problem of space debris, potentially triggering an ablation cascade – in which one collision results in more debris that makes further collisions more likely. Moreover, large numbers of satellites also interfere with astronomical research by simply blocking the view. The phrase "single-use satellite" may sound absurd, but the problem is inescapably reminiscent of plastic production and consumption.



➤ Figure 1. A general schema for satellite communication signal processing.



➤ Figure 2. Schematic representation of the 4-channel (DE)MUX filter module. The 4 independent paths leading out of the tuneable splitter each connect to an independent set of CROW and lattice filters. The power distribution is selected by the splitter, the CROW filters carve off the user-selected channel, and the lattice filters clean up the spectrum.

The alternative is flexible satellites that can be reconfigured in orbit, 'at runtime,' to process different kinds of signals as needed. Far from trivial, this goal is a focus of much R&D effort in the space sector. The electronics of flexible payloads are difficult to realise, while the equipment required to do the necessary signal splitting, filtering, amplifying, and combining is bulky, heavy, and energy intensive.

For a reconfigurable electronic payload, the required components start to pile up, making the whole endeavour less efficient. But our emphasis on 'electronic' here is not incidental. ICs may be the original kind of integrated circuit, but PICs have exactly the right set of advantages to tackle this problem.

The field of integrated microwave photonics (iMWP) in general addresses the need for photonic techniques to generate, distribute, process, and analyse high-frequency and broadband electronic signals, all on PICs. Compared with alternatives, PICs sidestep inherent obstacles like electromagnetic interference and crosstalk. They also bring their own distinct advantages, from performance enhancements and stability, to size, weight, power, and cost (SWaP-C) improvements. Furthermore, iMWP enables entirely novel functions in analogue components. For example, iMWP filters provide key advantages that surpass the performance of current state-of-the-art electronic filters. These include broadband tuneability and reconfigurability, as well as high frequencies, up to the terahertz range.

This is the context within which project ThoRmux aims to excel. In collaboration with the European Space Agency (ESA), Sener Aerospace, and Charles III University of Madrid, LioniX has been developing a tuneable iMWP radiofrequency (RF) DEMUX system, which allows flexible frequency allocation within broadband signals.

At the heart of the system is a PIC-powered (DE) MUX filter module, which enables multiplexing and demultiplexing of multiple channels with reconfigurable bandwidth and central frequency.

As each of these components is independently addressable, the channel selector can be fully reconfigured; each channel's central frequency and bandwidth can be tuned across the Ka, Q, and V RF frequency bands

The system makes use of our ultra-low-loss silicon nitride platform, TriPleX, and our holistic PIC module approach.

What's in a channel selector?

An iMWP module works in the context of electronic RF systems. Hence, for this module as well as others, the chain of operations includes light generation for the carrier signal, modulation (to up-convert and encode the RF signal into the light), the application-specific operation of the device (in this case, filtering), and finally, detection (to convert the light back to RF).

The ThoRmux DEMUX module specifically covers filtering, and is designed to process a broadband signal carrying 4 RF channels. Its function can be summarised as a channel selector. As shown in Figure 2, it is schematised as a tuneable 1:4 optical splitter, a set of filters based on coupled ring-resonator optical waveguides (CROW) for an infinity impulse response (IIR), then a set of filters based on a lattice of asymmetric Mach-Zehnder interferometers (aMZI) for a finite impulse response (FIR).

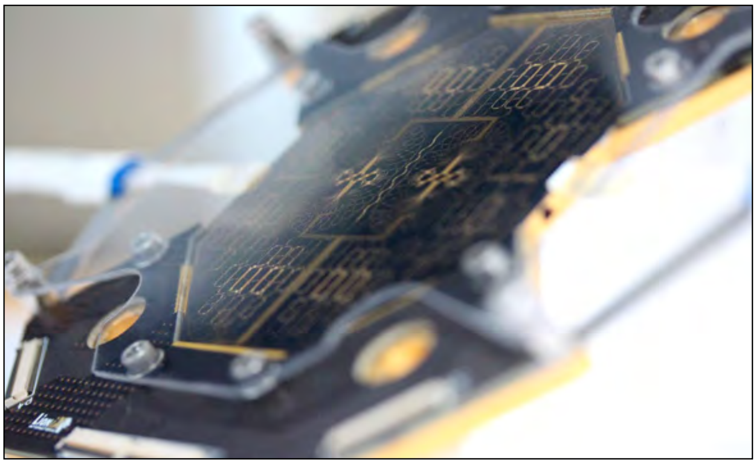
The first set of filters, based on CROWs, is the primary bandpass filter of the channel selector. They select each channel's central frequency and regulate its bandwidth. The filters have been designed for operation at 1550 nm and exhibit a free spectral range (FSR) of about 2.5 GHz. TriPleX silicon nitride has demonstrated optical losses lower than 1 dB per metre, which enabled the realisation of these microring resonator (MRR)-based filters with extremely high quality factor (Q factor up to 300.000). This results in high-resolution bandwidth and sharp roll-off filter response.

The second set of filters, based on aMZI lattices, serve as FSR extenders. CROW filters produce 2nd and 3rd parasitic passbands, which limit the FSR of their response. These lattice filters act as secondary band-stops, suppressing the parasitic passbands and extending the FSR of the channel selector to about 10 GHz. The distinct advantage of aMZI filters is that they can be realised with an unlimited FSR, whereas MRR filters are limited by practical considerations regarding their components, such as waveguide bending losses and phase shifter lengths.

As each of these components is independently addressable, the channel selector can be fully reconfigured; each channel's central frequency and bandwidth can be tuned across the Ka, Q, and V RF frequency bands. What's more, once it is tuned, it uses very little power. Our lead zirconate titanate (PZT) stress-optic actuators, used to tune the filters, have about 1 μW per actuator of power dissipation in quasi-static operation. Set it and forget it, until you want to reset it.

A flexible module needs lean work

Now we can inspect the device with an eye for its function. The TriPleX PIC comprises the majority of its surface area, in the middle of which are the 1:4 splitter and the 4 "mandala"-shaped IIR CROW filters (Figure 3). Blossoming out from these are the aMZI-based FIR lattice filters, which fill the rest of the chip.

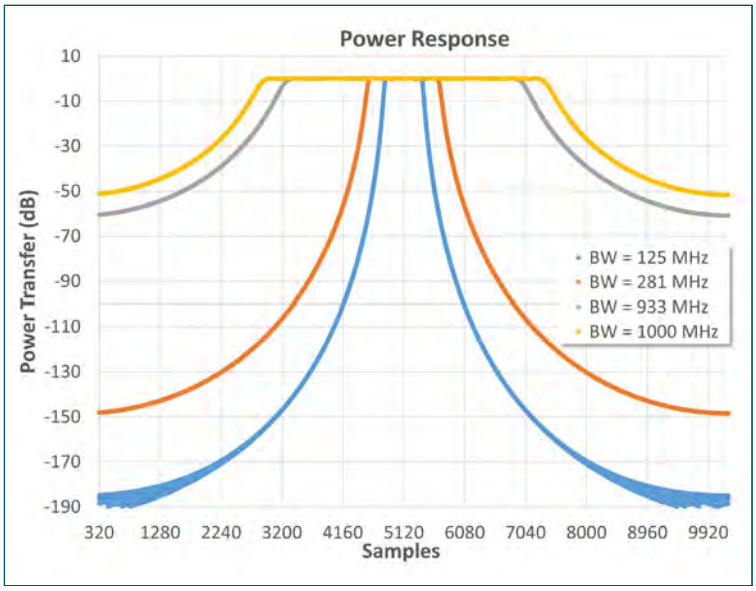


➤ Figure 3. A closeup of the ThoRmux module, with the 1:4 splitter and CROW filters in the chip centre, surrounded by an aMZI lattice. Wirebonds connect the PZT actuators to the surrounding PCB, which route to ribbon cable connectors.

The optical inputs and outputs are interfaced to fibre arrays at the east and west, while the tuner electrodes are placed on the diagonals and wire-bonded to a custom PCB.

The assembly is mounted on a copper sub-mount, with flat cable connectors that provide connectivity to the control electronics. A total number of 318 PZT-based tuning elements are employed to tune and reconfigure the various photonic filters in the device. Since the quasi-static power consumption per actuator is ≈ 1 μW, the total power consumption in the PIC is lower than 320 μW for the entire module. The total assembly spans 129 mm × 135 mm × 5 mm.

It takes a village to raise a child, and it took the



➤ Figure 4. Simulated spectral response of the 4-channel DEMUX filter.

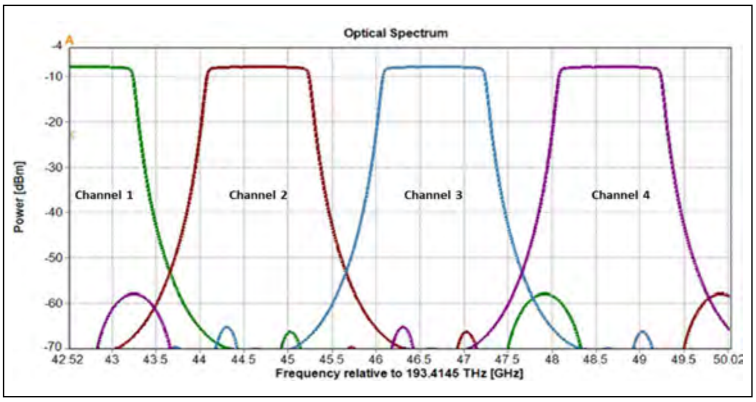


Figure 5. Simulated CROW filter power responses for different frequencies.

whole LioniX team to make this module. The nearly 4 metres of optical path length necessitated the use of ultra-low-loss TriPleX for the successful integration of the device. The circuit design had to consider the essential reconfigurability of the device and the long total waveguide length. It also had to take into account how the actuators could be connected to the control electronics, which meant that assembly and packaging considerations were included from the start.

From a chip fabrication point of view, everything from the splitting of the circuit design across multiple reticles and arrangement of processing tolerances, all the way down to polishing for optical integration, presented engineering challenges of their own. Finally, assembling this device, including the fibre array integration and wire-bonding, took practised expertise and operational flexibility.

The device is currently undergoing testing and characterisation in our labs. Early simulation studies showed very promising results vis-à-vis the filters' spectral response; simulations predicted flexible bandwidth reconfigurability, with the tuneable bandwidth ranging from 125 MHz to 1 GHz (Figure 4). This is achieved by adjusting the power coupling coefficients of the tuneable couplers between the 8 MRRs of the CROW filter.

We also simulated central frequency tuning of each channel selector filter's cascade. For the case shown in Figure 5, we turned the 4 individual passbands to have a channel spacing of 2 GHz. This is done by adjusting the tuneable phase shifts of the CROW MRRs and the lattice aMZIs. In general, the passband of each of the 4 channel selectors can be arbitrarily set to a different central frequency.

These simulation results have been presented in detail at the International Conference on Space Optics. The results of the ongoing characterisation work will be the subject of an upcoming talk at Photonics West. We don't want to spoil too much, so here's a buttoned-up teaser: the results are in good agreement with the simulation.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The evolving role of optics in AI clusters

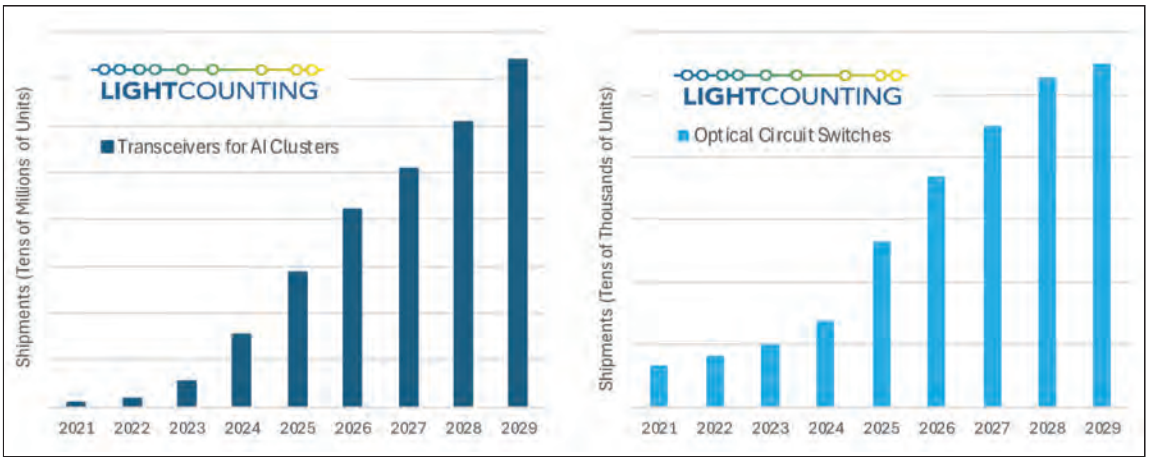
In the AI arms race between tech giants, there is more than one approach to using optics for efficient data handling in datacentres and AI clusters

BY VLADIMIR G. KOZLOV, CHIEF ANALYST AT LIGHTCOUNTING

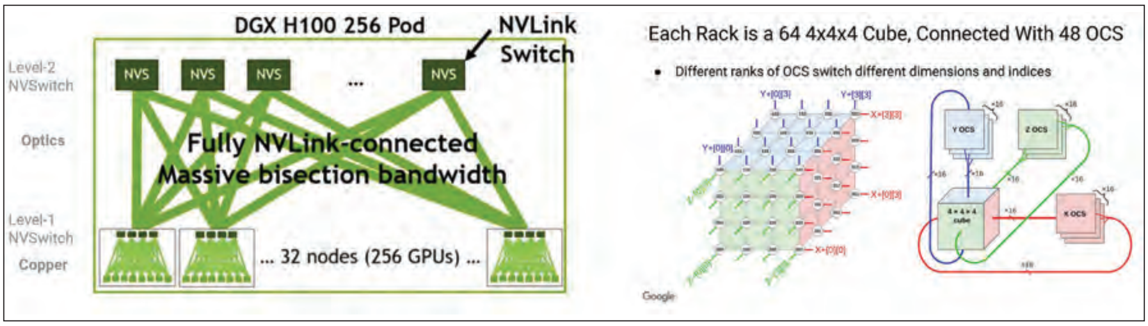
ARTIFICIAL INTELLIGENCE will transform a wide range of industries over the next decade, the manufacturing of optical components and interconnects being one of them. It is also one of the few industries directly impacted by the boom in construction of AI clusters, whose effects alone will be enough to reshape the sector. Although novel technologies and numerous startups will have an opportunity to succeed, it will be up to the largest customers to select the winners. Decisions made by Google, Microsoft, and Nvidia will define the directions for innovation, and there may be more than one path forward in this arms race.

Google and Nvidia already have diverging priorities for optical connectivity and switching, while other large customers may find new ways to use optics for AI. All-optical signal processing continues to improve, but it is hard to compete with billions of transistors in a single chip. The most advanced PICs are limited to a few thousand devices. Yet, there may be another way to perform analogue processing of the optics.

Video and image recognition are among the most exciting applications of AI, and probably the most consequential in their capacity to compete with human cognition and transform our world. All of this starts with the optics. Our own biological vision systems can zero in on what matters, rather than flooding our brains with information. Similarly, LiDAR technologies already enable video recognition



➤ Figure 1. LightCounting's forecast for shipments of optical transceivers and optical switches for AI clusters over the next five years. (Source: LightCounting)



➤ Figure 2. A comparison of the AI cluster architectures used by Google and Nvidia. (Source: Google)

to focus on moving objects instead of a static background. Are there more tricks for the optics to do? The answer is yes, but it is hard to predict exactly what these will be.

Considering what we already know, Figure 1 shows LightCounting's forecast for shipments of optical transceivers and optical circuit switches (OCS) for the next five years. Both charts show explosive growth, which may be interrupted by a slowdown at some point, but will likely resume soon after that. Currently, optical transceivers for AI clusters are shipping in tens of millions of units annually, and will reach close to 100 million units by 2029. Shipments of OCS reached 10,000 units in 2023 and will exceed 50,000 by 2029.

AI cluster architectures

Google started using OCS in their compute nodes and AI clusters more than a decade ago. The company reported on the advantages of OCS-enabled architecture in multiple recent publications. Several other large AI cluster operators are now also starting to use OCS, and many more are seriously considering the benefits of following suit.

There is little doubt that demand for OCS will be strong and there may be more complex applications of optical switching in the future. Packet switching is problematic, since there are no practical solutions for optical buffers, but elephant flows can be routed optically. One can "hear" such flows coming from a distance and pre-provide a path for them.

Google was also the first to use optical transceivers in its datacentres back in 2007. Although the company's adoption of this technology was briefly interrupted by the financial crises in 2008-2009, it resumed in full force in 2010. Many other cloud companies have followed Google's approach over the last decade. Nvidia (Mellanox) preferred active optical cables (AOCs) until two years ago, but it became the largest consumer of 400G/800G transceivers in 2023.

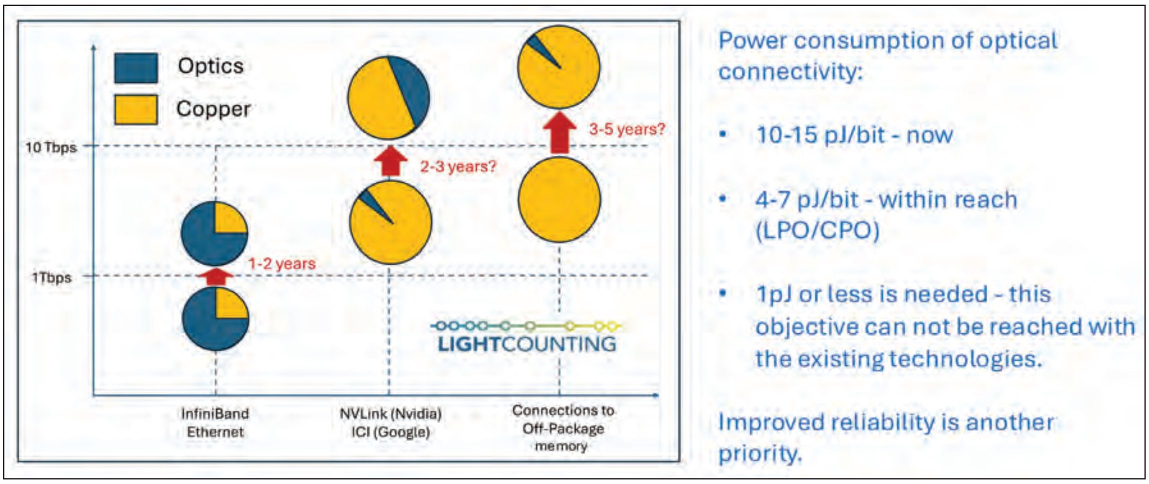
Nvidia is currently using optical transceivers for Ethernet and InfiniBand connectivity between racks of servers and switches. The company also announced plans to use optics for NVLink connections two years ago and demonstrated it in one of their internally built clusters. NVLink connections require 9 times more bandwidth than InfiniBand, so reducing the cost and power consumption of the optics is a must to enable this new application.

Figure 2 compares the AI cluster architectures used by Google and Nvidia. TPU clusters developed by Google do not require Ethernet or InfiniBand switches, but use OCS. Each TPU can communicate directly with its six nearest neighbours, and OCS can scale and reconfigure these tightly knit networks. In contrast, Nvidia's designs rely heavily on InfiniBand, Ethernet, and NVLink switches, requiring a lot more optical connectivity than Google's designs.

These differences in AI cluster architectures lead to diverging priorities for optical interconnects at Google and Nvidia, as illustrated in Figure 3. Google's use of OCS prioritises a higher link budget to offset the 1.5 dB optical loss of an OCS. Multi-wavelength FR4/FR8 transceivers increase the throughput of an OCS by a factor of 4 or 8, in comparison with DR4/DR8 modules.

Company	2015-2022	2022-2024	2025 and beyond	Key requirements to Optical I/Os	Average Transceiver to GPU/TPU ratio
Google	SR4, FR4	DR8, 2xFR4, FR8	FR8 re-timed pluggables only	Higher lane rate, more wavelength per fiber. Good link budget	1.5 for all generations
Nvidia	AOCs	SR4, SR8, DR8	DR8 re-timed pluggables, LPO/LRO and CPO	Lower cost and power consumption Improved reliability	2.5 now up to 10 in the futur

➤ Figure 3. Key requirements for the optics at Google and Nvidia. (Source: LightCounting)



➤ Figure 4. Applications of copper and optical interconnects. (Source: LightCounting)

On the other hand, Nvidia prioritises lower cost and power consumption to accommodate the larger quantities of transceivers required in its clusters, and is very supportive of linear-drive pluggable optics (LPO) and co-packaged optics (CPO) approaches. Google has no interest in LPO or CPO, since its designs will continue to use only 1.5 transceivers per TPU on average, whereas Nvidia may need up to 10 transceivers per GPU in the future to support NVLink over fibre.

For this reason, we expect that Nvidia will deploy LPO and/or CPO in the next 2-3 years to reduce power consumption from 10-15 pJ/bit to 4-7 pJ/bit, enabling NVLink over fibre, as illustrated in Figure 4. Google is already using optics for inter-core interconnects (ICI) between TPUs. Further improvements in the power efficiency of optical devices are needed to enable optical connections to off-package memory, also shown in Figure 4.

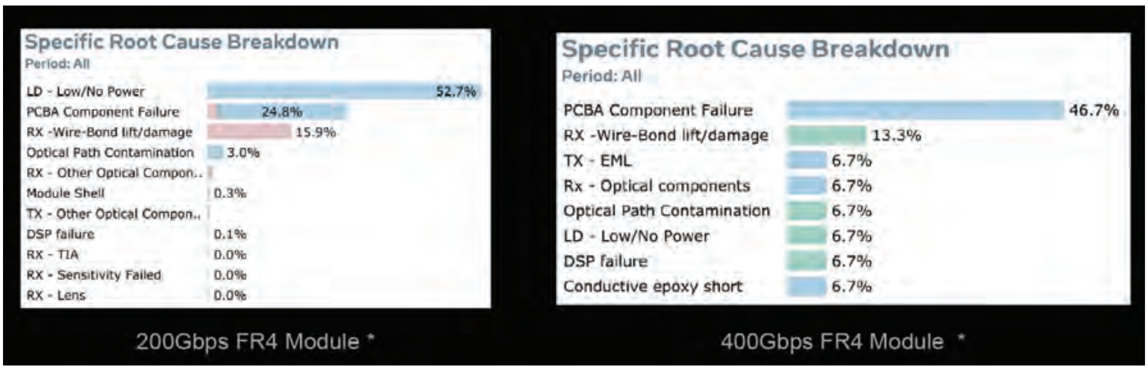
Challenges in scaling performance

The reliability of all components inside an AI cluster is becoming critical for scaling up these systems; a single failed GPU or network link can reduce the efficiency of the whole cluster by 40 percent, and mitigating failures (via software) could take up to 10 minutes. Such failures occur every 30-45 minutes on average. This problem will only get worse for larger clusters based on more complex GPUs and optics.

Figure 5 shows data on transceiver failure analysis for 200G FR4 and 400G FR4 modules. Directly modulated laser degradation was the main source of failures in 200G modules. Degradation in the performance of an externally modulated laser used in 400G transceivers was less of an issue than general manufacturing issues related to printed circuit board assembly and wire bonds. Adopting more integrated wafer-scale design and manufacturing is essential for improving the reliability of the optics.

GPU performance is expected to improve substantially by the end of this decade, through a combination of advances in CMOS, substrate and packaging methods, chip architecture, and better cooling techniques. Managing heat dissipation from these very large chip assemblies is one of many problems, so a roadmap for improvements in power efficiency is key for all technologies used in AI clusters. CMOS does have a roadmap from 5 nm to 3 nm and 2 nm within the next five years, but optical interconnects are still searching for a path to higher power efficiency.

LightCounting expects that linear-drive optics will be deployed in volume over the next five years, either as pluggable transceivers (LPO or linear receive optics) or as CPO. The industry will need new materials and devices to achieve further gains in power efficiency. Time to market may be as long as a decade for some of the novel technologies, but a few of these will be adopted within the next five years. It is worth bearing in mind that this is an arms race; there will be customers who are willing to take bigger risks.



➤ Figure 5. Transceiver failure analysis for 200G FR4 and 400G FR4 modules. (Source: Meta)

Bringing cutting-edge photonics into the classroom

With branches focusing on both industry and education, Spark Photonics is uniquely positioned to bring up-to-date research into its educational programmes, giving school students a glimpse into real-world photonics careers and putting advanced manufacturing on their radar.

AN INTERVIEW WITH KEVIN MCCOMBER, CEO OF SPARK PHOTONICS DESIGN AND EXECUTIVE DIRECTOR OF SPARK PHOTONICS FOUNDATION

LH: *Can you tell me about Spark Photonics and how it got started?*

KM: Spark Photonics is a brand name that's actually two legal entities. There's Spark Photonics Design, Inc., which is a commercial PIC design services company. Then there's Spark Photonics Foundation, Inc., which is a nonprofit STEM (science, technology, engineering, and mathematics) educational outreach company. I'm the CEO at the design company and the executive director of the foundation.

The genesis of both entities came from work we were doing at MIT back in 2018 and 2019. I was on staff doing education and workforce development (EWD) as part of AIM Photonics, which is a large PIC initiative out of New York. MIT at the time led all of AIM Photonics' EWD, and I was assistant director there. When I was hired, it was part of my job description to start up design services. I met my co-founder, Al Kapoor, at one of the AIM events where he was looking for PIC design services. That's how we came up with the idea for Spark Photonics Design.

At the same time, we felt there was a missed opportunity in K-12 to talk about photonics. AIM was focused mostly on graduate students and the incumbent workforce. We felt that, if we're going to build a long-term workforce, we're going to have to start early and work higher up in the funnel of future talent. That's where we can really move the needle. That was the genesis for Spark Photonics Foundation.

We started the two organisations on the same day in 2019. The foundation found its legs under a US Department of Defense (DoD) grant award to create what is now our flagship K-12 STEM educational outreach programme, SparkAlpha.

We like to think that we're unique in that the need of the technology side informs the need for the EWD, and that the latter is so closely aligned with industry and led by someone who has a technical background in the subject. We see a lot of EWD organisations led by folks who are traditionally in the education space. Or if they come from industry, they might not be up to date with the current technological advances.

We actively use what we're learning in design to inform our programming and the material that's being taught. For instance, we're working on a project with the University of Rochester and AIM to do sensors for human viruses on a chip, and we use that as an example for students in our educational programmes, because it is happening right now. It doesn't get any more current than this.

LH: *What role does Spark Photonics play within the broader integrated photonics ecosystem?*

KM: For Spark Photonics Design, we were established in large part because the US DoD and the defence industrial base were saying: "We need somebody domestic that can help us design PICs." Of course, we've branched out from defence, but we still have quite a bit of work there. Spark Photonics Design helps companies and others get into PICs from a technical perspective.

We see the foundation as the feeder of future employees into STEM jobs, and to some extent, the very early front door to PICs – as well as more broadly, photonics, semiconductors, and advanced manufacturing. This is how we recruit people into the ecosystem. A lot of us in the photonics industry focus on the tech, but there is no tech without people. We feel, too, that through the foundation, we're elevating photonics as a branch of STEM at large.

The foundation has a role not only in bringing more people into the PIC ecosystem, but also to use the novelty of photonics to showcase that there is a lot more to STEM than people might think. It's a unique opportunity to open people's eyes to worlds they didn't know about, especially photonics and PICs, and blow their minds.

LH: *Could you tell me more about how you work with partners in the industry?*

KM: This is mostly on the design side. Spark Photonics Design is the North American representative for Luceda Photonics, a leading PIC design and layout software company based in Belgium. In our partnership with Luceda, we offer a one-stop shop for design services on Luceda's platform. When our customers become successful and want to take on the design role themselves, we can help them transition onto Luceda's platform and still support them. It's a seamless, holistic approach to helping customers be successful in PICs, and it's possible through this unique partnership.

We're also OpenLight's layout partner for customers who want to tape out on their process, which is

➤ School students participating in SparkAlpha learn about photonics at Western New England University in Springfield, Massachusetts, an education partner of Spark Photonics

running at Tower Semiconductor. We use Luceda's software, and then we use OpenLight's process design kit (PDK) to help their customers tape out. It increases OpenLight's capacity so they can focus on their bread and butter, which is the development of that platform.

We don't have a formal partnership with Ansys, but we use their software to design the components we've released at AIM Photonics as part of their PDKs. On our nonprofit side, Ansys has donated to support the growth of our EWD programming. So Ansys has been a very good ally on the foundation side and technology provider on the design side, which is something we would like to see more of – closing the loop between the two entities.

LH: *Could you expand on the main activities of Spark Photonics Foundation?*

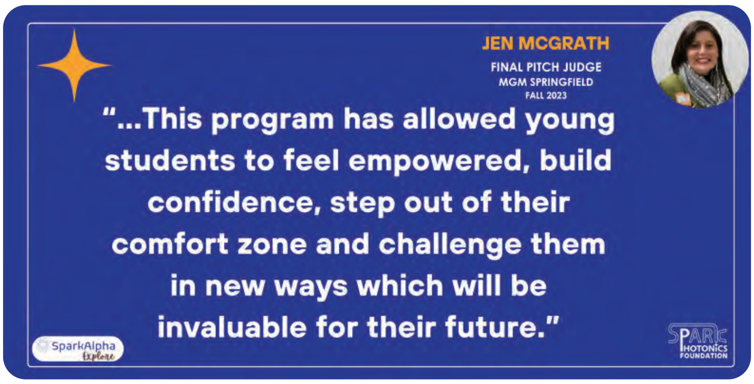
KM: Right now, we have a portfolio of three programmes that are meant to progressively deepen students' awareness and understanding of photonics, semiconductors, and advanced manufacturing overall. Our flagship programme,

An employee at Western New England University shows the components of photonic chips to school students participating in SparkAlpha

SparkAlpha, was created in 2021 and has been running for three years in Massachusetts with almost a thousand students. We're now expanding nationwide through a US DoD grant employing a "train the teacher" modality. We're running in Montana and we're actively seeking more schools across the country to implement this programming.

SparkAlpha is about making students aware of integrated photonics and semiconductors. Through project-based learning, they come up with a problem, address that problem with a photonics hardware product, make a business plan to launch and sell their product at a profit, and then do a live business pitch. They also take two in-person or virtual trips to an education partner – often a college or university – and an industry partner to see what employees' daily jobs look like.

Next we have SparkBeta coming out this fall. SparkBeta introduces students to the Python programming language, which is what we use on our design side. All advanced manufacturing starts with design, and Python is a very prevalent language that can be used for that. In SparkBeta, students do a mock PIC layout using Google Slides. Then they see an actual layout by one of our design engineers from our commercial side using Luceda's software, so they can relate to the real-life application.



SparkGamma is the third programme, which we're planning to roll out in 2025. In this, students learn about how PICs actually work: how light propagates on a chip, some of the basic PIC building blocks, and the process steps to fabricate a semiconductor chip. Then students do an actual chip layout using a PDK with Luceda's software through a portal hosted by Purdue University's Chipshub. They create an actual layout file of the chip that could be fabricated.

SparkAlpha is primarily for middle school and early high school, SparkBeta is early to middle high school, and SparkGamma is middle to late high school. SparkGamma is still in development, but we're getting a lot of good feedback that this three-part progression is something schools would really like to implement.

I also want to highlight that all our staff at the foundation are former educators. They have, on average, over a decade of experience in public education. I'm the only one with a technical photonics background. Although I touted that we have this unique bridge between design and foundation, we've consciously strived to make sure that our foundation staff understand education. They've also built up their photonics knowledge. But where the rubber meets the road is getting photonics into K-12 classrooms. That's best done by people who understand the K-12 landscape, and our staff definitely do. We've gone through a lot of iterations to make our programmes really age appropriate. Our staff are also very good at showing schools that this is something that will benefit their students and teachers and the stakeholders at large. They have walked the talk, so they can speak to teachers adopting the programme and explain the benefits.

LH: *Could you describe how the programme is run and delivered in schools?*

KM: SparkAlpha was traditionally done with our staff going into the classrooms, typically once a week for six weeks. But of course, that limits scalability when you have to physically be on site. Now, with another DoD grant, we've transitioned to a "train the teacher" modality, where we've created asynchronous training modules. Teachers can do the training in our online portal, which takes about three hours, and then they're qualified to run SparkAlpha in their classrooms.

SparkBeta and SparkGamma are self-contained, packaged curricula. They're meant to be something that the teacher can run without needing to know anything about the topic, and students work through the curriculum and all the activities.

We also add teachers to our community of practice platform, so they can contact other

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teachers or professionals who are implementing the programme. There are also folks from higher education and industry on the platform, so teachers have this network they can reach out to if they have any questions or need help. This is critical – sometimes programmes like this are just dumped on a teacher, and they are not supported. That's bad for them and their students. We want to be very thoughtful in making sure they are supported in a way that helps their professional development as well.

LH: *Have you had any feedback so far from SparkAlpha participants?*

KM: We do a post-programme survey with students, and from hundreds of responses, about 80-85 percent say it's increased their interest in and understanding of opportunities in STEM. Remember, kids can be harsh in surveys. We've got teachers who have seen us run the programme and have now taken on the "train the teacher" modality, because they see the value in it. In other cases, we've had teachers take it up without ever having seen it and they have also been successful. I think the fact that we have returning teachers and schools expanding the programme means it's filling a need.

At the start of every programme when we were running in schools, we always asked the students by show of hands, "Who's ever heard of photonics?" Usually no hands go up. Maybe one every once in a while. Then we asked, "Who's heard of integrated photonics?" Absolutely nobody. But then students come out of the SparkAlpha programme having given a presentation to their peers and a panel of judges about integrated photonics. We know that we're making them aware of the technology and the opportunities in it. We feel that's moving the needle.

We've done some initial teacher testing with SparkBeta. It actually ended up staying pretty similar to how we originally envisioned it. So again, a testament to our staff and their ability to predict how teachers are going to run it.

LH: *You mentioned Ansys' support for the programme earlier. Have other companies in the industry been getting involved too?*

AMBER O'REILLY
PARTICIPATING TEACHER
THE ACADEMY AT KILEY
FALL 2023

"Working with the Spark Photonics Foundation through their SparkAlpha Explore program was a great experience for both myself and my 8th-grade students...My students' innovative photonics device development provided an opportunity for each group members' strengths to shine...I highly recommend this partnership to other teachers and schools!"

SparkAlpha Explore

SPARK PHOTONICS FOUNDATION

KM: Yes they have. Ansys was a donor, but as part of SparkAlpha, students take an in-person or virtual visit to an industry partner. So far our partners have been in Massachusetts because that's where we'd been running up until the programme launched in Montana. MRSI/Mycronic, MACOM, Convergent Photonics, and IPG Photonics have been partners.

Then we've had other folks in the ecosystem who are not necessarily photonics companies but are part of the semiconductor supply chain. We had a company called Innovent Technologies that makes, among other things, the end effectors for the robots that handle the wafers. We've had a company called Flexcon that makes plastic sheeting and other plastic components used in the semiconductor supply chain. We try to think broadly about showing students what's in their community and then making the connection to how that feeds into the semiconductor supply chain. If there's nothing nearby, especially with rural communities, we can have students do a virtual visit with somebody in the industry and give them time to talk about their career.

When you think about all the components that go into electronic and photonic devices, it's a very broad supply chain. A large part of the reason for all these CHIPS Act initiatives is that the supply chain is just so expansive and hard to coordinate. We take that as an opportunity to show students that they can be part of the semiconductor industry from a variety of angles.

LH: *Last year, you received a three-year grant from the US government to expand your educational programmes. What are your aims for the next two years?*

KM: This grant was from the Manufacturing Engineering Education Program (MEEP) of the DoD's National Defense Education Program. It's a three-year award, and we're through year one already. The grant was to create this "train the teacher" modality, which we call SparkAlpha Explore, and then to deploy that first with schools in Massachusetts – that had already run under the SparkAlpha classic model – then to expand within Massachusetts with schools that hadn't run under the original model, and finally to expand nationally.

We've gone from the initial phase of our grant, implementing in schools in Massachusetts that are familiar with us, right to the national expansion, first with Montana. We see a need to demonstrate that it can be successful outside Massachusetts. We need to prove ourselves and have the confidence to say, "Yes, this worked in Massachusetts, and it can also work in Montana, Arizona, California, Colorado, Texas, and more."

We're trying to jump toward that national expansion because we see that there are communities that really could benefit from this programming. We


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want to think big and punch above our weight and get there as soon as we can, because now is the time to do it. We also explicitly want to use our programming to address underserved and underrepresented populations in STEM. We see a huge opportunity in middle school, especially with girls and underrepresented populations in STEM; it's in middle school that most students are making the choice as to whether they're going to pursue STEM pathways in high school and beyond.

We've gone as young as fifth grade. It's a very long-term play. For industry and higher education partners, it takes some visionary people to say: "If we're addressing a fifth grader, they're probably not going to be part of our student body or workforce for 8-15 years, but that's where we have to start because that's where the pool of talent is largest."

Addressing additional students that otherwise might be intimidated by STEM is something that we very squarely have in our mission. We want more women and underrepresented populations in the industry because we need them.

LH: *What are the biggest challenges that you come up against?*

KM: After revamping the entire programme, a big challenge is marketing it to people who have never heard of us – and in some cases have never heard of photonics. We found sometimes people feel that what they're doing is best and there's a "not-invented-here" mentality. They're worried about someone else coming in and telling them what to do. However, Montana has a very active photonics cluster, but the mentality was: "Hey, let's not reinvent the wheel if it works, and we can just plug it in and go with it." They also said that time is of the essence and we've got to get people now. Since SparkAlpha has been proven in Massachusetts, they didn't see any reason it couldn't work in Montana. We're piloting with two teachers in Montana now, and we've already had several additional teachers in Montana reaching out to us asking if they could have follow-ons to the piloting. So hats off to Montana.

➤ SparkAlpha participants visit MACOM in Lowell, Massachusetts

One big challenge isn't with the K-12 teachers – who are our ultimate users – but with getting to them, because there are often quite a few gatekeepers along the way. Often the refrain is teachers are too busy and we don't want to overwhelm them. But we found that there are teachers who are very excited about this and will make the time and the headspace to implement it.

Especially with STEM teachers, they immediately see that this is how they can show students and their guardians that what they're learning is relevant to their future and relate it to cool things that are happening in the world right now. One teacher told us the hardest question they ever get is: "Why am I learning this?" Now they have an answer.

We find it can be hard to reach those teachers, and sometimes we get screened out. But there are very few people coming to K-12 schools with a proposition like ours. Through our grant, schools are getting free programming in perpetuity related to a society-defining technology that is very much top of mind right now across the world. People generally understand this is something we should bring to our teachers and something we should focus K-12 efforts on, but it is still a struggle for us to get those connections sometimes.

LH: *How can people get involved, whether they are teachers, students, or industry professionals?*

KM: The crux of this programme is the teachers. We ask teachers to reach out to us through our website or social media, and we will work with them and their administration to evaluate the fit. Students are a great judge of where in their school this could work, but they're going to need to get us in contact with a teacher or administrator. Administrators know the teachers in their schools or districts who are likely to be very good fits for this.

Industry or higher education institutions can get in touch to be partners for some of the virtual or in-person visits. But at the end of the day, it all comes down to finding the teachers to run it. We are open to teachers broadly – anybody who's interfacing with students. We can implement SparkAlpha with faculty at two- or four-year institutions. We have run it in community colleges in introductory engineering programmes. It can also be done in summer programmes and after-school programmes, and we're talking with some folks about running it in museums and libraries. It's very flexible, but it does need a champion to take and implement it.

That's our big ask to anyone right now who's interested in this programme. Help us get to those teachers who will adopt it, and then the sky's the limit from there.

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Advancing the semiconductorisation of photonic chip packaging

The PIC industry needs scalable, cost-efficient packaging processes suitable for high volumes, like those in traditional semiconductor manufacturing. The Chip Integration Technology Center (CITC) and vario-optics are working on multiple projects to this end, including co-packaging EICs and PICs on a glass substrate, and evanescent coupling into polymer waveguides.

BY NIKOLAUS FLÖRY & VALENTIN STRÄSSLE, VARIO-OPTICS, SANDER DORRESTEIN, CITC, AND TAYNARA DE OLIVEIRA, TNO DELFT

OVER THE LAST DECADE, PICs and related technologies have matured tremendously and found use in a multitude of devices. Silicon photonics platforms, for example, have expanded their range of applications beyond transceivers to photonic computing, biomedical sensing, optical interconnects, and consumer applications.

The recent push towards adopting optical solutions in AI/ML hardware has further spurred the development of multi-chip modules that require high-density electrical and optical interconnects. These upcoming generations of PIC designs present common challenges in electrical and optical assembly and packaging, namely: increasing density (more functions per unit area); increasing bandwidth and reaching higher data rates while maintaining signal integrity; and developing cost-effective assembly processes for high-volume manufacturing.

So far, state-of-the-art assembly technologies developed for foundry-produced PICs have focused primarily on supporting businesses with prototyping, low-volume manufacturing, and fibre pig-tailing (Figure 1). This has resulted in a poor level of standardisation and highly complex systems and processes that are only suitable for low volumes, making it challenging for new companies to adopt these methods and establish a viable business model in the market.

Another factor contributing to this landscape is that PIC products need to be considerably differentiated, both to achieve their technological aims and to stand out commercially. However, this leads to high assembly costs, especially compared to those in the established semiconductor industry; assembly makes up about 80 percent of the total costs of an integrated photonic device, compared with just 20 percent for typical semiconductor devices. To provide cost-effective photonics products – and thus keep up with increasing demands in the future – assembly methods must be simplified and made scalable. Addressing these cost challenges is essential for PICs to transition from niche solutions to mainstream applications, especially in consumer electronics, telecommunications, and biomedical devices, where affordability and scalability are critical.

Fortunately, the semiconductor industry offers a range of assembly and packaging processes with proven scalability and cost efficiency, presenting valuable insights and methods that can be adapted for PIC packaging. However, integrated photonics has unique requirements, so these processes must be tailored to meet the specific needs of high-density optical interconnects. This adaptation process, termed the "semiconductorisation" of PIC packaging, focuses on simplifying assembly steps while enhancing accuracy and scalability.

For instance, streamlined assembly techniques, like automated passive alignment, can significantly reduce per-unit costs. Recent pilot projects show that simplified panel-level packaging can achieve cost reductions of up to 30-40 percent compared to traditional fibre pig-tailing and discrete component assembly. Such benchmarks offer a promising roadmap for further cost-cutting strategies as PIC technology scales to higher production volumes, potentially making photonic solutions more accessible for a range of applications.

Scalable co-packaging of chiplets

Supported by the Dutch Growth Fund PhotonDelta, the Chip Integration Technology Center (CITC) is developing a scalable panel-level assembly concept addressing many challenges of integrated photonics packaging. CITC is collaborating on this project with vario-optics, which provides the key optical interconnect technology. The concept utilises advanced assembly technologies from the semiconductor industry, but is tailored to co-package EICs and PICs in a single package. In other words, this programme adds the "optical element" of advanced assembly at the panel level.

This concept, shown in Figure 2, is based on a panel-level fan-out design, where electrical and optical chiplets are mounted on the panel. Electrical and optical redistribution layers (eRDLs and oRDLs) enable chip-to-chip and chip-to-world communications in both domains. An oRDL is produced on one side of the panel and an eRDL on the opposite side. Using through glass vias (TGVs) the electrical interconnects cross from one side of the panel to the other. A flip-chip bonding process mounts both EICs and PICs on the panel.

Once the panel is populated, the assembly is covered by an overmoulding compound to protect sensitive components. Single modules are then created by cutting the panel in a conventional wafer dicing process. After this step, the module's optical interface is accessible through a mechanical interface, which an optical connector can be plugged into, as shown in Figure 3. The end user can assemble the module according to the needs of their particular application, either in a land grid array or ball grid array.

Bearing in mind the key targets of scalability and cost-efficiency, every choice related to this packaging platform is made with the aim of simplifying the assembly process. This means

➤ Figure 1. Traditional way to optically couple to a PIC using direct attach fibre arrays units (FAUs). Such assemblies are suitable for companies seeking to assemble and package their (first) integrated photonic dies for prototyping. However, due to many discrete components involved, cumbersome footprints and loose fibres within the setup, such solutions are not suitable for mass-scale fabrication flows.

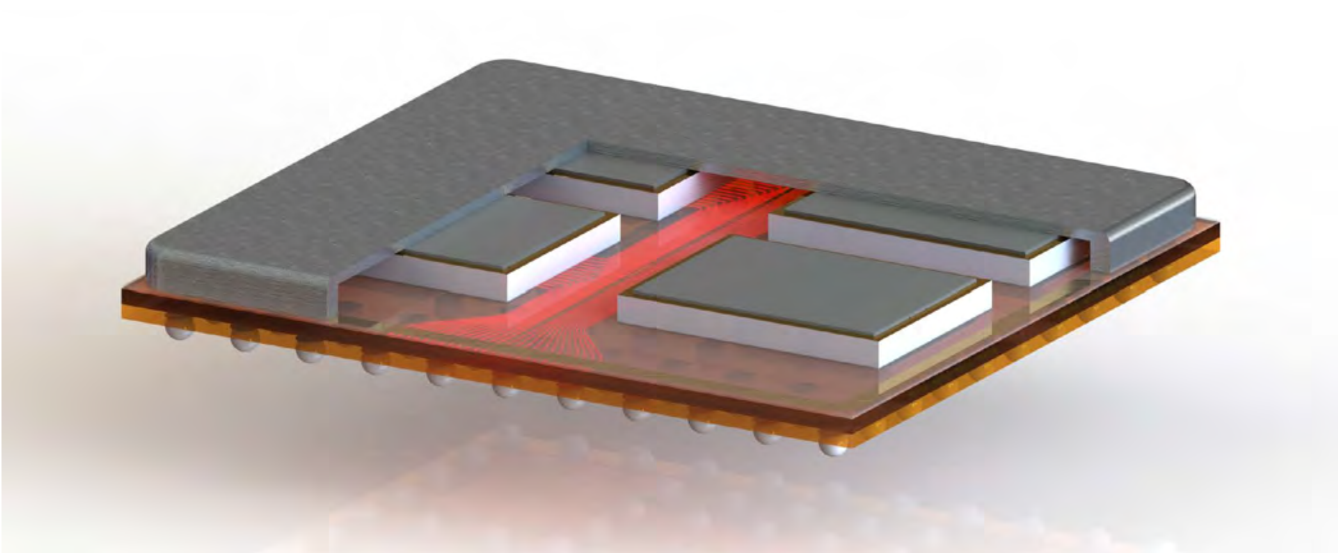


Figure 2. Concept for advanced packaging for integrated photonics. On the top side of a glass substrate there is an optical redistribution layer, and on the bottom side an electrical one. Combined they enable chip-to-chip and chip-to-world communication.

using known semiconductor assembly processes, realising relaxed alignment tolerances at the panel scale or wafer scale, and enabling short process times.

Photonic interposer based on PCBs

Many of the features and benefits of optical interposers stem from the semiconductor and microelectronics industry. The key difference in applying this concept to photonics is the addition of an oRDL that is compatible with various substrates (PCB, glass, silicon) and can be connected to photonic chips. Planar waveguides based on polymer or glass are an excellent candidate to fulfil these requirements.

One of the biggest challenges in coupling light into PICs is their inherently small mode field diameter (MFD). PIC platforms with very high confinement, such as InP, can exhibit MFDs of the order of only 1 µm. Coupling standard SMF-28 glass fibres to such small MFDs results in high optical losses due to the mode field mismatch. Although spot-size converters are available on most PIC platforms today, they typically require additional steps in the manufacturing process and exhibit large footprints, both of which increase the costs per unit area on the wafer. Moreover, to connect them to glass fibres or fibre arrays, additional fan-outs are necessary.

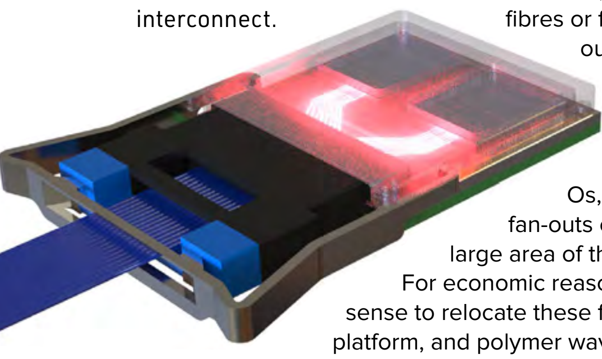


Figure 3. Optical module with pluggable fibre interconnect.

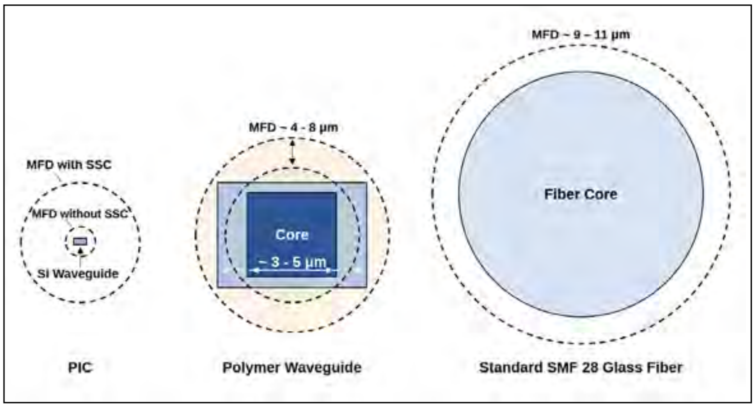
Depending on the pitch size (127 µm or 250 µm) and number of I/Os, spot-size converters and fan-outs consume a comparatively large area of the wafer. For economic reasons it therefore makes sense to relocate these features to another platform, and polymer waveguides can perform this task. They can be manufactured in large quantities on different substrates such as glass or silicon wafers or PCB panels using UV lithography. Polymer waveguides also require far fewer process steps, decreasing the costs per area. Larger features like spot-size converters, fan-outs, splitters, and combiners can therefore be fabricated at minimal cost.

Furthermore, the dimensions of the cores and thus the MFDs of the polymer waveguides can be varied without any additional effort, even on the same chip (see Figure 4). Thus, different PIC technologies like silicon photonics, silicon nitride, and InP as well as glass fibres can easily be connected. All these capabilities make polymer waveguides a first-class technology platform for hybrid integration and photonics at the PCB and interposer level.

Standard PCBs can include features such as high-speed RF interfaces, (glass) interposers, thermal dissipation layers, and electrical vias. Depending on the application, the polymer waveguides can be fabricated on top of the PCBs or sandwiched into them to form the optical connections of the electro-optical board. The PCB can also be substituted with other carriers such as silicon wafers or glass sheets. As polymer waveguide technology has advanced, it now supports single-mode operation at most common wavelengths (O-, C-, 850-nm-band). Moreover, polymer waveguides show high power damage thresholds, good environmental stability, and compatibility with reflow soldering processes.

Low-loss coupling: the holy grail

There are several ways of optically connecting PICs to oRDLs: edge coupling, surface grating coupling, and surface coupling by adiabatic or evanescent field couplers. The most important factors in choosing a coupling technique are: alignment



➤ Figure 4. Planar polymer waveguide platform. Typical mode field diameters are: 1 µm for InP; 2 µm for silicon nitride; about 10 µm for SMF28 glass fibre; and adjustable between 4-8 µm for polymer waveguides.

accuracy requirements, optical losses, wavelength variation sensitivity, polarisation sensitivity, and testing possibilities. Figure 5 compares the advantages and disadvantages of different optical coupling schemes.

Edge coupling is a well-established scheme suitable for a variety of PIC technologies. Many concepts have been developed to overcome tricky alignment routines. In the H2020 project QAMeleon, for example, vario-optics developed a micro-machined silicon carrier to act as a substrate for both an active InP chip as well as a passive polymer fan-out circuit (see separate box). The 3D patterned carrier enables highly accurate passive alignment of the optical parts.

At the same time, recent improvements in assembly equipment and alignment routines have made active alignment more compatible even with high-volume manufacturing. CITC is investigating test vehicles in which a fibre assembly unit (FAU) with standard SMF-28 fibres is bonded to a polymer waveguide chip (Figure 6). The technique involves actively aligning the outermost fibres of the FAU to optical loops on the polymer chip. The two parts are bonded together when the signal of both loops is optimised. In a second step, the package is positioned and bonded to a silicon nitride PIC with similar alignment loops and small MFDs of 2 µm.

This configuration has demonstrated coupling losses on the order of only 1 dB per facet (polymer-to-PIC) – significantly better than direct fibre-to-PIC connections, which typically have coupling losses of close to 3 dB. Polymer waveguide interposers therefore meet the requirements for low-loss fibre-to-chip coupling or even chip-to-chip coupling.

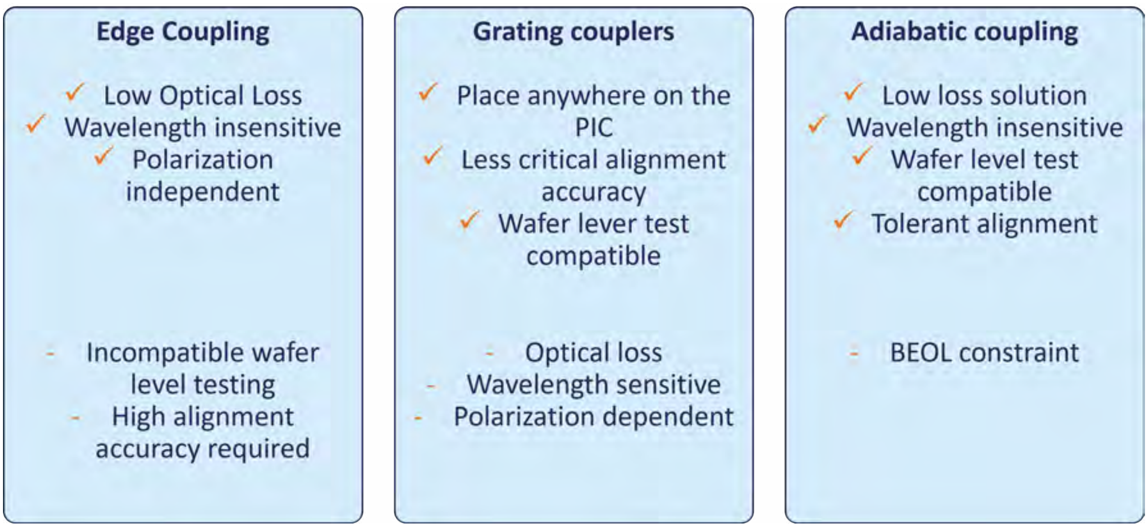
However, there are limits to how much this technique can reduce the overall system losses, even with tailored polymer waveguide geometries. This is because there are geometrical limitations in optimising for two different interfaces within one waveguide, as well as limits to alignment accuracy. Using an alternative approach of evanescent field coupling offers a viable solution for circumventing these constraints.

Evanescent surface coupling

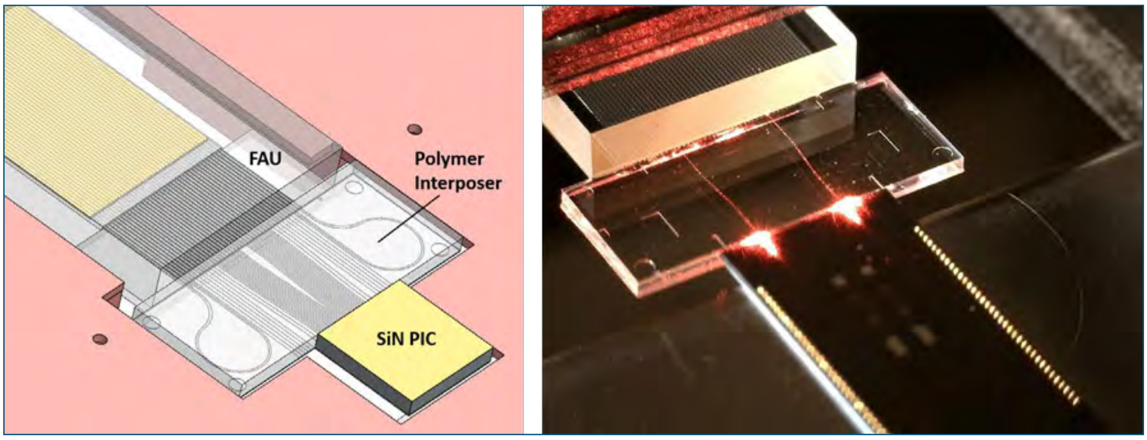
Evanescent coupling, commonly also referred to as adiabatic coupling, involves an energy transfer between overlapping evanescent fields in two waveguides. This technique relies on a near-field interaction at the surface interface, so it is essential to minimise the gap between the waveguide cores to increase the energy efficiency of the transfer. Both cores must therefore be exposed to allow for a low-loss coupling.

Figure 7 presents a schematic representation of the evanescent field coupling mechanism. In this process, light is out-coupled from the silicon nitride PIC via an inverted taper, which narrows to an optical tip, forcing the mode field out of the waveguide. During the assembly phase, this tapered section is aligned in proximity to the polymer waveguide on the oRDL, enabling efficient mode transfer whereby the light is captured and guided towards the package interface.

Results of design simulations highlight how optimising both the silicon and polymer waveguide structures can yield exceptionally low loss. For instance, using a 420 µm taper length with high refractive index contrast polymers results in coupling



➤ Figure 5. Comparison of different coupling schemes.



➤ Figure 6. A concept for simultaneously interfacing a polymer interposer with both an FAU and a small-mode-field PIC silicon nitride PIC, involving active alignment.

losses as low as 0.2 dB at a wavelength of 1550 nm. Extending the taper length to 900 µm further reduces the coupling loss to just 0.08 dB, which is very promising compared to the state of the art.

Furthermore, redesigning not only the taper but also the overall chip – including adjustments to refractive index contrast, cladding materials, and other factors – can minimise the footprint of these interconnects to hundreds of microns while maintaining coupling efficiency above 95 percent.

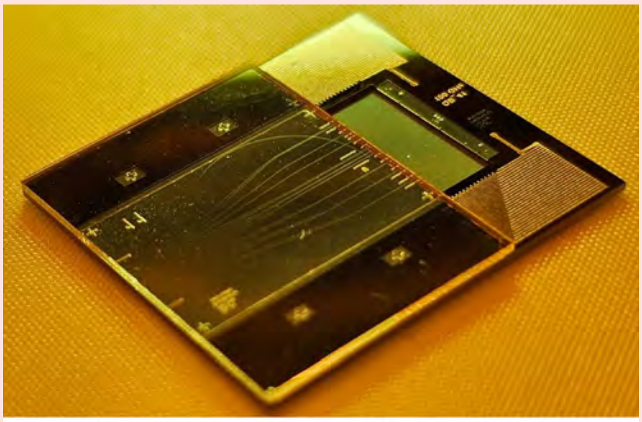
This approach also relaxes lateral alignment tolerances to approximately ±2 µm for both transverse electric (TE) and transverse magnetic (TM) polarisations. Previous experimental studies,

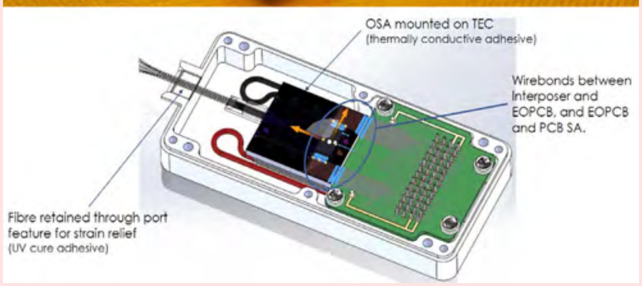
QAMeleon Project

THE H2020 QAMeleon project aimed to scale metro and core networks by providing faster, cheaper, and more compact optical components for generating, switching and receiving light under an automated, software-defined-networking (SDN) enabled environment. The different hardware developments are aimed at achieving ultra-high rates of up to 128 Gbaud and more than 3 Tb/s capacity on a single carrier, while reducing the energy consumption per bit.

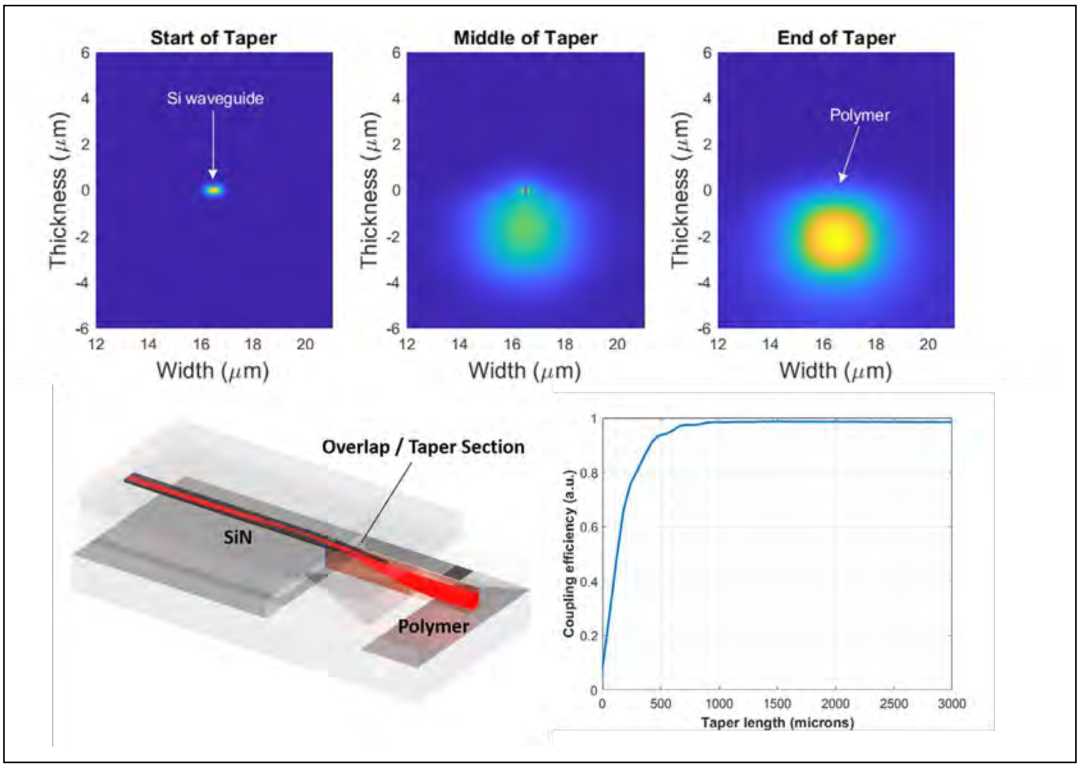
An essential part of this network is the InP-based wavelength selective switch, which can route different wavelengths from a single input into any one of N multi-wavelength outputs. The InP waveguides used, which exhibit a small mode field diameter of around 1 µm, are very challenging to connect directly to glass fibres, and would result in low density of optical I/Os limited by fibre cladding diameter. Therefore, InP chips were instead connected to an optical interposer, which can convert the mode field to match that of glass fibres. In addition, the optical I/Os were fanned out to make the best possible use of the space on the PIC.

The QAMeleon project developed a solution for a passive alignment between the PIC and optical interposer with <1 µm alignment accuracy, by placing the PIC and the polymer waveguide chip on a 3D patterned carrier. The carrier has different, very well-defined reference planes so the optical axes of the InP and polymer cores are aligned. Additional mechanical stops and alignment marks help to assemble the parts with an accuracy better than 1 µm.





Standard fibre arrays can be attached to the polymer optical interposer. The carrier is also equipped with electrical fan-out to connect the PIC electrically. This package consisting of PIC, waveguide chip, and electro-mechanical carrier form an electro-optical subassembly that can be easily connected to other components in a network.



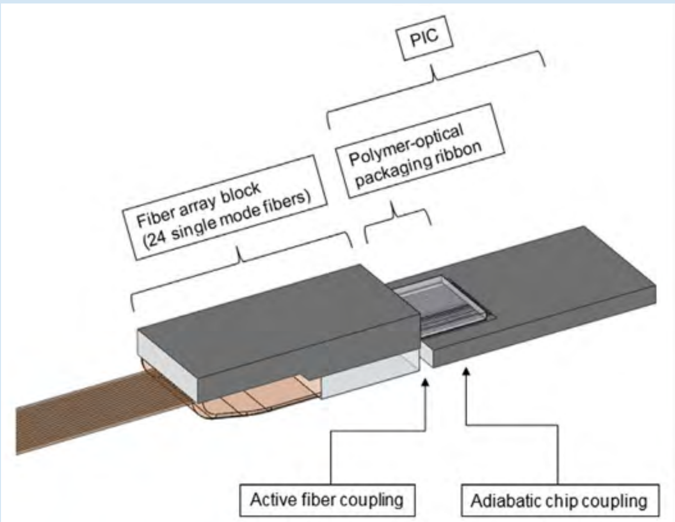
➤ Figure 7. Results from optical simulations of an adiabatic coupling interface. The modelling allows the extraction of critical taper dimensions on silicon nitride. Coupling losses of ~0.08 dB (98 percent coupling efficiency) can be achieved for a taper length of 1000 μm at a wavelength of 1550 nm. This is much more efficient compared to the industry standard of 1 dB for regular edge-coupling interfaces.

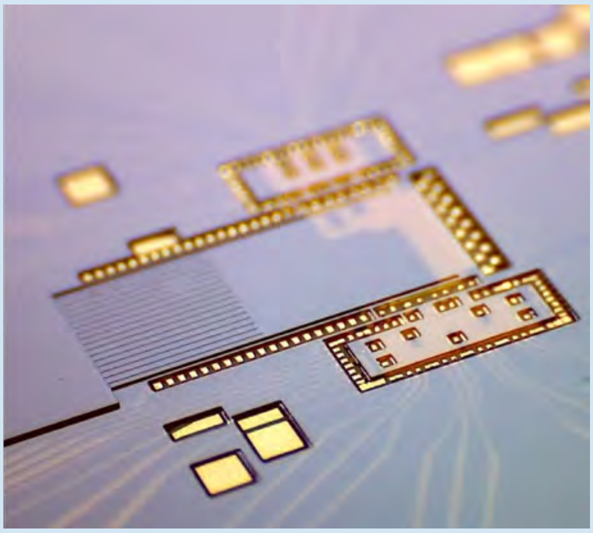
ICT-STREAMS Project

ADIABATIC COUPLING allows efficient light transfer from tapered silicon waveguides to the polymer waveguide platform. Prior works using FAU-attached polymer ribbons achieved fibre-to-polymer-to-PIC coupling losses of < 1.2 dB (left picture, demonstrated within ICT-COSMIC).

The H2020 ICT-STREAMS project focused on developing high-data-throughput communication between multiple computing nodes based on a silicon photonics platform using any-to-any optical connections. As part of the project, vario-optics developed a multi-socket optical PCB based on the polymer platform described in this article. The final oPCB consisted of an RF electrical interface with small metal pads (125 μm pitch) and a (transparent) polymer layer featuring optical waveguides with exposed cores (right picture).

The device achieved low insertion losses over a wide spectral bandwidth, as well as relaxed alignment tolerances of ± 2 μm. The broad operating wavelength range (> 100 nm) is particularly important for WDM applications. This system successfully demonstrated operation at a line rate of 50G per channel with an energy consumption of only 5 pJ/bit.





conducted independently by IBM and vario-optics, have already demonstrated the strong potential of this technique, achieving total coupling losses of less than 1.2 dB for a fibre-to-polymer-to-PIC setup, and showcasing the PCB-integration of adiabatic coupling interfaces, as demonstrated within the EU project ICT-STREAMS (see separate box).

While these results prove the viability of this scheme, previous realisations have been constrained by non-ideal planarity of PCB substrates and the limited availability of PICs with accessible core layers.In recent years, however, several foundries have added these features to their PDKs. Beyond that, the use of a glass substrate for both eRDLs and oRDLs is a great choice in terms of planarity for such an interface, finally allowing full exploitation of the advantages of evanescent coupling.

Outlook on scalable manufacturing for PIC packaging

Advanced and scalable panel-level processes, together with efficient coupling methods, hold great promise to fulfil the key requirements of future PIC packaging: low-loss optical interconnections with << 1 dB (20 percent) optical loss from PIC to oRDL; relaxed alignment tolerances >> 1 µm; and cost-effective assembly methods of PIC to substrates with automated passive alignment.

Both edge coupling and evanescent coupling schemes used in such a photonic interposer platform can provide excellent performance.

Each use-case requires a system-level evaluation to identify the most suitable coupling scheme, balancing efficiency, assembly tolerances, and most importantly cost per assembly.

In all cases, integrating both electronics and photonics in a single package is a key prerequisite for the successful semiconductorisation of PIC assembly and photonic packaging.

FURTHER READING / REFERENCE

- **Integrated Photonics Roadmap by CITC:** https://www.citc.org/resources/uploads/2024/04/CITC-Integrated-Photonics-Technology-Roadmap.pdf
- Electronic-photonic board as an integration platform for Tb/s multi-chip optical communication: https://doi.org/10.1049/ote2.12017
- Highly reliable polymer waveguide platform for multi-port photonic chip-packaging: https://ieeexplore.ieee.org/document/9501540

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Integrated photonics offers a promising route for quantum computing, communications and sensing. Which approaches are in development to bring about the quantum era?

Optimising materials and architectures to progress PICs

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PICs are a powerful and versatile technology; how might they help to transform healthcare, transport and other aspects of daily life?

PIC progress in the spotlight at 50th ECOC

Research into integrated photonics had barely begun when the first ECOC took place in 1975, but this year PICs were front and centre throughout the conference and exhibition.

BY LAURA HISCOTT, EDITOR PIC MAGAZINE

IN TODAY'S ERA of rapid technological progress, it is always possible to look back and be awestruck by the huge strides that have been made in a short time. But milestone anniversaries often serve as useful prompts for this kind of reflection, and this opportunity was not lost at the 50th edition of the European Conference on Optical Communication (ECOC), which took place in Frankfurt this September.

It was a record-setting event in many ways, with over 1800 conference participants attending from more than 30 countries – more participants than at any previous ECOC. There were also over 500 talks and more than 2000 pages of conference proceedings, compared with just 74 papers presented at the first event in London in 1975. The goal in focus at that first ECOC was Mb/s transmission speeds, but the industry is now setting its sights on Pb/s, a staggering nine orders of magnitude higher.

But the progress is perhaps even starker for the PIC industry specifically, considering that photonic integration was not even on the agenda in London in 1975. Indeed, research into the field had barely begun at that time, but it appeared as a firm fixture in Frankfurt this year.

Meint Smit, widely considered an early pioneer of PICs, opened the special symposium on 50 years of ECOC with an overview of the progress made in indium phosphide PIC technologies. Meanwhile, JePPIX, the Joint European Platform for Photonic Integration of Components and Circuits, which Smit founded, co-hosted an anniversary of its own; together with ePIXfab, they held the 15th European Photonic Integration Forum (EPIF).

AI was, of course, a running theme throughout both the conference and the exhibition, with numerous companies demonstrating innovations to boost transmission speeds for the data-hungry new world. In acknowledgement of this major topic, the event organisers had AI generate a song to celebrate the 50th ECOC – something that the attendees of the very first conference back in 1975 might not have been able to imagine.

During one of the plenary sessions, Joyce Poon, head of photonics architecture at Lightmatter, spoke about the company's interconnect product Passage, which incorporates 3D co-packaged optics to enable higher-bandwidth communications between chips – essential for AI applications.

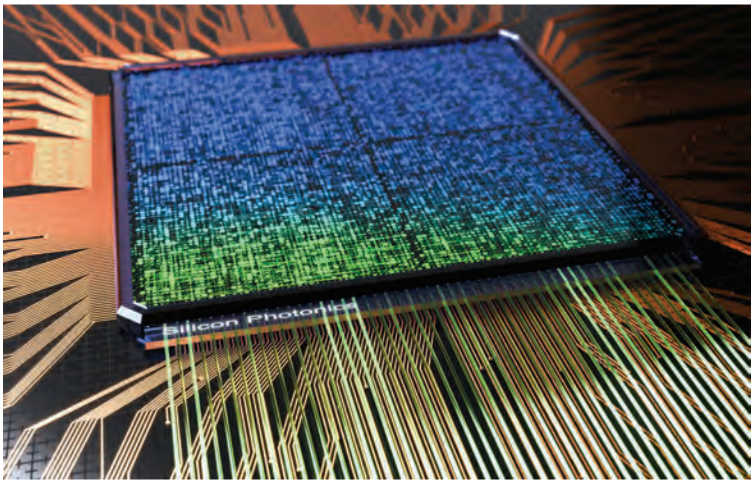
But Poon also flipped the script, asking not only what photonics can do for AI, but also what AI can do to advance photonics. To this end, Poon and her team are currently developing an AI-based photonics design assistant called PhIDO (Photonics Intelligent Design and Optimisation). The team hope to progress towards a tool that can interact with designers and speed up design optimisation, eventually generating first-time-right layouts and lowering the costs and barrier to entry in photonics. Closing her talk, Poon spoke about her optimism that we might see the emergence of an AI "super-engineer" within a decade, that could significantly accelerate progress in all branches of photonics research.

Attendees interested in PICs were also spoilt for choice when it came to the main schedule of presentations, with sessions dedicated to integrated photonics taking place every day of the conference. Klaus Jöns of Paderborn University opened a session on light sources for quantum communication with an overview of the "zoo" of different ways of achieving quantum light generation.

He first ran through several key figures of merit for these essential components, from the ability to generate background-free indistinguishable photons to the need for high brightness and tuneability to the desired wavelength. Jöns then described various sources, including 2D materials, colour centres, single atoms and ions, and spontaneous parametric down conversion. After summarising how well these techniques fit the essential criteria, he showed that quantum dots are a particularly promising light source, but with the caveat that they have benefitted from more years of research than 2D materials, for instance.

It is not only quantum applications that have a wide range of options for the underlying technologies. In a session on integrated sensing and communications, Antonella Bogoni from the Sant'Anna School of Advanced Studies in Pisa spoke about her group's aim of developing miniaturised radar systems based on integrated microwave photonics.

She compared several different material platforms that could be used for this task, showing that indium phosphide heterogeneously integrated with lithium niobate on insulator looks like the most promising option in terms of conversion performance and RF signal distribution. Although the technology is in its early stages of development, Bogoni emphasised that there is a lot of interest in the benefits that microwave photonics can bring to radar, so this will hopefully drive rapid progress in the area.



While ECOC is, of course, all about communications, these talks and others showcased the rich variety of other applications that PICs are now branching into. In another plenary session, Roel Baets, a PIC pioneer who previously worked at Ghent University and imec, highlighted that, at imec alone, PICs are being developed for everything from LiDAR to biosensing to optical coherence tomography. However, Baets also pointed out that there is a long way to go, noting that, when looking for non-transceiver PIC products, he and his colleagues were only able to find six that have so far made it to market.

In this vein, Baets set out his vision for "silicon photonics industry 4.0," highlighting the need to break down supply chain barriers for start-ups and scale-ups, despite diversifying technologies and markets. Some of the key ingredients he recommended to move in this direction included a decentralised open-access foundry and supply chain model, and standardised modules that can be reused for different applications. Baets concluded his talk with a call to mobilise resources towards making the diverse and exciting potential of PICs a reality.

This message echoed throughout the conference. With the ECOC lanyards featuring the NOKIA logo – a reminder of the connectivity giant's recent acquisition of Infinera – it appears that PICs are well established, having made themselves indispensable in communications. But there are also plenty of opportunities for growth across a broader range of markets. This is an exciting phase for any industry, but perhaps also an uncertain one. To really take off, these technologies will need much more investment and development. But the potential future fruits of those efforts, as envisioned and laid out by today's innovators in the field, will surely be worth it.

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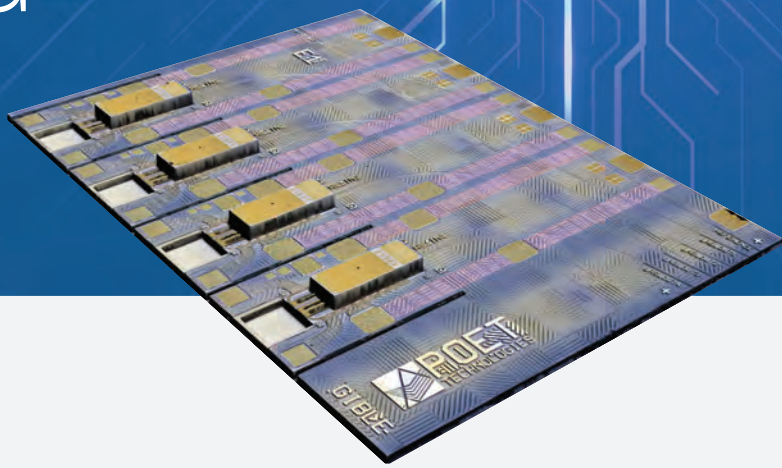

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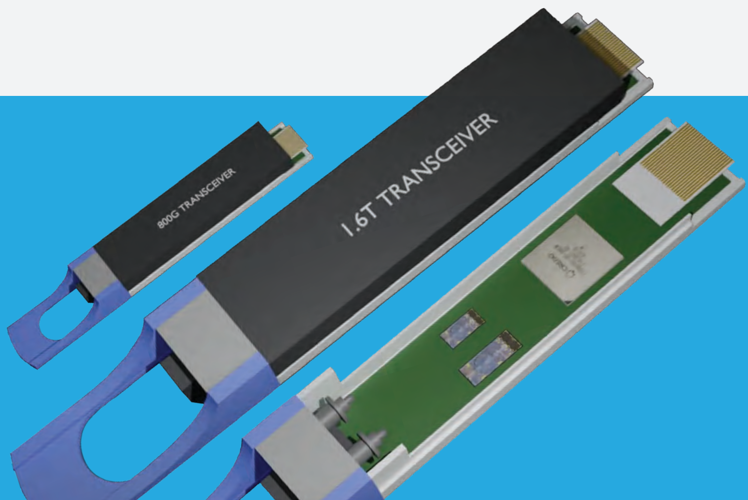

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