

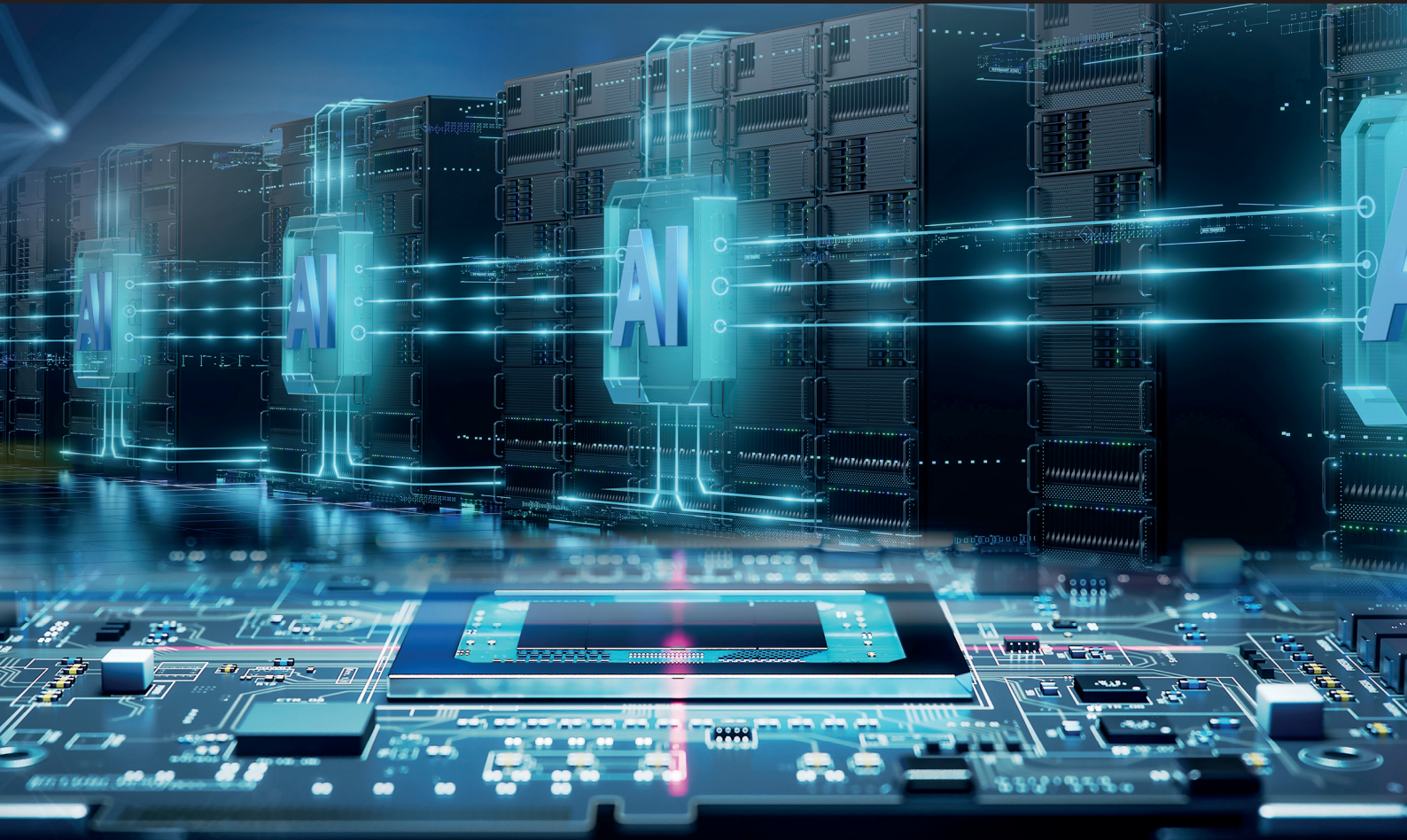


PHOTONIC INTEGRATED CIRCUITS

ISSUE IV 2026

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**FROM PROCESS DEVELOPMENT
TO HIGH-VOLUME MANUFACTURING
FOR SILICON PHOTONICS
& CO-PACKAGED OPTICS**

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Scaling photonics for AI

Artificial intelligence is accelerating one of the most significant transitions the photonics industry has experienced in decades. The conversation is no longer centred on whether photonic integrated circuits can deliver the performance required for next-generation communications. Instead, attention is shifting towards how the industry can manufacture, integrate and deploy these technologies at the scale that AI infrastructure demands.

As AI clusters continue to grow, every part of the optical ecosystem is under pressure. Greater bandwidth, lower latency, improved energy efficiency and higher integration density are no longer desirable goals—they are fundamental design requirements. Meeting them requires advances that extend well beyond individual photonic devices and into manufacturing, packaging, simulation and system architecture. This broader perspective defines the focus of this issue.

One theme that emerges repeatedly is the growing importance of integration. Future optical systems will depend on the ability to combine multiple material platforms, electronic and photonic functions, and increasingly sophisticated packaging technologies into manufacturable, scalable solutions. As photonic systems become more complex, success will rely on treating optics, electronics, thermal management and packaging as interconnected engineering challenges rather than isolated disciplines.

Manufacturing is becoming just as important as device innovation. As production volumes increase, yield, process variation, contamination control and production efficiency

are emerging as decisive factors in determining the commercial success of silicon photonics. The industry's next advances will depend not only on better devices, but on manufacturing technologies capable of delivering consistent performance at wafer scale.

At the same time, photonic integration continues to unlock entirely new capabilities. Rather than simply making optical systems smaller, integrated photonics is enabling new approaches to sensing, measurement and data acquisition that were previously impractical. These developments demonstrate how PICs are evolving from component-level innovations into technologies that fundamentally reshape system performance and engineering workflows.

Underlying all of these developments is a broader shift in engineering practice. The complexity of AI-era optical systems demands multidisciplinary design approaches that bring together simulation, manufacturing, packaging and photonic integration from the earliest stages of development. As these disciplines become increasingly interconnected, collaboration across the value chain will be essential to translating research into deployable infrastructure.

The photonics industry has spent years proving what integrated optics can achieve. The challenge now is delivering those capabilities reliably, efficiently and at the scale required by the AI era. The innovations featured in this issue reflect an industry moving beyond individual breakthroughs towards the practical realities of building the next generation of optical infrastructure.



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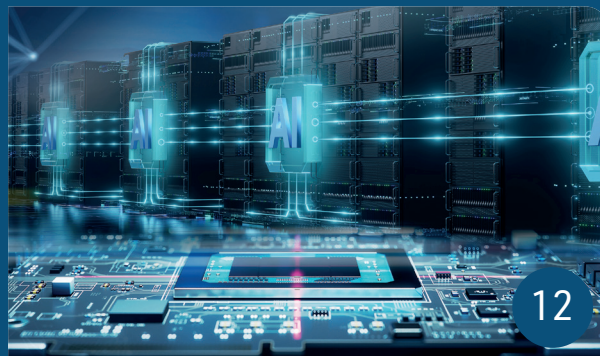
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IEEE backs micro-transfer printing

Researchers say micro-transfer printing could enable scalable heterogeneous integration of diverse materials on silicon photonics platforms, paving the way for more advanced photonic integrated circuits.

A NEW study published in the Journal of Lightwave Technology highlights micro-transfer printing (MTP) as a promising approach for enabling heterogeneous integration in silicon photonics, offering a pathway to more advanced photonic integrated circuits (PICs) for artificial intelligence, communications and sensing applications.

The research, led by scientists at Ghent University–imec, examines how MTP can overcome one of silicon photonics' longstanding challenges: integrating diverse material systems onto CMOS-compatible photonic platforms.

While silicon photonics benefits from mature semiconductor manufacturing processes, conventional silicon materials cannot deliver all the optical functions required for advanced photonic systems, particularly efficient on-chip light sources.

According to the study, MTP enables thin-film devices, or “coupons,” fabricated from materials such as indium phosphide (InP), gallium arsenide (GaAs) and lithium niobate (LiNbO_3) to be transferred onto silicon photonic wafers.

This allows each material system to be optimized independently before being integrated into a single photonic platform.

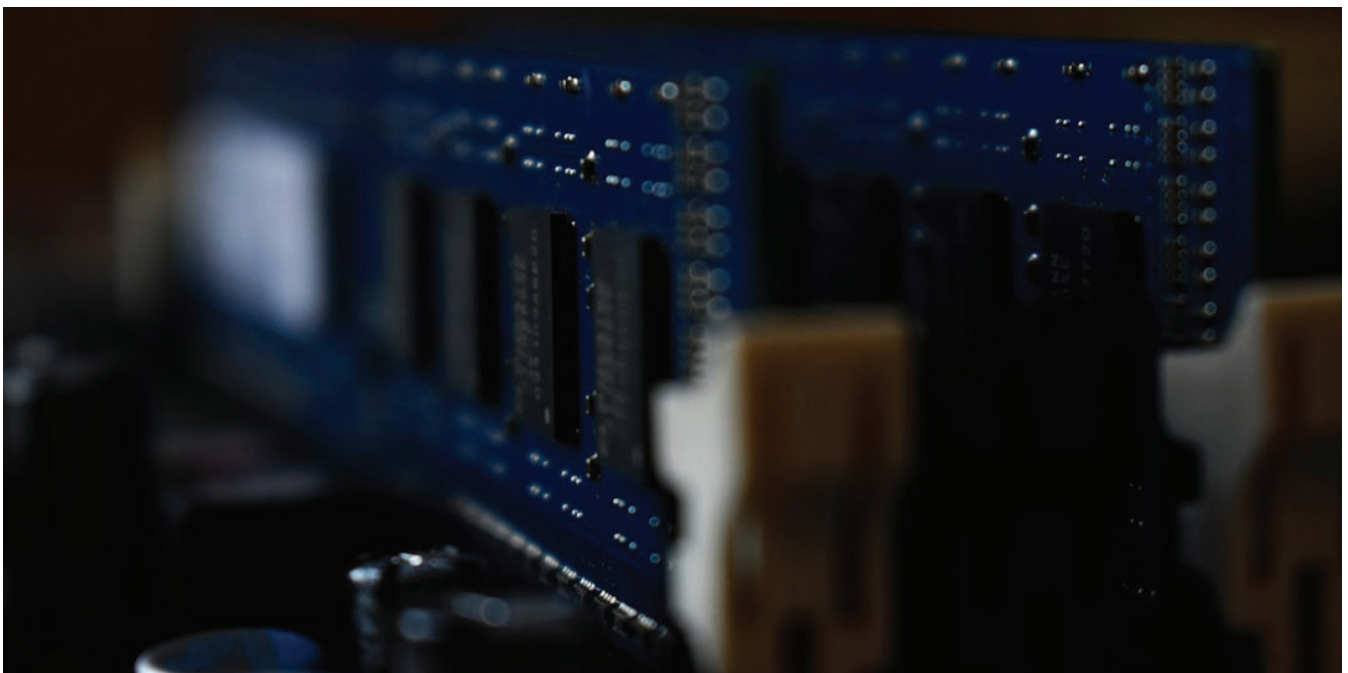
“Among the various approaches being pursued for enabling wafer-scale heterogeneous integration, MTP is an emerging highly versatile technique that combines benefits of die-level assembly with wafer-scale processing,” said Ir. Ye Chen of Ghent University–imec.

The paper highlights several recent demonstrations of the technology, including integrated silicon photonic

engines combining optical and microwave signal processing, InP lasers integrated with silicon nitride waveguides, lithium niobate modulators on silicon photonic circuits, and heterogeneous electronic-photonic receiver platforms.

The authors also discuss ongoing efforts to develop a pilot manufacturing line for large-volume industrial production while identifying remaining challenges related to yield, reliability, throughput and ecosystem development.

The researchers conclude that continued advances in micro-transfer printing could accelerate the commercialization of next-generation silicon photonics by enabling scalable heterogeneous integration using existing semiconductor manufacturing infrastructure.



New framework advances PIC design

Researchers develop a theoretical framework that enables directional light scattering in disordered materials, opening new possibilities for photonic integrated circuits, optical communications and LiDAR.

RESEARCHERS AT Seoul National University, in collaboration with the University of Seoul, have developed a new theoretical framework that enables precise control of light scattering in disordered optical materials, extending photonic design beyond conventional crystal structures.

The framework, known as Non-Hermitian Statistical Crystallography, incorporates not only refractive properties but also optical gain and loss, allowing researchers to suppress light scattering in some directions while enhancing it in others.

Unlike traditional approaches based on periodic crystal structures, the new theory applies to hyperuniform disordered materials structures that appear random at small scales but maintain uniformity over larger distances.

The researchers say this provides a new route to designing scattering behaviour in open optical systems where energy can be absorbed or amplified.

The team identified the conditions required to maintain scattering suppression while tailoring directional scattering through the spatial relationship between refractive index and optical gain or loss.

The approach also enables scattering patterns with rotational symmetries that are difficult to achieve in conventional energy-conserving materials.

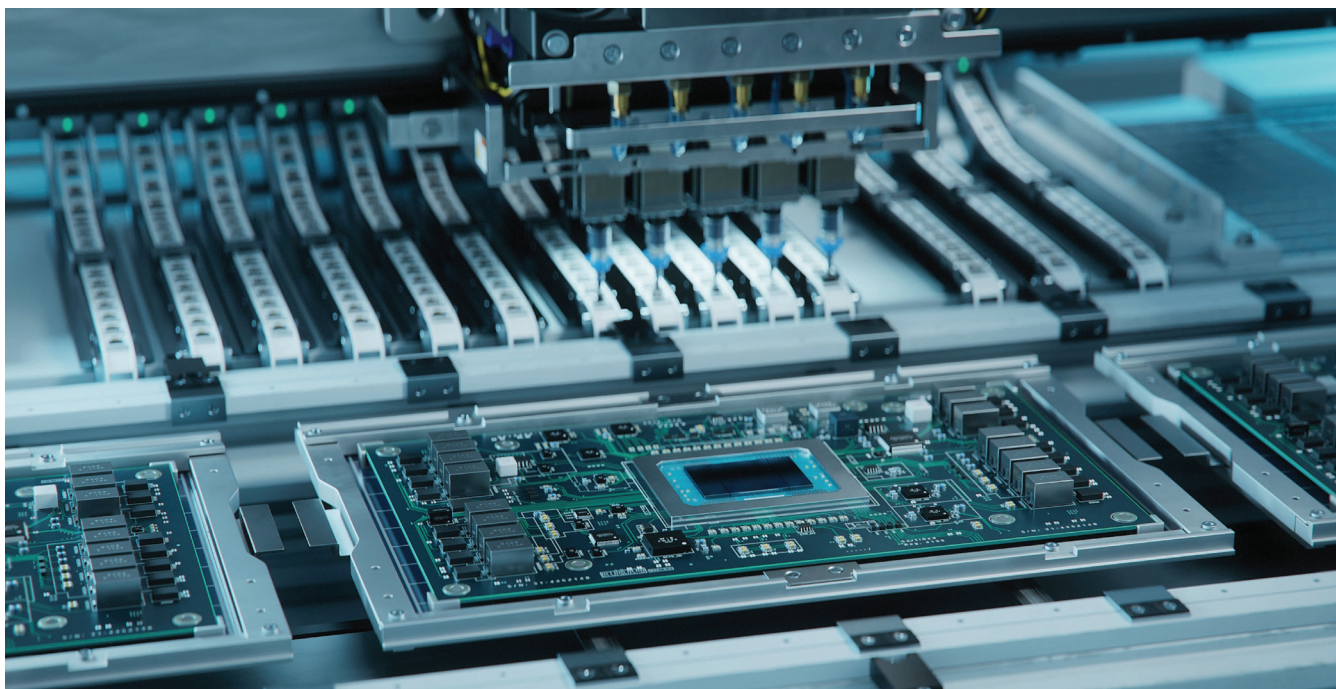
According to the researchers, the framework could support the development of next-generation photonic devices for optical communications, photonic integrated circuits (PICs), LiDAR, optical sensing,

displays and medical imaging.

Potential applications include reducing unwanted reflections in optical communication components, improving directional optical sensors and creating photonic devices that are more tolerant of manufacturing variations.

“This study connects two research areas non-Hermitian wave physics and hyperuniform materials and presents a new framework for designing the directionality and symmetry of scattering even in disordered open materials without periodicity,” said Professors Sunkyu Yu, Namkyoo Park and Xianji Piao.

The researchers plan to validate the theory using physical material platforms and extend the work to investigate strong multiple scattering and non-Hermitian band phenomena.



Shanghai backs SiPh innovation

Shanghai's Zhangjiang High-Tech 895 Incubator is strengthening the city's silicon photonics ecosystem by supporting startups developing optical interconnects, optical computing, and AI chip technologies.

SHANGHAI IS accelerating the development of its silicon photonics ecosystem through the Zhangjiang High-Tech 895 Incubator, which is supporting startups in optical computing, optical interconnects, and next-generation AI infrastructure.

The incubator has nurtured more than 1,600 technology companies since its launch in 2015, helping startups move from laboratory research to commercial deployment through funding, industry partnerships, and entrepreneurial support.

Among the companies benefiting from the ecosystem is optical computing

specialist Lightelligence, which relocated its operations from Boston to Shanghai in 2020.

The company cited Zhangjiang's integrated semiconductor supply chain, manufacturing capabilities, and support for emerging technologies as key factors behind the move.

Lightelligence CEO Shen Yichen said silicon photonic chips could account for more than 30% of chips used in computing centers within five years, compared with less than 3% today, driven by growing demand for AI infrastructure.

The ecosystem also supports startups such as optical computing company Lightning AGI, which leverages Zhangjiang's close network of design, tape-out, testing, packaging, and application development capabilities to accelerate commercialization.

Beyond silicon photonics, Zhangjiang has built a comprehensive semiconductor ecosystem spanning chip design, advanced packaging, testing, optical interconnects, thermal management, and power delivery technologies, positioning Shanghai as a key innovation hub for next-generation AI hardware.

EnSilica boosts photonics expansion

FABLESS SEMICONDUCTOR company EnSilica has announced plans to raise up to £15 million to support growth across its satellite communications and photonics businesses.

The fundraising, comprising a placing, subscription and retail offer, will provide capital to expand engineering capacity, support new customer programmes and accelerate development activities in high-growth markets.

EnSilica said the investment will help advance its SatCom application-specific standard product (ASSP) roadmap, increase satellite payload and positioning, navigation and timing (PNT) engineering capability, expand photonics opportunities and provide manufacturing working capital.

The company is also targeting growth in the photonic integrated circuit (PIC)

sector, where optical technologies are increasingly being adopted to address the bandwidth and power demands of artificial intelligence (AI) data centres.

EnSilica highlighted its data-centre photonics controller ASIC development programme with Oriole Networks as part of its expanding activity in this market.

Photonic technologies are gaining momentum in AI infrastructure due to their ability to deliver higher bandwidth and lower power consumption compared with conventional electronic interconnects.

Ian Lankshear, CEO of EnSilica, said the company has seen strong demand from customers in the space and photonics sectors and that the funding will enable it to pursue new opportunities and support ongoing growth.

The announcement follows EnSilica's recent business update, in which the company reported increased contract activity and a growing pipeline of opportunities across its target markets.



PICs advance next-generation sensing

Integrated photonic circuits are enabling more compact, precise and scalable sensing systems for applications ranging from metrology and vibration monitoring to FMCW LiDAR.

PHOTONIC INTEGRATED CIRCUITS (PICs) are continuing to expand their role in next-generation sensing and measurement by integrating multiple optical functions onto a single chip.

Compared with conventional optical systems, PICs offer greater precision, reduced size and weight, improved robustness and immunity to electromagnetic interference.

Advances in silicon photonics, silicon nitride and indium phosphide platforms are supporting applications including precision metrology, vibration sensing and frequency-modulated continuous-wave (FMCW) LiDAR.

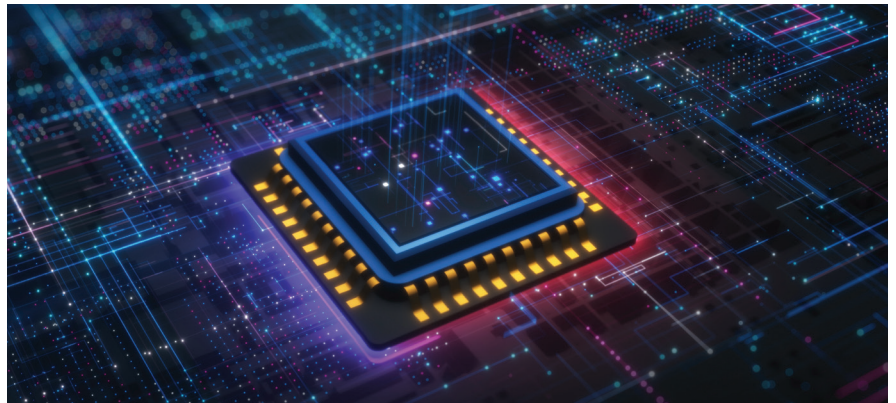
By enabling parallel optical processing and high-speed data acquisition, PICs are helping deliver more accurate and scalable sensing solutions for

industrial automation, aerospace, structural health monitoring and autonomous systems.

Despite challenges such as packaging, thermal management and system integration, continued progress in photonic manufacturing and foundry

ecosystems is expected to accelerate adoption.

As the technology matures, integrated photonics is set to play an increasingly important role in next-generation sensing and measurement across a wide range of industries.



RIT joins laser technology hub

THE ROCHESTER/FINGER LAKES region of New York has secured a \$15 million National Science Foundation (NSF) Regional Innovation Engine award to establish a national hub for laser technology development, with the Rochester Institute of Technology (RIT) serving as a key partner.

The STELLAR (Science, Technology and Engineering for Laser and Laser Applications Research) initiative will receive additional support through \$16 million in New York state funding and aims to build a globally competitive ecosystem for laser research, manufacturing, education, and commercialization.

RIT researchers will contribute expertise in photonic integrated circuits

(PICs), semiconductor fabrication, optical manufacturing, and photonics education.

Stefan Preble, a professor of microsystems engineering and an expert in photonic integrated circuits, is part of the STELLAR leadership team.

The initiative will leverage RIT's semiconductor nanofabrication capabilities, including facilities for fabricating semiconductor, laser, and photonic devices, to support next-generation optical technologies.

The STELLAR hub brings together universities, industry partners, startups, and economic development organizations across the Rochester region, including the University of

Rochester's Institute of Optics and Laboratory for Laser Energetics, Monroe Community College, NextCorps Luminate, and Greater Rochester Enterprise.

The program aims to address growing demand for domestic capabilities in laser and photonics manufacturing, while developing the skilled workforce needed to advance technologies used in communications, advanced manufacturing, healthcare, defense, and optical sensing.

By strengthening collaboration between research institutions and industry, STELLAR is expected to accelerate innovation in integrated photonics and help expand the U.S. supply chain for advanced optical technologies.

Hungarian team advances neurophotonic

A new laser microscopy platform has enabled researchers to observe neuronal activity in three dimensions, leading to new insights into how the brain processes information.

AN INTERNATIONAL research team led by Dr. Attila Losonczy of UT Southwestern Medical Center and Dr. Balázs Rózsa of BrainVisionCenter and the HUN-REN Institute of Experimental Medicine has combined a breakthrough in neurophotonics with new discoveries about brain function.

Published in *Neuron*, the team's new optical imaging platform enables high-speed, three-dimensional recording of neuronal electrical activity using genetically encoded voltage indicators.

The technology allows researchers to monitor individual neurons and their dendritic branches with high spatial and

temporal resolution across large tissue volumes in awake, freely behaving animals.

Unlike conventional electrode-based methods, the platform enables repeated long-term optical measurements over several months while maintaining signal quality.

The researchers say the approach provides an unprecedented view of neuronal activity and opens new opportunities for studying learning, memory and brain disorders.

Using the imaging system, the team reported in *Science* that dendrites the branching structures of neurons function as independent computational

units capable of simultaneously processing information about past experiences, current environments and future learning.

The findings challenge the traditional view of neurons as single processing units and suggest that individual dendrites dynamically contribute to information storage and computation.

Beyond fundamental neuroscience, the researchers believe the technology could advance studies into Alzheimer's disease, epilepsy and other neurological disorders while also inspiring new approaches to artificial intelligence based on distributed biological computing principles.



GF, Aeluma receive CHIPS funding

The U.S. Department of Commerce has selected seven semiconductor companies for up to \$874 million in funding, with GlobalFoundries and Aeluma receiving support for integrated photonics and related technologies.

THE U.S. DEPARTMENT of Commerce (DOC) has signed letters of intent with seven semiconductor technology companies for up to \$874 million in combined federal incentives under the CHIPS and Science Act, supporting technologies including integrated photonics, advanced packaging, substrates, materials and memory.

Among the recipients, GlobalFoundries (GF) is set to receive up to \$300 million the largest individual award to advance next-generation optical materials, wafer technology and advanced packaging.

The company said the funding will build on its recently introduced SCALE (Silicon Photonics Co-Packaged Advanced Light Engine) platform.

California-based photonics company Aeluma will receive up to \$30 million



to further develop its scalable, non-indium phosphide semiconductor manufacturing platform.

The technology is designed to support high-volume production of photonic components, including high-speed photodetectors and lasers, while helping to address supply chain constraints.

According to the Department of Commerce and the National Institute of Standards and Technology (NIST), the investments aim to strengthen U.S. leadership in critical semiconductor technologies that underpin advanced computing and AI infrastructure.

As a condition of receiving the funding, the Department of Commerce will acquire a minority, non-controlling equity stake in each of the seven companies.

China protects photonic chip designs

CHINA HAS revised its integrated circuit layout-design regulations to explicitly extend intellectual property protection to photonic and quantum chip layouts, marking a significant policy update for emerging chip technologies.

The revised Regulations on the Protection of Layout Designs of Integrated Circuits, adopted by China's State Council, take effect on 15 October 2026.

Among the key changes is an updated definition of integrated circuits that broadens the scope of protection beyond conventional semiconductor designs to include

photonic and quantum integrated circuits.

The regulations also introduce stricter requirements for layout-design registration, including originality statements, while allowing third parties to challenge registrations through a formal revocation process.

The revised framework strengthens enforcement by expanding remedies for infringement and reinforcing legal protection for registered chip layouts.

The policy follows growing activity in photonic and quantum integrated

circuit development, with experts cited alongside the regulations noting increasing innovation in these fields.

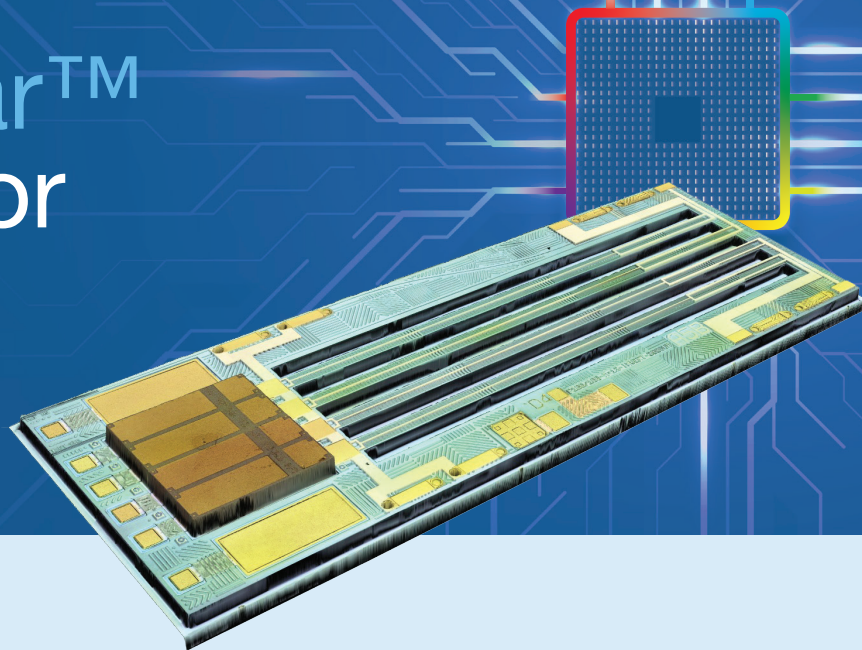
The revisions are intended to provide a legal framework that keeps pace with next-generation integrated circuit technologies and supports continued investment in advanced chip design.

By formally recognising photonic integrated circuit layouts within its IP framework, China aims to strengthen protection for emerging technologies as it expands research and commercial development in photonics and quantum computing.



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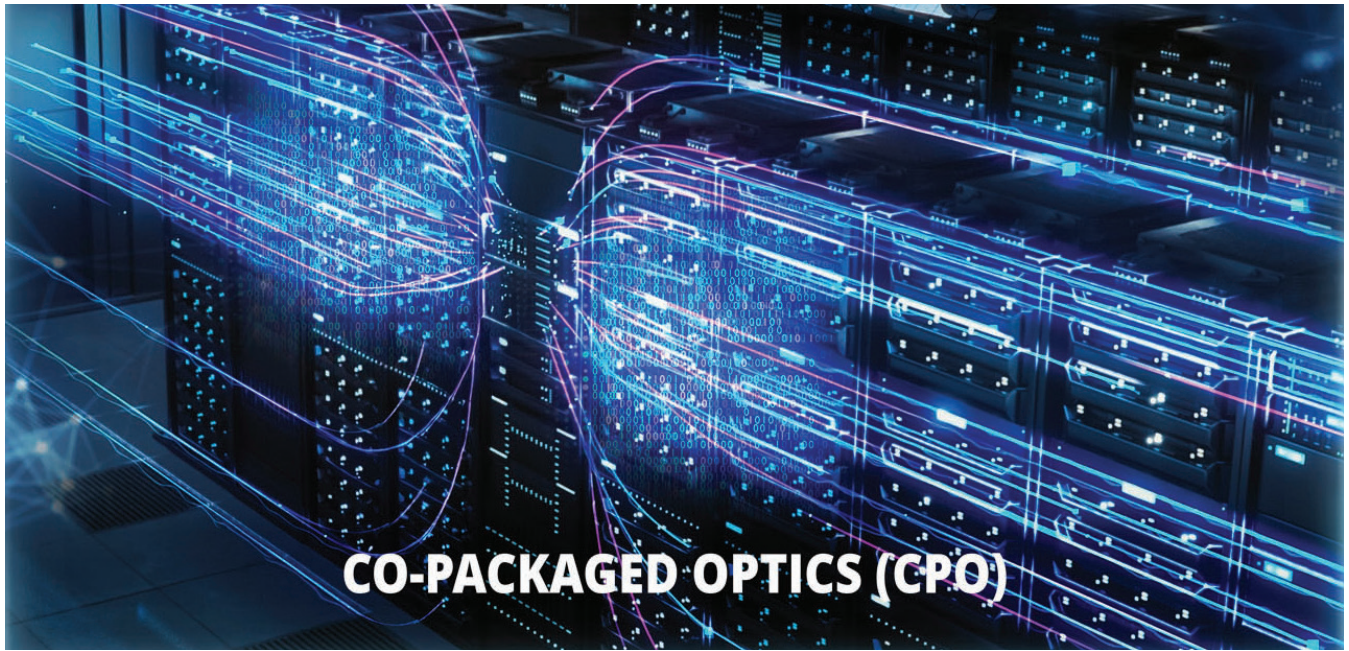
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From process development to high-volume manufacturing



ASMPT is experiencing strong demand for ultra-precision die-bonding systems – from manufacturers of AI infrastructure and optical interconnects to aerospace applications. As data rates continue to increase, scalable manufacturing of photonic devices is becoming a key enabler for the next generation of computing.

AN INTERVIEW WITH SEBASTIAN RAPPL, TECHNICAL SALES MANAGER AT ASMPT AMICRA GMBH

AI CLUSTERS, high-performance computing, and hyperscale data centres require faster, denser, and more energy-efficient data movement. Co-Packaged Optics integrates optical engines closely with ASICs or other high-performance processors in a single package, shortening electrical paths to reduce signal loss, power consumption, and latency. As data rates increase, manufacturers face demanding CPO assembly challenges: sub-micron optical alignment, reliable bonding, thermal management in compact packages, heterogeneous integration of optics and electronics, metrology, process control, and scalable production with consistent yield and reliability. ASMPT addresses these needs with high-precision

placement systems, proprietary vision alignment, in-line metrology, and automation capabilities for scalable CPO assembly. As optical interconnects increasingly replace copper connections in AI-enabled data centres, scalable optoelectronic manufacturing is becoming a key element of ASMPT's strategy to empower the Intelligence Revolution.

What are the key considerations in the volume production of co-packaged optics? We interviewed Sebastian Rappl, Technical Sales Manager at ASMPT AMICRA GmbH.

Q: Which CPO applications are driving current manufacturing requirements?

Sebastian Rappl: What we see today is that the discussion around co-packaged optics has become much more application driven. Customers are no longer asking about CPO as a system architecture. Instead, they are now developing concrete assembly processes for glass dies, micro-lenses, lens arrays, photonic integrated circuits and optical sub-assemblies integrated alongside ASICs, drivers and TIAs, e.g. processes for CoC-embedded CPO architectures or CPO systems supplied by external laser sources in an ELSFP form factor. Following alignment, these optical components are typically fixed using UV-curable adhesives. What makes these assemblies particularly demanding is the direct relationship between mechanical precision and

optical performance. Parameters such as x/y position, z-height, tilt, bond-line thickness and post-bond shift directly influence optical coupling efficiency. A mechanically acceptable assembly can therefore still fail to meet optical specifications if curing shrinkage, adhesive flow or substrate movement changes the optical path. Many engineers initially focus on placement accuracy. In practice, however, placement accuracy alone is no longer sufficient to ensure optical performance. In many photonics applications, the challenge is not only placing components accurately, but ensuring that this alignment is maintained throughout bonding, curing and subsequent handling. Manufacturing success depends on controlling the complete process rather than individual steps. Component handling, adhesive dispensing, alignment, placement, UV curing, post-bond inspection and metrology all must work together as one integrated process. Only then can highly sensitive optoelectronic assemblies be manufactured with the repeatability and scalability required for volume production.

Q: At what stage should customers start thinking about manufacturability in CPO?

Sebastian Rapp: One of the most important lessons we've learned is that manufacturability has to be addressed very early – ideally before the package architecture is frozen. Many later assembly limitations like component layout, optical access, fiducial strategy, substrate material, surface planarity, adhesive keep-out zones, thermal budget and the available space for tooling, dispensing, curing and inspection are already defined by design decisions. A good example is alignment access. If the design does not provide suitable optical or visual access, process control becomes much more difficult. The same applies to substrate warpage, adhesive flow paths or material combinations with different coefficients of thermal expansion. These factors can influence the final position of a glass die or lens after curing or during thermal cycling. One of the first tasks in CPO development is translating optical performance requirements into mechanical and process tolerances right from the start. It must be determined during the development phase how much placement deviation, bond-line

variation, post-cure shift or angular error the design can tolerate. Otherwise, the assembly process is forced to compensate for constraints that should have been considered during package design. This is why CPO requires close interaction between design, process engineering and equipment capability. Manufacturability is not a correction step at the end; it becomes part of the design strategy.

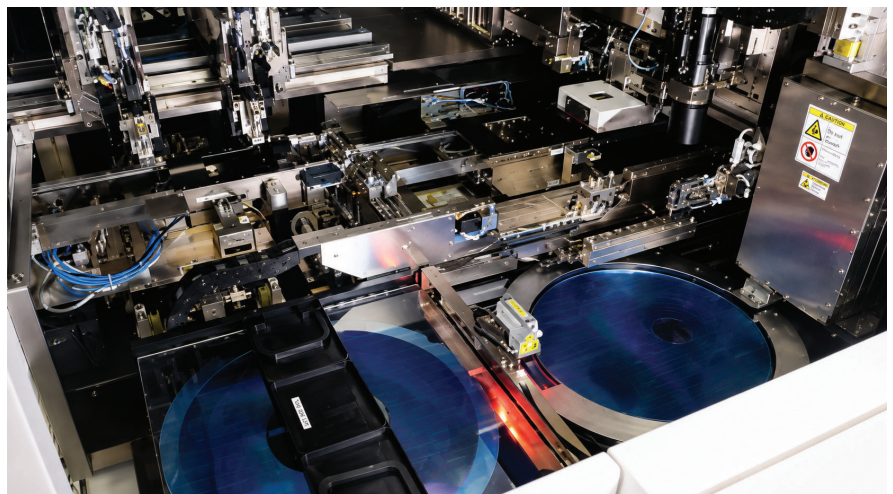
Q: Where does the main technical bottleneck occur when CPO moves from concept to manufacturable assembly?

Sebastian Rapp: In our experience, the bottleneck is rarely a single parameter. It is usually the accumulation of tolerances across the process chain. Placement accuracy, die geometry, substrate flatness, adhesive distribution, bond-line thickness, curing behaviour, thermal expansion and inspection limits all interact. A robust process window does not happen by accident – it has to be engineered deliberately. Only a sufficiently robust process window can absorb normal process variation without compromising optical performance or yield. Each step should be characterized based on how much variation it contributes to the final optical result. For example, if post-bond shift is the dominant factor, improving nominal placement accuracy alone will not solve the issue. If substrate planarity is unstable, better curing control may not be sufficient. A manufacturable CPO process only emerges when placement, bonding, adhesive behaviour, metrology

and automation are treated as one connected system.

Q: Why are glass dies, lenses and UV-curable adhesives particularly challenging in CPO assembly?

Sebastian Rapp: Glass dies and optical components combine mechanical, optical and material-related requirements within a single assembly process. Unlike conventional die attach, the final optical performance depends not only on placement accuracy but also on maintaining that alignment throughout adhesive curing and subsequent handling. UV-curable adhesives enable rapid fixation after alignment, but they also introduce critical process variables, including dispense volume, wetting behaviour, bond-line thickness, curing sequence and material shrinkage. Even very small movements during curing can alter the optical path and reduce coupling efficiency. This is why we always recommend looking beyond the alignment step itself. Alignment cannot be evaluated only before bonding. Manufacturers must verify whether the component remains within specification after curing and under realistic production conditions. A process that delivers good engineering samples but cannot maintain repeatability across substrates, material lots and thermal cycles is not scalable. Consequently, UV adhesive processing should be treated as an integral part of the optical alignment strategy rather than as a separate fixation step.



➤ The source stage of the MEGA multi-chip bonding platform is part of a flexible system that is able to provide different components in one single production step. Image credits: ASMPT

Q: How can process capability and yield be measured and optimized?

Sebastian Rapp: Customers often start by asking about placement accuracy. But nominal placement accuracy alone is not enough. For photonics assembly, the distribution of results is often more meaningful than a single best-case value. Useful indicators include placement repeatability, post-bond shift, bond-line variation, angular deviation, curing-related displacement and correlation with optical test data. This is why metrology plays such a central role. While visual inspection can confirm mechanical assembly quality, only the combination of machine data, in-line inspection and optical measurements provides a reliable assessment of process capability. This integrated data allows engineers

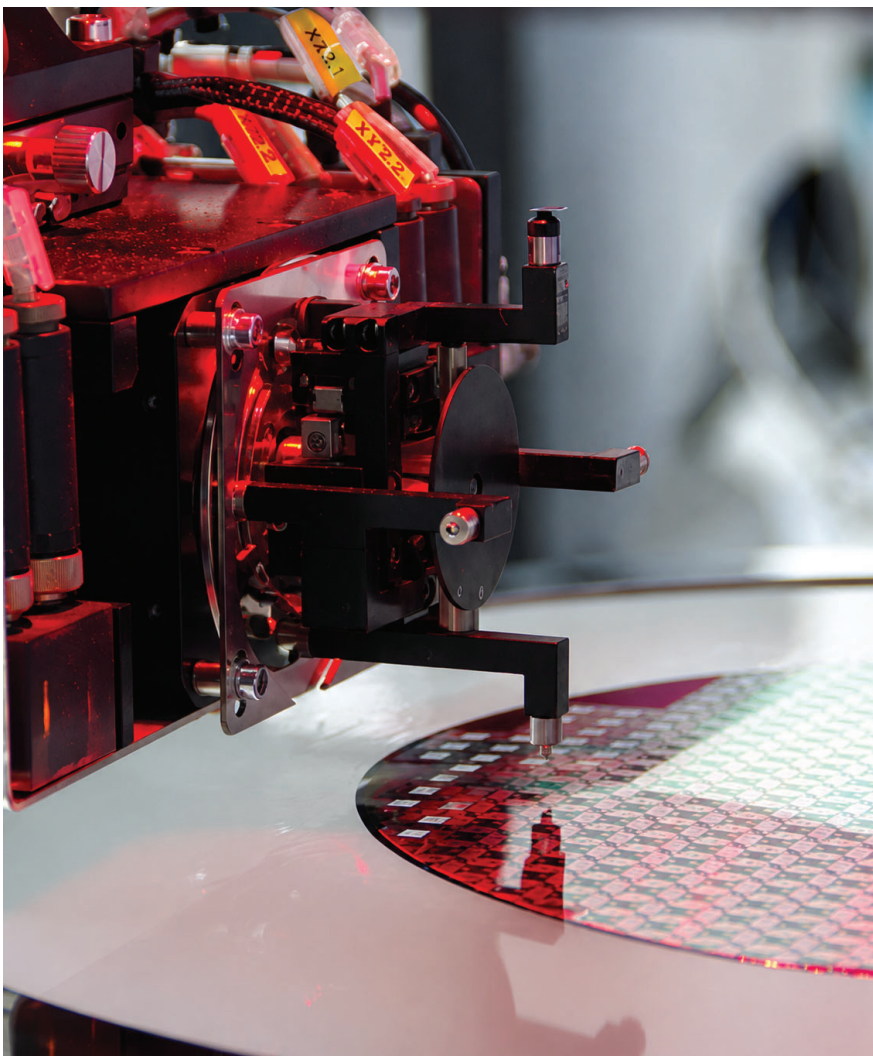
to distinguish whether yield losses originate from placement variation, adhesive behaviour, substrate effects or thermal stress. As CPO modules become increasingly complex, yield management extends beyond individual process steps. Every transfer, handling operation and interface introduces additional sources of variation. Reducing these transitions while maintaining complete process traceability is essential for stable, high-volume manufacturing. Ultimately, process capability depends on the ability to measure, understand and continuously control process variation rather than achieving a single best-case accuracy value.

Q: How do AMICRA NANO, AMICRA NOVA and MEGA support the transition to volume production?

Sebastian Rapp: As we work with customers moving from feasibility studies into production, we see that the requirements for manufacturing technology change significantly. For many customers, AMICRA NANO is the starting point during early process development. The platform provides the sub-micron placement accuracy and process stability required to evaluate alignment and bonding strategies as well as material interactions. AMICRA NANO features $\pm 0.2 \mu\text{m}$ @ 3σ placement accuracy, flip-chip bonding capabilities for advanced semiconductor packaging, a granite-based platform with high-resolution motion control for stable alignment, high-resolution imaging systems that enable dynamic alignment for precise bonding and a laser-based heating system that ensures controlled, localized bonding processes. Its controlled environment enables engineers to identify which process variables truly limit optical performance before scaling begins.

Once the process window has been established, AMICRA NOVA supports the transition to volume production with more than 1,000 UPH by combining high precision with higher throughput, dynamic alignment and robust process control. It features $\pm 1 \mu\text{m}$ placement accuracy for precise photonic and electronic component integration and dynamic alignment and high-resolution imaging for controlled positioning during bonding. It is designed for demanding photonics applications such as silicon photonics, optical transceivers and optical interconnect modules for AI data centres, where consistent optical performance must be maintained at production scale.

For increasingly complex multi-chip architectures, MEGA extends this capability by integrating multiple bonding, inspection and adhesive-related process steps into a single flexible manufacturing platform. MEGA is a multi-chip bonding platform for advanced semiconductor packages that integrate multiple dies in compact, high-performance architectures. Its look-through pattern recognition supports accurate die placement for complex assemblies. The photonics version MEGA-P achieves a throughput of up to 8,000 UPH and offers unparalleled precision of $\pm 2 \mu\text{m}$ @ 3σ and $\pm 0.1^\circ$ @ 3σ in terms of rotation. The MEGA platform offers various epoxy dispensers



➤ The AMICRA NOVA's four-arm flip unit supports the combination of high throughput and precision required for volume production of silicon photonics and optical interconnect modules. Image credits: ASMPT



➤ A look inside the AMICRA NANO: Source stage, flip unit and bond head support the sub-micron precision required to evaluate optical alignment strategies and process windows during early CPO development. Image credits: ASMPT

and stamp options, the ability to use multiple adhesives in parallel, and automatic switching between application variants. Since adhesive control is a critical factor in CPO manufacturing, MEGA also incorporates dedicated 3D inspection of epoxy dispensing. One of MEGA's key strengths is its ability to consolidate critical process steps into a single manufacturing platform, reducing handling, improving process visibility and minimizing cumulative process variation.

Together, these three platforms support the complete manufacturing journey – from process development and validation to scalable, high-yield production.

Q: What ultimately defines a production-ready CPO process?

Sebastian Rappl: Ultimately, a production-ready process is one where the critical variables are understood and kept under control. For glass die and lens attach, this includes alignment accuracy, bond-line thickness, adhesive volume, curing behaviour, post-bond shift, component stability and inspection capability. For us, repeatability – not peak performance – is what defines a CPO process ready for high-volume manufacturing. Every critical parameter

must remain measurable, reproducible and consistently controlled under real production conditions. The objective is not simply to build functional prototypes. It is to establish an integrated manufacturing process that consistently delivers predictable optical performance, stable yield and scalable production without relying on manual intervention or process-specific adjustments.

The industry is no longer asking whether co-packaged optics can be manufactured – it is asking how these highly sensitive assemblies can be produced at scale while maintaining optical performance, yield and long-term process stability.

Thank you very much for sharing your expertise and providing such valuable insights into the key manufacturing challenges and opportunities shaping the future of co-packaged optics.

Visitors to ECOC Exhibition 2026, Europe's largest exhibition and one of the world's leading meeting places for optical communications and photonics, taking place 21–23 September at FYCMA in Málaga, Spain, will have the opportunity to continue the conversation with Sebastian Rappl at the ASMPT booth 2158. Alongside

the topics discussed in this interview, ASMPT will showcase the AMICRA NANO, AMICRA NOVA and MEGA platforms, giving visitors the opportunity to explore solutions for sub-micron alignment, advanced bonding, adhesive processing, integrated inspection and process control. Whether discussing early process development, production scalability or the industrialization of next-generation photonic devices, ASMPT's experts will be available to discuss specific manufacturing challenges and application requirements.

The industry is no longer asking whether co-packaged optics can be manufactured – it is asking how these highly sensitive assemblies can be produced at scale while maintaining optical performance, yield and long-term process stability.

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Enabling network scalability through advanced photonic integration

AI is reshaping optical networks from the rack to the data centre and beyond. Advances in photonic integration, vertical integration and heterogeneous PICs are enabling the bandwidth, power efficiency and scalability needed for the next generation of AI infrastructure.

BY FADY MASOUD, OPTICAL PLUGGABLES SOLUTIONS; AJAY MISTRY, LEADER, SILICON PHOTONICS DESIGN; TERESA MONTEIRO, OPTICAL COMPONENTS SOLUTIONS; NOKIA

THE RAPID GROWTH of AI, cloud computing, hyperscale data centers and global networks is creating unprecedented demand for bandwidth. Networks must now scale compute inside racks, across data-center fabrics and over metro, long-haul and subsea links. These three models scale-up, scale-out and scale-across are reshaping how photonic integrated circuits (PICs) are designed for higher bandwidth, lower power, smaller footprints and faster deployment (Figure 1).

Scale-up increases compute capacity within a rack by connecting accelerators such as GPUs and TPUs, memory and switching resources with ultra-high bandwidth and very-low latency. These architectures require dense optical links that can deliver terabit-class throughput while minimizing power and latency.

Scale-out expands compute capacity horizontally across racks and nearby data centers. It places heavy demands

on pluggable optics, coherent interconnects and switching fabrics as AI and cloud workloads distribute traffic across larger pools of machines.

Scale-across extends GPU or TPU clusters beyond the physical walls of a single building, in effect fusing two or three data centres and their accelerated compute resources into one giant synchronous super-cluster. Scale-across is most applicable to hyperscalers training large language models, but the scale involved, connecting 100,000s of GPUs in one facility to 100,000s in a second or third site 100s of kilometres or more away.

Although each model has different reach, latency and capacity requirements, they all share the same basic need: higher bandwidth, lower power per bit, smaller form factors, lower cost, and faster deployment. Coherent optics, used for DCI, metro, long-haul and subsea transport, prioritizes reach, spectral efficiency,

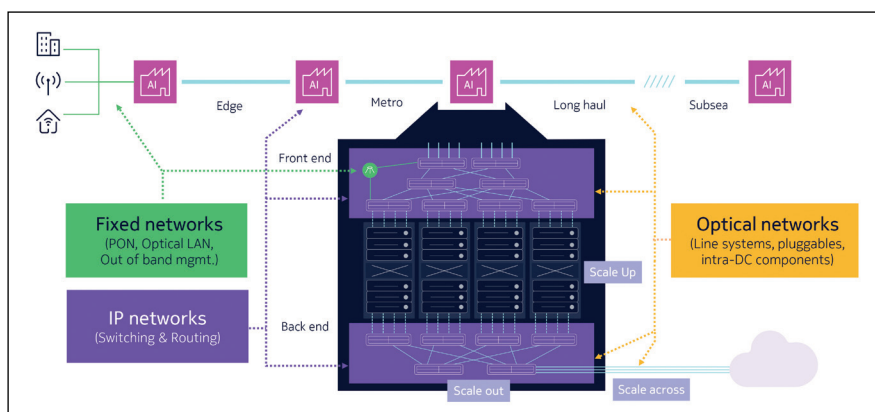
optical signal quality and tight integration with DSP-based signal processing. Conversely, intensity modulation direct-detect (IMDD) optics are used for short-reach intra-data-center connectivity, prioritizes low power, rack density, low latency, cost and high-volume manufacturability. This is why photonic integration and vertical integration are becoming central to the AI networking era.

The value of vertical integration

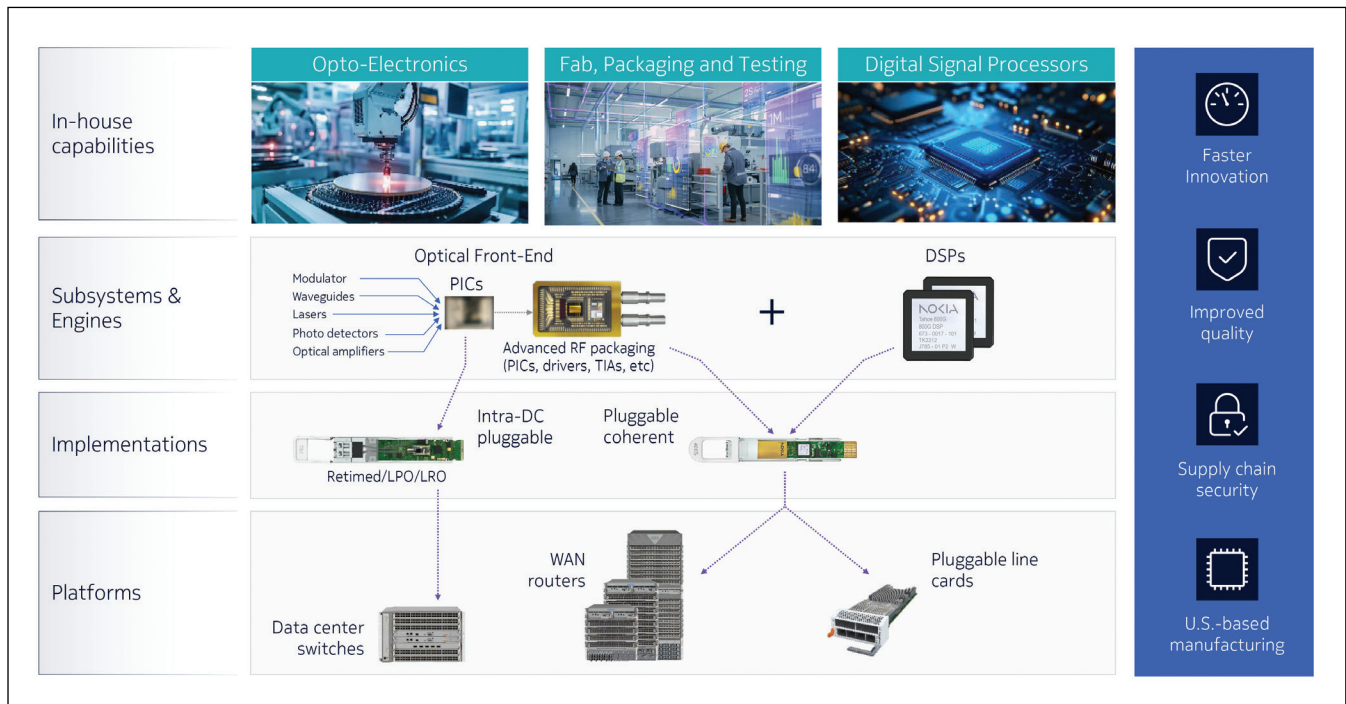
Deep vertical integration is a critical asset for advanced optical networking. Vertical integration refers to designing and controlling multiple layers of the technology stack, from photonic devices and DSPs to packaging, subsystem assembly and final optical system design. This includes in-house development of lasers, modulators, waveguides, photodetectors, optical amplifiers, RF drivers and Transimpedance Amplifiers (TIA), RF packaging, DSPs, controls, firmware, coherent engines, pluggable optics, optical transport, IP switching and routing platforms. Vertically integrated companies gain several important advantages.

First, vertical integration accelerates innovation. As baud rates increase and system architectures become more complex, performance optimization increasingly depends on co-design between optics, electronics, packaging and firmware. When all these domains are developed internally, engineering teams can optimize the entire system holistically rather than treating components independently.

Second, vertical integration improves quality and reliability. High-speed



➤ Figure 1: Network scaling models



➤ Figure 2: Vertical integration

coherent systems require extremely precise alignment between optical and electrical subsystems. Integrated development and testing reduce interface mismatches and manufacturing inconsistencies, resulting in higher yields and improved field reliability.

Third, vertical integration enhances supply chain security. Demand for optical components is increasing dramatically in the AI Supercycle, placing stress on global manufacturing ecosystems. Companies with in-house manufacturing, packaging and testing

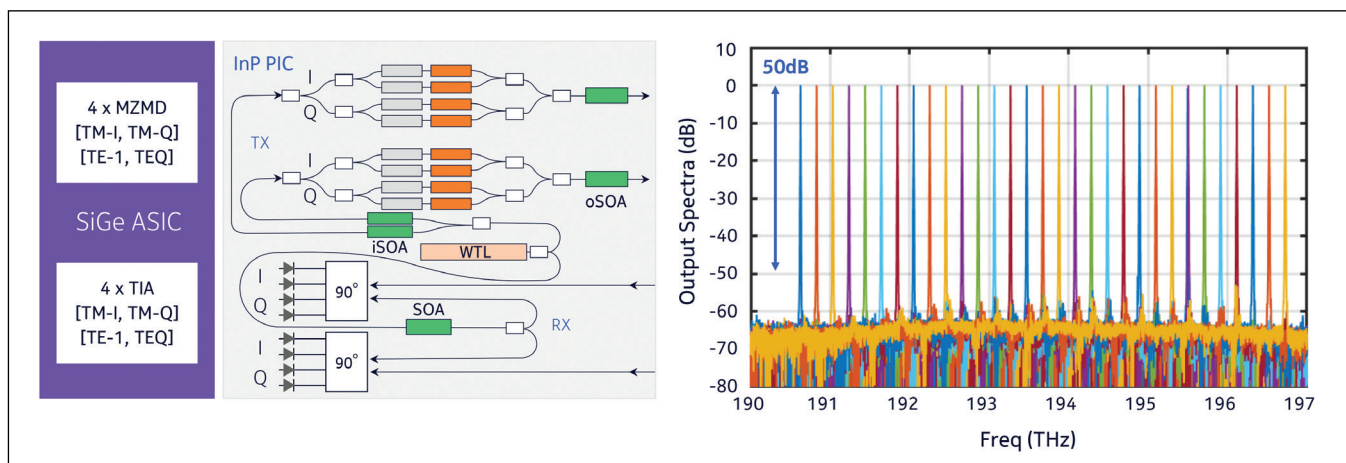
capabilities are better positioned to maintain product availability and protect intellectual property.

Finally, vertical integration enables faster product introduction cycles. AI and cloud operators expect rapid deployment of new technologies across both coherent transport and intra-data-center connectivity. Owning multiple stages of the value chain allows vertically integrated companies to respond faster to technology changes while optimizing performance, power and manufacturability (Figure 2).

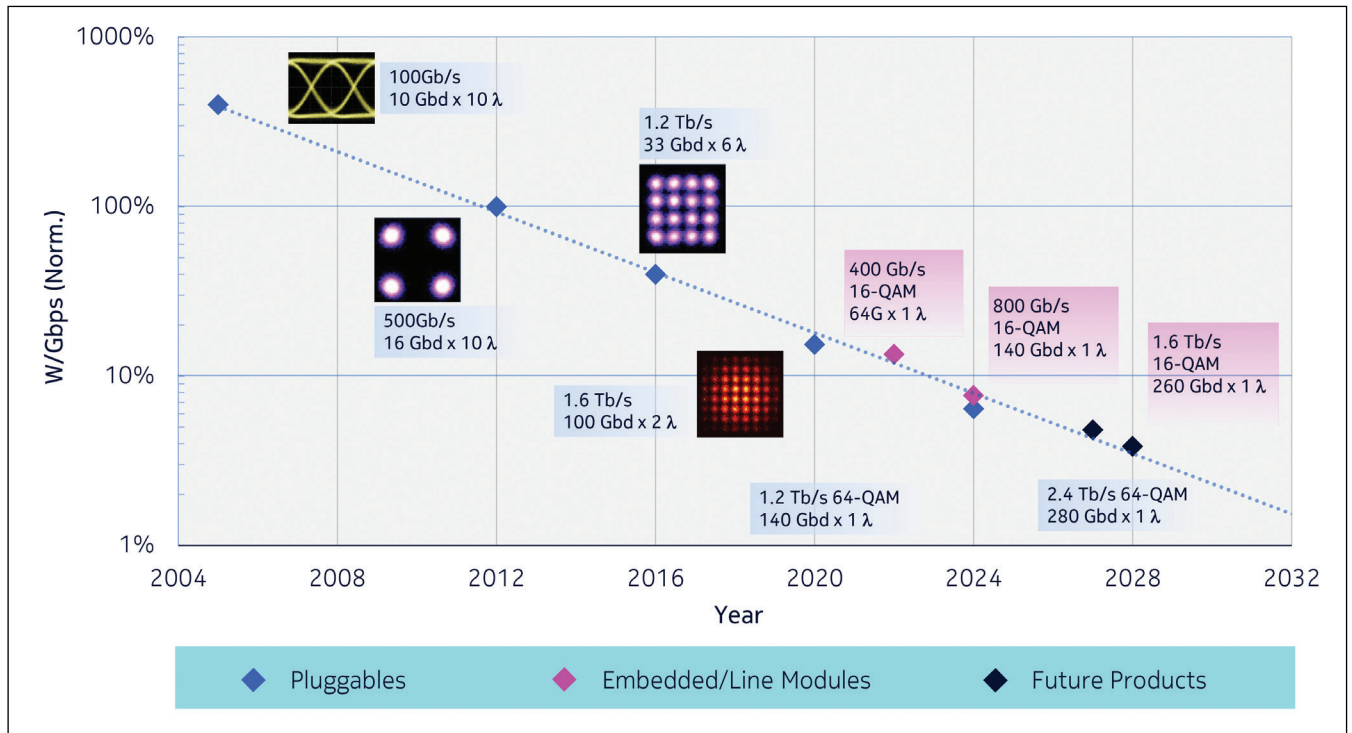
At the foundation of vertical integration in high-performance optics is the photonic integrated circuit (PIC).

Building photonic integrated circuits

PICs generate and manipulate light to perform transmission, modulation, amplification, switching and detection functions on a compact microchip. They can integrate optical functions such as distributed-feedback (DFB) lasers or laser arrays, tunable lasers, Mach-Zehnder modulators (MZMs), electro-absorption modulators (EAMs), photodiode arrays, and multiplexers or



➤ Figure 3: Monolithic InP coherent PIC



➤ Figure 4: Scalability and sustainability of power and capacity of InP PIC optical engines

demultiplexers into a single chip. This enables high-speed transmission with low power and simpler integration. Today, the two dominant PIC platforms are indium phosphide (InP) and silicon photonics (SiPh), while heterogeneous integration is increasingly used to combine the strengths of multiple material systems.

Silicon photonics

Silicon photonics uses mature semiconductor manufacturing to build optical circuits on silicon wafers. Its main advantage is scale: it can take advantage of established silicon foundries, packaging infrastructure and CMOS process control. Silicon photonics is well suited for passive optical functions such as waveguides, multiplexers, polarization management, filters and routing structures. It also supports advanced electronics integration and packaging, making it attractive for high-volume data-center applications. Modern SiPh process design kits (PDKs) include these functions, along with germanium-on-silicon photodetectors, edge couplers, tunable optical filters, optical attenuators, monitoring photodiodes and polarization-management functions. Integrating these building blocks on one PIC reduces packaging complexity and optical loss while improving transceiver performance, yield and cost.

Heterogeneous integration extends silicon photonics beyond the limits of native silicon. For example, thin film lithium niobate (TFLN) can be bonded to silicon to create very high-bandwidth modulators with lower drive voltages. This supports higher baud rates and better modulation efficiency than conventional silicon photonics. One example is the use of TFLN-based Mach-Zehnder modulators (MZMs) on a silicon photonics platform for high-performance coherent pluggable optics. These systems combine high-speed modulators, SiPh PDK components and high-speed photodetectors, enabling integrated transmit and receive functionality on a common platform.

Looking ahead, heterogeneous integration can combine InP and TFLN devices on a common silicon photonics platform. Because silicon cannot natively generate light, laser sources must be integrated through flip-chip assembly or wafer bonding.¹ In this architecture, InP devices enable active functions such as nano-integrable tunable laser assemblies (nITLAs), distributed-feedback (DFB) lasers and semiconductor optical amplifiers (SOAs).

By combining the strengths of each material system (InP for light generation

and optical gain, TFLN for high-speed modulation and silicon for large-scale photonic integration), future PICs can deliver higher functionality and performance on a scalable platform. This approach also supports wafer-scale production and provides a path to future 1.6T, 3.2T and higher-capacity coherent optical modules.

Monolithic indium phosphide PICs

While silicon photonics relies on heterogeneous integration for adding functionality or improving performance, indium phosphide itself offers a capable and established monolithic integration platform. InP can generate, modulate, amplify, and detect light directly on the same substrate. This enables tunable lasers, semiconductor optical amplifiers, modulators, detectors and monitoring functions on one chip, reducing optical interfaces, insertion loss, footprint, packaging complexity and power consumption.

InP also allows optical gain to be placed where it delivers the greatest system benefit. Integrated SOAs can improve optical signal-to-noise ratio, increase launch power and enhance receiver sensitivity, enabling high-performance coherent transmission over long distances (Figure 3). By integrating

lasers, amplifiers, modulators and detectors on one semiconductor platform, InP PICs support stable optical performance, simpler packaging and long operating lifetimes by minimizing mechanical bonds that often become failure points.

Monolithic InP solutions are especially attractive for coherent pluggables and long-haul transport systems. Recent demonstrations have shown 800 G coherent pluggables operating over uncompensated subsea fiber links spanning thousands of kilometers. These trials demonstrated the feasibility of using compact pluggable optics in applications traditionally dominated by large optical transport platforms.

InP is also compelling for intra-datacenter connectivity. Its monolithic integration can reduce modulation voltages and support power-efficient linear pluggable optics, helping address rack power density, cooling constraints and sustainability goals. Power-efficient intra-datacenter InP transmitter PICs were recently reported.^{2,3} When packaged in the linear pluggable optics (LPO) form factor, these InP PICs can be used to interconnect GPUs through switches and network interface cards with about 8 W of power dissipation per 1.6 Terabits/sec.

The sustainability of optical engines for power, space and throughput is an increasingly critical factor and requires a wide range of technical innovations to meet the application demands. Figure 4 illustrates an example for long-reach optical engines realized with monolithic InP PICs over multiple decades and the sustained long-term reduction in power per bit enabled by successive generations of optical engines.

Challenges and future directions

Despite major progress, the next generation of photonic integration will require innovation across devices, materials, electronics, packaging and system architecture. As baud rates increase, electrical interconnect loss, signal integrity and thermal density become more difficult to manage. Future systems will need shorter RF paths, lower-loss materials, tighter DSP-to-optics integration and advanced thermal designs suitable for compact pluggable modules.



Manufacturing scalability is equally important. High-volume optical platforms must maintain cost efficiency, reliability and stable performance while supporting increasingly complex assemblies.

This will require better packaging materials, improved degradation models, scalable characterization methods and simulation tools that model optical, thermal and electrical behavior together.

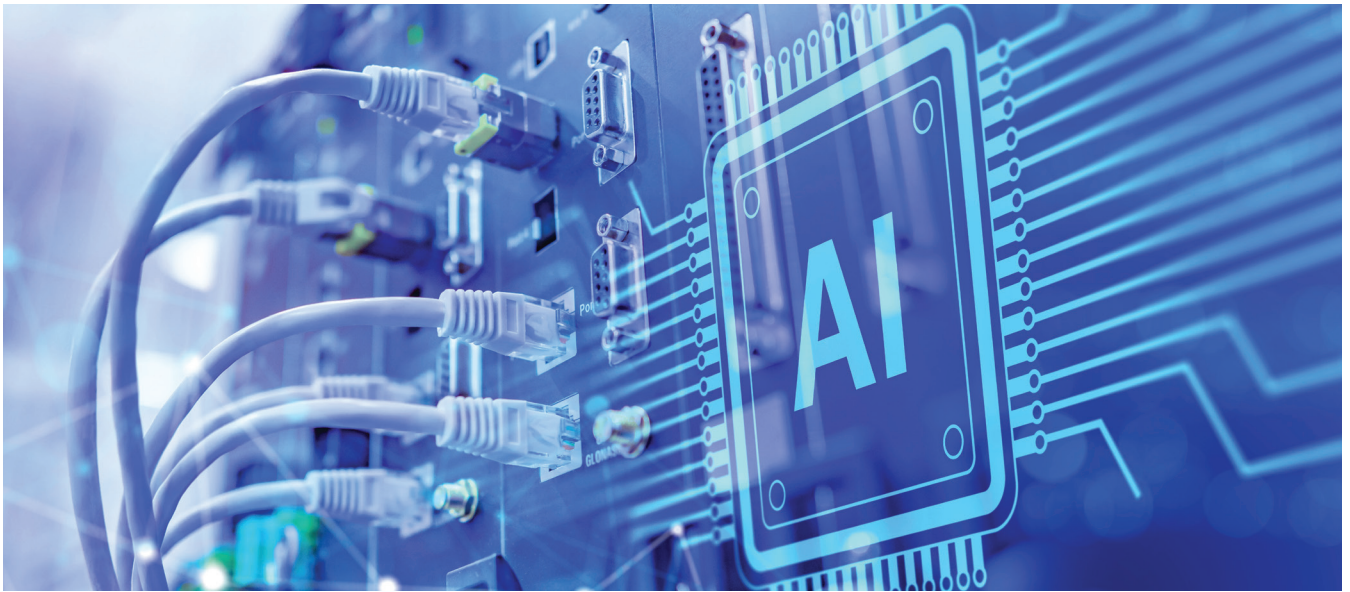
Photonic integration has already transformed optical networking by enabling bandwidth scaling from 10 Gbps to multi-terabit systems. The AI era now requires deeper co-design across photonics, electronics, materials, packaging and systems. The most scalable solutions will combine monolithic integration, heterogeneous integration, advanced packaging and vertical integration to deliver higher capacity, lower power and faster deployment.



► Authors from left to right: Fady Masoud, Ajay Mistry and Teresa Monteiro

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Co-packaged optics simulation for AI infrastructure



As AI data centres push interconnect bandwidth, power, and integration limits, co-packaged optics (CPO) demands a new generation of multiphysics simulation workflows that unite photonics, electronics, and advanced packaging design.

BY SHIN-SUNG KIM, SR. ARCHITECT, APPLICATIONS ENGINEERING, SYNOPSYS

Why AI infrastructure is driving the rise of CPO?

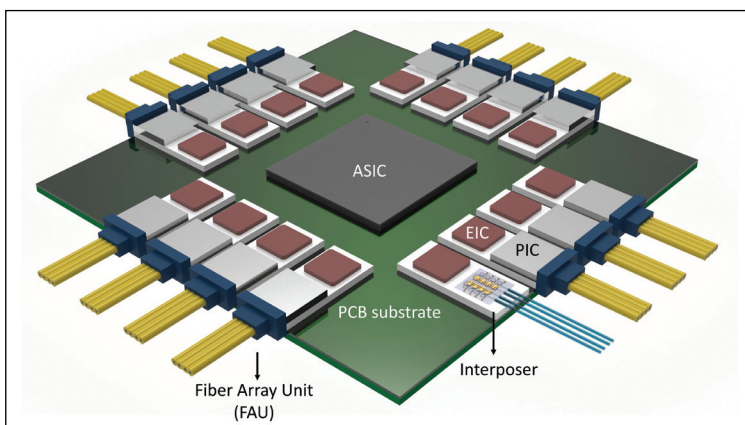
THE RAPID GROWTH of large-scale AI training and inference clusters is transforming the networking requirements placed on data centre infrastructure. As GPUs, accelerators, and switching ASICs continue to increase in performance, the amount of data that must move between devices is accelerating rapidly. Traditional copper

interconnects and pluggable optical modules are increasingly challenged by bandwidth density, power consumption, and packaging constraints.

CPO has emerged as one of the most promising solutions to overcome these limits. By integrating photonic and electronic functions within the same package, CPO dramatically shortens electrical interconnect lengths between the switching ASIC and optical engine. This reduces channel loss, lowers power consumption, and enables higher aggregate bandwidth. Studies show that CPO architectures can deliver substantial power savings compared with conventional pluggable optics, while enabling the scaling needed for next-generation AI fabrics.¹

However, achieving these benefits requires far more than simply placing optics closer to electronics. A modern CPO platform combines photonic integrated circuits (PICs), electronic integrated circuits (EICs), optical coupling structures, advanced packaging substrates, thermal management solutions, and high-speed electrical channels. Each influences the others through tightly coupled physical effects.

➤ Figure 1:
Co-packaged optics for AI infrastructure.



Consequently, multiphysics simulation has become a strategic enabler for AI infrastructure innovation.

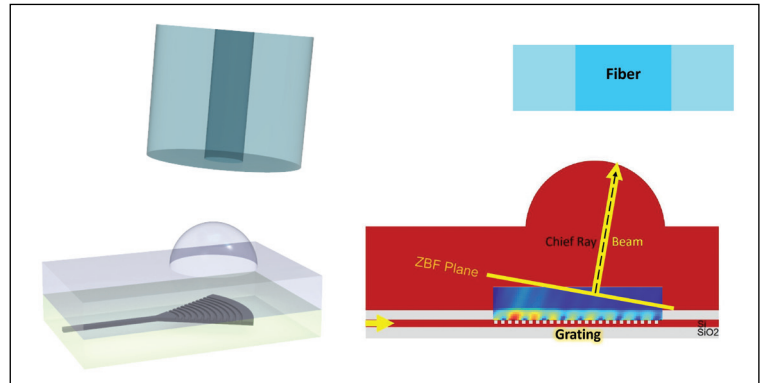
Why CPO creates new engineering challenges?

Unlike traditional optical modules, CPO architectures require optimisation across multiple engineering domains simultaneously. Four challenges are particularly significant:

- Optical coupling:** Light must be transferred efficiently between fibres and photonic chips despite large differences in scale and tight manufacturing tolerances. Small alignment errors can significantly impact coupling efficiency and system performance.
- Electrical-Optical interaction:** Photonic devices are inseparable from the electronic circuits that drive them. Signal integrity, routing structures, loss, crosstalk, and latency all influence optical link performance.
- Thermal management:** High-performance AI accelerators and switching ASICs generate substantial heat. Temperature directly affects wavelength stability, insertion loss, and photonic circuit behaviour, making thermal effects central to CPO design.
- Mechanical stress and packaging:** Advanced packaging introduces mechanical strain and thermal expansion mismatch that can affect optical properties, create alignment errors, and reduce overall reliability.

Why traditional simulation flows fall short for CPO?

Historically, photonic, electrical, thermal, and mechanical simulations have been performed independently. A photonic designer may optimise an optical modulator without considering package temperatures, while a packaging engineer may

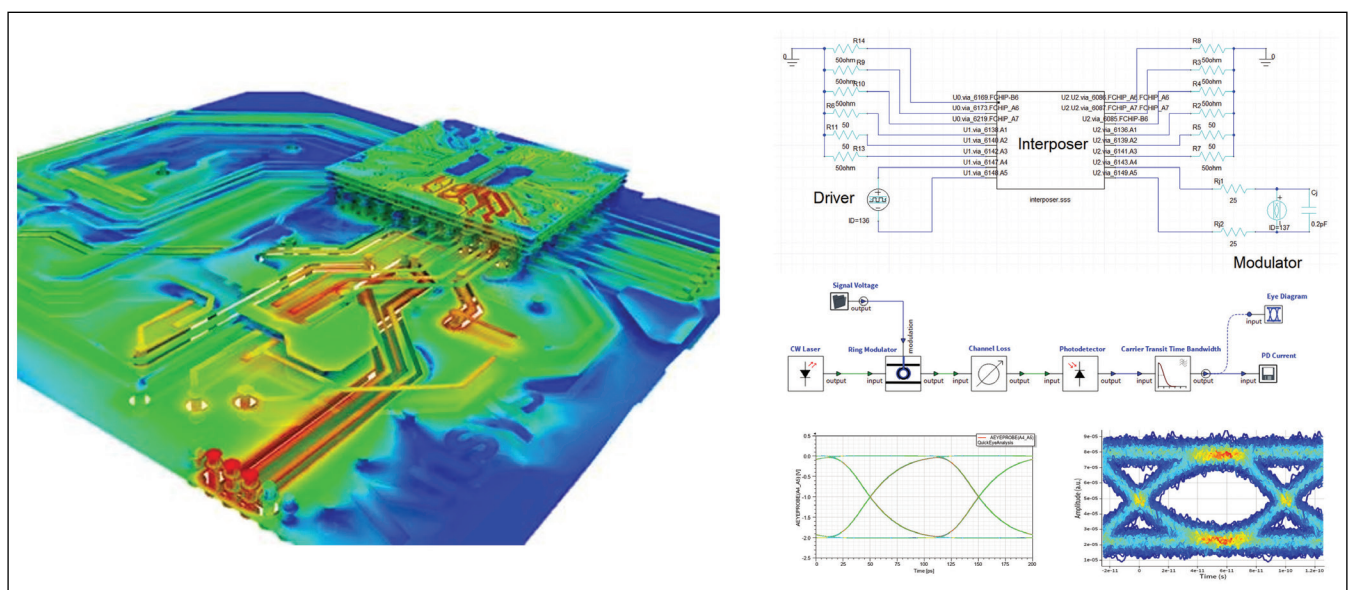


evaluate mechanical stress without understanding its impact on optical coupling efficiency.

While this siloed approach may be adequate for discrete optical modules, it fails in CPO environments where the interactions between physics domains directly determine system performance. Designers must simultaneously address nanometre-scale photonic structures, millimetre-scale optical interfaces, and centimetre-scale package assemblies while accounting for electrical, optical, thermal and mechanical effects.

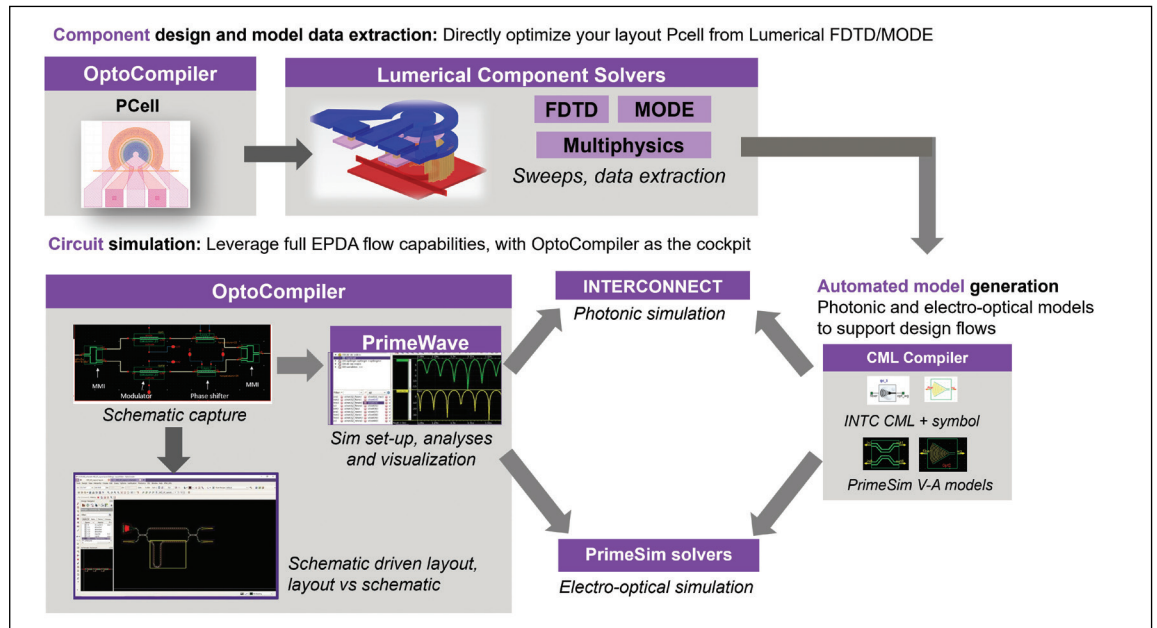
As a result, modern CPO development increasingly relies on comprehensive simulation environments that unify optical, electronic, thermal, and packaging analysis within a common workflow. Rather than treating these domains as separate tasks, they become part of a unified design workflow. For instance, Synopsys' CPO workflows identify thermal effects, stress effects, voltage drop, electromigration, cross-die electromagnetics, and optical I/O design as tightly interconnected

➤ Figure 2: Grating coupler with microlens, illustrating the field exchange between nearfield and free-space propagations.



➤ Figure 3: Full-wave EM simulation with Ansys HFSS and signal integrity analysis including packaging effects with Ansys Circuit and Ansys Lumerical INTERCONNECT™.

➤ Figure 4: End-to-end Synopsys photonics solutions, with OptoCompiler serving as the central cockpit for component simulation, circuit simulation, and layout design.



challenges requiring integrated multiphysics solutions.

Optical I/O: The critical interface between silicon and fibre

For many CPO systems, the greatest practical challenge lies at the optical interface itself. Even a highly optimised PIC delivers little value if light cannot be coupled efficiently between fibre and chip.

Optical I/O is fundamentally a multiscale problem. Silicon waveguides operate with dimensions measured in hundreds of nanometres, while optical fibres and packaging structures are orders of magnitude larger. Coupling technologies such as grating couplers, edge couplers, micro-lenses, and fibre attach systems must bridge these scales while maintaining high efficiency and manufacturability.

Synopsys combines Ansys Lumerical electromagnetic simulation with Ansys Zemax OpticStudio® optical system design software to address this challenge. Near-field optical behaviour can be modelled using rigorous photonic simulation, while free-space propagation and optical assembly effects are evaluated using optical system modelling. This enables designers to analyse complete fibre-to-chip coupling systems rather than isolated elements.

By combining electromagnetic simulation with optical system modelling, engineers can evaluate complete fibre-to-chip coupling systems and assess the impact of alignment tolerances, lens positioning, fabrication variation, and packaging constraints. These capabilities are increasingly important as AI systems require higher optical-port density and tighter manufacturing tolerances.

Electrical-Optical co-design

One of the defining characteristics of CPO is the close relationship between optical and electrical domains. Photonic devices do not operate in isolation; they are driven by electronic circuits, interconnected through advanced packaging and evaluated according to overall link performance.

Signal integrity directly influences photonic performance. Package routing, channel loss, crosstalk, and electromagnetic behaviour all influence overall link quality. Consequently, accurate simulation requires simultaneous consideration of electrical and optical behaviour.

Synopsys addresses this challenge through co-simulation capabilities linking photonic circuit modelling with electromagnetic analysis tools. High-frequency electrical structures can be characterised using full-wave EM simulation, while photonic circuits are represented through compact models and system-level simulation. The combined workflow enables end-to-end, electrical-optical-electrical evaluation of complete communication channels.

This integrated perspective is particularly important for AI clusters where aggregate bandwidth reaches unprecedented scales. Optimising only the photonics or only the electronics is no longer sufficient. True system performance depends on the interaction between both domains.

Designing and verifying photonic integrated circuits

Every CPO system begins with individual photonic components. Waveguides, grating and edge couplers, modulators, photodetectors, ring resonators, and multiplexers must first be designed and validated before they can be assembled into larger circuits.

Anslys Lumerical FDTD™, Anslys Lumerical MODE™, and Anslys Lumerical Multiphysics™ photonic-component simulation tools now part of the Synopsys portfolio provide the foundation for this process through rigorous 3D electromagnetic and multiphysics simulation. Component geometries, process information, and foundry PDK data can be used to analyse optical performance, fabrication sensitivity, and physical behaviour at the device level. Designers can evaluate not only optical characteristics but also the impact of thermal and mechanical effects on device operation.

Once validated, the behaviour of these devices can be translated into compact models using Anslys Lumerical CML Compiler™ development software. Compact models are essential because a realistic AI interconnect may contain hundreds or thousands of photonic devices. Running full-field simulation across an entire system would be impractical. Compact models capture the relevant device physics while providing the speed required for system-level analysis.

The result is a scalable workflow in which physical device accuracy is preserved while enabling

efficient circuit design. This bridge between rigorous multiphysics simulation and circuit abstraction is one of the key enablers for industrial-scale silicon photonics deployment.

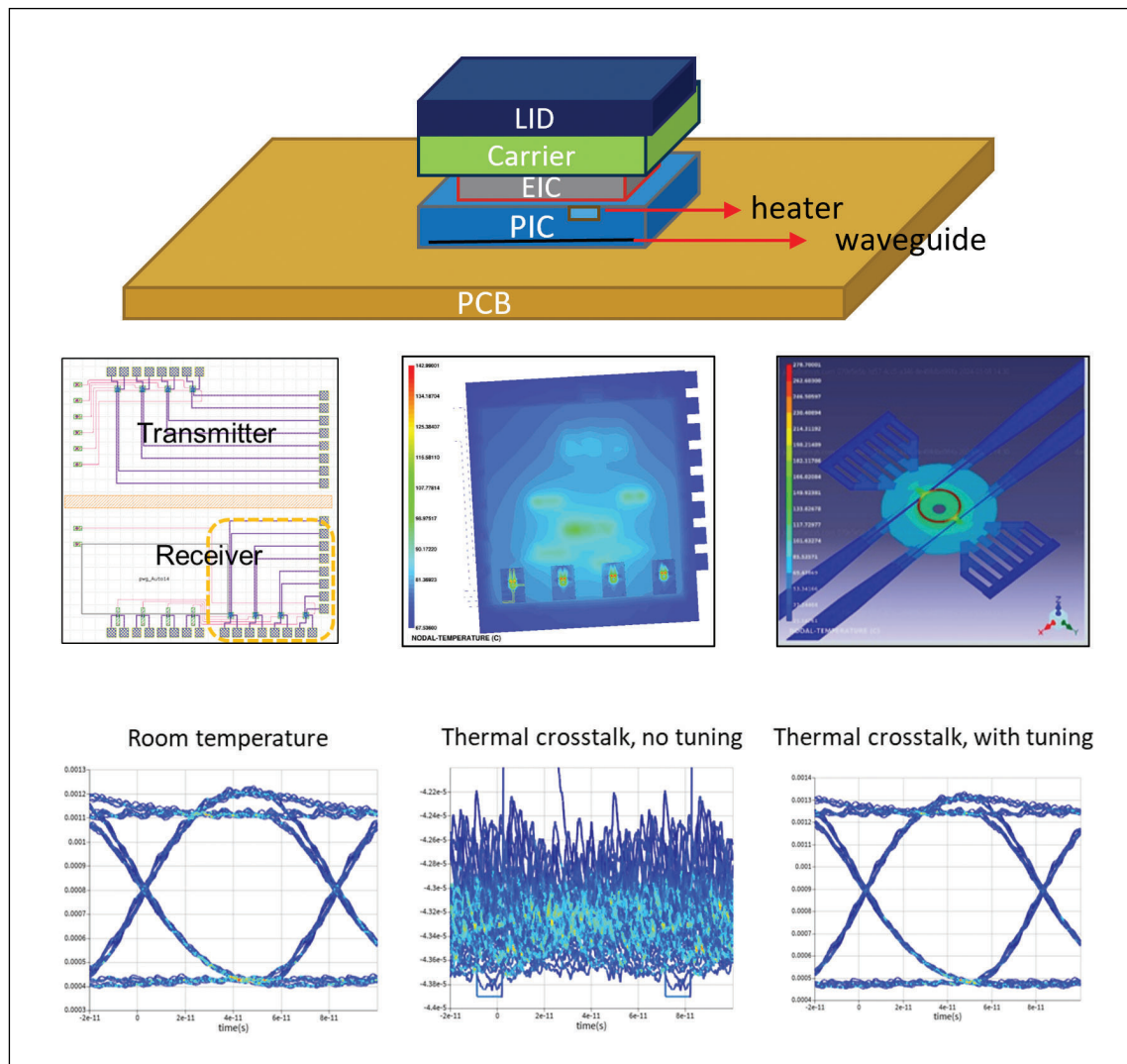
Synopsys OptoCompiler further extends this workflow into an end-to-end Synopsys photonics solution, spanning component simulation, circuit simulation, and layout design.

Thermal-aware and layout-aware design

Thermal management is one of the most significant concerns in co-packaged optics. As optical and electronic dies move closer together, temperature-induced performance variations become increasingly difficult to ignore.

Temperature affects wavelength stability, insertion loss, and overall circuit behaviour. In particular, ring resonators may experience resonance shifts due to thermal crosstalk. As optical and electronic dies move closer together, package-level thermal effects become increasingly difficult to ignore.

Synopsys supports a hierarchical thermal workflow spanning device, chip, and package levels. Chip



➤ Figure 5: Thermal analysis of a four channel WDM circuit with Anslys Redhawk SC – ET and Anslys Lumerical INTERCONNECT.

Thermal Models (CTMs) enable efficient package simulation while preserving sufficient accuracy for photonic analysis. Temperature maps generated during package simulation can then be imported into photonic design environments for thermal-aware circuit verification.

Mechanical effects must also be considered. Temperature gradients create thermal expansion mismatch, inducing strain within PICs and packaging structures. This strain can modify optical properties, create birefringence, reduce coupling efficiency and generate alignment errors. Synopsys workflows incorporate structural analysis alongside photonic and thermal simulation to address these challenges. Collaboration with major foundries has further enabled integrated packaging-stress workflows for advanced 3DIC architectures.

AI-assisted design optimisation

As CPO systems become more complex, traditional optimisation approaches struggle with the sheer number of design variables involved. Fibre position, coupler geometry, package dimensions, thermal parameters, and electrical configurations can create enormous design spaces.

AI-assisted simulation is emerging as a powerful solution. Synopsys workflows use machine learning techniques to accelerate exploration of large design spaces while maintaining correlation with physics-based simulation. This enables engineers to evaluate more design alternatives than would be possible with direct simulation alone.

In demonstrated optical I/O workflows, hundreds of physical simulations were used to train surrogate AI models capable of predicting performance with high accuracy. These models enabled optimisation processes more than 500 times faster than direct simulation while maintaining close agreement with rigorous solver results.²

The same philosophy is extending to broader system-level applications. AI-enabled reduced-order models can accelerate electrical-optical link analysis, helping engineers evaluate complex communication systems more efficiently than traditional approaches.

As AI drives unprecedented demand for bandwidth and energy efficiency, the irony is striking: AI is now helping design the optical infrastructure that makes large-scale AI possible. By combining rigorous physics with intelligent optimisation, engineers can evaluate more concepts, improve robustness and reach optimal solutions faster than ever before.

Conclusion

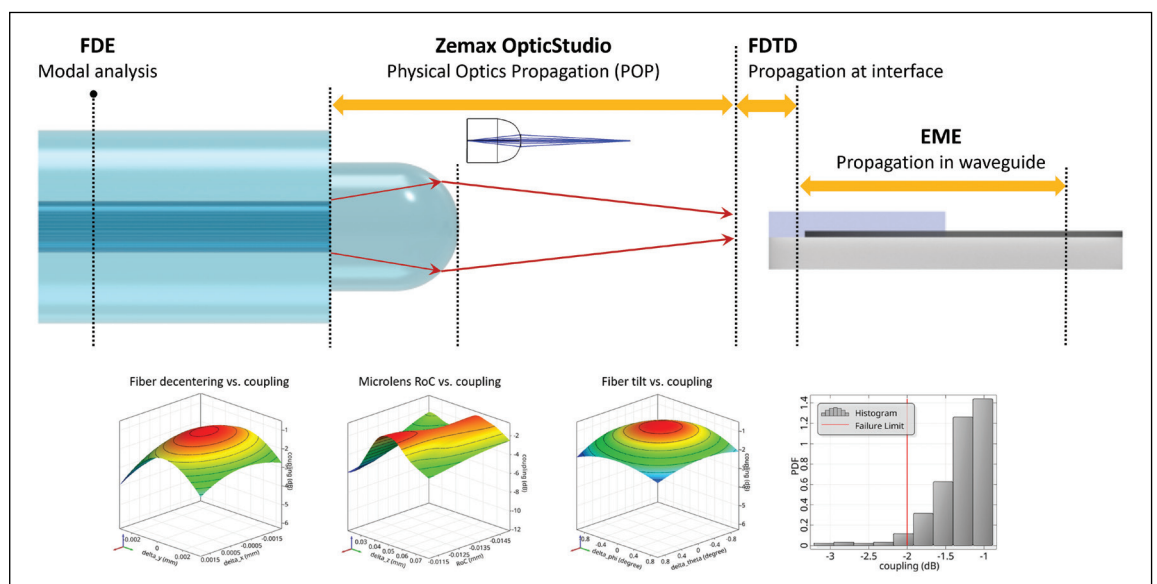
Co-packaged optics represents a fundamental shift in data centre architecture, bringing photonics directly into the heart of AI infrastructure. Yet the promise of CPO can only be realised through a holistic engineering approach that unifies photonics, electronics, and advanced packaging.

As AI systems continue to scale, multiphysics simulation is evolving from a design-support function into a strategic enabler. By providing a unified environment for modelling optical, electrical, thermal, and mechanical interactions, integrated simulation workflows allow engineers to accelerate innovation, reduce risk, and bring next-generation AI interconnect technologies to market more efficiently.

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➤ Figure 6: AI-assisted optimization of a lensed edge coupler using Ansys optiSLang.



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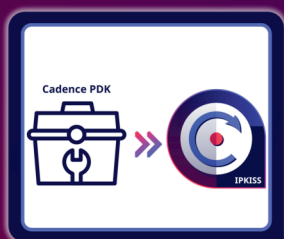
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Photonic integrated circuits drive parallel Laser RADAR performance



Ommatidia LiDAR uses photonic integrated circuits to turn parallel optical acquisition into a practical Laser RADAR workflow, helping engineers capture dense, time-coherent surface data at industrial speed.

BY OSCAR R. ENRÍQUEZ, PRODUCT SPECIALIST, OMMATIDIA LIDAR

Why parallel optical measurement matters

LASER RADAR and laser vibrometry are valued because they can measure a surface without touching it. They are especially useful when access is difficult, when contact sensors would change the behaviour of the structure, or when many points need to be measured with high accuracy. The remaining challenge has usually been speed. A sequential instrument can move from point to point, but the spatial picture is assembled over time.

That matters in structural testing, industrial diagnostics, modal analysis, product validation, and precision metrology. Real engineering events are often dynamic. A machine is running, a structure is vibrating, a component is deforming under load, or a surface is moving while it is being measured. The faster the instrument captures the

spatial field, the more directly the data represents the event itself.

Ommatidia LiDAR addresses this with a massively parallel Laser RADAR architecture based on photonic integrated circuits. Instead of observing one location after another, the system can acquire many optical channels simultaneously. Depending on configuration, Ommatidia systems measure up to 128 channels at the same time.

The gain is substantial. For an equivalent set of measurement points, parallel acquisition can reduce the time needed to capture the spatial field by roughly two orders of magnitude compared with point-by-point measurement. That speed advantage can be used in two complementary ways: to capture the same area much faster, or to increase

spatial resolution within the same measurement window.

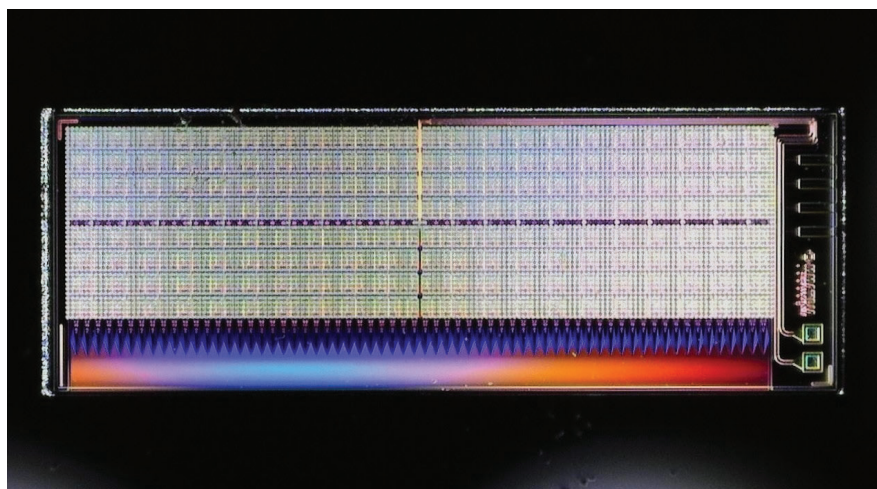
Higher spatial resolution changes the quality of the result. Engineers can work with a denser description of the surface, rely less on interpolation between sparse points, and detect local behaviour that was not known in advance. That is important in vibration work, but it is equally important in high-accuracy surface metrology, where local shape, displacement, and deformation can carry the information that determines performance.

The PIC as an enabling architecture

Photonic integrated circuits are often associated with smaller, more stable, and more scalable optical systems. In Ommatidia's platform, the PIC is also what enables the instrument to behave differently. It provides a compact and repeatable route to multi-channel optical processing, allowing the Laser RADAR system to acquire distributed surface information in parallel.

The result is a measurement architecture where integrated photonics is directly visible in the end-system performance:

- Simultaneous acquisition across many optical channels
- Fast measurement of dense spatial fields
- Stronger time coherence between measured points
- Less dependence on interpolation or repeated test runs
- Direct access to local dynamic and metrology information



➤ Figure 1: PIC-enabled massively parallel Laser RADAR concept image used in Ommatidia's original article. Credit: Ommatidia LiDAR.

This moves photonic integration from component advantage to

workflow advantage. The PIC helps the instrument observe more of the surface in the same physical moment. That creates a clearer picture of how a structure, machine, or manufactured component behaves under real conditions.

For dynamic applications, the advantage is immediate. If a structure is excited by wind, impact, rotating machinery, traffic, or a controlled shaker, a parallel instrument can capture the distributed response during the same event. Phase relationships, mode shapes, local hot spots, and transient effects can be interpreted with greater confidence because the points are acquired together rather than reconstructed from a long sequence.

For metrology applications, the same architecture supports fast, high-accuracy direct surface measurement. Dense optical acquisition can reveal local deformation, shape change, vibration, and surface motion without adding targets or contact probes. This extends the platform from vibration analysis into precision inspection and dimensional measurement workflows where accuracy and throughput matter together.

From sparse scans to dense spatial fields

Sequential point measurement has served optical metrology well, and it remains useful for many stable tasks. Parallel Laser RADAR expands the practical operating space by making dense fields easier to capture. When many points are observed at once, the instrument can deliver a spatially richer dataset before the physical state has had time to change.

That shift is especially valuable when the interesting behaviour is local. A crack-adjacent vibration hot spot, a fixture-induced deformation, a localised resonance, a component edge effect, or an unexpected surface-motion pattern may not be visible from a sparse measurement grid. A denser field improves the chance of seeing the behaviour directly.

It also improves the engineering workflow. Sparse scans often require interpolation to estimate what happens between measured points. Interpolation is useful, but it is still an assumption about the unmeasured surface. A



➤ Figure 2: Q2 Laser RADAR front view illustrating the deployed system form factor. Credit: Ommatidia LiDAR.

parallel system allows teams to increase the number of measured points and reduce the distance between them, so the final result is driven more by direct measurement and less by reconstruction.

This is where the two-order-of-magnitude speed advantage becomes commercially meaningful. Faster acquisition gives engineers the option to spend the saved time on spatial detail. A test that once collected a coarse grid can be turned into a denser map. A field inspection that once focused on a few expected locations can cover more of the asset. A metrology task that once balanced accuracy against throughput can move closer to both.

Practical Laser RADAR workflow

Ommatidia combines the PIC-enabled channel architecture with coherent detection, FMCW ranging concepts, and non-contact Laser RADAR and LDV workflows. The same platform can support geometric measurement, dynamic measurement, and direct surface observation.

In a practical workflow, the instrument measures surface motion, displacement, or geometry without installing sensors on the target. This reduces preparation time and helps preserve the natural behaviour of the object under test. It also makes the system attractive for large structures, inaccessible components, fragile

surfaces, moving machinery, and production environments where contact probing would slow the process down.

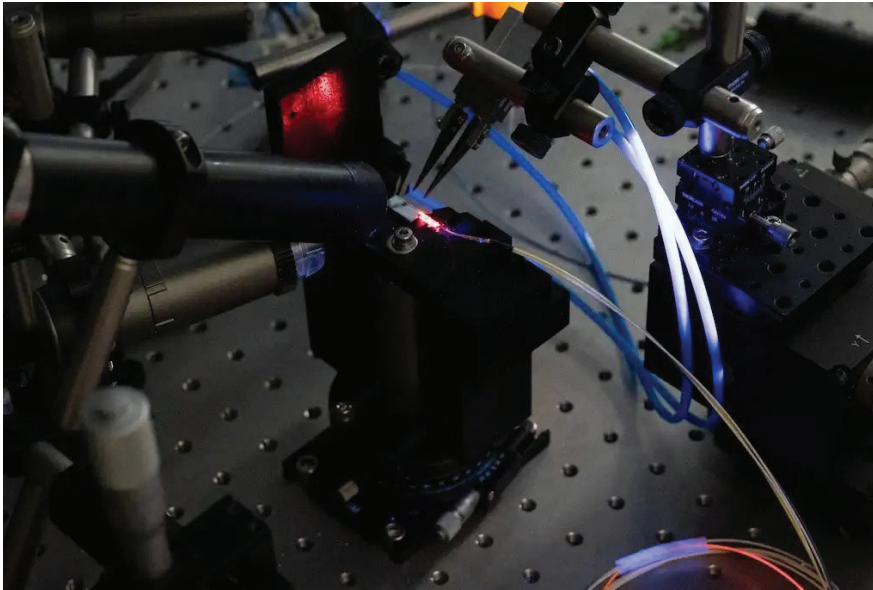
The high-channel architecture adds spatial context to that non-contact measurement. Instead of asking only what happened at one location, the user can see how the response is distributed across the measured area or line. In dynamic work, that supports modal analysis, operational diagnostics, and structural monitoring. In metrology work, it supports direct surface measurement, deformation tracking, and high-resolution comparison of measured shape under different states.

The instrument therefore becomes more than a faster scanner. It becomes a way to capture a physical event as a spatial field, with enough density to support confident interpretation and enough speed to keep pace with changing conditions.

Application value across engineering sectors

In structural monitoring, simultaneous optical channels help show how motion is distributed along a bridge, tower, test article, or large mechanical structure. Engineers can identify where the response concentrates, compare repeated campaigns, and use dense data to guide more detailed modelling or inspection.

In industrial diagnostics, parallel acquisition helps reveal local vibration



➤ Figure 3: Laboratory close-up of Ommatidia Laser RADAR hardware. Credit: Ommatidia LiDAR.

hot spots, coupled behaviour, and unexpected operating patterns. Dense non-contact measurement can be performed without covering a machine in sensors, which is useful when access is limited or when the installation itself would be disruptive.

In modal analysis and validation, the combined gain is more points with stronger time coherence. Mode shapes, phase relationships, and localised behaviour become easier to interpret when the spatial dataset is captured during the same event.

In product development, dense measurement shortens the path from test to design feedback. Engineers can observe how a prototype deforms or vibrates across a surface, compare results with simulation, and refine the design with less dependence on repeated single-point acquisitions.

In precision metrology, the same technology supports high-accuracy direct measurement of surfaces. Fast optical acquisition can capture shape, displacement, and deformation without contact, creating a route to inspecting surfaces under load, monitoring movement during operation, and detecting small local deviations that sparse measurement can miss.

These use cases share a common requirement: useful surface information

has to be captured quickly, accurately, and at enough spatial density to show what is really happening. Photonic integration gives the Laser RADAR system a scalable way to meet that requirement.

Integrated photonics as a product advantage

The strongest value of integrated photonics appears when it changes the end product. In Ommatidia's Laser RADAR platform, the PIC helps convert optical complexity into a usable multi-channel instrument.

That product-level advantage matters commercially. Measurement teams want faster setup, denser data, and clearer insight. Production teams want throughput without losing accuracy. Engineering teams want a better chance of detecting local behaviour before it becomes a failure mode or a missed design issue. Parallel Laser

RADAR supports those goals by making dense, time-coherent optical measurement more accessible.

The architecture also creates room for future scaling. As photonic integration continues to mature, multi-channel optical instruments can become more compact, robust, and deployable. The same direction supports higher channel counts, tighter integration, improved stability, and broader adoption of non-contact measurement in industrial environments.

Looking ahead

Massively parallel Laser RADAR shows how PICs can move measurement technology from point-by-point observation toward dense, time-coherent surface sensing. The platform brings together speed, spatial resolution, direct surface measurement, and practical deployment in a single optical workflow.

The two-order-of-magnitude improvement in measurement speed is a central part of that shift. It allows faster capture of dynamic events, higher spatial resolution within the same test time, less interpolation between points, and better detection of unknown local behaviour. For many engineering and metrology tasks, that combination is more valuable than any single specification on its own.

As industries demand faster inspection, better structural understanding, and more direct measurement of real surfaces under real conditions, parallel optical architectures will become increasingly important. Ommatidia's approach demonstrates how photonic integrated circuits can provide the foundation for that next generation of high-density, non-contact measurement systems.

FURTHER READING

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- 2. Wikipedia, "Photonic integrated circuit"
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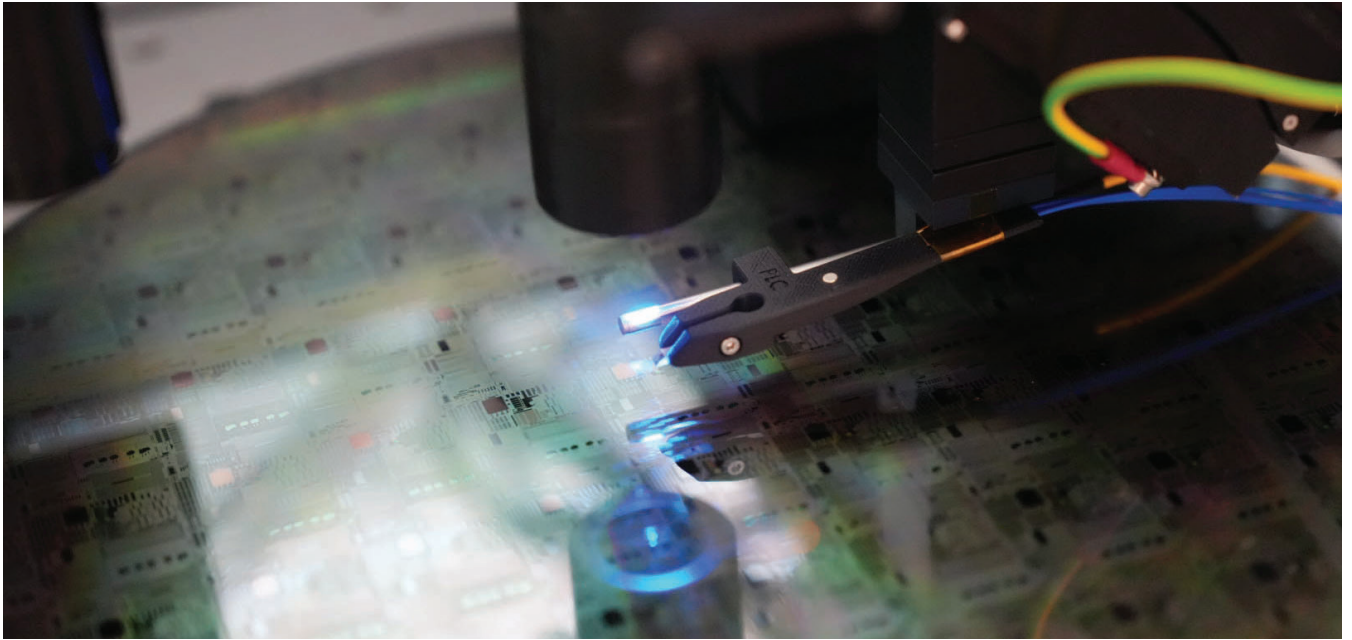
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The silicon photonics bottleneck: Why lasers are now essential

As AI infrastructure drives higher production volumes, manufacturing challenges are replacing device performance as the industry's biggest hurdle. Laser trimming and laser cleaning are emerging as key technologies for improving yield, scalability and reliability in silicon photonics manufacturing.

BY VINH DANG, BUSINESS DEVELOPMENT SEMICON SOLUTIONS, CARL PAQUET, DIRECTOR OF BUSINESS DEVELOPMENT, JEAN-PHILIPPE BÉRUBÉ, DIRECTOR, LASER APPLICATIONS, FEMTUM

THE SILICON PHOTONICS industry is entering a new phase of maturity. Over the past decade, the ecosystem has largely focused on proving device performance, validating architectures, and demonstrating the advantages of photonic integrated circuits for high-speed optical communication. That phase is now ending, and the rapid expansion of AI infrastructure is fundamentally changing the conversation.

Hyperscalers are no longer asking whether silicon photonics can work at scale. They are asking whether the industry can manufacture enough devices, with sufficient yield, consistency, and cost efficiency, to support the next generation of AI clusters and optical interconnect architectures. With co-packaged optics platforms moving from announcements toward commercial deployment, that question is no longer hypothetical.

This shift changes everything. The challenge facing the industry today is no longer device innovation

alone. The central challenge is now manufacturing scalability.

As co-packaged optics, high-bandwidth optical engines, and advanced photonic packaging move toward higher production volumes, two manufacturing bottlenecks are becoming increasingly difficult to ignore: wafer-level phase variation and contamination during back-end assembly. These are not secondary process issues. They are becoming some of the primary yield detractors limiting scalability across the silicon photonics manufacturing ecosystem, and traditional manufacturing approaches are no longer sufficient to solve them.

Silicon photonics is fundamentally more sensitive than CMOS

One of the biggest misconceptions outside the photonics industry is the assumption that silicon photonics manufacturing behaves similarly to traditional CMOS manufacturing. Although

dimensional variation also affects CMOS device performance, its impact on circuit functionality is generally less direct and can often be accommodated through design margins and system-level tolerances. A transistor may deviate slightly from its nominal electrical characteristics while the overall circuit continues to meet its functional specifications.

Photonic devices behave very differently. In silicon photonics, nanometer-scale dimensional changes directly affect optical phase. Even extremely small fabrication variations can shift resonance wavelengths, alter coupling efficiency, or degrade overall performance. These effects are especially consequential for functions such as DWDM filtering, high-speed optical modulation used in both direct-detection and coherent-detection systems, and dense optical switching. These functions rely on phase-sensitive building blocks, including microring resonators, Mach-Zehnder interferometers, and optical couplers, whose optical response depends strongly on their geometry. Consequently, small variations in waveguide width, sidewall angle, or slab thickness can produce measurable phase, resonance, or coupling errors at the chip output. There is no convenient noise margin to hide behind.

As PIC complexity increases, the cumulative impact of fabrication variation becomes increasingly severe. Every manufacturing step contributes to phase error accumulation, from lithography variation and etch non-uniformity to residual stress in deposited oxide, CMP variation, local pattern density effects and implantation damage. Collectively, these effects create large performance spreads across the wafer. This is why many PIC manufacturers observe highly non-uniform reticle-to-reticle variations in which devices near the center of a wafer meet specifications while edge dies fall significantly outside acceptable operating ranges.

The result is lower wafer yield, increased test complexity, and rising manufacturing costs. For years, the industry has largely relied on active compensation to solve this problem, but that strategy is beginning to show its limitations.

The hidden cost of active tuning

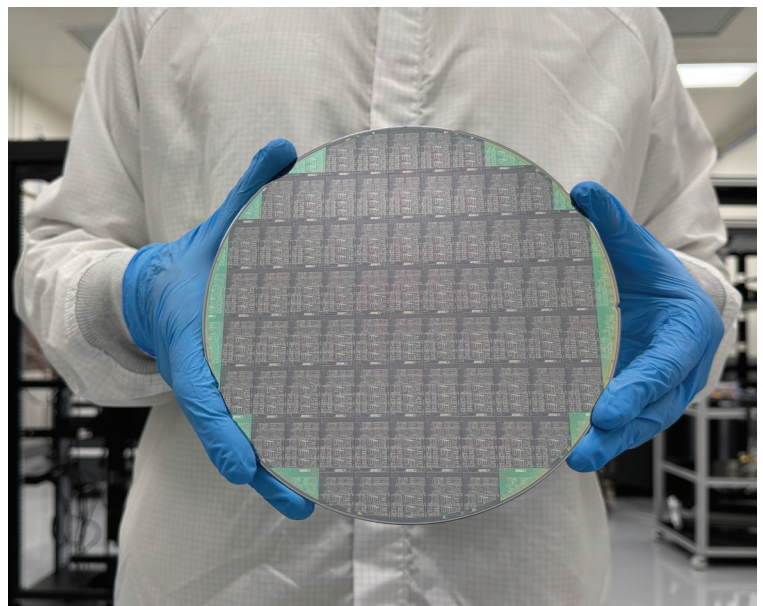
The standard industry approach has been to compensate for fabrication variations after wafer fabrication using thermal heaters, phase shifters, and electronic control loops. From a functional standpoint, this approach works. From a scalability and cost perspective, however, its tradeoffs are becoming increasingly difficult to justify.

Every additional tuning element introduces a cascade of penalties: higher power consumption, increased die area and routing complexity, more drivers and control electronics, longer calibration times, greater packaging overhead, and additional software validation requirements. Active tuning also adds significantly to test cost, which is already one of the

These penalties compound rapidly as photonic circuits scale to meet the demands of AI infrastructure. Photonic platforms are expected to reduce power consumption while simultaneously supporting higher channel counts and greater integration density.

dominant contributors to overall device economics in many advanced PIC products.

These penalties compound rapidly as photonic circuits scale to meet the demands of AI infrastructure. Photonic platforms are expected to reduce power consumption while simultaneously supporting higher channel counts and greater integration density. Large arrays of thermal phase shifters work against both objectives: they continuously consume power to maintain devices within specification, while their heaters, thermal isolation structures, electrical routing, and control electronics occupy valuable die area and constrain circuit densification, particularly in high-channel-count applications such as DWDM. Localized heating and thermal crosstalk further complicate system design and reliability. The industry is therefore pursuing greater power efficiency and integration density while relying on compensation mechanisms that inherently increase power consumption, footprint, and thermal complexity. As photonic circuits scale, this model becomes increasingly difficult to sustain.



➤ Figure: Wafer level photonics trimming is compatible with 200 or 300 mm silicon photonics wafers

Wafer-level laser trimming changes the manufacturing equation

This is where wafer-level laser trimming becomes strategically important. Instead of compensating for phase variation electronically after packaging, wafer-level trimming permanently corrects the variation directly on the wafer before the device ever reaches assembly. The process uses precisely controlled short pulses of laser light to induce localized material densification. The resulting change in optical properties permanently adjusts the effective optical path length, enabling phase errors to be corrected with extremely high precision, on the order of milliradians. The correction remains stable across the operating temperature range and throughout the expected lifetime of the device.

The impact on manufacturing can be significant. Wafer-level trimming enables permanent phase correction and improved device uniformity, recovers out-of-spec dies, reduces dependence on thermal tuning, lowers static power consumption, simplifies test procedures, shortens calibration times, and ultimately raises wafer yield. More importantly, it changes the overall manufacturing philosophy. Instead of designing photonic systems around process variation, manufacturers can

begin designing systems around performance optimization again.

This distinction matters. As device complexity increases, the ability to permanently stabilize optical performance at the wafer level becomes increasingly valuable for scalable production. The long-term implication is not simply higher yield; it is a fundamentally different cost structure for silicon photonics manufacturing. Wafer trimming also fits naturally into existing fab logistics. Because it can be deployed immediately after wafer-level optical test, dies flagged as out-of-spec can be routed to the trimming station, corrected, and returned to the standard flow without restarting any upstream process, preserving throughput while recovering yield that would otherwise be scrapped.

The back-end assembly problem few people talk about

Even when wafer-level yield issues are addressed, PIC manufacturing faces another major challenge: contamination during assembly and packaging. This problem receives far less attention publicly, but it is becoming increasingly critical as photonic packaging complexity grows. Unlike traditional semiconductor devices, photonic systems contain highly sensitive optical interfaces that are vulnerable to particulate contamination and process residues.

During assembly, PICs are exposed to numerous contamination sources, including dicing debris, polymer particles, epoxy residues, flux contamination, fiber handling contamination, operator-induced particles, and pick-and-place contamination. For many electronic systems, these contaminants may be relatively harmless. For photonic devices, they can be catastrophic. A microscopic particle near a grating coupler or fiber interface can introduce scattering losses large enough to push a device outside specification.

Contamination near bonded optical interfaces can also create long-term reliability concerns. These include localized optical heating, epoxy carbonization, optical drift, coupling degradation, and reliability failures over time. The issues become even more severe in advanced packaging environments involving co-packaged optics, fiber arrays, MEMS structures, suspended waveguides, micro-lens arrays, through-glass vias, and high-density optical I/O. As the industry moves toward higher production volumes, contamination control is becoming a major manufacturing bottleneck and traditional cleaning methods are increasingly struggling to keep up.

Why traditional cleaning methods are reaching their limits

Historically, semiconductor cleaning processes were designed around relatively robust substrates and



➤ Figure: Femtum's laser trimming and cleaning solution integrated into a ficonTEC equipment.

comparatively forgiving structures. Modern photonic devices are very different. Many optical interfaces are very sensitive to chemicals, mechanical stress, and this creates major limitations for conventional cleaning technologies.

Wet cleaning processes can introduce chemical compatibility issues, coating degradation, stiction risks, residue variability, and process inconsistency. Manual cleaning introduces additional variability and becomes nearly impossible to scale consistently in high-volume manufacturing.

Plasma processes often lack the selectivity required for delicate optical surfaces and can damage sensitive coatings or metallic interfaces. Mechanical cleaning methods can also create unacceptable risks for MEMS structures and suspended photonic components.

At the same time, contamination tolerances are becoming increasingly strict. The industry is therefore facing a growing mismatch between device sensitivity and the capabilities of traditional cleaning methods. This is where selective laser cleaning is beginning to emerge as an enabling manufacturing process.

Selective laser cleaning enables non-contact precision cleaning

Selective laser cleaning approaches contamination differently. Instead of applying broad chemical or mechanical cleaning processes, laser cleaning exploits the absorption interplay between contaminants and the underlying substrate. With the appropriate wavelength, pulse duration, and fluence, contaminants absorb energy far more efficiently than the surrounding material. This allows particles and residues to be selectively removed while leaving the underlying optical structure entirely unaffected. The

mechanism depends on a careful match between the laser source and the materials involved: pulse energies sit below the ablation threshold of the substrate but well above the threshold required to vaporize, eject, or photochemically decompose the contaminant. The process can be tuned site by site across the same chip.

The process offers several important advantages for photonic manufacturing. It is non-contact, requires no chemicals or solvents, provides high spatial selectivity, and is compatible with automation. It also reduces operator variability, operates in a dry processing environment, and remains compatible with the most sensitive optical structures. These attributes become particularly valuable in advanced photonic packaging flows where traditional cleaning approaches may no longer be viable.

Laser cleaning can also be integrated directly into automated assembly systems and adapted through

software-defined process recipes for different photonic structures. This flexibility is increasingly important as PIC architectures continue to diversify further. The goal is no longer simply cleaning. The goal is manufacturing robustness.

The real manufacturing advantage is operational simplicity

One of the most overlooked aspects of laser-based manufacturing processes is operational simplification, and the benefits extend far beyond the immediate yield improvement. When manufacturers reduce the number of manual interventions, chemical dependencies, and process variations inside the production flow, they also reduce long-term manufacturing instability.

This has major implications for process repeatability, line scalability, equipment standardization, environmental compliance, operator training, production uptime, and global manufacturing transfer. As production volumes increase, these operational advantages become increasingly valuable. In many cases, the manufacturing simplification enabled by automated laser-based processes may ultimately prove just as important as the direct yield improvement itself.

AI infrastructure is compressing the industry timeline

The rapid expansion of AI infrastructure is accelerating every manufacturing challenge facing silicon photonics. Higher bandwidth demand is driving larger PIC complexity, higher optical channel counts, more advanced packaging, tighter thermal budgets, greater power efficiency requirements, and faster production ramp expectations. Multi-billion-dollar supply agreements between hyperscalers and photonics suppliers reinforce the urgency, leaving far less room for inefficient manufacturing processes.

The industry is now approaching an inflection point like previous transitions in CMOS manufacturing, where entirely new process technologies became necessary to support scaling. Historically, semiconductor manufacturing evolved through major transitions such as chemical-mechanical polishing, ion implantation, immersion lithography, FinFET integration, and EUV lithography. Each transition emerged because existing manufacturing approaches could no longer support the next generation of device requirements.

Silicon photonics is approaching a similar moment. Wafer-level laser trimming and selective laser cleaning are no longer niche laboratory processes. They are increasingly becoming manufacturing-enabling technologies for high-volume photonic production, with equipment platforms now being qualified inside foundries and packaging houses rather than confined to research benches. The

strategic question is no longer whether these capabilities will become important. The real question is how quickly manufacturers will integrate them into scalable production environments, and how aggressively process development teams will treat them as default tooling rather than optional add-ons.

Manufacturing scalability will define the next phase of silicon photonics

The next decade of silicon photonics will not be defined solely by better device architectures. It will be defined by manufacturing scalability. The companies that successfully reduce phase variation, simplify test flows, minimize contamination-driven yield loss, and lower operational complexity will ultimately define the cost structure of future photonic systems. That cost structure will directly influence the economics of AI infrastructure itself. This is why manufacturing innovation is becoming just as strategically important as device innovation.

The industry has already demonstrated that silicon photonics can deliver the performance required for next-generation optical interconnects. Now the challenge is manufacturing enough devices reliably,



consistently, and economically to support global AI infrastructure deployment over the coming decade. Solving that challenge will require new manufacturing approaches designed specifically for the realities of photonic devices, not simply adapted from traditional semiconductor processes built around very different physical sensitivities. And increasingly, laser-based manufacturing technologies are becoming a central part of that solution. The manufacturers that recognize this shift earliest, and rebuild their process flows around it, will be the ones setting the pace for everyone else.



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Building smarter semiconductor manufacturing with AI

In this interview, Ivan Nikitski, Photonics Technology Expert from EPIC – European Photonics Industry Consortium, talks to Aftkhar Aslam, CEO at yieldWerx, a US developer of data analytics and AI software for the semiconductor manufacturing industry.

Ivan Nikitski: What's the background to you co-founding yieldWerx?

Aftkhar Aslam: In 1994, after studying computer science and pure maths, I joined Texas Instruments in Dallas, Texas, where I stayed for 15 years eventually becoming Director of Design/R&D Engineering Applications. Because TI is an integrated device manufacturer (IDM), it was a great learning experience as I got to know about the entire end-to-end process—from design to tape-out, through manufacturing, assembly, and testing.

In 2009, I joined Accenture and did management consulting, implementing digital transformations for companies like Intel, Qualcomm, and Lam Research. During this period, a colleague and I came to realise that there was a business opportunity. We could take the best of what we had learned at TI and apply it to help other companies overcome challenges.

Accordingly, in 2015, we started yieldWerx with me as CEO/CTO.

Ivan Nikitski: How has yieldWerx developed?

Aftkhar Aslam: We set up the company as an enterprise platform to enable IDMs, foundries, EDA vendors, and equipment manufacturers to analyse data in order to identify yield, process and design issues as well as to be better able to monitor processes, reliability, quality, sustainability, and overall portfolio health.

We started with primary modules for engineers to use for data analysis. Since then, we've developed our own IPs to help customers improve yield, particularly in life sciences and automotive. We're now applying those same reliability and quality modules to the quantum computing and photonics industries, because reliability will become increasingly important there.

Another major milestone has been the introduction of AI, which we are adopting cautiously because any product or quality escape can have catastrophic consequences in our industry. The next major milestone will be the use of agentic AI (autonomous AI systems to achieve specific goals), to tackle many of the industry's challenges and make our solutions even more comprehensive.

As regards customers, in the beginning we secured the US company Monolithic Power Systems and another anchor account who are still with us. Since then, we've developed an extensive network of partners who are trained on our platform and able to provide local support. This has allowed us to serve customers in the US, Europe and China, Japan, Korea, Taiwan, Singapore, Malaysia, and the rapidly growing market in India. In this period, our workforce has grown to more than

60 full-time staff based across the US, Europe, and Asia.

Ivan Nikitski: What are the main challenges in finding new customers?

Aftkhar Aslam: Our software is very modular to make it configurable and flexible and also beneficial from a pricing perspective because customers aren't paying for functionality they don't need. For example, a customer may have one product destined for the automotive industry, where the highest levels of reliability and quality are required. They may have other products for agricultural equipment or consumer markets, where those requirements are different.

Having said this, one of the biggest challenges has been helping customers understand the long-term vision. Many companies have homegrown solutions and believe they can solve problems better themselves. We try to demonstrate that we've worked with customers across many industries, platforms, and vertical markets, and that our solutions have been tried, tested, and trusted often providing advantages over internally developed systems.

Another challenge is convincing customers to adopt a brownfield implementation, where we integrate

the best of our platform with the best of theirs.

There's also the fundamental question of trust. Customers ask why they should trust us and what makes us different. This is where our experience from Texas Instruments becomes valuable as we speak the same language and can demonstrate how we've solved similar problems for other companies. Nevertheless, platform decisions are complex, lengthy, and often involve significant bureaucracy. And navigating that process is one of our biggest challenges.

Ivan Nikitski: What are the main challenges in working with AI?

Aftkhar Aslam: For the traditional semiconductor industry (analogue, signal processing, RF) AI is mature enough to be applied effectively. But when we move into areas like photonics, quantum computing, or microLEDs, there are several challenges.

The first is data quality. Labelling data correctly is very important. You need to know whether data is good, bad, or what we call "maverick" data—data whose quality is uncertain. In many cases, customers don't even have a methodology for labelling their data,

Our software is very modular to make it configurable and flexible and also beneficial from a pricing perspective because customers aren't paying for functionality they don't need.

which makes it difficult to achieve reliable results.

The second challenge is building and training the models and then proving to customers that the AI solution works for their specific products. Every product is unique, from die size to the test data collected and even the naming conventions used for test parameters.

The third challenge is security. Customers naturally want to know whether the data they're providing is secure. They also want assurance that the knowledge gained from their data won't be used to benefit another customer, particularly a competitor.



That's something we take very seriously.

The final challenge is managing expectations. Customers sometimes expect AI to perform miracles. In reality, AI is a journey. You observe, learn, train, refine, and gradually build trust in the system. Eventually, AI can take on more responsibility in processing incoming data and supporting decision-making.

Ivan Nikitski: What are the main challenges in accessing new markets?

Aftkhar Aslam: As regards photonics and quantum computing, one of the biggest challenges is data protection as there are many companies competing with one another.

Another challenge is the lack of collaboration, standards, and established methodologies within the photonics industry. This means that when it comes to testing photonic devices, questions remain such as what data should be collected, what standards should be used, and how electrical and optical data can be combined while maintaining traceability from design through wafer fabrication to a single die. This problem is going to be exacerbated as moving toward multi-stack dies and optical modules will create even greater complexity.

Ivan Nikitski: How do you see the future of yieldWerx?

The semiconductor industry has always been cyclical, but what we're seeing now is significant long-term growth, driven in large part by AI. It's not only software that's growing. The hardware ecosystem is expanding.

Aftkhar Aslam: I'm very optimistic about the future. The semiconductor industry has always been cyclical, but what we're seeing now is significant long-term growth, driven in large part by AI. It's not only software that's growing. The hardware ecosystem is expanding as well, and AI will touch many different aspects of people's lives.

We see quantum computing, photonics, lasers, and microLED technologies as a tremendous opportunity for us because these sectors will require increasingly sophisticated platforms like yieldWerx to improve yield, optimize designs, and refine manufacturing processes.

Looking ahead, quantum computing and photonic technologies will be instrumental not only in accelerating AI but also in making data centers more efficient, reducing power consumption, increasing data transfer speeds, and supporting sustainability. Over time, these technologies will also expand into industries such as automotive and life sciences.

For yieldWerx, the challenge is keeping pace with the increasing volume of data, the growing complexity of products, and the rapid evolution of technology. And we will need to continue accelerating our own platform development to meet those needs.

Ivan Nikitski: What's your advice for the next generation of entrepreneurs?

Aftkhar Aslam: Even if you're an excellent data scientist and you're able to leverage AI effectively, you still need to understand the basic underlying engineering principles of semiconductor technology: what a semiconductor is and how products are designed, manufactured, assembled, and tested.

As technology nodes continue to shrink, manufacturing equipment is becoming increasingly sophisticated, and the amount of data being generated is enormous. But without knowledge of basic engineering principles, it's very difficult to build solutions that truly serve the industry.





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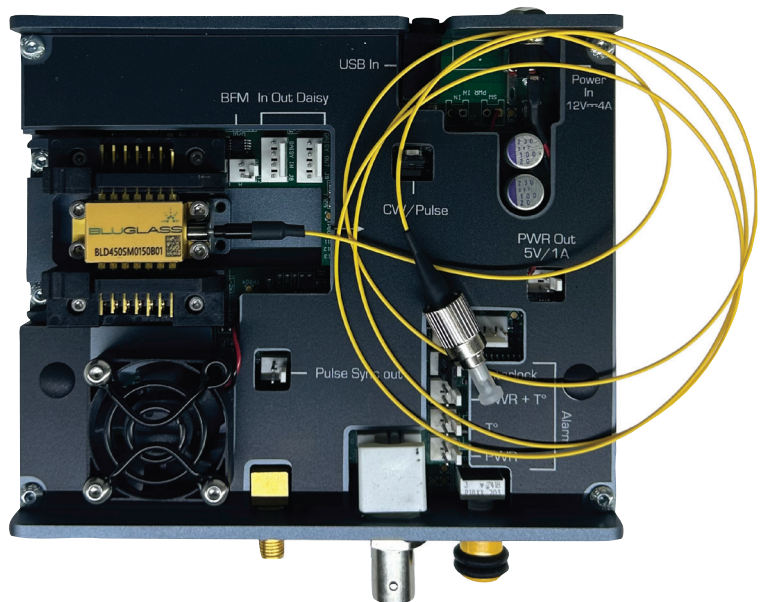
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GaN-based lasers for quantum applications

Blue lasers with surface gratings are delivering quantum precision from millimetre footprints

BY RYAN ANDERSON FROM
BLUGLASS



THE VISIBLE SPECTRUM is an exciting frontier for laser diode technology. Here emerging applications exist, demanding sources with a small size, low power consumption and high-fidelity.

Addressing this need are narrow-linewidth lasers. Capable of single-frequency emission, these emitters enable breakthroughs in quantum computing, quantum sensing, and secure communications.

For those in search of a narrow-linewidth laser, an attractive candidate is the GaN-based distributed feedback (DFB) laser, a device we have developed at BluGlass. We view this source as a significant

step in the progress of narrow-linewidth lasers, because our device combines a compact form with a relatively straightforward manufacturing process and a level of performance that promises to drive innovation in visible photonics.

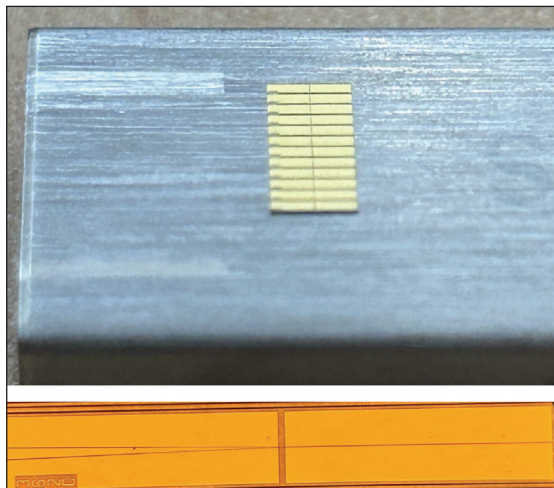
Precision emission

For every laser, its spectral linewidth has a profound impact on how it interacts with its environment. When the linewidth is narrow, nearly all emitted energy is concentrated into a useful optical frequency. That's a massive asset when serving in an atomic system, as this exactness makes the difference between realising the resonance for laser cooling or missing the absorption line entirely.

Quantum technologies, which depend on a high degree of accuracy and precision, rely on the excitation of sensitive atomic transitions by lasers emitting at specific wavelengths. Within this sector, Rydberg sensors are emerging as power detectors for electric fields. These sensors, requiring visible light with linewidths of hundreds of kilohertz, can target many applications, ranging from high-resolution RF imaging and communication and surveillance to quantum computing and networks for defence and aerospace.

In addition to quantum applications, lasers emitting in the blue and green are compelling candidates for underwater communications and lidar, thanks to operation in the spectral sweet spot for water penetration. Similarly, these wavelengths can

➤ A bar with 12 high power GaN laser chips on a USB stick for size comparison. The optical microscope image is a higher magnification of a single chip.



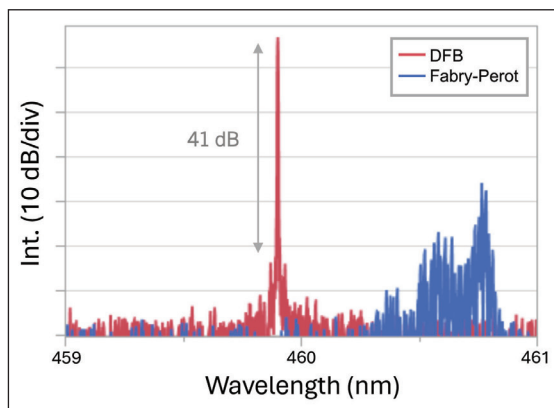
provide the optical source for remote detection of aerosols, gases, and clear-air turbulence, helping scientists understand weather patterns and pilots avoid dangerous flightpaths in otherwise impossible-to-detect conditions.

In all these applications, one theme is clear: there's a need for compact, stable, scalable narrow-linewidth sources in the visible regime.

Comparing options

The narrow-linewidth laser can take various forms, all involving significant trade-offs between performance, complexity and practicality.

In general, external cavity diode lasers are a well-established source with an excellent linewidth. Incorporating tuneable optical cavities outside the laser medium, this class of laser requires quite sophisticated precision optics. This often results in bulky but delicate benchtop systems, needing alignment, isolation, and complex packaging.



➤ The difference between a single-frequency laser and typical Fabry-Pérot laser diode are starkly evident when comparing the spectral characteristics measured in an optical spectrum analyser. The width of the DFB laser is less than 3 picometers and limited by the resolution of the measurement system, while the Fabry-Perot laser is approximately 0.5 nm.

Another promising approach for compact visible lasers are photonic integrated circuits (PICs) featuring GaN emitters. In this configuration, a laser gain section is fabricated on a chip that couples the optical output into waveguides, with external resonators or filters controlling the emission frequency. GaN-based lasers featuring a ring resonator as a PIC have produced impressively narrow linewidths, but at the expense of complex wafer bonding and multi-step processing. Each additional layer of integration may double or triple fabrication complexity.

We are trailblazing a third route: the GaN distributed feedback (DFB) laser. This design, already well-established in lasers made from traditional III-Vs,

uses a precisely defined grating that's built into the optical cavity to select and stabilise a single-emission wavelength. While DFBs are yet to match the sub-100 kHz linewidths of the most advanced PIC-based systems, they offer a balance of performance, size, and manufacturability practical for large-scale deployment.

In our view, all three classes of narrow-linewidth laser have a role to play in the application landscape. Here, the GaN DFBs occupy the critical middle ground, as they are simpler than external-cavity diode lasers and cheaper than heterogeneous PICs, while still delivering narrow linewidths and a stability sufficient for most quantum and sensing applications.

GaN DFB challenges

Replicating the processes employed for making III-V DFB lasers with a GaN-based material systems is far from trivial. The primary challenge stems from difficult epitaxial layer growth in the III-nitride hexagonal material system. With conventional III-V DFB lasers, fabrication involves overgrowth of patterned semiconductor layers, a step that's typically straightforward in a cubic material system. In stark contrast, regrowing GaN over etched gratings tends to introduce defects or roughness, compromising optical and electrical performance. To address this concern, some groups turn to porous GaN layers or laterally etched gratings. However, impressive results are realised with methods that add complexity or introduce new limitations.

We have developed a different approach that avoids deep etching and regrowth entirely. Instead, we form embedded surface gratings in the transparent, conductive material indium tin oxide (ITO).

With our approach, after epitaxial growth of our GaN laser structure, we deposit ITO as a transparent *p*-contact. We then define nanoscale gratings in this oxide by electron-beam lithography. After writing them, they are directly embedded under another thin ITO layer to preserve a smooth, conductive surface for current spreading.

This design, originally developed at the University of California, Santa Barbara (UCSB), and refined through our ongoing collaboration, avoids the most challenging aspects of GaN fabrication. It minimises damage to the *p*-GaN layer, maintains optical quality, and integrates the feedback mechanism directly within the device's current-spreading layer.

Record-breaking linewidths

Over the last few years our team has made significant strides in optimising the epitaxial structure and the embedded grating design. By refining the optical mode overlap and the coupling strength, we've realised side-mode suppression ratios (SMSRs) exceeding 40 dB, a clear indication of single-mode operation.

An even more impressive result is a linewidth of just 680 kHz, recorded when UCSB researchers measured the fundamental linewidth of our embedded-grating GaN DFB laser using a correlated self-heterodyne setup. To our knowledge, this is the narrowest fundamental linewidth reported for a nitride-based DFB laser.

Thanks to this result, we know that our GaN DFBs are within the performance range for laser cooling, atomic sensing and visible lidar applications – and they are within striking distance of 100 kHz, which could open the door to even more demanding quantum technologies.

Wavelength tuning

Linewidth is not the only critical characteristic for a single-frequency laser. It's also essential that accuracy and precision hit a bullseye regarding the target wavelength of a particular application; and the laser runs at a stable wavelength under a wide range of operating conditions.

To consider these criteria, we've compared our DFBs against Fabry-Pérot lasers from the same wafer, operating under varying temperatures and currents. Under those conditions, our lasers maintain single-mode operation and shift by only 17 picometers per degree Celsius. This is a remarkably low sensitivity to temperature compared with traditional III-V lasers. Our DFBs also exhibit a very low wavelength drift during current sweep. This robustness makes our sources ideal for portable applications, where environmental control isn't perfect.

For some applications it's essential to provide a modest tunability, on the order of a few nanometres – this feature enables locking to atomic transitions. It is challenging to meet this need with GaN, due to a relatively stable refractive index with temperature; and it's also not easy to take the well-trodden path

of adding regrown passive phase sections, to create a device that's similar to an external cavity.

As a first step towards coarse tunability, we have explored prototypes with two cavities resembling distributed Bragg reflector lasers. While these devices undergo mode hops during current adjustment, we are optimistic that clever design will enable pathways for realising controlled tuning in multi-section lasers. Through ongoing work, we are aiming to refine these structures and explore three-section architectures that combine stability with electronic control.

Scaling-up power

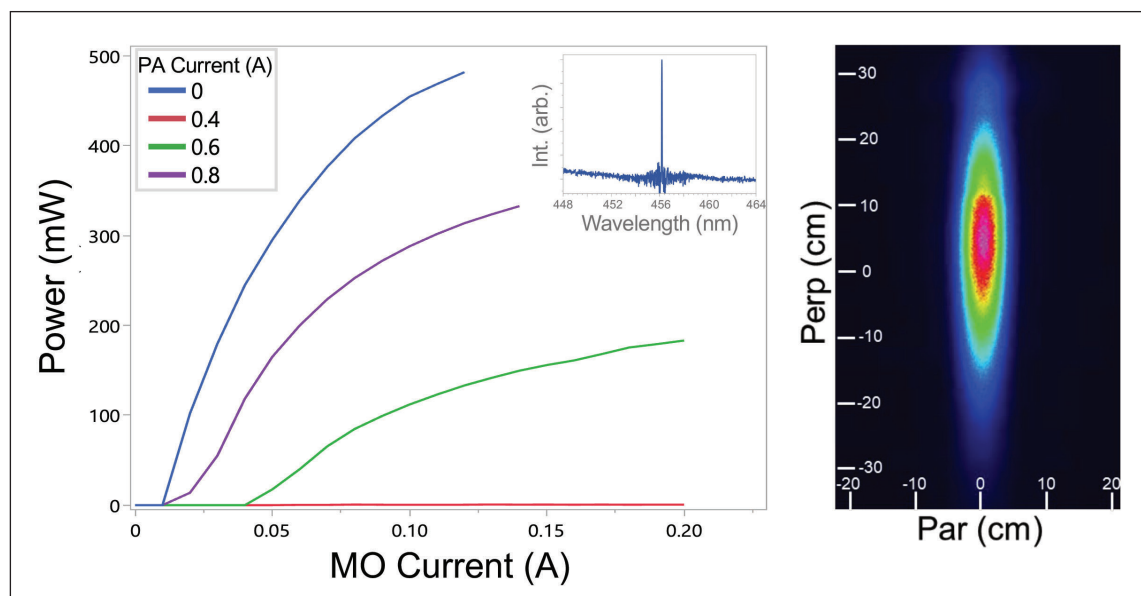
Many applications require not just stable light, but a lot of it. We have already demonstrated DFBs with up to 100 mW of single-frequency emission, and we are pushing toward hundreds of milliwatts and beyond, via the introduction of semiconductor optical amplifiers and configurations that include master oscillator power amplifiers.

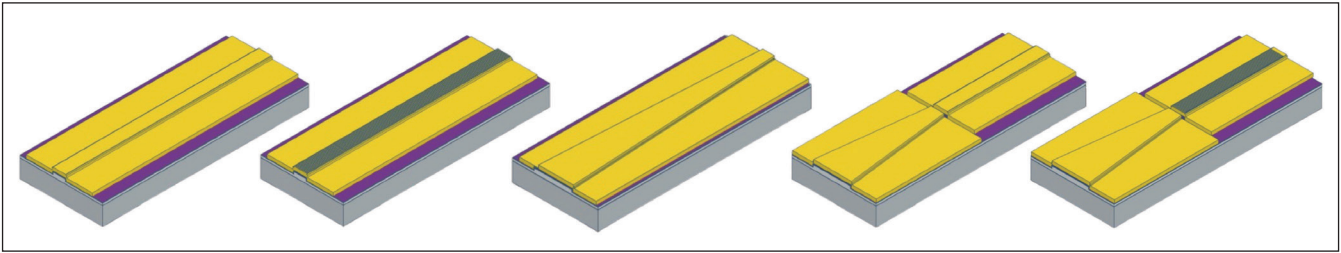
To create efficient amplifiers, we've developed anti-reflective coatings that have a reflectivity of less than 0.1 percent at 450 nm. According to initial tests, amplifiers with these coatings, which prevent unwanted feedback and lasing modes in the external cavity, provide up to 15 dB of optical gain with minimal optimisation.

We have also fabricated integrated devices with master oscillator power amplifiers that combine a Fabry-Pérot or DFB seed section with a tapered amplifier. By carefully controlling amplifier geometry and current drive, we have produced more than 400 mW of power under quasi-CW operation while maintaining a single spatial mode in the far-field.

Following additional refinements in epitaxy, facet coatings, and thermal design, we expect to propel output powers towards 1 W without compromising

➤ Light output for a master-oscillator and power amplifier configured laser diode. The inset exhibits the narrow linewidth spectral peak and the associated far-field mode profile at 400 mW of output power. The test is performed under quasi-continuous wave electrical injection.





➤ Chip types manufactured by BluGlass from left to right including basic Fabry-Pérot lasers, DFBs, semi-conductor optical amplifiers, single spatial mode MOPAs, and high-power single-frequency lasers.

linewidth or mode quality. That's a level of performance that could unlock new boundaries in visible-light sensing and communication systems.

Ensuring consistency

Equally important to achieving narrow linewidths is consistency across wafers and manufacturing batches. To succeed in this regard, we have partnered with Fred Kish's group at North Carolina State University, carrying out simulations that lead to improved laser diode performance. Their team's modelling combines band-structure calculations with carrier transport, cavity mode analysis and coupled-wave theory to elicit a model for fabricated devices.

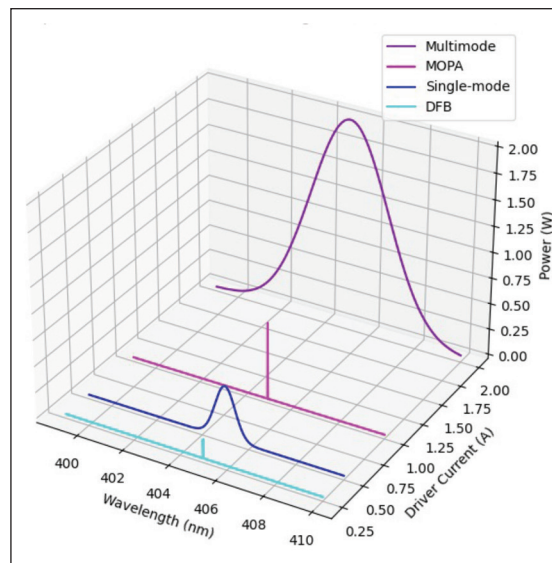
Using our data for a lower-performing 442 nm DFB laser, their model pinpointed two causes for poor performance: a low coupling coefficient, and a mismatch between the grating peak and gain peak. Modelling also determined that increases in the coupling coefficient produce a dramatic increase in the predicted side-mode suppression ratio and the threshold current, even with a slight detuning of the grating wavelength to the gain peak. These insights are guiding our epitaxial layer design, and enabling us to systematically realise higher-performing, more repeatable DFB lasers.

Looking forward

The promise of GaN DFB lasers lies not only in their performance, but in their scalability and versatility. Unlike high-end laser technologies that are confined to research labs, DFBs are chip-scale, manufacturable, and integrable. With careful design, they can be arrayed, wavelength-locked, or coupled to amplifiers – advances that create a platform for diverse applications, ranging from quantum networks to compact lidar sensors.

Our roadmap includes reducing linewidths to 100 kHz or less, increasing yield and reproducibility across wafers, enhancing tunability without sacrificing mode purity, and scaling output power to the watt range.

We view visible-light GaN DFBs as a foundational technology for the next generation of photonics in quantum systems. By combining materials innovation and optical engineering, while collaborating with leading academic partners, we



➤ The relative peaks and magnitudes of various devices manufactured by BluGlass under current in the violet wavelength regime.

are advancing practical, scalable solutions that will power the quantum and sensing systems of tomorrow.

The ability to generate blue light that's precise and stable is transforming what's possible in science and technology. Our GaN-based DFB lasers are compelling candidates for meeting the demand for a manufacturable platform that delivers narrow linewidths and high power in a compact form.

As our research continues, we have no doubt that the innovations provided by us, and our partners, will play a pivotal role in shaping the visible photonics landscape.

FURTHER READING

- R. Anderson *et al.* "Advancements in GaN DFBs with embedded gratings and a path to higher power", Proc. SPIE 13345, High-Power Diode Laser Technology XXIII, 1334510 (21 March 2025)



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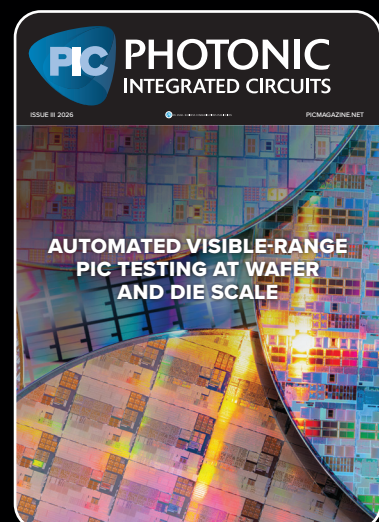
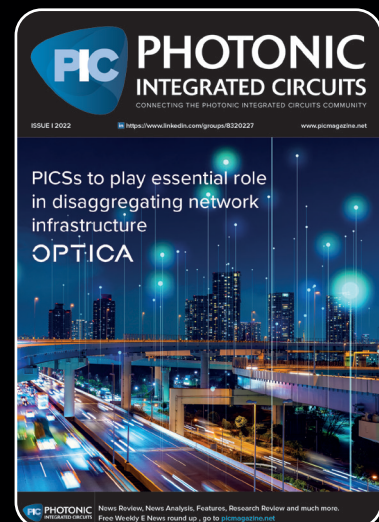
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