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ISSUE I 2025
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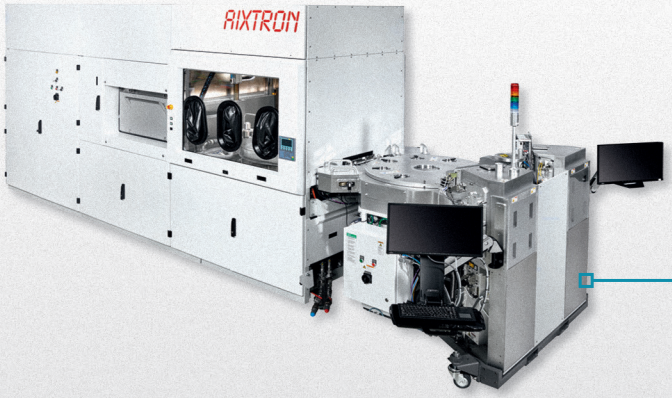

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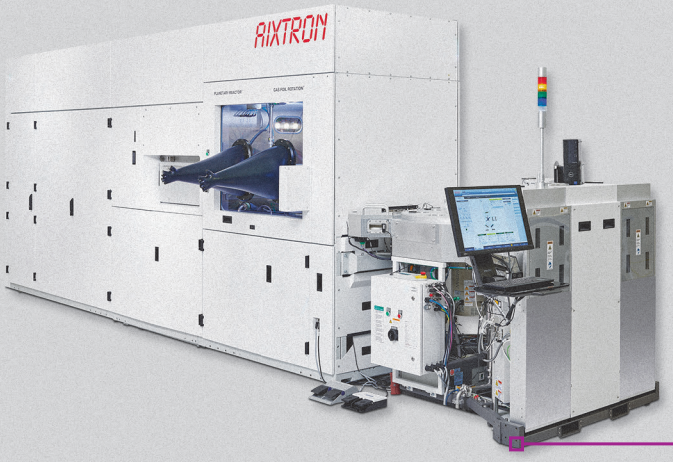

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VIEWPOINT

BY PHIL ALSOP EDITOR

A powerful year ahead

A SCAN of the news stories in this issue of PEW, alongside the many more to be found on the magazine website, provides any number of reasons to be optimistic for the power electronics sector, at a time when it is perhaps difficult to find too many reasons to be cheerful, amidst the ongoing global geopolitical uncertainties and the apparent growing momentum behind climate change push back (at least by the finance sector which bankrolls so much of the necessary investment activity).

'GaN adoption at tipping point' – Infineon believes that 2025 is the year when GaN will be a game-changing material across consumer, mobility, residential solar, telecommunication, and AI data centre industries, enabling more efficient performance, smaller size, lighter weight, and lower overall cost - substantially driving the market for GaN-based power semiconductors. Few will disagree with such an assessment – the more so as several governments have announced major AI-focused initiatives, which will require plenty of new data centres. I guess there is a slight note of caution while the 'mysteries' of the DeepSeek model are yet to be fully understood, but the direction of travel for digital transformation, with whatever level of AI-fuelled innovation, is clear for all to see.

'Medium-voltage SiC-based system developed at Fraunhofer ISE enables peak loads of several megawatts' – As the headline suggests, Fraunhofer ISE and partners have developed a SiC-based medium voltage system technology for fast charging stations that will enable peak loads of several megawatts in the future. The technology, which uses efficient SiC semiconductors and higher voltages, leads to lower material use and lower costs for fast charging stations.

At the same time, the system is very efficient and can be flexibly applied to charging stations of different sizes and different vehicle types. I have written previously about the 'chicken and egg' situation of what needs to come first – widespread EV adoption or the charging infrastructure to support EVs – and developments such as this one can only help to speed up what maybe will end up being the lockstep expansion of both EV ownership and charging station infrastructure expansion. Again, one slight note of caution – the US EV market could best be described as in something of a hiatus right now. Elsewhere, the EV commitment seems to be holding firm, if at varying rates of progress.

Perhaps the most encouraging of the news stories, alongside the innovation story above, are those which demonstrate the vibrant state of research and development work in the power electronics sector: 'EU project to develop high voltage DC WBG tech', 'UK team leads diamond-FET breakthrough', 'Transforming the current density of AlN Schottky barrier diodes', 'Turbocharging the GaN MOSFET with a HfO_2 gate', 'Boosting AlN-on-AlN Schottky barrier diode performance', 'Improving annealing conditions for GaN MOSFETs', 'Na flux method improves GaN device performance', 'German start-up secures finance for SiC processing tech'.

There's no doubting the huge commitment to power electronics innovation across the globe right now. However successful the attempts to 'derail' the climate change agenda, there's no doubting that energy resources, power infrastructure and power consumption will continue to remain a critical focus across all industry sectors, as well as in the domestic market. If there is one silver lining (and maybe the only one) to take out of the Ukraine/Russia conflict, it is the attention it has served to focus on all things energy and power related, with efficiency right at the top of the agenda. And the ongoing quest for more and more efficiency make sense for so many business reasons, whatever one's view on net zero.

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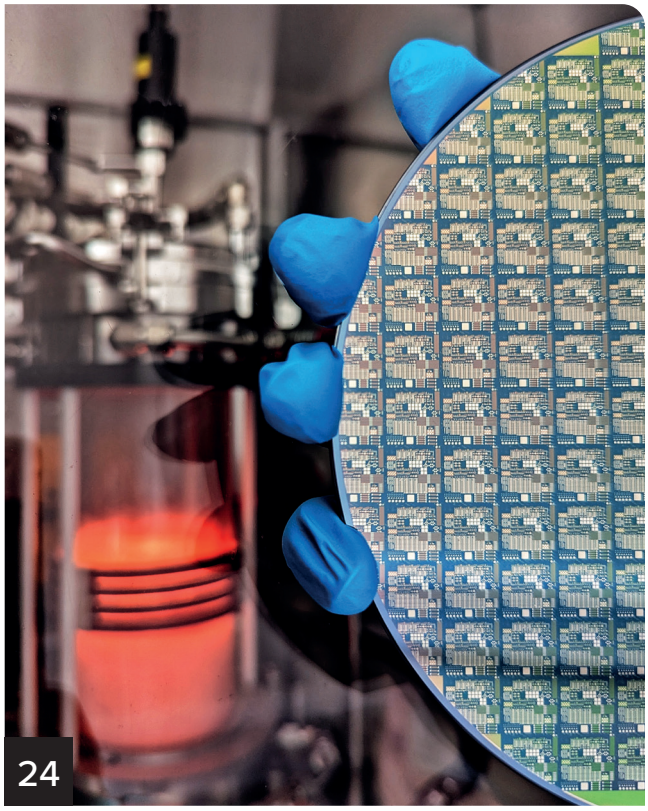

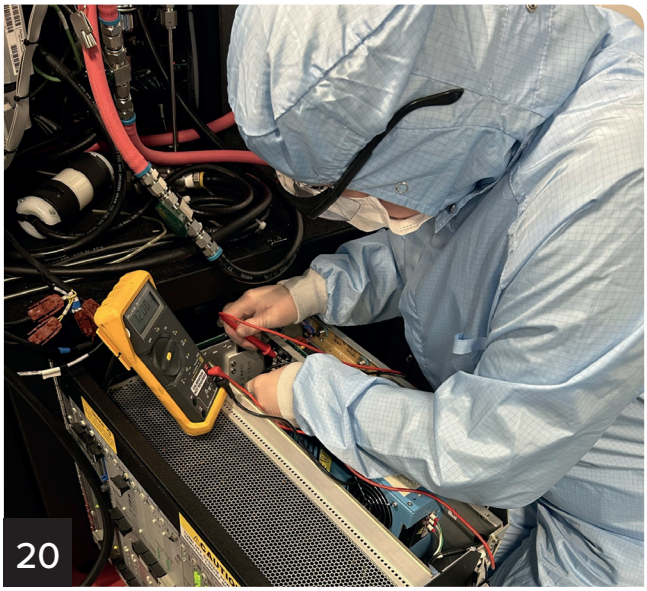

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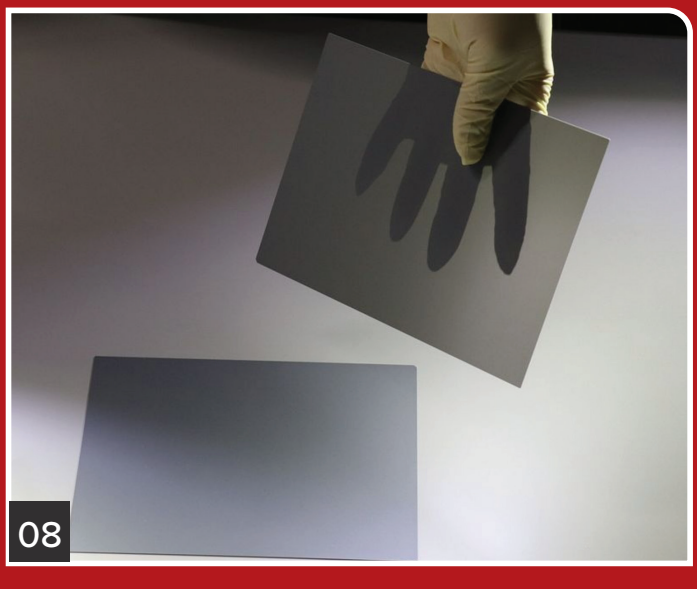

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Angel BUSINESS COMMUNICATIONS

SiC patenting strong in Q4 2024, says KnowMade

KnowMade's SiC Patent Monitor showed 900 new patent families and 400 newly granted patents

DURING Q4 2024, KnowMade's SiC Patent Monitor showed 900 new patent families and 400 newly granted patents. This period also saw over 100 patents expire or be abandoned and involved seven notable patent transfers.

There was no new IP litigation in the US or patent opposition in Europe. And the sector is "abuzz with ten notable patent collaborations and an influx of over 25 IP newcomers entering the field", according to KnowMade.

Innovation within the SiC industry, particularly in Bulk and bare wafers, has led to the emergence of better substrates and more reliable power devices. During Q4 2024, for example, NGK Insulators disclosed a composite SiC substrate with a biaxially oriented SiC layer that helps to reduce warpage.

Another player, SICC, published innovations improving 3D stress distribution and reducing internal stress in large diameter SiC wafers (> 150 mm). Sumitomo Electric continues to lead IP activities in epitaxial substrates, according to KnowMade, with four new inventions disclosed during Q4. One of these relates to issues in the epitaxial reactor, such as the presence of SiC particles on the susceptor, causing recesses in the rear surface of SiC epitaxial wafers.

Another invention focuses on the reduction of certain defects (bump, pit, carrot, triangular defect, downfall) that can be imaged using a confocal scanning device.

For devices, there has been patenting activity from several Chinese automotive players, such as NIO and FAW. NIO stands out this quarter with a European patent publication related to SiC trench MOSFET. Other players from the automotive supply chain have been actively filing patents during the quarter such as Bosch (e.g., to improve the short-circuit strength of SiC FET) and Nexperia (e.g., to improve on-resistance and surge performance of SiC Schottky diodes).

In terms of modules and packaging, Onsemi has disclosed electroless plating methods and systems suitable for SiC devices, and Mitsubishi Electric has two new inventions, of which one to suppress heat occurring in a SiC MOSFET connected in parallel with a Si IGBT, without providing a temperature detection circuit and a current detection circuit. GaN specialist Navitas Semiconductor is also looking to strengthen its patent portfolio for power SiC, with a new invention providing balanced current flow in SiC power modules.

For circuits and application, ZF has developed a method of driving parallel-connected SiC-MOSFETs and Si-IGBTs based on the rapid detection of the current load of the active (switched-on) device. Furthermore, a collaboration between BMW with CSA Catapult and the University of Warwick in the UK has led to a new patent publication describing a monitoring device to measure temperature or current in SiC devices under high current load even under rough mechanical conditions (e.g., under strong vibrations, in automotive appliances).

KnowMade closely follows SiC patenting, and has noted recently that the number of inventions disclosed in 2023 was more than 50 percent higher than it was in 2021. The number of inventions disclosed by Chinese players increased by about 60 percent between 2021 and 2023.

For circuits and application, ZF has developed a method of driving parallel-connected SiC-MOSFETs and Si-IGBTs based on the rapid detection of the current load of the active (switched-on) device. Furthermore, a collaboration between BMW with CSA Catapult and the University of Warwick in the UK has led to a new patent publication describing a monitoring device to measure temperature or current in SiC devices

SiC MOSFETs: Understanding the benefits of plasma nitridation

Annealing interfaces of SiC and SiO_2 formed by a process based on plasma nitridation reduces interface states and increases immunity to positive gate bias stress

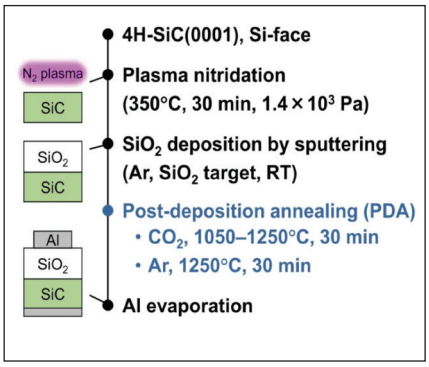
ENGINEERS from Osaka University are offering new insights into the benefits of their novel approach to forming the key interface for SiC MOSFETs.
The team has just determined that its approach – involving plasma nitridation of the SiC surface, sputter deposition of SiO_2, and post-deposition annealing – reduces the interface state density near the conduction band edge by more than an order of magnitude and delivers a substantial increase in immunity to positive gate bias stress.

These valuable findings highlight the benefits of moving away from standard approaches to making SiC MOSFETs, which despite significant commercial success suffer from a high on-resistance and poor reliability, according to the team from Osaka. This team attributes those weaknesses to a high interface state density and near-interface traps.

The Osaka University researchers say that interface nitridation with NO is widely used to reduce the interface state density and passivate defects. However, this approach is far from perfect: the reduction in the density of interface states is limited, probably due to saturation of nitrogen content at the interface; and there are reliability issues, such as a strong drift in threshold voltage with gate bias stress.

To address these concerns, the engineers from Osaka are pioneering an approach that suppresses nitrogen incorporation into SiO_2 while minimising oxidation of SiC. Their three-step process involves: plasma nitridation of the SiC surface; sputter deposition of SiO_2; and post-deposition annealing under CO_2.

According to the team, one of the benefits of this approach is that SiC is directly nitrided by a high-density



plasma, enabling a high proportion of nitrogen atoms to be incorporated at the SiC surface. Additional merits of their approach include sputter deposition of SiO_2 in a pure argon atmosphere to minimise SiC oxidation, and a post-deposition anneal that reduces the density of defects in the SiO_2 dielectric. The researchers previously established that their process trebled the density of nitrogen atoms incorporated at the SiC side of the interface, lowering the density of interface states to 1 x 1011 eV^{-1} cm^{-2}. However, they had not investigated the impact of post-deposition annealing on device characteristics.

They have just addressed this issue with a thorough investigation of the roles played by the particular gas employed and the temperature that's adopted for the post-deposition anneal. For this work, they produced SiC metal-oxide-semiconductor capacitors, using n-type SiC (0001) epilayers with a donor density of 1 x 10^{16} cm^{-3}. Following wet cleaning, they nitrided the surface of SiC for 30 minutes at 350°C with a high-density nitrogen plasma at 1.4 x 10^3 Pa, before sputtering a 30 nm-thick film of SiO_2 in a pure argon atmosphere. The final step involved a post-deposition anneal for 30 minutes under either CO_2or argon at a temperature between 1050°C and 1250°C. Comparing capacitance-voltage curves for annealing under CO_2 at different temperatures showed that carrying out this process at 1050°C ensured sufficient electron accumulation. However, this technique led to hysteresis and stretch-out due to interface traps. Both concerns were not found in capacitance-voltage plots for devices with a 1250°C anneal, suggesting a significant reduction in interface traps.

The researchers also observed a negative shift in the capacitance-voltage curve with increasing anneal temperature, indicating the presence of positive fixed charges at the interface. Additional investigations by the team considered the trapped charge density and the energy distributions of interface states. For annealing under CO2, the trapped charge density plumets with increasing annealing temperature. Under argon, the fall in trapped charge density is notably smaller, leading the team to conclude that the reduction in charge density is not simply an annealing effect, and involves a reaction of CO_2 molecules with interface traps.

Studying the energy distribution of the interface state density revealed that this fell with increasing temperature when annealing under CO_2. Switching to argon led to an insufficient reduction in interface state density, showing that the benefits of the team's process are not just plasma nitridation and minimised oxidation – they also include defect passivation by a CO_2 post-deposition anneal. The team have also carried out stress tests, applying a positive stress bias for up to 2000 s at field strength of 5-8 MV cm-1. This investigation revealed that a higher annealing temperature under CO_2 increases the immunity of the device.

Reference: H. Fujimoto et al. Appl. Phys. Express 17 116503 (2024)

Research initiative on SiN ceramic substrates

Japanese partnership to verify methods for evaluating thermal performance of ultra thin power module substrates

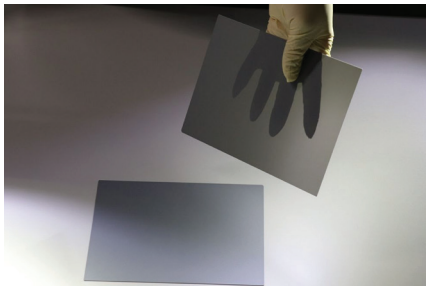
THE JAPANESE AIST Group (consisting of National Institute of Advanced Industrial Science and Technology and AIST Solutions) and NGK Insulators have embarked on joint research to validate methods for evaluating thermal diffusivity of SiN ceramic substrates used for power semiconductor components and modules.

SiN ceramic substrates play a pivotal role in Active Metal Brazing (AMB) substrates for heat dissipation in power modules in EV inverters and HEV motor control.

AMB substrates consist of a SiN ceramic substrate and two copper plates. The thinner the substrate and higher its thermal diffusivity, the greater the operational efficiency of the power semiconductor module.

With the increasing adoption of EVs and HEVs, there is rising demand for thinner substrates that feature substantial thermal dissipation performance. However, a lack of definitive methods for evaluating thermal diffusivity of substrates thinner than 0.5mm has given rise to challenges in ensuring consistency of measurement results.

This joint research enlists AIST and its knowledge of evaluation methods along with NGK and its ceramic substrate technologies in efforts to collect data for quantifying the preliminary process,



which affects measurement of thermal diffusivity of substrates. The aim is to verify methods for evaluating substrates that are thinner than 0.5mm, and are not yet defined under existing Japanese Industrial Standards (JIS) in order to bring about standardisation of evaluation methods in this sector.

GaN adoption at tipping point, says Infineon

IN ITS 2025 predictions, Infineon says GaN will be a game-changing material across consumer, mobility, residential solar, telecommunication, and AI data centre industries, enabling more efficient performance, smaller size, lighter weight, and lower overall cost.

While USB-C chargers and adapters have been the forerunners, GaN is now on its way to reaching tipping points in its adoption in further industries, substantially driving the market for GaN-based power semiconductors, according to Infineon.

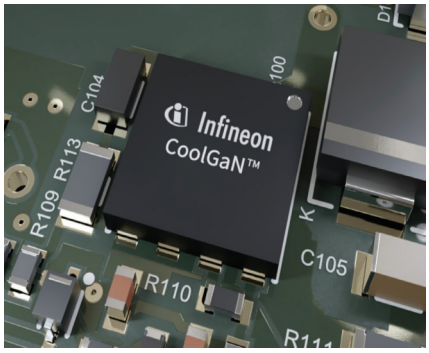
”Infineon is committed to driving decarbonisation and digitalisation through innovation based on all semiconductor materials Si, SiC, and GaN,” said Johannes Schoiswohl, head of the GaN business line at Infineon. “The relevance of comprehensive power systems will increase with GaN manifesting its role due to its benefits in efficiency, density, and size. Given that cost-parity with silicon is in sight, we will see an increased adoption rate for GaN this year and beyond.

Powering AI will be highly depending on GaN. The rapid increase of required computing power and energy demand in AI data centres will drive the need for advanced solutions capable of handling the substantial loads associated with AI servers.

Power supplies that once managed 3.3 kW are now evolving towards 5.5 kW, with projections moving towards 12 kW or more per unit.

By using GaN, AI data centres can improve power density, which directly influences the amount of computational power that can be delivered within a given rack space. While GaN presents clear advantages, hybrid approaches combining GaN with Si and SiC are ideal for meeting the requirements of AI data centres and achieving the best trade-offs between efficiency, power density and system cost.

In the home appliance market, Infineon expects GaN to gain significant traction, driven by the need for higher energy efficiency ratings in applications like



washing machines, dryers, refrigerators and water/heat pumps. In 800 W applications, for example, GaN can enable a two percent efficiency gain, which can help manufacturers achieve the coveted A ratings.

According to Infineon, GaN-based on-board chargers and DC-DC converters in electric vehicles will contribute to a higher charging efficiency, power density, and material sustainability, with a shift towards 20 kW+ systems.

Together with high-end SiC solutions, GaN will also enable more efficient traction inverters for both 400 V and 800 V EV systems, contributing to an increased driving range.

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Researchers develop tech for future fast-charging stations

Medium-voltage SiC-based system developed at Fraunhofer ISE enables peak loads of several megawatts

FRAUNHOFER ISE and partners have developed a SiC-based medium voltage system technology for fast charging stations that will enable peak loads of several megawatts in the future.

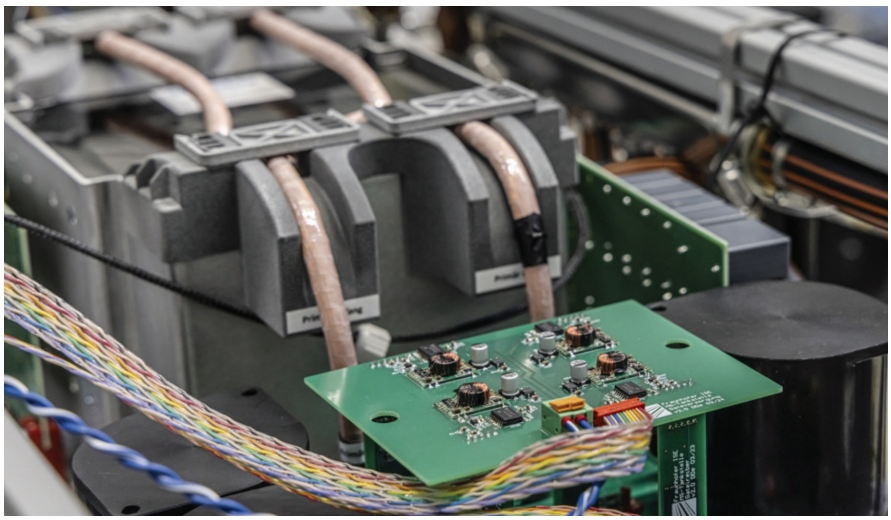
The technology, which uses efficient SiC semiconductors and higher voltages, leads to lower material use and lower costs for fast charging stations. At the same time, the system is very efficient and can be flexibly applied to charging stations of different sizes and different vehicle types, according to Fraunhofer ISE.

The system was developed in a project called MS-Tankstelle, to address the need for future charging stations along motorways, in parking lots or at logistics centres to be deliver much more power in a short space of time than they do today.

The average output of a fast-charging system for a car is 150 kW. This rises to 350 kW for buses, vans and small trucks, with higher charging capacities expected in the future. Since electric charging is slower than the refuelling process, around 15 to 25 charging points will be needed in the future instead of the typical eight gas pumps at filling stations today.

Together these charging points will draw around 1.5 to 3.5 megawatts of power when fast charging in parallel, which means that future fast-charging stations can no longer be supplied via the low-voltage grid. Even if the charging station is underutilized, the power required would exceed 300 kW. Also the power distribution within the charging station or parking lot should not be distributed in the low voltage grid. This would lead to big installation costs and large energy losses in cables, due to the long cable runs of e.g. 100 meters or more for 25 parking spaces, coupled with the high powers.
The power electronic system developed in the project with the partners Sumida Components & Modules GmbH, Infineon Technologies AG and AEG Powersolutions GmbH therefore relies on a medium voltage grid that is adapted to a voltage of 1500 VDC using a rectifier.

The higher voltage level enables a higher output at the same current without necessitating the cable cross-section to be increased. The significantly lower copper consumption that results contributes significantly to environmental protection and resource conservation. The value of 1500 VDC was selected for this unit, as it is the boundary limit of the low voltage standard. Above this value, other standards would apply.



An electrically isolated converter couples the direct current (DC) distribution network to the vehicle battery and controls the fast-charging process. The DC converters, each with an output of 175 kW, are designed so that they can easily be connected in parallel in the system. This modular approach makes it possible to build charging stations with lower power charging points for cars and higher power charging points for trucks.

In contrast to domestic wall boxes, charging stations must be highly compatible for different vehicle types. The concept of a central rectifier and a 1500 V DC distribution, which was developed in the project, is advantageous in that the grid connection components (transformer and rectifier) can be dimensioned and scaled more independently of the charging electronics. In view of the high demand for power electronics and components, like cables and transformers, the material requirements for this system are significantly reduced compared to other current solutions.
For an uncomplicated charging process, the charging station should be fully compatible with the CCS1 and CCS2 standards, which are widely established in Europe for vehicle currents up to 500 amperes and voltages up to 1000 volts. In addition, the concept also supports the Megawatt Charging System (MCS) standard. A second converter module is planned to address this. For this variant only a few components need to be adapted.

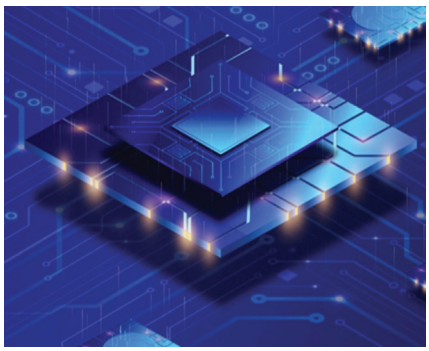
Mitsubishi joins Horizon Europe's FLAGCHIP project

Company to develop technology for monitoring SiC power module condition

MITSUBISHI ELECTRIC'S European subsidiary Mitsubishi Electric R&D Centre Europe BV will begin developing a prototype to demonstrate a junction-temperature estimation technology for SiC power modules, as a partner in the European Union's Horizon Europe FLAGCHIP project.

The technology will measure the condition of SiC-MOSFETs inside the power module, to provide data for accurately estimating module degradation.

FLAGCHIP (Flagship Advanced Solutions for Condition and Health Monitoring in Power Electronics)



involves 11 companies and academic institutions from nine European countries who will develop advanced power modules, condition and health monitoring technologies, and methods for calculating cost efficiency of renewable-energy power-generation systems and reducing associated costs.

The partners will demonstrate wind-power and solar-power generation systems using these technologies and methods at test facilities owned by project partners in Norway and France.

Starting in October 2026, the plan is to use the Mitsubishi Electric developed prototype at a test facility in France where direct current (DC) voltage is converted to a specific DC voltage for a wind-power generation system.

EU project to develop high voltage DC WBG tech

'MoWiLife' project to produce SiC and ultra wide bandgap devices for DC wind and solar energy applications

A NEW three-year multi-partner Horizon Europe funded project, called MoWiLife (Condition Monitoring and Wide Bandgap Power Electronics - Leading Innovations for the European Energy Sector), will be working on technology for DC wind and solar energy applications.

This includes the development of a 2.3 kV SiC MOSFET with temperature sensing and self-protection features. Additionally, the project explores the potential of ultra-high voltage and ultra-wide bandgap semiconductors, including diamonds as semiconductor materials, for energy savings.

The project features two wind energy converter pilots and two university-developed pilots: a TRL 5 DC-DC converter and a TRL 5 DC circuit breaker.

The basis for the four pilots is the 2.3 kV SiC MOSFET, which will be developed by project partner Infineon. It includes a source-gate PiN diode, whose on-state voltage has a strong temperature dependence and can be read out by the gate drive, which will be developed by Rostock University. In addition, self-protection features will be integrated into the SiC chip for robustness and direct water cooling will be realised for higher output power.

AC power can only be transmitted over relatively short distances with subsea cables, and as we look increasingly to offshore wind or tidal technology to meet growing demand, solutions are needed to create high-voltage direct current (HVDC) connections and to develop an HVDC grid

The two wind energy converter pilots are being realised by two industrial partners. As one of the technology leaders in wind energy, Vestas – supported by University of Aalborg – will develop a TRL 6 SiC converter with +20 percent power density and digital-twin Condition and Health Monitoring. The start-up RKL together with Rostock University will develop a TRL 5 wind energy power stack with Condition and Health Monitoring based on online chip temperature and on-state voltage measurement.

Solar medium voltage DC collection grids and meshed high voltage transmission grids will play an important role in the future. As third and fourth pilots, a TRL 5 DC-DC converter and a TRL 5 DC circuit breaker including condition monitoring are being developed by the MoWiLife university partners KTH Stockholm and University of Aberdeen.

The Aberdeen HVDC research team, led by Dragan Jovcic and Xin Yuan. will be responsible for developing and validating a functional SiC MOSFET hybrid high voltage DC circuit breaker, which builds on previous research projects at Aberdeen related to DC circuit breakers and DC transmission grid development.

Jovcic said: "DC (direct current) electrical systems have not been much utilised since AC (alternating current) systems have been preferred with traditional overland power transmission and conventional electricity generation.

"However, AC power can only be transmitted over relatively short distances with subsea cables, and as we look increasingly to offshore wind or tidal technology to meet growing demand, solutions are needed to create high-voltage direct current (HVDC) connections and to eventually develop an HVDC grid.

"We will use desktop research and also develop 5 kV DC CB demonstrator based on SiC MOSFETs in our HVDC laboratory for experimental testing."

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- ☑ Ohmic contacts
- ☑ Thick metal stack

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Nexperia: Expanding GaN and SiC operations

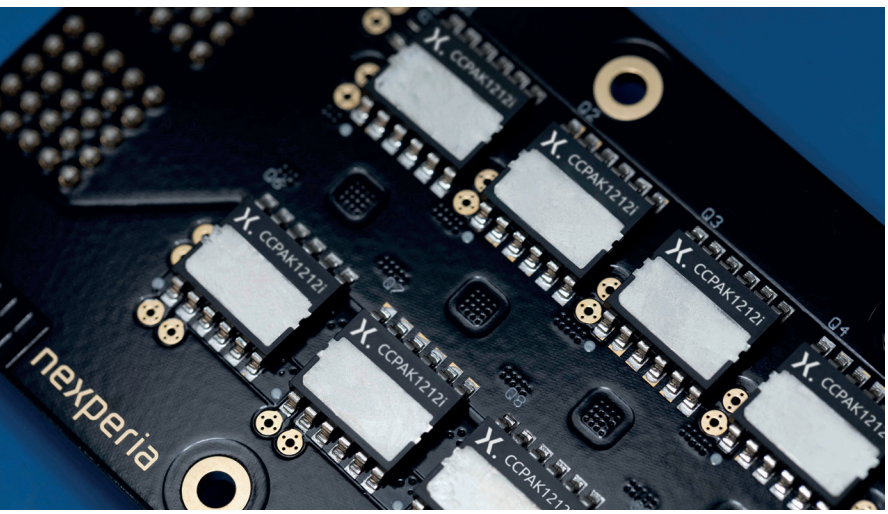
Re-fitting its Hamburg fab lays the foundations for Nexperia to hike its production of GaN and SiC transistors and diodes on 200 mm lines

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

INVESTING PHENOMENAL SUMS in infrastructure that enables the production of SiC and GaN devices is the new norm. In this regard the likes of Infineon, Wolfspeed and Innoscience are making the biggest splashes, by building fabs of breath-taking proportions that are propelling their capacity for high-volume production of wide bandgap power devices.

But as well as constructing new fabs, chipmakers are spending a lot of money on repurposing the space within them for the manufacture of SiC and GaN diodes and transistors. And in this regard, Nexperia is not holding back – it's investing $200 million in new tools and equipment to strengthen the development and production of its wide bandgap portfolio at its fab in Hamburg, Germany.

Nexperia has a tremendous pedigree in electronics, with a history going back 100 years, and second-generation parent companies that include the household name Philips. Production of vacuum tubes in Hamburg provided the first source of revenue in the 1920s, and in the decades that followed efforts extended to the research, development and production of semiconductor devices. Further milestones came in the 1980s and 1990s, including the first MOSFET and the first 150 mm line, respectively. And in this century, two of the biggest moves have been carving out NXP from Philips in 2006, and in 2017, spinning out NXP's standard product division under the name Nexperia.



➤ Nexperia's proprietary CCPAK packages

Today Nexperia is renowned as a major supplier of silicon power devices to automotive markets – this accounts for around half of its annual production of 100 billion discrete parts. However, over the last few years the power electronics producer has broadened its portfolio with the introduction of SiC and GaN devices.

Since 2019, GaN FETs have been part of this chipmakers' line-up. SiC products came in 2023, and now include SiC diodes and SiC MOSFETs, the latter in collaboration with Mitsubishi Electric.

An additional advance came this June, with the introduction of the production lines for high-voltage GaN D-Mode transistors and SiC diodes at the Hamburg site. And according to Nexperia, the next milestone will be modern and cost-efficient 200 mm production lines for SiC MOSFETs and GaN HEMTs.

These new lines will be established over the next two-to-three years at the Hamburg facility that is undergoing substantial change, as all activities unrelated to either lab or fab are relocated to another office in the city. It's a move that's enabling an increase in the capacity of the silicon side of the business, as well as the expansion of SiC and GaN capability.

Nexperia's Senior Director Product Management for SiC, Katrin Feurle, told *Compound Semiconductor* that most of the $200 million investment will be spent on new equipment and a remodelling of the fab to fit to the new machinery. Money is also allocated to increase the automation of existing infrastructure.

To scale epitaxial capabilities, Nexperia has placed orders with Aixtron. This German maker of MOCVD tools is a trusted partner that fulfils Nexperia's needs, according to Carlos Castro, Vice President and General Manager for GaN.

As well as purchasing a range of processing tools to turn epiwafers into devices, Nexperia is making substantial investments in metrology.

Castro claims that Nexperia has a strong reputation for really high standards in production and performance, adding: “Metrology is key, because it gives you a very precise characterisation and control of materials, structures, and the process.” In turn, this ensures performance, reliability, quality, and a competitive cost.

In addition to the equipment, Nexperia has recruited accompanying personal. “We have some people already on board there, experts in metrology,” says Castro.

This increase in headcount is part of a pattern of long-term growth in staff at the Hamburg site. In 2017 the facility had 950 employees, a figure that now stands at 1,600, with more than 50 added in the last three years for roles solely associated with wide bandgap devices.

Growth in GaN...

Since launching its first wide bandgap power device in 2019, the GaN FET, Nexperia has made much progress with this class of transistor. Each new generation features a 20 percent cut in specific on-resistance.

One of the strengths of Nexperia is that it supplies both E-mode and D-mode devices.

“We are the only supplier giving the option to customers to go for D-mode technology, which we believe is more suitable for high-voltage and high-power applications, as well for E-Mode devices, which are very successful right now in the market for low-voltage or low-power applications, like, for example, fast chargers for mobile phones or notebooks,” says Castro.

Another attribute of Nexperia’s GaN portfolio is that it draws on the company’s 20 years of expertise in copper clip technology. As well as ensuring a superior thermal performance, this packaging technology leads to better electrical performance, with a trimming of parasitics and stray inductance resulting in an increase in reliability. And that’s not all – the copper clip technology enables a much more compact design that ensures a higher efficiency, as well as the opportunity to turn to higher frequencies, a strength well suited to high-power applications, such as power supplies and electric vehicles.

While GaN power devices have much appeal, they are currently attracting bad press for patent battles fought between Innoscience and EPC and Infineon.

Castro is not expecting Nexperia to be on the wrong side of such skirmishes, since it has its own IP. Back in 2017 and 2018 the company worked with a collaborator in the US, an activity that involved some licensing, and since then it has been internally and significantly growing its IP portfolio.

➤ Lithography at Nexperia’s Hamburg Wafer-Fab

... and SiC power portfolios

In the last year or so Nexperia has expanded its SiC portfolio, to include 650 V diodes with a current rating from 6 A to 20 A, in a range of formats that incorporate both surface mount and through-hole configurations. Additional advances are the launch of the first automotive-grade product, announced at this year’s PCIM conference, and first design wins, especially in power supply applications.

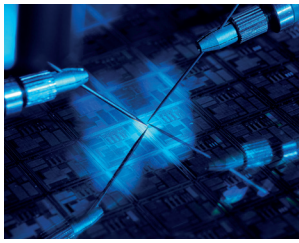
Feurle describes the relationship with Mitsubishi Electric, which is key to the production of discrete SiC MOSFETs, as a strategic collaboration that’s mutually beneficial for both sides. She says: “It’s supporting the mission of Nexperia, but also Mitsubishi, to meet the rapidly growing demand for silicon carbide.” By combining complementary expertise, both partners are reducing requirements for in-house development, and enabling them to go faster to market.

Obstructing Nexperia’s plans has been its forced sale of its fab in Newport, Wales, a move dictated by the UK government. While this has caused serious disruption, it has not impacted Nexperia’s compound semiconductor activities, as there were no plans to reintroduce them at the Newport site.

At the Hamburg fab, conversion of office space to clean rooms is underway, and over the next few years lines will be established for SiC and GaN production, with full production slated for 2027. “Selected key customers, of course, will receive samples in advance, to be able to qualify dedicated target applications,” remarks Feurle.

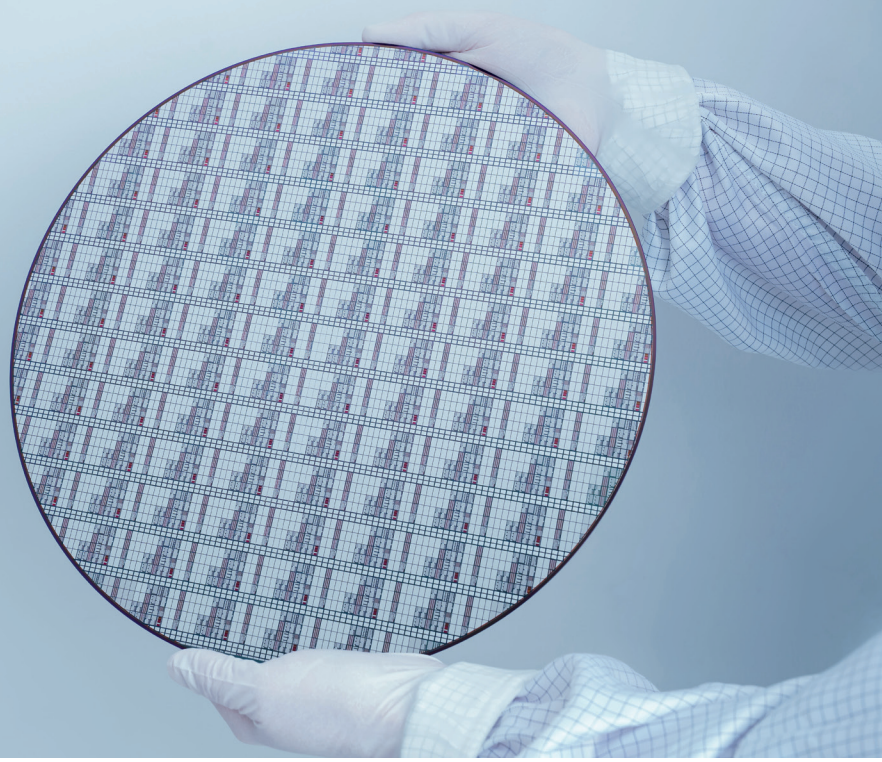
The balance between the production of SiC and GaN devices will be determined by the market. Today SiC dominates, but the gap is expected to narrow, with Castro expecting that by 2028, the SiC market will be around four times that of GaN.

Based on this forecast, and Nexperia’s substantial investment, this chipmaker is sure to be a significant supplier of a broad range of wide bandgap devices by the end of this decade.



➤ Electrical Testing in Nexperia’s R&D Labs

Power GaN: The 300 mm milestone



Migrating the manufacture of GaN power devices to 300 mm lines will boost yield, improve metrology and trim costs

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

➤ It has taken Infineon just 18 months to develop its 300 mm process, building on its 200 mm GaN-on-silicon technology.

A COMMON METRIC for measuring performance of any device is the bang per buck.

When it comes to GaN, there are many ways to measure that 'bang'. They include the on-resistance, the breakdown voltage, and the mobility of the two-dimensional electron gas.

But what about the 'buck'? That's a little harder to fathom, as chipmakers rarely reveal their yield, or the cost of producing their devices. But there are occasions when they will champion their efforts to trim their manufacturing costs, such as a move to larger wafers.

Claiming significant success on this front is the well-known European producer of power electronics, Infineon. It grabbed the headlines this autumn, when announcing the fabrication of the first GaN power devices on 300 mm wafers.

With manufacturers of GaN-on-silicon HEMTs currently carrying out production on substrates with a diameter of 200 mm, and sometimes less than that, Infineon's milestone is more than doubling the number of devices produced per wafer.

Note, though, that this gain is not the only one that will help to trim the cost of production. According to Johannes Schoiswohl, Infineon's Business Line Head for GaN, migration to larger wafers will also lead to improvements to the manufacturing process, such as a higher yield and access to superior metrology. Engineers at Infineon enjoyed these when progressing from 150 mm to 200 mm wafers, and they are seeing them again in the move to the 300 mm platform.

"We can get really great results – better than expected – because the 300-millimetre tools, from a performance perspective, from a monitoring perspective and a process control perspective, are better than the 8-inch tools," remarks Schoiswohl.

Due to these benefits, Infineon took just 18 months to develop its 300 mm process, building on its 200 mm GaN-on-silicon technology.

According to the company's projections, its GaN power devices could reach cost parity with their silicon equivalents. Helping to reach this goal will be: economies-of-scale; improvements in the technology itself, particularly the epitaxial stack; and the lower on-resistance of GaN, enabling smaller die to deliver the same performance as comparable products made from silicon.

To develop its trailblazing technology, Infineon's engineers have had to grapple with the lattice mismatch between GaN and silicon, as well as differences in thermal expansion coefficients.

"The bigger the wafer diameter, the harder it gets," admits Schoiswohl. "The wafers start to bow because of the lattice mismatch, and at a certain epi-thickness, they simply crack."

By developing and refining its epitaxial technology, Infineon releases strain during the growth.

Schoiswohl says that the particular epitaxial processes employed by providers of GaN power transistors are a key differentiator. According to him, the quality of the epitaxy determines the degree of early lifetime failures and often defines the device's failure mechanisms.

With Infineon's GaN power devices, a thicker epitaxial stack is needed to realise a higher blocking voltage. According to Schoiswohl, the company's engineers can see a path to progressing from 100 V to 650 V devices, but going beyond that will be more challenging. He says that one solution could be a switch to thicker wafers: "These are all details we have to figure out."

Infineon already offers wide bandgap power devices operating at a kilovolt or more, based on SiC. But that will not stop the company investigating what might be possible with GaN, which offers the tantalising possibility of a better performance at a lower cost.

Following the production of GaN-on-silicon epiwafers on dedicated MOCVD tools, processing of this material is undertaken on standard silicon lines – that's a significant merit from a CapEx perspective.

Infineon's pioneering work has been carried out at its facility in Villach, with attention paid to ensuring that processing of its GaN-on-silicon wafer in a 300 mm line did not introduce any contamination. As volume ramps, there will come a time when a 300 mm line can be devoted solely to the production of GaN devices. Infineon also has 300 mm equipment in Dresden that could be used for the production of GaN devices, and opportunities to potentially outsource due to established foundries.

At the upcoming trade show Electronica, to be held in Munich from 12-15 November, Infineon will release its next-generation G5 HV technology. The plan is to take this process and apply it to 300 mm wafers, with engineering samples reaching customers by the end of next year, and production ramping in 2026.
Today the biggest market for GaN power devices is consumer chargers. "We can see that this is now reaching points where some customers say 100 percent of their volume will move there," remarks Schoiswohl.

Additional opportunities are found in power supplies for AI, motor controls and inverters, as well as the automotive industry. While all these markets are important, Schoiswohl sees the automotive sector as an important one, due to the opportunity for higher volumes, with GaN a compelling candidate for the on-board charger.

Success will hinge on the bang-per-buck, helped by a move to 300 mm GaN-on-silicon.

➤ A technical engineer in the cleanroom at Infineon Technologies in Villach, Austria, holds a 300 mm GaN-on-silicon wafer.

Putting India on the global GaN stage

University spin-out Agnit has just secured funding to grow its GaN portfolio, a combination of epiwafers and power and RF devices

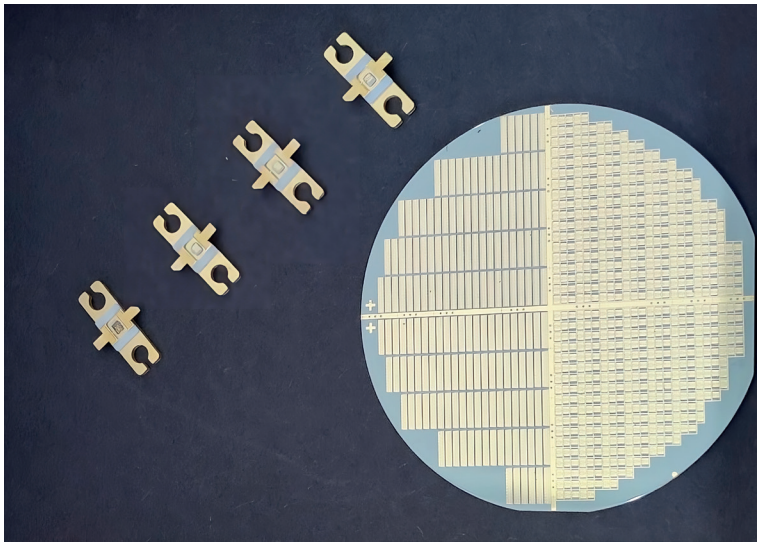
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THERE ARE a number of ways to measure the growth of an industry.

For GaN electronics, which serves both the power and RF sectors, evidence of its rapid rise is seen in its double-digit rises in revenue, which will swell this market to several billion dollars by the end of this decade. But that's not the only way to track success. The growth of GaN is also seen in the geographical expansion of its chipmakers. As well as big the names in the US, Europe, Japan and China – such as Navitas, EPC, Transphorm, Infineon, Toshiba and Innoscience – smaller players are cropping up all over the world, including in unfamiliar locations, such as India.

Breaking new ground on this sub-continent is Agnit, a spin-out of the Indian Institute of Science that has just raised another US $3.5 million to advance its GaN portfolio, a mix of epiwafers and power and RF devices.

Company co-founder and CEO, Hareesh Chandrasekar cannot lay claim to Agnit being the sole trailblazer for compound semiconductor manufacturing in India, because it's just possible that there is another maker of such devices hiding from view. But he is adamant that Agnit is the first to use indigenous technology, rather than getting it from somewhere else.



Introducing semiconductor manufacturing in India could be crucial to the growth of this nation's economy, says Chandrasekar. "If India is going to be a 5, 7, $10 trillion economy in the next decade or so, there's no way this is happening without us having a presence in the electronics manufacturing ecosystem."

While there are a number of options for gaining a foothold in the semiconductor industry, some are more attractive than others, with cutting-edge CMOS having a formidable financial barrier to entry.

"We felt that gallium nitride was a nice sweet spot," says Chandrasekar, who argues that while this technology is not as complex as state-of-the-art CMOS, and doesn't demand fabs with price tags of several billion dollars, it's up and coming, and there is a local pull for products.

An academic heritage

Founded in late 2019, but initially impeded by the global pandemic that stalled the start of this company's operations until January 2021, Agnit receives tremendous support from the Indian Institute of Science, in terms of both facilities and expertise.

This institute is a great incubator for Agnit, having constructed a pilot production line for GaN that has a peak capacity of about ten 6-inch wafers per day. Supporting this is a very good characterisation suite.

Another asset of this institute is its extensive development of GaN technology, creating a strong IP base that draws on many, many years of research.

Imparting expertise from the Institute to Agnit is seamless, as four of the seven founders, all still involved, are academics with complementary capabilities related to the fabrication, operation and reliability of GaN devices. The other three co-founders, now the core management team, have PhDs in the field of GaN, but bring a different skillset, partly thanks to time spent working in the semiconductor industry. Strengthening this team are a growing number of employees, now totalling 16.

In terms of the commercialisation of its GaN device portfolio, Agnit has initially focused on the RF, before more recently expanding into the power domain.

Agnit's RF devices are marketed to the telecom and the strategic sector. Products from rival suppliers are already being deployed in base stations, encouraging the Bangalore start-up to pursue more niche applications associated with 5G networks. "It could be things like private networks," says Chandrasekar.

For the power market, which Chandrasekar describes as "pretty hot now", there are many players with unique business models. To carve out a space in this sector, he and his colleagues are trying to address a particular set of problems associated with the unique, local market. Prototyping is underway.

To support its device development, Agnit is packaging its die in-house. But this will change when it moves into production, with this final manufacturing step outsourced, using the strong local ecosystem.

"We are also exploring global partnerships to see how we can actually leverage the global packaging capacity for the GaN chips that we make," says Chandrasekar.

The third string to Agnit's bow is its supply of GaN epiwafers to chipmakers.

"We had already supplied to academia," says Chandrasekar, adding that the new additional capacity is enabling Agnit to expand its horizons and build foundry relationships for the global supply of GaN-based power and RF epiwafers.

One of the issues hampering the GaN industry for many years is that epi is a "black box," according to Chandrasekar. "When you buy a batch of wafers, you never know if they're the right ones to begin with for your process or not. That has always been a big stumbling block."

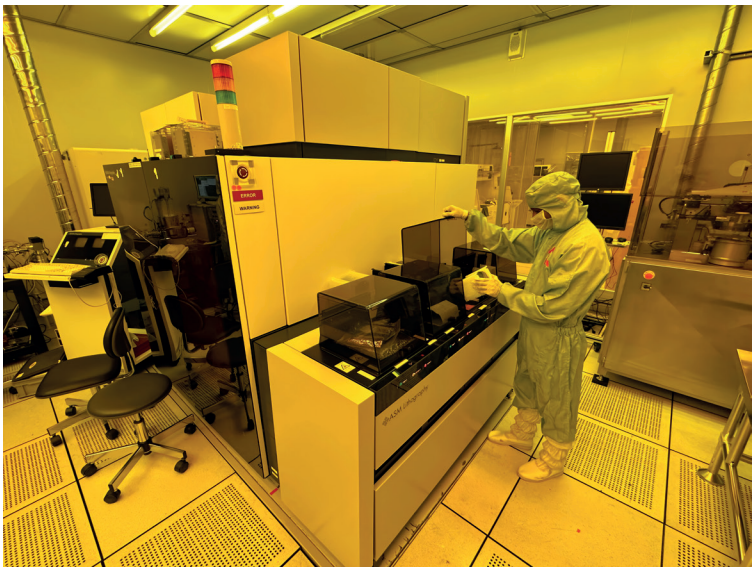
Agnit is addressing this concern by offering the capability to adjust the epitaxial process based on internal device feedback. This helps customers target particular performance specifications.

Patents and IP

Agnit has a strong IP portfolio, supported by technology developed from the Indian Institute of Science, which it licences exclusively. The start-up has more than 20 patents, of which 15 or so are global patents.

Like the leaders of many foundries, those calling the shots at Agnit have thought very carefully about what IP requires patenting, and what is best left undisclosed. Such decisions are guided by whether patents have the potential to expose and demonstrate infringement. "If you can't do that, then it makes very little sense to patent your IP," argues Chandrasekar.

Highlighting the need for defendable IP are the patent battles being fought between Innoscience and EPC and Infineon. While such skirmishes may alarm some chipmakers within the GaN industry, they are not a major concern to those leading Agnit. "Everything that we commercialise has our own patents as a backing, or our trade secrets and know-how as a backing," says Chandrasekar. "We are quite careful about that."



➤ Agnit produces GaN power and RF devices at the incubator at the Indian Institute of Science.

Investing in its future

The US$3.5 million raised this Autumn came from a seed round led by 3one4 Capital and Zephyr Peacock.

This investment will help to increase production yields for 4-inch GaN-on-SiC epiwafers for RF devices, and for 6-inch GaN-on-silicon wafers for the power sector.

In addition, the funding will be used improve device reliability, an issue that Agnit takes very seriously. "This will help our devices be qualified for various reliability standards that we are targeting based on the markets that we choose to go after," remarks Chandrasekar.

As well as advancing yield and reliability, the seed funding will support prototype development – in particular, power devices for the domestic market, as well as RF devices for the telecom sector.

Two big goals for the next 12 months are to get RF products in the market, in both the telecom and strategic sectors, and to grow the epiwafer supply business, supporting these customers with device data.

"In 24 months, we'll also have the first alpha samples available on the power devices that we're working on, which will be sampled to customers for integration into their systems," adds Chandrasekar.

The CEO expects the majority of its sales over the next few years to come from domestic markets, but 30 percent will be overseas. If such success follows, that will surely help to grow the role of India on the global GaN stage.

Clas-SiC expands technology in its stride

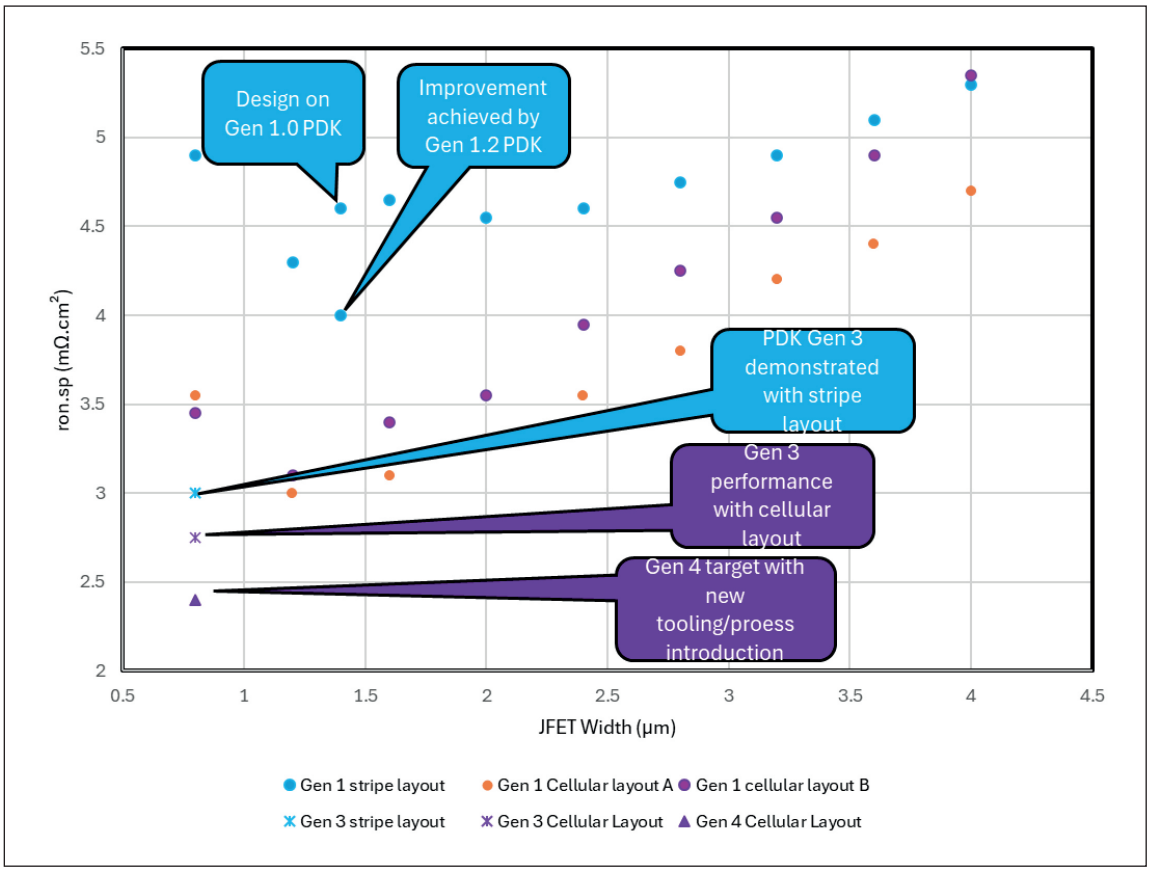
Not content with opening the world's first SiC foundry that partners with power device designers, Clas-SiC Wafer Fab is evolving and adapting to grow its success

BY JEN WALLS AND DAVID CLARK FROM CLAS-SIC

FOUNDED IN 2017, Clas-SiC Wafer Fab is the world's first open foundry dedicated to SiC. At our facility, located in Lochgelly on the outskirts of Scotland's capital city, Edinburgh, we have adopted a pure-play approach, which means that we'll never be in competition with our device customers. Instead, they draw on our standard process flows and flexible Process Design Kits (PDKs) to simply and quickly design highly customised SiC devices. By using PDK models to minimise non-recurring engineering and trim the cost and cycle time, our customers can work with us to produce a range of competitively priced SiC transistors and diodes operating at 650 V, 1.2 kV, 1.7 kV and 3.3 kV on both conventional and engineered SiC substrates.

Our mission is to provide a low barrier to entry for all of our customers seeking to develop new products. We support them at every step, from proof-of-concept to market seeding, low-volume production, right through to high-volume production. This sets us apart, as we are the only foundry in the SiC industry that takes customers through all stages of product lifecycle. Most of our business comes from the manufacture of enhancement-mode MOSFETs, but we also produce depletion mode MOSFETs and two forms of diode – the merged *p-i-n* Schottky diode, and the junction barrier Schottky diode. We use PDKs to support a high level of integration, during successful customer designs for highly customised unique devices, even to the extent of including integrated sensors as part of the device design. Our customers can have confidence in these PDKs – as well as having reliability proven on our reference devices, they have been used by customers that conduct reliability trials on their own specific devices, with efforts on this front demonstrating that our foundry produces devices that satisfy AEC-Q101 using JEDEC 22 conditions.

Since releasing our initial generation of PDKs in 2022, we have been working on developing Generation 3 PDKs. These successors deliver significant improvements in the performance of 1.2 kV planar MOSFETs, realised by shrinking transistor dimensions (see Figure 1). With favourable wafer-level results, Generation 3 devices are currently undergoing reliability trials, ahead of a scheduled release at the end of 2024. In parallel we are qualifying devices fabricated on engineered substrates to add to our PDK offerings.



➤ Figure 1. Reducing the width of the JFET is leading to a reduction in specific on-resistance.

We are now starting to turn our focus to Generation 4 MOSFETs. They feature a shrinking of the transistor interconnect, a refinement that enables a further reduction in cell pitch and thus a corresponding reduction in specific on-resistance. To produce these transistors, we are investing in upgrading and expanding our tooling.

Right now, we are on the cusp of this exciting new phase, with the new tooling being identified, procured and installed ahead of interconnect technology development. Our timescales are governed by tool delivery times, and we are forecasting the introduction of our Generation 4 PDK in 2026. We plan to begin our Generation 3 and 4 technologies on 1.2 kV MOSFETs, before subsequently extending this technology to 1.7 kV and then 3.3 kV variants.

While we are currently focusing on planar MOSFET technology, this has not stopped us from conducting trench processing work for specific customer projects. As part of this effort, we are investing in process tooling to expand our trench processing capabilities, and support the possibility of developing our own trench MOSFET PDKs in the future.

We have drawn on our standard process modules that underpin our PDKs to fabricate novel trench and planar SiC MOSFETs, using heavily customised process flows. In addition, we have adopted this approach to produce *p-n* diodes, JFETs, and other customised devices, including both lateral and vertical device architectures.

As well as producing a wide range of SiC devices, we are active in UK innovation-based funding calls. They include APC (Advanced Propulsion Centre), DER (Driving the Electric Revolution), as well as the EU Horizon scheme. Projects in progress include an automotive BEV/FCEV project, a Solid-State Transformer project, and a project for Condition & Health Monitoring in Power Electronics. To keep close to technology advances, we are maintaining close academic links with research teams in the UK, at the University of Glasgow and Warwick, as well as overseas, such as at Purdue University.

Our innovation surrounding process development extends beyond ‘normal’ process advancements. We are closely involved in wafer fabrication tool development, partnering with major industrial players that advance semiconductor equipment design. This extends through to our work with substrate and epitaxy providers, to help them validate their materials for the market. Through this work we are advancing the world of SiC device processing.

As well as technology development, which is the R&D part of our business and where we tend to begin our engagement with customers, we have another two business streams. They are Low-Rate Production (LRP), and Licensing, Royalty and Consulting (LR&C) (see Figure 2 for a summary of our business streams).

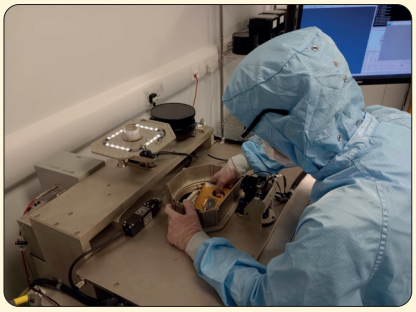
Views from Clas-SiC apprentices

Clas-SiC has a strong, well-established apprenticeship programme. Below, told in their own words, are the stories of three of those involved: Dani Johnston, a Modern Apprentice Manufacturing Equipment engineer (top left); and Duncan Colston (bottom left) and Kieran Healy (bottom right), both Graduate Apprentice engineers.

I AM IN MY final year as a Modern Apprentice at Clas-SiC Wafer Fab. My journey with this unique company started in 2020. I began as an operator, before I was given the opportunity to progress my career as an apprentice equipment engineer.

Starting off as an operator allowed me to gain a lot of understanding and knowledge of not only each tools' capabilities, but also an insight into the various processes applied to semiconductors. This has benefited my ability to fulfil my role within the apprenticeship programme.

While progressing towards my HNC qualification I have gained a wide variety of experience by working alongside very knowledgeable process, equipment and facility engineers, who have guided and mentored me. My responsibilities as a equipment engineer include carrying out tasks such as preventative maintenance, fault diagnosis, and testing mechanical and electrical equipment.



I AM REALLY enjoying the second year of my apprenticeship experience with Clas-SiC. It is a challenging but rewarding environment, where I have been surrounded by knowledgeable people to help me get the most out of my apprenticeship, both on the work side and with university.

At university I am working through my degree, which is a BEng design and manufacture (electrical) at Heriot Watt University in Edinburgh. I attend once a week and complete work-based learning tasks, and write reports on those tasks to consolidate my knowledge and complete the modules, along with gaining hands-on skills through working in the cleanroom.

I have gained a lot of relevant knowledge in the past year working in the test department, and spending some time working in the photolithography department. There has always been someone to help me when I'm stuck or confused. I started with learning the basics of operation, for example, how to run the tools and process batches. Now I am being introduced to more of the process aspects in semiconductors. I've also enjoyed the exposure I've had so far with the layout of the devices with the software we use, as I had an interest in CAD drawing at high school.

THE GRADUATE apprenticeship programme inside Clas-SiC has given me the opportunity to gain valuable industry skills whilst still having the possibility to be recognised with an educational degree (BEng – Engineering design and manufacture; electronic) that will be important for my future. Being local to me, Clas-SiC provides an easy stepping stone into the semiconductor industry, in which I have been able to gain an appreciation for the industry and its significance in the world.

My experience at Clas-SiC has been positive, and I am now in the third year of my studies. I have been able to work alongside experienced engineers who are happy to share their knowledge with me. This has accelerated my development in both semiconductor knowledge and process engineering skills, learning different ways to carry out tasks such as data collection/presenting.

My time has been spent on a mix of day-to-day activities (monitoring SPCs, keeping batches moving etc.) and being involved in larger projects (process optimisation, development of new products), with a larger focus on the etching processes, dry and wet.

I have had support, where needed, from the Clas-SiC team. This has helped me in my university learning, where I have been able to lean on expertise to aid my understanding of topics, as well as with aspects such as time management. During my apprenticeship I have been given various opportunities to represent the company, attending schools to talk about Clas-SiC and the opportunities available, as well as events such as awards evenings.

I am looking forward to continuing my learning with Clas-SiC on their journey in SiC and hoping I can be a part of their growth.

Our LR&C business stream enables customers with ambitious expansion plans to ramp up to high-volume/low-cost manufacture. This initiative provides support for independent foundries in low-cost manufacturing locations, such as those in Asia, to set up replicas of Clas-SiC processes. Our capacity in Scotland is limited to low-rate production, so this model allows us to access much higher volumes without Capex investment, keeping prices down for our customers.

For those that work with us under LR&C contracts, the norm is that a defined portion of their capacity is reserved for Clas-SiC customers. When our customers outgrow the capacity of Clas-SiC foundry, we outsource production to one of these associated but independent fabs. Throughout this evolution our customers maintains their partnership with us, utilising our advancing PDKs for their next-generation devices as they start another R&D cycle.

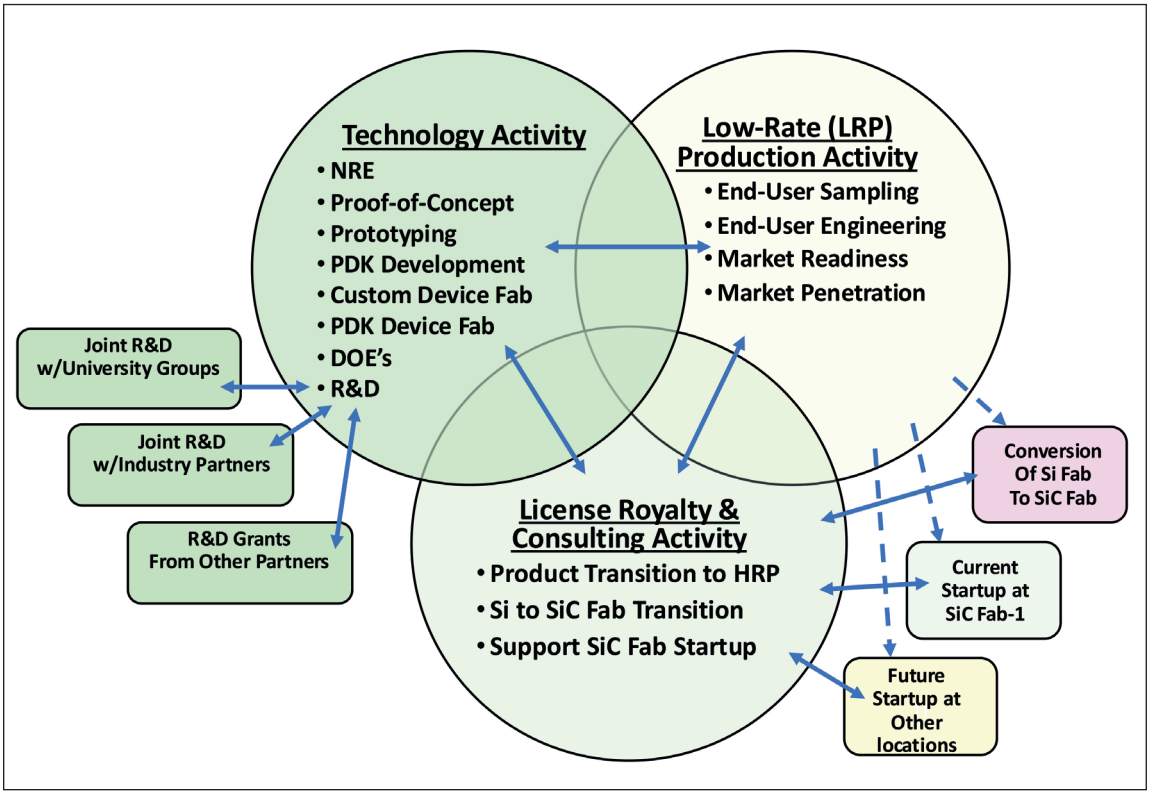
The first wafer fab utilising this model is now well advanced. Supported by our team, this fab has been constructed, facilities and tooling are installed, processes have been set up, and production will soon begin. We also have a number of other potential LR&C projects at the stage of advanced discussion.

Key to our success is our continual re-investment, not only in capital equipment, but also in our people. Our staff, with their advanced skill sets and out-of-the-box thinking, are our greatest asset. We now have more than 320 man-years of experience in SiC device processing, putting us in an unrivalled position for taking on the challenges of our customers. We pride ourselves in the continual development of our workforce, from our production operators through to our senior management team.

Training has been crucial to our advancing over the last year, as we have undergone exceptional growth and transitioned to a 24/7 operation for device production. More than 80 percent of our direct labour has received advanced training to fully utilise and build their skillsets, a move that has led to a more flexible and satisfied workforce. Our investment in new entrants, in the form of modern apprentices and graduate apprentices, is also well advanced. As well as ensuring that we keep the talent pipeline in a healthy state, this introduction of 'young blood' maintains a well-balanced age demographic within our workforce.

Despite the tough investment environment throughout the world, we have managed to secure equity investment from Archean Chemical Industries Ltd. We are excited to have them on our team and looking forward to the exciting times ahead. This funding will help to grow our business, supporting the launch of Gen 4.0 technology in 2026, as well as strengthening our Board of Directors.

We have been privileged to have both the financial support and the wisdom of knowledgeable investors since our foundation. One of our founding members, Carl Johnson, launched a CdTe crystal growth company just over fifty years ago that has blossomed into Coherent. By drawing on this expertise, we are well supported in our efforts that will see us take Clas-SiC to the next level and beyond.



➤ Figure 2.The business stratergy of Clas-SiC Wafer Fab

Enhancing β-Ga_2O_3 with hetero-integration

Thanks to the introduction of a far higher thermal conductivity and *p*-type doping, better devices are realised when pairing β-Ga_2O_3 with SiC or diamond

BY ARPIT NANDI, ADITYA BHAT, INDRANEEL SANYAL, SAI CHARAN VANJARI, JAMES POMEROY, MATTHEW SMITH AND MARTIN KUBALL FROM THE UNIVERSITY OF BRISTOL

CLIMATE CHANGE and unpredictible extreme weather are impacting human life more frequently than ever. In just the last few months many in central Europe have suffered from such events, with severe flooding occuring at the same time that more than 5,000 firefighters were fighting wildfires in northern Portugal. These events underscore the urgent need to decarbonise the energy sector, an endeavour where power electronics can play a crucial role.

Within the power electronics portfolio, different materials are seeing deployment at different voltages. For low-to-medium-voltage applications, it is the silicon-based devices that dominate, due to their cost-effective manufacturing processes. But in the mid-to-higher voltage range, GaN and SiC have gained traction, with GaN-on-silicon benefiting from silicon-style manufacturing. And there is also Ga_2O_3 to consider – it has emerged as a highly promising material for power electronic devices, due to its large bandgap (4.8 eV), its tolerance for high electric fields (8 MV cm^{-1}), and the promise of cheaper production than the more established SiC.

Researchers working with this ultra-wide bandgap oxide have enjoyed tremendous success over the last decade or so, with interest ignited by the first report of a Schottky barrier diode in 2013. Spurred on by this triumph, alongside the ease of *n*-type doping and the availability of melt-grown substrates, these pioneers are now gaining further encouragement as 6-inch substrates appear on the horizon, as well as a push from multiple material vendors across the globe. There are now producers of Ga_2O_3 substrates in Japan, the US, Germany, South Korea and China. Based on all this promise, commercialisation of Ga_2O_3 looks inevitable for high-voltage applications.

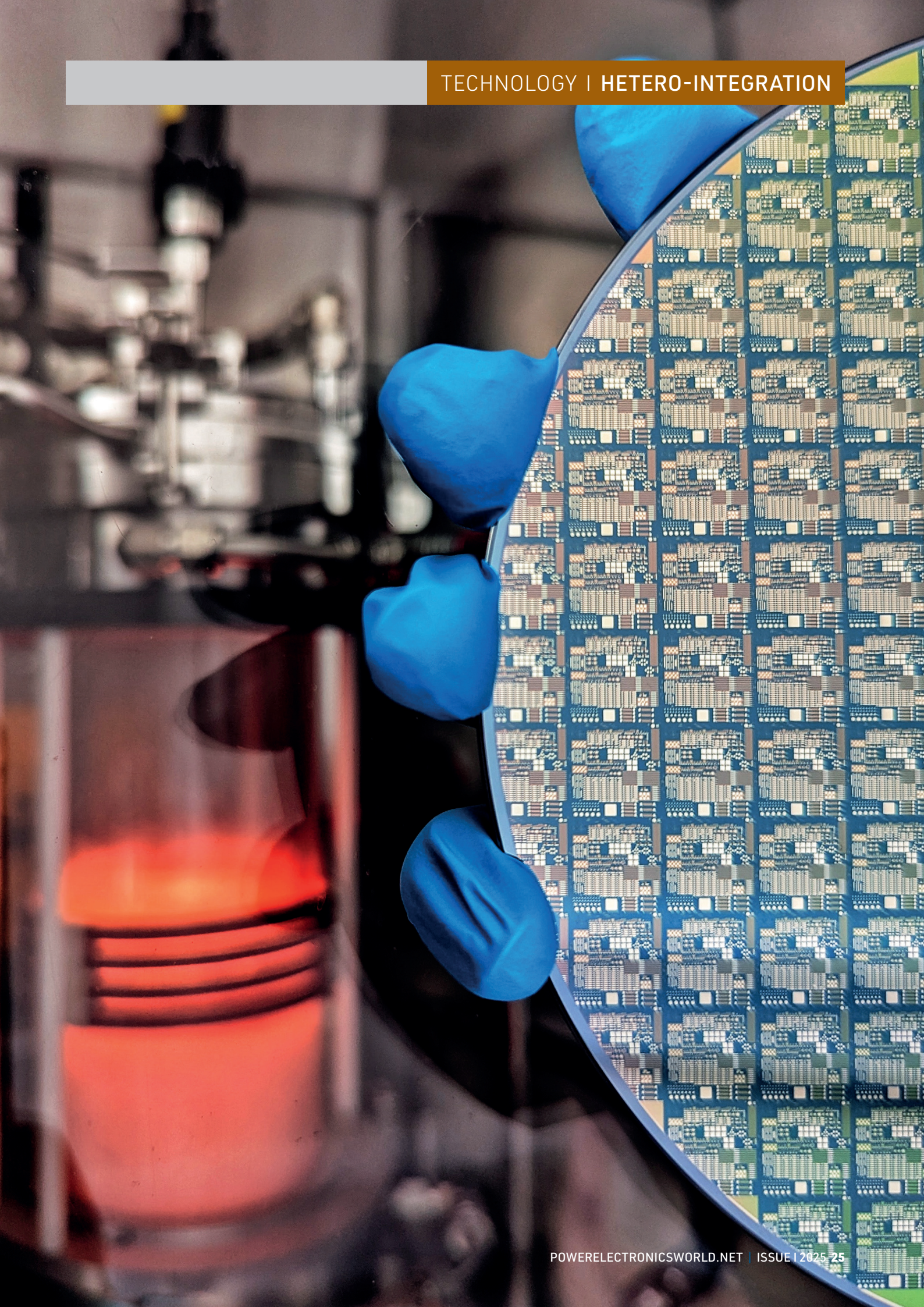
Those developing Ga_2O_3 material and devices include the UK government-funded Innovation and Knowledge Centre REWIRE, led by our team at the University of Bristol. While we acknowledge that today's Ga_2O_3 devices exhibit excellent performance, with breakdown voltages that can exceed 8 kV, there are drawbacks that we are starting to address. Significant concerns preventing this material from harnessing its full potential include an on-state currents that's relatively low, and a device reliability that still needs to be established and proven.

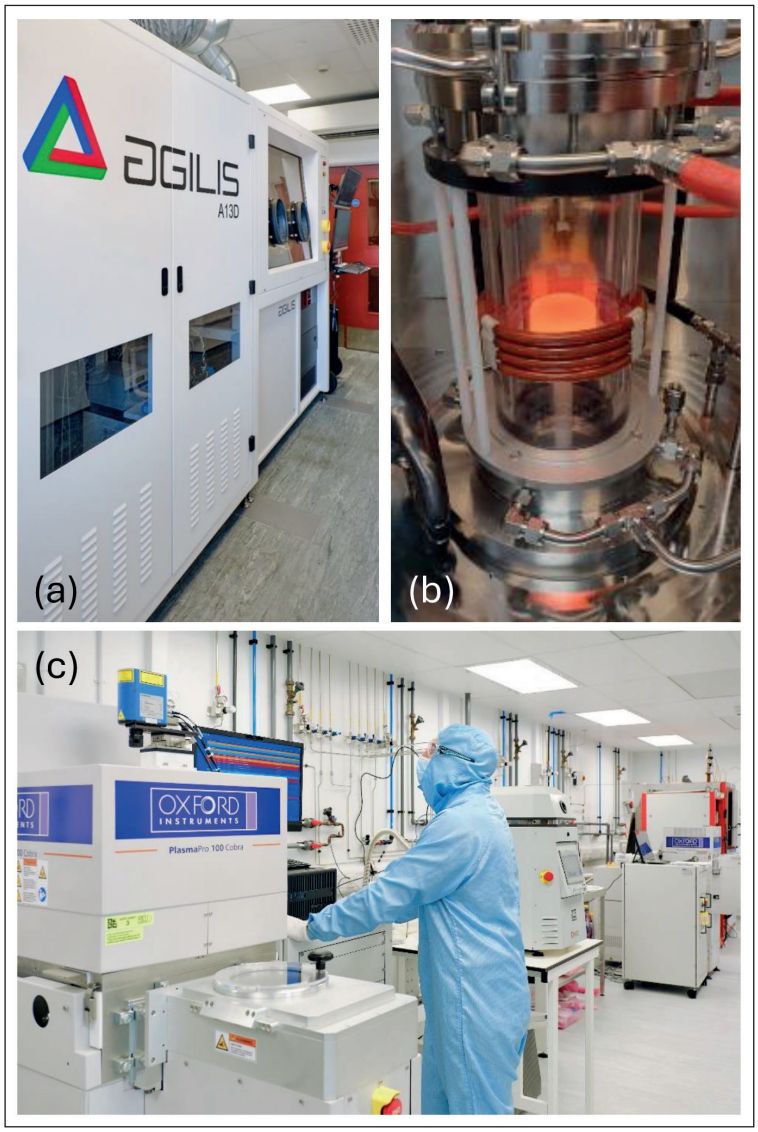
Behind these limitations are: a lack of useable *p*-type doping for Ga_2O_3, primarily due to the flatness of the valence bands; and a low thermal conductivity. But there are ways to mitigate this through the heterogeneous integration of Ga_2O_3 with SiC and diamond – they are materials with high thermal conductivity and *p*-type doping. Combining Ga_2O_3 with other materials is an increasingly popular approach to tackling the critical technological bottlenecks. For example, Ga_2O_3 MOSFETs attached to diamond through mechanical exfoliation and bonding are showing good promise, as are devices featuring composite wafer fabrication with SiC. Still, concerns remain related to scalability, impairing manufacturing. Note that in addition to Ga_2O_3 and its alloys, REWIRE is exploring, amongst others, SiC, AlGaN, diamond and BN device technologies, in a team with partners at Warwick University and Cambridge University.

Powered by state-of-the-art growth and clean room facilities at the University of Bristol, we are approaching heterogeneous integration of Ga_2O_3 in various ways. Our goals include: optimising Ga_2O_3 heteroepitaxy on SiC and diamond substrates, the latter in collaboration with Element Six Technologies and Orbray; and in partnership with Srabanti Chowdhury's Wide Bandgap Lab at Stanford University, exploring thin *p*-type diamond overgrowth on Ga_2O_3.

Pairing Ga_2O_3 with diamond...

Pairing Ga_2O_3 with diamond is very attractive. With a bandgap of 5.4 eV, *p*-type conductivity, a thermal conductivity of up to 2000 W m^{-1} K^{-1}, and a predicted critical electric field strength of 10 MV cm^{-1}





➤ Figure 1. (a) and (b) Ga_2O_3 MOCVD, and (c) clean room facility at the University of Bristol.

– that's even higher than that of Ga_2O_3 – diamond compliments and enhances the effectiveness of Ga_2O_3 when its adequately integrated.

Our initial work on this front has involved the growth of Ga_2O_3 on single-crystalline diamond substrates. For this effort, we faced two underlying challenges: prevention of oxidation of the diamond surface at high temperatures during initial growth stages; and overcoming the challenge of realising good nucleation, which is plagued by the high surface energy differences between Ga_2O_3 and diamond.

To address these concerns, we have pursued a two-step process, beginning with the low-temperature growth of a thin layer of Ga_2O_3 that protects the diamond surface, followed by high-temperature growth of an epitaxial layer. Our detailed analysis of the microstructures and grains produced during this process has revealed two-grain variants aligned to [110] diamond and its perpendicular direction. Due to a peculiar asymmetric hexagonal (-201) face and mirror symmetry, each set has its own four equivalent subvariants (for more details see Nandi *et al.* Crystal Growth & Design **23** 8290 (2023)).

One of the important outcomes of our study is that it has helped us to identify the off-cut directions that are needed to eliminate grain variants and improve the epitaxial structure. Our approach is following in the footsteps of many other prior material systems, given that the use of off-cut substrates has a strong and well-established track record in reducing the multiplicity of grain variants. We have employed Ga_2O_3 growth on off-cut diamond substrates to refine the quality of the epitaxial layers and eliminate one set of sub-grains. By introducing a unique, improvised seeding layer, we have produced better, smoother coalesced surfaces with larger grains and similar sets. With this approach we have grown a variety of layers, including that with a thickness of around 250 nm (see Figure 2 (a)).

Another part of this work has been the growth of an *n*-type doped Ga_2O_3 cap layer on undoped material. This epistructure is a starting point for fabricating quasi-vertical power devices, currently under development. Supporting such efforts is the availability of 2-inch free-standing diamond substrates, with *p*-doping of this material set to follow.

...and SiC

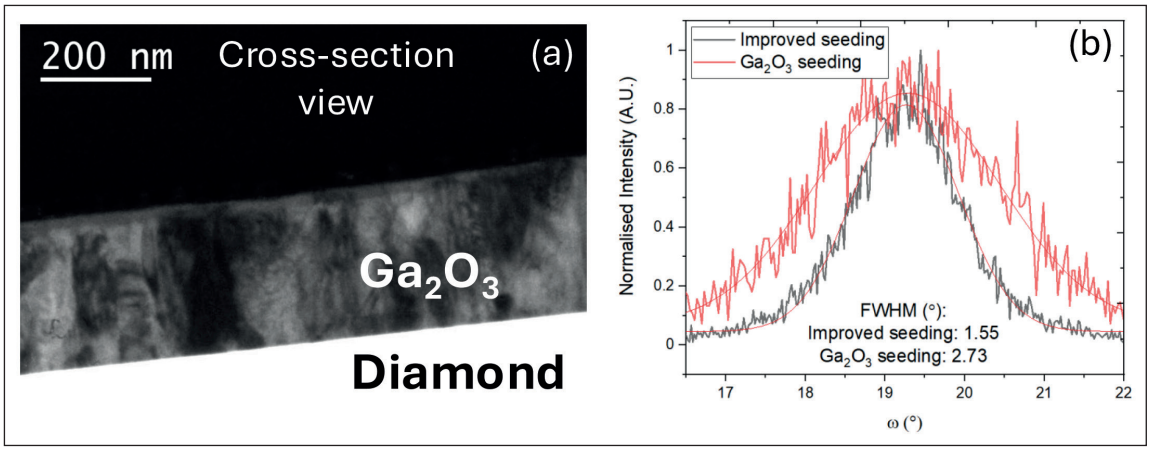
Composite bonded SiC-Ga_2O_3 substrates have also been gathering interest, due to their potential to deliver a significant reduction in the Ga_2O_3 device temperature. However, the weak van-der Waals bonding at the interface between the two materials threatens to impede the mass adoption of such an approach, effectively impacting yield.

One alternative is the heteroepitaxy of Ga_2O_3 on SiC; though similar to growth on both sapphire and diamond, this is a rather complex process with limited thermodynamic understanding. To try and shed new light on this, we have established a detailed thermodynamic picture that encapsulates the growth of Ga_2O_3 on foreign substrates, and assumes a Volmer–Weber growth mode, where the substrate surface energy is lower than the epilayer surface energy.

Our investigations have determined that growth of Ga_2O_3 on SiC is favourable at higher temperatures, a finding that falls in line with the widely adopted approach for growth on sapphire substrates. A preference for higher temperatures on both these foundations is mainly due to the comparable interface energies required for forming Ga_2O_3 islands during nucleation with unit volume.

Heterogeneous device engineering

In addition to materials integration via growth, improved device engineering is critical to alleviating Ga_2O_3 challenges. Diamond promises to play a role, thanks to its capability to combine excellent heat extraction with *p*-type conduction, realised



➤ Figure 2. (a) Cross-sectional TEM image, low magnification plan view of Ga_2O_3 thin film grown on diamond. (b) The rocking curve illustrates grain size increase after incorporating an improvised seeding layer, reflecting a decrease in FWHM.

by boron doping. This conductivity opens the door to advanced device architectures that combine a low conduction loss with a high breakdown – a combination that can break through the typical trade-off between on-resistance and breakdown.

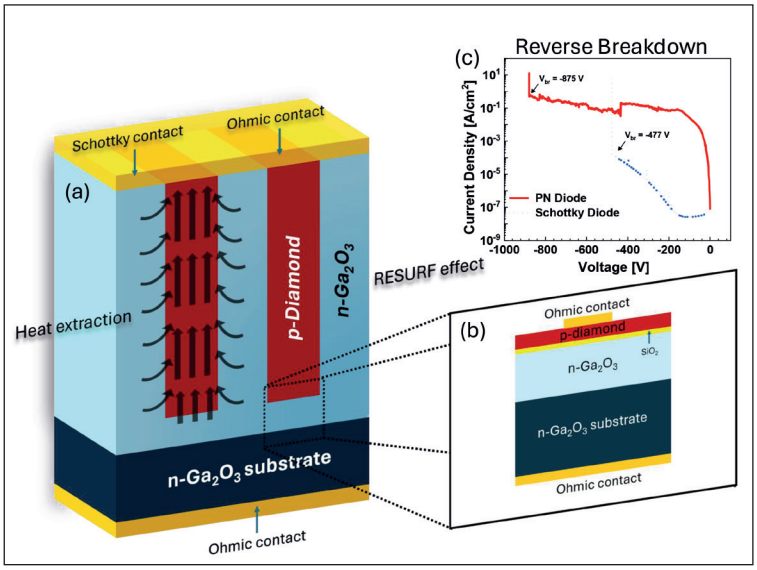
A team from Xidian University have pursued this type of approach, uniting *p*-type NiO with *n*-type Ga_2O_3. Devices with a breakdown voltage of more than 8 kV have followed, an outstanding result. However, the practical potential of these devices may be limited by the low thermal conductivity of both constituent materials, a weakness that ultimately restricts the current-carrying capacity.

Promising to overcome this limitation is the super-heterojunction Schottky diode formed from *n*-type Ga_2O_3 and *p*-type diamond (Figure 3 (a)). Simulations suggest that this device, which we are pursuing, can deliver off-state breakdown voltages of more than 4 kV, and an on-state resistance of just 2-3 mΩ cm^2. The introduction of diamond quashes the peak temperature rise by up to around 60 percent compared with conventional Schottky diodes; and the advanced device structure aids electric field management in Ga_2O_3. We expect this super-heterojunction diode to drastically outperform SiC in medium and high-voltage DC power converter applications where there is a low elevation in case temperature.

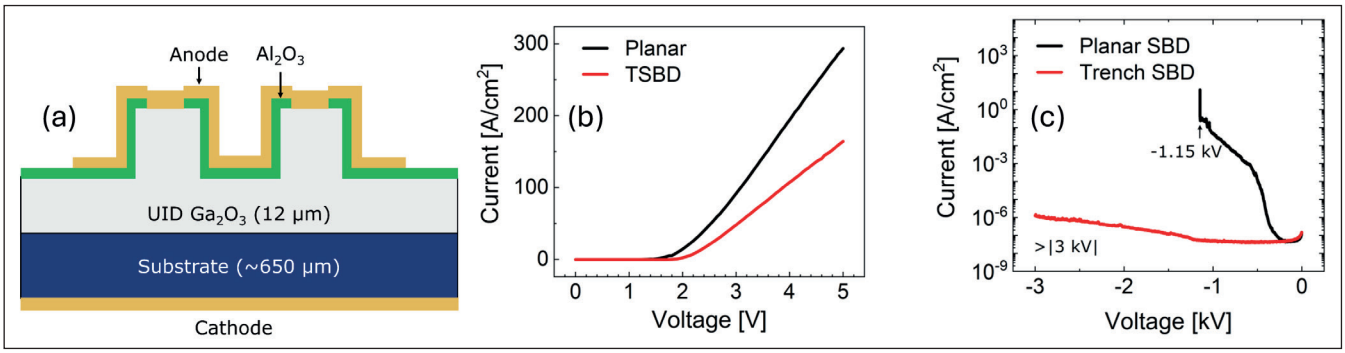
The working principle of the super-heterojunction Schottky diode that pairs *n*-type Ga_2O_3 and *p*-type diamond builds on the prior three-dimensional Ga_2O_3 device structures of trench Schottky barrier diodes. It is well known that despite the high critical electric field strength of Ga_2O_3, devices based on this oxide are yet to deliver a high breakdown, due to catastrophic breakdown that stems from a peak electric field at the metal-Ga_2O_3 interface in planar Schottky diodes. This peak field is behind the early breakdown and unreliable device operation. Trench Schottky barrier diodes offer some promise in this regard, as they have been shown to push the peak electric field away from the interface and reduce the surface electric field (see Figure 4). We are not alone in demonstrating devices that operate on this principle – other groups have also enjoyed success, such as teams from Cornell University and the University of California, Santa Barbara.

By reducing the surface electric field, due to sidewall MOS capacitances, we have trimmed the parasitic leakage current and realised an off-state breakdown of more than 3 kV (see Figure 4 (c)). Previously we reported that fins fabricated along [010] orientation deliver the highest current and the lowest parasitic charge trapping. In sharp contrast, fins with the [100] orientation show poor reliability. Another interesting finding by our team is that according to UV-assisted capacitance measurements, Al_2O_3 dielectrics for MOS capacitors show less trapping, suggesting that they could ensure a more reliable device performance. We are in the process of assessing failure modes and reliability of Ga_2O_3 trench Schottky barrier diodes.

Combining knowledge from device simulation and fabrication, we have taken the first steps towards realising super-heterojunction diodes based on *p*-type diamond and *n*-type Ga_2O_3. These efforts began by optimising and characterising the



➤ Figure 3. (a) 3-D visualization of simulated Ga_2O_3 / diamond superjunction diode, (b) schematic of planar *p-n* diode fabricated and (c) its measured reverse breakdown at −875 V.



➤ Figure 4. (a) Schematic of trench Schottky barrier diode fabricated at the University of Bristol and its (b) forwards and (c) reverse characteristics.

interfaces between these two materials, with studies investigating 100 nm-thick boron-doped diamond, grown on *n*-type Ga_2O_3 that has been deposited at Stanford University using the microwave plasma CVD technique.

Electrical measurements of devices we've made in this manner have produced promising results, including a catastrophic breakdown of 875 V with a peak electrical field of 4 MV cm^{-1}, which could be reduced with appropriate edge-termination techniques. Based on these results, integrating these materials in the three-dimensional structure that's illustrated in Figure 3 (a) would enable a breakdown voltage of more than 4 kV in that super-heterojunction device. The planar diode also exhibits a low thermal resistance, confirming that diamond delivers excellent heat extraction when deployed in advanced device structures based on Ga_2O_3. Additional promising findings, emerging from Chowdhury's group at Stanford University, are diamond integration using low-temperature CVD, and demonstrating the possibility of the same on Ga_2O_3.

There's no doubt that Ga_2O_3 possesses impressive material properties that ensure it will play a vital role in the power electronics sector. To enhance such success, this oxide should be integrated with other ultra-wide bandgap materials, such as diamond and SiC, that can improve electro-thermal co-design. Note also that Ga_2O_3 has several polytypes, and while we have focused on the β form, other phases should not be forgotten – they provide an opportunity to explore even higher bandgaps and also polarisation. Like other research groups, we are exploring these forms.

Such efforts will help to advance the capabilities of Ga_2O_3 devices, which we forecast to provide a prolonged device lifetime, along with gains at the system level, in terms of size, weight and efficiency. Early studies of converters that employ Ga_2O_3 are already demonstrating potential system benefits, which can lead to a trimming of carbon footprints and help to turn the tide on an escalation in the frequency and severity of natural disasters.

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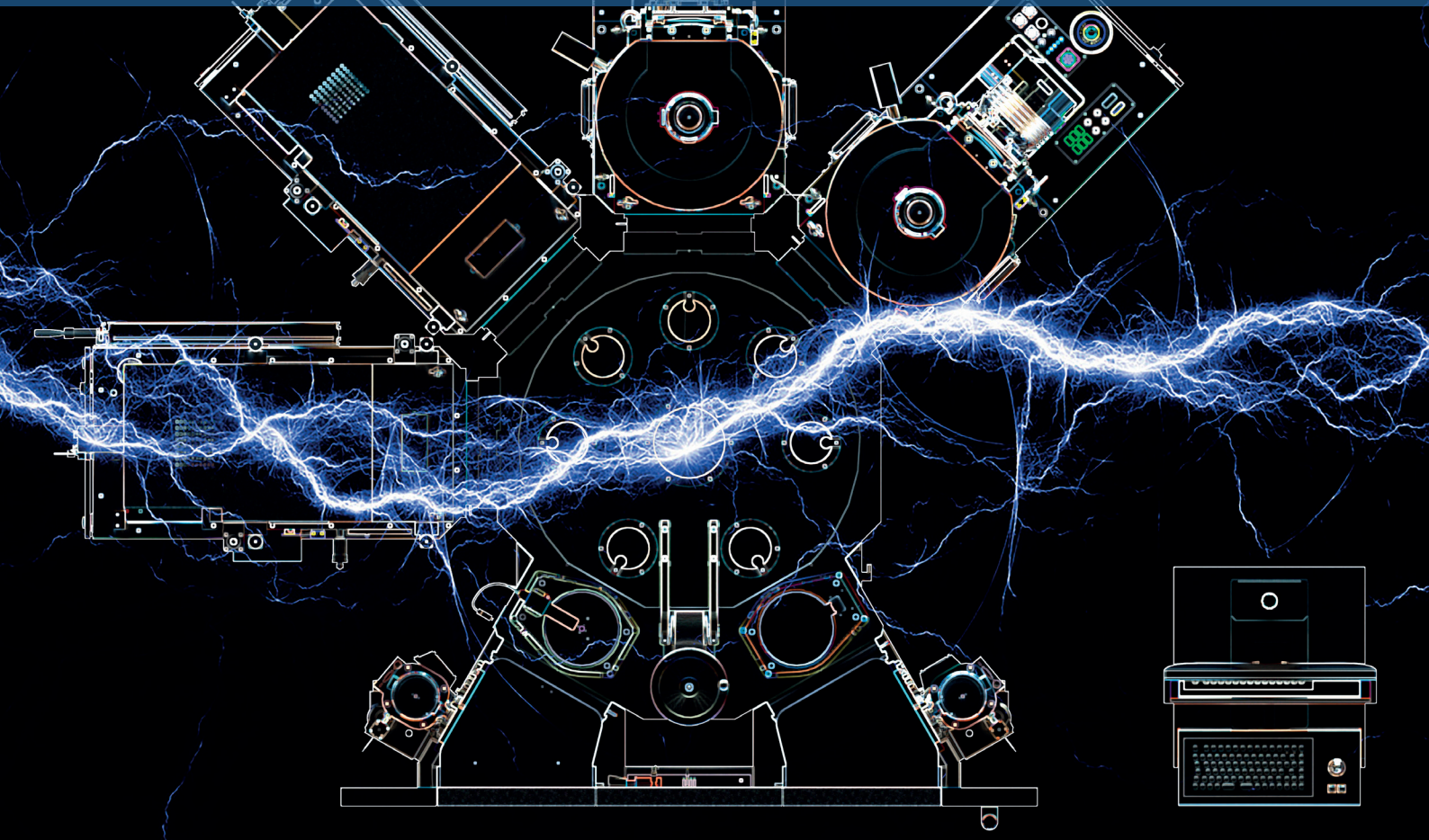

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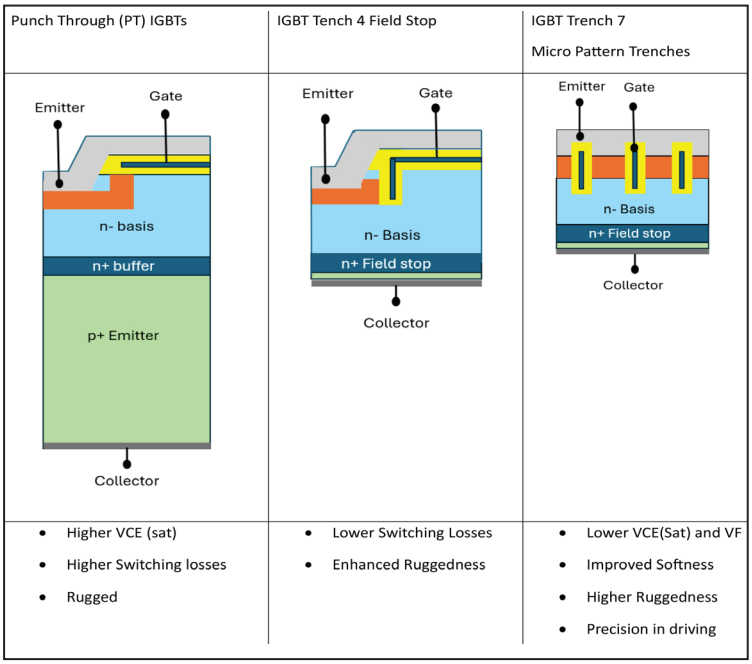
Next-generation IGBT7 technology: versatile and simplified power management

IGBTs have been a mainstay in the industry, combining the advantages of high power with simple driving mechanisms. The new IGBT7 technology has succinct differentiation in device characteristics such as lower forward voltage, higher current ratings, 175°C over-load capacity, improved dv/dt control and enhanced freewheeling diode. When paired with innovative low-inductance packaging, IGBT7 technology offers ease of use, enhanced ruggedness, higher power densities, and improved efficiency, all while reducing system costs. Essential for motor drive applications, the versatile IGBT7 devices will empower a wide range of industries, including aerospace, renewable energy, energy storage systems (ESS), data centers, and commercial and agricultural vehicles.

BY AMIT GOLE, PRODUCT MARKETING MANAGER FOR MICROCHIP TECHNOLOGY'S INTEGRATED POWER SOLUTIONS

AN Insulated-Gate Bipolar Transistor (IGBT) is a power semiconductor device with a collector, emitter and gate. It is called a bipolar transistor as the conduction happens because of the movement of electrons and holes. IGBTs are power horses for a plethora of power electronics applications, including power converters, inverters and choppers.



➤ Figure 1. IGBT technology progression.

IGBTs are widely used in mains-powered systems and equipment with medium or high switching performance from a few kWs to MWs. IGBT power modules are essential components in contemporary power electronics. These modules control and convert electrical power in various applications, including industrial motor drives, renewable energy systems, Electric Vehicles (EVs) and power grids.

Next generation IGBT7

The seventh generation of IGBT power modules are now available in seven packages across multiple parts. These devices feature lower VCE (sat) and VF, overload capacity at TJ of 175°C, 50% higher current capability, enhanced controllability of dv/dt, improved FWD softness and simpler driving compared to previous legacy generations. These features offer a differentiated value proposition of high-power density, durability, reduced system costs, higher efficiency, ease of use and faster time to market

IGBT7 Trech technology

The IGBT Trench7 uses Micro-Pattern Trench (MPT) technology, which consists of parallel trench cells separated by submicron mesas as compared to the square trench cells used in previous generation. Figure 1 below shows the cross section of the different technologies from punch through to the IGBT7. The carrier storage close to the emitter electrode increases for the IGBT7 trench cells due to smaller cell pitches and narrow mesas between

the gates. This results in improvement in electrical conductivity in drift zone, which in turn reduces the forward voltage drastically, resulting in lower conduction losses for the IGBT7 technology.

Figure 2 shows the relative comparison of different IGBT generations including 2, 3,4 and the latest IGBT7. IGBT7 has the lowest on-state voltage, around 15 to 20% reduction compared to previous generation of IGBT4. This low on-state loss results in low conduction losses and, in turn, increases the efficiency for low-to-mid switching frequency applications. Additionally, the IGBT7 comes with a soft antiparallel diode that has better reserve recovery characteristics and low forward voltage (Vf), reducing the losses further to provide higher power density.

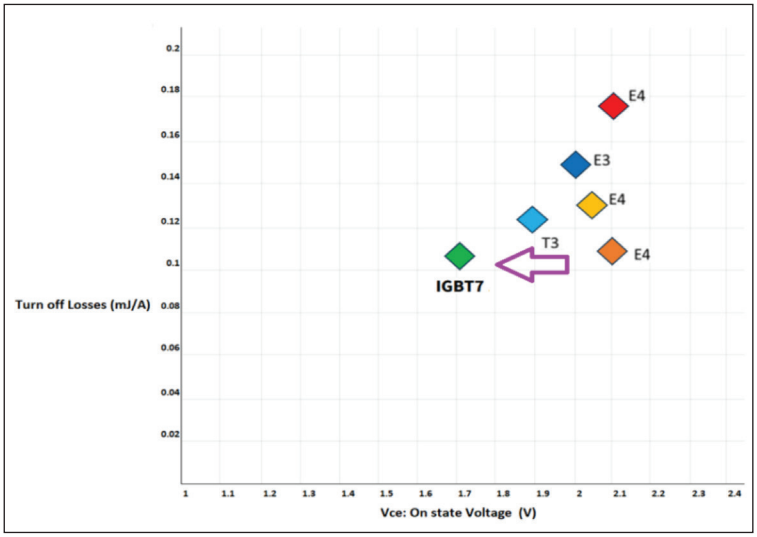
IGBT7 portfolio

IGBT7 power modules are available in the industry-standard 62 mm packages for phase leg or half bridge configuration in D3 package and for single-switch configuration in D4 packages. Microchip offers low-inductance/low-profile packages in 62 mm, such as SP6C, SP6P and SP6LI, offer reduced profile height and lower package inductance and enable high-power density with high reliability. Lower power levels can be served with smaller packages such as SP1F and SP3F, which are also low-profile packages available in various configurations. The ratings extend up to 900A with 1200V and 1700V.

Lower on-state voltage VCE (sat) and lower Vf with improved FWD

With 15 to 20% lower on-state voltage, there is significant loss reduction up to mid switching frequency applications, while the conduction losses at the given dv/dt limitation are decreased and there is a reduction in antiparallel diode loss.

Conduction losses of the IGBTs are directly proportional to the VCE (sat) of the IGBT technology.



➤ Figure 2. Comparison of IGBT technologies (IGBT3 (T3/E3) at TVJ (op): 125°C while IGBT4 and IGBT7 at TVJ (op): 150°C.

IGBT7 has around 1.77V of typical VCE (sat) at TJ 175°C that is far lower than the VCE (sat) of IGBT4, which is 2.1V at TVJ 150°C. This reduction of VCE (sat) by 15% reduces the conduction losses significantly.

Also, reduced forward voltage of the antiparallel diode helps in reducing the diode losses, so the improved diode reduces the forward voltage by 100 mV compared to IGBT4, which reduces the conduction further.

- Total conduction loss = IGBT conduction loss + diode conduction loss
- Total switching loss = IGBT switching loss + diode switching loss
- Total power loss = total switching loss + total power loss
- Efficiency = output power/input power = input power + total power loss/input power

SN	IGBT7 portfolio Features	Application Benefits	User Benefits
1	Lower on-state voltage VCE (sat) and Vf with improved FWD	15% Lower Power Losses Vs IGBT4	High Efficiency
2	Overload capability at TVJ (op) is 175°C	Design flexibility, avoids overdesign	Reliability, High performance to cost ratio
3	Enhanced controllability of dv/dt	Precise control, reduced EMI issues	Reliability, Ease of use
4	Optimized for simple driving	Simplified driver design	Ease of use
5	Higher Current capability	Reduced need for paralleling, Frame size jump	High Power Density, Faster time to Market
6	Lower Inductance /Low profile packages	Avoids overdesign	Reliability, reduced cost

➤ Table 1. IGBT7 Portfolio Features, application benefits and end user benefits.

➤ Table 2. An example comparison between IGBT4 and IGBT7 specs VCE (sat).

Technology	IGBT4	IGBT7	Difference	% reduction
Part	APTGL325A120D3G	APTGX300A120D3G		
Package	D3 62mm standard			
VCE (sat)Typical at TJ = 125 °C VGE = 15V IC = 300A	2.2V	1.7V	0.5V	**22.72%**

Overload capability at TVJ (op) is 175°C

Maximum junction temperature of 175°C compared to 150°C (IGBT4), which is key for motor drives for repetitive, short term overload operation. The IGBT7 power modules are built for challenging applications as they can withstand junction temperature of 175°C during overload condition as opposed to 150°C for IGBT4. This 25°C improvement not only has tremendous advantages in the reliability and durability of the drive power inverter, but also can result in cost-saving benefits with the high-performance-to-cost ratio of the IGBT7 over any other technology.

Inverter motor drivers used in multiple applications such as Commercial and Agricultural Vehicles (CAV), industrial plants and railways where it is important to withstand the short-term overload while working at the normal operating temperature for not less than 1 minute/60 seconds. The same is true to applications such as UPSs where short term overload are critical for the power specifications where the typical overload durations could vary greatly, for example 110% for 10 min+ 125% for 120 sec+ 150% for 15 sec.

During these overall intervals, the inverter and, in turn, the switches carry more current that result in higher junction temperatures. The power switch must be capable of inherently withstanding such overload and the wear and tear caused by the repetitive nature, during its lifetime.

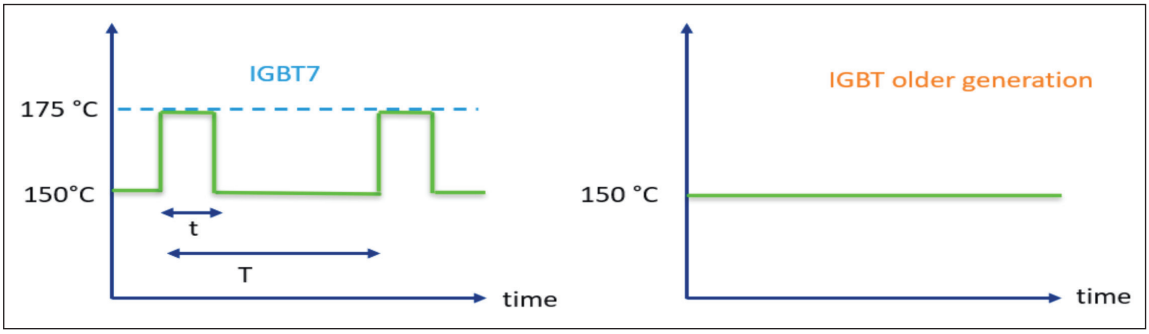
Repeated overloads are a part of industrial motor applications and need to be factored into the design of the inverter and the selection of proper power semiconductor switches. It is important to preserve the durability of the switch when dealing with these overload intervals for prolonged and successful operations.

Enhanced controllability of dv/dt

High level of controllability (ability to vary the dv/dt by adjusting the value of the gate resistor (Rg)) to match the motor insulation requirements or EMI limitations. Inverters are used to drive the motor use Pulse-Width Modulation (PWM) signals do not produce sinusoidal output voltage waveforms. In addition to lower-order harmonics, these waveforms also have superimposed on them steep-fronted, single-amplitude voltage spikes. Turn-to-turn, phase-to-phase and ground insulation of stator windings are subjected to the resulting dielectric stresses. High switching frequency implies higher and steeper pulse rise times.

This higher pulse rise time of the switches results in high dv/ dt, which is further exacerbated by the long cables used in the motor drive application from the inverter to the motor, resulting in higher peak voltages right at the motor terminals. The rise time could also damage the bearings due to parasitic currents flowing from the rotor to the motor frame. These dangerously high voltage spikes due to rise time can result in arching and eventually insulation failure. Longer motor cables even result in higher voltage overshoot with peak values as high as five times the system operating voltage (> 2000V for 415V systems). High voltage spikes can lead to insulation breakdown, resulting in phase-to-phase or turn-to-turn short circuits, with subsequent over-current trips by the drive sensor.

This is why motor manufacturers strongly recommend not exceeding the dv/dt of 5 kV/µs at the inverter terminal in the worst-case scenario for 3-phase motors of typical 380/415/440 VAC.
The higher the length of connection between the motor and inverter, the higher the possibility of peak dv/dt and sharpness of dv/ dt that could increase the



➤ Figure 5. Maximum operation junction temperature comparison between the IGBT7 and older IGBT generations.

Momentary Overload /Base Current	Time Interval between overload (minutes)
110%	>= 9
125%	>= 28
150%	>=60

➤ Table 3. Example of overload durations for Inverter-Fed Polyphase Motors (per ANSI/NEMA MG 1-2016 (Revised 2018)).

voltage at motor terminal to dangerous levels. It is important to optimize the voltage gradient dv/dt as per the motor insulation requirement while carefully designing the general-purpose industrial drive.

To achieve this optimization, IGBT7 demonstrates the highest level of perfection in controlling the inverter's ability to change the dv/dt through adjustment of gate resistor (Rg). When Rg in increased, both turn-on and turn-off dv/dt decrease, while turn-on dv/dt decreases significantly with Rgon in the optimum range, Rg value needs to be optimized to achieve the desired dv/dt < 5 kV/µs.

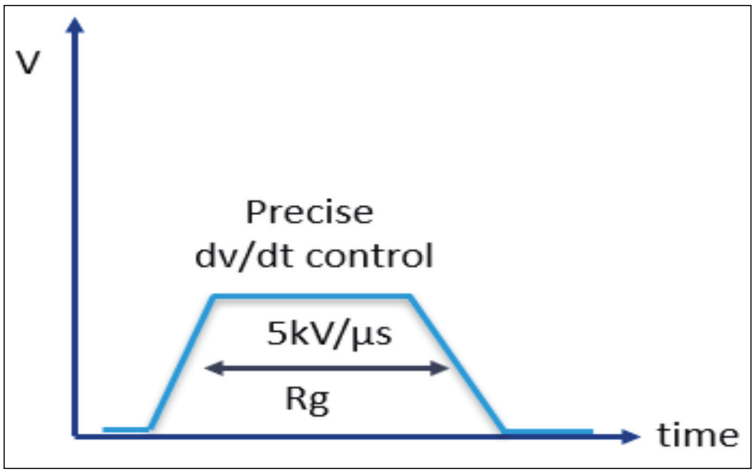
Microchip can provide the graph of Rg and relative dv/dt on special request for optimization of dv/dt which alleviates major design concerns for design and application engineers of Industrial motor drive.

Simple and Hassle-Free gate driving

CGE (Gate Emitter Capacitance) and CGC (Gate Collector capacitance) are balanced to give the IGBT7 full control over the dv/dt, and to optimize the switching waveform and CGE is designed to avoid parasitic turn-on effects, so zero voltage supply for turn-off is feasible (unipolar gate driver power supply).

Higher current capability

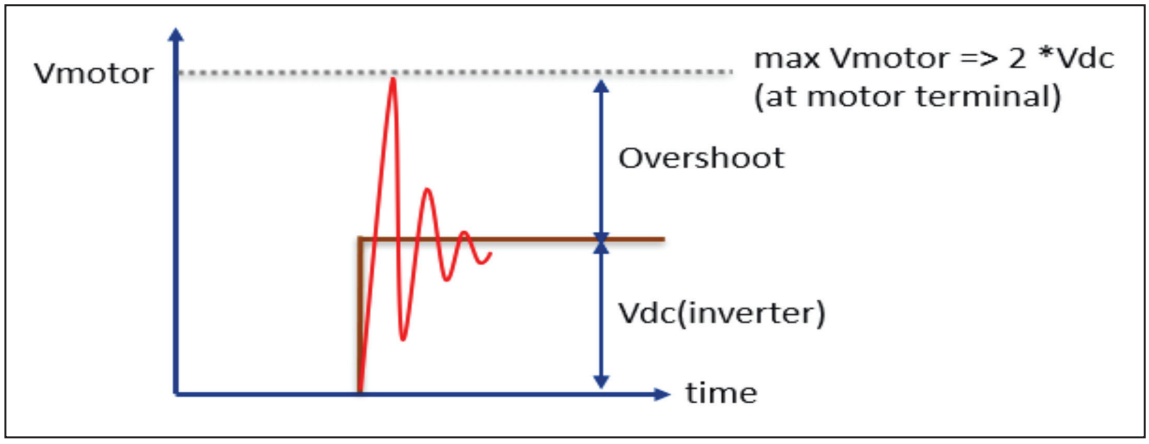
The IGBT7 chip inherently has more current capability than the previous generation IGBT4. This results in higher output power for the given footprints, resulting in frame size jump, which implies a lower frame size can be used in lieu of bigger ones. This also increases the overall power density as more power can be compressed in a given area, avoids paralleling of number of switches, reduces the complexity and improves reliability and durability. Higher power density reduces the power system Bill of Material (BoM) costs and offers faster time to market.



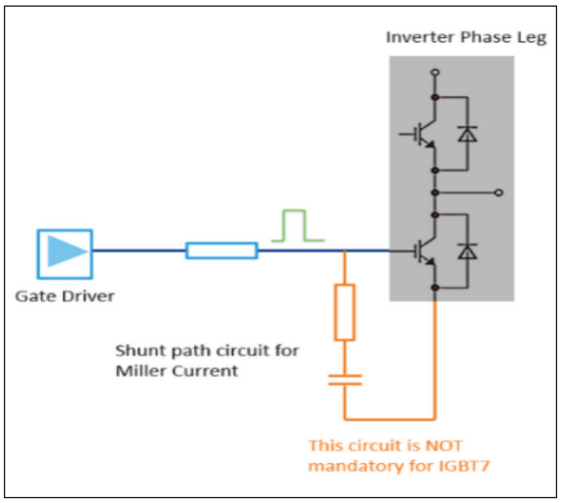
➤ Figure 7. Optimization of dv/dt with Rg using IGBT7.

Lower inductance and lower profile packages

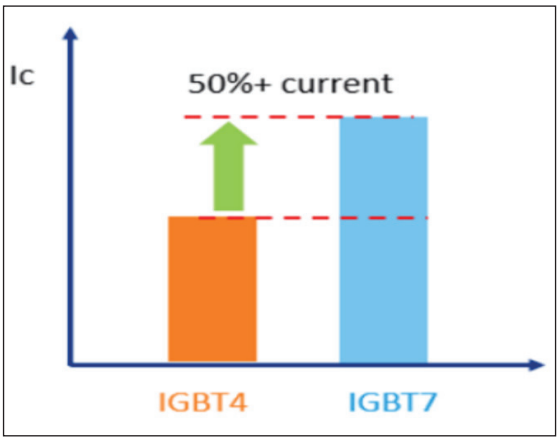
Microchip's low parasitic inductance packages reduce the voltage overshoot enhancing the durability and reliability. Lower profile enables packing more power in less volume improving the power density when used with IGBT7 technology. With lower overshoot voltage, it becomes relatively easier for the user to use 1200V modules for DC link up to 700 to 800V instead of 1700V provided overall inverter lay out is low



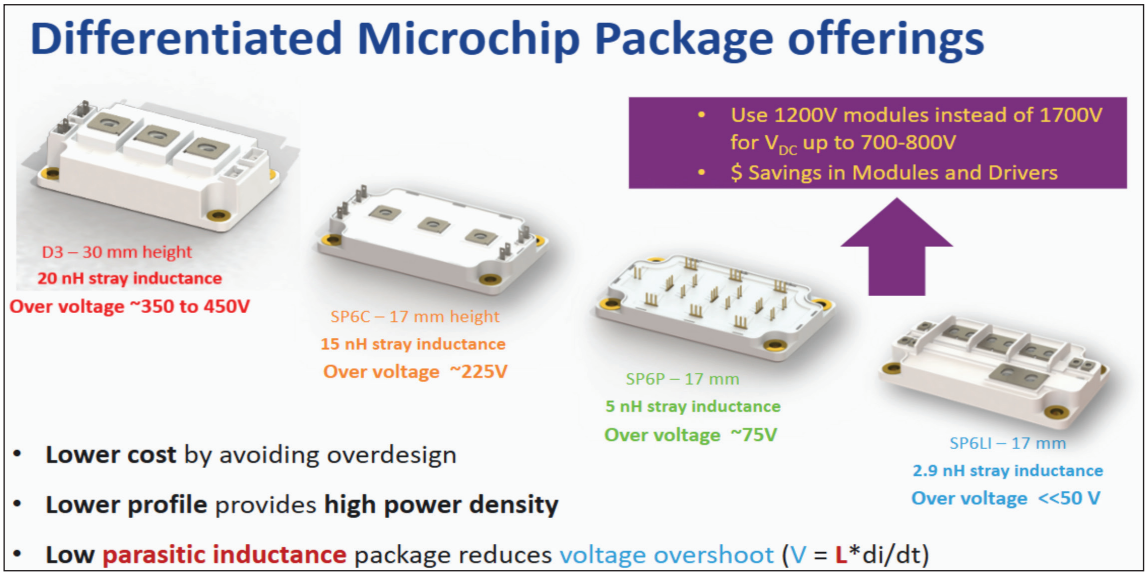
➤ Figure 6. Motor voltages at the motor terminal.



➤ Figure 8. IGBT7 Driver Circuit.



➤ Figure 9. Frame Size jump with 50% higher current in same package.



➤ Figure 10. Differentiated Microchip Packaging.

Package	D3	SP6	SP6P	SP6LI
Height:	30mm	17mm	17mm	17mm
stray inductance:	30nH	15nH	5nH	2.9nH
Voltage overshoot	~350 to 450V	~225V	~75V	~< 50V

➤ Table 4.

FURTHER READING / REFERENCE

- https://www.fluke.com/en-us/learn/blog/power-quality/cable-length-vfd-motors
- https://www.nema.org/docs/default-source/standards-document-library/mg-1-part-31-watermark.pdf?sfvrsn=649fb42f_1
- Application Manual Power Semiconductors (Semikron)
- TRENCHSTOP™ 1200 V IGBT7 T7 Application Note (Infineon) (AN2018-14)
- Amit's Tech Corner, Microchip Aviation and Defense Newsletter Edition 23 Dec 2024

inductive with sandwiched busbar. This saves considerable cost for not only modules but also gate driver board resulting in low-cost power system design.

The IGBT7 features and its end user benefits makes these power modules versatile for multiple applications and megatrends from low to Mid switching frequency applications.

The ease of use without complexity in gate drive mechanism makes the design hassle free and obviates the resources in designing new drivers. The multiple topologies can be readily used as a building blocks for converter of multiple applications providing design flexibility and faster time to market.

IGBT7 power modules enable multiple applications such as solar, wind, motor drive, Energy Storage System (ESS), Commercial and Agricultural Vehicles (CAVs), data center, railways, E-mobility, transmission and distribution, and aviation with their versatility and provide great benefits to customers with power, precision and performance.

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Achieving next generation power density and efficiency for AI and hyperscale data centre PSUs

This article examines the state of the industry, the challenges it faces and outlines advances in PSUs that will take the industry to 8 kW and above, that are essential to support the next phase of generative AI.

BY TAO WEI, SR. APPLICATIONS MANAGER & LLEW VAUGHAN-EDMUNDS, SENIOR DIRECTOR, PRODUCT MANAGEMENT & MARKETING, NAVITAS SEMICONDUCTOR

THE ADOPTION of generative AI has brought step-change benefits to many industries and its use is increasing exponentially. And with exponential growth in use comes the potential for an exponential growth in power consumption. Left unchecked this would see demands for increased data processing, storage and transmission leading to significantly increased operating costs and emissions, putting the net-zero targets of these companies, and the countries in which they operate, at risk.

To counter this, each generation of AI processor has become more efficient per operation, but the rate of growth is far outstripping these efficiency gains. Data center operators are therefore looking to improve efficiency and Power Usage Effectiveness (PUE) on a holistic level by targeting the next two biggest consumers of energy - cooling and the power supplies.

At the same time, the adoption of the latest and most powerful/efficient processors, such as NVIDIA's Blackwell, requires architecture changes in order to supply the vastly increased amount of energy that these run on. Currently, only 5% of global data centers are equipped to deliver this. With these data centers using a fixed-size CRPS/OCP form factor power supply, the move to these next-generation processors urgently demands significant increases in PSU power density.

Until relatively recently silicon was the semiconductor of choice for power devices, but this has reached its physical limits, with a migration to gallium nitride (GaN) and silicon carbide (SiC) now essential. The physical properties – switching speeds, thermal management – of these semiconductors enable significant leaps to be made. Navitas is a pure-play wide bandgap semiconductor company, focused solely on GaN and SiC power technologies. Recognizing how these technologies can address the challenges facing data center architects and operators, the company has set about creating world-leading data center power supply

reference designs to showcase how advanced GaN and SiC technologies can deliver the industry's highest power densities and efficiencies.

How much power does AI consume?

Current energy usage

As a result of the growth in AI, energy consumption by data centers is rising rapidly. Data from the International Energy Agency (IEA) suggests that in 2022 alone, approximately 460 terawatt-hours (TWh) were consumed globally by data centers, approximately 2% of global energy production. In the US, data centers accounted for approximately 3% of all energy consumed in 2023.

The International Energy Agency has forecast that combined global data center electricity consumption will reach 1,000 TWh by 2026. Yet, planning regulations in many western countries have limited the building of additional renewable energy capacity, with AI power consumption accelerating faster than renewable energy capacity globally. An analysis by Bloomberg has suggested AI will consume more energy than all but 12 countries by 2030.

AI's adoption is far from its peak and power consumption by data centers is forecast to grow considerably.

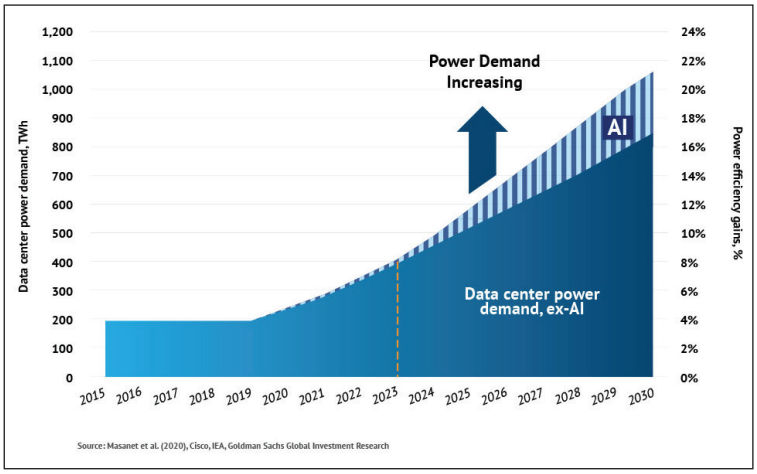
Growth Trends

As above, the IEA has stated electricity consumption by data centers could reach more than 1,000 TWh by 2026. And the US alone will reach this figure just four years later. Goldman Sachs data suggests the share of power used by data centers will more than triple over the course of this decade (2020 – 2030), to c.8%, attributing virtually all of the acceleration in electricity demand to AI.

The US is not alone in its forecast growth. Sweden is expected to see energy use from data centers double as a result of AI by 2030, and double again by 2040. In the UK, AI energy use is set to rise more than 5X over the next 10 years.

Bloomberg estimates that there are more than 7,000 data centers that are either built or in construction. This compares with 3,600 in 2015. And their energy consumption by 2034 will be approximately the same as the entirety of India.

This growth in energy consumption for AI data centers is being accelerated by a consumer shift towards using generative AI as a search engine, with ChatGPT queries being between 6X and 10X as power intensive as traditional Google searches.



➤ Figure 1: Forecast growth of AI and data center power demands to 2030, extrapolated from Goldman Sachs data.

According to Goldman Sachs, the growth in energy consumption by AI data centers will be higher than for any others of its tracked sectors, causing more than a third (38%) of all energy consumption growth. This is 50% more than either of the next two biggest causes of increased energy consumption: residential and transportation.

Takeaway

As we can see, significant efficiencies are needed to mitigate the effect of generative AI, and these are needed across the board. The processors need to reduce the energy-per-operation, but with the scale of growth taking place this will not be enough and power supplies, as one of the next biggest consumers of energy in the data center, must also evolve to reduce losses while meeting the increased power demands of AI servers.

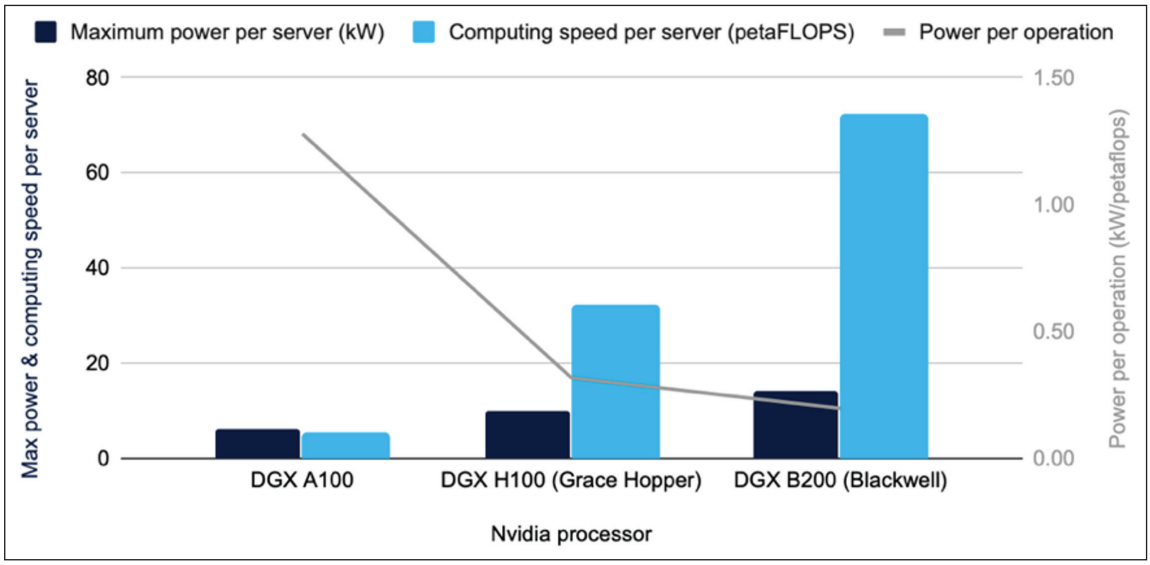
Navitas is addressing the challenge of power supplies, delivering more power more efficiently and enabling AI data centers to adopt processors such as NVIDIA's Blackwell and Rubin, which significantly reduce the power required per operation.

Power Consumption by AI Processors

AI Processors are quickly becoming more efficient, with each subsequent generation requiring less energy per flops, as can be seen in the below table showing AI processor evolution from 2014 to 2018. Today, further leaps have been made and the rise of AI has meant the world's most valuable company

Year	Processor	Watts	Teraflops	Efficiency (kW/petaflops)
Early AI evolution (pre 2015)				
2014	AMD FirePro S9150	235	5.07	46.4
2014	NVIDIA Tesla K80	300	8.73	34.4
2015-18				
2017	NVIDIA Tesla v100	300	125	2.4
2018	Google TPU v3	450	420	1.07

➤ Figure 2: Early evolution of AI processors demonstrates efficiency gains, with each generation requiring less power per operation.



➤ Figure 3: Blackwell DGX B200 server systems will improve further on Grace Hopper to enable 72 petaflops, but do so at just 0.2 kW per petaflops.

is NVIDIA. Recent evolutions of its server system specifications are indicative of increasing max power per server but with lower power intensity per petaflops.

Operating at 0.32 kW per petaflops, NVIDIA's DGX H100 (Grace Hopper) is capable of 7X computing speeds of NVIDIA's previous generation (DGX A100), but only uses 1.5X the power. The Blackwell DGX B200 server system will improve further on Grace Hopper to enable 72 petaflops, and do so at just 0.2 kW per petaflops.

Specifications for the newly announced NVIDIA Rubin have not yet been announced.

It should however be noted that this is still a power increase per server system of 40%, shifting from 700 W each for Grace Hopper, to 1,000 W for Blackwell and this necessitates advances in power supplies.

The rise of these more efficient (but more powerful) processor configurations also presents a major challenge for data centers, requiring multiple changes in their architecture in order to power them, with an analysis by AMAX suggesting fewer than 5% of the world's data centers are currently capable of supporting even 50 kW per rack. Blackwell configurations require 60 kW to 120 kW per rack. AMAX has suggested this could create two tiers of data center.

Takeaway
AI processors are quickly becoming more efficient, with each subsequent generation requiring less energy per flops. But increase in use is far outstripping these gains in efficiency.

PSU power densities therefore need to rise quickly if these more efficient processors can be adopted more widely.

Navitas' CRPS185 reference design has achieved the highest densities of any data center PSU and the lessons from this have been applied to its 8.5 kW PSU — announced at electronica 2024 (see section 6.2). Navitas has also set out its roadmap to 10 kW PSUs and will announce this in 2025.

Power Supply Efficiency

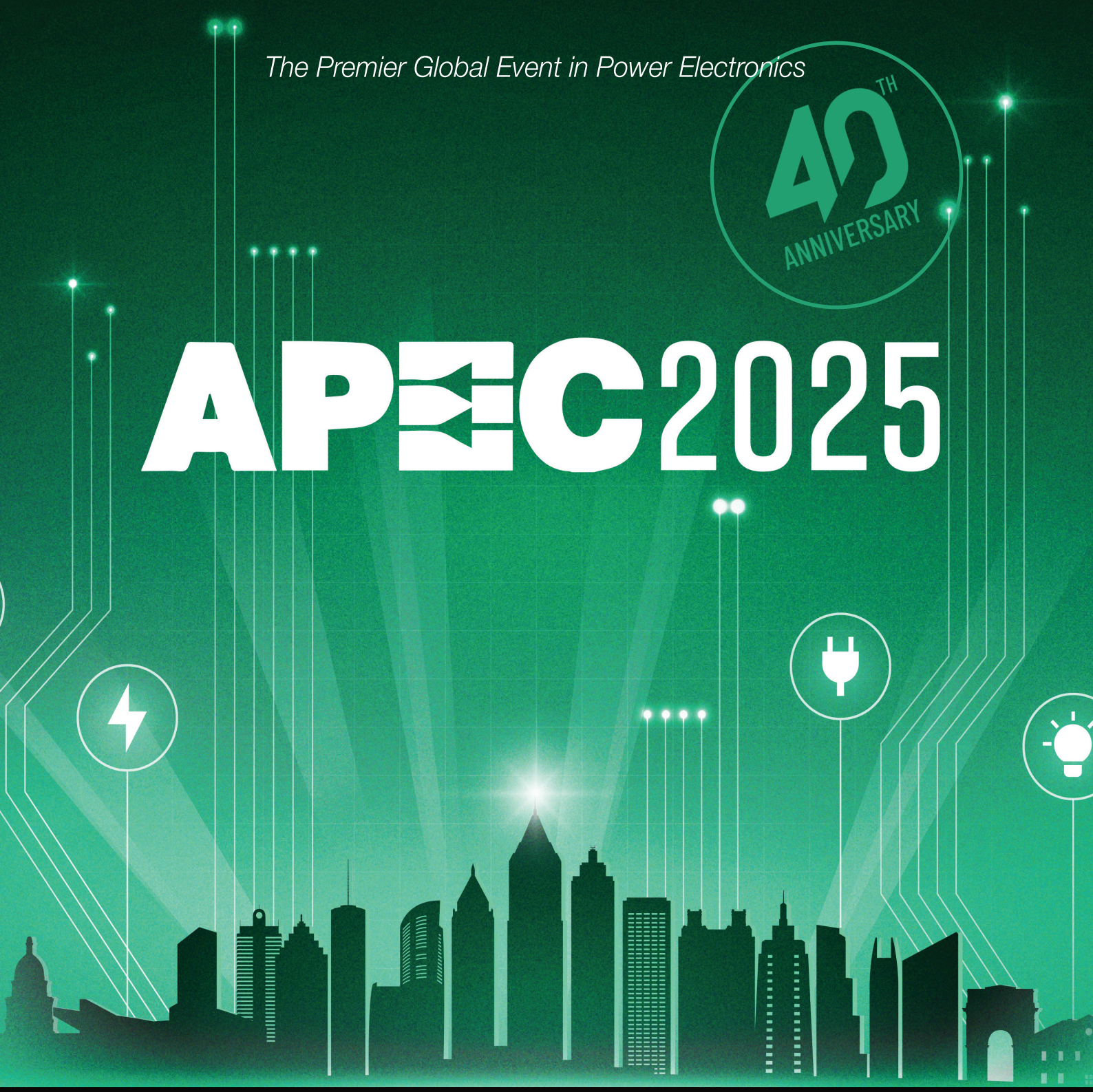
80 PLUS Certification
To minimize the power consumed through losses in the power supply, industry standards have been applied. The key standard for the PSU sector is the 80 PLUS certification, a voluntary program aimed at encouraging manufacturers to produce more energy efficient products.

Since its inception in 2004, the standard has evolved with five additional levels of increasing efficiency being added to further improve PSU efficiency as technologies improve. Since 2012, the top standard has been Titanium. This requires that PSUs are 90% efficient at 10% of load, 96% at 50% and 91% at 100% of load with a 230 V input. While not officially mandating the standard, the EU has aligned its EcoDesign Directives with the 80 PLUS certification standard and data centers, including those for AI, operating in EU territories are legally required to comply with these EcoDesign Directives.

In addition, 80 PLUS Titanium specifies a power factor of at least 0.95 at lower load levels. Effectively, this calls for compliant power supplies to contain active power-factor correction (PFC).

Future evolutions of the 80 PLUS standard are expected to stipulate efficiencies over 97% at 50% of load, as well as increased power densities, peak power and hold up time.

Takeaway
The minimum PSU efficiency standards will continue to improve and Navitas is working to deliver world leading efficiencies for designs using its latest range of power ICs. In July 2024 Navitas announced a PSU with a world leading 137 W/in^3 power density.



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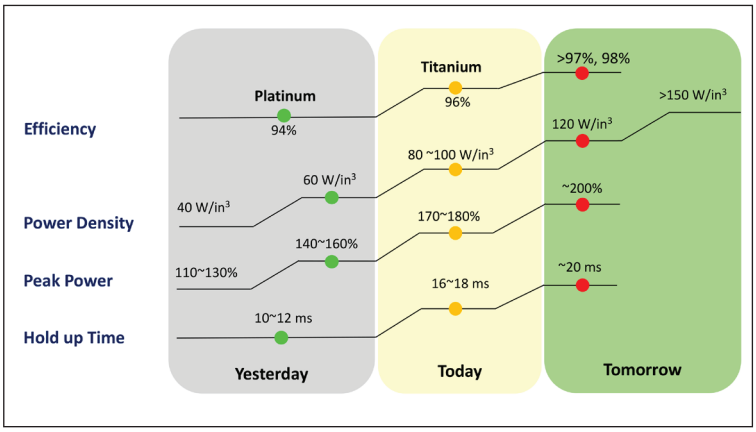


➤ Figure 4: The 80 PLUS PSU efficiency standard is set to become ever more stringent

PSU power density

PSU form factors

To simplify deployment and maintenance by enabling modularity and flexibility, as well as easing redundancy, AI and hyperscaler data center power supplies come in three form-factors: CRPS185 (common redundant power supply), CRPS265 and OCP (Open Compute Project).

These measure the same width and height (73.5 mm x 40 mm), but vary in length (CRPS185 = 185 mm, CRPS265 = 265 mm, OCP = 600 mm), with these specifications developed and defined by the hyperscale Open Compute Project, whose members include Dell, Facebook/Meta, Google, Intel and Microsoft. By having these common standards, the industry is able to maximize interoperability and therefore simplify upgrades / minimize downtime in the event of a failure. As these are fixed sizes, delivering more power to AI servers necessitates an increasing power density, and at the same improved efficiency, reliability, and manageability.

Building a high-frequency CRPS LLC converter

Building a multi-output LLC converter using silicon ICs calls for a delicate balance between minimizing transformer winding losses, switching and conduction losses in the synchronous rectifiers, and power-supply termination losses.

While raising the switching frequency is desirable to allow for smaller magnetic components, termination losses are increased. However, the frequency, density, and efficiency advantages of GaN in bridge topologies such as active-clamp flyback (ACF), CrCM totem-pole PFC and LLC, means using these devices offers a number of benefits that directly address the challenges of designing next- generation PSUs for data centers.

Takeaway

Silicon has reached its physical limits in terms of power density and efficiency. Wide bandgap semiconductors must play a key role in the next generation of power supply architectures. These semiconductors bring myriad benefits, from increased densities, to improved efficiencies and also enhanced thermal properties. But their use requires expertise, for example GaN FETs have more fragile gates than silicon and require protections be engineered to prevent voltage spike damage and to avoid ringing. This has been addressed in Navitas power ICs such as GaNFast and GaNSafe.

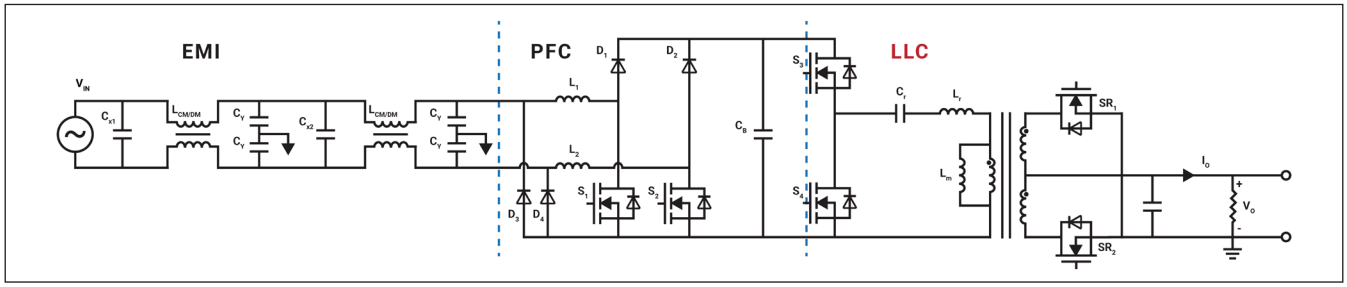
Silicon vs. Wide Bandgap Materials in PSUs

Wide Bandgap Semiconductors in PSUs

The bandgap is the energy needed to free an electron from its orbit around the nucleus. As this directly determines the electric field that a given material can withstand, a wider bandgap enables the development of semiconductors with very short or narrow depletion regions. This enables device structures that possess very high carrier densities, and therefore smaller transistors and shorter current paths with ultra-low resistance and capacitance, as well as switching speeds that are orders of magnitude higher.
Bandgap is measured in eV (electron volts), with silicon having a bandgap of 1.12 eV.

Silicon Carbide

Silicon carbide (SiC) is a compound known for its high thermal conductivity, high electric field breakdown strength, and excellent thermal stability. It has a bandgap of 2.26 eV. SiC-based components can operate at higher temperatures and voltages than their silicon counterparts, resulting in more efficient power conversion and reduced energy losses. SiC MOSFETs and diodes enable faster switching speeds and lower power losses, enhancing the overall efficiency and while their physical and switching properties tend to make them more applicable to the automotive, industrial,



➤ Figure 5: Schematic of a power supply suitable for 80 PLUS Titanium, combining active PFC, essential EMI filtering, and an efficient LLC resonant converter with synchronous rectifiers (SR1, SR2).

and renewable energy sectors, they have a crucial role to play in PSUs for AI data centers too.

Gallium Nitride

With a bandgap of 3.39 eV, GaN possesses a high electron mobility and these devices allow much higher switching frequencies and support the use of planar transformers.

Using this technology, it is possible to build the LLC converter to meet the CRPS form-factor requirement in a multi- transformer design to deliver the desired output power. For example, building a high-efficiency and high-density LLC converter can be facilitated by using Navitas's proprietary GaNFast half-bridge ICs with robust, high-speed integrated GaN drive to address the sensitivity and fragility issues associated with discrete GaN chips (see below). GaNFast power ICs offer extremely low switching losses, with a transient-voltage capability up to 800 V, and other high-speed advantages such as low gate charge (Qg), output capacitance (COSS) and no reverse-recovery loss (Qrr). Navitas estimates that GaNFast power ICs save 5% of the LLC-stage system material cost, plus $64 per power supply in electricity over 3 years thanks to high-speed switching and size, weight and cost reduction of passive components.

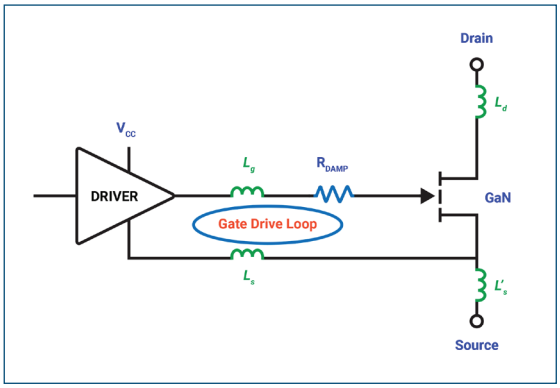
Fragile gate structures

When designing with GaN devices it is essential that its fragile gate structures are not exposed to voltage spikes or ringing. Integrating an optimized gate driver with the GaN FET helps designers properly control induced Ldi/dt voltage spikes on the gate-source voltage (VGS) to avoid these risks. Implementing the driver with the GaN FET minimizes the stray gate loop inductance, preventing excessive peak voltages. Leveraging protection features also integrated in the package, designers can take a "digital in, power out" approach to simplify power supply design with faster switching, higher efficiency, and superior power density.

Navitas' GaNSafe™ has high-speed protection with autonomous 'detect and protect' that acts within 50 ns. ESD protection is also implemented to protect against events up to 2 kV. And to protect against extraordinary application conditions, GaNSafe integrates a 650 V continuous and 800 V transient voltage rating.

Takeaway

As the adoption of generative AI grows rapidly, wide bandgap materials such as SiC and GaN play a pivotal role in enabling AI data centers to meet the demands being placed on them. Navitas is among the world's leaders in GaN and SiC power ICs with a roadmap that is helping AI data center operators to both improve efficiencies from PSUs, but also to deliver the power densities required to bring on board more efficient processors like Blackwell and Rubin.



➤ Figure 6: Integrating an optimized gate driver in the same package as the GaN HEMT helps designers properly control negative spikes in the gate-source voltage to avoid these risks.

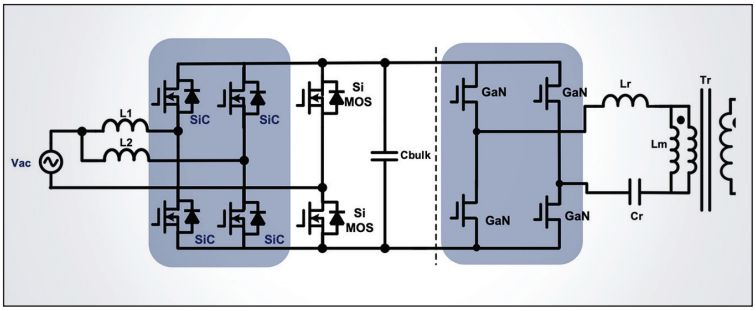
A roadmap to 12 kW and beyond

If AI is to advance further, and if the industry is to be able to implement the more efficient generation of processors, it is vital that power supply improvements keep pace with processor evolution. Here at Navitas, we are working to ensure the power required by processors such as Blackwell and Rubin can be delivered, and that this is done as efficiently as possible.

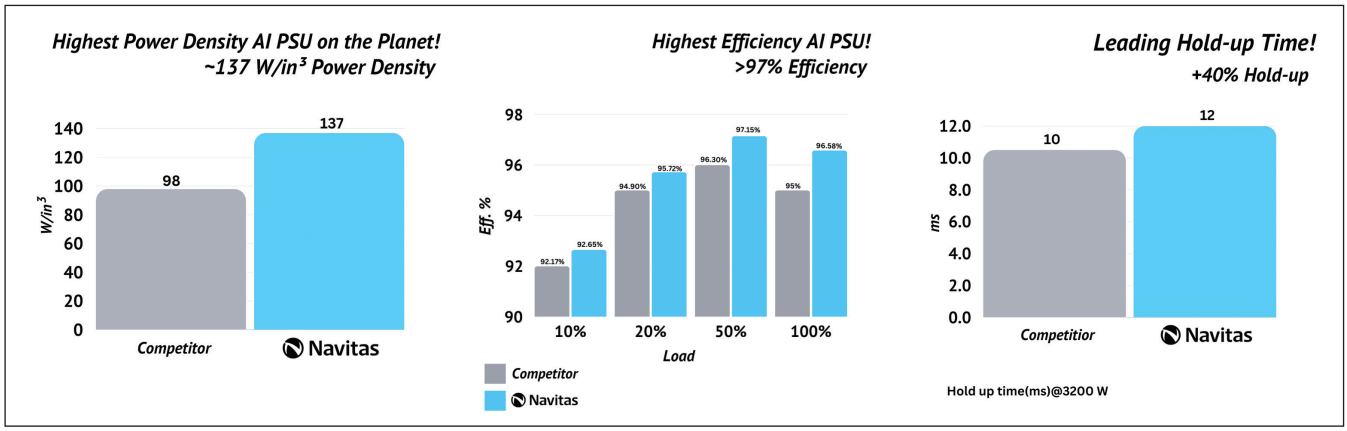
The industry's highest power density

In July 2024, Navitas announced an AI data center server PSU reference design with an industry leading 137 W/in^3. This 54 V AC-DC power supply has been created using Navitas' GaNSafe and GeneSiC families of products and is designed in a CRPS185 form factor. At the heart of the design is an interleaved CCM totem-pole PFC using SiC, with a full-bridge LLC topology based on GaN. In this design, the fundamental strengths of each semiconductor technology are exploited for the highest frequency, coolest operation, optimized reliability and robustness, and highest power density and efficiency.

The 650 V G3F SiC MOSFETs feature 'trench-assisted planar' technology, which delivers world-leading performance over temperature for the highest system efficiency and reliability in real-world applications. For the LLC stage, the power IC is a 650 V GaNSafe chip with integrated power, protection, control, and drive in an easy-to- use, robust, thermally-adept TOLL power package. GaNSafe power ICs offer extremely low switching losses, with a transient-voltage capability up to 800 V, and other high-speed advantages such as low gate charge (Qg), output capacitance (COSS),



➤ Figure 7: A CRPS185 PSU reference design capable of delivering an industry leading 137 W/in^3.



➤ Figure 8: Improvements seen in the testing of Navitas' 4.5 kW versus a comparable 3.2 CRPS185 PSU.

and no reverse-recovery loss (Qrr). High-speed switching reduces the size, weight, and cost of passive components in a power supply, such as transformers, capacitors, and EMI filters. As power density increases, the implementation of GaN and SiC enables sustainability benefits, specifically CO_2 reductions due to system efficiency increases and 'dematerialization'.

Data from testing of the reference design showed an increased efficiency of more than 97% with an increase in power density from 98 W/in³ to 137 W/in³ versus a comparable 3.2 kW CRPS solution. This translates to a power output of 4.5 kW. The test data also showed it was possible to reduce waste power and mitigate the need for additional thermal management provision.

The pathway to 12 kW AC-DC converters and beyond

To support 2025 AI power requirements, Navitas has announced its roadmap, which outlined its plans to announce an 8.5 kW power platform by the end of 2024, and a 10 kW PSU shortly thereafter.
In November 2024, at electronica, the company launched the industry's first 8.5 kW power platform powered by GaN and SiC. This AI-optimized 54 V output PSU achieves a 98% peak efficiency and complies with Open Compute Project (OCP) and Open Rack v3 (ORv3) specifications. It utilizes high-power GaNSafe and Gen-3 Fast SiC MOSFETs, configured in 3-phase interleaved PFC and LLC topologies, to ensure the highest efficiency and performance, with the lowest component count. Navitas' unique design center is creating systems based on GaNSafe and GeneSiC that address dramatic increases in AI data center power requirements, assisting customers to deploy platforms quickly and effectively to meet the accelerated time-to- market demands of rapid AI advances.

These include complete design collateral with fully tested hardware, schematics, bill-of-materials, layout, simulation and hardware test results to maximize first-time-right designs and fast revenue generation.

Navitas is already engaged with major data center customers, and the full platform launch completes a 3X increase in power demands in less than 18 months.

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Rewiring the road

Harnessing the power of 48V. Part 1.

BY KIRK ULERY, BUSINESS DEVELOPMENT MANAGER, MOLEX TRANSPORTATION SOLUTIONS

AS THE MODERN driving experience demands more electronics, the shift toward 48V electrical system technology is rapidly gaining traction, disrupting traditional automotive power architectures. Today's increasingly electrified vehicles needs more. This surge in demand is propelling innovation and investment in 48V systems as automakers seek to enhance vehicle performance and efficiency.

Are we at a tipping point?

48V technology is a key enabler for advanced automotive features such as electric turbocharging, regenerative braking and advanced infotainment systems. It provides a compelling solution for a range of vehicles, from gas-powered to electric, and is poised for widespread adoption.

But it's not that easy. For 48V systems to be successfully implemented, challenges such as standardization and cost reduction must be addressed.

How do we clear the hurdles to move forward? What will it take for 48V power to become the new normal? Let's explore these questions together.

The rise of 48v: a new standard for automotive power

For decades, 12V electrical systems have powered everything from headlights to entertainment systems in vehicles. But the automotive industry is evolving, and the way vehicles are powered is evolving along with it.

By quadrupling the system voltage, 48V enables significant advancements in power delivery, representing a substantial departure from the conventional 12V electrical structure. This new level of power enables comprehensive and evolved features such as electric turbocharging, regenerative braking and battery preconditioning for accelerated auxiliary charging, to name a few. From wiring and connectors to power management systems and components, a fundamental redesign is necessary to maximize the technology benefits of 48V.

Key characteristics of 48v systems

It's important to focus on what differentiates 48V systems from traditional 12V systems. In addition to the fundamental components described above, here are the overarching features that highlight the evolution of vehicle power systems.

Higher voltage

While increasing voltage from 12V to 48V can reduce amperage in some applications, assessing the system's overall power requirements is crucial. Larger wire gauge might be sufficient for certain components, but high-power demands, like those of electric motors or high-power accessories, may still require bulky cables. Striking the right balance between voltage, amperage and wire gauge is essential to optimizing system efficiency and performance.

Increased power capacity

48V systems offer a significant boost in power output. This increased capacity enables the electrification of essential vehicle components, such as power steering pumps, air compressors and water pumps. By operating independently from the engine's accessory drive, these components are expected to allow optimization for efficiency and reliability.

Improved efficiency

Reduced resistive losses in power transmission contribute to higher efficiency. Powering electric compressors and pumps directly from the 48V system reduces the engine load, enabling it to operate more efficiently. Regenerative braking, a

core component of 48V systems, also significantly heightens efficiency by recovering energy that would otherwise be lost as heat.

Flexibility and scalability

48V technology is adaptable to a wide range of vehicle architectures, from traditional internal combustion engine (ICE) vehicles to fully electric models. This flexibility allows automakers to gradually introduce 48V systems into their product lines, as we will explore later. Additionally, 48V architecture lays the groundwork for future electrification strategies, offering a scalable path to higher voltage systems as battery technologies advance.

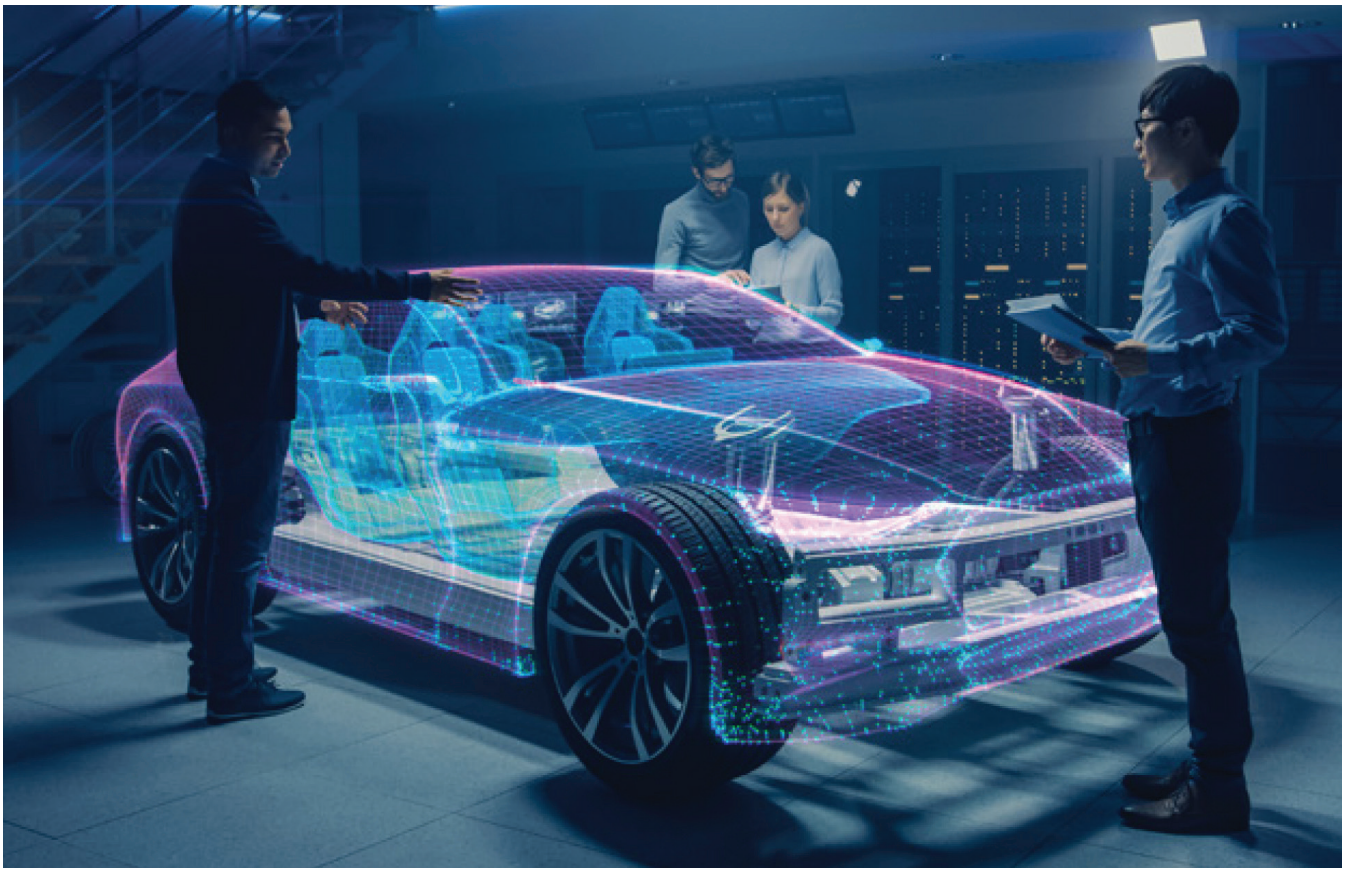
By understanding these core characteristics, we can better appreciate the benefits and applications of 48V technology in the automotive industry, recognizing the significant leap forward that 48V represents.

48v system versatility and efficiency

New 48V technology serves as a versatile platform that enhances vehicle efficiency and performance and benefits both traditional and electric vehicles. What does this mean for each market?

For traditional vehicles

48V systems present significant advantages over traditional 12V systems, including improved power delivery for advanced features such as electric turbocharging, idle stop-start and regenerative braking. While some of these functions are possible with 12V systems, the higher voltage of 48V systems enables them to operate with greater efficiency and effectiveness. Additionally, 48V systems are better



equipped to handle more demanding electrical loads, which translates to enhanced vehicle performance and improved fuel economy.

For EVs
48V systems serve as a secondary power source for auxiliary components in EVs, easing the load on the primary high-voltage battery. In some instances, 48V architecture can accelerate charging times by aiding battery preconditioning. Incorporating 48V electronics aids overall EV efficiency by minimizing power losses, maximizing component performance and boosting energy recovery.

Keeping up with connectors

While 12V connectors have been adequate for decades, 48V electrical systems need a new level of connector performance and reliability. While 12V connectors may be able to handle higher currents, they would need to be designed with larger contact areas or different materials to ensure reliable performance and prevent overheating. This can lead to increased size and weight. However, because of advancements in 48V connector technology, advanced mid-voltage connectors can provide highly effective support for 48V automotive power systems.

Material science advancements
While 48V connectors may utilize similar materials as 12V connectors, specific materials and their properties are crucial for ensuring reliable and efficient performance in 48V applications. Advanced materials like high-temperature resistant plastics and specialized metal alloys can enhance insulation, conductivity and overall durability, meeting the demanding requirements of 48V systems.

design innovations
Enhanced contact designs are essential to reduce contact resistance and improve current handling capabilities. This can be achieved through multiple contacts or larger contact surface areas. Robust locking mechanisms ensure secure connections in harsh automotive environments. Redesigned connector housings with larger contact areas and improved sealing mechanisms are also necessary to effectively handle higher currents and ensure reliable performance in 48V systems.

Manufacturing processes
Precision manufacturing ensures tight tolerances and consistent performance, which is crucial for 48V connectors. Automated assembly processes facilitate production efficiency and minimize errors.

Tes**ting and validation**
Advanced connectors undergo rigorous testing for performance validation under extreme conditions, including temperature cycling, vibration and humidity. Computer-aided engineering (CAE) tools can simulate connector performance and identify potential design vulnerabilities during the development stages. By incorporating these advancements, connector manufacturers can produce products that meet the stringent specifications of 48V automotive systems, ensuring reliable and efficient power delivery.

Paving the way for 48v success

The transition to 48V technology presents significant opportunities, but the path forward will require solutions such as standardization and cost reduction. As it adopts this new electrical architecture, the automotive industry must navigate a range of challenges. Success will require strategic planning, continuous innovation and strong industry collaboration. If the shift to 48V systems were simple, it would already be standard across the industry. However, a combination of technical and economic challenges has slowed the transition.

Core obstacles to widespread 48v adoption

The adoption of 48V systems faces two major hurdles: cost and complexity. First, the upfront investment in 48V components, including batteries, power electronics and electric motors is likely to be higher than for traditional 12V systems, which can impact vehicle prices and potentially limit consumer interest. Second, integrating 48V technology into existing vehicle platforms is expected to require significant engineering efforts. Ensuring compatibility with current electrical systems and safety features adds both development time and costs for OEMs.

Technical challenges in connectivity

Interconnectivity and compatibility are critical hurdles in 48V system integration. This involves a deep understanding of the multiple requirements and complexities of the vehicle architecture and, therefore, a careful connector selection to ensure system reliability and efficiency. These systems must support reliable and secure data communication to optimize the performance of the 48V-powered components. Engineers must also address electromagnetic interference (EMI) to ensure safe and reliable vehicle operation, preventing disruption between the high-voltage system and other electronic components.

The higher voltage levels in 48V systems can lead to increased EMI emissions, making it more challenging to shield against interference than it is with lower voltage systems. Wiring and harness designs are crucial, as higher voltage and current requirements introduce challenges related to weight, space and cost.

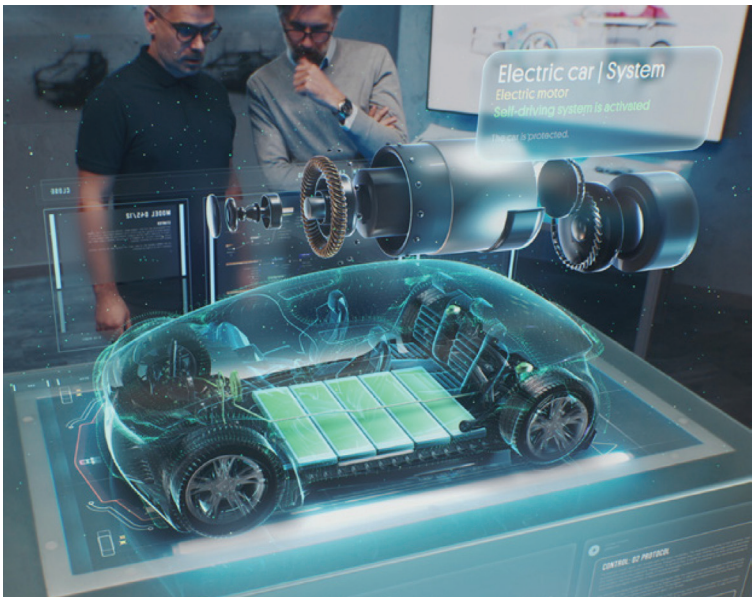
Design considerations

Incorporating 48V systems calls for careful thermal management and electrical system architecture modifications to ensure optimal performance and reliability. To prevent overheating, engineers must include efficient cooling systems for 48V components, such as the battery and power electronics, into the overall vehicle thermal management strategy. Modifying the electrical architecture of existing vehicle models to accommodate 48V components while ensuring compatibility with the existing 12V system demands careful planning and design.

Solutions and strategies to overcome 48v challenges

Overcoming barriers to 48V system adoption warrants a strategic, collaborative approach. For manufacturers and tiers, addressing these challenges means quickly delivering clear value. Reducing costs is critical for both manufacturers and consumers. Achieving economies of scale is one effective strategy. Standardizing components across vehicles can decrease manufacturing complexity and costs. Whether through shared drivetrains or uniform infotainment systems, standardization enables more efficient production while supporting the adoption of advanced power systems. Automakers and OEMs can enhance system integration through modular design. Modular components empower automakers to adapt to

Successful 48V system integration demands painstaking attention to technical details. Standardizing connectors can simplify assembly and reduce costs. To ensure secure and reliable data communication within the 48V system and with other vehicle components, manufacturers should establish robust communication protocols



various vehicle platforms, streamline component usage and reduce development time. This approach also futureproofs systems and makes responding to market trends and technological advancements easier.

Successful 48V system integration demands painstaking attention to technical details. Standardizing connectors can simplify assembly and reduce costs. To ensure secure and reliable data communication within the 48V system and with other vehicle components, manufacturers should establish robust communication protocols. Additionally, implementing effective EMI shielding and developing lightweight, durable wiring solutions can lead to significant weight and cost savings without compromising performance or reliability.

Engineers have options regarding difficult design considerations. They can address thermal management concerns by adopting advanced cooling technologies, such as liquid cooling and heat exchangers, to manage thermal loads effectively. Flexible and scalable electrical system architectures are essential to accommodate 48V components while maintaining compatibility with existing systems. This will involve work from every stakeholder, from design to the final product, but achieving widespread popularity of the 48V system will allow the automotive industry to continue making meaningful technological leaps.

Igniting automotive innovation: opening new roads

Initially focused on mild and plug-in hybrid vehicles, 48V systems offer broad applicability across the automotive landscape, including traditional ICE vehicles. Far from being just a transitional step, 48V technology represents an even larger platform for groundbreaking innovation. Let's delve into why this is the case.

Unlocking new vehicle capabilities

The increased electrical power density from 48V systems opens up a wide range of possibilities for expanding vehicle performance, comfort and functionality.

Enhanced powertrain performance
By powering electric compressors or motors, 48V systems can drive turbochargers or superchargers independently of the engine, eliminating turbo lag and boosting low-end torque. Additionally, these systems enable efficient energy recovery during deceleration, storing energy in the battery for later use and optimizing fuel consumption and overall performance.

Advanced comfort and convenience
48V technology transforms comfort and convenience features by enabling the efficient operation of electrically powered components such as air compressors, water pumps and power steering systems. This translates to more responsive and efficient climate control, precise engine temperature management and superior steering responsiveness, elevating the experience for both the driver and passengers.

Improved driver assistance systems
Advanced driver assistance systems (ADAS) greatly benefit from the robust power delivery of 48V systems. By delivering higher current and voltage, these systems can efficiently power the sensors, actuators and control units required for ADAS functionalities. From radar to LiDAR systems to electric power steering and braking, 48V ensures reliable and responsive operation, elevating vehicle safety and driver confidence. This enhanced power delivery paves the way for more complex ADAS functions, such as automated parking, highway pilot and — ultimately — full autonomous driving.

Precise control and customization of cabin environments
Elevating vehicle comfort and luxury, 48V systems enable more complex and sophisticated features than traditional 12V systems. This includes — but is certainly not limited to — accessories such as multi-contour seat adjustment, advanced ventilation systems and enhanced climate control. This expanded capability creates a more refined and personalized experience for drivers and passengers alike.

Vehicle-to-load (V2L) capabilities
48V power systems open the potential for V2L options, turning vehicles into mobile power sources. With sufficient power density, 48V systems can enable bidirectional power flow, allowing stored energy to be discharged to external devices. This functionality expands a vehicle's utility, enabling it to power camping equipment, electronic devices or even serve as a backup power source during emergencies.

Part 2 of this article will appear in PEW Issue 2

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Improving annealing conditions for GaN MOSFETs

While a high-temperature anneal is ideal for reducing electron traps in GaN MOSFETs, lower temperatures are needed to prevent severe hole trapping

RESEARCHERS at Osaka University have demonstrated that low-temperature post-deposition annealing slashes the density of hole traps at the interface between SiO_2 and *p*-type GaN. It's an observation will aid the development of *n*-channel GaN MOSFETs, which are promising high-voltage devices.

The tremendous potential of these transistors has spurred extensive studies of interface properties, with investigations of *n*-type GaN capacitors with a SiO_2 dielectric uncovering a gallium oxide interfacial layer that reduces the electron trap density near the conduction band to below 10^{11} cm^{-2} eV^{-1}. Thanks to this, mobility in *n*-channel GaN MOSFETs is more than 100 cm^2 V^{-1} s^{-1}.

However, the reliability of these transistors is impaired by a high density of hole traps near the valence band edge. The density of these traps is so high that *p*-type GaN metal-oxide-semiconductor (MOS) capacitors tend to exhibit insufficient hole accumulation, and the threshold voltage of MOSFETs shifts during switching. Consequently, to develop highly reliable GaN MOSFETs, it is crucial to quash the density of these hole traps – a task that must begin by uncovering their origin.

The team from Osaka have devoted much effort to this issue. Previous investigations include the use of sub- and above-bandgap illumination to reveal that hole traps have a variety of origins.

Now they are adding to this body of work by studying hole trap generation in GaN MOS structures, with investigations considering a variety of post-deposition annealing conditions for the fabrication of *p*-GaN MOS capacitors.

To undertake this particular investigation, the team began by taking *n*-type GaN substrates, loading them into an MOCVD reactor, and depositing a silicon-doped GaN layer with a doping of 2 x 10^{18} cm^{-3}, followed by a pair of magnesium-doped GaN layers with doping concentrations of 3 x 10^{18} cm^{-3} and 2 x 10^{16} cm^{-3}. Following a wet clean, these samples were annealed under nitrogen for 20 minutes at 800 °C to activate magnesium dopants, prior to a second wet clean and the addition of a 20 nm-thick SiO_2 gate dielectric by plasma-enhanced CVD. The researchers completed fabrication of these capacitors with post-deposition annealing for 30 minutes, at temperatures ranging from 200 °C to 800 °C under either oxygen or nitrogen gas, before depositing nickel gate electrodes and aluminium back contacts.
Using the same procedure, the researchers also fabricated *n*-type GaN MOS capacitors to act as a control.

Comparing capacitance-voltage curves for both types of capacitor produced using an 800 °C post-deposition anneal under oxygen revealed a small hysteresis for the *n*-type variant, and a large hysteresis for the *p*-type variant. According to the team, this shows that the *p*-type structure suffers from strong pinning, due to hole trapping at the MOS interface.

The researchers concluded that post-deposition annealing at 800 °C is ineffective at improving the interface in SiO_2/*p*-GaN MOS structures.

Capacitance-voltage plots were also compared for SiO_2/*p*-GaN MOS capacitors produced without annealing, and with annealing at 200 °C and 800 °C. All the samples produced a large hysteresis, but the one annealed at 200 °C exhibits successful hole accumulation.

To understand the role of the gas used for annealing, the researchers compared capacitance-voltage profiles of SiO_2/*p*-GaN MOS capacitors subjected to a post-deposition anneal under either oxygen or nitrogen at a range of temperatures: 200 °C, 400 °C, 600 °C and 800 °C.

Reseults revealed unusual electron accumulation under forward bias in the nitrogen-annealed samples, and no electron accumulation in oxygen-annealed variants. Regardless of the annealing gas, the team noted hole accumulation in samples with a post-deposition anneal at 200 °C. Higher annealing temperatures under both gases introduced a strong pinning of the surface potential, due to a high density of surface traps.

Following detailed analysis of the capacitance-voltage profiles, the team speculated that the hole trap that causes surface potential pinning is an interface defect, generated at an elevated temperature.

The researchers also noted the presence of high-density oxide traps, even in samples annealed at 200 °C, that trap holes after interface traps are filled.

The team will now focus on the origin of the oxide traps and their reduction.

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