SILICON SEMICONDUCTOR

Connecting the Silicon Semiconductor Community

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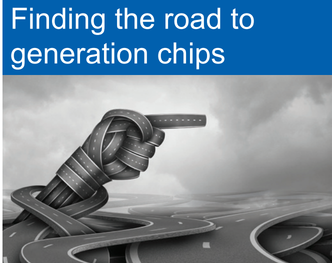
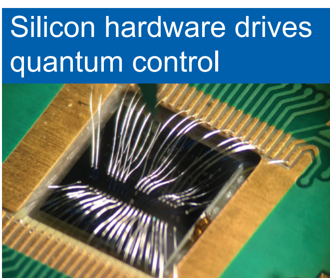
Secure IoT devices from chip to cloud

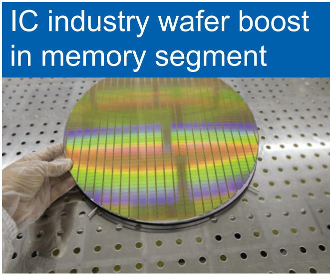
Finding the road to generation chips



Silicon hardware drives quantum control



IC industry wafer boost in memory segment



Ghent University: The future is optical

Brewer Science delivers next-gen DSA and WLP solutions

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Brewer Science is a global technology leader in developing and manufacturing innovative materials, and processes for the fabrication of semiconductors and microelectronic devices. In 1981, Brewer Science revolutionized lithography processes with its invention of Brewer Science® ARC® anti-reflective coatings. Today, we continue to expand our technology portfolio to include products that enable advanced lithography, 3-D integration, chemical and mechanical device protection, nanotechnology, and thin wafer handling.

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Brewer Science continues to revolutionize lithography technologies including anti-reflective coatings, DSA materials, EUV underlayers, and other key materials. Our line of products stretches across the whole spectrum of lithography wavelengths and is the most comprehensive product lineup in the industry. We are dedicated to pursuing the most advanced lithography technologies in the market today.

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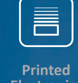
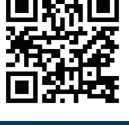
Lithography


Printed Electronics

Protective Coatings

Wafer-Level Packaging



editor's view

By Mark Andrews, Technical Editor

The future is in the chips

A TECHNOLOGY MAGAZINE saying that it is 'looking to the future' is no surprise. Technology ***is*** the future; every edition looks that direction. Our focus is always about pushing boundaries while avoiding setbacks and detours. The thing is, getting to 'the future' for silicon device manufacturers used to be a comparatively simple exercise in scaling. How the times have changed!

For the silicon semiconductor industry, delivering greater performance at lower costs used to rely upon traditional geometric scaling principles even if the details involved many twists and turns. But we knew the way. Getting from 48/45nm features to 28nm was straightforward: decrease transistor element sizes 'x' amount using processes well established at the last node, plus some innovations here and there. While this observation dramatically oversimplifies complex lithographic feats du jour, new materials exactness and myriad other complications, transitioning meant using know technologies to deliver what customers wanted to buy: greater densities, faster speeds, superior efficiencies and overall greater performance.

Today, all bets are off when it comes to tried and true approaches to achieving 7/5nm device geometries. Getting to 14nm and then 10nm was challenging enough. That journey took new approaches and increasingly complex photo lithographic feats that today involve 3D structures such a FinFETs, double- and quadruple multi pattern immersion lithography, wafer bonding and obsessively demanding material purity standards.

For years the industry's largest device fabs including Intel, Samsung, TSMC, Globalfoundries and others pinned future hopes to the development and roll-out of extreme ultraviolet (EUV) lithography. But enabling EUV to meet the demands of highly-demanding customers has dragged on. For years. Not enough power; problematic pellicles; and so on. Delays were followed by more delays; major foundries postponed their switch-over. And by the way, did we mention the current price for a single EUV tool? About USD $100 million. Ouch….

In this Silicon Semiconductor we explore how different companies are looking to the future and seeing it not as a destination with one road, but as having many different means to arrive at different places. On page 22 we explore solutions for many device types and alternative technologies beyond CMOS scaling. Our cover feature on page 16 looks at the work of Brewer Science and two product lines supporting temporary wafer bonding (TWB) and their breakthrough work in directed self-assembly (DSA).

Join us in the future. There are many roads, and a ticket doesn't require a billion-euro fab.

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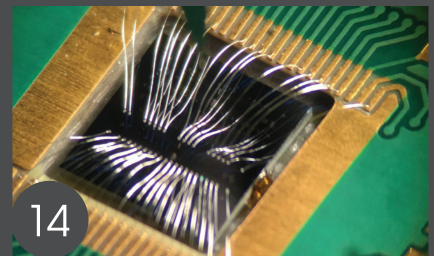
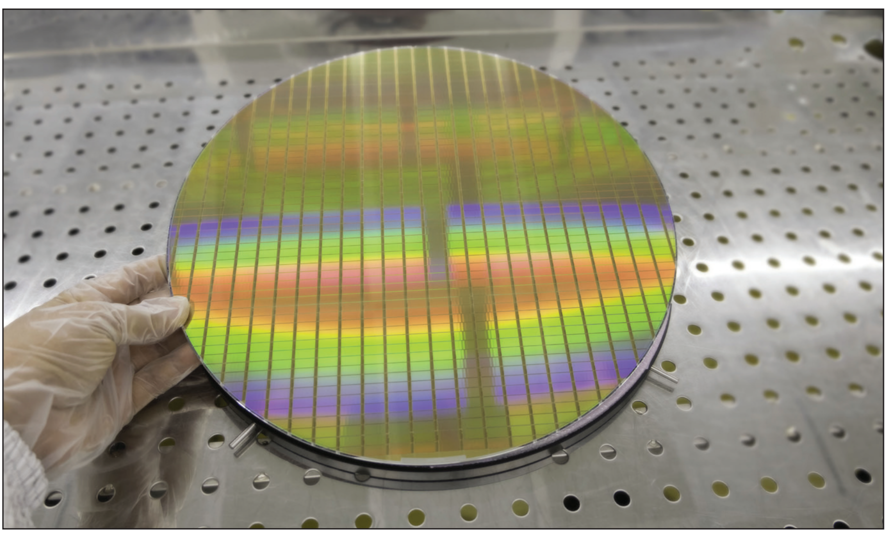
Arm is the critical player in the global semiconductor market. While it does not manufacture its own chips, its processor designs enable approximately 100 billion silicon chips, powering products from the sensor, to the smartphone to supercomputers



IC industry gets wafer boost in memory segment



IC INDUSTRY wafer capacity, specifically in the memory segment, was inadequate to meet demand throughout 2017. However, with Samsung, SK Hynix, Micron, Intel, Toshiba/WD, and XMC/ Yangtze River Storage Technology planning to significantly ramp up 3D NAND flash capacity over the next few years, and Samsung and SK Hynix boosting DRAM capacity this year and next, what does this mean for total industry capacity growth?

In its 2018-2022 Global Wafer Capacity report, IC Insights shows that new manufacturing lines are expected to boost industry capacity 8 percent in both 2018 and 2019 (Figure 1). From 2017-2022, annual growth in IC industry capacity is forecast to average 6.0 percent compared to 4.8 percent average growth from 2012-2017.

Large swings in the addition or contraction of wafer capacity by the industry appear to be moderating. Since 2010, annual changes in wafer capacity volume have been in the relatively narrow range of 2-8 percent, with the largest year-to-year difference being just three percentage points. This suggests that IC manufacturers are better today than in years past about trying to match supply with demand. It's still an incredibly difficult task for companies to gauge how much capacity will be needed to meet demand from customers, especially given the time it takes a company to move from the decision to build a new fab to that fab being ready for mass production.

Many companies, DRAM and NAND flash suppliers, have become much more active with new fab construction and expansion projects at existing fabs. This surge in activity comes after four years (2014-2017) when capacity growth lagged wafer start volume increases. During the past few years, IC producers have worked to increase utilization rates from the low levels in 2012-2013. If all the new fab capacity expected to be brought on-line in 2019 happens as planned, the volume of capacity added that year will approach the record set in 2007.

Figure 2 shows more that 18 million wafers per year of new capacity is expected to be added in 2019, and this number even assumes some of the massive DRAM and NAND fabs being built by Chinese companies will not be carried out quite as aggressively as has been advertised. IC Insights believes that construction of these China-owned fabs is progressing slower than planned.

Tokyo Electron begins accepting orders for dry etch system

TOKYO ELECTRON (TEL) announced before Christmas that it is now accepting orders for the Betelex 1800 PICP, a dry etch system capable of processing the 6th generation glass substrates (1500 mm x 1850 mm). The Betelex 1800 PICP supports up to five chambers featuring a Planar Inductively Coupled Plasma (PICPTM)* mode for high resolution processes.

The Flat Panel Display (FPD) industry is pushing screen resolutions to the levels of 600, 700, and even 800 pixels per inch (ppi) for smartphones and similar devices. At the same time, demand for augmented reality (AR) and virtual reality (VR) applications that require a resolution of 1,000 ppi or more is growing. The technology shift from LCD to OELD is also expected to generate new innovations in such areas as flexible displays and advanced user interfaces.

As the industry environment calls for greater sophistication in process performance and process steps, dry etch systems are required to achieve even better productivity than before.

The Betelex 1800 PICP supports up to five process chambers, enabling a significant productivity increase over the previous model which supported up to three chambers. Because the same level of production volume can be maintained with fewer mainframes, the Betelex 1800 PICP can reduce the overall system footprint and associated facility cost to customers. The Betelex 1800 PICP has already been receiving favourable reviews from some early customers.

"We've developed the Betelex 1800 PICP by building on the performance of our previous equipment at the customers' production lines," said Tsuguhiko Matsuura, Vice President and General Manager, FPDBU at TEL. "We are confident that the system will help significantly improve the manufacturing yield of our customers' most advanced processes and boost their productivity."

** Planar Inductively Coupled Plasma (PICP): A technological concept for generating highly uniform, high-density plasma on a panel substrate.*

ASML exceeds €9 billion sales 2017

IN JANUARY, ASML Holding N.V. published its 2017 fourth-quarter and full-year results. The 2017 figures show net sales EUR 9.05 billion, and net income EUR 2.1 billion.

For the first-quarter of 2018, ASML expects net sales around EUR 2.2 billion, a gross margin between 47 and 48 percent, R&D costs of about EUR 350 million, SG&A costs of about EUR 115 million.

ASML expects Q1 2018 net sales around EUR 2.2 billion and a gross margin between 47 and 48 percent.

CEO Statement

"ASML generated record sales and net income in 2017, helped by a strong fourth quarter. Due to industry strength, some customers requested earlier shipments of their lithography systems, which we were able to accommodate. Earlier-than-expected revenue recognition of two Extreme Ultraviolet (EUV) systems contributed to the strong performance in the fourth quarter as well. With EUV sales crossing the 1.1-billion-euro mark, 2017 was the year in which preparations for inserting EUV into high-volume chip manufacturing shifted into a higher gear. This is underlined by orders for 10 more EUV systems in the fourth quarter. Sales of our Holistic Lithography and Installed Base Management products also showed significant growth in 2017," ASML President and Chief Executive Officer Peter Wennink said.

"These results reflect our technology leadership and the success of our comprehensive product portfolio as well as the strong growth fundamentals in our industry, which enable the continued innovation in personal electronics, artificial intelligence, cloud computing and mobility. For 2018 we expect continued solid growth of sales and profitability."

With a total of 161 new DUV systems shipped in 2017, a 21 percent increase from 2016, ASML's supply chain and factories were capable of significantly boosting output in reaction to increased customer demand, supporting fast ramps of advanced nodes in memory and logic. We also provided three customers with early-access versions of the TWINSCAN NXT:2000i, our most advanced immersion lithography system, for process development of next node devices. As a sign of the continuously increasing maturity of the NXT platform, the NXT:2000i system meets or exceeds all of its performance targets.
For 3D NAND customers, we expanded our options portfolio to improve focus performance on high-topography wafers and handle strongly-warped wafers, both of which are typical for this application.

Our Holistic Lithography product portfolio showed growth in all product categories: computational lithography software products, metrology and inspection systems and process window control software products. ASML also broadened its product offering with the creation of an e-beam-based pattern fidelity metrology system, ePfm5, and shipped the first HMI eXplore 6000 EUV reticle defect inspection system.

ASML shipped 10 EUV systems to multiple customers in support of their plans to use the technology in high-volume manufacturing starting in 2018 and 2019, up from 4 shipments in 2016. ASML also demonstrated a number of technology milestones, achieving a throughput of 125 wafers per hour, demonstrating a full-size, defect-free EUV pellicle, and achieving EUV-to-DUV immersion overlay of 2 nanometers, which is in line with the requirement for the 5 nanometer logic node. Installed Base Management sales surpassed EUR 2.6 billion in 2017, an increase of more than 25 percent over the prior year.

ASML continued to support China's expanding semiconductor industry. Our system sales to China grew by more than 20 percent in 2017. Alongside shipments to mainland fabs operated by non-Chinese customers, we are planning to ship to five domestic Chinese customers in 2018.

Veeco, AMEC, and SGL settle patent litigation

VEECO INSTRUMENTS, Advanced Micro-Fabrication Equipment, and SGL Carbon SE, have announced that they have mutually agreed to settle the pending litigation among the parties and to amicably resolve all pending disputes, including AMEC's lawsuit against Veeco before the Fujian High Court in China and Veeco's lawsuit against SGL before the U.S. District Court for the Eastern District of New York.

John R. Peeler, Chairman and CEO of Veeco, commented:
"I am pleased to report that we have reached a mutually agreed settlement of the pending IP disputes and we are back to normal business operations in our MOCVD business." AMEC's Chairman and CEO, Dr. Gerald Yin, stated: "This settlement is a good example of how competitors can resolve IP matters for the benefit of their global customer base."

As part of the settlement, all legal actions worldwide (in court, patent offices and otherwise), between Veeco, AMEC and SGL, and their affiliates, will be dismissed and/or otherwise withdrawn. As a result, all business processes, including sales, service and importation, will be continued.

Terms of the settlement were not disclosed.

Technical trends demand advanced equipment solutions

ACCORDING to "Global Semiconductor Equipment: Markets, Market Shares, Market Forecasts," the front-end equipment market, which grew 18.4% in 2014 based on revenues converted to dollars, the 2015 market decreased 2.4%. A number of technical and operational trends within the semiconductor manufacturing industry are strengthening the need for more effective advanced equipment solutions.

These trends include:

Development of Smaller Semiconductor Features. The development of smaller features, now as small as 20nm in production and 10nm in R&D, enables semiconductor manufacturers to produce larger numbers of circuits per wafer and to achieve higher circuit performance.

Transition to 3D device structures. Foundries are adopting 3D FinFET transistors starting at 14/16 nm technology nodes to get improved performance and use less power in 1x technology nodes. Memory makers will move to 3D NAND and vertical structures for next generation NAND technology

Transition to 3D Integration Technology. Three-dimensional (3D) integration of active devices, directly connecting multiple IC chips, offers many benefits, including power efficiency, performance enhancements, significant product miniaturization, and cost reduction. It provides an additional way to extend Moore's law beyond spending ever-increasing efforts to shrink feature sizes. A critical element in enabling 3D integration is the Through-Silicon Via (TSV); TSV provides the high-bandwidth interconnection between stacked chips. The TSV process is beginning to enter production. In the case of TSV, since multiple chips are connected, the process must achieve and maintain very high yield levels in order to be economically viable.

Shortening of Technology Life Cycles. The technology life cycle of integrated circuits continues to shorten as

semiconductor manufacturers strive to adopt new processes that allow a faster transition to smaller, faster and more complex devices. In the past, the technology life cycle was approximately three years; it is now only two years.

New materials. Copper metal layers continue to be the key material for the back end of line for advanced integrated circuits in order to increase performance and reduce the cost of integrated circuits. The Industry is continuously searching directions to reduce the effective K of the low K materials and to reduce the barrier thickness and material types.

These changes require new processing and metrology equipment and thus represents challenging developments for the semiconductor manufacturing industry. In addition, in order to overcome limitations in the continued shrink of transistor dimensions, leading edge integrated circuit manufacturers are introducing new materials in the transistor gate stack. The adoption of high-k dielectrics is a key element for gate control in the most advanced technology nodes of 28nm, 20nm and 14nm currently in production, while R&D work to implement the next gate control material being done with III-IV materials. These new materials, combined with metal layers, require new processing and metrology equipment and thus represent a challenging development for the semiconductor manufacturing industry. Increasing use of multi patterning lithography. The continuous need for scaling to meet reduced transistor costs combined with delays in EUV lithography is pushing the industry to develop alternative lithography techniques such as multi patterning, DSA and E-Beam. These alternative technologies are increasing the Etch and CMP process steps and thus increasing the process control and metrology steps in these areas accordingly.

Increase in Foundry Manufacturing. Because of the rising investment needed for semiconductor process development and production as well as the proliferation of different types of semiconductors, semiconductor manufacturing is increasingly being outsourced to large semiconductor contract manufacturers, or foundries. A foundry typically runs several different processes and makes hundreds to thousands of different semiconductor product types in one facility, making the maintenance of a constant high production yield and overall equipment efficiency more difficult to achieve. This trend of shifting to foundries for manufacturing needs has progressed even further during recent years.

This report forecasts for all WFE equipment 2012-2018. Market shares for 2015. Profiles of all equipment vendors.

GF 45nm RF SOI ready for volume production

GLOBALFOUNDRIES has announced that its 45nm RF SOI (45RFSOI) technology platform has been qualified and is ready for volume production. Several customers are currently engaged for this advanced RF SOI process, which is targeted for 5G millimeter-wave (mmWave) front-end module (FEM) applications, including smartphones and next-generation mmWave beamforming systems in future base stations.

As next-generation systems move to frequencies above 24GHz, higher performance RF silicon solutions are required to exploit the large available bandwidth in the mmWave spectrum. GF's 45RFSOI platform is optimized for beam forming FEMs, with features that improve RF performance through combining high-frequency transistors, high-resistivity silicon-on-insulator (SOI) substrates and ultra-thick copper wiring.

Moreover, the SOI technology enables easy integration of power amplifiers, switches, LNAs, phase shifters, up/down converters and VCO/PLLs that lowers cost, size and power compared to competing technologies targeting tomorrow's multi-gigabit-per-second communication systems, including internet broadband satellite, smartphones and 5G infrastructure.

"GF's leadership in RF SOI solutions makes the company a perfect strategic partner for Peregrine's next generation of RF SOI technologies," said Jim Cable, Chairman and CTO of Peregrine Semiconductor. "It enables us to create RF solutions that provide our customers with new levels of product performance, reliability and scalability, and it allows us to push the envelope of integrated RF front-end innovation for evolving mmWave applications and emerging 5G markets."

"To bring 5G into the future, mmWave innovations are needed for allocating more bandwidth to deliver faster, higher-quality video, and multimedia content and services," Bob Donahue, CEO of Anokiwave. "GF's RF SOI technology leadership and 45RFSOI platform enables Anokiwave to develop differentiated solutions designed to operate between the mmWave and sub-6GHz frequency band for high-speed wireless communications and networks."

"GF continues to expand its RF capabilities and portfolio to provide competitive RF SOI advantages and manufacturing excellence that will enable our customers to play a critical role in bringing 5G devices and networks to real-world environments," said Bami Bastani, senior vice president of the RF Business Unit at GF. "Our 45RFSOI is an ideal technology for customers that are looking to deliver the highest- performing mmWave solutions that will handle demanding performance requirements in next-generation mobile and 5G communications."

GF's RF SOI solutions are part of the company's vision to develop and deliver the next wave of 5G technology aimed at enabling connected intelligence for next-generation devices, networks and wired/wireless systems. GF has a successful track record in manufacturing RF SOI solutions at its 300mm production line in East Fishkill, N.Y. Customers can now start optimizing their chip designs to develop differentiated solutions for high performance in the RF front end for 5G and mmWave applications.

Amphion video decoder IP for SoC implementation update

AMPHION SEMICONDUCTOR, a video codec silicon IP provider, has announced the release of the latest version of its successful, 'Malone' video decoder IP core optimized for SoC implementation.

Architectural optimizations have enabled Amphion's video SoC experts to realize further reductions in the size of the core area while maintaining the performance necessary to support the latest resolution and frame rate demands.
In addition to supporting all legacy formats, the CS8141 version of the Malone video decoder supports the very popular HEVC and VP9 formats in a single core. VP9 is supported for Profile 0 and Profile 2 at Level 5.1, giving up to 12-bit color depth and covering resolutions and frame rates up to 4Kp60.

Furthermore, for applications that require it, the core can be configured for frame rates of up to 120fps and image resolutions of up to 8K. The Malone family of advanced video decode cores have been licensed by many semiconductor and SoC companies. Due to the modular nature of the Malone architecture, customers can select which formats they need to support and at what resolution and frame rate and Amphion will configure a highly optimized solution which is minimal in both silicon area and power consumption for their application.

Infineon defies weaker US$ with strong momentum

INFINEON TECHNOLOGIES AG reported its results for the first quarter of the 2018 fiscal year (period ended 31 December 2017).

"Infineon has made a strong start to the new fiscal year, stated Dr. Reinhard Ploss, CEO of Infineon. Earnings and margin were better than forecast – despite the expected slight seasonal dip in revenues. The market for electro-mobility continues to drive growth. Infineon offers solutions for the entire range of drivetrain systems from hybrid to pure electric vehicles.

Moreover, we continue to benefit from excellent market conditions, which are driving high demand for power components used in applications across the board, such as solar power plants, especially in China, and for data centres. Operationally we are fully on track. We could still defy the headwind from the weaker US$ in the fiscal first quarter. Adjusted for the depreciation of the US$ from 1.15 to 1.25, our revenue momentum is unchanged, in terms of the Segment Result Margin even slightly better. However, we are unable to compensate a further depreciation of the US$ by another 8 percentage points, which negatively affects more than half of our revenues. As such, we currency-adjusted our outlook accordingly."

Compared to the preceding quarter, revenue declined by 2 percent to €1,775 million in the first quarter of the 2018 fiscal year. Revenue in the previous quarter had amounted to €1,820 million. Compared to the first quarter of the 2017 fiscal year, revenues increased by 8 percent. The Industrial Power Control (IPC), Power Management & Multimarket (PMM) and Chip Card & Security (CCS) segments all reported seasonal decreases, whereas the Automotive segment (ATV) recorded seasonally atypical revenue growth in line with expectations.

The gross margin in the first quarter came in at 36.4 percent, compared to 37.5 percent in the previous quarter. These figures include acquisition-related depreciation and amortization as well as other expenses attributable to the International Rectifier acquisition totaling €17 million. The adjusted gross margin

came in at 37.4 percent, compared with 38.6 percent in the preceding quarter. The first-quarter Segment Result amounted to €283 million, compared to €328 million in the fourth quarter of the previous fiscal year, with the Segment Result Margin declining from 18.0 percent to 15.9 percent.

The first-quarter non-segment result improved to a net loss of €35 million, compared to the net loss of €56 million reported for the preceding quarter. Of the first-quarter figure, €18 million related to the cost of goods sold, €16 million to selling, general and administrative expenses and €1 million to research and development expenses. The non-segment result for the first quarter includes €30 million of depreciation and amortization arising in conjunction with the purchase price allocation and other expenses for post-merger integration measures relating to International Rectifier.

Operating income for the first quarter totalled €248 million, compared to €272 million in the preceding quarter. Income from continuing operations for the three-month period improved to €206 million. The corresponding figure for the previous quarter had been €177 million. Income from discontinued operations remained stable at a negative amount of €1 million. Net income increased from €176 million to €205 million quarter-on-quarter. The first-quarter income tax expense amounted to €28 million, significantly lower than the tax expense of €84 million reported for the fourth quarter.

Earnings per share improved quarter-on-quarter from €0.16 to €0.18 (basic and diluted in each case). Adjusted earnings per share1 (diluted) amounted to €0.20, compared to €0.22 in the fourth quarter. For the purpose of calculating adjusted earnings per share (diluted), a number of items are eliminated, most notably acquisition-related depreciation/amortization and other expenses (net of tax) as well as valuation allowances on deferred tax assets.

Investments – which Infineon defines as the sum of purchases of property, plant and equipment, purchases of intangible assets and capitalized development costs – amounted to €293 million in the first quarter of the 2018 fiscal year, compared to €370 million in the preceding three-month period. Depreciation and amortization remained almost unchanged at €204 million, compared to the previous quarter's €205 million.

First-quarter free cash flow2 from continuing operations was a negative amount of €135 million, compared to a positive amount of €249 million one quarter earlier. Net cash provided by operating activities from continuing operations amounted to €158 million, compared to the previous quarter's €616 million.

The gross cash position at the end of the first quarter of the 2018 fiscal year amounted to €2,312 million, compared to €2,452 million at 30 September 2017. The net cash position amounted to €503 million, compared to €618 million three months earlier.

Provisions relating to Qimonda decreased from €33 million at 30 September 2017 to €32 million at 31 December 2017. These provisions are recognized for legal costs in conjunction with the defense against claims made by the Qimonda insolvency administrator and for residual liabilities related to Qimonda Dresden GmbH & Co. OHG. In the second quarter of the 2018 fiscal year, Infineon expects a quarter-on-quarter revenue increase of 4 percent (plus or minus 2 percentage points).

The forecast is based on an assumed exchange rate of US$1.25 to the euro for the remainder of the quarter. At the mid-point of revenue guidance, the Segment Result Margin is expected to come in at 16 percent.

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Columbia engineers

develop flexible lithium battery for wearable electronics

Shaped like a spine, new design enables remarkable flexibility, high energy density, and stable voltage no matter how it is flexed or twisted.

THE RAPID DEVELOPMENT of flexible and wearable electronics is giving rise to an exciting range of applications, from smart watches and flexible displays—such as smart phones, tablets, and TV—to smart fabrics, smart glass, transdermal patches, sensors, and more. With this rise, demand has increased for high-performance flexible batteries. Up to now, however, researchers have had difficulty obtaining both good flexibility and high energy density concurrently in lithium-ion batteries.

A team led by Yuan Yang, assistant professor of materials science and engineering in the department of applied physics and mathematics at Columbia Engineering, has developed a prototype that addresses this challenge: a Li-ion battery shaped like the human spine that allows remarkable flexibility, high energy density, and stable voltage no matter how it is flexed or twisted. The study is published today in Advanced Materials.

"The energy density of our prototype is one of the highest reported so far," says Yang. "We've developed a simple and scalable approach to fabricate a flexible spine-like lithium ion battery that has excellent electrochemical and mechanical properties. Our design is a very promising candidate as the first-generation, flexible, commercial lithium-ion battery. We are now optimizing the design and improving its performance."

Yang, whose group explores the composition and structure of battery materials to realize high performance, was inspired by the suppleness of the spine while doing sit-ups in the gym. The human spine is highly flexible and distortable as well as mechanically robust, as it contains soft marrow components that interconnect hard vertebra parts.

Yang used the spine model to design a battery with a similar structure. His prototype has a thick, rigid segment that stores energy by winding the electrodes ("vertebrae") around a thin, flexible part ("marrow") that connects the vertebra-like stacks of electrodes together. His design provides excellent flexibility for the whole battery.

"As the volume of the rigid electrode part is significantly larger than the flexible interconnection, the energy density of such a flexible battery can be greater than 85 percent of a battery in standard commercial packaging," Yang explains. "Because of the high proportion of the active materials in the whole structure, our spine-like battery shows very high energy density—higher than any other reports we are aware of. The battery also successfully survived a harsh dynamic mechanical load test because of our rational bio-inspired design."

Yang's team cut the conventional anode/separator/cathode/separator stacks into long strips with

The energy density of our prototype is one of the highest reported so far," says Yang. "We've developed a simple and scalable approach to fabricate a flexible spine-like lithium ion battery that has excellent electrochemical and mechanical properties

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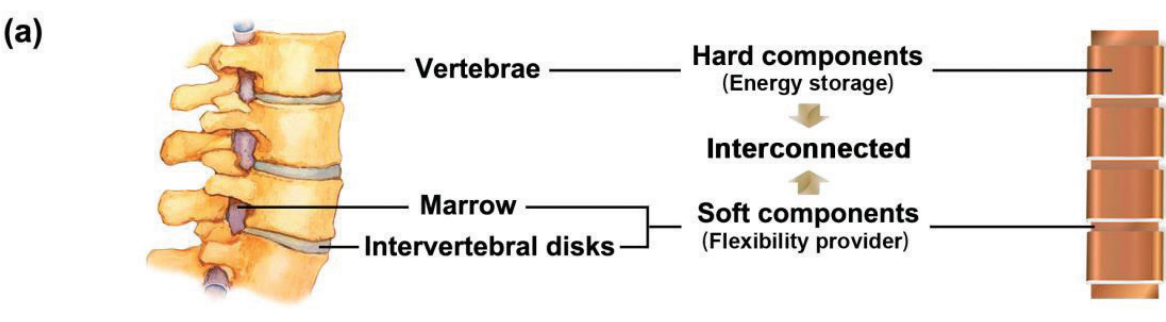

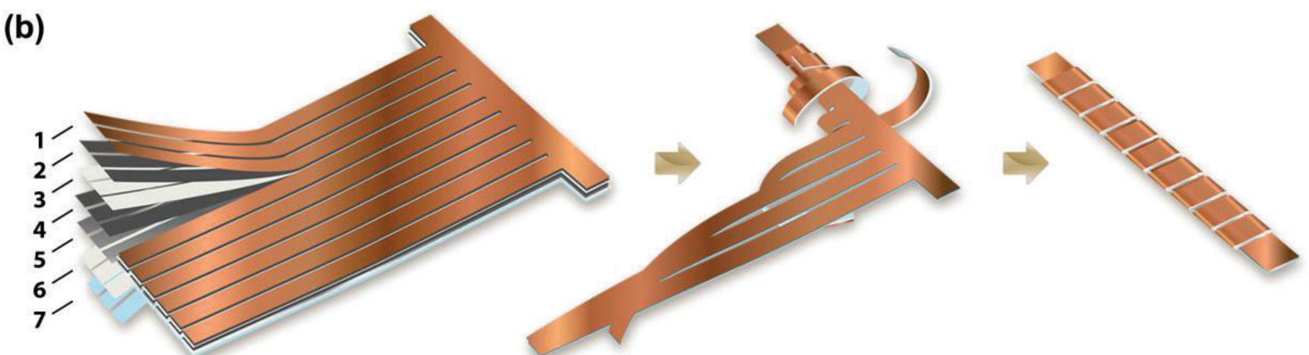

1-Copper current collectors, 2-Graphite anode, 3/6-Separator, 4-Lithium cobaltate cathode, 5-Aluminum current collectors, 7-Polyethylene supporting film.

multiple "branches" extending out 90 degrees from the "backbone." Then they wrapped each branch around the backbone to form thick stacks for storing energy, like vertebrae in a spine. With this integrated design, the battery's energy density is limited only by the longitudinal percentage of vertebra-like stacks compared to the whole length of the device, which can easily reach over 90 percent.

The battery shows stable capacity upon cycling, as well as a stable voltage profile no matter how it is flexed or twisted. After cycling, the team disassembled the battery to examine the morphology change of electrode materials. They found that the positive electrode was intact with no obvious cracking or peeling from the aluminum foil, confirming the mechanical stability of their design.

To further illustrate the flexibility of their design, the researchers continuously flexed or twisted the battery during discharge, finding that neither bending nor twisting interrupted the voltage curve. Even when the cell was continuously flexed and twisted during the whole discharge, the voltage profile remained. The battery in the flexed state was also cycled at higher current densities, and the capacity retention was quite high (84 percent at 3C, the charge in 1/3 of an hour). The battery also survived a continuous dynamic mechanical load test, rarely reported in earlier studies. "Our spine-like design is much more mechanically robust than are conventional designs," Yang says. "We anticipate that our bio-inspired, scalable method to fabricate flexible Li-ion batteries could greatly advance the commercialization of flexible devices."

About the Study

The study is titled "Bio-inspired, spine-like flexible rechargeable lithium-ion batteries with high energy density."

- The authors declare no financial or other conflicts of interest.

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New silicon hardware drives quantum control behaviour

A team led by Princeton University researchers has created an essential component for making quantum computers from an everyday material, silicon. The researchers demonstrated the ability to control the behavior of two silicon-based quantum bits, or qubits, paving the way for making complex, multi-qubit devices using technology that is less expensive and easier to manufacture than other approaches. Photo by David Zajac.

IN A MAJOR STEP toward making a quantum computer using everyday materials, a team led by researchers at Princeton University has constructed a key piece of silicon hardware capable of controlling quantum behaviour between two electrons with extremely high precision. The study was published in December 2017 in the journal Science.

The team constructed a gate that controls interactions between the electrons in a way that allows them to act as the quantum bits of information, or qubits, necessary for quantum computing. The demonstration of this nearly error-free, two-qubit gate is an important early step in building a more complex quantum computing device from silicon, the same material used in conventional computers and smartphones.
"We knew we needed to get this experiment to work if silicon-based technology was going to have a future in terms of scaling up and building a quantum computer," said Jason Petta, a professor of physics at Princeton University. "The creation of this high-fidelity two-qubit gate opens the door to larger scale experiments."

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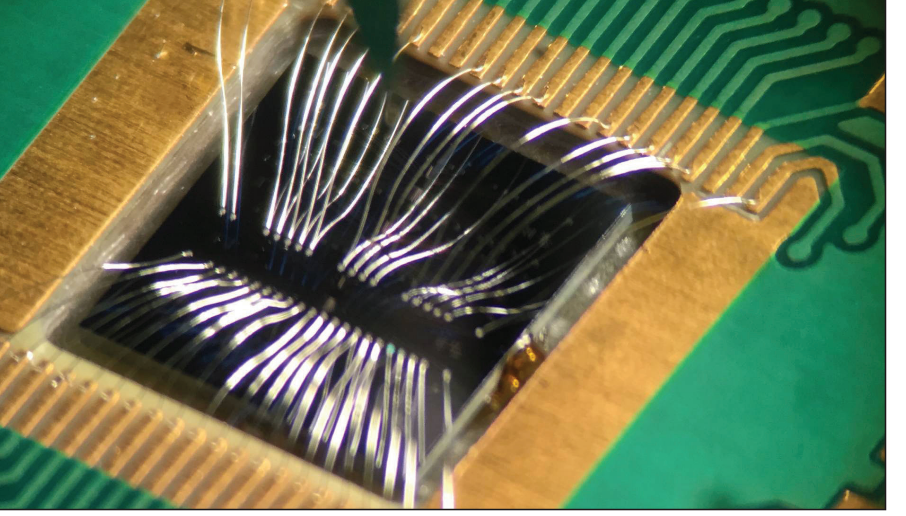
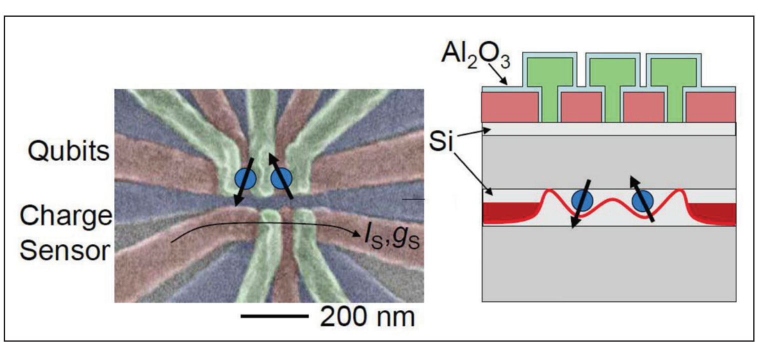


Silicon-based devices are likely to be less expensive and easier to manufacture than other technologies for achieving a quantum computer. Although other research groups and companies have announced quantum devices containing 50 or more qubits, those systems require exotic materials such as superconductors or charged atoms held in place by lasers.

Quantum computers can solve problems that are inaccessible with conventional computers. The devices may be able to factor extremely large numbers or find the optimal solutions for complex problems. They could also help researchers understand the physical properties of extremely small particles such as atoms and molecules, leading to advances in areas such as materials science and drug discovery.

The two-qubit silicon-based gate consists of two electrons (blue balls with arrows) in a layer of silicon (Si). By applying voltages through aluminum oxide (Al2O3)wires (red and green), the researchers trapped the electrons and coaxed quantum behaviors that

transform their spin properties into quantum bits of information, or qubits. The image on the left shows a scanning electron micrograph of the device, which is about 200 nanometers (nm) across. The image on the right is a diagram of the device from the side. Image credit Science/AAAS.



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Building a quantum computer requires researchers to create qubits and couple them to each other with high fidelity. Silicon-based quantum devices use a quantum property of electrons called "spin" to encode information. The spin can point either up or down in a manner analogous to the north and south poles of a magnet. In contrast, conventional computers work by manipulating the electron's negative charge. Achieving a high-performance, spin-based quantum device has been hampered by the fragility of spin states — they readily flip from up to down or vice versa unless they can be isolated in a very pure environment. By building the silicon quantum devices in Princeton's Quantum Device Nanofabrication Laboratory, the researchers were able to keep the spins coherent — that is, in their quantum states — for relatively long periods of time.

To construct the two-qubit gate, the researchers layered tiny aluminum wires onto a highly ordered silicon crystal. The wires deliver voltages that trap two single electrons, separated by an energy barrier, in a well-like structure called a double quantum dot.

By temporarily lowering the energy barrier, the researchers allow the electrons to share quantum information, creating a special quantum state called entanglement. These trapped and entangled electrons are now ready for use as qubits, which are like conventional computer bits but with superpowers: while a conventional bit can represent a zero or a 1, each qubit can be simultaneously a zero and a 1, greatly expanding the number of possible permutations that can be compared instantaneously. "The challenge is that it's very difficult to build artificial structures small enough to trap and control single electrons without destroying their long storage times," said David Zajac, a graduate student in physics at Princeton and first-author on the study. "This is the first demonstration of entanglement between two electron spins in silicon, a material known for providing one of the cleanest environments for electron spin states."

The researchers demonstrated that they can use the first qubit to control the second qubit, signifying that the structure functioned as a controlled NOT (CNOT) gate, which is the quantum version of a commonly used computer circuit component. The researchers control the behavior of the first qubit by applying a magnetic field. The gate produces a result based on the state of the first qubit: If the first spin is pointed up, then the second qubit's spin will flip, but if the first spin is down, the second one will not flip.

"The gate is basically saying it is only going to do something to one particle if the other particle is in a certain configuration," Petta said. "What happens to one particle depends on the other particle."
The researchers showed that they can maintain the electron spins in their quantum states with a fidelity exceeding 99 percent and that the gate works reliably to flip the spin of the second qubit about 75 percent of the time. The technology has the potential to scale to more qubits with even lower error rates, according to the researchers.

"This work stands out in a worldwide race to demonstrate the CNOT gate, a fundamental building block for quantum computation, in silicon-based qubits," said HongWen Jiang, a professor of physics and astronomy at the University of California-Los Angeles. "The error rate for the two-qubit operation is unambiguously benchmarked. It is particularly impressive that this extraordinarily difficult experiment, which requires a sophisticated device fabrication and an exquisite control of quantum states, is done in a university lab consisting of only a few researchers." Additional researchers at Princeton are graduate student Felix Borjans and associate research scholar Anthony Sigillito. The team included input on the theory aspects of the work by Jacob Taylor, a professor at the Joint Quantum Institute and Joint Center for Quantum Information and Computer Science at the National Institute of Standards and Technology and the University of Maryland, and Maximilian Russ and Guido Burkard at the University of Konstanz in Germany.

Research was sponsored by U.S. Army Research Office grant W911NF-15-1-0149, the Gordon and Betty Moore Foundation's EPiQS Initiative through grant GBMF4535, and National Science Foundation grant DMR-1409556. Devices were fabricated in the Princeton University Quantum Device Nanofabrication Laboratory.

The study, "Resonantly driven CNOT gate for electron spins," by David M. Zajac, Anthony J. Sigillito, Maximilian Russ, Felix Borjans, Jacob M. Taylor, Guido Burkard and Jason R. Petta was published online in the journal Science on Dec. 7, 2017.

Brewer Science

delivers next-gen DSA and WLP solutions

Traditional CMOS scaling faces compound lithographic challenges at each new node. Brewer Science's materials experts are reducing complexities and improving performance through new directed self-assembly innovations, while enabling packaging advancements with its temporary wafer bonding portfolio for WLP. Whichever direction the industry pivots, Brewer Science offers solutions.

THE ROAD to next generation semiconductors becomes increasingly complicated at each new node. Geometric CMOS scaling worked well through 28nm, but today's 14/10nm devices typically rely on double- or quadruple-patterning solutions plus a litany of other complex techniques to create transistor elements, manage edge roughness and control pitch. Getting smaller isn't getting any easier.

Major semiconductor manufacturers pursuing greater density, high efficiency and better performance have pinned their hopes to extreme ultraviolet (EUV) lithography for transistors below 7nm. But development complications have repeatedly pushed the introduction of EUV to succeeding generations.

Ram Trichur of Brewer Science

Intel, Samsung, TSMC and other major fabs have indicated they will introduce EUV at 7-5nm by the end of this decade. But what comes after 5nm? Will it be affordable and flexible enough to fit wide-ranging circuit requirements? This is uncharted territory where no one can risk multimillion, let alone multibillion, dollar/pound/euro investments.

Many manufacturers are actively seeking alternatives to EUV for myriad reasons including the fact that cost/benefit ratios that have favored incremental lithographic technique enhancements are getting much harder to calculate. As sophisticated tools have driven costs up sharply, manufacturers need mutigenerational benefits to commit resources. Many seek alternatives to market requirements or have explored alternative scenarios to leverage existing capital investments. Some shifted part of their capacity to manufacturing micro electromechanical systems (MEMS) devices that do not depend on 300mm wafer fabs or the most advanced process technology, showing it is possible to create value and strong revenue streams while diversifying product portfolios.

Brewer Science (Rolla, Missouri and worldwide) has been supporting advanced lithographic materials and process technology requirements since 1981 when company founder and CEO Terry Brewer created and delivered antireflective coatings that enabled new lithographic solutions—foundations of today's industry standards. The company continues to pioneer new technologies, including its significant work with temporary wafer bonding (TWB) and debonding solutions.

"In backend manufacturing, we look for technical problems where the material solutions for existing requirements do not meet the future needs of our customers. We offer advanced material solutions that

go beyond present day customer requirements by also offering a clear advantage in terms of process simplification, yield improvement and/or throughput enhancement," said Ram Trichur, Director of Wafer Level Packaging Business Development at Brewer Science Inc.

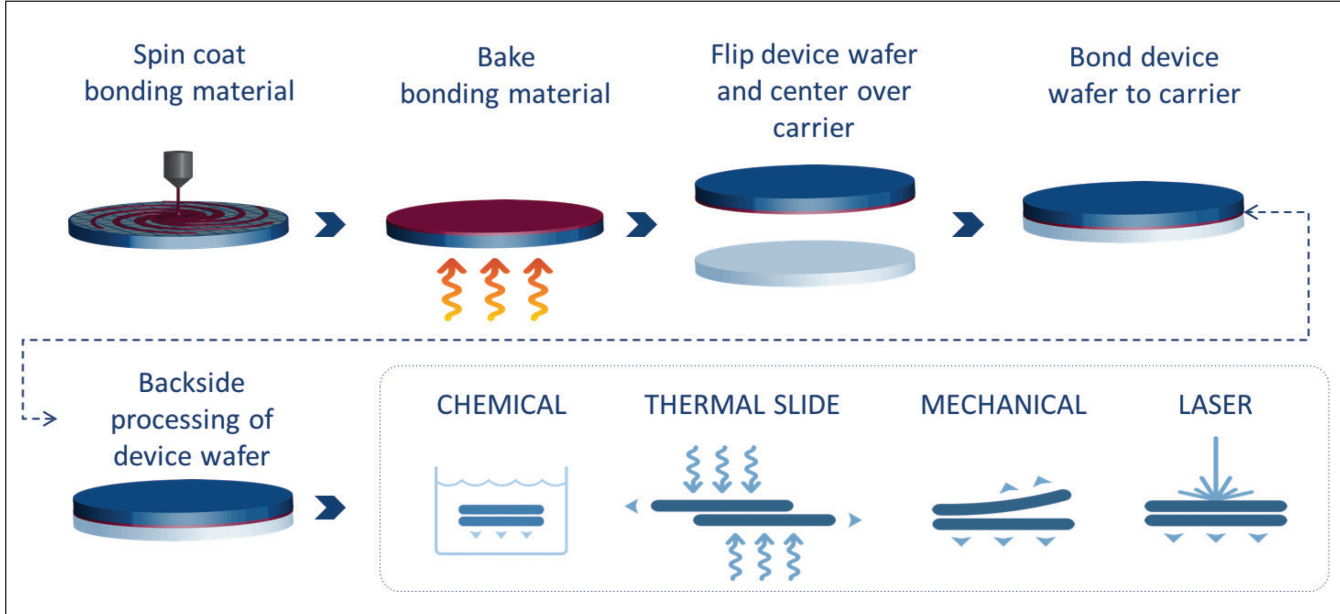
Brewer Science's temporary bonding and debonding techniques are especially applicable in fan-out wafer-level packaging (FOWLP). While the 'chip-first' approach has been in high volume manufacturing for some while, the 'chip-last' approach is still developing. Brewer Science sees many of its product solutions as offering a complete range of options for customers, whichever approach they are taking.

TWB has become the technology of choice for most applications in which a 300mm silicon wafer is thinned, flipped and temporarily mounted on a carrier after which its backside is further processed on the road to producing 3D integrated circuits. Creating and handling thinned wafers is a challenging process; however, thin wafer-based devices allow for better heat dissipation, reduced form factors, greater performance and less power consumption. But thinning involves risks including fragility, stress leading to warpage or cracks, and thermal expansion match issues. After thinned wafers receive backside processing, the temporary mount needs to be smoothly dislodged (debonded) and device wafers need to be cleaned before subsequent processing. Manufacturers typically utilize one of three main approaches to safely and cleanly dislodge a temporary bond: thermal slide, mechanical or laser.

Brewer Science has supported temporary bonding/ debonding requirements across multiple device generations and is one of the few companies to support every major type of physical debonding approach. Their products continue to evolve and now include fourth generation solutions for laser systems; they have succeeded in raising the temperature range of these processes up to 350° C.

"We have almost 15 years of experience in temporary bonding materials development and commercialization for the manufacturing of 2.5D, 3D, compound semiconductor, fan-out and other process flows. We realized very early that one product or even one platform of temporary bonding materials may not

Brewer Science's manufacturing automation is key to ensuring quality is maintained.



TWB process flow showing all major methods of temporary bond release.

be suitable for all of the processes used in advanced packaging applications. Each process flow or device type has a unique set of requirements, and we offer a broad portfolio of bonding materials and release layers designed to support these individual processes. This approach results in maximized customer benefits in terms of delivering simple processes with high yield and low cost of ownership," said Trichur.

The company is seeing growing interest in the latest generation of tools, especially across Asia and most notably in China. While all customers see benefits, some report rather remarkable results, especially when they had previous solutions that were not delivering as needed.

"All of our customers benefit from the advances we deliver, yet some have particularly striking success stories. A manufacturer that was producing compound semiconductor devices and bonding with wax materials had a total yield loss of around 30 percent during backside processing due to the poor thermal and mechanical properties of wax. We introduced a new temporary bonding material, and their yields subsequently increased to over 99%," said Trichur.

> Historically, the industry has relied on equipment enhancements to reach the next technology node. Now, materials solutions are stepping in to provide that edge and extend tool capabilities. The OptiLign™ product family is an example of this paradigm shift

Other new device architectures are key to many companies' strategies to either delay or bypass the need for expensive EUV transitions. A new technology seeing widespread development work on the road to commercialization is directed self-assembly (DSA). Brewer Science partnered with Arkema (Grenoble, France) in 2015 to bring first-generation DSA materials to the commercial marketplace. Arkema is a high-performance materials specialist with a global presence and 2016 sales of 7.5 billion euro. The companies' collective goal is to ultimately support device geometries down to 5nm and below so that regardless of the path to next-generation devices that manufacturers choose, Brewer Science will have an advanced solution enabling faster throughput, higher yield and superior performance.

At the SPIE Advanced Lithography 2018 conference (February 2018), Brewer Science announced that it had achieved a new milestone in the support of commercial-quality DSA materials. Brewer Science's new OptiLign™ system includes three DSA materials: block copolymers, neutral layers and guiding layers that Brewer Science and Arkema believe provide a cost-effective path to advanced node wafer patterning processes for feature sizes down to a 22nm pitch.

"Taking OptiLign materials from pilot line to commercial-scale production represents the next significant milestone in making DSA a viable option for

semiconductor manufacturing," said Dr. Srikanth (Sri) Kommu, executive director, Semiconductor Business, Brewer Science Inc. "Historically, the industry has relied on equipment enhancements to reach the next technology node. Now, materials solutions are stepping in to provide that edge and extend tool capabilities. The OptiLign product family is an example of this paradigm shift."

Brewer Science's OptiLign family of DSA products provides all the materials needed for self-assembly. Block copolymers define the pattern. Neutral layers allow the pattern to be formed on each layer. Lastly, guiding layers give the material directional orientation. All the materials are designed to work together for optimal performance, and are dependent on material and surface energy.

Through its partnership with Arkema, Brewer Science has tapped into a way to deliver DSA materials that allows for consistent feature sizes via a unique polymer production process. Critical to high-volume manufacturing is the fact that this new process enables the type of scaling needed to support an entire technology node, as well as unique polymer quality and reproducibility, all of which sets OptiLign materials apart from competing solutions.

Block copolymers (BCPs) are polymers containing two (or more) polymers joined together that will spontaneously segregate when coated and annealed on a neutral layer. The neutral layer has a surface energy that both blocks will adhere to equally; hence the name neutral layer. However, the features naturally created by BCP are random, so a "guide" is needed to make the BCP go where circuit designers wish.

There are many process flows for guiding the BCP, including creating physical features and aligning the BCP between them (graphoepitaxy), or treating the surface to create areas of the neutral layer that have a preference for one section of the BCP in order to align them (chemoepitaxy). Depending on the BCP and guiding method that are used, DSA can be used to create lines, holes, pillars, and other features.

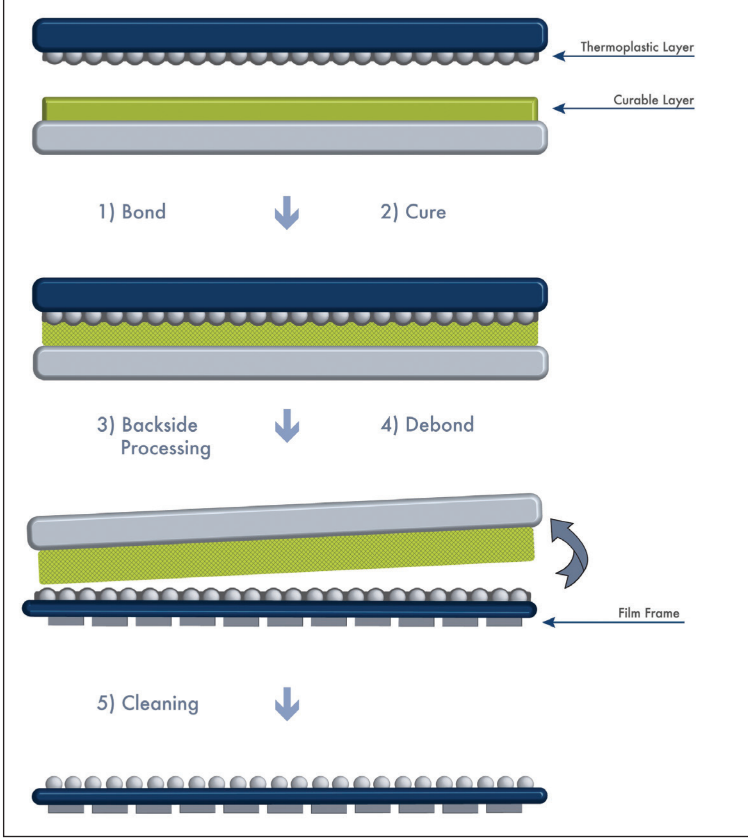
"Feature size is built into the molecular structure of the DSA materials and can vary from batch to batch, so securing a sub-nanometric reproducibility can be challenging," explained Dr. Ian Cayrefourcq, Director of Emerging Technologies, Arkema. "Arkema's special process for formulating large batches of polymers of the same size allows Brewer Science to supply a fab with consistent feature sizes for the technology node's life span."

In July 2017, Brewer Science announced that it had extended its relationship with Arkema to further work towards next-generation DSA materials. Brewer Science scientists have been able to reduce the feature size by 20% compared to the first-generation materials, another milestone towards the ultimate goal of supporting 5nm and smaller features. This benchmark is important since most industry experts agree that extending device scaling without relying on EUV or complex multi-patterning schemes is essential to any new technologies' ultimate success. And DSA offers even more benefits.

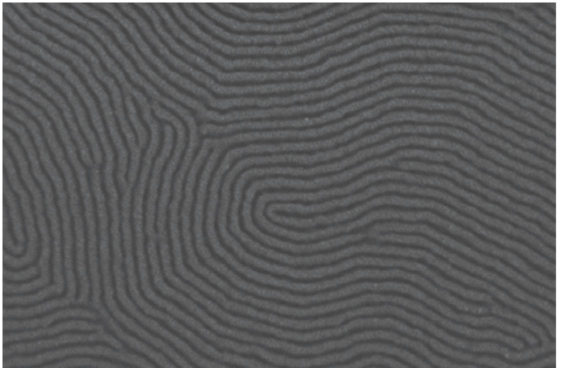
"DSA represents a lower-cost and higher-throughput solution over EUV, but another big cost advantage lies in the reduced mask requirements. DSA still needs lithography and etch processes, but these are lower cost compared to multiple patterning. EUV masks are a significant part of the EUV step cost. DSA also offers a technical advantage in that it can reach lower feature sizes now (compared to) other patterning technologies," said Hao Xu, Director of Semiconductor Business Development at Brewer Science.

Xu also believes that major fabs which have already committed to EUV may conclude that combining DSA with EUV will better support their ultimate goals.

"DSA and EUV are complementary because smaller pitches can be printed with EUV that are not accessible with immersion litho. Smaller pitches means two things: lower multiplication factors can be done with DSA, which leads to a lower possibility for defects. Also, there is the possibility of eliminating the trim etch step in the chemoepitaxy flow when using EUV. EUV can also provide graphoepitaxy templates for contact hole multiplication. It is also important to note that because of the resolution limitations of



Brewer Science Gen4 TB-DB process flow.



9nm lines formed using Brewer Science's next-generation OptiLign™ DSA materials.

EUV at smaller nodes, it is possible that DSA will help stretch out the timing for, or even eliminate, the need for high-NA (numerical aperture) EUV tools," Xu added.

Conclusion

Brewer Science enabled key developments in semiconductor photolithography with its introduction of antireflective coatings. The company grew and expanded to offer a wide range of advanced solutions for global semiconductor manufacturing. Today, Brewer Science products and services support all major approaches to advanced lithography, thin-wafer handling and 3D integration as well as chemical and mechanical device protection and products based on nanotechnology. In its quest to support next-generational / emerging technologies, Brewer Science enables 3D advanced semiconductors through its temporary wafer bonding (TWB) and debonding product lines.

Its latest Gen4 solutions for laser-based applications have elevated working temperatures to 350° C. Recognizing the potential of directed self-assembly (DSA) to revolutionize advanced device fabrication, Brewer Science partnered with Arkema in 2015 to introduce commercial-ready OptiLign™ materials for DSA features down to 22nm pitch.

That partnership, extended in 2017, is positioned to continue innovation with next-generation solutions for even smaller DSA features; on-going work targets supporting devices to 5nm and below. As manufacturers seek alternatives to multi-pattern lithography that are less complex and costly, or for those seeking to delay or augment extreme ultraviolet (EUV) lithography, Brewer Science offers alternatives that extend device scaling while reducing costs, increasing performance and simplifying complex advanced node manufacturing.

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- SEMI Europe Award Ceremony
- Lucky Draw

Speakers' Outline

- David Bloss, VP, Technology Manufacturing Group, Intel
- Holger Blume, Professor, University of Hanover
- Leo Clancy, Head of Technology, Consumer & Business Services, IDA Ireland
- Jean-Frederic Clerc, Deputy CEO & CTO, CEA Tech
- Kevin Cooney, Senior VP & Managing Director, Global CIO, Xilinx EMEA,
- Jean-Christophe Eloy, CEO, Yole Développement
- Ann-Charlotte Johannesson, CEO, CEI-Europe AB
- Cheryl Miller, Founder/Executive Director, Digital Leadership Institute
- Mick A Morris, Director AMBER Research Centre, Professor of Surface & Interface Chemistry, Trinity College Dublin
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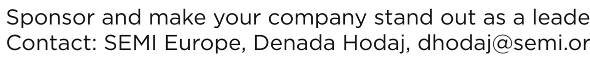


Finding the road
to next-gen chips

New transistor and IC technologies are rising to address the issues of complexity, cost and risk as manufacturers and researchers alike look beyond conventional CMOS device scaling evolution. Multiple manufacturers and researchers are seeking new paths and innovating new processes and materials to find lower cost, higher performing solutions for next-generation chips – Mark Andrews explores several leading and promising avenues for devices below 10nm.

Some of the world's largest semiconductor manufacturers, fabless design houses, startups and materials innovators all share a common goal: create paths to next-generation device technologies that reduce complexity and cost while delivering better performance.

The search for alternatives to existing scaling roadmaps is seen as essential by growing numbers of supply chain industry experts who believe that costs and complexities have grown to the point that only the largest fabs and device makers can compete. While global fab leaders can benefit from multi-billion dollar investments tied to their unique product road maps, opportunities have grown for other technologies; researchers are constantly seeking alternatives and novel approaches that avoid IP and patent issues while offering means to create faster, secure technologies.

Micro electromechanical system (MEMS) sensors exemplify advanced technology untethered to the costs and volumes of 300mm fabs. MEMS designs do not rely on cutting edge hardware, but instead often utilize legacy 200mm technologies including refurbished tools and well established fab techniques. Such fabs can find ample reservoirs of quality, trained operators and service experts anxious to get into a new game.

MEMS technology has amply demonstrated that a major new market does not necessarily require the latest transistor technology wedded to 300mm wafers. The MEMS market took-off with the advent of smartphones in 2007. Today, MEMS growth is pegged as much on new applications including drones and IoT network devices as it is on smartphones. MEMS high-end sensors (HES) support industrial and commercial requirements along with virtual assistants and other end use products that did not exist five years ago. The ideal wafer size for MEMS is presently 200mm, which has led to six new 200mm wafer fabs being built in China to satisfy global capacity requirements.

Many experts see node migrations as moving horizontally or vertically toward 3D designs before large scale adoption of extreme ultraviolet (EUV) lithography that manufacturers such as Intel, Samsung and TSMC have predicted will occur later this decade. Many expect significant improvements at 7nm compared to immediately preceding nodes, which may delay the need for 5nm devices until late in the 2020s. Manufacturers are also expected to create hybrid technologies that incorporate any number of non-traditional approaches including carbon nanowires, fully-depleted silicon on insulator (FDSOI), and different types of wafer bonding. We can expect multiple iterations of existing FinFET and other 10nm architectures before the trek to 7/5nm commences en masse. Meanwhile, the researchers at CEA Leti report that their 3D stacking technology, CoolCube, has reached new performance milestones and that manufacturing partners for pilot production runs are now being sought. The CoolCube approach operates at lower temperatures compared to other bonding techniques, which better preserves transistor functionality during alignment and other processing steps. CoolCube attained offset pitches of 1nm or less in earlier production stages, alignment accuracy that alludes some higher temperature processes.

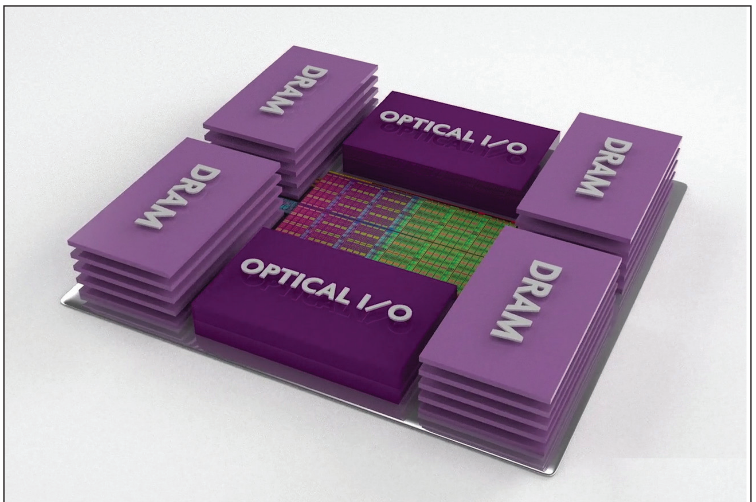
Source: EV Group (EV

Wafer-to-wafer bonding enabling next-generation chips

The drive to find new approaches to device evolution and scaling is also a product of the growing disparity between design and manufacturing capabilities. Traditional node scaling has become so expensive that it is no longer the 'go-to' solution for increasing density and performance. To paraphrase the old analogy: if you build it, will the market buy it?

Even the largest companies explore alternatives. This is especially true for fabless design groups that cannot sink billions into each new node since there are not always multimillion device market opportunities to amortize 10-figure investments. While fabless designers explore alternatives, major consumer device manufacturers such as Samsung and Apple are having a go at building their

Ram Trichur of Brewer Science



Illustrating principles of multicore processor repartitioning.

own mobile device chips and major data center operators including Amazon, Facebook and Google are creating cloud chip designs. This shift equates to fewer high-volume markets for independent developers and fewer instances in which high cost designs and fab expenses can be amortized across multi-tier/multi-generational product lifetimes.

Most manufacturers and supply chain vendors wish there was a pipeline full of new end use products like smartphones and laptops just waiting for top-dollar chips in multimillion quantities. There are instead new opportunities requiring a few million devices, or hundreds of thousands of chips to support automotive, Internet of Things (IoT), machine learning, augmented / virtual reality, medical device, wearable and printed flexible circuit applications. Even exciting new markets such as the IoT that is already generating billions in revenue seek low-cost chips, with more than one major potential user of IoT technology seeking advanced devices at less than $1 per chip. Although seemingly 'chump change' compared to high price legacy processors, emerging applications including the IoT/IIoT are already driving markets and moved semiconductors to 20 percent growth in 2017.

Once final figures are tallied, it's expected 2017 sales topped (USD) $400 billion while fab tool sales jumped well beyond $50 billion, both first time milestones. 2017's growth was uncommon, but the fact that so much ground was gained by emerging applications has prompted market analysts to predict solid opportunities in 2018 and beyond. The SEMI trade group estimates automotive electronics markets (ADAS, vehicle autonomy, infotainment, etc.) will achieve (USD) $280 billion in sales by 2020 and that electronic medical devices will grow to more than $200 million by 2024. Today's $2 trillion supply chain is projected to reach $4 trillion by 2022. Now that's potential.

The appetite for alternative technologies is driven by more than cost and complexity avoidance. There is a growing realization that it is simply harder to design, inspect and test devices at advanced nodes compared to 28nm transistors in classic 2D architectures. Physical effects that impact device performance and product lifetime are more fully understood now since industry has tried its hands at next generation ICs. As geometries shrink and die are made from thinned wafers, so also do heat buildup, ESD and signal interference become more critical issues; this often results in more elaborate (and expensive) testing protocols and mitigation techniques. Smaller die also frequently have different current requirements to speed signals across increasingly complex circuit pathways, and even if this is an incremental increase in the microwatt range, it represents still another hurdle that designers and manufacturers must overcome.

These factors are of particular concern in the ever-increasing number of mobile applications. An excellent example of new challenges can be found in lithographic edge placement errors (EPEs) that were manageable at larger nodes, but are increasingly counterproductive as geometries shrink to 7/5nm and below. EUV by itself won't solve all the issues related to reduced node and transistor feature scaling. Defect elimination also becomes more challenging at the parts-per-trillion scale, which effects multiple critical resources across the supply chain from

Alexandra Laufer-Müller of AP&S

liquid and gaseous chemicals to filtration, sub-fab vacuum and abatement, and so forth. There is no such thing as a perfectly smooth line at atomic scale and variations that were inconsequential at larger nodes can be ‘killer’ below 10nm.

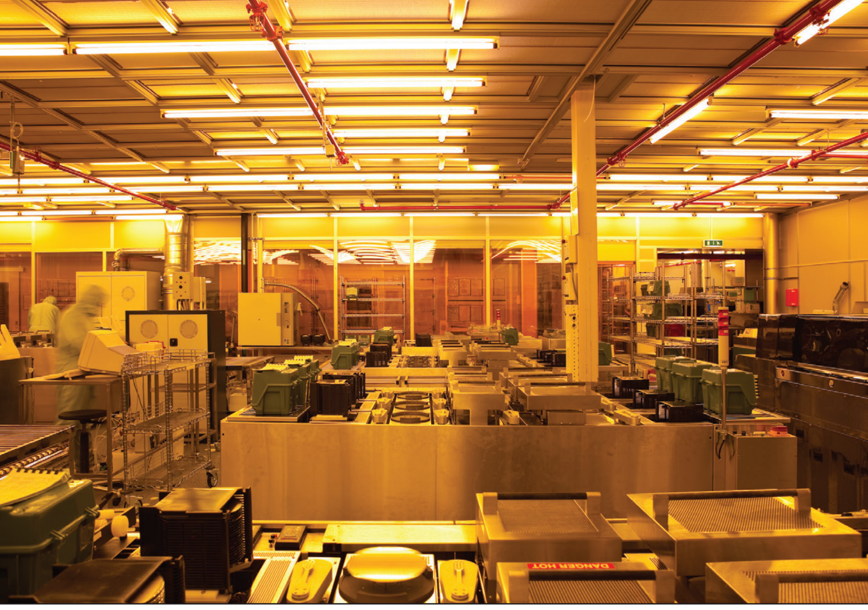
The issues large and small related to device scaling, increasing performance and reducing power consumption are finding solutions through a diverse array of new tools and materials innovations. In addition, new processes and techniques that improve upon throughput and accuracy of existing techniques are showing promise, not just for emerging markets but also for reducing costs and allowing for more product variation in the multimillion device markets with us today.

Applied Materials, a longtime, industry-leading supplier of materials innovation, is one company that is looking ahead to next-generation needs while it supports current requirements in global high volume manufacturing centers.

At the 2017 SPIE Advanced Lithography conference, Applied Materials’ Uday Mitra, vice president of etch and patterning strategy, coauthored a paper about reducing edge placement errors that reported they had cut the critical line error rate (LRE) from a standard 3.4nm to 1.3nm through the use of the company’s Sym3 reactor and proprietary techniques. Performance gains can also be achieved through the use of the latest, highly advanced 3D modeling programs such as Coventor’s software solutions that enable designers to perform process integration experiments in virtual space. This data also provides a means to estimate yield losses in pattern transfer due to variations in side wall profiles and LER.

Semiconductor supply chain leaders are also addressing the needs of present and future designers and manufacturers through expansion, diversification and comprehensive services targeting the needs of a more diverse international manufacturing community. AP&S International GmbH (Donaueschingen, Germany) is a prime example of a company that has reinvented itself, expanded and then redesigned its offerings to meet the needs of global manufacturers. The company specializes in different aspects of wet processing and offers a unique metal lift-off approach to support 3D device manufacturing as well as solutions for both front- and back-end production chains.

To support large companies, research groups and startups—all with unique requirements, the company offers a wide range of tools beginning with manual wet benches through fully automated, multi-chamber systems as both new and refurbished tools. Recognizing that smaller customers often need more assistance incorporating new tools into their operations, the company offers extensive pre-sales and after-sales support, including a fully functioning



Demo Center where customers can literally try-it-before-they-buy-it. Support now includes a growing array of IoT interfaces paired with 24/7 off-site customer support that is accessible by technicians whenever needed. At SEMICON Europa (November 2017) the company introduced its augmented reality programs for diagnosis and trouble-shooting. These additional capabilities and a customer service mentality that permeates all they offer is especially beneficial for remedying a wide variety of issues that may arise over the course of production cycles. AP&S also reconditions equipment (their own and other major brands,) which helps startups and research institutes leverage limited capital equipment budgets.

Newer, smaller semiconductors are frequently being designed to utilize ultra-thinned wafers, which present their own unique handling and testing requirements. Defects occurring throughout production, especially during the grinding and polishing (CMP process stages), may crack delicate die or set the stage for eventual device failures.

UnitySC (Grenoble, France) is expanding thanks in part to the popularity of its 4See Series of devices that go beyond traditional backside wafer inspection. Designed to spot nanometer-scale defects, their approach utilizes phase-shift deflectometry (PSD) and conformal confocal (CC) inspection technology; Unity’s system is unique and patented. A number of customers are utilizing the UnitySC system for inspection of two-layer, bipolar IGBT power devices. The company expects greater growth potential as spotting more defects on the backside of a semiconductor as well as its top with one tool becomes more critical with each new device generation.

Another sign of expanding reliance on sophisticated inspection and metrology tools was an announcement

EVG GEMINI Automated Production Wafer Bonding System

by Rudolph Technologies in 2017 that its Firefly inspection system was selling briskly in China and that the first delivered devices had qualified to enter production. Firefly provides high-resolution visual and non-visual inspection to support a variety of advanced packaging processes including fan-out wafer-level packaging, panel- and wafer-level CSP. Rudolph expected over (USD) $5 million in revenue in Q3 2017 from the systems.

Mieke Van Bavel, PhD, Imec Science Editor

As various next-generation device architectures move from design to production, 2017 also experienced growth in areas that are not traditionally seen as the sources of continual innovation: the sub-fab. Reno Sub-Systems (Reno, Nevada, USA) announced that its late-2017 funding round garnered (USD) $11.2 million in investments, which is not record-setting by itself, but interesting in the fact that major backers included Intel Capital, Samsung Venture Investment Corporation, Hitachi HighTech, sk Hynix (a South Korean memory chip powerhouse), Lam Research (that bought advanced modeling expert Coventor in 2017,) and MKS Instruments (USA, with offices across Asia, Europe and North America).

Reno specializes in two principal technologies: flow control for gases used in chip making and RF power generation with impedance matching of process electrical loads. Both of the company's primary products offer substantial increases in performance compared to legacy solutions, and are targeting next-generation device manufacturing requirements where tightly controlled performance and faster production is more critical to a company's success.

As more semiconductor manufacturers diversify their approach to future markets, this in turn drives responsiveness from vendors who are constantly challenged to develop new ways to address future requirements. One company responding with a growing product line is Brewer Science (USA) that provides materials and processes addressing key device architecture needs by reducing wafer stress, warpage, and high temperature limitations while also enabling faster throughput and reduced form factors.

Brewer Science's temporary bonding and debonding techniques are especially applicable in fan-out wafer-level packaging (FO-WLP). While the 'chip-first' approach has been in high volume manufacturing for some while, the 'chip-last' approach is still developing. Brewer sees many of its product solutions as offering a complete range of options for customers, whichever approach they are taking.

Like other companies serving different segments of the supply chain, Brewer Science offers a wide assortment of options to fit the diversity found across global manufacturing. Brewer has supported temporary bonding/debonding requirements across multiple device generations and is one of the few companies to support every major type of physical debonding approach. Their products continue to evolve and now include fourth generation solutions for laser systems; they have succeeded in raising the temperature range of processes they can support up to 350° C.

"We have almost 15 years of experience in temporary bonding materials development and commercialization for the manufacturing of 2.5D, 3D, compound semiconductor, fan-out and other process flows. We realized very early that one product or even one platform of temporary bonding materials may not be suitable for all of the processes used in advanced packaging applications. Each process flow or device type has a unique set of requirements, and we offer a broad portfolio of bonding materials and release layers designed to support these individual processes. This approach results in maximized customer benefits, in terms of delivering simple processes with high yield and low cost of ownership," said Ram Trichur, Director of Wafer Level Packaging Business Development at Brewer Science.

Trichur said that the company is seeing growing interest in the latest generation of tools, especially across Asia and most notably in China. While all customers see benefits, some report rather remarkable results, especially when they had previous solutions that were not delivering as needed.

"All of our customers benefit from the advances (we) deliver, yet some have particularly striking success

stories. A manufacturer in North America that was producing compound semiconductor devices and bonding with wax materials had a total yield loss of around 30 percent during backside processing due to the poor thermal and mechanical properties of wax. We introduced a new temporary bonding material, and their yields subsequently increased to over 99%," said Trichur.

In addition to solutions that increase accuracy of mask alignments and that enable processing of thinner films at lower temperatures, manufacturers are also looking to atomic level deposition (ALD) and its cousin, atomic level etch (ALE) to control materials removal much more precisely than in the past. Current etchants are typically used to remove materials across entire wafers, which is not always desirable. ALE offers greater accuracy and continual advancements in the field are redefining precision etching. Applied Materials sees their processes as complimentary with ALE, offering the customer even more control including a new approach under study that would enable the ability to 'erase' unwanted material without substantially delaying production, implementing EUV, or installing other leading-edge lithographic tools.

Directed Self Assembly (DSA) continues to gain interest as a means of supporting advanced node scaling while it also helps reduce line-edge roughness (LER). Brewer Science joined with Arkema Group in 2015 to facilitate high-volume production of first-generation DSA polymers. Arkema is a high performance materials specialist based in France with a global presence and 2016 sales of 7.5 billion euro. Brewer Science also is developing second-generation polymers that are essential to enabling DSA at future nodes. The partnership between Brewer and Arkema now seeks to commercialize these high-x (chi) block copolymers for DSA. First generation polymers supported devices down to 22nm while generation two research targets 5nm and below, which the company and most industry experts agree is critical to extending device scaling without relying on EUV or complex multi-patterning schemes.

"DSA represents a lower cost and higher throughput solution over EUV, but another big cost advantage lies in the reduced mask requirements. DSA still needs lithography and etch processes, but these are lower cost compared to multiple patterning. EUV masks are a significant part of the EUV step cost. DSA also offers a technical advantage that it can reach lower feature sizes now than other patterning technologies," said Hao Xu, Director of Semiconductor Business Development at Brewer Science.

In addition to its cost advantages over EUV, Brewer indicated that it continues to explore DSA advantages because they see the process as complimentary with EUV. Companies that have already committed to EUV may conclude that combining DSA with EUV will better support their goals.

"DSA and EUV are complementary because smaller pitches can be printed with EUV that are not accessible with immersion litho. Smaller pitches means two things: lower multiplication factors can be done with DSA, which leads into lower possibility for defects. Also, there is the possibility of eliminating the trim etch step in the chemoepitaxy flow when using EUV. EUV can also provide graphoexpitaxy templates for contact hole multiplication. It is also important to note that because of the resolution limitations of EUV at smaller nodes, it is possible that DSA will help stretch out the timing for, or even eliminate, the need for high-NA (numerical aperture) EUV tools," Xu added.

EMD Performance Materials (a division of Merck KGaA, Darmstadt, Germany,) continues to grow its commitment to advanced semiconductor processing materials science. Rico Wiedenbruch, head of the IC Materials Business Unit at Merck, said his unit is focused on the many scaling related challenges that the industry faces, offering a wide variety of novel solutions to meet these demands and solve miniaturization roadblocks that challenge the limits of physics. The company's advanced precursors for atomic-layer deposition are a turnkey solution for producing very thin, highly controlled conformal films, he indicated.

The EMP portfolio extends to a number of areas for conventional semiconductor manufacturing including front- and back-end packaging. Wiedenbruch noted that EMP's latest solutions target microprocessors, DRAM and NAND Flash memory and are being extended to support ALD precursors for memory devices and 3D NAND cells. He noted some of the biggest problems customers face have to do with pattern collapse, which they address with their FIRM line of processing rinse materials; they also offer block copolymers for DSA. Their line of RELACS Shrink

Production hall at AP&S headquarters

Fully automated A-Series wet bench from AP&S

Materials are designed to support the manufacture of devices with much more narrow features than was previously possible.
While materials suppliers are developing and proving resources for next-generation nodes, others are utilizing those tools to further advance such technologies as 3D stacking. CEA Leti (Grenoble) and EV Group (St. Florian, Austria), announced late in 2017 that they had achieved what both organizations believe is an industry first: a successful 300mm wafer-to-wafer direct hybrid bond with pitch dimension connections as small as 1μm (micron).

Vertical stacking of semiconductor devices has become an increasingly viable approach to enable continual progress towards greater device density and higher performance. Wafer-to-wafer bonding is an essential process step in building 3D stacked devices. Tight alignment and overlay accuracy between the wafers is required to achieve good electrical contacts while minimizing the interconnect area at the bond interface. This is a critical factor since achieving it increases space for more viable die on each wafer, thus delivering higher yield. The constant reduction in pitches that are needed to support component roadmaps is fueling tighter wafer-to-wafer bonding specifications with each new product generation. The product demonstration at Leti's facilities in Grenoble utilized an EV Group Gemini FB XT automated production fusion bonding system.

> Vertical stacking of semiconductor devices has become an increasingly viable approach to enable continual progress towards greater device density and higher performance. Wafer-to-wafer bonding is an essential process step in building 3D stacked devices

"To our knowledge, this is the first reported demonstration of sub-1.5μm pitch copper hybrid bonding feasibility," said Frank Fournel, head of bonding process engineering at Leti. "This latest demonstration represents a real breakthrough and important step forward in enabling the achievement and eventual commercialization of high-density 3D chip stacking."

Research into alternative approaches to transistor design and manufacturing is a robust activity at Leti, the imec group (Leuven, Belgium,) and multiple Fraunhofer institutes in Germany and elsewhere. One recent announcement from imec researchers involved gate-all-around nanowire field effect transistors (FETs) that they organized into a novel vertical configuration. This technology is considered a strong candidate to extend today's CMOS scaling to its ultimate limit. With an excellent performance-to-area ratio, vertical nanowires seem particularly attractive for making highly dense static random access memory (SRAM) cells, imec notes. Moreover, when used to build those SRAM cells, vertical nanowire FETs may play a key role in hybrid scaling – an emerging approach that integrates multiple transistor architectures in one system-on-chip.

Nanowire FETs can be implemented in a lateral or a vertical configuration. Devices configured laterally still utilize conventional 2D layouts, which means they will eventually hit physical limits that are similar to the roadblocks that existing FinFETs are already experiencing. In the case of nanowires organized horizontally, the space available for gate and contact placement will become so small that the devices may no longer function effectively.

Moreover, in the back-end-of-line, too many metal lines in increasingly narrow spaces can give rise to interconnect routing congestion and the possibility of current leakage. Imec researchers believe these issues present an opportunity for vertical GAA nanowire FETs. With these devices, designs can move from 2D to 3D layouts, wherein the gate length is defined vertically. Such a disruptive innovation requires early process-design co-optimization, but it also means that the gate length can be more relaxed without consuming a larger area on the wafer. It also allows some relaxation in the nanowire diameter while preserving control over the short channel effects.

AP&S Demo Centre

Conclusion

Traditional CMOS scaling has become increasingly complex and expensive, which has led semiconductor manufacturers to seek alternatives to meet demands for higher performance at lower costs. That drive includes the development of extreme ultraviolet (EUV) lithography to replace multi-patterning immersion litho; the latest EUV forecasts by ASML (The Netherlands) and mega-scale manufacturers Intel and Samsung indicate EUV is reaching stabilization.

Once implemented, EUV is likely to require additional refinement to extend the number of wafers per hour that can be produced with acceptable yields. Intel, Samsung and TSMC have all indicated they plan to utilize EUV at future technology nodes, varying between 7nm and 5nm.

At the same time, all major manufacturers are seeking alternatives for long-term device scaling that either avoids EUV altogether or delays its introduction.

Scaling (with or without EUV,) below 5nm is possible. An increasing number of researchers, device manufacturers and materials experts are exploring alternatives to the 'brute force' scaling approach that previously served industry when moving to a new node meant a relatively simple exercise in miniaturization.

The future of transistor design for high performance requirements will no doubt include a variety of approaches that could feature various 3D architectures using bonded and stacked devices, and alternative technologies such as fully depleted silicon on insulator (FD-SOI) championed by Globalfoundries, STMicroelectronics, CEA Leti and Samsung, among many companies.

Atomic scale deposition and etch will likely support these strategies as materials science continues to play a larger role supporting new architectures and processing techniques.

Multiple strategies are certain to emerge as effective means for enhancing performance while controlling costs within the global semiconductor marketplace. While major consumer product segments including smartphones, computing and entertainment are expected to continue driving memory and other high-performance applications at high volume, more opportunities are emerging that will require lower volume approaches and rapid customization.

Emerging applications such as the IoT, the IIoT, automotive electronics, medical and wearable electronics are shaping a new global semiconductor market and will continue to do so in the years to come.

The future is **optical!**

The demand for mobile data is expected to increase seven times between 2016 and 2021. Silicon Semiconductor invited the head of IDLab, an imec research group at Ghent University (Belgium), to discuss the future of high speed mobile and fixed data transmissions. By: Professor Piet Demeester – Head of IDLab, an imec research group, Ghent Universit

THE MAINSTREAM ADOPTION of cloud computing applications and the projected, sevenfold increase in global mobile data traffic between 2016 and 2021[1] are just some of the recent trends that continue to boost the demand for high-speed broadband communications.

To cater for that need, the international research community has increasingly been focusing on advancing optical communication systems, using light to transport huge amounts of data from one place to another.

The need for (ever more) speed

To transmit those light beams – and the data they carry – optical communications systems make use of optical fibers; flexible, transparent (glass or plastic) fibers with a diameter slightly thicker than that of a human hair. Compared to legacy (copper) cables, they enable data to be transmitted over longer distances, considerably faster.

At the September 2017 European Conference on Optical Communication (ECOC), for instance, Japanese researchers presented a massive breakthrough in terms of how much data can be transmitted through a single optical fiber – reaching a transmission speed of 10 petabits (10 million gigabits) per second; a landslide achievement that will undoubtedly revolutionize the way in which intercontinental fiber-optic communication networks will be built and operated going forward.

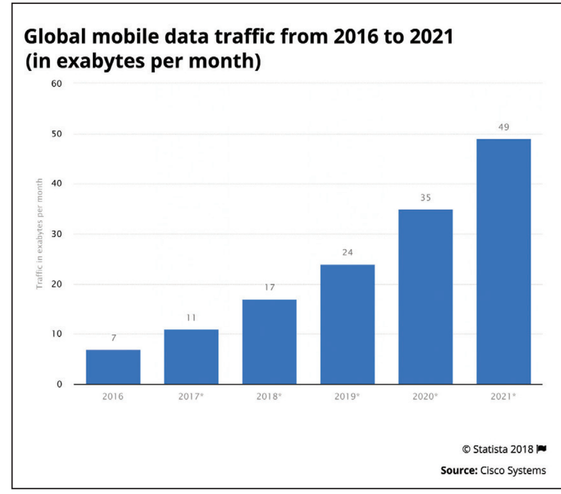


Figure 1: Cisco Systems projects that the demand for mobile data traffic will increase seven times between 2016 and 2021.

In pursuit of these ever more powerful optical communication systems, increasingly faster and efficient optical transmitters and receivers at both ends of the optical fibers need to be developed. That is exactly one of the key strengths of our researchers at IDLab, an imec research group at Ghent University.

Breaking the barriers of fiber-optic communications
Our research in this space aims at improving the performance of four technologies in particular:

- Short-reach datacenter interconnects: using fiber optics to interconnect servers in a datacenter to an Ethernet switch, so as to provide access to network resources or allowing server-to-server communication;
- Passive optical networks (PONs): a network architecture in which a single optical fiber provides multiple end-points (such as homes and offices) with high-speed broadband connectivity;
- Long-reach coherent technology: enabling the long-distance transmission of massive amounts of data over a fiber-optic cable by using modulation of the amplitude and phase of the light, as well as transmission across two polarizations;
- Radio-over-fiber for 5G (and beyond): as 5G networks require the deployment of a multitude of small cells, radio-over-fiber (RoF) technology allows wireless signals to be optically distributed to these cells directly at high frequencies and converted from the optical to the electrical domain before being amplified and radiated by an antenna; as a result, no frequency up-down conversion is required at the cell, which results in less complex and more cost-effective implementations.

Figure 2: Imec and its IDLab research center are testing new approaches to optical communication. Shown is the testing environment of imec's new 'opto-antenna' that eliminates the conventional electrical amplifier previously required to create an RF signal.

In 2017, our teams contributed significantly to pushing the data rates that these technologies can accommodate. In the datacenter realm, for instance, the broadband speeds attained by our demonstrators run 5 to 10 years ahead of the Ethernet Alliance's standards. And the same goes for our research into PON networks, where we currently achieve bitrates 5 times higher than today's commercial solutions.

New perspectives: radio-over-fiber

The radio-over-fiber (RoF) track is the latest addition to our research agenda, and will become increasingly important in the course of 2018.
As mentioned already, RoF is poised to become an essential enabler of the wireless 'small cells' technology that already surrounds us today – with large amounts of wireless antennas that each cover a small area (or cell) to enable very high-speed wireless broadband. The smaller the cell, the higher the bitrates that can be attained.

The trend towards installing increasingly smaller cells is not new; but the tendency to aggregate more and more functionality from individual small cells base stations in a so-called 'cloud radio access network' (cloud RAN, also called centralized RAN) is new. Traditional cellular networks consist of many stand-alone base stations, with each of those base stations processing and transmitting their own signals to and from mobile terminals, and forwarding the data payload to and from the mobile terminal and out to the core network. Each base station has its own cooling, backup battery, monitoring system, and so on.

In a setting where growing numbers of small cells are being installed, the value proposition of a centralized RAN is obvious: as functionalities and hardware are shared, costs decrease. And RoF will be fundamental to making the communication between a cloud RAN and its remote antennas as easy and cost-effective as possible.

Up until today, this topic has not yet been explored in detail by the international research community – so we really have the potential to generate substantial impact in this domain. One nice example is the so-called opto-antenna we developed; a passive antenna that directly connects to an optical fiber; it no longer requires an (electrical) amplifier to produce an RF signal. With all of its active functionalities residing in the cloud RAN, our opto-antenna could easily be

integrated in a number of materials (floor tiles, wall paper, etc.) for very high-speed wireless connectivity at short range. In our first tests, for instance, we achieved bitrates of 0.5 Gbps at distances up to 20cm. (Production Note: Figure 2 image should be located as close to the above text as possible)

The future is optical

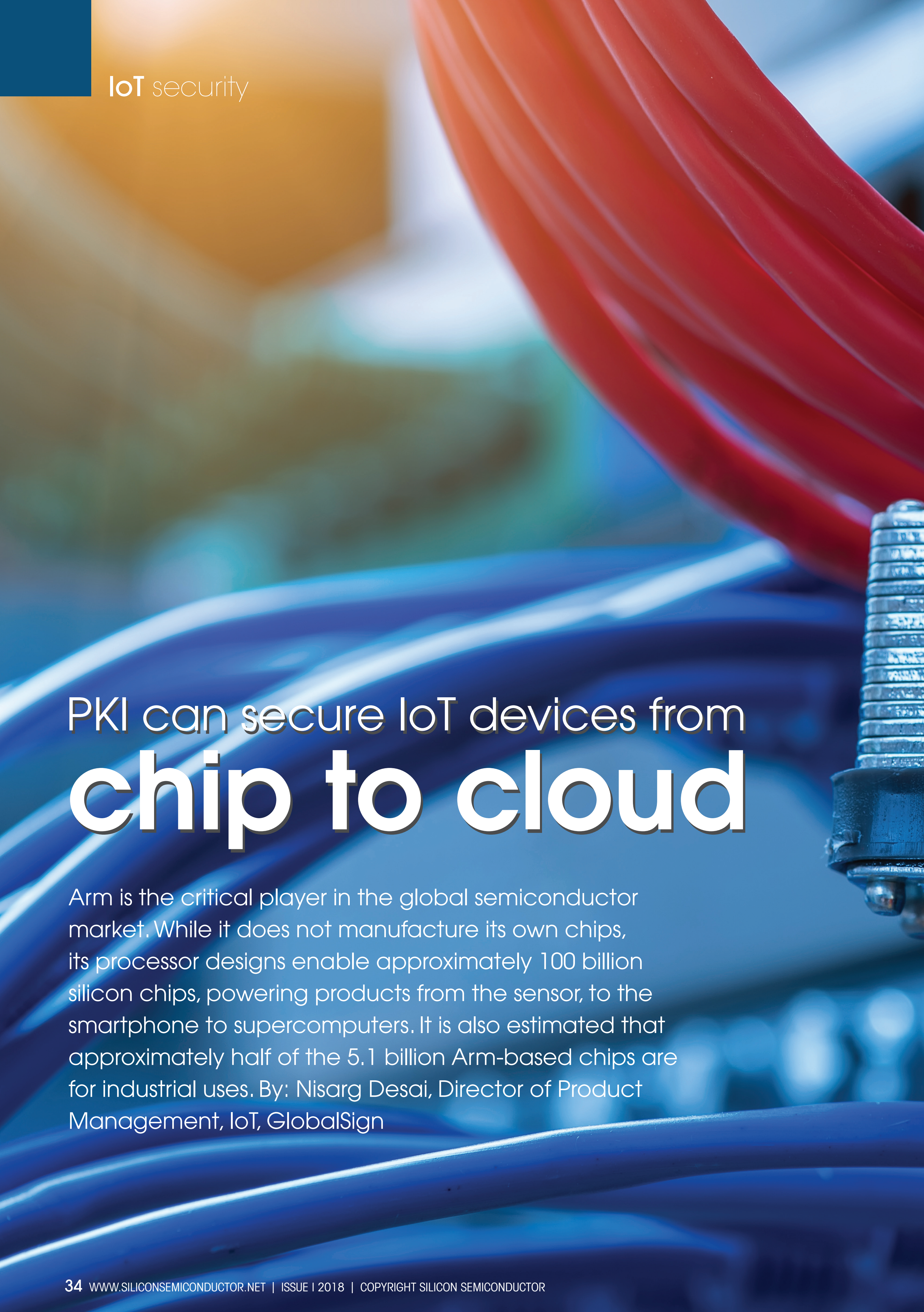
In the next couple of years, the improvement and refinement of optical technologies will remain very high on our research agenda. If one needs to send lots of data over longer distances, it is clear that optics remains the way to go – not only in the wireline, but also in the wireless domain.

And our research into RoF will be fundamental to making this a reality. As wireless spectrum and spectral efficiency are reaching their scaling limits, deploying increasingly smaller cells will be key to continue to increase wireless bitrates. And more cost-efficient technologies, such as RoF, will be required to accommodate this.

Thanks to a close collaboration with other imec research teams working in the area of wireless communications and photonic technologies and devices, we are uniquely positioned to contribute to this evolution.

Biography Piet Demeester

Piet Demeester is professor in the Faculty of Engineering and Architecture at Ghent University, IEEE Fellow and holder of an ERC Advanced Grant. He also heads IDLab, an imec research group at Ghent University and the University of Antwerp. After finishing a PhD on Metal Organic Vapor Phase Epitaxy for photonic devices in 1988, he established a research group in this area working on different material systems (AlGaAs, InGaAsP, GaN). This research was successfully transferred to imec in 2002. In 1992, Piet started research on communication networks and established the IBCN research group (now integrated in IDLab). IDLab is focusing on several advanced research topics: Distributed intelligence for IoT, Machine Learning, Data Mining, Semantic Intelligence, Multimedia Processing, Cloud and Big Data Infrastructures, Fixed and Wireless Networking, Electromagnetics and Transceiver IC Design for Optical and Optical-Wireless Networks.



PKI can secure IoT devices from chip to cloud

Arm is the critical player in the global semiconductor market. While it does not manufacture its own chips, its processor designs enable approximately 100 billion silicon chips, powering products from the sensor, to the smartphone to supercomputers. It is also estimated that approximately half of the 5.1 billion Arm-based chips are for industrial uses. By: Nisarg Desai, Director of Product Management, IoT, GlobalSign

LIKE ANY semiconductor company, Arm (now owned by Japan's SoftBank) is very much focused on security, and has a company-wide mandate to ensure secure products across the board from the chip up to the cloud.

Arm recently announced its 'Platform Security Architecture' initiative, aimed at providing security guidance for IoT device developers. It has four recommended security tenets, one of which is certificate-based authentication, a market that is expected to grow in the coming years. This is not a surprise given the current trends reported by The Ponemon Institute, one of the world's top providers of research on the information security industry. Its 2017 Public Key Infrastructure (PKI) Global Trends Study, which gathered input from more than 1,500 IT security practitioners worldwide to determine where PKI is heading, found that 43 percent of IoT devices will adopt digital certificates for authentication within the next two years.

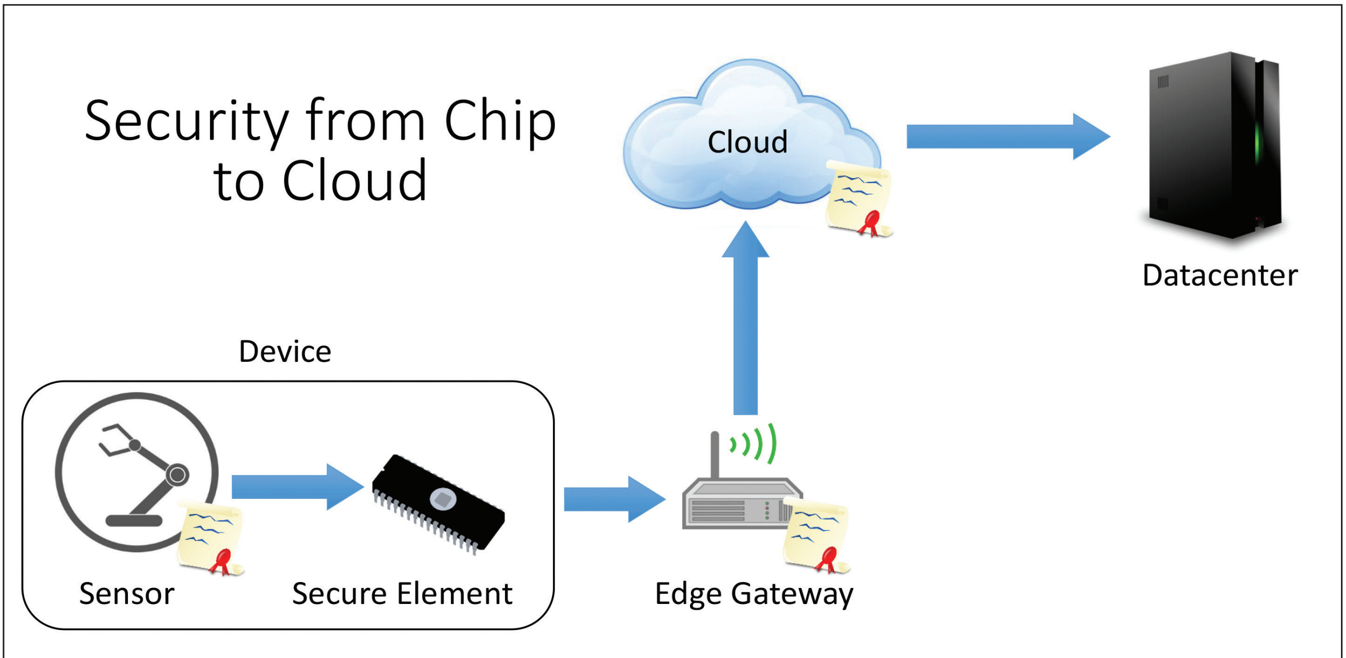
GlobalSign has long been a provider of PKI-based solutions, because it is time-tested, open standards-based, easily implemented and a widely accepted technology. PKI is even more relevant in this case, because it lends itself very well to IoT devices. It can be implemented in a relatively lightweight fashion on different classes of devices. Most IoT devices, by definition, are data gatherers, data transmitters and sometimes, data processors. Thus, secure communication is very important to IoT devices, and PKI is a simple and cost-effective way to achieve this. Asymmetric cryptography, which forms the basis of PKI, is mathematically and empirically proven to be an effective means of providing secure distribution of encrypted messages to targeted senders.

Security chips

Chip enabled and accelerated functions form the bedrock of most secure software and hardware implementations today. For example, the core identity of any device is stored in something called a Secure Element, a chip that forms the root-of-trust for a device. It serves as a Trust Anchor, which then enables other security functions such as Secure Boot and Remote Attestation. Many of these functions require a great deal of processing power – hence dedicated cryptographic chips accelerate these operations, making them faster and/or enabling them to consume less power. Quite a few of these chips are based on Arm designs. It is important to understand there are various options to adding a secure element. A Trusted Platform Module (TPM) chip is a crypto co-processor that sits alongside the primary processor and requires a redesign of the board to allow its integration. A more novel, equally secure but much more cost-effective option is to use a (Physically Unclonable Function (PUF). There are various other options, but discussing these in detail is out of scope of this article.

PKI for IoT devices

PKI's roles, policies, and procedures are needed to create, manage, distribute, use, store, and revoke digital certificates and manage public-key encryption. PKI has been relied upon since the 1970's and was first used in technologies such as e-signatures in the 1990's. Today, it is viewed as one of the most reliable ways to secure IoT devices.
All IoT devices require a strong identity and need to prove that they are who they claim to be, and not something else. This identity should be universal and easy to verify for the communicating party. Soon, they will



PKI enables 'lightweight' IoT security from chip to cloud. Image courtesy of GlobalSign.

even generate their own identity and store it safely, directly as a result of PKI's unique mathematical capabilities. Also coming soon are IoT devices that will each have their own individual and unique certificate to prove their trustworthiness. By using PKI in this fashion, IoT devices will be more trustworthy, limiting the chances of unauthorized access.

Chip to cloud security

As alluded to earlier, Arm has a directive to ensure security across the board, from its chips, through their IoT stack, and up to the cloud embedded onto a chip. Arm takes its own low power Cortex-M product family and adds support for its open-source Arm Mbed OS embedded operating system. This combination is easy to use and to configure out of the box, making it ideal for small scale developers designing an IoT device and are at the stage where they are ready to begin creating design applications – they can simply use Mbed OS as their embedded operating system.

The Arm Mbed family also includes a cloud platform as a service, called Mbed Cloud. Since most IoT use cases today involve collecting sensor data from an IoT device on the edge and then transmitting it up to a cloud application for further processing, this cloud service is very useful. Mbed OS can natively integrate and connect to Mbed Cloud. Now, Transport Layer Security (TLS) is the protocol of choice for most device to cloud connections. This requires the use of digital certificates.

What is significant about Mbed Cloud is that it supports a "bring your own Certificate Authority (CA) program." You can have a third-party CA create a dedicated PKI hierarchy and upload the Root CA Certificate to Mbed Cloud. This enables certificate-based authentication to automatically accept connection requests from all your devices that have a certificate issued from that particular hierarchy.

Getting started

A very important first step for IoT device developers is enabling security across the vertical IoT platform stack – right from the end device or sensor node, through the edge and fog layers, up to the cloud-platform and underlying data and application infrastructure. This can be achieved by ensuring that, as data is passed through these layers, each step in the chain is verifying it is communicating a party's identity and authority, while ensuring data privacy and integrity. This is attainable through PKI.

For those not intimately familiar with PKI, it is a commonly used approach to encryption and authentication. The architecture provides a greater level of confidence for sharing information electronically. First, we can look at how devices can ensure integrity within themselves. One way to achieve this is Secure Boot. A Digital Signing Service can be used to sign and compute the hash of any firmware, before loading onto the device. The public key used to sign the firmware is stored on the device, in non-erasable memory. Whenever the device boots up, a hash of the bootloader (the process of applying an algorithm to generate a small string from a larger file that can later be used to verify the file's integrity) is generated and signed by the public key. Now if we can trust this public key, and verify this signed record to be accurate, then we have proved that the bootloader (and anything else that was checked) is genuine. If we then send this signed report or file to a remote server, periodically, to prove that the bootloader is genuine, we have remote attestation.

3 EVENTS 2 DAYS 1 TICKET

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Now that we have established a device and its code are genuine, we can move onto secure communications outside it. A device can present its identity certificate to the edge router or gateway it is communicating with. The gateway can then inspect and validate the certificate, and following that, accept the incoming data packet. Now the edge gateway can establish a (TLS) connection with the cloud platform server and prove its identity to the server via its own certificate. Conversely, the edge gateway can also require and verify the server's identity certificate thus enabling a mutual TLS connection.

This bi-directional verification provides security against eavesdropping, injection and other Man-in-the-Middle (MITM) attacks.
Device certificates can also support role-based authorization. Since the certificate cannot be modified once issued by a CA, one can insert specific identifier fields (or roles) that this device is allowed to assume. Now, we can not only verify the source of data, but also whether a device is allowed to transmit or accept that piece of data.

These two basic security tenets – authentication and authorization – can easily be implemented by device designers by simply integrating a secure certificate provisioning step into their device manufacturing process. This then easily extends to stricter security techniques like secure boot and firmware attestation. Some CA's, including GlobalSign, have tools and platforms available to help achieve these security goals. One example of this would be our new device enrollment service. All of the suggested cryptographic techniques mentioned here utilize asymmetric cryptography as a basic building block. Device certificates, publicly trusted roots and code signing, are all implemented using PKI.

By allowing support for third party CAs, ARM has effectively and easily enabled adopters of Mbed a plethora of options to implement device-based security features.

Conclusion

This is an exciting time for PKI, and it is likely that many organizations will embrace it as a first step to securing their IoT devices. Identity is the foundation of security, and secure authentication and authorization the first two targets to accomplish – PKI seamlessly enables this. Device designers and manufacturers relying on PKI will find that this tried-and-true technology will enable them to successfully launch secure applications and products such as the one that are described, opening up new windows of possibility to them. With both silicon vendors, embedded OS makers and cloud platform providers natively supporting, and in some cases requiring, a PKI-based credential, IoT makers should now find it both easy and cost-effective to include security as part of their product design. This will ultimately lead to a more secure Internet of Things for all of us.

Real-world application in the retail industry

THERE are an increasing number of projects being developed using the approach outlined above. One such example is an effort by GlobalSign, where we are leveraging ARM's Mbed OS and Mbed Cloud for a project on behalf of a Japanese bookseller.

The project involves tracking the sales of new books with hidden sensors that are placed on the backside of an 8 ½ x11 polycarbonate board also called a plaque. The sensor tracking the books in the plaque's proximity runs Mbed OS on a Cortex-M based chip. Each chip uses a digital certificate provided by GlobalSign. That certificate then talks to Mbed Cloud, notifying that an event – in this case, a book being picked up from a stack – has occurred. In addition, a mobile app is available that enables users to view the number of books that were picked-up or sold. On the front of the plaque is an E-Ink display that shows details of the book such as the price, a description of the contents, etc. This can also be dynamically updated via the app.

A certificate identifies the sensor and display to prove the source of the data. When someone walks over to the table and picks up a book, a near-field proximity sensor is triggered which detects the presence (or absence) of an obstruction. Based on a configured image map, the application can detect that someone came near it, picked up a book, then left, leaving the book stack shorter. The sensor will then issue a notification via Mbed OS to be sent to Mbed Cloud. The bookseller can use the app to track the number of books picked up.

Why do we need to implement a security solution for such a benign use-case, and why does it have to be PKI-based? First, the bookseller might be integrating an inventory system into this workflow. Whenever a book is picked-up (without being replaced) an automatic counter decreases the available stock. Thus, we need to ensure the accuracy and integrity of this data. In addition, there may be several books and stations in a store, thus the identity of the plaque and reporter of the information are critical. Second, PKI is an easy way to implement this kind of a solution, and is what was used for the project. However, it is not the only way. Since Mbed OS has a low resource footprint, and Cortex-M chips are very power efficient, low-powered battery operated devices can be used to enable this application, without compromising security.

At this time, it is expected that approximately 100 plaques will be built by late spring 2018 and subsequently deployed. Once this pilot project is completed, it may be expanded to all of the bookseller's locations throughout Japan.

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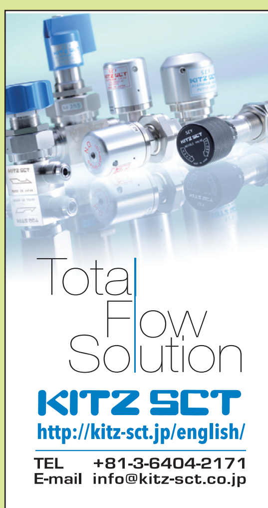

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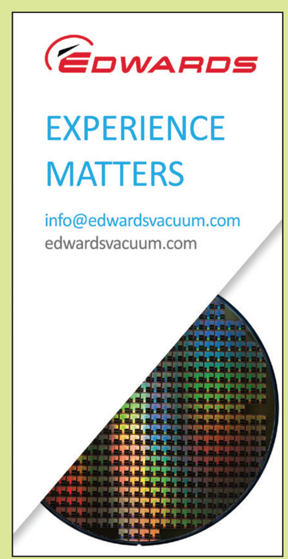

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