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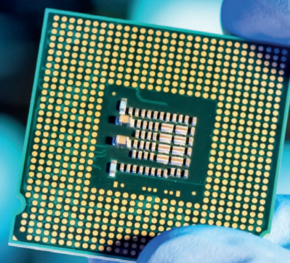

VOLUME 45 ISSUE X 2024

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INSIDE
News Review, Features
News Analysis, Profiles
Research Review
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A new patented approach to diffusion bonding

An innovative process is reducing diffusion bonding time of aluminum and aluminum alloys by up to 50%

The semiconductor industry with AI and simulation

It's no secret that the semiconductor industry has been in a state of flux since generative AI exploded into the mainstream

Subfab maintenance through Industry 4.0 technologies

The semiconductor industry is driven by relentless innovation, pushing the boundaries of technology and efficiency

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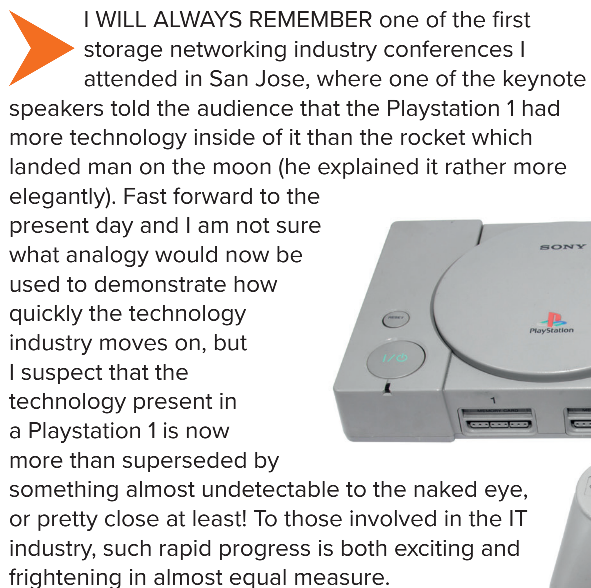
VIEWPOINT

By Phil Alsop, Editor

Intel outside?

I WILL ALWAYS REMEMBER one of the first storage networking industry conferences I attended in San Jose, where one of the keynote speakers told the audience that the Playstation 1 had more technology inside of it than the rocket which landed man on the moon (he explained it rather more elegantly). Fast forward to the present day and I am not sure what analogy would now be used to demonstrate how quickly the technology industry moves on, but I suspect that the technology present in a Playstation 1 is now more than superseded by something almost undetectable to the naked eye, or pretty close at least! To those involved in the IT industry, such rapid progress is both exciting and frightening in almost equal measure.



For every company, there's the very real prospect of developing something so groundbreaking that it will turn all received technology wisdom on its head. And there's the equal possibility that somebody else will develop something so groundbreaking that it will return all received wisdom on its head, and every other company has to re-think its strategy, and fast.

The departure of Pat Gelsinger from Intel fits somewhere within this narrative, all be it the timeframes and changes involved were not of the 'overnight sensation' variety. I am sure it's a complicated story, and no 'one size fits all' narrative, but to this observer looking in, the multiple pressures of the tech world – the pressure to keep reinventing yourselves, the pressure to stick with what you do well and has served the company so well in the past, the intense pressure from disruptors with some smart new technology – all have no doubt played a part in what I think it is fair to say is Intel's struggle to identify the best way forward. Does it cannibalise itself, abandon its traditional technology strongholds and go all in on the bleeding edge – GPUs and who knows what else to come? Does it continue to do what it does well, and accept some rate of decline? And how does it respond to the folks developing smart new chips in today's AI-obsessed world?

I don't think there are any easy answers – and not just for Intel. Silicon photonics and optical computing advances point to a future of massively different compute architectures and solutions. Are the traditional server manufacturers ready for this future? And where does quantum computing fit into the mix – even if it is still somewhere over the horizon? And what does the continuing move to software-as-a-service and the cloud mean for sales of hardware over time?

I am sure there are plenty more questions which could be asked, but rather fewer certain answers. Maybe the only certainty we can bank on in the semiconductor space is the certainty of uncertainty. Just look at the EV market right now – turmoil seems something of an understatement to summarise what's going on. Just imagine if all the bets on AI, which seem entirely credible as of now, come in significantly under expectations.

As for Intel itself – well, I am not confident enough to make any major prediction. Merely to observe that any history of the IT industry includes once household names which are no longer with us, and it also includes household names which are. Call me a fence-sitter if you like, but that seems a comfortable seat right now!

A happy festive season to one and all.

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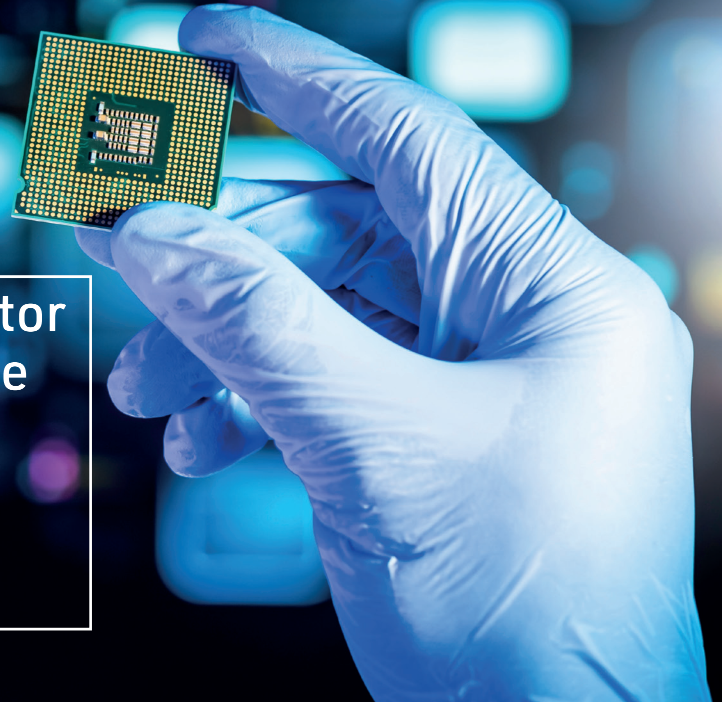

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Back-end semiconductor equipment: advanced packaging drives revenues in 2025

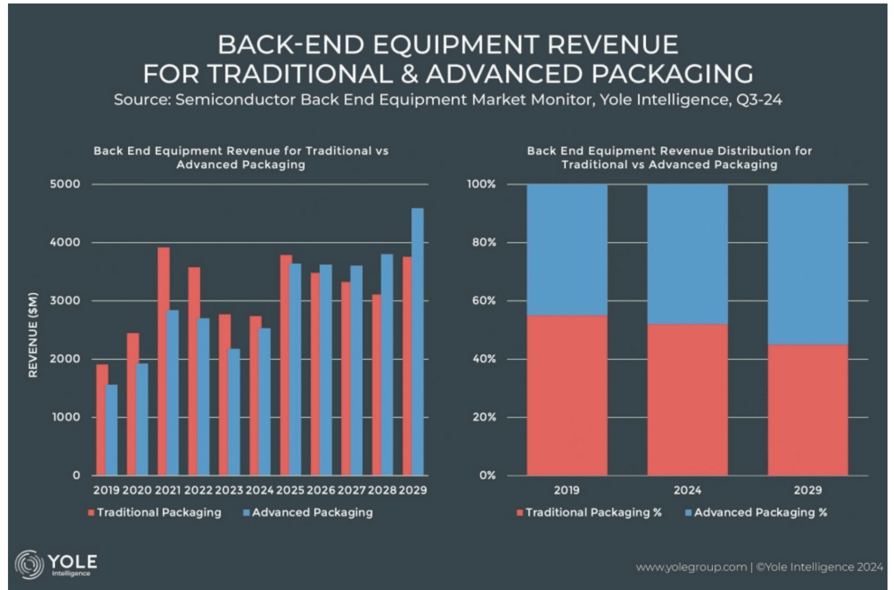
Back-end semiconductor equipment market faces short-term decline but anticipates recovery with adoption of advanced packaging techniques.

BACK-END EQUIPMENT spending has always been in the range of 1% of the total semiconductor industry revenue, confirms Yole Group. Hence, the back-end segment is expected to grow in line with semiconductor growth.

The semiconductor market recovery in mainstream segments like automotive, industrial, and consumer has been slower than expected in Q2 and will continue so in Q3 2024. Excess inventories and muted demand are prolonging the downturn in these sectors, with utilization rates still below optimal levels, particularly in traditional wire bonding. As an example, ASE reports utilization of just 60% in some of its conventional back-end equipment segments, while ASMPT confirms softness in China's high-end smartphone and industrial markets. However, these sectors are expected to improve in late 2024 or early 2025, with recovery expected in 2025.

This is reflected in the back-end equipment market, where the quarterly revenue dipped from $1.4 billion in Q1-24 to $1.29 billion in Q2 2024, a -8.1% decrease quarter to quarter; the market is expected to dip further in Q3. However, Yole Group's analysts expect a rebound in Q4 2024, with quarterly revenue reaching $1.31 billion, which is expected to grow further to $1.74 billion in Q1 2025. Indeed, at the beginning of 2025, the market is showing a strong recovery in demand, coupled with increased adoption of advanced packaging.

The back-end equipment market, integral to semiconductor assembly and packaging, is positioned for strong growth over the next few quarters, though near-term challenges persist. Insights from major OSATs, leading back-end equipment vendors, and standard industry outlooks suggest several key trends and opportunities shaping the sector.



Advanced packaging is the main driver for the back-end equipment market. Demand for advanced packaging technologies, all related to the push for AI and high-performance computing (HPC), remains resilient. Indeed, both Besi and ASMPT have reported substantial order volumes for 2.5D/3D packaging equipment as well as hybrid bonding systems supported by AI servers and high-bandwidth memory (HBM). These technologies are becoming increasingly essential for next-gen AI chips and photonics applications.

Investment in advanced packaging capacity is ramping up significantly. Besi, for instance, has increased its R&D and CapEx spending, focusing on hybrid bonding and TCB capabilities to meet the expected surge in AI demand. Similarly, K&S and ASMPT are actively expanding in thermocompression bonding and related flux-less processes, positioning themselves well for ongoing AI-driven growth. This level of investment is a clear indicator that the major players are preparing for a more dynamic second half of 2024 and into 2025.

Yole Group has launched its first semiconductor product, the Semiconductor Back-End Market Monitor, which focuses on packaging processes starting at the middle-end stage. Covering 36 segments and analyzing 66 leading equipment companies, this Market Monitor provides quarterly insights into back-end equipment markets, essential for advancing chip technology and supporting digital transformation. With the growing demand for advanced packaging solutions including 2.5D/3D packaging and hybrid bonding, for example, the market is evolving to support cutting-edge applications in AI and high-performance computing. At the same time, traditional packaging methods remain essential for various semiconductor applications, ensuring a balance between innovation and established techniques and driving efficiency across multiple industries.

Semiconductor patent applications up 22% globally

AI demand helping drive semiconductor innovations. Sharp rise in patents filed in China as industry responds to US export controls on semiconductors. Suggests industry sees China a continued key market.

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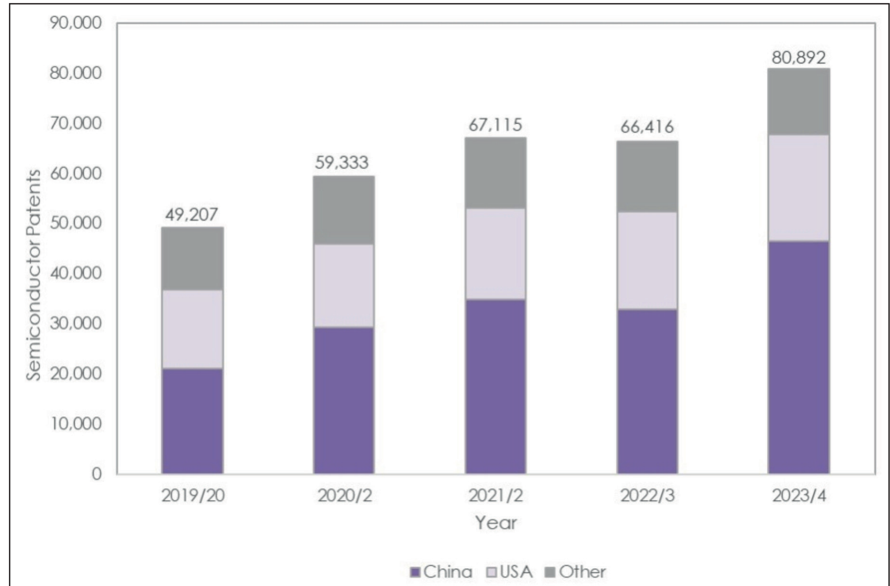


There has been a 22% increase in global semiconductor patents filed, rising from 66,416 in 2022/3* to 80,892 in 2023/4 (year-end March 31), shows new research by Mathys & Squire, the leading intellectual property law firm. Dr Edd Cavanna, partner at Mathys & Squire, says the rise in new inventions in the sector is partly being driven by the boom in the AI sector which has dramatically increased the market cap of chip companies such as Taiwan Semiconductor Manufacturing.
Dr Cavanna says: “Gen-AI is the most recent technology that is spurring R&D in the semiconductor industry and leading to an associated rise in patent applications.”

Chinese patents up 42% as domestic industry responds to US export restrictions of some semiconductors
Global semiconductor patent applications filed in China have risen 42% to 46,591 in 2023/4, up from 32,840 the year before.
The sharp uptick in Chinese applications is in keeping with a general trend recently of strong growth and large filing numbers. In contrast, new US patent application filings have remained reasonably steady over the past few years.

Dr Cavanna says: “This is likely an indication that the rivalry between US and China in the semiconductor patent space is heating up.”

Export restrictions on some semiconductors from the US to China and concerns that more export restrictions could be announced in the future may have encouraged more investment and R&D from the Chinese semiconductor industry.

The Chinese government has previously called for China to ‘step up’ progress in the innovation of key technologies, including semiconductors as well as AI research which depends heavily on semiconductor technology.

Global semiconductor sales increase 23.2%

THE SEMICONDUCTOR INDUSTRY ASSOCIATION says that global semiconductor sales were $166.0 billion for the third quarter of 2024, an increase of 23.2% compared to the third quarter of 2023 and 10.7% more than the second quarter of 2024.

Global sales were $55.3 billion during the month of September 2024, an increase of 4.1% compared to the August 2024 total of $53.1 billion. Monthly sales are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.
SIA represents 99% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms.

“The global semiconductor market continued to grow during the third quarter of 2024, with quarter-to-quarter sales increasing at the largest rate since 2016,” said SIA President and CEO John Neuffer. “Sales in September reached the market’s highest-ever monthly total, driven by a 46.3% year-to-year increase in the Americas.”

Regionally, year-to-year sales in September were up in the Americas (46.3%), China (22.9%), Asia Pacific/All Other (18.4%), and Japan (7.7%), but down in Europe (-8.2%). Month-to-month sales in September increased in Japan (5.3%), Asia Pacific/All Other (4.5%), the Americas (4.1%), Europe (4.0%), and China (3.6%).

Silicon photonics market worth $7.52 billion by 2029

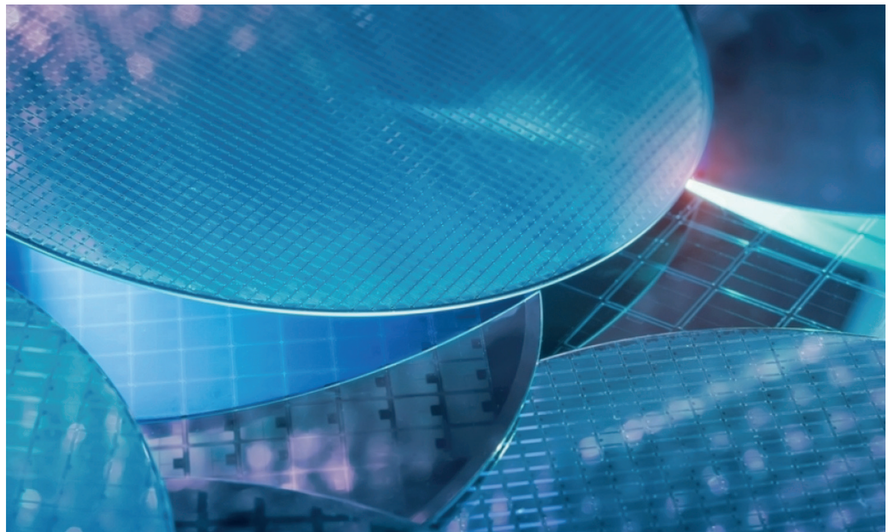
The global silicon photonics market was valued at USD 2.16 billion in 2024 and is projected to reach USD 7.52 billion by 2029, growing at a CAGR of 28.3% from 2024 to 2029 according to a new report by MarketsandMarkets.

THE PRIMARY FACTOR driving the silicon photonics market growth is the focus on power consumption using silicon photonic-based transceivers. It is challenging to meet the ever-increasing demand for high-speed data transfer with conventional copper cables.

Compared to traditional electronic transceivers, silicon photonics transceivers have several advantages, including higher bandwidth, lower latency, and lower power consumption. They can help lessen energy costs by reducing the power needed for data transfer. In addition, silicon photonics technology can enable new applications previously impossible with traditional electronic transceivers.

The silicon photonics market for data centers is expected to grow at the largest market during the forecast period. The data center industry includes applications like data center trans receiver, 5G trans receiver, photo processing, CPO, and optical interconnect. The silicon photonics market is rapidly expanding, with numerous applications of silicon photonics technology and products based on this technology in the computing industry across various countries worldwide.

This market is projected to grow due to the increasing research & development investment by silicon photonics companies in developing this technology and the rising global demand for multimedia extension connectors (MXC) connectors, photonic-integrated circuits, silicon optics, and more. Mega data centers are facing the problem of heavy internet traffic. They are steadily increasing their investments in large data centers as they implement cloud-based extensive data services that can be crowdsourced and crowd-distributed. They used machine-to- machine and inter-data centers and high-performance computing transactions to power the mobile web. For instance, in February 2023, Marvell Technology, Inc. selected Amazon Web Services, Inc. (AWS) as its cloud provider for electronic design automation (EDA).



The optical waveguide segment is expected to witness the highest CAGR during the forecast period.
The optical waveguide as the component is expected to grow with the highest CAGR during the forecast period. They are applied to the transfer and control of light in integrated circuits in the field of photonics.

Typically, lithography techniques are used to etch a silicon substrate to form a waveguide pattern. It has several benefits, such as low power consumption, high integration density, and ease of integration into electronic circuits due to its compatibility with complementary metal-oxide-semiconductor (CMOS) processing technology. The market is expanding due to major companies increased strategic development. For example, in 2021, Anello Photonics, the developer of the Silicon Photonic Optical Gyroscope, and Tower Semiconductor, the leading foundry of high-value analog semiconductor solutions, announced a strategic partnership for a new low-loss silicon optical waveguide technology and manufacturing process.

The US to holds the largest market in North America during the forecast period.

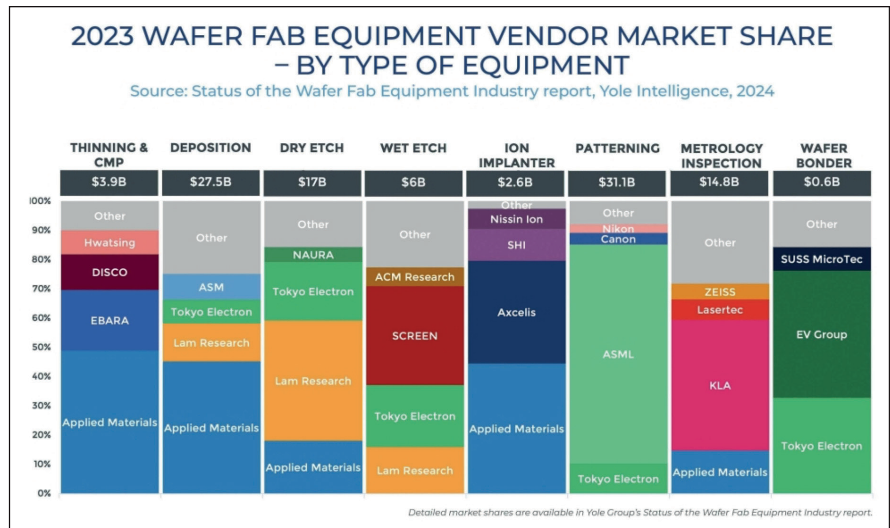
The US is one of the most developed countries in North America. The use of silicon photonics in telecommunications and data communication in the US is driving the country's silicon photonics market growth. In the US, it is found that mergers & acquisitions and partnerships are playing a pivotal role in developing the silicon photonics market. In March 2021, Cisco Systems, Inc. (US) acquired Acacia Communications, Inc. (US) for USD 4.5 billion for manufacturing high-speed, optical interconnectivity, and photonic-integrated modules and transceivers, increasing its presence in the silicon photonics industry.

Global Wafer Fab Equipment revenue poised to surge

With semiconductor device revenue showing 19% year-over-year growth (2) , WFE vendors are adapting to uneven CapEx by broadening their application mix...

WAFER FAB EQUIPMENT (WFE) vendors' overall revenue for 2024 is projected at $133 billion, with 83% coming from shipments and 17% from service & support. The overall market will reach $165 billion by 2029. USA-headquartered companies traditionally lead in revenue generation. On the other hand, in 2023 and 2024, mainland China will be the most important equipment shipment destination, with a third of the overall WFE revenue.

WFE market leaders are ASML, Applied Materials (AMAT), Lam Research, Tokyo Electron Limited (TEL), and KLA.



The semiconductor industry is on a strong upward trajectory, with revenue expected to reach $630 billion by 2024 and a 19% year-over-year growth from 2023 to 2024. However, beneath these impressive figures, the reality is more complex. Growth will vary significantly across different device segments. Yole Group analysts attribute this surge primarily to investments in generative AI for DRAM / HBM and processors, while NAND CapEx remains weak, and CapEx in the legacy logic and specialty markets faces potential risks. In this uncertain landscape, WFE vendors are navigating uneven capital expenditures by diversifying their application portfolios to sustain or boost their revenue levels.

By 2029, overall WFE revenue is projected to reach $165 billion, maintaining similar proportions with 2024 between the two segments, shipments and service & support, announces Yole Group in its new report, Status of the Wafer Fab Equipment Industry.

WFE shipments are expected to grow to $139 billion during this period, with a +4.7% CAGR . This segment is clearly driven by changes in device architecture across memory and logic. At the same time, the service & support segment is set to generate $27 billion in revenue, with a +3.3% CAGR (4). Indeed, it is pushed by the surge in installed base utilization rates and increasing machinery complexity.

Yole Group has unveiled its latest semiconductor manufacturing report, Status of the Wafer Fab Equipment Industry. This comprehensive technology and market analysis provides a thorough overview of the semiconductor equipment market, including annual market size data and a detailed historical perspective.

Yole Group's analysts offer a compelling breakdown of the wafer fab equipment (WFE) market by process technology and device application, along with an in-depth analysis of vendor market shares. The report also explores the relationship between WFE market size,

the semiconductor device market, and CapEx, covering related market segments, subsystems, components, and modules. Additionally, it offers a technological outlook, detailing equipment characteristics such as equipment morphology with detail on chamber types, substrate types and sizes, and emerging process parameter trends that influence equipment architecture.

The study also includes a significant analysis of the supply chain, recent mergers and acquisitions, and updates from the equipment industry.
This report is part of Yole Group's global semiconductor manufacturing collection, which includes resources such as the Wafer Fab Equipment Market Monitor and the upcoming Back End Equipment Market Monitor. The complete collection can be accessed HERE.

From a player point of view, the overall market is dominated by the big-five WFE vendors that have occupied their position for many years: ASML, which has been leading the market since 2023, followed by AMAT (Leader in 2022), Lam Research, TEL, and KLA.

Industry records strong growth in Q3

The global semiconductor manufacturing industry in the third quarter of 2024 showed strong momentum with all key industry indicators performing positive quarter-on-quarter (QoQ) increases for the first time in two years, SEMI has revealed in its Q3 2024 publication of the Semiconductor Manufacturing Monitor (SMM) Report, prepared in partnership with TechInsights.

THE GROWTH is fueled by seasonal factors and strong demand from investments in AI data centers, however, the consumer, automotive, and industrial segments are experiencing a slower pace of recovery. The growth trend is expected to continue into the fourth quarter of 2024.

After declining in the first half of 2024, electronic sales rebounded in Q3 2024, growing 8% QoQ, with a projected QoQ increase of 20% in Q4 2024. IC sales also rose by 12% QoQ in Q3 2024 and are expected to grow another 10% in Q4 2024.

Overall, IC sales are forecasted to increase over 20% in 2024, primarily driven by memory products due to price improvement across the board and strong demand for data center memory chips.

Similar to the electronics sales, semiconductor capital expenditures (CapEx) decreased in the first half of 2024, but the trend is turning positive starting in Q3 2024. Memory-related CapEx is surging 34% QoQ and 67% year-on-year (YoY) in Q3 2024 reflecting improvement in the memory IC market compared to the same period of the last year. In Q4 2024, total CapEx is expected to jump 27% relative to Q3 2024 levels and 31% YoY, with memory-related CapEx leading this growth at 39% YoY.

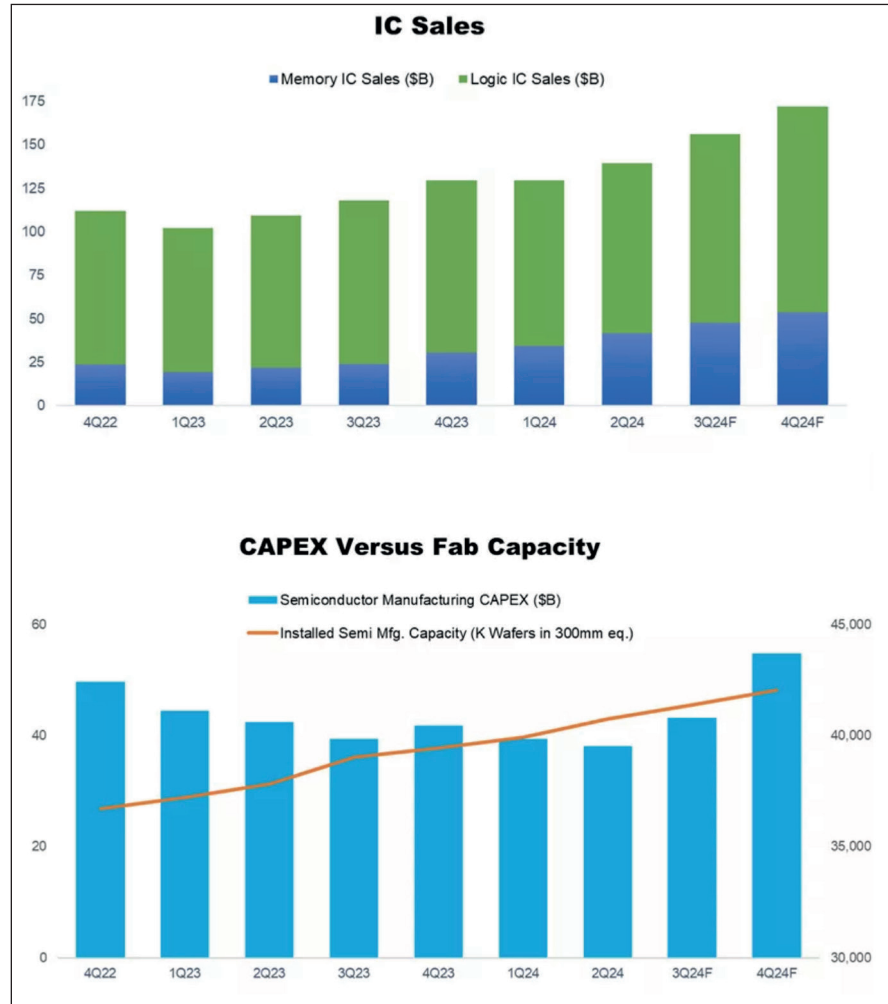
The semiconductor capital equipment segment remains strong and is performing better than previously expected due to substantial investments from China and increased spending for high-bandwidth memory and advanced packaging. Wafer Fab Equipment (WFE) spending increased 15% YoY and 11% QoQ in Q3 2024. China's investment continues to play a significant role in the WFE market.

Additionally, both the Test and the Assembly and Packaging segments experienced impressive YoY increases of 40% and 31%, respectively, in Q3 2024, and this growth is anticipated to continue for the remainder of the year. In Q3 2024, installed wafer fab capacity reached 41.4 million wafers per quarter (in 300mm wafer equivalent) and is projected to rise by 1.6% in Q4 2024. Foundry and Logic-related capacity

continues to show stronger increases, growing 2.0% in Q3 2024 and is projected to rise 2.2% in Q4 2024 driven by capacity expansion for both advanced and mature nodes. Memory capacity increased 0.6% in Q3 2024 and is forecasted to maintain the same pace of growth in Q4 2024. This growth is driven by strong demand for high bandwidth memory (HBM) but is partially offset by process node transitions.

"The semiconductor capital equipment segment continues to exhibit growth momentum, bolstered this year by strong investments from China and increased spending on advanced technologies," said Clark Tseng, Senior Director of Market Intelligence at SEMI. "Additionally, the continued expansion of fab capacity, especially in the foundry and logic segments, underscores the industry's commitment to meeting the growing demand for advanced semiconductor technologies."

"2024 has shown two sides within the semiconductor industry," said Boris Metodiev, Director of Market Analysis at TechInsights. "While consumer, automotive, and industrial markets have struggled, AI has thrived, boosting average selling prices in memory and logic products. As interest rates decrease heading into 2025, consumer sentiment is expected to improve, encouraging larger purchases and supporting both the consumer and automotive markets."



Schneider Electric recognised as a DEI leader

SEMI Europe and the SEMI European Advisory Council for Diversity and Inclusion announced Schneider Electric as the recipient of the 2023 SEMI Industry Leader in Diversity and Inclusion Award. Frederic Godemel, Executive Vice President, Power Systems and Services at Schneider Electric accepted the award presented at SEMICON Europa 2024 during the SEMI Networking Night Dinner.

"This recognition highlights Schneider Electric's steadfast commitment to creating an inclusive environment where every individual can thrive and contribute to the company's collective success," said Frederic Godemel, Executive Vice President, Power Systems and Services of Schneider Electric. "Our Multi-Hub model reinforces this commitment by fostering diverse and inclusive teams across various regions, ensuring that our global workforce reflects the communities we serve. At Schneider Electric, we believe great people make a great company, and we are dedicated to supporting their growth and well-being. We are equally committed to making a positive impact in our communities, ensuring that our initiatives promote sustainability, equity, and opportunity for all. We are deeply honored to receive this award from SEMI Europe."

"The semiconductor industry is at a pivotal moment, where embracing diversity and inclusion is essential for driving innovation and staying competitive in a rapidly changing market," said Laith Altimime, President of SEMI Europe. "Schneider Electric exemplifies this commitment by fostering an inclusive culture that values diverse perspectives. Their dedication to equity and gender equality not only enhances employee engagement but also sets a benchmark for the entire industry. By prioritizing diversity, they demonstrate that diverse teams are crucial for unlocking creative solutions and achieving sustainable growth."

The semiconductor industry is at a pivotal moment, where embracing diversity and inclusion is essential for driving innovation and staying competitive in a rapidly changing market

Arm, ASE, BMW Group, Bosch, Cadence, Siemens, SiliconAuto, Synopsys, Tenstorrent and Valeo commit to join imec's Automotive Chiplet Program

Imec invites the global automotive ecosystem to join its effort to mutually explore the opportunities presented by chiplet technology.

AT A RECENT gathering in Ann Arbor (MI), bringing together the global automotive ecosystem to discuss the evolution towards chiplets in cars (Automotive Chiplet Forum 2024), imec announced that Arm, ASE, BMW Group, Bosch, Cadence Design Systems, Inc., Siemens, SiliconAuto, Synopsys, Tenstorrent and Valeo are the first that have committed to join its Automotive Chiplet Program (ACP). The program brings together stakeholders from across the automotive ecosystem in a pre-competitive research effort unparalleled in the car manufacturing industry. The program's goal is to evaluate which chiplet architectures and packaging technologies are best suited to support car manufacturers' specific high-performance computing and strict safety requirements, while striving to extend the benefits of chiplet technology – such as increased flexibility, improved performance and cost savings – to the entire automotive industry.

Car makers have been integrating chip technology into their vehicles since the late 1970s. Lately, however, traditional chip architectures have struggled to meet the requirements of ever more demanding automotive solutions, such as advanced driver assistance systems (ADAS) and immersive in-vehicle infotainment (IVI) services. Enter chiplets – i.e., modular chips that are specifically designed to perform specialized functions efficiently and can be seamlessly combined to create more sophisticated compute systems.

"The adoption of chiplet technology would signal a disruptive shift in central vehicle computer design, offering distinct advantages over traditional monolithic approaches. Chiplets facilitate rapid customization and upgrades, while reducing development time and costs," explained Bart Placklé, vice-president of automotive technologies at imec. "However, moving to a chiplet architecture is prohibitively expensive for OEMs if done in isolation. Commercial viability thus hinges on industry alignment around a set of chiplet standards, enabling car manufacturers to procure chiplets from the market and integrate them with proprietary chiplets to build unique offerings."

In search of a chiplet architecture that combines performance, energy efficiency, robustness, cost effectiveness and customization Companies developing supercomputing, data center and smartphone solutions have long explored the benefits of chiplet technology to meet their rapidly increasing computing needs. But the automotive industry has been somewhat more reluctant to embrace the chiplet paradigm due to the unique challenges they face.

First, automotive solutions must meet strict robustness and reliability requirements, ensuring continuous operation and passenger safety over a car's typical lifespan of ten to fifteen years. Moreover, cost is another crucial factor to consider. And, finally, superior performance and exceptional energy efficiency are critical to preserving a car's battery life. These are some of the urgent issues imec's Automotive Chiplet Program will address.

A pre-competitive, collaborative research effort unparalleled in the automotive industry

Imec's Automotive Chiplet Program leverages imec's world-leading track record in advanced 2.5D and 3D packaging with resources and expertise

from different parts of the automotive value chain. Bart Placklé: "The agility of chiplets will allow the automotive ecosystem to respond quickly to changing market demands and technological breakthroughs. They also facilitate flexible component integration, limiting the risk of vendor lock-in and improving supply chain resilience. In addition, their optimized performance leads to lower power requirements, enabling compact device design."

"We are convinced that all stakeholders will gain important insights from the program's pre-competitive, collaborative approach – leveraging the partners' collective wisdom and means to make rapid progress. The valuable precompetitive learnings from the program can be instantiated in further R&D and product innovation to accelerate the partners' own differentiating, long-term roadmaps.

In fact, this methodology mirrors the successful practices established in the semiconductor industry over the past four decades. With 40 years of experience in designing, building, and optimizing chip architectures and technologies, and without allegiance to any stakeholder in the automotive ecosystem, imec is uniquely positioned to guide the car manufacturing industry towards the development of a groundbreaking new chiplet architecture tailored to the sector's specific needs," he concluded.

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Evolving the semiconductor industry with AI and simulation

It's no secret that the semiconductor industry has been in a state of flux since generative AI exploded into the mainstream. And as adoption of both AI models, and AI-powered smart products, continues to increase, so will the already extreme demand for semiconductor chips.

BY MAZEN EL HOUT, SENIOR PRODUCT MARKETING MANAGER, ANSYS

THE SEMICONDUCTOR INDUSTRY is now on the front line of innovation, with Gartner predicting that global revenue will increase by 14% in 2025, totalling $717bn. Yet, the industry is scrambling to keep up with demand. Continued investment is supporting efforts; in the UK, for instance, £11.5m has been set aside to support semiconductor innovation and evolve the £10bn industry. Yet, the complexities of chip design and manufacturing, and skyrocketing demand following a global shortage, require increasingly sophisticated technologies.

Naturally, chip manufacturers are turning to tools like simulation and generative AI to overcome these challenges. By doing so, they can evolve intricate processes that traditionally consume vast amounts of time, money, and engineering resources. They can also explore how to support sustainable semiconductor manufacturing, without compromising on innovation. And beyond the semiconductors themselves, manufacturers can develop fabrication plants, or fabs, to drive development at scale.

The fact is, simulation alone can be immensely beneficial for chip manufacturers; generative AI just takes its capabilities a step further. But how exactly does this two-pronged approach work? With this in mind, let's explore how simulation is already supporting chip manufacturing, and how AI can evolve design and development to push the boundaries of innovation and meet global demand.

The overarching benefits of leveraging simulation and generative AI

In the case of semiconductors, simulation can help engineers validate characteristics that would otherwise be difficult, time-consuming, and costly to physically test. And since simulation can identify critical design flaws before a semiconductor is built – be it a single chip or a giant factory – it can accelerate the overall development cycle and reduce time to market, a crucial objective for manufacturers.

But whilst simulation does play a vital role across semiconductor manufacturing, its benefits can be further enhanced through the power of generative

AI. When a model is trained on specific data, it can produce accurate predictions in minutes, drastically cutting down computing time. As such, engineers can quickly adjust design parameters and receive immediate feedback through real-time simulations. Ultimately, this creates a loop; the more data the simulations generate, the more efficient and accurate the AI model will be. And in, for instance, the design process, this approach can be the difference success and failure.

Supporting reliability assessments in chip design

Chip design is neither swift, nor simple. Manufacturers usually have to deal with nonlinear, unexpected behaviour, and need to take electrical, thermal, and structural characteristics into account; even the slightest modifications or error can impact other components. Additionally, engineers can struggle with successfully mapping spatial distribution uncertainty and variations in chip parameters, including die size and heat transfer coefficient (HTC) values. Whilst simulation as a standalone tool can support here, engineers risk spending unnecessary time simulating, modifying, and re-simulating a single chip, and the overall complexities of the design process mean that scalability is limited.

Again, complementing simulation with generative AI can add additional benefits, alleviating these challenges. Take a thermal analysis as one example; if an AI model is trained on datasets generated from thermal simulations, it can quickly generate a temperature distribution map and accurately pinpoint thermal critical locations. This empowers engineers to make the right design modifications that can ultimately optimise thermal performance, manage temperature fluctuations, and mitigate overheating issues. But reliability assessments are just one piece of the puzzle. To meet global demand, chip manufacturers need to be able to experiment with more innovative and sustainable design choices.

Powering sustainable semiconductor innovation
Sustainability is influencing product design across every sector; the semiconductor industry is no exception, thanks to its significant environmental output. For instance, fabrication plants require significant amounts of water and energy to manufacture chips, whilst a complex global supply chain – including the extracting of large amounts of raw materials, and worldwide distribution – contribute to greenhouse gas emissions. In conjunction with this, many consumer products that rely on semiconductors, like smartphones and laptops, are designed with planned obsolescence in mind. This means that more chips are being discarded, keeping demand up and generating material waste.

Improving sustainability in the semiconductor industry calls for a collective effort. But there are steps manufacturers can already take here, like combating waste reduction in chip design. Simulation can be of use here; for instance, it can identify areas of excessive power consumption and optimise energy efficiency. Simulation also calls for fewer physical prototypes are made, so less waste is created. So where does AI fit in? The technology allows engineers to gain insights into the material process-property relationship through AI-based material selection. Essentially, a manufacturer's material data is used to predict how different materials can impact product design and performance, which enables better decision-making for sustainable design. Evidently, giving manufacturers next-generation tools and technologies can open the door to new innovations in the chips themselves. But how can AI-infused simulation support the industry on a larger scale?

Overcoming fabrication plant challenges to enable innovation at scale

Chip design isn't the only focus for manufacturers. To sustain the global supply chain, fabrication plants need to evolve their capabilities, but this comes with its own challenges. As fabs strive to keep up with the pace of demand for chips, equipment can run continuously for weeks or even months at a time, increasing the chance of machinery fatigue and running the risk of costly and time-consuming maintenance. And if failures do unexpectedly occur, organisations must decide between halting production immediately, or waiting for a scheduled maintenance window. Since a single tool failure can have an impact on the entire manufacturing process, organisations can't afford to gamble on the health of their operational equipment.

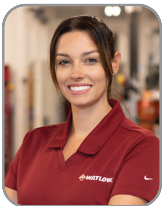
Manufacturers must mitigate fatigue and failures to avoid disrupting these highly interconnected processes. And to do so, they can look to AI-powered digital twins. These connect data from physical semiconductor manufacturing assets to their simulated counterparts, allowing engineers to monitor equipment health in real-time, and predict issues before they occur. Moreover, if the AI model is lacking data on specific defects, it can create a synthetic dataset to incorporate this and train the digital twin. By working in tandem, AI and simulation will allow semiconductor manufacturers to maintain operational efficiency, avoid production downtime and better anticipate maintenance.

The future of semiconductor manufacturing
For semiconductor firms, the demand for chips isn't slowing down. But the right tools can be crucial in helping bolster supply and maintain a competitive edge – and, naturally, AI is the common thread. AI-accelerated solvers, AI-powered digital twins, and AI-based material selection are just three examples of how technology can evolve processes, underpin advances in design, and keep operations running smoothly. And the organisations that invest in these capabilities now will be better positioned to dominate the supply chain and pave the way for the future of the semiconductor manufacturing.

Advancements in semiconductor subfab maintenance through Industry 4.0 technologies

The semiconductor industry is driven by relentless innovation, with each advancement pushing the boundaries of technology and efficiency. Industry 4.0 introduces a suite of smart technologies that can transform maintenance and operational safety in semiconductor manufacturing. It represents the integration of advanced digital technologies into manufacturing processes, utilizing sensors, data analytics, automation, and real-time monitoring – all critical in managing the complex and sensitive processes involved in producing semiconductor devices.

BY CHELSEA HOGARD, ENGINEERING TEAM LEADER, INDUSTRY 4.0 DEVELOPMENTS AT WATLOW



THE IMPLEMENTATION of smart technologies facilitates significant improvements in leak detection and operational optimization in subfabs—critical elements in maintaining the high standards of performance and safety that the industry demands. Through its in-depth understanding of heater technology and subfab processes, Watlow has designed solutions for thermal pattern analysis and power consumption monitoring to enable facilities to receive early warnings of potential system inefficiencies, ensuring that semiconductor facilities operate at their peak without compromising safety.

Advanced leak detection through thermal pattern analysis

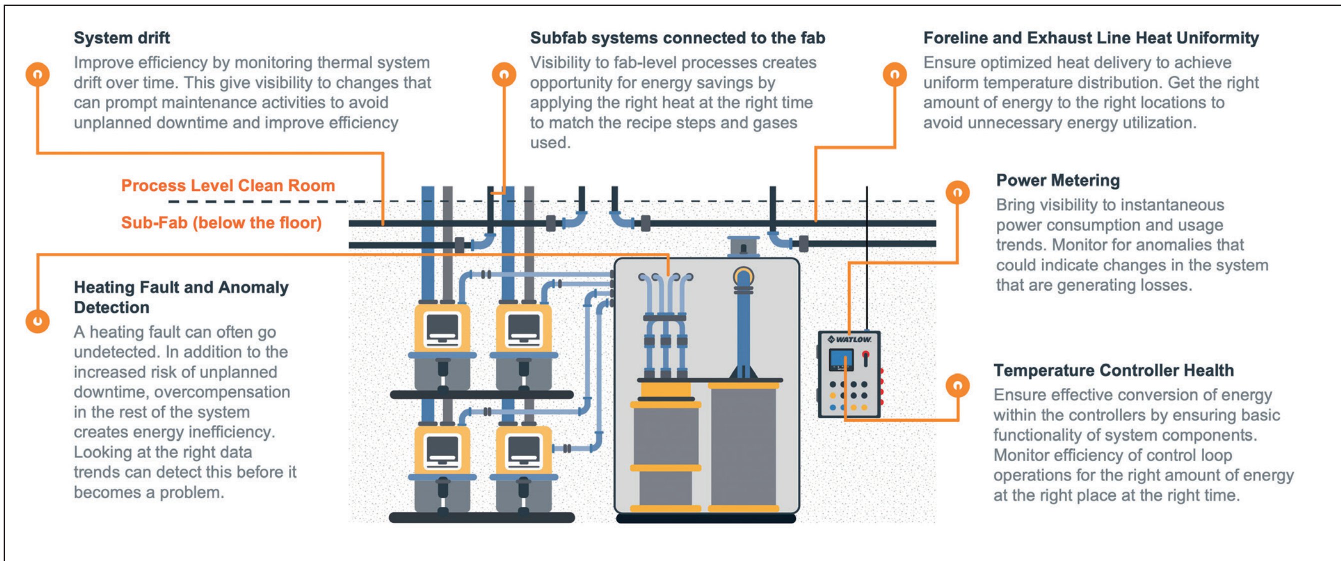
Leak detection in subfabs is not merely about preventing downtime due to equipment failure; it is also integral to maintaining the safety and integrity of the entire operation. Traditional methods of leak detection have often been reactive, identifying problems only after they have caused significant disruptions. However, recent innovations have shifted the focus towards a more proactive approach using thermal pattern analysis.

In a subfab environment, where miles of piping are essential for the transport of various gases and chemicals, the potential for leaks, particularly at vulnerable points like flange connections, is a constant concern. By leveraging thermal pattern analysis, semiconductor facilities can monitor temperature variations along these pipes in real-time. Sensors strategically placed along the piping detect even minor deviations from normal temperature patterns, which can indicate the presence of leaks. For example, signal changes in temperature and power data can signal that a leak has occurred, causing the material inside the pipe to react with external elements, potentially leading to dangerous outcomes like pyrophoric events.

This method is particularly effective because it allows for the detection of leaks long before they become critical issues. Early detection not only prevents damage to equipment but also mitigates the risks of safety hazards, such as fires caused by leak-induced reactions with pyrophoric gases. Identifying and addressing these leaks promptly is a significant step forward in subfab safety and efficiency.

Power consumption data, when analyzed in conjunction with thermal patterns, offers a comprehensive picture of the subfab's operational status. This dual approach allows for more accurate diagnostics and timely interventions. By understanding where and how power is being consumed, operators can identify areas where efficiency can be improved or where potential problems may arise. For example, if certain zones within the subfab are consuming more power than expected, it could indicate that those areas are

➤ Right: Loose insulation has the potential for multiple costly problems: Overheating, higher power cost, downtime. Monitoring power usage identifies issues so action can be taken.



compensating for inefficiencies elsewhere, such as a misaligned heater or an obstruction in the piping that requires additional energy to maintain the desired temperature.

Real-time monitoring and predictive maintenance

While current systems often rely on monthly reports to analyze thermal and power data, the future of subfab management lies in real-time monitoring and predictive analytics. The goal is to move towards a system that not only monitors conditions as they happen but also predicts potential issues before they occur.

To achieve this, semiconductor facilities are increasingly adopting advanced data acquisition edge solutions that integrate with existing control systems. As these panels collect detailed data from various sensors, machine learning algorithms can be developed and deployed on the edge to analyze this information in near real-time. The result is a system that can alert operators to potential issues, such as leaks or clogs, before they cause significant damage or downtime.

The shift towards predictive maintenance is a game-changer for the semiconductor industry. By continuously monitoring the health of the subfab and predicting when and where issues might occur, facilities can schedule maintenance more effectively, reducing downtime and improving overall operational efficiency. Moreover, this approach enhances safety by ensuring that potential hazards are identified and mitigated before they can escalate.

Real-world applications of advanced leak detection

The practical benefits of these innovations are best illustrated through real-world case studies. In one instance, a semiconductor facility identified a significant leak in its subfab piping through the combined analysis of thermal patterns and power consumption data. The leak, which was initially detected through changes in power consumption, was found to be cooling the air around it, causing a clog to form in the pipe. By identifying this issue early, the facility was able to schedule maintenance before the clog became a major problem, avoiding costly downtime and potential safety hazards.

In another case, power consumption data revealed an unexpected increase in energy usage in certain zones of the subfab. Upon further investigation, it was discovered that a heater had been left unplugged after a maintenance event, causing the system to consume more power to maintain the necessary temperature. Through Watlow's analysis of the data, the facility was able to quickly identify and rectify the issue, optimizing the system's performance and preventing further inefficiencies.

Conclusion: Enhancing Efficiency and Safety in Semiconductor Subfabs

The innovations in leak detection and operational optimization in semiconductor subfabs represent a significant advancement in the industry's ability to maintain high levels of efficiency and safety. By leveraging thermal pattern analysis and power consumption monitoring, facilities can detect and address potential issues before they lead to costly and dangerous problems. As the industry continues to move towards real-time monitoring and predictive maintenance, these innovations will play an increasingly critical role in ensuring that semiconductor fabs operate at their peak, delivering the performance and safety that the industry demands.

These technologies are not just about improving efficiency—they are about creating safer, more reliable semiconductor manufacturing environments. As the semiconductor industry continues to evolve, the integration of advanced monitoring and predictive analytics will be essential in maintaining the cutting-edge performance that drives the technology forward.

> Monitor systems to address issues before they become problems.

Making sure that AI and High Bandwidth Memory stack up

A Q and A on Lam Research technology solutions designed to address the AI-fuelled demand for High Bandwidth Memory.

WITH AARON FELLIS, CORPORATE VICE PRESIDENT AND GENERAL MANAGER OF WET EQUIPMENT TECHNOLOGY SYSTEMS AT LAM RESEARCH

PA: *This new world of AI requires High Bandwidth Memory (HBM). Why is HBM so critical to the performance of GPUs and, by extension, the advancement of AI?*

AF: GPUs are critical to generative AI, but arguably just as critical are the semiconductor innovations that support it — particularly HBM.

GPUs have become the standards for AI training. However, inference from cloud to edge is creating tension between traditional CPU architectures and accelerators as companies try to balance infrastructure performance and efficiency. These solutions share the challenge of feeding huge data sets into incredibly fast processing complexes.

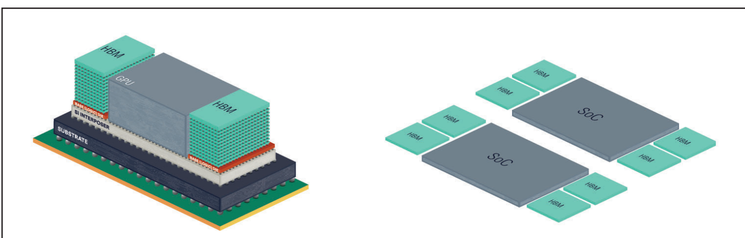
While traditional memory may bottleneck with increasing AI workloads, HBM — a newer form of high-speed memory — provides greater bandwidth and power efficiency to deliver these data sets with near lightning speed. In an HBM chip stack, multiple layers of DRAM chips are vertically integrated, which enables the rapid data exchange needed to perform complex AI tasks.

> In an HBM chip stack, multiple layers of DRAM chips are vertically integrated to enable the rapid data exchange needed for complex AI tasks.

HBM leverages 2.5D and 3D stacking and cutting-edge packaging to deliver improved memory bandwidth while achieving better power efficiency and a smaller footprint than traditional memory alternatives.

PA: *How do 2.5D and 3D stacking and 'cutting edge' packaging deliver improved memory bandwidth and higher efficiencies?*

AF: Semiconductor breakthroughs, particularly advanced packaging, are enabling the creation of new HBM memory to meet the performance and unique demands of generative AI applications. Advanced packaging technologies, such as 2.5D and 3D integration, allow for the stacking of memory and logic chips. Stacking relies on through-silicon vias (TSVs) and microbumps. The more TSVs in a chip stack, the higher the interconnect density. This also means data can travel faster and more efficiently.



But as more TSVs are created, their openings get narrower. When this happens, the relative height to that opening (aspect ratio) increases, which makes the electrofill process much more challenging. Proper filling of TSV structures and creation of microbumps is essential to stack HBM chips.

Meanwhile, 2.5D today uses multi-layer submicron metal lines on a silicon interposer to connect multiple dies horizontally and as close possible with minimal routing. These metal lines are formed using fab-based metal damascene processes which include dielectric deposition, etching, cleaning, metal deposition, and, finally, polishing.

PA: *New HBM requires a complex set of manufacturing steps – tell me about this?*

AF: HBM has many advantages, but it is not without technical challenges. In the manufacturing of HBM, extremely narrow and tall features must be created with very high precision and repeatability.
TSVs, for example, require difficult, multi-step processing. Plasma-based deep silicon etch process tools are used to selectively remove silicon to precisely form uniform, high aspect ratio holes.

After cleaning and depositing oxide materials and barrier seed, the microscopic holes are filled through advanced copper electroplating, with care taken that the fill is void-free. At every step, sophisticated tools and equipment play an important role in helping to create consistent and predictable yield.

Lam Research brings expertise in advanced deposition, etch and clean packaging technologies to help chipmakers address manufacturing

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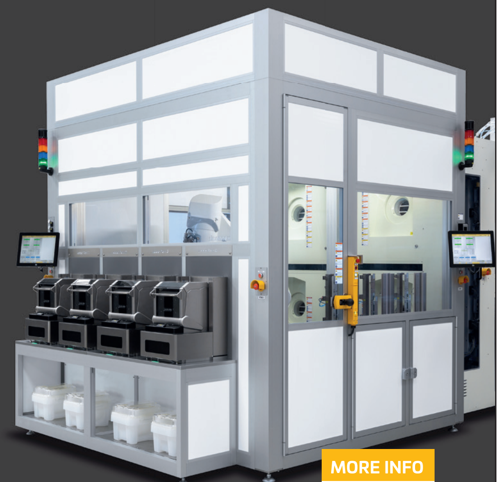

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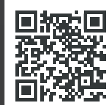

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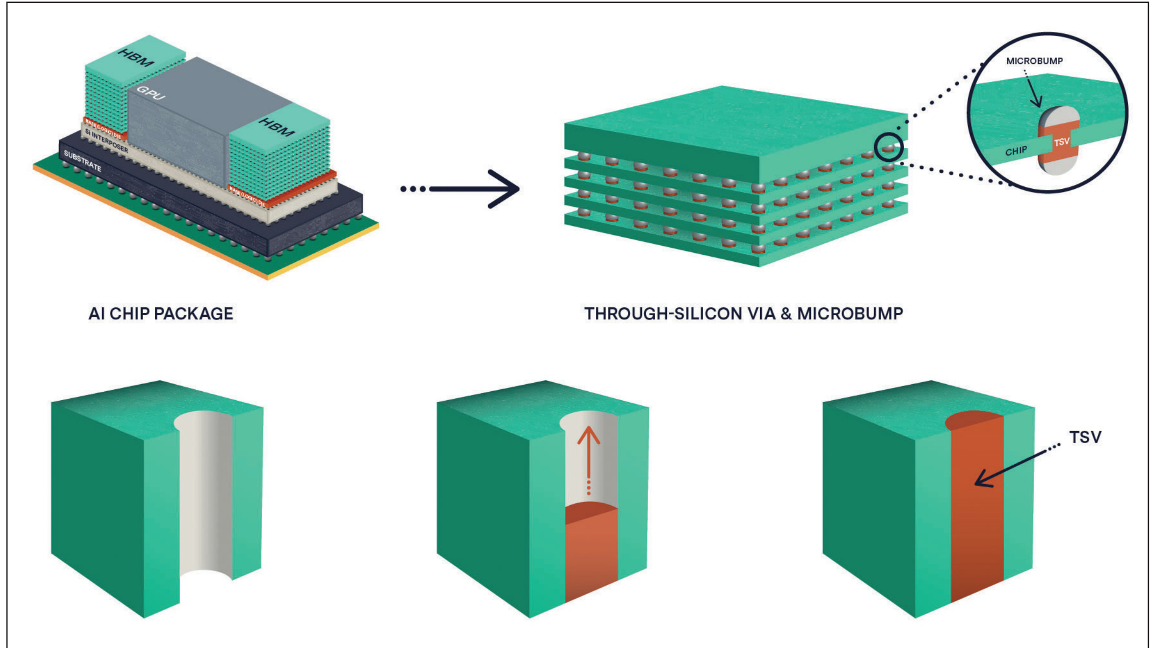

TSV and microbumps are critical to enable high-density 3D stacking of memory dies. Major TSV formation steps include uniform deep silicon via etch and fast, void-free, bottom-up copper electro filling.

challenges and ensure that HBM devices meet the stringent performance and reliability standards required by AI applications.

PA: *What are some of the Lam tools and technologies involved in 2.5D and 3D stacking?*

AF: Lam provides an industry-leading portfolio of solutions for advanced packaging and 2.5 and 3D stacking. It includes SABRE® 3D, Striker® and Syndion®, which deliver precision and uniformity at the atomic level. These tools are critical enablers of HBM manufacturing and are used by all major memory manufacturers.

- SABRE® 3D electrofill tool is used to metalize TSVs. It fills the etched vias with copper, ensuring solid electrical connections between the stacked layers. This process is crucial for maintaining the performance and reliability of HBM devices.
- Striker® atomic-layer deposition (ALD) delivers an oxide liner that is necessary for TSVs because it helps isolate the copper that is deposited with SABRE 3D. It also reduces process times by using rapid cycles and ALD-rated components, software, and controls.
- Syndion® etch technology uses deep reactive ion etching to deliver a smooth and repeatable profile at a high etch rate. Rapidly alternating process (RAP) — quickly switching between etch and deposition steps during manufacturing — enables the creation of deep, uniform TSVs while protecting sidewalls.

PA: *How are tool vendors, such as Lam Research, developing packaging innovations and collaborating with customers to deliver them?*

AF: Leveraging our expertise in etch, deposition and clean processes, Lam continually collaborates with chipmakers to understand their needs and deliver innovative products,

technologies and solutions that address their scaling challenges. We identify the most efficient and cost-optimized way to deliver on a customer's technical requirements with the fastest processing speed. This allows them to benefit from the most efficient use of capital equipment in their factories and accelerate their abilities to deliver on their HBM product roadmaps.

PA: *We've covered quite a lot of ground. If you can, please summarize just how you see this AI opportunity playing out for the semiconductor industry, and Lam Research in particular?*

AF: Advanced packaging solutions like HBM are critical approaches for chipmakers to optimize the performance, power, form factor, and cost of their devices. But continuous innovation in chip design and manufacturing processes will be necessary for HBM to propel the AI era. Lam's expertise and innovations in etch, deposition, and advanced packaging make it well positioned to meet the manufacturing requirements for HBM.

Advanced packaging solutions like HBM are critical approaches for chipmakers to optimize the performance, power, form factor, and cost of their devices. But continuous innovation in chip design and manufacturing processes will be necessary for HBM to propel the AI era

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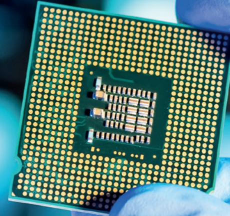


Reduction of outgassing and elimination of contaminants is a pressing need for an industry spanning a wide variety of new markets.

BY JASON DAVIS, NEW BUSINESS DEVELOPMENT, JUNKOSHA USA INC.

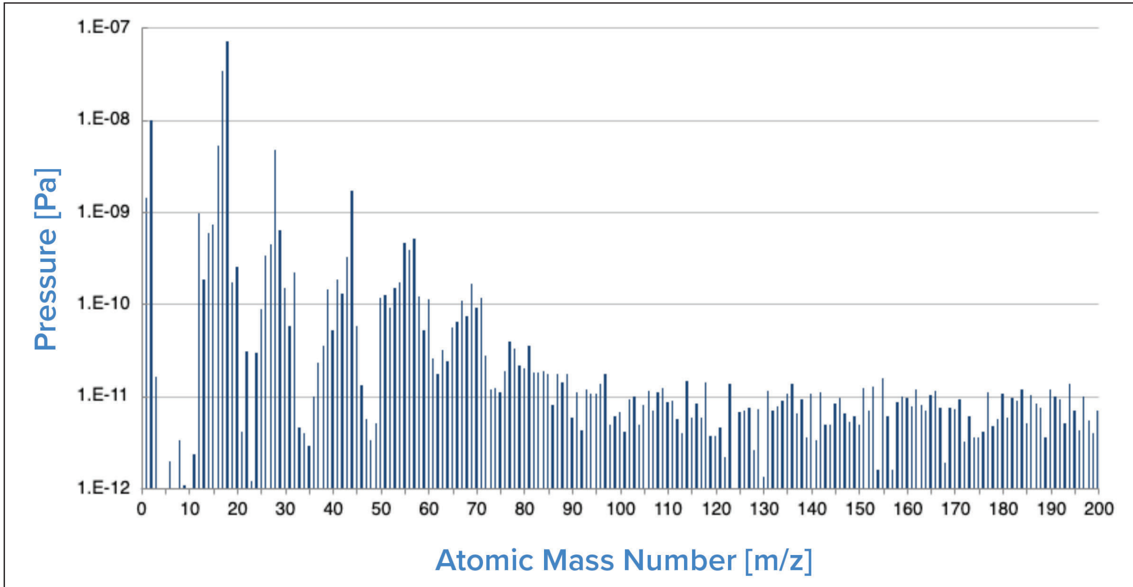
THE GLOBAL SEMICONDUCTOR manufacturing industry is in the throes of change. The last several years have welcomed a new set of challenges that have impacted the industry and propelled it towards innovation. Major trends and requirements are coming to the forefront that will define the future of the semiconductor manufacturing industry, including ensuring supply chain resiliency; the rise of generative AI; fast scalability; meeting OEM's growing needs across a multitude of markets; navigating geo-political tensions; and developing a diverse workforce. Traditional semiconductor manufacturing processes have inherently weak links and limitations in the ability to manufacture next generation chips which are produced in clean rooms containing a range of equipment used to manufacture CPUs and other advanced semiconductors.

The manufacturing equipment used can include more than 50 different units ranging from epitaxial reactors and chemical vapour deposition systems to photolithography equipment. It is often processes that include ultra-high vacuum (UHV) that dictate the success or failure of product quality and yield in the quest for scalability of advance semiconductor chips.

The semiconductor industry continues to grow at a rapid pace with Moore's law – double the performance, halve the cost - looming above like a long shadow. Amid today's technological advances what has changed, however, is the influence of several global trends including the rise of Artificial Intelligence (AI), electric vehicles and autonomous driving. In the past, semiconductor growth was attributed to personal computer and mobile innovation but today semiconductor influence is seen in virtually every industry in the modern global economy with even more anticipated breakthroughs to continue as 5G wireless technology broadens demand over the next decade.

An average electrical vehicle, for example, contains 1000-3500 semiconductors used for parts such as MCUs and analog for electric power steering to boost fuel efficiency.[1] Given the advancement of automotive intelligence, rapidly changing communication trends and electrification in general, the demand for semiconductors in a multitude of markets will continue to be steady and long-term.

Even as traditional uses for semiconductors continue to exist in high demand, the proliferation of key trends such as hyperscale cloud computing, Internet of Things (IOT) and AI have piled on to the growth trend. Thanks to the increasing need for higher computing power, data processing capabilities, complex language models, and big data analytics in data centers, this technology has very quickly evolved out of its prototype phase and expanded beyond the data center, reaching



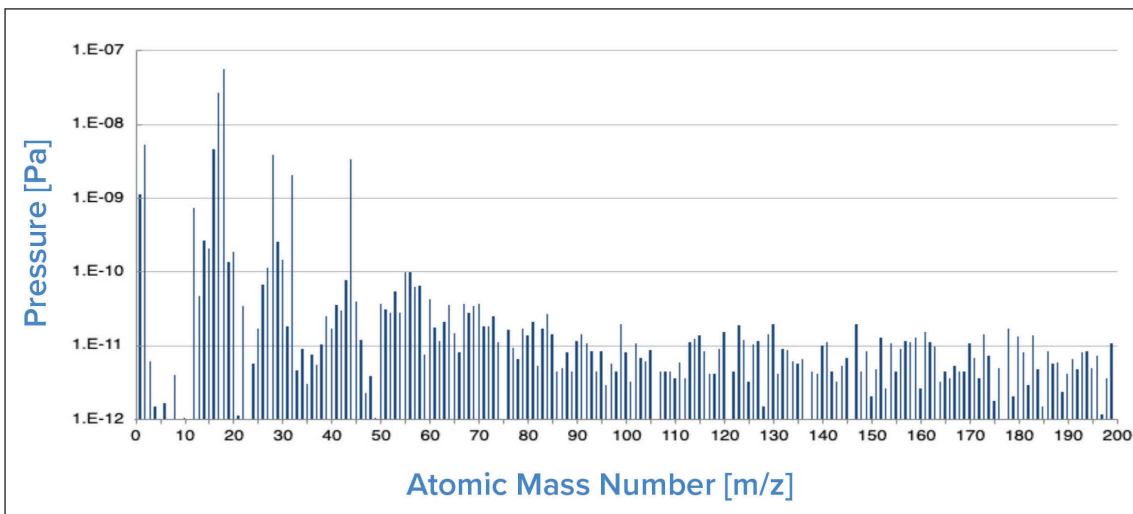
➤ SLO Cable*

personal devices driving demand for AI powered chips. McKinsey estimates that the global market for semiconductors is projected to reach $1 trillion by the end of the decade.[2] What all of this means is that the production of semiconductors, often seen as the brain of digitization, will remain one of the most valued and traded goods in the world.

In addition, increasing demand from a wider variety of sectors, such as automotive and defense, is pushing semiconductor manufacturers to produce smaller, faster and smarter chips at scale. Moore's law has had the industry increasing transistor densities roughly two times every two years[3], which requires manufacturing to continually refine all of its processes. Today, Taiwan Semiconductor Manufacturing Co. (TSMC) transistors are down to just over two nanometers – the smallest in the world with Intel's transistor density soon to be on par[4]. The pursuit of these more advanced and powerful chips has led to increasing process complexity because wafer manufacturing is a cycle of defining features with lithography and building them up with deposition, etch, and other process steps to meet key requirements. With ever-shrinking chip features comes mutually with the need for more stringent outcomes, necessitating new equipment with highly controlled environments to minimize contamination of sensitive machine components.

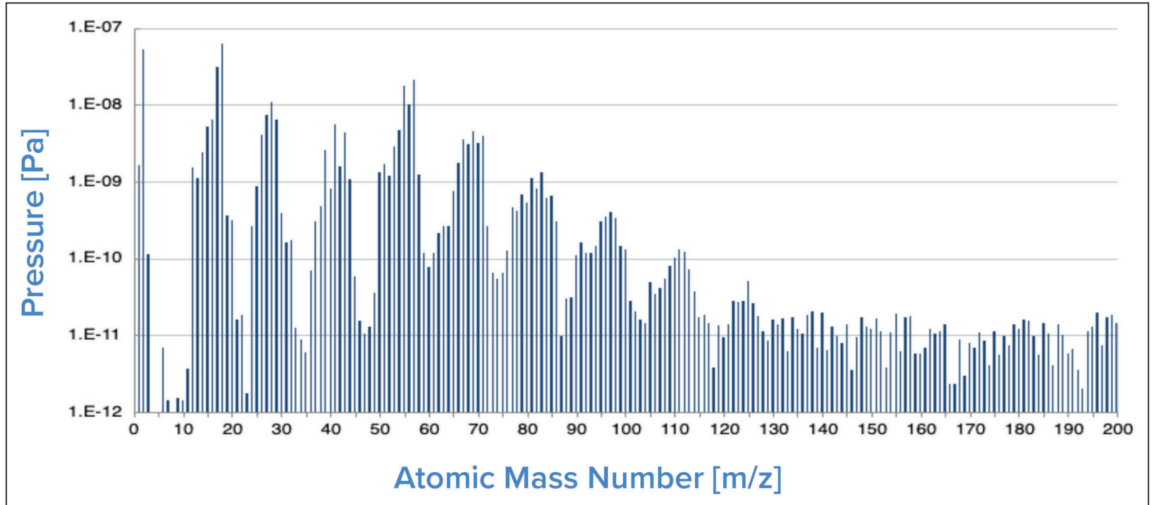
Manufacturing a microchip is no small feat. To make any chip, numerous processes play a role and precision is key.[5] As chipmakers push towards smaller nodes, stringent control of molecular contamination becomes critical. Fabs face many hurdles to trust that their metrology equipment is giving them an accurate read of what occurs on the wafers they are processing. For semiconductor processing and fabrication equipment designers and manufacturers, control of airborne particle concentration by introducing vacuum environments is becoming equally crucial.

Extreme ultraviolet (EUV) lithography is seen as one of the biggest breakthroughs for advanced semiconductor manufacturing as the central process for high-volume semiconductor manufacturing. Particle interference, refraction and other physical



➤ Background Empty Chamber*

Conventional ePTFE Cable*



or chemical defects that occur during this process can massively increase manufacturing costs and significantly increase yield losses. As such, the key challenges in EUV lithography, particularly in semiconductor manufacturing cleanrooms, stem from the need to control molecular contamination.

How does the industry keep up with the increasing challenges?

The industry is approaching the problem from several angles. One key approach involves manufacturers turning to advanced materials and techniques to limit outgassing and maintain a pristine vacuum environment, ensuring that lithography systems can operate with the high precision required for producing next-generation chips. Outgassing occurs when materials, such as cables or other system components, release volatile compounds into the vacuum environment, which can lead to contamination. Additionally, the complexities involved in EUV lithography extend beyond contamination control. The sheer intricacy of the equipment, high costs, and the necessity for a well-trained workforce further complicate its implementation in semiconductor production lines. As a result, cleanroom environments must now be more sophisticated and rigorously maintained to support these operations.

In response to this challenge, Junkosha has developed the cleanest cable assemblies in the semiconductor manufacturing industry to date. Using proprietary manufacturing steps, Junkosha Super Low Outgassing (SLO) cables have the lowest outgassing and particulation levels available on the market, enabling semiconductor manufacturers to maintain an extremely clean environment within their systems. In addition, Junkosha's cables combine a high level of mechanical flexibility with the ability to integrate multiple cables making it ideal for vacuum chamber environments with moving parts such as linear stages integrated with motors and encoders.

Semiconductor manufacturing is dependent on vacuum technology because it plays an integral part in the efficiency of processes and yield, particularly when producing advanced chips. Ultra-high vacuum in a processing chamber is generally achieved using a turbomolecular pump located at the processing tool followed downstream by a dry vacuum pump. These sensitive process chambers demand high performing materials that also relates to cabling that are utilized for data and power transmission. In all vacuum (and non-vacuum) processing equipment, residual gases may originate in the process chamber and even from the contaminated silicon substrates. In the graphs below, we see the results of the RGA test[i] conducted over 240 minutes on both the SLO cable and a conventional ePTFE cable.

Semiconductor manufacturing requires precision at a swift pace. Because velocity and precision are generally at odds - you move fast, you break things or at a minimum, make unusable product- achieving increased throughput and higher wafer-per-hour speeds places the highest demand on all mechanical components, including cables. By deploying an SLO cable, manufacturers can drastically cut down on the outgassing molecules that latch on to sensitive components such as mirrors and compromise image quality, which directly correlates with the quality of the chip circuitry.

Moreover, SLO cables enable manufacturers to reach the required vacuum levels much faster. This provides an ultra-low pressure environment utilizing vacuum pumps to create advanced chips. Cables and other polymer-based products which do not emit outgas are essential to the success of overall system output.

The graph on the next page breaks down how vacuum levels shift over time across three key factors. The blue line represents the background, while the red line shows our conventional cable which fails to hit the 10^-5 Pa vacuum pressure mark even after 480 minutes. In contrast, the yellow line tracks the SLO cable, reaching that same pressure in just half the time—240 minutes. As a result, there is

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a substantial reduction in time for customers, driving more efficient operations.

The challenges faced in boosting production

Optimizing process flows has the same level of focus for fabrication equipment designers and manufacturers as it has for fabs. As fabs boost production of silicon chips they simultaneously churn out more liquids, slurries, and gases around the facility placing more pressure on both process and material-handling equipment. This challenge intensifies as line diameters and wafer thicknesses decrease, pushing equipment to meet increasingly stringent requirements. Wet chemical processes used in etching, cleaning, and other stages in chip manufacturing rely on carefully controlled transport of chemicals.

These liquids must be handled in properly sealed containers to prevent leakage of gases or fluids that could compromise safety or purity of the product. Beyond resistance of aggressive chemicals, the materials used must also not contribute organic or trace metallic contamination which could otherwise degrade the effectiveness of the cleaning or stripping fluids.

To address this challenge, manufacturers must use the right equipment to prevent deterioration and gas permeation. PFA stands out as one of the very few materials that is inert, stable, and impermeable enough to handle the aggressive chemicals used in fabs and to keep ultrapure chemicals – including water—free from particles and leachates. Currently, Junkosha High Barrier PFA Tubing is the most durable tubing solution available for piping in wet processes in semiconductor manufacturing. Developed with two heat fusion bonded layers, it has an excellent barrier against strong acids, alkalis and organic solvents, resulting in a reduction in the number of replacements needed.

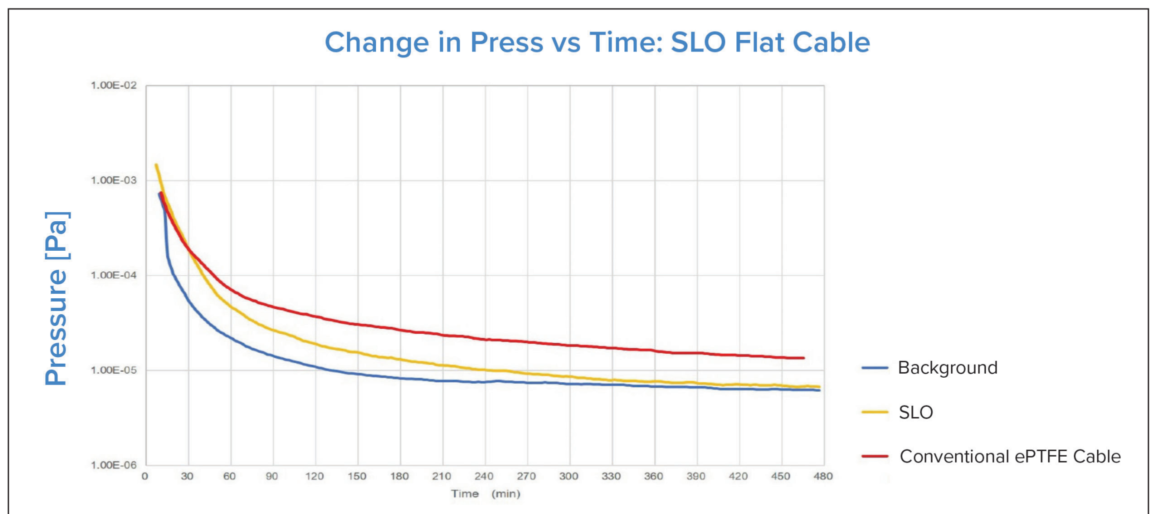
The inner layer, made from high purity PFA, offers chemical resistance, heat durability and adhesion resistance. The outer layer is made from fluoropolymers with excellent barrier properties against acids (for example hydrochloric acid and nitric acid) from the inside and water vapor from the outside.

Furthermore, the tubing maintains transparency over a long period of time, which is an indicator of lack of tube deterioration. For fabs seeking to reduce downtime, the High Barrier PFA Tubing is the ideal solution due to its unique ability to manage the flow of highly toxic and corrosive materials, helping to reduce maintenance and corrosion of surrounding metal parts.

Safeguarding production output

All manufacturing in the world is built upon stacking multiple processes and systems with various tolerances and variation ranges to get a consistent product. Nowhere is this more evident than in semiconductor manufacturing due to being the single most complicated manufacturing process with the lowest tolerance for error in the world. The global semiconductor supply chain is a web of interdependent, critical links that would take trillions of dollars and at least a decade to fully reconstruct. While TSMC in Taiwan and ASML in the Netherlands are the typical examples of dependencies, there are many more similar representations within the semiconductor supply chain ranging from equipment to chip design. These supply chain dependencies call for businesses to understand the semiconductor industry supply chain's vulnerability to safeguard production output.

This has brought to the forefront supply chain specialists who possess expertise in the processes surrounding chip production that can make or break the successful fulfilment of orders. Their focus is on strategies that can help the industry curb the bottlenecks for advanced semiconductor manufacturing as demand continues to outstrip supply. For example, delivering quality products is a collective requirement for the entire supply chain.



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Contact: Jackie Cannon at jackie.cannon@angelbc.com

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Given the high R&D investment costs and large capital expenditures, subpar products would have severe ramifications. Even if the physical damage to the fab is avoided, inconsistencies in materials means that equipment breaks down faster and critical chemicals such as photoresist can cause significant variations in circuit lines, potentially grinding fabs to a halt. Similarly, any particulates or molecular contamination caused by outgassing from machine cabling when the cable is bent or moving within the vacuum can condense on sensitive components like electronics, lenses and mirrors or even on the wafer itself, and therefore would have severe consequences.

Consistent manufacturing and stringent quality control measures at every step of the process ensure that Junkosha's products are trusted for precision and performance. Junkosha Super Low Outgassing Cable portfolio uses a highly controlled end-to-end manufacturing process, starting from our in-house material development of PTFE composite films. After careful material selection, Junkosha conducts a series of stringent cleaning, outgassing and particle reduction steps throughout each part of the complex production process, including planning and design, cable manufacturing, assembly, packaging and RGA evaluation. Through these highly controlled production steps, Junkosha optimises the delivery of high quality cable products with extremely low outgassing and low particulation characteristics. By incorporating these benefits with a long and durable cable life, semiconductor manufacturers achieve a reduction in equipment downtime and a significantly lower number of maintenance interventions.

Conclusion

As semiconductor manufacturers race to meet the demands of new and emerging markets, they are confronted with a complex web of challenges – from maintaining clean room integrity to supply chain complexities across various process technologies.

The need to reduce outgassing and eliminate contaminants is more important than ever as the industry expands into areas like autonomous driving, AI, IoT, next generation mobile electronics and beyond. At the center of these changes is a dependency on vacuum environments that either make or break the quality and scalability of modern chip production. In this evolving landscape, success will depend not just on the technological advances but also on securing long term resiliency of the supply chain with top quality equipment. The future of semiconductors is being shaped in real time and those that are ready to confront the current weak links in manufacturing processes will be the ones leading the charge.

FURTHER READING / REFERENCE

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i RGA testing equipment available for planning and design purposes only

* All tables represent internal tests conducted by Junkosha

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Event-driven architecture: the backbone of the high-tech smart factory

As manufacturing advances into Industry 5.0, the landscape is rapidly transforming to focus on real-time data sharing and seamless machine-to-human collaboration.

BY TOM FAIRBAIRN, DISTINGUISHED ENGINEER, SOLACE

AT THE HEART of this shift lies event-driven architecture (EDA), a technological framework enabling factories to operate with greater agility, responsiveness, and integration across diverse systems. By replacing traditional, batch-based data handling and bridging the IT/OT divide with real-time event streaming, EDA allows factories to achieve smarter, faster, and more adaptable production. This shift is key to realising the vision of a high-tech, event-driven manufacturing future.

Understanding EDA in the context of smart factories
Event-driven architecture is a modern approach to data flow in which systems detect, capture, and respond to events as they occur rather than relying on scheduled updates or centralised processing. In the context of a smart factory, these events could range from equipment malfunctions to fluctuations in supply levels or shifts in customer demand.

Unlike legacy systems, where applications would only update periodically or in a batch format, EDA allows for real-time event publication on an event mesh. This mesh functions as a universal data fabric, securely routing information to any application or system that needs it, instantly and seamlessly.

For instance, consider a production line breakdown in a high-tech manufacturing setting. Using EDA, this incident is immediately published as an event on the event mesh, alerting interconnected systems, such as the Manufacturing Execution System (MES), Enterprise Resource Planning (ERP) software, and relevant supply chain stakeholders. This instant communication facilitates real-time visibility, enabling swift response and efficient resource allocation to minimise disruption.

Moving beyond Industry 4.0: the evolution toward Industry 5.0

While Industry 4.0 focuses on integrating Information Technology (IT) and Operational Technology (OT) to enhance automation, Industry 5.0 takes this integration a step further. This next phase emphasises a sustainable, human-centred manufacturing approach, blending advanced technology with human insight and creativity. Industry 5.0 aims for resilient, adaptive production

processes that empower the workforce with data-driven insights, foster sustainable practices, and support autonomous operations.

This progression toward Industry 5.0 requires that IT and OT systems share data continuously and seamlessly, bridging the gap between the factory floor and decision-making levels. In this setting, EDA becomes the central nervous system, enabling real-time data sharing across diverse systems and devices, supporting accurate decision-making by frontline workers, and enabling quick informed responses to operational changes.

Enhancing real-time data flow with EDA
One of EDA's defining features is its ability to move beyond rigid, centralised and siloed data architectures to create a flexible, distributed event streaming network. Traditional data exchanges in manufacturing were predominantly one-to-many, requiring a central data repository. In contrast, EDA's many-to-one and many-to-many capabilities allow factories to stream data across multiple applications and devices simultaneously, making it especially valuable for complex manufacturing ecosystems.

EDA supports the exchange of data from MES systems, SCADAs, and sensors with IT systems, allowing seamless integration of information across inventory, logistics, and supply chain processes. For example, a high-tech manufacturer operating hundreds of facilities globally can leverage EDA to share critical data in real-time. Event-driven architecture enables seamless, asynchronous connections between data centres and individual plants, delivering context-rich, time-sensitive information to each location. The immediate and autonomous flow of data means that even the smallest event—like a delay in the supply chain or an unexpected machine fault—can trigger responses across global sites, minimising the risk of downtime and ensuring uninterrupted production.

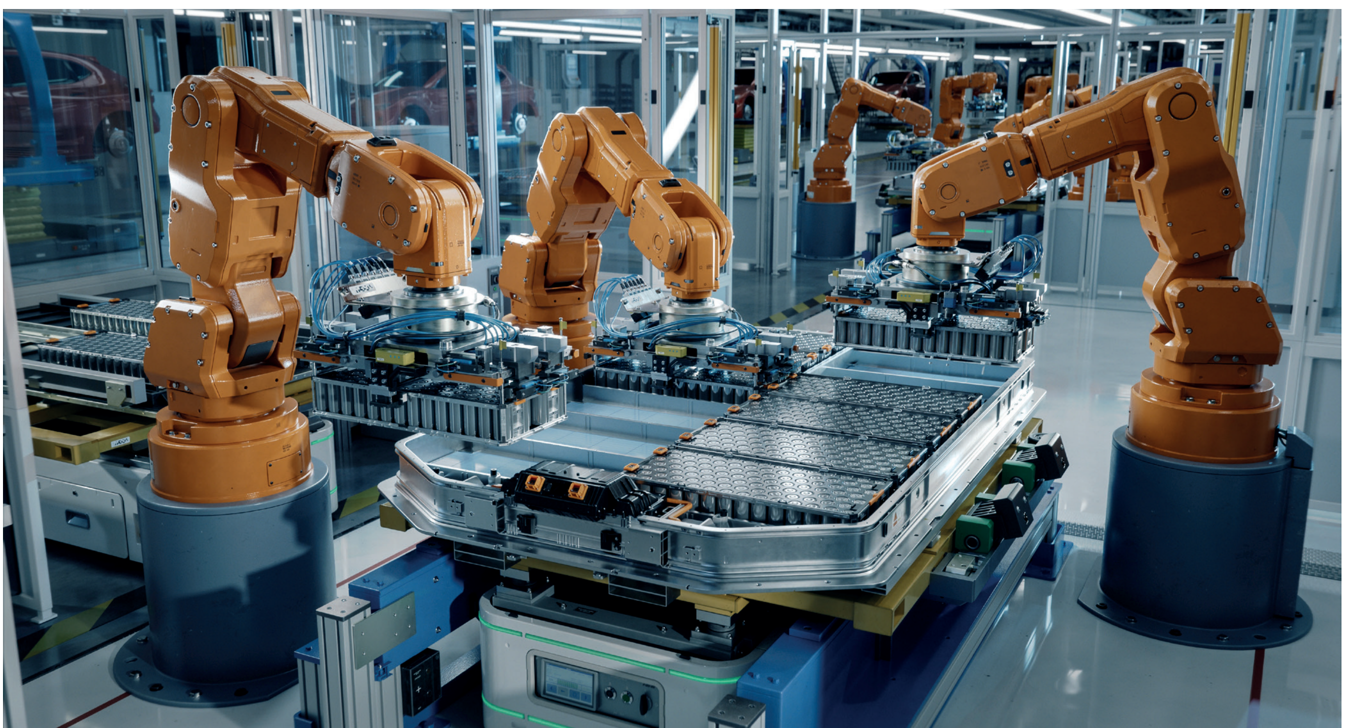
This progression toward Industry 5.0 requires that IT and OT systems share data continuously and seamlessly, bridging the gap between the factory floor and decision-making levels

The future of smart factories with EDA

As factories continue to adopt and expand AI, IoT, and real-time data analytics, event-driven architecture will play a critical role in shaping the future of manufacturing.

With EDA, manufacturers are better equipped to meet the demands of Industry 5.0 by facilitating human-machine collaboration, supporting sustainable practices, and enabling resilient, data-driven operations. This approach allows for real-time decision-making and continuous optimisation, transforming factories into adaptive, high-tech environments ready to meet the demands of the next industrial era.

Overall, EDA is empowering manufacturers to go beyond acclimating to today's challenges by providing a stable, scalable framework to lead the industry into a future where data flows freely, decisions are proactive, and production is both flexible and efficient.



Testing microchips for AI applications: Unveiling the challenges

Microchips are the backbone of artificial intelligence (AI) applications, powering everything from self-driving cars to virtual assistants. With the growing complexity of AI algorithms and the need for faster processing speeds, testing these microchips has become a major challenge for semiconductor companies.

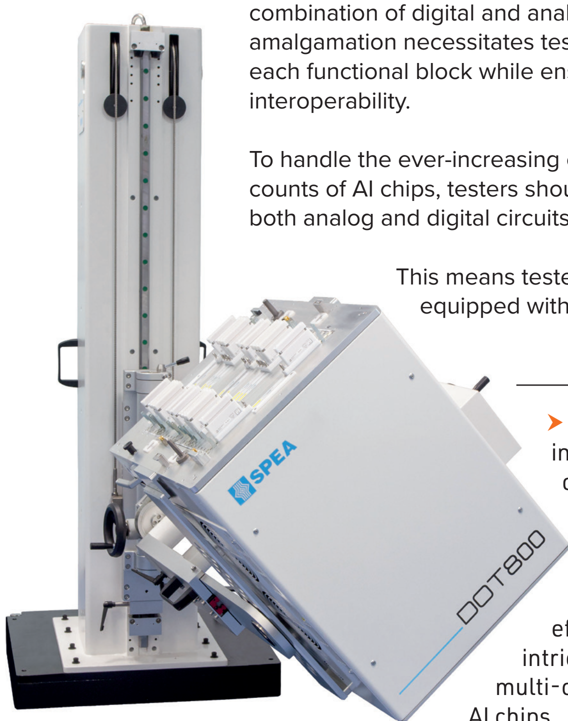
AI CHIPS are designed to process large amounts of data and make decisions in real-time, making them crucial for the success of final applications. Without proper testing, these chips may not function as intended, leading to errors and potentially dangerous consequences. This is especially true for applications that require real-time decision making, where any errors or malfunctions can have serious consequences.

In this article, we will explore the challenges in testing microchips for AI applications and the evolving capabilities required of mixed signal testers for robust AI microchip validation.

The challenge of testing complex AI chip designs
One of the main challenges in testing microchips for AI applications is the complexity of the algorithms they are designed to support. Modern AI chips often integrate diverse processing elements like CPUs, GPUs, specialized AI cores, and rely on a combination of digital and analog signals. This amalgamation necessitates tests that cater to each functional block while ensuring seamless interoperability.

To handle the ever-increasing complexity and pin counts of AI chips, testers should excel at testing both analog and digital circuits with high precision.

This means testers should be equipped with a variety of features and capabilities, including high-speed digital and analog testing, low-noise signal generation and analysis, high-speed digital pattern generation, and advanced data processing.



➤ Distributed intelligence based on a multi-core architecture makes new-generation mixed signal testers able to effectively test the intricate multi-die and multi-core architecture of AI chips

To keep pace with the evolving architecture of AI chips, testers need to boast increasingly sophisticated capabilities. As chip designers leverage technologies like 3D-stacking to enlarge bandwidth and facilitate the transfer of massive datasets in record time, new-generation testers must adapt accordingly. This necessitates a large quantity of high-speed digital channels, capable of handling frequencies ranging from 400MHz to tens of GHz. Additionally, large memory depth is crucial for accommodating the extensive test data these complex chips require.

The intricate multi-die/multi-core architecture of AI chips presents another challenge. Neural processing units (NPUs), for instance, often incorporate multiple cores. To effectively test these chips, testers require a new level of intelligence. Distributed intelligence based on a multi-core architecture enables the tester to perform multiple, simultaneous computations in an asynchronous manner. Imagine a tester with its instruments and components functioning as independent, intelligent modules capable of launching test patterns autonomously. This distributed processing power significantly enhances test efficiency and streamlines the validation process for complex AI chips, enabling the tester to mimic intricate real-world operating conditions.

The need for speed and efficiency

Another challenge in testing microchips for AI applications is the need for speed and efficiency. As AI applications become more prevalent, the demand for faster processing speeds and lower power consumption is increasing.

This puts pressure on semiconductor companies to develop microchips that can meet these demands while still being thoroughly tested. Traditional testing equipment and methods can be time-consuming

and may not be able to keep up with the pace of development, leading to delays in bringing products to market. To keep up with efficiency, testers should be capable of high multi-site capabilities, and should incorporate specific features aimed at maximizing the test execution speed. Distributed intelligence is a game-changer: multiple CPUs embedded within the tester and its instruments, all working simultaneously, allow the tester to run multiple test processes concurrently, significantly accelerating test execution.

Furthermore, multi-time domain capability is essential for maximizing test speed. This feature enables the tester to run digital signals with different time domains at the same time. This translates to testing concurrently the various blocks within the chip under test, decreasing dramatically the overall test-time.

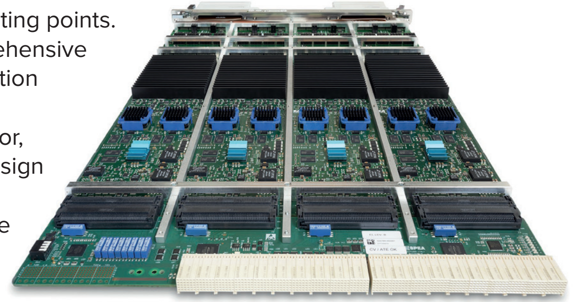
Other key features that contribute to test time optimization include embedded Digital Signal Processing (DSP) units on both analog and digital instruments. These on-board DSP units perform data de-coding and computations directly on the instruments, eliminating the need for data transfer back and forth to a central processing unit, which can slow down the testing process. Additionally, a protocol-aware instrument architecture is crucial. By understanding the communication protocols used by the DUT, the tester can streamline pattern complexity and optimize communication efficiency, further accelerating test execution.

Monitoring the chip power consumption

A hallmark of AI chips is their focus on power efficiency. This makes power management expertise one of the key characteristics that a new-generation mixed signal tester for AI microchips must possess. These chips often boast high-density layouts, integrating diverse processing elements with their own specific power requirements. This translates to a multitude of power domains, each requiring meticulous verification.

The tester needs to be adept at precisely controlling and monitoring power delivery across these domains, not just at the system level, but also for individual sections of the chip. This granular power management ensures that the chip operates under realistic conditions, allowing for accurate power consumption verification and the detection of power-related defects that might otherwise go unnoticed.

Furthermore, the immense processing power required by AI chips makes them inherently energy-consuming. This high-power draw translates to significant energy costs and thermal challenges for data centers, causing headaches for IT managers. To address this concern, mixed-signal testers must be equipped with a robust suite of power supplies capable of accurately stimulating the AI chips under test at various operating points. This enables comprehensive profiling and verification of the chip's power consumption behavior, ensuring it meets design specifications and contributes to a more energy-efficient overall system. By closely mirroring real-world power conditions, testers can help mitigate the data center power consumption woes associated with AI deployments. Additionally, the dynamic nature of AI chip operation necessitates new generation testers with a suitable number of high-current analog channels. Unlike traditional chips with steady power demands, AI chips exhibit fluctuating power consumption as workloads change.



➤ To handle the ever-increasing complexity of AI chips, tester instrumentation should include high-speed digital and analog capabilities, low-noise signal generation and analysis, high-speed digital pattern generation, and advanced data processing.

The tester's analog channels need the capacity to deliver these high currents while maintaining precise control. Fast instrumentation is equally important for effectively modulating the current supplied in response to the chip's real-time requirements. This ensures that the chip receives the exact amount of power it needs at any given moment, mimicking real-world operating conditions and enabling comprehensive power integrity testing.

Conclusion

Testing microchips for AI applications is a crucial step in the development process, but it comes with its own set of challenges. The complexity of AI algorithms, the need for speed and efficiency, and the importance of power consumption monitoring all make testing these microchips a difficult task. Investing in the right test equipment is essential to maximize AI chip performance and stay ahead of the competition in this rapidly advancing field. The new generation of mixed signal testers, as the SPEA DOT800, includes features like:

- High-speed digital and analog testing capabilities
- Large memory depth
- Distributed intelligence on a multi-core architecture
- Multi-time domain operation
- DSP units on analog and digital instruments
- Protocol-aware instrumentation
- A robust suite of power supplies

These features enable testers to mimic real-world operating conditions, perform comprehensive power integrity testing, and streamline test execution. By embracing these advancements, semiconductor companies can ensure the robust validation of AI microchips, paving the way for the next generation of groundbreaking AI applications.

The future of AI microchip testing is bright, characterized by continuous innovation and a symbiotic relationship between cutting-edge chip design and powerful testing methodologies.

A new patented approach to diffusion bonding offers speed and improved process control

An innovative process is reducing diffusion bonding time of aluminum and aluminum alloys by up to 50%, energy use by 30%, and improving quality.

BY PVA TEPLA AMERICA

CONTRACT MANUFACTURERS and design engineers in the aerospace, semiconductor, high-power electronics, and energy industries have been turning to diffusion bonded metals to produce new cutting-edge innovations.

Diffusion bonding is an essential joining method used to achieve a high-purity interface when two similar or dissimilar metals require superior structural integrity, and a traditional brazing approach fails to yield quality results. The process involves applying high temperature and pressure to metals mated together in a hot press, which causes the atoms on solid metallic surfaces to intersperse and bond.

Today, much of the innovation occurring in either in high-demand or high-quality industrial sectors involves aluminum as one or more of the layers of metals that are bonded. Aluminum, and its broad family of alloys, is prized as a lightweight metal with strong structural integrity, high electrical and thermal conductivity, corrosion resistance, and a malleability that makes it easy to shape.

➤ The technique ensures precise and uniform bonding by using advanced software and feedback sensors.

Aluminum's unique blend of lightness, strength, and purity makes it indispensable across various industries. In aerospace, its high strength-to-weight ratio is crucial for structural components. For semiconductor equipment, aluminum enables the fabrication of intricate, contamination-free channels essential for gas and fluid flow, avoiding the impurities inherent in traditional joining methods like brazing or welding. Furthermore, aluminum's compatibility with diffusion bonding allows for the creation of complex cooling channels in high-power electronics, injection molds, and specialized heat exchangers—designs often impossible to achieve through conventional machining.

Unfortunately, the characteristics of aluminum present a challenge for the traditional diffusion bonding process, which involves the application of radiant heat into the metal layers while in a vacuum furnace. Aluminum tends to reflect radiant heat and has a relatively low melting point in relation to the temperatures that must be achieved for proper diffusion bonding.

Engineers cleverly confronted the issue by developing a conductive heating method which more rapidly reaches bonding temperature. This new approach offers an alternative to traditional diffusion bonding by circumventing the slow process of radiant heating structural assemblies in a vacuum environment.

The c.BOND machine utilizes precisely controlled heat conduction, instead of radiation, to enable high speed production of aluminum-to-aluminum, or aluminum-to-dissimilar material parts. After several years of developmental research, the c.BOND tool

can now reduce total diffusion bonding process time essentially in half, and thus reducing the energy required during processing by as much as 30%. This also improves the quality of the bond in certain instances.

Expediting Aluminum Diffusion Bonding
In the traditional diffusion bonding process, a vacuum furnace provides radiant heat to the surface of the part. Subsequently the heat is conducted through the assembly and transmitted to the faying surface where required. However, when radiation becomes the dominant form of heat transfer, particularly at relatively lower temperatures in vacuum, below 600°C, aluminum's thermal conductivity is time consuming.

Aluminum excels at conducting heat, particularly at lower temperatures, making it ideal for applications requiring efficient heat dissipation, such as in electronics and automotive components.

"Aluminum's high reflectivity poses a challenge in traditional diffusion bonding. It's like trying to heat a mirror with a spotlight – the energy is reflected away instead of being absorbed into the material [using the traditional diffusion bonding process]," says Horst-Gunter Leng, Product Manager, PVA TePla Industrial Vacuum Systems, GmbH, a subsidiary of PVA TePla AG, a global manufacturer of industrial furnaces and PulsPlasma nitriding systems.

Horst-Gunter Leng adds that diffusion bonding of aluminum requires superior temperature control throughout the process. To prevent overheating of the load, slow heating rates traditionally are applied, leading to long process times.

In addition, aluminum alloys have a narrow processing temperature range for successful bonding. When temperatures fall outside that critical temperature band a poor bond is produced.

To overcome the existing challenges of bonding aluminum, PVA TePla and its partner initiated an extensive development program and came up with an innovative solution: integrating heating elements directly into the press platens, explains Horst-Gunter Leng. "This approach speeds up the bonding process, and significantly enhances efficiency by directly transferring heat to the aluminum components."

The culmination of extensive research and development is the c.BOND machine, features a unique combination of direct conduction heating through the top and bottom platens which are in contact with the assembly. This innovative design ensures bi-directional homogenous heating and more precise temperature at the bonding interface where it is required.

The c.BOND machine utilizes a hot-press tool with advanced software and feedback sensors to achieve micrometer-precise pressure control across the entire component surface. This ensures uniform bonding over large areas. Furthermore, the system allows for selective heating of specific areas, preventing unnecessary heat exposure to other parts of the component.

➤ A new patented approach to diffusion bonding has been developed which significantly enhances speed and process control, particularly for aluminum components.

The high-vacuum atmosphere within the chamber eliminates contamination and prevents voids in the bonded joint.

"With the [c.BOND] the time to heat the part to the ideal temperature for bonding is cut in half compared to traditional radiant heating. With less processing time required, the energy requirements are reduced by up to 30% as well," says Horst-Gunter Leng. He notes that multilayer stacking is also possible, which can further increase productivity.

The c.BOND technology demonstrates significant quality improvement of bonded aluminum components. The technology improves temperature homogenity in the load by 70%, which enhances bonding across the the entire surface. The technology also improves the parallelism of parts by 50%, which enhances the accuracy of geometric dimensions, tolerances, and product specifications.

According to Horst-Gunter Leng, the c.BOND furnace technology by PVA TePla is commercially available today for high volume production. The innovative furnace technology incorporates another feature unique to the industry, utilizing PVA TePla's proprietary automatic bonding software (ABP).

"With the automatic bonding software, you place your parts in the furnace, input a few parameters such as the size of the bonding area and the software calculates automatically the optimum processing parameters. No specific diffusion bonding knowledge from the operator is required," says Horst-Gunter Leng.

He notes that the recipes can be modified according to the type of material being bonded, the thickness of the material, its surfaces, and other factors. During the process the software continuously monitors the process in real-time and adjusts parameters accordingly.

A c.BOND unit is installed at a national research facility in Germany, The Günter Köhler Institute for Joining Technology and Materials Testing (ifw Jena) an independent, non-university industrial research institution that conducts research in diffusion bonding, additive manufacturing, brazing, welding, laser processing, material science, and other forms of bonding.

The c.BOND system is compact, requires minimal maintenance, and enables high-volume production of aluminum components for diverse industries. Its benefits are being realized in aerospace, where it creates lightweight yet strong aircraft components. In the semiconductor industry, it provides a cleaner alternative to brazing, eliminating the risk of solder contamination. There is also growing demand for diffusion-bonded aluminum heat sinks, crucial for cooling high-power silicon carbide (SiC) electronics.

Diffusion bonding also has applications for conformal cooling. The concept is to bond layers of sheet metal that contain machined channel/microchannel structures. When combined, the channels provide a path for heat dissipation. Current applications include power electronics for effective heat management and rapid cooling of molds utilized in injection and blow molding processes. With the size of components continually getting smaller in sectors like semiconductors and electronics, controlling the amount of time, and by extension heat, introduced into the part becomes more critical.

"As the features [of the internal channels] become more miniaturized, it becomes even more important to control the heating during the diffusion bonding process to avoid any distortion in the part," says Horst-Gunter Leng. "If you can shorten the cycle time, you introduce less heat into the part. This will facilitate creating parts with conformal cooling channels that have finer and finer features."

Diffusion bonding is increasingly valuable for joining dissimilar metals, such as aluminum to steel or titanium. This allows engineers to design components and assemblies with the best properties of each metal. For example, one metal might offer superior corrosion resistance while the other provides greater strength. This 'packaging' of dissimilar metals opens up new possibilities in design, particularly for overall weight reduction of design and enhancing performance in challenging environments.

When joining dissimilar surfaces, a liquid-phase diffusion bonding process is utilized, particularly when the bonding interface extends beyond R&D sized samples. This often involves an interlayer of an alloy that typically melts at the faying surfaces. When the interlayer includes aluminum, the c.BOND can delivery controlled heat to increase the bonding speed.

Although the c.BOND technology is designed to improve the diffusion bonding of aluminum, PVA TePla can design the machine around the specific needs of the customer customized for the alloy, including copper, which has many applications in specialized heat exchanger or for products used in the microelectronics industry. The company is exploring options to modify the c.BOND to achieve even higher temperatures above the current maximum of 800°C, according to Horst-Gunter Leng.

As diffusion bonding of aluminum gains importance across industries, contract manufacturers and design engineers must embrace the latest advancements to remain competitive. By adopting fast, energy-efficient diffusion bonding technologies for aluminum and other materials, they can unlock higher production volumes, reduce costs, improve or achieve global sustainability targets, and realize increased profitability.

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New Clean ID hose streamlines the semiconductor supply chain

How could companies benefit from a flex hose with a truly clean ID? How much time and money would be saved using a hose that comes off the machine without moisture, oils or grease?

BY ROBERT BARKER, PRESIDENT, PENFLEX

THROUGHOUT the semiconductor supply chain, high purity gases play a key role in supporting clean and precise operations. The purity of these gases must be ensured at each step of shipment, storage and delivery, a task that relies on the cleanliness of the conduits themselves.

What traditional hose manufacturing processes leave behind

Making metal hose begins with thin strips of material. The edges are brought together to form a straight tube. Corrugations are then introduced to deliver a hose that can bend and flex in response to the needs of many applications.

Various processes are used to create corrugations. Hydroforming uses high pressure water to "push" the material from the inside into dies surrounding the hose. The shape of the dies determines the shape of the corrugations.

Mechanical forming uses either dies that are split into two sections of a ring, which squeeze the tube and move towards one another to form a corrugation, or a series of dies that rotate around the tube progressively creating deeper indentations that ultimately form the corrugations.

Both production methods produce a quality hose for most applications. However, for the most stringent use cases, like those seen in semiconductor manufacturing, they may be unsuitable. The important question for high purity gas applications is: "Will a hydroformed hose ever truly be rid of moisture?"

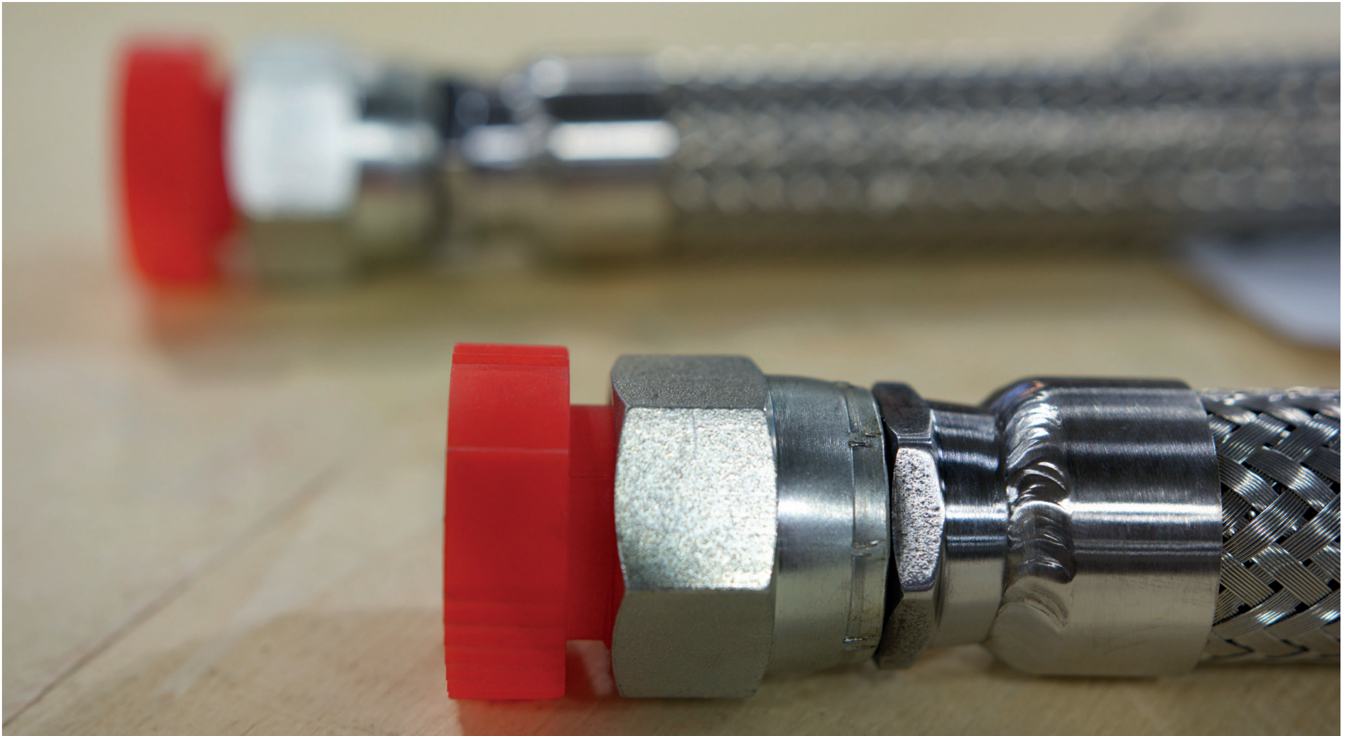
Earlier mechanical forming processes relied on a sizing ball on the inside of a hose to help maintain the shape of the tube before corrugations were created. To prevent wear, a small amount of lubrication oil was often used.

Required post-production cleaning, draining and drying

Hoses transporting high purity gases must be adequately cleaned to remove such harmful contaminants. This often means specifications requiring post-production cleaning and further testing accompany purchase orders for metal hose assemblies.

These specifications describe how to clean a hose with a spar nozzle or interior mandrel using various aqueous solutions and detail how they then must be drained and oven dried. Each process requires

➤ Clean ID CL3 metal hose assembly tested, tagged, bagged and ready for shipment.



➤ Skills of Penflex's ASME Sec. IX certified welders can be seen on small diameter hose assembly.

a high degree of labor. Then, to confirm cleanliness, these instructions lay out additional testing procedures to confirm the absence of hydrocarbons and particulate. Though a requirement, these processes themselves can sometimes lead to recontamination. Cleaning agents may remove the oil, but they may also leave behind solvent, acid or alkali residues.

Draining, drying and multiple rounds of testing contribute to the added costs and long lead times users have come to expect, but it may be time to rethink those expectations. All this post-production work and testing is unnecessary. Mechanical forming can now produce a hose without the need for lubrication.

An innovation in metal hose forming technology

Consistent refinements have led to the removal of internal tooling in Penflex's new CL3 mechanical forming process. The sizing ball is no longer needed thanks to greater precision and the result–the new Clean ID product line–is a hose devoid of any oils or tooling marks. Current post-production requirements can be removed. In a process that uses neither water nor lubrication on the inside, there is no need for additional cleaning, draining, drying and retesting that layer in costs and extend delivery times.

> “Mechanical forming uses either dies that are split into two sections of a ring, which squeeze the tube and move towards one another to form a corrugation, or a series of dies that rotate around the tube progressively creating deeper indentations that ultimately form the corrugations”

And, as an added benefit, with less risk of moisture exposure to the test equipment, CL3 enables faster, more reliable mass spectrometer leak testing.

As anyone working in the semiconductor space would be quick to note, a truly clean inside presents opportunities for streamlined supply chains and greater efficiencies in operation.

Streamlined supply chains and more efficient processes

One leading US manufacturer of cryogenic coolers found that switching to Clean ID allowed them to eliminate a time-consuming cleaning process, meaning hoses could be installed sooner and the team of five responsible for cleaning the inside of the hoses could be reassigned.

Made from 316 or 321 stainless steel, Clean ID is currently available in sizes ½”, ¾” and 1”. With a lightweight construction and design that prioritizes flexibility, the hose makes for easy handling and installation.

With the projected increase in the semiconductor manufacturing industry, companies that find ways to shorten their supply chains and maximize the efficiency of their processes will be best-placed to capitalize on that growth. Albeit a small one, Clean ID has an important role to play in helping these companies succeed. After all, you can't take out what was never there!

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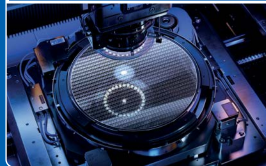

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