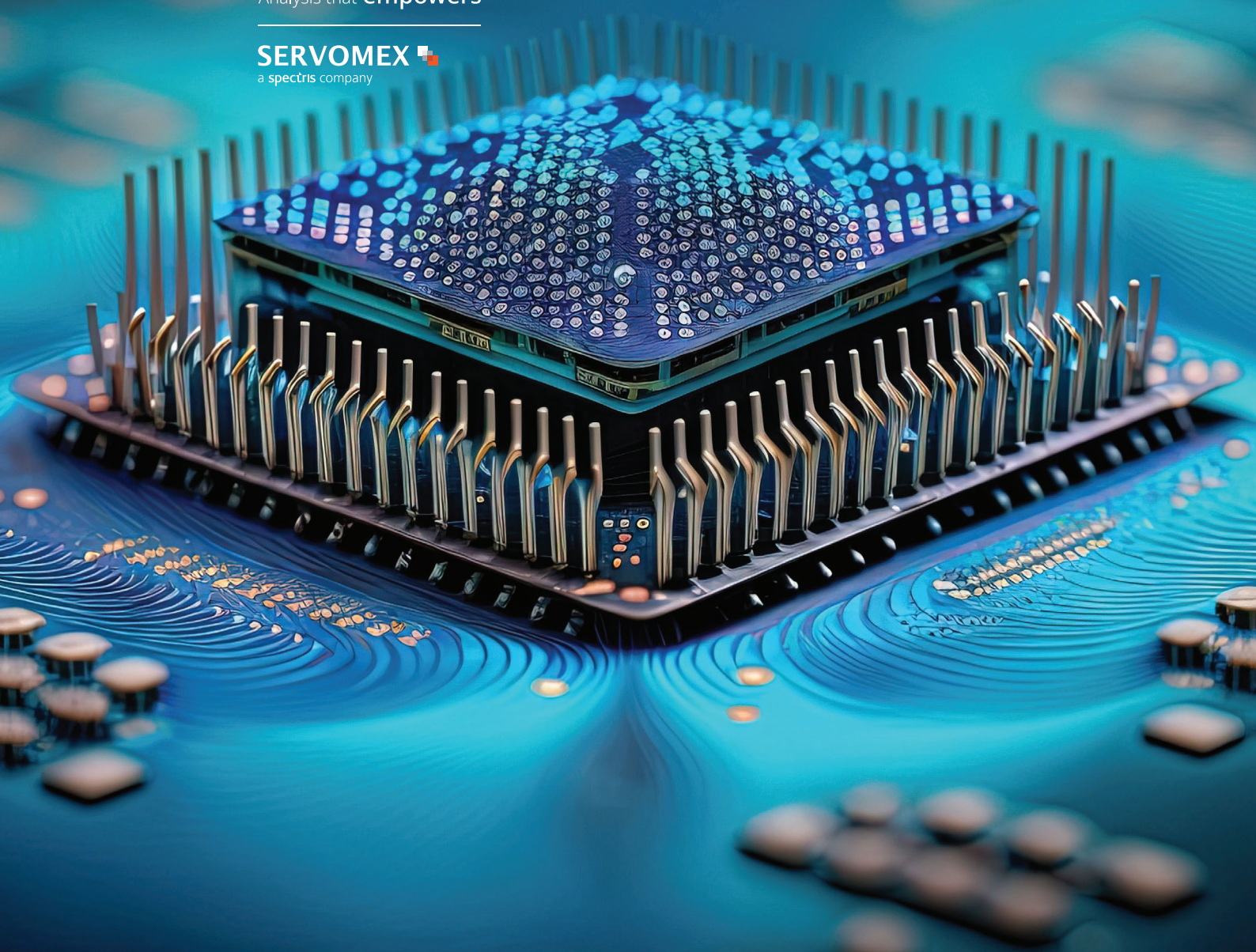
SILICON SEMICONDUCTOR

ISSUE II 2026

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

SILICONSEMICONDUCTOR.NET

TDLAS VS CRDS: WHICH GAS ANALYSIS TECHNOLOGY TRULY PERFORMS IN THE FAB?



EVG®

invent
innovate
implement

www.EVGroup.com

FUSION AND HYBRID BONDING FOR HETEROGENEOUS INTEGRATION

- Enabling advanced 3D device stacking and chiplet integration for CMOS image sensors, memory and 3D system-on-chip (SoC)
- High-volume production equipment and process technology for Wafer-to-Wafer (W2W) and Die-to-Wafer (D2W) hybrid bonding
- GEMINI® FB Automated Production Wafer Bonding System delivers industry leading alignment accuracy and bonding performance
- Heterogeneous Integration Competence Center™ serving as leading-edge innovation incubator for EVG customers and partners

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

VIEWPOINT

BY PHIL ALSOP
EDITOR

Celebrating Europe's research success

EUROPE'S semiconductor ambitions are often framed in terms of manufacturing scale or geopolitical urgency. Yet, as recent developments from CEA-Leti and imec demonstrate, the continent's true competitive strength lies deeper—in a uniquely integrated R&D ecosystem that consistently translates fundamental science into system-level innovation.

Across multiple fronts, European research organisations are not simply advancing individual technologies; they are redefining how innovation flows from laboratory to industry. Nowhere is this more evident than in silicon photonics. CEA-Leti's latest work on hybrid III-V/silicon quantum cascade lasers (QCLs) for mid-infrared applications exemplifies a pragmatic, architecture-driven approach. Rather than converging prematurely on a single solution, the team has developed multiple integration pathways, each balancing manufacturability, flexibility, and performance. This is not just clever engineering—it reflects a broader European philosophy: innovation as a portfolio of options, de-risked through rigorous experimentation.

The same system-level thinking extends to emerging application spaces. The co-packaging of microLEDs with organic photodetectors illustrates how Europe's R&D centres are collapsing traditional boundaries between components, systems, and end-use cases. By embedding sensing directly into display architectures, CEA-Leti moves beyond incremental improvement toward functional convergence—an increasingly critical differentiator in markets such as wearables and biomedical devices.

Meanwhile, advances in photonic interconnects and chip-scale instrumentation highlight Europe's ability to tackle bottlenecks that will define next-generation computing. The demonstration of a dynamically routed electro-optical router—capable of nanosecond-scale reconfiguration—addresses a fundamental limitation in chiplet-based architectures. Similarly, the development of a battery-operated EPR spectrometer on chip underscores Europe's leadership in scientific instrumentation, where deep domain expertise meets advanced CMOS integration.

Crucially, these breakthroughs are not occurring in isolation. They are embedded within a growing network of pilot lines and collaborative platforms designed to accelerate industrial uptake. The FAMES pilot line is a case in point: already delivering validated results across FD-SOI, 3D integration, and embedded memory, it represents a functioning model of "lab-to-fab" transition. Its open-access structure—serving startups, SMEs, and large industry alike—reinforces a distinctly European approach to innovation: collaborative, distributed, and strategically aligned with public policy frameworks such as the EU Chips Act.

A similar dynamic is visible at imec, where the NanoIC pilot line is pushing beyond the 2nm frontier while simultaneously lowering barriers to entry through early-access PDKs. By enabling designers to explore A14 logic or embedded memory architectures before physical hardware exists, imec is effectively compressing innovation cycles. The addition of heterogeneous materials such as barium titanate to silicon photonics platforms further highlights Europe's willingness to invest in long-term, high-risk technology bets that could unlock step-change performance gains.

Taken together, these developments point to a critical insight: Europe's semiconductor strength is not defined by scale alone, but by the density and quality of its R&D infrastructure. Organisations like CEA-Leti and imec act as hubs where academia, industry, and government converge—creating an environment where ideas can be rapidly prototyped, validated, and transferred.

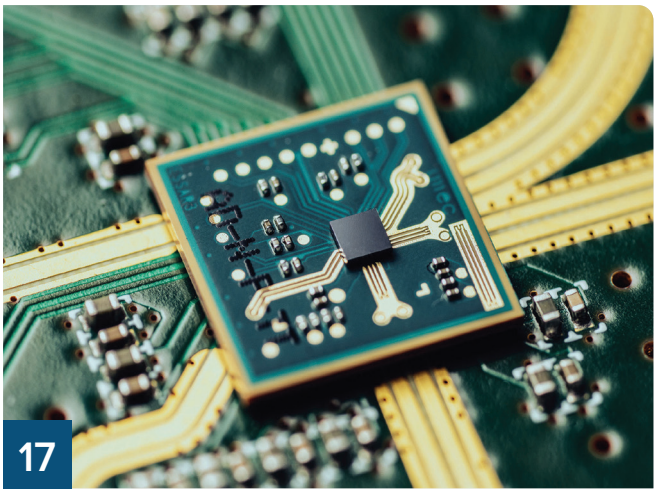
As global competition intensifies, this model may prove to be Europe's most durable advantage. Manufacturing capacity can be built, and supply chains reshaped, but replicating decades of accumulated expertise, collaborative culture, and system-level thinking is far more challenging. In that sense, Europe's R&D organisations are not just supporting the semiconductor ecosystem—they are defining its future trajectory.

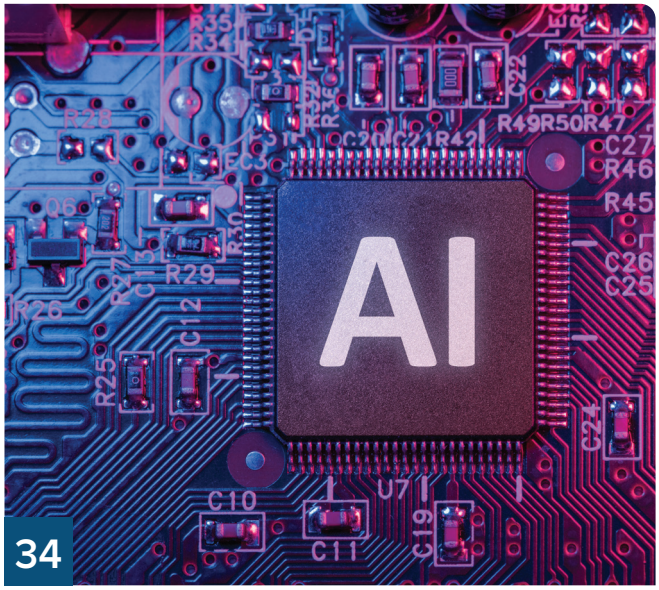
Contents

COVER STORY

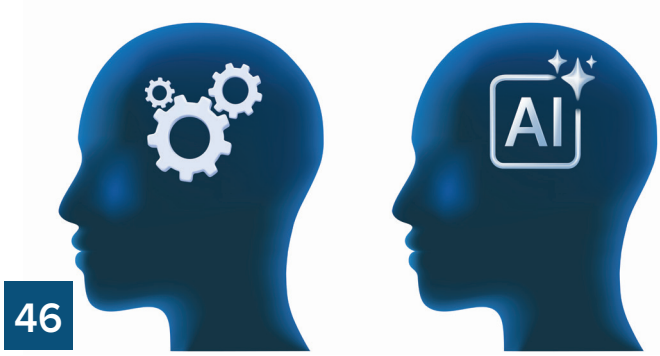
TDLAS vs CRDS: Which gas analysis technology truly performs in the fab?

When even parts per trillion (ppt) moisture can cause serious defects and delays, fabs must keep conditions pristine and gas quality optimized.





26



46

NEWS

08

Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Editor Phil Alsop phil.alsop@angelbc.com
Sales & Marketing Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Graphic Design and Multi Media Harvey Watkins harvey.watkins@angelbc.com
Chief Executive Officer Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970

Chief Technical Officer Scott Adams scott.adams@angelbc.com +44 (0)2476 718970
Directors Jackie Cannon, Sharon Cowley

Published by Angel Business Communications Ltd, 6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com

Silicon Semiconductor is published ten times (6x print and 4x video issues) a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £50.00 per annum (UK) , €60.00 per annum (Europe), $90 per annum (air mail)(USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2026. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing. US mailing information: Silicon Semiconductor, ISSN 1096-598X, is published 5 times a year by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. Airfreight and mailing in the USA by agent named World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA. Periodicals Postage Paid at Brooklyn, NY 11256. POSTMASTER: Send address changes to Silicon Semiconductor, Air Business Ltd, c/o World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA.

We strive for accuracy in all we publish; readers and contributors are encouraged to contact us if they recognise an error or omission. Once a magazine edition is published [online, in print or both], we do not update previously published articles to align old company names, branding, marketing efforts, taglines, mission statements or other promotional verbiage, images, or logos to newly created or updated names, images, typographic renderings, logos (or similar) when such references/images were accurately stated, rendered or displayed at the time of the original publication. When companies change their names or the images/text used to represent the company, we invite organizations to provide Angel Business Communications with a news release detailing their new business objectives and/or other changes that could impact how customers/prospects might recognise the company, contact the organisation, or engage with them for future commercial enterprise.
Printed by: The Manson Group. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online) © Copyright 2026.

Cosmic is born

The international growth journey launched in 2022 following Xenon Private Equity's investment in Microtest reaches a significant new milestone with the creation of Cosmic, the new name of the Group.

THIS UNITES the different industrial companies integrated over the last few years under a single brand identity. Two complementary divisions will operate independently: Cosmic Equipment and Cosmic Services.

Following the acquisitions of Test Inspire in the Netherlands, Gedec in Italy, and RoodMicrotec – a company listed on the Amsterdam Stock Exchange with a strong presence in the German market – the expansion continued in 2024 with the addition of ipTEST in the United Kingdom and Focused Test in the United States. Today, these combined capabilities converge into a single global brand, designed to enhance the technological heritage and distinctive expertise of each organization.

With more than 400 professionals and 15 direct locations across Europe, the United States, and Asia, Cosmic combines the strength of an international structure with close proximity to local markets. Cosmic offers customers a solid, integrated, and highly specialized global presence.

A portfolio of specialized solutions: equipment and services

Cosmic operates through two distinct and complementary divisions, enabling the Group to address a comprehensive portfolio of semiconductor test solutions.

The Cosmic Equipment division is dedicated to the design and manufacturing of advanced test solutions, including Automatic Test Equipment (ATE) systems for mixed-signal and high-power applications, as well as handlers and burn-in systems. This division represents the technological core of the Group and focuses on developing high-performance platforms capable of meeting the growing demands of the automotive, industrial, power, and high-reliability markets.

The Cosmic Services division provides a comprehensive portfolio of test services, supporting customers throughout the entire device lifecycle. Cosmic Services offers everything from customized test solution development, ASIC design with design-for-testability (DFT) support, to wafer sort and final production testing. On top of this, the division specializes in characterization and qualification testing in addition to burn-in and reliability testing.

Cosmic ensures high-quality standards and fast execution for device troubleshooting projects ensured by advanced Failure & Technology Analysis capabilities which enable precise identification of device failures through sophisticated failure analysis techniques, thereby supporting continuous improvement and product optimization processes.

"The creation of Cosmic represents a fundamental strategic step in our journey to consolidate our position as a leading international player in the semiconductor test industry," stated Ruud van der Linden, CEO of Cosmic Group. "The integration of technological, industrial, and operational expertise on a global scale now enables us to offer our customers a unique value proposition that combines innovation, efficiency, and added value.

With Cosmic, we are establishing a strong global corporate identity that brings our Equipment and Services divisions under one organization while preserving their distinct focus, leadership, and strategic direction. Each division will continue to operate with clear accountability in its respective markets, supported by the strength and visibility of a unified corporate name".

Samsung and AMD expand strategic collaboration

The companies will collaborate on industry-leading HBM4 supply for AMD Instinct™ MI455X GPUs and next-generation DDR5 solutions for AMD EPYC™ processors and the AMD Helios platform.

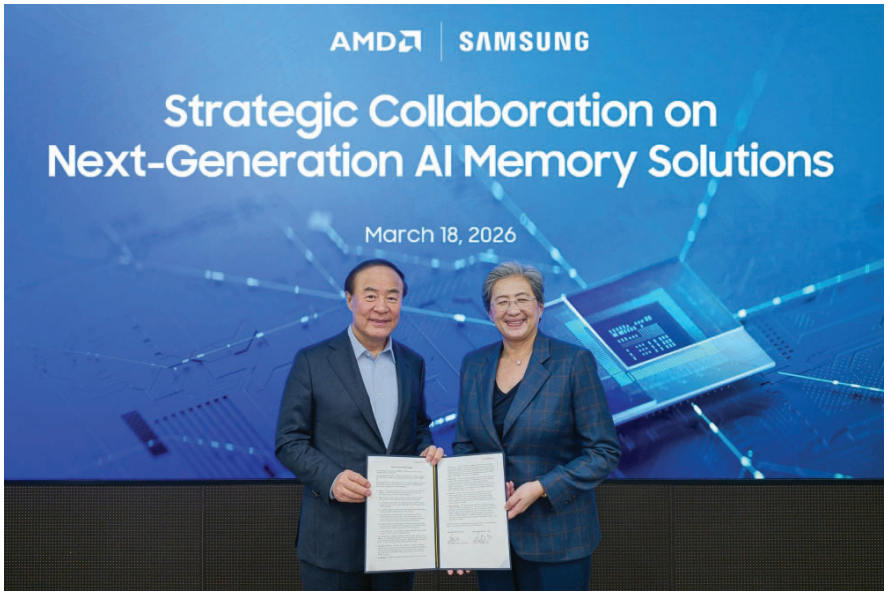
SAMSUNG ELECTRONICS has signed a Memorandum of Understanding (MOU) with AMD to expand their strategic collaboration on next-generation AI memory and computing technologies.

The signing ceremony was held at Samsung's most advanced chip manufacturing complex in Pyeongtaek, Korea, attended by Dr. Lisa Su, Chair and CEO of AMD, and Young Hyun Jun, Vice Chairman & CEO of Samsung Electronics.

"Samsung and AMD share a commitment to advancing AI computing, and this agreement reflects the growing scope of our collaboration," said Young Hyun Jun, Vice Chairman & CEO of Samsung Electronics. "From industry-leading HBM4 and next-generation memory architectures to cutting-edge foundry and advanced packaging, Samsung is uniquely positioned to deliver unrivaled turnkey capabilities that support AMD's evolving AI roadmap."

"Powering the next generation of AI infrastructure requires deep collaboration across the industry," said Dr. Lisa Su, Chair and CEO of AMD. "We are thrilled to expand our work with Samsung, bringing together their leadership in advanced memory with our Instinct GPUs, EPYC CPUs and rack-scale platforms. Integration across the full computing stack, from silicon to system to rack, is essential to accelerating AI innovation that translates into real-world impact at scale."

Under the MOU, Samsung and AMD will align on primary HBM4 supply for the next-generation AMD AI accelerator, the AMD Instinct MI455X GPU, as well as advanced DRAM solutions for 6th Gen AMD EPYC CPUs, codenamed "Venice." These technologies will support next-generation AI systems combining AMD Instinct GPUs, AMD EPYC CPUs and rack-scale architectures such as the AMD Helios platform.



Samsung and AMD are closely collaborating on advanced memory technologies for AI and data center workloads. As memory bandwidth and power efficiency become increasingly critical to system-level performance, this collaboration will help deliver more optimized AI infrastructure for customers.

An industry-first to enter mass production, Samsung's HBM4 is built on its most advanced 6th-generation 10-nanometer (nm)-class DRAM process (1c) and a 4nm logic base die, featuring processing speeds of up to 13 gigabits-per-second (Gbps) and maximum 3.3 terabytes-per-second (TB/s) bandwidth that exceeds industry standards.

Powered by Samsung HBM4's industry-leading performance, reliability and energy efficiency, the AMD Instinct MI455X GPU is expected to be the optimum solution for high-performance systems handling AI model training and inference.

The MI455X GPU will serve as a key building block for the AMD Helios rack-scale architecture, designed to deliver the performance and scalability required for next-generation AI infrastructure.

As part of their collaboration, Samsung and AMD will also work together on high-performance DDR5 memory optimized for the 6th Gen AMD EPYC CPUs. The companies aim to deliver industry-leading DDR5 memory solutions for systems built on the AMD Helios rack-scale architecture.

The two companies will also discuss opportunities for foundry partnership, through which Samsung would provide foundry services for next-generation AMD products.

Samsung and AMD have collaborated for nearly two decades across graphics, mobile and computing technologies, including Samsung serving as the primary HBM3E partner to AMD, powering the latest AMD Instinct MI350X and MI355X AI accelerators.

Imec receives 'the world's most advanced' High NA EUV system

Operating the High NA EUV system in direct connection with state-of-the-art metrology and patterning equipment/materials accelerates learning cycles to unlock the performance needed for sub-2nm logic and future memory technologies, supporting the rapidly scaling AI and high-performance computing (HPC) markets.

IMEC announces the arrival of the ASML EXE:5200 High NA EUV lithography system, said to be the most advanced lithography tool available today. With this strategic milestone, imec reinforces its position as the industry's launchpad into the ångström era, giving its global partners ecosystem unparalleled early access to the next generation of chip-scaling technologies. Integrated directly with a comprehensive suite of patterning and metrology tools and materials, the High NA EUV system will empower imec and its ecosystem partners to unlock the performance needed to pioneer sub-2nm logic and high-density memory technologies that will fuel the rapid growth of advanced AI and high-performance computing.

Luc Van den hove, CEO of imec: "The past two years have marked an important chapter for High NA (0.55NA) EUV lithography, with imec and ASML joining forces with the ecosystem in its joint High NA EUV Lithography Lab in Veldhoven (The Netherlands) to pioneer High NA EUV technology.

With the installation of the EXE:5200 High NA EUV lithography system into our 300mm cleanroom in Leuven (Belgium), we aim to bring these High NA EUV patterning technologies to an industry-relevant scale and to develop the next-generation High NA EUV patterning use cases. Its unmatched resolution, improved overlay performance, high throughput, and a new wafer stocker that improves process stability and throughput, will give our partners a decisive advantage in accelerating the development of sub-2nm chip technologies. As the industry moves into the ångström era, High NA EUV will be a cornerstone capability, and imec is proud to lead the way by offering its partners the earliest and most comprehensive access to this technology."

This milestone is a key element of imec's five-year strategic partnership with ASML supported by the EU (Chips Joint Undertaking and IPCEI), the Flemish government, and the Dutch government. Luc Van den hove:

"As an integral part of the EU funded NanoIC pilot line, the tool is set to play a pivotal role in strengthening Europe's position as a leader in advanced semiconductor R&D in the decades to come."

Having the ASML EXE:5200 High NA EUV lithography system in imec's cleanroom firmly positions imec as the most comprehensive development environment for advanced patterning. Imec's deep ecosystem collaboration with leading chip manufacturers, equipment, material and resist suppliers, mask companies, and metrology experts will allow us to ramp up learning cycles and enhance process stability to develop and demonstrate cutting-edge patterning for next generation logic and memory device technology, driving breakthroughs that will shape the future of advanced computing and AI in the years to come.

Christophe Fouquet, CEO of ASML: "Imec's installation of the EXE:5200 marks an important step into the ångström era. Together, we're accelerating High NA EUV extendibility for the next generations of advanced memory and compute."

Imec anticipates the EXE:5200 High NA EUV lithography system to be fully qualified by Q4 2026. In the meantime, the joint ASML-imec High NA EUV lithography Lab in Veldhoven will remain operational, ensuring continuity in the High NA EUV R&D activities for imec and its ecosystem partners.

STMicroelectronics enters high-volume production of its silicon photonics platform

PIC100 technology in 300 mm high-volume production for leading hyperscalers, with plans to quadruple capacity by 2027 and further expand in 2028.

PIC100 TECHNOLOGY in 300 mm high-volume production for leading hyperscalers, with plans to quadruple capacity by 2027 and further expand in 2028.

STMicroelectronics is now entering high-volume production for its state-of-the-art silicon photonics-based PIC100 platform used by hyperscalers for optical interconnect for data centers and AI clusters. The 800G and 1.6T PIC100 transceivers enable higher bandwidth, lower latency, and greater energy efficiency as AI workloads surge.

"Following the announcement of its new silicon photonics technology in February 2025, ST is now entering high-volume production for leading hyperscalers. The combination of our technology platform and the superior scale of our 300 mm manufacturing lines gives us a unique competitive advantage to support the AI infrastructure super-cycle," said Fabio Gualandris, President, Quality, Manufacturing & Technology, STMicroelectronics. "Looking ahead, we are planning and executing on capacity expansions to enable more than quadrupling of production by 2027. This fast expansion is fully underpinned by customers' long-term capacity reservation commitments."

"The data center pluggable optics market continues to expand strongly, reaching $15.5 billion in 2025. We expect the market to grow at a compound annual growth rate (CAGR) of 17% from 2025 through 2030, surpassing $34 billion by the end of the forecast period. In addition, co-packaged optics (CPO) will emerge as a rapidly growing segment, contributing more than $9 billion in revenue by 2030. Over the same period, the share of transceivers incorporating silicon photonics modulators is projected to increase from 43% in 2025 to 76% by 2030," said Dr. Vladimir Kozlov, CEO and Chief Analyst at LightCounting. "ST's leading silicon photonics platform coupled with its aggressive capacity expansion plan illustrates its capabilities to provide hyperscalers with secure, long-term supply, predictable quality, and manufacturing resilience."

Upcoming PIC100 TSV platform technology

AI infrastructure is experiencing unprecedented scaling, with cloud-optical interconnect performance becoming a critical bottleneck. Drawing on years of silicon photonics innovation, ST's PIC100 platform provides state-of-the-art optical performance, including best-in-class silicon and silicon nitride waveguide losses (respectively as low as 0.4 and 0.5 dB/cm), advanced modulator and photodiode performance, as well as an innovative edge coupling technology.

In parallel with high-volume PIC100 production, ST is planning to introduce the next step in its silicon photonics technology roadmap: the PIC100 TSV, a new and unique platform that integrates through-silicon via (TSV) technology to further increase optical connectivity density, module integration, and system-level thermal efficiency. The PIC100 TSV platform is designed to support future generations of Near Packaged Optics (NPO) and co-packaged optics (CPO), aligning with hyperscalers' long-term migration paths toward deeper optical–electronic integration for scale up.

STMicroelectronics is now entering high-volume production for its state-of-the-art silicon photonics-based PIC100 platform used by hyperscalers for optical interconnect for data centers and AI clusters.

Cloudberry launches Europe's first semiconductor venture fund

Cloudberry, a venture capital firm based in Helsinki and London, has launched what is believed to be Europe's first semiconductor venture fund with an initial close of €30 million.

THE FUND invests in companies advancing the technological frontier with semiconductors, photonics and advanced materials to advance compute, connectivity, sensing and power.

Anchored by Finnish state-owned investment company Tesi, Cloudberry's fund is supported by international LPs across Europe, Asia and the United States, including GlobalFoundries, one of the world's largest semiconductor foundries, Radiant OptoElectronics, a global leader in photonics, and numerous family offices and angel investors. Other than Tesi's support, the fund has secured 85 per cent of its capital from outside Finland.

The launch comes as Europe accelerates its EU Chips Act, a €43 billion initiative to double the continent's global semiconductor market share to 20 per cent by 2030. The act aims to ensure Europe's capacity in advanced chip design and manufacturing, strengthening resilience across global supply chains.

Beyond recent policy shifts, the semiconductor and photonics industries are expanding rapidly. Together, they form a global market of approximately USD 1.5 trillion, expected to surpass USD 2 trillion within the decade. Both sectors continue to grow faster than global GDP and underpin strategically critical industries in AI, space, telecommunications, and defence.

"We see this as the start of a long-term effort to build Europe's semiconductor ecosystem," said Veera Pietikäinen, Founding Partner at Cloudberry. "Europe has world-class talent and deep technology capabilities in semiconductors and photonics, but has lacked investors who truly understand how to support and scale them. We are now building a specialist platform that helps these companies grow and strengthen Europe's technological sovereignty in the process."

In Europe, the photonics sector includes more than 5,000 companies and employs over 430,000 people, while the semiconductor industry adds hundreds of thousands more across design, materials, equipment, packaging and specialised R&D. Despite their strategic importance, most investment still flows to large manufacturing and infrastructure projects, leaving early-stage innovation and deep-tech ventures underfunded. Cloudberry aims to close this gap by investing up to €1 million in pre-seed and seed rounds as well as maintaining sufficient reserves to support portfolio companies as they scale. The team plans to invest in up to 20 companies across Europe, ranging from early R&D spinouts to teams commercialising innovations within the fund's core focus areas of semiconductors, photonics and advanced materials.

"The Cloudberry team, experienced deep-tech investors and industry operators with broad networks, are in a good position to capture value in domains that not only have significant market opportunities but also advance strategically critical technologies. Finland has a strong legacy of innovation in semiconductors and photonics, so the new fund is a welcome addition to the local VC ecosystem", explains Asseri Lehtiniemi, Investment Director in Tesi's Fund Investments team.

Cloudberry's long-term ambition is to build Europe's leading platform for semiconductor investment and support, spanning from early-stage to growth-stage capital. The firm's experienced team combines decades of operational, technical and venture expertise from companies such as ASML, Bosch, Heptagon and leading deep-tech VC firms, giving Cloudberry a unique ability to identify and scale Europe's most promising semiconductor innovators.

"The semiconductor industry requires investors who understand technical complexity and the rigorous qualification needed to build strong foundry partnerships. At GlobalFoundries, we are committed to supporting the next generation of innovators as they scale from prototype to volume, and we can help them reach global scale.

Cloudberry's focused approach fills a crucial gap in early-stage hardware funding, giving these companies the backing and expertise they need to grow," says Manfred Horstmann, General Manager and Senior Vice President at GlobalFoundries Europe.

"Cloudberry connects us directly to Europe's semiconductor and photonics ecosystem. We've expanded significantly in the Nordics because the region is central to next-generation materials and optics. This partnership gives us early visibility to the teams building these breakthroughs," said Justin Wang, Chairman and President of Radiant Opto-Electronics.

‘Only photonics’ can satisfy AI’s insatiable appetite for compute power

As artificial intelligence expands, its soaring electricity use is putting unprecedented pressure on power grids, driving up costs and threatening to slow Europe’s energy transition. But a new report shows that only light-based computing can keep AI’s ever-expanding power demands at bay without triggering a surge in emissions.

THE STUDY, published by Photonics21 and compiled by market intelligence agency TEMATYS, finds that as electricity use from AI rises sharply, and conventional silicon chips struggle to keep pace with the twin pressures of ever-larger models and expanding data centres, Europe risks undermining its clean-energy goals and increasing reliance on fossil fuels.

Entitled “AI Desperately Needs Photonics,” the report concludes that photonics, which uses light rather than electricity to move and process information, offers the only viable pathway to scale up AI computing while dramatically reducing energy consumption. The study reveals that integrating photonic technologies into data-centre and chip architectures can help AI growth remain compatible with Europe’s climate commitments.

A growing AI problem

AI is scaling faster than the world’s power grids can handle. Each new generation of larger, more complex models demands exponentially greater computing power, sending data-centre energy use soaring.

The International Energy Agency puts global consumption at roughly 415 TWh in 2024, and TEMATYS warns it could more than double by 2030 as AI workloads dominate digital infrastructure.

Sébastien Bigo, Nokia Bell Labs Fellow and Photonics21 Work Group Leader for Digital Infrastructure, said, “Photonics can provide the infrastructure that will determine whether AI becomes cleaner and more competitive or simply costlier and dirtier. Europe has the research base to lead; what it lacks is coordinated investment and industrial scale.”

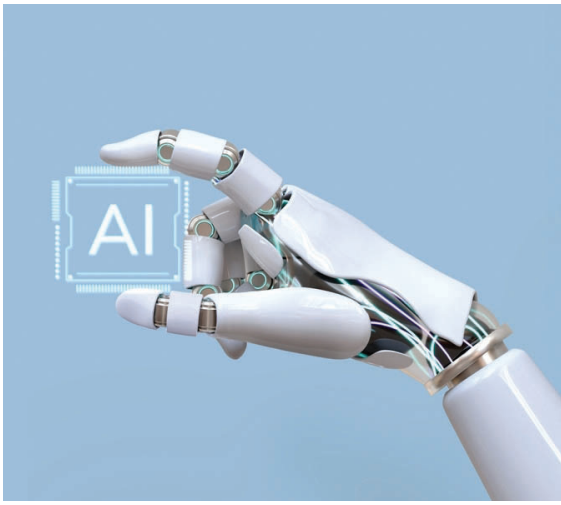
The report shows that bringing photons much closer to the compute (whether through co-packaged optics or other emerging photonic integration approaches) and using light to handle increasing parts of data movement or specific acceleration tasks can considerably improve the carbon and cost profile of AI. While photonics is not a replacement for CPUs or GPUs, it can become a critical complement that eases the pressure on them. If Europe wants sovereignty in future AI hardware and to meet its climate commitments, the report stresses that Europe’s policy and investment decisions in the coming years will be decisive.

Photonics is already essential

The report finds that photonics is already indispensable to the digital world. Fibre optics underpins today’s internet and data-centre infrastructure, and the next step of integrating light directly into chip architectures through co-packaged optics is already underway.

These advances, however, will not be enough on their own. Even with industry claims of 3.5 times greater power efficiency, TEMATYS concludes that these gains cannot fully offset the surge in energy demand driven by AI’s rapid expansion.

The study also shows that optical computing is no longer theoretical. Laboratory breakthroughs and start-up prototypes, including MIT’s 2024 demonstration of an integrated photonic chip performing neural-network computations entirely with light, reveal a clear technical path towards fully photonic processors.



Finally, the report warns that Europe has the expertise but not yet the scale. World-class research and promising start-ups exist across the continent, but without faster investment, large-scale manufacturing, and workforce development, Europe risks surrendering this strategic market to competitors abroad.

The report urges European institutions, national governments and private investors to treat photonics as strategic infrastructure for AI.

Recommended actions include: dedicated funding for pilot manufacturing, incentives to scale photonics start-ups, inclusion of photonics in Chips/AI/Green tech funding streams, and skills initiatives to build a manufacturing workforce. Without these steps, Europe risks ceding critical parts of the AI hardware value chain to overseas competitors while facing higher energy bills and emissions.

Innovations focus on photonics and FAMES success

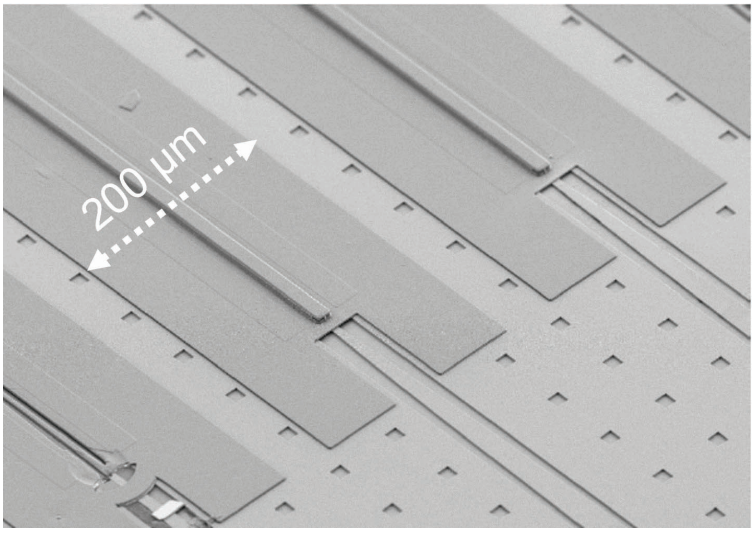
CEA-Leti has been busy in recent weeks, presenting new research at the recent SPIE Photonics West and ISSCC events, as well as focusing on the FAMES pilot line.

CEA-LETI presented new research at SPIE Photonics West highlighting major progress in the integration of quantum cascade lasers (QCLs) with silicon photonic platforms for mid-infrared (MIR) applications.

The paper, "Advanced Architectures for Hybrid III-V/Silicon Quantum Cascade Lasers: Toward Integrated Mid-Infrared Photonic Platforms," compares three complementary hybrid laser architectures that collectively advance the practicality, flexibility, and scalability of MIR photonics.

Toward 'smaller, more robust, and more manufacturable MIR systems'

Mid-infrared light plays a critical role in technologies such as gas sensing, chemical spectroscopy, biomedical diagnostics, and security, because many molecules exhibit strong absorption signatures in this spectral region. Despite the technology's importance, MIR photonic systems remain large, costly, and difficult to manufacture at scale. Integrating MIR light sources directly onto silicon photonic platforms offers a path toward smaller, more robust, and more manufacturable systems—bringing mid-infrared photonics closer to the level of integration in the near-infrared.



➤ III-V/Si Distributed FeedBack QCL.

Photo credit: Maxime LEPAGE

Three architectures, three integration strategies

In its Photonics West presentation, CEA-Leti demonstrated and compared three distinct hybrid III-V/silicon QCL architectures, each addressing a different integration challenge:

Hybrid distributed feedback QCL on silicon-on-nothing-on-insulator with adiabatic coupling

- This approach enables robust single-mode emission around 4.3 µm with efficient optical power transfer from the III-V active region into silicon waveguides. High-index-contrast silicon photonics provide precise feedback and light routing, making this architecture well suited for scalable photonic integrated circuits targeting spectroscopy and chemical sensing.

Hybrid QCL with an external silicon distributed bragg reflector cavity

- In this configuration, optical gain and optical feedback are decoupled: the III-V material provides amplification, while wavelength selection and feedback are implemented in silicon using distributed Bragg reflector (DBR) cavities. This separation offers enhanced design flexibility and opens a clear path toward tunable and multifunctional MIR sources for advanced spectroscopic and sensing systems.

Ultra-compact QCL micro-sources based on photonic crystals & micro-rings

- Miniature light sources in these devices achieve footprints below 100 μm^2 by leveraging strong optical confinement and resonant effects. The resulting extreme miniaturization enables dense on-chip integration and supports new system architectures where size, power consumption, and integration density are critical.

From passive platform to active host

Collectively, the results show that silicon photonics can play an active role in mid-infrared laser systems. By combining adiabatic optical coupling, silicon-based feedback and cavity engineering, and ultra-compact laser concepts, CEA-Leti establishes several viable integration pathways rather than a

single, one-size-fits-all solution. The work highlights how different architectures trade off stability, flexibility, and footprint, providing designers with a practical toolkit for MIR photonic systems.

"By combining quantum cascade lasers with silicon photonics, we are bringing mid-infrared sources closer to the level of integration and scalability that silicon platforms have already achieved in the near-infrared," said **Alexis Hobl, presenter and lead author of the paper.**

Looking ahead

Future work will focus on further improving optical coupling efficiency, fabrication robustness, and thermal and electrical management, as well as integrating additional on-chip photonic functions such as filters, multiplexers, and interferometric circuits. Demonstrating wafer-scale reproducibility and packaging-ready designs will be key milestones on the path toward fully integrated mid-infrared photonic systems. Acknowledgements: L'Institut des Nanotechnologies de Lyon (INL), III-V Lab, and Fraunhofer Applied Solid State Physics IAF contributed to this project.

Combined MicroLED and organic photodetector architecture

CEA-Leti also demonstrated a co-packaged microLED and organic photodetector (OPD) architecture that enables optical sensing functions. This solution paves the way to integrate sensing capabilities directly within a microLED display, without compromising display performance. The work, presented in the Photonics West paper, "Co-Packaging of Organic Photodetector with MicroLED Matrix for Multifunctional Display Bio-Application", validates a system-level approach combining device design, electronics, and modeling for multifunctional display applications.

MicroLEDs deliver high radiance using only a limited fraction of the pixel surface, leaving space for additional functionality. Leveraging this characteristic, CEA-Leti developed a microLED array co-packaged with a tailored OPD, with both devices optimized for operation at green wavelengths relevant to photoplethysmography (PPG) signal extraction.

Technology performance assessment

To move beyond component-level demonstrations, the researchers designed a dedicated electronic platform enabling full end-to-end characterization of the complete signal chain—from microLED driving, through a device under test, to photodetection and readout circuitry. Lock-in detection techniques were implemented to improve signal-to-noise ratio and suppress static parasitic components. This is particularly relevant for biosensing detection where AC/DC ratio should be enhanced.

System validation was performed using optical phantoms engineered to replicate the absorption and scattering properties of biological tissue. This approach provided a controlled and repeatable environment for assessing biosensing performance under realistic conditions. Experimental results were combined with analytical modeling to derive a closed-form expression linking microLED operating conditions, photodetector responsivity, and device-under-test reflectance to the detected signal.

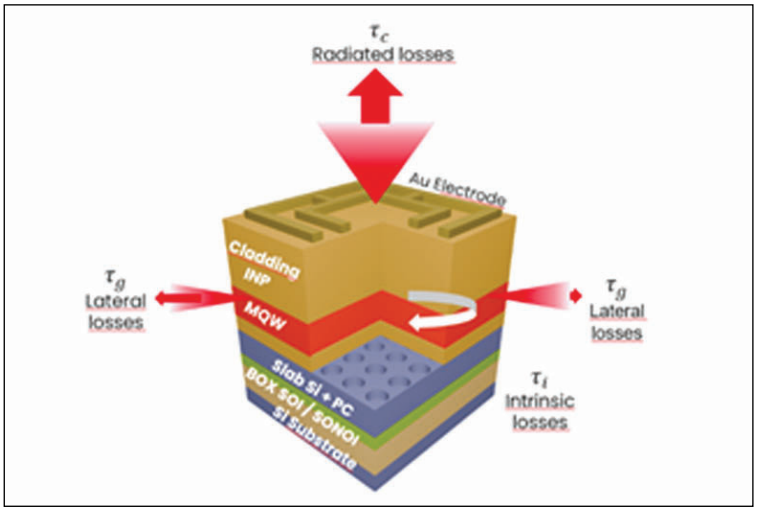


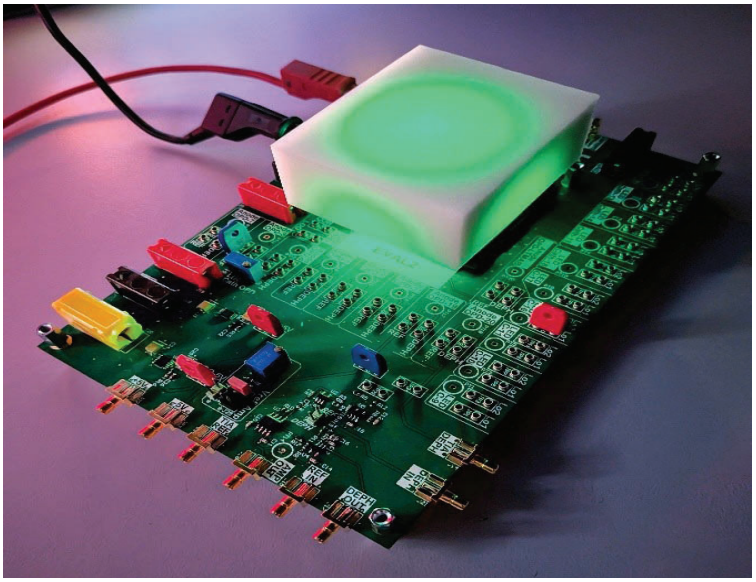
Image Credit: Alexis Holb

➤ III-V/Si Photonic Crystal Surface Emitting QCL & Micro-resonator Ring.

The co-packaged microLED devices demonstrated optical power up to 12 mW at a wavelength of 525 nm. On the detection side, OPD responsivity was tuned by adjusting the thickness of the ZnPc active layer to align with the microLED emission peak, achieving a responsivity of 0.083 A/W at the wavelength of interest.

Benefits of MicroLED technology

The results show that microLED displays can support integrated optical sensing at the pixel level without forcing trade-offs between brightness, resolution, and sensing area. Unlike OLED-based approaches, where display and sensing functions compete for the same



➤ Characterization platform including custom electronic board and biological phantom mimicking human tissues
Photos credit: Eric Kroemer/CEA-Leti

Photo credit: Eric Kroemer/CEA-Leti

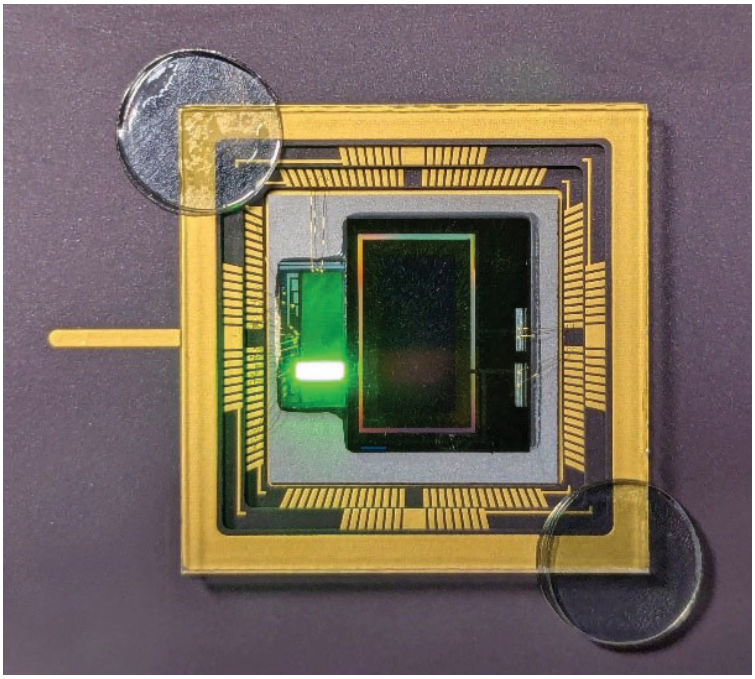
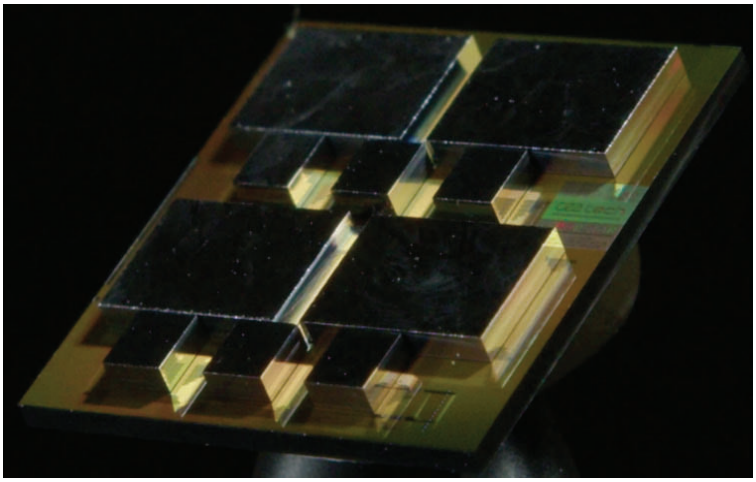


Illustration of co-packaged OPD and MicroLED matrix

Photo credit: KAM Productions



Detail view of the system-on-interposer, with a companion electro-optical router for each computing die and two additional routers for primary IO. Light coupling to the optical network on interposer is achieved on fiber coupling visible on the bottom-right corner.

surface, this architecture allows both functions to coexist within the same front plane.

The fully characterized, end-to-end system establishes a technical foundation for displays that combine visual output with integrated sensing and adaptive functions, with potential relevance for next-generation displays. Rather than relying on sensors located usually in the bezel of the display, this approach enables sensing capabilities to be designed directly into the display and widespread.

System-technology co-design approach

"This work illustrates CEA-Leti's system-technology co-design approach, from concept definition and microLED technology to photodetector co-design, electronics development, and experimental validation under realistic conditions," said Michaël Pelissier, lead author of the paper. "By combining hardware development with analytical modeling and simulation, we establish a concrete framework for evaluating and scaling sensing-integrated display architectures."

The study establishes practical know-how for co-integrating microLED displays and optical sensing functions. The architecture is inherently scalable and can be adapted to different pixel pitches and resolutions, depending on the targeted application—from medium-size displays such as smartphones and wearables to larger formats including monitors and televisions.

The results provide a technical foundation for future multifunctional displays in which visual output and sensing capabilities are designed together, at the system level, rather than added as separate components. This work is part of the IPCEI Microelectronics and Connectivity and was supported by the French Public Authorities within the frame of France 2030.

First dynamically routed electro-optical router for photonic interposers

Researchers from CEA-List and CEA-Leti unveiled at ISSCC the first electro-optical router with dynamic, frame-level optical routing integrated with CMOS control logic, marking a major step toward practical optical networking inside advanced chiplet-based packages.

Their paper, "**A 3.19pJ/bit Electro-Optical Router with 18ns Setup Frame-Level Routing and 1-6 Wavelength Flexible Link Capacity for Photonic Interposers**", demonstrates an electro-optical router implemented in 28 nm CMOS on a photonic interposer, capable of establishing optical paths in 18 nanoseconds. It dynamically selects one-to-six wavelengths per link, and achieves an energy efficiency of 3.19 pJ/bit with an active area of just 0.007 mm^2 per link.

Moving optical links beyond static point-to-point

Today's optical interconnects are largely limited to static, point-to-point links, with initialization and training times ranging from microseconds to milliseconds. While suitable for board-level or rack-scale communication, those latencies prevent optical links from being used as a true networking fabric inside multi-die packages.

The router addresses this gap by integrating optical switching, routing control, serializer/deserializer (SerDes), and clocking logic directly with silicon photonics. The result is a dynamically routed optical interconnect that operates at nanosecond timescales, enabling optical communication across centimeter-scale interposers with responsiveness

previously limited to short electrical links. It supports frame-level routing, allowing optical paths to be established and torn down on demand, and adjusts link capacity dynamically by selecting between one and six wavelengths, according to application needs. This flexibility enables efficient use of optical bandwidth, while maintaining ultra-low latency.

Architecture and implementation

The prototype is fabricated in a 28 nm CMOS process and integrated on a photonic interposer. Compact analog drivers, combined with standard-cell-based SerDes and clocking circuits, enable dense integration of optical endpoints close to compute and memory resources. While the architectural target includes CPUs, GPUs, and high-bandwidth memory (HBM) in large 2.5D and 3D packages, the current chip serves as a proof of concept, demonstrated on a small-scale multi-die system derived from CEA-Leti's earlier INTACT active interposer architecture (ISSCC 2020).

A first integrated dynamic optical routing

This is the first demonstration of dynamic optical routing in an integrated photonic switch that includes CMOS logic up to the protocol level. Previous optical switch demonstrations typically rely on standalone photonic devices with static or slowly reconfigured paths and do not integrate the full driving, control, and routing logic required for packet-level operation. In contrast, the router operates as a miniature network switch inside the package, combining microring-based photonic devices with digital control logic to move data efficiently across the interposer. Compared with electrical routing fabrics or active interposers, the approach avoids power and latency penalties that scale with distance, relaxing constraints on data locality and enabling more flexible hardware architectures and software data placement.

Enabling new chiplet architectures

By bringing dynamic, ultra-low-latency optical networking into the package, the technology opens new possibilities for high-performance computing, AI accelerators, and data-intensive systems, where growing model sizes and memory demands increasingly stress conventional interconnects.

Rather than forcing all data to reside near compute cores to minimize electrical routing costs, dynamically routed optical links allow architects to treat memory and compute resources across the interposer as part of a unified, high-reach fabric without sacrificing latency or energy efficiency.

"As chiplet systems continue to grow in scale and complexity, the ability to move data efficiently across the entire package becomes essential," said CEA-List's Yvain Thonnart, lead author of the paper. "Our goal was to demonstrate that photonic links can provide that reach without sacrificing the flexibility designers expect from modern interconnects. This router is a step toward practical, dynamically routed optical networks that fit within standard CMOS design flows and real product constraints."

Validating first ultra-fast, battery-operated EPR Spectrometer at chip scale

Researchers at CEA-Leti and CEA-IRIG-SyMMES have validated a chip-scale electron paramagnetic resonance (EPR) spectrometer that achieves unprecedented scan speed, spectral span, and sensitivity from a battery-operated integrated circuit. By replacing the bulky electromagnets used in conventional EPR instruments with an ultra-fast frequency-scanned architecture, the system enables high-performance paramagnetic sensing in portable and space-constrained environments where traditional systems cannot operate.

The results were presented at ISSCC 2026 in the paper "**A 1400 THz/s Ultra-Fast-Scan 14 GHz EPR-on-a-Chip Based on Injection-Locked Phase Detection Featuring 120 µM Concentration Sensitivity.**"
Miniaturized EPR spectrometers transform a complex laboratory instrument into a portable, low-power microchip capable of detecting reactive chemical species that influence energy storage, materials reliability, environmental safety, and biomedical processes. By eliminating the bulky electromagnet that traditionally limits EPR instruments to centralized facilities, this technology, sometimes dubbed "EPR-on-a-chip", makes it possible to perform high-precision analysis directly in the field, at industrial sites, or inside research systems where traditional tools don't fit.

Record performance at milliwatt power levels

The system delivers:

- 1,400 THz/s scan rate
- 100-Gauss equivalent spectral span
- 120 µM concentration sensitivity
- 96 mW power consumption
- 200 ns scan time across the full span

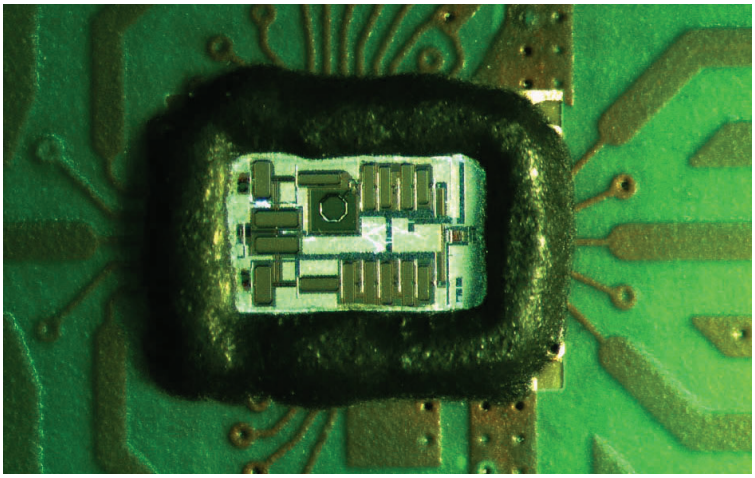
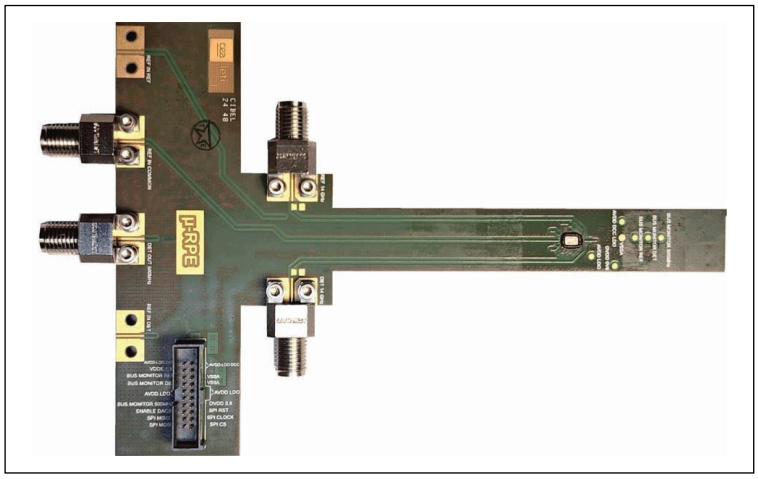


Photo credit: JB.David_CEA

➤ On-chip EPR spectrometer, fabricated on CMOS GF22nmFDSOI technology. The 4.4mm2 passivated circuit is mounted on a Printed Circuit Board (PCB), and bondings are molded. The sample to be analyzed is directly deposited onto the chip.

Photo credit: JB.David_CEA



➤ The 96mW on-chip EPR spectrometer is programmed, driven, and monitored through a dedicated Printed Circuit Board. The PCB aspect-ratio fits with the need to insert the chip inside a 0.5T permanent magnet.

This performance exceeds that of state-of-the-art miniaturized EPR devices, which typically trade sensitivity and spectral range for speed. The combination of ultra-fast scans and wide spectral coverage enables observation of fast-passage effects and transient phenomena in chemical reactions that are difficult or impossible to capture with existing systems.

New applications across healthcare, materials, and the environment

By shrinking EPR to chip scale, CEA-Leti and CEA-IRIG open new application paths in healthcare diagnostics, materials characterization, and environmental monitoring. Portable, low-power EPR sensing could support on-site chemical analysis, embedded monitoring in research systems, and distributed sensing networks. As development advances toward a full prototype, the technology represents a significant step toward making high-precision spectrometry more accessible and deployable beyond the laboratory.

Injection-locked phase detection enables high sensitivity

At the core of the system is an original injection-locked phase-detection architecture that encodes the EPR signal as a phase shift rather than an amplitude or frequency change. By exploiting the intrinsically low phase noise of injection-locked oscillators, the design achieves unprecedented sensitivity for a single-sensor, chip-scale EPR system.

"Our goal is to create a compact, portable EPR spectrometer that operates on just a few watts of power, enabling on-site analysis in environments where conventional instruments simply cannot operate," said Serge Gambarelli, research director at CEA-IRIG and EPR spectroscopy expert.
"By adapting RF and frequency-synthesis architectures originally developed for telecommunications, we were able to integrate a complete EPR system on a single 22 nm chip," said Alexandre Siligaris, senior research engineer at CEA-Leti.

A milestone for european scientific instrumentation

The circuit is the first scientific instrument fabricated using the advanced 22 nm FDSOI technology. While manufactured by GlobalFoundries, an international fab partner of CEA, the system architecture, circuit design, and measurement approach were fully developed and patented by CEA. The work marks a major milestone in CEA's Moonshot µ-RPE program, which aims to develop a compact, deployable EPR spectrometer to support key missions of CEA—and highlights Europe's leadership in advanced microelectronics for scientific instrumentation. The Moonshot program also includes R&D on planar magnets, which are key to future spectrometers, because they increase the number and field of applications.

"Typically applied in electric mobility and energy transition sectors, this expertise is now being leveraged to design the magnetic system for the µ-EPR spectrometer, demonstrating a valuable transfer of knowledge into the field of instrumentation," said Celine Delafosse, laboratory manager at CEA-Liten, which is leading that research area.

FAMES pilot line inaugurated after delivering

The FAMES Pilot Line was officially inaugurated at the end of January - two years after it began, now delivering validated technical results across advanced FD-SOI, RF, embedded non-volatile memories, 3D integration technologies, and Power Management ICs. Those results, produced on a 300 mm line and reported at leading international conferences, confirm that the European tech-sovereignty initiative is already operating as a working European semiconductor capability.

The inauguration, attended by more than 350 people, marked the launch of a cleanroom extension at CEA-Leti's Grenoble site. The open-access feature of the pilot line makes the FAMES technologies accessible primarily, but not exclusively, to European startups, SMEs, industrial groups, and research organizations seeking to prototype, qualify, and de-risk advanced semiconductor technologies before industrial deployment. The initiative is coordinated by the CEA.

Technological momentum

Since entering operation, the pilot line has generated concrete advances across its core domains, spanning substrates, embedded ferroelectric non-volatile memories, advanced FD-SOI, 3D integration, high performance RF passive components—areas critical to next-generation chips.
"The breakthrough technologies developed within FAMES are intended to support future generations of sub-10 nm FD-SOI chips, enabling

high-performance and low-power components for Europe," said Jean-René Lèquepeys, deputy director and CTO of CEA-Leti. "Scaling down the FD-SOI technology to 10 and 7nm will bring significant chip performance improvements compared to current nodes, in density, power consumption, speed and radio-frequency behavior."

Among the most recent milestones, CEA-Leti recently presented results at IEDM 2025 demonstrating fully functional 2.5 V SOI CMOS devices fabricated at a thermal budget of 400 °C. Achieving performance comparable to conventional high-temperature CMOS, the work removes a key barrier to large-scale 3D sequential integration and enables dense multi-tier chip architectures compatible with advanced back-end processes—one of the central technical objectives of FAMES.

Ultra-efficient ecological systems

With 2,000 m^2 of cleanroom space, the new facility expands CEA-Leti's cleanroom space to 14,000 m^2. It will house more than 80 state-of-the-art 300mm cleanroom tools. Two basement levels help manage complex technical installations, and a five-meter ceiling height accommodates large equipment. In addition, very low vibration levels and dedicated electrical back-up systems will ensure uninterrupted operation.

In addition to housing some of the semiconductor industry's most specialized and sophisticated tools, the facility has been equipped with systems and processes enabling advanced optimization of its environmental footprint. The building incorporates high-performance insulation requirements and will enable the implementation of waste-energy recovery solutions (residual heat recovery).

Following the French France 2030 NextGen project, which was launched in 2022, the FAMES pilot Line project provided additional momentum in 2023 under the EU Chips Act. These two initiatives were designed to shorten the path from research to industrial readiness by providing a leading edge, open-access environment for technology innovation.

'The role FAMES is meant to play'

"The fact that results are already being published and validated internationally underscores the role FAMES is meant to play," said Dominique Noguet, vice president at CEA-Leti and coordinator of the pilot line. "This is not a future manufacturing line. It is an operational platform where advanced technologies are being matured, demonstrated, and prepared for transfer to industry."

With a total investment of €830 million, co-funded by the European Commission under the Chips Act and by participating Member States, FAMES brings together 11 partners across eight countries. Its objective is to reduce the time between research and industrialization, while strengthening Europe's technological autonomy in semiconductor domains that underpin strategic sectors including automotive, telecommunications, edge AI, industrial systems, health, space, and cybersecurity.

By inaugurating a pilot line that is already producing validated results, FAMES exemplifies the lab-to-industry model at the core of Europe's semiconductor strategy—providing industry with access to mature technologies, proven processes, and a direct path toward future manufacturing.

'Fully aligned with the ambition of the chips act'

"With the inauguration of FAMES, the CEA is providing Europe with a unique capability to accelerate the maturation of strategic technologies and their transfer to industry," said Anne-Isabelle Etienvre, the Director General of the CEA. "This success illustrates the strength of our 'lab to industry' model, based on scientific excellence and close operational relationships with industrial players. It is fully aligned with the ambition of the Chips Act and is already preparing the next step: consolidating, with our partners, a long-term European dynamic to secure innovation and technological sovereignty in microelectronics."

Pivotal milestones in silicon photonics and the NanoIC pilot line

Imec has been as busy as ever, collaborating with Veeco Instruments to accelerate datacom and quantum computing applications, as well as sharing recent NanoIC pilot line developments.

VEECO INSTRUMENTS and imec announced have collaboratively developed a 300mm high volume manufacturing compatible process that enables the integration of barium titanate (BaTiO3 or BTO) on a silicon photonics platform. BTO is a promising material with unique electro-optical properties that can be used for high-speed and low-power light modulation in emerging applications such as high-speed optical transceivers, quantum computing, light detection and ranging (LiDAR), and AR/VR applications. Historically, approaches to integrate BTO have struggled to meet the desired cost targets to make it viable for high-volume manufacturing.

Veeco has now delivered its first Molecular Beam Epitaxy (MBE) based cluster system, marking a significant milestone in Veeco's and imec's partnership and their dedication to enhance silicon photonics platform capabilities. The new 300mm platform is designed for the epitaxy of BaTiO3 single crystalline thin films on silicon, available with both solid and hybrid Molecular Beam Epitaxy (MBE) solutions. With the integration of these alternative growth techniques, the system will be capable of BTO-on-Si deposition with improved repeatability and at a lower cost than classical MBE methods.

The optical transceiver market for datacom is expected to grow to $13.1 billion in 2030, up from $2.9 billion in 2024. However, to alleviate the trade-offs of current silicon modulator technologies, including high power consumption, performance (speed, drive voltage), and area, the introduction of novel electro-optic materials, like BTO, into silicon photonics will be crucial. At present, there is no commercially available production-compatible solution for manufacturing these materials. In partnership with Veeco, imec is now addressing this industry need to develop scaled solutions that allows the integration of materials such as BaTiO3 and SrTiO3 onto a 300mm silicon platform.

"Over the past 4 years, imec and Veeco have collaborated on developing alternative techniques for BaTiO3-on-Si and benchmarking both material and electro-optic properties towards defining a strategy for advancing large-scale manufacturing solutions," says Clement Merckling, Scientific Director at imec. "With the introduction of Veeco's first-of-its-kind MBE solution, we are expanding our capabilities for heterogeneous integration of beyond-Si electrooptic materials, strengthening our R&D offering for current and new partners with an interest in exploring and prototyping next-generation silicon photonics technology." added Joris Van Campenhout, imec Fellow and Optical I/O Program Director.

"This partnership with imec is a monumental step forward for the MBE industry, datacom and quantum computing production," commented Matthew Marek, Senior Director of Marketing for Veeco's MBE Product Line. "The historic view of MBE processing has been that it is slow and expensive; however, new hardware developments that our team validated in partnership with imec bring MBE into a cost-effective domain that is suitable for semiconductor fabs. We are excited about the work underway between our two organizations to demonstrate a repeatable, high-volume BTO production process. We anticipate this effort will help us achieve our shared goal to unlock BTO photonic modulator breakthroughs for a better and greener future."

Imec inaugurates NanoIC pilot line

Imec recently inaugurated a 2,000m^2 cleanroom expansion at its Leuven headquarters, marking a pivotal milestone in the deployment of Europe's NanoIC pilot line. The event was attended by European EVP Henna Virkkunen, Belgian Prime Minister Bart De Wever, Flemish Minister-President Matthias Diependaele, and ASML CEO Christophe Fouquet, alongside representatives from the European high-tech ecosystem – including industry and startups – the NanoIC pilot line consortium, and policymakers from the EU, Belgium, and Flanders. With a capacity of over 12,000 m^2, imec's cleanroom plays a crucial role in the European Chips Act's ambitions to position Europe at the forefront of next-generation semiconductor innovation and manufacturing; a strategy that will be instrumental in reinforcing the continent's industrial fabric in the AI era, while safeguarding a climate of sustained economic growth, security, and prosperity for decades to come.

"Since announcing in May 2024 that imec would host the NanoIC pilot line, we've moved at full speed – accelerating tool acquisition and launching a comprehensive recruitment program. Today, that effort culminates in the inauguration of a 2,000m^2 cleanroom extension at the imec premises. It will house a best-in-class toolset, including ASML's next-generation High NA EUV scanner that is scheduled to arrive mid-March," said Luc Van den hove, CEO of imec.

"Imec researchers are working here side by side with IDMs, foundries, equipment and materials suppliers, system companies, start-ups, universities, and fellow European RTOs. Together, we have embarked on an ambitious journey to push semiconductor technologies beyond the 2nm node. By providing access to cutting-edge semiconductor technologies, the NanoIC pilot line will play a crucial role in strengthening Europe's industrial fabric in the AI era, and ensuring a climate of economic growth, security, and prosperity for decades to come," he added.

Strategic importance and future outlook

And the momentum continues. With strong backing from the European, Belgian, and Flemish governments – and a robust network of industry partners – imec will soon begin construction of a whole new 4,000m^2 cleanroom at its Leuven campus, another key asset to bring Europe's NanoIC initiative to full cruising speed. Over the next five years, the NanoIC pilot line will integrate more than a hundred new tools, distributed across imec and partner sites at CEA-Leti (France), Fraunhofer (Germany), VTT (Finland), CSSNT-UPB (Romania), and Tyndall National Institute (Ireland).

"We don't have the luxury of being the biggest or the strongest, but we do have the choice to be the best," explains Matthias Diependaele, Flemish Minister-President. "Imec brings together talent, knowledge, and international collaboration. With the NanoIC pilot line, Europe is making that choice a reality: for technological excellence and strategic independence. The fact that imec is hosting this pilot line underscores the exceptional strengths that Flanders has developed in research and innovation. Here, we are demonstrating how a world-class region can shape the chip technology of tomorrow."

A step forward for European semiconductor leadership

Christophe Fouquet, President and CEO of ASML commented: "Today we are making a step forward in strengthening the chip technology ecosystem in Europe to serve our customers, the world's chipmakers. Through our 40 years partnership at imec, together we have been driving faster innovation, fostering stronger collaboration, and supporting the development of regional talent, all of which are needed to support the advancement of the worldwide chip industry and AI. We are today

➤ Imec's cleanroom provides the foundation for NanoIC's PDKs, based on 2 nm process flows.

inaugurating the NanoIC pilot line, that includes ASML's High NA EUV system and which is the best example of what we can do when worldwide leaders in technology partner to bring together their latest technology and talent. Thanks to the strong support of EU President Von der Leyen and the European Chips Act, we are all very proud and thankful that this is happening at the heart of Europe and will allow Europe to play an even more critical role in the global semiconductor ecosystem"

NanoIC extends its PDK portfolio

The NanoIC pilot line, a European initiative coordinated by imec and dedicated to accelerating innovation in chip technologies beyond 2nm, has released two new process design kits (PDKs): an A14 pathfinding PDK for advanced logic scaling and an eDRAM system exploration PDK for advanced memory innovation. Both PDKs are firstoftheirkind releases, providing early access to cutting-edge design rules and flows, and giving users a unique gateway to investigate advanced technology nodes and embedded memory designs.

The advanced Process design kits (PDKs) from the NanoIC pilot line play a key role in advancing semiconductor innovation. They give designers early access to realistic design rules and implementation workflows long before hardware for a new technology exists. With the introduction of the A14 and eDRAM PDKs, NanoIC for the first time gives designers early insight into two critical technology areas for future compute systems: logic scaling at the A14 Angstrom node and embedded memory integration.

By making these PDKs freely accessible, NanoIC seeks to connect early-stage design exploration with real-world integration, helping researchers and startups explore emerging nodes, anticipate integration challenges, and benchmark designs against realistic scaling metrics. "PDKs like A14 and eDRAM are catalysts for learning and design", Marie Garcia Bardon, Department Director at imec and work package leader within the NanoIC project, explains. "They offer a robust environment for hands-on evaluation and quantitative comparison of different technology choices. This approach accelerates learning, de-risks architectural and design innovation, and helps designers prepare for advanced logic nodes and embedded memory technologies well before hardware becomes available."

"By making these PDKs broadly accessible, we lower barriers for universities, industry, and startups to engage with next-generation technologies", Giuseppe Fiorentino, program manager for NanoIC continues. "Access to realistic rules and flows enables teams to explore new research directions and breakthrough concepts that will feed directly into the European semiconductor value chain."

A14 pathfinding PDK: scaling down to the 14-Angstrom node

As the first of the newly launched PDKs, the A14 pathfinding PDK provides a virtual design environment for exploring scaling at the 14Angstrom node, one of the next major steps in device miniaturization. A key innovation at this node is the introduction of a direct backside contact as a new scaling booster. Whereas the earlier N2 PDK supported backside power delivery through TSVMiddle (TSVM) structures, the A14 node advances this concept by replacing TSVM with a more compact direct backside contact scheme. By

routing power directly from the wafer's backside to the gates and removing the need for complex topside metal routing, this architecture reduces IR drops and delivers an 18% area gain and 7% power reduction compared to N2 at iso frequency and cell density.

Imec is the first to release a PDK at this node. The kit includes a comprehensive 162SDC library and is supported by two major EDA vendors, Cadence and Synopsys.

eDRAM system exploration PDK: enabling embedded memory exploration

Complementing the logic pathfinding work enabled by the A14 PDK, the NanoIC pilot line also introduces a first eDRAM system exploration PDK, an important step toward addressing one of the biggest challenges in advanced systems: providing dense, low-latency on-chip memory. Central to this effort is bringing memory closer to the processing units, a key strategy for reducing latency and improving power efficiency in advanced compute architectures.

The current eDRAM PDK provides a virtual platform for exploring embedded memory solutions that bridge the gap between dense but power-hungry off-chip DRAM and fast but area-limited on-chip SRAM. With a focus on systemlevel behavior in dataintensive and AI workloads, it enables researchers to evaluate new memory architectures and integration strategies that bring higherdensity memory closer to processors and GPUs, reducing data movement, improving energy efficiency, and enhancing overall system performance.

Looking ahead, the eDRAM PDK will evolve into a full system exploration platform. This next phase will allow designers to move beyond virtual validation and analyze complete system-level interactions. As the platform matures, future development steps include hardware validation and, eventually, opportunities for tapeout and prototyping on the NanoIC pilot line.

Access and training opportunities

Both PDKs, together with the previously launched N2 PDK, are available through Europractice. To encourage adoption and hands-on exploration, NanoIC will also host a dedicated workshop on the N2 and A14 PDK on March 25–26, 2026, and on the eDRAM PDK on May 26, 2026. These workshops will offer practical guidance, technical insights, and direct interaction with the development teams. All practical details and registration are available on the NanoIC website.

This work has been enabled in part by the NanoIC pilot line. The acquisition and operation are jointly funded by the Chips Joint Undertaking, through the European Union's Digital Europe (101183266) and Horizon Europe programs (101183277), as well as by the participating states Belgium (Flanders), France, Germany, Finland, Ireland and Romania. For more information, visit nanoic-project.eu.

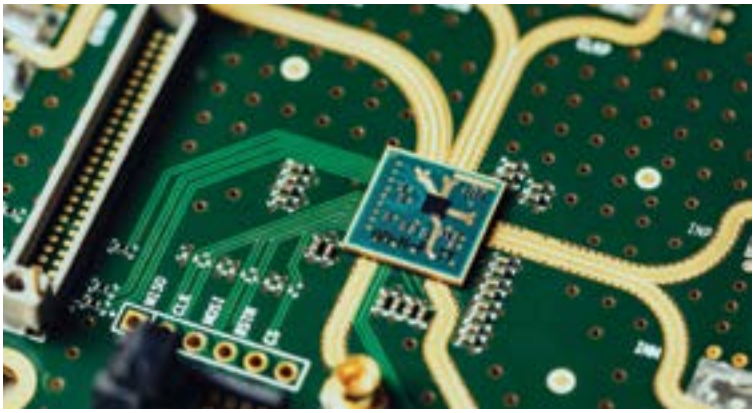
NanoIC adds advanced SRAM memory macros
NanoIC pilot line has also released the N2 P-PDK v1.0, an important update of its N2 Pathfinding Process Design Kit (P-PDK). This new version introduces several new features, including a library of 29 SRAM memory macros, allowing designers to explore and benchmark system-on-chip (SoC) designs with frontside and backside power routing. By adding the SRAM macros in the design options, the N2 P-PDK v1.0 marks an important milestone in enabling research, learning, and design exploration on advanced and future nodes.

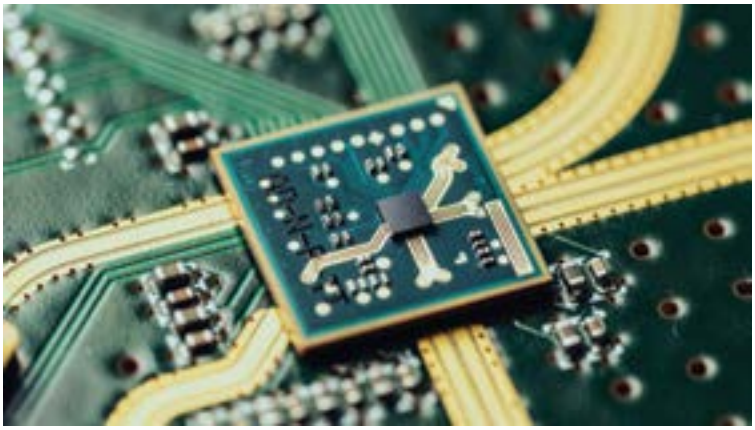
Towards next-generation SoC designs

As chip technologies scale beyond 2nm, the ability to explore full System-on-Chip (SoC) architectures with novel technology enablers becomes increasingly important. SoCs, integrating logic, memory, and interconnect capabilities into a single chip, are the backbone of a wide variety of digital applications, from smartphones and AI accelerators to automotive controllers. However, early-stage SoC design exploration is often constrained by limited access to complete and realistic design kits that include advanced or future technology scaling boosters such as power delivery networks. This gap makes it difficult for designers to validate architectural concepts, experiment with emerging technologies, or to train the next generation of chip designers on advanced nodes.

NanoIC's low-barrier N2 P-PDK v1.0 aims to bridge this gap, offering instant access to a wide variety of new design features, including a portfolio of 29 ready-to-use SRAM macros with both frontside and backside power routing configurations.

This dual configuration, offered for the first time in a pathfinding PDK, enables designers to experiment with and optimize memory integration within realistic, advanced power networks. As a result, NanoIC's N2 P-PDK v1.0 now provides the building blocks of a complete SoC as well as the architectural context to explore how those blocks interact within realistic power networks. It enables users to move beyond simple logic design and explore and





validate full SoC systems that reflect the challenges and opportunities of next-generation semiconductor design.

Lowering barriers for learning and exploration
By making these advanced features freely available to academic researchers, startups, and design teams, NanoIC significantly lowers the barriers to innovation, empowering the development of next-generation applications, and strengthening Europe's position in the global semiconductor landscape.

"This v1.0 version of our N2 P-PDK enables designers to evaluate the impact of new technology features and integration options on their designs before they exist in foundry offerings. It provides a unique environment to connect technology pathfinding with practical design enablement, ensuring that breakthroughs in device research translate into system-level advances.", Marie Garcia Bardon, Department Director at imec and work package leader within the NanoIC pilot line, summarizes.

Building on the learnings from the previous N2 P-PDK, this release lays the groundwork for future PDK iterations, launching additional advanced logic, memory, and interconnect PDKs in the coming years. The roadmap includes future versions of the N2 P-PDK, as well as upcoming A14 and A7 logic P-PDKs, eDRAM and SOT memory PDKs, and advanced interconnect solutions (RDL, hybrid bonding, interposers), empowering innovation across the full spectrum of next-generation chip technologies.

Imec unveils 7bit, 175GS/s massively time-interleaved slope-ADC

At the recent IEEE ISSCC 2026, imec – a world-leading R&D center in advanced semiconductor technologies – unveiled a 7bit, 175GS/s analogtodigital converter (ADC) that combines a record-small footprint (250 x 250µm^2) and low conversion energy with one of the fastest sampling speeds ever reported. As such, imec's ADC meets the rapidly increasing throughput and processing demands of AI- and cloud-driven data centers, without the area and power explosion typically seen at ultra-high sampling rates.

Driven by AI and cloud applications, data centers' optical communication networks need constant upgrades to handle ever-higher throughputs and processing demands. But as sampling rates climb beyond 100GS/s, the underlying components – such as wireline ADCs, essential in optical transceivers – tend to grow in size, requiring longer interconnects, and introducing parasitics and energy loss.

At the 2024 edition of the IEEE International Solid-State Circuits Conference (ISSCC), imec tackled this challenge with a breakthrough: a massively time-interleaved slope-ADC architecture at least twice as compact as conventional designs and featuring state-of-the-art power efficiency. Building on that approach, imec now takes the next step with the introduction of a record-small ADC that ensures precise signal conversion and wide bandwidth at ultra-high sampling rates.

Patented linearization and switched input buffers techniques

"Our 7-bit, 175GS/s ADC – implemented in 5nm FinFET technology – pairs a record-small core area of 250 x 250µm2, and low conversion energy (2.2 pJ per sample), with a sampling speed that ranks among the fastest ever reported. This makes it a compelling solution for upscaling digitalintensive wireline interconnects, where every square micron and milliwatt count," said Peter Ossieur, portfolio director at imec. Two patented innovations make this possible. First, a novel linearization approach – shaping the slope signal – corrects distortions. Second, switched input buffers efficiently feed the ADC's 2,048-channel time-interleaved array, minimizing electrical load and enabling ultra-fast sampling without compromising signal integrity.

Pushing toward – and beyond – the 300GS/s milestone

Building on the ADC presented at this year's ISSCC, imec is now developing a 3nm followon design and exploring 14 Ångstrom designs, in particular how such advanced nodes can be leveraged for high-performance wireline data converter designs.

Peter Ossieur comments: "Imec has a long-standing track record in developing high-speed integrated circuits for communication applications. One of our key research tracks focuses on optical transceivers (and their building blocks) that can keep pace with the rapidly increasing data rates in wireline systems. In this context, our ADCs represent a crucial step toward a new generation of compact, low-power converters for future wireline applications, pushing beyond the performance limits of SAR-based ADC architectures at ultra-high speeds. To accelerate this effort, we warmly invite partners – including fabless companies developing wireline connectivity building blocks – to join our ADC and DAC research programs, with licensing options available to access imec's underlying IP portfolio."

Powerful inspection solutions for wafer and chip level packaging.

From root cause analysis in the lab, to fast process analysis in the fab, Comet's leading 2D and 3D X-ray technology provides powerful inspection solutions for wafer and chip level packaging, enhanced with incredible AI-based software.

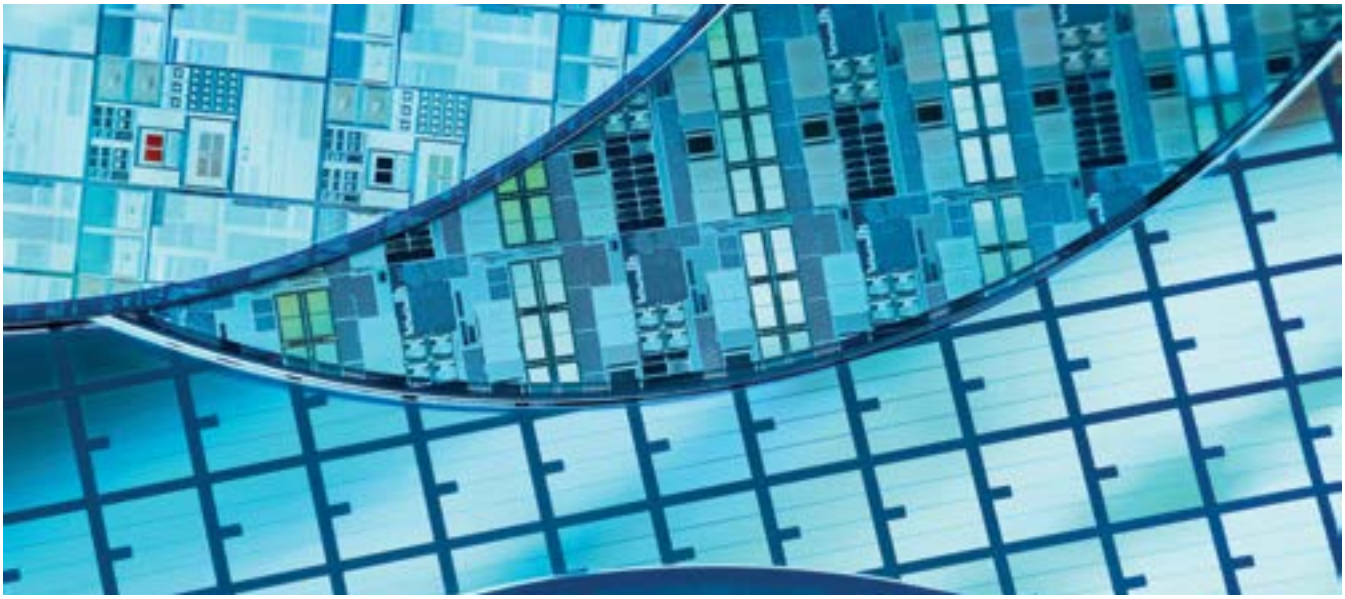
	Height	Diameter
TSV	105 µm	10 µm
Void	50 µm	6 µm

Visualization of 3D X-ray inspection results of TSV fills in a wafer. Wafer designed for Comet by Fraunhofer IZM_ASSID, it contains voids for illustrative purposes.

Contact us to learn more, or explore our entire portfolio

comet

yxlon.comet.tech



Semiconductor memory market: the forerunner of the next wave of digital transformation

As we stand at the abyss of the AI transformation, automation, and the hyper-connected Internet of Things (IoT), semiconductor memories are meeting all the requirements of the digitized ecosystem. In this blog, let's dive deeper into the facts that make the industry a revenue-generating and one of the most important markets in the future.

DATA CENTERS are rapidly proliferating to meet the global demand. Moreover, Saudi Arabia's HUMAIN–National Infrastructure invested around USD 1.2 billion for 250MW of AI data center capacity in January 2026, signaling how the world depends on digitalization. As the world enters the era of data and digital information, semiconductor memories become the trailblazer for having smoother storage and effective operations. As we stand at the abyss of the AI transformation, automation, and the hyper-connected Internet of Things (IoT), semiconductor memories are meeting all the requirements of the digitized ecosystem.

The Semiconductor Industry Association (SIA) shared that the global semiconductor industry sales reached more than USD 75.3 billion as of November 2025, which demonstrated an increase of almost 29.8% compared to November 2024. These statistics showcase the highest demand for semiconductors across industries, which is a key enabler of the advancements of the memory industry.

In this blog, let's dive deeper into the facts that make the industry a revenue-generating and one of the most important markets in the future.

Rapid demand of semiconductor memory in cross sectors - from being a storage keeper to a key enabler

The concept of memory has redefined itself from just a data retention to an active intelligence enabler. This exceedingly data-driven world creates a pressing need for memory solutions that are faster, denser, more energy-efficient, and increasingly specialized. Here are a few sectors that make the most use of semiconductor memories.

- **Artificial Intelligence and Cloud Infrastructure**

The emergence of AI has massively transformed the way memory was perceived earlier. High-bandwidth memory (HBM) architectures, engineered to support massive data throughput, are now a needed ingredient in AI accelerators and data center servers. In fact, a leading key player, Samsung Electronics, predicts a shortage of chip production due to the AI boom, with strong memory demand benefiting its mainstay chip business. These high-performance, advanced memory chips help in keeping the data close for low latency of networks. Giant industry players like Samsung, SK Hynix, and Micron are making unwavering efforts to scale HBM manufacturing. For instance, Samsung projects a robust tripling of HBM revenue as demand skyrockets, specifically among hyperscale AI customers, whereas SK Hynix commands over 60% of the share in the next-generation memory market.

- **Consumer Electronics**

Memory chips remain embedded in the ecosystem of consumer devices. As the demand for advanced smartphones, gaming consoles, laptops, and wearables increases, the demand for DRAM and NAND flash increases for high-speed data access and storage performance. In fact, the trade data reports confirmed that consumer

electronics accounted for more than 35% of market share in 2024. The ongoing supply challenges are primarily due to memory capacity being reallocated to high-end AI infrastructure, increasing the use of semiconductor memory across consumer electronics. As the demand for consumer electronics grows, for instance, India's electronics manufacturing increased by around sixfold and exports accelerated to nearly eightfold from 2014 to 2025, the need for seamless storage systems increases.

Automotive and Industrial IoT

As the global mobility systems become smarter and the incorporation of sensors and ADAS becomes essential to monitor the electric systems, the memory chips are becoming critical in the automotive industry. The global governments are vigilant on reducing CO_2 emissions and making unwavering efforts to promote vehicles that do not run on fossil fuels. Also, the official data implied that worldwide, more than 22% of passenger vehicles sold in 2024 were electric, which is around eightfold compared to earlier 5 years, and China alone sold nearly 11.3 million EVs. This significant number suggests that the world is inclining towards electric and non-fossil fuel mobility systems, which in turn require better grid systems and powerful memory backup.

Meanwhile, industrial automation and edge computing systems require domestic intelligence and system reliability, for which they depend on memory. The world is continuously adopting automation across smart factories. Here's how the robotics installations increased from 2021 to 2023.

The rising robotics adoption creates a pressing demand for semiconductor memory, which presents a great opportunity for manufacturers and suppliers. These applications underline performance under turmoil conditions

> Data centers are rapidly proliferating to meet the global demand. Moreover, Saudi Arabia's HUMAIN–National Infrastructure invested around USD 1.2 billion for 250MW of AI data center capacity in January 2026, signaling how the world depends on digitalization. As the world enters the era of data and digital information, semiconductor memories become the trailblazer for having smoother storage and effective operations

and energy efficiency, expanding opportunities for specialized memory types, including MRAM and ReRAM.

Edge Computing & 5G/6G Networks

These memories are one of the most integral ingredients in edge computing and 5g network infrastructure to provide low latency, real-time network monitoring, and many more. In edge computing, memory helps to keep data close so that, in times of need, it can retrieve the data for low latency, and it reduces the need for dependency on distant cloud services. The official credentials project that 5G will account for more than 1.2 billion connections by 2025, covering almost 26% of global connections worldwide. This creates a staggering demand for advanced technologies like semiconductor memory. Thus, key players, including Micron Technology, planned to invest around 24 billion USD in a new memory chip fab in Singapore to boost global supply amid tight conditions.

What's the world doing – regulatory efforts

The governments all over the world are making efforts to expand their memory production to reduce supply chain vulnerabilities. Countries are strengthening their domestic manufacturing systems to limit reliance on others. Here are a few efforts taken by the governments of different countries.

- The U.S. allocated more than USD 52 billion in subsidies to revitalize its semiconductor industry in 2022 under the CHIPS and Science Act. This regulatory norm is made to support manufacturers in setting up U.S.-based foundries that are capable of manufacturing the next generation of chips.
- The EU also regulated the Chips Act in September 2023. Under this, more than €43 billion in public and private investments to strengthen the EU's semiconductor ecosystem and double up the production.
- China has also planned to provide subsidies of around USD 70 billion to reinforce its semiconductor industry. This plan is still in process in 2025, and if it's implemented, it is going to be one of the largest government efforts to support semiconductor production in the world.
- South Korea also unveiled a nearly USD 518 billion strategy to expand its semiconductor sector and challenge global leaders like the U.S. and Taiwan. These investments are supporting the expansion in the Asia Pacific region.

Final thought

The importance of semiconductor memory has spread across virtually every technology domain. As the world transitions towards an AI-driven economy, understanding the trajectory of semiconductor memory is not an IT concern anymore for business leaders across industries; it is the primary pillar for a lucrative future.

Source: https://www.researchnester.com/reports/semiconductor-memory-market/8301

Year	China	Japan	The U.S	South Korea	Germany
2021	Almost 268,195	Around 47,182	Nearly 40,373	Approximately 31,083	Around 25,636
2022	Nearly 290,258	Approximately 50,413	Roughly 39,576	Almost 31,000	Nearly 25,636
2023	More than 290,000	Over 4 4,500	Around 34,200	Roughly 30,600	Almost 26,982

➤ Country-wise Robot Installation (2021 – 2023)
Source: International Federation of Robotics (IFR)

HVAC for semiconductor back-end market to surpass $4.7 billion by 2033

According to **Research Intelo**, the Global HVAC for Semiconductor Back-End market size was valued at $2.1 billion in 2024 and is projected to reach $4.7 billion by 2033, expanding at a robust CAGR of 9.2% during the forecast period of 2025–2033.

THE PRIMARY driver fueling this impressive growth is the intensifying demand for advanced semiconductor manufacturing, which necessitates highly controlled environments to ensure yield, reliability, and quality. As semiconductor devices become more complex and miniaturized, the need for precision climate control in back-end processes such as assembly, packaging, and testing has become paramount, propelling the adoption of sophisticated HVAC systems across global semiconductor facilities.

The semiconductor industry operates at the forefront of technological precision, where even the slightest variations in temperature, humidity, and air purity can impact yield and performance. Within this ecosystem, Heating, Ventilation, and Air Conditioning (HVAC) systems play a pivotal role, particularly in the back-end semiconductor manufacturing process. This phase, which includes assembly, packaging, and testing, demands highly controlled environmental conditions to ensure product reliability. As semiconductor fabrication shifts toward higher complexity and smaller geometries, the HVAC for Semiconductor Back-End Market is experiencing accelerated growth, driven by cleanroom expansion, sustainability goals, and automation integration.

Key growth drivers

Rising demand for cleanroom expansion

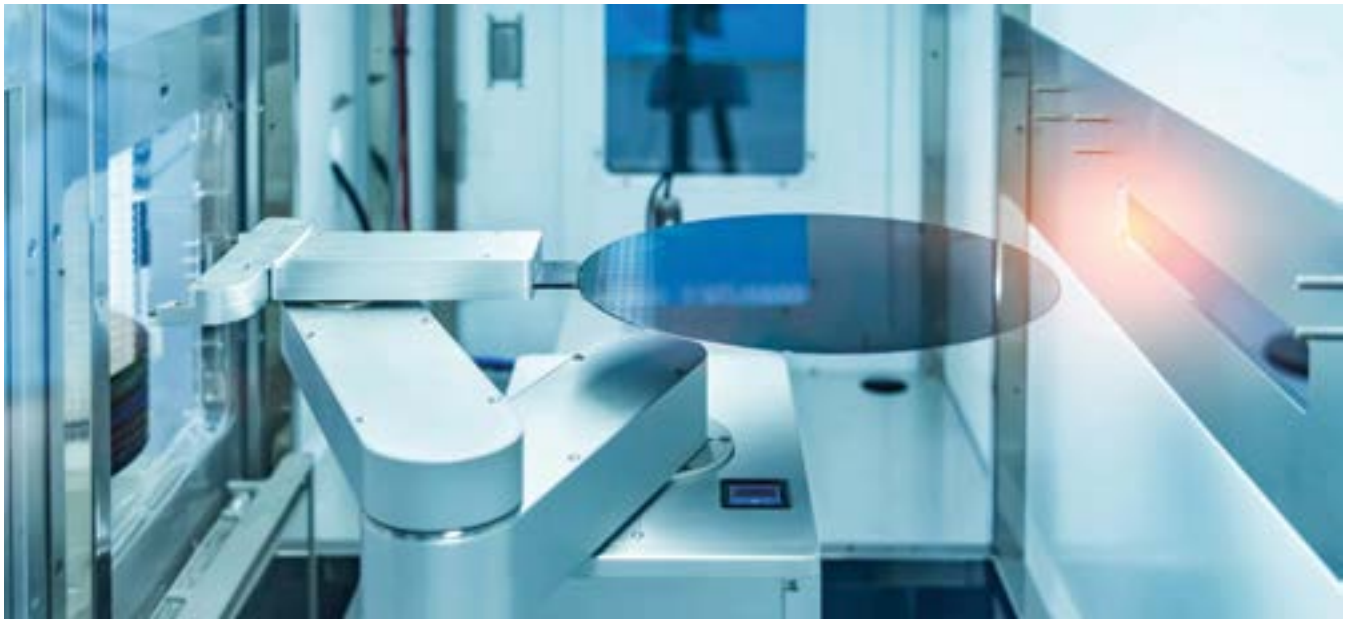
As the semiconductor industry witnesses massive investment in new packaging and testing facilities, the demand for cleanroom-based HVAC solutions has surged. The miniaturization of chips and advanced packaging technologies like 3D stacking, wafer-level packaging (WLP), and system-in-package (SiP) require contamination-free environments. HVAC systems are thus being customized to provide laminar airflow, HEPA filtration, and precise humidity control, ensuring consistent process outcomes.

Growth of advanced semiconductor packaging

The migration from traditional wire-bond to advanced packaging methods has created a need for high-precision HVAC systems capable of controlling micro-vibration, electrostatic discharge (ESD), and temperature gradients. Efficient HVAC management minimizes mechanical and thermal stress during die attach and bonding processes, improving yield rates and device reliability.

Sustainability and energy efficiency

Semiconductor facilities are among the most energy-intensive industrial environments. Consequently, manufacturers are prioritizing green HVAC technologies such as variable refrigerant flow (VRF) systems, heat



recovery ventilation (HRV), and smart airflow controls. These innovations reduce operational costs while supporting corporate carbon reduction goals. The adoption of AI-driven HVAC monitoring systems for predictive maintenance and energy optimization is becoming increasingly common.

Regional manufacturing expansion
The global realignment of semiconductor manufacturing especially with new fabs and packaging plants in Asia-Pacific, North America, and Europe is fueling market growth. Countries such as Taiwan, South Korea, Japan, China, and India are leading back-end assembly and testing operations, while the U.S. and EU are focusing on semiconductor supply chain localization, all of which require advanced HVAC infrastructure.

Technological advancements shaping the market

Smart HVAC Integration
Digital transformation is redefining HVAC performance in semiconductor facilities. The use of IoT sensors, real-time analytics, and machine learning algorithms allows dynamic control of air quality, temperature, and energy consumption. Smart HVAC systems can automatically adjust airflow patterns based on occupancy, production schedules, and real-time contamination levels.

HEPA and ULPA filtration enhancements
The evolution of High-Efficiency Particulate Air (HEPA) and Ultra-Low Penetration Air (ULPA) filters has significantly improved contamination control. These filtration systems are designed to capture even nanoscale particles, ensuring compliance with ISO cleanroom standards essential for packaging and testing environments.

Hybrid and modular HVAC units
Manufacturers are increasingly adopting modular HVAC systems that allow flexible scaling with production capacity. Hybrid models combining air-cooled and liquid-cooled units are gaining traction, offering improved temperature management for high-power testing equipment.

Humidity and ESD control
Maintaining relative humidity (RH) between 40%–60% is critical to prevent electrostatic discharge during chip packaging. Modern HVAC systems integrate electronic humidification controls and ESD-safe airflow systems to maintain the ideal environment, minimizing material damage and improving yield consistency.

Challenges in the HVAC for semiconductor back-end market

Despite rapid innovation, several challenges persist:

- **High Capital Expenditure:** The initial investment in cleanroom-grade HVAC infrastructure is substantial, especially for facilities requiring ISO 5 or cleaner classifications.
- **Complex Maintenance:** HVAC systems in semiconductor environments require continuous calibration, filter replacements, and cleanroom validation.
- **Energy Consumption:** Even with energy-efficient systems, the sheer operational scale of semiconductor plants leads to high energy demands, prompting the need for renewable integration.
- **Customization Requirements:** Each semiconductor facility has unique HVAC needs based on its layout, process sensitivity, and local climatic conditions, increasing system design complexity.

Future outlook: toward smart, sustainable HVAC solutions

The future of the HVAC for Semiconductor Back-End Market lies in convergence where sustainability, automation, and precision intersect. AI-optimized energy management, digital twins for HVAC modeling, and integration with building management systems (BMS) will define next-generation facilities. Furthermore, the push toward net-zero emissions will accelerate the development of low-carbon HVAC materials and refrigerants.

As semiconductor packaging technologies evolve and demand for high-performance chips rises, HVAC systems will continue to serve as the unsung enablers of yield consistency, product reliability, and manufacturing efficiency.

Source: https://researchintelo.com/report/hvac-for-semiconductor-back-end-market

PIC INTERNATIONAL CONFERENCE

ANGELTECH

20-22 APRIL 2026
BRUSSELS
BELGIUM

CONNECTING, EDUCATING & INSPIRING THE PIC INDUSTRY

The 11th PIC International builds on the strengths of its predecessors, with around 40 leaders from industry and academia delivering presentations falling within four key themes:

Those attending these sessions will gain greater insight into device technologies while learning of the latest opportunities and trends within the PIC industry. Delegates will also discover significant advances in tools and processes that deliver enhanced yield and throughput.

Attendees at this two-day conference will also meet a wide variety of key players within the community, from investors and analysts to fab engineers and managers.

PIC International is part of AngelTech, which delivers a portfolio of insightful, informative, highly valued chip-level conferences. Bringing together an Innovate Summit and four conferences with more than 120 presentations, more than 700 delegates and over 80 exhibitors,

AngelTech is the premier global event covering compound semiconductors, photonic integrated circuits, power electronic technologies and advanced packaging.

With a significant overlap between the four conferences, attendees and exhibitors are exposed to the full relevant supply chains and customer and supplier bases.

Key Themes for 2026

Foundations of PIC design: materials, devices and processes

While PICs are well established, they still face technological limitations. How can new materials and devices improve their performance and expand their range of functionalities, and how can we accelerate these innovations to market?

Connectivity and scalability for secure, high-speed data networks

Data communications networks face numerous challenges, including soaring AI-driven demands, high energy consumption, and the possibility of future quantum technologies breaking current encryption methods. How can PICs help to solve these issues and underpin the high-speed, energy-efficient, quantum-secure networks of the future?

Emerging applications: photonics for sensing, imaging and beyond

Integrated photonics has a wide range of potential applications. From self-driving cars to miniaturised molecular sensors and non-invasive healthcare, how are PICs making these possibilities a reality?

Future computing: PICs for photonic processing, quantum computers, and neural networks

Computing power is integral to the modern world, but established technologies have limits, and novel systems could herald more powerful devices. From fully photonic processing to photonics for neuromorphic and quantum computing, how are PICs transforming the way we process data?

ANGELTECH

CS INTERNATIONAL CONFERENCE | PIC INTERNATIONAL CONFERENCE | PE INTERNATIONAL CONFERENCE | AP INTERNATIONAL CONFERENCE | AIS ANGELTECH INNOVATE SUMMIT

SPECIAL Event Discount:

Register before 31 MARCH 2026

and get 10% OFF!

Registration to AngelTech allows you to access both days of **PIC International**, **CS International, Advanced Packaging** and **PE International.**

EVENT SPONSORS

PLATINUM SPONSORS

AIXEMTEC, Ansys part of Synopsys, APEX, Argotech, BÜHLER, cadence, CRAFT, ADCA, EVG, FEMTUM, ficontec, imec, LIGENTEC, LIGHTIUM, LUCEDA PHOTONICS, nanoscribe, PhotonDelta, PI, PIC advanced, QCI, scia systems, SHINCRON, vanguard AUTOMATION MYCRONIC, VIAVI, VPIphotonics, YOLE Group

GOLD SPONSORS

ASMPT, CPFC, eblanaphotonics, ephos, EPIC, Fraunhofer Heinrich Hertz Institute, helbling, HYBPIC, ISP SYSTEM, KRELLTECH, NAMICS, OPTICA, phix, PIX Europe, set, SIEMENS, SMART PHOTONICS, yelo

SUPPORTING PARTNER

LIGHTWAVELOGIC

STARTUP

OPHOX

SUPPORTING PARTNER

NOKIA

MEDIA PARTNERS

electronic specifier, Electro Optics, electropages, Microwave Journal, PHOTONICS spectra, PHOTONIC INTEGRATED CIRCUITS, POWER ELECTRONICS INTERNATIONAL, Semiconductor Review, SLJ

ORGANISERS

Angel BUSINESS COMMUNICATIONS

ANGEL EVENTS

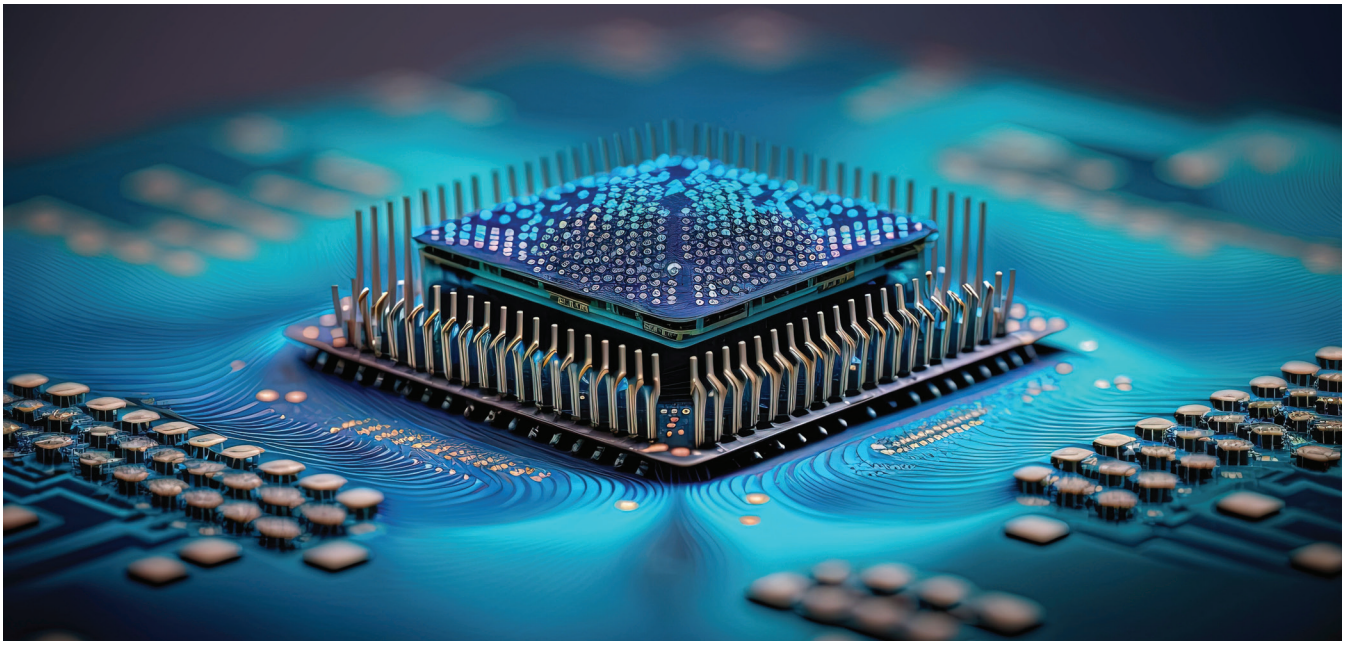
To find out more about our sponsor and speaker opportunities, contact us today on:

+44 (0) 2476 718970
info@picinternational.net
picinternational.net

ORGANISED BY

Angel BUSINESS COMMUNICATIONS

ANGEL EVENTS



TDLAS vs CRDS: Which gas analysis technology truly performs in the fab?

When even parts per trillion (ppt) moisture can cause serious defects and delays, fabs must keep conditions pristine and gas quality optimized.

BY JOSEPH HA, MARKET SEGMENT MANAGER, P&S AT SERVOMEX

ENGINEERS rely on gas-analysis tools to verify purity and catch issues early. Two leading options are Tunable Diode Laser Absorption Spectroscopy (TDLAS) and Cavity Ring-Down Spectroscopy (CRDS). But how do they measure up?

TDLAS tunes a laser to specific infrared wavelengths and reads the absorbed light fingerprint of target gas molecules. It then calculates concentration from that absorption signal, using separate temperature and pressure readings for the gas to ensure accuracy. This approach delivers real-time, in-situ, ultra-trace measurements in critical Ultra High Purity (UHP) applications, allowing for better control of manufacturing processes.

CRDS uses a different readout. It traps light between high-reflectivity mirrors and measures how quickly the signal decays. This effectively correlates signal deterioration, or the “ring-down” time constant with the concentration.

When considering the right gas analysis for your semiconductor fabrication, it’s crucial to assess how each tool characterizes process gas composition and quality at every critical point. The most accurate analysis optimizes fabrication and helps teams resolve contamination threats with minimum disruption.

Purity under pressure

A semiconductor fabrication plant uses many types of gases, serving various, and specific functions. So, the right analyzer must be able to handle specialty gases, as well as atmospherics – oxygen, hydrogen, nitrogen, argon, and helium – to purge systems and reduce contamination. All gases must be extremely high purity at source, and plants must keep this quality constant across the entire distribution system.

Engineers first analyze gas bulk delivery before it’s pumped into the piping network. They test it again at the purification skids before the gas reaches the cleanroom. Technicians verify purity at the distribution manifold before the gas is flowed into the internal stainless-steel pipelines. They run further checks on the glass cabinets at each process tool where specialty gas enters the line, and again at point of use (POU).

It’s no surprise that reliability is a non-negotiable expectation in high-precision environments. Even sub-parts-per-billion (ppb) contamination can irreversibly damage wafers, reduce yield, or trigger a total fabrication shutdown. As production shrinks ever closer to the 1.4nm node, fabs tolerate virtually no impurities, which makes gas analysis even more integral for performance and profitability.

TDLAS and CRDS are both proven technologies. They deliver accurate, non-destructive measurements and work without consumables. TDLAS uses advanced, laser-based optical components for robustness, providing ultra-trace moisture, fast response, and in-situ monitoring that is ideal for high-purity gases for semiconductor processes. CRDS, on the other hand, is best suited for applications where trace impurity in gases is non-negotiable, and rapid measurements not so critical.

Speed that safeguards production

The complete fabrication of a semiconductor device takes 12-16 weeks on average, but gas analysis can't sit idle when protecting them. Sensitive processes and expensive materials demand fast interception of trace contaminants. Early detection prevents process yield loss and equipment damage and ensures safety. Analysis tools must find leaks and contamination within seconds to protect wafers, workers, and production. This means they must reach sub-ppb final readings with utmost urgency.

TDLAS and CRDS both use optical spectroscopy technology and offer rapid, ultra-trace analysis for high-purity and electronic specialty gases. They deliver real-time, non-contact measurements and outperform traditional gas chromatography in speed and specificity. Both rely on highly selective laser absorption, which reduces cross-interference and false positives in complex gas mixtures. TDLAS achieves the fastest response time to gas concentrations. It uses wavelength modulation spectroscopy (WMS) with a tunable laser diode to pair high sensitivity with high-speed scanning. Its sub-second scan rate supports ultrafast and ultra-trace monitoring (ppt levels) with real-time diagnostics.

CRDS enables ultra-trace monitoring. Despite its slower response, it still delivers near real-time monitoring of moisture impurities in ultra-high purity (UHP). TDLAS is the better choice for high-speed, process-ready monitoring where ppb- or ppt-level changes matter, delivering rapid ultra-trace impurity measurements. CRDS is suited for trace impurity analysis that does not require the fastest response or the best accuracy.

Neither technology needs to 'wet-up' or 'dry-down', which is to say adsorb and then desorb a test sample to reach baseline, which slows surface-based sensors. Both TDLAS and CRDS simply shoot a laser through a sample cell, for rapid, non-invasive results.

Maintenance that won't slow you down

This trouble-free approach is crucial when working with semiconductors, where uptime, yield, and contamination control make a difference to throughput with already tight margins.

Both TDLAS and CRDS deliver high-performance gas sensing using highly specific optical techniques. However, their maintenance needs differ. TDLAS generally requires less maintenance, operating for months or even years without calibration. These systems are based on fundamental principles of gas, allowing operation over extended periods of time with no impact due to laser drift, detector drift, or mirror reflectivity. The technology also requires minimal-to-no gas conditioning.

CRDS, on the other hand, need more delicate handling. Operators must perform more frequent zeroing to compensate for background drifts. And the mirrors must stay clean to achieve long optical path lengths and preserve high-sensitivity performance.

Another key difference lies in their measurement principles. These are fundamental to whether the instruments can meet strict semiconductor specifications and prevent costly failure. They will literally make or break the viability of a chip.

TDLAS use direct absorption – the system passes a laser through the gas and measures drop in light intensity. CRDS measures the decay rate constant of light trapped between two mirrors. Both provide incredible accuracy, but again, the application determines the better fit. CRDS can provide purity verification, but its slower response time, higher cost, and sensitivity to mechanical vibration and environmental changes make it less suited to critical semiconductor settings. TDLAS offers greater robustness, superior speeds, and strong inline process-control monitoring, especially in production phases where ultra-high sensitivity measurements are needed. TDLAS is often dubbed a workhorse. In contrast, CRDS requires a more complex, laboratory-grade setup and more complex data processing. Both stay highly stable compared to older gas-analysis techniques, but the specific needs of a fabrication plant will ultimately decide which technology is the best match.

The definitive challenge of contamination

Contamination is the point at which the unique qualities of TDLAS and CRDS technologies diverge. Their optical designs make contamination susceptibility quite different. As already stated, TDLAS is more robust, extremely sensitive, and suitable for a variety of environments, while CRDS needs stricter environmental control or frequent adjustments or alignment.

With TDLAS almost immune to contamination, it's no surprise response times are also superior. This makes TDLAS favorable for real-time, process control, with rapid start-up/warm-up meaning it's ready to measure within minutes of activation. It's adaptable and versatile, well suited for in-situ and online. And it handles dynamic concentration changes faster, making it ideal for process monitoring.

As we've seen, CRDS is best suited for analytical applications where longer averaging times are more acceptable. Its "ring down" technique combined with heavy signal filtering often means response time is slower than TDLAS, and the complex system can increase set-up and calibration.

When sensitivity meets reality

Noise affects each gas analysis technology differently. CRDS excels in laboratory settings due to the need for extremely stable, low-vibration environments, while TDLAS is the ruggedized choice for in-situ industrial and semiconductor process control. Earlier generations of laser spectroscopy faced challenges when optical interference fringes overlapped with target absorption signals. But modern TDLAS, using advanced WMS and second harmonic (2f) detection, effectively cuts interference to achieve ppt-level detection.

For CRDS to perform at peak efficiency, it needs more maintenance and isolation. Beyond the noise challenges of the industrial environment, precision is compromised by mirror contamination, and response times suffer when vibrations and temperature changes disrupt the high-finesse optical cavity. TDLAS, on the other hand, provides non-contact, real-time measurements in high-temperature, corrosive, and dust-laden settings.

CRDS effect versus TDLAS advantage

Low detection is still critical for chip fabrication. Even trace-level impurities can destroy silicon wafers, reduce yield, cause safety risks, and compromise performance. Semiconductor processes run at such tight purity margins that microscopic deviations can bring catastrophic defects.

Both gas analysis solutions bring the precision and productivity

semiconductor production demands. However, TDLAS offers clear operational advantages in demanding environments. This gives it the edge over CRDS in day-to-day use. It is simpler, ultra-sensitive, and more robust. It's also less expensive to build, maintain, and scale. TDLAS responds more rapidly to leak detection – even at ppt-level changes – and integrates easily with existing fab infrastructure. Its sensitivity is ideal for real-world process requirements, where any sharper detail would add unwanted complexity.

The Servomex DF-700 series is a TDLAS solution that incorporates this advantage. These analyzers combine TDLAS practicality with semiconductor-grade performance. They deliver stable, repeatable, industry-leading lower detection limits for moisture impurities. This makes them effective for quality control of gases, and gas-cabinet leak detection. In an industry where uptime is everything, the DF-700 series uses solid-state storage, doesn't need consumables, and stays calibrated, with excellent baseline stability. Their fast response empowers real-time detection of impurities and leaks – crucial for protecting chambers and wafer yield. This is why UHP gas producers worldwide trust this analyzer platform.

As we've explored, the latest generation of gas analyzers challenge long-held misconceptions about their role in chip fabrication. With 1.4mn assembly fast approaching and tolerances tightening, fabs must weigh their priorities carefully.

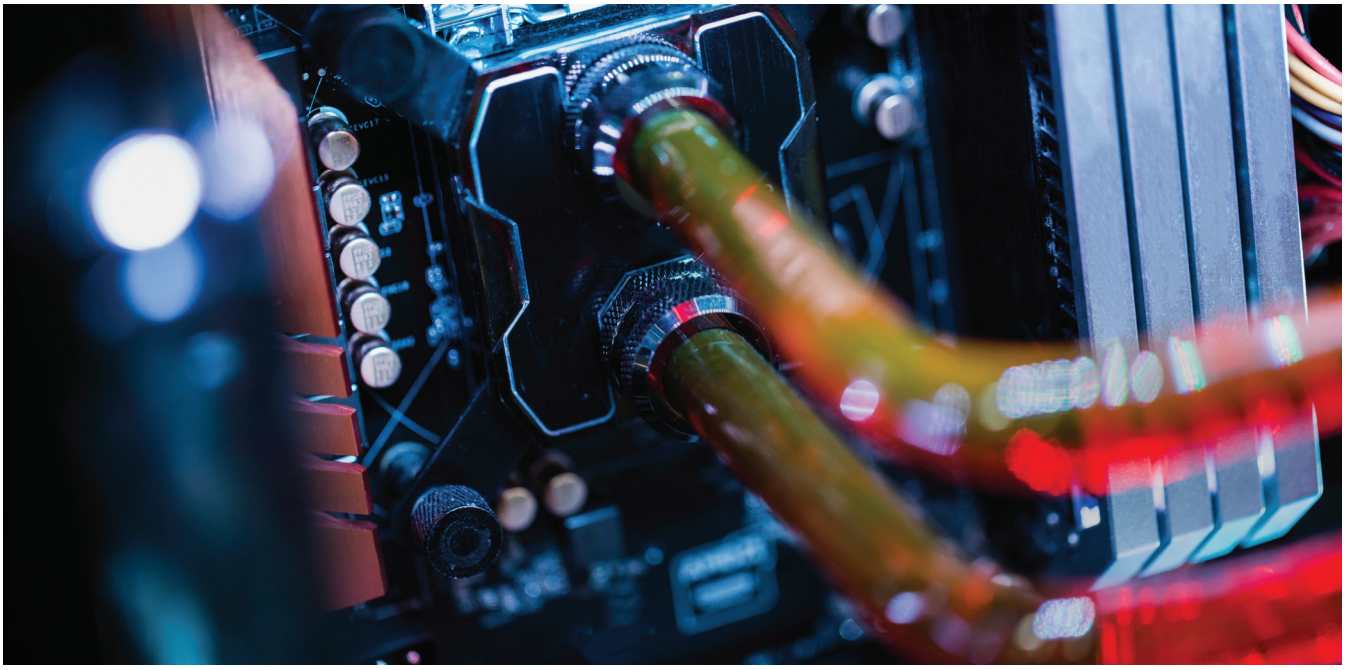
What is clear is that modern gas analysis technology equips semiconductor manufacturers to meet ever-increasing precision demands, ready to rise to the next generation of challenges.

EDWARDS

[enabling environments where innovation thrives]

Ganymede

Performance without compromise



Liquid cooling option STR provides SLT and BI solution for HPC, AI and automotive devices

Davette Berry, sr. director of business development for Advantest, discusses the expansion of the company's 7038 System-Level Test Platform, with right-sized single test rack solution for high volume manufacturing. The new liquid-cooling enabled system delivers affordable, high-density SLT and burn-in test for high-demand, lower-volume HPC, AI, and automotive devices. Davette also looks forward to Advantest's presence at SEMICON West and also shares some insights as to what will be keeping the company busy over the coming months.

IN THE relentless push toward higher computational performance, semiconductor testing has become as much about managing heat, data, and design complexity as it is about validating functionality. As processors and system-on-chips (SoCs) become denser and more heterogeneous, traditional testing methodologies face new limits. Advantest's latest evolution of its system-level test (SLT) platform - the **TAS 7038 Single Test Rack (STR)** - is a direct response to those limits, providing a compact, thermally advanced, and fully integrated solution designed to meet the changing demands of AI, automotive, and high-performance computing (HPC) devices.

Announced earlier this year, the 7038 STR extends the established 7038 family of SLT systems with a right-sized, liquid-cooled configuration that bridges the gap between engineering development and mid-volume production. In doing so, Advantest is addressing a crucial segment of the market - where unit volumes may not rival mobile processors, but performance and power density are increasing exponentially.

Evolving the system-level test platform

The 7038 platform has long served as the cornerstone of Advantest's SLT offering. It combines mechanical handling, electrical interface, and thermal management in a single integrated system. The newest addition - the single test rack variant - derives from the dual-rack architecture that underpins Advantest's high-volume production systems but reimagines it for customers whose production scales are smaller and whose devices push the limits of power and thermal design.

"The platform integrates a chip handler, an elevator, and a multi-slot rack," explains Davette Berry. "Each slot is a standalone system-level tester. The single test rack version is effectively a smaller derivative of our dual-rack system, with one elevator instead of two. It's the same DNA - just in a more compact footprint."

That smaller footprint carries significant implications. By maintaining full compatibility with the larger 7038 systems while streamlining size and complexity, Advantest enables customers to align their test infrastructure with evolving production needs. Automotive and computing customers, for instance, may run tens or hundreds of thousands of units per month—volumes that don't justify the

highest-throughput configurations used in smartphone SoC production, but which demand the same precision and environmental control.

Liquid cooling: meeting the thermal challenge

While the physical configuration may have shrunk, the power profiles of devices under test have not. If anything, they've grown dramatically. The increasing computational density of AI and HPC processors, combined with advanced packaging techniques such as 2.5D and 3D integration, is concentrating heat generation into smaller areas of silicon. Traditional air cooling, long the mainstay of test and validation environments, is fast becoming inadequate.

"The biggest addition is the combination of air and liquid cooling," says Davette. "Liquid cooling existed in our larger footprint systems, but the 7038 STR now integrates it directly into a smaller test rack. In system-level testing, devices are exercised to their extremes - they're running full workloads, and they get hot. The liquid cooling integration allows active thermal control so the logic can get hot enough to operate properly, but not overheat."

The comparison to data centres is apt. Just as hyperscale servers have shifted to direct-to-chip liquid cooling to manage soaring thermal loads, test systems are now following suit. The physics are the same: higher power density, unevenly distributed hotspots, and rising ambient temperatures make precision thermal management indispensable.

"Data centres and automotive processors have already moved beyond pure air circulation," Advantest's expert notes. "In test mode, the stress on the device is even greater. We're replicating real-world workloads, often pushing chips beyond nominal operating conditions to ensure reliability. That's why liquid cooling isn't just a luxury—it's a requirement."

The result is a system that can support significantly higher power envelopes, opening the door to testing the latest generation of AI accelerators, automotive compute platforms, and edge processors without throttling or compromising throughput.

"The biggest addition is the combination of air and liquid cooling," says Davette. "Liquid cooling existed in our larger footprint systems, but the 7038 STR now integrates it directly into a smaller test rack.

A turnkey, single-vendor solution

Beyond thermal engineering, the 7038 STR embodies a holistic approach to automation and integration. In a production environment, efficiency hinges on more than just throughput; it depends on the seamless interaction of mechanical, electrical, and software subsystems. That's where Advantest's "single-vendor turnkey solution" comes into play.

"System-level testing is inherently complex," Davette Berry explains. "You're loading a chip onto an application board, running native software, and validating real-world functionality. But to achieve high utilisation and throughput, you need to optimise across multiple engineering disciplines simultaneously - electrical integrity, mechanical stability, thermal dissipation, and factory automation."

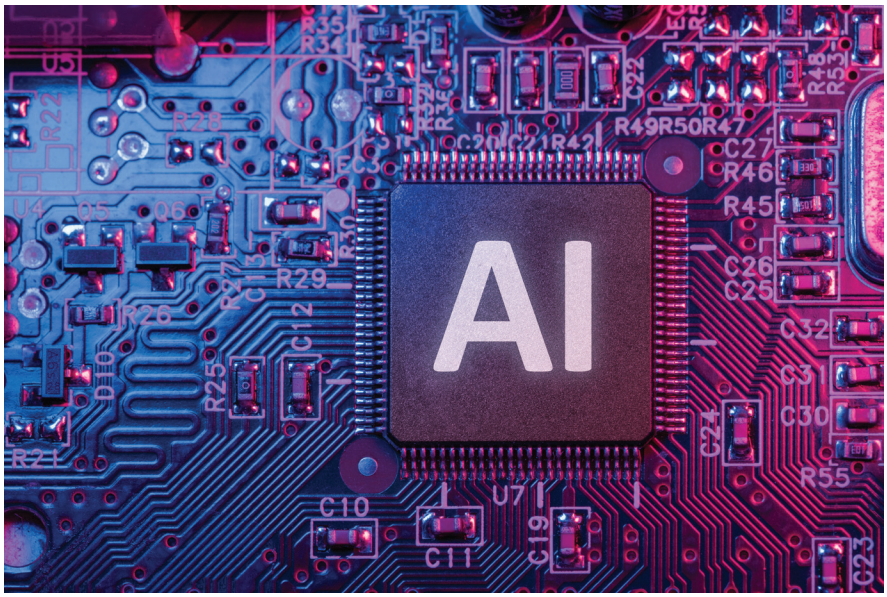
By consolidating these competencies within a single platform, Advantest relieves customers of the burden of system integration. The turnkey approach means that the handler, tester, software, and support infrastructure all originate from one source - and, crucially, are designed to work together from the outset. This reduces both the time and risk associated with deployment while ensuring consistent data integrity and tool uptime across production sites.

"That's what makes these systems financially achievable and operationally efficient," Davette says. "It's about aligning the test floor ecosystem - hardware, software, data, and service - into a coherent whole."

Optimised for the mid-volume market

Historically, Advantest's system-level test expertise has been most visible in ultra-high-volume environments such as mobile applications processors. Those systems, produced in the hundreds of millions, demanded the dual-rack, high-parallelism version of the 7038 platform. However, as new segments - particularly automotive and HPC - rise in prominence, a different set of constraints and requirements has emerged.

"Automotive and high-performance compute devices are much more complex," Davette notes. "They're thermally demanding, they draw more power, and the units shipped per month are lower. The single test rack is right-sized for that market - perfect for tens



or hundreds of thousands of devices per month, not hundreds of millions."

This right-sizing doesn't mean compromising capability. The STR retains full compatibility with the broader 7038 family, ensuring that hardware, software, and thermal infrastructure can be interchanged across configurations. The modular architecture means that as a customer's production scales, their test investment remains protected.

"The beauty of the 7038 architecture," Davette explains, "is that every slot in the system is a standalone tester, and the components are interchangeable between the engineering station, single test rack, and dual test rack. Electrically, thermally, and from a software perspective, they're identical - the difference is automation level. So if a customer's volume grows, they can migrate the same test content to a dual test rack for higher parallelism, or back to a single rack for pilot runs or engineering."

This modularity reflects a central principle of Advantest's platform design: **scalability without reinvention**. Customers can start small, iterate, and expand seamlessly, all within a unified ecosystem.

Activate 360: software for a data-driven test future

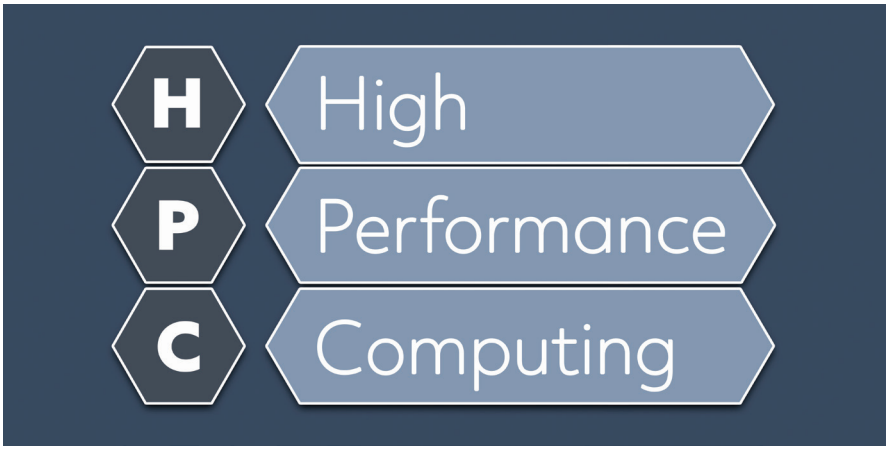
Hardware is only half the equation. As test environments become more integrated into digital manufacturing ecosystems, software increasingly determines how effectively those systems perform. Advantest's new **Activate 360** software suite represents a complete rethinking of the company's test management stack, extending three decades of Activate software heritage into a modern, AI-ready architecture.

"Activate 360 includes four major components," Davette explains. "Facility 360 manages communication with the factory network, exchanging data about tester status and performance. Cell 360 handles the pass/fail binning and recipe coordination between the tester and the handler. Studio 360 is our integrated development environment for test program generation. And the newest piece - Device 360 - serves as the software interface between the customer's device and our test environment."

Device 360, in particular, reflects the increasing diversity of devices being tested. System-level testing of a smartphone SoC bears little resemblance to that of an AI accelerator or an automotive compute platform. Each device brings unique firmware, power profiles, and functional modes. Device 360 abstracts this variability, allowing customers to run their native application suites within the Advantest framework.

"In system-level testing, every customer's device behaves differently," says Davette. "Device 360 allows them to bring their own software environment while we manage the reliability, throughput, and data integrity that production demands."

The broader Activate 360 environment also lays the groundwork for a future where test data becomes an active asset. As part of Advantest's ongoing push toward cloud integration and analytics-driven optimisation, the suite is designed to facilitate real-time data exchange between test floors and higher-level enterprise systems.



From test to insight: AI and the cloud

As the semiconductor industry races to design and produce chips that enable artificial intelligence, it is also turning to AI to improve its own processes. At last year's Semicon West, Advantest showcased precisely that duality: using AI-powered analytics to enhance test efficiency and yield, even as it tests AI processors themselves.

"The data generated by our testers and handlers is extremely valuable," Davette explains. "With the right infrastructure, that data can be used to accelerate time-to-market, improve yields, and optimise test costs. We're highlighting our cloud-based data solutions that enable real-time data flow from the tester into analytic environments."

By enabling actionable insights - such as predictive maintenance, adaptive test optimisation, and yield learning - Advantest's data infrastructure closes the loop between design, test, and production. Machine learning algorithms can identify patterns in device behaviour, suggest process adjustments, and continuously improve both throughput and test coverage.

In parallel, the company's Silicon Validation Group demonstrated **Psychonic**, a toolset aimed at accelerating the transition from first silicon to high-volume ramp. The collaboration between this group and the SLT division ensures test pattern portability between silicon validation and production environments - a critical capability for today's complex, multi-die devices.

"Advantest is uniquely positioned across the entire test lifecycle," Davette says. "From design validation through system-level testing to production optimisation, we're making sure that data, test content, and infrastructure remain actionable and interoperable."

Looking ahead: co-packaged optics and the next frontier

As semiconductor architectures continue to evolve, Advantest sees a new class of challenges on the horizon - particularly around **co-packaged optics (CPO)** and **silicon photonics**. These technologies promise to overcome electrical interconnect bottlenecks by bringing optical communication directly into the package, dramatically

increasing bandwidth while reducing power consumption. However, they also introduce an entirely new dimension of test complexity.

“In order to keep up with Moore’s Law, data transfer to computational engines will increasingly move through light rather than electrical pathways,” Davette notes. “Incorporating optical interfaces into the package changes everything. You now have to manage the mechanical alignment of optical engines, deal with nonlinearities in light transmission as the device heats up, and integrate that into high-uptime, turnkey test solutions.”

For test engineers, this means mastering a convergence of mechanical precision, optical alignment, and thermal control that far exceeds anything seen in traditional electrical test environments. Advantest’s long-standing emphasis on multi-disciplinary integration - combining thermal, electrical, and mechanical expertise - positions it well to take on this challenge.

But before co-packaged optics reach production-scale volumes, there are more immediate concerns to tackle. Devices are growing larger, heavier, and hotter, challenging the robotics and JEDEC transport mechanisms that move parts through the back-end flow. The next generation of SLT equipment will need to accommodate these physical and thermal realities while continuing to deliver higher power and improved cooling.

“In the near term,” says Davette, “we’re focused on supporting larger, higher-power devices and improving the robotics that handle them. That’s happening now. Longer-term, co-packaged optics will drive the next wave of test innovation.”

The road ahead

From its origins in mobile SoC testing to its expanding role in automotive and AI device qualification, Advantest’s 7038 platform embodies the evolution of system-level test from a niche capability into a cornerstone of semiconductor manufacturing. The introduction of the 7038 STR extends that evolution, offering a flexible, thermally robust platform that meets the needs of a rapidly diversifying market.

Whether it’s liquid-cooled thermal management, modular scalability, or data-driven software integration, the STR represents more than an incremental update - it’s a statement of direction. In an era defined by AI, heterogeneous integration, and exponential data generation, system-level test is no longer an afterthought; it’s an enabler of performance, reliability, and time-to-market.

As Advantest prepares for the next wave - co-packaged optics, photonics, and beyond - it is clear that the company views system-level testing not just as a validation step, but as a strategic pillar in the semiconductor lifecycle. In doing so, it continues to bridge the gap between silicon and systems, between test data and actionable insight, and between today’s challenges and tomorrow’s possibilities.

The 10 most common mistakes when using turbomolecular vacuum pumps and how to avoid them

Turbomolecular vacuum pumps, also known as turbopumps, are at the heart of many high-tech processes – from semiconductor manufacturing to research laboratories. Yet even small mistakes in their setup or operation can lead to costly downtime, equipment damage, or complete vacuum pump failure. In this article, Busch Vacuum Solutions discusses the ten most common pitfalls and how to overcome them.

Incorrect dimensioning of high-vacuum lines

HIGH VACUUM lines and valves should be designed in accordance with the nominal pumping speed of the high vacuum pump. Otherwise, there will be considerable losses in the effective pumping speed due to unfavorable conductivity.

To illustrate the effect that an incorrectly designed high vacuum line can have, here is an example using a turbopump with a nominal pumping speed of 260 l/s, air as the pumped medium, and a vacuum line with a length of 250 mm:

If a vacuum line much smaller than the flange diameter of the turbopump (DN 100 (100 mm)) is used, the effective pumping speed will decrease. A DN 25 (25 mm) vacuum line will result in only around 7.4 l/s at the end of the line.

By using the same diameter as the turbopump, the effective pumping speed will increase to 170 l/s.

Even a turbopump with a flange size of DN 320 (320 mm) and a nominal pumping speed of 3200 l/s would only offer approximately 7.6 l/s at the end of a DN 25 size vacuum line. This means that this turbomolecular vacuum pump, which is twelve times bigger than the vacuum pump in the first example in terms of nominal pumping speed, actually delivers virtually no additional benefit.

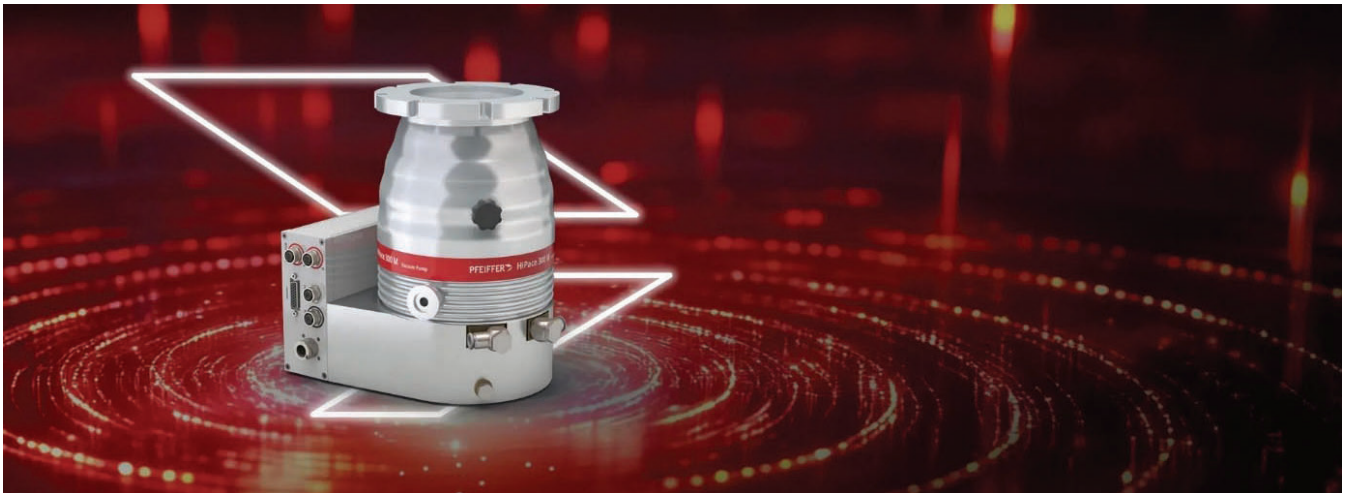
Rigid vacuum connections

Most applications require a rigid connection between the high vacuum flange of the turbopump and the chamber for safe, sustainable installation. However, in such cases, it is important to leave the forevacuum line connection or the lower end of the turbopump flexible. A rigid connection means that the vacuum pump housing cannot expand when exposed to heat. This will cause material stress, building up to impermissible levels that can eventually cause stress failures.

A rigid mounting method has further disadvantages: The rotor cannot oscillate freely and the existing minimum residual imbalance can lead to possible bearing failure and rotor damage over time.

Uncontrolled vibration from resonant frequencies

Turbomolecular vacuum pumps are balanced to ensure low vibration operation and optimal bearing life. During normal run-up, however, all turbopumps move through certain resonant frequencies. If these



➤ HiPace 300 M Vacuum Pump
Image source: Pfeiffer Vacuum & Fab Solutions

frequencies reach the resonant frequency of the vacuum chamber or the entire system, their amplitude increases significantly. This naturally occurring phenomenon causes the vacuum pump to vibrate and generate higher-than-usual sound levels. Although this effect in itself is normal and not the result of any problem with the turbopump, it is best to avoid the frequencies that trigger it to stop any damage from vibrations occurring. It is therefore advisable to determine the eigenfrequency of the system and discuss these values with the vacuum pump manufacturer to see how vibration can be avoided. This could be by means of reinforcements, such as vibration-damping mounts or pads between the vacuum pump and vacuum chamber, additional weights, changing the nominal speed of the turbopump, or design modifications.

Inadequate connections between inlet flange and vacuum chamber

Turbopumps store an enormous amount of mechanical energy, comparable to the energy of a turbopump free-falling from 300 m. In the event of a rotor crash, this energy is released in a matter of milliseconds and generates significant torque. Improper vacuum chamber design or incorrect attachment of the turbopump can result in deformation of the chamber and, in the worst case, twisting or even tearing of the turbopump from the flange.

Tests by turbopump manufacturers have revealed that the flange connection should ideally be designed in ISO-F. The turbopump is prevented from rotating in an ISO-F flange by its slotted holes and, for ISO-CF, by the fixing screw holes. Manufacturers offer mounting kits, which contain the appropriate number of clamps or fixing screws in the required material quality, as well as suitable centering rings. This is the only way to ensure that the connection remains intact and leak-tight in the event of a crash. The torque values can be found in the instruction manual for the turbopump and must be strictly observed.

Inadequate protection against foreign objects

Foreign objects falling into the turbopump rotor can cause irreparable damage. To prevent this, it is recommended to fit a splinter shield or protective screen in the inlet flange of the turbopump. While this will protect the vacuum pump from debris, it has the side effect of conductance loss. This causes the pumping speed to be reduced – by up to 30% depending on the gas type. Another solution is, if possible, to position the turbopump upside down on the chamber, as foreign objects will fall due to gravity. However, care must be taken to ensure that the vacuum pump is suitable for upside-down operation. If this type of installation is not possible, the vacuum pump can be mounted on a t-piece at an angle of 90° to the side. The backing port should face downwards.

Vacuum pump bake-out at excessive temperatures

In some applications, the system and turbopump must be conditioned to achieve optimal process parameters, including improved repeatability, reduced residual gas load, and higher vacuum pump efficiency. One means of conditioning is baking out. When baking out the turbopump, it is important to observe the maximum inlet flange temperatures that are specified by the manufacturer. These typically lie between 100 and 120 °C. Exceeding the permitted temperature will cause the vacuum pump to overheat and may result in damage to bearings or rotors. During bake-out, water cooling is mandatory. The bake-out period should be at least 6 hours.

Exceeding maximum permitted backing pressure

Turbopumps that have additional high compression stages alongside the turbo stages can handle backing pressures of over 30 hPa (mbar). However, pure turbo-stage vacuum pumps with just one turbomolecular compression stage can typically only tolerate 2-3 hPa (mbar). The limits differ according to the pumped medium. Exceeding these can overheat the rotor and the entire turbopump, leading to damage or even total failure due to excessive gas friction and insufficient heat dissipation.

A turbopump cannot operate against atmospheric pressure and therefore is always operated in combination with a backing pump at its exhaust. This vacuum pump – commonly a rotary vane vacuum pump or a dry vacuum pump – reduces the backing pressure from atmospheric to rough or medium vacuum. If this backing pump malfunctions and is not equipped with a high vacuum safety valve, the turbopump will back vent through the exhaust line. This can lead to contamination of the turbopump and attached system caused by oil particles from the backing pump. In addition, it can exert mechanical stress on the fast-spinning rotor. If a larger vacuum chamber is attached to the turbopump, air inrush through the exhaust line can cause the rotor to lift – a phenomenon called the “helicopter effect – and trigger a rotor crash. To prevent this, manufacturers offer safety valves, either integrated into the respective backing pumps or as separate solutions that isolate the turbopump and the chamber should a fault happen with the backing pump. These valves close within milliseconds in the event of failure and can be triggered by a pressure sensor or a vacuum pump failure signal.

Foreign objects falling into the turbopump rotor can cause irreparable damage. To prevent this, it is recommended to fit a splinter shield or protective screen in the inlet flange of the turbopump

Not, or incorrectly, venting the vacuum pump and system

Turbopumps generate very clean, hydrocarbon-free vacuum due to their superior compression and unique design properties. However, after shutdown of the turbopump or entire vacuum system, pressure equalization from the backing side to the high vacuum side can cause contaminants and oil particles to migrate back into the turbopump if precautions are not taken. If no valve or gate is installed on the high vacuum side, this contamination will continue into the equipment. One way to prevent this is by venting the turbopump with dry gas, such as nitrogen or oil-free air, creating a positive pressure gradient from the high vacuum side toward the backing side. This controlled gradient prevents contaminants from being

pulled upstream during pressure equalization and also dilutes any residual vapors, reducing their partial pressures so they cannot migrate into the turbopump.

To further reduce the risk of contamination or even potential damage, a high vacuum safety valve to the backing pump is required to prevent air inrushes from the exhaust when the backing pump is stopped, as referenced in point 7. The drive electronics of the turbopump offer intelligent modes for safe venting at a particular speed in combination with the appropriate venting valve. Since the compression ratio of a turbopump also depends on the speed, the optimal moment to start venting is when the speed of the turbopump has dropped to approximately 50% of the nominal value. In unstable networks with frequent power failures, it is recommended to use what is known as a power failure venting valve, which automatically vents the vacuum pump and stops it properly in the event of a power failure.

Inadequate protection from magnetic fields, radiation and excessive heat sources

Magnetic fields generate eddy currents in the rotor of a running turbopump that work against its rotation. The energy this effect requires causes the motor to draw more current from its electrical connection.

This can cause the rotor to overheat rapidly. The maximum permissible magnetic fields for the vacuum pump are specified in the instruction manuals in millitesla (mT). If these values are exceeded, the vacuum pump must be shielded with appropriate covers or, if the distribution of the magnetic field is known, arranged differently.

Neutron and gamma radiation of varying intensity and duration occur in particle accelerators. This radiation destroys power transistors, diodes, and electronic components which are typically essential elements of the drive electronics. To avoid this, the electronic components need to be removed from the affected area, requiring remote drive electronics to be installed at a safe distance from the radiation via a connecting cable.

Under vacuum conditions, heat is transferred predominantly via heat radiation. In cases where the application requires hot or very hot surfaces, such as in certain coating processes for wear protection, the rotor of the turbopump needs visual protection from these hot surfaces, such as a protective screen. Otherwise, this induced heat will not be sufficiently dissipated and can cause the rotor to overheat. Proper shielding is therefore required, as this can cause severe damage.

Failure to take precautions for the process

It is essential to select a turbopump suitable for the process and ensure it is properly prepared. For example, for corrosive processes – especially in the semiconductor industry – there are several precautions that should be taken to protect the turbopump.

EVG®

invent
innovate
implement

www.EVGroup.com

FUSION AND HYBRID BONDING FOR HETEROGENEOUS INTEGRATION

- Enabling advanced 3D device stacking and chiplet integration for CMOS image sensors, memory and 3D system-on-chip (SoC)
- High-volume production equipment and process technology for Wafer-to-Wafer (W2W) and Die-to-Wafer (D2W) hybrid bonding
- GEMINI® FB Automated Production Wafer Bonding System delivers industry leading alignment accuracy and bonding performance
- Heterogeneous Integration Competence Center™ serving as leading-edge innovation incubator for EVG customers and partners

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

AI and the future of semiconductor design

SiS talks to Lorenzo Servadei, Head of AI for Chip Design, Sony AI.

SIS: *How do you see AI-powered EDA redefining the chip design process from initial concept through to fabrication — compared to traditional approaches?*

LS: AI-powered EDA has the potential to augment the entire design and manufacturing flow. Take, for instance, the capability to fully connect requirements, design, and fabrication stages using cross-functional data. In this case, the conventional waterfall paradigm is substituted by a comprehensive data infrastructure.

This methodology can give engineers an understanding of what is going to happen in later stages, identify bottlenecks in the design stages, and accelerate the chip design process. Additionally, AI-powered EDA has the potential to assist in evaluating complex trade-offs, learning complex surrogates that can encompass multi-physics effects, and predicting the best design parameter choices.

SIS: *In your view, what are the biggest bottlenecks in semiconductor design today that AI has the potential to alleviate or even eliminate?*

LS: Design centers and fabs generate a large amount of data daily. This consists of information about products under development, manufacturing data, legacy technologies, and even deprecated products. In the AI-powered EDA era, there should be more attention paid to these design and manufacturing processes, as well as how to collect and reuse these types of data for future projects. AI models can be trained and used not only to automate and optimize designs, but also to support decisions, and help in the creation of new product roadmaps. Bottlenecks such as productivity constraints, long design-cycles, and lengthy iterations in design optimization can be reduced by these tools, which collect experience and outputs from previous flows and design choices.

SIS: *How might AI-driven design tools change the skill sets and day-to-day responsibilities of engineers across the semiconductor supply chain?*

LS: The ability to use automation software and AI tools will be essential for engineers across the semiconductor supply chain, as it is already very relevant today in software development, among other fields. For quick development and the exploration of ideas, products, and potential designs, engineers should be empowered to express the intent of their design flows with AI copilots. Engineers will need to master reward shaping for AI surrogates and optimizers so that models can gain a deeper understanding of the design intent and high-level functionalities.

Fine-grained knowledge of code will still be relevant, but mostly in a smaller percentage than it currently is. We will also see the demand for engineers who have a high level of understanding of AI flows and constraints continue to grow.

SIS: *EDA has long been central to chip design — what's fundamentally different now that AI is being integrated into these tools?*

LS: While traditional EDA tools have been used to speed up and automate traditional, manual design flows and relieve the engineers from computationally heavy tasks, AI-powered EDA aims to expand its horizon in areas such as coding,

review, and architectural design-space exploration, which have previously been constrained to experts in the field. Today, AI-tools can support engineers by augmenting and accelerating creative and explorative tasks, and have had a positive impact on many roles inside design R&D centers.

Research Impact: GENIE-ASI and Schemato

SIS: *Your recent work on GENIE-ASI introduces a training-free, LLM-based method for analog subcircuit identification. What inspired you to explore this "training-free" direction, and what does it enable that previous methods couldn't?*

LS: We wanted a solution that copied how often engineers work: first by explaining the reasoning, and then turning that reasoning into a tool. GENIE-ASI leverages one- and few-shot capabilities of LLMs to produce human-readable instruction steps followed by executable Python code from just a handful of examples, sometimes even a single example. This avoids the heavy cost of large, labeled datasets and brittle, hand-crafted rules. Practically, it enables rapid adaptation to new or uncommon subcircuit variants, allows teams to quickly bootstrap detection logic, and yields reusable code that can be applied at scale without repeated LLM inference.

SIS: *How does GENIE-ASI's ability to generate executable Python code from a few examples change the workflow for analog designers?*

LS: GENIE-ASI moves subcircuit identification from a largely manual or offline ML task into a lightweight coding loop that the designer can run and inspect immediately. Designers get a plain-language detection procedure, along with Python that runs against large netlist collections. This allows for faster iteration, reproducible tooling, and the ability to treat the generated detectors as first-class automation assets rather than opaque model outputs.

SIS: *You also developed Schemato, which translates netlists into human-readable schematics. Why is interpretability such a crucial challenge in ML-generated circuit design, and how does Schemato address it?*

LS: Interpretability is crucial because designers often evaluate and trust circuits visually. A netlist is exhaustive, but not human-friendly. If an ML system produces a design that an engineer cannot readily inspect in schematic form, adoption could stall. Schemato tackles this by translating netlists into LTSpice .asc schematics with attention to connectivity and layout fidelity. By fine-tuning a domain model and using prompt and in-context examples, Schemato produces schematics that engineers can load into LTSpice for immediate verification. This helps restore the human-in-the-loop: experts can see topology, run simulations, and judge intent quickly.

SIS: *In your experiments, Schemato achieved higher compilation success and structural similarity than other LLMs. What does this suggest about the future role of foundation models in bridging the gap between machine-generated and human-interpretable designs?*

LS: The metric gains show that foundation models can do more than generate text that looks plausible. They can produce syntactically correct, structurally faithful artifacts that plug directly into engineering tools. This suggests that foundation models can act as translators and codifiers in the design flow, bridging machine-generated ideas and human-interpretable artifacts, reducing manual conversion steps, and increasing trust. Remaining gaps, such as larger or very rare components, indicate the following steps thereafter, including broader datasets, decomposition strategies, and hybrid pipelines that combine LLM reasoning with deterministic post-processing. In short, foundation models will be collaborators that produce verifiable, reusable outputs rather than black-box recommendations.

Innovation and efficiency

SIS: *Can AI-assisted analog and mixed-signal design bring about measurable gains in performance, power efficiency, or time-to-market for semiconductor products?*

LS: Yes, AI-assisted analog and mixed-signal design can produce measurable gains in performance, power efficiency, and time-to-market. Surrogate models and physics-inspired neural networks can accelerate the exploration of large parameter spaces, enabling designers to find better trade-offs, more quickly.

Generative and optimization tools can reduce iterations in layout and sizing, cutting development time while improving metrics like noise, linearity, and power.

SIS: *How close are we to seeing AI-based EDA methods like GENIE-ASI or Schemato integrated into commercial design toolchains?*

LS: Today, we are closer than many expect. Early deployments already show that AI tools can plug into existing flows when they produce verifiable artifacts that engineers can inspect, edit, and reuse. Methods, such as GENIE-ASI and Schemato, point to how this integration will happen – by generating human-readable logic, executable code, and tool-compatible schematics rather than opaque outputs.

Several vendors are introducing similar capabilities for estimation, topology detection, and layout assistance. Full integration into commercial suites will still arrive in stages, but the trajectory is clear. Assisted features are landing now, and domain-specific automation that can be validated, versioned, and audited is following quickly.

We wanted a solution that copied how often engineers work: first by explaining the reasoning, and then turning that reasoning into a tool. GENIE-ASI leverages one- and few-shot capabilities of LLMs to produce human-readable instruction steps followed by executable Python code from just a handful of examples, sometimes even a single example

SIS: *Do you see AI as primarily augmenting human engineers, or could it eventually automate significant portions of circuit design on its own?*

LS: Over the next few years, AI will primarily augment engineers, amplifying creativity and throughput. Over time, for well-bounded tasks with abundant data and clear objectives, AI could automate significant portions of design. However, full end-to-end automation across all analog and mixed-signal tasks remains unlikely without strong verification and interpretability advancements.

SIS: *How does your team evaluate the trade-off between automation and human oversight in the design process — particularly when reliability and verification are so critical?*

LS: At Sony AI, we treat automation as a force multiplier, not a replacement for human oversight. We have defined safe automation envelopes, which allow us to determine which steps can be trusted to run autonomously, which require human review, and which must remain manual. Reliability is enforced by conservative validation, cross-checking with physics-based models, and mandatory human sign-off for release-critical decisions.

Cross-disciplinary and industry implications

SIS: *Your work mentions "multi-physics device technologies." Could you elaborate on how AI models help optimize across electrical, thermal, and mechanical domains simultaneously?*

LS: AI models accelerate multi-physics co-optimization by providing fast surrogates that link electrical, thermal, and mechanical responses. This makes it feasible to search for joint design spaces where, for example, thermal gradients affect electrical behavior. The key is embedding physics constraints so the model respects conservation laws and known couplings while remaining fast enough for optimization loops.

SIS: *Beyond analog design, what other domains of chip design (e.g., digital layout, verification, photonics) stand to benefit most from AI-powered EDA?*

LS: Many domains stand to benefit from AI-powered EDA, as many applications are expanding as quickly as the computing technology is. Photonics and heterogeneous integration are two that stand out because there are many possible application fields, such as the time-consuming and computationally expensive EM / optical simulations, or complex multi-physics coupling (optical, thermal, electrical). Other top-of-mind areas are 3D stacking, chiplet partitioning, and thermal management

SIS: *How might AI-enhanced design tools impact collaboration between design houses, foundries, and system integrators across the semiconductor ecosystem?*

LS: AI-enhanced tools can standardize and speed handoffs across design houses, foundries, and system integrators by codifying best practices into reproducible flows. They can enable higher-fidelity virtual prototypes that reduce back-and-forth. That said, IP protection, data-sharing agreements, and validation standards will determine how close these parties can collaborate.

SIS: *What kind of data infrastructure or standardization do you think is needed to make AI-powered EDA scalable across the industry?*

LS: Scalable AI-powered EDA needs curated, interoperable datasets, standardized metadata, and agreed-upon interfaces for models and flows. Versioned model registries, common exchange formats for design intents and measurement data, and privacy-preserving federated learning constructs will be important. Equally important are benchmarks and shared verification suites to measure gains reliably.

Ethics, trust, and the human element

SIS: *As AI takes on a larger role in chip design, how do we ensure transparency and trust in AI-generated design decisions?*

Transparency starts with explainable models, traceable decision logs, and interfaces that can articulate why a recommendation was made. Combining data-driven suggestions with physics-based checks makes outputs easier to trust. Documentation, reproducible training data lineage, and the ability to reproduce or audit a design step are critical.

SIS: *What challenges do you foresee in validating or certifying AI-generated designs, particularly for safety-critical applications like automotive or aerospace?*

LS: Certification for AI-generated designs will be challenging because regulators and customers demand deterministic guarantees. There will need to be hybrid validation strategies, which include formal verification where possible, exhaustive simulation of critical corners, and independent audits of model training and test sets. For safety-critical systems, AI-generated designs will likely require conservative constraints and pedigree – like what is used today – for tool qualification.

SIS: *How do you balance the excitement of rapid AI innovation with the practical realities of tool qualification and adoption in semiconductor workflows?*

LS: When balancing the excitement of rapid AI innovation with the practical realities, you have to be very disciplined. Running rigorous experiments, quantifying gains, and exposing failure modes early is critical. Short-term pilots should focus on high-ROI problems where validation is tractable. At the same time engineers should invest in tooling for traceability, test suites, and risk assessment so adoption does not outpace qualification.

Looking ahead

SIS: *What's next for your research — are there areas where you see AI pushing the boundaries of what's possible in semiconductor design in the next five years?*

LS: While I am not able to share any specific details at this time, we will have some work focused on integrated, multi-objective systems that link physics, circuit implementation, and system-level metrics in a single optimization loop. Advances in physics-inspired models, generative physical layout, and faster verification flows will push boundaries. Over the next five years, we expect AI to enable faster exploration of novel technologies and to unlock design points that were previously infeasible because of complexity or simulation time.

semi

MEMS & SENSORS® EXECUTIVE CONGRESS

MARCH 31–APRIL 2, 2026 | HYATT REGENCY | CAMBRIDGE, MA

REGISTER NOW

SENSORIZING THE FUTURE: MEMS AND SENSORS AT THE EDGE OF PERCEPTION

Get a deep dive from industry leaders on topics including—

- Bio-Medical/MEMS Healthcare
- Investment Trends
- Disruptive Technologies: AI, Robotics, Advanced Sensor Technologies
- Market Dynamics
- MEMS & Sensors Expansion
- Positioning, Navigation, Timing
- Roadmaps 2030 and Beyond
- Sensor Manufacturing
- Sensor Startups
- Supply Chain & Geopolitics
- Strategic Outlooks
- and More

www.semi.org/msec

SEMIEXPO HEARTLAND

APRIL 29–30, 2026 | DETROIT, MICHIGAN

SMART MANUFACTURING

SMART MOBILITY

semi

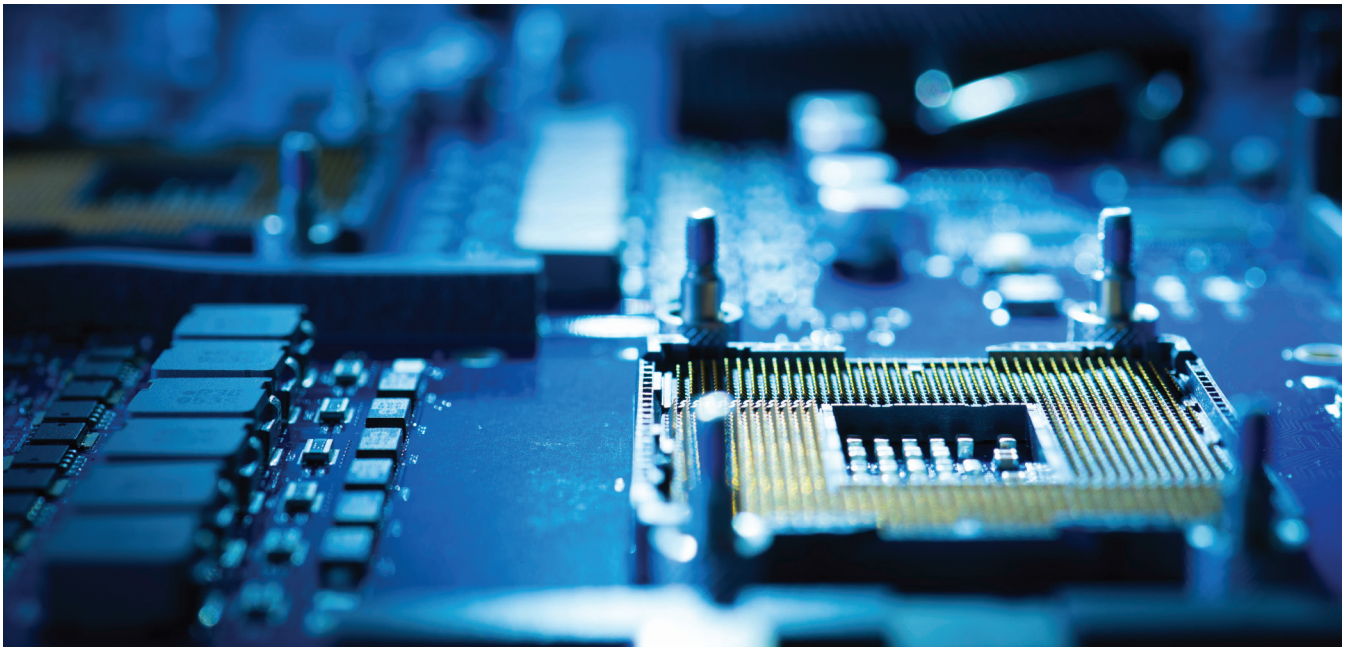
REGISTER NOW

EXHIBIT AND SPONSORSHIP OPPORTUNITIES

Boost your visibility at SEMIEXPO Heartland with customizable sponsorship options designed to fit your branding, marketing goals, and budget.

semiexpo.semi.org

Plan to Exhibit or Sponsor: Shane Poblete | +1 202-847-5983 | spoblete@semi.org



Scaling 3D chips with molybdenum-based metallisation

Kaihan Ashtiani, Corporate Vice President and is General Manager of ALD/CVD Metals Product Group at Lam Research, discusses the reasons behind the chip industry's new focus on Molybdenum, explains why this metal is critical to the future of computing, the three main challenges when it comes to current Atomic Deposition Layer (ALD) methods and how the company has stepped in to develop the ALTUS Halo molybdenum deposition tool, which overcomes these obstacles and helps to underpin the metal's benefits in the era of smaller, faster and more sophisticated 3D chips.

Advancing semiconductor materials and processes for the AI era

THE DIGITAL WORLD is transforming at an unprecedented pace, with artificial intelligence (AI) leading a wave of data-intensive applications that demand increasingly powerful computing platforms. At the heart of this transformation lies the semiconductor industry, which is undergoing its own revolution to meet the growing computational and memory requirements of modern digital technologies. AI and other data-centric applications are creating pressures on semiconductors to be smaller, faster, and more sophisticated, requiring advances not only in chip design but also in materials science and process technologies.

The evolution of semiconductor technology is a one-way journey, driven by the pervasive role that computers, smartphones, and other digital devices now play in everyday life. The performance requirements of these devices are accelerating rapidly, creating a continuous demand for innovations that push the limits of current semiconductor capabilities. The industry's response to these demands is multifaceted, spanning improvements in computational capacity, memory performance, and interconnect efficiency, all of which are essential for realizing the next generation of digital devices. As a result, semiconductor companies are investing heavily in both materials innovation and high-precision manufacturing equipment, enabling the production of chips that operate faster, more efficiently, and at greater scale than ever before.

One area where these technological pressures are particularly visible is in the realm of metalization, a critical process in chip fabrication. Traditional metals such as copper and tungsten have long been the materials of choice for interconnects, the pathways that carry electrical signals across semiconductor devices. However, the shift toward 2.5D and 3D chip architectures, with multiple layers and increasingly complex electrical connectivity, is exposing the limitations of these conventional materials. The industry now faces a critical inflection point where new metals with superior properties must be employed to maintain performance as device dimensions continue to shrink.

The challenge arises from a phenomenon known as thin-film resistivity. While the bulk resistivity of metals like copper and tungsten is well understood, their behaviour in extremely thin films - on the order of nanometers - introduces additional complexity. As the thickness of an interconnect approaches or falls below

the mean free path of electrons within the material, the resistivity increases due to electron scattering. This effect becomes particularly significant at the transistor level and in the first few layers of interconnects, where high-speed signal transfer is essential. The combination of bulk resistivity and mean free path forms a figure of merit that dictates the suitability of a given metal for these ultra-thin applications. When copper and tungsten reach the limits of their performance under these conditions, the search for alternative metals becomes necessary.

Molybdenum has emerged as a promising candidate for these high-performance interconnects. Among the many elements in the periodic table, molybdenum offers a combination of electrical conductivity, thermal stability, and process compatibility that makes it ideal for replacing tungsten in critical areas of advanced semiconductor devices. The transition to molybdenum is not a wholesale replacement; it is targeted to specific layers where thin-film resistivity poses a limitation. By integrating molybdenum interconnects at these critical points, chip manufacturers can maintain high signal integrity and improve overall device performance, particularly in memory and logic applications where scaling continues unabated.

Achieving this transition, however, requires more than just identifying the right material. The deposition of molybdenum must be executed with extraordinary precision, which is where atomic layer deposition (ALD) technology becomes essential. ALD enables the controlled deposition of materials one atomic layer at a time, and in some cases even half a layer, ensuring that the properties of the deposited metal meet the stringent requirements for modern semiconductor devices. As chip dimensions shrink to scales thousands of times smaller than a human hair, precision deposition becomes critical not only for performance but also for yield and uniformity across large wafer surfaces.

Lam Research's recent introduction of the ALTUS Halo ALD tool exemplifies the level of innovation required to meet these challenges. Building on two decades of experience in ALD, including pioneering the first high-volume manufacturing of tungsten ALD, Lam has developed a tool capable of handling the unique challenges presented by molybdenum. Unlike tungsten, which can be delivered as a liquid precursor with high vapor pressure, molybdenum is deposited from a solid precursor. This necessitates careful sublimation, gas transport, and precise thermal management to deliver the material uniformly to the wafer. The ALTUS Halo system integrates proprietary hardware and process sequences to ensure that each atomic layer of molybdenum maintains the desired electrical properties, enabling faster, more efficient chip performance.

Developing the ALTUS Halo was not simply a matter of adapting existing techniques. The project involved extensive collaboration with chemical vendors to create a suitable molybdenum precursor and delivery system. Lam's expertise in ALD processes, built over decades, was applied to design a system capable of delivering solid precursors reliably in a high-volume manufacturing environment. This required sophisticated engineering to control temperature, gas flow, and deposition sequences, ensuring that every wafer processed meets the stringent electrical and structural requirements of advanced semiconductor devices. The integration of hardware precision and process expertise allowed Lam to overcome the unique challenges posed by molybdenum and introduce a tool that has been well received across the semiconductor industry.

The successful deployment of the ALTUS Halo highlights the importance of collaboration across the semiconductor supply chain. High-volume manufacturing of advanced devices relies on a close partnership between equipment suppliers, chemical vendors, and chip manufacturers. Each stakeholder contributes critical expertise, from precursor chemistry to process integration and device validation. For memory applications, including DRAM and NAND flash, as well as logic and foundry processes, the precise integration of molybdenum interconnects requires iterative evaluation of electrical performance and process compatibility. Only through this comprehensive collaboration can a new material and deposition tool be qualified for high-volume semiconductor production, where reliability and reproducibility are paramount.

The introduction of molybdenum via ALD is not the endpoint but rather a foundation for continuous improvement. The pace of innovation in semiconductors is relentless, driven by the need to support increasingly powerful AI applications and the broader digital ecosystem. Once a material and process are deployed in manufacturing, the work does not stop. Continuous improvement plans, known in the industry as CIPs, are implemented to optimize tool productivity, enhance material properties, and anticipate the requirements of next-generation devices. Even as molybdenum ALD becomes a long-lasting technology, ongoing refinements are necessary to address increasingly stringent performance and cost requirements. This iterative development ensures that the technology remains viable and competitive for the next five to ten years and beyond.

The role of materials innovation extends beyond electrical performance. Selecting the appropriate material involves considering factors such as thermal conductivity, mechanical stability, and compatibility with other process steps. In the case of molybdenum, its unique combination

of properties makes it suitable for integration into multilayer interconnect structures, facilitating the continued miniaturization of semiconductor devices. The ability to deposit this material with atomic precision is critical to leveraging its advantages fully, and it underscores the broader importance of materials research in driving the semiconductor industry forward.

From a broader perspective, the adoption of molybdenum ALD reflects a paradigm shift in semiconductor manufacturing. As device dimensions shrink and computational demands grow, traditional materials and processes can no longer meet the performance targets required for modern applications. The transition to new metals, coupled with high-precision deposition techniques, represents a fundamental advancement in the industry's capability to deliver faster, more efficient, and more reliable semiconductor devices. This innovation is particularly critical for AI workloads, which require massive computational throughput, low latency, and high memory bandwidth, all of which depend on optimized interconnect performance.

The impact of these advancements extends across the digital ecosystem. Faster interconnects enable higher data transfer rates within chips, improving the performance of everything from consumer electronics to large-scale server farms that power cloud computing and AI inference. Memory chips benefit from reduced resistivity and improved signal integrity, enabling higher-density storage and faster access times. Logic devices gain enhanced performance through lower latency interconnects, supporting more complex computation and accelerating AI model training and deployment. Collectively, these improvements contribute to a broader trend of digital acceleration, where semiconductors continue to drive innovation in virtually every sector of technology.

Lam Research's ALTUS Halo ALD tool exemplifies the synthesis of materials science, process engineering, and supply chain collaboration. By overcoming the challenges of depositing molybdenum with atomic precision, the tool demonstrates how equipment innovation can unlock new material capabilities, directly impacting the performance of semiconductor devices. This achievement underscores the broader principle that semiconductor advancement is not solely about device design but also about enabling technologies that make new materials practical and reliable at scale.

Looking ahead, the development of tools like the ALTUS Halo points to a future in which semiconductor innovation continues to accelerate. While molybdenum ALD represents a significant milestone, ongoing research and development will be required to address the next generation of device architectures, further miniaturization, and emerging applications in AI, high-speed networking, and beyond. Continuous improvement initiatives ensure that even established technologies evolve to meet higher performance standards, greater throughput demands, and tighter cost constraints. In this way, the semiconductor industry remains in a constant state of technological evolution, responding to the ever-expanding demands of the digital world.

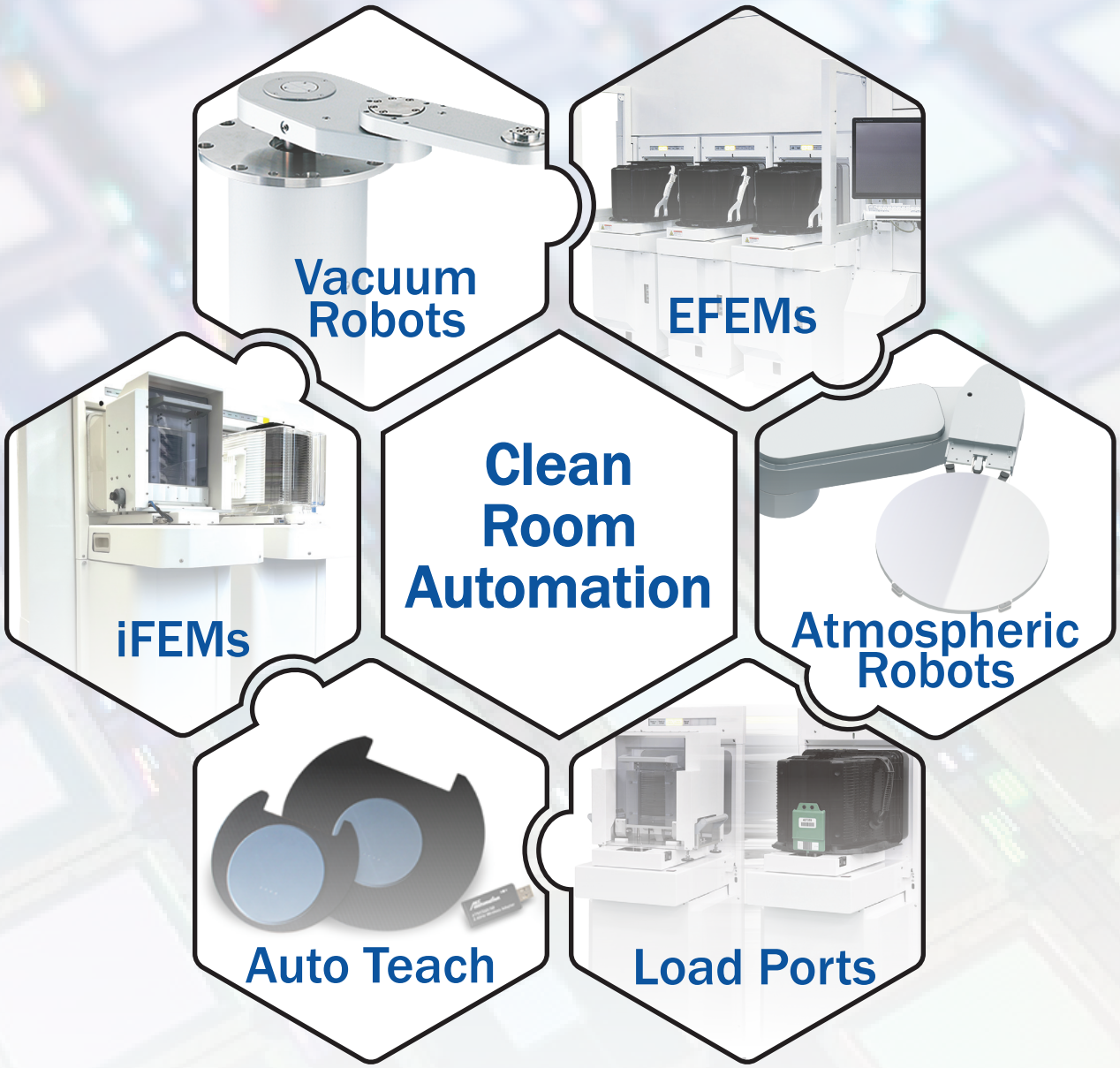
The journey from material discovery to high-volume manufacturing is complex, involving multiple layers of collaboration, innovation, and engineering. Identifying an element with desirable electrical properties is only the first step; translating that discovery into a scalable, reliable process requires sophisticated equipment, precise control, and rigorous validation. Lam's experience with ALD over the past two decades highlights how expertise in both hardware and process development is essential for introducing new materials into semiconductor production. The integration of molybdenum into advanced interconnect structures demonstrates the practical application of these principles, providing a blueprint for future innovations in semiconductor materials and processes.

In conclusion, the semiconductor industry is at a pivotal moment, driven by the dual forces of increasing computational demand and device miniaturization. AI and other digital applications are accelerating the need for advanced materials and precise manufacturing techniques, challenging the industry to innovate at every level. The adoption of molybdenum interconnects via atomic layer deposition exemplifies how materials science, process engineering, and collaborative development converge to meet these challenges. Tools like the ALTUS Halo not only enable the production of faster and more efficient semiconductor devices but also provide a platform for continuous improvement and future innovation. As the digital world continues to evolve, the ability to translate fundamental materials discoveries into practical, scalable manufacturing solutions will remain a defining feature of semiconductor technology, ensuring that the industry can support the next generation of computational demands and maintain its central role in driving technological progress. The relentless pace of innovation ensures that semiconductor companies, researchers, and engineers remain at the forefront of technological advancement, constantly pushing the boundaries of what is possible.

From a broader perspective, the adoption of molybdenum ALD reflects a paradigm shift in semiconductor manufacturing. As device dimensions shrink and computational demands grow, traditional materials and processes can no longer meet the performance targets required for modern applications. The transition to new metals, coupled with high-precision deposition techniques, represents a fundamental advancement in the industry's capability to deliver faster, more efficient, and more reliable semiconductor devices.

AES motomation

Providing innovative and competitive solutions worldwide. From individual modules to entire platforms, for semiconductor and flat panel display industry as well as laboratory automation.



Visit us at Semicon Europa and Semicon West or
www.motomation.com

With our partners at :

JEL JEL CORPORATION SINFONIA Nidec

No longer optional: precision sensing for yield improvement in advanced semiconductor manufacturing

How Kistler empowers Semiconductor Equipment Manufacturer for the next era of 3D heterogeneous chip integration.

BY ROBERT HILLINGER, KISTLER INDUSTRY LEAD SEMICONDUCTOR

THE SEMICONDUCTOR industry has entered a phase in which every micron counts, each defect costs thousands of dollars, and process stability is non-negotiable. From grinding, CMP, thermocompression bonding to advanced testing, machine builders can no longer treat advanced sensing technology as an add-on. Traditionally, MEMS or strain gauge (DMS) sensors were used, but their resolution and stability are no longer sufficient at today's scale. Integrating high-precision piezoelectric sensor systems, such as those from Kistler, as early as possible in the R&D phase of semiconductor equipment design has become indispensable for meeting the rising demand for yield, quality, and efficiency throughout the machine's lifecycle.

Heterogeneous 3D integration is redefining semiconductor manufacturing by stacking and interconnecting logic, memory, RF, and chiplets into compact, high-performance systems. This technology enables breakthroughs in AI, high-performance computing (HPC), and 5G/6G. However, the complexity of wafer bonding, die stacking, and through-silicon via (TSV) processes poses significant risks. As devices shrink and incorporate fragile new materials, tolerances for force, pressure, vibration, and temperature become critically tight. Yield

➤ Ultra-compact piezoelectric force sensors, such as the Type 9172CD from Kistler, measure micro-forces ranging from sub-newton to kilonewton, providing high-resolution, real-time data directly from critical process points. This helps manufacturers prevent failures such as die shift, and pressure-induced microcracks.

risks emerge in every step, from alignment in wafer-to-wafer bonding, to void formation in TSV filling, die shift during pick-and-place, and pressure-induced cracks in encapsulation. At the same time, the economic impact of defects increases quickly. Each of the failure modes named above can multiply costs, each worth several thousand dollars apiece.

The conclusion is inevitable for both equipment manufacturers and semiconductor fabs: only machines with built-in, high-precision monitoring and control can ensure process stability, safeguard yield, and protect the massive value tied to every wafer.

Why semiconductor equipment manufacturer carry the burden of precision

They are at the heart of this transformation, setting industry standards for precision, reliability, and throughput. In the past, success was defined by cycle speed and mechanical accuracy. Today, Semiconductor Manufacturer demand far more, including embedded sensors, closed-loop process control, and traceable quality data that enables predictive maintenance. As a result, machines are evolving from precise mechanical tools into intelligent systems with built-in monitoring and adaptive control.

Failure modes: where yield is put at risk

3D integration introduces many different complex and costly failure modes. Methods, such as inline optical inspection, can detect defects, for example, cracks, and misalignment. More damaging risks occur during production and remain invisible to these techniques. Thermal-mechanical stress from coefficient of thermal expansion (CTE) mismatches can cause warpage or micro-cracks. TSV processes are prone to incomplete filling and void formation, which compromise electrical integrity. As well a shift or tilt of a few microns during pick-and-place can disrupt chip alignment and prevent accurate contact matching between interconnect structures, while incorrect pressure during encapsulation can damage fragile dies.

Advanced sensor technologies: the backbone of smart, high-yield 3D integration

High-resolution piezoelectric force sensors integrated directly into bonding heads provide continuous monitoring to help mitigate these risks. Kistler's sensor portfolio allows Semiconductor Equipment Manufacturer to implement closed-loop control and ensure consistent process transparency. It also provides high resolution with reliable signal integrity data for process optimization and traceability. At the same time, the sensors remain stable and reliable even in high-temperature bonding and encapsulation, and are also suitable for cleanroom and vacuum applications.

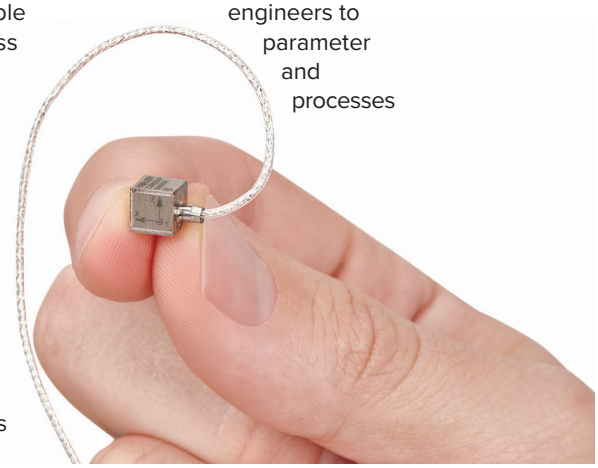
Compact, high-sensitivity force sensors cover ranges from nanonewton to kilonewton, supporting applications from precise grinding, CMP, bonding to chiplet placement and packaging. By detecting micro-forces in real time, these sensors enable precise process control at bonding points, minimize the risk of die damage, and maintain stability even at high throughput. As placement heads accelerate and decelerate, Acceleration sensors track micro-vibrations and shocks that can shift dies by mere microns. When the process continues into encapsulation, underfill, or TSV filling, next-generation pressure sensors provide real-time cavity monitoring to detect voids, maintain uniform fill, and secure stable process conditions.

To tie these signals together, the industrial charge amplifier delivers force monitoring with real-time signals for the Semiconductor Equipment control system. Designed for multipurpose use with piezoelectric sensors, the Amplifier converts charge signals from sensors into voltage and/or digital outputs. This closed-loop control system ensures precise bonding alignment and prevents defects caused by overpressure. Additionally, handheld diagnostic tools with integrated charge amplifiers enable engineers to validate process parameter verification and quality control processes anywhere.

> High-resolution sensors will become even more central to securing long-term competitiveness

Sensor placement: there is no one-size-fits-all solution

Designing equipment for heterogeneous 3D integration means more than simply selecting the appropriate sensing technology. It also requires placing sensors exactly where they deliver maximum insight. The ideal measurement location may not offer the environmental conditions needed for long sensor life. For example, while piezoelectric sensors can tolerate high temperatures, they still have operational limits. In certain applications, it may be necessary to use a more heat-resistant sensor or adjust the placement to ensure equipment protection and reliability.



➤ The new Miniature Triaxial Acceleration sensor Z22198 from Kistler is designed for high-precision vibration analysis, including micro-vibrations and shocks. The lightweight miniature Sensor is ideal for dynamics testing and monitoring, especially in tight spaces.

Kistler works closely with Semiconductor Equipment Manufacturer to identify the most sensitive points within their systems, ensuring that force, pressure, and vibration sensors are embedded where they capture the most informative data. Further services such as calibration, and system validation during equipment build, ensure long-term accuracy and reliability.

Taking bold action: securing yield and strategic advantage in 3D integration

Delaying investments in advanced sensor systems and smart manufacturing technologies presents risks for Semiconductor Equipment Manufacturer. As product requirements evolve – such as miniaturization or the use of new materials – process stability can be compromised. Retrofitting sensors into completed machines is often technically challenging. Space constraints and even minor modifications can disrupt process balance or amplify existing issues. Even, when possible, retrofits rarely match the performance of solutions integrated during the design phase. Looking ahead, more sophisticated – and expensive – wafer materials, like Gallium Nitride and Siliciumcarbid, and the further advancement of manufacturing processes will only increase the need for better monitoring strategies. High-resolution sensors will become even more central to securing long-term competitiveness.

How silicon became the hidden backbone of AI

AI's next phase will be shaped as much by power delivery and materials as by model capability. The core question isn't just how fast models can advance, but whether the infrastructure beneath them can keep pace.

BY RENÉ JONKER, CHIEF PRODUCT OFFICER, SOITEC FOR SILICON SEMICONDUCTOR

AI IS BECOMING a power and electricity problem. The industry has been dealing with the power side of scaling for years, but demand is now outpacing the assumptions that data center infrastructure was built on.

While headlines focus on capacity growth, frontier models, and agentic AI, the more pressing issue lies lower in the stack at the silicon and materials layer. Increasingly, engineered substrates are emerging as the hidden backbone, shaping whether AI can continue scaling quickly without making energy use and reliability unsustainable.

Data centers are turning to silicon carbide for efficiency

According to the International Energy Agency, in 2024 data centers consumed 415 tera-watt hours (TWh), representing about 1.5% of the global electricity generation. In 2025 this figure approached 500 TWh, and it is projected to more than double by 2030 as AI workloads expand.

At scale, the challenge shifts from compute availability to power efficiency: how effectively electricity moves from the grid down to servers, accelerators, and out through cooling systems. Silicon carbide (SiC) power devices are becoming more common because they offer the best power efficiency for the new 800V data center power distribution topologies, dissipate better energy losses, and present a proven high reliability, which is crucial for facilities that run continuously.

Engineered substrates can further improve SiC devices' performance. SmartSiC™, Soitec's SiC engineered substrates, are composed of a thin, high-quality SiC single-crystal layer on top of an ultra low-resistivity handle wafer. These substrates have demonstrated to improve device robustness and reliability while lowering conduction and switching losses. For AI data centers, these substrate-level gains translate into reduced heating across the power conversion stages, an increasingly critical factor as power density rises and data centers scale up.

How AI is shifting infrastructure priorities

AI models are advancing quickly, creating a greater spotlight on the infrastructure required to grow efficiently. Under sustained & high-intensity workloads, power delivery, thermal management and reliability of the complete system are fundamental for a cost effective service.

That reality reinforces the role of engineered substrates. They directly affect power efficiency, heat management, and behavior under sustained load. GPUs remain central, but they cannot solve system-level efficiency constraints alone. As power and energy constraints tighten, engineered substrate choices become one of the most effective levers for scaling AI infrastructure without breaking down.

Why AI power is driving deeper US-Europe collaboration

AI infrastructure spans materials, devices, manufacturing and deployment, and today, no single region dominates all four of these areas. As AI energy demands rise at unprecedented speeds, this raises the stakes for global supply chain reliability, scale and resilience, welcoming cross-regional collaboration.

Europe has a clear leadership role in advanced semiconductor materials with deep expertise in engineered substrates and power materials. The United States, by contrast, remains competitive in device design, manufacturing scale and AI deployment. Together, these two regions cover far more of what AI power systems actually require.

In the past year, European materials suppliers and United States device manufacturers partnered to validate how materials improvements translate into device-level efficiency gains. Work like this strengthens the foundation for AI power infrastructure, and we'll continue to see regions partner together to close gaps across the semiconductor supply chain as AI scales.

What comes next for AI infrastructure

AI's next phase will be shaped as much by power delivery and materials as by model capability. The core question isn't just how fast models can advance, but whether the infrastructure beneath them can keep pace. Increasingly, the answer will be shaped by silicon, materials, and the global collaborations needed to build AI power systems that can scale, reliably, and sustainably.

ANGELTECH

CS INTERNATIONAL CONFERENCE | PIC INTERNATIONAL CONFERENCE | PE INTERNATIONAL CONFERENCE | AP INTERNATIONAL CONFERENCE | AIS ANGELTECH INNOVATE SUMMIT

SAVE THE DATE

12-14 APRIL 2027

Sheraton Brussels Airport Hotel

To find out more about our sponsor and speaker opportunities, contact us today on:
+44 (0) 2476 718970

or email:

info@angel-tech.net

AP INTERNATIONAL CONFERENCE

ANGELTECH

20-22 April 2026

Sheraton Brussels Airport Hotel, Brussels, Belgium

CONNECTING THE ADVANCED PACKAGING INDUSTRY

The 1st Advanced Packaging International builds on the momentum driving the next era of semiconductor innovation. Over three days, industry leaders and academic experts will deliver around 40 presentations across four key themes:

- Heterogeneous Integration
- Getting the Best Out of Incumbent Solutions
- Advancing Thermal Management
- Optimising Packaging Architecture
- Manufacturing & Pilot Lines
- Design, Simulation and Reliability

Conference attendees will gain insights into the materials, methods, and technologies reshaping chip-level packaging and system integration.

From cutting-edge thermal solutions to the reimagination of wirebond and leadframe formats, the event provides a comprehensive look at how packaging is enabling system-level innovation.

The three-day conference also includes expert panels and a dedicated poster sessions, creating multiple avenues for peer-to-peer engagement and technical exchange across the packaging ecosystem - from researchers and R&D teams to product engineers and system architects.

Advanced Packaging International is part of AngelTech, which delivers a portfolio of insightful, informative, and highly valued chip-level conferences.

Bringing together an Innovation Summit and four co-located conferences with more than 120 presentations, 700+ delegates, and over 80 exhibitors, AngelTech is the premier global event covering compound semiconductor, photonic integrated circuit, power electronic, and advanced packaging technologies.

With significant overlap between the conferences, attendees benefit from exposure to full supply chains, customer bases, and partner ecosystems.

Event Discount Code: MP10

10% OFF

Register your place and get 10% off using promo code: MP10

Registration to AngelTech allows you to access both days of **Advanced Packaging International, CS International, PIC International** and **PE International.**

To find out more about our sponsor and speaker opportunities, contact us today on:
+44 (0)2476 718970 or email: info@angel-tech.net https://ap-international.net

CO-LOCATED WITH:

CS INTERNATIONAL CONFERENCE
PIC INTERNATIONAL CONFERENCE
PE INTERNATIONAL CONFERENCE

ORGANISED BY

Angel BUSINESS COMMUNICATIONS
ANGEL EVENTS

CLEAN AIR

INSPECTION SYSTEMS

COMPONENTS

ETCH

FLUID SYSTEMS

GAS DELIVERY SYSTEMS

GAS PURIFIERS

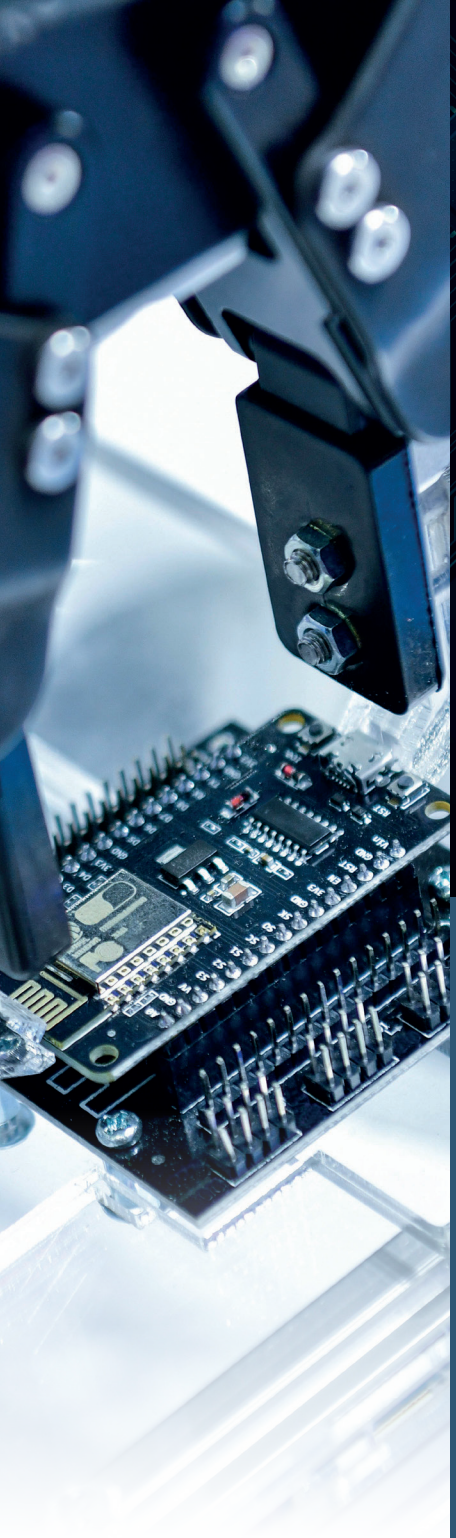
HYDROGEN GENERATORS

GAS ANALYSERS

PLASMA TECHNOLOGY

TEST

VACUUM EQUIPMENT



Upgrade to measure trace oxygen and moisture before contamination spreads

GEN-7 SERIES

The Gen-7 SERVOPRO DF-700 series

delivers ultra-trace oxygen and moisture analysis:

- Easy, reliable digital operation with larger screen and buttons
- Measure moisture down to 55ppt with TDLAS technology
- Future-ready with long-life solid-state drive and improved filter

Earlier insight.
Faster action.
Higher purity.

Ready to upgrade?
Find out more at:
servomex.com/gen7

Analysis that **empowers**

SERVOMEX
a spectris company